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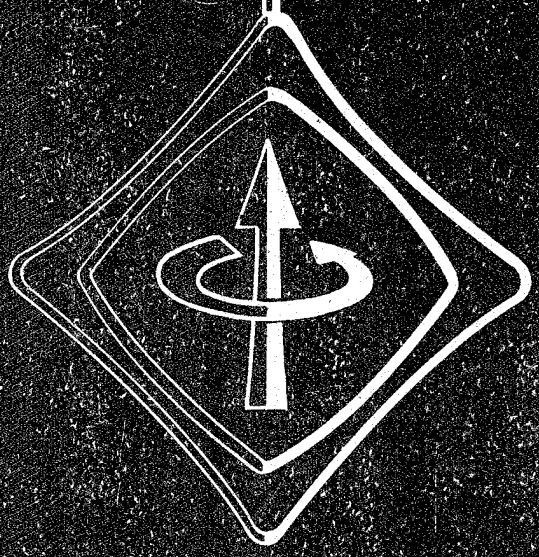

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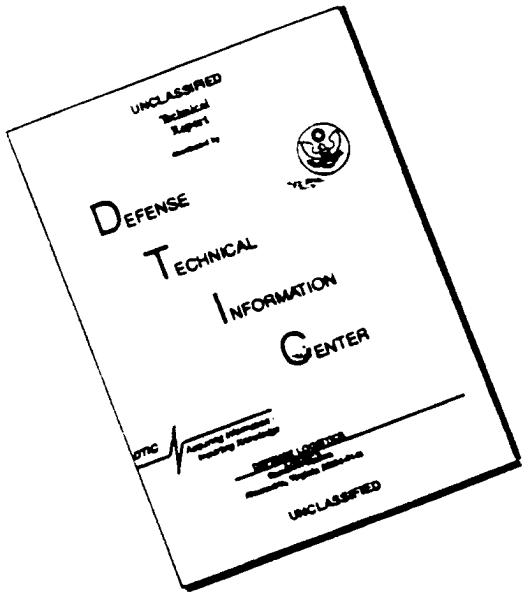

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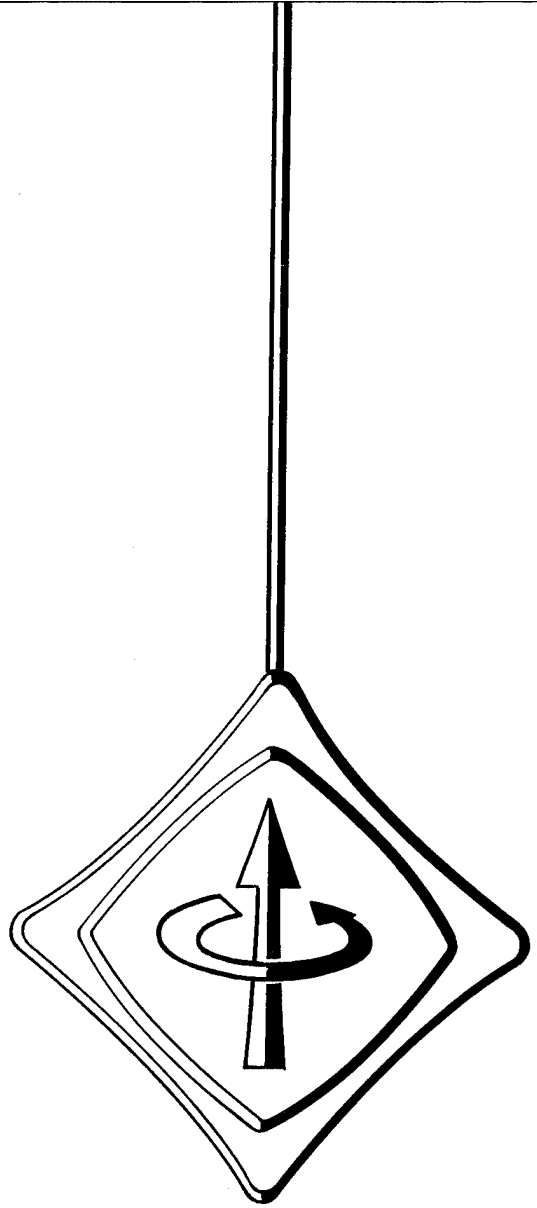

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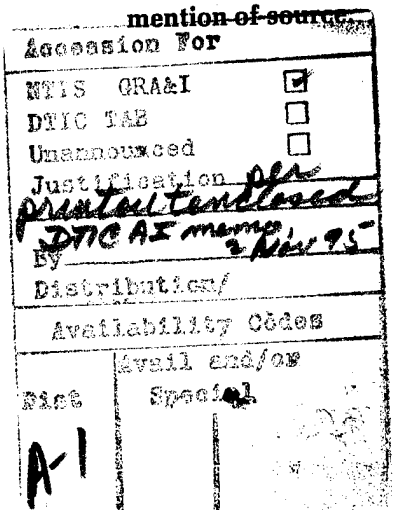

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THE MECHANISMS OF DEGRADATION IN AN OPTICALLY COUPLED ISOLATOR

Edward F. Thomas
NASA-Goddard Space Flight Center
Greenbelt, Maryland 20771

Abstract

Degradation was observed in optically coupled isolators that were operated under both photodiode and phototransistor biasing configurations. The device "on" state current decreased during operation due to degradation of the light emitting diode radiant power output. This decrease in radiant power output was associated with an increase in the nonradiative, space charge recombination current component of the light emitting diode forward current. In addition, large and rapid increases were observed in the optically coupled isolator "off" state currents. This degradation was due to formation of a surface inversion channel in the base region of the photosensitive transistor.

Introduction

Optically coupled isolators contain, within a single package, both a GaAs light emitting diode and a photosensitive silicon semiconductor device. It has been established through various investigations that GaAs light emitting diodes degrade during operation, and that this degradation can be large. One would expect, therefore, that optically coupled isolators that contain GaAs light emitting diodes would also exhibit some type of degradation when operated for extended periods of time. The purpose of this investigation was to define the degradation characteristics of an optically coupled isolator, and to identify the physical mechanisms responsible for this degradation.

Device Description

The optically coupled isolator subjected to testing contained, within a standard TO-5 type package, a zinc diffused, GaAs light emitting diode (LED) and a high gain, silicon, NPN photosensitive transistor, separated by an 8.6×10^{-3} cm thick glass layer (Figure 1). The schematic model of Figure 2 illustrates the interaction of these elements and identifies the various device parameters. Radiant power (P_O) produced by the forward biased LED strikes the photosensitive transistor, enhancing the transistor reverse leakage currents. The enhanced collector-base leakage current is defined as the photocurrent (I_P), while the enhanced collector-emitter leakage current is defined as the collector current (I_C). Collectively, these currents make up the optically coupled isolator "on" state currents (I_{ON}) for photodiode and phototransistor operation respectively. The device "off" state currents are the transistor reverse leakage currents with no excitation applied to the LED.

Test Conditions

Optically coupled isolators were operated for a period of three thousand hours under both photodiode and phototransistor bias configurations, with full rated forward current applied to the light emitting diode. For photodiode operation, a collector-base reverse bias of 10 volts was applied, resulting in an average "on" state current (I_{ON}) of 0.06 mA and an average transistor power dissipation (P_D) of 0.6 mW. Those devices configured for phototransistor operation received a collector-emitter reverse bias of 5.7 volts, resulting in an average I_{ON} of 43 mA and an average transistor P_D of 245 mW.

Experimental Results

Shown in Figure 3 is the degradation that occurred in the optically coupled isolator "on" state currents for both photodiode and phototransistor operation. As might be expected, due to the higher power dissipation under phototransistor biasing, this operating mode resulted in the larger degradation. This is even more evident when the photocurrents for both operating modes are compared as in Figure 4.

During operation, the photocurrent was measured at three levels of light emitting diode forward current, 5 mA, 10 mA and 40 mA. Shown in Figure 5 is the degradation that occurred in the photocurrent measured at each of these current levels for a device operated under phototransistor biasing. Although the shape of each curve is identical, the amount of degradation that was observed was a direct function of the light emitting diode forward measuring current, with the largest degradation occurring at the lowest LED current.

Measurements were also taken of the light emitting diode forward voltage at two levels of forward current, 10 mA and 40 mA. Plotted in Figure 6 is the degradation that occurred, also for a device operated under phototransistor biasing. The degradation of the forward voltage was similar to that of the photocurrent, showing the same variation with LED forward measuring current.

In addition to the degradation of the optically coupled isolator "on" state currents, large and rapid increases were observed in the "off" state currents of additional devices that were operated with maximum power dissipation in the transistor. These devices were operated with a LED forward current of 60 mA and a transistor collector-emitter bias of 5.5 volts, resulting in an average collector current of 52 mA and an average transistor power dissipation of 286 mW. Plotted in Figure

7 is the degradation that occurred in the "off" state current for three devices operated under the above stress conditions. The current increases were large, spanning four to five orders of magnitude.

Degradation Mechanisms

The close similarity between the degradation of the transistor photocurrent and the light emitting diode forward voltage strongly indicates a cause/effect relationship. The degradation of zinc diffused GaAs light emitting diodes supposedly results from an increase in the nonradiative, space charge recombination current component of the total forward current. For constant current excitation, this increase in nonradiative current would cause both the radiant power output and the forward voltage of zinc diffused, GaAs light emitting diodes to be reduced. Since, at the lower forward currents, the percentage of nonradiative current is greater, parameter degradation caused by an increase in this current component would be larger when measured at the lower currents. As shown in Figures 5 and 6, both the degradation of the photocurrent and the LED forward voltage were larger when measured at the lower LED forward currents.

For LED degradation that is due solely to an increase in the nonradiative current component, measurement of the radiant power output under constant voltage would not reveal measurable degradation. Additional optically coupled isolators were operated for one thousand hours at an accelerated stress level, with measurements of the photocurrent taken under both constant current and constant voltage excitation of the LED. For measurement under constant current excitation, a total decrease of 54% was observed in the device photocurrent. No significant degradation was measured in this parameter when measured under an equivalent LED constant voltage. It is, therefore, concluded that the degradation of the optically coupled isolator "on" state current is the result of a decrease in LED radiant power output caused by an increase in the LED nonradiative current component.

The large and rapid increases that occurred in the optically coupled isolator "off" state currents cannot be attributed to degradation of the light emitting diode. Therefore, this degradation must be due to a second degradation mechanism. Similar degradation was observed in identical devices subjected to high temperature reverse bias (HTRB) tests performed at the Martin Company, Denver, Colorado. Mr. E. R. Freeman[1] of that company postulated that the degradation was due to surface inversion channel formation occurring in the base region of the photosensitive transistor. The effect of this surface inversion could be cured by subjecting the devices to a thermal anneal without bias. He further concluded that the source of the surface inversion was most likely positively charged hydrogen ions originating within the silicone material that covers the device structure.

Since the operating life tests performed at the Goddard Space Flight Center resulted in an HTRB type of stress, it was hypothesized that the "off" state current degradation shown in Figure 7 was also the result of surface inversion. One of the three devices shown there was removed from testing after one thousand hours of operation, subjected to a 40-hour thermal anneal at 398 K without bias, and then placed back on operating life for an additional one thousand hour period.

As shown in Figure 8, the degraded "off" state current returned to normal during the thermal anneal, and, after stress was reapplied, once more exhibited the rapid and large increase as before. Based on these results, it is concluded that the "off" state current degradation is due to surface inversion in the transistor base region.

Conclusions

It has been shown that optically coupled isolators operated with rated LED forward current undergo considerable degradation with regard to the device "on" state currents. The cause for this degradation has been identified as being due to degradation of the internal LED. Therefore, in order to reduce this type of degradation, it would be necessary to operate the optically coupled isolator with derated LED forward current. Finally, if operating conditions present a sufficient HTRB stress environment (i.e. high device temperature with several volts reverse bias), a surface inversion channel will form in the transistor base region, causing large and rapid increases in the optically coupled isolator "off" state currents. If, as postulated, the source of the inversion channel is hydrogen ions originating in the silicone overcoat material, then removal of this material from the device design is necessary in order to eliminate this "off" state current degradation.

References

1. E. R. Freeman, "Viking Failure Analysis Report," Martin Marietta Company Failure Analysis Report SPL-505, July 2, 1974.

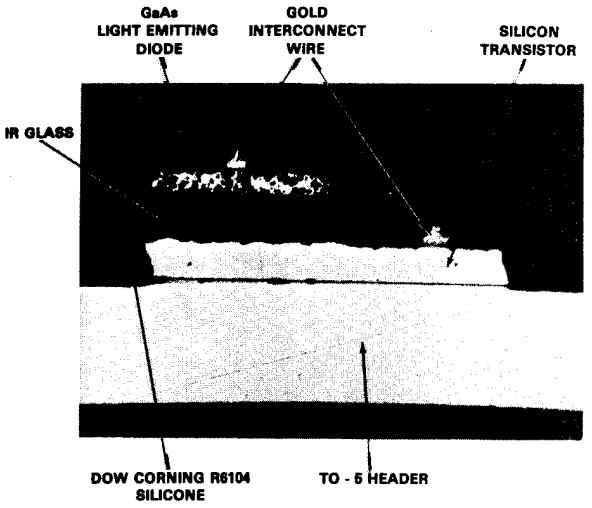

Figure 1. A Cross-Sectional View of the Optically Coupled Isolator Showing the Device Structure (145X MAG)

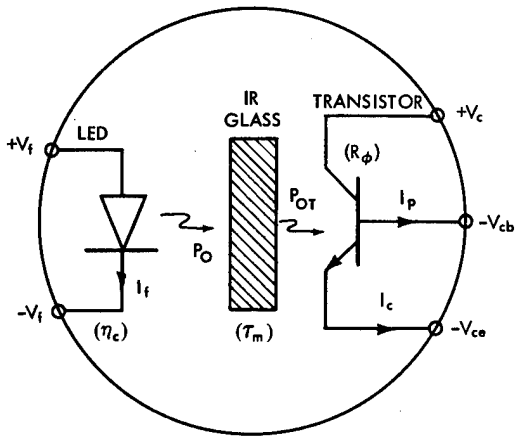

Figure 2. Schematic Model for the Optically Coupled Isolator

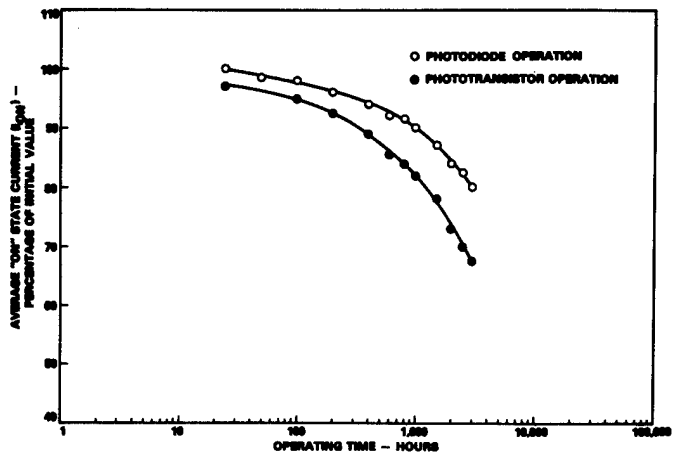

Figure 3. A Plot of the Average Degradation of the Optically Coupled Isolator "On" State Currents for Photo-Diode and Phototransistor Operation

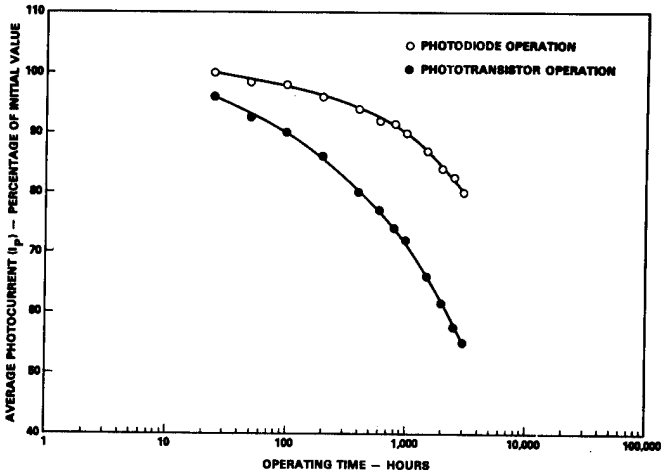

Figure 4. A Plot of the Average Degradation of the Optically Coupled Isolator Photocurrent for Photodiode and Phototransistor Operation

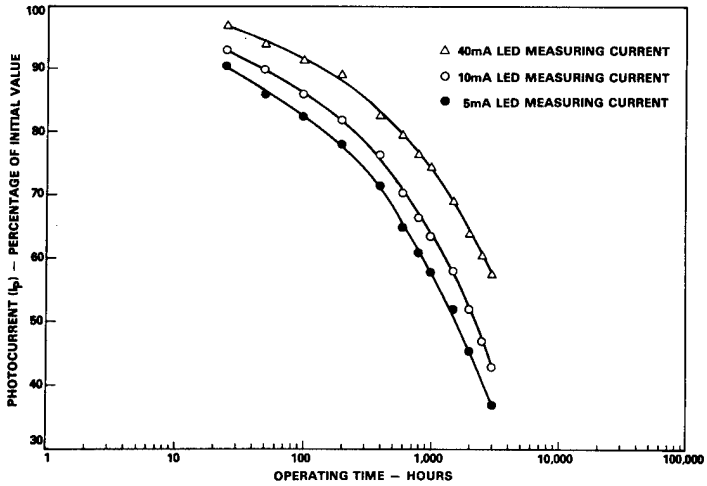

Figure 5. A Plot of the Degradation of the Optically Coupled Isolator Photo-current as a Function of LED Measuring Current for Phototransistor Operation

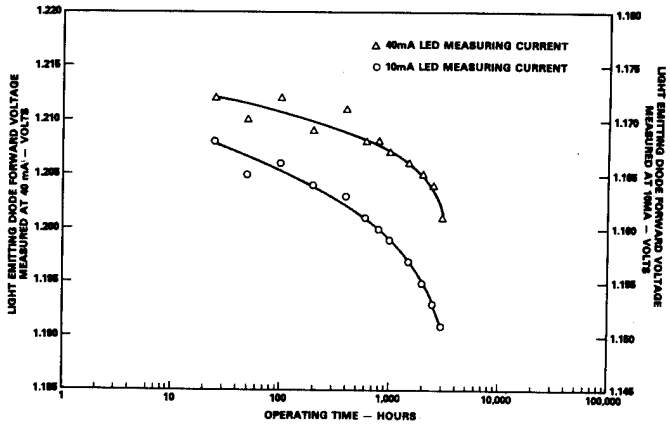

Figure 6. A Plot of the Degradation of the LED Forward Voltage as a Function of LED Measuring Current for Photo-transistor Operation

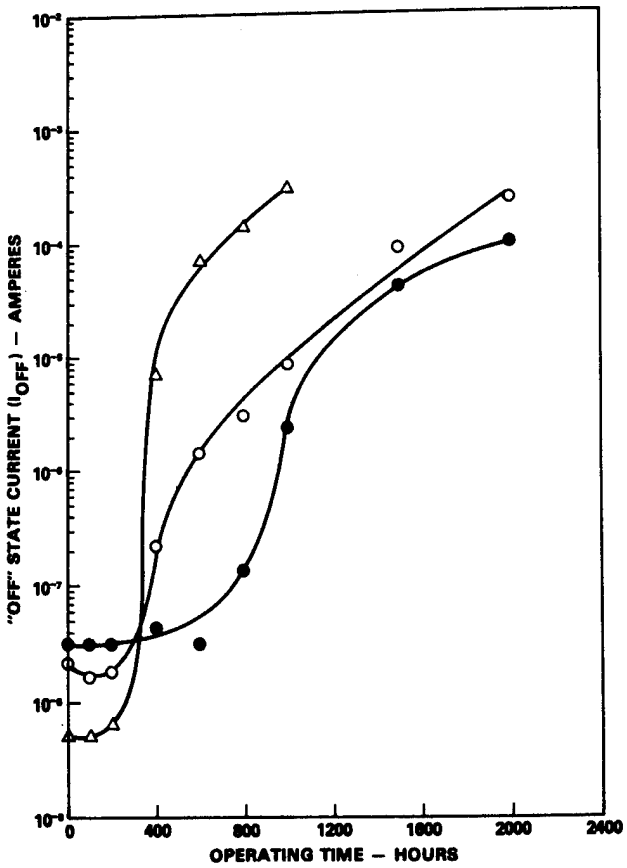

Figure 7. A Plot of the Degradation of the Optically Coupled Isolator "Off" State Current for Photo-transistor Operation

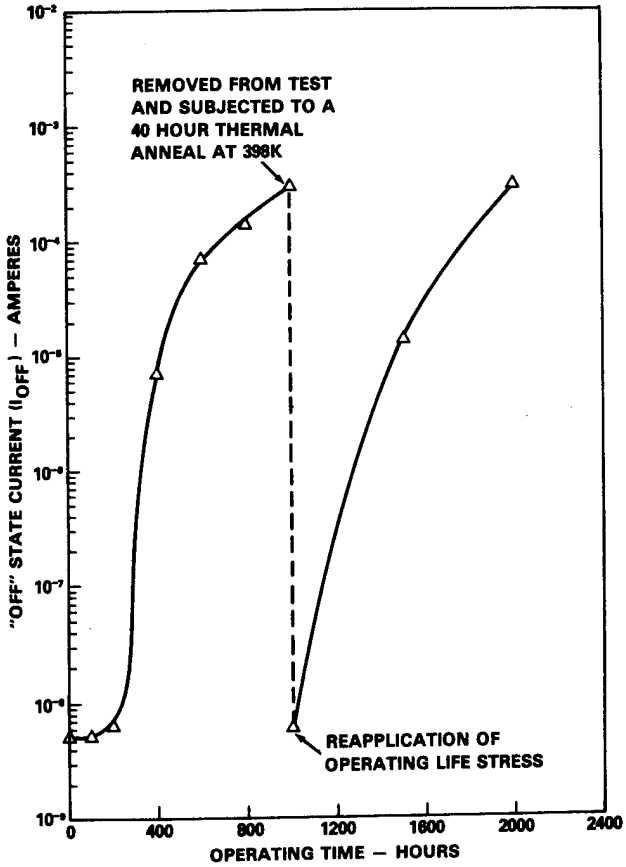

Figure 8. A Plot of the Effect of a Thermal Anneal on the Degradation of the Optically Coupled Isolator "Off" State Current During Photo-transistor Operation

THE RELIABILITY OF INTEGRATED INJECTION LOGIC CIRCUITS FOR THE BELL SYSTEM

by

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Allentown, Pennsylvania 18103

Abstract

The reliability of Integrated Injection Logic (I^2L) or Merged Transistor Logic (MTL) circuits fabricated in a standard bipolar technology with Ti-Pt-Au interconnection is reported. The study is based on accelerated stress aging and actual field results.

Experiments are described which demonstrate that I^2L circuit failure in humid ambients due to Au electrolysis will not occur because of low voltage operation. Failure rates less than 10 FITs for an LSI part (.001% failure per 1000 device hours) under normal stress over a 40 year life are predicted for the main population by accelerated bias temperature and bias humidity stress. Well behaved current gain (βu) under bias temperature step stress indicates that βu degradation will not be a significant failure mechanism.

At this writing, more than 60 million device hours have been accumulated for LSI chips in specific applications with no reported chip failures. This field result firmly supports accelerated stress reliability predictions.

I. Introduction

This paper reports on the evaluated reliability of Integrated Injection Logic[1] (I^2L) or Merged Transistor Logic[2] (MTL) circuits fabricated in a standard bipolar technology with Ti-Pt-Au interconnection (Beam Lead Sealed Junction or BLSJ Technology[3]). Experiments are described in which I^2L circuits are subjected to corrosive medium, bias temperature, and bias humidity stresses. Field results in specific applications are discussed.

I^2L is a bipolar circuit technique which may be fabricated using standard bipolar technology. A schematic of an I^2L logic unit (with FO=4) is shown in Figure 1, and the corresponding topography and cross section in Figure 2. An active pnp load injects base drive into the bases of the npn switching transistors which are operated inversely and direct coupled to obtain logical functions. The logic swing and power supply voltage are equal to a forward diode voltage (<1.0v). Each output is constrained to tie to only one input and must be capable of sinking current supplied to that node. Therefore, for identical units, the current gain of each output (βu) must be ≥ 1.0.

Low voltage operation is a novel feature of the I^2L circuit technique which contributes to excellent reliability. Independent electrolysis tests with metal "comb" patterns indicate a threshold for Au electrolysis occurring at $\sim$1.0v in salt water for the BLSJ system. I^2L operating voltages are well below this threshold. In addition, low voltage on metal lines and high surface concentrations on all surfaces (see Figure 2) makes the I^2L unit less sensitive to surface inversion than most other bipolar and MOS configurations.

The unit may be fabricated with three selective diffusions into n/n+ material. The complete process with contact window and metalization operations requires five masks. Two additional diffusion steps, buried layer and isolation, are required if other bipolar circuit forms, e.g., T^2L, are desired on the same chip (a seven mask process). These processes are referred to as the nonisolated and isolated processes, respectively.

Both nonisolated and isolated I^2L circuit forms have been fabricated in the BLSJ technology. A nonisolated circuit form requiring no on-chip voltage greater than 1.0 volt is the vehicle used to demonstrate I^2L BLSJ circuit immunity to Au electrolysis. An isolated custom LSI part has been subjected to bias temperature and bias humidity accelerated stress. Failure rates less than 10 FITs under normal stress over a 40 year life are anticipated based on these results.

Finally, step stress aging of the I^2L transistor indicates current gain stability under the specified conditions.

At this writing, more than 60 million device hours have been accumulated in the field with no reported chip failures.

II. Devices and Stress Conditions

A nonisolated gated inverter chain (Figure 3) which requires no on-chip voltage above 1.0v has been mounted on a TO-5 header with no moisture protection and operated in salt water. Au wire bonds were used for this test device instead of beam leads. The circuit continued to operate when immersed in Pur-A-Gold 70GV, a high speed neutral type electroplating formulation. The output device driving an external resistive load tied to a variable voltage supply is shown in the segment of inverter chain schematic, Figure 4. The potential of node A monitored by an oscilloscope is equal to the variable supply voltage for half the period of oscillation. The potential on node B is held at V_{SAT} (saturation voltage <0.1v). In this configuration, a voltage greater than the Au electrolysis threshold voltage may be applied between nodes A and B. These results are reported in Section III a.

Another device, a 250 gate, T^2L compatible, I^2L random-logic chip for a telephone system application (Figure 5) requires device isolation and a 5.0v supply for the T^2L-compatible buffers. This chip has been packaged in a 24-pin ceramic DIP (Figure 6) with flow coat (RTV) for moisture protection and subjected to bias temperature (100 units/20mW/300°C) and bias-humidity (74 units/24mW/85°C/85% RH + HCl dip before stress) stresses. The inputs were tied alternately to 0v and 4.5v to assist electrolysis failures which could occur in the T^2L buffer sections (see Figure 5) during bias humidity stress. Device failures as functions of time for each of the samples are contained in Section III b and c.

The LSI chip contains a single logic unit located in the upper right hand corner with accessible input and output (Figure 7). Twenty-five units have been mounted on TO-5 headers and subjected to bias temperature step stress. The stress conditions were 3.0v reverse bias on the collector and emitter junctions with temperature varying from 150°C to 325°C in 25°C increments, one week for each increment. The current gain

was measured at each interval using the circuit configuration in Figure 8. The purpose of this step stress acceleration was to determine current gain stability in time. These results are contained in Section III d.

Section III e reports currently available field results.

III. Results

(a) Electrolysis

Operation of the ring oscillator chip in salt water is demonstrated in Figure 9. Salt water is placed on the chip surface which is kept wet by the water bubbler (foreground). The waveform is displayed on the oscilloscope and supply voltage (650mV) on the digital multimeter in the background. The variable supply voltage is set at 0.7 volts. The frequency of operation is much lower for a wet chip than a dry one because of parasitic capacitances introduced between lines by the water. Thus, a frequency monitor determines moisture presence. Figure 10 is a photomicrograph of this chip which shows the presence of moist salt crystals. Two devices have successfully operated in this ambient for more than 1000 hours each. One unit experienced a package failure after approximately six weeks; a header lead post disintegrated. The second inverter chain failed after two and one-half months. The precise cause of failure was not determinable since the chip was coated with various deposits and/or organic growths and could not be cleaned.

A voltage was applied to the external resistor of a third inverter chain which resulted in a potential difference between nodes A and B (see Figures 4, 11, 12 and 13) greater than the threshold for Au electrolysis in salt water. In less than one minute, the output waveform dropped to V_{SAT} indicating a short circuit between nodes A and B.

A scanning electron micrograph 500X, Figure 11, shows a dendritic growth which occurred at the point where the lines are most closely spaced (12μm). The Au wire from the bonding post may be seen in the foreground. An SEM close-up (5000X) is pictured in Figure 12. Au has been transported from the anode, node A, to the cathode, node B, and piled up in fern-like deposits which build back towards the anode. The X-ray image, Figure 13, positively identifies the dendrite as gold.

A fourth unit was successfully operated in Pur-A-Gold 70GV, a neutral type gold plating formulation for more than one hour. The experiment was terminated at this time without failure. At this writing, twenty units are being placed in a well controlled chlorine gas ambient for analysis.

(b) Bias Temperature

Cumulative failures at each test point for the isolated I^2L BLSJ circuit form (Figure 4) are given in Table 1. For a log normal failure distribution (Figure 14) these data indicate a 600,000 hour median life and a 3.99 standard deviation. The failure rate calculation as outlined by Peck and Zierdt[4] using a conservative activation energy of 1.02 ev predicts a failure rate of <1.0 FIT for this mechanism at 60°C operation.

Table 1

Bias Temperature Stress (100 Units)

Time (hours)	Cumulative Failures
8	0
48	0
283	2
1000	8
2000	8
3000	8
4000	8
5000	9

(c) Bias Humidity

Table 2 contains the cumulative failures at each test point for bias-humidity stress of the same 250-gate circuit. For the log normal distribution (Figure 15), the median life is 100,000 hours and the standard deviation is 2.3. Using the electrolysis model[5] and a 10°C rise in junction temperature above ambient, the failure rate for the typical U.S. condition[5] (25°C/50% RH) is <10 FITs over a 40 year life. For a severe U.S. condition,[5] a summer night in Baton Rouge, La., the predicted maximum failure rate is ∿50 FITs over a 40 year life.

Table 2

Bias Humidity Stress (74 Units)

Time (hours)	Cumulative Failures
7	0
80	0
300	0
500	1
1000	1
2000	5
3000	5
4000	6
5000	6
6000	11
7000	11
8000	11

(d) Current Gain

The twenty-five (25) I^2L units subjected to bias temperature step stress showed slight gain degradation with a maximum of 21%. Average current gain (βu) versus temperature is contained in Table 3. One unit failed catastrophically at the 300°C test point. Examination revealed severe mechanical damage (cracked chip) apparently present from the outset which caused premature failure in this unit (#5). These data indicate that an initial gain specification 10% greater than than the end of life requirement (40 years which equivalently occurs between the 250°C and 275°C step stress data points for a 1.02ev activation energy) is conservative in providing adequate gain during life.

Table 3

Average Current Gain at Each Temperature
25 Units

Temperature (C)	Average Current Gain (βu) @ I_{BX}=10μa V_{CE}=.5v
Initially	2.40
150	2.45
175	2.40
200	2.40
225	2.34
250	2.35
275	2.30
300	2.27
325	2.19

Average % Change = -8 3/4%
Worst Case % Change = -21%
Unit #12

(e) Field Results

Two different systems have been in field trial for over 6 months. The first of these has 2 beam leaded LSI I^2L chips packaged in a single 24 pin ceramic DIP with RTV encapsulation. The system operates on customer premises and devices have purposely been put in service in unfavorable environments. As of March 1, 1976, 4.7 million device hours have been accumulated with no device failures.

A second system, utilizing one I^2L chip design, has accumulated 8.3 million device hours in field trial in a central office environment with no device failures. Product shipments are now underway and more than 60 million device hours have been accumulated with no device failures reported.

In all cases, no burn-ins or humidity screens have been employed on the encapsulated chips prior to service. The composite of all data at this time would indicate an average failure rate over early life less than 17 failures/10^9 device hours.

IV. Conclusions

Successful Operation of a nonisolated I^2L BLSJ circuit form in salt water and a neutral type gold plating solution has been demonstrated. This result suggests that failure due to Au electrolysis will not occur in such circuits because of the low voltage operation.

Failure rate calculations based on bias temperature stress of a T^2L compatible I^2L BLSJ chip predict a conservative failure rate <1 FIT at 60°C due to temperature-bias induced mechanisms. Failure rate calculations based on bias humidity stress of the same circuit predict a failure rate <10 FITs for typical U.S. conditions and ∿50 FITs maximum for a severe case when operating 10°C above ambient.

Finally, I^2L current gain stability under bias temperature step stress aging indicates current gain degradation will not be a significant failure mechanism.

At this time, 60 million device hours have been accumulated in the field with no reported chip failures. This result firmly supports accelerated stress reliability predictions.

Acknowledgments

The authors thank B. R. Jones and C. H. Zierdt, Jr. for informative discussions; R. A. Darnall for supplying bias-temperature, bias-humidity, and step stress data; and J. B. Bindell and B. J. Snyder for the scanning electron micrograph work.

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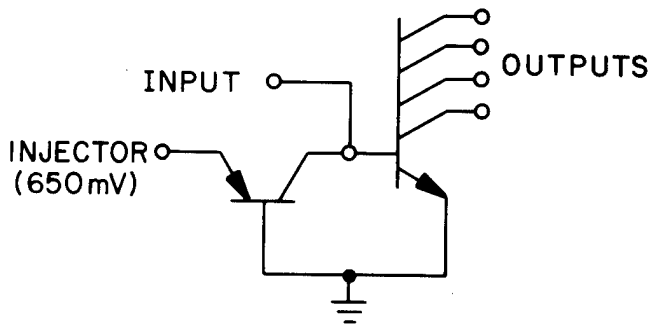


Figure 1. Integrated Injection Logic Unit

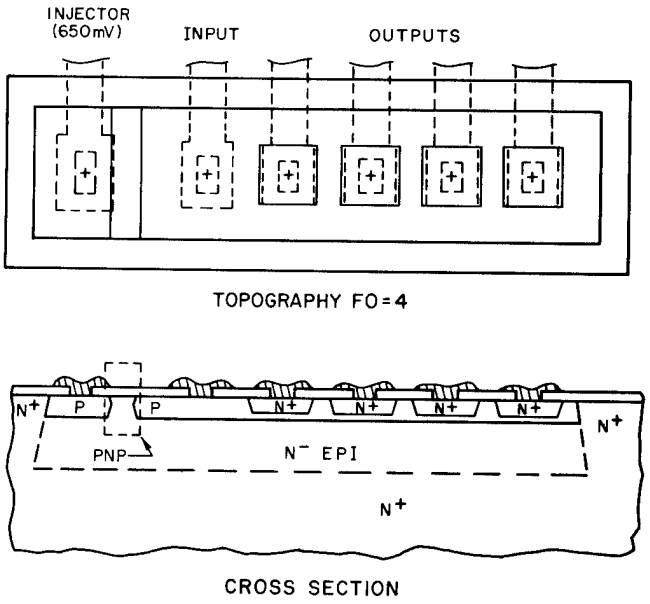


Figure 2. Logic Unit Topography and Cross Section

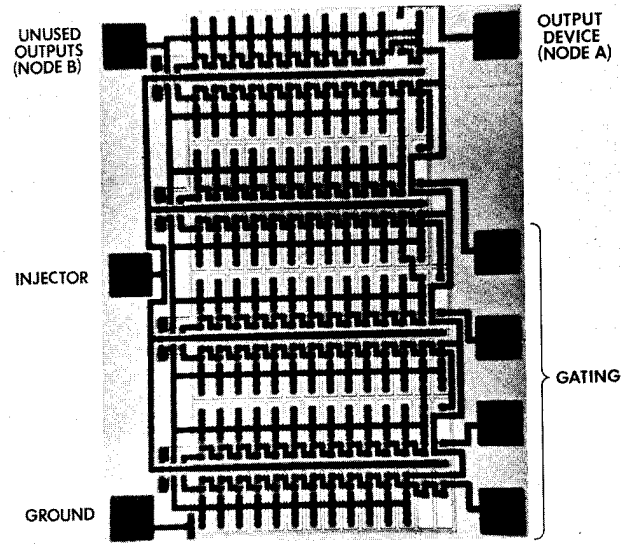


Figure 3. Photomicrograph of Gated Inverted Chain

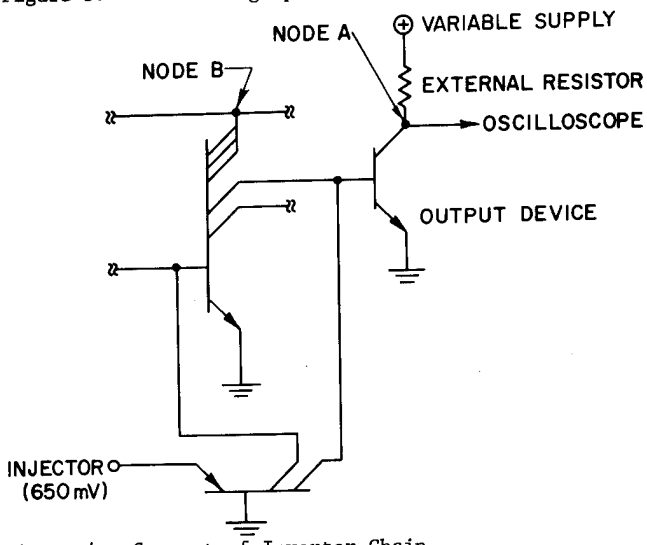


Figure 4. Segment of Inverter Chain

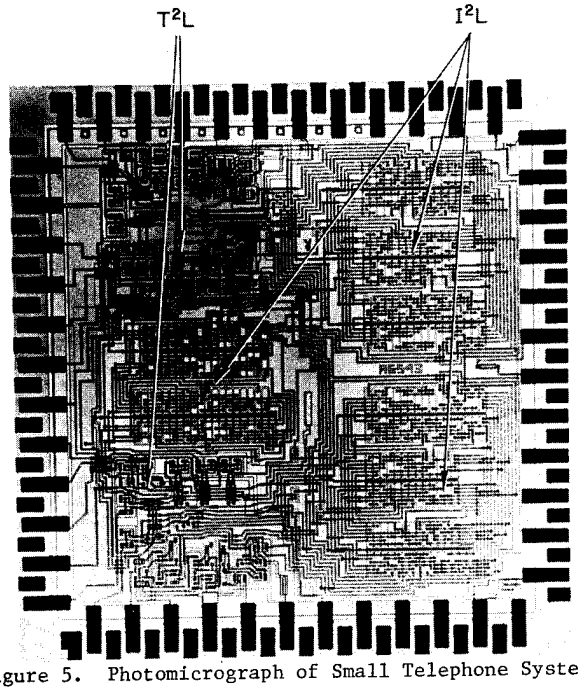


Figure 5. Photomicrograph of Small Telephone System IC

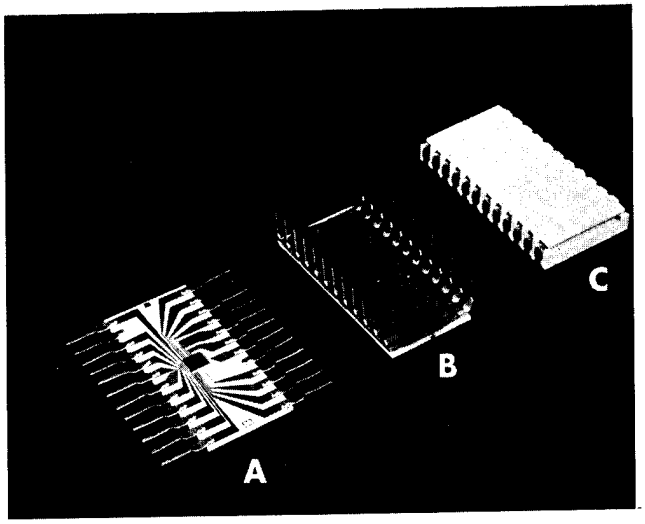


Figure 6. 24 Pin Ceramic DIP

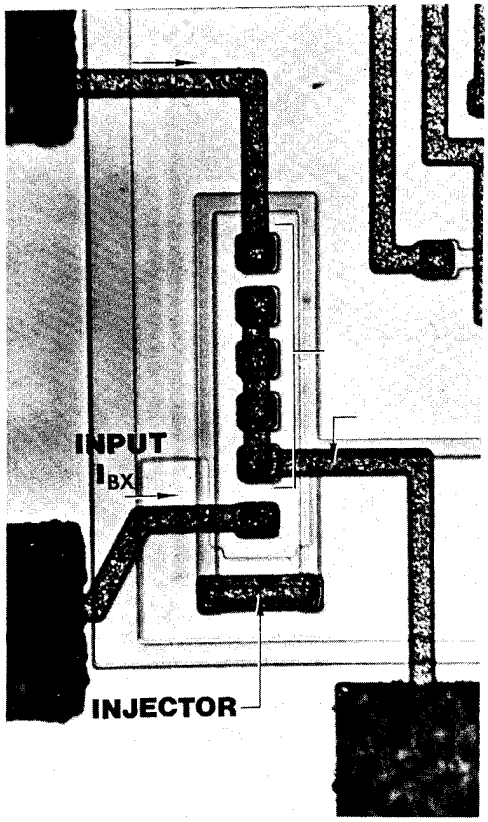
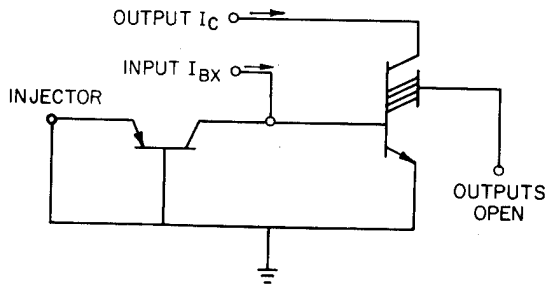


Figure 7. Single Logic Unit



$$\beta_u \equiv \frac{I_C}{I_{BX}} \geq 1.0$$

Figure 8. Logic Unit Configured for Gain Measurement (Worst Case)

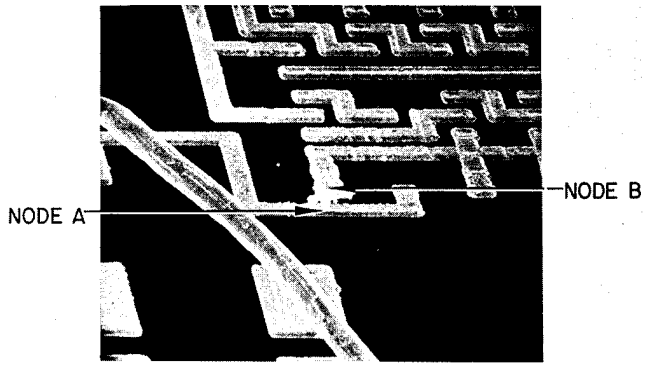


Figure 11. Scanning Electron Micrograph of Dendritic Growth (500X)

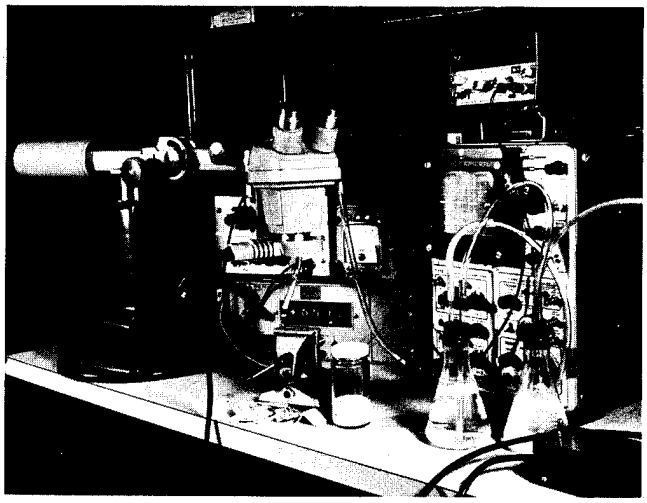


Figure 9. Corrosive Medium Test Setup

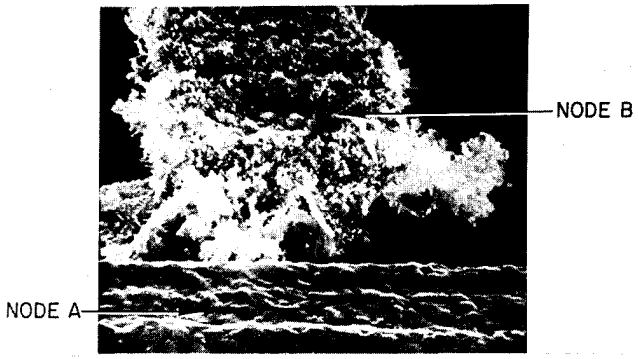


Figure 12. Scanning Electron Micrograph of Dendritic Growth (5000X)

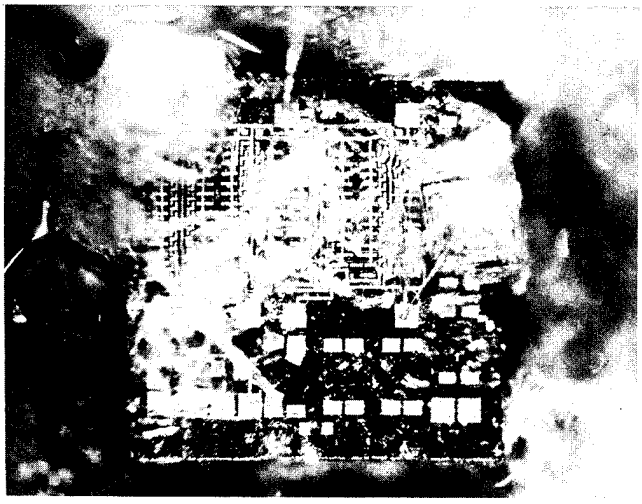


Figure 10. Photomicrograph of Gated Inverter Chain Showing Moist Salt Crystals

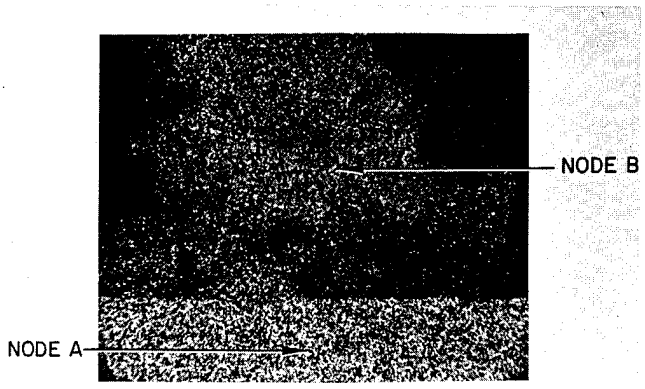


Figure 13. Gold X-ray Image (5000X)

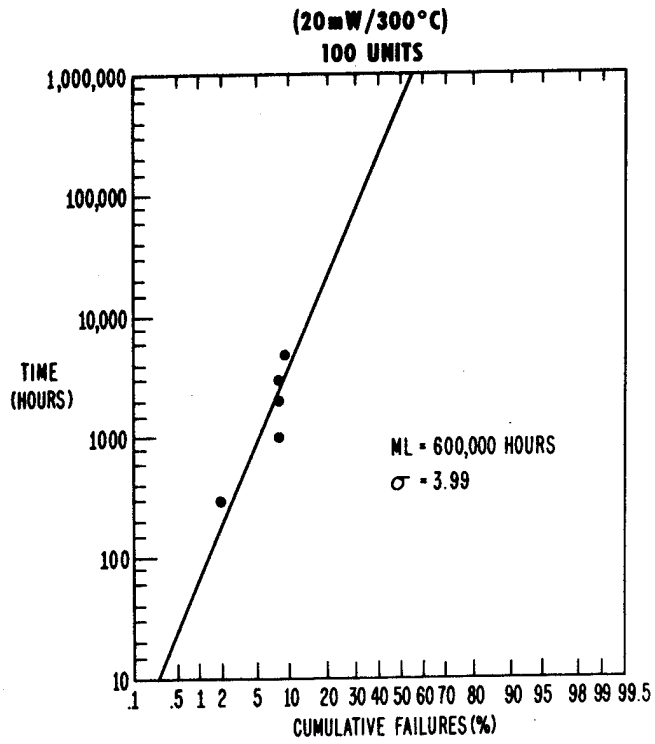


Figure 14. Cumulative Failure Distribution Bias Temperature Stress

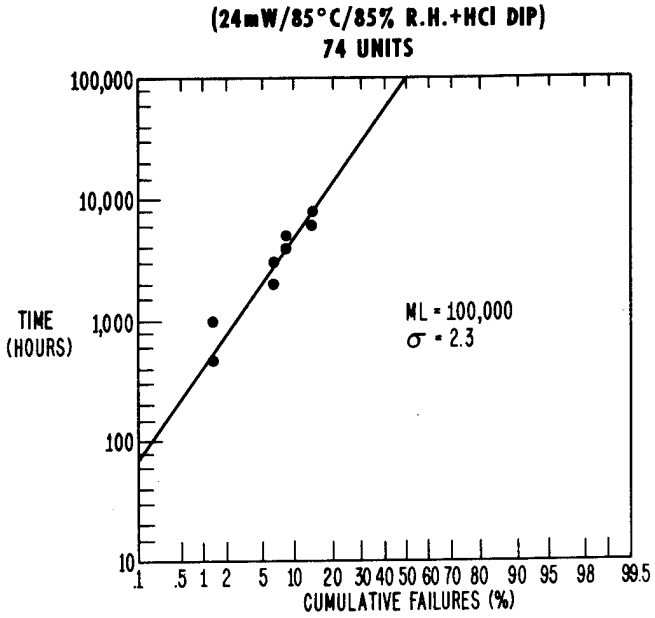


Figure 15. Cumulative Failure Distribution Bias Humidity Stress

A STUDY OF SURFACE CHARGE INDUCED INVERSION FAILURE OF JUNCTION ISOLATED MONOLITHIC SILICON INTEGRATED CIRCUITS

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Abstract

The development of charge on the dielectric surface of junction isolated monolithic SICs can result in significant reductions in operating life. The transient and steady state characteristics of IC failure caused by the development of charge on the dielectric surface have been studied under room ambient conditions by monitoring the current through the inversion layer formed between circuit components of like conductivity type. The results of this study indicate that this IC failure mechanism is sensitive to IC layout geometry and suggest that conservative junction isolated monolithic SIC designs should have an inversion threshold voltage greater than the operating voltage.

I. Introduction

The deleterious effects of charge on the outside surface of dielectric passivated semiconductor devices are sufficiently well understood to have been described in such standard texts as Grove,[1] and Burger and Donovan.[2] This charge may develop in a number of ways. In the example discussed by Grove,[1] the charge spreads from conductors on the dielectric surface. In the example discussed by Burger and Donovan,[2] the charge develops in response to the fringing field about reverse biased P-N junctions in the underlying semiconductor substrate. In the well documented Telstar I case,[3] the charge was drawn to the device surface from the ionized ambient within the device encapsulation.

Independent of the way in which the charge develops, its rate of redistribution will be controlled by conduction on the dielectric surface.[4] Several methods of controlling the conductivity of dielectric surfaces, including the application of synthetic polymer films, have been developed for vacuum tube envelopes,[5] because the reliability of vacuum tubes is affected by the magnitude of the leakage currents. The application of a hydrophobic, insulating coating to bonded semiconductor chips has been recommended to protect them from corrosion and mechanical damage,[6] because this coating limits the currents associated with corrosion. In some cases, however, the reliability of semiconductor devices is affected more by the surface charge distribution produced by these currents than by the currents themselves. In this report, the failure of junction isolated monolithic silicon integrated circuits caused by the development of charge on the dielectric surface is examined.

II. Integrated Circuit Reliability

Figure 1 displays the temperature storage life and the operating life of an SIC operational amplifier susceptible to failure caused by the development of charge on the dielectric surface while operating. Integrated circuits exhibiting the temperature storage life of Figure 1 under all stress conditions are desirable. Unfortunately, the data of Figure 1 indicates substantially reduced life under operating conditions.

Figure 2 summarizes the results of efforts to improve the operational life for one operational amplifier code. The data represents the frequency of occurrence of failures in samples of 20 devices subjected to a 150°C operational life test for 16 hours for two design modifications of an SIC operational amplifier. The frequency distribution labeled "Initial" reflects the unsatisfactory device quality of the initial device design. The failure percentage was decreased from 21% to 5% by enlarging the metal contacts to the collector of NPN transistors wherever possible. This improvement is shown in the frequency distribution labeled "Field Plates." The improvement obtained with the field plates is thought to be caused by a reduction in the potential of the dielectric surface for the modified IC layout. The process modification we are using today reduced the failure percentage from 21% to 0.7% with no field plates. This improvement is shown in the frequency distribution labeled "Surface Concentration Enhancement" and resulted from an increase in the inversion threshold voltage of the epitaxial layer. The inversion threshold voltage was increased by decreasing the surface resistivity of the 2-4Ω-cm N-type epitaxial layer used in the manufacture of the affected devices.

III. Phenomenological Description of Failure

The cause of failure of these devices is depicted in the lower section of Figure 3. This figure shows the presence of sufficient negative charge on the dielectric surface to cause inversion of the underlying N-type silicon. At sufficiently negative values of V_D, the resultant P channel FET would be in saturation and a channel current controlled by the potential on the dielectric surface would flow from the base to the isolation diffused regions.

The behavior of this device is analogous to that of the more conventional IGFET structure shown in the upper section of Figure 3. However, there are several obvious differences. The potential on the dielectric of the lower structure is strongly related to the potential difference applied between the two P-diffused regions, is not constant over the dielectric surface, and will respond slowly to changes of the applied potential difference.

In the operational amplifiers, the channel current flowing from a base diffused region to an isolation diffused region resulted in a partial to complete loss of current from a current repeater in the first gain stage. The loss of this bias current was manifested by a change in quiescent output voltage. The quiescent output voltage would frequently attain that of the positive power supply. In contrast to the structures shown in Figure 3, the structure of the operational amplifiers was such that the contact to the isolation diffused region was well removed from the site of the induced channel, so inversion was due to charge separation produced by the fringing field about the reverse biased isolation junction.

In the next three figures, some important characteristics of this failure mechanism are displayed. The data was obtained at room temperature using a test structure like the lower structure of Figure 3, but with the contact to the isolation diffused region well removed from the site of the induced channel. For these studies, none of the devices were protected with the synthetic polymer film used on the packaged devices for which life data was presented earlier in Figures 1 and 2. The effect of this polymer film on device life is suggested by the change in time units from hours in Figure 1 to seconds in Figures 4-6.

Figure 4 shows the time development of the base to isolation channel current with 50V applied to reverse bias the isolation junction, V_D=-50V. The dashed curve indicates the degree of reproducibility of the results. This data represents the bias polarity actually existing in the operational amplifiers and indicates a projected time of 10 to 20 seconds to develop the 15 to 30 μA channel current that would cause failure of the operational amplifiers. This exceptionally short life was manifested in problems of testing operational amplifier chips. The shape of this curve, with the channel current attaining a maximum at some short time and subsequently reverting to a lower value, was typical. This behavior was manifested in operational amplifier behavior by complete or partial recovery after sufficiently long times under bias. This behavior will be shown to be attributable to charge separation produced by the fringing field about the reverse biased isolation junction.

Figure 5 shows the time evolution of isolation to base channel current with 50V applied to reverse bias the base junction, V_D=+50V. Again, the dashed curve indicates the degree of reproducibility of the results. Notice that these data exhibit more structure than the data of Figure 4 and that the channel currents at short times are much smaller than those shown for the reverse biased isolation junction. The short time behavior shown in Figure 5 is attributable to charge separation about the reverse biased base junction, while the subsequent increase in channel current is attributable to charge spread from the base contact. The increase in channel current at long times is not seen in the data of Figure 4, because the contact to the isolation diffused region is well removed from the site of the induced channel.

The difference in channel current levels observed during the early stages of the development of charge on the dielectric surface in Figures 4 and 5 is attributable to the different surface potentials developed with the two bias polarities. The magnitude of the surface potential is a strong function of the device topology which is partially determined by the junction bias as well as the integrated circuit layout. This dependence of the surface potential on the device topology accounts for the partial success of the enlarged NPN transistor collector contacts in providing improved device life.

Figure 6 displays the time to obtain a channel current of 100 μA as a function of ambient relative humidity at room temperature for several values of the two bias polarities. The trend lines clarify the failure acceleration indicated by the data bars for increased relative humidity, increased reverse bias above the inversion threshold of the epitaxial layer, and choice of bias polarity. The data bars associated with each observation of Figure 6 indicate the range of relative humidity of the device ambient during the course of each trial. For clarity, the data bars for negative values of V_D have been terminated in open circles, while those for positive values of V_D have been terminated in parentheses.

IV. Model

So far, qualitative explanations for some important characteristics of the mechanism for operational amplifier failure have been presented. Now, the problem of quantitative explanation and design will be addressed.

There are two distinct aspects to this problem. On the one hand, we have the problem of determining the inversion threshold of a given device design. Since the design equations[7] for this determination are well known, these design equations will not be

reviewed here. On the other hand, we have the problem of determining the maximum voltage against which a given device must be protected. It may be obvious that the maximum surface potential developed in response to charge spread from conductors will not exceed the potential applied to the circuit, but it may not be obvious that this is also true of the surface potential developed in response to the fringing field about reverse biased P-N junctions. Since there is less familiarity with the development of surface potential in response to the fringing field about reverse biased P-N junctions, the important relations will be reviewed and some results for a specific example will be presented.

For the slowly varying fields of interest here, the development of charge on the dielectric surface of an integrated circuit can be described by the diffusion equation with a diffusion constant given by the reciprocal of the product of a resistance and the local dielectric capacitance per unit area. This diffusion equation can be derived from the equations describing the propagation of signals along a parallel plane transmission line[8] with no shunt conductance and no series inductance. The diffusion equation obtained is

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = RC \frac{\partial V}{\partial t} \qquad (1)$$

Equation (1) actually describes the development of the potential difference through the dielectric, V(x,y,t), at point (x,y) on the dielectric surface and at time "t" produced by the field aided drift of charge across the dielectric surface. In general R will be the sum of the sheet resistances of the substrate and dielectric surface.[9] For our purposes, the sheet resistance of the dielectric surface will dominate and the silicon substrate potential will be independent of time. Under these conditions, Eq. (1) may be considered to describe the diffusion of the dielectric surface potential. Eq. (1) could then be rewritten to describe the diffusion of dielectric surface charge density by multiplying through by the local dielectric capacitance density, but the initial and boundary conditions are more easily established for the dielectric surface potential. In the absence of a net charge on the dielectric surface, the dielectric surface potential at time t=o is equal to the potential of the underlying semiconductor region. At conductors on the dielectric surface, the dielectric surface potential is equal to that of the conductor. At the edges of the dielectric, the component of the gradient of the dielectric surface potential normal to the edge equals zero. With these boundary conditions, Eq. (1) has been used to evaluate the development in time of the dielectric surface potential[10] produced by the fringing field about a reverse biased P-N junction. For this analysis, a one-dimensional representation of the test structure used to gather the data of Figures 4-6 with no conductors on the dielectric surface has been used. The results of this evaluation are displayed in Figures 7 and 8.

Figure 7 shows the surface potential as a function of position on the sample and a diagram of the model structure. The gradient of the dielectric surface potential at the edges of the sample is zero and the potential difference between the isolation and base diffused regions is V_o. The potential distributions shown in Figure 7 are analogous to those for particle diffusion from a limited source into a finite region. At short times, the potential distribution pivots about $V_o/2$ at "a", the edge of the source; at long times, the potential approaches a constant value, $V_o(\ell-a)/\ell$ where "ℓ" is the length of the sample. Notice that the final value of surface potential is just that required to assure charge conservation on the sample surface. It should be clear from the potential distributions of Figure 7 that increasing the space between the two P-regions will increase the time required to attain a given value of the average surface potential over the N-region susceptible to inversion.

Figure 8 shows the average potential over the N-region susceptible to inversion, the region between points "a" and "b", as a function of time for several modifications of the sample geometry. These results show that the average surface potential over the N-region susceptible to inversion can decrease at long times for a/ℓ values greater than 0.5 and that the final value of this potential increases as a greater fraction of the dielectric surface covers the diffused region biased at the high potential. Figure 8 shows that the dielectric surface potential produced by the fringing field about a reverse biased P-N junction will not exceed the applied potential if there is no net charge on the dielectric surface.

On the basis of this discussion, it should be clear that a conservative integrated circuit design should have not only sufficient breakdown voltage but also sufficient inversion threshold voltage to sustain the operating voltage. The design implications of this statement are brought out by Figure 9. Figure 9 shows the breakdown voltage of a one-side abrupt junction versus background concentration and inversion threshold voltage versus background concentration for three values of dielectric capacitance. The inversion voltages were calculated for no interface or oxide charge. The presence of positive charge in the oxide would increase the inversion threshold voltage of N-type silicon and decrease the inversion threshold voltage of P-type silicon. For a conservative integrated circuit design, the point at the total operating voltage and minimum impurity concentration should fall below both the breakdown voltage line and the inversion threshold line for the design oxide capacitance. Special design precautions should be taken if this is not the case.

V. Summary And Conclusion

In this presentation, the failure of junction isolated monolithic silicon integrated circuits caused by inversion of the epitaxial layer in the presence of charge on the dielectric surface has been discussed. Provided no net charge exists on the dielectric surface of the device, the potential difference between the dielectric surface and the underlying semiconductor material will not exceed the voltage applied to the integrated circuit. The actual magnitude of the dielectric surface potential at any time after application of the operating voltage will depend on details of the integrated circuit design and the resistivity of the dielectric surface or of any protective film applied to this surface. Because the resistivity controlling charge redistribution may depend on environmental factors such as ambient humidity and temperature, control of surface resistivity may not always be a desirable way of maintaining the reliability of junction isolated monolithic silicon integrated circuits. The results of this study suggest that junction isolated monolithic silicon integrated circuits designed to have an inversion threshold voltage greater than the operating voltage will be protected from inversion of the epitaxial layer caused by charge spread from conductors and by charge separation produced by the fringing field about reverse biased P-N junctions.

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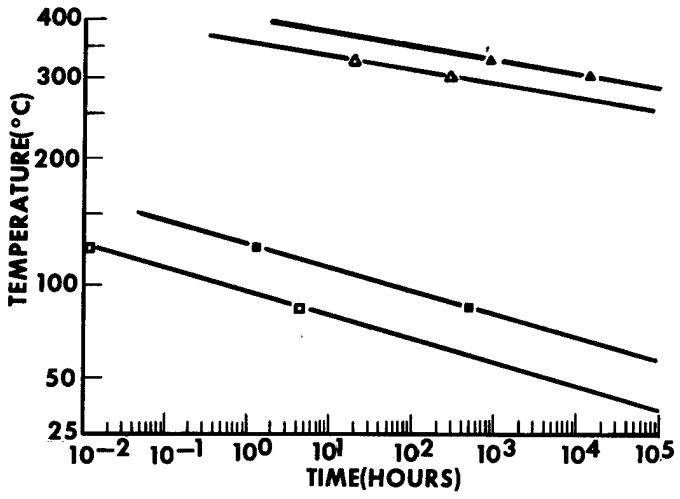

Figure 1. The Effect of Two Stress Conditions on the Reliability of Operational Amplifiers Susceptible to Failure Caused by the Development of Charge on the Dielectric Surface While Operating.

▲ - High Temperature Storage Life for 50% Failure.

△ - High Temperature Storage Life for 0.1% Failure.

■ - High Temperature Operational Life for 50% Failure.

□ - High Temperature Operational Life for 10% Failure.

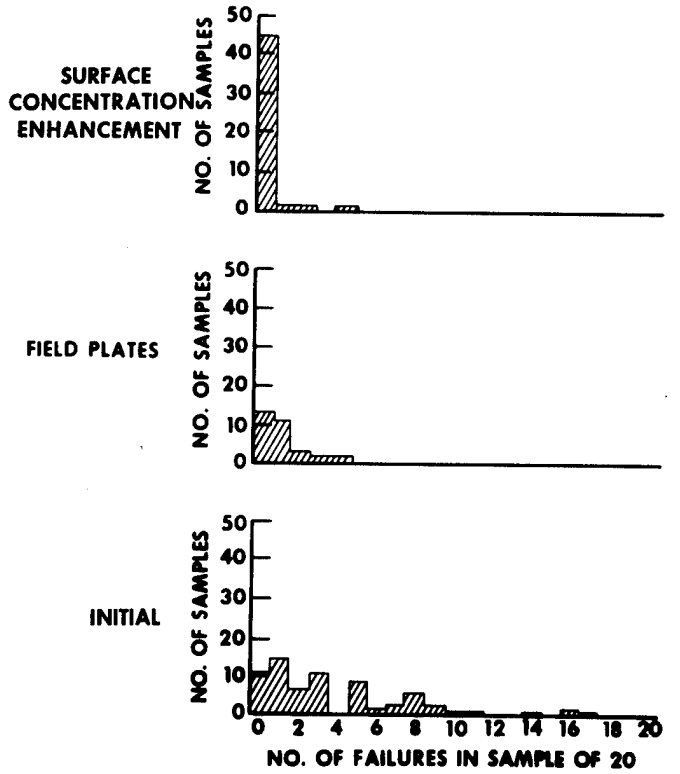

Figure 2. Frequency of Occurrence of Failure in Samples of Size 20 Subjected to a High Temperature Operational Life Test at 150°C for 16 Hours for the Circuit Design Modifications Discussed in the Text.

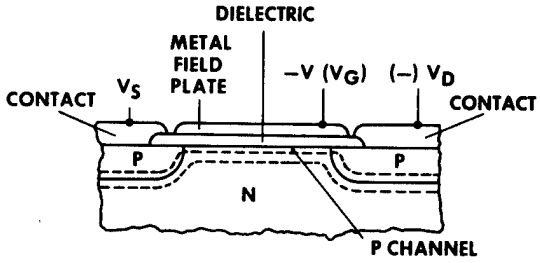

DIAGRAM OF IGFET WITH SUFFICIENT GATE VOLTAGE, V_G, TO INVERT THE EPITAXIAL SURFACE.

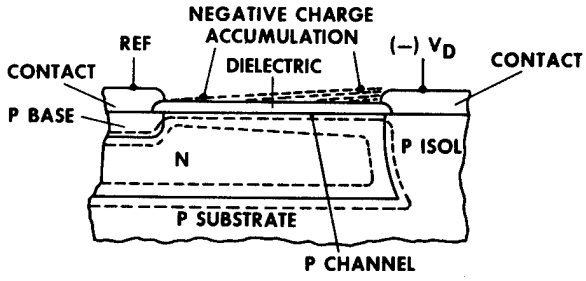

DIAGRAM OF AN IC REGION WITH REVERSE-BIASED ISOLATION JUNCTION AND SUFFICIENT CHARGE ACCUMULATION ON DIELECTRIC SURFACE TO INVERT EPITAXIAL SURFACE.

Figure 3. Comparison of the Controlled Formation of an Inversion Layer in an IGFET, Top, and of the Uncontrolled Formation of an Inversion Layer in a Junction Isolated Monolithic Silicon Integrated Circuit, Bottom.

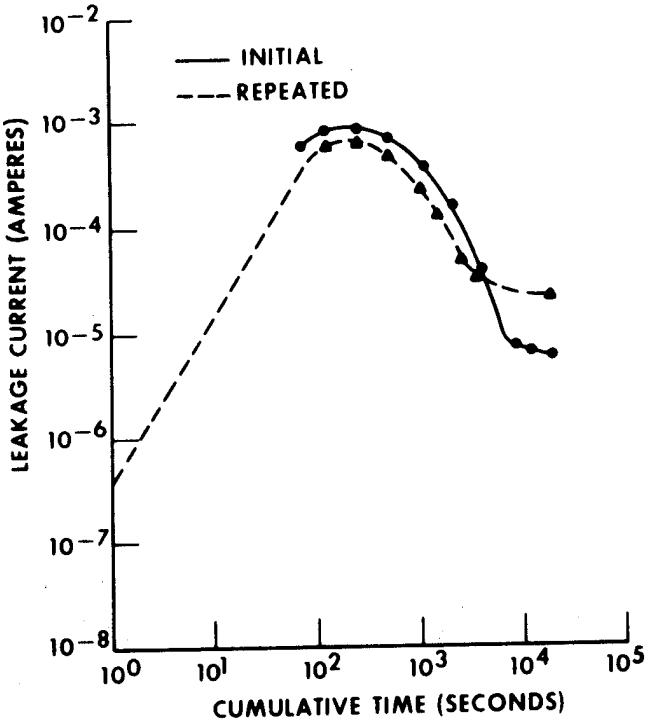

Figure 4. Observed Time Development of Channel Current of the Structure Shown in the Bottom Section of Figure 3 in Room Ambient with V_D = –50 V. The Two Sets of Data Points Show the Degree of Reproducibility Observed in Two Trials.

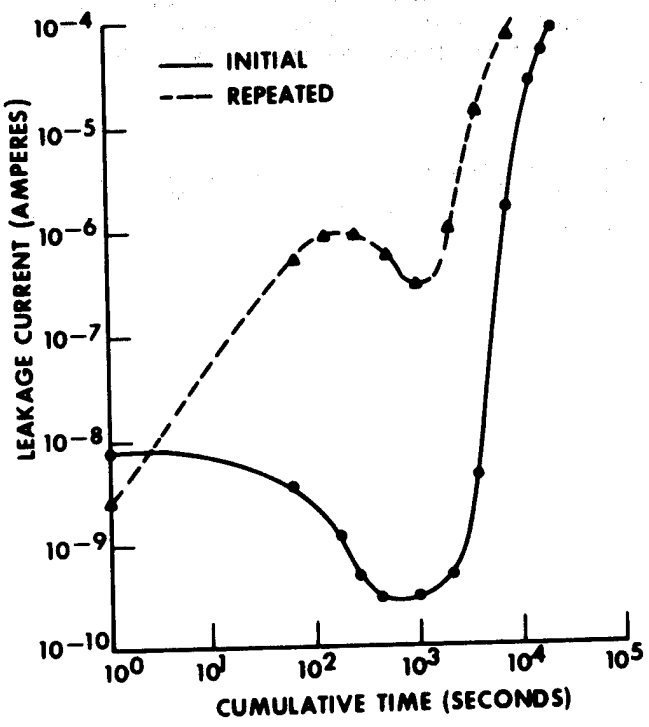

Figure 5. Observed Time Development of Channel Current of the Structure Shown in the Bottom Section of Figure 3 in Room Ambient with V_D = +50 V. The Two Sets of Data Points Show the Degree of Reproducibility Observed in Two Trials.

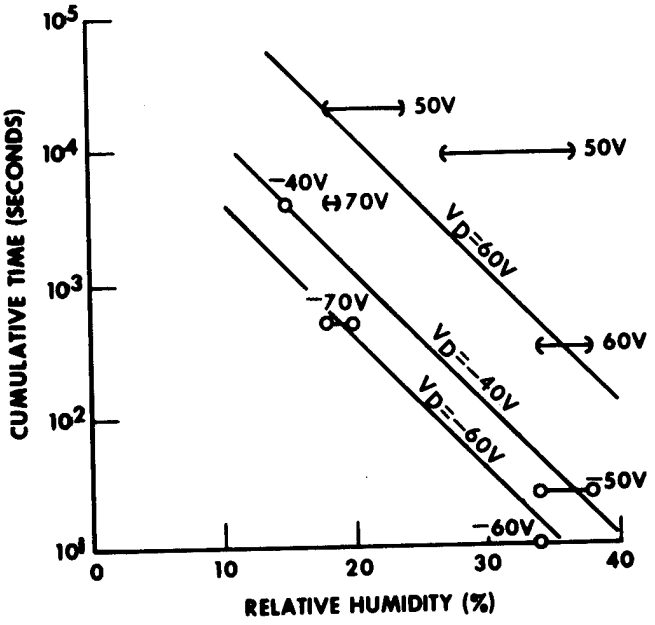

Figure 6. Cumulative Time to Obtain a Channel Current of 100 μA in the Structure Shown in the Bottom Section of Figure 3 Versus Ambient Relative Humidity for Different Values of V_D at Room Temperature. The Data Bars Show the Range of Ambient Relative Humidity Observed During Each Trial at Different Values of V_D. For Clarity, the Data Bars for Negative Values of V_D Have Been Terminated in Open Circles, While Those for Positive Values of V_D Have Been Terminated in Parentheses. The Solid Lines Only Serve to Indicate the General Trends Exhibited by the Data.

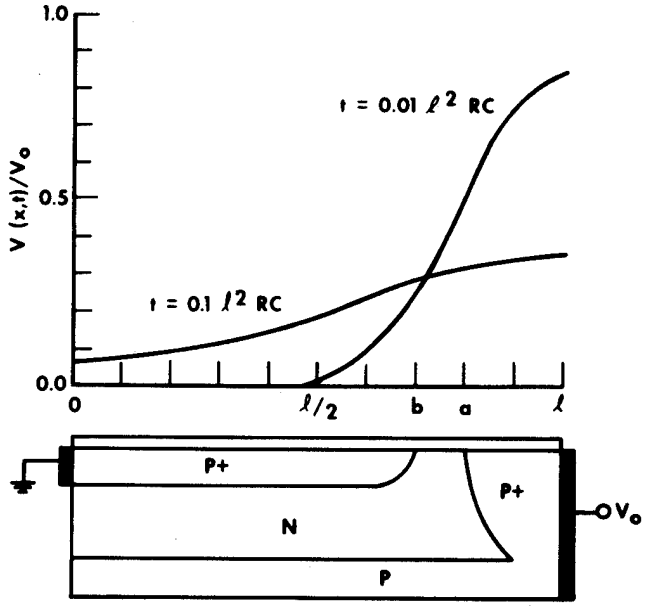

Figure 7. Calculated Values of the Normalized Surface Potential Caused by Charge Separation on the Dielectric Surface Versus Position on the Physical Structure at Two Normalized Times.

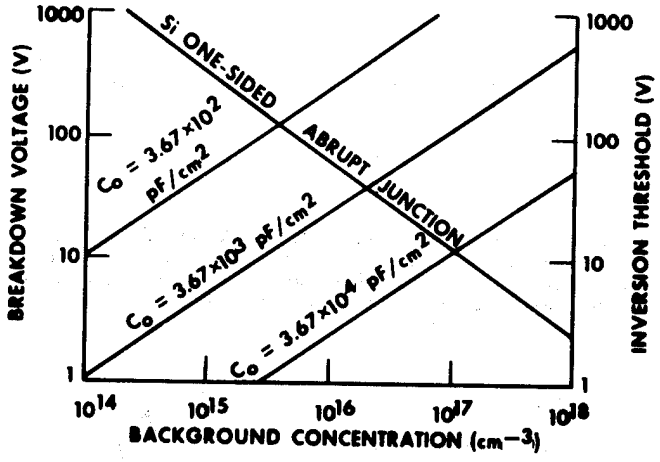

Figure 9. Breakdown Voltage of a One-Sided Abrupt Junction in Silicon and Inversion Threshold Voltage in Silicon in the Absence of Charge in the Passivating Dielectric Versus Background Concentration.

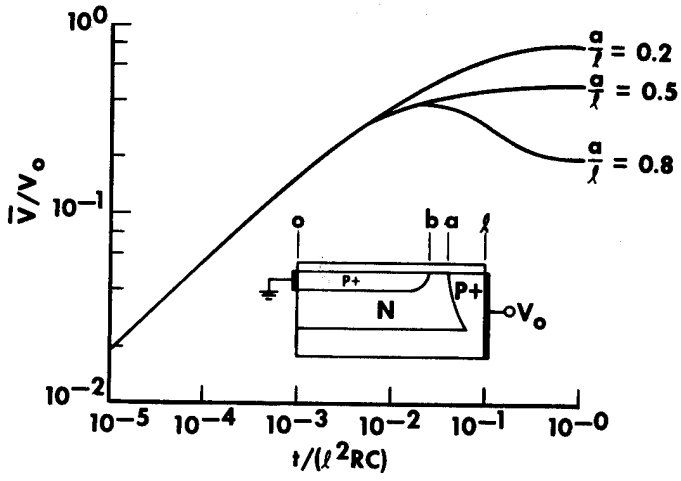

Figure 8. Calculated Values of the Average Normalized Surface Potential Over the Region Susceptible to Inversion $\bar{V}/V_o$ Versus Normalized Time for Three Sample Geometries With b = a –0.1ℓ.

RELIABILITY IMPLICATIONS OF HOT ELECTRON GENERATION AND PARASITIC BIPOLAR ACTION IN AN IGFET DEVICE

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Abstract

Potential reliability effects due to a profusion of hot electrons generated by a parasitic bipolar have been identified in short channel N-type IGFET devices. An explanation of the phenomenon as well as a mathematical and circuit model for the effects are presented. Results from the model will be used to predict changes in device characteristics with time.

Introduction

When IGFETs are aggressively designed with short channel lengths for better performance and density, the effects due to the lateral parasitic bipolar transistor that resides between source and drain can be quite detrimental to device operation and reliability. The most readily realized effect is that the IGFET exhibits premature drain breakdown because of bipolar open-base limitations.[1,2] These limitations are prevalent when substrate current flows as a result of impact ionization in the drain depletion region. The amount of holes that constitute the substrate current is initially related to the amount of IGFET channel current. As the magnitude of the substrate current increases with increasing channel current, a point is reached where there is a sufficient potential across the substrate resistance to cause the substrate-to-source junction to forward bias. This accounts for the bipolar-like sustaining characteristics shown in the photograph in Fig. 1 of a short channel IGFET device.

Bipolar action ensues when the source conducts leading to a significant bipolar current that is added to the IGFET channel current. This in turn increases the amount of impact ionization which adds to the bipolar's base current. Although the process is regenerative, it stabilizes with some value of electrons entering the drain depletion region. The number of electrons is larger than one would expect from just IGFET considerations. A fraction of these electrons is redirected by phonon collisions in the depletion region after being accelerated by the electric fields that are present. Some of these electrons travel toward the gate oxide and are accelerated by the gate field. If they obtain sufficient energy, there is a finite probability that they will be injected into the oxide where they can be trapped and become resident as negative charge in the oxide region adjacent to the drain.[3,4]

Negative oxide charge near the drain of an N-channel device causes the linear device threshold voltage to increase. In addition, the negative charge causes the gated surface breakdown to decrease. As the surface breakdown decreases with time, even more impact ionization occurs in the drain depletion region causing more "hot" electrons to be injected into the gate oxide region near the drain.

The mechanisms described above can continue until there is a sufficient linear threshold shift and/or a sufficient surface breakdown shift to cause the device to fail over some period of time. In the case of complementary IGFET devices, the turning-on of the bipolar source-to-substrate junction can trigger a potentially destructive SCR inherent in the structure.[5]

The phenomenon involved in describing the interactions between the IGFET current flow, the impact ionization, the parasitic bipolar, and the charge injection and oxide storage is very complex and dependent upon many device parameters. Since it is very important to quantize these effects so that reliability predictions can be made, a mathematical model has been created that uses a circuit simulation program for solution. The rest of this report will examine the pertinent physical mechanisms and generate the model. Results from the model will be given and discussed.

Physical Mechanisms and Modeling

Consider the N-channel IGFET structure of Fig. 2 which is biased in its saturation region of operation, i.e., $V_D > V_{DSAT}$, the linear-to-saturation drain crossover voltage. When the drain voltage is sufficiently large, impact ionization or multiplication will occur in the depletion region adjacent to the drain diffusion. Because of the electric field patterns present in the region, a fraction of the channel current (I_C) will hover near the surface while the remainder is drawn down into the bulk. Since the multiplication at the surface (M_S) is dependent upon the gate potential and the multiplication in the bulk (M_B) is not, two separate regions of multiplication should be considered.

The fraction of the total channel current that flows at the surface is proportional to the ratio of the vertical component of the field at the surface and the horizontal component of the field in the bulk. This fraction is referred to as the split ratio (S) as plotted in Fig. 3 and given by:

$$S = 1 - \{1 + 2.5(1-V) \exp [-2.5(1-V)]\}$$

where:

$$V = \frac{V_D - (V_G - V_{FB}) \frac{5 \times 10^{-6}}{T_{OX}}}{(V_D - V_S) \frac{6 \times 10^{-5}}{W_B}} \qquad (1)$$

and: V_D is the drain voltage in volts
V_G is the gate voltage in volts
T_{OX} is the oxide thickness in cm
V_S is the substrate voltage in volts
W_B is the bulk drain depletion width in cm
V_{FB} is the flatband voltage in volts.

Equation 1 was empirically determined from the measurable quantity M, the total effective multiplication in the drain region as given by:

$$M = M_S S + M_B (1 - S) \simeq \frac{I_D}{I_S} \qquad (2)$$

where:

$$M_S = \frac{1}{1 - \left(\frac{V_D - V_{DSAT}}{BV_S}\right)^n} \quad (3)$$

$$M_B = \frac{1}{1 - \left(\frac{V_D - V_S}{BV_B}\right)^n} \quad (4)$$

where: $V_{DSAT} = (V_G - V_T)$ is the drain voltage at the onset of saturation and
V_T is the threshold voltage in volts
BV_S is the breakdown voltage at the surface in volts
BV_B is the breakdown voltage in the bulk in volts
n is the Miller empirical breakdown constant
I_D is the drain current in amps
I_S is the source current in amps

BV_S is a function of gate voltage and is given by the empirical equation:[6]

$$BV_S = \frac{6E_C T_{OX} + (V_G - V_{FB})}{1 + \frac{3T_{OX}}{W_B}} \quad (5)$$

where: E_C is the critical field at breakdown in volts/cm

BV_B is a function of substrate concentration (N_A) and junction depth (d) as given by:[7]

$$BV_B = 60 \left(\frac{E_C}{1.1}\right)^{1.5} \left(\frac{N_A}{10^{16}}\right)^{-0.75} \left\{\left[\left(2 + \frac{d}{W_B}\right)\frac{d}{W_B}\right]^{0.5} - \frac{d}{W_B}\right\} \quad (6)$$

Likewise E_C is a function of N_A which is given by:[7]

$$E_C = 1640\ (N_A)^{.15} \quad (7)$$

Referring again to Fig. 2, one sees that holes are generated by the drain multiplication. These holes are accelerated by the drain and gate fields into the substrate region. Within this region there are three basic paths that they can pursue. Intially, path "a" is preferential because along this path the electric field is greatest. However, as the hole current increases due to an increased channel current and/or increased drain multiplication, a potential rise occurs across the substrate resistance (R_S). This potential rise forward biases the source-to-substrate junction, allowing some of the holes to find path "b" to be preferential.

Holes that travel along path "b" traverse the potential barrier that exists across the substrate-to-source junction immediately below the channel. Holes that emanate from the drain multiplication region could also travel along path "c" such that they cross the substrate-to-source junction even deeper in the bulk. Path "b", however, is a higher field path initially because the band bending due to the gate just below the channel lowers the potential barrier of the source junction in this region. It can be shown that the average amount of potential barrier lowering is given by:

$$\Delta V_b = \frac{\phi_F}{3} \quad (8)$$

where ϕ_F is the Fermi potential for the substrate region.

Equation 8 is derived from the surface band bending potential (ψ) diagram as shown in Fig. 4. Although the region where the intrinsic level (E_i) is below the Fermi level is N-type, a P-N source junction exists between the Fermi crossover point and the bottom of the surface depletion region (W_S) as well as in the bulk. Integrating between the crossover and W_S (X_i) yields the average potential given by Eq. 8. This value lowers the built-in junction voltage for that part of the source junction that is affected by the gate field.

As the hole current increases even more, the junction voltage along path "b" become sufficiently high such that some of the additional holes begin to flow along path "c". Since path "c" represents the section of the source junction that is below the channel depletion region, the junction properties along this path are normal; i.e., there is no barrier lowering due to the gate field.

As holes cross into the source region along paths "b" and "c" they cause the potential barriers to be lowered and electrons are injected from the source into the substrate region. The source electrons are accelerated by the drain field toward the drain multiplication region. If the distance between source and drain is small compared to an electron diffusion length, very few electrons will recombine with holes and the source electrons will in effect add to the channel electrons as they enter the drain multiplication region. The total drain current that subsequently flows in the saturation region can be given by:

$$I_D = M\frac{\gamma_m}{2}\frac{W}{L}(V_G - V_T)^2 + \frac{M\alpha}{1 - M\alpha}\left[(M-1)\frac{\gamma_m}{2}\frac{W}{L}(V_G - V_T)^2 - \frac{V_S}{R_S} + \frac{I_{DR}}{\alpha}\right] \quad (9)$$

where: γ_m is the IGFET gain parameter in mhos/v
α is the grounded base bipolar transistor gain
I_{DR} is the reverse current of the drain in amps.
W/L is the IGFET width to length ratio

The first term on the right hand side of Eq. 9 is the component of drain current due to multiplied IGFET channel current in the saturation region. The second term is the component of drain current due to the injected electrons from the source. Since these electrons obey bipolar transistor theory, the second term is also referred to as the parasitic bipolar component of current.

(Although the parasitic bipolar effect is more pronounced when the channel lengths are short, we have decided to use the simple IGFET equation[8] instead of short-channel IGFET equations in an attempt to keep the overall discussion simple. In cases where the short-channel IGFET effects are pronounced, then more complex forms for the IGFET channel current should be used.)

Within the brackets of the bipolar component of Eq. 9, the first term represents the hole current that is generated by the multiplication of the channel current and the second term is the hole current that leaves through the substrate contact along path "a" in Fig. 2. In effect, the quantities within the brackets constitute the net bipolar base current. The multiplication of the bipolar's electron current is

accounted for by the factor that multiplies the bracketed quantity. Note that as the denominator of the factor approaches zero, the value of the factor becomes very large. This effect can cause the bipolar component of current to far exceed the IGFET component of current as the drain voltage increases from low values to high values because of the multiplication's dependence upon drain voltage.

The aforementioned effect of the gate influenced junction barrier lowering can be accounted for in Eq. 9 by realizing that the substrate voltage, V_S, is related to the current through the low barrier region, I_L, and the current through the high barrier region, I_H, (paths "b" and "c", respectively, in Fig. 2) by the following equation:

$$V_S = \frac{kT}{q} \ln \frac{I_L}{I_{RL}} - \Delta V_b = \frac{kT}{q} \ln \frac{I_H}{I_{RH}} \qquad (10)$$

where: I_{RL} = reverse current for the low barrier region in amps
I_{RH} = reverse current for the high barrier region in amps

Taking into account the division in bipolar current between the high and low barrier regions of the source, the information in Eqs. 9 and 10 can be better modeled by the equivalent circuit of Fig. 5. In Fig. 5 the low barrier and high barrier bipolar effects have been modeled separately. Furthermore, since each bipolar device will experience different current levels, the proper current dependencies for each current gain can be modeled as shown in Fig. 5.

Because of the complexity and interdependencies inherent in a simultaneous solution of Eqs. 1-10, a very powerful technique for solving for the drain characteristics for the IGFET with parasitic bipolar current is to use a circuit simulation program. To accomplish this, the circuit of Fig. 5 was modeled with the ASTAP program.[9] (Linear region IGFET operation, although not explicitly discussed in this report, was also included in the model.)

The characteristics of the bipolar transistor that exists between the source and the drain was determined by a device modeling program that converts doping profiles into electrical information. From this program, junction parameters and current dependent gain information was gathered. These numbers were inserted into the ASTAP equivalent circuit for Fig. 5.

The effect that "hot" electron injection into the gate oxide region just above the drain depletion region has upon the IGFET device characteristics can be modeled by sensing the current and multiplication levels in the equivalent circuit and relating the number of injected electrons to these levels.[3] Once the injected oxide charge is determined, the linear region threshold voltage and the gated surface breakdown voltage is varied by changing the flatband voltage appropriately. From Ref. 3, the relationship between the current in the oxide due to electron trapping (J_t) and the current injected into the oxide (J_i) is given by:

$$J_t = N_T \sigma J_i \exp\left(\frac{-\sigma J_i t}{q}\right) \qquad (11)$$

where: N_T is the density of trapping states in the oxide
σ is the trapping cross-section in cm^2
t is duration of injection in seconds.
q is the charge of an electron

Discussion of Results

When the model for Fig. 5 is inserted into the equivalent circuit for an ASTAP curve tracer, a set of grounded source drain characteristics as shown in Fig. 6 results. Below a drain voltage of approximately 5 volts, there is no multiplication and the IGFET characteristics appear normal. Above 5 v with a gate voltage that is below the threshold voltage, a gated surface breakdown of 14 v is observed. As the gate voltage is increased above threshold to +3 v, a negative resistance can be seen at high drain voltages.

This "snapback" is caused by the denominator of the bipolar factor in Eq. 9. At low values of current, α is low and M has to be high for $M\alpha$ to approach 1 such that large bipolar currents will flow. However, as drain current increases, α increases and M can decrease to maintain $M\alpha = 1$. Since M is proportional to drain voltage, a negative resistance region is exhibited.

The region of drain characteristics, where $M\alpha = 1$ causes a set of vertical sustaining voltages, indicates that very high bipolar currents can flow. These high currents are limited by the external circuit. If the external load is small and the drain voltage is high, circuit latch-up and even device destruction could result. Note that the sustaining voltages occur well below either the surface or the bulk breakdown voltages. In effect, the bipolar effects significantly limit the useful voltage range of a short channel IGFET.

At higher gate voltages the sustaining voltages are higher because the surface breakdown increases with gate voltage according to Eq. 5. At even higher values of gate voltage the successive sustaining voltages tend to congregate more and more. This phenomenon is caused by the fact that the surface breakdown voltage exceeds the value for the bulk breakdown at large values of gate voltage for this example. Since the bulk breakdown now dominates and it is not a function of gate voltage, the change in sustaining voltages tends to be less sensitive to variations in gate voltage.

Figure 7 shows a somewhat typical plot of substrate current (I_{SX}) vs. gate voltage at a fixed value for drain voltage for the conditions given in Fig. 6.[10] An explanation for the shape is given as follows by referring to the split ratio of Eq. 1 and Fig. 2 with the knowledge that the surface breakdown voltage increases with gate voltage as shown in Eq. 5.

At low gate voltages most of the channel current is in the bulk where the multiplication is low because the bulk breakdown is high. As the gate voltage increases, the combination of more current being drawn to the surface and the lower surface breakdown causes the number of holes flowing in the substrate to increase rapidly. At some point, however, the surface breakdown increases and the amount of total multiplication begins to fall with increasing gate voltage for a given drain voltage. Even larger values of gate voltage draw more current to the surface, but also cause less and less multiplication; hence, the substrate current falls off.

The effect of "hot" electron injection can be seen in the drain characteristics of Fig. 8 which are for the same device as Fig. 6, except that the device has been stressed for the conditions shown. Note that the slope of the linear region characteristics is more shallow, indicating that the linear threshold voltage has increased. Below the onset of any multiplication

effects, the saturation region curves have not changed because "hot" electron storage in the oxide above the drain does not affect the saturation threshold voltage. (With pinch-off occurring before the point where the "hot" electron storage occurs, one would not expect any effect in the saturation region.)

Figure 8 also depicts a general decrease in the drain voltage at which the sustaining characteristics occur, especially for the lower gate voltages. This is because the "hot" electron injection has lowered the gated surface breakdown voltage by increasing the field at the surface.

The substrate current curve after the same stress conditions as in Fig. 8 is shown in Fig. 9. Note the general shift to the right because the linear threshold has increased. Also observe that the peak current has increased because the surface breakdown has decreased, causing the surface multiplication to increase.

Summary and Conclusions

In an attempt to completely account for the time dependent shift in linear threshold voltage and the lowering of surface breakdown voltage due to "hot" electron injection into the oxide above the drain region, a model that includes parasitic bipolar multiplication, as well as IGFET multiplication, has been presented.

Another reliability concern that limits the useful voltage range of an IGFET device when the bipolar effect is strong is the general lowering of the value of the sustaining voltages as "hot" electron injection progresses. All of these effects have been both qualitatively and quantitatively observed with experiments as well as with the model.

It should be concluded that because of the bipolar and "hot" electron effects in IGFETs, there are limits to the improvements in performance and density that one can expect. In particular, shortening the channel length and reducing the oxide thickness will tend to aggravate these problems. With the model we have presented, we believe an aid exists for determining the IGFET limits.

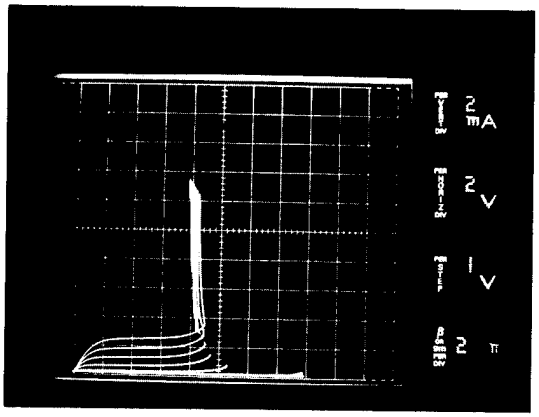

Fig. 1. Photo of a short channel IGFET depicting sustaining voltages characteristic of a parasitic bipolar.

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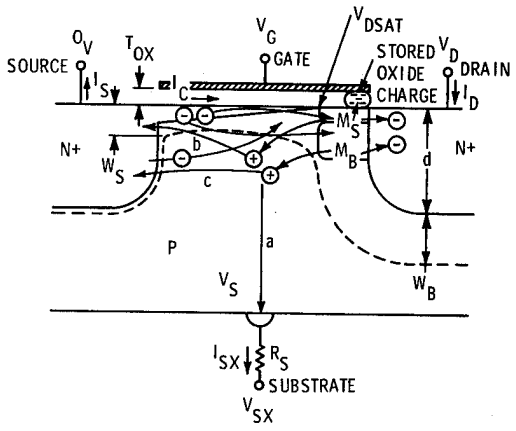


Fig. 2. Cross-section of an N-channel device showing multiplication and current paths.

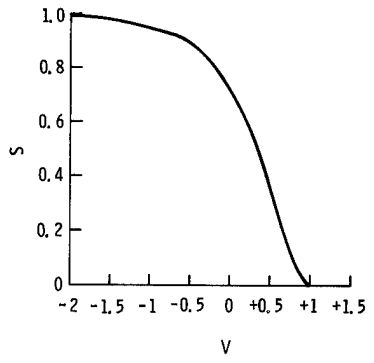


Fig. 3. Plot of the split ratio.

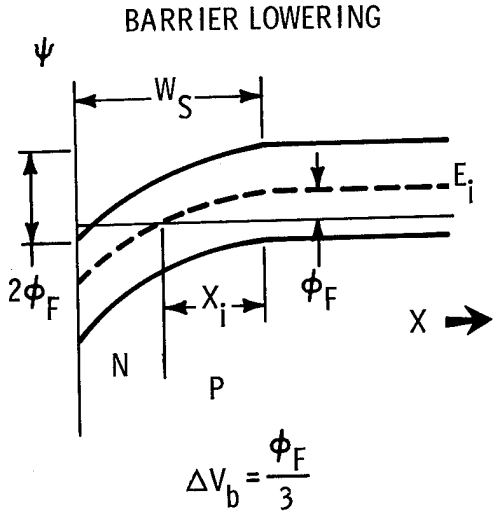


Fig. 4. Band bending in the vicinity of the source junction due to the gate field.

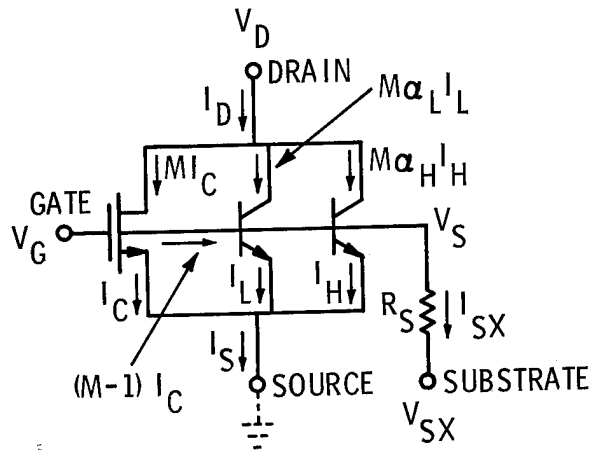
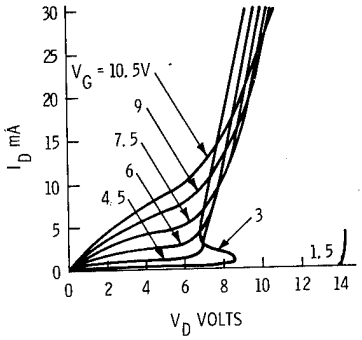


Fig. 5. An equivalent circuit for an IGFET illustrating the bipolar and multiplication effects.



$\frac{W}{L} = 10$ $B_{VB} = 20V$ $t = 0$

$N_A = 4 \times 10^{16}$ a/cc $V_T = 1.9V$ $R_S = 5K$

$L = 1 \times 10^{-4}$cm $n = 2$ $T = 25^{\circ}C$

$V_{SX} = 0$ $d = 1 \times 10^{-4}$cm

$\sigma = 4 \times 10^{-13}$cm^2

Fig. 6. Grounded drain characteristics for an IGFET with bipolar and multiplication effects.

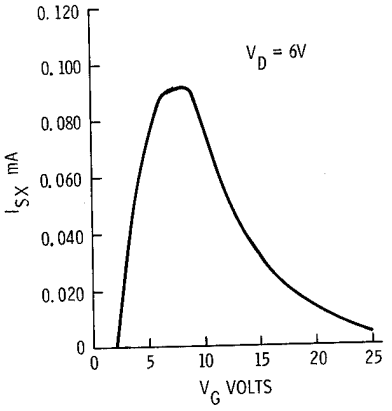
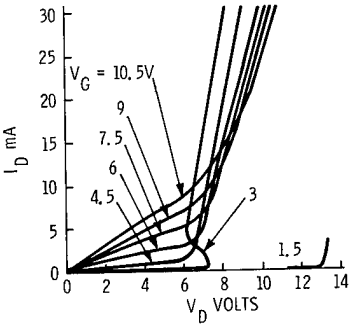


Fig. 7. Plot of substrate current vs gate voltage.



STRESS CONDITIONS:

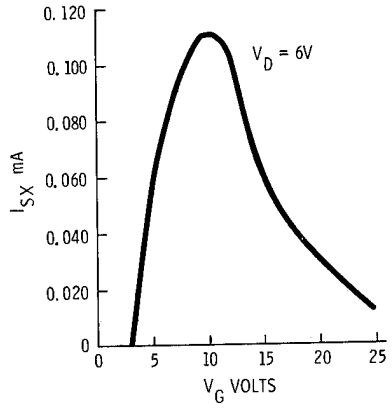
V_D = 5V

V_G = 12.5V

t = 100 hrs.

T = 25°C

Fig. 8. Drain characteristics that indicate the results of "hot" electron injection into the gate oxide.



STRESS CONDITIONS

V_D = 5V

V_G = 12.5V

t = 100 hr.

T = 25°C

Fig. 9. Substrate current after a "hot" electron stress.

A CMOS/SOS Reliability Study

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Summary

With over 100,000 hours of reliability testing of complementary metal oxide semiconductor devices built on sapphire substrates, a pattern of failure mechanisms has emerged. Not surprisingly, the well known gate oxide charge instabilities and gate oxide shorts commonly found in CMOS are also present in this latest technology innovation. The sapphire technology has added to these failure mechanisms several problems related to the input protective network and the so called back-channel leakage current stemming from the silicon-sapphire interface.

Introduction

In the Spring of 1975, RADC embarked on a preliminary reliability assessment of the CMOS/SOS technology in anticipation of future systems applications. This technology offers the distinct possibility of providing a high speed, low standby power, LSI packing density device for digital microcircuits. The intent of the program was to identify the principal failure mechanisms associated with CMOS/SOS and provide the manufacturers with information leading to corrective actions. Simultaneously, the effort would provide information needed to formulate a set of quality control and screen tests. In this first study our attention was directed toward identifying inherent stability problems with the chip and only nominal attention was paid to the package, wire and die bonds, lead frames, etc. It was assumed that failure analysis would be capable of separating effects of packaging on the chip. In this respect, the reliability evaluation is incomplete.

The vehicle chosen for the effort was a readily available dual complementary pair plus inverter similar to the CMOS/Bulk 4007 microcircuit. The simplicity of this device, wherein access to each P and N channel transistor was possible, permitted us to focus on fundamental parameters without being required to grapple with problems due to circuit complexity either in testing or failure analysis. A step stress program using temperature storage, static bias and parallel excitation tests was chosen to provide the maximum stability information at minimum program cost. Extensive electrical parameter data was taken throughout the program and parameter shifts monitored.

Device Characterization

The devices selected for study came from four different manufacturing processes. The approaches to building CMOS on Sapphire differed substantially among manufacturers. Samples from each process underwent extensive physical characterization so that a failure analysis base line could be established.

Common features of Manufacturers A, B and C were the use of aluminum flying lead wires, aluminum chip metallization and floating channel regions. Manufacturer A used a MOSFET pair for gate protection while Manufacturers B and C used zener diode stacks coupled with current limiting resistors. Manufacturer C used a self aligned gate (SAG) process to further minimize gate capacitance. The structural features as determined by profilometer measurements are shown in Table 1.

Manufacturer D's product had a double dielectric sandwich of Si_3N_4 and SiO_2 for the gate insulator. The input protection consisted of clamping diodes between gate and V_{SS} and V_{DD}. The channel region contained substrate tiedown thus eliminating the "kink" effect often found in sapphire MOST's. A gold flying lead wire made contact to an aluminum chip metallization.

Electrical Parameters

Electrical tests were performed initially and after each temperature stress step to provide data for electrical characterization, failure identification and parameter drift analysis. Included in the testing, accomplished on a Tektronix S-3260 Automatic Integrated Circuit Testing System were threshold voltage and inverter parameter measurements. Initial and final measurements were performed at -55°C, 25°C and 125°C; interim measurements were taken at room temperature.

While CMOS/SOS is commercially available, there was, at the time this study began, no firm electrical parameter specifications which could be used as the criteria for failure. A rather arbitrary criterion was chosen which was sufficiently generous that few users would argue that a part possessing these degraded electrical parameters would be desirable for systems applications. The failure criteria was chosen using Mil-M-38510/52A, the purchasing specification for the bulk CMOS 4000, as a guide. Typical incoming threshold voltage, leakage current and timing parameter measurements, along with our failure criteria are shown in Table 2. These parameters, defined in the specification, are those of a single device chosen at random.

It should be noted that all the measurements were taken with a V_{DD} to V_{SS} of 10 volts except for the N and P channel threshold voltages and the corresponding gain factors. The threshold voltages and gain factors were obtained at 3 volts V_{DD} by a least squares fit of the square root of drain current as a function of gate voltage in the current range from 10μA to 100μA. This choice of V_{DD} was made to avoid the introduction of the "kink effect" that appears at higher drain voltages in the transfer characteristics. The threshold voltages taken at 3 volts V_{DD} describe the true state of the insulator in the MOS transistor.

Step Stress Test Program

Three step stress tests were performed on each of the four CMOS/SOS technologies. Devices identified as failures during electrical parameter testing were removed from test for analysis. The stress tests are described as follows:

Static Bias Test

The first and perhaps most important was the static bias-temperature stress test. The test configuration is given in Figure 1. This test is designed to move mobile charges, if present, in the gate insulator and thereby alter the MOST transfer characteristics. Since we are dealing with both P and N channel transistors, it can be seen in Figure 1, that this test is really two separate stress tests. In one case an electric field is impressed across the P-channel gate insulator and in the other case the field is across the N-channel gate insulator. The nominal load placed at the output is adjusted so that the total current drawn by the parallel combination of the three stressed transistors is 9mA. The devices placed on static bias stress were subjected to successive 168 hour temperature steps of 75°C, 125°C and 200°C.

Dynamic Test

The purpose of the dynamic stress test is to exercise the technologies at elevated temperatures to accelerate any operationally induced changes. The dynamically stressed devices were also subjected to successive 168 hour temperature steps of 75°C, 125°C and 200°C. The schematic for the dynamic test is shown in Figure 2. The dynamic drive was a square pulse at 1MHz, 50% duty cycle with a V_{DD} to V_{SS} of 10 volts. The drive was confined to a single device of three serial inverters. The devices were driven in parallel through 1.25kΩ resistors, the last inverter being loaded with a 200kΩ resistor and 80pf capacitor. As in the static bias test, the oven was cooled to room temperature at the end of each stress step with full power and signal maintained.

Temperature Storage

A step stress temperature storage test was performed on ten units from each of the representative technologies. These devices were subjected to successive temperature steps of 125°C, 200°C and 300°C for 168 hours per step. This test is performed so that the effects of bias in the static bias and dynamic tests may be isolated from the effects of temperature.

Stress Testing Results

A summary of the program test results is given in Table 3. The table lists the number of devices that failed at each stress step and provides a description of those failures occurring at or below 125°C. A detailed discussion of the principal failure mechanisms is given in the Failure Analysis Section of this report. Included in the table is a second set of Manufacturer D's devices. The two sets were of the same processing approach, the major difference between the two being the brand of epoxy die attach used.

The threshold voltage stability of the P and N channel transistors which comprise CMOS is of major importance for reliability assessment. The observed changes in threshold voltage throughout the life of the stress test program for each of the manufacturers is given in Table 4. Care was taken to assure the changes seen were due to threshold voltage shifts and not simply the influence of excess leakage current in the measuring scheme. An example of the separation method is shown in Figure 3. In order to determine the threshold voltage of a given transistor, a number of drain to source current as a function of gate voltage measurements were made on the automatic tester. When these data are plotted as shown, the expected result is a straight line with the voltage intercept at zero current being defined as the threshold voltage. To generate a straight line from the measured data, the computer performed a least squares fit. Unfortunately, if there is an excessive gate voltage independent leakage current, the ideal straight line will show some curvature (See Figure 3). The computer includes this excess leakage current in its least squares fit computation resulting in a ficticious threshold voltage shift. So as not to be misled, computer plots of the data were manually scanned for curvature and the real threshold voltage shifts retrieved. Of course, this process also permitted the detection of excess leakage currents for failure analysis.

Failure Analysis

The results of detailed failure analysis provide the system contractor with a list of failure modes and mechanisms which can be associated with CMOS/SOS technology. Because each of the manufacturers involved used a different approach in building a CMOS/SOS device, an opportunity was presented to obtain a broad look at the technology from the failure mechanism standpoint. It is convenient to discuss the failure analysis according to manufacturer. In most cases the mechanisms observed in one process could have occurred readily, through lack of process control, with the other manufacturers. Where a failure mechanism is believed to be unique to a given process, it will be stated as such.

Since all stress testing was performed identically for each inverter, and it was possible to trace a given failure down to a single inverter, the individual manufacturer failure analysis summary tables include information for inverters as well as devices. In the tables, the sums of failures for all failure mechanisms do not necessarily equal the total number of failures because a given device or inverter may have had two or more failure mechanisms associated with it.

Manufacturer A

The failure analysis results for Manufacturer A are summarized in Table 5. As can be seen, the predominant modes of failure, gate to source and gate to drain shorts, were attributed to gate oxide breakdown. The appearance of the shorts (See Figure 4) ranged from obvious electrical overstresses, as exhibited in device 715, to barely perceptible oxide breakdowns (See device 714, metallization removed). Most of the shorts were of the device 714 category and had resistance values between 1kΩ and 4kΩ. Of the 29 gate oxide shorts observed, 25 occurred in the P-channel transistors.

Although several precautionary measures were taken during device handling, electrical testing and stress testing in an effort to prevent voltage transient damage to the parts, transient damage cannot be completely ruled out as a cause of the gate oxide shorting. All of the units in the testing program experienced similar conditions, but only the devices of Manufacturer A suffered gate oxide shorts. Oxides grown on SOS devices have been observed to break down at voltages up to 50 percent lower than their comparable counterparts on bulk silicon.[1] The Manufacturer A devices may have had significantly lower oxide breakdown voltages than the other manufacturers, and/or they may not have had adequate input protection. It would have been very difficult, if not impossible, to determine the gate oxide breakdown voltages on completed devices, and time did not permit an evaluation of the effectiveness of the various input protection schemes.

It is concluded that the gate oxide shorting mechanism is related to the thickness of the silcion islands. From Table 1 it can be seen that the Manufacturer A silicon island thickness is roughly half that of the other manufacturers. The silicon near the sapphire is known to be disordered.[2] Because the

epitaxial silicon layer of these devices was so thin, it is postulated that the silicon was disordered to some comparatively high degree. A gate oxide grown on this thin silicon is expected to be of poorer quality than were it grown on a thicker, more ordered epitaxial layer. It is believed that the probability of the occurrence of gate oxide pinholes is higher due to the thin silicon.

A second shorting mechanism is related to the growth of the gate oxide near the silicon-sapphire interface. At the island edge, the natural growth of the oxide normal to the silicon surface will tend to make the oxide at the base of the island slightly thinner.[3] In view of this factor and the fact that the silicon at the base of the island is highly disordered, it is believed that this area is a potential source of shorting problems. In the Manufacturer A devices, the gate oxide was the only insulation between the gate metal and the source and drain diffusions. Thus, the gate metal ran directly over the area of questionable oxide integrity. The other manufacturers, however, took various steps to better insulate the gate metal from the source and drain diffusions.

The mask misregistration failure mode is related to the gate oxide shorting mechanism. Figure 5 is an example of this mode. Note that the metallization line going to pin 6 partially overlaps a silicon island, rather than running between the islands. Here also, the gate oxide is the only insulation between the metal and the silicon. This particular situation presents the possibility of a short between pin 6 and pin 1. All of the misregistration failures were shorts from pin 6 to pin 1.

There was a small number of devices which failed because of drain to source leakage currents. Separating excess leakage current from threshold voltage shifts was discussed earlier. The source of this leakage current, (since it was only weakly affected by gate voltage) is probably in the silicon near the silicon-sapphire interface. Typical annealing results at 125°C for 24 hours, shown in Figure 6, indicate some recovery of the leakage with slight effect on threshold voltage. The exact origin of this leakage current, however, could not be defined.

Manufacturers B and C

Because the failure mechanisms of Manufacturers B and C were essentially identical, each mechanism described applies to both processes. Tables 6 and 7, respectively, give a summary of the failure analysis findings for each process as a function of the stress tests. Two modes of failure existed for these parts - excessive leakage current and threshold voltage shifts.

The leakage current, 10μA or more of inverter I_{SS}, was determined to have been caused by a problem associated with the two zener diode stacks used for input protection on these devices. Figure 7 shows the two protective diodes with metallization lines scribed out for isolation. The V-I characteristics for each of the diodes are also shown. Both zener stacks exhibited soft breakdown characteristics and in the case of D1 there was an abrupt increase in leakage above 10 volts. This behavior suggested surface charging effects. Baking the devices for 16 hours at 125°C with no bias did not appreciably alter the V-I characteristics. To isolate the location of the trapped charge, an experiment was performed in which the V-I characteristics were monitored as a function of glassivation removal. After 1 minute of glassivation etching, the V-I characteristics of D1 were essentially unchanged, as shown in Figure 8a. However, after 3 minutes of glassivation etch, which completely removed the glassivation the input networks regained their normal low leakage, abrupt breakdown characteristics as can be seen in Figure 8b. From this behavior it is concluded that an ionic specie migrated to the glassivation-silicon dioxide passivation interface. These charges, in turn, influenced the breakdown voltages of the diodes, causing excessive leakage current. The charges may have resided at the edge of the silicon island forming the diode rather than the surface. This input protection leakage current problem was in some cases quite severe and for those cases, glassivation removal did not completely eliminate the problem. Figure 9 is an example of this case.

Not all the leakage current observed was due to the input protective network. Examination of the transistor characteristics after isolation of the input protective network revealed a drain to source leakage current in both P and N channel transistors. Figure 10 shows the low current inverter transfer characteristics, and the N-channel reverse bias characteristics before and after a 24 hour, 125°C bake. As a result of the bake, both the leakage current and the drain to source breakdown voltage have improved significantly. The effect was undoubtedly caused by mobile charges, but whether they were located in the gate oxide or sapphire substrate could not be determined unequivocally since, as will be discussed, the threshold voltages shifted as well. It is believed, however, that the mobile charges causing the reduction in drain to source breakdown voltage were also responsible for the threshold voltage shifts, and hence, were present in the gate oxide.

Significant shifts in threshold voltage occurred for both Manufacturers B and C. The magnitude of those shifts is given in Table 4. As can be seen, except for slight positive P-channel shifts in the Manufacturer B devices, both the N-channel and P-channel transistor threshold voltages shifted negatively. It is surmised that these negative shifts are caused by mobile positive charge accumulation at the $Si-SiO_2$ interface. There is not enough data to develop an activation energy for an identification of the species. However, considering the high temperatures required for charge movement, sodium is a likely candidate.

Manufacturer D

A summary of the failure analysis for these devices is given in Table 8. In general, they performed well in our stress testing. As can be seen in the table, there were four modes of failure - excess leakage currents, threshold voltage shifts, bond lifts and $\sqrt{K_N}$ shifts. Of the four modes, excess leakage currents and threshold voltage shifts are considered to be the more significant.

There were 18 inverter leakage current and threshold voltage shift failures, 12 of which were associated with the N-channel transistors. The failure analysis showed the leakage current to be related to the transistors themselves and not the input protection diodes. The source of the leakage, in most cases, was shown to be the N-channel drain to substrate junction (See Figure 11). Leakage currents noticeably increased and the drain to substrate junction breakdown voltages decreased at the end of the 125°C step in the static and dynamic tests and at the end of the 200°C step in the temperature storage test. Both the leakage and breakdown voltage were improved as a result of a 24 hour bake at 125°C. In addition, it was possible to "turn off" the leakage by applying a negative potential from gate to source. This can be interpreted as positive charge in the gate insulator near the drain to substrate junction.

In an effort to determine the location of the charge, glassivation etching experiments, similar to those previously described, were conducted (see Figure 12). Removal of the glassivation improved the transistor drain to source breakdown characteristics. Therefore, it was concluded that the positive charge was located at the glassivation-gate insulator interface. The charge location may be associated with the physical step over the drain-substrate junction which runs the entire length of the channel, or it could be located where the drain and channel stop regions intersect.

Of the six remaining leakage and threshold failures, three (occurring on a single chip) were caused by severely degraded input protection networks. This part, which failed initial electrical testing, had the only three protective network failures.

There were three occurrences of P-channel transistor degradation. Two of the three were due to excessive leakage caused by a drain to source short. The characteristics of all other combinations - drain to substrate, source to substrate, gate to drain and gate to source - were good. In this case, removal of the glassivation had no effect on the leakage of these failures. Thermal liquid crystal analysis was performed, but failed to identify the location of the problem. The exact cause and location of the shorts were not identified.

Threshold voltage shifts were the second most prevalent failure mode. The thresholds of the Set II N-channel transistors moved away from depletion (positively), while those of the Set I N-channel transistors moved towards depletion (negatively). The thresholds of all P-channel transistors, which were turned on during stress testing, moved away from depletion (negatively), while the thresholds of those turned off moved slightly toward depletion. Negatively shifting thresholds are commonly due to mobile charge contamination. The fact that these shifts were not bake recoverable at 125°C does not rule out this possibility.

The increasing thresholds incurred in the second set of N-channels tested are considered to be due to avalanche injected charge which, after moving through the SiO_2, becomes trapped in the Si_3N_4. These thresholds were not bake recoverable at 125°C, but could be improved by the application of ultraviolet light with a corresponding electric field to drive electrons from the insulator to the silicon. The rate of improvement, however, was very slow and showed a saturating recovery rate indicating that these are deep traps. The reason for the opposite N-channel threshold shifts in both sets of parts was not determined.

During the initial electrical testing of the Set I devices, it was discovered that there was a shift in threshold voltage caused by the automatic tester. Since this product was built with a double dielectric, SiO_2 and Si_3N_4, there was concern of electrons being trapped at the dielectric interface by tunneling across the oxide layer. However, this concern was not supported by stress testing results. The tester induced shift came about as a result of the electrical test configuration and was likely due to the development of hot electrons from the reverse biased drain to substrate junction, with subsequent injection into the oxide and trapping at the dielectric interface. This effect, while not restricted to the double dielectric construction, is greatly enhanced by it and cannot be considered a common CMOS/SOS problem. A test configuration modification prevented any further tester induced threshold voltage shifts.

The last two modes of failure were ball bond lifts and $\sqrt{K_N}$ shifts. This manufacturer used a gold wire, aluminum chip metallization system which suffered purple plague (See Figure 13). This problem is regarded as external to the chip technology and, for this reason, will not be addressed here.

There were only two occurrences of a $\sqrt{K_N}$ value exceeding the failure criteria. In one case, the failure was not noted and the part recovered during the next stress step (125°C). It is known that a change in this parameter is related to a change in channel mobility. The reason for the change, however, was not determined.

Conclusion

In general, the CMOS/SOS devices tested in this program behaved reasonably well showing adequate stability at temperatures of 200°C for 168 hours. The main problems associated with CMOS are present in the CMOS/SOS technology with understandable changes in emphasis.

A primary cause of failure was attributed to the gate input protection network. A review of the four manufacturers shows that each had his particular approach to protecting the gate oxide from electrostatic discharge. It is known from pulse power testing that Manufacturer A's network offers inadequate protection against transients of 10 microseconds or less. Manufacturer D's network relies solely on forward diode conduction without a voltage dropping resistor and, while no pulse testing was performed on these devices, it is expected that the networks of Manufacturers B and C would prove to be superior from a static discharge standpoint. The principal source of difficulty with the B and C networks was the excess leakage current from the zener diodes. A device with normal substrate leakage currents of nanoamps could develop currents in the microamp and milliamp range due solely to the input protection network diodes. The leakage currents observed were traced to charges trapped at the silicon dioxide-glassivation interface. In addition to increasing leakage currents, the trapped charge altered the breakdown voltage of the protection diodes. It is evident that a standard input protection scheme needs development, where, in addition to the static discharge protection, long term stability is also considered.

As with any MOS device, threshold voltage shift failures due to mobile insulator charges were fairly common. There is no evidence suggesting that gate insulators in the SOS technology are inherently more sensitive to this failure mechanism. The support of this statement lies in the excellent threshold voltage stability observed in one of the products.

A third principal cause of failure was the appearance of gate oxide shorts. Data was presented suggesting that the oxide shorts are temperature related. One could conclude that the dielectric strength in at least one of the products degraded as a result of the accelerated aging experiments. It is considered unlikely that electrical overstress was involved in the shorting mechanism. The cause of the oxide shorts may be rooted in the condition of the silicon during oxide formation and/or the condition of the oxide at the base of the silicon island. Since the condition of the epitaxial silicon is related to its thickness on the sapphire, it is likely that thick silicon islands produce gate oxides less prone to the shorting problem.

A surprising and as yet unexplained observation is the relatively large threshold voltage shifts caused by the dynamic stress test in comparison to the

static bias test. A time varying signal on a CMOS gate should not have as large an effect on threshold voltage as a constant gate bias. Some consideration should be given to employing the dynamic stress test as the burn-in condition to obtain Class B reliability for the CMOS/SOS technology.

At the beginning of the program there was some concern that charge accumulation in the sapphire at the silicon-sapphire interface might create, as a result of ageing, a "back channel" effect. There was no evidence during the testing program that this was ever a problem with these devices.

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TABLE 1

Summary of Structural Features

	A	B	C	D
Total area of p and n channel devices (mil^2)	426	702	702	420
Active chip area (mil^2)	900	1400	1400	2700
Total chip area (mil^2)	2300	2500	2500	5400
Apparent channel length (μm)	7.5	7.5	6.5	5.0
n channel device channel width (μm)	1030.0	1024.0	1024.0	800.0
p channel device channel width (μm)	1290.0	1280.0	1280.0	1200.0
oxide for scratch protection (μm)	1.170	0.720	0.290	0.760
field oxide (μm)	none	none	0.270	0.610
metallization thickness (μm)	1.200	1.070	1.190	1.530
p channel device channel height (μm)	0.285	0.660	0.615	0.410
p channel device source and drain height (μm)	0.285	0.660	0.550	0.410
n channel device channel height (μm)	0.300	0.660	0.620	0.430
n channel device source and drain height (μm)	0.216	0.500	0.470	0.328
passunder height	none	0.480	0.480	0.275
silicon nitride gate passivation (μm)	none	none	none	0.080
thermal silicon dioxide gate passivation (μm)	0.100	0.100	0.100	0.009

TABLE 2

TYPICAL ELECTRICAL PARAMETERS

PARAMETER	FAILURE CRITERIA	A	B	C	D
V_{THN}	> 3.00 V < 0.00 V	1.24 V	1.79 V	1.951 V	1.315 V
V_{THP}	> 0.00 V < -4.0 V	-2.29 V	-2.26 V	-1.589 V	-2.057 V
I_{SSL}	> 10 μA	17.0 nA	30.8 nA	42.5 nA	38.1 nA
I_{SSH}	> 10 μA	11.3 nA	30.4 nA	21.7 nA	29.4 nA
I_{IL}	< -500 nA	-200 pA	-14.4 nA	-25.10 nA	-800 pA
I_{IH}	> 500 nA	2.4 nA	13.8 nA	3.2 nA	2.35 nA
T_{PHL}	> 100 ns	16.35 ns	16.8 ns	21.4 ns	8.2 ns
T_{PLH}	> 100 ns	21.30 ns	20.05 ns	24.2 ns	9.25 ns
T_{THL}	> 50 ns	17.30 ns	16.30 ns	18.25 ns	11.75 ns
T_{TLH}	> 50 ns	23.0 ns	20.49 ns	29.5 ns	25.5 ns

TABLE 3

FAILURE SUMMARY

STATIC N-CHANNEL BIAS

	TOTAL NO. DEVICES	INITIAL	75°C	125°C	200°C
MANUFACTURER A	7	0	0	1^B	3
MANUFACTURER B	8	0	0	0	8
MANUFACTURER C	7	0	0	0	6
MANUFACTURER D (SET I)	8	0	0	0	4
MANUFACTURER D (SET II)	5	0	-	0	1

STATIC P-CHANNEL BIAS

	TOTAL NO. DEVICES	INITIAL	75°C	125°C	200°C
MANUFACTURER A	8	2^A	0	0	5
MANUFACTURER B	7	0	0	0	7
MANUFACTURER C	8	0	0	0	8
MANUFACTURER D (SET I)	7	0	0	0	0

DYNAMIC STRESS

	TOTAL NO. DEVICES	INITIAL	75°C	125°C	200°C
MANUFACTURER A	10	0	1^A	0	9
MANUFACTURER B	10	0	0	3^B	7
MANUFACTURER C	10	0	0	0	9
MANUFACTURER D (SET I)	12	$2^{B,B}$	$2^{D,E,F}$	0	3
MANUFACTURER D (SET II)	9	0	-	0	4

TEMPERATURE STORAGE

	TOTAL NO. DEVICES	INITIAL	125°C	200°C	300°C
MANUFACTURER A	10	1^A	1^C	5	1
MANUFACTURER B	10	0	0	0	1
MANUFACTURER C	10	0	0	0	1
MANUFACTURER D (SET I)	10	0	0	1	3

A = MASK MISREGISTRATION C = OXIDE SHORT E = $\sqrt{K_N}$ SHIFT

B = LEAKAGE CURRENT D = THRESHOLD SHIFT F = BOND LIFT

TABLE 4

AVERAGE CHANGES IN THRESHOLD VOLTAGE

	A	B	C	D_{II}	D_{II}
N-CHANNEL STATIC BIAS (AFTER 200°C)					
$\overline{\Delta V_{THN}}$	0.02	-0.13	0.0	-0.31^A -0.29^B	0.21^A 0.54^B
σ	0.07	0.18	0.45	0.37^A 0.40^B	0.23^A 0.36^B
$\overline{\Delta V_{THP}}$	0.02	0.01	-0.45	0.06	0.10
σ	0.05	0.45	0.51	0.04	0.19
P-CHANNEL STATIC BIAS (AFTER 200°C)					
$\overline{\Delta V_{THN}}$	0.02	-0.06	-0.86	-0.04^A -0.06^B	
σ	0.04	0.04	0.76	0.02^A 0.02^B	NO DATA
$\overline{\Delta V_{THP}}$	-0.20	0.21	-1.92	-0.66	
σ	0.17	0.30	0.64	0.06	
DYNAMIC (AFTER 200°C)					
$\overline{\Delta V_{THN}}$	0.06	-1.38	-1.18	-0.45^A -0.57^B	-0.004^A 1.21^B
σ	0.02	0.27	0.42	0.28^A 0.36^B	0.16^A 1.20^B
$\overline{\Delta V_{THP}}$	-0.09	0.10	-0.01	-0.46	-0.39
σ	0.04	0.35	0.10	0.22	0.44
TEMPERATURE STORAGE (AFTER 300°C)					
$\overline{\Delta V_{THN}}$	0.002	-0.09	-0.59	-0.23^A -0.71^B	
σ	0.01	0.20	0.84	0.14^A 0.32^B	NO DATA
$\overline{\Delta V_{THP}}$	0.05	0.20	0.01	0.14	
σ	0.04	0.05	0.02	0.02	

A - TRANSISTOR N1 B - TRANSISTORS N2, N3

σ - STANDARD DEVIATION

ALL UNITS ARE VOLTS

TABLE 5

FAILURE SUMMARY - MANUFACTURER A

D = DEVICE I = INVERTER

STRESS TEST	TOTAL ON TEST		NO. FAILED		OXIDE SHORTS		MASK MISREGISTRATION		Iss LEAKAGE	
	D	I	D	I	D	I	D	I	D	I
STATIC N-CHANNEL BIAS	7	21	4	7	2	4	1	1	2	3
STATIC P-CHANNEL BIAS	8	24	7	9	4	6	4	4	0	0
DYNAMIC	10	30	10	13	8	10	3	3	0	0
TEMPERATURE STORAGE	10	30	8	13	6	9	2	2	2	2

TABLE 6

FAILURE SUMMARY - MANUFACTURER B

D = DEVICES I = INVERTERS

STRESS TEST	TOTAL		NO. FAILED		LEAKAGE		THRESHOLD SHIFT	
	D	I	D	I	D	I	D	I
STATIC N-CH BIAS	8	24	8	24	8	24	0	0
STATIC P-CH BIAS	7	21	7	21	7	21	0	0
DYNAMIC	10	30	10	30	10	24	5	11
TEMPERATURE STORAGE	10	30	1	1	1	1	0	0

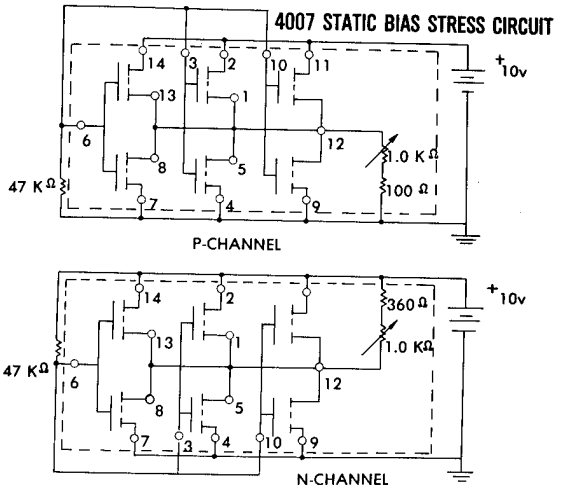


Figure 1. Static Bias Stress Circuit

TABLE 7

FAILURE SUMMARY - MANUFACTURER C

D = DEVICES I = INVERTERS

STRESS TEST	TOTAL		NO. FAILED		LEAKAGE		THRESHOLD SHIFT	
	D	I	D	I	D	I	D	I
STATIC N-CH BIAS	7	21	6	18	6	18	1	1
STATIC P-CH BIAS	8	24	8	24	8	24	6	11
DYNAMIC	10	30	9	27	9	27	1	1
TEMPERATURE STORAGE	10	30	1	3	0	0	1	3

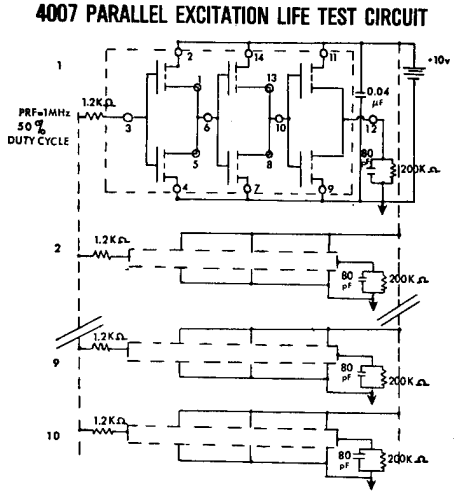


Figure 2. Dynamic Life Test Circuit

TABLE 8

FAILURE SUMMARY - MANUFACTURER D

D = DEVICES I = INVERTERS

SET I STRESS TEST	TOTAL		NO. FAILED		LEAKAGE		THRESHOLD SHIFT		BOND LIFT		$\sqrt{K_N}$ SHIFT	
	D	I	D	I	D	I	D	I	D	I	D	I
STATIC N-CH BIAS	8	24	4	6	2	2	0	0	2	4	0	0
STATIC P-CH BIAS	7	21	0	0	0	0	0	0	0	0	0	0
DYNAMIC	12	36	7	12	5	7	2	2	1	2	1	1
TEMPERATURE	10	30	4	6	1	1	0	0	3	5	0	0
SET II												
STATIC N-CH BIAS	5	15	1	1	1	1	0	0	0	0	0	0
DYNAMIC	9	27	5	9	0	0	4	5	2	3	1	1

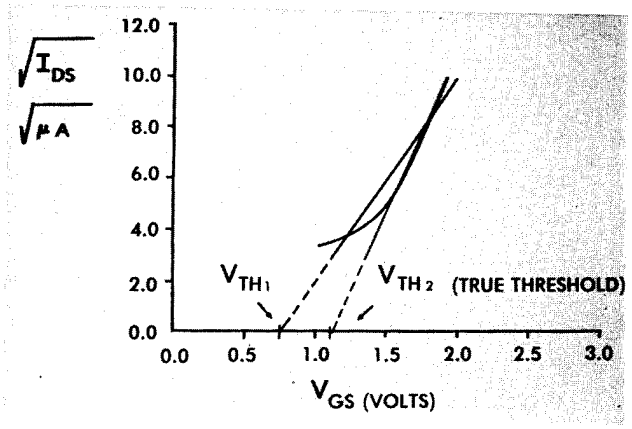
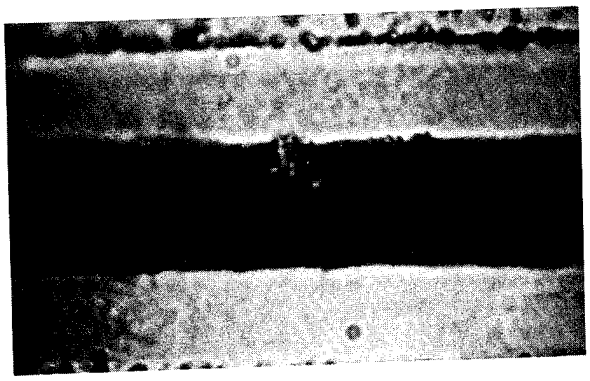
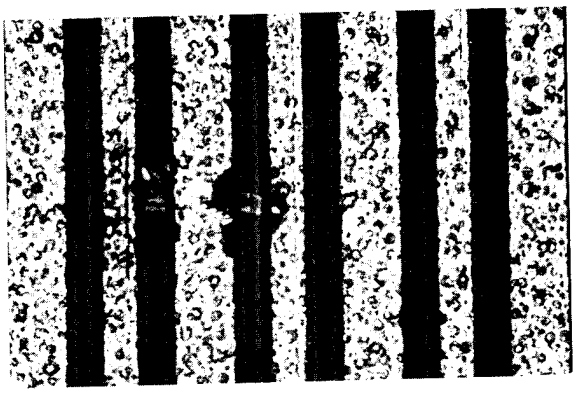


Figure 3. Leakage Current Separation Method

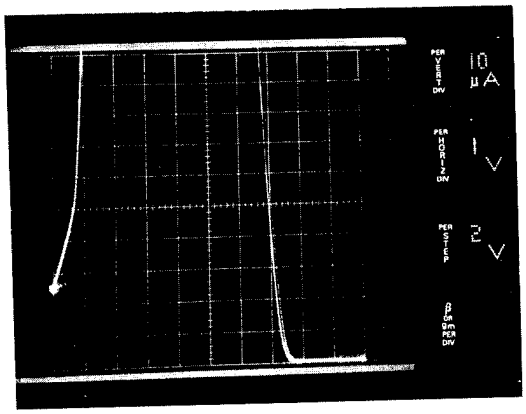


a. Device 714 - 2000X

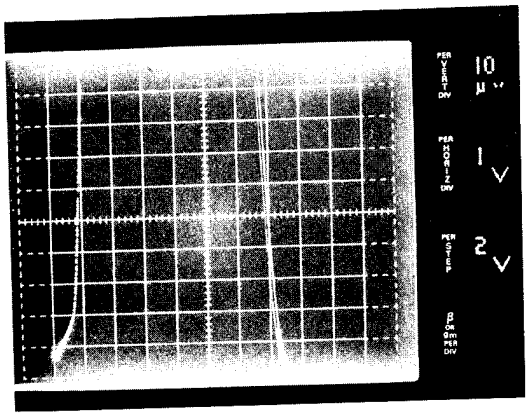


b. Device 715 - 830X

Figure 4. Gate Oxide Shorts - Manufacturer A



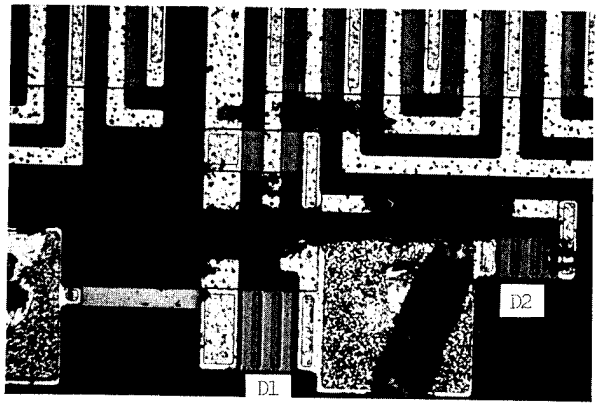
a. After 168 Hours, 200°C Static N-Channel Bias (Inverter 3)



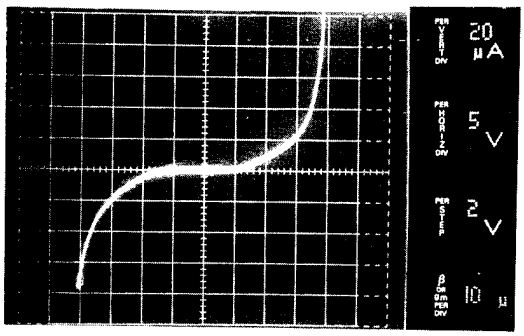
b. After 24 Hours, 125°C Bake (Inverter 3)

Figure 6. Bake Recoverable Drain to Source Leakage Failure - Manufacturer A

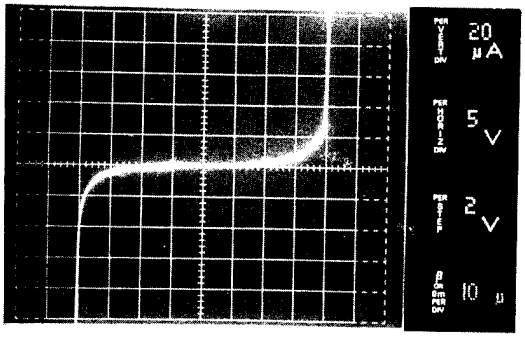
Figure 5. Typical Misregistration Failure - Manufacturer A



a. Protection Diodes D1, D2 Scribed Out - 280X

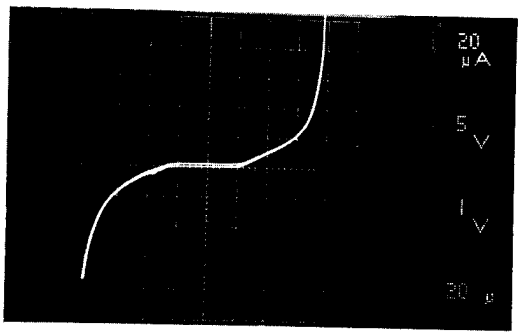


b. D1 V-I Characteristics

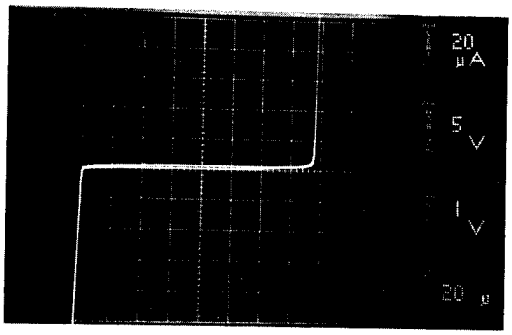


c. D2 V-I Characteristics

Figure 7. Input Protection Leakage Failure - Manufacturers B, C

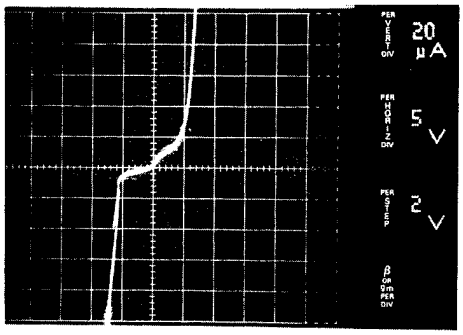


a. D1 V-I Characteristics After 1 Minute Siloxide Etch

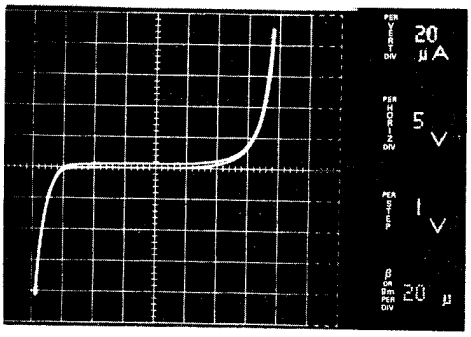


b. D1 V-I Characteristics After 3 Minutes Siloxide Etch

Figure 8. Effect of Input Protection Glassivation Removal - Manufacturers B, C

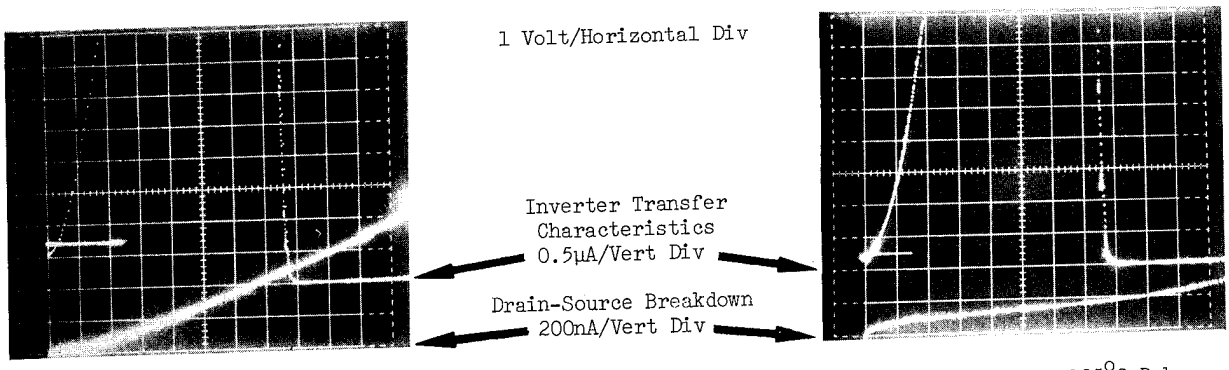


a. Before Glassivation Removal



b. After Glassivation Removal

Figure 9. Effect of Glassivation Removal on Severe Input Leakage Problems (Inverter 2 Gate to V_{DD} Protection Network)



a. After 168 Hours, 125°C Dynamic Stress

b. After 24 Hours, 125°C Bake

Figure 10. Drain to Source Leakage Current - Manufacturers B, C

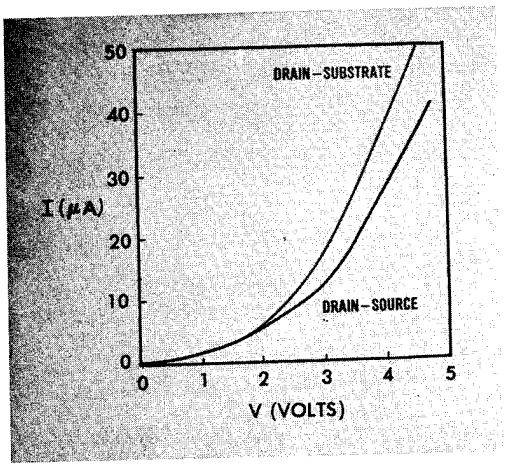


Figure 11. N-Channel Breakdown - Manufacturer D

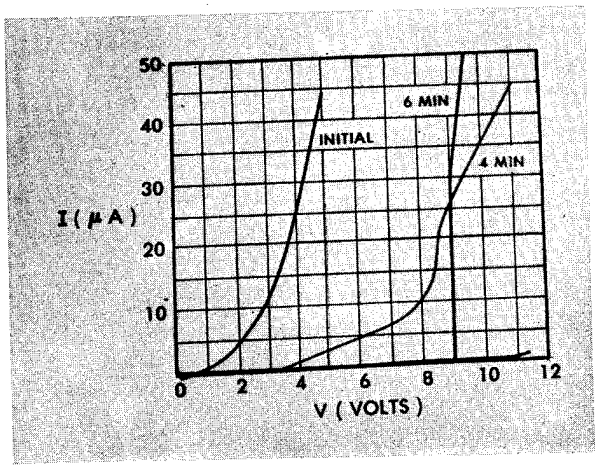
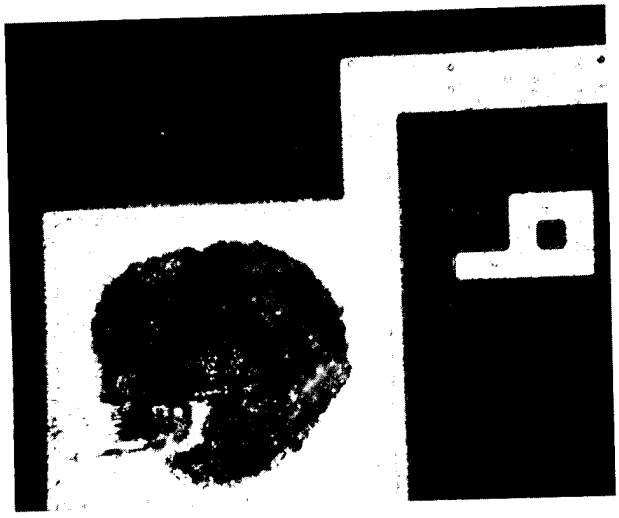
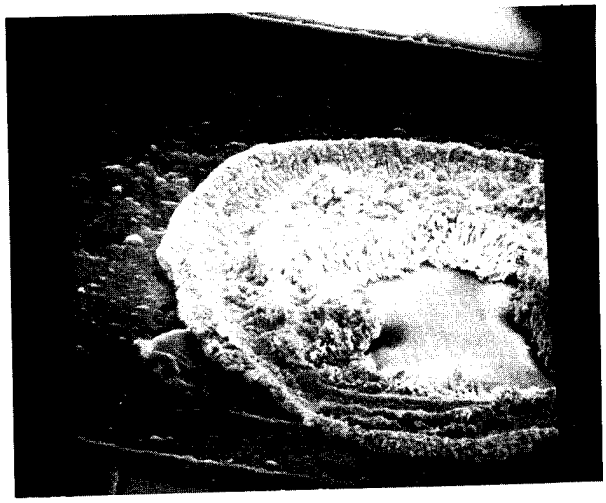


Figure 12. N-Channel Drain-Source Breakdown as a Function of Glassivation Etch Time - Manufacturer D



a. Optical - 500X



b. Scanning Electron Microscope - 1300X - 60°

Figure 13. Bond Degradation, Purple Plague - Manufacturer D

MICROSURGERY AS A TOOL IN THE ANALYSIS OF L.S.I. SILICON CHIPS

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Summary

The ability to open or bridge selected conductors on an L.S.I. chip opens up a wide range of analytical opportunities in the field of failure analysis, design debugging, and commercial device analysis. Simple methods of severing, repairing and interconnecting conductors in high density L.S.I. silicon chips are described. The design details of a simple precision tool serving the dual functions of microsurgery and subsequent electrical probing of components is discussed. Results obtained with the methods described on various commercial & custom L.S.I. circuits are presented.

Introduction

The information which can be extracted from a modern L.S.I. microcircuit when addressed through its external leads, is in general of a functional nature, relating to the design specification rather than to the physical structure or the particular technology used to fabricate that physical structure. There are many analytical situations where more specific information is needed than can be aquired by the black box approach. For example in failure analysis both the exact failure site and the physical cause of failure must be determined in order to feed back useful information for corrective action. All manufacturers need to maintain an awareness of how they stand relative to the competition and this involves detailed analysis of competitive devices and processes. Finally the device designer, faced with a prototype that does not function according to expectations, needs to identify the problems and be highly confident that he knows the right answers before undertaking an expensive and time consuming iteration through mask making & wafer processing.

In order to aquire this type of information it is necessary to work on devices which may comprise up to 20,000 components interconnected by metal and sealed under a layer of glass, in an area typically around 4 mm square. Interconnections are typically down to 6 to 8 microns wide with similar spacings; a contact hole is typically 6 X 6 microns, and a memory cell may be only 25 X 25 microns. What is required is to be able to carry out, on this scale, substantially the same functions as are commonly used in the diagnosis and repair of full sized circuits - isolation and testing of separate components, probing internal test points to measure or inject signals and remaking or changing connections.

The object of this paper is to demonstrate simple versatile techniques using low cost equipment to achieve some of these objectives and to demonstrate the extent to which silicon microcircuits can be controllably dissected without loss of valid operation of components, functional groups or total circuit function.

Apparatus

Cutting aluminum conductors by means of focussed laser energy has been described by Reese[1]. More recently Spano[2] has described an ultrasonic cutting tool for multilevel metallization systems. Ebel and Engelke[3] describe various methods including combined mechanical and etch cutting, but observe that the latter is inapplicable to high density situations. It will be demonstrated that for the very widely used single level aluminum system, use of a mechanical probe in combination with chemical etching is fast, simple and particularly effective in high packing density situations if the tool is suitably designed for this work.

The basic apparatus consists of a manually operated mechanical prober. Whilst there are many manual probers on the market they are primarily designed for gathering process control data and are not well suited to the needs of microsurgery. Table 1 lists the requirements of such a prober.

Table 1

Requirements of Microsurgery Tool

- Fully independent x, y, z motions.
- Freedom from vibration and backlash.
- High rigidity.
- Small tool tip radius.
- Metallurgical type microscope system giving erect image at greater than 200X.
- Rapid interchangeability of cheap or repairable tool tips.

These requirements may be well met by a prober made up from components normally found in any semiconductor laboratory. The prober shown in Fig. 1 consists of micrometer controlled XYZ micropositioners (supplied by Kulicks & Soffa Industries Inc. Horsham, Pa.) on which are mounted tool holders designed to operate under a metallurgical mono-objective microscope. The particular microscope shown is a made-up hybrid containing a roof prism in order to achieve an erect image. (This is highly desireable especially when two or more tool heads are used as in the electrical forming of contracts, to be described later). Long working distance objectives are advantageous but the tool holder shown in Fig. 2 is capable of working under a standard 20X metallurgical objective, which is approximately the maximum useable power due to restricted depth of field.

The tool holder shown is fabricated from a standard #19 hypodermic syringe modified to accomodate a tool retainer fabricated from a common sewing needle. The tool itself is an anodically pointed 5 mil. tungsten

wire. The kind of tip quality which can be readily achieved is shown in Fig. 3. Tool tips are very easily and quickly replaced although they may be repointed many times in situe.

With this type of micropositioner and the good visibility provided by a metallurgical type viewing system the tool may be positioned with adequate precision for any existing production circuit as is demonstrated in Fig. 4.

Cutting Aluminum Conductors

With the widespread use of protective glass, it is difficult to achieve a truly isolating mechanical cut through aluminum conductors since the glass lying on the oxide adjacent the metal is extremely adherent and forms side walls which retain a fillet of smeared metal. Mechanical removal of this metal requires forces great enough to cause damage to underlying silicon. Such methods are not compatible with the fine tooling and positional accuracy required in the dissection of high packing density devices.

The ease with which the glass is shattered when supported on soft yielding metal is utilized to sever conductors using chemical etching. The tungsten tool is merely brought to bear on the glass over the Al conductors with sufficient force to shatter the glass locally. No attempt is made to sever the conductor itself at this time. If the circuit is now immersed for a short time in an aluminum etchant (e.g., typically 30 sec. in H_3PO_4 at 80°C) the conductor is cut cleanly through at the desired point. Thus the protective glass is used as a mask for etch cutting the Al. conductor. This simple technique permits any number of cuts to be made rapidly & easily in the highest density metallization and with a high confidence level of achieving true open circuits without otherwise damaging the circuit (Fig. 5).

The glass is generally sufficiently good to avoid unintentional conductor cuts due to etch penetration through random defects. Attack of the aluminum through stress cracks, which are often found in the glass on commercial circuits, is generally too slow to result in accidential cuts if etch time is not excessive. However, the method may be applied successfully even with very poor quality glass if the whole device surface is precoated with a thin layer of etch resistant wax. This is easily achieved by flooding the device with a dilute solution of a suitable wax in a volatile solvent (e.g., Apiezon wax in trichlor ethylene) and allowing it to dry thoroughly. The wax effectively fills all unwanted holes in the glass but is scratched away locally with the tungsten tool when the glass is shattered. The same layer of wax also serves to protect bond pad metallization during etching.

Basically the same method can be used with glasses other than the conventional low temp. CVD SiO_2. Fig. 6 shows cuts made using the layer of silicon nitride found on some commercial devices. This layer is generally very much thinner than is common with CVD SiO_2 coatings (Approx. 2000Å versus 10,000 - 20,000Å). Such a layer has sometimes been found to be marginal in masking efficiency but performs adequately when backed up by a thin wax re-inforcement.

There is no reason why the same technique should not be applicable to other metallization and glass combinations provided that the metal is sufficiently thick and malleable to permit easy glass fracture and the glass is resistant to the appropriate metal etchant.

Poly-Silicon Conductors

With the continuing importance of the silicon gate technologies it may sometimes be desirable to cut poly-silicon conductors for analytical purposes. Unfortunately an equally simple procedure to the foregoing is not known since the poly-silicon layer does not have the necessary thickness and malleability to permit easy mechanical glass fracture. Poly-silicon conductors can be etch cut using the overlying CVD glass as a mask but the main difficulty of the method lies in obtaining a well defined aperture in what is often a multiple layer of thermal oxide & CVD glasses of widely varying phosphorous concentration and hence variable etch rate. However, fairly well defined cuts can be made using the following method. The device is masked with a thin transparent layer of wax as previously described. The wax is scratched away over the poly-silicon conductor using the tungsten tool and the glass etched through using dilute HF. This is a critical step which requires some experimentation in order to achieve complete glass and oxide removal from the surface of the poly-silicon without excessive undercut. Once exposed, the poly-silicon is severed by a brief etch in 10:6:1 HNO_3: CH_3COOH: HF. (Fig. 7).

Access to Interconnect Metallization

Another technique of great value to the device analyst and especially useful in design debugging is the establishment of contact to interconnect metallization for bringing out external connections to internal nodes and for bridging between conductors in order to modify the interconnection pattern.

It is neither necessary nor feasible to reproduce the quality or resolution of the original metallization since in general it is only required to establish contact to the metallization through a hole in the glass and to run a conductive path from there to some other point. Hence, only the placement of the hole requires precision commensurate with circuit dimensions; the conductive path can be relatively crude in geometry provided it does not result in unacceptable capacitance to other parts of the chip.

Satisfactory results have been achieved using silver loaded epoxy of the type commonly used for chip mounting in hybrid circuits. (e.g., EPO-TEK H20E, Epoxy Technology Inc., Watertown Mass.,). This material, which is a two part thixotropic paste, can be mixed in small quanitites on a microscope slide. It does not contain volatile solvents, therefore, has no tendancy to dry up on the applicator - a very important practical consideration which disqualifies air drying conductive materials. Holes in the glass are formed in the same manner as for conductor cutting except that after shattering, lateral motion of the tool is used to scrub away some of the material and expose the aluminum surface. The conductive paste is applied using a single hair mounted on a micropositioner as applicator. Typical tracks would average about 75 microns wide and be about 50 microns thick. With a specific resistivity of the cured epoxy of approx. 2 X 10-4 ohm. cm. such tracks are less than 1 ohm per mm. The epoxy is cured by heating the device for approx. 30 min. on a hot plate at 120°C. (Fig. 8).

The electrical quality of contacts to the aluminum is extremely variable until they have been "formed". "Forming" consists of passing a relatively heavy current for a short time which reduces resistance to 10 ohms or less. The current is passed between a probe contacting the cured epoxy and a second probe

contacting the aluminum conductor through another hole in the glass. The second probe is grounded in order to protect the device. A convenient current source is the collector supply of a transistor curve tracer which is also used to monitor the contact characteristic.

Applications

Useful applications of the foregoing techniques are to be found in many areas of device analysis. A few examples will be taken from failure analysis, design debugging and commercial device analysis.

A common device failure mode is high leakage or short circuit characteristics on one particular pin. In many L.S.I. devices an input pin may well be directly connected to thirty or more components. In such cases isolation of the components followed by electrical probing quickly identifies the defective component and focusses detailed analysis to determine the physics of failure. In devices showing quite similar degradation of terminal characteristics, failures have been located in bonding damage to oxide under bond pads, degraded diffused junctions in protection diodes and underpasses and perforated MOS gate oxides. None of these failures gave rise to externally visible defects, nor could they be localized by black box electrical testing.

A good example of how to maximize the information yield of a nominally unsuccessful developmental prototype run occurred recently on an experimental signal processing custom circuit of considerable novelty & complexity. The first devices assembled were only partially functional due to accidental reversal of two conductors in a densely packed area of the circuitry. This fault was rectified by Al cutting & reconnecting on several package chips, thereby giving the designers plug-in functional devices with which they were able to proceed with a performance analysis. This analysis revealed subtle anomalies in the characteristics of a multi-stage, high gain amplifier section. The amplifier was then brought out stage by stage and in various combinations. External pins were freed for the purpose by severing and clamping unused parts of the circuit and the designers were able to complete their analysis on plug-in testable amplifiers without the use of probes. Thus the next mask iteration, which included the correction of the original simple human error, was undertaken with assurance of the basic functionality of the circuit and included a local redesign based on a detailed electrical analysis.

Finally in commercial device analysis, the ability to make isolation cuts easily in the highest density circuits permits extensive characterization of the fabrication process and of many separate components.

Fig. 9 shows part of the memory cell array of a a commercially available 8 kilo-bit n-channel Programmable Read Only Memory. This device is representative of 'state of the art' packing density on production devices and includes interesting new storage technology. The cell area is approximately 25 X 25 microns (or 160,000 per sq. cm.). Fig. 10 shows part of a block of 160 cells which were isolated in a matter of a few minutes. All 160 devices were electrically probed and shown to be functional with highly uniform characteristics, illustrating the typically high yield in the isolating process even in high density situations. Fig. 11 shows typical electrical characteristics of the floating gate storage transistor and the effect of substrate bias which is of value in estimating the substrate resistivity. Fig. 12 shows the progressive threshold voltage shift as the floating gate is charged by successive voltage pulses through externally controlled resistors. Practically any device characteristic or electrical parameter can be extracted by appropriate isolation and probing.

Conclusions

Isolation and reconnection methods which are simple, perhaps to the point of obviousness, are shown to be valuable tools for the device analyst. Packing density in 'state of the production art' devices does not yet tax the full capability of these simple methods which are likely to be of value as long as optical imaging is used for device fabrication. Although the examples given are primarily from MOS technology the methods & principles are equally applicable to bipolar technology as well as to other metallization systems having suitable masking coatings.

References

(1) Reese W. E., Use of a Pulse Laser Technique in Failure Analysis, Proc. 11th Reliability Physics Symposium, P. 124-126, Apl. 1973.

(2) Spano J., LSI Failure Analysis . . . a better way, Quality, P. 14-16, Dec. 1975. See also this Symposium, Tutorial Session 1.

(3) Ebel G. H., and Engelke H. A., Failure analysis of Oxide Defects. Proc. 11th Reliability Physics Symposium P. 108-116. Apl. 1973.

Figure 1. Prober Suitable for Microsurgery.

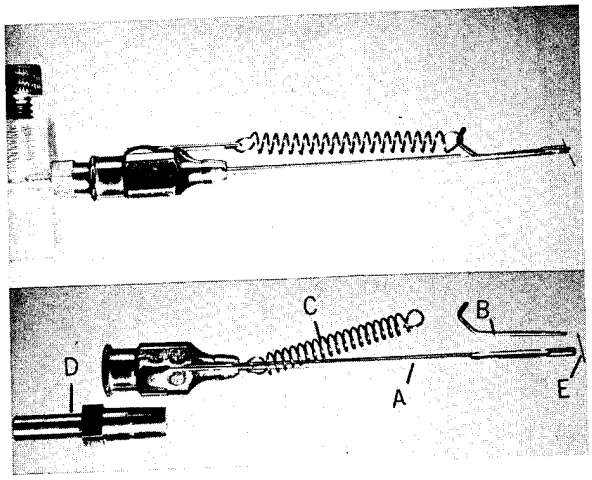

Figure 2. Tool Holder

(a) Hypodermic tube
(b) Retainer
(c) Retainer Spring
(d) Mounting Stub
(e) Tungsten Point

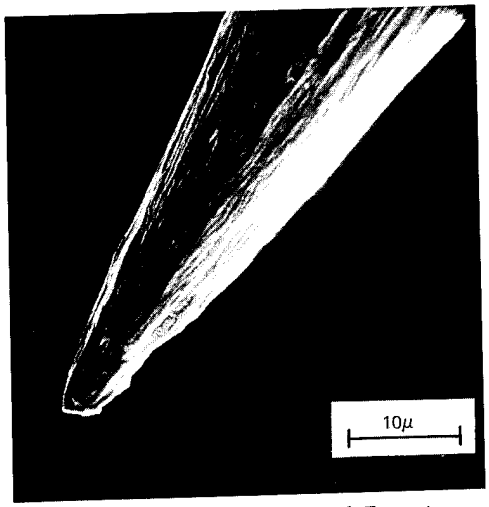

Figure 3. Anodically Formed Tungsten Point. S.E.M. X 1900

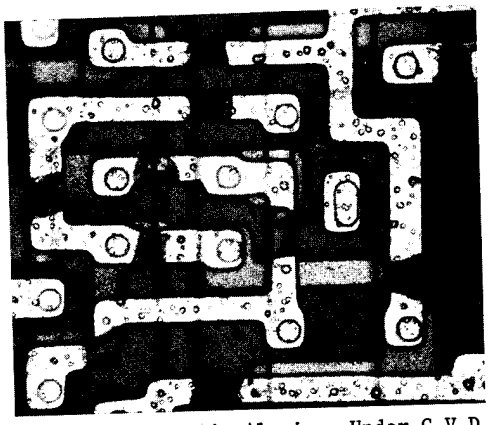

Figure 5. Cuts in Aluminum Under C.V.D. SiO_2.

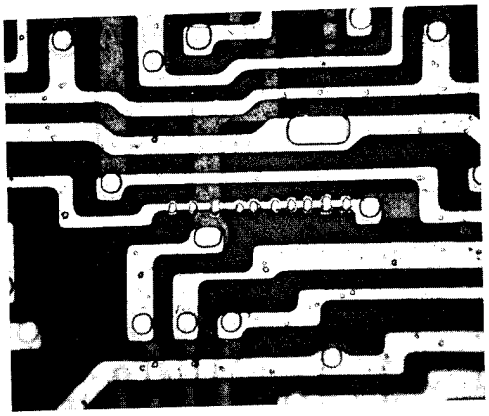

Figure 4. Probe Placement on a 2.5 Micron Aluminum Conductor.

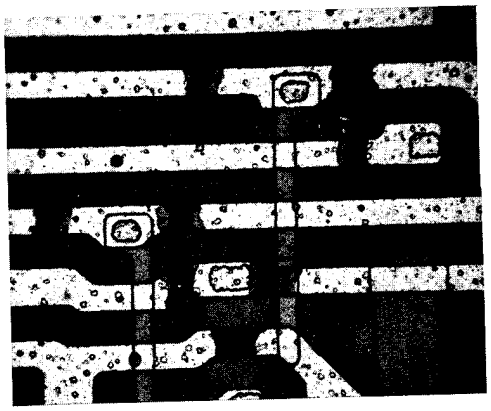

Figure 6. Cuts in Aluminum Under Si_3N_4.

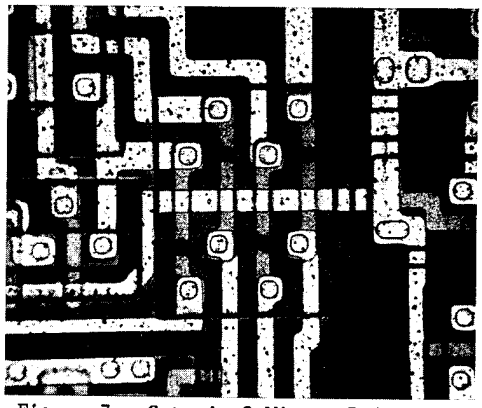

Figure 7. Cuts in 8 Micron Poly Si Conductors Using the Wax and CVD SiO_2 masked method described in the Text.

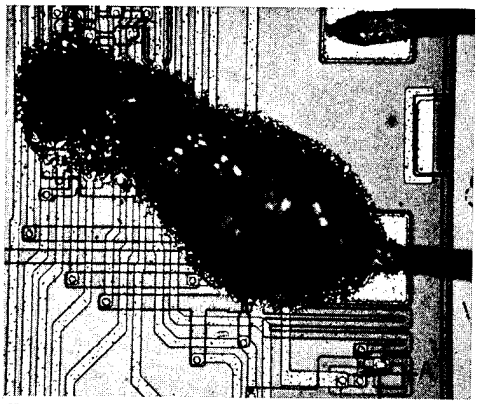

Figure 8. Conductive Epoxy Link From Amplifier Circuit to External Bond Pad. Note Cut Aluminum Link at A to Free Pad for this Use.

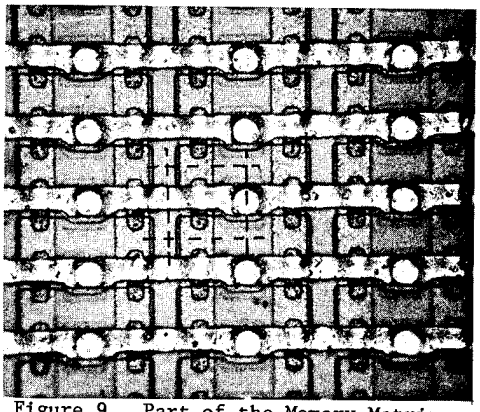

Figure 9. Part of the Memory Matrix of 8192 bit n-channel PROM. Single Cell (outlined) is Approx. 25 X 25 Microns.

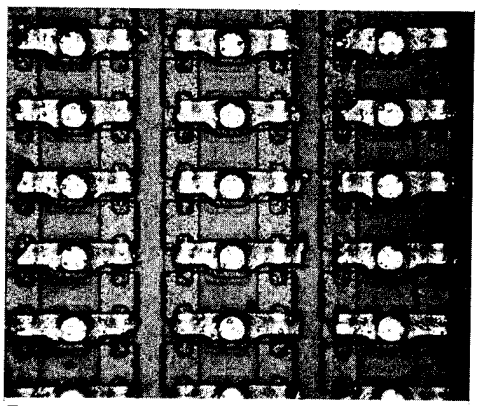

Figure 10. Same Matrix as Fig. 9. Part of Block of 160 Isolated Cells.

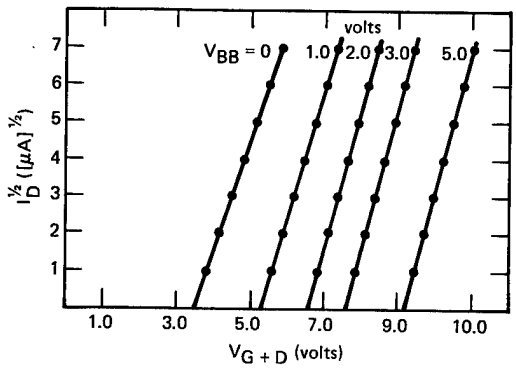

Figure 11. Turn-on Characteristic of One Cell of Fig. 10. (unprogrammed)

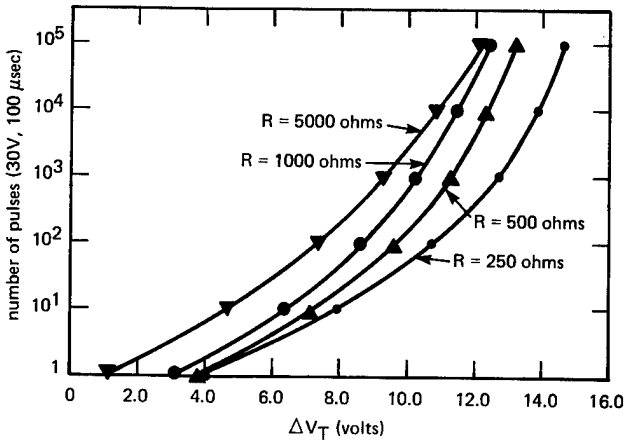

Figure 12. Change of V_T of PROM with Successive 30 V, 100 μ Sec Pulses through Various External Resistors.

HOT ELECTRON INDUCED DEGRADATION OF N-CHANNEL IGFETs

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Abstract

Under certain bias conditions, electrons flowing through the channel of an n-channel IGFET can be injected into the gate insulator. A fraction of the injected electrons is trapped in the dielectric, producing a shift in device operating characteristics. This phenomenon is minimized by proper device design. A model is described to predict long-term shifts from accelerated stress test data.

Introduction

The present trend in n-channel insulated gate field effect transistor (IGFET) device technology is to reduce the channel length (L), gate insulator thickness (t) and source-drain junction depth (X_j). At the same time, the channel doping (N_A) is increased to maintain sufficient threshold and punchthrough voltage. These design changes have created a new reliability exposure, a hot electron induced shift of the device current-voltage (I_D-V_G) characteristic.[1,2]

Each of the above design changes increases the electric field (E_{si}) in the channel. This larger field increases the probability that a channel electron gains enough kinetic energy to be injected into the gate insulator. A fraction of the injected electrons is trapped in the gate insulator near the drain and shifts the device's I_D-V_G curve.

This paper presents experimental data measured on a variety of n-channel IGFET device designs. The data illustrates the relationship between the hot electron induced I_D-V_G shift and the device parameters and stress conditions. An empirical model relates accelerated stress test data to long term shifts. The model is used to predict long term shifts for several device designs.

Description of the Phenomenon

Electrons flowing from source to drain gain kinetic energy from the electric field and lose energy via lattice and surface scattering. If the field becomes sufficiently large, the electrons can become hot enough to be injected via Schottky emission into the gate insulator. The barrier height between silicon and silicon dioxide is 3.1 eV. Equation 1 relates the electron temperature (T_e) and the silicon field, where k is the Boltzmann constant, λ is the electron mean free path and ε_r is the energy loss per optical phonon collision.

$$kT_e = \frac{(q\,E_{si}\,\lambda)^2}{3\,\varepsilon_r} \qquad (1)$$

For a given bias point, E_{si} increases as L, t or X_j is reduced or as N_A is increased. Alternately, E_{si} can be increased by raising the biases. The electric field in the channel is largest near the drain and, consequently, hot electron injection occurs mainly at the drain end of the channel. Charge trapped near the drain end of the channel produces a non-uniform spatial distribution of charge in the gate insulator. The trapped charge shifts the device's I_D-V_G characteristic and the size of the shift depends on the amount of trapped charge and the position of the charge with respect to the source and drain diffusions as well as the position relative to the gate electrode.

A quantitative relation between trapped charge and I_D-V_G shift has been developed using a two-dimensional IGFET model by Cottrell and Buturla.[3] Charge trapped near the drain shifts the I_D-V_G curve more if the device is operated in the reverse mode after stressing, that is, with source and drain interchanged. Figure 1 illustrates this effect. Since the shifted curve is not parallel to the original one we chose to measure the normal and reverse shifts, ΔV_{GN} and ΔV_{GR}, respectively, at I_D equal to 4 μa per mil of device width (W).

The hot electron induced I_D-V_G shift depends on the gate insulation trapping efficiency (TE)[2] and stress temperature (T) as well as E_{si}. A SiO_2-Si_3N_4 insulator has a higher TE than a SiO_2 or SiO_2 + PSG insulator. Raising the stress temperature lowers the electron mean free path and therefore reduces the injection probability. Note that $T_e \gg T$ for there to be appreciable hot electron injection. A measurable shift occurs at $T_e = 2400^{\circ}K$.

The shift also depends on stress time (τ). Equation 2 describes trapping for an insulator having a monoenergetic trap with cross-section σ and trap density N_t per cm^2.

$$N(\tau) = N_t\,(1 - e^{\frac{-\sigma J_i \tau}{q}}) \qquad (2)$$

$qN(\tau)$ is the total charge/cm^2 trapped after stress time τ and J_i is the current/cm^2 injected into the gate insulator.

Experimental Data

Aluminum gate n-channel IGFETs were fabricated on <100> boron doped substrates. These devices were made with a SiO_2, SiO_2 + PSG or SiO_2 + Si_3N_4 gate insulator. Silicon gate devices were made with a SiO_2 + Si_3N_4 gate dielectric. Source and drain regions were formed using a $POCl_3$ diffusion process.

Devices were stressed in the dark at $23^{\circ}C$ and at elevated temperature. The hot electron induced I_D-V_G shifts, ΔV_{GN} and ΔV_{GR}, were measured at I_D equals 4 μa x W and V_D = 8 volts.

Figure 2 illustrates the effect of the gate insulator TE on ΔV_{GR} for aluminum gate devices. The higher TE of the SiO_2 + Si_3N_4 insulators is clearly evident here. Estimated TEs are 0.0015, 0.4 and 0.8, respectively, for the SiO_2, 5/1 oxide/nitride and 1/1 oxide/nitride gate insulators.

ΔV_{GN} and ΔV_{GR} are compared in Fig. 3 for an Al gate device with a 5/1 oxide/nitride dielectric. ΔV_{GR} is much larger than ΔV_{GN} because the hot electrons trapped near the drain end of the channel have little effect on the normal mode saturation I_D-V_G curve.

Figure 4 shows the voltage dependence on ΔV_{GR} for an Al gate device with a SiO_2 gate insulator. ΔV_{GR} is plotted as a function of 1/L in Fig. 5 for a silicon

gate device which has a 1/1 oxide/nitride gate insulator. In Figs. 4 and 5 the increased shift is caused by increased Schottky emission according to equation 1.

Figure 6 contains the temperature dependence of ΔV_{GR} for an Al gate device. The shift is proportional to $T^{-4.8}$ between 296°K and 393°K. The reduced shift at higher temperature results fron increased lattice scattering and consequently a reduced probability for Schottky injection into the gate insulator.

Experimental data in Figs. 2 to 6 show ΔV_{GR} increases if the insulator TE or stress voltage are increased or if L or T are reduced. Tables 1 and 2 show that ΔV_{GR} increases when X_j is reduced or N_A is increased.

Model

An empirical model was developed to predict the hot electron induced I_D-V_G shift.[2] The model uses short terms accelerated stress test data to predict long term shifts. Parameters sensitivity is contained in the model. This methodology simplifies the model because a completely physical model requires accurate knowledge of the electric field distribution in the channel, the energy distribution of electrons incident on the Si-SiO_2 interface and gate insulator trapping properties.

Figure 7 compares experimental data and the model calculations for Al gate IGFETs with different gate dielectrics. Table 3 gives the gate insulator trapping properties for these devices. The model was used to calculate long term shifts for several device designs. Figures 8 to 10 contain the results. These figures show the voltage and channel length limitations imposed by the insulator trapping efficiency, source-drain junction depth and channel doping.

Summary

Hot electron trapping can occur at the drain end of the channel in an n-channel IGFET. The trapped charge shifts the I_D-V_G curve and the shift is larger when the device operates in the reverse mode. The magnitude of the shift depends on device parameters such as channel length, channel doping, source-drain junction depth and gate insulator trapping efficiency. The shift is also a function of stress voltage, stress time and chip temperature. The shift is increased by increasing channel doping, insulator trapping efficiency or bias and by reducing channel length, source-drain junction depth or chip temperature. A model incorporating accelerated stress test data was used to predict long term I_D-V_G shifts.

References

1. S. A. Abbas and R. C. Dockerty, Applied Physics Letters, 27, 147 (1975).

2. S. A. Abbas and R. C. Dockerty, Technical Digest of the 1975 IEEE IEDM, 35 (1975).

3. P. E. Cottrell and E. M. Buturla, Technical Digest of the 1975 IEEE IEDM, 51 (1975).

TABLE 1 V_{GR} for a L = 15 μ Device

X_j	ΔV_{GR} at t = 1 min
1.0 u	3500 mv
3.75	600 mv

TABLE 2 V_{GR} for a L = 15 μ Device

N_A	ΔV_{GR} at t = 2 min
8.0×10^{15} cm^{-3}	10 mv
2.6×10^{16}	800

TABLE 3 Gate Insulator Trapping Parameters

Gate	N_t	σ	T.E.
2% HCl SiO_2	5×10^{12} cm^{-2}	3×10^{-16} cm^2	0.0015
300/300 O/N	5	1.6×10^{-13}	0.8
500/100 O/N	5	8×10^{-14}	0.4

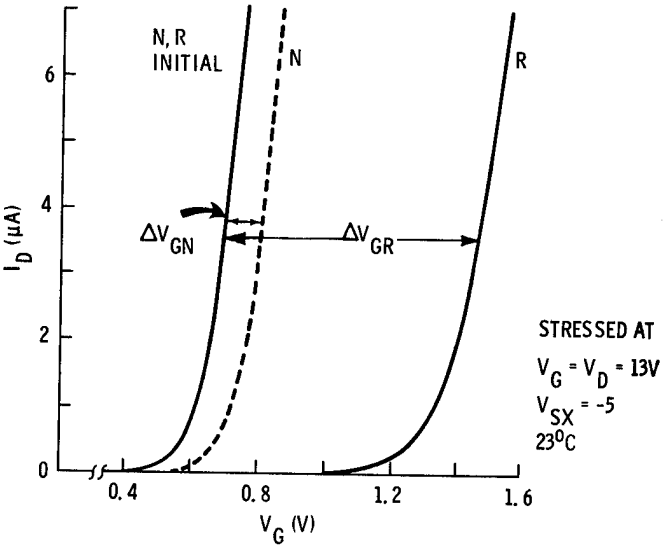

FIG. 1. $I_D - V_G$ SHIFT FOR A L = 2.6μ DEVICE.

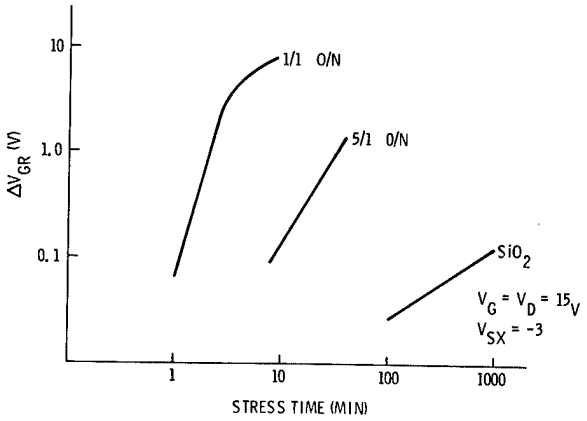

FIG. 2. SHIFT AT 23°C FOR L = 15μ.

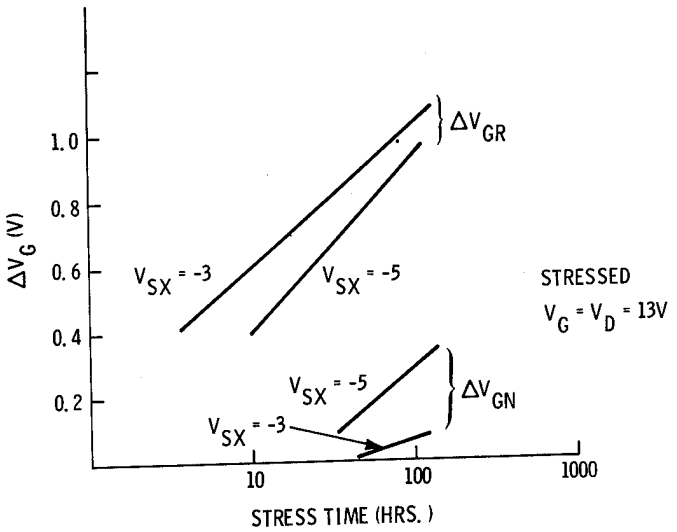

FIG. 3. SHIFTS AT 23°C FOR A L = 2.6μ DEVICE.

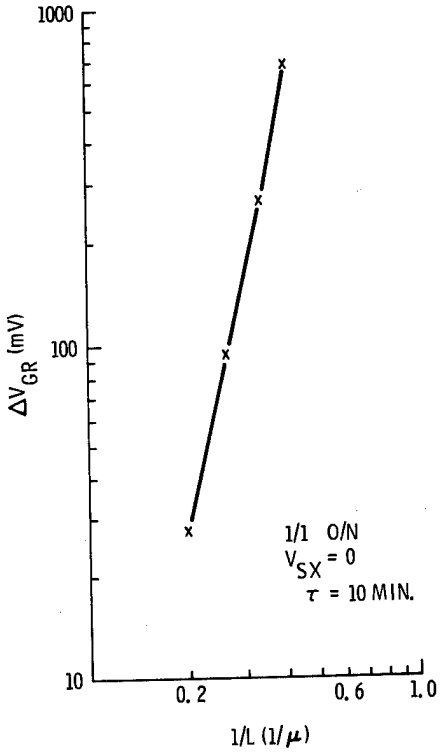

FIG. 5. ΔV_{GR} FOR $V_G = V_D$ = 12.5V.

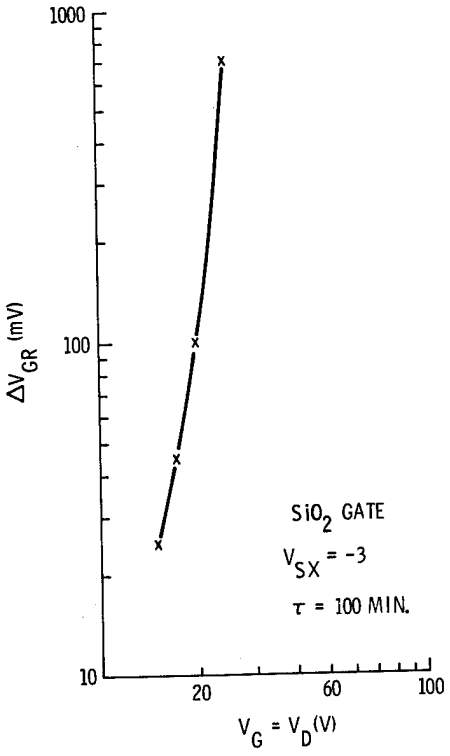

FIG. 4. ΔV_{GR} FOR A L = 15μ DEVICE.

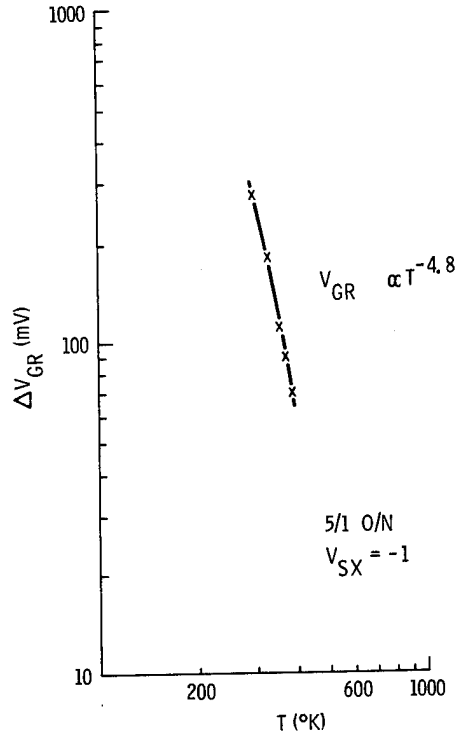

FIG. 6. ΔV_{GR} AT $V_G = V_D$ = 17 FOR A L = 2.6μ DEVICE.

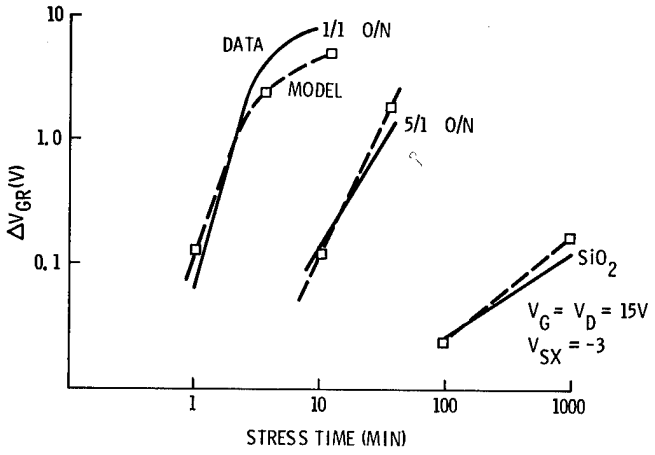

FIG. 7. DATA COMPARED WITH MODEL.

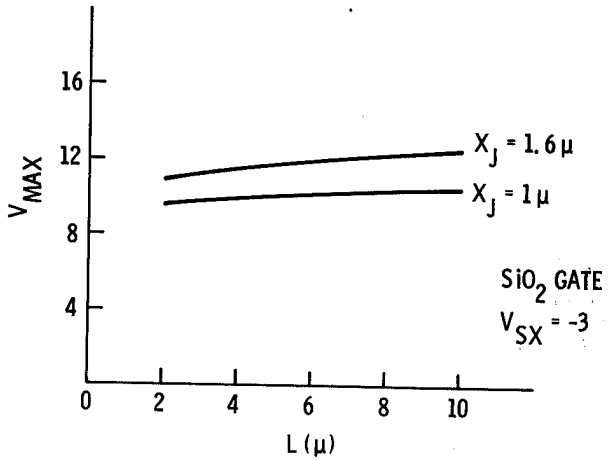

FIG. 9. $V_G = V_D$ FOR $\Delta V_{GR} = 500$ mV AND $\tau = 10^5$ HRS.

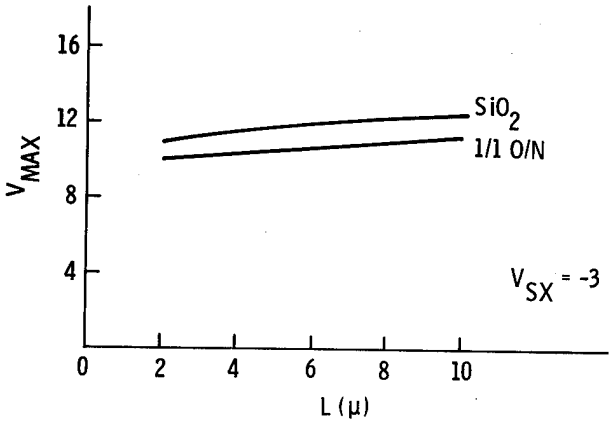

FIG. 8. $V_G = V_D$ FOR $\Delta V_{GR} = 500$ mV AND $\tau = 10^5$ HRS.

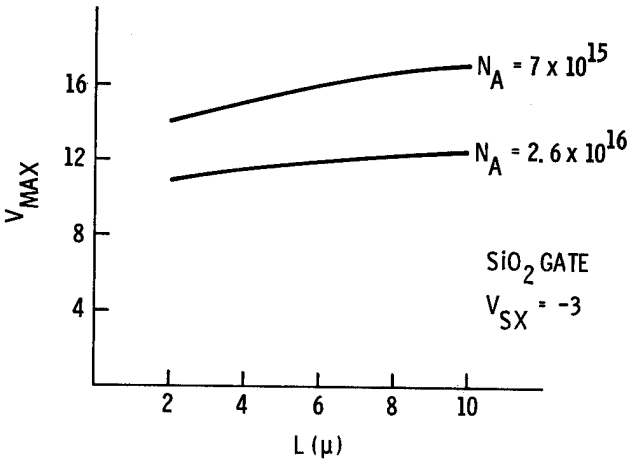

FIG. 10. $V_G = V_D$ FOR $\Delta V_{GR} = 500$ mV AND $\tau = 10^5$ HRS.

THE EFFECT OF IMPURITIES ON THE CORROSION OF ALUMINUM METALLIZATION

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Abstract

Surface impurities are an important factor that affects the reliability of semiconductor devices exposed to THB environments. Aluminum metallized specimens were intentionally contaminated with controlled amounts of Na, K, and Cl. Corrosion was observed at both the anode and cathode following THB tests. The corrosion rate was proportional to the log of the impurity concentration. A model is proposed to explain the observed corrosion processes.

Introduction

The failure of plastic-encapsulated semiconductor devices often results from the corrosion of the aluminum metallization. The failure rates for devices exposed to temperature, humidity and bias (THB) stresses depend upon the following factors: The specific encapsulating material, the package design, the metallization, the passivation glass, ionic contamination, the temperature, the relative humidity and the applied bias. The purpose of this paper is to study the effects of ionic contamination on the corrosion failure of semiconductor devices that have aluminum metallization.

There are several sources of impurities. First, the encapsulating material itself can be a source of impurities. A second source of impurities is external to the package, as in a salt spray test. Third, residual impurities may remain from wafer processing steps. Fourth, the plated lead frames or packages may be a source of impurities. Impurities that may become trapped during the plating process can be released during die-bonding or other high temperature operations. Any combination of these sources may contribute ions to the semiconductor surface. These sources of impurities have been reported by other investigators. It is well known that impurities, especially Na ions, affect the stability of semiconductor devices. References to these effects were given in a recent review of passivation coatings by Schnable, Kern and Comizzoli.[1] Lawson[2] has shown the failure rate of plastic encapsulated devices to be proportional to the impurity content of the encapsulant. The conductivities of the aqueous extracts from different molding compounds varied from 33 to 2500 μmho. In addition, the leakage current under a reverse-bias was proportional to the conductivity of the extract and also proportional to the square of the R.H. Lawson and Harrison[3] extended this work to show that the pH of the aqueous extracts ranged from 2.8 to 6.8. They also measured the impurity content of epoxies and found 0.18 to 4.35 microequivalents per gram of the alkali metals and 15 to 1150 ppm for the total halide content. They also measured the water permeation rates of the epoxies. Furthermore, it was also shown that the migration rate of Na^+ ions through epoxies was greatly accelerated with a 5 volt bias.

The effect of external salt environments has been studied by Hakim.[4] He showed that the log of the failure rate is proportional to the logarithm of the salt concentration. Also the failure rate was greater for unbiased transistors than for those with a 10 volt bias. In addition, silicone devices had a higher failure rate than epoxy-encapsulated transistors. Impurities will also cause the failure of gold-metallized circuits.[5,6] On these failed parts, Na, K, Hg, Cl, Br and I impurities were found. It was also demonstrated that no gold dendrites would form in pure water.[6] However, in 10^{-3} M solutions of NaCl, KBr and KI, the gold dendrites would easily grow. The degradation of Al wire bonds on silver-plated parts was attributed by Jellison[7] to high humidity and Cl impurities.

Brandewie, Eisenberg and Meyer[8] showed that Al can corrode inside hermetic packages that contain both Cl and H_2O. In THB tests, the applied bias causes a surface current to flow. Koelmans[9] measured the surface conductivity in humid atmospheres and showed that the adsorbed water follows the shape of the BET adsorption isotherms. He also noted that Na may increase the pH of the cathode and Cl may cause non-sealing oxides at the anode. Peck and Zierdt[10] gave the failure rates for transistors exposed to THB tests and noted that impurities may alter these failure rates. It is evident from these papers that impurities are present and they affect the reliability of semiconductor devices.

This paper is divided into five sections. Following the introduction, the experimental procedures are described. The experimental results are then given along with the application of these results to device failures. The final discussion section contains a model for the observed corrosion results.

Experimental Procedure

The specimens were made by evaporating 1 μm of Al onto 0.5 μm of thermally oxidized Si wafers. The Al stripes were made using conventional photoresist techniques. The scribed die were eutectically bonded to gold plated TO-5 headers. Contacts to the stripes were made by the ultrasonic bonding of 1 mil Al-1% Si wire. Following the wire bonding, the samples were rinsed in flowing 18 megohm distilled water and then quickly dried. Controlled amounts of impurities were added by immersing the samples in salt solutions with concentrations of 1, 10, or 100 ppm. The corrosion tests consisted of exposure to temperature, humidity and bias conditions (THB). A Blu-M humidity chamber was used for all the tests and it controlled the temperature to $\pm$ 0.5°C and the R.H. to $\pm$ 1%. A constant bias of 20 volts between adjacent stripes was used for all the tests. Control specimens were also run on each test. One control specimen was biased but was not contaminated. A second control was contaminated but was not biased. The third control was neither contaminated nor biased during the tests. Following the exposure to the THB conditions for fixed time intervals, the extent of the corrosion was evaluated optically. A ranking of 0 to 10 was given, where 0 indicated no corrosion and 10 indicates corrosion of the entire stripe and bonding pad area. Therefore, the corrosion measurements only give a qualitative indication of the corrosion rate.

Experimental Results

Samples that were doped with NaCl and KCl were exposed to the THB conditions. Representative pictures of corroded specimens are shown in Figures 1 and 2. Figure 1 shows corroded specimens after 185 hours at 85/85/20 that were contaminated with 1, 10, and 100 ppm

NaCl. The wider stripe in all the pictures was the cathode. The corrosion rate increases with increasing amounts of NaCl. In addition, the corrosion is more intense on the cathode than on the anode. Corrosion is occurring on the stripes as well as on the bonding pads. The corrosion characteristics for specimens doped with KCl (Fig. 2) show similar trends. Higher concentrations of impurities cause more corrosion and the cathodic corrosion is more intense than the anodic corrosion. Corrosion begins at the grain boundaries for the Al films. The grain boundaries have been clearly delineated (Fig. 3) on specimens doped with 100 ppm NaCl.

The average corrosion intensity for 20 specimens is plotted as a function of log C in Figure 4, where C is the NaCl concentration. The corrosion intensity increases linearly with the log C for both the anodic and cathodic corrosion. The cathodic corrosion, indicated by circles in Fig. 4, was always larger than the anodic corrosion (plus signs). Similar results were observed for KCl contaminated specimens (Fig. 5). The corrosion intensity increased linearly with log C and the cathodic corrosion was more intense than the anodic corrosion. Differences in the measured corrosion rates were observed between NaCl and KCl impurities. The reason for these differences is not known. However, only the solutions' concentrations were known. A quantitative measurement of the actual surface concentration was not made. The differences in the corrosion rates may be caused by differences in the actual impurity concentrations.

The corrosion rate was measured at 85, 50, and 25°C at a constant 85% R.H. Figure 6 shows the cathodic corrosion rates for KCl doped specimens as a function of log C. The corrosion rate was linearly dependent upon the log C for all temperatures. The qualitative results in these experiments prevent the calculation of an activation energy for the corrosion process. A similar decrease in the corrosion rate was observed for specimens contaminated with NaCl. Both the anodic and cathodic corrosion rates decrease at lower temperatures.

The effects of cations and anions on the corrosion process can be considered independent of one another. This was examined experimentally by contaminating specimens with 1, 10 and 100 ppm K_2CO_3 solutions. After exposure to 85/85/20 conditions, the resulting corrosion was observed mainly at the cathode. The cathodic corrosion intensity was the same as shown in Fig. 5, for KCl contamination. Some anodic corrosion was seen at the 100 ppm level, however, the resulting corrosion was half that observed for KCl contaminated specimens. At 1 and 10 ppm K_2CO_3, no anodic corrosion was observed, in contrast with the KCl and NaCl contamination (Figs. 4 and 5).

Three types of control specimens were exposed to the temperature-humidity conditions. Negligible corrosion under any condition was observed on the first set of control specimens that were neither biased nor contaminated. A second set of control specimens was biased but not intentionally contaminated. A slight amount of corrosion was detected on some of these specimens. However the observed intensity was less than one on the corrosion scale. A third type of control specimen was not biased but was contaminated with salts. With 100 ppm NaCl or KCl some corrosion could be observed. In contrast, no corrosion was observed with 1 and 10 ppm impurities for the unbiased, contaminated control specimen. Therefore, the observed Al corrosion is caused by the applied bias, the high humidity and the impurities.

The surface impurities that affect corrosion can be identified and measured using Auger spectroscopy. The Auger spectra of specimens following die bonding and wire bonding frequently indicated the presence of K, Na and Cl. After rinsing with 18 megohm water, none of these elements could be seen in the Auger spectra. The effects of these impurities on the Al corrosion can be seen after THB tests. Three sets of test specimens with 1 μm of 1.0 wt. pct. P-doped passivation glass were prepared. The first set was not rinsed. The second set was rinsed for 15 minutes in 18 megohm water. The third set was rinsed for 3 hours in 18 megohm water. These specimens were then exposed to 85/85/20 for 330 hours. The resulting corrosion intensities are as follows: No rinse gave an intensity of 3.7, a 15 minute rinse gave an intensity of 0.1, a three hour rinse gave an intensity of 0.2. Hence, the surface impurities on the unrinsed specimens cause extensive corrosion. In addition, the 15 minute water rinse is sufficient to remove these detectable ions. The differences between the 15 minute and 3 hour rinses are not significant.

Both the impurities and the moisture must have access to the metallization, in order to observe corrosion failures. Generally the Al is covered with P-doped passivation glass. The removal of the glass from the bonding pad areas exposes the underlying Al. The effects of impurities on specimens with passivation glass were also studied. Passivated specimens were doped with NaCl and exposed to THB environments. The CVD passivation glass contained 1.0 wt. pct. P, in order to minimize the effects of the phosphorus. When the step coverage was good (1 m glass over 1 m Al), corrosion was observed on the bonding pads, as shown in Figure 8. With occasional pinholes or cracks, Al corrosion may be observed along the stripes (Fig. 9).

Electrophoretic effects were observed by the use of Auger spectroscopy. That is, the chlorine ions were observed to accumulate at the anode and the sodium and potassium ions accumulated at the cathode. Test samples were doped with 100, 10, and 1 ppm NaCl. Before the THB tests, the Na and Cl were detected only on the 100 ppm doped specimens. However, following the THB tests, both Na and Cl could be detected on all the test samples. The Cl peak was approximately twice as high on the positively-biased Al as on the negatively-biased Al. Similarily, the Na peaks were higher on the negatively-biased Al stripe than on the positively-biased ones. Since the impurities are mobile on the surface, they will migrate to the electrodes and affect the corrosion processes.

Discussion

Impurities affect the aluminum corrosion processes in several different ways. These processes will now be discussed in terms of the available information on the corrosion of bulk aluminum. The effects of the chloride ion on the corrosion of Al have been studied on bulk Al using potentiostatic and galvanostatic techniques. The corrosion rate of Al is controlled by the surface oxide film. Foroulis and Thubrikar[11] studied the corrosion of preanodized Al in KCl solutions. They observed an induction time τ before the pitting of the surface was observed and corrosion could start. The induction time depended upon the Cl^- concentration, followed an Arrhenius dependence upon temperature, was independent of pH, and increased with oxide thickness. The proposed corrosion mechanism consisted of the adsorption of Cl^- on the surface followed by the local dissolution of the $Al(OH)_3$. The oxide dissolution follows the equation[11]

$$Al(OH)_3 + Cl^- \longrightarrow Al(OH)_2\,Cl + OH^-. \quad (1)$$

Once the surface oxide is dissolved, the underlying Al reacts with the Cl^- by the equation[12,13]

$$Al + 4Cl^- \longrightarrow Al(Cl)_4^- + 3\,e^- \qquad (2)$$

The $Al(Cl)_4^-$ will then react with the available water by the reaction

$$2AlCl_4^- + 6\,H_2O \longrightarrow 2Al(OH)_3 + 6H^+ + 8Cl^-. \qquad (3)$$

This process liberates the Cl^- ion, which is then available to continue the corrosion process via equations 1 and 2. By this corrosion process, a small amount of Cl^- can be recycled to cause a large amount of corrosion. An additional reaction that occurs at the positive terminal is the anodization of the aluminum. The anodization process will grow a thicker oxide on the Al surface. Anodization is a competing reaction with the chloride-ion aided dissolution of the surface oxide (Eq. 1). This anodization process causes the anodic corrosion rate to be slower than the cathodic corrosion rate (Figs. 4 and 5).

This chloride ion corrosion model can account for the THB failures of encapsulated semiconductors. The encapsulating materials absorb water vapor both through the bulk material and along the lead frame--packaging material interface.[3] Relative humidities above 50% will provide several monolayers[8] of adsorbed water at the surface of the die. This adsorbed water is the solution through which the impurities can migrate, both across the surface and through the molding compounds. The applied bias provides the driving force for the corrosion process and also attracts the impurities to the electrodes. The chloride ions cause the aluminum hydroxide to dissolve and then attack the underlying Al. The resulting corrosion product is $Al(OH)_3$. The volume expansion[19] of the $Al(OH)_3$ is sufficient to crack the passivation glass and allows the corrosion to continue.

Extensive cathodic corrosion of the aluminum was observed with the K and Na impurities. Cathodic corrosion was also observed as the failure mode for P-doped SiO_2 glass corrosion.[14] The most common cathodic reactions are the reduction of hydrogen

$$2H^+ + 2e^- \longrightarrow H_2, \qquad (4)$$

and the reduction of oxygen

$$O_2 + 2H_2O + 4e^- \longrightarrow 4\,(OH)^- \qquad (5)$$

Since Al is amphoteric, it can corrode in either acidic or basic solutions.[15] In acid solutions Al corrodes according to the equations[16]

$$\begin{aligned} 2Al + 6H^+ &\longrightarrow 2Al^{+3} + 3H_2, \\ 2Al^{+3} + 3H_2O &\longrightarrow 2Al(OH)_3 + 6H^+. \end{aligned} \qquad (6)$$

In corresponding equations for basic solutions are[16]

$$\begin{aligned} Al + 3(OH)^- &\longrightarrow Al(OH)_3 + 3e^- \\ O_2 + H_2O + 4e^- &\longrightarrow 4(OH)^-. \end{aligned} \qquad (7)$$

The presence of sodium or potassium ions affect the reactions at the cathode. These ions migrate to the cathode and the following sequential reactions can occur:[17]

$$\begin{aligned} Na^+ e^- &\longrightarrow Na \\ Na + H_2O &\longrightarrow Na^+ + OH^- + H \end{aligned} \qquad (8)$$

By these reactions, the solution pH at the cathode will increase.[18] This increase in the pH will cause the Al to corrode according to Equation 7. Therefore, the presence of Na and K ions cause an increase in the pH at the cathode, which causes the Al to corrode. The corrosion product is $Al(OH)_3$, as is the product at the anode.

The potential E at which the corrosion process is occurring is proportional to log I, where I is the corrosion current. The measured corrosion intensities appear to be related to the corrosion potentials. The experimental results showed that the corrosion rate increased linearly with the log of the impurity concentration. This logarithmic dependence is consistant with the results predicted from the Nernst equation.[17]

$$E = E^o - RT \ln \frac{(\text{products})}{(\text{reactants})} \qquad (9)$$

where E^o is the standard potential, R the gas constant and T is the temperature. Applying the Nernst equation to the corrosion of Al by the chloride ion (Eq. 2) yields the following expression at 25°C,

$$E = E^o - 0.0197 \log(AlCl_4^-) + 0.0787 \log(Cl^-), \qquad (10)$$

where the standard emf E^o is approximately 2.64 volts.[21] The effect of the chloride ion concentration on the driving force for Eq. 2 can be seen as follows. Assuming $(AlCl_4^-) = 10^{-6}$ and $(Cl^-) = 10^{-6}$, Eq. 10 reduces to $\Delta E = -0.354$. With a higher chloride ion concentration of $(Cl) = 10^{-3}$, Equation 10 becomes $\Delta E = -0.118$. Therefore, with a positive E^o of 2.64 volts,[21] the driving force for the corrosion of Al by chloride ions increases with increasing chloride ion concentration.

There are several variables that will influence the corrosion rate for real devices. First, the thickness of the Al_2O_3 on the Al metal will affect the corrosion rate as given in Eq. 1. The oxide thickness depends upon the time and temperatures that the device has seen.[20] The distance between the anode and cathode will also influence the corrosion rate. This distance can be as large as the bond pad separation or as small as the distance between adjacent metal runs. The applied voltage is another variable. Higher voltages will give rise to faster corrosion rates. However, the corrosion potentials are not directly given by the applied voltage.

The surface material between the electrodes is another variable. It has been shown that the amount of phosphorus in the passivation glass is linearly related to the failure rate.[13] This surface will affect the amount of adsorbed water and the resulting surface conductivity.

The impurities that are important for corrosion are those that are on the surface and are mobile in the presence of adsorbed water. The source of the impurities determines the ease with which they can be controlled and the resulting corrosion prevented. The removal of surface ions by rinsing will eliminate impurities except those that are introduced by the packaging operation. Therefore, the impurity corrosion rate will depend upon the transport of impurities from other sources rather than depending only on the arrival of water at the die surface.

The effects of impurities on the corrosion of Al metallization can be summarized as follows:

1. Chloride ions migrate to the anode and cause anodic corrosion.
2. Sodium and potassium migrate to the cathode, raise the local pH and cause cathodic corrosion.
3. The cathodic corrosion rate is larger than the anodic corrosion rate.
4. The corrosion rate is proportional to the log (C).

5. The corrosion rate increases with increasing temperature.

6. The impurity corrosion can be minimized by careful cleaning procedures.

Acknowledgments

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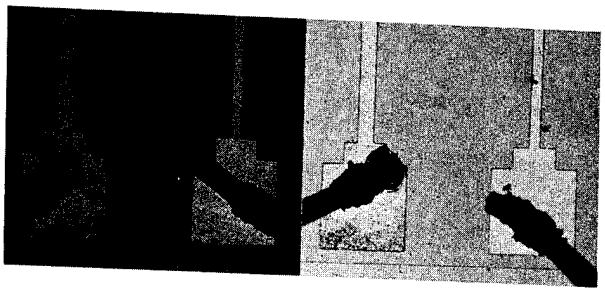
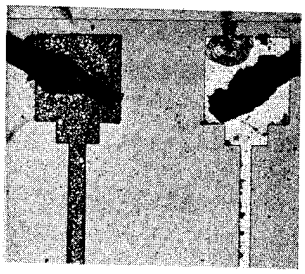
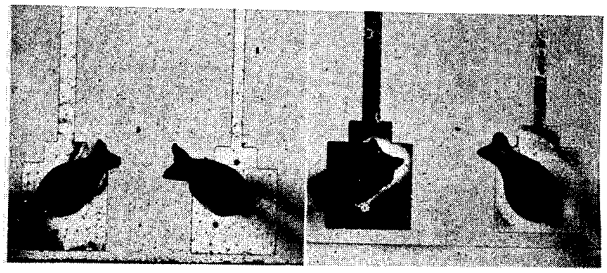


A. 1 ppm NaCl B. 10 ppm NaCl

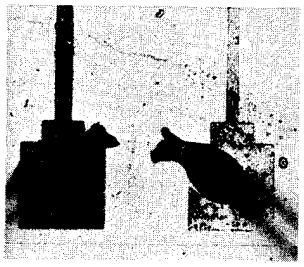


C. 100 ppm NaCl

Figure 1. Aluminum Corrosion for Samples Doped With NaCl After 185 Hours at 85/85/20. Cathode is the Wider Stripe.



A. 1 ppm KCl B. 10 ppm KCl



C. 100 ppm KCl

Figure 2. Aluminum Corrosion for Samples Doped With KCl After 133 Hours at 85/85/20. Cathode is the Wider Stripe.

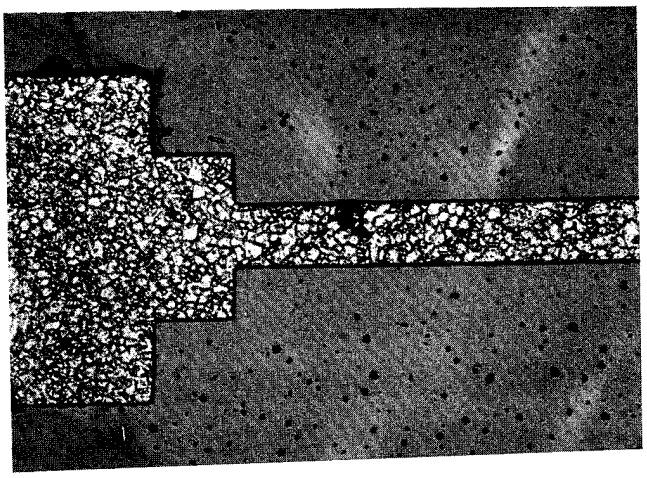


Figure 3. Grain Boundary Corrosion for Samples Doped With 100 ppm NaCl After 185 Hours at 85/85/20. Cathode Stripe (Fig. 1).

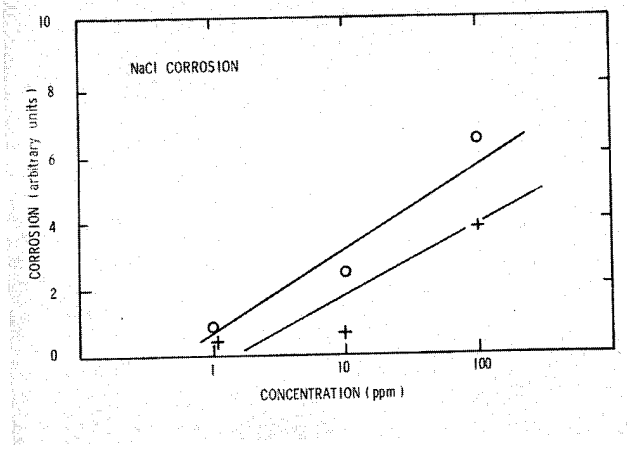


Figure 4. The Average Corrosion Intensity Versus Concentration for NaCl Impurities at 85/85/20. Anode, + and Cathode, O.

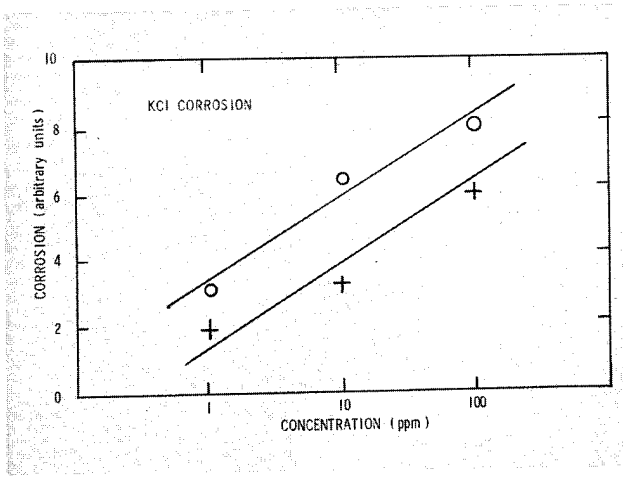


Figure 5. The Average Corrosion Intensity Versus Concentration for KCl Impurities at 85/85/20. Anode, + and Cathode, O.

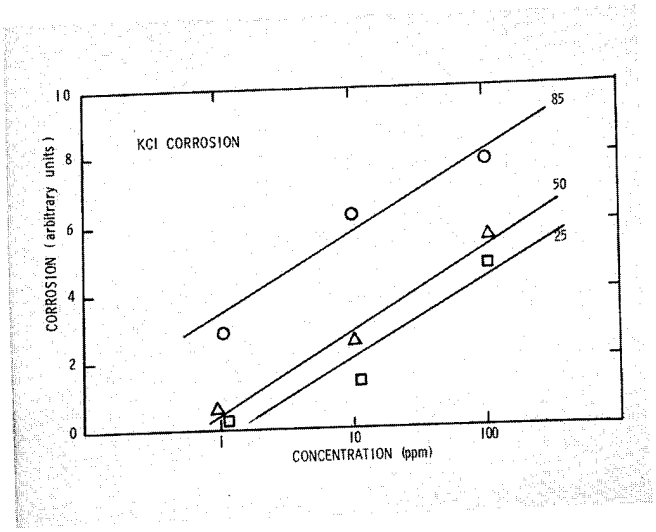
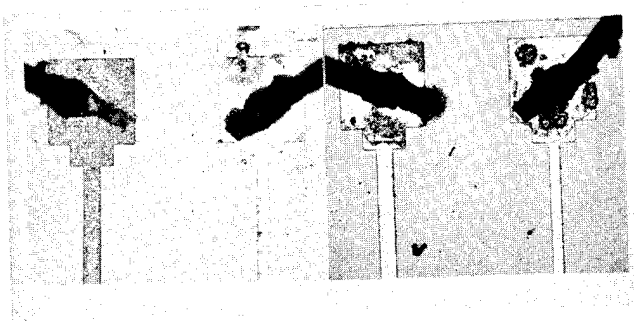
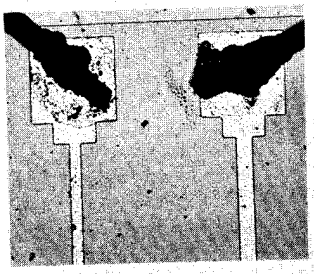


Figure 6. The Cathodic Corrosion Intensity Versus Concentration at 25, 50 and 85°C for KCl Impurities.



A. 85°C B. 50°C



C. 25°C

Figure 7. Aluminum Corrosion for NaCl Impurities.

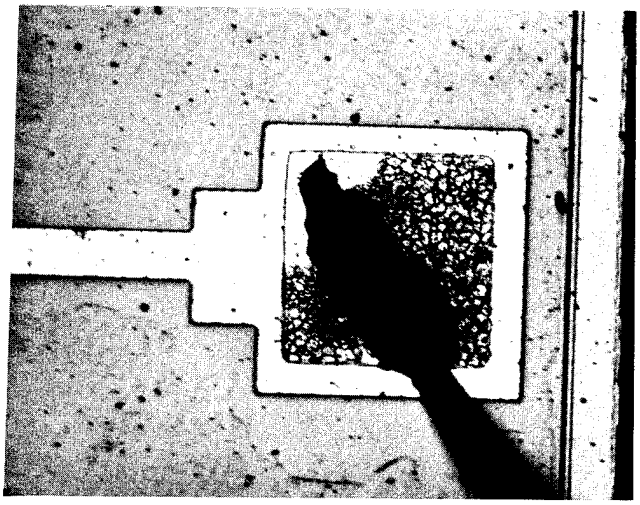


Figure 8. Bonding Pad Corrosion for Glass Passivated Samples That Were Doped ith 1 ppm NaCl.

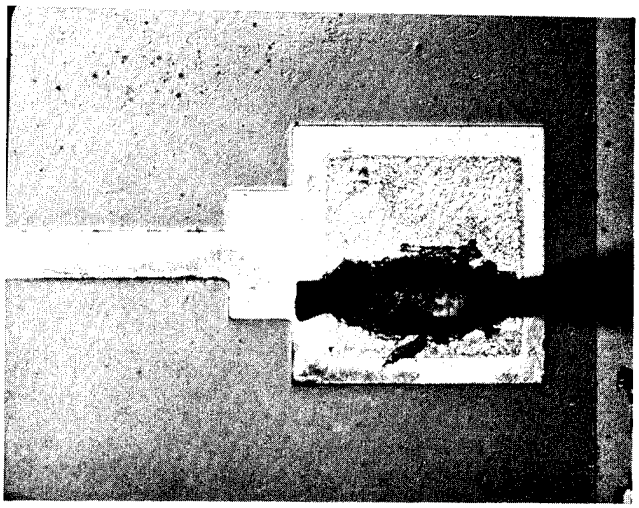


Figure 9. Cracks and Pinholes in the Passivation Glass Cause Corrosion Along the Al Stripes in Addition to the Bonding Pad Corrosion With 10 ppm NaCl.

BERYLLIUM - A HIGH RELIABILITY METALLIZATION

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Abstract

The results of an experimental study of beryllium and beryllium-aluminum alloys as high reliability advanced metallizations for use on semiconductor devices is presented. Methods for the deposition of thin films and the properties of these films are described and the application of these metallizations to actual devices is discussed. In addition, since beryllium can be a toxic material, precautions necessary for its use are detailed.

Introduction

For applications in semiconductor devices, thin film metallization systems must meet many dissimilar requirements. For normal applications, a thin film metallization must meet the basic criteria listed in Table I. In addition to these requirements, any advanced metallization must also offer some improvement in some or all of the areas listed in Table II. Many of the requirements listed are related to specific material properties as shown in the right hand column of these tables.

Aluminum is the most widely used thin film metallization and it satisfies all of the basic requirements given in Table I. In addition, it can meet to a limited degree some of the requirements of Table II by, for example, alloying with copper to improve its electromigration properties or alloying with silicon to reduce silicon dissolution on shallow junction devices. However, for high reliability applications complex and costly multilayer gold metallizations are frequently employed.

Very few metallization systems have been shown to satisfy all of the requirements given in Tables I and II. Moreover, in those instances where significant improvements in some properties have been obtained, these advances have often been at the expense of other properties or in added cost and complexity in processing. In the following sections, we will present the results of a study of beryllium thin film metallizations which show that beryllium and, in particular, beryllium-aluminum alloys can offer many significant improvements over aluminum and aluminum alloys and, in many cases, can be employed with only minor changes in the processing methods used for aluminum metallization systems.

The Physical Properties of Beryllium

Beryllium has an atomic number of 4, an atomic weight of 9.0122 and a density of 1.8477 g/cc. It has a melting temperature of 1290°C and a boiling point of 2970°C. In spite of its high melting temperature, it has a high vapor pressure which is virtually identical to that of aluminum. Because beryllium has a hexagonal crystal structure, many of its physical properties are anisotropic. Only values for polycrystalline samples will be given here since these values will better approximate those expected in deposited thin films.

Beryllium is a metallic conductor exhibiting a positive Hall coefficient[1] indicative of a hole majority carrier. The electrical resistivity of bulk samples varies considerably, values from 3 to 6 μohm-cm having been reported at 20°C. The data shown in Figure 1 is for high purity hot pressed beryllium powder, giving a room temperature resistivity of 4.3 μohm-cm and a temperature coefficient of resistivity of 0.03 ohm-cm/°C. Vacuum distilling of the metal, however, results in a much higher resistivity ratio ($\rho_{RT}/\rho_{4.2°K}$) than obtained for the hot pressed metal[3], indicating a higher purity. No resistivity data could be found for thin films such as used on semiconductor devices.

No data was available regarding the Schottky barrier height of beryllium on either n or p type silicon and hence no predictions could be made regarding the nature of ohmic contacts to silicon. However, since most metals in contact with silicon have a barrier height roughly 2/3's of the silicon band gap, it is reasonable to expect that beryllium will make ohmic contact with silicon at doping levels similar to those used for aluminum.

Although an a priori determination of the electromigration properties of any metallization system is not possible, a qualitative relative estimate of the electromigration lifetime can be made by the comparison of the self-diffusion coefficients in different metallization systems. The values for these self-diffusion coefficients in aluminum, gold, and beryllium are given in Table III. Assuming that the mean time to failure (MTTF) is proportional to these coefficients with all other features effecting electromigration being equal, these values indicate that the MTTF for beryllium should be roughly an order of magnitude greater than that for aluminum and an order of magnitude less than that for gold.

Chemically, beryllium is quite similar to aluminum, forming a nonporous, passivating oxide about 100 Å thick after approximately two hours exposure to air at room temperature. At higher temperatures, the oxidation rate of beryllium obeys an Arrhenius law dependence. When one considers the passivating effect of this oxide layer, the corrosion rate of beryllium is almost identical to that of aluminum. The oxide of beryllium (BeO) is the major impurity in metallic beryllium, comprising approximately 1 wt. % in high purity nuclear grade material. The vapor pressure of this oxide, however, is approximately six orders of magnitude less than that of beryllium at the same temperature, thereby allowing one to employ relatively impure source materials for the evaporation of thin films. This feature further enhances the economic advantage of beryllium over gold, since 99.0% pure beryllium can be obtained at a cost of less than $50/kg.

Beryllium can be chemically etched in dilute HF, HCl and HNO_3 as well as most common aluminum etchants. It is also attacked by some of the common photoresist stripping agents, notably J100*, while others such as RT1* have little effect.

An important property of beryllium is that it has no appreciable solid solubility for silicon, forming a simple eutectic system with a eutectic temperature of 1090°C (Figure 2). This makes beryllium most attractive for shallow junction devices and high temperature processing. In contrast to this lack of solubility for silicon, beryllium readily reduces SiO_2, the free energy of formation of BeO and SiO_2 being -1136 kJ/mole of O_2 and -804 kJ/mole of O_2 respectively at 100°C. The combination of the ability to reduce SiO_2 with no solubility

*J100 is a registered trademark of IRCL, Inc., while RT1 is a registered trademark of Allied Chemical Company.

TABLE I

Requirements for Normal Thin Film Metallizations

Low resistivity (<5 μohm-cm)	Metallic conduction, impurity content
Good adhesion to silicon and thermally grown and deposited SiO_2	Heat of formation of oxides, ability to reduce SiO_2
Ability to make ohmic contact to both n and p type silicon	Schottky barrier height, ability to reduce native SiO_2
Amenable to practical production methods of deposition and delineation	Melting temperature, vapor pressure, chemical reactivity
Favorable mechanical properties for wire bonding operations	Yield strength, hardness, chemical compatibility
Stable properties with time	Oxidation rate, corrosion rate, passivating properties

TABLE II

Requirements for Advanced Thin Film Metallizations

Resistance to electromigration induced failures	Self-diffusion coefficient, grain boundary diffusion coefficient
Resistant to oxidation and corrosion	Heat of formation of oxides, electrochemical potential, passivating properties
No detrimental phases with other metals	Phase diagram, mechanical and electrical properties of phases
No silicon dissolution	Phase diagram with silicon
Fine line processing	Chemical reactivity, grain size
Multilayer metallization processing	Ability to reduce SiO_2 and other surface barriers (Al_2O_3), yield strength, step coverage

TABLE III

Self-Diffusion Coefficients for Al, Au, and Be

$$D_s = D_o \exp(-Q/RT)$$

	Q(kJ/mole)	$D_o(cm^2/sec)$
Al	142.2	1.71
Au	174.5	0.091
Be	160.8	0.36

for silicon is virtually unique among practical metallization systems and should promote both good adhesion to thermally oxidized substrates and good ohmic contact to silicon.

Mechanically, beryllium is both stronger and harder than aluminum, having an elastic modulus of 2.54×10^{11} N/m^2, a tensile strength of 2.75×10^8 N/m^2 and a hardness of 6 to 7 on the Mhos scale. Because of beryllium's high strength, thin films should show no surface reconstruction with thermal cycling. Moreover, its higher hardness should result in less deformation of bonding pads during wire bonding and, hence, more reliable wire bonds provided the native oxide can be broken up during the bonding process. It should be noted, however, that beryllium like aluminum does react with gold to form low melting point intermetallic phases and hence gold wire bonds should not be used unless further reliability studies are made of this system.

Experimental Methods

Previous work[5,6] indicated that beryllium thin films could be deposited by several methods, including evaporation and sputtering methods. Because of the reactivity of beryllium with both tantalum and tungsten, evaporation from filament and boat sources is not practical. Electron beam methods employing both crucibles and unlined copper hearths were found to be well suited to the evaporation of beryllium and the work described in this paper was carried out using a 270^0 bent beam electron source with an unlined, water cooled copper hearth.

Typically the charge, between one and ten grams of material, was premelted prior to evaporation in order to homogenize the charge and to eliminate dissolved gasses which cause spattering of the charge. Beryllium-aluminum alloy sources were prepared in a similar manner by melting both beryllium and aluminum in the hearth to form a single source. This was possible because of the identical vapor pressures of beryllium and aluminum which allows one to use a single source without depletion of one alloying element due to unequal evaporation rates. The substrates were placed on a heated susceptor located approximately 45 cm above the source. The temperature of the substrates could be varied between room temperature and 600^{0}C with an accuracy of $\pm$ 20^{0}C at the higher temperatures. The deposition rate could be varied between virtually zero and a maximum of 1.5 μm/min depending on the power setting. Typical deposition rates were between 0.9 μm/min and 1.2 μm/min.

The oil diffusion pumped vacuum system was typically evacuated to less than 1.33×10^{-4} N/m^2 (1×10^{-6} torr) prior to the evaporation and remained below 6.7×10^{-4} N/m^2 (5×10^{-6} torr) during the run. The entire vacuum station was enclosed in a plexiglass cabinet which was in turn exhausted thru an absolute air filter and a water scrubber before venting into the atmosphere. A minimum of 4.5 m^3/min (150 cu. ft./min) air flow into the station was maintained through the openings to the evaporator. The foreline pump exhaust was also vented into the same system. Material for evaporation, substrates coated with beryllium, and waste containers were handled in a similarly exhausted cabinet attached to the evaporation system.

Resistivity measurements on the deposited thin films were carried out using a conventional four-point in-line probe. Measurement of stress in the films was performed using a Lang x-ray topographic unit. In this method, the radius of curvature of the silicon substrate with the metal film was determined from the angular variation of the (220) diffraction peak as the incident x-ray beam was scanned radially across the wafer. The stress in the metal film was then calculated from this radius of curvature using Stoney's equation[7],

$$\sigma = \frac{Ed^2}{6(1-\nu)Rt}$$

where E and ν are Young's modulus and Poisson's ratio for the substrate, d and t the thickness of the substrate and film respectively, and R is the radius of curvature.

Electromigration data was obtained using an electromigration test pattern consisting of eight "dogbone" stripes, each 5 μm wide by 500 μm long by 0.5 μm thick, on an oxidized silicon die which was soft soldered to a nine pin TO-3 header. Each stripe was connected through 50 μm (0.002") diameter aluminum-0.5 % magnesium wires and 100 ohm ballast resistors to a constant voltage power supply. Test samples of up to 300 stripes were powered in a temperature controlled oil bath at current densities of up to 5×10^6 A/cm^2 and the cummulative failure rate was recorded as a function of time using an inductive pulse detection circuit and a digital printer.

Experimental Results

Because of the reported variation in the resistivity of bulk beryllium samples, the effect of the deposition conditions on the resistivity of thin beryllium films was of primary concern. Thus a matrix of experiments was set up to determine the influence of variables such as deposition rate, substrate temperature, and vacuum level on the resistivity of the deposited film. In brief, the results of these studies indicated that while beryllium did appear to be more prone to contamination in poor vacuum than did aluminum, the only variable which had a major effect on the resistivity of the deposited film was the temperature of the substrate. The higher the temperature of the substrate, the lower was the resistivity of the deposited beryllium film. This result is shown in Figure 3. As can be seen from this figure, for temperatures above 500^{0}C the film resistivity approaches an asymptotic value around 4.3 μohm-cm as compared to the bulk value of 3.25 μohm-cm. However, values below 4.0 μohm-cm have been obtained in thin films of beryllium.

While it was not possible to unequivocably establish the origin of this temperature dependence of the resistivity, it was observed that the grain size of the film increased considerably from less than 0.1 μm to greater than 0.1 μm as the deposition temperature was increased (see Figures 4(a) and 4(b)). Thus, a considerable portion of the resistivity in thin films deposited at low temperatures may be due to grain boundary scattering as has been previously reported for other metallization systems.[8,9] Annealing of films deposited at room temperature did reduce the resistivity of these films, although not to values comparable to those measured in films deposited at elevated temperatures. This result tends to support the hypothesis of grain boundary scattering effects, although it was not possible to prove that grain growth was occurring during annealing due to the poor contrast of beryllium in the transmission electron microscope.

Severe problems were encountered in pure beryllium thin films deposited at temperatures above 300^{0}C, however, due to stresses resulting from the dissimilar thermal expansion coefficients of the film and the substrate. In thicker films in particular, these thermal stresses were sufficient to cause the film to peel from the substrate by fracturing of the thermal oxide at the SiO_2/Si interface. The cause of this problem is the high tensile strength of beryllium which prevents the

film from deforming at lower stresses and thereby relieving the stress in the film. Even in thinner films which were stable after deposition, peeling of the film was encountered after patterning. This peeling was highly erratic and unpredictable, occurring over periods ranging from hours to even days depending on the deposition conditions. Because of this peeling problem, it was concluded that pure beryllium could not be used in applications requiring low resistivity films which could only be obtained by high deposition temperatures.

Since the origin of the stress problem lay in the limited ductility of pure beryllium, a search was undertaken to find alloy systems of beryllium which would provide greater ductility and hence lower thermal stresses when deposited at elevated temperatures. Certain restrictions were obvious, however, in the choice of this alloy system, particularly the requirement that there be no appreciable solid solubility or intermetallic phase formation between the alloying elements in order to preserve the low resistivity of beryllium deposited at high temperatures. By a fortuitous chance, it was found that the addition of aluminum to beryllium results in a considerable enhancement in the ductility of the alloy and, furthermore, the equilibrium phase diagram of beryllium and aluminum shows a simple eutectic system with no mutual solid solubility between the two elements (see Figure 5). Moreover, because beryllium and aluminum have virtually the same vapor pressure at all temperatures it is possible to use a single alloy source for the deposition of the alloy films without encountering problems due to the segregation of one element into the molten source due to unequal evaporation rates.

To verify that the beryllium-aluminum alloy system would indeed achieve the desired objectives, a series of alloys ranging from 5 to 40 wt. % aluminum were made and deposited over a range of substrate temperatures from room temperature to 560°C, the choice of this maximum deposition temperature being dictated by the presence of the aluminum-silicon eutectic temperature of 577°C. From these studies, it was found that the resistivity of the alloy films and its dependence on the deposition temperature was the same as in pure beryllium. The stress in the alloy film, however, decreased rapidly with increasing aluminum content, as shown in Figure 6. From these results, it was concluded that an alloy containing 10 wt. % (4 at. %) aluminum would provide a sufficient reduction in stress while minimizing the aluminum content. This latter consideration is important if one is to avoid dissolution of the silicon by the aluminum eutectic phase in these alloy films. This alloy (Be-10% Al) was selected as the standard beryllium alloy for all subsequent electromigration and device application studies.

Schottky barrier height measurements were made for both pure beryllium and for the Be-10% Al alloy on n-type silicon. These results are preliminary in that only one method was used to determine ϕ_B and only n-type silicon was employed. Guard ring structures were fabricated using 1 ohm-cm n-type epi on n^+ substrates. The metal was e-beam deposited at 350°C and patterned into circular dots over the active area and the guard ring.

Barrier height measurements were made for the as-deposited metal and after annealing at 475°C. Table IV gives the value of ϕ_B after deposition and after annealing for 2 hours at 475°C. For pure beryllium, the value of $_B$ increased with anneal but stabilized after approximately 1/2 hour to its final value of 1.33×10^{-19} J (0.83 eV). The barrier height of the Be-10% Al alloy did not vary appreciably with anneal. However, a slight increase in the scatter of the measured barrier height was observed after the anneal.

The ability to make ohmic contact to silicon depends on (1) the barrier height between the metal and silicon, (2) the doping of the silicon, and (3) the presence of any intervening interface films, e.g. - native SiO_2. Since the measured barrier height of beryllium and the Be-10% Al alloy is close to that of pure aluminum (0.72-0.80 eV) and since beryllium can reduce any residual SiO_2, ohmic contact for beryllium should be about the same as for aluminum.

Other processing features of beryllium and the Be-10% Al alloy were as predicted from the phase diagrams and from previous work in the literature. No silicon dissolution was observed between pure beryllium and silicon for temperatures up to 650°C. A few very shallow dissolution pits were seen for the Be-10% Al alloy after annealing on silicon for 1 hour at 550°C. Patterning of these metallizations was practically identical to that for pure aluminum. Beryllium etches somewhat faster than aluminum in most common aluminum etchants as well as in dilute HF. Ultrasonic bonds of aluminum and aluminum alloy wires to beryllium and Be-10% Al exhibited good pull strengths, although the load-time-power windows for beryllium are somewhat smaller than for pure aluminum. Also, because beryllium has less ductility than aluminum, less deformation of the bonding pads was observed. However, at high power settings it is possible to fracture the underlying thermal oxide due to this lack of ductility, resulting in a "burn off" of the metallization.

While the results of electromigration studies conducted thus far are only preliminary, they do indicate that the Be-10% Al metallization is far superior to aluminum and aluminum alloys. This is shown in Figure 7 for the Be-10% Al alloy powered to a current density of 5×10^6 A/cm^2 at 168°C. The MTTF under these conditions was found to be 280 hours as determined from a Weibull analysis of the cummulative failure versus time. In comparison, a test of pure aluminum using identical stripe geometry gave a MTTF of only 68 hours for a current density of 2×10^6 A/cm^2 at 168°C. Using the normalized figure of merit developed by Black[10] as shown in Figure 7, this corresponds to roughly a one hundredfold improvement in the electromigration failure rate for beryllium over that of aluminum. Electromigration induced hillock growth was observed in failed Be-10% Al stripes, the hillocks occurring at the positive terminal of the stripe as in aluminum. There is tentative evidence that these hillocks are enriched in aluminum.

Finally, since the ultimate proof of the credibility of any metallization system rests in its application to practice, several test devices were chosen for evaluation employing the Be-10% Al metallization. The first of these devices was a 12 volt, 5 watt NPN UHF power transistor having a washed-emitter structure. This particular device poses many challenging problems, having a very shallow emitter-base junction which comes within less than 0.5 μm of the edge of the emitter cut and requiring very fine line geometry at high current densities. The Be-10% Al alloy was deposited directly on the substrate with no intermediate diffusion barrier metallization. No premetallization etch of the emitters was necessary, since it was found that a short anneal of approximately 20 minutes at 400°C was sufficient to remove any native oxide present, thereby establishing excellent ohmic contact. While some small problems were encountered in shorting of the emitter-base junction after this anneal due to silicon dissolution at the edge of the emitter cut, wafer yields were similar to those obtained using standard aluminum alloy metallizations with underlying diffusion barrier metallization. These devices were then packaged to TO-39 headers and subjected to the same final test used with the standard product. In brief, they passed all tests,

TABLE IV

Schottky Barrier Height and Ideality Factor
for Beryllium-Silicon Schottky Barriers

	As Deposited		Annealed 2 Hours at 475°C	
	ϕ_B	n	ϕ_B	n
Beryllium	1.25×10^{-19} J (0.78 eV)	1.05	1.33×10^{-19} J (0.83 eV)	1.03
Be - 10% Al	1.17×10^{-19} J (0.73 eV)	1.04	1.17×10^{-19} J (0.73 eV)	1.05

TABLE V

Premissible Air Tolerance Levels of
Beryllium and Other Toxic Materials
Used in the Semiconductor Industry

Material	$\mu g/m^3$
Beryllium	2
PH_3	70
Mercury	100
Phosphorus	100
Arsenic	500

both DC and RF, with roughly the same yield as the standard product. Lastly, a small signal NPN device was fabricated using the Be-10% Al alloy. The elctrical parameters of this device were identical to that of the standard product, even after being subjected to anneals of up to 600°C for 1 hour.

In general, beryllium and Be-10% Al alloys appear to be a highly viable metallization system, particularly in applications where high current densities and shallow junctions are encountered. Beryllium is also attractive for processes where high post-metallization temperatures are encountered and may be very useful in radiation hardened devices.

Safety Procedures

Beryllium and beryllium alloys can and have been handled safely.[11] The primary hazard of beryllium is its toxicity by inhalation.[12] The permissible tolerance levels as published in the Federal Register Vol. 36 #157 Friday, August 13, 1971, are given in Table V. For comparison, the acceptable tolerance levels for several other materials commonly found in the semiconductor industry are also listed. Because of these potential safety problems, processing steps where air borne particles or fumes could be generated must be carefully controlled. However, the metallization in its fabricated form presents no hazard. Several reports[13,14] describe laboratory and processing procedures and these techniques were implemented for the work described here. Surface and air samples within the processing areas were taken routinely and analyzed for beryllium content using atomic absorption methods. These results showed no hazardous levels and indicated that beryllium could be easily and routinely handled without undue hazard to personnel.

Conclusions

The results of this work demonstrate that beryllium and beryllium-aluminum alloy metallizations are well suited to semiconductor device applications. Among its major advantages are (1) excellent resistance to electromigration induced failures, (2) its lack of any significant chemical interaction with silicon, and (3) its ability to reduce SiO_2, thereby forming excellent ohmic contact to silicon and promoting adhesion to SiO_2. Insofar as is known, the combination of these two latter properties are unique among practical metallization systems.

It is not without its limitations, however, (1) requiring high deposition temperatures (560°C), (2) being slightly higher in resistivity than aluminum (typically 4.0 to 4.5 ohm-cm), and (3) requiring some care in handling due to toxicity. In addition, there are minor changes required in photoresist and wire bonding methods due to the slightly rougher surface texture encountered in the films deposited at elevated temperatures. None of these problems present any significant limitation to the use of this metallization, however, and its advantages far outweigh its disadvantages in those applications which require high current densities and high reliability.

Acknowledgments

We would like to thank Dr. W. M. Paulson for providing the transmission electron micrographs of the beryllium thin films. The assistance of Messrs. D. Burt and J. A. Tchida in processing the RF test devices is

greatly appreciated as are many helpful discussions with Mr. J. R. Black and Dr. E. Philofsky. Special thanks are due Mrs. Marlene Robertson for her efforts in the preparation of this manuscript.

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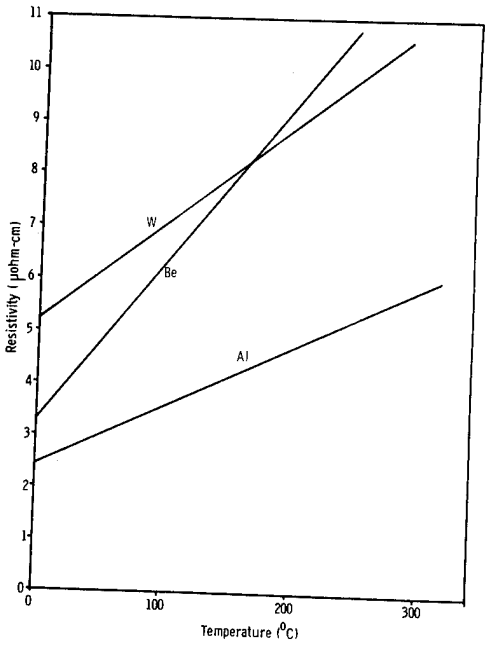


Figure 1. Electrical Resistivity of Beryllium from 0 to 300°C. (after Hausner, Ref. 2)

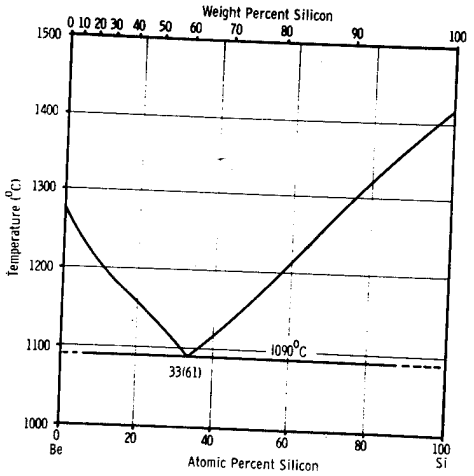


Figure 2. The Beryllium-Silcon Phase Diagram. (after Hansen, Ref. 4)

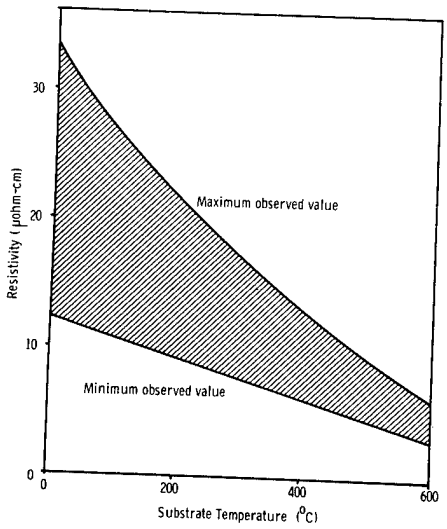
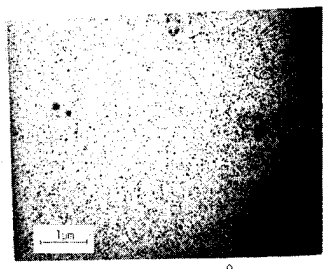
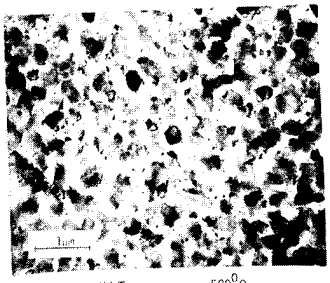


Figure 3. Film Resistivity versus Substrate Temperature for Electron Beam Deposited Beryllium Thin Films. (All films were approximately 1 μm thick)



(a) $T_{substrate} = 25^{0}C$



(b) $T_{substrate} = 580^{0}C$

Figure 4. Microstructure of Electron Beam Deposited Beryllium Thin Films. (a) Substrate at Room Temperature. (b) Substrate at $580^{0}C$.

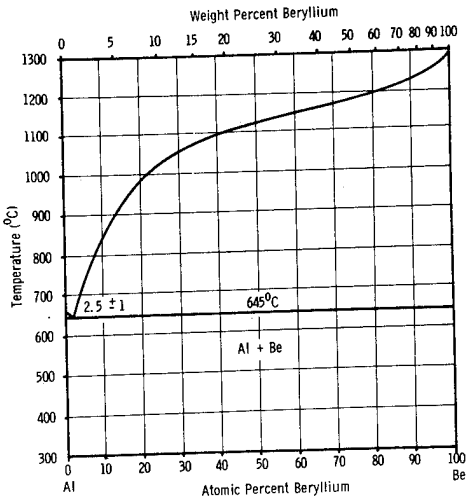


Figure 5. The Beryllium-Aluminum Phase Diagram. (after Hansen, Ref. 4)

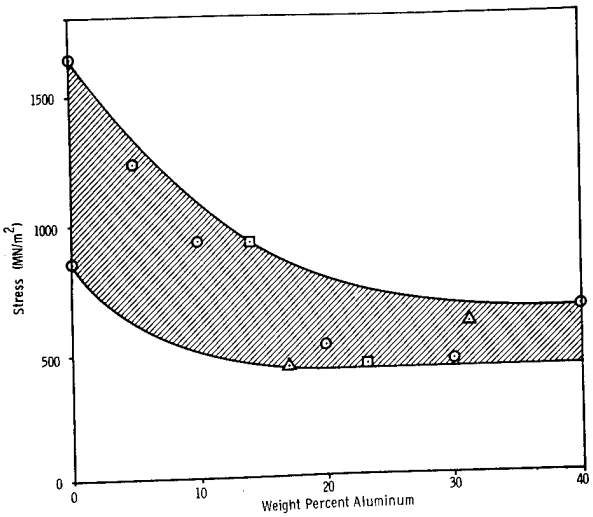


Figure 6. Thermal Stress versus Weight Percent Aluminum for Be-Al Thin Films Deposited at $560^{0}C$. (All films were approximately 1 μm thick)

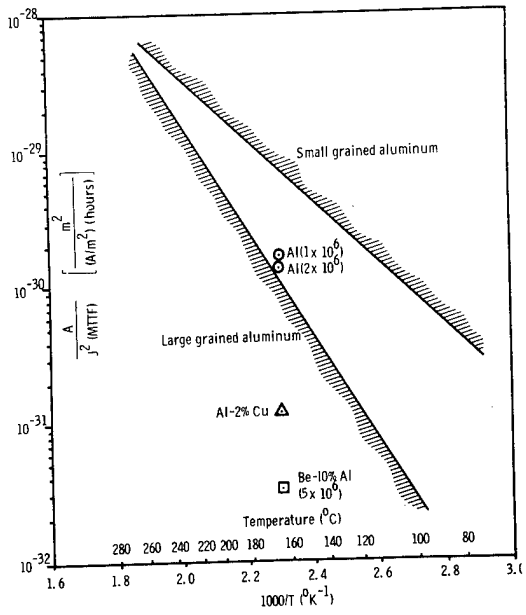


Figure 7. Electromigration Lifetime for Be-10% Al Thin Film Metallization. $J = 5 \times 10^{6}$ A/cm^{2}. (after Black, Ref. 10).

SAND76-5286

GOLD ALUMINUM INTERCONNECT STABILITY ON THIN FILM HYBRID MICROCIRCUIT SUBSTRATES

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ABSTRACT

The effects of gold aluminum intermetallic growth on the stability of interconnects to thin film hybrid microcircuits were studied. Three different metallization systems were evaluated using three types of bonding wire. Tantalum-nitride-chromium-gold was bonded using 0.031 mm aluminum 1% Si wire and 0.031 mm aluminum 1% Mg wire. These two wire types were also bonded to substrates metallized with tantalum-nitride titanium-palladium-gold. Also, gold wire (0.025 mm) was bonded to aluminum metallization. These metallization-bond systems were evaluated by subjecting the tests specimens to various known temperatures and time environments followed by loop pull tests to destruction, bond shear tests to destruction, and four-point probe electrical resistance measurements. The environments included:

1. 1000 hrs. of storage at 100°C, 200°C, and 300°C.
2. Temperature cycling from -40°C to 200°C for 10, 50, 100, 500, 1000 cycles.

The data shows that the electrical resistance shows drastic increases long before mechanical integrity is degraded. It was not uncommon to see kilohms.

The results of aging of gold wire bonding to aluminum metallized substrates is described. Stabilized and unstabilized wire were used, and the effects of time and temperature on bond integrity are reported. Both were types degraded mechanically and electrically with little differences between the two.

Introduction

The identification of gold-aluminum intermetallics is not a new discovery. The liquidus curve for these alloy compositions was determined completely in 1900.[1] The well-known purple plague ($AuAl_2$) was characterized in 1938 by Arthur S. Coffinberry and Ralph Hultgren.[2] The electronics industry became keenly aware of the significance of gold aluminum intermetallics in the mid 1960's.[3] Transistors and integrated circuits were interconnected by thermocompression bonding pure gold wire to the aluminum metallization on the silicon chips.[4] In an effort to avoid the bond failures due to intermetallic embrittlement and Kirkendahl voiding[5] at the semiconductor chip interconnect, ultrasonic aluminum wire bonding[4] began to replace the gold wire bonding. This technique resulted in an aluminum-aluminum monometallic bond at the chip. The gold-aluminum interconnect at the package pinout did not contribute significantly to the failure rate of devices. This lead to the belief that the presence of silicon accelerated the formation of purple plague and interconnect failure.[6] In the past fifteen years many papers have been written to explain the characteristics of gold-aluminum interconnects, and just about as many conflicting conclusions have been reached. It appears than many of the conclusions reached are indeed valid for the systems evaluated. There is, however, a danger in extrapolating the conclusions drawn from one system to a different system including gold and aluminum as part of the metallization interconnection. For instance, Elliot Philofsky[7] arrived at four major conclusions on gold-aluminum systems concerning intermetallic phases, kinetics of intermetallic formation, effect of silicon, and strength of the bond. Subsequent to his paper, Philofsky suggested[8] caution in accepting his conclusions in systems other than apparent infinite thickness pure gold and pure aluminum.

In the past, Sandia Laboratories has tried to maximize the use of monometallic gold-to-gold interconnections in hybrid microcircuits by using beam-leaded devices and tantalum-nitride chromium-gold-thin-film metallization on ceramic substrates. However, recent design definition at Sandia Laboratories will require the use of CMOS devices. A literature search and an industry survey by the author indicate that CMOS chips will have aluminum metallization at least for the next 2 years. There are several new interconnect methods being developed such as Tape Automated Bonding (TAB)[9] and the 3M leadless hermetic package[10], but there will not be adequate enough production data available to effect current programs.

Aluminum wire has been selected to avoid the gold-rich[11] gold-aluminum intermetallic at the chip. Since the semiconductor industry is using aluminum ultrasonic wire bonding on discrete device and integrated circuit chips, there are millions of performance hours of this monometallic bond indicating no significant problem with the chip metallization interconnect.

The remaining questions then are what is the stability of the ultrasonic bond on gold thin film metallization and how is the stability effected by changes in the traces of impurities found in the potential metallizations that may be used. Although gold wire is not presently being considered because of potential problems with the bond at the device, it is being evaluated here as information on its performance on an aluminum metallized substrate in case this system is considered in the future. It was also evaluated to look for performance differences between gold stabilized and unstabilized gold wire.

Materials and Procedures

Two types of aluminum wire were used (1% Mg and 1% Si) with two types of thin film gold metallization. The first gold metallization is the standard now being used in Sandia Laboratories designs. The metallization consists of a 50.0 mm thick sputtered tantalum-nitride resistor layer, a 30.0 mm evaporated chromium adhesion layer, and a 3 μm evaporated layer of gold.

The substrate material in all of the metallizations evaluated was 99.6% pure, as-fired alumina. The second gold metallization was a resistive layer of tantalum-nitride followed by evaporated layers of titanium (200mm), paladium (200 mm), and a final layer of plated gold 2.5 μm to 3.5 μm.[12] These systems were selected because they are the two gold systems that are most likely to be considered by Sandia. These metallization combinations were compared with 1.5 μm to 2.0 μm of evaporated aluminum metallization bonded with both stabilized and unstabilized gold wire.[13,14] (Stabilized gold wire has impurities added such as beryllium or titanium on the order of 100 PPM. These impurities are added to limit the maximum gold grain size. There have been indications that the added impurities enhances the formation of intermetallic.)

All metallized substrates were processed photolithographically, resulting in a test pattern (Fig. 1). This pattern provided islands for bonding probing pads for electrical monitoring and metallization bars for resistivity checks.

The ultrasonic bonding was performed using Tempress 1100 bonder modified to provide a 60° bonding capability (Fig. 2).[15] Both the aluminum-1% silicon and the aluminum-1% magnesium wire were 0.03 mm in diameter. A bond schedule was developed that resulted in a minimum deformation with a failure mode that was predominantly heel breaks for loop pulls in the as-bonded condition. This was done to keep the bond heel damage to a minimum (Fig. 3) and thus provide more data on the bond strength by decreasing low strength heel fracture during testing.

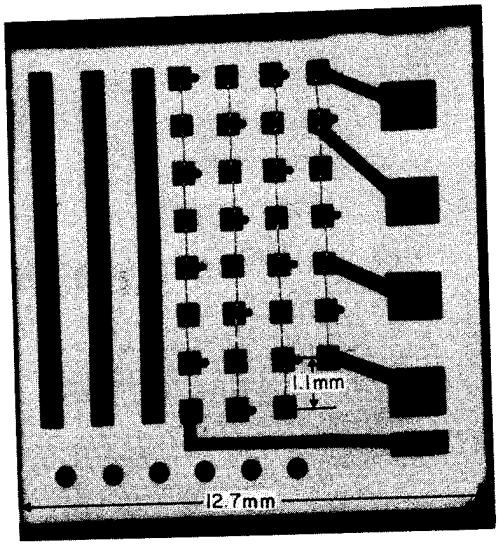


Figure 1. Test Pattern

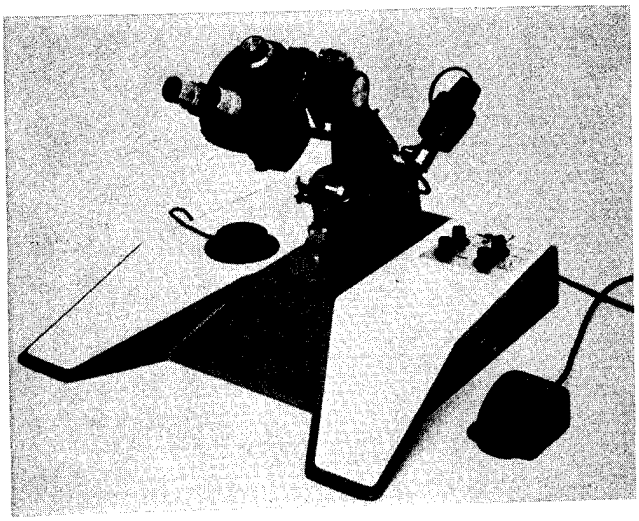
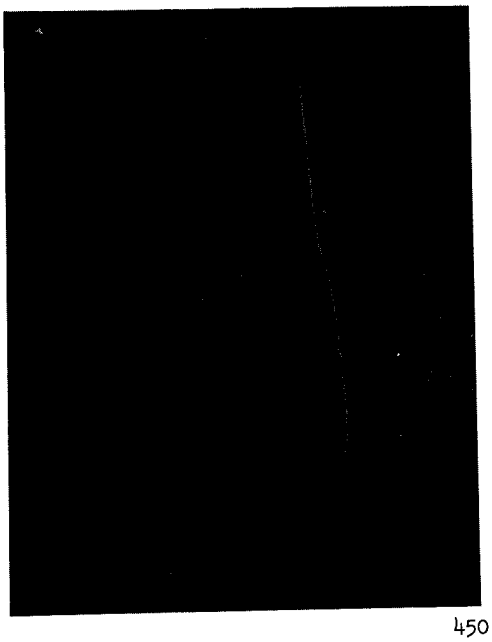


Figure 2. Tempress 1100 Ultrasonic Wire Bonder



450 X

Figure 3. Bond with Minimum Heel Damage

The thermocompression gold wire bonding was performed using the K & S model 475 Bonder. Both types of gold wire were 0.0254 mm in diameter.

Experiment Description

All of the aluminum bonds were made on the same bonder by the same bonding operator. Each wire type came from a single spool, and the bonding parameters (time, force, and energy) were held constant for each metallization system. All bonding for each system was done in as short a period as possible to avoid any time dependent drifting. All of the chromium-gold-metallized substrates were made in the same evaporation run. The aluminum-metallized substrates were also made in one run. The titanium-palladium-gold-metallized substrates were made in two plating lots.

After the bonding was completed in laboratory ambient conditions, the substrates were randomly selected to be evaluated in a specific environmental condition. Table I is a list of the environments that were selected for this investigation. The temperature cycle was from -55°C to 200°C at the rate of one cycle per hour. Table II shows an example of the matrix used on each metallization system. Each substrate was tested after a specific environment so that the collective effects of multiple environments does not need to be taken into account.

After the substrates with bonds were subjected to their respective environments, the bond integrity was evaluated by performing a loop pull test,[16,17,18] a bond shear test, and electrical resistance measurements.[19]

Table I

Environmental Conditions

A. Shelf (To be held in controlled environment for future need or evaluation.)

B. Control (Interconnects will be evaluated in the "as bonded" condition; no environments.)

C. Temperature Cycling (-55°C to +200°C)
   1. 10 cycles
   2. 50 cycles
   3. 100 cycles
   4. 500 cycles
   5. 1000 cycles

D. High Temperature Storage -- 1000 hours
   1. 100°C
   2. 200°C
   3. 300°C

Table II

CrAu-1% Mg Wire

		Test Condition and Number of Substrates					
		PULL	SHEAR	RADIATION	ELECT.	METALL.	
A	Shelf	158	204	202	227	231	
B	Control	151	172	166	238	219	
C1	Temp Cycling 10 ~	128	174	214	226	229	
C2	50 ~	156	130	144	162	211	
C3	100 ~	215	134	154	223	205	
C4	500 ~	230	218	177	208	148	
C5	1000 ~	126	224	135	221	165	
D	Hi Temp Storage						
D1	@ 1000 Hours 100°C	181	212	169	132	203	
D2	200°C	222	150	213	152	129	
D3	300°C	233	145	216	228	121	

On the bond many of the post environment failures were low strength wire break or a bond heel break. metallurgical examinations were performed on many of the bonds of these wire failures to obtain more information about the condition of the bond.

Results

A total of 21,600 bonds were evaluated in this study. The data from pull testing, shear testing, and resistance measurements were analyzed for each metallization system. The data were compared from one system to another, and correlation checks were run to look for similarities between shear test results and pull test results.

Pull Testing

The results of the pull testing are shown in Table III. The CrAu-Aℓ 1% Si wire had a slightly higher average pull strength after the more severe environments. It also had a smaller standard deviation and a higher minimum of pull than the other metallization systems. Table IV shows a comparison of failure modes for aluminum wire. It is significant to note that CrAu-Aℓ 1% Si had no bond lifts. A bond that lifts in pull testing in considered a poor quality bond. All other metallization systems had a large number of bond lifts.

Table III

Average Pull Strength in grams

Environment	Metallization					
	CrAu - Si	TiPdAu - Si	CrAu - Mg	TiPdAu - Mg	Al - Au Stabilized	Al - Au Unstabilized
Control	17.3	14.2	19.9	13.9	4.8	7.2
Temp. Cycle (-50 to +200°C)						
10	10.5	15.1	8.8	—	—	—
50	10.3	12.9	8.2	—	—	—
100	7.9	9.2	6.4	5.4	—	—
500	9.7	5.9	7.1	0.8	3.7	3.6
1000	10.6	7.0	7.9	0.4	6.4	7.7
High Temp. Storage (1000 hrs.)						
100°C	13.0	11.5	7.2	13.1	7.4	8.7
200°C	7.3	6.7	2.4	4.4	1.0	0.4
300°C	6.6	6.5	6.7	5.4	2.2	1.3

The TiPdAu-Aℓ 1% Si and the CrAu-Aℓ 1% Mg were the next best systems with little difference in the overall bond strengths. Although the TiPdAu-Aℓ 1% Si had twice the number of band lifts as the CrAu-Aℓ 1% Mg it showed more consistancy in bond strength through environments.

The TiPdAu-Aℓ 1% Mg system showed erratic behavior compared to the other systems. In most environments, this system was lower in pull strength. After 500 and 1000 temperature cycles, the bond strength dropped to near zero and the failure modes were lifts and heel

breaks. It is apparent that this system is inferior to the other aluminum wire systems. The results correlate with the fact that difficulty was experienced in establishing a bonding schedule for the TiPdAu metallization. The increased deformation required to get a satisfactory bond increases the bond heel damage and increased heel breaks during pull testing.

The unstabilized gold wire had a higher "as bonded" strength, but it decreases to half of the stabilized wire bond strength after 200°C and 300°C soak. Both gold wire types have considerably less strength than the aluminum wires after heat soak and the predominent failure mode for both gold wires was bond lifts.

Table IV

Failure Mode by Metallization After Environments

Metallization	Wire Break	Heel Break	Lift	Total
CrAu - Si	73	275	0	348
TiPdAu - Si	0	150	244	394
CrAu - Mg	82	145	116	343
TiPdAu - Mg	0	120	192	312

Table V

Average Shear Strength in grams

Environment	Metallization					
	CrAu - Si	TiPdAu - Si	CrAu - Mg	TiPdAu - Mg	Al - Au Stabilized	Al - Au Unstabilized
Control	14.7	6.2	15.6	2.6	15.8	21.7
Temp. Cycle (-50 to +200°C)						
10	19.7	13.6	11.3	—	—	—
50	20.3	17.6	14.9	—	—	—
100	21.2	7.2	11.7	2.7	—	—
500	21.2	17.0	13.9	0.5	78.6	85.0
1000	19.1	20.8	8.4	0 0	58.5	72.7
High Temp. Storage (1000 hrs.)						
100°C	18.8	18.1	9.9	2.2	95.4	88.4
200°C	17.1	17.8	11.6	3.0	54.4	62.8
300°C	17.9	9.9	9.0	2.6	83.6	91.2

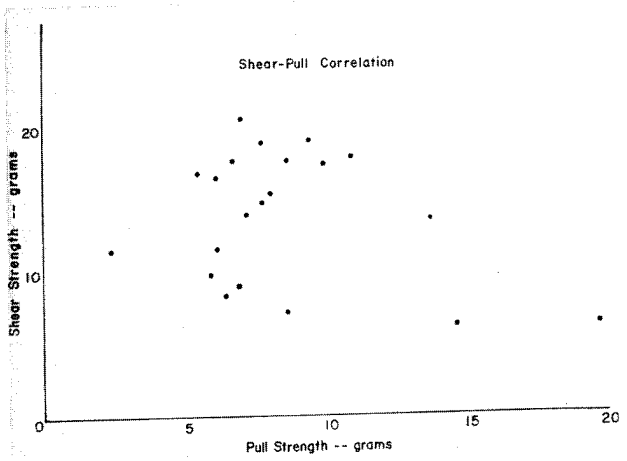


Figure 4. Shear-Pull Correlation

Shear Testing

Again, as shown in Table V the results of TiPdAu 1% Mg were erratic and very low strength. This system was not considered in any further analysis of the shear results. The CrAu - 1% SiAl proved to be superior to the other systems in shear. The mean was significantly higher. The minimum were three grams higher than the next nearest system, and the standard deviation was as good as any of the systems. The presence of the brittle intermetallic can be seen with the gold wire bonding by the increase in shear strength with increased environments. A test for correlation between shear testing and bond pull testing was made. Figure 4 is a plot of the shear strengths versus the pull strength (lifts only) of substrates that had seen like environments. There appears to be no correlations between the two test methods. An analysis of variance was performed on pull test results and shear test results. This analysis indicated that the pull stability was strongly dependent on the environments while the shear stability was metallization dependent. This should be a factor in deciding which bond evaluation to use in similar programs.

Electrical Tests

The metallization resistivity was measured on each test substrate after the environments. There was no significant changes in any of the metallizations. Therefore, any resistance increases can be attributed to the increase of bond resistance. Six loops (twelve bonds in series) were probed on the substrated, and the resistance measurements were recorded in ohms. The results of these measurements were so wide spread that a statistical analysis could not be performed. The wide variation was due, in part, to resistance healing[18] A potential of one volt was applied to the bonds during the four point probe resistance measurements. This was enough voltage in some cases to cause the bond resistance to drop after the initial probe contact. Some bond resistances dropped from kilohms to ohms.

The mechanism for this healing could not be positively identified. It was surprising to find that many of these resistance readings reached up to kilohms and even open circuits. Following the electrical tests, many of these loops were pulled to destruction. There was no correlation between high-resistance and low-pull strength.

If we consider the upper limit for a series of twelve bonds to be 1.0 ohm and ignore the drastic increases that occur above 1.0 ohm, Table VI shows that there is no significant difference among the four metallization system. The 1.0 ohm resistance was an arbitrary level based on approximately three times the as-bonded resistance.

Metallurgical Analysis

It is beyond the scope of this report to cover all of the metallurgical analysis performed in relation to this testing; however, some of the more significant results are reviewed. Figure 5 shows the difference between an aluminum wire failure in the "as-bonded" condition as compared to the failure after exposure to 300°C for 1000 hours. The time at temperature anneals the wire; however, although ductility versus a low ductility analysis was not performed, intermetallic growth in the bond heel area appears to cause low ductility fracture when the loop is flexed during pull testing.

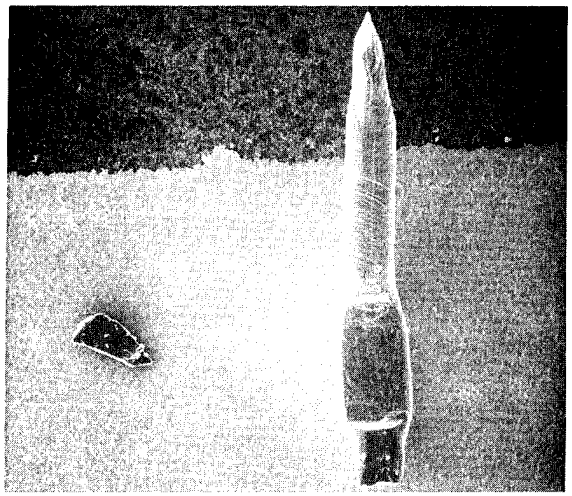
Table VI

Electrical Resistance in ohms

Environment	Metallization					
	CrAu - Si	TiPdAu - Si	CrAu - Mg	TiPdAu-Mg	Al - Au Stabilized	Al - Au Unstabilized
Control	.377	.326	.304	.302	.340	.350
Temp. Cycle (-50 to +200°C)						
10	.328	.344	.260	—	—	—
50	.363	.750	.467	—	—	—
100	.487	10.52	154.0	.468	—	—
500	9.06	6.57	35.4	89.3	.800	.780
1000	26.7	20.9	14.6	62.1	.800	.770
High Temp. Storage (1000 hrs.)						
100°C	344.0	.361	1.09	.304	.730	.710
200°C	56.0	58.8	22.0	33.5	15.9M	15.9M
300°C	675.0	1.1K	18.8	2.88	15.9M	15.9M

In Figure 6 we see the difference in the metallization between CrAu and TiPdAu after the two systems were exposed to 300°C for 1000 hours. Notice the migration of the gold metallization to the bond site in the case of the CrAu. It appears that the gold is depleting at the grain boundaries. There is little evidence of this depletion in the TiPdAu.

To gain a better understanding of the bond area and the intermetallic growth, metallized substrates (one CrAu, one TiPdAu) with 1% Si-Al wire were dipped in a sodium hydroxide solution. The solution etched away the aluminum wire but did not attack the substrate

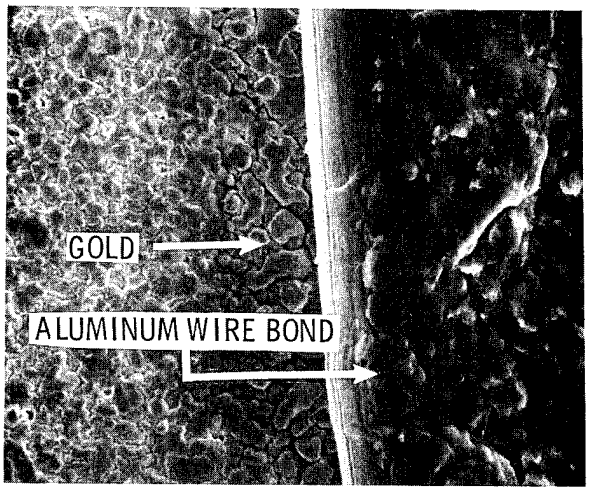


(a) Ductile Failure 600X

1500X

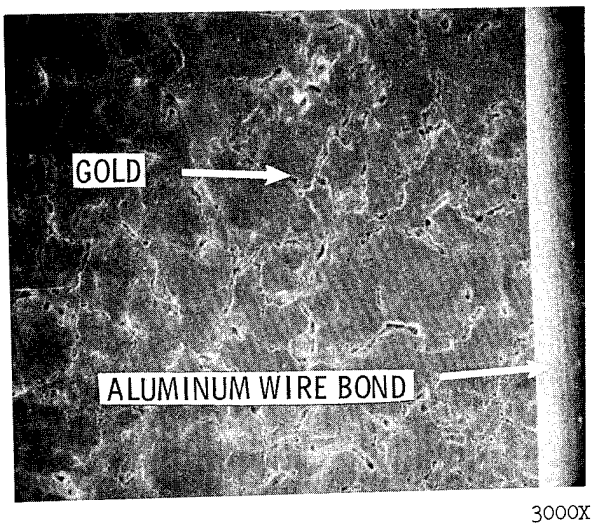
(b) Brittle Failure

Figure 5. Ductile Failure vs Brittle Fracture



(a) CrAu - 1% Si-Al 3000X

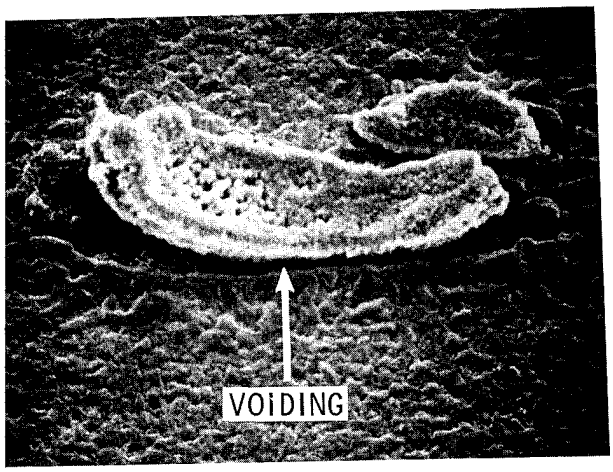
Figure 6



3000X

(b) TiPdAu - 1% Si-Aℓ

Figure 6. CrAu Metallization vs TiPdAu Metallization After 300°C, 1000 hrs.

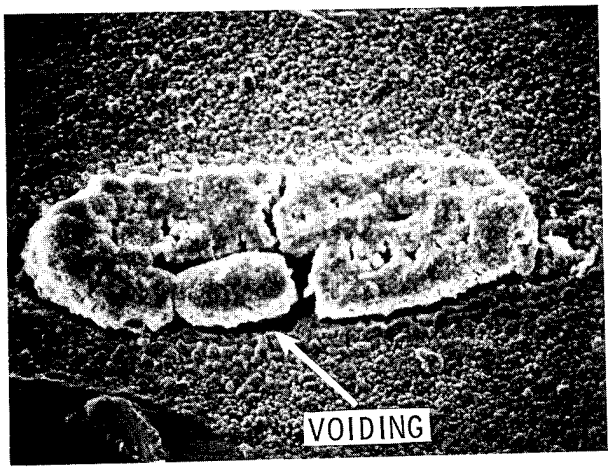


1000X

(b) TiPdAu - 1% Si-Aℓ After 300°C for 1000 hrs.

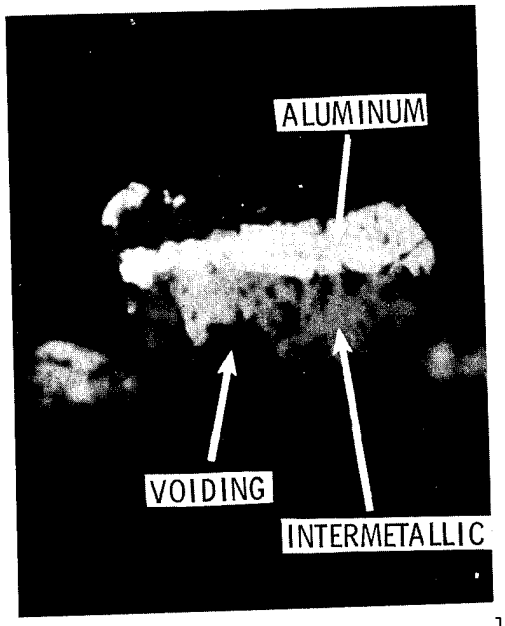
Figure 7. Intermetallic Formations

metallization in the region of the intermetallics. Figure 7 shows the results of this etch. Both systems show that the gold around the bond perimeter has been used up in forming the intermetallics. An Auger analysis in the TiPdAu sample revealed that palladium is exposed under the intermetallic nugget. From these scanning electron microscope pictures (which are typical examples) taken at 1000X, it can be seen that a bond was achieved over a smaller area for the TiPdAu than for the CrAu, and that the former appears to be a stress condition that caused a curling, further reducing the bond area. Figure 8 shows a cross section of an aluminum wire bond on the CrAu metallization. As expected, the voiding and intermetallics can be plainly seen.



1000X

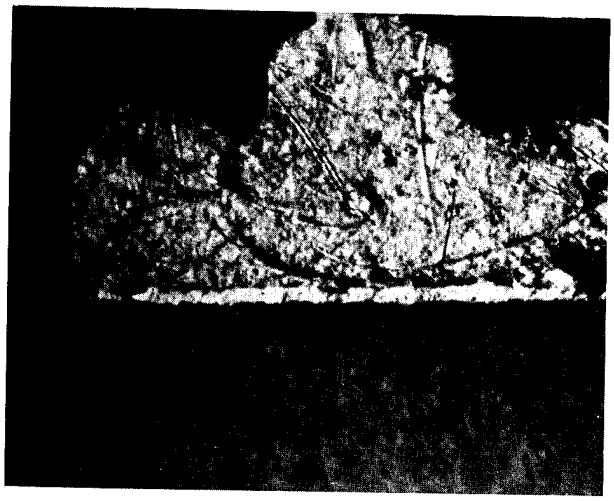
(a) CrAu - 1% Si-Aℓ After 300°C for 1000 hrs.



1000X

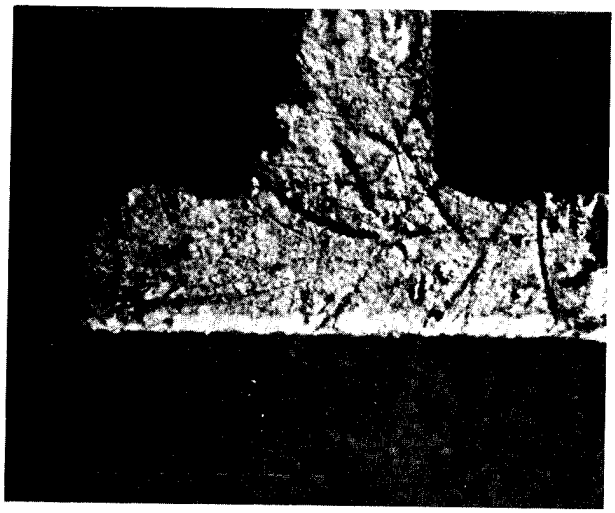
Figure 8. Au-Aℓ Intermetallic Formation

There appeared to be no difference in the formation of the intermetallics using stabilized gold wire and unstabilized gold wire as seen in Figure 9. Both of the bonds in Figure 9 were exposed to 200°C for 1000 hours. The intermetallic growth appears to be equivalent. Figure 10 shows scanning electron microscope pictures of the ball and wedge bonds after 300°C for 1000 hours This loop was electrically open before pull testing and pulled at less than a gram.



600X

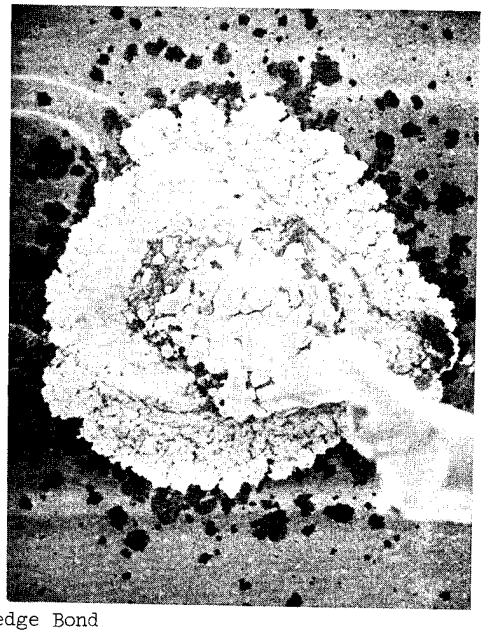
(a) Stabilized



600X

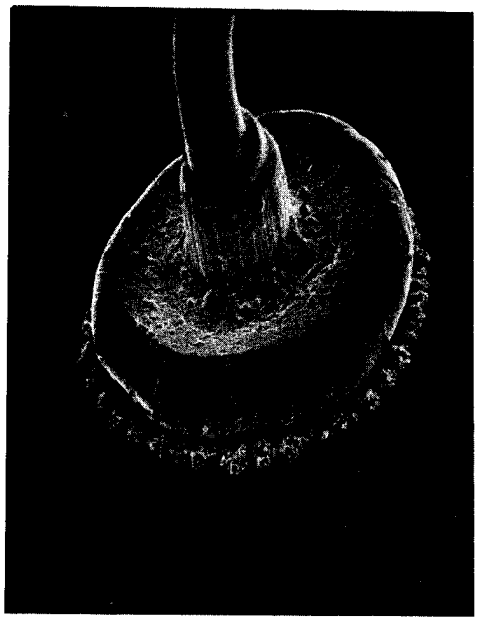
(b) Unstabilized

Figure 9. Bonds of Stabilized vs Unstabilized Gold Wire



600X

(a) Wedge Bond



400X

(b) Ball Bond

Figure 10. Gold Bonds After 300°C for 1000 hrs.

Conclusions

Based on the pure gold and aluminum activation energy for the formation of intermetallics calculated by Philofsky[7] (19.5 Kcal/mole), we selected 1000 hours at 300°C as an accelerated life condition to simulate the minimum twenty-years systems performance required at Sandia Laboratories. The condition of time and temperature extrapolates out to an order of magnitude worse than twenty-years at room temperature. Additional conditions of temperature, temperature cycling and times were added to provide progressive information of the effects of these environments on the bonds of the systems considered. The following conclusions were reached based on this evaluation.

1. Electrical resistance of the bonds for the CrAu Aℓ 1% Si are TiPdAu - Aℓ 1% Si metallization systems will probably become the controlling factor long before the mechanical integrity of the bonds is a concern.

2. Of the systems evaluated, the CrAu-Aℓ 1% Si yielded the best results for the environments selected.

3. The systems using Aℓ 1% Mg were more erratic and showed considerable degradation after environments. The TiPdAu - Aℓ 1% Mg system gave the poorest results of all the systems tested.

4. The high temperature storage at 200°C and 300°C result in electrical open circuits for both types of gold wire bonded to aluminum metallization.

5. In the bimetallic systems studied it appears that there are many variables beyond the basic metallization systems that effect bond stability. Although the means of the bond data took definite trends, the raw data showed wide variations from one bond or substrate to another for samples that had seen the same environment, perhaps indicating multiple mechanisms for bond degradation.

6. The gold aluminum intermetallics can be formed without the presence of silicon, but it appears that the

metallurgical structure of the intermetallics can be significantly different for each system.

Where possible, a monometallic interconnect will be used in the Sandia Laboratories hybrid microcircuits, preferably gold to gold. However, where this is not possible, this study indicates the greatest bimetallic interconnect stability will be achieved using CrAu metallization and Aℓ - 1% Si wire.

Due to the apparent sensitivity of the bond stability to variations in added alloys and perhaps small concentrations of contaminents, it is advisable to run an evaluation of any specific gold-aluminum interconnect system prior to incorporation into product. This evaluation should include mechanical and electrical evaluation of the interconnect after exposure to the equivalent of times and temperatures that are required by the next assembly. Data extrapolation from independent similar systems could be misleading.

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METALLURGICAL ASPECTS OF ALUMINUM WIRE BONDS TO GOLD METALLIZATION

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Abstract

A study is made of the intermetallics which form when aluminum wire is ultrasonically joined to thin and thick film gold metallizations and stored for extended times at moderate temperatures. Conclusions are reached concerning the effects of conductor surface topography, thickness, and purity on bond reliability.

Introduction

Two of the authors have recently published papers[1,2] which discuss aluminum ultrasonic wire bonding to gold metallizations on hybrid substrates. Their work indicated that aluminum wire bonding to gold metallizations can be satisfactorily achieved if consideration is given to certain heat aging effects. These papers discussed the effects of temperature on two thick film systems (Owens-Illinois 99+ and EMCA 212B) and a conventional nichrome, nickel, and gold thin film system. These systems were chosen for investigation because of previous usage. This paper will give the metallurgical aspects of their findings.

In the experiments conducted, a wire bond test pattern was generated which contained 128 bond sites (Figure 1). After controlled wire bonding, initial resistance measurements were made and the pull strength destructively measured for 25 bond pairs. The remaining loops on the substrate were then conditioned at the following temperatures; 25, 75, 125, 150, 160, 175 and 200°C for 168 hours in an air circulating oven. At the conclusion of the storage cycle, the bond resistance was measured and another 25 bonds pulled and the break mode noted.

To explain the changes observed in break mode, pull strength, and bond resistance data, the remaining bonds on the stored samples were microsectioned, photographed with high resolution optical and scanning electron microscopes, and quantitatively analyzed using an Energy Dispersive X-ray Spectrometer (EDS). The results from the pull tests and resistance measurements shown in Figures 2, 3, 4, and 5 will be explained in terms of the metallurgical changes which occur with temperature.

Preparation of the Wire Bond Microsections

The substrates with the remaining bonds were potted in Shell Epon 815 epoxy resin and given a slow cure at room temperature to eliminate additional temperature exposure during the curing. The bonds were then sectioned lengthwise in order to expose a larger cross section. Standard metallographic procedures were used to grind and polish the samples with the exception of the final polish. The final polishing was done with 0.05 micron alumina using additional water for an extended period. This polishing procedure tended to round off the cross sections because of the hardness of the alumina substrate compared to the aluminum and gold. However, it was beneficial in that it provided surface relief which aided in distinguishing the intermetallics. Etching of the cross sections was not necessary with this procedure and in the case of the SEM samples, it was not desired since a smooth surface is required for quantitative analysis. Final preparation for the SEM samples consisted of the deposition of approximately 200Å of carbon for preventing charge buildup.

Evaluation of the Microsections

The sectioned bonds were first examined optically at magnifications up to 1500X and selected samples in the SEM up to 20,000X. For each substrate sample at least a dozen wire bonds were inspected. Table 1 is a compilation of the significant results from this investigation. (See Figures 8 through 11 for typical sections.)

There is a great similarity in the appearance of the three metallization systems. This is not unexpected since the same mechanisms responsible for growth of the intermetallic phases are present in all three materials.[3,4] However, these mechanisms are modified by the individual properties of the different systems. Initially the similarities will be examined followed by a discussion of the individual properties of each system which modify the growth of the intermetallics.

Similarities

Disregarding the lower temperatures for the moment, the greatest similarity in the three systems is the final condition of the bonds on the 200°C samples. These bonds are to a great extent isolated from the gold because of the cracks around the bonds. The volumetric expansion (pedestal effect) of the intermetallics which are formed at the elevated temperatures creates severe mechanical stress cracks at the vertical interface with the gold. This condition is expecially prevalent in the thick film samples because of the larger volume of gold under the bonds.

Another similarity is the temperatures at which the different intermetallics appear.

TABLE 1.

Summary of Optical and SEM Findings for the Three Gold Systems

	EMCA 212B	Owens-Illinois 99+	Honeywell Thin Film
Physical Characteristics	Rough, pitted gold surface. Irregular interface between gold and aluminum causes non-uniform intermetallic growth (Figure 6A).	Rough gold surface but not as pitted as EMCA 212B. Intermetallic growth is more uniform than for EMCA 212B (Figure 6B).	Uniform surface. Gold 1/3 the thickness of thick film conductors. Interface between gold and aluminum is uniform as well as intermetallic growth (Figure 6C).
Constituents and Energy Dispersive Spectrometer (EDS) Analysis	Thick film ink with frit for mechanical adhesion to substrate. The frit contains silicon, bismuth, and cadmium as major constituents. The concentration of bismuth was found to be higher at the intermetallic diffusion front than in either the intermetallic or the gold. Au_4Al, Au_5Al_2, AuAl, and $AuAl_2$ intermetallic phases identified with the AuAl and $AuAl_2$ not detectable for low temperatures.	Fritless thick film ink with copper additive for wetting the substrate. No other detectable impurities. The concentration of copper follows the same pattern as the bismuth in the EMCA 212B (Figure 12). Au_5Al_2, AuAl, and $AuAl_2$ intermetallic phases present but no Au_4Al. AuAl and $AuAl_2$ appear at the higher temperatures.	Gold over nickel and nichrome. No detectable impurities. Au_5Al_2, AuAl, and $AuAl_2$ intermetallic phases present in detectable quantities with AuAl and $AuAl_2$ appearing at the higher temperatures.
Temperature: 25°C	No detectable intermetallics.	No detectable intermetallics.	No detectable intermetallics.
75°C	Significant thickness of gold rich intermetallic visible Au_4Al (tan) (Figure 9A).	No detectable intermetallics (Figure 10A).	No detectable intermetallics (Figure 11A).
125°C	Visible lateral voiding and annular cracks at gold interface. Visible elevation of bond above surface of gold due to volumetric expansion of intermetallic. Second gold rich phase appears Au_5Al_2 (tan) (Figures 8A, 8B and 9B).	First gold rich intermetallic phase appears. Identified as same phase which appears at this temperature for the EMCA 212B (Figure 10B).	First gold rich intermetallic phase appears. Identified as same phase which appears at this temperature for the EMCA 212B (Figure 11B).
150°C	Consumption of gold continues with associated increase in lateral voiding, annular cracks and bond elevation. Au_4Al narrowed to thin line by growth of Au_5Al_2 when supply of gold to intermetallic has been limited by voiding.	Intermetallic continues to consume gold.	Gold under the bond consumed if lateral voiding has not occurred. Some annular cracking and lateral voiding observed.
160°C	The gold under the bond is consumed if lateral voiding has not occurred. The width of the Au_4Al and Au_5Al_2 are approximately equal. A fine line of a third intermetallic phase appears at the aluminum interface, identified by coloration as $AuAl_2$ (purple) (Figure 9C).	Annular cracking becomes visible with elevation of the bond above the surface of the gold. $AuAl_2$ appears to be present as a fine line at the aluminum interface (Figure 10C).	Visible elevation of the bond above the gold surface with an increase in the annular cracking. $AuAl_2$ appears to be present as a fine line at the aluminum interface (Figure 11C).
175°C	AuAl (white) phase appears and width of $AuAl_2$ increases to a clearly defined band. Extensive annular cracking and lateral voiding cause slowdown in the growth of the Au_4Al and Au_5Al_2. Au Al reduced to a narrow band adjacent to the diffusion front on all samples (Figures 8C and 9D).	AuAl phase appears and width of $AuAl_2$ increases. Some lateral voiding found at gold interface where initial intermetallic diffusion front was irregular. Annular cracking continues to increase (Figure 10D).	AuAl phase appears and width of $AuAl_2$ increases. The increase in annular cracking with growth of the intermetallics continues (Figure 11D).
200°C	Width of aluminum rich phases increases, growing into both the bond and gold rich phases. Lateral voiding appears at aluminum interface. The width of $AuAl_2$ is approximately three times that of the AuAl (Figures 8E, 8F and 9E).	Width of aluminum rich phases increases, growing into both the bond and gold rich phases. Lateral voiding appears at aluminum interface. Gold under bond consumed if lateral voiding has not occurred. The width of the $AuAl_2$ is approximately twice that of the AuAl and one-half the width of the $AuAl_2$ in the EMCA 212B samples (Figures 8D and 10E).	Width of aluminum rich phases increases, growing into both the bond and gold rich phases. The AuAl and $AuAl_2$ phases are each about one-half the width of the $AuAl_2$ phase in the EMCA 212B (Figure 11E).

At 125°C Au_5Al_2 appears in all three samples, while at 175°C both AuAl and $AuAl_2$ appear in detectable amounts.

A third, and most significant similarity, is the presence of lateral voiding when the diffusion front into the gold is nonuniform. The irregular diffusion front enhances the formation of lateral voiding and is related to the initial surface texture of the gold.

Differences

EMCA 212B - EMCA 212B is a gold metallization which is characterized by a rough and porous surface. This appearance is caused by the melting of the frit during the firing process (see Figure 6A). The rough surface causes spotty bonding and significantly contributes to the irregularity of the diffusion front.

At the relatively benign temperature of 75°C, a significant thickness of Au_4Al has formed which was not detected in the other systems at any time, indicating a lowering of the activation energy for this intermetallic. (See Table 2.)

up of bismuth at the diffusion front of the intermetallic as it grows into the gold. The presence of the impurities (bismuth, cadmium, and silicon) from the frit appears to contribute to the formation of the voiding at the gold interface and enhances the growth of the intermetallics, e.g., the presence of Au_4Al at 75°C and the appearance of Kirkendall voiding at 125°C. This is the first direct verification of the Horsting impurity enhanced voiding mechanism.[5]

Owens-Illinois 99+ - The surface of the Owens-Illinois 99+ is somewhat smoother than the EMCA 212B but still has some irregularity in the diffusion front, which contributes to nonuniform growth (see Figure 6B). The growth of the intermetallics is slower than with the EMCA 212B and less lateral voiding occurs under the bond. As with the impurities in the EMCA 212B, an analysis of the 99+ constituents detected a higher concentration of copper at the intermetallic-gold interface than in either the intermetallics or the gold. Figure 12 shows a qualitative comparison of the copper concentration in the three regions. The copper has the beneficial

Table 2. Phase Identification Versus Temperature for EMCA212B, Owens-Illinois 99+, and Honeywell Thin Film

	EMCA 212B							O.I. 99+							HONEYWELL THIN FILM						
TEMP °C	25	75	125	150	160	175	200	25	75	125	150	160	175	200	25	75	125	150	160	175	200
PHASE																					
PURPLE ($AuAl_2$)	–	–	–	–	●	●	●	–	–	–	–	●	●	●	–	–	–	–	●	●	●
WHITE (AuAl)	–	–	–	–	–	●	●	–	–	–	–	–	●	●	–	–	–	–	–	●	●
TAN (Au_2Al)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
TAN (Au_5Al_2)	–	–	●	●	●	●	●	–	–	●	●	●	●	●	–	–	●	●	●	●	●
TAN (Au_4Al)	–	●	●	●	●	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Data for Table 2 was obtained from EDS analysis similar to those shown in Figure 7. In Figure 7 the variation in the peak heights for the $AuAl_2$ is due to the heterogeneous structure of this band. Aluminum is interspersed within the $AuAl_2$. The volume of X-ray emission overlaps into the aluminum, thereby producing the inconsistency from sample to sample.

The 125°C samples exhibited Kirkendall voiding and visible elevation of the bonds due to volumetric expansion of the intermetallics. Isolation of the bond has also started to occur at this temperature. This metallization system exhibits a rapid initial growth of the intermetallics followed by a slowdown as the Kirkendall voiding limits the diffusion of the gold into the intermetallic. Energy dispersive spectrometer analysis of the sectioned bonds indicates a build-

effect of slowing the growth rate of the intermetallics without contributing to the formation of voids at the diffusion front.[6]

Honeywell Thin Film - Of the three metallization systems, the thin film gold exhibits the most classical behavior. The intermetallic diffusion front is uniform and relatively void free under the bond. Even though the gold is consumed by 150°C, the peripheral cracking is not as severe because of the thinner gold.

Correlation of Findings with Previous Data

The similarity in the growth of the intermetallic phases exhibited by the three metallization systems is reflected in the general shape of the data graphs shown in Figures 2 through 4. Both the pull strength and percentage of bond lifts graphs are similar

in form and vary only in magnitude for a particular temperature. In interpreting these graphs with respect to the findings of Table 1, consideration must be given to the annealing of the wire. For instance, the downward trend of the pull strength curves with temperature is primarily due to the decreasing strength of the wire. The contribution of the changes in wire strength makes the interpretation of these graphs difficult. In spite of this difficulty, significant changes in the graphs can be related to the findings.

An attempt will be made to explain the behavioral changes by stepping through the temperature range of 25°C to 200°C and observing the effects on bonds to 212B gold. Similarities and differences in the graphs of the other two gold materials will then be discussed as they occur (reference Table 1).

25°C - Bond strength is approximately 12.5 grams or about 60 percent of the wire strength. No detectable intermetallics. Bond resistance, including wire loop, is approximately 80 milliohms. Bond break mode upon pulling to destruction is mostly heel breaks at the first bond, the normal place. Owens-Illinois 99+ and thin film bonds are similar except that the pull strength for 99+ is somewhat higher.

75°C - The increase in the pull strength (Figure 2), accompanied with the increase of the percentage of bond lifts is difficult to explain, especially since the graph indicates that the wire itself loses tensile strength due to annealing. The most likely explanation is that the annealing removes the stress from the heel area therefore strengthening the bond and relocating the breakage point to the next weakest area. The weak area appears to be at the wire to gold interface because of spotty bonding. On 99+ and thin film the annealing retained the original bond strength while the better bonding surface affects little or no increase in lifts. The bond resistance remains unaffected (Figure 5) because no separations have occurred.

125°C - The pull strength has decreased significantly, mostly due to the annealing effects of the wire, making the bond heel once more the weakest link in the system and reducing the number of lifts to zero. Even though the second intermetallic has appeared and voiding is present, the system has retained more mechanical strength than the wire (heel). The electrical resistance is not affected because only slight voiding has occurred.

150°C - The bond strength decline has leveled off indicating that no additional major changes have occurred. Resistance is still unchanged, percentage of bond lifts is still low, indicating the wire at the bond heel is still the weakest link in the system.

160°C - Major changes are now taking place. Lateral cracking has mechanically weakened the bonds and the break strength of the system sharply declines. The number of lifts increases, indicating separation within the intermetallic interfaces. Annular and lateral voiding now constitute a separation between the intermetallics and the gold around the bond. Therefore, the resistance begins to increase sharply.

175°C - Bond strength continues to decline. Mechanical weakness due to cracking and voiding has caused a large percentage of bonds to separate at these interfaces when pulled. Resistance of 212B bonds continues to climb sharply, indicating continuing separation. However, resistance increase in bonds to thin film and OI 99+ has leveled off. Apparently the presence of an impurity such as copper has delayed the formation of voids and cracks in 99+. In that case, the cracking is not continuous and the bond is not isolated. The resistance rise is, therefore, limited to a finite value. For the thin film, the resistance rise is only slight because of the presence of the nickel nichrome layer.

200°C - The bond strength remains constant, remaining at approximately 4 to 5 grams, deceptively adequate. But bond resistance has increased to values higher than 1 ohm, excessively high. Resistance of bonds to 99+ and thin film remain essentially stable at values seen at 175°C for the same reasons mentioned above. Bond lifts once more decrease sharply, apparently indicating a continuing reduction in the strength of the wire.

Summmary of Findings

The classical mechanisms responsible for the failure of thin film metallization systems (Au or Al) are exaggerated with thick or thin film systems on ceramic substrates. Interpretation of the aforementioned data is summarized as follows:

1. The relatively thick gold used on ceramic substrates produces greater volumetric expansion and mechanical stress at the intermetallic interfaces of the bond when subjected to elevated temperatures. Because of the thick gold, there is also a higher incidence of Kirkendall voiding occurring at the gold-intermetallic interface prior to the depletion of the gold under the bond.

2. Impurities included in 212B thick film frit enhance intermetallic formation and voiding at the gold-intermetallic interface. This leads to the rapid growth of the intermetallics at relatively low temperatures.

3. Rough, porous surfaces associated with thick film inks may cause spotty bonding and a nonuniform intermetallic growth. This condition also increases the risk of voiding and cracking due to the increased stress at the interface.

4. Cracks which form around the bonds tend to isolate the conductor from the bond and thereby increase the electrical resistance.

5. Copper as an additive to thick film inks is not as detrimental to bond integrity as frit since it tends to inhibit the formation of the intermetallics for a given temperature.

Recommendations

As advice to the potential user of aluminum wire bonds to thick and thin film gold systems, it is recommended that consideration be given to the compatibility of materials

when subjected to temperature aging. Each system that is intended for use should be thoroughly qualified through a series of tests as indicated in this paper. It is realized that there are many wire manufacturers and many different methods for forming the gold metallization. Thus, to arrive at universal conclusions is difficult. However, the following guides are presented based upon the metallization systems considered herein.

1. It appears that 212B and similar fritted gold pastes should not be used in applications where extended periods of time above 125°C are experienced.

2. For applications at temperatures above 125°C and extended periods, Owens-Illinois 99+ or similar fritless gold pastes or thin film gold appear reasonable alternatives.

3. For high reliability applications at high temperatures, the use of gold wire rather than aluminum is recommended.

4. Bond pull tests alone are a necessary but not sufficient evaluation tool in determining the reliability of a bonding system. Pull testing and resistance measurements after heat aging are a necessity. Sectioning of samples will yield additional information on what changes are taking place.

5. Intermittent burn-in, on-off cycling, or temperature cycling after burn-in will provide an additional test of bond integrity.

References

1. "Changes in Strength and Resistance of Aluminum to Gold Ultrasonic Bonds After Temperature, Electrical, and Environmental Stress", R. G. Oswald, W. R. Rodrigues de Miranda and C. W. White; International Society of Hybrid Microelectronics, Proceedings of, 1975.

2. "Changes in Strength and Resistance After Burn-In of Aluminum Wire Bonds to Thick and Thin Film Gold", W. R. Rodrigues de Miranda and R. G. Oswald; International Society of Hybrid Microelectronics, Proceedings of, 1974.

3. "Purple Plague Revisited", E. Philofsky; Solid State Electronics 13, 1391, 1970.

4. "Kinetics of Phase Formation in AuAl Thin Films", S. U. Campisano, et al; British Philosophical Magazine, May 1975.

5. "Purple Plague and Gold Purity", C. W. Horsting, Reliability Physics Symposium, 1972.

6. "Gold Thick Film Conductors For Aluminum Wire Bonding", J. B. Prather, S. D. Robertson, and J. W. Slemmons, International Microelectronics Conference (IMC 1974 West), February 1974.

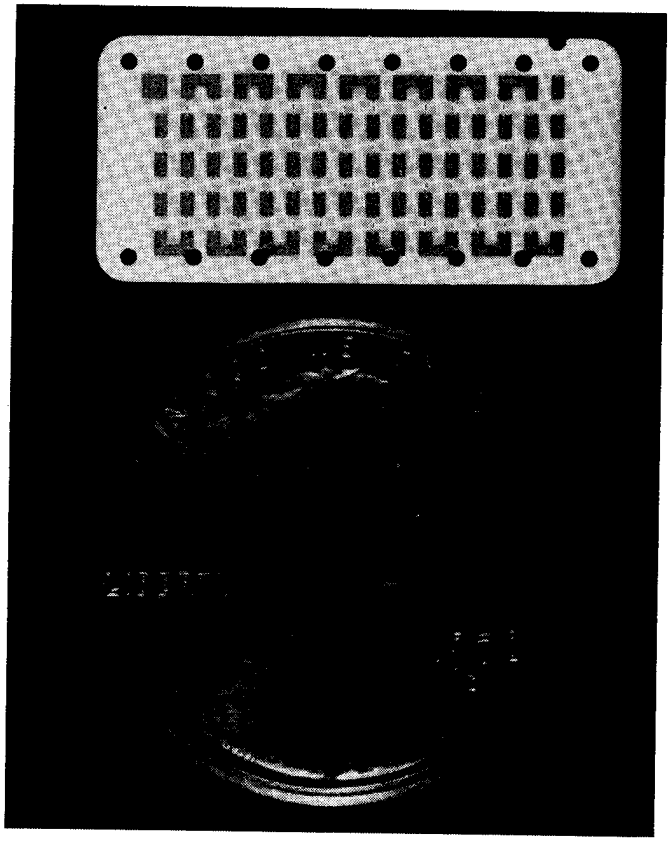


Figure 1. Wire Bond Test Substrate

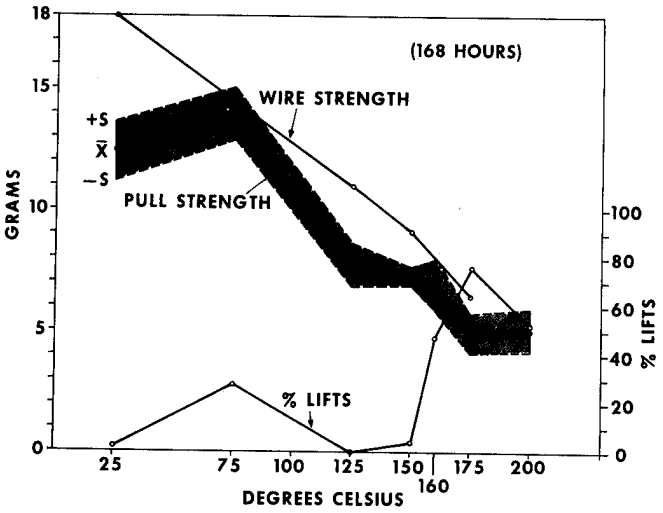


Figure 2. Pull Strength, Percentage Bond Lifts and Wire Strength as a Function of Storage Temperature (EMCA 212B)

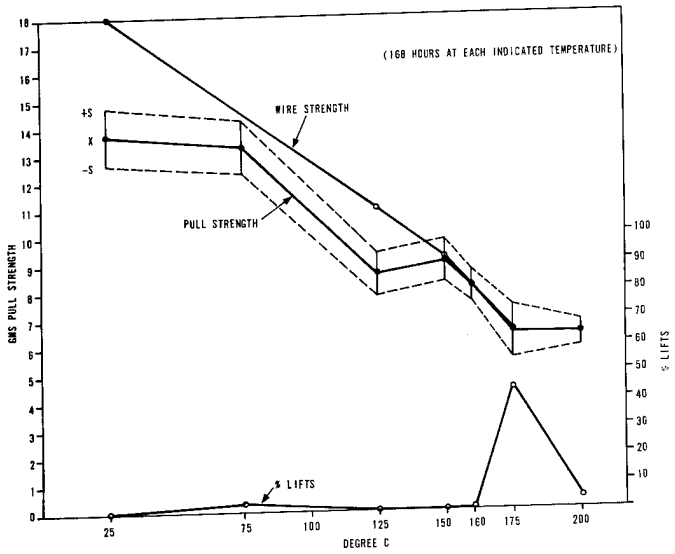


Figure 3. Pull Strength, Percentage Bond Lifts and Wire Strength as a Function of Storage Temperature (O.I. 99+)

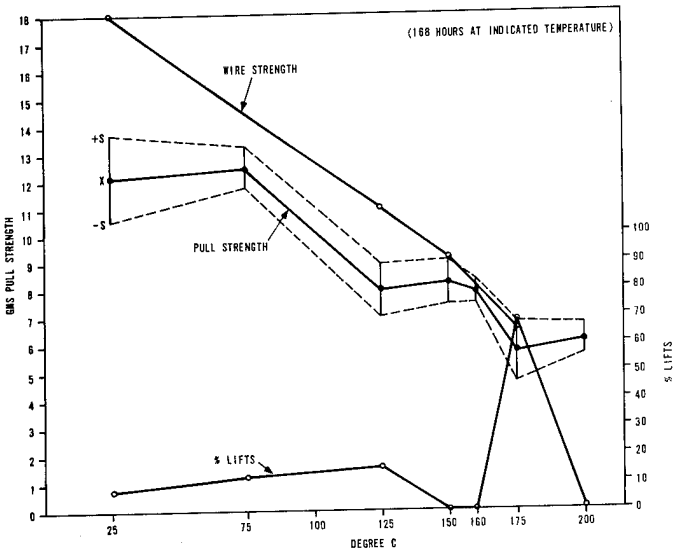


Figure 4. Pull Strength, Percentage Bond Lifts and Wire Strength as a Function of Storage Temperature (Thin Film)

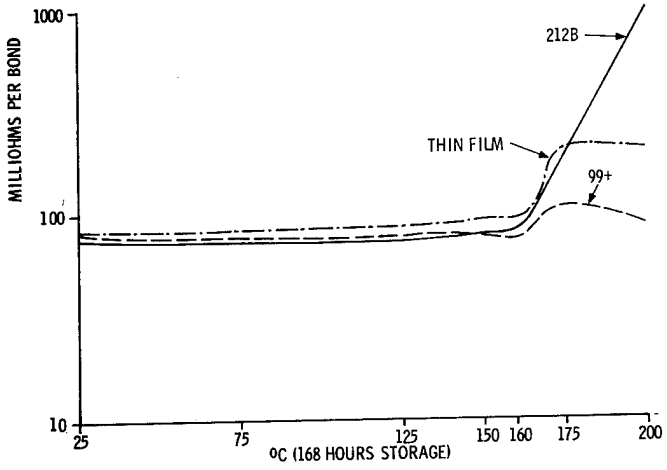
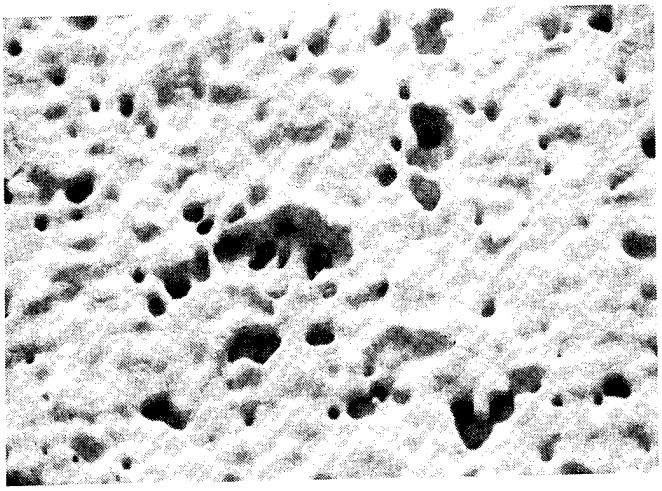
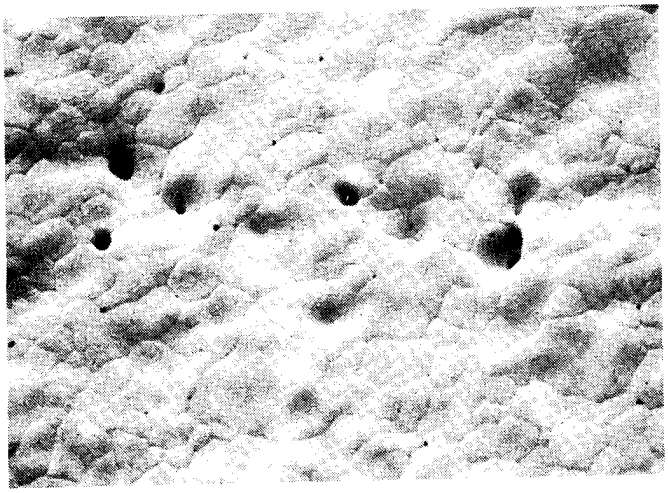


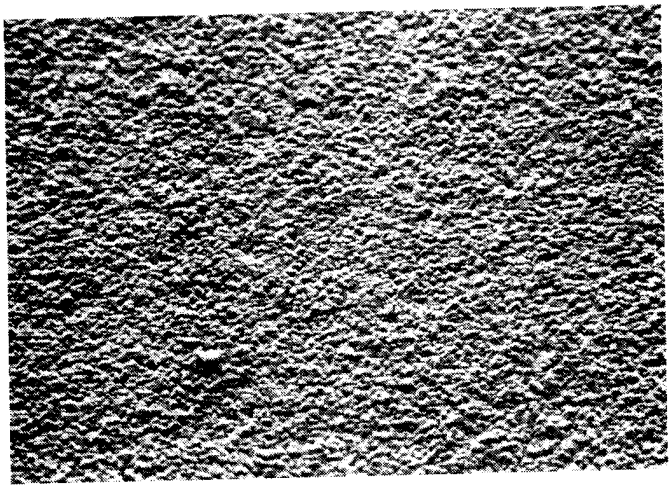
Figure 5. Bond Resistance as a Function of Storage Temperature (Average Value per Bond of 36-60 Bond Loops in Series)



A. EMCA 212B



B. 0/1 99+



C. THIN FILM

Figure 6. SEM Photographs Showing the Surface Texture of the Three Gold Metallization Systems (500X)

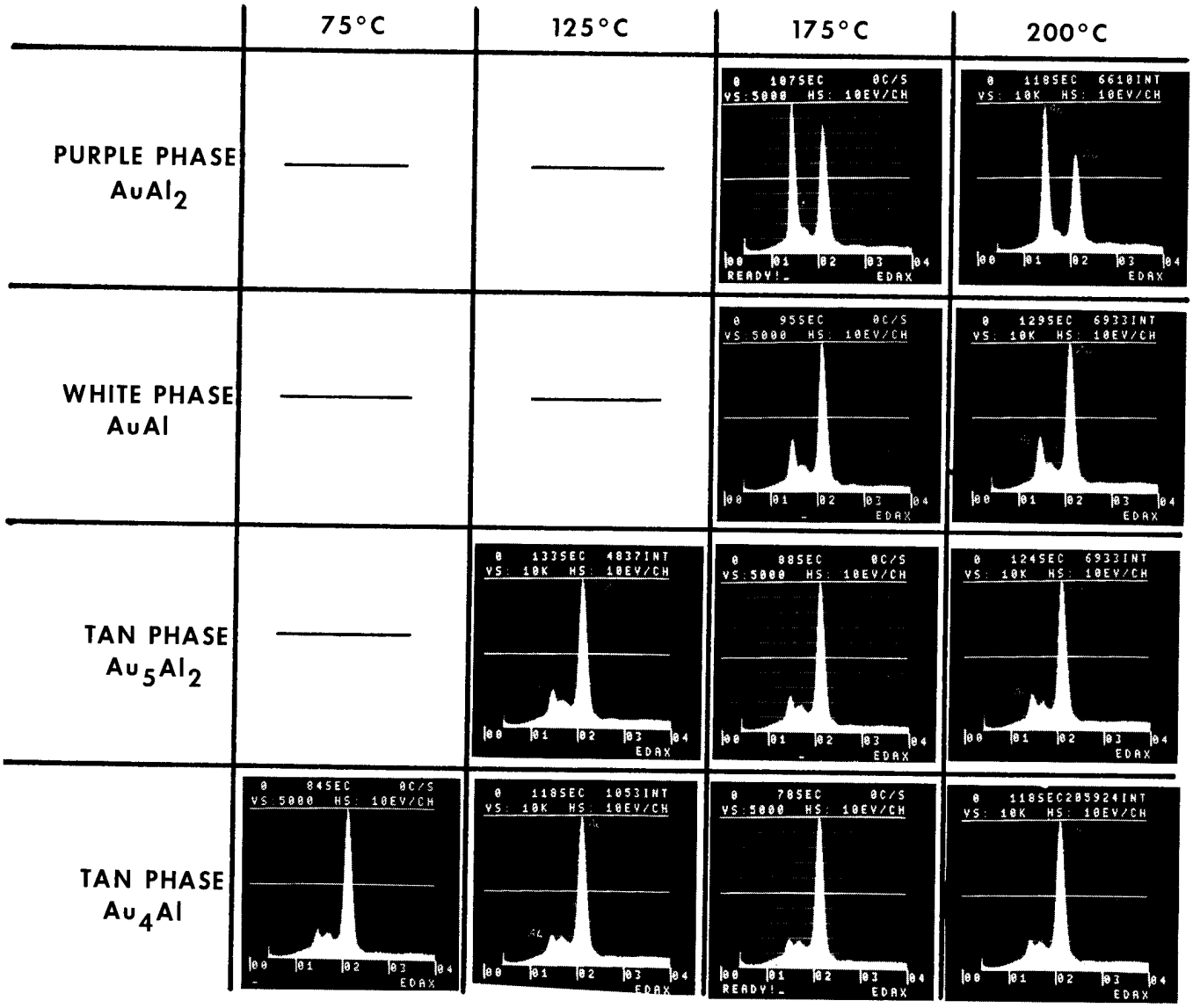
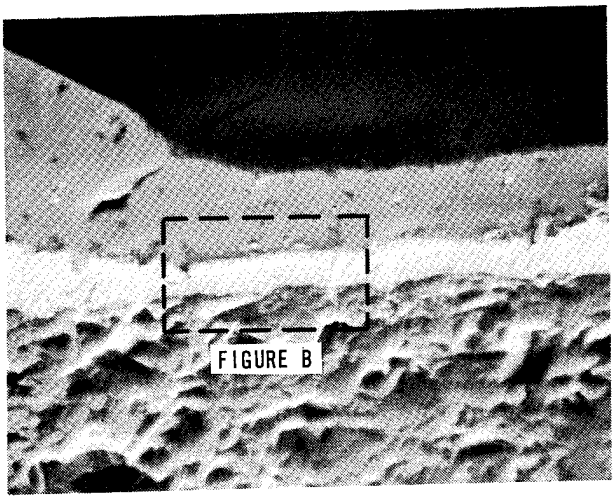
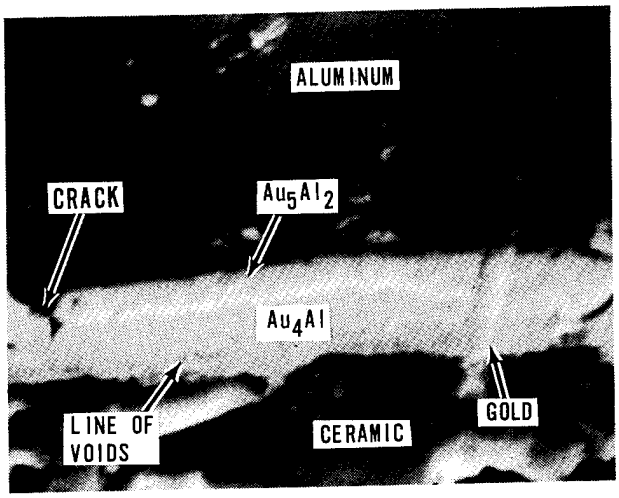


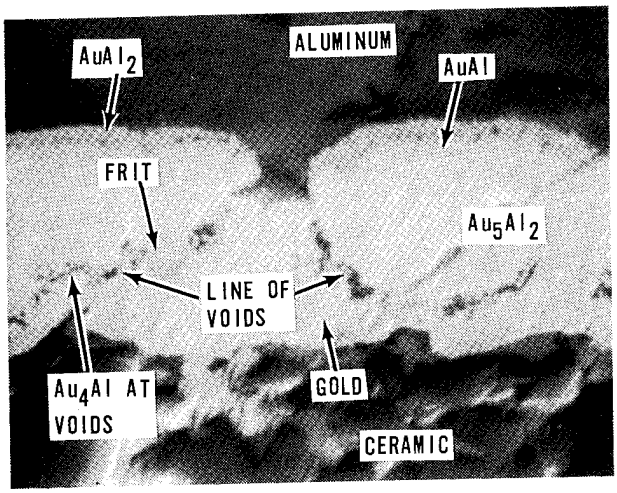
Figure 7. Intermetallic Phase Identification Versus Temperature for the EMCA 212B Metallization System)



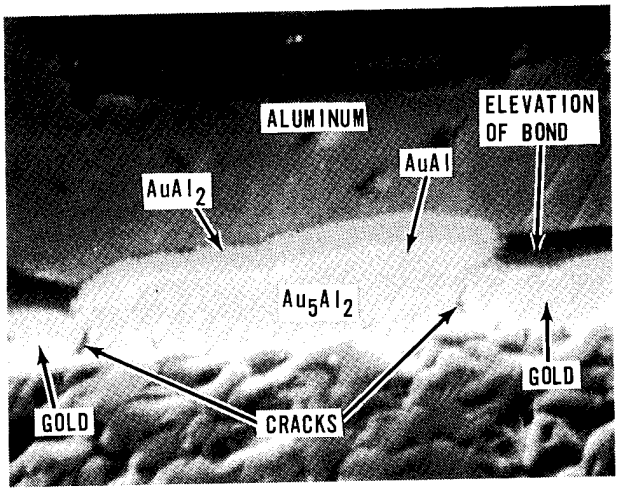
A EMCA 212B 125°C



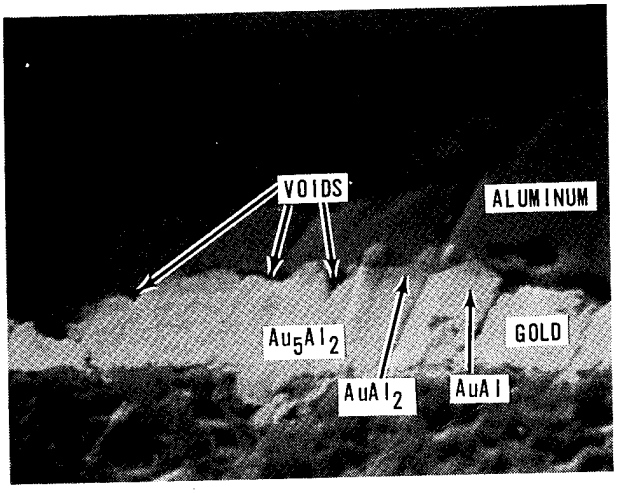
B EMCA 212B 125°C



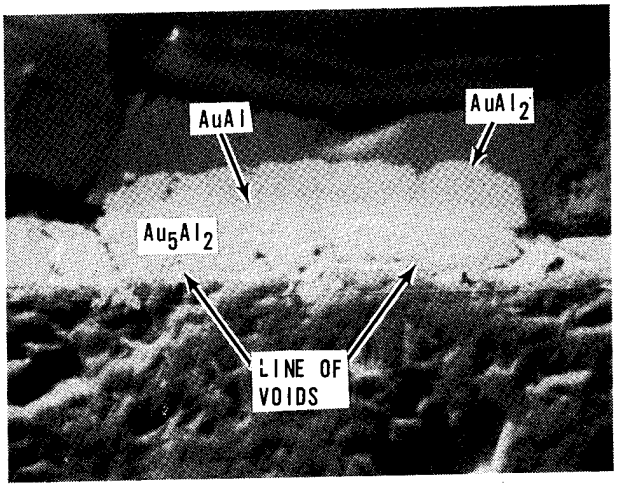
C EMCA 212B 175°C



D 01 99+ 200°C



E EMCA 212B 200°C



F EMCA 212B 200°C

Figure 8. SEM Photographs of Typical Microsectioned Bonds

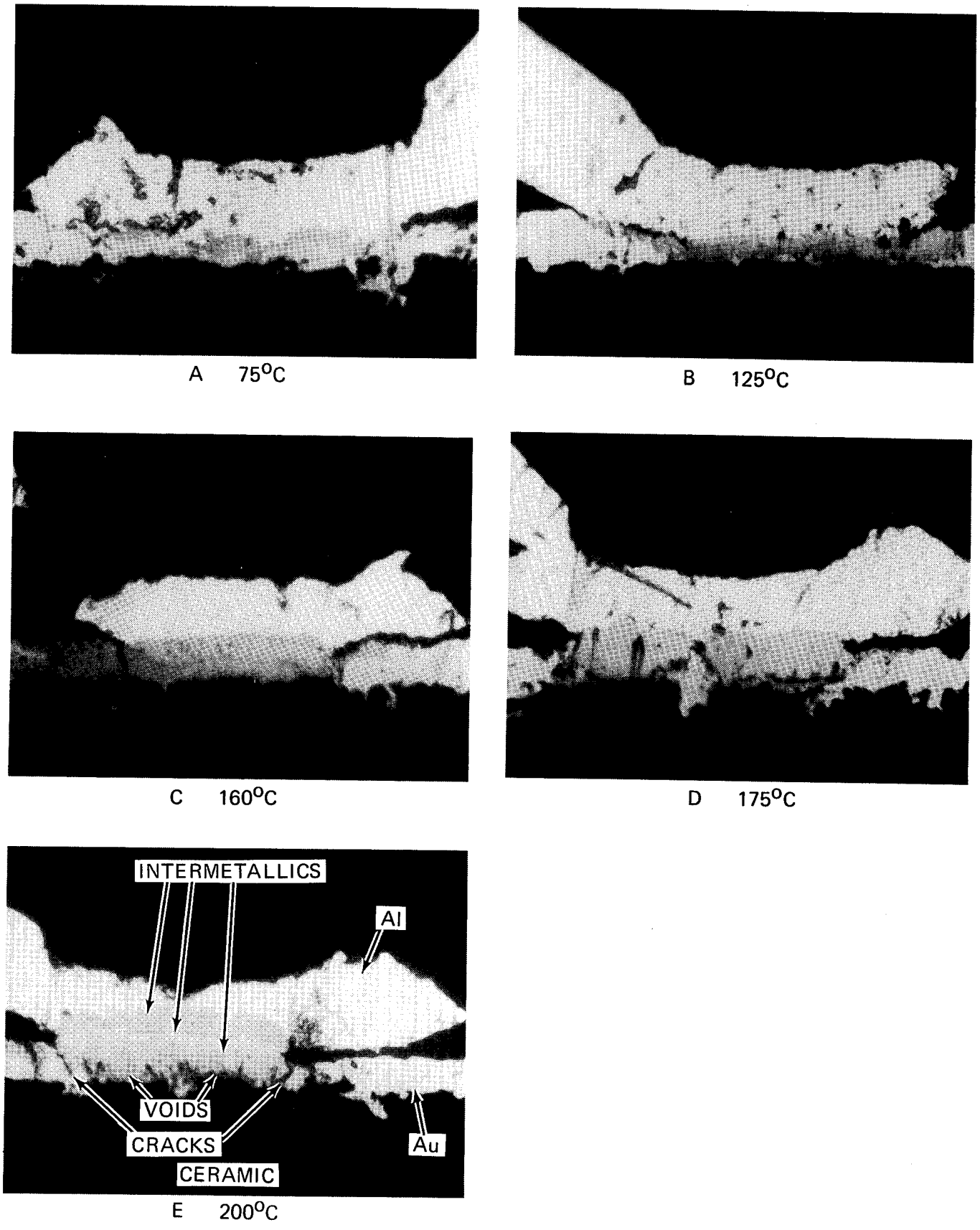
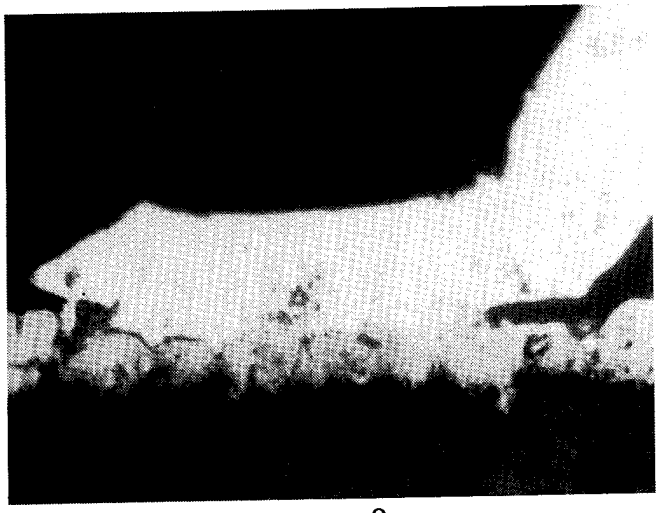


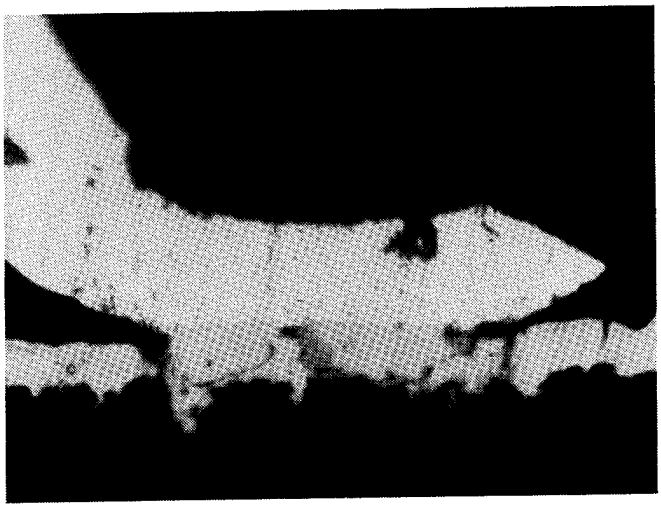
Figure 9. Cross-sections of Aluminum Wirebonds to EMCA 212B Gold Metallization After 168 Hours Storage at the Designated Temperature



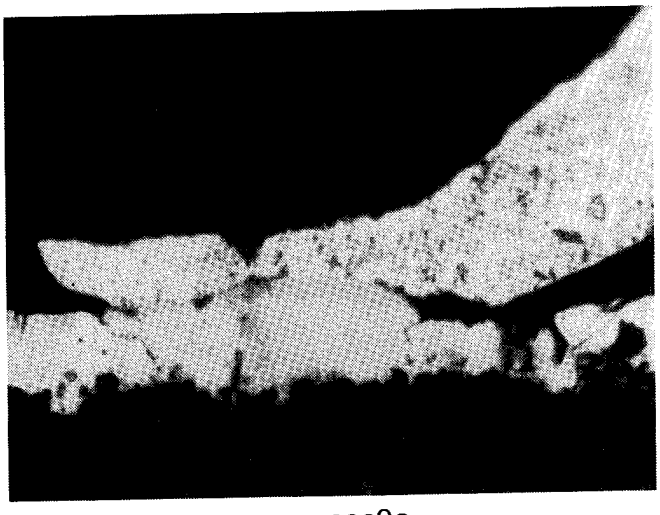
A 75°C

B 125°C

C 160°C

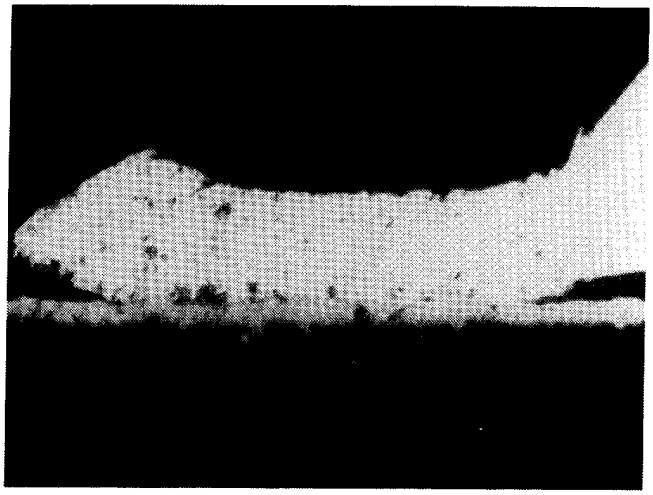


D 175°C

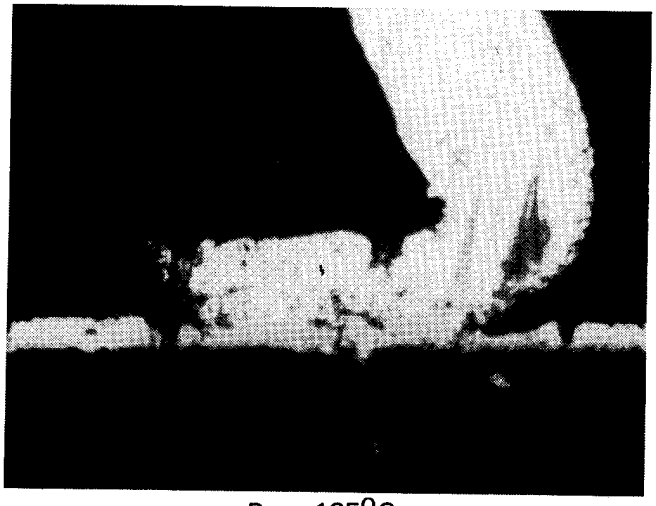


E 200°C

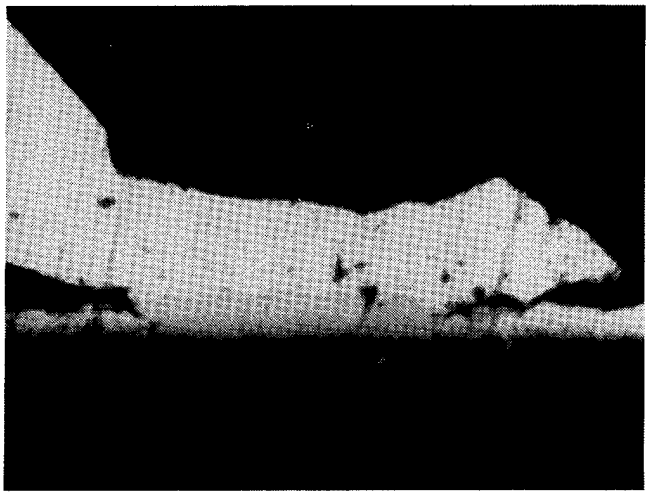
Figure 10. Cross-sections of Aluminum Wirebonds to Owens Illinois 99+ Gold Metallization After 168 Hours Storage at the Designated Temperature



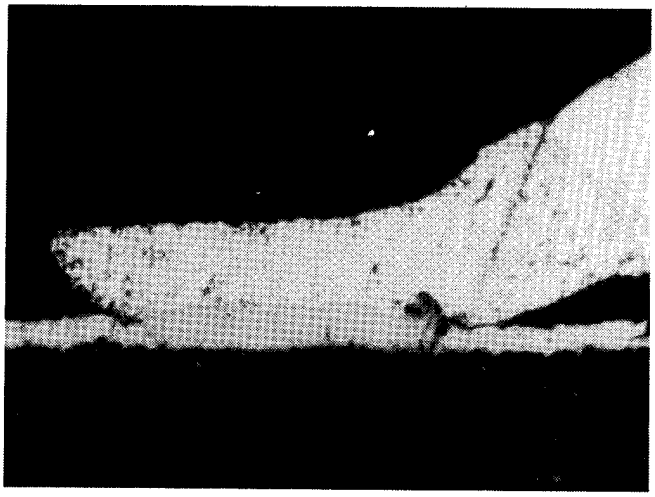
A 75°C



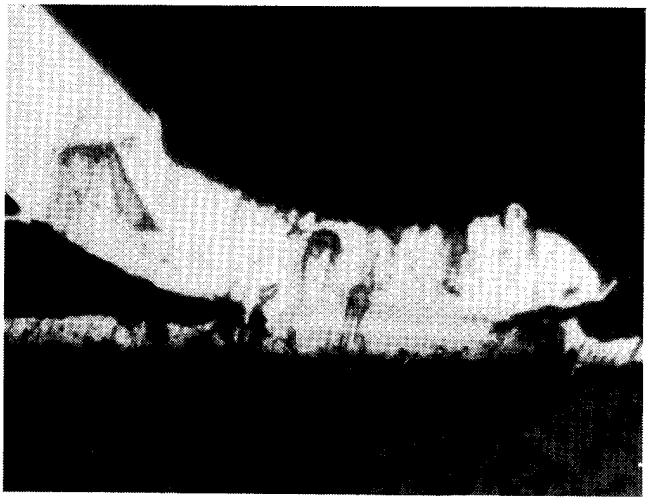
B 125°C



C 160°C

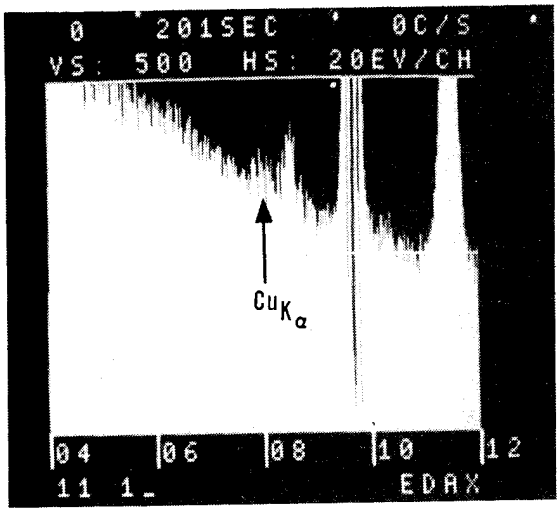


D 175°C

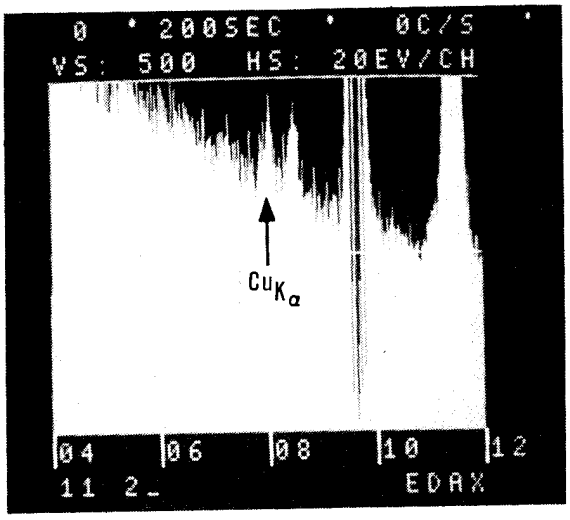


E 200°C

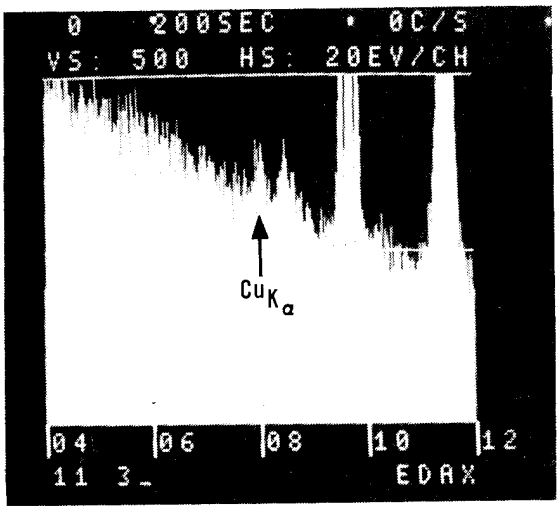
Figure 11. Cross-sections of Aluminum Wirebonds to Honeywell Thin Film Gold Metallization After 168 Hours Storage at the Designated Temperature



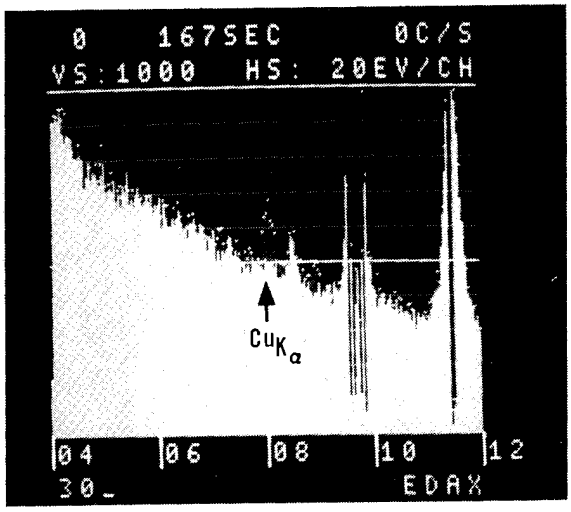
NO. 1. Cu CONCENTRATION IN THE INTERMETALLIC OF OI 99+



NO. 2. Cu CONCENTRATION AT THE Au INTERMETALLIC INTERFACE OF OI 99+



NO. 3. Cu CONCENTRATION IN THE Au OF OI 99+



NO. 4. COMPARISON OF Cu CONCENTRATION IN THE INTERMETALLIC AND AT THE INTERFACE. DOTS DENOTE THE INTERMETALLIC INTERFACE SPECTRUM

FIGURE 12. ENERGY DISPERSIVE SPECTRUMS OF THE OWENS ILLINOIS 99+ METALLIZATION SYSTEM SHOWING THE VARIATION IN THE COPPER CONCENTRATION ACROSS THE BOND INTERFACE

INVESTIGATION INTO FAILURES OF Al WIRES BONDED TO Au METALLIZATION IN MICROSUBSTRATES

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Abstract

The morphology and microstructural characteristics of Al-wire bond to Au metallization in microsubstrates was investigated by SEM, electron probe and Auger spectroscopy. It is shown that the ultrasonic bonding creates an interaction zone about 5 μm deep. Low bond strength and failure of the bond after H_2 soldering cycle is attributed to impurities in the Au inks. These impurities form brittle intermetallics with Al and brittle, readily reducible, low melting glasses.

Introduction

The deterioration of Al wire-Au metallization bonds have been the subject of many recent investigations.[1-5] More references to this problem can be found in each of the cited above. There is no full agreement on the mechanisms of failure. However, most authors agree that bond failures result from the formation of intermetallic compounds in the Au-Al system. It is to be noted that the works cited above were concerned with time-temperature effects on bond reliability. Usually, well bonded Al wire to Au metallization exhibit deterioration after a prolonged exposure at a relatively low temperature. The work reported here examines failures of bonds that occur throughout, or immediately at, the end of the production cycle. The purpose of this investigation was, thus, to analyze and provide failure mechanism(s) for Al wire ultrasonically bonded on thick film Au metallization in a microsubstrate (Fig. 1). This substrate is a part of a hybrid RPC unit.

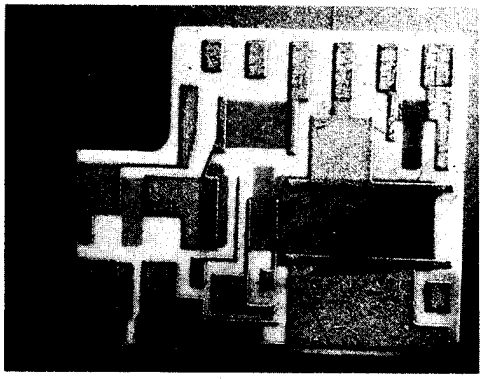


Fig. 1. Microsubstrate, 5X

The manufacturing steps are as follows:

a) A layer of 10 μm (0.4 mils) of "fritted" Pt-Au (DuPont 9596 ink) is defined by a screen printing process over Al_2O_3 substrate. The metallization is then sintered in air at 900°C for about 10 min.

b) A second layer of 10 μm "frittless" Au (EMCA 3264 ink) is defined over the Pt-Au and again sintered in air at 900°C for 10 min.

c) Oxide resistors are defined in certain locations on the substrate in air at 850°C for 10 min.

d) Leaded glass ("glaze") is layed over the substrate in defined areas and sintered in air at 650°C for 2-4 min.

e) Transistors are eutectically bonded to the Au metallization.

f) 0.003" Al-1 Mg wire is ultrasonically bonded to the transistors and to the metallization. This was done on a model 484 K and S ultrasonic bonder using a microswiss wedge tool.

g) Bond strength is tested by standard "pull-strength" method.

h) The substrate is processed in Hz atmosphere in two steps, 10 min at 275°C and 10 min at 245°C for application of solder to the external tabs.

i) Bond strength to the substrate is again tested. Severe deteriorations of bond strengths was observed at this stage. This was then the incentive for investigation reported in this paper.

Results

Typical data of bond strengths are shown in Table I. All bond lifts occurred on the metallization. The data demonstrated clearly severe deterioration in bond strength following the H_2 atmosphere firing stage (step h above).

Table I

Bond* Strength Data

0.003 Al wire, microswiss tool wedge (maximum load 30 g)

As Bonded	After 10 min in H_2 at 275°C	After Additional 10 min in H_2 at 245°C
30 NF	10 BL	9 BL
30 NF	2 BL	4 BL
28 BL	1 BL	6 BL
30 NF	30 NF	28 BL
30 NF	3 BL	4 BL
30 NF	5 BL	5 BL
30 NF	22 BL	5 BL
20 BL	8 BL	4 BL

NF: No Failure; BL: Bond Lift

*Bonding parameters: Power - 6; Time - 4; Load - 65 g

At this point, the investigation was directed towards a complete metallurgical characterization of the metallization and wire-metallization bond interfaces. This study utilized chemical analysis, scanning electron microscopy (SEM), equipped with "EDAX" X-ray analyzer, electron microprobe analysis, and scanning Auger spectroscopy.

Spectrographic chemical analyses of the two gold inks are shown in Table II. One should note the high content of Bi and Pb in the 9596 ink. Also note that the ink contains about 3% Pd. The 3264 ink is relatively clean. Bi and Cd are present in small amounts along with Cu.

Table II

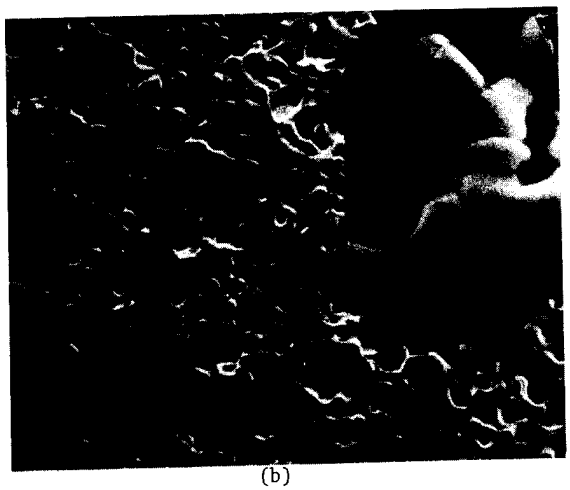
Spectrographic Analysis of Au Inks
Results in wt%; Accuracy 1/3 to X3 Amount Reported

	Al	Ag	B	Bi	Ca	Cd	Co
Au-Pt DuPont 9596	0.08	0.01	0.05	5%	0.2	0.1	0.01
	Cr	Cu	Fe	Mg	Pd	P	
	0.01	0.005	0.04	0.02	3%	0.1	
	Pt	Mo	Nb	Ni	Pb	Sb	
	∿10%	< 0.01	< 0.01	< 0.01	0.8	< 0.01	
	Si	Sn	Ti	Zn	Zr		
	0.4*	< 0.01	0.01	0.01	0.02		
	Al	Ag	B	Bi	Ca	Cd	
EMCA Au 3264	0.01	0.001	< 0.01	0.4	0.5	0.3	
	Co	Cr	Cu	Fe	Mg	Pd	
	< 0.01	< 0.01	0.1	< 0.01	0.004	0.1	
	P	Pt	Mo	Nb	Ni	Pb	
	< 0.1	< 0.05	< 0.01	< 0.01	< 0.01	0.2	
	Sb	Si	Sn	Ti	Zn	Zr	
	< 0.01	0.02	< 0.01	< 0.0001	< 0.01	< 0.01	

*Si content in DuPont 9596 ink was also analyzed by wet chemistry method, which showed 1.3% Si. If all the Si is tied in glass ("frit"), this accounts for 2.8 wt% SiO_2.

The general morphologies of as-fired surfaces of the Au metallization are shown in Fig. 2. Note the smooth appearance of the EMCA Au when it is layed directly over the substrate (Fig. 2a). This is contrasted by the rough appearance and indication of glassy nodules in the same EMCA when it is deposited

(a)



(b)

Fig. 2. SEM micrographs of unburnished Au top surfaces a: 3264 EMCA Au, single layer on substrate; b: 3264 EMCA Au over 9596 Pt-Au layer. 1000X (Inset: 5000X detail of glassy particles).

over a layer of 9596 Pt-Au (Fig. 2b). Energy dispersive X-ray data related to Fig. 2 are shown in Fig. 3. Area scan of the single layer of EMCA Au shows Si and traces of Pd, Fe and Pt (Fig. 3a). Point analysis on one of the glassy nodules in Fig. 2b shows a very high concentration of Bi, Al, Si, Cd, Ca, Fe and Zn (Fig. 3b). Most of these elements are oxide formers and combine readily in low melting glasses.[6]

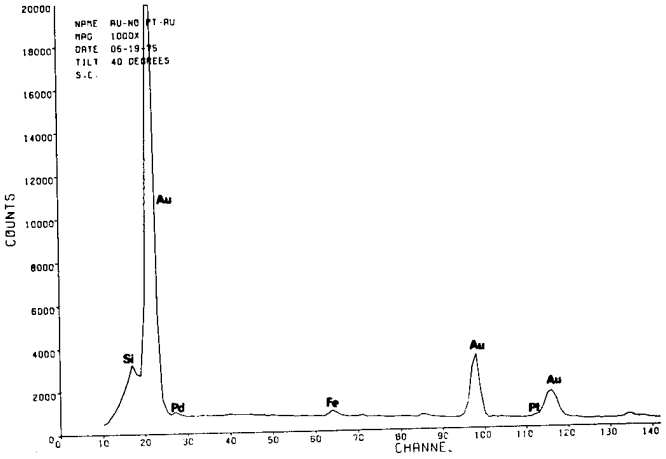


Fig. 3a. Energy dispersive X-ray spectra, EMCA Au only (Fig. 2a).

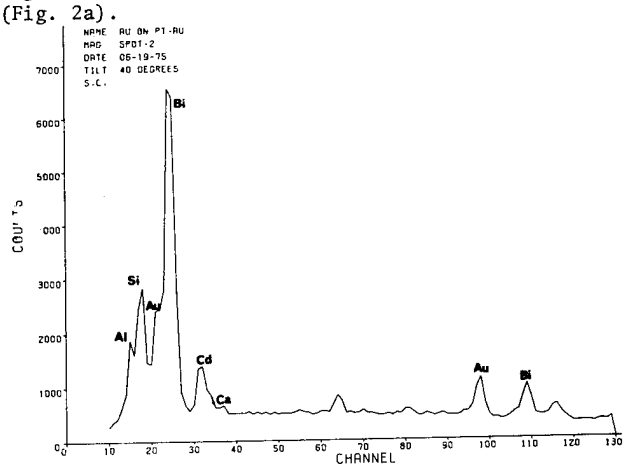


Fig. 3b. Energy dispersive X-ray spectra of typical glassy particle, EMCA Au over Pt-Au, such as particle 2 in Fig. 2b.

Burnishing is often employed as a means of "cleaning" the surface of a metallization. The data shown in Table I was obtained on wires bonded to burnished surfaces. The burnishing procedure may spread a layer of "pure" metal over the surface, but this layer does not extend to any appreciable depth. Figs. 4a-4f show the results of electron-microprobe scans over a burnished surface (Fig. 4a). Since the electron beam integrates data from a depth of no more than 2 μm[7] it is apparent that the glassy nodules are not removed, but are merely covered by a thin layer of pure metal. Note that the nodules contain Cd, Bi, Si and Ca. This is evident from the direct correspondence among the bright areas in the various scans of Fig. 4.

It is of interest to compare the electron microprobe data to Auger spectra taken over an area similar to that shown in Fig. 4a. Fig. 5 does not indicate concentrations of the impurities found in the glassy nodules. This is due to the fact that Auger electrons escape from a depth of no more than 10 A.[8] Such data may be, therefore, misleading in that it will indicate a clear surface. However, when a bond is made, the wire is pushed to a depth of a few microns, where it comes in contact with the nodules.

The Al wire-Au interface of a typical failed bond is shown in Figs. 6a and 6b; X-ray analysis of a glass nodule is shown in Fig. 6c. The micrograph indicates that (a) a layer of Au, a few microns thick, has been pulled away, which is indicative of at least a partial "metallurgical" bond, and (b) a substantial fraction of the failed interface contains the glassy nodules.

Discussion

Analysis of Data

Examination of the chemistry of the starting Au inks leads us to the conclusion that the inks are the source of the contaminants found in various compounds formed throughout the metallization, and in the Al wire-metallization interaction zones. It is also apparent that the larger contribution of contamination is drawn from the first layer of metallization, i.e., the 9596 Pt-Au ink.

Diffusion coefficients of few elements in Au at the applicable temperature range are shown in Table III. Although data for Bi are not available, we assume its behavior to be similar to Sb and Sn. The diffusion distance can be approximated by

$$X = \sqrt{2\,Dt} \qquad (1)$$

where D is the coefficient of diffusion and t the time, we get:

for $D = 1 \times 10^{-8}$, $t = 1200$ sec* $X \approx 5 \times 10^{-5}$ cm ≈ 50 μm

These results show that all the contaminants can diffuse through the top Au layer during the time at temperature. Pt is the slowest diffusing element and, thus, is found in much smaller quantities than Pd, for example, although the bottom layer contains about 15% Pt and only 3% Pd (Table III).

The driving force for diffusion is readily available for all elements considered because:

(a) the top, relatively pure EMCA Au, provides an unsaturated sink for the solid-solution elements, see Table IV.

Table III

Diffusion Coefficients of a Few Elements in Au

Element	Temp. °C	D cm^2/sec	Ref.
Pd	400-600	2×10^{-8}	9
Cu	700-900	3.5×10^{-9}	10
Pt	700-900	1.2×10^{-10}	11
Sb	900	2×10^{-8}	12
Sn	800	7×10^{-9}	12
Si	Diffuses readily at low temp. in air (~350°C) to form SiO_2 on surface		13

Table IV

Solubility Limits of Various Elements in Au in wt% (Ref. 14)

Al	3 at 545°C
Cd	15
Bi	Practically nil
Fe	3 at 300°C
Pd	Continuous series of S.S.
Pt	Continuous sereis of S.S. Miscibility gap above 20% Pt
Si	Nil, eutectic at 5.8% Si and 370°C

(b) the firing in air provides oxygen potential for the strong oxide formers such as Si**, Cd, Bi and Al.

Bi_2O_3 is liquid above 825°C and forms lower melting eutectics with ZnO, MgO, Al_2O_3, Fe_2O_3, SiO_2, etc.[6] The formation of Bi rich nodules, such as found on and under the surface of the top Au layer and which are associated with the lifted bond (Fig. 6) is therefore certain to occur during the sintering steps.

Aluminum forms a low melting eutectic (~615°C) with Pd and Pt which results in the formation of intermetallic hard and brittle phases[8] of the type Al_3Pd or Al_3Pt.

Bond Failure Mechanism

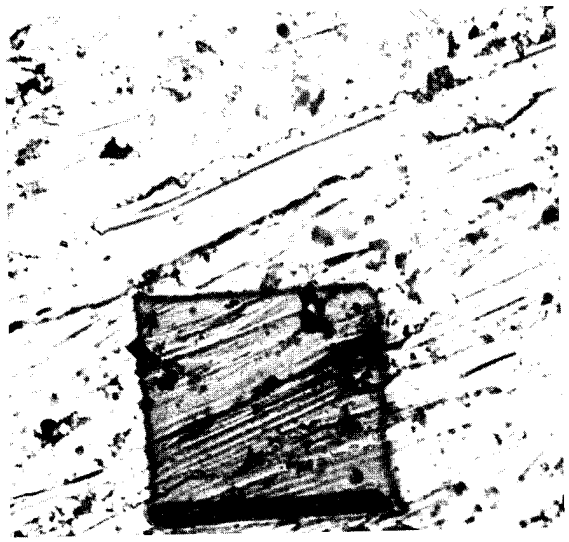
It is intuitively obvious that bonding to a material containing brittle glass will be difficult. However, we intend to show that the effect of the glass is more profound, and is manifested primarily during the brazing cycle in H_2.

Figure 6 shows that bond fracture occurred within the Au metallization, about 5 μm below the Al wire-metallization interface. This fact can be ascribed to two factors: a) embrittlement of the Au metallization due to the presence of the brittle glass nodules and Al-Pd-Pt intermetallics, and b) the catastrophic effect of the H_2 brazing cycle on the bond strength is attributed to reduction of the glass nodules. Al_2O_3 and SiO_2 are not likely to be reduced at 275°C (548°K). The reaction for Al_2O_3 reduction, for example, is described as:

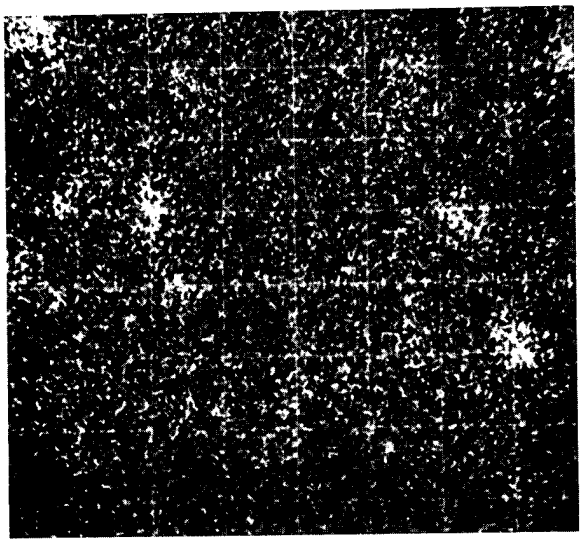
$$Al_2O_3 + 3\,H_2 \rightarrow 2\,Al + 3\,H_2O(g) \qquad (2)$$

*10 minutes Au firing at 900°C + 10 minutes resistor firing.

**Since we find Si in the EMCA Au also, we assume that not all Si in the "fritted" Pt-Au is tied as SiO_2.

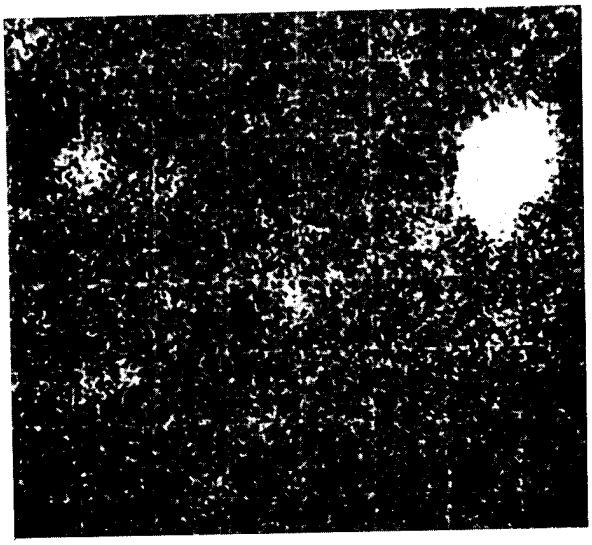


(a)

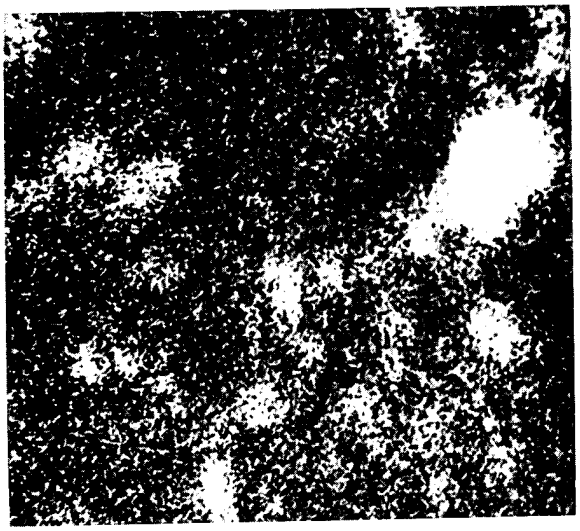


(d)

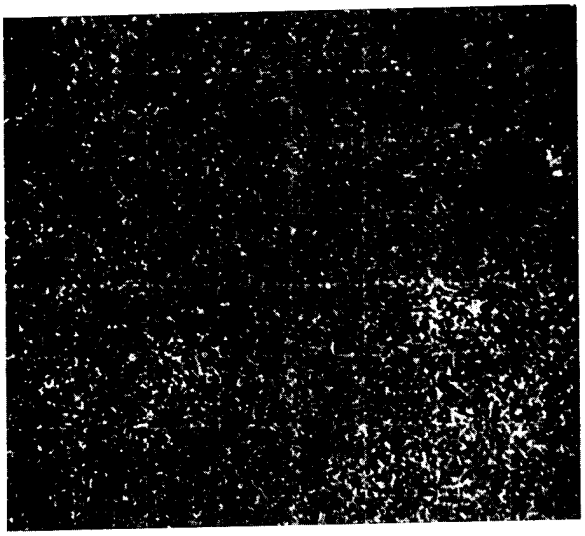
(b)



(e)



(c)



(f)

Fig. 4. Electron microprobe scans, burnished surface of Au metallization
(a) Light micrograph, 500X; (b) Bi; (c) Si; (d) Cd; (e) Ca; (f) Pd.

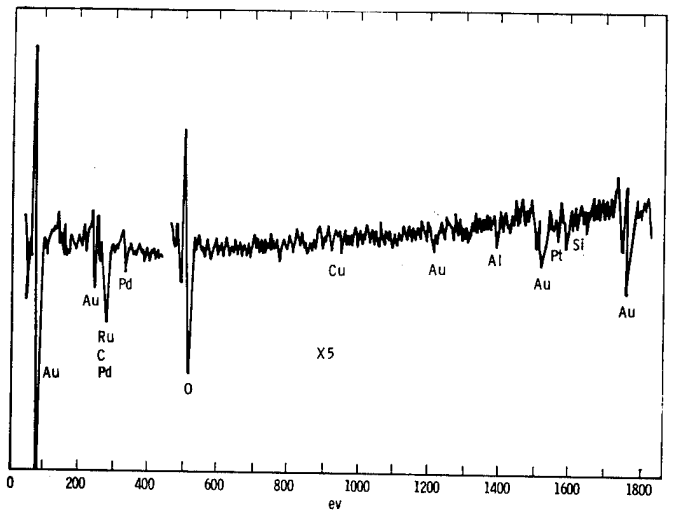
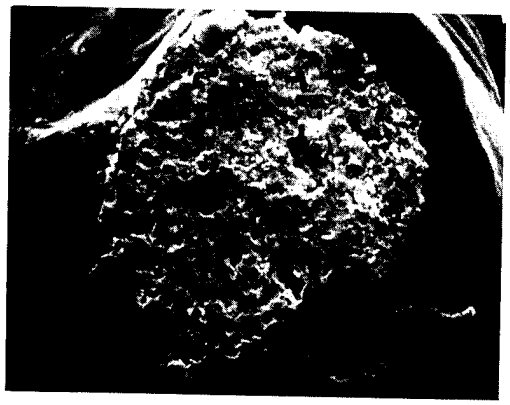


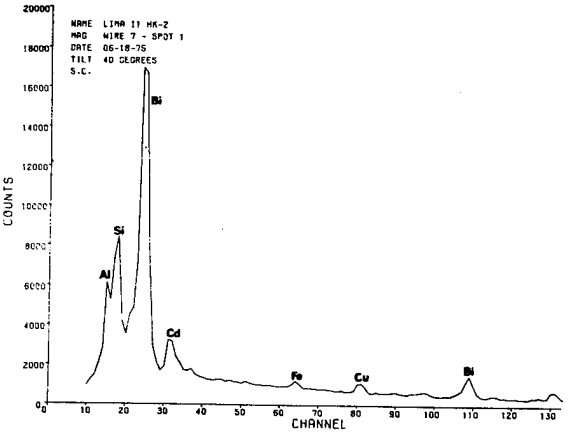
Fig. 5. Auger spectra burnished Au metallization, Fig. 4a surface sputtered 30 sec. at 2 mA 30 kV



(a)

(b)

Fig. 6. Bond side of failed Al wire (a) 600X; (b) 6000X; (c) energy dispersive spectra, spot 1, Fig. 6b.



(c)

and the full energy balance

$$\Delta G = 0 = \Delta G^{o} + RT \ln \frac{(PH_2O)^3}{PH_2} \quad (3)$$

from which

$$PH_2O \cong 1 \times 10^{-30} \text{ atm} \quad (4)$$

where PH_2O is the water pressure generated during the reaction of Al_2O_3 and H_2 at 548°K. Similarly, there will be negligible reaction of H_2 with SiO_2.

However, the activities of CdO and Bi_2O_3 are quite higher, and are expected to be even higher when these oxides are combined to lower melting compounds. Unfortunately, free energy data for Bi_2O_3 are not available. We can show, however, that CdO is most likely to be reduced and generate high enough water vapor pressure to break, or severely deteriorate, the bonds

$$CdO + H_2 \rightarrow Cd + H_2O(g) \quad (5)$$

from which

$$PH_2O \text{ (at } 548°K) \cong 1.5 \times 10^{-2} \text{ atm} \quad (6)$$

Reduction of the Bi rich glassy nodules is, therefore, certain to occur.

The water vapor pressure generated within the volume occupied by a glassy nodule is given by:

$$P_1 = \frac{V_2}{V_1} \frac{T_1}{T_2} P_2 \quad (7)$$

from

$$PV = nRT$$

we get that n, the number of moles of water vapor generated by the reaction

$$Bi_2O_3 + 3 H_2 \rightarrow 2 Bi + 3 H_2O \quad (9)$$

is equal to 3.2×10^{-12}. V_1 is the volume of the nodule, and assuming d = 5 μm dia $V_1 = 6 \times 10^{-11}$ cm^3. P_2 = 1 atm and V_2 is the free volume of the water vapor $V_2 = 22.4 \times 10^3 \times 3.2 \times 10^{-12} = 7.3 \times 10^{-8}$ cm^3. Taking T_1 = 500°K, we get

$$P_1 = \frac{500}{273} \times \frac{7.3 \times 10^{-8}}{6 \times 10^{-11}} = 2200 \text{ atm}^* \qquad (10)$$

A typical bond area is A = 1500 μm^2 or 1.5×10^{-5} cm^2. The maximum lifting force acting on the bond through the volume of Au lifted is then

$$F = 2.2 \times 10^{6} \times 1.5 \times 10^{-5} = 33 \text{ g} \qquad (11)$$

This is high enough a force to severely deteriorate, or completely lift the bond during the soldering cycle in H_2.

To confirm the failure model, two additional tests were run.

(a) Al wire was bonded to a double layer of EMCA Au and the assembly subjected to the H_2 cycle. Improvements in bond strength would confirm the effect of the glassy nodules.

(b) A normally bonded substrate was subjected to a simulated H_2 cycle, using the same time-temperature profiles in N_2 atmospheres. An improvement in bond strength would confirm the reduction hypothesis. The results of these tests are summarized in Tables V and VI, respectively.

Table V

Bond Strength Data

0.003" Al wire on double thickness EMCA Au (maximum load 30 g)

As Bonded	After 10 min at 275°C in H_2	After Additional 10 min at 275°C in H_2
30 NF	30 WB	28 WB
30 NF	28 WB	30 NF
30 NF	28 WB	30 WB
30 WB	29 WB	29 WB

NF: No Failure; WB: Wire Break

Table VI

Bond Strength Data (pulled to failure)

0.003" Al wire on microsubstrate N_2 atmosphere cycle

As Bonded	10 min at 295°C + 10 min at 275°C in N_2
35 BL	
50 WB	29 WB
45 WB	27 BL
50 WB	17 BL
30 WB	22 BL
35 WB	27 WB

The results in Tables V and VI confirm the deleterious effect of the combination of glassy nodules and H_2 atmosphere cycles. The temperature cycle at 275°C and 295°C in N_2 atmosphere for substrates containing the glassy nodules is still causing deleterioration of the bond, although to a lesser degree than in H_2. This can be attributed to embtittlement effects of the glassy nodules and other phases due to differential thermal expansion. There is, however, a minimal deterioration through the normal cycle if a "clean" Au ink is used (Table V).

*The calculation is somewhat conservative since we ignored the volume occupied by the free element generated by reaction (9). The real pressure is then expected to be even higher.

Summary and Conclusions

From the chemistry of the starting materials, metallographic evidence, and bond strength data, we conclude that:

1. The bond extends beyond a surface reaction and indicates interaction between the Al wire and the Au metallization.

2. Bi rich glass nodules and Al-Pd-Pt intermetallics are responsible for a low bond strength, mainly due to embrittlement of the Au metallization-Al wire reaction zone.

3. Reduction of the glass during the brazing cycle in H_2 results in a catastrophic failure of the bond.

4. Most of the impurities are diffusing from the bottom layer of Pt-Au.

Acknowledgments

The cooperation and contributions from J. J. Schreurs and S. C. Singhal of the Research Laboratories and M. Schuster of Baltimore ATL are mostly appreciated. Invaluable technical assistance was provided by C. W. Hughes, A. Wolfe and T. J. Mullen.

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Note Added

After the completion of the manuscript, Harman[5] suggested to consider the interaction of H with Pd in the Au ink. Pd can absorb large amounts of H.[14] The β phase, also noted as Pd II, dissolves up to 1800 relative volumes of H, where the gas is arranged in interstitial positions. The lattice parameter is enlarged to a maximum value of 4.026 Å at 1 atm H pressure[16] compared to 3.891 Å for pure Pd. The absorption of H constitutes, therefore, a maximum increase in volume of about 4%. Since the DuPont 9596 ink contains about 3% Pd, we conclude that the internal expansion of the Pd phase could not contribute significantly to the severe deterioration of the bonds (Table I).

DESIGN AND USE OF A LASER INTERFEROMETER FOR ULTRASONIC BONDING STUDIES

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Summary

Design

An in-line laser interferometer was developed to study motions during ultrasonic bonding. The interferometer consists of a 2 milliwatt He-Ne laser with output mirrors at both ends, a lens with adjustment apparatus, and a photodiode detector. The detector output is displayed on an oscilloscope. The lens permits the beam to be focussed to a spot diameter less than 25 micrometers. The beam is focussed on a periodically moving target which results in a fringe pattern displayed on the oscilloscope. Peak-to-peak displacements up to 50 micrometers have been measured with an accuracy of $\pm$ 25 nanometers.

The fringe pattern observed may be described in terms of a Michelson interferometer. The experimentally observed fringe pattern corresponds exactly to the theoretical plot using the Michelson interferometer. Peak-to-peak displacements are determined by counting the number of fringes on the oscilloscope.

Applications

In an effort to derive a model for the mechanisms involved in ultrasonic bonding, motion at the wire-bonding pad interface was measured. A 150 micrometer diameter gold wire was bonded to a gold plated copper pad on an epoxy-glass substrate. The interfacial peak-to-peak motion was significantly less than 250 nanometers for a tip motion of 4 micrometers. These measurements indicate essentially zero relative motion at the interface, an important consideration in modeling ultrasonic bonding.

A second application was in monitoring the motion of wires and staples during bonding. Observations have been made in the industry of weakening of the first bond after performing the second bond; i.e., device pad to header pad wiring. Measurements were made on straight wires and on staples (rectangular shape) of the transverse motion of the wires during the second bond. Nodes and antinodes were observed along the length of the wire. Theoretical analysis of the system agrees with the experimental results. Transverse peak-to-peak displacements as large as 25 micrometers have been seen for bonding amplitudes of 2.5 micrometers. These resonance conditions can severely stress the first bond, causing reduced pull strength and even fracture during bonding.

Design

The first interferometer design tested was a laser Michelson interferometer. The results will be described in detail, since they apply to the in-line interferometer design. Figure 1 shows the Michelson design. The reference beam travels from the laser to the beam splitter and is reflected to the fixed mirror and back through the beam splitter to the detector. The measuring beam travels from the laser through the beam splitter to the target; it is reflected to the beam splitter and then to the detector. These two beams superimpose, and light and dark fringes are formed at the detector as the target moves. These fringes occur because of the phase modulation of the measuring beam induced by the target motion. If the reference and measuring beam path lengths are r_1 and r_2, the electric fields are:

$$E_1 = \varepsilon_1 e^{\frac{i\,2\pi}{\lambda}(ct - r_1)}$$

$$E_2 = \varepsilon_2 e^{\frac{i\,2\pi}{\lambda}(ct - r_2)} .$$

The intensity I is

$$I = |E_1 + E_2|^2 \qquad (1)$$

$$= \varepsilon_1^2 + \varepsilon_2^2 + 2\varepsilon_1\varepsilon_2 \cos\left(\frac{2\pi}{\lambda}(\Delta + A \sin 2\pi f t)\right)$$

where λ is the wavelength of the light, Δ is the path difference when the target is at rest, A is the peak-to-peak target displacement, and f is the frequency of the target sinusoidal oscillation.

Figure 2 is a computer plot of the intensity equation for λ = 632.8 nanometers, Δ = 130 nanometers ($\pm$ any integral number of half-wavelengths), A = 2.79 micrometers, and f = 60 kHz. Figure 3 is an oscilloscope trace obtained for ultrasonic tip motion using the Michelson configuration. The unique patterns at the ends and middle of the traces are the extremes (or turn-around points) of the target motion. One complete oscillation cycle is shown, beginning at one extreme and returning to it. The peak-to-peak amplitude of target motion is obtained by counting the fringes between the extremes. Since the measuring beam path length is changed by twice the target motion, each fringe corresponds to $\lambda/2$ or $\sim$ 316 nanometers.* It is necessary to determine the relative intensity of the end points in order to obtain maximum resolution. From the intensity equation (1), the two extremes will have the same intensity only for $\Delta = 0 \pm n\,\lambda/4$ where n is any integer. For all other equilibrium path differences, one turn-around point will be different from the other, as in Figs. 2 and 3. In these traces there are 8.8 fringes, or 2.79 micrometers peak-to-peak displacement. It is not difficult to determine the positions of the extremes to an accuracy of 25 nanometers.[1]

The in-line configuration was a result of the Michelson experiments. Some of the energy reflected by the fixed mirror was reflected by the beam splitter back into the laser. Any changes in this optical path length caused external cavity modulation of the laser, with corresponding intensity fluctuations at the detector. This external cavity principle was used in the final in-line design shown in Fig. 4. By eliminating the beam splitter and the fixed mirror, and moving the detector "in-line", behind the laser, the mechanical design is simplified, and the physical size reduced. The laser has been modified by using two partially transmitting mirrors to provide output from both ends.

Figure 4 shows an added optical element, a lens. The lens focusses the laser beam to a spot less than 25 micrometers in diameter. The interferometer may therefore be used to measure the motion of extremely small objects. Equally important, the lens autocollimates the light reflected from the target.

*For the He-Ne 6328 Å visible line.

This feature permits measurement of a wide range of targets normally considered non-reflecting. No special care need be taken with regard to object flatness or surface condition. Critical alignment procedures are unnecessary; all that is necessary is that energy be returned to the laser cavity.

Figure 5 compares the fringe patterns obtained from a single moving target using the in-line and Michelson configurations. The upper trace of each pair is the in-line output; the lower trace of each pair is the Michelson output. The fringe count is identical for the two interferometer designs. Equation (1) may, therefore, be used to calculate the peak-to-peak displacement for the in-line configuration. For simplicity, the in-line design may be described similarly to the Michelson. The detector measures the interference between two beams, a reference beam emerging directly from the laser to the detector and a measuring beam, which leaves the opposite end of the laser, travels to the target and back through the laser to the detector.[2]

In Fig. 5, the in-line trace shows attenuation of the fringe intensity contrast at the high target velocity (approximately 1 meter per second) in the lower pair. At the lower velocity (upper pair) no such attenuation is observed. The light reflected by the moving target is Doppler shifted and the laser cavity attenuates the reflected frequency shifted beam. It is important to note that the reduction in fringe intensity contrast has no effect on the accuracy of the technique, since it is the number of fringes, not the intensity, which determines the amplitude of the motion.

Figure 6 is a photograph of the in-line system. The He-Ne 2 milliwatt laser has been modified for equal output from the front spherical mirror and the rear flat mirror. Any low power He-Ne laser may be used in this manner if the mirrors are adjustable to obtain single mode operation. This permits maximum signal-to-noise ratio. The lens is housed in rotatable eccentric tubes for ease of adjustment of focal point. The surface barrier photodiode is mounted on the other end of the laser. The housing contains the circuit shown in Fig. 7. The signal output is connected via an FET probe or built-in FET circuit to an oscilloscope. This is required for high frequency signals to reduce signal attenuation due to cabling capacitance. For applications where extraneous vibrations are present, a storage oscilloscope may be needed to provide readable fringe patterns.

Applications

The interferometer was originally used to measure the motions of ultrasonic bonding tips. Such motions have been described earlier[3,4,5] and will not be discussed here. Two ultrasonic bonding applications will be described, wire-pad interface motion and transverse wire resonance.

Wire-Pad Interface Motion

Due to the focussing lens, the interferometer is uniquely suited to measure motions of bonding wires and pads. Figure 8 illustrates the procedure used. A gold wire (150 micrometers in diameter) is placed on a gold-plated copper bonding pad. The pad, epoxy-glass substrate, and wire have been ground to provide vertical surfaces perpendicular to the bonding tip motion. The wire is placed flush with the bonding pad, and the bonding tip is placed as close to this plane as possible. This provides essentially a continuous vertical surface formed by the tip, wire and pad. The laser is focussed on the tip, wire, or pad and a bond is made. The peak-to-peak displacement is recorded for the motion of a component during bonding. A new wire and pad are bonded for each data point.

Figure 9 is a plot of 30 such measurements. The variations in motions at a particular position are not excessive considering each point represents a different wire bond. It is seen from this figure that the relative motion between the wire and bonding pad is minimal since there is no obvious discontinuity at the interface. These measurements have been used in modeling the mechanism of ultrasonic bonding.[6]

Transverse Wire Resonance

In an effort to examine the phenomenon of weakening or fracture of the first wire bond while making the second bond,[7] measurements were made of wire motion perpendicular to the bonding tip motion. Figure 10 illustrates the arrangement used for staples. Straight wire segments were measured in the same manner. Typical bonding tip motion was 2.5 micrometers peak to peak. By focussing the laser on the wire, measurements were obtained of the motion of one point on the wire during bonding. It was found that some points on wires had peak-to-peak transverse displacements greater than 25 micrometers and that these maxima were periodic. Figure 11 represents the type of pattern seen.

To accurately plot the resonance, the same arrangement was used except that after the second bond had been made the bonder tip motion was reduced to 80 nanometers and was left on. This continuous excitation caused the transverse motions seen in Fig. 12. Note that the pattern is very regular with nodes appearing approximately every 1.3 millimeters. This is in good agreement with calculated resonance lengths for 60 kHz natural frequency.[8] Other frequencies would have different lengths. Experiments were also performed for various lengths of wire showing that at 60 kHz, maximum amplitudes were observed for wire lengths which were multiples of 1.3 millimeters and that the number of antinodes were equal to the multiplier.

Metallurgical analysis of first bond fractures has shown that the transverse motion can indeed fatigue the wire to failure. Resonance motion could be prevented by misshaping the wire or by clamping. Also reduction in bonding tip motion directly reduces transverse motion. In many systems the fatigue strengths of the wire used are sufficient to prevent degradation.

Acknowledgements

The author greatly appreciates the contributions to this work by several people at IBM Endicott, New York. The in-line suggestion and early development efforts were made by A. D. Wilson. The lens was suggested by J. P. Kirk and the detector circuit was developed by D. H. Strope. The staple motion measurements were made by J. S. Drotar.

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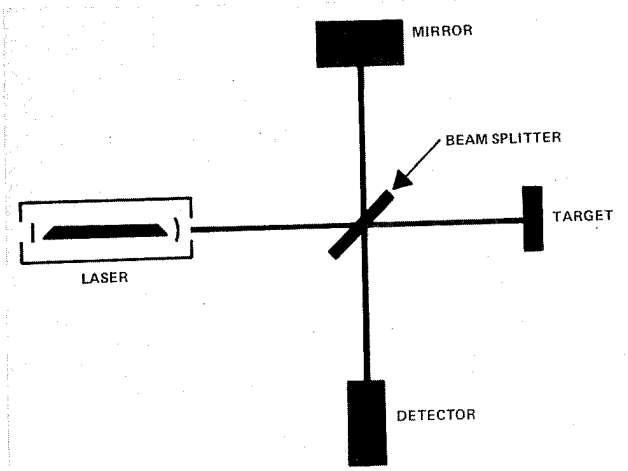

Fig. 1. Laser Michelson interferometer.

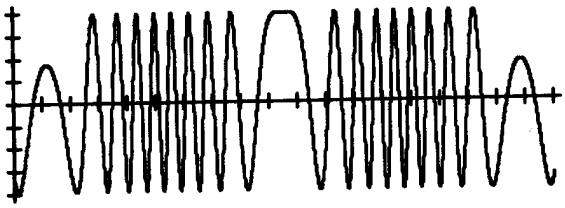

Fig. 2. Calculated fringe pattern.

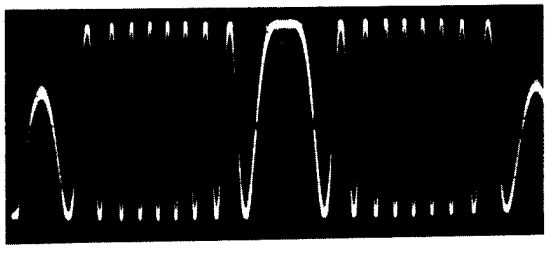

Fig. 3. Experimental fringe pattern.

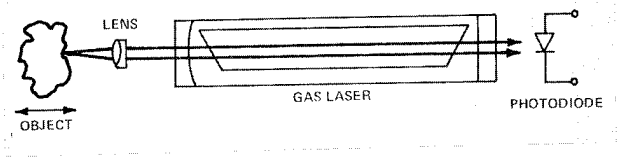

Fig. 4. In-line laser interferometer.

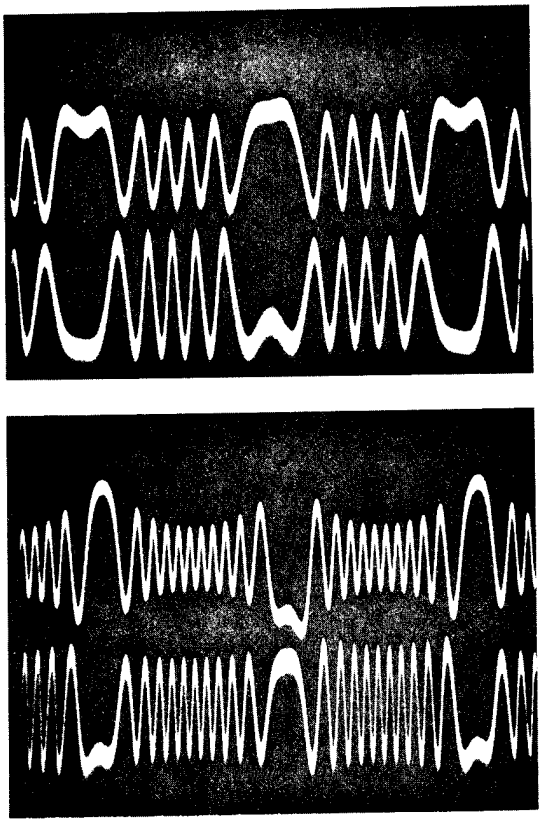

Fig. 5. Michelson and in-line fringe patterns.

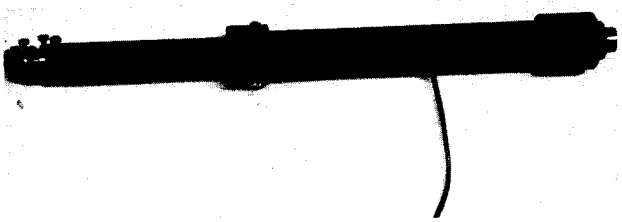

Fig. 6. Photograph of in-line laser interferometer.

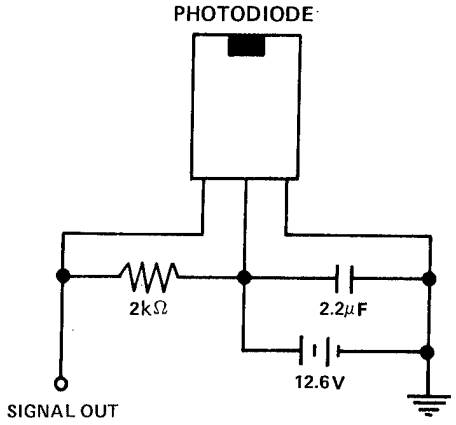

Fig. 7. Photodetector circuit.

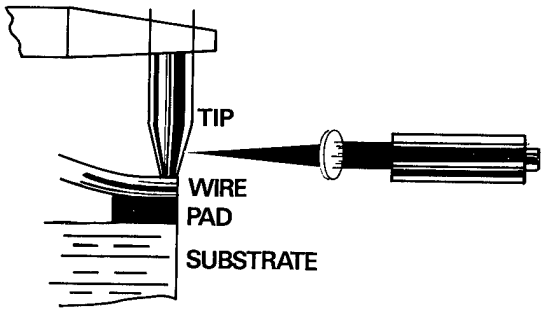

Fig. 8. Measurement of wire-pad interfacial motion.

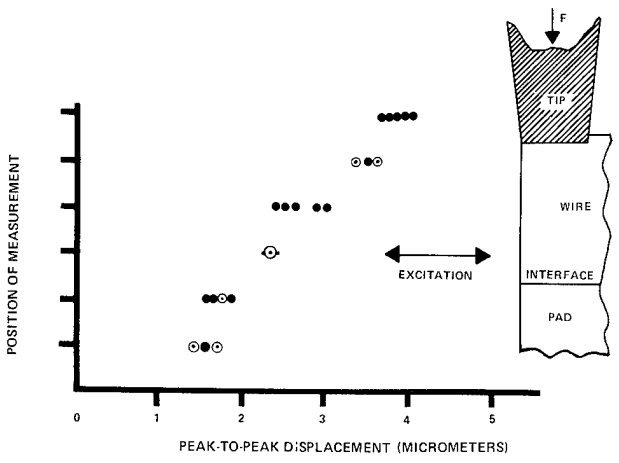

Fig. 9. Peak-to-peak displacement measurements.

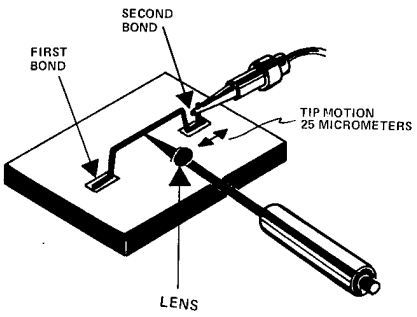

Fig. 10. Transverse wire motion measurement.

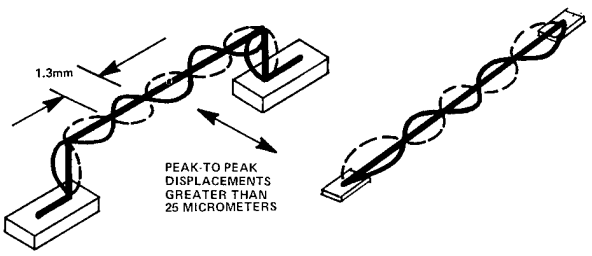

Fig. 11. Excitation of transverse resonance.

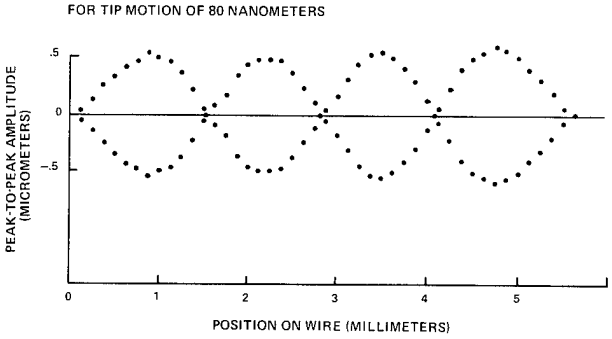

Fig. 12. Peak-to-peak displacement measurements.

THE USE OF ACOUSTIC EMISSION IN A TEST FOR BEAM LEAD BOND INTEGRITY*

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ABSTRACT

The use of Acoustic Emission (AE) in a test for beam lead bond integrity has been investigated. AE refers to emission of broad band stress waves when materials are broken, cracked, or deformed. A major problem in the present work was to develop means of nondestructively stressing the delicate, irregularly extending beam leads. The most promising of the methods developed are a silicone rubber (SR) pull test, a push down test on SR encapsulated devices, and various probe methods of applying force to the beams without contacting the chip. AE bursts from weak bonds or beam anchors are detected with a substrate detector operating at 375 kHz or a probe detector operating at 1.1 MHz or both. The study has revealed considerable differences in the mechanical integrity of beam lead bond-anchor systems. General deterioration of the beam-anchor system begins at pull forces per beam of from approximately 1.0 to 2.5 gf, depending on the manufacturer's procedure. The forces applied to the beam-anchor system for all methods of stressing, except the pull test, are dependent upon the shape of the individual beams as they extend from the chip, as well as the uniformity of the bugging height. There are many other potential uses of AE in electronics, such as to insure the bonding integrity of flip chips, capacitor chips in hybrids, and bonds on automated tape-bonded integrated circuits. The latter two uses were experimentally demonstrated in the present work. Thus, it appears that AE will have an increasing role in assuring reliability in the microelectronics field.

1. INTRODUCTION

Two destructive tests are currently used to measure the strength of beam lead bonds. The more frequently used of these is the push-off test which requires that the device be bonded over a hole in the substrate. A rod is pushed through the hole and the force required to break the beams, or frequently the silicon, is measured. The pull-off[1], or hot melt glue method, is the more accurate destructive test. In this case, glue is melted on the top of the chip and a wire (sometimes also the glue heater) is embedded in it. After the glue has hardened, the wire is pulled upward and the force required to break the beams is recorded. A recent review and comparison of these two methods was given by Riggs and Ondrick[2]. Both of these methods are useful in developing a bonding schedule and for maintaining statistical control of production bonding. Both of these methods yield an average device beam pull strength. Variations in pull force obtained from pulling multibeam devices will generally mask one or more weak or unbonded beams.

A differential pressure test method has also been devised[3]. It consists of a pressurizing chamber with an evacuation tube placed over the device being tested. This method can be used as either a destructive or a nondestructive test. In the latter case a subsequent electrical test or visual inspection of the device is required to reveal any unbonded beams. Except in its originating organization, this test is seldom employed, possibly because it requires special pressure chambers operating at 150 psi (≈1.0 MPa) or more.

Beam lead bonding is generally reliable once an optimum bonding schedule is achieved, based on a destructive pull or push test. However, as with any thermal compression bonding system, contamination in the bond interface may inhibit welding[4,5] on one or more beams in an unpredictable manner. In addition, if the hardness of the beam gold varies for devices from different wafer lots or different manufacturers, a bonding schedule optimized for one lot may produce erratic bond reliability for another. Thickness irregularities in thick-film bonding metallization may also reduce bond adherence for one or more beams on a multibeam device. Thus, it would be desirable to have a simple 100% nondestructive test that will detect one or two poorly bonded beams out of a large number of well bonded ones and not require a subsequent visual inspection or electrical test to reveal the results.

In the present work the use of acoustic emission (AE) in a nondestructive test for beam lead bond integrity has been investigated. Acoustic emission[†6] (AE) refers to emission of broadband stress waves within the material when that material is broken, cracked, or merely deformed, although the emission mechanism may be quite different in each case. The emitted frequency spectrum can range from the audible into the megahertz region, but the maximum energy is generally greatest at the mechanical resonance frequencies of the specimen. With only one notable exception AE has not found use in electronics and most microelectronic engineers and scientists are unaware of its potential. Vahaviolos[7] has applied AE, or stress wave emission, to the detection of cracks in ceramic hybrid substrates that can result from the high pressures of compliant bonding rams. His paper also gives clear explanations of AE phenomena, theory, and equipment.

*This work was sponsored by NBS and the Defense Advanced Research Agency, under ARPA order 2397.

† Technically the phenomenon should be called stress wave emission; however, for historical reasons it is generally referred to as acoustic emission.

AE has been studied in a variety of materials by many workers. However, there is only one known study of such emission from gold, the material used in the beam lead bond system. Schofield[8] reported that "the occurrence and behavior of AE in gold was undoubtedly the most consistent and certainly the most active of any of the face centered cubic metals previously studied." He verified the Kaiser effect[9] for the high frequency emission (i.e., that AE is irreversible during application of a given load. A higher load must then be applied or that specimen must be annealed in order to observe additional AE). However, he found that certain "burst emissions" were reproducible without annealing. Schofield's work was on gold single crystals in two orientations; however, some specimens that had been elongated during a first test were then annealed and developed a relatively coarse grain structure. These polycrystalline samples also emitted AE upon further testing. Thus, for the present work we concluded that the gold in beam leads should be capable of AE if poorly welded beams could be stressed adequately to strain or break some of the microwelds in the few bonded areas.

II. METHODS OF APPLYING A MECHANICAL STRESS TO THE BEAM-LEAD SYSTEM

The problem of mechanically stressing a bonded beam-lead device in a nondestructive manner is a formidable one. The most desirable method is to lift the device upward. This would stress both the beam anchors (the attachment to the chip) as well as the beam bonds. The most obvious method of doing this would be to slip hooks under the corners of the bonded beam-lead device and pull upward. However, since the bugging height* can be less than 25 μm and may vary from corner to corner, such a grappling hook could crack the thin silicon at the edge of the chip, causing extraneous AE, unless extreme care was exercised by the operator. Another method of pulling the device upward would be to epoxy tiny hook-shaped wires to the top of the chip and pull the device with a wire bond puller. A more convenient version of this technique is to use the hot-melt-glue pull-test, applying a force well below the pull-off level. However, the glue used for this purpose would remain on the chip, and that organic material is not a desirable additive to a hybrid package. Also the brittle hot melt glue can develop cracks during pulling and emit extraneous, misleading AE.

One simple alternative to the glue method is to apply a "dab" of a silicone rubber (SR) to the top of the beam lead chip and let it cure overnight at about 50°C or higher. Then a sharply pointed hook can easily pierce the rubber parallel to the chip as shown in Fig. 1. The hook is then pulled upward; about 40 gf can be applied to a 1 x 1 mm chip before the rubber breaks.† A tweezer type of device or

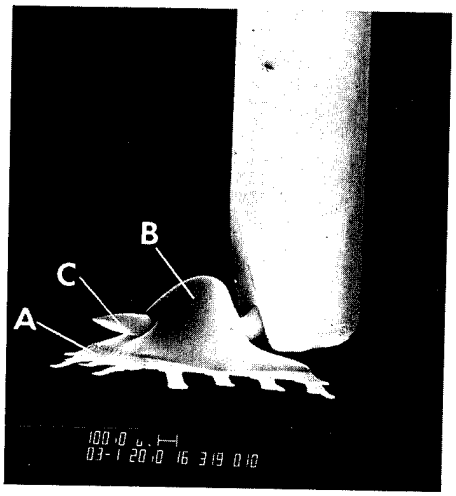

Fig. 1: Scanning electron micrograph of a weakly bonded beam lead device (A) with a silicone rubber "dab" (B) on top, that has been pulled up by an electrolytically etched, 150 μm diameter tungsten hook (C). (It is important that the hook be very smooth and have a sharp point so that the rubber is not torn while it is being pierced.) The hook carrier (D) is a section of a no. 22 hypodermic needle in which the hook had been inserted and rigidly epoxied in place.

a flatter shaped hook could be used in place of the present hook if it is desired to apply greater pull-forces. To verify that this method produced no extraneous AE, similar sized "dabs" of SR were bonded directly to the substrate and pulled with the hook. The SR emitted no measurable AE until the force that ruptured the rubber was reached. The silicone rubber used for this purpose was usually the stiff version of the methanol-base resin that some organizations use to protectively coat beam-lead devices. When the device is subsequently encapsulated the new resin will seal the punctured rubber and fill the bugging height. Therefore, this pull method and its residue can be considered nondestructive to both the device and the substrate. A sample quantity of devices may be tested on each substrate as a control. A high strength silicone rubber can be applied to the chip and this hook method can then be used as a destructive pull test. Pull forces of up to 100 gf have been applied to 1 x 1 mm chips.

Another method of pulling a chip is to mold a vacuum cup out of SR or another elastomer into the shape of the chip. When vacuum is applied to a device, an upward force of about 0.5 gf per beam can be obtained for a 14 or 16 beam device having an Electronic Industries Association registered chip outline. A third method of forcing the chip upward and the beams outward is to inject the silicone protective coating resin under the chip and allow it to cure. The material has a much higher coefficient of expansion than the gold beams. Preferential heat (such as infrared) applied to the chip will expand the rubber enough to stress very weak bonds. This method works best with high bugging heights, which allows more resin under the chip.

An alternative method of stressing the bonds is to push downward on top of the chip. Some of the force will be applied to the bond heels in the shear direction. This is the simplest

*Defined as the vertical distance from the substrate metallization to the bottom of the chip.

†If the chip is not clean this resin may pull free with about 20 to 30 gf. An adequate cleaning procedure is to immerse the bonded substrate in a fluorocarbon solvent and then air blow off the remainder of the solvent.

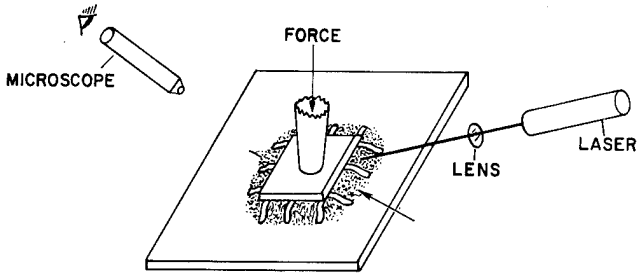

Fig. 2: A simple method of measuring the threshold of downward motion of a beam lead chip. The arrow points to the static interference pattern (the dots between the beams). When force is applied, the pattern changes.

method of applying force to the beam lead system. Depending on the angle at which the beams project from the chip, the uniformity of the bugging height around the chip, variation in beam dimensions, and the gold hardness, a 16 lead device will collapse to the substrate, accompanied by large bursts of AE, with the application of about 30 to 60 gf. This collapse force may be less if it is applied off center or the bugging height is not uniform. An improved variation on the simple push-down technique is to simultaneously push downward on top of the chip and, with an equivalent force, push horizontally along a diagonal of the chip. The force is applied with a molded SR probe that fits over the chip. The advantage of this method is that part of the horizontal force is applied to the bonds in a peel direction. Care must still be exercised to prevent collapse of the bugging height.

It has been found that roughly three times as much force in a downward direction can be safely used if it is only applied to the beams, leaving the chip free. A simple resolution of forces analysis based on typical bonded beam dimensions shows that with all beams uniformly stressed downward, ∿90% of the force is applied at the bond heel in the shear direction and no net torque is applied to the beam anchors (the beam attachment to the chip). However, when the beams along only one side of the chip are stressed at one time, the chip is rigidly held in place by the other beams and then essentially all of the applied force appears as a torque on the anchors. Thus, it is possible to provide an AE test for both beams and anchors by applying the stress appropriately. This assumes that the beams project horizontally outward from the chip for ∿50 μm before curving downward and bonding ∿100 μm away from the chip. In some bonding situations the beams leave the chip downward at ∿45 deg. and the bond occurs only 25-50 μm outward from the chip. No anchor torque is possible in this case. Thus, care in beam alignment during bonding, resulting in reasonably uniform bugging height, is essential in order for this test method to be applicable.

To determine the effectiveness of the chip push-down method a simple technique was developed to determine the downward force necessary to produce threshold deflection of the chip as well as of the bonded beams. A 1 mw He-Ne laser with a focused spot diameter of ≤25 μm was directed under the chip at a low angle between two of the beam leads as shown in the sketch of Fig. 2. The force was applied by the apparatus described in section IV that is normally used for such purposes in the AE test. The laser light was multiply-reflected back and forth between the substrate and the chip and established a complex static interference pattern that could be seen extending outward from the edges of the chip for 125-250 μm. Downward or upward deflection of the chip by only a small fraction of a wavelength produced changes in the interference patterns that could be easily seen through a 40X binocular microscope, even though no direct motion of the chip was discernible. The threshold of observable motion of an individual unbonded beam could also be seen by this method.* Such motion of the chip occurs with an applied force as low as 3-5 gf. Essentially unbonded beams require the application of about 10 to 15 gf to the chip before movement is observed, and this requirement varies according to the angle at which the beam lead approaches the substrate.

One method of protecting the chip from collapse, if the force is applied only to it and in the downward direction, is to first inject the silicone protective coating resin under and around the chip and let it cure. Then a force of several hundred grams can be applied to the top of the chip without danger of collapse. The rubber under the device will be partially squeezed out applying an outward force to the beams and a weak beam will partially lift, emitting stress waves in the process. If the probe is also heated to about 200°C then the combination of the SR thermal expansion and the downward force will result in a greater outward force on the beam bonds. Such a test should weed out devices that are predisposed to fail during thermal cycling.

III. PREPARATION OF CONTROLLED BONDABILITY SUBSTRATES

Various unpredictable bonding conditions can result in one or more of the beam leads being weakly welded as discussed in the introduction of this paper. It is difficult to obtain weakly bonded leads deliberately. The usual method of obtaining weakly bonded beams by lowering the bonding temperature is unreliable. The first bonded devices of such an intentionally weak bonding series may increase in bond strength while the rest are being bonded, due to gold sintering. Even temperatures as low as 85 to 150°C for one hour can significantly increase gold to gold bond strength on uncontaminated bonding surfaces,[10] and higher temperatures require even less time. Such sintering strengthening of beam lead bonds has been verified in the present study. Therefore, such methods of producing weak bonds are not desirable for use in developing a new measurement method.

In order to obtain weak beams specified in both number and position, an effect that is normally avoided was used. It is well known that chromium-locked-gold metallization must be kept at relatively low temperatures or the chromium will diffuse to the surface, oxidize,

*Although qualitative in nature, this simple technique may be useful in other types of visual inspection and should be a valuable aid in the observation of the relative thermal expansion of components and possibly in trouble.shooting unbonded capacitor and other chips in hybrids, as well as for studying creep phenomena.

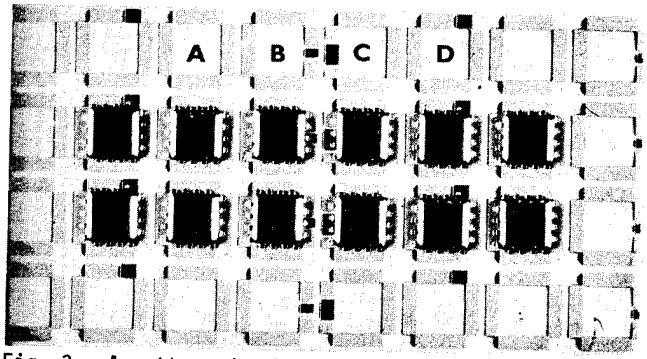

Fig. 3: A patterned substrate showing bonded beam lead devices. Chromium oxide covered areas for bond strength inhibition are stained black to increase visibility. The vertical row patterns are: (A) bonding controls (all good bonds), (B) pattern containing one weak bond in the center of the span, (C) pattern containing two weak bonds in the center, (D) pattern containing one weak bond on a corner. The chip dimensions are 1 mm on a side.

and severely decrease the thermal compression bondability.[11] Therefore, tantalum nitride-chromium-gold† substrates were heated to 310°C for two hours to diffuse the chromium to the surface. A special photomask set was used to pattern the metallization and a cerric ammonium nitrate etch[12] was used to preferentially remove the chromium oxide in all but specifically designated areas. Figure 3 is a photomicrograph of such a substrate bonded with beam lead devices. For clarity of presentation the chromium oxide covered areas have been darkened (normally they are the same color as the rest of the metallization). The four different patterns can be clearly seen. They include a single poorly bonded beam on a corner location, a single weak beam in the center, two weak beams in the center, and a control pattern for making all well bonded beams.

It should be pointed out that when using the chrome-diffused gold bonding pads, some degree of control over the beam-lead bond-peel-strength (essentially all the bonds so prepared peel) can still be exercised by varying the bonding parameters (force and temperature). In this manner the peel force for an individual beam can be varied from <0.5 to ∿3 gf.

It was established that the chrome oxide method of producing controlled weak bonds still left a few areas that were welded and therefore could produce valid AE signals when the beam was stressed. In addition, it was desirable to determine the minimum AE signals that could be detected with the available equipment. Devices were bonded following various bonding schedules to substrates that had chromium oxide on the surface. The devices were stressed and acoustic emission signals were recorded on digital pulse capturing equipment. The poorly bonded beams were then peeled back and examined for evidence of torn welded areas and therefore of AE point sources. Figure 4a is an SEM photograph of the chromium-gold coated

†Efforts to use chromium-gold metallized substrates resulted in rapid etching of the undiffused chromium, thus undercutting the gold. The reason for this is unknown.

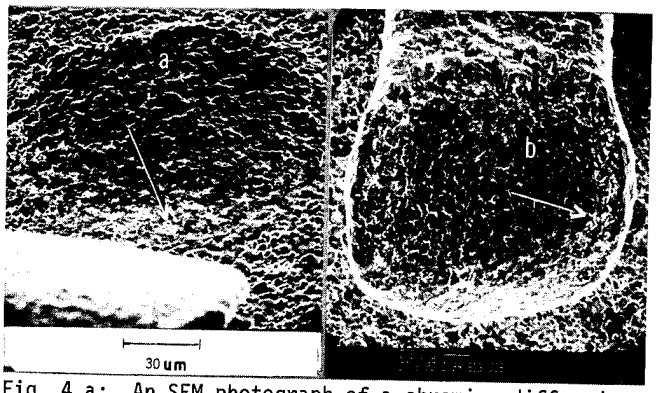

Fig. 4.a: An SEM photograph of a chromium diffused gold coated ceramic substrate with a peeled up beam lead in the foreground. An arrow reveals some of the tiny broken substrate welded areas.

Fig. 4.b: An SEM photograph of a peeled up beam lead revealing the tiny white appearing dots near the perimeter that were the welded areas.

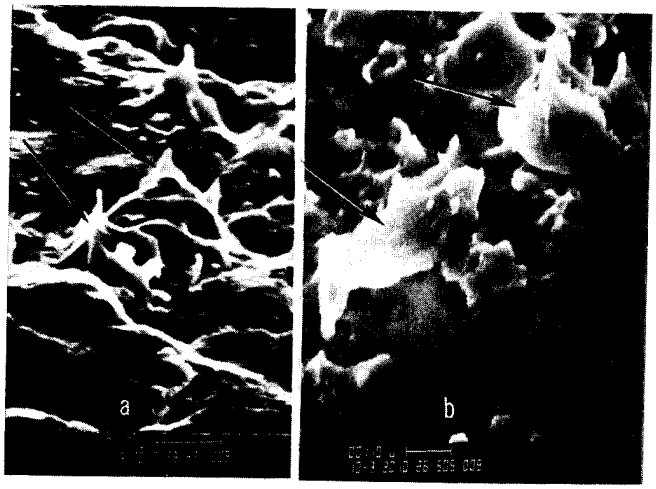

Fig. 5.a: The SEM photograph showing pieces of the substrate pulled off and sticking to the beam lead.

Fig. 5.b: High magnification SEM photograph of substrate weld breaks. (These are indicated by the arrows.)

ceramic substrate with a peeled up beam in the foreground. Examination of the beam lead bond depression in the substrate revealed tiny broken welded areas around the perimeter. The largest of these are indicated by the arrow. The beam is shown in Fig. 4b. The tiny white dots near the perimeter are the broken welded areas. The fact that the welded areas lie around the perimeter is in agreement with the deformation theory of thermal compression bonding by Tylecote[13]. A higher magnification view of substrate weld breaks is given in Fig. 5a. The arrows designate pulled up gold areas of one to two micrometers width. Figure 5b shows part of the beam-lead, clearly revealing pulled-off metal pieces from the substrate. In this case their size is two to three micrometers in width.

IV. EXPERIMENTAL APPARATUS

All stressing experiments and AE measurements were made using the versatile apparatus of Fig. 6. The force gage (A) can measure either an upward or downward force. The entire gage-probe apparatus can be rocked in front-to-back and sideways directions by the knob (B) en-

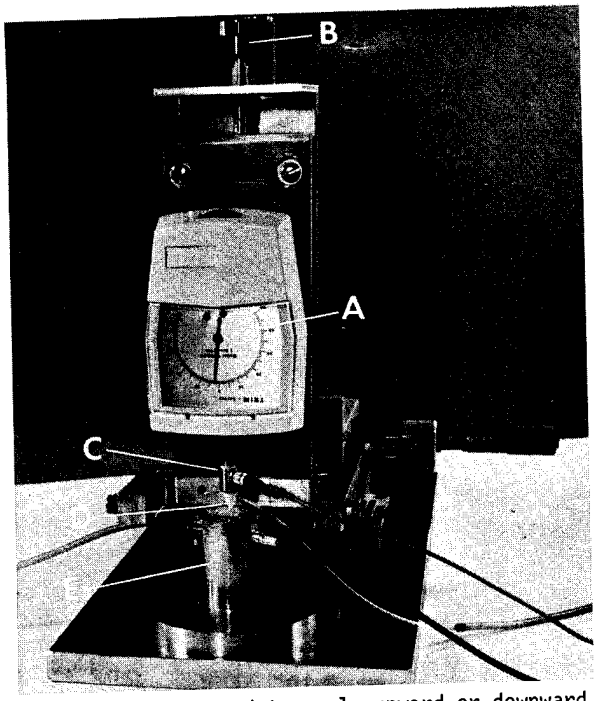

Fig. 6: Apparatus used to apply upward or downward force on beam lead devices and to detect any resulting AE. (A) force gage, (B) force angle control, (C) acoustic emission detector, (D) acoustic waveguide and force probe, (E) substrate holder with vacuum hold down and substrate AE detector.

abling a downward or upward force to be applied at an angle to a single row of beams at a time. The top AE detector-force probe (C-D) is screwed into the gage, facilitating rapid probe changes. The bonded test substrate is held on (E) which contains the substrate AE detector.

Close-up photographs of several top detector probes are shown in Fig. 7. Figure 7a is a ceramic probe designed to apply a uniform pressure on SR encapsulated beam lead chips. Figure 7b is a tungsten carbide conical probe with a 75 μm diameter flat on the bottom. This probe is used to test individual beams for AE. In Fig. 7c the probe is made of tungsten carbide and is essentially a beam lead bonding tool with smaller dimensions so that it contacts the horizontal projection of the beam near the silicon. The tips of all probes are coated with from 25-75 μm of SR to increase the acoustical coupling to the beams and to avoid metal to metal or silicon contact, since scraping can result in extraneous AE.

A substrate detector fixture is shown in Fig. 8. In this particular fixture the test substrate is held down against the AE detector by a cylindrical weight. Other substrate detector fixtures, such as the one that was shown in Fig. 6, use a vacuum hold down. The detectors are forced upward against the substrate by a spring. The surface of the substrate detectors is coated with a thin film of very compliant SR to facilitate acoustical mating with the ceramic substrate, thus avoiding the use of various sticky organic coupling materials that must be removed later. A textured SR surface is best. This is obtained by pressing ground glass, treated with a mold release agent, against the detector while the resin cures.

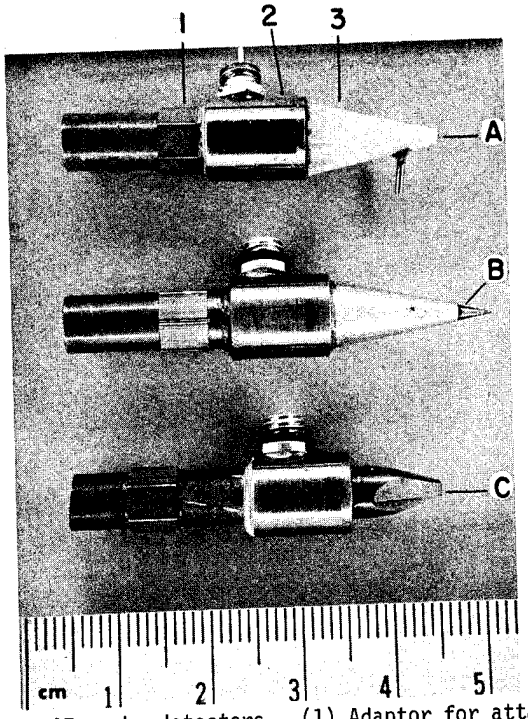

Fig. 7: AE probe-detectors. (1) Adaptor for attachment to the force gage, (2) AE lead zirconate titanate type detector, (3) acoustic waveguide and probe. Fig. 7a is designed to apply uniform pressure on SR encapsulated beam lead chips. The waveguide portion is ceramic and its tip is coated with SR or polyamide. Fig. 7b is designed to probe individual beams. The center tip is of tungsten carbide and has a 75 μm flat portion which is coated with SR. Fig. 7c is a modified tungsten carbide beam-lead bonding tool in which the inner walls are about 25 μm larger than the silicon chip on all sides.

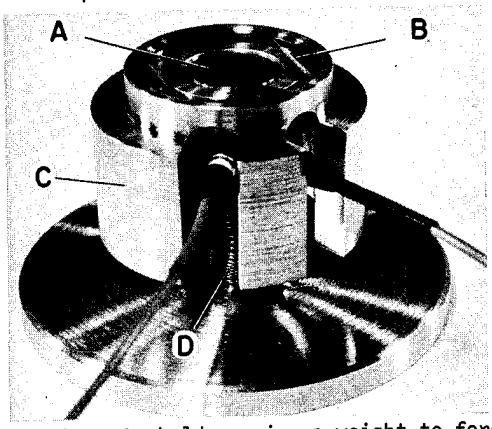

Fig. 8: Substrate holder using a weight to force the substrate against the detector: (A) AE detector, (B) simulated substrate (glass), (C) removable brass weight, (D) spring to force the detector against the substrate.

Several arrangements of signal preamplifiers, filters, and the digital pulse capturing equipment have been employed for various purposes. However, Fig. 9 shows the block diagram of the most frequently used system. The total gain in each amplifier channel is 80 dB. Each channel has a 24 dB/octave band pass filter or a tunable filter or both. The special digital trigger circuit[14] requires that a given number of cycles, selectable from 1 to 10, of a separately specified positive and negative amplitude signal occur within a specified time

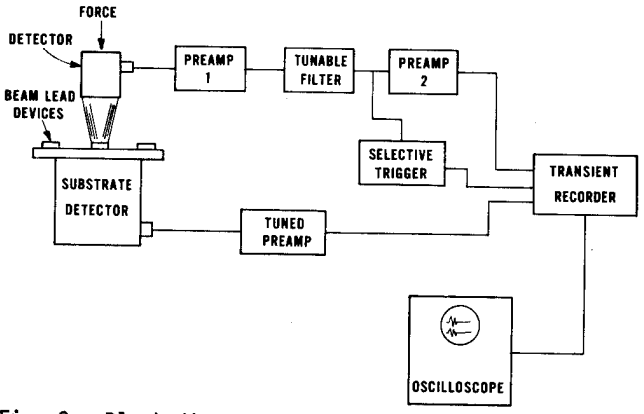

Fig. 9: Block diagram of the acoustic emission test apparatus.

frame for triggering the dual-channel pulse capturing equipment. The overall system is capable of detecting AE signals barely above the average noise level of the preamplifiers and considerably below various system and line transients. Most AE detector output signals produced in the present experiments were in the range of about 10 to 100 μV and were easily captured by the above equipment. Because of the variety of gain adjustments possible (preamplifiers, pulse capturing equipment, and oscilloscope), the vertical scale of most AE oscillograms will not be specified. The only important consideration is the signal to noise ratio and this can be easily observed from the photograph.

Experiments were run using various AE substrate detectors with the tunable filter. It was found that the maximum AE output was obtained from the 1 inch ceramic substrates at 350 to 400 kHz, and from bonded 16-lead, beam-lead chips at approximately 1 MHz. Calculations of the mechanical resonances of the substrate and chip could not anticipate the actual boundary conditions and were off by more than a factor of two. As a result of the measurements the substrate preamplifiers and detectors were chosen to peak at 375 KHz and the chip probe equipment at 1.1 MHz. The AE experiments to be described below will all assume such frequency responses unless otherwise stated. The digital trigger has been used in either the substrate or probe circuit but in most cases, it was used in the latter.

When the probe was in contact with the chip, there was essentially no mutual response from the probe and substrate detectors resulting from random AE sources remote to the beam lead device, regardless of the operating frequencies of each detector. A crack in the substrate would be strongly picked up by the substrate detector, but not by the probe, and a ceramic scribe-scratch on the tapered probe, which saturated its detector preamplifier, was only negligibly registered on the substrate detector. However, stress waves generated by a failure within the beam bond-anchor system resulted in a substantial signal in both channels. Therefore, in experiments where both substrate and probe detectors were employed, some AE output was required from each detector in order to define a failure, although their relative amplitude as well as the number of bursts recorded from each detector often varied considerably when the detectors were operated at different frequencies. The purpose

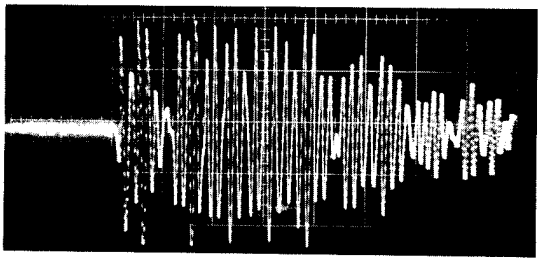

Fig. 10: Oscillogram of the AE obtained from pulling off a single well bonded beam lead with a force of ∿3.5 gf. Horizontal scale is 20 μs/div. The peak to peak output of the detector was greater than 1 mV.

of the present study was to develop a specific test method; however, monitoring a single AE source in two or more frequency bands, as in the present experiments, may be a fruitful approach to understanding the nature and mechanism of stress wave emission

V. EXPERIMENTAL RESULTS

(A) AE Results from Pulling Beam Leaded Devices

The silicone rubber-hook method of pulling beam-leaded devices, as described in Section II, was used to obtain quantitative information of various beam failure modes, since the pulling force is equally distributed between all beams. For this work the apparatus of Fig. 6 was used. The hook of Fig. 1 was substituted for the probe detector and all AE was picked up by the substrate detector.

In order to demonstrate the sensitivity of the AE method, all beams except one were cut and the remaining one was pulled to destruction. It broke at the bond heel. Figure 10 gives its AE pattern. Clipped waveform peaks indicate that the substrate detector output was significantly greater than one millivolt peak-to-peak during the initial part of the break. AE from such breaks generally continues erratically for several times the 200 μs shown in the figure. Most AE signals in this work are much smaller and of shorter duration.

For comparison a well bonded device with weak anchors had all but one of its beams cut in a similar manner to the above. Figure 11 gives the AE pattern of the single anchor failure. The peak to peak detector output in this case was approximately 0.3 mV.

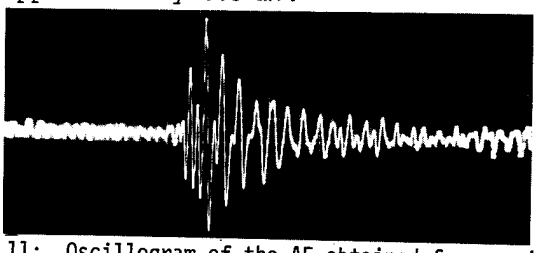

Fig. 11: Oscillogram of the AE obtained from a single anchor peeling off under a load of ∿3 gf. All other leads on the device were cut. Horizontal scale is 16 μs/div.

Pull tests were conducted on several well bonded devices that had weak anchors (peel strength ∿3 gf/anchor); a series of short bursts was observed starting at ∿1.5 gf/beam. Figure 12 gives a typical AE signal from peeling anchors. Similar well-bonded devices with

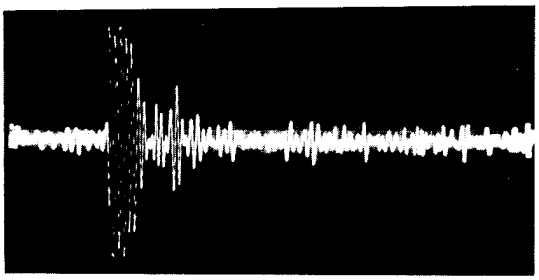

Fig. 12: A typical AE burst from a weak anchor. A pull-force of only 1.5 gf/beam was applied. The entire sweep is 200 μs in duration and the main AE burst is about 15 μs long.

strong anchors produced no AE until a force per beam of approximately 2.5 gf was applied and the bursts in this case were longer and higher in amplitude.

Pull tests were conducted on strongly bonded beam-lead devices to serve as controls for weakly bonded-beam experiments. A number of devices from four different manufacturers were tested. The devices from three of these sources produced no detectable AE until stressed to about 2.5 gf/beam, at which point the beam and the anchor system began to deteriorate. However, devices from the fourth source were quite different. Large bursts of AE were emitted when the devices were stressed to only 1 gf/beam and these bursts increased with increasing stress. This result was verified on three different device types and on lots purchased 18 months apart. Examination of these devices after they had been stressed to the 1 gf/beam level revealed no obvious problems; however, examination of them after stressing to the 2.5 gf/beam level (the point where well bonded devices from other sources generally emitted their first AE bursts) revealed elongation of the beams, separation of the relatively thick titanium layer, anchor peeling, nitride separation from the beams or silicon, and chips of silicon broken off at the anchor location, as shown in Fig. 13. Figure 14 gives a typical AE burst obtained by pulling a similar device to 1.2 gf/beam. Any of the mechanisms of beam system degradation shown in Fig. 13 could be responsible for bursts such as that of Fig. 14. It should be noted that a normal destructive pull-off or push test would not have revealed any problem since these beams ultimately broke with forces similar to those from other sources.

Poor mechanical integrity could possibly lead to premature electrical problems resulting from thermal cycling if the device is encapsulated in silicone rubber. Also, Dias[15] has calculated the forces on the beam lead system during bonding, and although not explicit in his calculations, it appears that beam system degradation forces may occur during bonding. If so, then these devices with poor mechanical integrity might occasionally be damaged during the bonding process and predisposed to relatively early field failure. It should be emphasized, however, that there is no experimental proof of this possible result of poor beam-anchor mechanical integrity, since no electrical tests have been performed in this study.

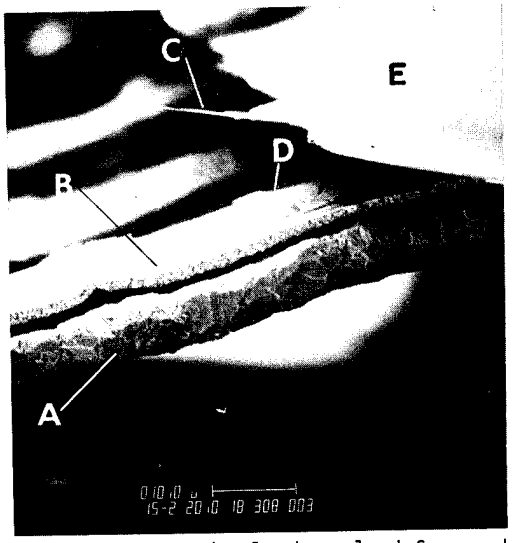

Fig. 13: SEM photograph of a beam lead from a device having poor mechanical integrity. The device had been subjected to a pull force of approximately 2.5 gf/beam. (A) gold beam, (B) separated titanium layer, (C) silicon nitride, (D) broken piece of silicon, and (E) silicon chip.

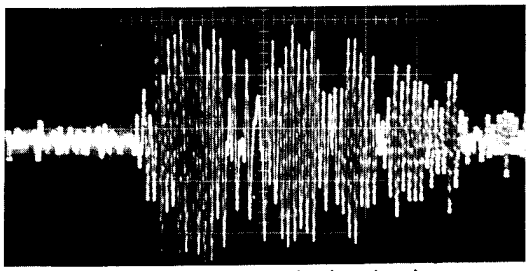

Fig. 14: An AE burst from a device having poor mechanical integrity as shown in Fig. 12. The pull force to produce this burst was only 1.2 gf/beam. Horizontal scale is 20 μs/div.

In a large series of SR pull tests on devices bonded to the chrome diffused substrates of Fig. 3, it was found that a pull force of between 1.0 and 1.5 gf/beam was required to produce AE from one or two weakly bonded beams on an otherwise well bonded device. A lower force, of between 0.5 and 1.0 gf/beam, was often sufficient when all of the beams were poorly bonded (i.e., the device would pull off at a force of 1.0 to 1.5 gf/beam).

(B) The Push-Down Test on Silicone Rubber Encapsulated Devices

Both well bonded controls and poorly bonded devices were encapsulated, except for the top of the chip, with a xylene-thinned silicone rubber[16] and allowed to cure for several days at room temperature, or in some cases overnight at 50°C. The top of the chip was then uniformly pressed downward by an SR tipped AE probe (Fig. 7a) mounted on the apparatus of Fig. 6. Well bonded controls of mechanically strong samples (2.5 gf/beam for initial AE in the pull test) required forces greater than 450 gf on a 16 beam chip before producing AE bursts. Well bonded devices of poor mechanical integrity (1.0 to 1.5 gf/beam for initial AE) required 200 to 250 gf to produce their first AE bursts. For both of these cases, devices containing one or more weak bonds (pull strength <1 gf/beam) generally emitted the first AE bursts

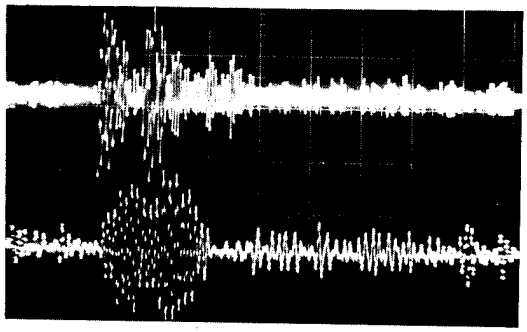

Fig. 15: AE bursts obtained by applying 75 gf downward on a silicone rubber encapsulated device. Horizontal scale is 20 μs/div. The top trace is the output from the force probe detector at 1.1 MHz and the lower trace is from the substrate detector at 375 kHz.

between 50 and 150 gf of downward force. An example of such AE output is shown in Fig. 15. AE from stronger bonds (∿2 to 3 gf/beam) was seldom detected until control-sample-magnitude forces (∿450 gf) were reached. The bonds in this study were covered with an opaque SR encapsulant making immediate examination and verification of failure modes impossible.

Although Fig. 15 shows the amplitudes of the top and bottom channels to be about equal, the AE output for this method of stressing is generally more intense in the top probe detector than in the substrate detector. The explanation is not apparent since the silicone rubber encapsulant is a reasonable transmitter of high frequency stress waves.

(C) Tests That Apply Force Only to the Beams

The two silicone rubber tipped probes, designed to avoid contact with the chip, have been used to apply a downward force on the horizontal portion of the beam extending outward from the chip. As previously stated, the simple resolution of forces analysis of a single beam indicates that ∿all of that force is applied as a torque tending to peel the anchor. Thus, probing a single beam or a single row of beams along one side of the chip provides an anchor adherence test. If all beams are probed at the same time, the torque cancels out, and force is applied only to the bond system.

Individual beams were probed with the silicone rubber tipped tungsten carbide probe of Fig. 7b to establish AE patterns for both anchor and beam failures. Figure 16 gives the twin AE oscilloscope traces resulting from applying a downward force of approximately 2 gf to a beam with a weak anchor. The anchor failed at an applied force of 3.5 gf. A well bonded beam having a strong anchor would typically collapse (curve downward until it touched the substrate) with a downward force of from 6 to 10 gf depending on the beam curvature and the bugging height. The beam-probe AE detector usually produces a larger signal than the substrate detector for anchor failures. When a very weak bond (failing at ≲1 gf/beam pull force) is probed in a similar manner, to about 3 or 4 gf, the AE signal intensities are generally reversed, as shown in Fig. 17. However, it should be emphasized that while these are typical AE patterns for their respective failure modes, those same failure modes may at times produce entirely different patterns.

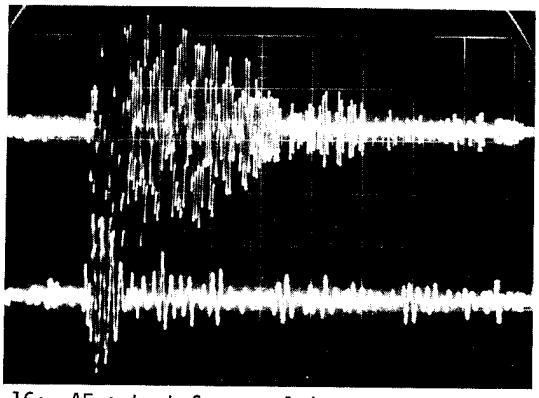

Fig. 16: AE output from applying a downward force of ∿3.5 gf to a single well bonded beam that had a weak anchor. The horizontal scale is 20 μs/div. The upper trace is from the probe of figure 7b (peak response is 1.1 MHz). The lower trace is from the substrate detector (peak response is 375 kHz).

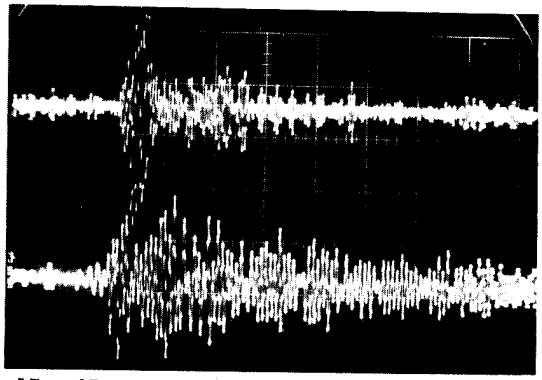

Fig. 17: AE output oscillogram resulting from a downward force of ∿4 gf with the probe of Fig. 7b on a single very weakly bonded beam (<1 gf pull force). The scales are the same as in Fig. 16.

Some experiments were performed using the single probe to try to detect AE from silicon nitride breaks. In general, breaks in the thin (∿2000Å) nitride skirt breaks were not detected, under normal circumstances. This was believed to result from higher frequency emission as well as poor stress-wave coupling into the chip and substrate. This was verified by coating the single beam probe with viscous acoustic mating compound and moving it sideways into an extended nitride skirt. A small AE burst was recorded in the probe detector circuit (1.1 MHz) but not in the substrate detector.

A different type of probe is shown in Fig. 7c. It is essentially a beam lead bonding tool but with shorter sides that contact the beams about 25 μ outward from the chip. In another experiment the rim of the probe was coated with silicone rubber and molded with a deep-undercut pattern of the beams, as shown in the sketch of Fig. 18. The operating principle of the probe is as follows: the probe is pressed down on top of the beams, the lower portion of the silicone rubber is forced against the substrate and bulges underneath the beam in such a manner as to lift the downward curving portion of the beam. A weak beam (failing at ≲1gf/beam in a pull test) will be lifted upwards resulting in AE. If the bugging height is uniform, and the probe is properly aligned and perpendicular with respect to the substrate, approximately 150 gf can be applied before collapse of the bugging height. Most of this force is dis-

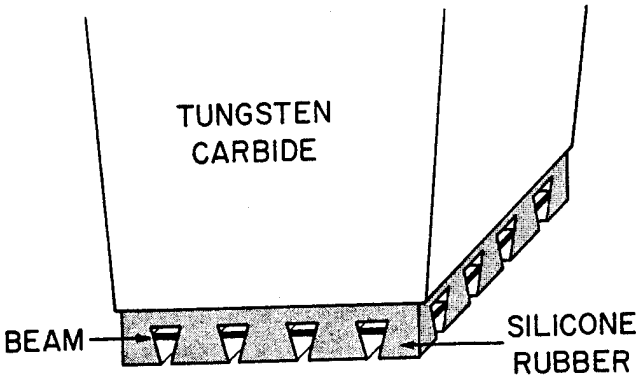

Fig. 18: Sketch of the undercut silicone rubber probe. The center portion of the probe is hollow so that no contact is made with the chip. When downward force is applied the SR elastomer is designed to compress and bulge under the beams.

sipated by compressing the SR and only a very small amount is actually applied as a lift force to the beams. The AE oscilloscope waveform of a weak bond stressed with this probe is given in Fig. 19. The largest AE signal generally appears in the substrate detector, partly because the bond is more closely related to the substrate and partly because of the relatively poor stress-wave coupling from the beams through the silicone rubber to the probe. After about 50 to 100 probings, the undercut portion of the SR on the probe became frayed and torn and had to be remade.

This probe concept appears to offer the best method of stressing weakly bonded beams. However, considerably more development is required to obtain reliable high force stressing by optimizing the elastomeric properties of the probe as well as obtaining better stress-wave coupling to the probe detector. This type of probe is only effective on devices having relatively uniform bugging height and with bonds that are extended away from the chip at least 75 to 100 μm. If the bond is very close to the chip there is no room for the rubber to bulge under the beam. If the bugging is nonuniform, one row of beams may be stressed more than another. In all cases there is nitride damage, which will be discussed in Section V(D). Thus, considerably more development is required before this probing method can be considered practical.

(D) Damage to the Silicon Nitride Skirt

The SR pull method, the single beam probe-push method, the chip-push method and the SR encapsulated-chip push-down method produce no observable damage to the silicon nitride skirt around beam lead devices, when used at reasonable force levels. However, the SR molded probe (Fig. 18) cleanly strips off the free silicon nitride skirt in all areas away from the beam and anchor, but it does not disturb the nitride on top of the beams. Potential damage due to moisture or other electrical leakage resulting from this has not been experimentally assessed in the present study.

The effect of nitride skirt damage is not clearly defined. If beam-to-silicon-chip electrical leakage is measured and if a nitride crack is also observed extending under the beam anchor, then inevitably the leakage is blamed on the crack, even though this requires a simultaneous

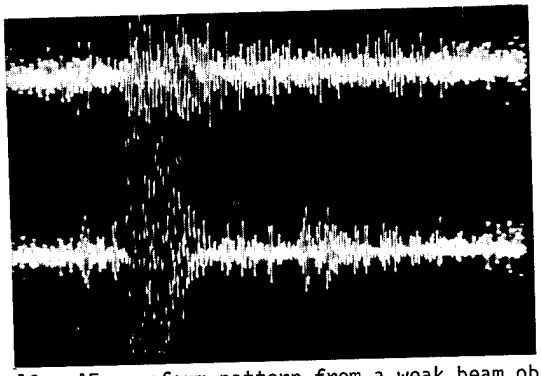

Fig. 19: AE waveform pattern from a weak beam obtained by applying a downward force of 50 gf to the beam system using the undercut silicone rubber probe of Fig. 18. Both the probe and substrate detectors were peaked at 1.1 MHz. The horizontal scale is 20 μs/div.

failure of the silicon dioxide protective layer. If no crack is observed, the blame is placed elsewhere or is considered indeterminate. An investigation of nitride integrity along with supporting beam lead device failure data was recently published by Swafford[17]. In the present program the nitride on innumerable integrated circuit beam leaded devices, bonded by a large number of different organizations, was visually examined and rarely revealed continuous nitride skirts. Generally, these skirts are at least frayed and torn at places in between the beams. Often, misalignment of the beams on the bonding tool during chip pickup resulted in nonuniform bugging height, and the nitride over the beams was cracked, separated, and/or strained. The ability of some SR conformal coatings to prevent electrical leakage and metal migration in corrosive atmospheres has been recently demonstrated by Jaffee and Sbar[16]. Such coatings may also protect and prevent leakage in the case of nitride damage by gettering out any residual moisture in the crack during rubber polymerization and then protecting the crack from subsequent moisture condensation. Since damage to the extended nitride skirt is so common, a logical solution to the problem would be to develop a method of manufacturing beam lead devices having no nitride extending past the edge of the silicon except for a short distance over the beams. As an alternative, a method should be found to remove the excess nitride after chip separation. Until a solution to the extended nitride problem is obtained or proof that a conformal coating will prevent any possible electrical leakage, the nondestructive status of the SR molded probe (Fig. 18) will be open to question.

VI. OTHER POTENTIAL USES FOR AE IN ELECTRONICS

There are a number of semiconductor device areas in which AE may be used to insure mechanical integrity. One of the most straightforward uses should be in assuring bond integrity on automated film carrier and reel systems. The mechanical stressing of bonds may be accomplished automatically as the carriers bend during winding on a reel: A rubber coated detector could be pressed against part of the outer or inner bonded lead frame as the frame undergoes some maximum allowable flexing or bending during or before being wound onto the reel. Both the inner and outer lead bonds could be tested at one time.

To show the feasibility of this procedure, some

Fig. 20: The top illustration is an SEM photograph of a portion of an automated gang-bonded integrated circuit. The bond on the left lifted up during minimal bending of the lead frame. The lower illustration is the AE waveform resulting from the lift up. The signal was picked up by the substrate detector tuned to 375 kHz. The horizontal scale is 20 μs/div.

AE tests were performed on three different types of automated gang-bonded integrated circuits. The first was of solder bump-Kovar inner-lead construction. The results of a slight bending at 15 gf applied to the uncut inner-lead frame produced the lifted lead shown in the upper illustration of Fig. 20. The lower illustration of Fig. 20 shows the substrate detector response to the AE resulting from that single bond lifting. Examination of this device and others from this lot revealed a tendency for the solder bump and its interfacial plating to separate from the aluminum bonding pad. A second type of gang-bonded device having an aluminum inner-lead construction, made several years ago, was tested in a manner similar to that used for the solder bump unit. One of these devices had several weakly bonded leads which emitted bursts larger than that of Fig. 20 when they separated. Similar tests on several minimodular type of bonded devices revealed no failures even though the visual appearance of one was quite poor, as shown in Fig. 21. Destructive pull tests verified that the few available samples, including that of Fig. 21, happened to be well bonded. Thus, an AE test can be used to assure bond integrity on gang-bonded systems.

Various discrete components such as chip capacitors bonded into hybrids can be stressed by applying a small shear force. If weakly bonded, then AE should be detectable. One such capacitor was subjected to a downward

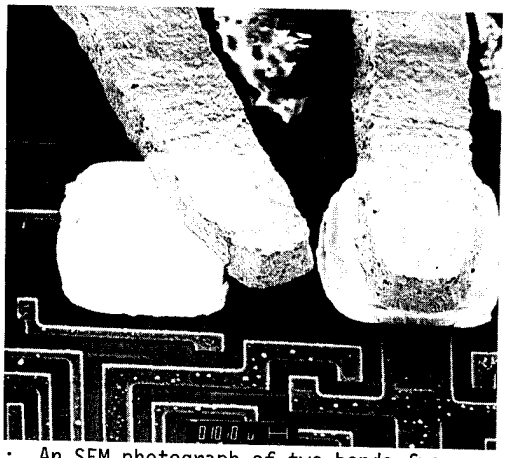

Fig. 21: An SEM photograph of two bonds from a minimodular type of bonded integrated circuit. This device, including the visually poor bond, remained intact and produced no AE even though the bonds were stressed to approximately four times the value required to produce the bond break in Fig. 20.

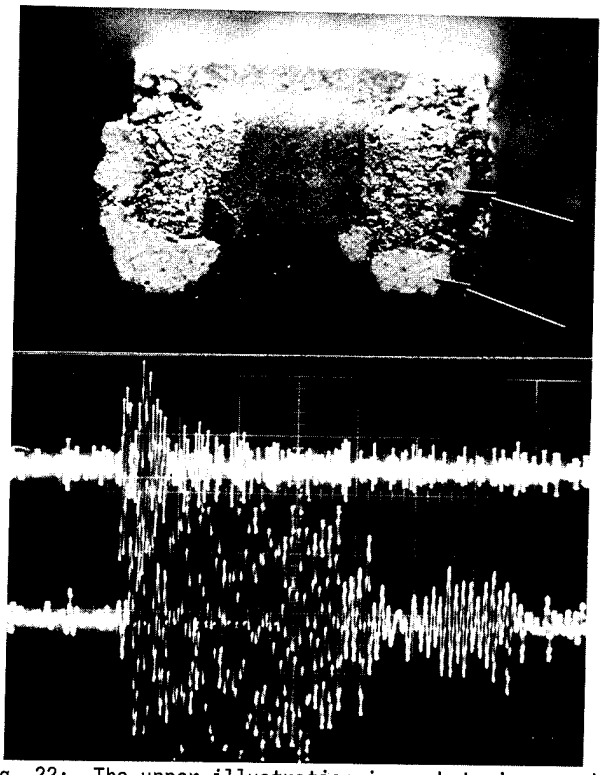

Fig. 22: The upper illustration is a photomicrograph of a 2 mm long chip capacitor removed from its hybrid circuit. The arrows point to the very small areas that had been conductive epoxy bonded to the circuit. Below is the AE waveform resulting from applying 200 gf with an AE probe to the top on the capacitor before it was removed from the circuit. Both 1.1 MHz probe detector and 375 kHz substrate detector waveforms are shown. The horizontal scale is 20 μs/div.

force of 200 gf. It emitted the AE signals shown in the lower portion of Fig. 22. The capacitor was then broken free and photographed. Only about 15% of the intended area was actually epoxy bonded as shown by the arrows on the right side.

Since propagating cracks emit stress waves, cracks in power device chips should be detectable by current pulsing the device. Nonuni-

form heating of the chip during such pulses should expand the crack and cause the emission of stress waves. Cracks and flaws in hybrid substrates should also be detectable. One such cracked substrate was detected in the present program while pressure testing silicone encapsulated devices. General package integrity should be assessable with AE by stressing the package under pressure or with rapid heating. Such conditions have been observed to destroy the hermeticity of weak packages[18]. AE detection equipment could be used in conjunction with the nondestructive wire-bond pull-test to assist in determining the maximum nondestructive force to be applied. It could then be used to monitor that test to give ultimate assurance of its nondestructive nature. A limited evaluation of this was carried out as a preliminary to the present work and it appears promising. Bonds that partially lifted up during a nondestructive pull were easily detected.

VII. CONCLUSIONS

This study has revealed considerable differences in the mechanical integrity of beam lead bond-anchor systems and demonstrated that AE testing offers a unique method of assessing new beam lead-nitride-anchor designs and of maintaining quality control on normal production. General deterioration of the beam-anchor system begins at pull forces of from 1.0 to 2.5 gf/beam, depending on the manufacturer. Thus, no test can be considered nondestructive that applies forces higher than about 2.0 gf/beam to the mechanically stronger beam systems and perhaps 0.8 gf/beam to the weaker ones. The maximum safe force for each separate manufacturing procedure must be obtained experimentally. It was found that a pull force from about 1.0 to 1.5 gf/beam was required to reveal a few poorly bonded beams in otherwise well bonded devices; however, this force is equal to the beam-system deterioration force for devices with poor mechanical integrity. For such devices no meaningful nondestructive pull test is possible. The forces applied to the beam-anchor system for all methods of stressing, except the pull test, are dependent upon the shape of the individual beams as they extend from the chip, as well as upon the uniformity of the bugging height. Thus, to effectively use these tests, more operator care is required than is usually achieved in typical production line environments. Compliant bonding and other systems incorporating automatic chip loading should be more adaptable to the probe type measurements. The SR pull test is simple to employ and can be considered nondestructive if the user does not object to leaving cured SR in the package. The same material is, after all, often used as a conformal coating. The silicone resin could be applied to chips with modified epoxy die-attach equipment at either a 100% or some lower percentage sampling basis. Of the methods studied, only the pull test could reliably reveal weak bonds having equivalent strengths greater than 1 gf, although the undercut silicone rubber probe and the sideways shove method can probably be developed to exceed that force.

The main difficulty in the present work was encountered in the development of means of nondestructively stressing delicate, irregularly extending beam leads. However, many other potential uses of AE in electronics offer no such problems. Any system whose bond strength normally is destructively tested by shearing or probing, such as flip chips or capacitor chips in hybrids, can be nondestructively tested by that same method at a lower force using AE as the failure indicator. Both the inner and outer lead bonds on automated tape-bonded integrated circuits can be flexed or probed, while monitoring for failures with AE equipment, to gain assurance that they are well bonded. The mechanical integrity of large packages can likewise be assessed by rapid heating, high or low pressure, or other means of stressing. Thus, it appears that AE will have an increasing role in assuring reliability in the microelectronics field.

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AN EVALUATION OF SILICON DAMAGE RESULTING FROM ULTRASONIC WIRE BONDING

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Summary

Ultrasonic wire bonding is a dynamic process which has been found to introduce material damage to improperly protected silicon. Damage is detected through the generation of steam oxidation induced stacking faults in the silicon after the metal and oxides have been removed. Silicon of both (100) and (111) orientations were evaluated with faulting being found predominately on those (111) planes whose lines of interesection with the surface were most nearly perpendicular to the applied direction of ultrasonic motion. Stacking faults predominate at the outer periphery of the bond. In addition to a correlation between the direction of ultrasonic motion and the fault planes observed, different fault planes operate at the toe and heel of the bond. No stacking faults are induced for normal ultrasonic bonding parameters and standard thicknesses of metallization (10 KÅ) using 2-mil bonding wire. This method of analysis provides a means for evaluating changes in materials and processing to improve bond reliability.

Introduction

Purpose

Established methods for the detection of wafer defects are used to evaluate ultrasonic wire bonding damage to the silicon substrate of semiconductor devices. The technique for growing thermally induced oxidation stacking faults at locations of surface damage is particularly suited for ultrasonic bond studies because a directionality of stress can be determined. By utilizing silicon as a defect gauge, a relative measure of the effectiveness of changes in bonding materials and machine designs becomes possible. Strain features associated with catastrophic breakage (cratering) of the silicon below the bond provide information on the mode of loading which contributed to the failure.

Historically, bond improvements have been related to pull-strength data. As the desired bonding conditions are approached by increasing bonding parameters, the failure mode shifts from the bond interface to the wire.[1] This study represents an effort to monitor changes at the bond interface for the total range of bonding conditions. Ideally, this approach will complement the work of other investigators who are concerned with improving process control variables.[2-3]

Methods for Investigating Defects

Wire bonding to a zero defect silicon surface and subsequently removing the wire material chemically allows bond damage to be studied directly. The three forms of defect analysis selected for this study were etching, x-ray topography, and thermally induced stacking faults by steam oxidation. Standard etch pitting techniques are useful in establishing the presence of line or planar defects at the surface of the sample.[4] X-ray topography provides information concerning not only physical defects, but also strain fields in the crystal.[5-6] Steam oxidation followed by etching detects strain effects which are less than the resolution of x-ray topography. This study is predominately involved with oxygen induced stacking faults as a technique for evaluating ultrasonic bonding defects.

Mechanical damage on a silicon crystal surface provides nucleation sites for the growth of extrinsic stacking faults during high temperature oxidation.[7-10] The slip planes for deformation are also the extrinsic fault planes formed in silicon during oxidation. This results in a correspondence between stress damage that is so slight that it cannot be directly detected and growth defects which are easily observable. A unique advantage of the stacking fault approach is that the orientation of faulting characterizes the direction of stress which generated the surface damage.

The magnitude of the resolved shear stress, τ, on a given slip plane for an applied stress, σ, can be determined by $\tau = \sigma \cos\phi \cos\lambda$ where ϕ is the angle between the tensile axis and the normal to the slip plane and λ is the angle between the tensile axis and the direction of slip. The condition for shear becomes optimum when the Schmid factor, $(\cos\phi \cos\lambda)$, reaches its maximum value of 0.5. While the {111} planes for (100) silicon wafers have a Schmid factor of 0.472, those for (111) silicon are 0.315. Because the Schmid factor for the (100) orientation is more favorable for shear than that of (111) silicon, it can be postulated that the (100) orientation would be more sensitive to stress than the (111) surfaces.

Ultrasonic bonding involves an applied two-directional force system. In addition to the pulse developing a stress parallel to the surface, there is a machine load which produces a normal stress to the silicon. While a stress in one direction might be relieved by flow along several different planes with a favorable Schmid factor, the addition of a second force direction effectively limits the number of active planes. Figure 1a illustrates the condition of gross flow along a slip plane with two-directional loading. Following steam oxidation, extrinsic fault growth as exposed by etching has a lenticular configuration with the curved portion of the fault being in the original stress direction (Figure 1b).

Experimental Procedure

Equipment and Techniques

The major portion of the bonding program was performed using 1 and 2-mil* wire on a High Rel K & S 484 wire bonder with a UTI transducer and a model 5C-HR power supply. This was complemented by bonds using 10-mil wire on a K & S 486 large wire bonder, an Orthodyne transducer, and a model 363-15 power supply. An Orthodyne model 20 bonder was used for 20-mil wire. Ribbon bond characteristics were obtained using a Motorola bonder with an Orthodyne transducer and a model 363-23 power supply. Flat bonding wedges were used for 1 and 2-mil wires and concave wedges for the 10 and 20-mil wires.

Samples were fixtured to the bonder both in the standard manner and using a vacuum chuck. Comparative pull-strength tests for the two methods proved identical.

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*0.001 in = 1-mil = 25.4 μm

Bond Materials

For this study, 1, 2, 10, and 20-mil round wire and 3.5-mil x 2-mil ribbon wire were selected. The Al-0.5% Mg composition was chosen for the majority of the bonding because of its observed versatility to satisfactorily bond to aluminum metallization, silicon, and thermal oxide.

As a bonding surface, silicon possesses various unique features. It has a well defined crystalline surface which can be repeatedly controlled from one test condition to another and has been extensively studied with respect to its deformation properties. For these reasons, it was selected as a gauge material to evaluate the effects of the various bond parameters.

Bond patterns on silicon can be viewed directly by chemically removing the wire and aluminum metallization with warm, concentrated HCl. Thermal oxide and other residual oxides are dissolved using HF. Surface defects including stacking fault features are revealed by a Wright etch solution.[4]

Defect Study

Thermally induced stacking faults generated by steam oxidation represents a sensitive technique to evaluate critically strained regions in silicon. This procedure involves steam oxidizing the silicon (after metal removal) at 1115°C for 100 minutes. The oxide is then removed and the sample etched for 30 to 300 seconds. The stacking faults observed at the surface of the silicon lie on {111} planes and are readily evident following etching. To complement the surface defect study, standard x-ray topography methods provide a means for determining the significance of bulk silicon damage resulting from ultrasonic wire bonding. The Lang transmission and Berg-Barrett reflection x-ray techniques were utilized. In the former, 220 reflections (MoL_α) were used to investigate defects throughout the crystalline bulk while the 440 reflections (CuK_α) for the Berg-Barrett method provided data on surface imperfections. Exposures were several times longer with transmission than reflection and the resolution for transmission was somewhat poorer.

Experimental Results

General Bond Features

The ultrasonic bond pattern between aluminum wire and aluminum metallization has been well documented as initiating at the bond periphery.[2-3] Figure 2 shows the bond pattern for an underdeveloped 20-mil wire bond to an aluminum plate which has been exposed by peeling away the wire. The substrate is textured so that the severity of the wire flow to this surface can be readily identified. While the central area has not experienced damage as evidenced by the texture of the plate still being visible, both bonding and surface damage are located at the periphery of the bond.

Pull-test values have been the standard means for evaluating improvements to bond reliability. For any particular set of bonding material conditions (metallization--thickness, hardness, surface impurities; or wire properties--composition, hardness), there are normally several bond parameter settings of load, power, and time which produce acceptable pull-strengths. A typical bond "window" for pull-strengths exceeding 15 gm for various ultrasonic power and pulse duration (time) values at a constant load using ribbon wire and Al metallization (10 KÅ)* are presented in Figure 3a. It is evident that high strength bonds are made at many power-time combinations. A typical distribution of lifts and breaks is given in Figure 3b. Highest strengths are associated with the region of lifts plus breaks, i.e., conditions at which both lifts and breaks are observed. In the pure lift region, bonding has not developed adequately, while in the pure break region, good bonds have been formed but the wire is so grossly deformed that failure occurs at the heel. Bonding of the wedge to the top of the wire becomes significant with increased power and time. The range of wedge adherence exceeding 21 gm is presented in Figure 3c with the combined features of the bond window given in Figure 3d.

Ultrasonic bonding directly to silicon results in a peripheral pattern being permanently grooved into the silicon. In Figure 4, the bond pattern in silicon after etching is observed to have a grooved structure perpendicular to the pulse direction. This appearance is similar to the microridge configuration commonly observed on the top of the wire.[2] Because silicon is brittle, the pattern cut into the surface represents a permanent record of the bond formation history and has been used to account for features of the bonding mechanism.[11]

Defects Generated During Ultrasonic Bonding

Since both bulk and surface damage to silicon was of concern, two methods were employed to evaluate ultrasonic wire bonding damage to silicon--x-ray topography and steam oxidation induced stacking faults.

1. X-ray Topography

X-ray topography is a standard method used in the semiconductor industry to detect the presence of damage in silicon. For example, dislocations, slip, stacking faults, and gross strains are distinguishable with this analytical tool. Studies on silicon, where both 2-mil and 10-mil wires were ultrasonically bonded and chemically removed, revealed no detectable damage using either the Lang (transmission) or the Berg-Barrett (reflection) technique. This is illustrated in the reflection topograph of Figure 5a where a reference mark is present on the wafer near a residual bond site. Topographs (both reflection and transmission) revealed the reference mark; but no line defects, planar defects, or even strain fields could be associated with the bond. This does not mean that bond regions are strain free as will be discussed further in the next section. It does indicate that x-ray topography is not sensitive enough to detect the residual strains formed by ultrasonic wire bonding.

2. Thermally Induced Stacking Faults by Steam Oxidation

Considerable work has been documented concerning the evaluation of defects in silicon through the use of steam oxidation.[7,8] Following the removal of the steam oxide, stacking faults are not evident until the sample has been etched. To most fully characterize the nature of faulting, samples are normally etched for various times. Short etching times have the advantages of distinguishing faults in high fault density regions. Longer etching clarifies the directionality of faulting, however, individual faults in the high density regions tend to become indistinguishable. The sample which had been studied using x-ray topography (Figure 5a) was steam oxidized at 1115°C for 100 minutes. The location of the bond pattern, which was not evident previously, now can be located exactly in the x-ray topograph of Figure 5b as a result of the steam oxidation treatment.

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*10 KÅ = 1 μm

A series of 2-mil Al-0.5% Mg wires was bonded directly to a (100) silicon wafer (no metallization) using a variety of machine parameters. It is evident from the typical stacking fault pattern of Figure 6, that faulting correlates with the outer periphery of the bond as did the deformation characteristics of the Al-Al bond of Figure 2. Several fault features are obvious. Faulting is highly directional with respect to a force system in the pulsing direction. There is no distinct relationship between the intensity of grooving and the concentration of faulting. Fault density does not increase in proportion to either increased power or increased time. Bond dependent faults are predominately of the same size.

Because silicon is brittle, the grooved pattern cut into the surface represents a total record of the bonding process. The grooved structure is indicative of the surface material being forcefully dissociated from the silicon while stacking faults delineate strained regions in the crystal lattice. The characteristics of faulting predominate at the bond periphery and relate to a loading in the pulse direction. There is a gross flow of wire material due to the ultrasonic softening.[12] The observed fault patterns suggest that the ultrasonic motion is the source of the damage which results in faulting. Peripheral faulting does not substantiate a concept of the wire being scrubbed across the surface during bonding.

To verify the uniqueness and sensitivity of the oxidation process, another zero defect (100) wafer was bonded and the wires chemically removed. This sample was heated at 1115°C for 100 minutes in N_2 instead of steam. Etching of the wafer resulted in a stacking fault free structure. Reheating the wafer to 1115°C for 100 minutes in steam, cleaning the oxide from the surface, and etching, resulted again in a defect free structure. It is concluded that the residual damage to silicon as a result of ultrasonic wire bonding in this case is not severe, even with no thermal oxide or aluminum metallization on the chip.

Induced Stacking Faults - Tool for Defect Study

For {100} silicon with the wire and pulse along the <110> direction, the line formed by the intersection of the [111] stacking fault planes and the surface is either perpendicular to or parallel with the pulsing direction. Specifically, for pulses in the $[1\bar{1}0]$ and $[\bar{1}\bar{1}0]$ directions on a (001) Si surface, the $(\bar{1}11)$ and $(\bar{1}\bar{1}1)$ planes intersect the surface as lines perpendicular to the direction of wedge motion and the $(1\bar{1}1)$ and $(\bar{1}11)$ planes intersect as lines parallel with the pulsing direction (Figure 7a). The presence of different directions is maximized on silicon for bonds to a protective thermal oxide surface (Figure 7b). Note that the obvious silicon damage of Figure 4 is avoided by the oxide protection.

For a force in the $[1\bar{1}0]$ direction, maximum shear occurs on the $(\bar{1}11)$ plane and for a force in the reverse direction, $[\bar{1}10]$, the maximum shear is on the $(\bar{1}\bar{1}1)$ plane. In evaluating numerous bond patterns, it became evident that one half of the bond (toe or heel) encounters a stress predominating in one direction while the other half of the bond encounters a stress in the reverse direction. This is particularly evident in Figure 8a where the lighter appearing lines (faults on $(\bar{1}11)$ planes) were caused by forces in the $[1\bar{1}0]$ direction and the darker lines (faults on $(\bar{1}\bar{1}1)$ planes) were caused by forces along $[\bar{1}\bar{1}0]$ direction. The boundary separating the toe and heel regions is oftentimes not at the same position on both sides of the same bond as exemplified in Figure 8b. This indicates that the bond experienced twisting during its formation.

It is concluded that superimposed movements occur during bonding. In addition to the two-force system applied, a subsequent rocking and twisting promotes a moment force which is a resultant variable to the bonding process. The stacking fault method of analysis provides sufficient sensitivity to bonding stresses for it to be a tool in evaluating the force systems imposed upon the bonding process.

To verify the observations made for round wire on (100) silicon, stacking fault features for flat ribbon bonds to (111) silicon were investigated. The bonding tool extended completely across the width of the ribbon so that the sides of the bond were directly below the wedge. For a pulse in the $[11\bar{2}]$ direction on a (111) surface, the high shear stress stacking fault plane is $(11\bar{1})$; for the reverse direction of $[\bar{1}\bar{1}2]$, two stacking fault planes, $(\bar{1}11)$ and $(1\bar{1}1)$, equally realize a maximum shear stress condition as shown in Figure 9a. From the ribbon bond stacking fault pattern for (111) silicon in Figure 9b, it is evident that one-half of the bond (toe) has mainly $(11\bar{1})$ faults; while the other half of the bond (heel) is characterized by $(\bar{1}11)$ and $(1\bar{1}1)$ faults.

The stacking fault patterns for ribbon wire correlate with the information from the round wire study. Again, damage predominates at the outer periphery of the bond.

Material Considerations

Both Al-0.5% Mg and 99.99 Al wire bonded more readily to silicon and silicon oxide than Al-1% Si wire. The ability to wire bond directly to Si and SiO_2 allows a continuous study of bond features as a function of metallization thickness. While bonding can be achieved through a range of metallization thicknesses, the bond window does shift. The bond times required for Si and SiO_2 surfaces are relatively long compared to those samples with increased metallization thicknesses. Both round and ribbon wire bonds were made to metallization thicknesses of 0.5, 1, 3, 6, 10, 20, and 30 KÅ of aluminum directly over Si. The wire and metallizations were dissolved chemically to confine as much as possible the interpretation of observed defects to the bonding process. Tensile strengths for the 2-mil round wires are given in Table I.

TABLE I

2-Mil Round Wires

Wire	Tensile Strength (gm)
Al-1% Si	47
Al-0.5% Mg	39
99.99% Al	21

Bonds to metallization thicknesses up to 3 KÅ resulted in pronounced surface cutting of the silicon at the bond periphery. The tendency to crater was most prevalent for the thin metallizations. The 6 KÅ condition represents the transition range in which surface damage to the silicon and some cratering is still observed. For 10 KÅ to 30 KÅ Al, surface damage becomes undetectable using acceptable bond window machine parameters. The frequency of cratering tended to increase with increased wire hardness. A direct correlation between the 3 wires to Table I was not possible because a consistent set of bond parameters did not produce the same bond and deformation features.

A 10 KÅ thickness of thermal oxide provided suitable protection to the silicon for standard bond window parameters. For excessively high power, directionality of faulting tends to be more mixed than that observed for direct bonding to silicon (Figure 7b).

Cratering

The bonds of Figure 10 typify the cratering problem with silicon failure at the center of the bond in one case, and in the other, fracture outside the bond region. The wire of Figure 10a is bent in the opposite direction from the configuration it had at the time of bonding. This shows wedge adherency continued after bond formation and silicon failure. An example of another bond (1 KÅ aluminum metallization) in which cratering has occurred is present in Figure 11. Distinctive regions of forward and reverse forces are evidenced by the stacking fault orientations. The unequally balanced directionality of faulting on the sides of the bond can be attributed to a stress direction which is angled with respect to the wire axis. Cutting patterns in the silicon at the opposite ends of the bond confirm a misalignment between the wire axis and the deforming stress direction. (A similar pattern existed in Figure 8b).

Holographic studies have shown that when the wire deviates from a linear alignment with the wedge displacement, a twisting motion is developed through the wedge to the horn assembly.[13] Wedge adherency to the top of the wire combined with a twisting motion out of the bond plane would account for the cratering observed in silicon.

To maximize silicon deformation features for determining directional forces, bond orientations may be varied. A bonding pulse in the [$\bar{1}$01] and [10$\bar{1}$] directions for (111) silicon (Figure 12) results in an equal probability of fault growth in each direction. To better sense a twisting action, bonding in the <100> directions for (100) silicon provides a two-plane probability for both pulse directions (Figure 13). Note that the faults are longer yet less numerous for (100) as compared to (111) silicon.

Cratering features are predominately related to the last phase of bonding. Wedge adherency due to excessive bond parameters as well as external low frequency ambient vibrations have been observed to be particularly detrimental. Material modifications such as thicker metallization and softer wire are considered to effectively reduce the intensity of twisting forces between the wedge and the silicon substrate.

Conclusions

Ultrasonic wire bond damage to the silicon substrate of semiconductor devices for a controlled process is not detectable by standard techniques. The probability of damage increases as the bonding process becomes uncontrolled. Wedge adherency is particularly detrimental and increases with increasing power and time. Variable loading including misalignment between the wire axis and pulse direction promotes silicon failure (cratering).

Bulk silicon damage for normal bonding parameters is less than the resolution of x-ray topography. Oxidation induced stacking faults distinctively define regions of ultrasonic wire bonding damage. Not only is this method highly sensitive to surface defects, it also provides a means for recording stress directions imparted to the silicon during bonding.

For those conditions where cratering continues as a reliability factor, increased metallization thicknesses and softer bonding wire remain as material modifications to limit catastrophic failures of the silicon substrate.

Acknowledgments

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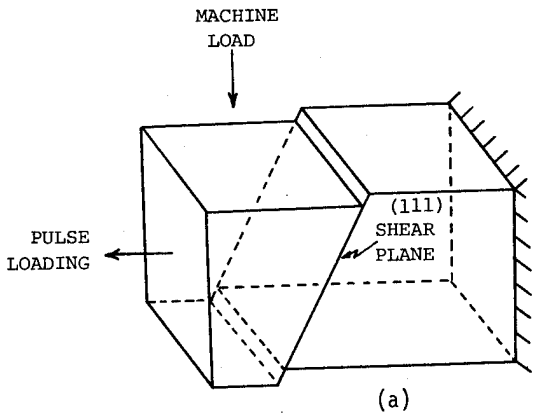
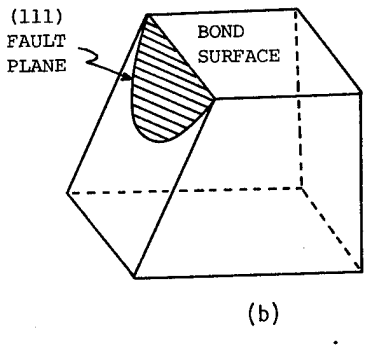


Figure 1. (a) Gross flow resulting from the 2-force bonding system is restricted to planes of a specific orientation.



(b) Extrinsic fault growth initiating from a surface damage site, as exposed by etching, has a configuration with the curved portion of the fault being in the original stress direction.

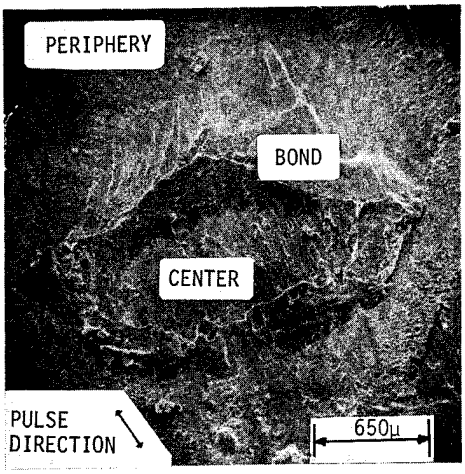


Figure 2. Peeling a 20-mil Al-0.5% Mg wire from an aluminum plate reveals a bond pattern existing within a roughened outer bond periphery.

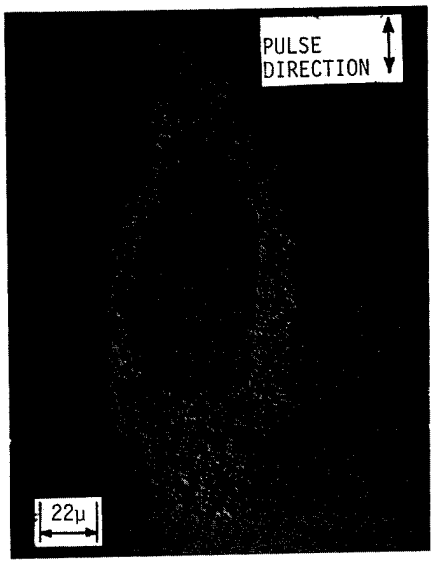


Figure 4. Chemically removing the aluminum wire from a direct bond to silicon and etching results in a grooved peripheral region and an apparently undamaged central area.

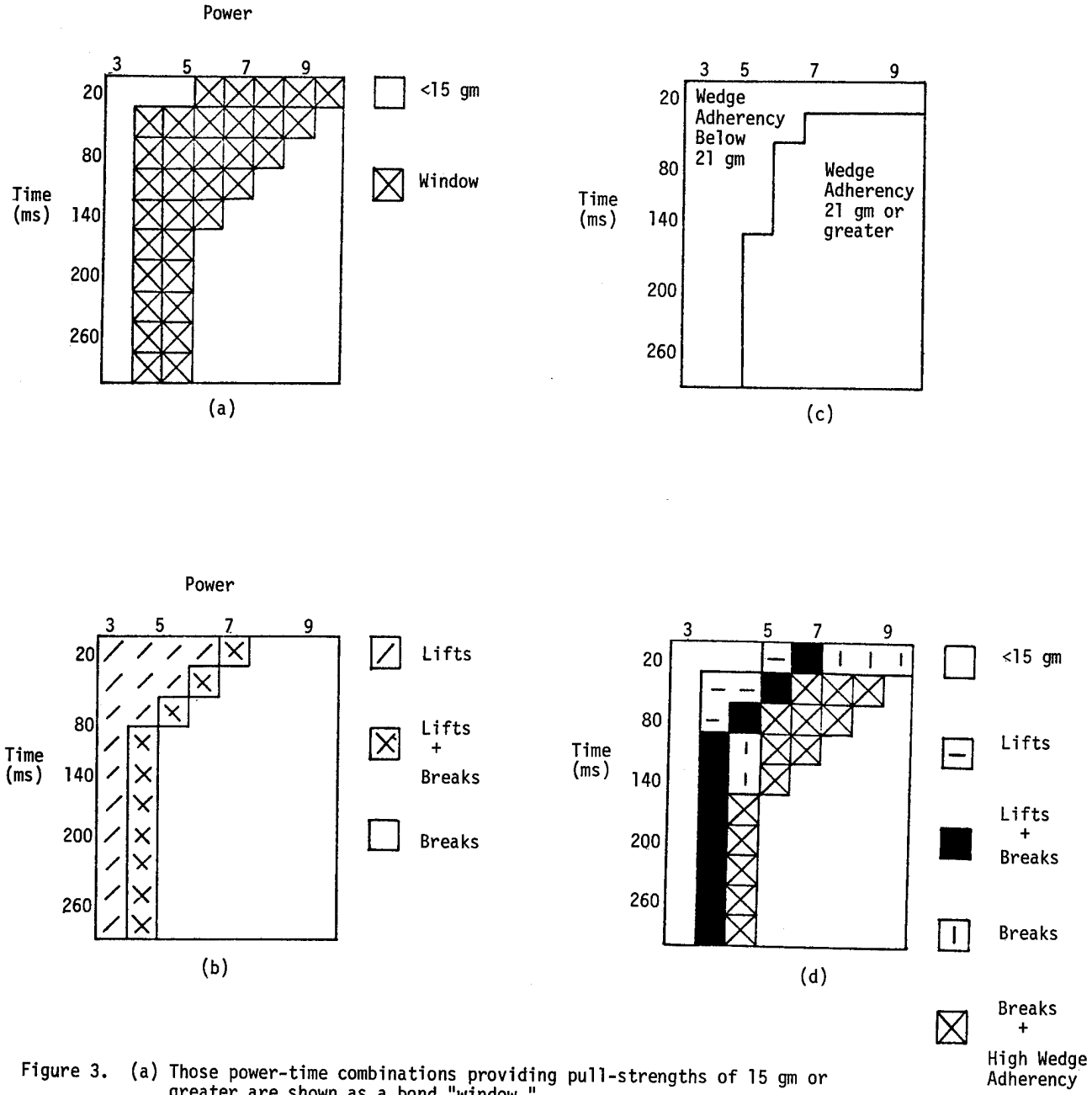
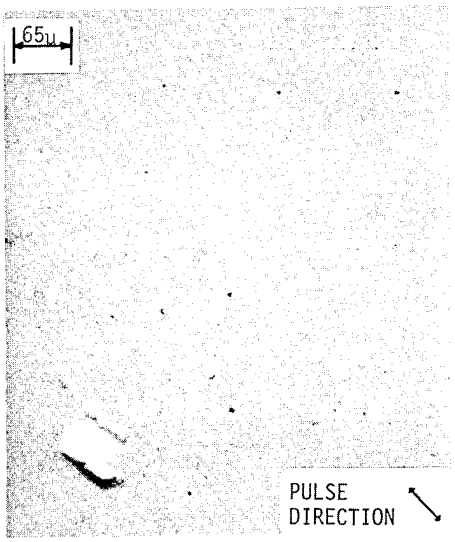
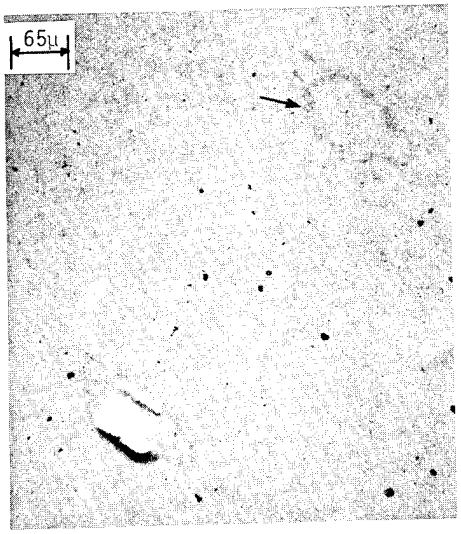


Figure 3. (a) Those power-time combinations providing pull-strengths of 15 gm or greater are shown as a bond "window."
(b) The types of failures reveal the lifts plus breaks region to lie within the bond window.
(c) Wedge adherency becomes appreciable within the bond window as evidenced by the location of the 21 gm "sticking" boundary.
(d) Combined factors present within bond window.



(a)



(b)

Figure 5. A cratered wire bond position is evident in the lower left-hand corner of both the (a) and (b) reflection topographs. Only with thermally induced stacking faults does the strain pattern of another bond become detectable by x-ray topography (upper right-hand corner of b).

Figure 6. Stacking faults in (100) silicon typically form at the bond periphery from forces in the pulsing direction.

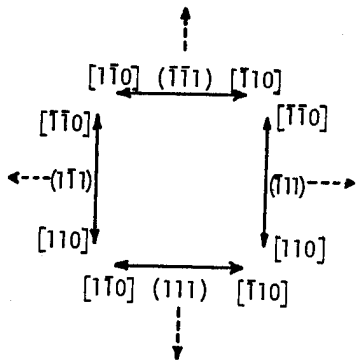


Figure 7a. Solid arrows show the line orientations observed for the intersection of {111} stacking fault planes with a (001) reference surface. Dotted arrows represent the direction of the intersecting planes into the crystal.

Figure 7b. The directions for the stacking fault pattern on the (001) silicon surface for a 2-mil round wire bonded to SiO_2 can be interpreted from the orientations given in Figure 7a.

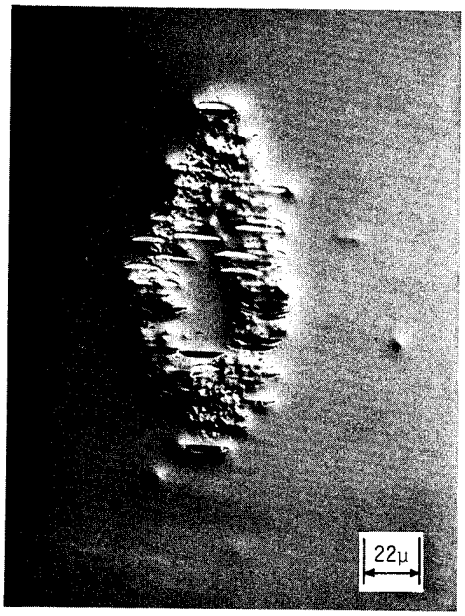


Figure 8a. Stacking faults in (100) silicon form at the bond periphery from force in the pulsing direction. Note that the dark appearing faults tend to be at one end of the bond and light faults at the other. This indicates that a different force direction predominates at opposite ends of the bond.

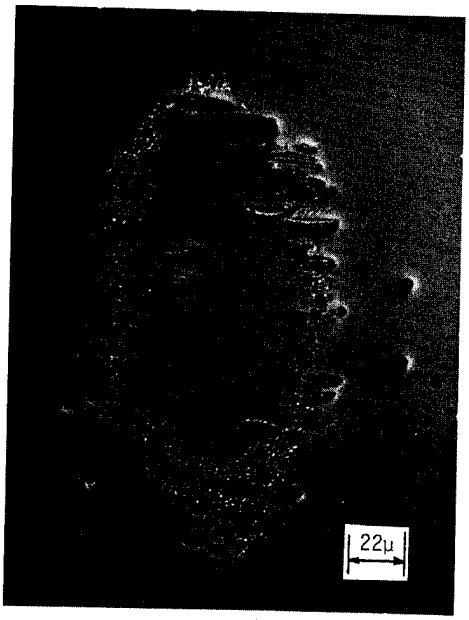


Figure 8b. For this bond, the position for the transition change in primary fault directions is not the same on each side of the bond. (Note the crater at the top end of the bond.)

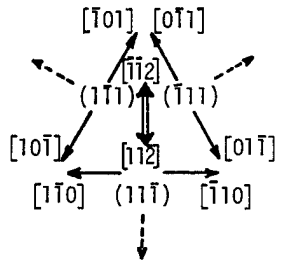


Figure 9a. For a (111) wafer, three line orientations are formed by the {111} stacking fault planes intersecting the crystal surface. The double line arrows show the pulsing directions used for (111) wafers.

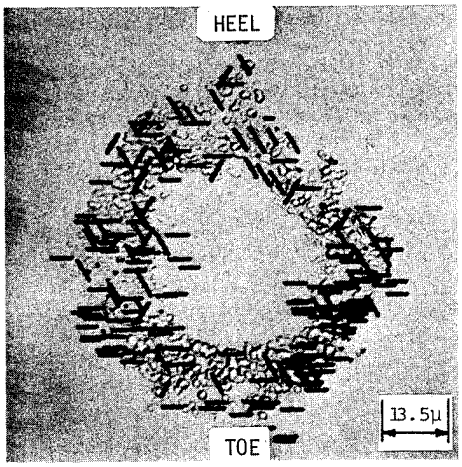
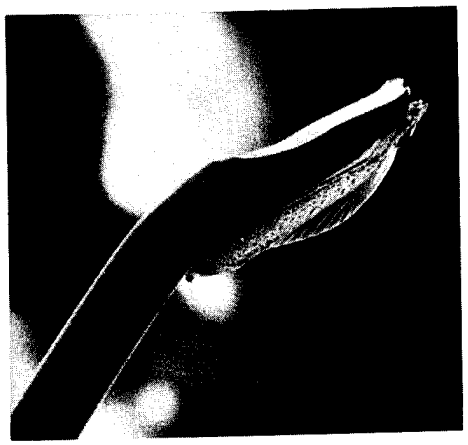
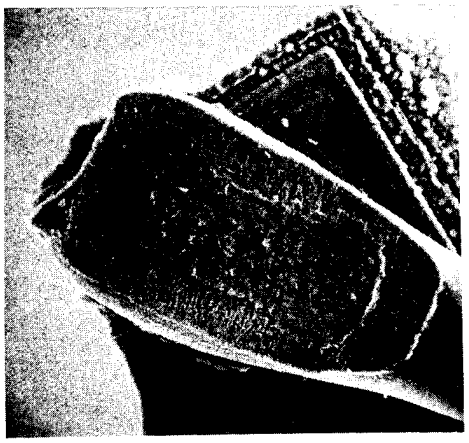


Figure 9b. The directions for this stacking fault pattern of a ribbon wire bond to a (111) silicon wafer are given in Figure 9a. Note that for a stress in one direction, two planes are operative (predominate feature on upper half of bond) and that for the reverse direction, only one plane is involved (lower half of bond).



(a)



(b)

Figure 10. The cratered wire bond (a) shows a reverse bend of the wire due to wedge adherency. Amounts of silicon fractured varies from being slight (Figure 8b) to extending outside the bond (b).

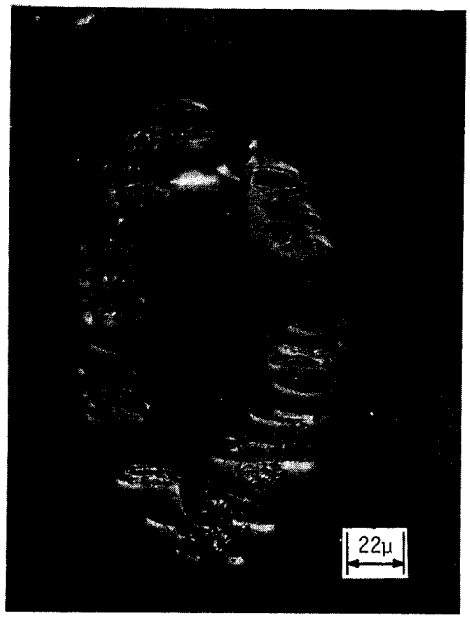


Figure 11. The stacking fault pattern for this cratered bond indicates the force system (large arrow) was not aligned with the bond axis. While the fault division (line) indicates a more severely angled force direction (small arrow), the lack of vertical faulting does not support this degree of misdirection.

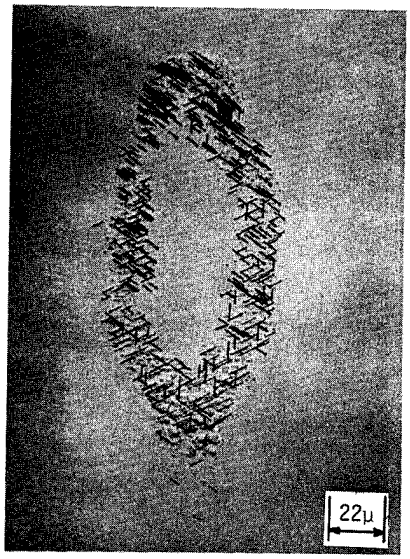


Figure 12. With a pulse in the $[\bar{1}01]$ direction for (111) silicon, the $(\bar{1}11)$ slip planes predominate, and for $[10\bar{1}]$, the $(11\bar{1})$ planes. (See Figure 9a).

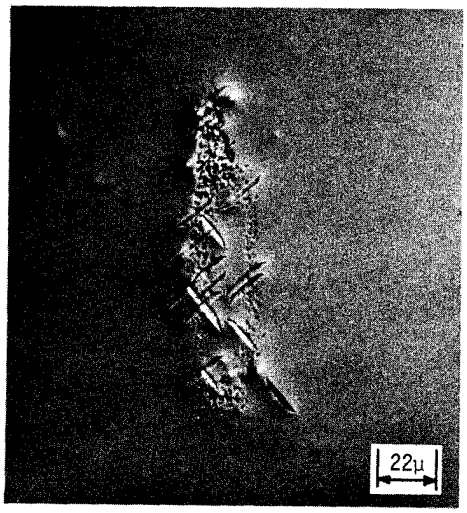


Figure 13. For this 1-mil bond pattern on (100) silicon the <100> bond orientation forces a condition of 2 possible faulting planes for each pulse direction.

ACCELERATED LIFE TESTING OF FLEXIBLE PRINTED CIRCUITS

Part I
Test Program and Typical Results

P. J. Boddy, R. H. Delaney, J. N. Lahti, E. F. Landry,
and R. C. Restrick

Part II
Failure Modes in Flexible Printed Circuits Coated With UV-Cured Resins

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Abstract

Part I of this paper describes a facility which has recently been developed to conduct accelerated life tests on printed wiring products. Procedures developed for the evaluation of flexible printed circuits are outlined, and a representative set of life test data is reviewed to illustrate the kinds of information obtainable with this facility. In conducting accelerated life tests on fineline flexible printed circuits coated with UV-cured resins, failures have been observed to occur in virtually every part of the circuit structure. In Part II, the various failure modes are described and are categorized according to the principal structural element involved (e.g., covercoat, substrate, etc.). In many cases environmental domains have been identified, within which there is a clear predominance of a specific failure mode.

Part I: Test Program and Typical Results

Introduction

Part I of this paper describes certain facilities and procedures recently developed to conduct accelerated life tests on printed circuitry. It includes a description of the environmental conditioning equipment; the ranges of temperature, humidity, and voltage employed; and a brief description of the automatic data acquisition facilities and data reduction procedures used.

A summary of results are also presented which illustrate how this facility is being applied to the study of the reliability potential of fineline flexible circuits. As presently manufactured, these are copper circuits with line widths and spaces in the 5 - 10 mil range. They are encapsulated, or covercoated, with a resin which is patterned and cured with ultraviolet light.[1] The data presented in Part I relate to one of a number of materials systems which have been considered for use in flexible printed circuit applications.[2] The covercoat is a photocuring polyblend (acrylate-thioether) designated here as Type-A resin; the substrate is the commonly used fire retardant form of G-10 epoxy-glass, FR-4. Figure 1 shows the forms of construction typical of this kind of circuit.

The objectives in this test series were to determine the forms of the time-to-failure and charge-to-failure distributions, and to establish the temperature-, relative humidity-, and voltage-dependence of the parameters of the latter distributions. An extrapolation of the data obtained to typical use conditions suggests this materials system is capable of providing median service life measured in tens of years.

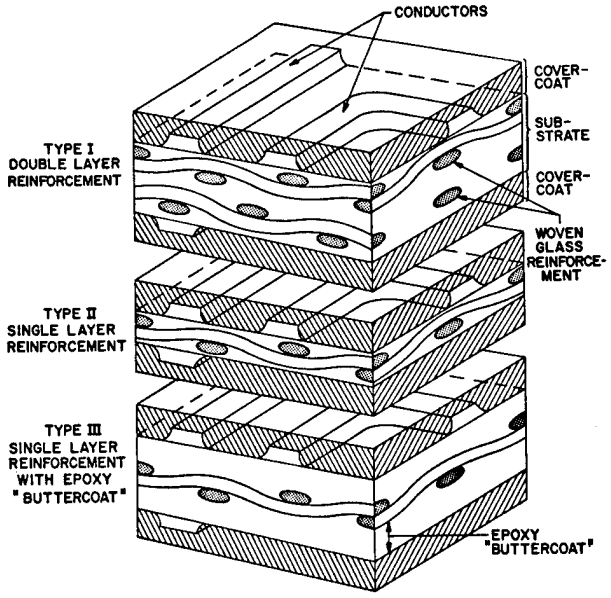

Figure 1

Typical Flexible Printed Wiring Constructions
Which Make Use of Woven Glass Reinforcement

Methods and Procedures

Test Conditions

The test environments are selected with the objective of gathering life data in the shortest time consistent with the need to preserve the dominance of the "real life" wearout modes: i.e., the wearout modes felt to dominate under use conditions. The procedure generally followed is to start at the most severe test conditions anticipated, to obtain a bench-mark, and then to test over a reasonably wide range of each environmental parameter, while holding the others fixed. Following this procedure, tests have been run from 35° to 95°C, from 25% to 95% RH, and with voltages ranging up to 400V.

Samples

The need to collect "statistically significant" amounts of data all but precludes the use of real circuits as test samples in most instances. As an alternative, fineline, double-sided orthogonal comb patterns are used. See Figure 2. These comb patterns are made using standard fineline PC technology (.008" lines, .009" spaces). They can be processed using the same materials and processes as would be used in the manufacture of the appropriate printed circuit. The

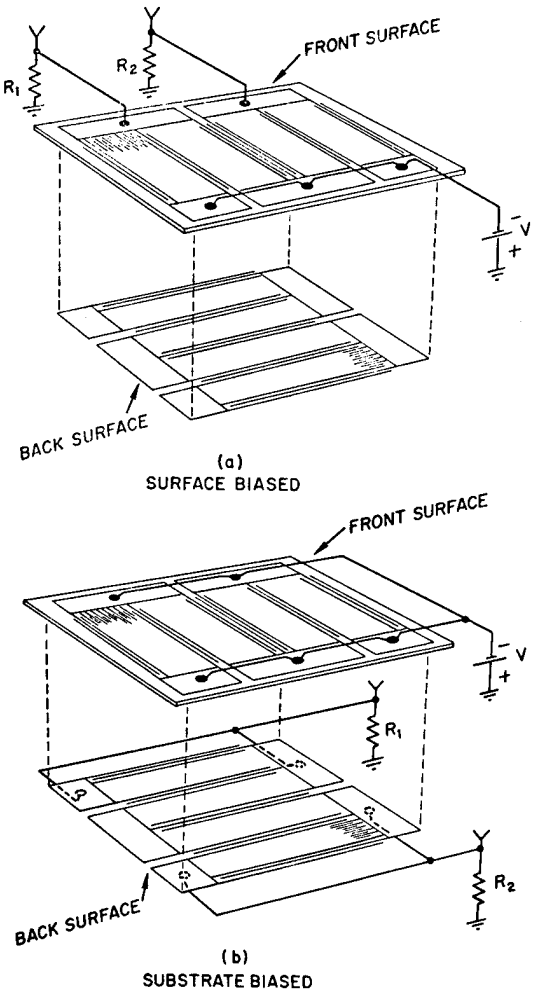

Figure 2

Fine Line Comb Electrical Configurations

only significant difference is the absence of plated-through-holes.*

A sample size of twenty is commonly used. This seems to be a reasonable compromise between the need for large samples to tighten confidence limits on the sample statistics, and the desire to keep the sample size small to minimize sample preparation and data collection/processing effort. Such a sample requires 2 - 3 man-days of effort to prepare for testing, a level which has been found to be feasible.

Prior to environmental testing, the covercoated comb patterns may undergo a sequence of operations to simulate the assembly process: they are fluxed, passed through a wave soldering machine, and cleaned in vapor degreasing equipment. This sequence simulates very closely that which is commonly used in the fabrication of printed circuit assemblies. The samples are then examined microscopically for flaws and the results of the inspections are recorded. Next the combs are mounted on test fixtures and wires are attached for electrical bias and monitoring. The electrical configurations used are shown in Figure 2.

* To the authors' knowledge no through-hole related failures have been observed in flexible circuits.

Test Facilities

The test environments are obtained by the use of precision-controlled, forced-convection ovens* and closed inner containers which hold saturated salt solutions. The fixtures on which the combs are mounted are made of epoxy-glass, stainless steel, and Teflon. The combs are held in place by nylon screws and porcelain standoffs. The cables which carry the standing voltage into the containers and provide return (sense) lines are laced bundles of Teflon insulated wires. A view of the closed container assembly is shown in Figure 3.

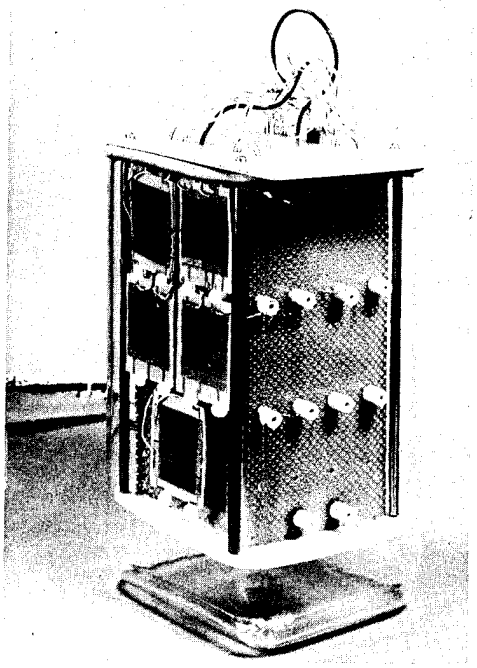

Figure 3

Closed Container and Mounting Fixture

In operation, the combs are fastened on the faces of the mounting fixture and the bias and sense leads are soldered into place. A thick ring of stopcock grease is placed around the inner wall of the container about 2" above the bottom. A portion of an appropriate salt is then placed in the bottom of the container and distilled water is added to form a saturated solution at the test temperature. The mounting fixture is lowered into place, and the top fastened. The closed container is then placed in the oven and the cable fed out through a small port. The oven is then closed and brought up to temperature. Bias is then applied to begin the test.

Data Acquisition and Processing

A special purpose data acquisition system was designed and constructed which consists of three basic elements: 1) test point scanner/controller, 2) master controller/signal processor, 3) data recorder. In operation, the leakage currents are monitored by sensing the voltage at the test points on each comb pattern. See Figure 2. The test points selected by the controller are sequentially accessed by the scanner

* A number of small natural-convection ovens are also available and have been used in some of these tests.

(a 1475:1 switching matrix, built of rotary stepping switches and relays). The test point voltage is fed through the scanner to the signal processor which performs a logarithmic transformation before digitizing and encoding; this transformation results in a four decade dynamic range on any given range setting. The digitized voltages are then read out and recorded on a digital magnetic cassette recorder. The system is capable of unattended operation, and data can be collected at programmed intervals.

During the initial phases of most tests, and throughout some of the short-term experiments, data is collected at 2-hour intervals. As testing progresses, however, the data collection interval is generally increased to 4, 6, and ultimately, to 24 hours.

As data accumulates, the cassettes are periodically read into a central computer facility for long term storage and processing. Using the measurement parameters, insulation resistance values are calculated from the raw data and stored. At the termination of a test, and on occasion as testing is in progress, the insulation resistance trajectories are plotted using a batch program, which produces graphs by means of a computer-graphics system. Having curves of insulation resistance vs. time readily allows identification of failure times. At present, this is done manually, as is construction of the sample distributions of time-to-failure (t_F). From the latter distributions, the sample statistics (median t_F, standard deviation) are easily found.

A program has also been written to calculate cumulative charge transfer as a function of time. At the time the insulation resistance plots are generated, this program is run to compute a set of charge transfer curves, from which the charge-to-failure information can easily be obtained. The latter data are then used to manually construct charge-to-failure distributions and obtain the corresponding sample statistics.

Typical Test Results

As noted earlier, the data presented in this part were obtained on one of a number of materials systems which have been tested. Again, the substrate is conventional FR-4 epoxy-glass, nominally 5 mils thick; the covercoat is a photocured resin, designated here as Type-A.

Failure Modes

Two failure modes have been observed in the Type-A/FR-4 system which seem intrinsic to this combination. Both involve a catastrophic loss of insulation resistance due to the formation of conductive bridges between conductors. One mode results in shorts which form through the substrate. Failures of this type are difficult to localize; it is conjectured that they form when (conductive) corrosion products fill voids and fissures which occur at the interfaces between the substrate epoxy and fibers of the woven glass reinforcement. This mode predominates at high temperature and humidity, but does not prevail below 75°C and 80% RH. Since it appears to be of no consequence at use conditions, failure data from this mode will not be included here. The second intrinsic mode is similar to the first, but involves shorts which form between conductors on the same side of the substrate. Here the fault sites are readily identified and clearly involve the accumulation of conductive material in the fissures or capillary spaces which form along the glass bundles when the bonds between the glass fibers in these bundles and the surrounding epoxy break. Figure 4 shows a typical site where this has occurred. The latter failure mechanism has been observed at all test conditions; it is the dominant failure mode observed in these tests below 75°C and 80% RH. This dominance is assumed to extend to typical use conditions; e.g., 25°C - 35°C, 40% - 60% RH.

Figure 4

Sub-Surface Short

A third mode has been observed in this system. It produces early failures and arises when the substrate becomes contaminated with ionic material prior to the application of covercoat. Failure again results from the formation of shorts, only now by the growth of copper dendrites at the covercoat/substrate interface. See Figure 5. Since the samples used in this test series were carefully cleaned prior to coating, premature failure by this mechanism did not occur.

Time-to-Failure

A set of surface insulation resistance curves for a typical experiment is shown in Figure 6. These data were obtained at 85°C/80% RH/78V. Failure is usually manifested by an abrupt drop in insulation resistance. For the most part, therefore, the time-to-failure is rather unequivocal. There are some cases, though, in which the insulation resistance decays erratically before dropping to very low values. In such instances, t_F is taken to be the time at which the trajectory in question deviates from the insulation resistance envelope defined by the main sample population. This "envelope breakout" criterion is conservative in that it underestimates t_F; breakout invariably signals imminent failure, however, and suggests that the

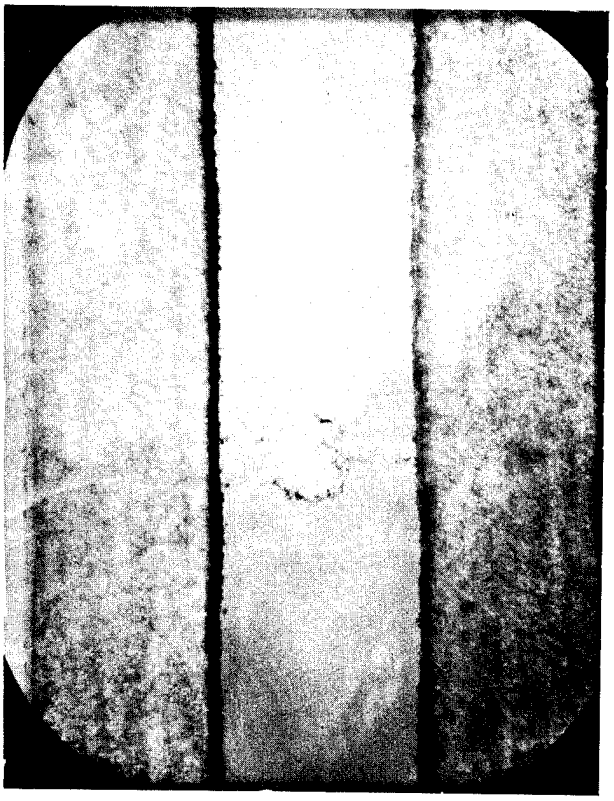

Figure 5

Interfacial Dendrite

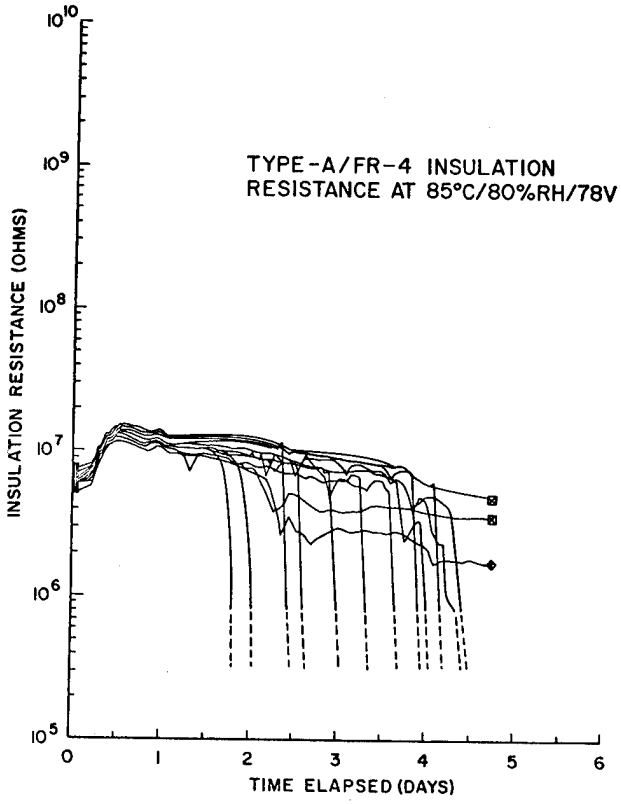

Figure 6

phenomenon which produces failure has reached an advanced state.

As described earlier, values of t_F are determined from the individual insulation resistance plots. Sample distributions are then formed and the corresponding median t_F's and standard deviations are identified. The sample distribution of t_F corresponding to the insulation resistance trajectories shown in Figure 6 is presented in Figure 7. Note that the data are plotted on log-normal paper (a log-normal distribution appears as a straight line) and that this distribution seems to represent the data reasonably well. The indicated fit is typical of most tests run in this series, at least in terms of the central portions of the t_F-distributions. In a number of cases, however, the tails deviate noticeably from log-normal behavior. The median values of t_F (denoted by t_{FM}) are read directly off the sample distributions as the time to reach the 50th percentile; likewise the standard deviations are read off as the differences in log t_F between the 16th and 50th percentiles. Note that these statistics are obtained from the "best" log-normal fit to the data.

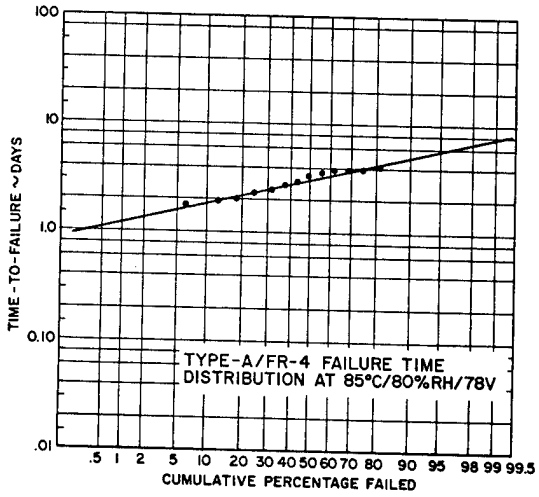

Figure 7

Figure 8 shows the median failure times and standard deviations plotted against the reciprocal of absolute temperature (but labeled in °C for convenience) for nominal humidities ranging from 40 to 80% RH. Since the median-t_F data are plotted on a semi-log scale, the straight line relationships shown correspond to Arrhenius functions. The 80% RH data indicate a breakpoint at 75°C; hence the data have been fit by two-segment Arrhenius curves. The activation energies for surface failures are .41 eV above, and 1.41 eV below the breakpoint, respectively.

Similar Arrhenius curves are shown which pass through the data points at 85°C and at lower humidities. The use of the latter curves is supported by an experiment which is still running at 50°C/60% RH: Although failures have not yet been encountered, it is obvious that the data will reach or exceed the level predicted by the simple Arrhenius relation.

An examination of the median failure time data at 85°C reveals that the humidity-dependence can be

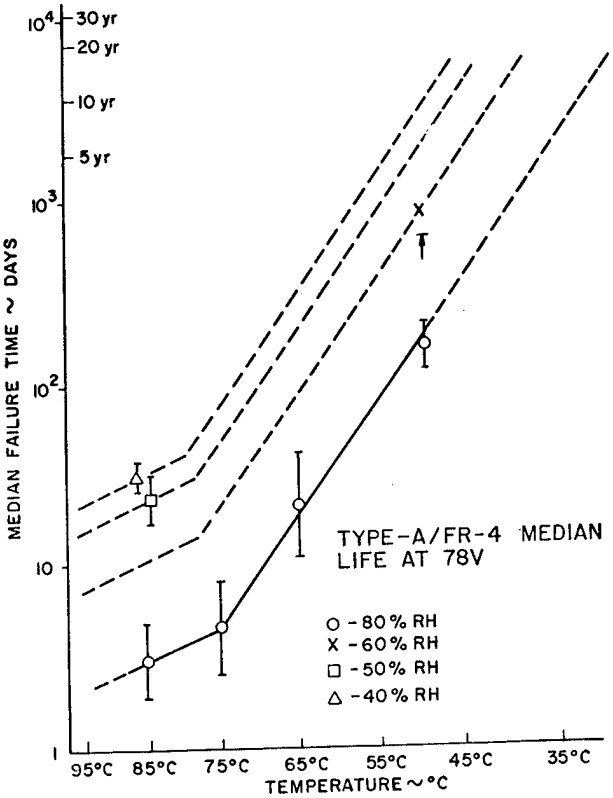

Figure 8

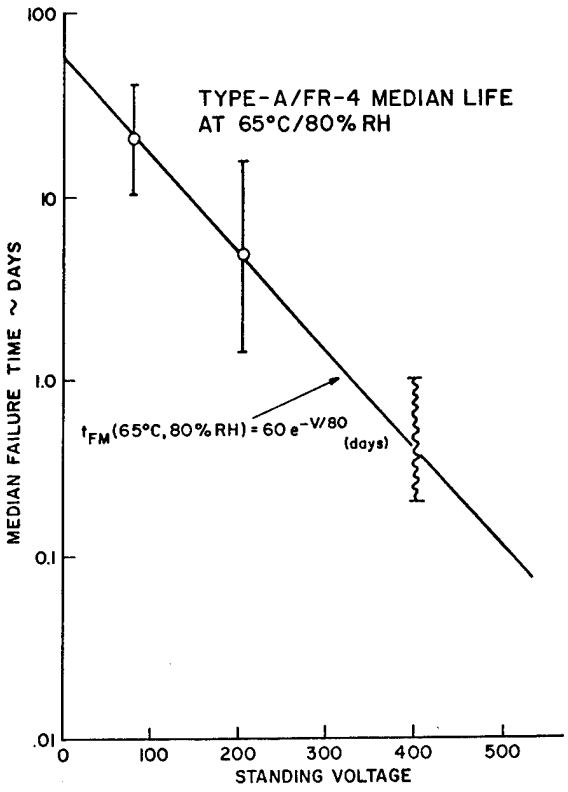

Figure 9

reasonably represented by

$$t_{FM}(85°C,78V) = 600e^{-.068\,RH} \text{ (days)}. \qquad (1)$$

In addition, the data in Figure 8 do not reveal any significant variation in σ_{t_F} with temperature, and at best, only a mild dependence on humidity.

Figure 9 shows the variation in failure statistics with voltage at 65°C/80% RH. Again the data can be represented quite well by an exponential function of the form

$$t_{FM}(65°C,80\%\ RH) = 60e^{-V/80} \text{ (days)}. \qquad (2)$$

Unfortunately, experimental difficulties precluded accurately defining t_{FM} at 400V, or establishing the corresponding σ_{t_F}; all failures occurred between 0.2 and 1.0 days as indicated by the bars and wavy line. The 78V and 200V data do not reveal a strong voltage dependence on the part of σ_{t_F} at 65°C/80% RH.

The t_{FM} data for the Type-A/FR-4 system suggest that for operating voltages below 100V, median lives in typical air-conditioned equipment space (25° - 35°C, 40% - 60% RH) will be conservatively measured in tens of years.

Charge-to-Failure

Figures 10, 11, and 12 show the charge-to-failure (Q_F) statistics corresponding to the previously discussed t_F data. The means by which the Q_F data were

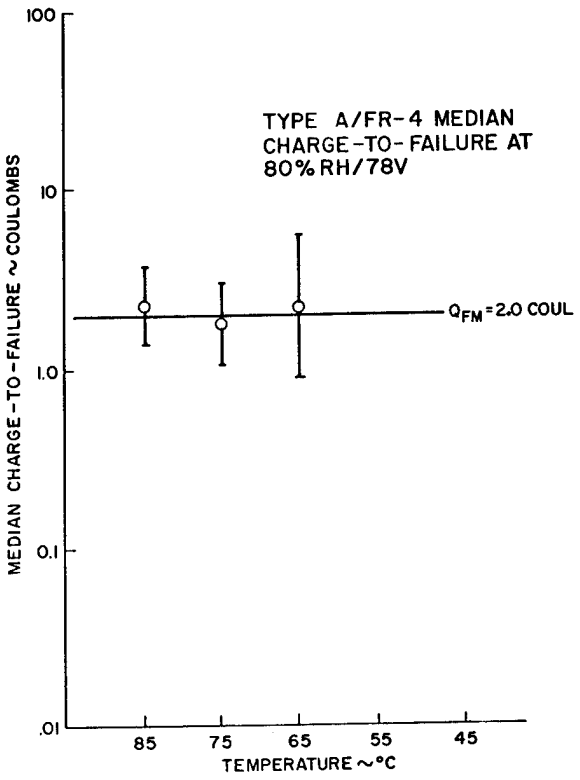

Figure 10

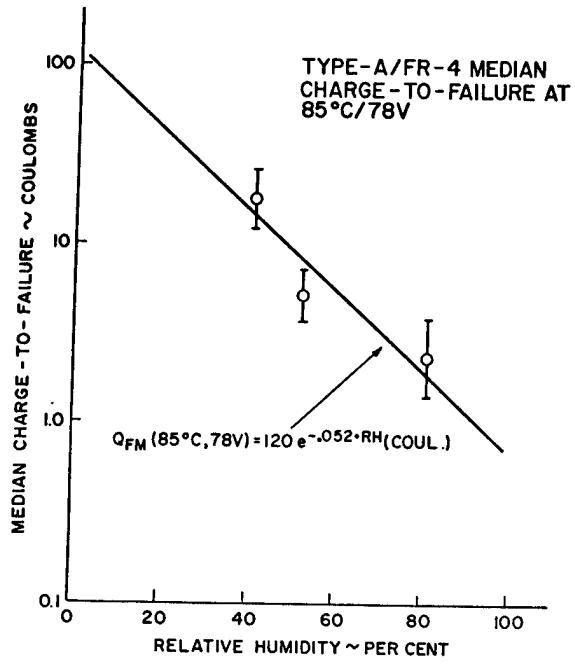

Figure 11

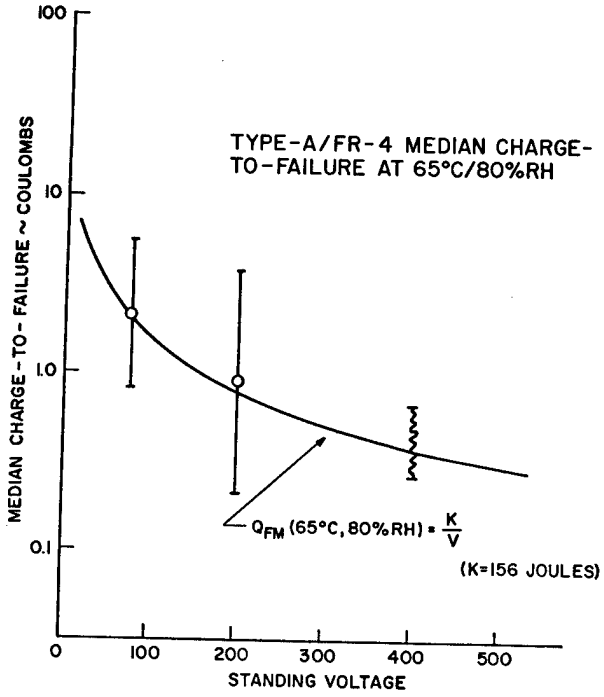

Figure 12

obtained was indicated earlier. Note that the charge-to-failure was also assumed to be log-normally distributed, and it was found that the fit was about as good as with the t_F data.

Figure 10 shows the temperature-dependence of the charge transfer statistics at 80% RH/78V. The relative constancy of the median Q_F is striking. The data show a tendency for σ_{Q_F} to increase as the temperature is reduced.

Figure 11 shows the humidity-dependence of the charge-to-failure statistics. The median Q_F data is shown fitted by a negative exponential,

$$Q_{FM}(85°C,78V) = 120e^{-.052\,RH} \text{ (coulombs)}. \qquad (3)$$

There is no indication of a significant RH-dependence in σ_{Q_F} at 85°C/78V.

Figure 12 presents the voltage-dependence of the charge-to-failure statistics at 65°C/80% RH. The limits connected by the wavy line at 400V are best estimates of the actual data which was lost as noted earlier. The data are shown fit by a function of the form

$$Q_{FM}(65°C,80\%\ RH) = KV^{-1} \text{ (coulombs)} \qquad (4)$$

where K = 156 Joules. There is no indication that σ_{Q_F} is strongly dependent on V at 65°C/80% RH.

The time- and charge-to-failure data presented correspond to the fineline comb pattern described earlier. The length of parallel conductors involved is 1.57m (62 in): hence normalized charge-to-failure levels are roughly in the 1 - 10 coulomb/meter range (except at the high voltage extreme). This level of charge transfer has been found to be characteristic of a number of materials systems examined to date. Hence, if an IR level can be determined for a given set of operating conditions, a rough indication of t_{FM} can be obtained by calculating the time to transfer a charge of one coulomb/meter.

Summary and Conclusions

Following a brief description of the hardware which has been assembled to provide test environments for accelerated life testing of printed circuits, the philosophy of test parameter selection was described and it was noted that tests have been run from 35° to 95°C, from 25% to 95% RH, and at standing voltages ranging up to 400V. The need for a small but representative test piece was mentioned, and a fineline comb pattern was described which fills this need adequately for flexible printed circuits. Typical sample preparation procedures were also outlined. The basic elements of the special-purpose data acquisition hardware were identified and the data collection, storage, and display procedures were described. It was noted that, at present, the time- and charge-to-failure statistics are manually extracted from the computer-generated plots of insulation resistance and charge transfer.

A set of data was presented which was collected on the Type-A/FR-4 materials system. It was noted that the distributions of both time- and charge-to-failure data can be modeled reasonably well by log-normal distribution functions. The temperature, humidity, and voltage dependences of the median and standard deviation were shown for both time- and charge-to-failure. The median failure time data were fit by simple Arrhenius curves, and an extrapolation of the latter to typical use conditions (25°C - 35°C, 40% - 60% RH) indicated the Type-A/FR-4 system can provide median life measured in tens of years for operating voltages below 100V. It was observed that

the median charge-to-failure for this system is relatively insensitive to environmental conditions, and that the one coulomb/meter order-of-magnitude number found here is quite consistent with results obtained on a number of other materials systems. It was noted that this observation provides a rough means for estimating the median life to be expected under various operating conditions.

As the latter data indicate, the printed circuit accelerated life test facility (hardware/software/procedures) has been established as an extremely valuable entity in the study of printed circuit reliability. The flexibility and high throughput of this facility are felt to be unique.

Acknowledgments

The authors gratefully acknowledge the efforts of G. B. Fefferman, T. V. Lake, and M. J. Sharp in the preparation of samples; and those of F. A. Scaglione and J. G. Tetz in conducting the accelerated life tests.

Part II: Failure Modes in Flexible Printed Circuits Coated With UV-Cured Resins

Introduction

Part II of this paper describes the various means by which electrical failures have been observed to occur in the accelerated life testing of fineline flexible printed circuits. The results presented here relate to copper circuits fabricated on FR-4 epoxy-glass substrates which range in thickness from 5 to 7 mils. The finished circuits were coated with resins[1,2] which were patterned and cured with ultraviolet light.* Figure 1 again shows the general construction of this type of circuit, and Table 1 identifies the coating resins examined in this study.

RESIN TYPE	CHEMICAL CLASS	FIRE RETARDANCY ACHIEVED BY
A	ACRYLATE-THIOETHER POLYBLEND	NON-REACTIVE ADDITIVE
B	THIOETHER	SOME INHERENT, PLUS REACTIVE ADDITIVE
C	THIOETHER	SOME INHERENT, PLUS NON-REACTIVE ADDITIVE

Table 1

Identification of UV-Curable Coating Resins[2]

The data presently available indicate that of the possible modes of electrical failure, failure due to aging is most likely to occur as a result of a loss of electrical isolation between conductors. Furthermore, while a slow, general degradation of the insulation is often observed, failure has almost invariably occurred by an abrupt, catastrophic loss of isolation in localized regions. This happens long before the gradual degradation would result in failure.

Of the various failure modes observed in accelerated life testing, some would appear to dominate at use conditions, while others occur only in the most severe test environments. In what follows, the various modes will be grouped according to the principal structural component involved (e.g., substrate, overcoat, interface, etc.), and where they have been identified, the domains of dominance will be described.

Substrate-Related Failures

Through-Substrate Shorts

Failures have been observed to result from shorts which form through the thin (5 - 10 mil) epoxy-glass substrates used in flexible circuits. The detailed mechanism is not understood in this case. It is often difficult to locate fault sites of this type, since they occur beneath the conductors, and it is also quite difficult to examine such a site once it has been found. It is presently believed that small fissures form in the substrate epoxy which act as capillary spaces and tend to collect conductive residues (an active source of the latter would of course be a conductor corroding under bias in the presence of moisture). The presence of these residues might serve to advance fissure growth,* and the tendency for the substrate epoxy to separate locally from the glass reinforcement might also contribute to the formation of conducting paths which span conductors on opposite sides of the substrate. See Figure 13.

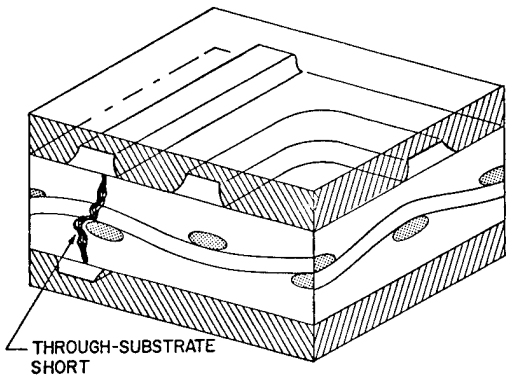

Figure 13

An Illustration of the Type of Path Thought to be Followed by Through-Substrate Shorts

If the local separation of the epoxy and glass reinforcement were a significant factor, then one would expect substrates which permit the glass fibers to contact (or nearly contact) the undersides of the conductors to be more susceptible to this failure mode than those which provide a thick "buttercoat" of epoxy.† The available data support this view; however this assertion must be qualified since the substrates examined with and without buttercoats utilized different epoxy systems, and differed by about 50% in overall thickness, favoring the buttercoated material.

In any case, this failure mode has been observed to dominate only at the extremes of high temperature and high humidity used in accelerated life testing:

---

* It should not be inferred that the failure modes described in this paper are necessarily unique to circuits encapsulated with such resins.

* A similar phenomenon has been suggested to underly the degradation of polyethylene cable insulation.[3]

† The buttercoat, as shown in Figure 1, is a layer of epoxy applied over the glass-reinforced core of the substrate.

e.g., in the system containing little or no buttercoat, through-the-substrate failures dominate only at 80% RH and at temperatures above 75°C, conditions well beyond typical use environments for flexible printed circuits.

Sub-Surface Shorts

A second substrate-related failure mode has been observed in circuits fabricated on substrates with little or no buttercoat. Here shorts from between lines on the same side of the substrate. In this case the mechanism has been identified: conductive material fills voids which form around glass fibers, and bundles of fibers, which pass near the underside of conductors. These voids or separations propagate along the fiber bundles. It could again be conjectured that as the conductive material begins to enter the void, void growth is further stimulated. In any event, when the void and the material contained therein span adjacent conductors, shorting takes place. Figure 14 illustrates a typical fault of this kind; Figure 4 is a photograph of a case in which voids have formed around two adjacent glass bundles. Note that, as in the case of the through-substrate failure, a thick buttercoat will inhibit this mechanism.

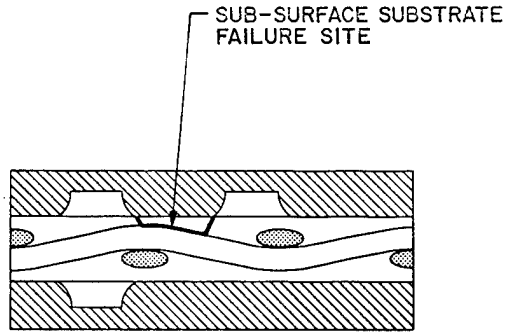

Figure 14

An Illustration of a Typical Path Taken by a Sub-Surface Substrate Short

The rate at which this mechanism progresses can be affected by the presence of a covercoat,* and the rate is greatly increased by elevating either temperature or humidity. Data quantifying the latter statement for the Type-A/FR-4 system are contained in Part I of this paper. The Type-A resin does in fact accelerate the formation of sub-surface substrate shorts. This acceleration presumably results from covercoat hydrolysis, the products of which serve to attack and solubilize copper at the surfaces of the positively biased electrodes (anodes).

Covercoat-Related Failures

Dendritic growth in the bulk of the covercoat material has been observed to produce failure. Here, too, covercoat hydrolysis is suspected to be the prime source of those species which result in metal migration. Copper ions move from the anode (positive conductor) to the cathode (negative conductor), where they deposit electrolytically to form a dendrite which grows from cathode to anode. Where it has been examined carefully, the direction of dendritic growth follows what one would expect to be the electric field pattern (streamlines).

The Type-B resin was found to be hydrolytically unstable and resulted in a very rapid and profuse dendritic growth in the covercoat bulk. Some typical results obtained with this coating material at 50°C/80% RH are shown in Figure 15. The instability in this system was traced to the reactive fire retardant. Failure, of course, occurs when the dendrites grow to the point at which they bridge conductors to form a short circuit.

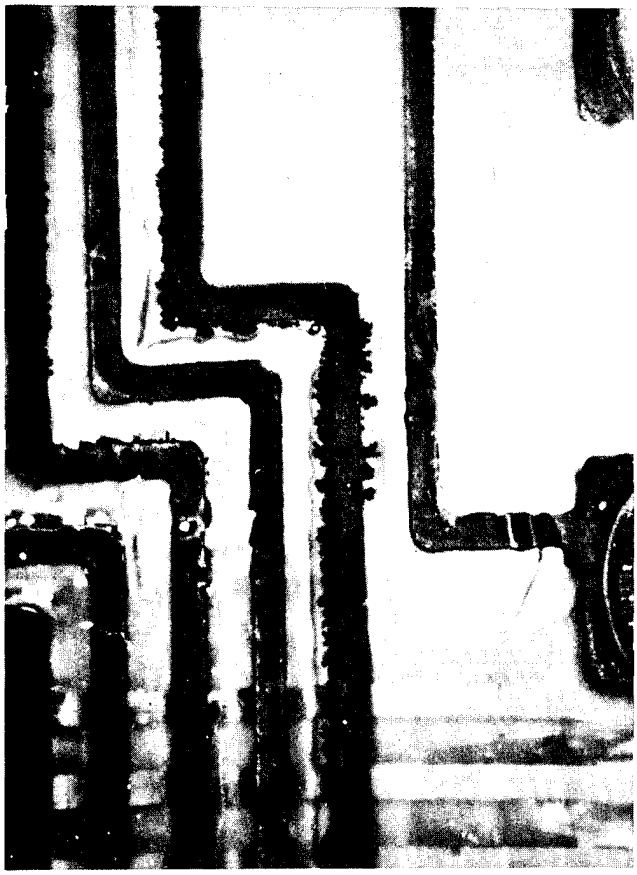

Figure 15

Dendritic Growth in Covercoat

In the Type-A resin system, dendritic growth also occurs in the covercoat, but at a much slower rate than with the above material. While failures would eventually result from dendrite shorting, the Type-A/FR-4 system tested* appears to be dominated by the sub-surface substrate failure mode described above for $T \leq 75°C$, $RH \leq 80\%$.

A third covercoat material which is superior to the others evaluated to date also shows dendritic activity in the bulk of the coating. This is the Type-C resin system. Here the bulk resistivity of the covercoat is relatively high, and there is often a tendency for the dendrites to grow from the cathode towards the coating surface, then across the surface and down through the coating again to the anode. See Figure 16. Cross sections of circuits containing dendritic growths have revealed concentrations of growth in areas of high field strength (also shown in

* Although there is relatively little data at present, the existing evidence indicates that through-substrate failures are also affected by the coating material.

* The FR-4 substrate used in this case had little or no buttercoat. In a system which employs a thicker buttercoat, failure by dendritic growth in the covercoat might well become the dominant mode.

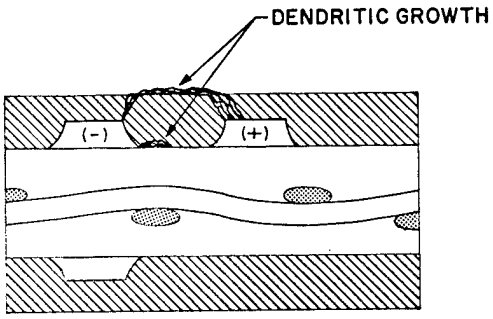

Figure 16

Typical Dendritic Growth Pattern Observed in the Type-C/FR-4/Materials System

Figure 16) and have also revealed a condition of covercoat embrittlement in the area immediately surrounding the anodes. In systems which use the Type-C resin over some form of FR-4 substrate, it is expected that dendritic growth in the covercoat will be the predominant failure mechanism at typical use conditions.

A fundamentally different covercoat failure mechanism has also been observed with the Type-C resin and one particular type of FR-4 substrate. It involves a highly localized anodic reaction which produces an eruption at the covercoat surface. See Figure 17. Frequently a plume-like structure is observed which extends from the edge of the anode conductor up to the covercoat surface, terminating beneath the eruption.

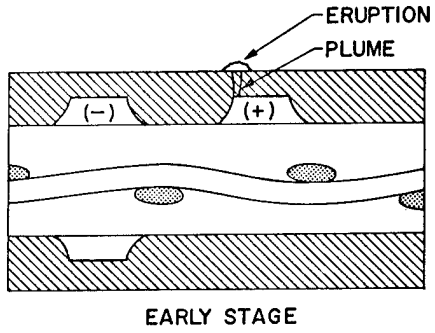

Figure 17

An Illustration of the Anodic Eruption Failure Mode Observed in the Type-C/FR-4 System at High Humidity Conditions (95% RH)

It often appears that the erupted material has been transported up through the plume. The surface eruption acts as a focus for leakage current and results in a rapid, localized degradation of the surface of the covercoat immediately surrounding the eruption. This degradation is manifested by a charring of the coating. Failure results as the charring spreads and proceeds into the bulk of the coating, finally reaching the cathode and causing a short circuit. The details of the mechanism by which the anodic eruptions occur are not understood. Nonetheless, it is fairly clear that this mode is not germane at typical use conditions. It has only been observed at 95% RH, and has not been observed at or below 80% RH. At 95% RH, this mechanism has been observed to occur with particular intensity at 75°C.

Interface-Related Failures

Failures which have been observed to result from covercoat/substrate interface effects have invariably occurred prematurely (i.e., they have fallen in the infant mortality category). The interface failures observed to date have resulted from dendritic growth or blistering (delamination) at the interface. See Figure 18. The latter may or may not also involve dendritic activity (which would be concealed by the delamination). Furthermore, interface failures have been seen to follow from the entrapment of contaminants at the covercoat/substrate interface. Such contamination can result from faulty processing and/or handling prior to covercoat application. It has been

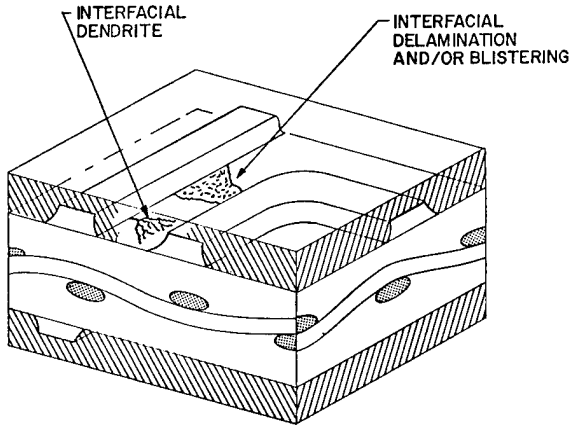

Figure 18

An Illustration of the Two Types of Interface Failures Observed to Result from Entrapped Contamination

found that a level of contamination exceeding the equivalent of 10^{-6} to 10^{-5} gm/cm^2 of NaCl are required to affect circuit life,* and that once above the 10^{-5} gm/cm^2 level, the effects become significant, resulting in the kinds of interface failures described above.

Summary and Conclusions

This paper has provided a brief review of the various failure modes that have been observed in the accelerated life testing of flexible printed circuits.

It was noted that two types of substrate failure have been encountered. In some materials systems, shorting between conductors on the same side of the substrate due to conducting paths which form in the substrate is likely to be the prevalent failure mode

* Based on work by Wargotz and Wargotz and Delaney which is to be published.

at use conditions. While through-substrate shorts have been observed at high temperatures and humidities, they quickly cease to dominate as milder conditions are approached and it is felt that this mode will seldom be seen at use conditions.

Failure by dendritic growth in the covercoat can occur in any of the UV-cured coating resins examined to date. In some cases, this mechanism is expected to dominate at use conditions. A very aggressive anodic failure mechanism has been encountered, but it has been observed only at conditions far removed from any reasonable use environment.

It was also observed that one clear cause of infant mortality in flexible printed circuits is contamination entrapped at the covercoat/substrate interface. Such contamination results in failure by dendritic growth and/or severe blistering and delamination at the interface. Failure by this mechanism should not occur in properly manufactured circuits.

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MEASUREMENT OF THERMO-MECHANICAL STRAINS IN PLATED-THROUGH-HOLES

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Abstract

Knowledge of thermo-mechanical strains in plated-through holes, complemented by an understanding of failure mechanics, yields valuable information about the effect of materials, design and process parameters on product reliability potential. A technique is described for measuring central barrel strain and surface land rotation for plated-through-holes during thermal transients.

Introduction

During thermal excursions, plated-through-holes (PTHs) in multilayer boards (MLBs) undergo thermo-mechanical deformation which may lead to mechanical failures. Knowledge of these deformations as a function of temperature, coupled with an understanding of failure mechanics, greatly aids one in determining the influence of design, process and materials parameters on product quality and to assess the reliability potential of multilayer printed wiring boards.

Failure Mode Specific Testing

The concept of failure mode specific testing, by which is meant the preferential excitation of selected failure modes by proper choice of thermal stress stimuli, springs naturally from these measurements and the associated model of PTH failure mechanics discussed by Oien.[1] When coupled with failure mode specific instrumentation[3,4] and fluidized bath thermal cycling,[5] substantial improvements in reliability test resolution are obtained with concomitant reductions in testing time.[2]

Measurement of Displacement

This paper describes an experimental technique for measuring central barrel strain and surface land rotation of a PTH undergoing a thermal excursion. A modified, commercially available, thermo-mechanical analyzer (TMA) is used in conjunction with specially designed interface extensometers and fixturing. The modified TMA (Perkin Elmer model TMS-1), which is thermally and seismically isolated from the environment, can repeatably resolve displacements of less than 1 micro-inch. Figure 1 shows a simplified block diagram of the TMA and associated X-Y recorder. The heating rate of the specimen oven may be preselected from an available range of 0.31 to 320°C/min. The typical rate used is 10°C/min. For convenience the specimen temperature is inferred from a masked thermocouple with closely matched thermal response characteristics which is mounted near the test specimen in the oven. Tests show that the temperature correlation between sample and masked thermocouple is quite good with a temperature lag of about 3°C. It should be noted that the temperature lag only affects the shape of the displacement versus temperature curves during the start and stop transients. This is adequate for most engineering purposes. The thermocouple temperature is recorded on the horizontal axis of the X-Y recorder. The linear voltage differential transformer (LVDT) displacement sensor is mechanically coupled to

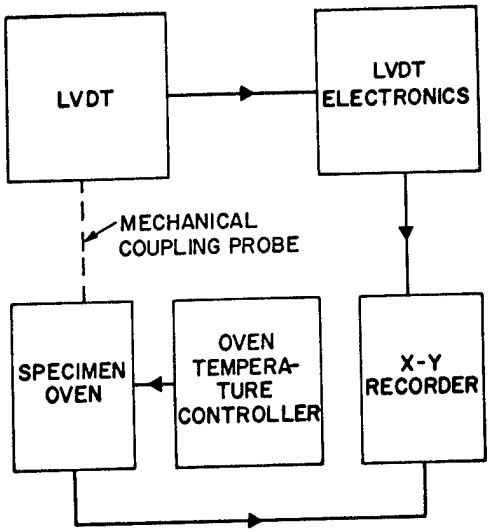

Figure 1

Simplified TMA Block Diagram

the PTH mounted extensometers which will be described later. The LVDT output is recorded on the vertical axis of the X-Y recorder. The resulting displacement vs. temperature signature characterizes the thermo-mechanical behavior of the PTH through the extensometer transfer function.

The following different thermo-mechanical responses are readily measured with the TMA extensometer system:

1. Transverse free-field dielectric expansion,
2. PTH barrel strain,
3. PTH surface land rotation.

A description of the associated procedures follows.

Normal Free-Field Dielectric Expansion

To measure normal free-field dielectric expansion, a 3/8 inch square sample is mounted in the TMA as shown schematically in Figure 2. The differential expansion of the quartz TMA fixturing is negligible compared to the expansion of the test specimen. A typical transverse displacement vs. temperature curve for a MLB sample is shown in Figure 3. The thermal response is bi-linear with a "break-point" at the epoxy-resin glass transition temperature. This behavior is characteristic of the epoxy-glass dielectrics used in printed circuit technology. The slope of the curve in Figure 3 corresponds to the effective thermal expansion coefficient of the sample. Typical coefficients are about 75×10^{-6}/°C below glass transition and 400×10^{-6}/°C above glass transition. These values of thermal expansion coefficient are high compared to the thermal expansion coefficient of copper, which is 17×10^{-6}/°C. The constrained differential thermal expansion between the

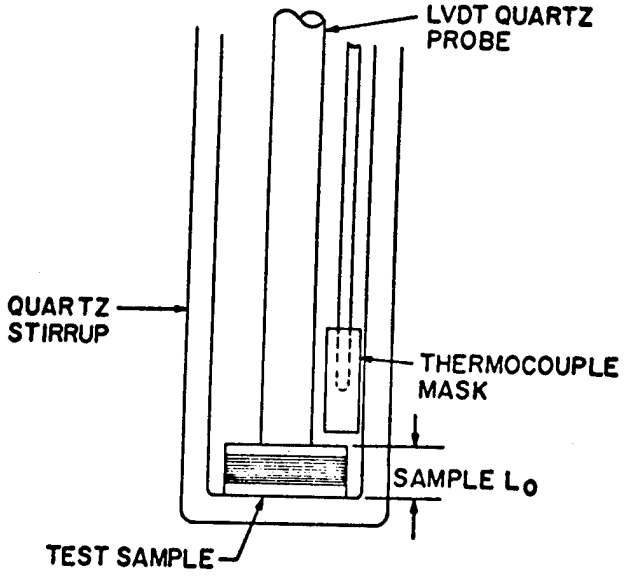

Figure 2

Specimen Mounting for Normal Free-Field Dielectric Expansion Measurement

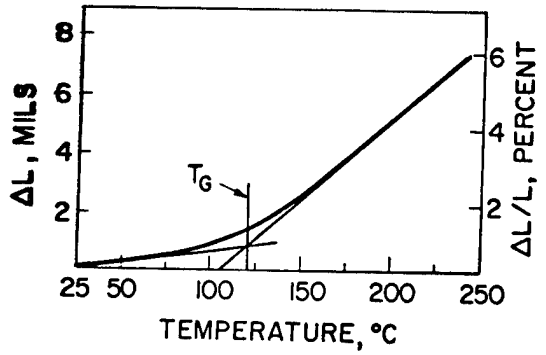

Figure 3

Typical Normal Dielectric (Epoxy-Glass) Free-Field Expansion

copper barrel and dielectric is the source of thermo-mechanical PTH failure.

Barrel Strain Measurement

The unit axial elongation or strain, ε, impressed on a PTH barrel by the differential thermal expansion of the epoxy-glass and copper is of interest in assessing the severity of various thermal stimuli for reliability projection. One dimensional strain, ε, is defined as the change in length, ΔL, of some arbitrary dimension or gage length, L. Thus

$$\varepsilon = \frac{\Delta L}{L} . \qquad (1)$$

Typical gage lengths in standard tensile tests range from 0.5 to 10 inches. Because of the small size of the PTHs, gage lengths employed here are much smaller.

The barrel strain is inferred from the relative displacements of the centrally mounted extensometer as shown in Figure 4. The extensometer consists of two

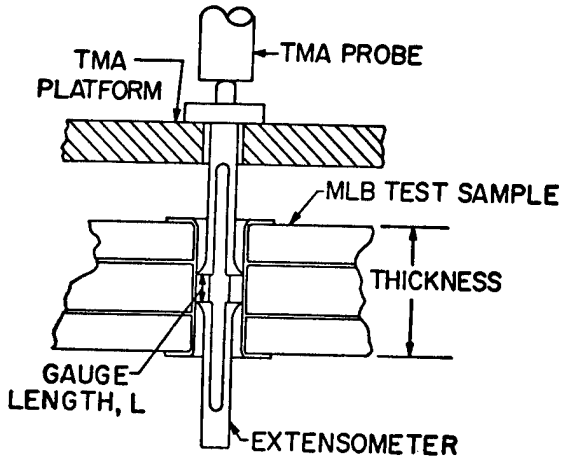

Figure 4

Extensometer Arrangement for Barrel Strain Measurement

miniature, three-pronged grippers which are mounted in the central region of the barrel where maximum strains normally occur. The grippers are held in place by their cantilever spring tension. Differential motion between the grippers is transmitted to the TMA sensor probe via the central rod which is attached at one end to the bottom of the lower gripper. A typical extensometer gage length is about 20 mils. Actual gage lengths are selected to minimize the effect of placement errors relative to the internal PTH lands. Figure 5 shows a typical barrel elongation vs. temperature plot as sensed over the gage length of the

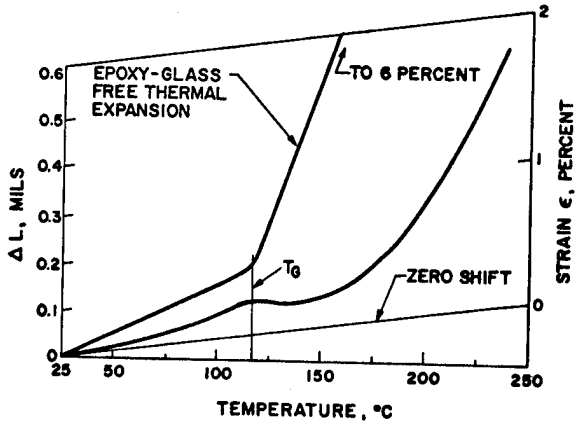

Figure 5

Typical Elongation and Strain Measurements as a Function of Temperature

extensometer. To obtain the thermo-mechanical elongation impressed on the copper barrel, the free-field copper thermal expansion and the extensometer differential thermal expansion must be subtracted from the plotted elongation. For a well designed extensometer, the extensometer differential thermal expansion can be made negligibly small.

The copper free-field expansion correction is equal to the product of gage length, coefficient of thermal expansion of copper, and the temperature difference from starting temperature. The combined correction function for copper free-field expansion and

extensometer differential expansion is most readily obtained by mounting the extensometer in a copper sleeve with the desired extensometer gage length. The resulting curve is labeled zero shift in Figure 5. All stress induced barrel elongations are measured in reference thereto. The associated barrel strain is obtained by dividing the elongation by the gage length (Equation (1)), and may be read directly on the auxiliary scale in Figure 5. The barrel strain as monitored near the midpoint over the 20 mil gage length is a good indicator of the maximum strain level encountered in the barrel.

Also shown on Figure 5 is a typical dielectric free-field expansion curve scaled to the extensometer gage length. It is of interest to note that the stress induced component of barrel strain is bounded above by the dielectric free-field thermal strain, and is bounded below by the copper free-field thermal strain. Implications of the barrel strain signature are discussed in greater detail in companion papers by Oien.[1,2]

Land Rotation Measurement

The fixturing for measuring surface land rotation is depicted in Figure 6. The upper barrel ID gripper

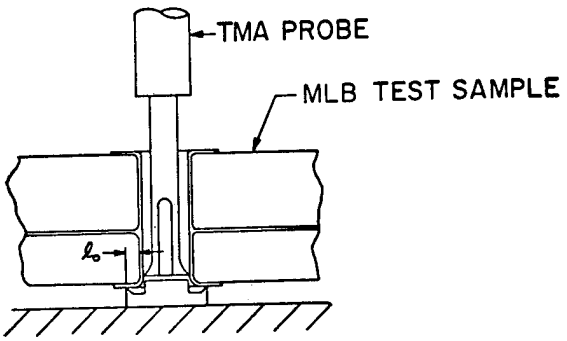

Figure 6

Land Rotation Measuring Fixture

as used with the barrel strain extensometer is mounted near the lower mouth of the PTH barrel. The lower surface land is supported an incremental radial distance ℓ_o further out than the PTH mouth OD. As the surface land rotates through some angle during a thermal excursion, a change of length is transduced by the TMA and plotted versus temperature as shown in Figure 7. Again an empirical correction is needed to compensate for the thermal expansion of the fixture. For small deformations, the deflection angle may be approximated by the tangent of the angle, $\Delta\ell/\ell_o$, i.e.

$$\phi \simeq \tan \phi = \frac{\Delta \ell}{\ell_o} . \qquad (2)$$

Again the angular deformation may be read directly from the auxiliary scale on Figure 7. It is of interest to note that essentially no land rotation occurs below the dielectric glass transition temperature, and that above glass transition, the land rotation is proportional to the temperature increment above glass transition.

Summary

An experimental technique is described which facilitates precise measurement of dielectric

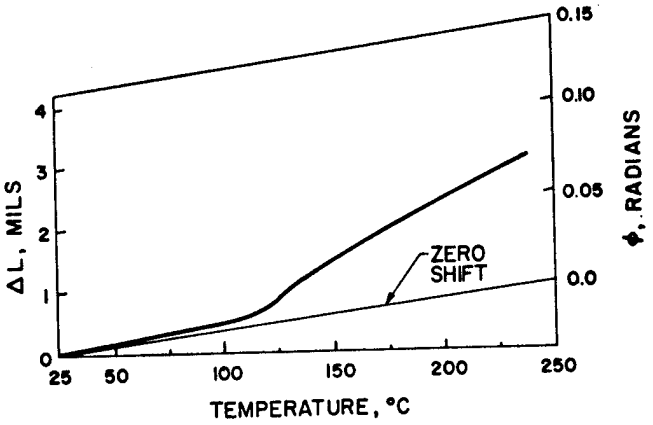

Figure 7

Typical Land Rotation Measurement as a Function of Temperature

free-field expansion, PTH barrel strain, and PTH surface land rotation as a function of temperature. These thermo-mechanical deformations are directly related to PTH failure mechanics.[1,2] Excessive barrel strains correlate with circumferential barrel cracking while barrel/land interface failures are correlated with excessive surface land rotations. Knowledge of the relevant thermo-mechanical deformations, coupled with an understanding of failure mechanics of the PTH structure, greatly facilitates the assessment of the influence of design, materials and process parameters on product performance. The described method for measuring thermo-mechanical strains in the PTH structure offers a powerful diagnostic technique.

The concept of failure mode specific testing which is discussed in a companion paper by Oien,[2] follows naturally from the measured thermo-mechanical deformation signatures and the Oien model of failure mechanics.

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A SIMPLE MODEL FOR THE THERMO-MECHANICAL DEFORMATIONS OF PLATED-THROUGH-HOLES IN MULTILAYER PRINTED WIRING BOARDS

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Abstract

A simple model is described which provides a basic understanding of the relationship between the thermo-mechanical deformations of a plated-through-hole and the consequent principal failure modes of the PTH structure. The model facilitates the design of effective reliability test programs and the interpretation of experimental results.

Introduction

It is well known that failures in electrical continuity can occur in multilayer printed wiring boards (MLBs) as a result of variable thermal environments. Such failures are generally associated with fractures which develop in copper plated-through-hole structures as a result of thermo-mechanical deformations which occur during a thermal excursion. To facilitate the economical manufacture of a reliable multilayer printed wiring product and extend the applicability of the technology, it is of interest to determine the influence of the principal design, materials and process parameters on the reliability of plated-through-holes (PTHs) under thermal stimuli. This is difficult to achieve by a purely empirical approach because of the complex and highly variable nature of the manufacturing process. To design an effective experimental program and properly interpret the data, it is almost essential to have some knowledge of the basic failure mechanics of the PTH structure.

Considering the complex statistical and nonlinear behavior of the materials involved, it is fortunate to find that an elementary one-dimensional model is sufficient to provide good insight into the thermo-mechanical behavior of the PTH, but is also simple enough to have intuitive appeal to those nonspecialists in mechanics who most often design reliability test programs. This paper will describe the model and show how it may be used to interpret experimental measurements of the two thermo-mechanical deformation components of a PTH structure which are most directly relatable to the principal failure modes of the structure. Applications of this analytical technique will be described in a companion paper.

Description of a Simple Model for PTH Barrel Strains

One of the principal failure modes of a PTH structure is the formation of a circumferential crack around the central portion of a PTH "barrel" (Figure 1). Such cracks may form when the MLB is heated to soldering temperatures. The polymer dielectric material expands much more rapidly with temperature than the copper of a PTH barrel. This produces axial tensile stresses in the barrel which can result in the fracture of a defective barrel.

To examine the axial strain of the PTH barrel as a function of temperature, consider the simple model shown in Figure 2. The model consists of two linear elements, each of which is characterized by a thermal expansion coefficient, α, and a stiffness parameter, k. One element represents the copper PTH barrel and the other element represents the surrounding dielectric material which is usually an epoxy-glass composite.

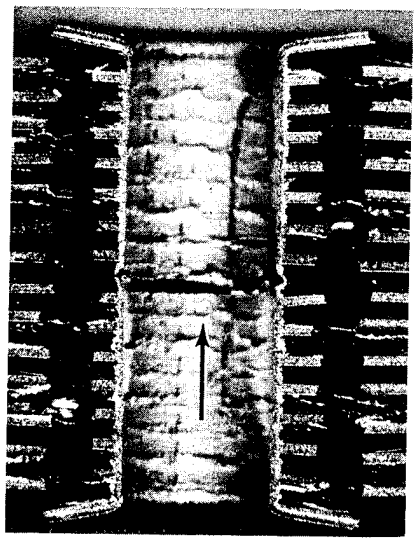


Figure 1

Illustration of a Circumferential Barrel Crack in a Plated-Through-Hole

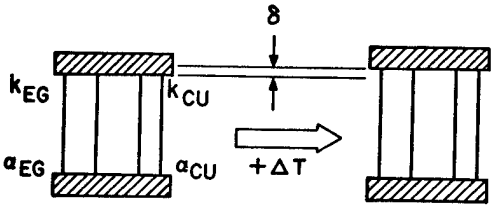


Figure 2

Simple Model for Plated-Through-Hole Barrel Strains

The two elements are constrained to have a common deformation, δ, resulting from a thermal excursion, ΔT. Here we are ignoring the axial variations in strain in order to simplify the problem.

The mechanics of deformation of the model during a thermal excursion is illustrated in Figure 3. The difference in thermal deformation of the two elements results in the stretching of the copper barrel, ε_{CU}, and the compression of the epoxy-glass, ε_{EG}. An analysis of the model results in the equation

$$\frac{\Delta\varepsilon_{CU}}{\Delta\alpha\Delta T} = \frac{1}{1 + \frac{k_{CU}}{k_{EG}}} \qquad (1)$$

where $\Delta\alpha = \alpha_{EG} - \alpha_{CU}$ and $\Delta\varepsilon_{CU}$ is the incremental mechanical strain of the barrel element resulting from

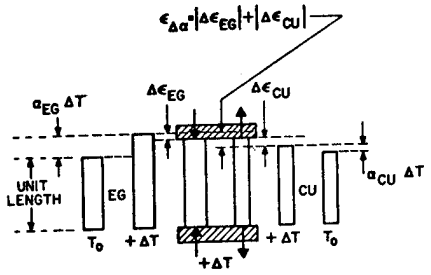


Figure 3

Schematic of the Barrel Strain Model Behavior

the temperature increment, ΔT. Note that we have excluded the thermal strain component of the barrel element corresponding to a free thermal expansion and are only considering in this equation the mechanical strain component associated with stresses and the development of a fracture.

The important conclusion to draw from equation (1) is that if the copper barrel element is relatively stiff compared to the epoxy-glass, the barrel undergoes little mechanical strain. But if the epoxy-glass is relatively stiff compared to the PTH barrel, the barrel will suffer mechanical strains nearly equal to the difference in thermal expansion between the two materials. While this may not seem to be very profound, it has very important implications because the effective relative stiffness ratio of the PTH barrel and surrounding epoxy-glass matrix tends to change dramatically during large thermal excursions, and assume values which are either very large or very small. Consequently, the model, coupled with a crude (order of magnitude) understanding of the mechanical behavior of the materials involved, leads to a simple but effective characterization of the thermo-mechanical deformations of a PTH structure.

First let us review the thermal expansion rates for the two material systems. Copper has a nearly constant thermal expansion rate of about $17\times10^{-6}/°C$ over the entire temperature range of interest (-65°C to +260°C). The transverse thermal expansion coefficient for the epoxy-glass composite varies with composition (which varies), but is generally in the neighborhood of the values

$$\alpha_{EG} \simeq \begin{cases} 75\times10^{-6}/°C & \text{for } T < T_G \\ 400\times10^{-6}/°C & \text{for } T > T_G \end{cases}.$$

Here T_G is the glass transition temperature below which the epoxy is in a hard, glassy state, and above which the epoxy is in a soft, rubbery state. $T_G = 110°C$ roughly marks the center of what is usually about a 20°C to 30°C wide transition zone from the glassy to the rubberoid state.

It is difficult to obtain precise information on the mechanical behavior of the epoxy resin systems commonly used in manufacturing MLBs, but the general behavioral characteristics of this class of polymers have been studied. An illustration of the typical behavior of the shear modulus of a cross-linked polymer as a function of temperature is shown in Figure 4. The

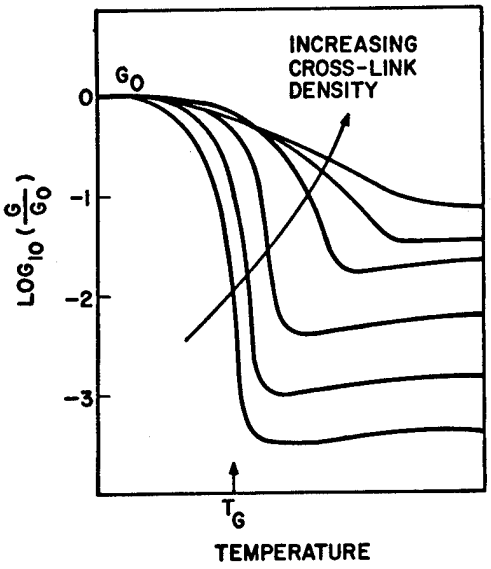


Figure 4

Typical Behavior of Shear Modulus (Normalized) Versus Temperature for a Cross-Linked Polymer

shear modulus has been normalized to illustrate that lower cross-link density polymers such as the epoxies used in MLBs undergo a drastic reduction in stiffness as they pass through the glass transition zone. The shear modulus in the rubberoid state above glass transition can be expected to be roughly two to three orders of magnitude lower than in the glassy state below the glass transition temperature, T_G.

The shear modulus of a material indicates how readily it can be deformed at constant volume. The resistance of a material to volume changes is given by the bulk modulus. It is characteristic of polymers that the bulk modulus does not change greatly in passing through the glass transition temperature. This means that in the rubberoid state, an epoxy may be relatively easily displaced away from the neighborhood of a PTH barrel by high stresses, but it cannot be easily compressed. This will have important implications when land rotations are considered.

For the purpose of the simple barrel strain model, it is sufficient to characterize the epoxy-glass element as exhibiting a bilinear behavior as a function of temperature. The stiffness of the element is assumed to diminish by about an order of magnitude in passing through a small glass transition zone coupling two linear regimes of constant stiffness. The order of magnitude drop in stiffness has been found to be about the change required for the model behavior to correspond to experimentally observed deformations in a PTH structure. This change of the epoxy-glass element is smaller than might be expected on the basis of the behavior of the epoxy alone, but can be explained in terms of the stiffening effect of the glass fibers of the composite, as well as an increase in the "effective area" of epoxy-glass material interacting with the PTH barrel.

The mechanical behavior of copper will be assumed to be independent of temperature, but to vary greatly

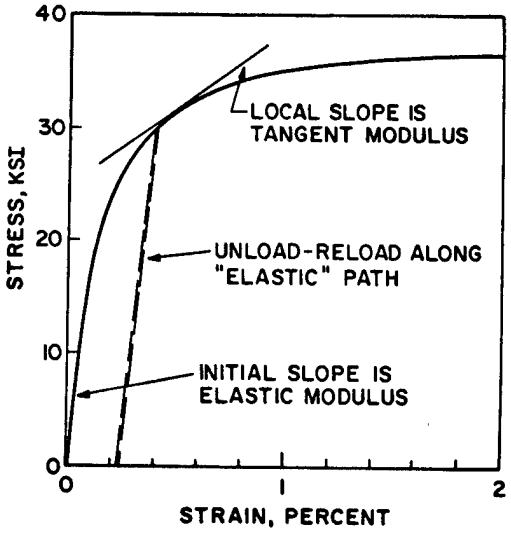


Figure 5

Stress-Strain Curve for an Electroplated Copper Foil

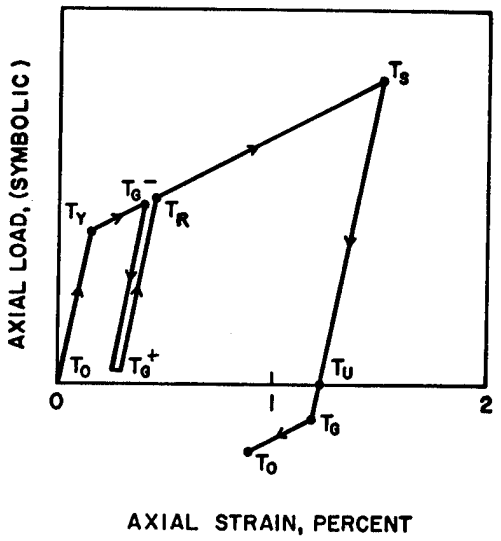


Figure 6

Load-Strain Curve for the Copper Element of the Barrel Strain Model

with the state of stress or more appropriately, strain. A typical stress-strain curve for a plated copper foil is shown in Figure 5. The material remains nearly elastic up to a stress level of about 20,000 psi, with an elastic modulus of about 17×10^6 psi as indicated by the initial slope of the curve. As plastic strain is initiated, the resistance of the foil to further deformation is given by the tangent modulus, that is the local slope of the stress-strain curve. As illustrated in Figure 5, the tangent modulus can decrease by an order of magnitude as the strain level approaches 1 percent. A second characteristic of the mechanical behavior of copper which should be noted in Figure 5 is that any unloading and subsequent reloading of the foil will follow a stress-strain path parallel to the initial elastic slope, with plastic deformation being resumed when the foil is fully reloaded. This is a bit of an idealization, but essentially true.

To simplify the nonlinear mechanical behavior of the copper for the purposes of the barrel strain model, it is assumed that the stiffness of the copper barrel element is bilinear as shown in Figure 6. This idealization of the copper as being a linear elastic/work-hardening plastic material is common to plastic analyses. The numerical values are not so important here as the concept that the effective stiffness of the copper barrel can undergo an order of magnitude change in passing from an elastic to plastic deformation regime, and vice versa.

The additional notation shown in Figure 6 will be explained later, but it should be noted that the figure indicates that compressive plastic strains are initiated at a relatively small compressive load. This is a common feature of the plastic behavior of metals and is called the Bauschinger effect.

Discussion of Computed PTH Barrel Strains

In this section we will discuss the characteristics of the deformations that can be computed from the simple barrel strain model as a PTH is heated through its initial soldering transient.

Keep in mind that the purpose of the model is to provide a simplified qualitative understanding of the thermo-mechanical deformations of a PTH structure. It will later be shown how the model facilitates the interpretation of the more complex experimentally measured deformations of a PTH.

Figure 7 presents a plot of PTH axial barrel strain versus temperature computed on the basis of the linearized order-of-magnitude characterizations of material behavior developed earlier. Included in Figure 7 are curves representing the free thermal expansion of the PTH copper and epoxy-glass composite. The mechanical strain component for the PTH is represented by the total strain shown minus the free thermal expansion component for the copper.

Experimental results indicate that the copper barrel and surrounding epoxy-glass composite tend to be of comparable stiffness during the initial stages of thermo-mechanical deformation. Consequently, we show the PTH barrel to be straining at about half the differential rate of expansion of the epoxy-glass composite and copper. This expansion occurs in a linear fashion until the yield point of the copper is reached at T_Y. As indicated in Figure 6, at this point the effective stiffness of the copper barrel to resist further incremental deformations is suddenly reduced by an order of magnitude as the copper moves into the plastic deformation regime. The glassy epoxy-glass composite is much stiffer than the plastic copper in this "glassy/plastic" regime so that the rate of deformation approaches that of the free expansion of the epoxy-glass composite.

In passing through the glass transition zone (T_G^- to T_G^+ in Figure 6), the stiffness of the epoxy-glass composite drops by about an order of magnitude and as a consequence the copper barrel unloads along a relatively stiff elastic path as shown in Figure 5. This results in a recovery of much of the elastic strain stored in the PTH barrel and an accompanying

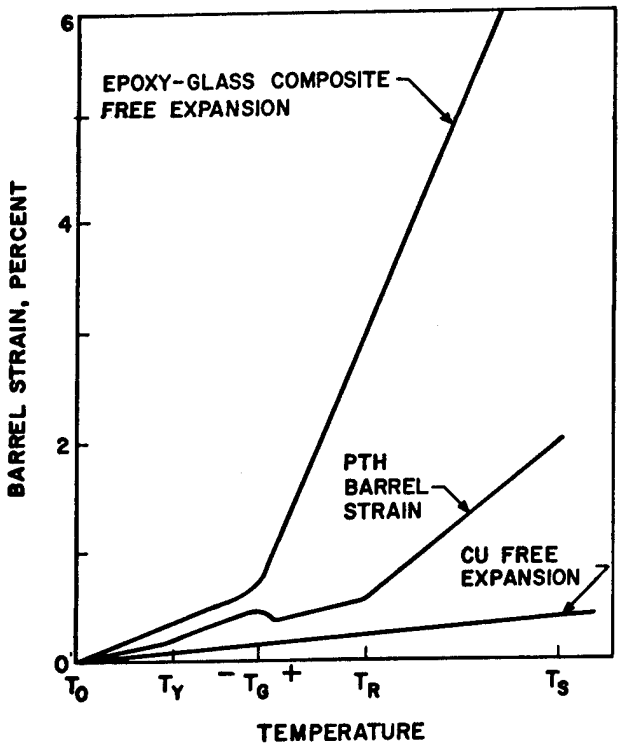


Figure 7

PTH Barrel Strain Versus Temperature Based on the Simple Piece-Wise Linear Model

contraction as indicated in Figure 7. As the rubberoid epoxy expands rapidly on continued heating, the PTH barrel is reloaded along the elastic path shown in Figure 6. In this "rubberoid/elastic" regime, the copper barrel is much stiffer than the epoxy-glass composite and the straining of the barrel takes place at a rate only slightly greater than the free thermal expansion rate of the copper.

The copper barrel reaches the point where it is fully reloaded at what we will call the recovery temperature, T_R. At this point the stiffness of the copper barrel suddenly drops by an order of magnitude as plastic deformation is resumed (see Figure 6). As a result of this change the plastic copper barrel and rubberoid epoxy-glass composite once again are of comparable stiffness, and significant mechanical deformation of the PTH barrel resumes in this rubberoid/plastic regime. As shown in Figure 7, this deformation mode continues up to the soldering temperature, T_S.

Once again, we point out that the detailed quantitative aspects of this analysis are not important. The important thing to note is that the deformations fall naturally into five distinctive thermal regimes: (1) glass/elastic, (2) glassy/plastic, (3) glass transition, (4) rubberoid/elastic, and (5) rubberoid/plastic, each of which corresponds to a markedly different regime of material behavior and mode of interaction between the PTH barrel structure and the surrounding epoxy-glass material.

Interpretation of Measured PTH Barrel Strains

Having gained some insight into the nature of the thermal response of a PTH structure based on the analysis of the simple piece-wise linear model, it is not difficult to interpret the more complex patterns of barrel strain measured experimentally during a thermal excursion. The most notable difference between the idealized and measured barrel strains results from making the simplifying assumption that the copper behavior is bilinear. Recall that the stiffness (tangent modulus) of a copper barrel actually varies continuously as plastic deformations progress. This nonlinear behavior eliminates the sharp distinction between the piece-wise linear thermal regimes discussed in the analysis of the simplified model. As shall be seen, it is nonetheless useful to interpret the actual PTH deformations in terms of these same five thermal regimes.

Figure 8 presents a trace of the axial barrel strains of a PTH measured during its first excursion to a soldering temperature. The curve was obtained using

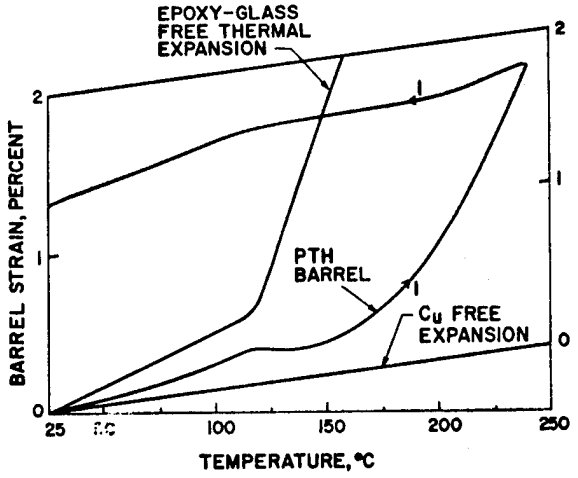


Figure 8

Experimentally Measured PTH Barrel Strains for the Initial Soldering Transient

the experimental technique described in a companion paper by Ammann and Jocher.* The curve actually presents the total axial barrel elongation measured over a 16.5-mil gage length at the center of a PTH barrel in a sample taken from a 120-mil thick, 16-layer MLB, but has been normalized to represent average strain over the gage length. No correction has been made to account for the influence of internal copper layers as would be required for a more precise analysis. The free thermal expansion rate for copper and the equivalent free transverse thermal expansion rate for the epoxy-glass composite (including copper inner layers) are also shown in Figure 8 as a basis of comparison. Keep in mind that the mechanical strain component of the barrel which contributes to fracturing is the excess of the total barrel strain over the free thermal expansion of copper.

Referring to Figure 8, it can be seen that the initial rate of mechanical barrel strain is about 1/3 of the differential rate of free thermal expansion of copper and the epoxy-glass composite. The initial curvature is attributed to a transient thermal response lag characteristic of the experimental technique which

* Ammann, H. H. and R. W. Jocher, "Measurement of Thermo-Mechanical Strains in Plated-Through-Holes," 14th Annual Proceedings, IEEE Reliability Physics Symposium, 1976.

tends to obscure the expected linear glassy/elastic regime. As the temperature rises, plastic flow is initiated in the barrel. Increased strain leads to a continual reduction in the copper stiffness in this glassy/plastic regime, and the rate of strain of the barrel approaches the free expansion rate for the epoxy-glass composite.

Continuing to refer to Figure 8, the MLB sample passes through a glass transition zone in the neighborhood of 115°C, and the recovery of the elastic strain evidenced by the contraction of the barrel can be readily observed. The reloading of the barrel along an elastic path takes place over a range of about 20°C which corresponds to the rubberoid/elastic regime, and plastic deformation of the barrel is resumed at about 150°C. Owing to the complex nonlinear behavior of the copper, the plastic strain is reinitiated earlier and more gradually than was indicated by the idealized linear model. Plastic straining of the barrel continues in the rubberoid/plastic regime up to the soldering temperature of about 240°C. In this regime, the barrel is apparently somewhat more stiff than the surrounding epoxy-glass composite.

The barrel suffers a maximum mechanical strain of about 1.7 percent at the highest temperature. Recall that this is averaged over a 16.5-mil gage length near the center of the barrel. A small correction for the influence of the two copper lands straddled by the extensometer must be made to arrive at a more precise estimate of the strain level in the plated copper foil of the barrel between lands, but development of the rationale for such a correction is beyond the scope of this paper. A 15-percent increase in the measured strain would be a reasonable correction. This, of course, assumes that the barrel is straight and of uniform quality, and does not suffer from defects which lead to localized strain amplification.

If one has gained a mechanistic understanding of the thermal response of the PTH barrel on heating, it is not difficult to extend the analysis to the cooling cycle. However, there is an additional key phenomena which must be brought into the analysis, namely, the tendency of the epoxy to debond from the copper surfaces when in tension. This regularly occurs along the barrel wall, and sometimes also occurs along the surfaces of the lands and copper inner layers. Debonding can have a significant influence on the PTH deformation following the initial heating transient during which the epoxy-copper interfaces are in compression.

Consider the PTH barrel strains shown in Figure 8 for the cooling cycle. The initial phase of the response on cooling is once again perturbed by a transient thermal lag characteristic of the experimental technique. This tends to obscure the rather rapid recovery of the elastic tensile strain in the barrel during the initial phase of cooling. In this rubberoid/elastic cooling regime, the high thermal contraction rate of the rubberoid epoxy leads to a rapid unloading of the PTH barrel along an elastic path as illustrated in Figure 6 (i.e., path T_S to T_U).

Further cooling and contraction of the epoxy would tend to place the plastically deformed (elongated) barrel in axial compression and the adjoining epoxy matrix in tension. But the PTH barrel is relatively resistant to compressive axial deformations (i.e., stiff) when being loaded along an elastic path as illustrated in Figure 6. Consequently, the tensile stresses in the epoxy matrix quickly increase to the low level required for debonding along the PTH barrel wall. (Debonding occurs less readily along the surfaces of the lands because of special processes performed to promote bonding.) The debonding along the barrel wall allows a lateral contraction of the rubberoid epoxy which results in a relaxation in the tensile stresses in the transverse or axial direction. As a consequence of this debonding and relaxation of tensile stresses, the continued thermal contraction of the rubberoid epoxy may proceed without resulting in a significant axial loading of the copper barrel. Thus, as illustrated in Figure 6, the axial barrel strain tends to parallel the free thermal contraction of copper as the sample is cooled to the glass transition zone.

In passing through glass transition, the epoxy becomes relatively stiff. In the glassy state the relaxation of lateral stresses accompanying the debonding from the barrel no longer results in a substantial reduction in the transverse stresses. As a consequence, the effective stiffness of the epoxy-glass composite greatly increases with respect to the PTH barrel, and significant mechanical deformations of the barrel resume as the sample is cooled below glass transition. As can be seen in Figure 8, the rate of barrel strain in this regime is comparable to the rate of free thermal transverse contraction of the epoxy-glass composite. This suggests that the barrel is fairly compliant compared to the surrounding epoxy-glass matrix because it is being deformed along a plastic path, T_G to T_o, as illustrated in Figure 6.

For the test sample illustrated in Figure 8, the residual axial strain (elongation) near the center of the PTH barrel is about 1.3 percent at the end of the initial thermal cycle to a soldering temperature. The magnitude of the residual strain is primarily dependent on the relatively large plastic strains which take place at temperatures well above glass transition on the initial heating to a soldering temperature. As shall be seen, this large plastic strain increment occurs only for the initial "soldering transient." This is very significant to the failure mechanics and testing of PTH barrels.

PTH Barrel Strains for Multiple Cycles

After the initial soldering transient, subsequent thermal cycles to the same soldering temperature result in a range of axial PTH barrel strains which is significantly smaller than that experienced on the initial transient. This is because the initial soldering transient alters the mechanical behavior of the PTH copper (work-hardening) and epoxy-glass composite (debonding), and leaves the barrel in an elongated state.

Figure 9 presents a trace of the experimentally measured axial barrel strains for both the initial and second soldering transient of the same PTH sample considered in the previous section. During the second heating cycle, the barrel strain occurs in an almost linear fashion up to the glass transition zone. This corresponds to an extended glassy-elastic regime resulting from the work-hardening of the copper. In passing through glass transition the second time, there is very little evidence of elastic strain recovery indicating a lower state of strain.

On further heating, the PTH barrel exhibits a strain rate only slightly greater than the rate of free thermal expansion of copper as shown in Figure 9. In this regime the expanding rubberoid epoxy is refilling the free volume voided on the previous cooling cycle as a result of the lateral contractions that occurred following the debonding from the PTH barrel wall. These voids are completely refilled as the soldering

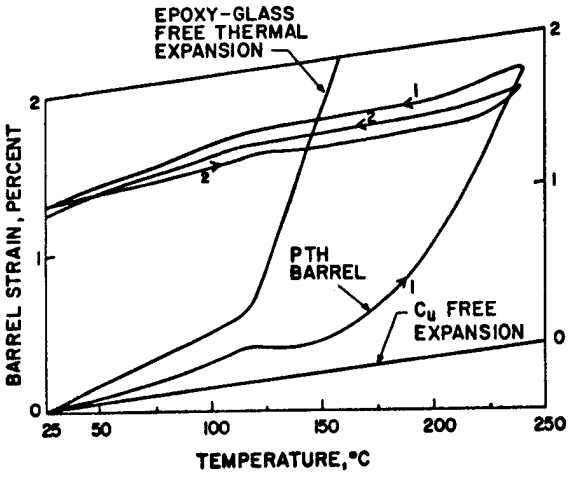


Figure 9

Experimentally Measured PTH Barrel Strains for the Initial and Second Soldering Transients

temperature is approached. Further heating beyond the previous high temperature would result in significant reloading of the PTH barrel and reinitiation of the relatively high strain rate experienced in the rubberoid/plastic regime of the initial transient. Stopping the heating on the second cycle at the previous high temperature and cooling back to ambient results in a barrel strain curve quite similar to that generated during the initial transient as shown in Figure 9.

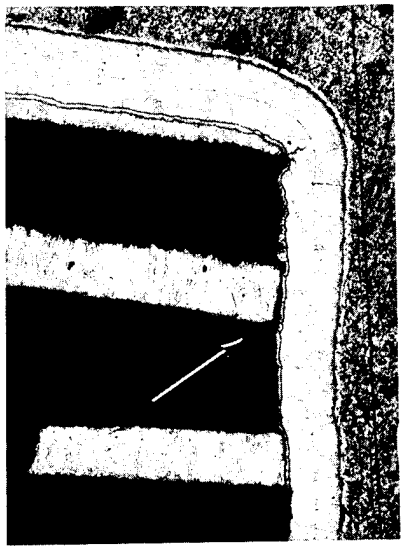
Although not illustrated here, subsequent cycling to the same high temperature will generally produce a barrel strain curve quite similar to the second cycle. An important thing to note is that on repeated thermal cycling from ambient to a fixed temperature above glass transition, the rate of axial barrel straining with temperature tends to be much greater below glass transition than above.

Description of a Simple Model for Land Rotations

A second principal failure mode of PTH structures is the formation of fractures at or near the interface between the PTH barrel and the outermost copper inner layers. Incipient failures of this type are illustrated in Figure 10. Fractures tend to occur either along the electroless copper between the PTH barrel and outer land as shown in Figure 10a, or in the vendor copper of the outer land as shown in Figure 10b. Both of these type fractures are associated with the bending of the outer lands with respect to the PTH barrel which takes place as the PTH is heated to soldering temperatures.

A simple model for the deformation of the lands with respect to the PTH barrel is shown in Figure 11. The model consists of a rigid "land" hinged on one end to the previously considered PTH barrel strain model and driven on the other end by an element representing the transverse free thermal expansion of the epoxy-glass composite at some distance from the plated-through-hole. In this case the PTH barrel model should be interpreted to represent the displacement at the point where the land joins the barrel.

For significant deformations, the bending of the land tends to be concentrated near the interface



(a) Fracture Along the Electroless Copper at the Barrel/Land Interface

(b) Fracture in the Inner Layer Land Copper Near the Barrel/Land Interface

Figure 10

PTH Barrel/Land Interface Failures

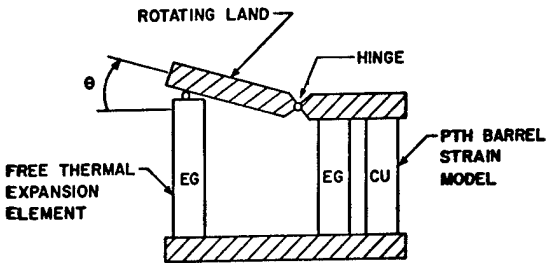


Figure 11

Simple Model for PTH Land Rotations

at what is referred to in mechanics as a "plastic hinge." This concentration of plastic strain is a result of the nonlinear behavior of copper. Notice in Figure 5 that a moderate increase in stress can result in a large increase in plastic strain. Because of the formation of a plastic hinge, the outer part of a land tends to rotate about it in a relatively rigid fashion as suggested by the model.

A more detailed analysis than can be presented here also suggests that as the angle of land rotation, θ, increases, the plastic strains would become even more concentrated at the hinge, and the amplitude of plastic strain leading to the formation of fractures would increase more rapidly than a linear dependence on θ. Then for a PTH with a number of inner lands, one could expect the angle of rotation, θ, or a given land to be roughly proportional to the distance, Z, from the central plane of the board, and expect the magnitude of plastic strains to increase more rapidly than a linear dependence on Z.

A companion paper by Ammann and Jocher describes a method of measuring the rotation of surface lands with respect to the PTH barrel axis. Experimental results for surface land deformations confirm that significant deformations are well modeled by a nearly linear rotation of the land about a hinge at the corner of the PTH. To the degree that land rotations are proportional to the distance of the land from the central plane, the surface land rotations can be used to estimate the inner land rotations. Since the analysis of the land rotation model behavior is easily understood, we shall proceed directly to its use in interpreting experimental results.

Interpretation of Measured Surface Land Rotations

A trace of the deformations of a surface land with respect to the corner of the PTH barrel as a function of temperature is presented in Figure 12. The

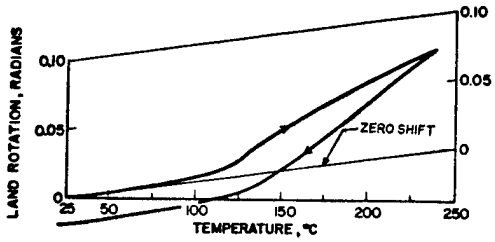


Figure 12

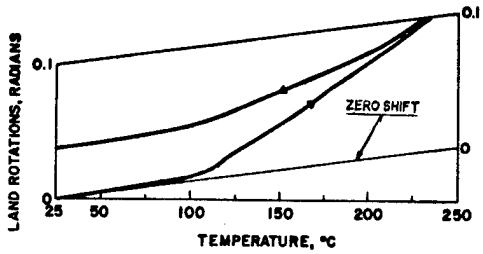
Experimentally Measured PTH Surface Land Rotations for the Initial Soldering Transient

deformations were measured over a 20-mil gage length using an experimental technique described in the companion paper by Ammann and Jocher. The test sample PTH was taken from a 120-mil thick, 16-layer MLB. Also shown in Figure 12 is the calibration curve for the extensometer used in measuring the deformations. The difference between the measured displacements and the calibration curve, normalized by the gage length, provides an estimate of the angle of rotation of the land with respect to the PTH barrel axis.

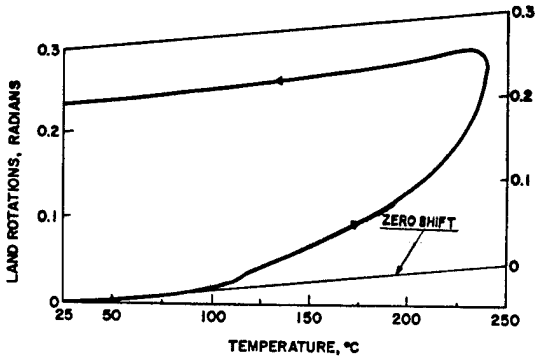
As can be seen in Figure 12, the land rotations are markedly different in two thermal regimes. Below the glass transition temperature, the rate of rotation with temperature is almost negligible. Upon considering our model, this should be expected. As was shown in Figure 8, the difference between the rate of axial PTH barrel strain and the transverse free thermal expansion of the epoxy-glass composite is relatively small in the glassy regime. On the other hand, above glass transition, the difference between the rate of axial PTH barrel strain and transverse free thermal expansion of the epoxy-glass composite is comparatively large in the rubberoid regime. Recall that even though the shear modulus of the epoxy is greatly reduced above glass transition, the rubberoid epoxy is relatively incompressible. This allows a displacement of the epoxy away from the PTH barrel, but augments the forced rotation of the lands.

Note in Figure 12 that the angle of land rotation is almost linearly proportional to the temperature increase above glass transition. The observed deviations from linearity can be explained by considering the changes in the rate of axial PTH barrel strain above glass transition. In particular, note that on heating, an accelerated rate of barrel strain at higher temperatures as shown in Figure 8 leads to a corresponding diminution of the rate of land rotations as seen in Figure 9. Further, note that the residual elongation of the PTH barrel on cooling to ambient leads to a corresponding negative residual land rotation.

It is not uncommon for the surface lands to debond from the epoxy or for the epoxy-glass composite to degrade and exhibit a permanent increase in thickness upon returning to ambient after an initial soldering transient. This results in a residual positive land rotation as shown in Figure 13. When this occurs, it becomes questionable as to what degree inner lands might exhibit proportional deviations, particularly



(a) Illustration of the Effect of Debonding



(b) Illustration of the Effect of Epoxy Degradation

Figure 13

PTH Surface Land Rotations for Defective Product

on subsequent cycling. For "good" product not exhibiting these faults, subsequent cycling leads to a quite repetitive and predictable behavior.

Figure 14 presents a trace of surface land rotations versus temperature for the initial soldering transient considered in Figure 12 as well as a subsequent soldering transient. The deformations for the second cycle are more linear, as might be expected from a consideration of the second PTH barrel strain cycle shown in Figure 9. The land rotations for subsequent cycles tend to be very similar to those for the second cycle.

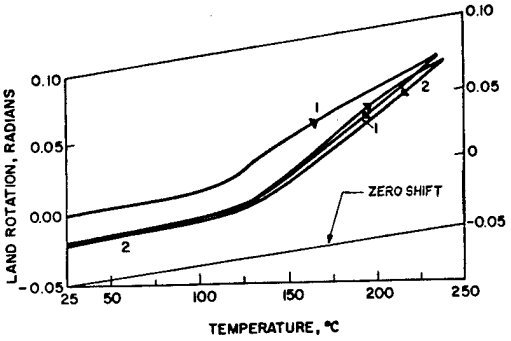


Figure 14

Experimentally Measured PTH Surface Land Rotations for the First Two Soldering Transients

Summary

The foregoing analysis of the mechanical response of a PTH structure to thermal stimuli has established several important points. In general the thermo-mechanical deformations of a PTH structure are of a fundamentally different nature above and below the glass transition temperature.

For the axial PTH barrel strains associated with the formation of circumferential barrel cracks, the initial soldering transient leads to a relatively large plastic strain increment near the soldering temperature which results in a residual elongation of the PTH barrel. Subsequent cycling produces a repetitious pattern, with barrel strains being on the order of the transverse free thermal expansion of the epoxy-glass composite below glass transition, and with relatively little plastic straining occurring above glass transition.

Significant deformations of the type associated with the formation of fractures near the outer PTH barrel/land interfaces occur only above the glass transition temperature. The amplitude of these deformations varies almost linearly with the temperature range above glass transition.

Acknowledgments

The author would like to thank R. W. Jocher and T. A. Early for performing the experimental measurements of PTH deformations, and H. H. Ammann for helpful discussions regarding the modeling and interpretations of these deformations.

METHODS FOR EVALUATING PLATED-THROUGH-HOLE RELIABILITY

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Abstract

The principal thermo-mechanical failure modes of a plated-through-hole structure are described and the major factors contributing to such failures are discussed in mechanistic terms. This leads to the development of an improved methodology for evaluating the reliability of plated-through-holes.

Introduction

This paper reviews several methods which are useful in addressing reliability problems associated with the thermo-mechanical failure of plated-through-holes (PTHs) in multilayer printed wiring boards (MLBs). These failures are of two principal types, 1) barrel cracks extending around the circumference of a PTH, and 2) fractures in the neighborhood of the interface between the PTH barrel and lands on the copper inner layers. Barrel cracks and interface fractures are stimulated by the types of thermo-mechanical deformations of a PTH structure discussed in the preceding paper.[1] The mechanistic interpretation of the thermal response of a PTH described in that paper is applied here in developing a methodology for evaluating the reliability of PTHs and examining the underlying causes of failures.

The general approach to be used here is to consider failure mechanisms in terms of three principal factors, 1) the nominal thermo-mechanical deformations and associated stresses and strains characteristic of a PTH in a well manufactured MLB, 2) the localized amplifications of stresses or strains which may occur in defective product, and 3) the level of local copper strength or ductility which is available to resist these stresses and strains. Extensive reliability testing has shown that PTHs of well manufactured MLBs have a very high reliability potential. Reliability problems are primarily due to the large amplifications of strain and/or reductions in effective copper ductility or strength which result from a highly variable manufacturing process.

PTH Barrel Cracks

An earlier paper by Ammann and Jocher[2] described a method for directly measuring the axial strain averaged over a central portion of a PTH barrel. This is the measurable strain component most directly relatable to circumferential PTH barrel fractures. Experimental results show that for a well manufactured 120 mil thick, 16 layer epoxy-glass MLB with approximately 1.5 mils thick copper plated in the hole, the nominal maximum axial strain near the center of the barrel for an initial soldering transient up to about 240°C is only on the order of 1.7%. On the other hand, a good quality ductile electroplated copper foil can exhibit a strain to failure in excess of 20%. Clearly then, a well manufactured MLB should be highly resistant to the formation of PTH barrel cracks.

Nevertheless, it is not uncommon to encounter manufacturing difficulties which result in PTHs which are subject to the formation of barrel cracks. This tendency to form barrel cracks is generally due either to imperfections in the PTH barrel wall which greatly amplify the level of axial strains, very poor effective ductility of the copper plating, or a combination of these two factors. Poor drilling or excessive acid etching during the hole wall cleaning process can lead to rough barrel walls. A well leveled but thin plating of the rough barrel wall may then result in localized stress concentrations and large plastic strains. For certain copper electroplating systems, the rough hole wall may also have a detrimental influence on grain growth and produce locally weakened intergranular boundaries which are easily fractured. Even if the PTH walls are smooth, variable electroplating processes may yield copper of very low ductility.

Generally, the fracturing of deficient PTHs is initiated during the first soldering transient. It was pointed out in Reference [1] that for a conventional thick epoxy-glass MLB, the PTH barrel undergoes a relatively large plastic strain increment at higher temperatures which is not repeated on subsequent cycles to the soldering temperature. It is in this regime that barrel fractures are initiated at localized defects in the barrel wall. However, these cracks may be arrested as they propagate into a barrel zone of better quality, and it may take a number of subsequent thermal cycles to propagate them entirely around the circumference of the PTH barrel and produce an electrical malfunction. This creates the appearance that "failures" result from thermal cycling. Actually the mechanical failure (i.e. fracture) is initiated during the first soldering transient and only becomes functionally (electrically) manifested after some cycling.

The failure to perceive that barrel cracking is initiated on the first soldering transient is largely due to the insensitivity of conventional experimental techniques. The presence of reflowed solder can easily mask a significant barrel fracture, and the test circuits and testing criteria which have commonly been used are not sufficiently sensitive to the small resistance changes which are characteristic of incipient failures. A highly sensitive technique for electrically testing for the occurrence of barrel cracks in individual PTHs is described in a companion paper by D. A. Rudy.[3] Using this technique, one can readily monitor the extent of cracking of a solder stripped PTH barrel.

If a PTH barrel remains uncracked during the initial soldering transient, it will generally require hundreds of rather severe thermal cycles to produce cyclic fatigue cracking of the barrel. As indicated in Reference [1], for thermal cycles following the initial soldering transient, the greatest opportunity for significant cyclic plastic straining of a PTH occurs in the regime below glass transition. For epoxy-glass boards which remain well bonded, it requires hundreds of cycles between -65°C and +85°C (just below the onset of glass transition) to produce true cyclic fatigue failures of a PTH barrel. Cycling of an epoxy MLB between room temperature and temperatures above glass transition produces only a small plastic strain increment and is ineffective toward initiating cyclic fatigue barrel cracking.

For most MLB applications, true cyclic fatigue circumferential barrel cracking is not a viable failure mechanism and one need only be concerned with the

capacity of PTHs to survive the initial soldering transient without cracking to assure adequate barrel quality. In this case, the sensitive measurement of the change in PTH barrel resistance as a result of the initial soldering transient is the most expeditious means of assessing barrel quality.

PTH Barrel/Land Interface Failures

As pointed out in Reference [1], PTH barrel/land interface failures are of two types. Fractures occur either 1) along the electroless copper between the PTH barrel and outer lands, or 2) in the inner plane copper near the barrel/land interface. Both of these type failures are stimulated by the flexing of the land with respect to the barrel axis which takes place as the MLB is heated above the glass transition temperature. However, the two types of failures are generally associated with distinctively different manufacturing deficiencies.

Fracturing along the electroless copper interface can be ascribed to either faulty hole wall preparation (principally cleaning) or deficient electroless copper plating. In either case, the fracture can be thought of as resulting from a stress level which exceeds either the "strength" of the electroless copper or the bond strength between the electroless copper and the land. On the other hand, fracturing adjacent to the interface can be ascribed to either a lack of inner layer copper ductility, or the imposition of excessive plastic strains associated with defective product, or a combination of the two.

It is important to make a distinction between failures which are associated with either stresses or strains. Because of the nonlinear behavior of copper in the plastic regime, the stress level which occurs at the electroless copper barrel/land interface varies only moderately as the plastic deformation progresses. Consequently, there is little opportunity for significant amplification of the nominal stress levels which occur at the interface for good quality product, and failures can be attributed directly to marked deficiencies in electroless copper plating or bond strength at the interface.

On the other hand, as explained in Reference [1], epoxy degradation at soldering temperatures can lead to a significant increase in land rotations and consequently a large amplification of the plastic strain level in the inner-plane copper near the outer barrel land interfaces. Other variables such as board thickness, relative thickness of the barrel and inner layer copper, or resin content adjacent to the PTH can also significantly influence the level of plastic strains near the interface. Factors affecting the amplification of land rotations and the consequent high plastic strain levels can be examined using the experimental technique for measuring surface land rotations described in the companion paper by Ammann and Jocher.

Variations in the ductility of the inner layer copper are much more difficult to assess and deal with. This material is usually supplied to MLB manufacturers in the form of a copper clad epoxy-glass laminate and the ductility of the copper is not well controlled. This places the burden of avoiding fractures of the inner layer copper on a control of the factors lead to excessive land rotations and plastic strains.

As for circumferential barrel cracking, the initiation of fracturing at or near barrel/land interfaces generally occurs during the first soldering transient. These initial fractures are often of only a limited extent and further thermal cycling is required to propagate the cracks entirely around the barrel/land interface and cause a loss of electrical continuity. Since even sizable interface fractures cause only a small change in resistance of a series circuit, it is difficult to detect incipient cracking by conventional electrical testing techniques. However, a test circuit which is particularly sensitive to resistance changes caused by the development of fractures at a PTH barrel/land interface has been designed by J. N. Hines and is presented in a companion paper.[4] Using the experimental techniques described in that paper, the development of interface fractures can be readily detected.

It was pointed out in Reference [1] that for epoxy-glass MLBs which do not degrade or debond from the PTH lands, the land rotations which give rise to barrel/land interface failures are roughly proportional to the temperature increment above glass transition and are repeatable upon continued cycling. Consequently, even if a fracture is not initiated on the first soldering transient, there is a possibility that cyclic fatigue fractures may occur in the inner layer copper of the lands due to the sizable plastic strain increment which may occur on repeated cycling to soldering temperatures of even fairly well manufactured product. As a result a single soldering transient may not be sufficient to test the quality of MLBs which are to be subjected to numerous cycles to soldering temperatures. Less rigorous requirements for repeated cycling to temperatures somewhat above glass transition poses little potential for stimulating cyclic fatigue interface failures.

Failure Mode Specific Testing

The relation between thermal environments and thermo-mechanical failure mechanisms of PTH structures as discussed here, coupled with the availability of specialized test circuits, leads naturally to the development of a test philosophy which we will call failure mode specific testing. Embodied in this test philosophy are two major elements.

The first element involves the use of that specialized test circuit which most directly and sensitively measures the initiation and progression of fractures associated with an individual thermo-mechanical failure mode of a PTH structure. For circumferential barrel cracks this implies the use of the PTH barrel resistance measurement scheme described in the companion paper by D. A. Rudy,[3] and for barrel/land interface failures it implies the use of the PTH barrel/land interface resistance measurement scheme described in the companion paper by J. N. Hines.[4]

The second element involves the use of that thermal test environment which provides the most direct and expeditious stimulation of the relevant failure mechanism. An initial transient to a conservatively high soldering temperature can provide an adequate stimulus for acceptance testing under most quality requirements. For the most part, thermal cycling need only be carried out to establish the relationship between the ultimate reliability potential of a PTH structure under prescribed environmental conditions, and the indications of product quality found from the initial soldering transient test. In performing such tests, large amplitude thermal cycles below the glass transition temperature will generally stimulate barrel cracking most effectively while large amplitude cycles above glass transition tend to stimulate interface failures most effectively.

It should also be recognized that there is an important distinction to be drawn between the thermo-cyclic propagation of fractures initiated during the first soldering transient, and the stimulation of true cyclic fatigue fractures. Cyclic fatigue results in the slow development of microcracks. However, once a fracture becomes sizable, it may propagate rapidly and in an erratic manner. Consequently, test methods which require large resistance changes to reveal failures are not very satisfactory for investigating the influence of design, materials or process parameters on the reliability of PTHs. The failure mode specific test methodology described here provides the optimal means of stimulating thermo-mechanical failures of PTH structures and perceiving them in an incipient stage. This represents a significant improvement over existing methodology.

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MEASUREMENT OF LAND TO PLATED-THROUGH-HOLE INTERFACE RESISTANCE IN MULTILAYER BOARDS

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Abstract

Thermally induced cracks can occur at the interface between land and PTH barrel, hence, a measure of electrical continuity of the interface connection is important in product quality assessment and reliability projection. Series circuits with poor resolution are generally used to monitor circuit integrity during thermal tests. A much more sensitive method of measuring the interface directly is described.

Introduction

This paper describes a technique for observing the onset of failure in the land to plated-through-hole (PTH) interface connection resulting from thermally induced stresses in a multilayer board (MLB). Simply stated, a measurement is made of the resistance of a circuit in a test coupon that includes an interface and a minimum amount of circuit resistance, so that small changes in circuit resistance, and in particular changes due to cracks at the interface, are readily detected. Periodic measurements are made on the coupon during thermal cycling, and the changes in resistance with the number of cycles are used to determine failure history.

Previously, MLB test coupons were made with series circuits consisting of a string, or strings, of printed wiring, lands, and PTHs meandering through the layers to test for the thermal life of both PTHs and their connections to printed wiring. Normally, circuit continuity was tested by measuring the total circuit resistance and determining the change in resistance of the string. Such a circuit has the advantage of testing a large number of circuit components (PTHs, interfaces, etc.) at one time, but has the disadvantages that small resistance changes (incipient failures) are masked by the gross resistance of the circuit, and that diagnostic measurements are required to locate and type a failure (an open circuit) when one occurs.

Measuring Technique

As stated previously, a MLB coupon circuit was designed so that measurements can be made across a single land to PTH interface with a minimum of circuit resistance included for increased resolution. Since the resistance is small, four terminal resistance measuring techniques are required to eliminate effects of instrumentation contact resistance. This is illustrated in Figure 1, where current I flows from printed wire to land and out of the bottom of the PTH, the potential drop is measured as shown, and the interface resistance is defined as the ratio of V to I. As defined, this includes a finite but small amount of circuit resistance, usually less than 100 μΩ.

A routing diagram of an actual signal layer circuit in an MLB coupon is shown in Figure 2, and a schematic diagram showing PTH connections between printed wire lines (indicated as "X" on the diagram), and points of contact of the measuring probes in Figure 3. To measure the interface resistance at PTH (8, 14), for example, current will enter the coupon

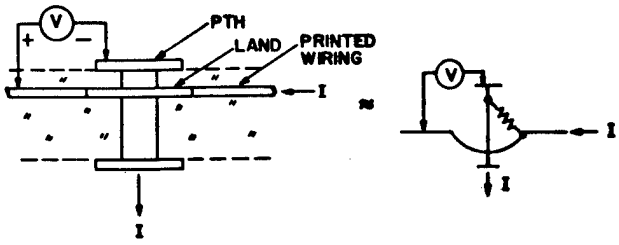
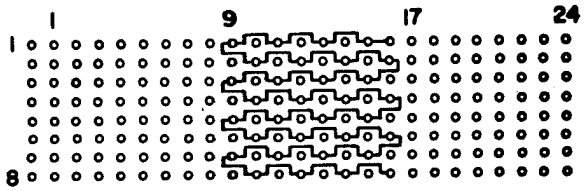


FIGURE 1

Interface resistance ≡ V/I.



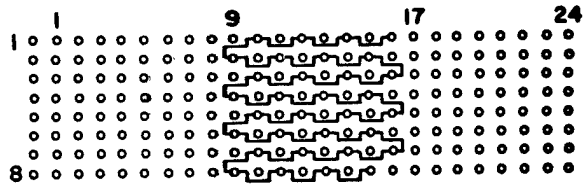


FIGURE 2

Routing for land to PTH interface circuit on signal layers.

through the permanent contact and flow along the printed wire line directly to the PTH and out the switched connection at the bottom. The voltage drop across the interface circuit is obtained from the switched and permanent voltmeter connections as shown. The permanent voltmeter contact is connected to the interface circuit via the printed wire line on the lower layer to PTH (1, 16), then back to the subject PTH via the printed wire line on the upper layer. Since no current flows in this path during the measurement, the voltage drop measured is that across the interface circuit. It is evident from the above discussion that a measuring system with high resolution and rapid switching capability must be employed.

A block diagram of the measuring system is shown in Figure 4. It is a Hewlett-Packard Model 9500B Automatic Test System with TOPTS software (i.e., Test Oriented Paper Tape System), uses a HP modified BASIC as the programming language, and operates under programmed control of the 2100 minicomputer. The

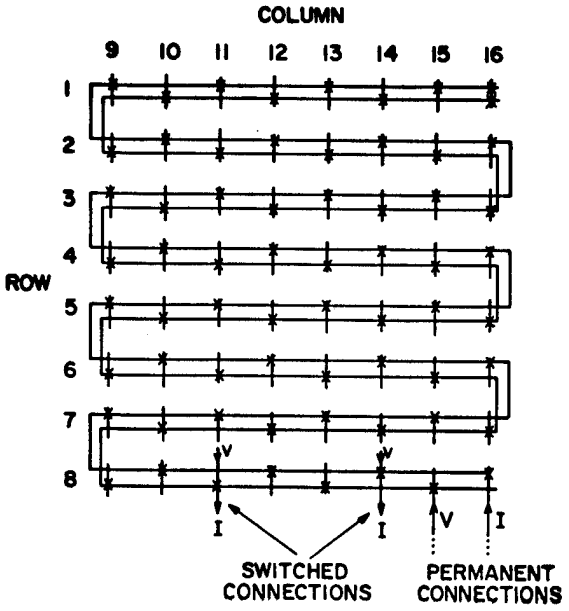


FIGURE 3

Schematic diagram of land to PTH interface resistance circuit ("X" denotes a connect).

operating system tape and application programs are input via a high speed reader. Record-keeping data and program run control are input via a teletypewriter terminal and/or the control panel, hardcopy copy is available from the terminal. The magnetic tape unit is used for mass storage of data. The system measures the magnitude of the current and the voltage drops in the test circuit and calculates resistance values.

The instruments used in measurements consist of:

1. DVM with 1 μv resolution.
2. Programmable constant current power supply set for a nominal value of 1 ampere.*
3. A 6 wire, 100 channel crossbar scanner and its control, the modular switch. (The output of the power supply is reduced to zero before the crossbar scanner is switched between channels.)
4. A one-ohm standard resistor.
5. An interface connector to connect to test fixtures.

In operation, the crossbar scanner first connects power supply and DVM to the standard one ohm resistor to measure the voltage drop across it. This value is stored in memory as the magnitude of the current. It then connects them to up to 99 channels to measure the voltage drops across the respective test circuits. These are used to calculate the corresponding values of resistances and store them in core memory. To eliminate biasing effects of contact potentials in the measuring circuit, the polarity of the power supply is reversed, the measurement repeated, and the two values averaged and stored on mag tape. Time per measurement is controlled by relay and power supply settling times and averages approximately two measurements per 3 seconds. To date the system has been used to measure interface, barrel, and series circuit resistances.[1,2,3,4]

* System resolution is proportional to the current; however, the heating effect of the current flow on circuit resistance must be determined.

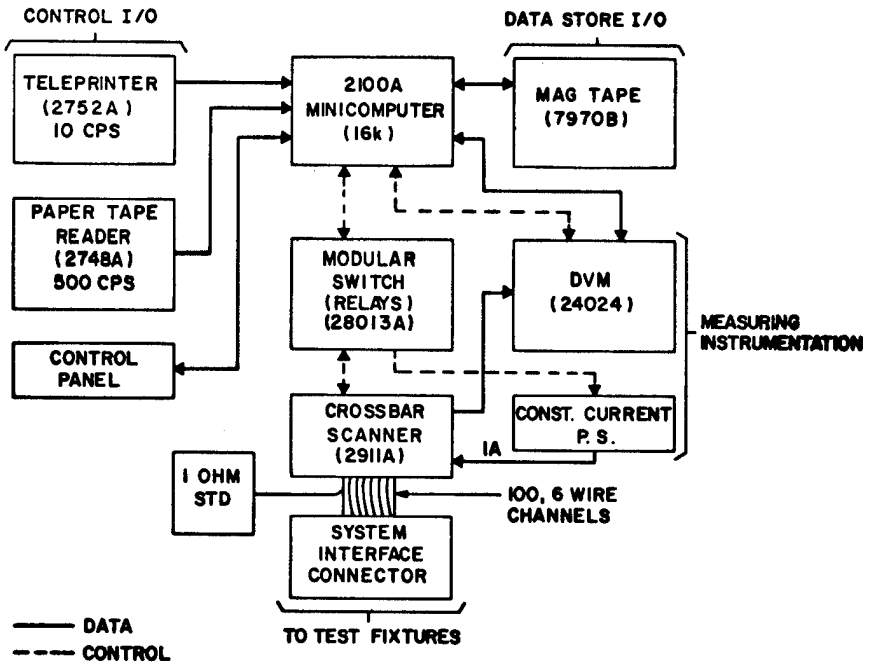


FIGURE 4

Data acquisition system for testing MLBs; system block diagram.

The results of an experiment designed to determine overall system precision has shown that for PTH barrel resistance measurements the average standard deviation, σ, is 0.5 μΩ. The distribution of the standard deviations was such that $P[\sigma \leq 2.0\ \mu\Omega] = 0.999$. The systematic error at the time of the experiment was +0.4 μΩ. The upper limit of the heating effect of the current flowing through a PTH during a measurement was estimated and found to be less than 0.1 μΩ; a negligible effect. This appears to be substantiated by the statistics of the test results.

It was determined from this experiment that the variability of the PTH barrel resistance measurement is primarily due to variations in positioning the test coupon under the contacting probe head. In addition, variations in measured resistances were observed that resulted from circuit heating by the test current flowing through a high resistance contact between a measuring probe tip and a cover-layer land. This usually occurred when the probe tip contacted the land in a crater resulting from a previous measurement and failed to break the surface film. Careful cleaning and roughing up the surface of the land eliminated most of this variability.

An example of the results of interface resistance measurements is shown in Figure 5. Here is shown

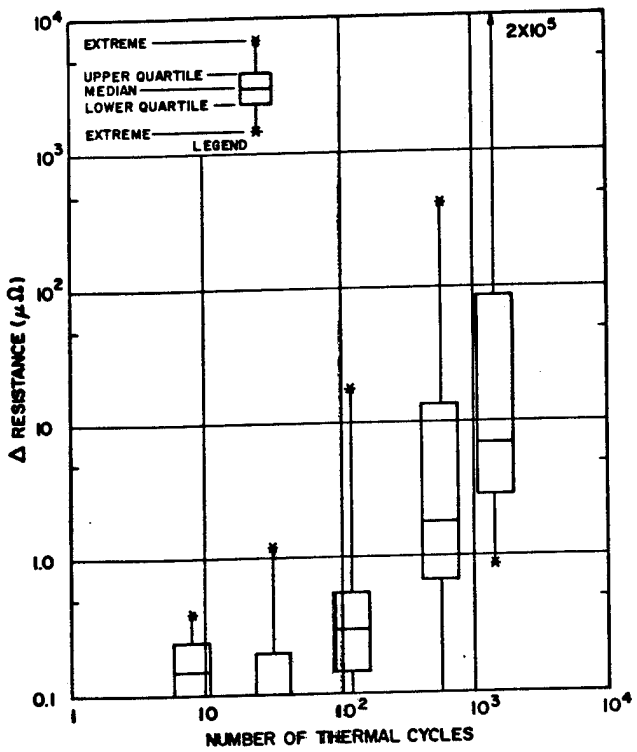


FIGURE 5

Distribution of the change in interface resistance with number of thermal cycles.

statistical distributions of the changes in resistance resulting from a sequence of thermal stress stimuli.

The test coupons were subjected to a solder transient (∿240°C, 1 min) during the time pins were reflow soldered into the PTHs using a hot air gun. They were then subjected to repeated cycles between 25°C and 175°C (i.e., above dielectric glass-transition temperature) with a two minute immersion time at each temperature[5]. Measurements were made after soldering, and during cycling as shown. The statistical quantities used are defined in the legend of the figure. Note the monotonic change in interface resistance with number of stress stimuli.

Summary

A technique has been described for early detection of land to plated-through-hole interface cracks in a failure mode specific test, that is, using appropriate thermal stimuli and test circuits. Measurements are made using instrumentation that features high resolution and a rapid scanning capability; e.g., changes in interface resistance of one micro-ohm are easily resolved.

Acknowledgment

It is a pleasure to acknowledge the contributions of R. J. Biola in carrying out careful measurements both in evaluating the measuring system and during the interface resistance tests.

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THE DETECTION OF BARREL CRACKS IN PLATED THROUGH HOLES USING FOUR POINT RESISTANCE MEASUREMENTS

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Abstract

The influence of voltage and current probe connections on the detection of barrel cracks and similar flaws in plated through holes is discussed. Theoretical calculation of the sensitivity of a four point resistance measurement to the length of a barrel crack is compared to experimental results for a variety of current voltage probe configurations.

* * * * *

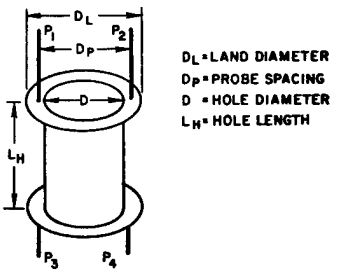
Four point resistance measurement have been used extensively as a means for testing the integrity of plated through holes (PTHs) in multilayer boards (MLBs). This paper describes the analytical and physical modeling of a plated through hole containing a representative flaw. Since controlled flaws are difficult to introduce into a device the size of a PTH the measurements were made on an enlarged analog consisting of a stainless steel tube with a diameter of 1-1/2 inch. The influence of the land areas at the end of the PTHs was represented by a simple extension of the tube. The effect of lands can be precisely accounted for analytically when the lands have a significant influence on the measurements.

We shall first discuss the model used, then the analytic treatment, and finally the corroborating measurements. A plated through hole is essentially a conducting cylinder with small lands at each end as shown in Figure 1(a). As a first approximation the lands can be accounted for by letting the tube effectively extend beyond the normal length of the PTH as in Figure 1(b) and making measurements at the normal PTH length (shown by dotted lines on Figure 1(b)).

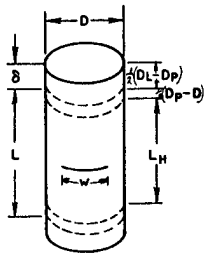
The most common barrel flaw seen in cross sections of failed PTHs is a circumferential crack. The influence of most other flaws can be interpreted in terms of the results of measurements on this kind of flaw. The crack is represented as a slit of length W near the center of a tube of radius r and circumference C. The wall thickness is t and the electrical conductivity is σ.

We begin by discussing the current distribution due to injecting and removing the current at point contacts. We consider only the two cases where either the source and sink lie on a vertical line along the tube length or diametrically opposed (Figures 2(a) and 2(b)). In either case there are vertical lines of symmetry, at and diametrically opposed to the sources or sinks, across which no current flows. A cut can be made along either of these two lines and the tube unfolded to make a flat strip. The boundary conditions are then that no current flows across the ends of the tube and that the solution be symmetrical at the cut lines. Such a problem can be solved by images.

When the barrel length L is small with respect to the circumference C, the current distribution is similar to the flux distribution of a simple dipole field; while when the source and sink are far apart, the current density J across the strip (or around the tube) become essentially uniform in the region between the source and sink. Figure 3 shows the maximum

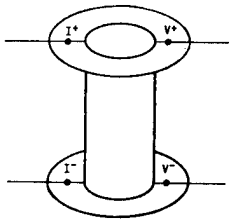


(a) PICTORIAL REPRESENTATION OF A PTH WITH PROBES ATTACHED TO LANDS



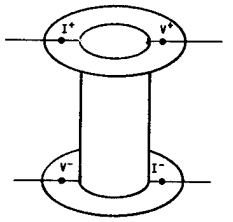
(b) LANDS REPRESENTED AS AN EXTENSION OF THE PTH BARREL

Figure 1



(a) LOCATION OF CURRENT AND VOLTAGE PROBES WITH CURRENT PROBES VERTICALLY ALIGNED

I^+ - CURRENT SOURCE
I^- - CURRENT SINK
V^+ - POSITIVE VOLTAGE PROBE
V^- - NEGATIVE VOLTAGE PROBE



(b) LOCATION OF CURRENT AND VOLTAGE PROBES WITH CURRENT PROBES DIAGONALLY ALIGNED

Figure 2

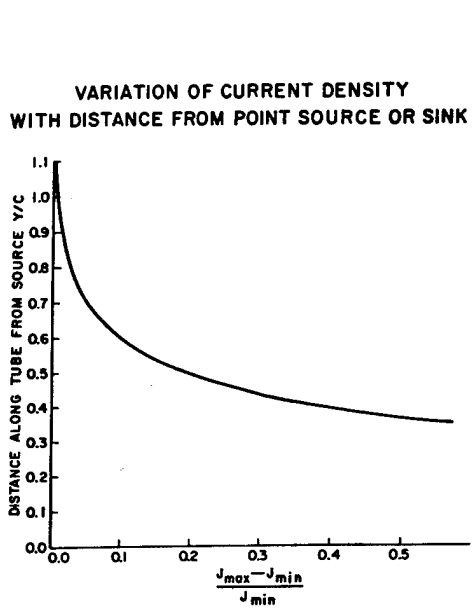


Figure 3

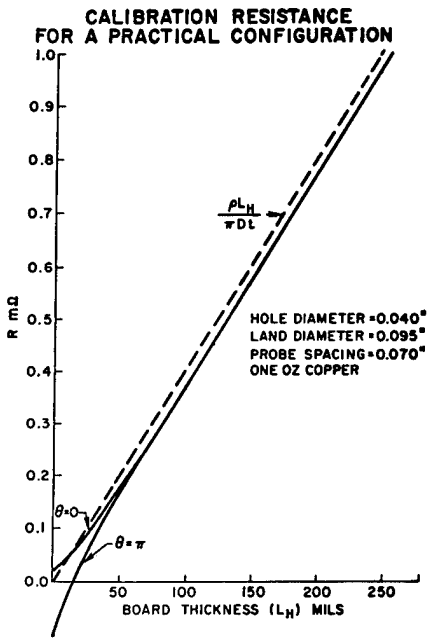


Figure 4

variation of current density across the strip as one moves away from a source or sink when the source and sink are far apart. As long as the source and sink are more than the width of the strip apart the current density comes within 10% of uniformity midway between source and sink. As source and sink are further separated the degree of uniformity and the extent of the region of current uniformity increases rapidly.

Calculation of the measured resistance of a flaw-free PTH shows that the resistance can be expressed as three terms

$$R = \frac{\rho L_H}{\pi Dt} + \frac{\rho(D_p - D)}{\pi Dt} - \frac{\rho}{\pi t} \ln 2\left[1 + \exp - 2\left(\frac{D_L - D_p}{D}\right)\right] \quad (1)$$

where t is the thickness of the barrel wall and ρ is the resistivity of the wall material. The other symbols are defined in Figure 1. The first term is the classical resistance of a cylinder of length L_H and diameter D, the second term is a correction to account for the location of the current and voltage probes while the third term corrects for the finite dimension of the lands. Details of the calculations and the results of the calculations are presented elsewhere.[1] Figure 4 is a typical plot of the resistance as a function of the length of the barrel. The two curves marked θ = 0 and θ = π represent the configurations of Figures 2(a) and 2(b) respectively. Either curves, such as Figure 4, or equation (1) can be used for a precise determination of ρ/t or σt which will be needed to evaluate the resistance change due to a barrel crack.

We now turn to the consideration of the effect of a flaw such as a circumferential crack on the current distribution in the PTH and on the resistance as determined by a four point measurement. The cylindrical tube shown in Figure 1(b) can be cut along a line bisecting the slit of width W to form the strip in

Figure 5. In order to avoid the influence of end effects and to simplify the computation of the resistance change due to the circumferential slit we shall consider the strip to have an unlimited extent in the vertical (Y) direction. The strip, of width C, is partially cut by insulating boundaries from either side leaving a gap in the center of width g = C - W.

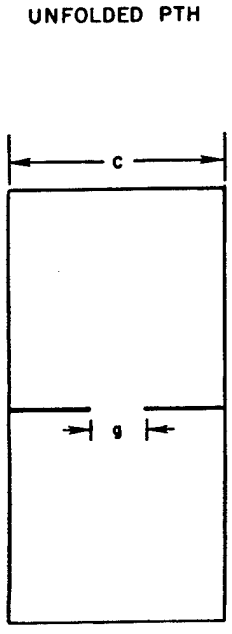


Figure 5

By using a conformal mapping sequence[2,3] we can map the slit strip into an unslit strip. The complex potential is then

$$\omega = E\omega(Z) \tag{2}$$

$$\omega = \frac{EC}{\pi} \sin^{-1}\left[\frac{\sin\frac{\pi Z}{C}}{\sin\frac{\pi g}{2C}}\right] \tag{3}$$

The potential in the strip with the slit is found from

$$V = \mathrm{Im}(\omega) \tag{4}$$

where Im represents the imaginary part of the function and $Z = X + iY$. The components of the current density are

$$J_x = \sigma \mathrm{Im}\left|\frac{d\omega}{dZ}\right| \tag{5}$$

and

$$J_y = \sigma \mathrm{Re}\left|\frac{d\omega}{dZ}\right| \tag{6}$$

where Re denotes the real part of the function and $\sigma = (\rho)^{-1}$ is the electrical conductivity. Equation (2) contains the assumption that far from the slit the current density is uniform and of magnitude

$$|J| = \sigma E \tag{7}$$

i.e., the total current is a constant independent of the slit size (as long as there is some finite gap for the current to flow through). Thus the total current I is

$$I = \sigma t\, CE \tag{8}$$

and the resistance $R = 2V/I$ is

$$R = \frac{2}{\pi\sigma t} \sinh^{-1}\left(\frac{\sinh\frac{\pi Y}{C}}{\sin\frac{\pi g}{2C}}\right) \tag{9}$$

where the resistance is measured between points at ±Y which are far from the slit. We are interested in the change in resistance ΔR which is due to the introduction of the slit,

$$\Delta R = R - Ro \tag{10}$$

where

$$Ro = \frac{2Y}{\sigma tC} \ . \tag{11}$$

In this particular calculation we have not included the correction terms for probe position or land edges because they are eliminated by the assumption in equation (2).

If we take the difference, expand the inverse hyperbolic sine and then let Y become arbitrarily large we are left with

$$\Delta R = -\frac{2}{\pi\sigma t} \ln \sin\left(\frac{\pi g}{2C}\right) \tag{12}$$

or

$$\Delta R = \frac{2}{\pi\sigma t} \ln \sec\left(\frac{\pi W}{2C}\right) \ . \tag{13}$$

This function is plotted in Figure 6.

The validity of this formula is predicated on the assumption that the current density approaches uniformity as one moves away from the immediate

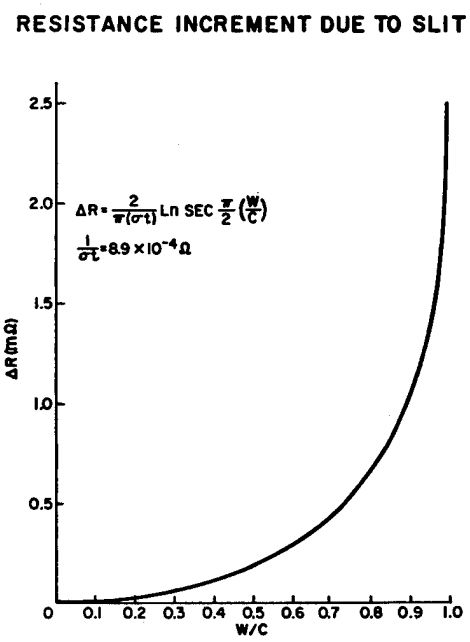


Figure 6

vicinity of the slit. Since practical resistance measurements involve current and voltage probes which are point contacts, these probes must be far enough from the slit that the current becomes essentially uniform at some point between the current probes and the slit. In other words, the current distributions due to the point current probes and due to the slit must not interfere. When the probes are too close to the slit the measured resistance becomes strongly dependent upon the precise location of the probes.

The required separation between the current probes and the slit can be estimated from Figures 3 and 7. Figure 3, as described before, shows the extent of the current nonuniformity due to the current probes while Figure 7 shows the extent of the current nonuniformity near the slit with the size of the slit as a parameter. The extent of the current nonuniformity due to the slit when the tube is almost completely cut through is almost identical to that of the point current contact.

If the current probes are a distance greater than roughly half the circumference of the PTH away from the slit, the influence of the slit and the influence of the current probes on the current distribution will be essentially independent. The angular position of the current probes around the circumference of the cylinder (PTH) should not affect the measured resistance.

To test the dependence of the measured resistance on probe position, aspect ratio and slit length, a set of measurements has been made on enlarged analog models of a cylindrical PTH. The models were 1-1/2" diameter stainless steel tubes of sufficient length to give the desired aspect ratios. The ten voltage and current probe configurations are shown in Figure 8. In configurations (A) through (E) the voltage and current probes are attached at the same points, while in configurations (F) through (K) voltage and current probes are attached diametrically opposite. Four aspect ratios of 2.93, 1.40, 1.35 and 0.633 were tested. In each case a slit was cut around a circumference at the

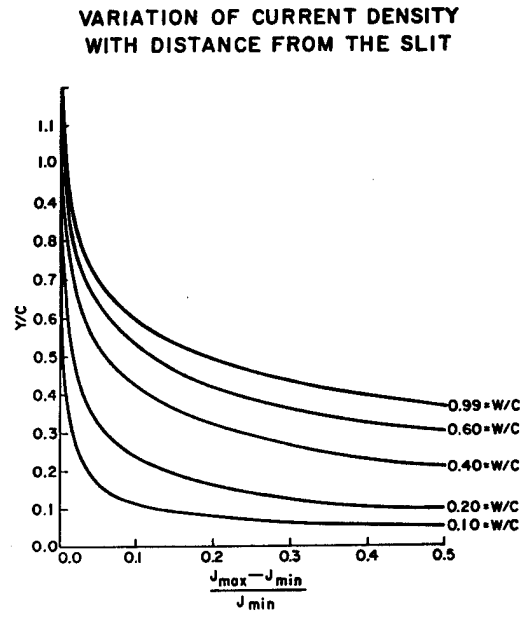


Figure 7

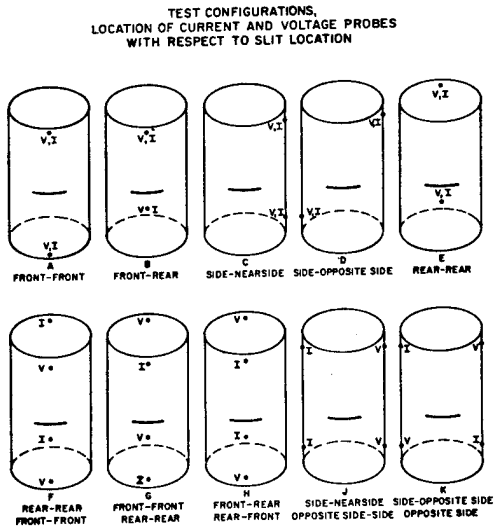


Figure 8

middle of the tube as shown in each of the configurations of Figure 8 and the resistance was measured as a function of slit length.

The measured resistance of a tube with an aspect ratio of 2.93 is shown in Figure 9. The resistances

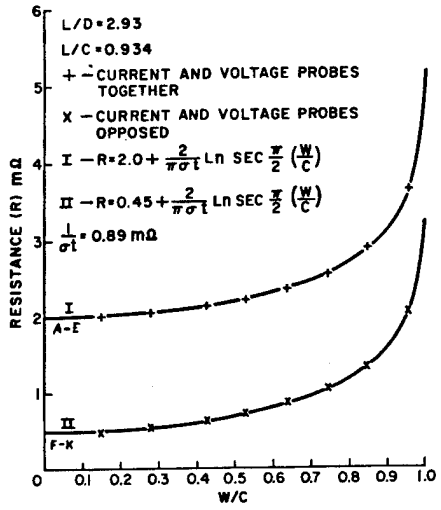


Figure 9

measured in configuration (A) through (E) fall on curve I while all the resistances from configurations (F) through (K) fall on curve II. The change in resistance due to the slit fits the data extremely well and no angular dependence is detectable.

The only difference which exists between the configurations (A) through (E) and configurations (F) through (K) of Figure 8 is the larger "constriction resistance" at the contacts in configurations (A) through (E). Since configurations (A) through (E) do not represent a desirable method for resistance measurements these configurations were not included in further data.

When the aspect ratio is reduced to 1.40 or 1.35 as shown in Figures 10 and 11 respectively the current distributions begin to interfere and the separate configurations become distinguishable. There can now be a change in measured resistance as the measuring probes are moved around the cylinder with respect to the slit. The change is slight and can easily be masked by error fluctuations.

Figure 12 shows the measured resistances for a very short cylinder with an aspect ratio of 0.633. Each of the voltage-current probe configurations is easily distinguished here.

When the voltage and current probes are diametrically opposed some of the resistance measurements are "negative". With the width of the strip (circumference of the cylinder) much larger than the length, the voltage probes are physically much closer to the opposite polarity current probe and the flaw free resistances are inverted.

From the above results we can come to several conclusions about the use of four point resistance measurements to evaluate plated through holes:

RESISTANCE OF A CYLINDER WITH ASPECT RATIO 1.40

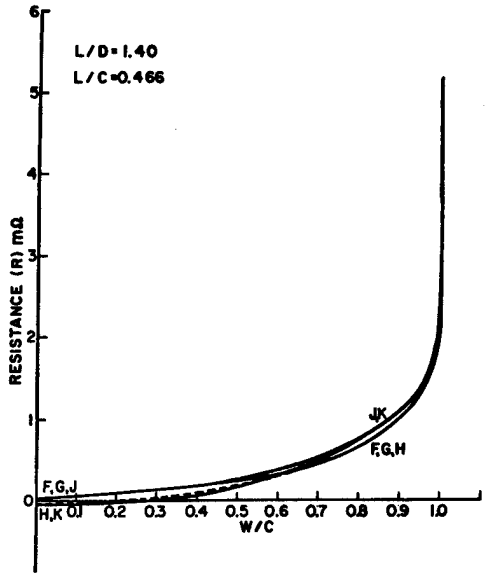


Figure 10

MEASURED RESISTANCES OF A CYLINDER WITH ASPECT RATIO 1.35

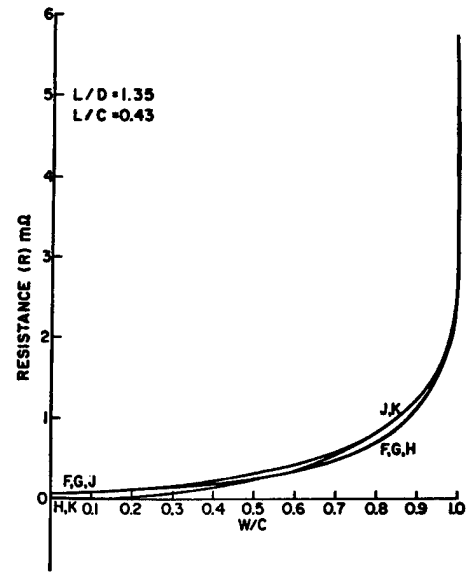


Figure 11

1. The technique is insensitive to pinholes or cracks much less than one tenth of the way around the barrel. Flaws which should not lead to failure will not be easily detected.

MEASURED RESISTANCES FOR A CYLINDER WITH ASPECT RATIO 0.633

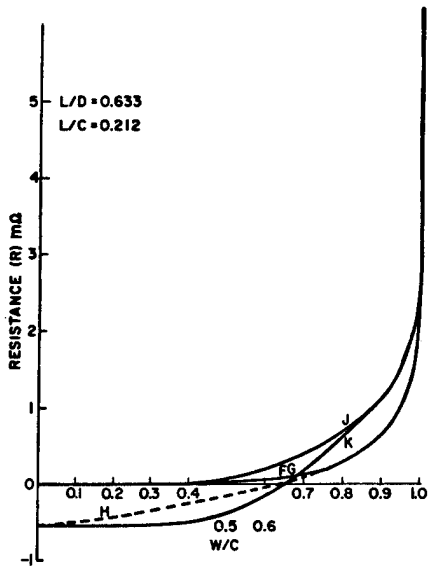


Figure 12

2. The technique is easily capable of sensing large flaws, such as barrel cracks which have propagated a large part of the way around the barrel. Flaws subject to imminent failure should show up quickly.

3. Measuring the angular dependence of the resistance to detect flaws is not more sensitive to cracks than a simple resistance measurement at an arbitrary angle. In fact, for large aspect ratios there is no angular dependence at all.

Four wire plated through hole resistance measurement can be used to detect the reliability of product and its sensitivity to barrel cracking by measuring the resistance before and after applying a thermal stress cycle to a sample product or coupon.

For small cracks the resistance change can be approximated as

$$\Delta R \simeq \frac{\pi}{4\sigma t}\left(\frac{W}{C}\right)^2 \qquad (14)$$

which increases very slowly for small cracks. For large cracks the resistance change increases very rapidly. For a typical PTH resistance measuring system, a resistance change of about 5 micro ohms can reliably be measured. Such a resistance change would correspond to a crack about 8 to 10% of the way around a barrel.

Using a fixed resistance change criterion to detect a barrel crack biases the selection criteria against thin copper walls or high resistivity copper because the resistance change would be higher under these conditions for the same crack length. This bias might be justified if it were considered that either thin walls or high resistivity copper represented a less reliable product. If on the other hand, an objective criteria employing the same crack length for all product is desired then the product of σt must be

found from the measurement of the unstressed product and equation (1). The latter procedure is to be preferred because it determines the true nature of the barrel carck and permits an objective evaluation of the failure. If a bias in the evaluation is to be preferred it should be inserted explicitly.

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2. Morse, P. M., and Feshbach, H., "Methods of Theoretical Physics," McGraw-Hill, 1953, p. 1238ff.

3. Kober, H., Dictionary of Conformal Representations, Dover, 1957.

SIMULATION OF THERMAL STRESS STIMULI IN THE TESTING OF PRINTED WIRING PRODUCTS

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Abstract

Simulated thermal stress stimuli are used for reliability testing and quality assessment of printed wiring products. Heat transfer is discussed in terms of internal conduction and measured surface convection coefficients encountered during manufacture and testing. The fluidized particulate bath is discussed as an attractive medium for applying thermal stress stimuli.

Introduction

Heating and cooling processes are encountered in the manufacture, acceptance testing, assembly and service life of printed wiring products such as multilayer boards (MLBs). Thermo-mechanical failure of plated-through-holes (PTHs) is an established failure mechanism in MLBs. Thermal strains may be imposed on the composite structure of a MLB due to the steady state and transient components of the impressed thermal field. The steady state strains result from the different thermal expansion characteristics of the constituents of the composite, while the transient strains result from thermal gradients in the structure. In a PTH, the two components of strain are subtractive during the heating phase, and additive during the cooling phase. Dielectric deterioration of MLBs at soldering temperature has also been observed. This dielectric degradation appears to be activation energy controlled, and progresses rapidly at soldering temperatures.

Simulated soldering transients are widely used as thermal stress stimuli for end product quality assessment. Accelerated thermal cycling is used to project life in a variety of service environments. To facilitate characterization of the resulting thermal strains, it is useful to first characterize the thermal field of an MLB undergoing a heating or cooling process.

Newtonian Heating and Cooling

To determine the relevant characteristics of a wide variety of heating environments encountered, it is necessary to define the thermal field generated in an immersed object. This time dependent field may be characterized to first order in terms of Newtonian heating or cooling. Consider an object (Figure 1) of volume V, density ρ, specific heat c, surface area A, and initial temperature T_o immersed into a fluid of temperature T_∞ and heat transfer coefficient h. It can be shown[1] that for either heating or cooling

$$\frac{T-T_\infty}{T_o-T_\infty} \equiv \frac{\theta}{\theta_o} = e^{-\frac{hA}{\rho cV}t} \qquad (1)$$

where t is the time after immersion. It is of interest to note the analogy of heat transfer in Newtonian heating and cooling and the charge transfer in a series capacitor and resistor in response to a change in applied voltage.

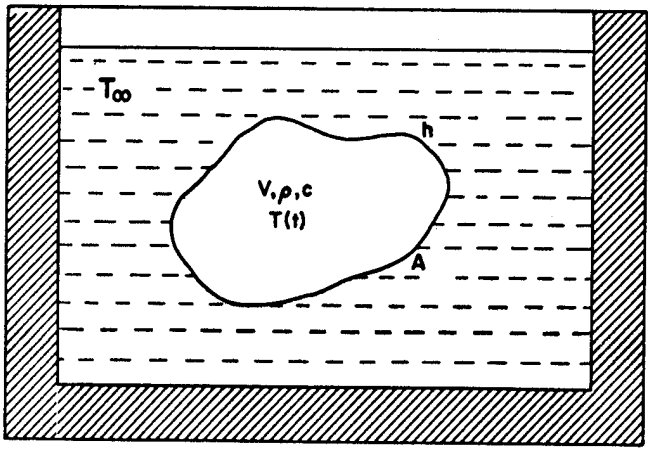


FIGURE 1

Newtonian heating/cooling

Table 1 shows the analogous lumped parameters. Figure 2 is a symbolic plot of Eq. (1) for heating and cooling, which again depicts the similarity between Newtonian heating/cooling and the capacitor charging/discharging process.

PARAMETERS	ELECTRICAL RC NETWORK	NEWTONIAN HEATING/COOLING
Capacitance	C	ρcV
Resistance	R	$\frac{1}{hA}$
Time dependent potential difference	E(t)	$\theta(t)$
Applied potential difference	E_o	θ_o
Charge/Heat transferred	C·E(t)	$\rho cV\theta(t)$

TABLE 1

Analogous Parameters for RC Circuit and Newtonian heating/cooling

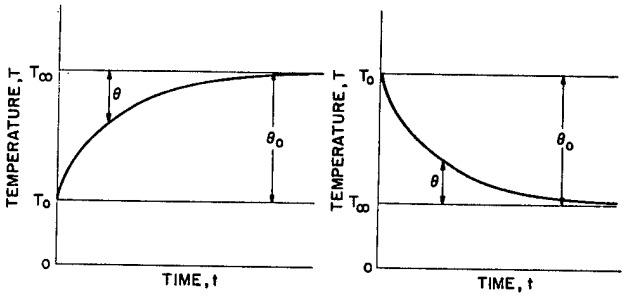


FIGURE 2

Symbolic plot of Newtonian heating/cooling

It is of interest to investigate factors influencing the rate of change of temperature. Differentiating Eq. (1) with respect to time yields

$$\frac{d\theta}{dt} = \frac{dT}{dt} = -\theta_o \frac{hA}{\rho cV} e^{-\frac{hA}{\rho cV} t} \qquad (2)$$

The following parametric groupings are of interest:

θ_o - the initial temperature difference, may be preselected within limits allowed by thermophysical properties of the heating/cooling environment

h - the heat transfer coefficient is a characteristic of the heating medium

ρc - the volume specific heat, depends on the constituents of the object

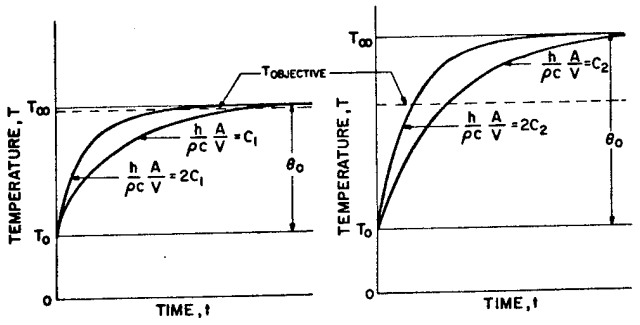
$\frac{A}{V}$ - the surface area to volume ratio, depends on the configuration of the object

t - the immersion time; at large times, the rate of change of temperature approaches zero.

Heating and Cooling of Printed Circuits

For the purpose of heating and cooling printed circuit product either for a manufacturing process and for test purposes, it is useful to discuss selection of parameters for the process, keeping in mind that excessive temperatures and time at temperature tend to degrade the dielectric. The latter constraint argues for a relatively rapid heating rate with good control of the peak temperatures reached. For a given object the volume specific heat, ρc, and the surface area to volume ratio, $\frac{A}{V}$, are fixed. The heat transfer coefficient, h, is characteristic of the heating environment which, within limits, may be suitably chosen. The initial temperature difference, θ_o, is also open to choice within allowable limits of the selected environment.

Figure 3 depicts two heating strategies that might be selected, individually or in combination. The asymptotic strategy of Figure 3a is attractive since



ASYMPTOTIC HEATING STRATEGY

EXCESS TEMPERATURE HEATING STRATEGY

FIGURE 3

it features excellent control of maximum temperature, even if the surface area to volume ratio changes drastically as it does when printed circuit product of differing thickness is processed. Also, the surface area to volume ratio and the volume specific heat may vary spatially due to a variety of components that may be attached to the board. A prerequisite for exercising the asymptotic strategy is the availability of a sufficiently high heat transfer coefficient in the heating environment to avoid excessive processing time which is costly and may be damaging to the dielectric. A heating environment may be considered in spite of its low heat transfer coefficient due to attractiveness from other considerations, such as low product contamination and fluid cost. In that case, one may resort to raising the fluid temperature substantially above the objective temperature (Figure 3b). In that way, rapid heating rates are achieved at the cost of simple object temperature control.

Table 2 gives typical values of ρc and V/A for three different multilayer printed circuit boards. The values of $(\rho c)_{av}$ are volume averaged from constituent properties. The value of V/A for a flat plate is approximately the half thickness. Table 3 gives typical values of heat transfer coefficients used in the processing and testing of printed circuit product, and the estimated time to reach a temperature change of 0.95 θ_o for three typical MLB configurations. Values of heat transfer coefficients for liquid solder, glycerol, condensing Freon E-5, a fluidized particulate bath, and forced hot air were measured between ambient and soldering temperature using a transient isothermal calorimeter. The other two values are text book estimates. The range of times estimated from Newtonian heating/cooling to reach a temperature change of 0.95 θ_o for the 16 layer MLB in the environments is about 3 seconds to 2100 seconds. The thermal response is quite rapid except for the air and radiant heating environments. Limitations of the Newtonian heating/cooling model are discussed in the next section.

MATERIALS

	COPPER	EPOXY-RESIN	GLASS
$\rho \cdot c$	50.9	36.8	31.2

MULTILAYER BOARDS

No. of Layers	$x = \frac{1}{2}\frac{V}{A}$ mil	$(\rho \cdot c)_{av}$
5	42	~35.5
10	60	~36.5
16	60	~38.9

TABLE 2

Typical Values for Volume Averaged Specific Heat, $\rho \cdot c$ Btu/cu-ft.F, of Selected Materials and Multilayer Boards

Region of Validity of Newtonian Heating Model

The intrinsic assumption to the Newtonian heating model is that internal temperature gradients in the heated object are relatively small. A parameter which is indicative of the magnitude of gradients to be expected is the Biot number, Bi. For a flat plate the Biot number is given by:

$$Bi = \frac{h}{k} x$$

FLUID	Measured Heat Transfer Coefficient h Btu/hr.sq-ft.F	5 Layer Board 0.95 θ	10 Layer Board 0.95 θ	16 Layer Board 0.95 θ	Average Times From Infinite Series Solution (Figure 4)
MOLTEN SOLDER	~750	1.78	2.63	2.80	9.6
GLYCEROL	~125	10.72	15.78	16.8	26
CONDENSING FREON E-5	~90	14.89	21.92	23.3	N.A.
FLUIDIZED BATH	~75	17.87	26.31	28	37
FORCED HOT AIR	10-25	134-53.6	197-79	210-84	130
STILL AIR	~1*	1340	1974	2100	N.A.
RADIANT ENVIRONMENT	5-10*	268-134	395-197	420-210	N.A.

NOTE:

* Textbook values

TABLE 3

Calculated Values of Times, in Seconds, to Reach a Temperature Change of 0.95 θ_o ($\theta/\theta_o = 0.05$) for Three Typical MLBs (from the Newtonian Heating/Cooling Equation).

where h is the heat transfer coefficient of the fluid environment, k is the thermal conductivity and x is the half thickness of the plate, respectively. The Biot number can be considered as the ratio of the internal to external impedance to heat flow. As long as the Biot number is small compared to unity, Eq. (1) yields a good estimate of rate of temperature change. Table 4 lists Biot numbers for a flat plate of thermophysical properties similar to a 16 layer MLB of half thickness of 0.0625 inches. The small Biot number criterion is not met for the high heat transfer coefficient environments.

Molten Solder	10
Glycerol	1.7
Freon E-5	1.2
Fluidized Bath	1.0
Forced Hot Air	0.13-0.33
Still Air	0.01
Radiant Env.	0.07-0.14

TABLE 4

Typical Values of Biot Number, $Bi = \frac{h}{k} x$ for a 16-Layer MLB with a Total Thickness of 125 mil

Figure 4 is a plot of normalized surface and midpoint temperature versus time for four heating environments for a typical MLB, while Figure 5 is a similar plot of the normalized temperature differences between surface and midplane. The curves were generated by a computer evaluation of the infinite series solution of the Fourier heat conduction equation for the infinite plate with surface convection[1]. It is seen that substantial temperature differences exist during the early phases of the heating process, but as the plate approaches thermal equilibrium with the bath, these die out. A cross-comparison of Figures 4 and 5 shows that when $\frac{\theta}{\theta_o}$ is less than 0.1, the normalized temperature difference is less than 0.1.

Figure 6 shows a comparison of thermal response of a MLB immersed into a fluidized bath predicted from Newtonian heating/cooling and from the complete solution of the Fourier equation for the infinite flat plate with surface convection. $\frac{\theta_s}{\theta_o}$ and $\frac{\theta_m}{\theta_o}$ refers to the normalized surface and midplane temperature respectively as obtained from the complete solution. $\frac{\theta}{\theta_o}$ is the normalized temperature response from the Newtonian model as equilibrium is approached. This temperature lag is a function of Biot number, increasing with increasing Biot number.

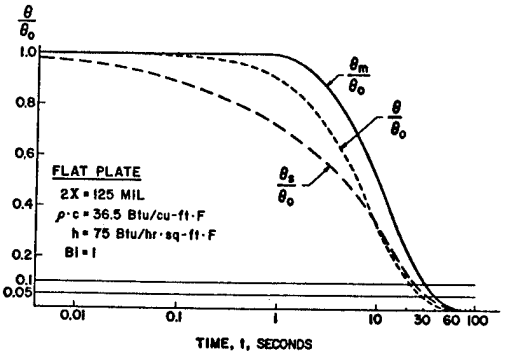


FIGURE 6

MLB thermal response in a fluidized bath from Newtonian heating/cooling, $\frac{\theta}{\theta_o}$, and from a complete solution of Fourier equation

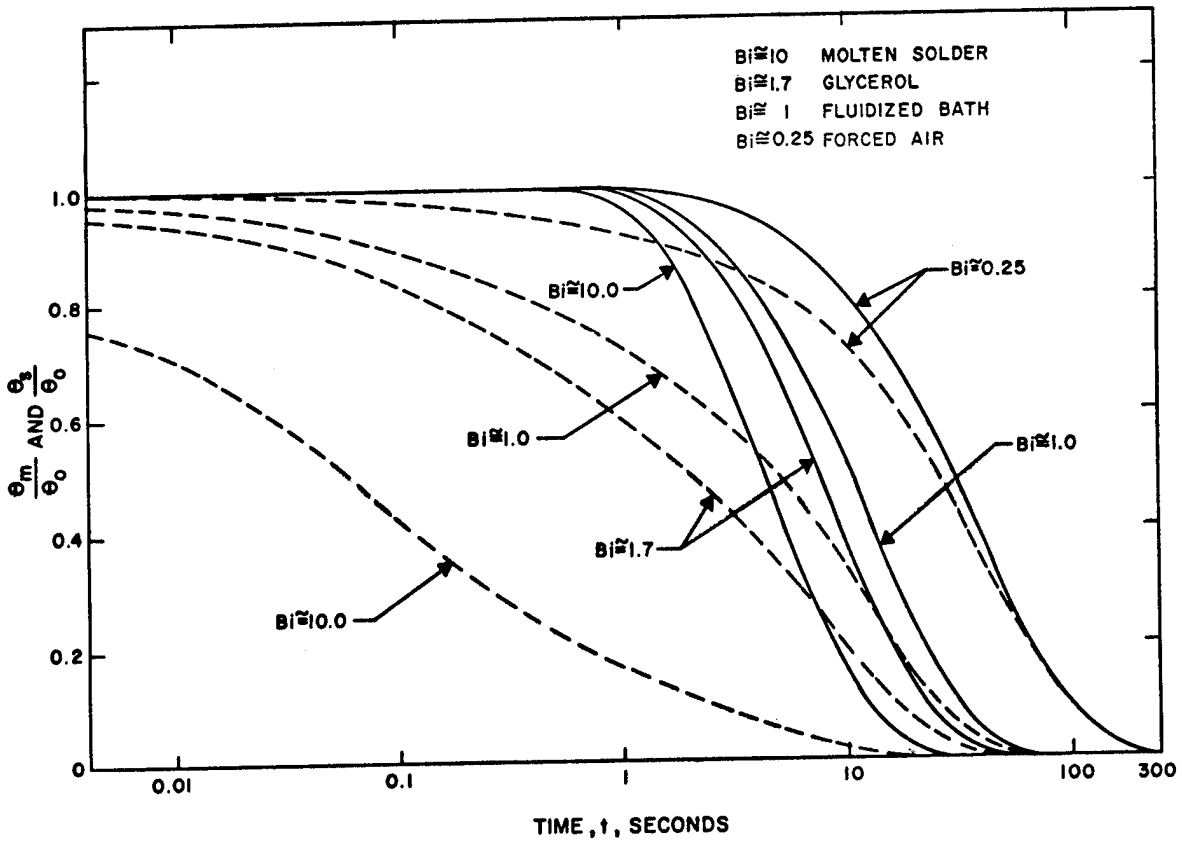


FIGURE 4

Normalized surface and midplane temperature versus time curves for an isotropic infinite plate with low thermal conductivity in different heating or cooling fluids. k = 0.365 Btu/hr.ft.F; ρc = 36.5 Btu/cu-ft.F; 2X = 0.125 inch Computer evaluation of the Fourier equation. Solid lines: θ_m/θ_o; Dotted lines: θ_s/θ_o

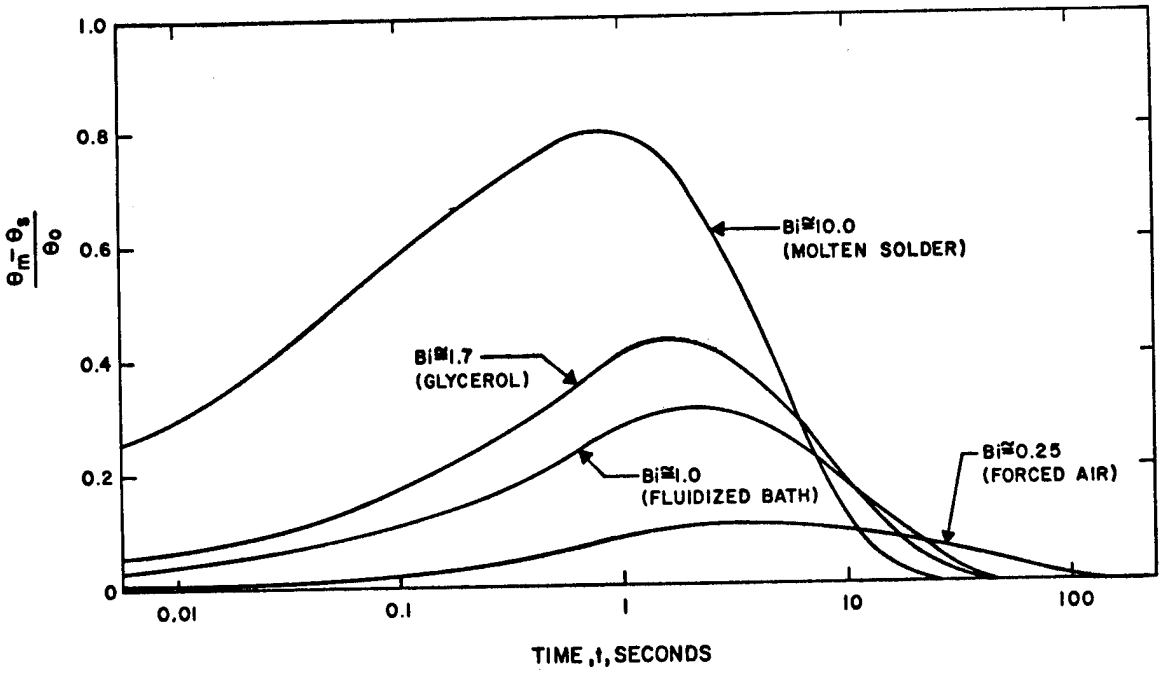


FIGURE 5

Normalized temperature differences between midplane and surface of above infinite plate.

Despite occurrence of substantial temperature gradients during the early phases of high Biot number heating processes, the asymptotic temperature/time history predicted by the Newtonian heating/cooling model is a good engineering approximation, especially for Biot numbers less than or equal to unity.

Another assumption made in the Newtonian heating/cooling model is that the heat transfer coefficient is constant. Tests with the transient isothermal calorimeter showed that heat transfer coefficients in some environments were not strictly constant, but for engineering purposes one may assume them to be. Figure 7 shows the thermal response of the transient isothermal calorimeter in the tested environments. Indications about the constancy of the heat transfer coefficient may be deduced from these curves. The isothermal calorimeter consisted of a thermocouple instrumented thin copper plate such that worst case Biot number was less than 0.02 and the resulting normalized temperature differences $\frac{\theta_m - \theta_s}{\theta_o} < 0.01$.

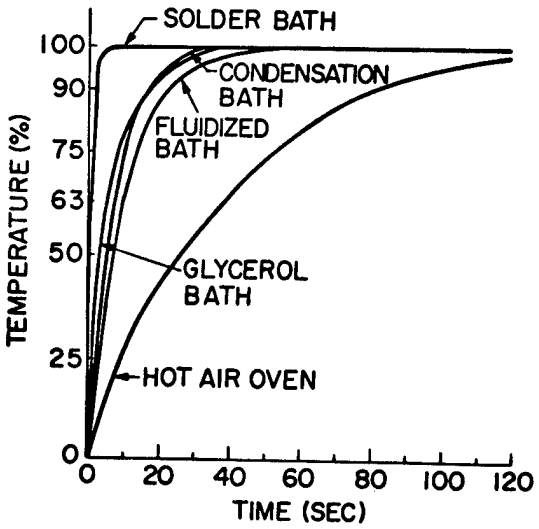


FIGURE 7

Transient thermal response of isothermal calorimeter in various heating environments.

Effect of Temperature Gradients on PTH Barrel Strain

As mentioned earlier, the transient and steady state contributions to barrel strain are subtractive during heating and additive during cooling. If we use an asymptotic strategy of heating, the worst strain applied is the steady state strain since the gradients die out as equilibrium is approached. During asymptotic cooling the strains are additive and high gradients may give an additional strain increment.

It can be shown, however, that among the worst circumstances, if the copper barrel temperature of 125 mil thick MLBs suddenly dropped from molten solder temperature to ambient, the barrel strain increment is of the order of 0.4%. This 0.4% strain is about 20% of the total barrel strain of ∿2% at soldering temperature[2,3]. Thus, its influence appears negligible. In the fluidized bath environment, in particular, the normalized temperature difference (Figure 5) is less than 40% of that assumed above, and the resulting strain increment is proportionally less.

Fluidized Bath Thermal Cyclers

Figure 8 shows the thermal cycling apparatus utilizing two fluidized baths and a cycling mechanism with appropriate logic circuitry to allow alternate immersion and dwell of test samples in one bath and then the other. The baths are set at temperatures to supply the desired failure mode specific stress stimulus of predetermined amplitude. Stability of thermophysical properties of the bath environment results in a usable temperature range by cold bath fluidization with liquid nitrogen boil off of -65°C to +300°C. Typical dwell time per bath is 60 seconds, which from Eq. (1) yields $\frac{\theta}{\theta_o} < 0.001$ for MLB test samples of 125 mil and less.

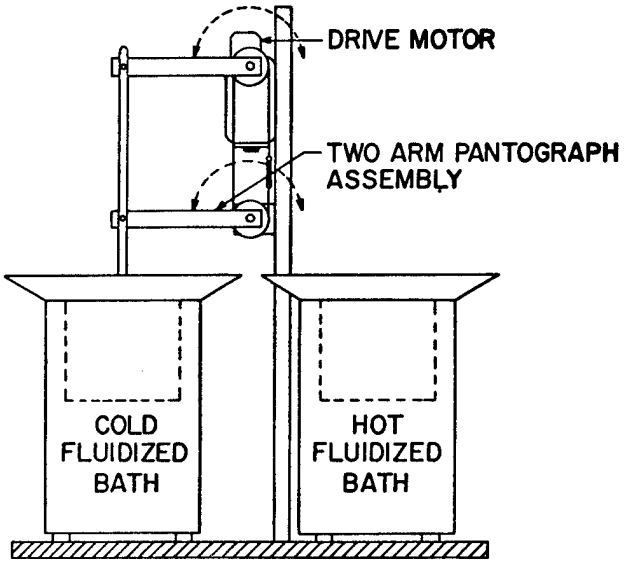


FIGURE 8

Fluidized Bath Thermal Cycler

Figure 9 shows a typical, measured, test coupon thermal response during cycling between fluidized baths operating at 25°C and 175°C. Coupon temperature was measured by using internal printed circuitry as a resistance thermometer. With 60 second dwell time (2 minute cycle period), the test coupon approaches to within 4°C of the hot bath and 2°C of the cold bath. Bath set points may be adjusted to compensate for these end point temperature differentials if desired. It should also be noted that the impressed temperature extremes are highly repeatable from cycle to cycle.

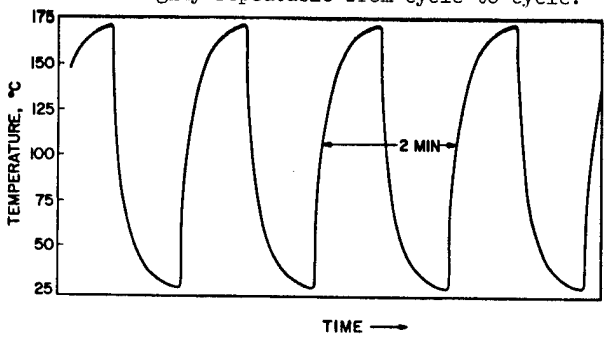


FIGURE 9

Typical test coupon temperature response in fluidized bath thermal-cyclers

Table 5 shows failure mode specific stress stimuli selected for an on-going study of low-cycle fatigue of barrel cracks and land to barrel interface cracks. Electrical readout of failure progression utilizing methods described by Rudy[4] and Hines[5] are employed.

Barrel Cracks Temperature Range (Upper Limit < T_G)	Land Rotation Temperature Range (Upper Limit > T_G)
-65°C to +85°C	25°C to 125°C
-25°C to +85°C	25°C to 143°C
0°C to 85°C	25°C to 175°C

TABLE 5

Selected Failure Mode Specific Stress Stimuli

Compared to typical cycle periods of several hours encountered in conventional thermal cycling chambers, the 2 minute cycle period of fluidized bath thermal cyclers allows a substantial compression of testing schedules. When simulating soldering transients in a fluidized bath (asymptotic strategy) a 60 second immersion results in a repeatable and characteristic stress stimulus for thick (125 mil) or thin MLB samples. In view of the primacy of the first solder transient discussed by Oien[2], this is important in end product quality assessment. The lack of contamination introduced during fluidized bath solder transient simulation, in comparison to solder or glycerol immersion, facilitates subsequent electrical readout of sample response. We have found the fluidized bath thermal cyclers to be useful for our activities concerned with end product quality assessment, reliability testing, and for evaluation of impact of design and process parameters on product reliability potential.

Acknowledgments

It is a pleasure to acknowledge the assistance of Messrs. W. H. Hewitt, R. W. Jocher, T. A. Early and R. J. Biola in the design, construction and characterization of the fluidized bath thermal cyclers.

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A Study of Dielectric Absorption in Capacitors by Thermally Stimulated Discharge (TSD) Tests

by

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Abstract

The dielectric absorption (DA) of capacitors with various dielectrics has been studied by the use of Thermally Stimulated Discharge (TSD). It has been shown that this test gives a much more accurate measurement of DA and in addition gives information about the mechanism of absorption. The charge determined by TSD has been correlated with noise which reduces the reliability of the capacitors in high gain circuits.

Introduction

Dielectric absorption is a term used to describe qualitatively the build-up of voltage across the terminals of an open circuited capacitor that has been charged to voltage, usually rated voltages, and momentarily discharged. An attempt has been made in specifying capacitors in the past to use a more quantitative measure of this parameter by specifying the recovery of the voltage at room temperature in terms of the percentage of the previous charging voltage. More recently the test has been extended by performing it at temperatures above room temperature since it is reasoned that some capacitors will be operated over a wide range of temperature.

These tests, as will be shown below, are next to useless because the voltage recovery will be a function of the previous history of the capacitor even including the manufacturing history of the dielectric such as the anodic oxide in a tantalum. What is not generally known is that the voltage recovery is a function of the complete previous thermal and applied voltage history of the capacitor and, in some cases, even of the dielectric film itself such as the procedure used in anodizing a film of tantalum electrolytic capacitors.

"Permanent" charge is used to describe the charge that will not discharge with a momentary room temperature short circuiting of the charged capacitor. If, however, the capacitor is short circuited at room temperature for a very long time the charge will decay and the measure of this time is established by a characteristic time constant defined as that required for the stored charge to decay to 1/e of its initial value which occurs when U = kT, where U is the activation energy for the particular mechanism responsible for polarizing the dielectric under the action of an electric field, k is Boltzman's constant and T is the temperature ^{o}K.

The charging and discharging mechanisms are complicated, involving both Maxwell-Wagner and Debye polarization as well as true space charge layers involving motions of either electrons and holes or ions and ion vacancies. These come into play at various temperatures and depend on the specific molecular structure, polymer structure (in polymeric dielectrics), crystal structure, grain structure (in ceramic dielectrics), domain structure (in ferroelectric materials), and on the donor and acceptor energy levels in a crystalline material which has substantial impurities (doping).

All dielectrics tested thus far show the ability to store charge by one or more of the mechanisms noted above and each shows a characteristic TSD (thermally stimulated discharge) curve. The curve of Figure 1 is a typical example for a Mylar capacitor. It is obtained by first charging the capacitor in a suitable way, discharging the fast charge, and then measuring the discharge current continuously as the capacitor is heated at approximately a $4^{o}C$/minute constant rate.

The area under the TSD curve, when the abscissa is time instead of temperature, gives a quantitative measure of the stored charge to the extent that the discharging is complete; but it should be emphasized that sometimes this entails heating the capacitor considerably in excess of its normal rated temperature, and thus it would only be done in some type of diagnostic or qualification testing in specific cases.

There are many critical applications of capacitors in which the stored charge has an adverse effect on an electronic system. Earth sensors for satellites represent one such system. Here charge transfer to the capacitor electrodes creates spurious signals. Long term precise timing circuits are

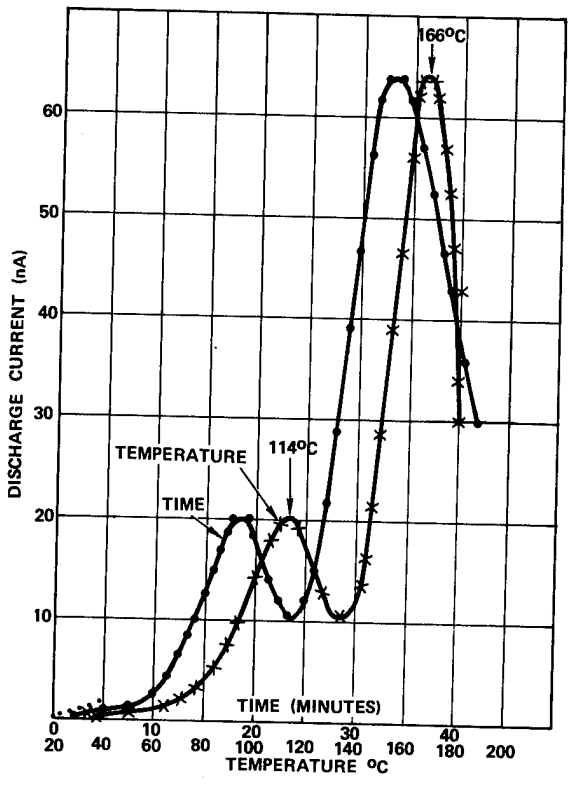

Figure 1. TSD for 0.33 μF 400-Volt Mylar Foil Capacitor Impregnated with Oil (Charged 1 Hour, 190 Volts at $175^{o}C$).

particularly affected when there is a wide temperature excursion. Cables have a distributed capacitance in which noise from stored charge can be triggered by mechanical and thermal stresses. Dielectric layers on ICs can get charged and cause them to malfunction. With the advent of very high gain amplifiers, dielectric noise can become a limiting circuit design factor. The safety hazard due to the dielectric absorption in high voltage capacitors is, of course, well known.

TSD curves are sensitive to moisture, variations in the dielectric material processing and composition and are thus of diagnostic value in failure analysis and manufacturing control. The effect of moisture and impurities in materials on the shape of the TSD spectrum promises to be a very simple and effective way to identify these variables. In the case of plastics the spectrum is sensitive to changes in crystallinity, mechanical stresses, and the presence of plasticizers.

In the past attempts to control the capacitor dielectric absorption (DA) characteristics in such critical applications have been confined to laborious and uncertain selection screening methods which are not only costly but ineffective. It is the purpose of this paper to show that relevant parameters can be measured quantitatively and can be controlled in a predictable way to greatly improve the reliability of these critical circuits.

Theory

The normal method of measuring dielectric absorption (DA) is illustrated in Figure 2 where the percent voltage rises in five minutes is given for a number of types of capacitors over the range of 25 to 125°C. There is no apparent regularity to the DA and the inorganic materials, particularly mica, which has been considered near to an ideal type of dielectric appears to be worse than the polymeric film types using Mylar,* polycarbonate and Paralene.**

It will become obvious that the curves in Figure 2 have no fundamental significance if one considers the simple case of Mylar. When a DA test is done at various temperatures, for example, a different result will be obtained depending on whether the tests start at the low end or the high end of the range. This illustrates that this measurement is extremely sensitive to the thermal-charge history of the capacitor. Results even at the same temperature will differ when the sequence of heating, cooling, and polarization is varied. These facts simply illustrate that the phenomenon is a complex one and, unless the molecular mechanisms of polarization and charge transfer in dielectrics under a nonisothermal condition with an applied field are understood, no true progress can be made in controlling DA from a component engineering point of view.

It is a surprising fact, for example, that if a Mylar capacitor is charged to obtain the maximum permanently stored charge at rated voltage and 125°C for one hour (longer times at this temperature produces a negligible increment) by TSD test to 150°C, the charge drained is two to three times that which one obtains from the familiar equation Q = CV, where V is the charging voltage and C is the 1 KHz value of capacitance. Thus, if we define DA by a figure of merit Q/Q_{Theo} where Q_{Theo} is the value

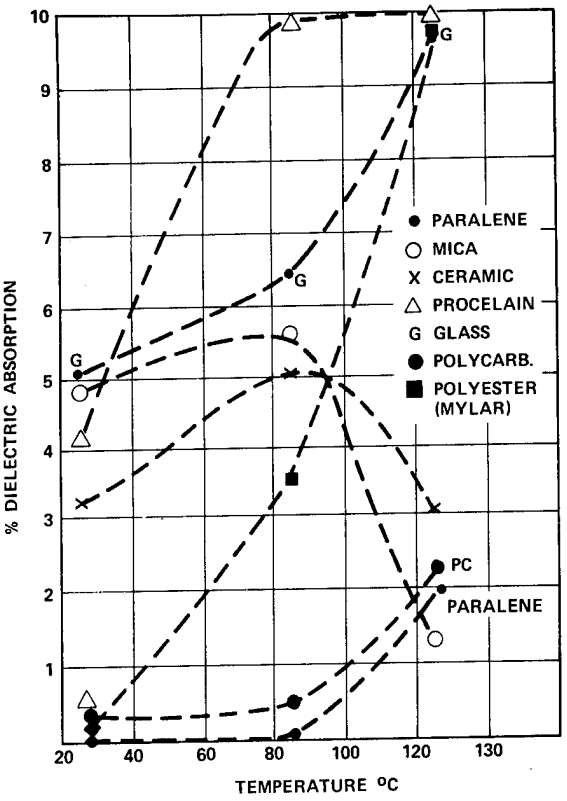

Figure 2. Standard Dielectric Absorption Curves for Different Types of Capacitors.

noted above, we get a DA of perhaps 300 percent instead of 0.3 percent as Figure 2 indicates, or a difference of 1000 to 1!

The charge drained by a correctly designed TSD test thus is a quantitative method of measuring all the permanently stored charge. How this stored charge is going to affect the circuit in which the capacitor is applied depends on the circuit design and the environment under which the circuit operates. The decay of this charge and its influence on the external circuit depend on the instantaneous dQ/dt during rapid temperature changes.

The theory of nonisothermal discharging of dielectrics and electrets has been developed by Bucci et al[1] and a summary is given by Perlman.[2] This can be applied to capacitors with polymeric film dielectrics and for the purpose of this paper it is unimportant whether films have vapor metallized electrodes or Al foil, or even whether they are liquid impregnated. This is, however, not to say that the complicated mechanisms of charging and discharging are not affected by these factors in construction.

In the case of a polar dielectric material like Mylar, the discharge current from the TSD while heating at β°C/minute is given by (1)

$$I(T) = \left[\frac{N\mu^2 E_p}{3\,kT_p\,\tau(T)}\right] \exp\left(-1/\beta \int_T^{T_2} \frac{dT}{\tau(T)}\right) \quad (1)$$

Thus the current is a linear function of the electric field Ep and the temperature Tp at which the capacitor (film) was polarized during the charging. (All

*Mylar Du Pont TDM
**Paralene UCC TM

T's are temperature.) The dipole moment of the orientable dipoles is μ and the number of dipoles/cc is N. The relaxation time of the dipole is τ and it is a function of temperature. Boltzman's constant is the usual k.

The relaxation time constant is that characteristic of dipole reorientation and is given by (2)

$$\tau(T) = \tau_o \exp(U/kT) \qquad (2)$$

where U is the activation energy to affect the reorientation.

One of the distinctive features of TSD curves is the presence of various peaks which occur at specific temperatures, given by (3)

$$T_{mx} = \left(\beta \frac{U\tau(T_{mx})}{k}\right)^{1/2} \qquad (3)$$

It is clear that the temperature at which the discharge current maximum occurs is independent of the temperature at which the capacitor was charged and the electric field used, but depends on the rate of heating and the heat of activation with a square root dependence. The number of peaks appearing depends on the various ways in which dipoles can relax involving different polymer chain motions.

Experimental

All TSD runs were made on capacitors by heating them at approximately 4°C/minute while shorted through an HP425 $\mu\mu$ammetter. The current and temperature were recorded simultaneously on a X-Y recorder using thermocouple output on the X-coordinate. The meter scales were switched during the run to obtain the best sensitivity, hence there were discontinuities in the actual current temperature plots. These were rectified by redrawing the curve on a uniform coordinate scale and the curves presented in this report are therefore handdrawn from the graph on the data obtained at about 10°C intervals.

Figure 3 shows a TSD of a 0.33 μF, 200-volt Mylar capacitor which was charged to 200 volts at 125°C for one hour and cooled while at 200 volts to room temperature. The current shows a characteristic peak at about 80°C and it goes through a minimum at 107°C and rises again to a large current as the 160°C terminating temperature is approached. Referring to Equation (3), the peak which is fairly well isolated is associated with the glass transition temperatures of Mylar and the position at 80°C agrees well with Tg obtained for Mylar at low frequencies. The energy of activation can be derived from a plot of the log of the discharge current versus temperature for the rising side of the current peak and a value of 3.4 eV is obtained in fair agreement with that obtained from dc conductivity measurements.

Figure 4 compares two different capacitors of the same rating as that used in Figure 3 which had been drained of charge as completely as possible, and subsequently were given a TSD after charging 112 hours at 30 volts and 38°C. Both capacitors show close agreement in their thermal discharge spectrum. The essential features are the presence of a peak at about 80°C showing a positive polarization and a negative stored charge comprising about 20 percent of the total with a maxima at 140°C. The total charge is small compared to a fully polarized unit which reflects both the fact that the polarizing temperature is well below the glass transition and the electric field is only 15 percent of the rated value.

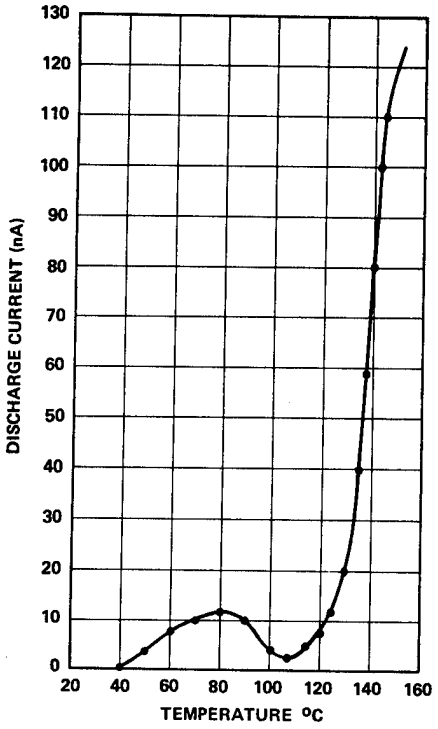

Figure 3. TSD for a 0.33 μF 200-Volt Mylar Capacitor Impregnated with Oil (Charged 1 Hour, 200 Volts at 125°C).

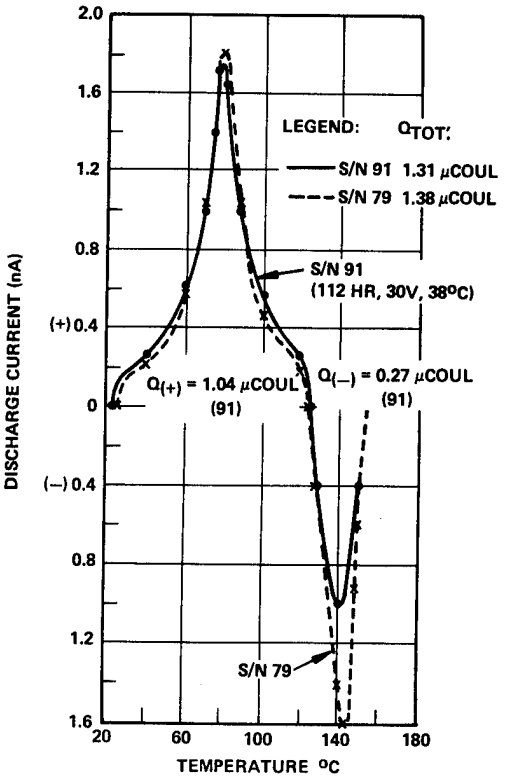

Figure 4. Comparison of TSD Thermal Spectra for Two Mylar Capacitors (Charged 112 Hours, 30 Volts at 38°C After Completely Draining Stored Charge of 0.33 μF, 200 Volts).

Although the rated voltage has been used to fix the theoretical value of Q in the relation Q = CV it is clear that the significant parameter is E or V/d, where d is the dielectric thickness and since the stored charge is also a function of E as seen from Equation (1), one should define the dielectric absorption in terms of the maximum E that can be sustained without breakdown. As a practical matter we have found that the dielectric absorption of different capacitors should be established at the maximum electric stress and temperature the capacitor is apt to see during its manufacture and acceptance testing.

Charging under different wave forms produces variable amounts of stored charges. Figure 5 compares the same unit charged 95 hours at ±280V with a squarewave one minute wide and a one-hour charge at 200 volts at 125°C. The latter gives 162 μC, whereas, the former gives 12.8 μC with the second peak accounting for the bulk of the stored charge.

A comparison of the stored charge in the other polymer film dielectric capacitors shown in Figure 2 illustrates the role that the glass transition temperature plays in DA. A polycarbonate capacitor containing the stored charge which it had on receipt from the manufacturer is shown in Figure 6. It has a thermal peak at about 128° which agrees with the glass transition temperature for this film and explains the lower apparent DA in Figure 2 at the high temperature of 100°C, but the value at room temperature as can be seen is not particularly different. Correspondingly, the stored charge from a Paralene capacitor is shown in Figure 7. The total stored charge here measured to 160°C shows only 0.018 μC, and again at 100°C is qualitatively less than polycarbonate. These two capacitors have, however, not been fully charged.

Figure 8 is a TSD of the polycarbonate capacitor shown in Figure 5 which was completely discharged and has decreased from 89 μC to 0.75 μC or by a factor of 118. Thus in the fully charged condition the polycarbonate capacitor has a charge comparable to Mylar.

Polysulfone capacitors have also been given a TSD test. Figure 9 represents such a test on a

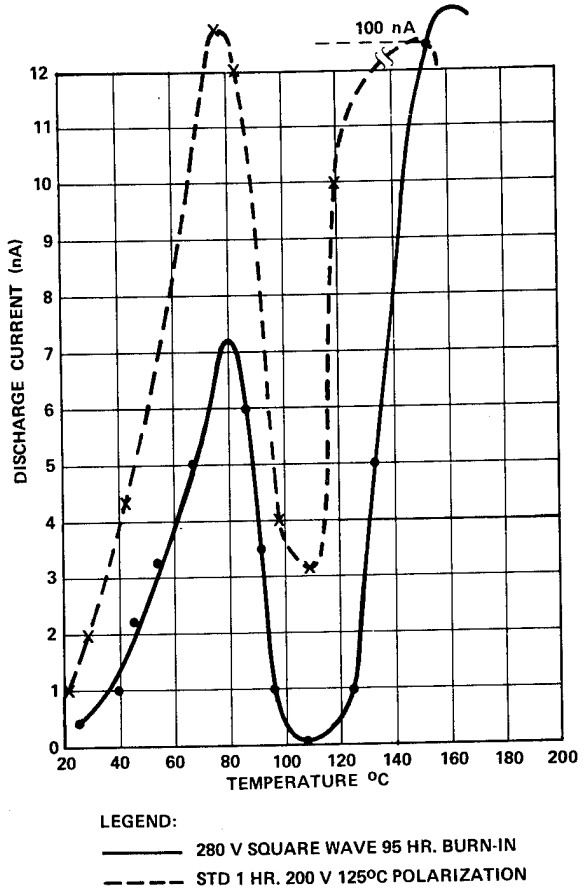

Figure 5. TSD for a 0.33 μF 200-Volt Mylar Capacitor Under Different Charging Conditions (S/N 4).

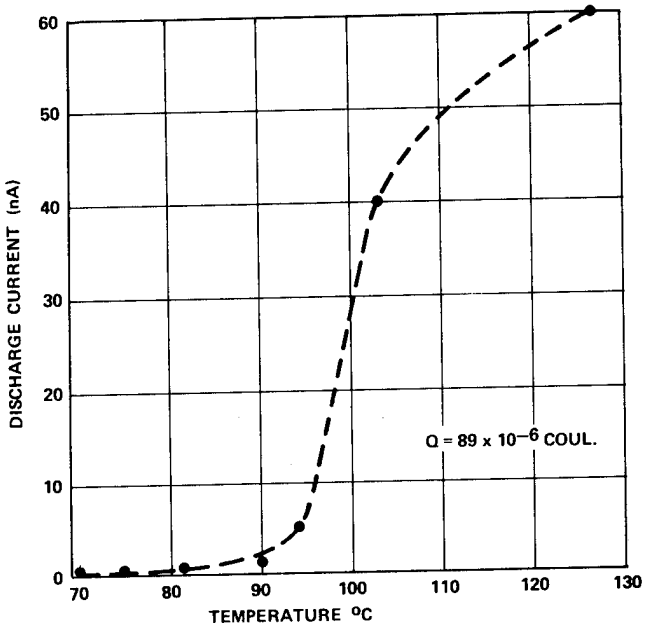

Figure 6. TSD for a 0.33 μF 200-Volt Polycarbonate Capacitor (Charged 1 Hour, 200 Volts at 125°C, Cooled (Forced) for 20 Minutes).

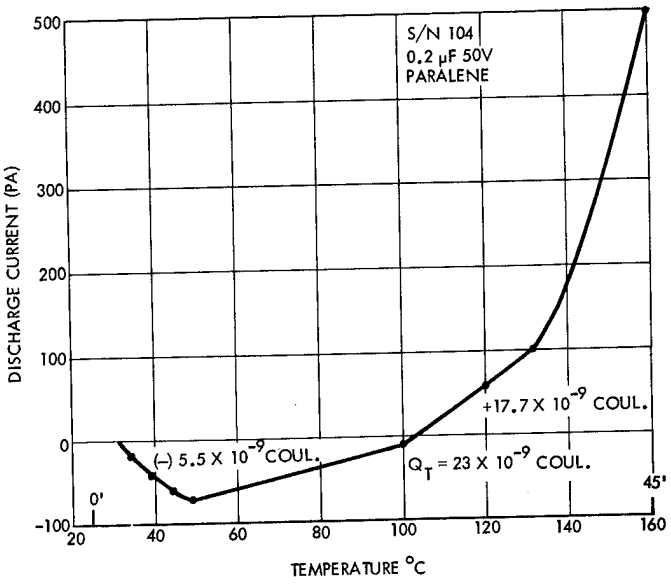

Figure 7. TSD for a 0.2 μF 50-Volt Paralene Capacitor (Charged 1 Hour, 50 Volts at 125°C).

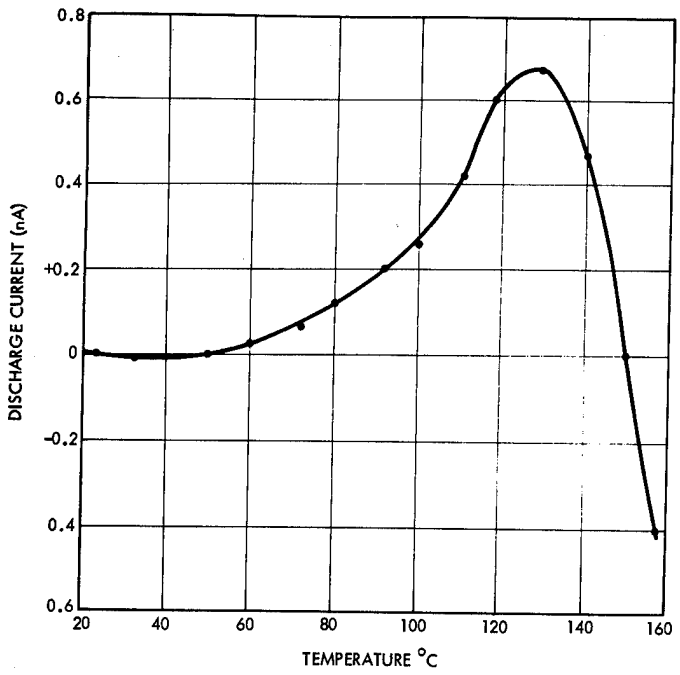

Figure 8. TSD Curve for 0.33 μF 200-Volt Polycarbonate Capacitor; Q = 0.75 μC (S/N 40).

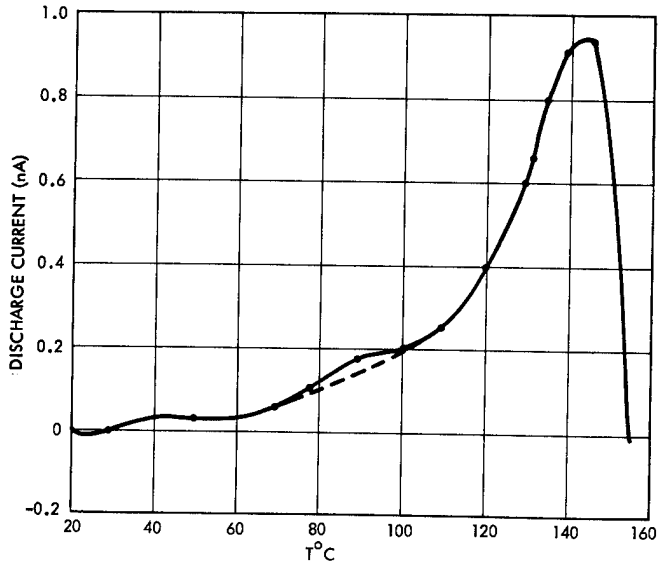

Figure 9. TSD for 0.33 μF 200-Volt Polysulfone Capacitor After Squarewave Charge and "Glitch Test" (Q_T = 0.404 μC).

0.33 μF 200-volt unit from CRC.* This has been given a squarewave charge of 93 hours at 0.008 Hz and then polarized in a test circuit at 15 volts during a noise test. The stored charge is only 0.404 μC after this charging history.

The polysulfone has a more complicated spectrum indicating several molecular chain motions correlated with the charge release. No attempt has been made in this work to identify these. The main peak, however, is at about 140°C similar to the polycarbonate.

*CRC (Component Research Corp.)

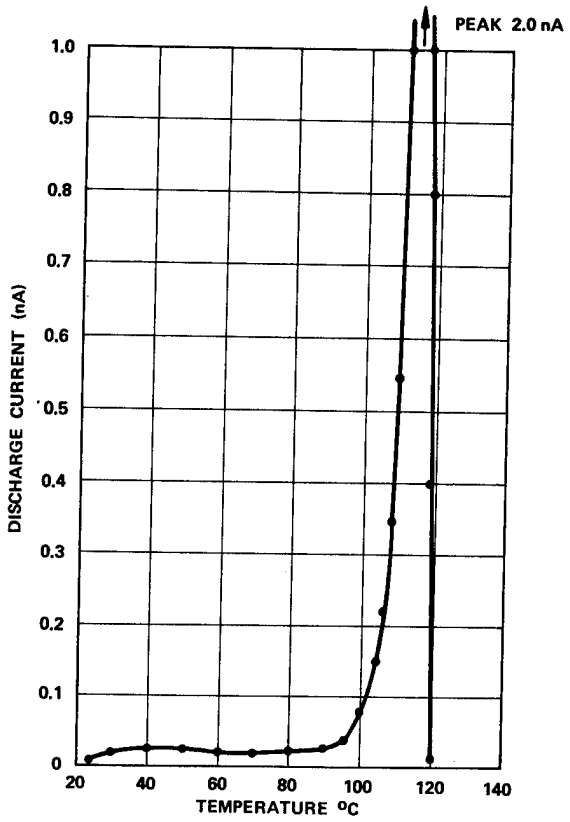

Figure 10. TSD of a 0.1 μF 200-Volt Polystyrene Capacitor (Charge 1 Hour, 100 Volts at 100°C, Q = 0.7 μC).

A 0.1 μF 200 volt polystyrene capacitor was charged to 200 volts at 100°C for one hour and given a TSD test with the result shown in Figure 10. As is well known, the linear chain-type polystyrene begins to soften at 90°C but it was heated to 120°C to fully discharge it. It can be observed that a very significant thermal peak occurs at 115°C corresponding to the motion of charge carriers, very likely ionic impurities. The broad peak at 42°C indicates some sort of chain segment motion since polystrene is not completely devoid of a dipole moment.

Metallized teflon film capacitors were charged to 200 volts at 125°C for 162 hours and produced the TSD spectra shown in Figures 11 and 12. Two units are shown because they have significantly different spectra even though they were from the same lot of capacitors. The unit in Figure 11 shows both negative and positive charge with the majority being (-). There are also thermal peaks of both polarities. The total charge is only 0.007 μC and is the smallest value obtained on any dielectric tested. The unit of Figure 12 has two orders of magnitude greater charge and is for the most part positive. This comparison illustrates the effect of impurities on the TSD and the capacitor S/N 76 actually produced spike noise in a sensitive amplifier, whereas, S/N 81 did not. This illustrates sensitivity of the total stored charge test compared to the standard DA test which in these capacitors shows no difference at all. The surprising thing is that even with a stored charge of 0.7 μC "dielectric" noise can be observed in the teflon capacitors. Obviously, here the signal-to-noise ratio is the critical factor.

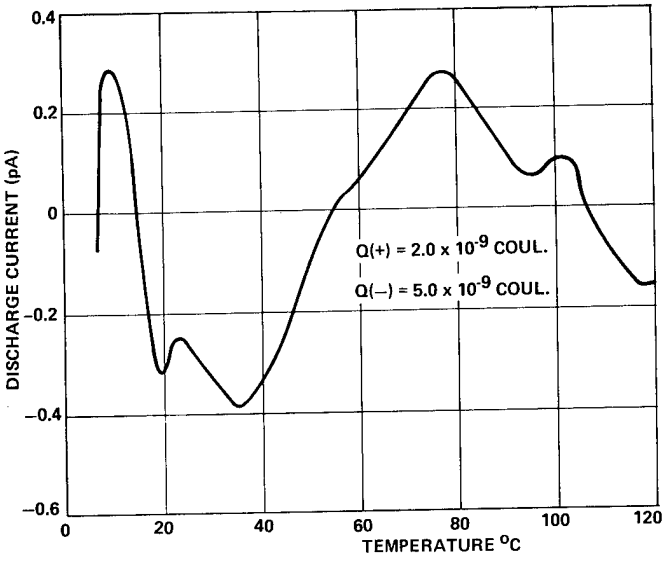

Figure 11. TSD Thermal Spectrum for a Metallized Teflon Capacitor (Q_T = 7 x 10^{-9} coul, S/N 81).

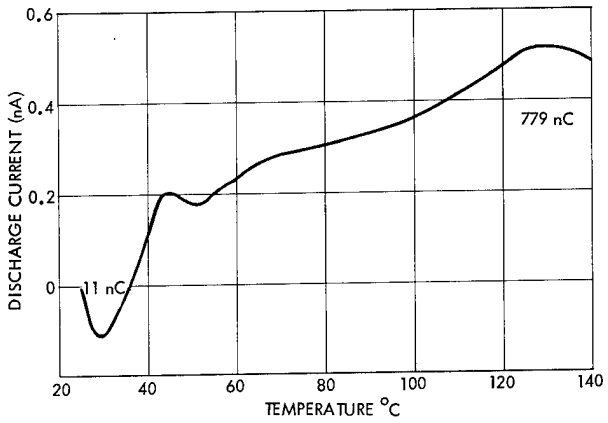

Figure 12. TSD for 0.33 μF 200-Volt Teflon Capacitor (Charged 162 Hours, 200 Volts at 125°C; Cooled 68 Hours + 200 Volts; S/N 76).

DA of tantalum electrolytic capacitors has also been shown to exist in "wet" and so-called "solid" capacitors. Figure 13 is a TSD for a solid 6.8 μF 75-volt Ta electrolytic comparing the "as received" unit with the same unit after charging. The current on the as-is unit is rising to a peak at about 150°C, and when the same unit is charged 1 hour at 125°C and 50 volts the TSD is much higher giving a subsidiary peak at 114°C. The total stored charge is 55 μC for the charged and 11 μC "as is," and in an attempt to drain the charge completely the unit had to be heated to 200°C to reduce it to 0.92 μC. One peculiar thing about the solid Ta capacitor is that a repetition of the TSD to 150°C without intermediate charging always resulted in about 12 percent of the stored charge remaining (based on the fully charged condition). If we compare the fully charged case (125°C, 50 volts) with the Q_{Theo}, we find the former to be only 16 percent of the latter. This is contrasted to Mylar, for example, where the percentage can be as high as 300 percent. In this sense, Ta solids have a relatively smaller dielectric absorption than Mylar capacitors. This is even more significant than it appears because the electric stress (charging) on the tantalums is 3 to 10 times higher.

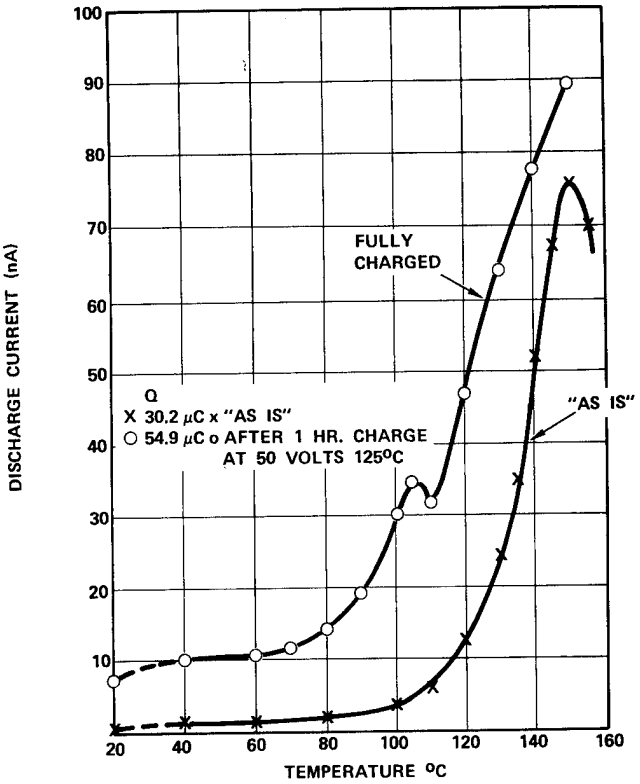

Figure 13. TSD for a 6.8 μF 75-Volt Solid Tantalum Electrolytic Capacitor.

A comparison of a "wet" and a "solid" is also interesting. As shown in Figure 14, a 66 μF "wet" was charged to 50 volts at 125°C and gave a TSD with a very monotonic current rise to 150°C with only a small broad peak at 64°C. The stored charge was 1440 μC. This compared to 443 μC as received and 15.5 μC after draining at 175°C for one hour. It is significant that the discharge current in this case reached as much as 1.7 μA at 150°C. The theoretical fast charge on such a unit is 66 x 50 x 10^{-6} or 3300 μC, thus the stored charged unit in this instance is 44 percent and the best charge free state is 0.5 percent of the Q_{Theo}.

As we noted in Equation (1), the polarization is linearly related to the stress and we can test this dependence in comparing the "wet" and the "solid." The comparative data is shown in Table 1.

If we normalize the stored charge for both capacitance and polarizing field, we see that the solid has 6.08 μC/μF of stored charge and the "wet"

TABLE 1

Comparison of Ta_2O_5 Parameters for 6.8 μF, 75V Solid and a 66 μF, 50V "Wet" Tantalum Electrolytic

Type	Capacitance	Stored Charge at 50V, 125°C	Estimated Electric Field During Charge
Solid	6.8 μF	55 μC	1 x 10^6 V/cm
Wet	66.0 μF	1440 μC	3.3 x 10^6 V/cm

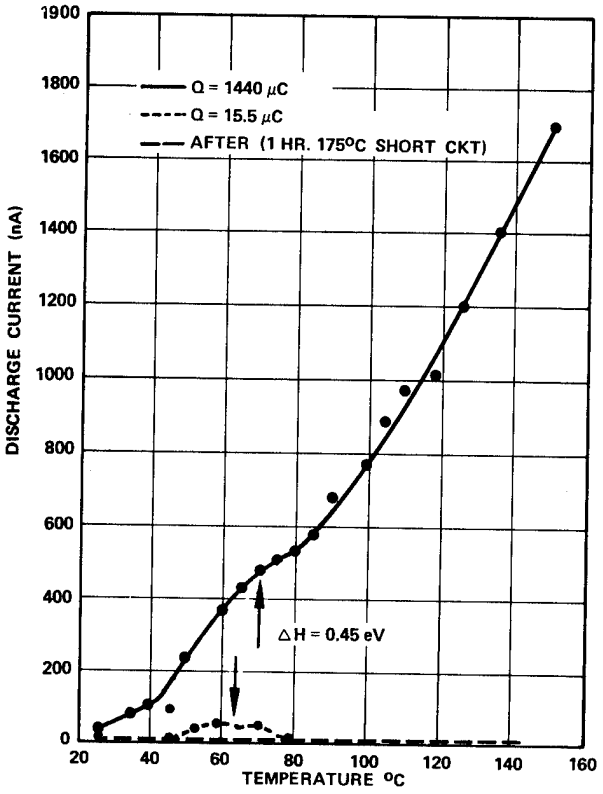

Figure 14. TSD of All-Tantalum Wet Electrolytic Capacitor (Charged 1 Hour, 50 Volts at 125°C, S/N 121).

has 21.8 x 1.0/3.3 (i.e., 6.6 μC/μF). Notwithstanding the difference in electrolyte and capacitor design the stored charge agrees to about 10 percent. Thus we can conclude that the stored charge is a bulk effect in the oxide and not associated with a thin interfacial film. It also suggests the electrolyte-oxide interface does not play any special role in the dielectric polarization of this type of capacitor. One can derive an activation energy as noted by Bucci and a value of 0.45 eV is obtained.

The interpretation of the mechanism of charging in the case of the inorganic solid Ta_2O_5 is, of course, different from that of the organic polymer film. There are virtual dipoles due to ion or ion vacancy motions whose net effect is to result in dipoles changing direction. The mechanism proposed by Avis, et al[4] cannot be the one involved here because it occurs at about 450°K and the dipole concentration is orders of magnitude higher.

Monolithic Hi K ceramic capacitors have also been shown to have a significant amount of stored charge in this study. A 0.13 μF 100 volt chip has been charged at 90 volts at three different temperatures from 30 to 160°C in order to span the Curie point. The TSD for these charge conditions are shown in Figure 15. These curves have been plotted versus time, but they are thermal spectra and the peaks have been indicated.

The 160°C charge curve shows a stored charge of 9.27 μC which is 70 percent of the theoretical. It shows two maxima, one at 108°C and the other at 164°C. The former represents the alignment, in the field, of the ferroelectric domains and the latter a dipole motion involving ion and vacancy hops similar to that of crystals with defects. In this case, ion space charges at grain boundaries can also be

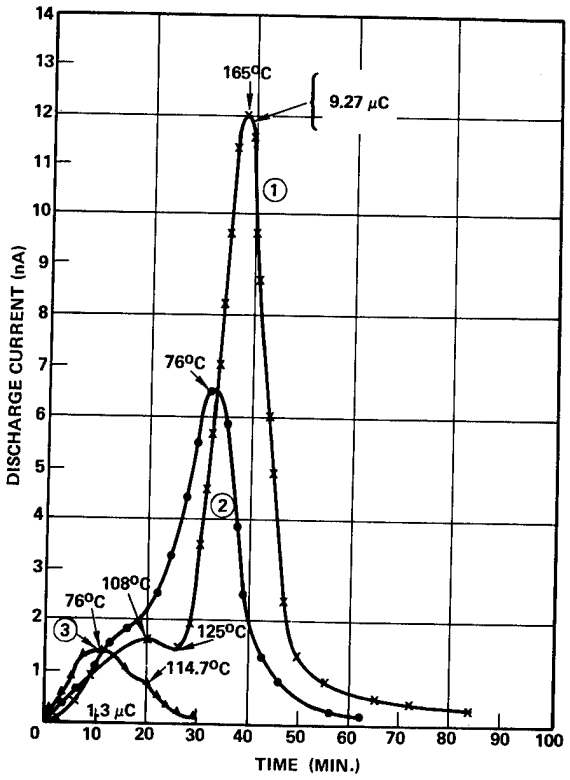

Figure 15. TSD Tests of Ceramic Chip Capacitors.

involved which amounts to a Maxwell-Wagner type of polarization. When the polarizing is done below the Curie point, the ferroelectric domains are oriented to various degrees depending on the polarizing temperature.

Another type of capacitor which has been studied by TSD is a resin impregnated Mica paper. It was expected that this type would show the polarization due to the polymer material involving organic dipole relation, Maxwell-Wagner polarization at the boundaries of the microcrystals. Figure 16 is a TSD of a typical polyester impregnated mica resin which has several interesting features. This capacitor was charged at only 27V/mil (10.5 kV/cm), but nevertheless shows a DA of 670 percent (Q/Q_{Theo}). The rising portion of the TSD also gives an activation energy of 1.12 eV for this particular type of polarization.

Application of Capacitor TSD Data

The quantitative measure of stored charge provides a method for designing capacitors suitable for very high gain amplifiers such as used in earth sensors for accurately pointing antennas on a communication satellite. It was established that a stored charge in a 0.33 μF 200-volt capacitor, whether of Mylar or polycarbonate, would create transient voltage spikes of 10 to 300 μV amplitudes during the thermal cycling of the sensor. This was correlated with a high stored charge which was found to be in the range of 20 to 150 μC depending on the capacitor history. When the charge was drained by a TSD test and reduced below about 1 μC, the spikes were either eliminated or showed negligible amplitude.

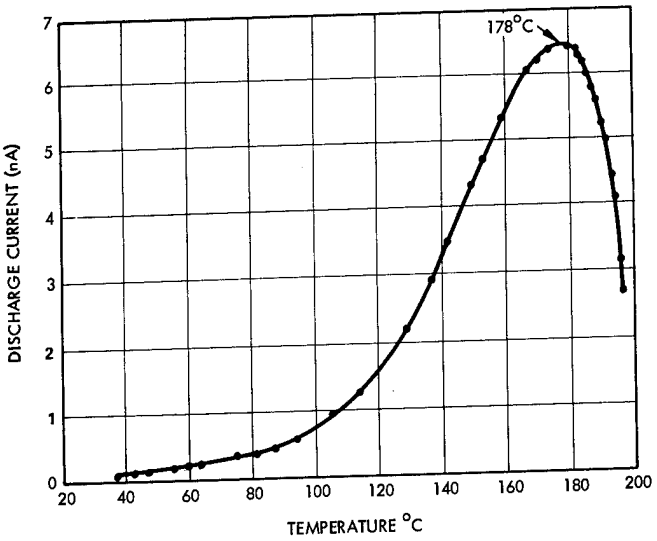

Figure 16. TSD for Resin Impregnated Mica Paper Capacitor (Charge 1 Hour, 190 Volts at 195°C; 0.0125 μF, 9 kV).

It was further determined that the stored charge was acquired by the capacitor during use. Figure 17 shows the rate of charge accumulation. Capacitor S/N 55 showed that at 120V/mil and 38°C it accumulated about 1 μC every two decades of time, and having established that 4 μC represented a threshold value for producing these transients, it could be readily predicted that the capacitor would remain noise free for at least seven years (the life time required). In contrast to S/N 55 it was shown that S/N 1 operated at 3.3 times the voltage which would be expected to produce transients after about 50 hours of operation.

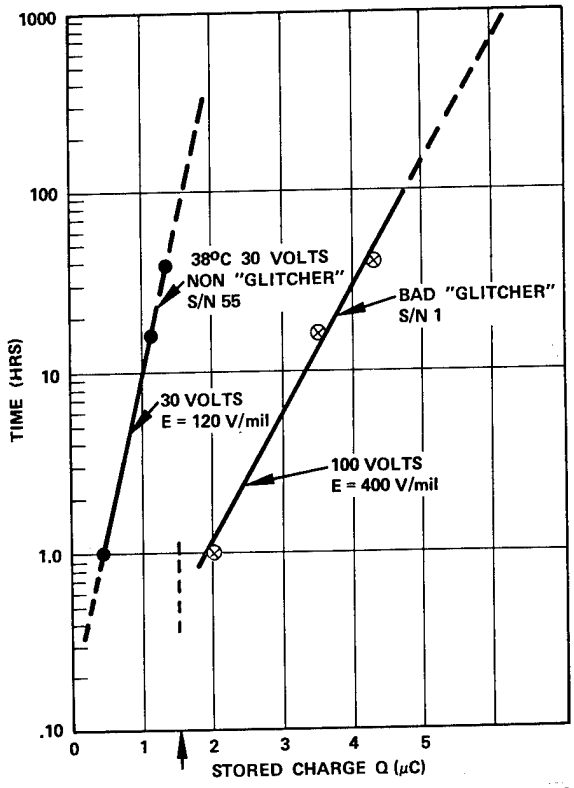

Figure 17. Stored Charge Build Up at 40°C ± 2°C, 100 Volts on 0.33 μF, 200-Volt Mylar Capacitor.

Comparison of Different Capacitors

Although the absolute maximum stored charge has not been determined for each type of capacitor discussed in this study, a useful list has been compiled which shows the relative true quantitative dielectric absorption in Table 2 when each capacitor is charged for one hour at 125°C at rated (or derated) voltage.

TABLE 2

Comparative Values of Quantitative Dielectric Absorption in Capacitors With Different Dielectrics

Number	Type of Capacitor	Stored Charge Percent of CxV Rating	Electric Stress Approximate kv/cm
1	Mylar	300	320
2	Polyvinyledene Fluoride	173	570
3	Polycarbonate	100	280
4	Solid Ta	100	1000
5	Wet Ta	100	3000
6	HiK	70	20
7	Mica Paper	670	10.4
8	Polysulfone	10	250
9	Polypropylene	3	290
10	Polystyrene	0.1	120
11	Teflon	0.1	200
12	Paralene	0.05	160

Discussion

It is evident that all dielectrics used in capacitors can store charge permanently. The method that has been in vogue to provide a figure of merit for this parameter called "dielectric absorption" is totally inadequate and is, in fact, misleading when a nonisothermal condition exists in the application. Since this is nearly always true in the majority of cases, this method should be discarded in favor of a TSD test prescribed under controlled discharging conditions and preceded by a well defined method of charging which realistically reflects the environmental conditions of test and use.

TSD tests not only accurately measure the quantity of stored charge, but provide information about the previous charging history. Any variations in the thermal current spectrum can also be used to identify material and process variations which will be of diagnostic value for analysis of failed parts to provide feedback for better manufacturing controls. The presence of moisture, for example, can be detected.[6]

An accurate measure of stored charge makes it possible to control certain types of dielectric noise in very sensitive circuits. However, it has been found that although the amount of stored charge is a necessary condition for creating dielectric noise there are piezoelectric and pyroelectric sources of

noise which are not easily distinguished from this and may, in fact, induce the transfer of stored charge from the dielectric to the capacitor electrodes. The capacitor may be subjected to thermal stresses, for example, under changing temperatures; and if the dielectric is piezoelectric a voltage will be generated which will alter the stored space charge.

The TSD method of measuring stored charge is applicable to all dielectrics but the correct charging conditions are not always easily defined. For plastic film dielectrics the correct charging temperature is approximately 25° above the glass transition temperature (T_g). But it should be noted that there may be one or more molecular mechanisms for dipole relaxation involving different atomic groups which rotate separately or in cooperation with the motion of chain segments, thus it is the highest T_g which is of consequence.

Most plastic films, whether polar or not, have a thermal current peak associated with ions which have higher diffusional activation energies. Thus Mylar in the capacitor (in Figure 1) showed an activation energy for the 164°C peak of 3.39 eV which is in agreement with Amborski's[7] value of 3.43 eV for dc conduction activation in the amorphous film. The ion activation peak thus can be said to be associated with the amorphous part of the film. Strictly speaking, the T_g of Mylar is characteristic of the amorphous regions. Ion movement, however, also occurs in the crystalline regions and for these the activation energy is 1.64 eV according to Amborski. A value found for a Mylar capacitor for the 44°C peak is 1.77 eV which would seem to be correlated to this portion of the film.

The method of charging the capacitor as already noted is of particular significance. A Mylar capacitor (S/N 13) shown in Figure 18 which was charged with a 285 volt squarewave at 0.016 Hz shows both a positive and a negative charge about equally divided and a total of 11.2 μC. Under the standard 1 hour 125°C dc charge, the same capacitor had a stored charge of 124 μC.

Ceramic capacitors, as noted in Figure 15, show a thermal peak at about 165°C. This temperature is well in excess of the Curie temperature and, therefore, cannot be due to domain orientation. It can be ascribed to a virtual dipole in the ionic lattice of crystal grains or to a Maxwell-Wagner type of relaxation. The activation energy has been found to be 1.67 eV. If it is interfacial polarization it would, no doubt, occur in the grain boundaries of the polycrystalline ceramic. A comparison of the activation energy for dc conductivity which is approximately 2.0 eV suggests that the activation corresponds to migration of ions to the grain interfaces and the stored charge is actually a double layer space charge localized at the grain boundaries.

As already noted, the solid and wet tantalum electrolytic capacitors show a common activation energy which proves that the stored charge is due to ion improvement in the bulk oxide. It is, of course, possible that in this case the activation energy is simply the energy required for electrons to escape a trap of 0.43 eV depth. It is, however, not a surface state; the activation energy is the same with both a solid semiconducting electrolyte as well as with a wet sulfuric acid electrolyte.

The appearance of noise spikes from Mylar capacitors was definitely correlated with the magnitude

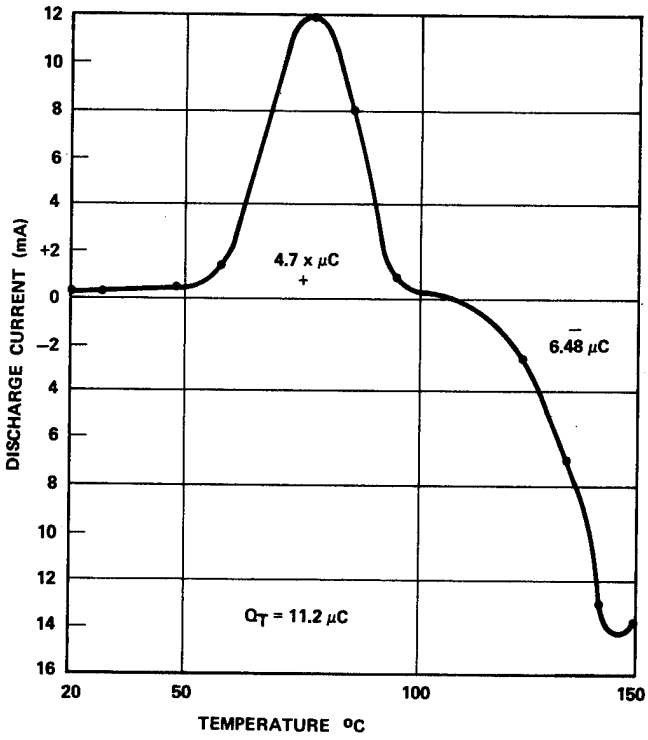

Figure 18. TSD for 0.33 μF 200-Volt Mylar Capacitor. Burn-in (Cooled (+)), 285-Volt Squarewave, One Minute Positive, One Minute Negative.

of the permanently stored charge. It was determined that when the stored charge is less than 1 μC the noise is negligible.

Dielectric noise measurements were made on Mylar capacitors during TSD tests. A 1/f noise was observed between 10 and 1000 Hz with noise root mean squared currents of the order of 10-20 to 10-24. The values could not be correlated with the thermal discharge current spectrum. Thus, where a peak in the thermogram developed, the dielectric noise did not seem to be any different.

Conclusions

The dielectric absorption in capacitors has been quantitized by the integration of the thermally stimulated discharge current. It has been found that some capacitors store a relatively enormous amount of charge which is characteristic of the dielectric used and that the traditional method of measuring dielectric absorption (DA) is useless in determining this and is even misleading. Thus, for example, a capacitor of Mylar at room temperature appears to have almost the same percent DA as a Paralene capacitor by this method, but the actual amount of charge that a Mylar can store in comparison to a Paralene unit is over 10,000 times greater under the same stress and temperature charging conditions. A true measure of DA can be given in terms of the relation Q = CV where the C is the measured (1 kHz) capacitance at room temperature and V is the rated voltage. Thus, if one charges the capacitor at rated voltage one obtains the theoretical or fast charge as it is called. Then the ratio Q(stored)/Q(theoretical) gives a quantitative

measure of the dielectric absorption. When dielectric absorption is measured in this manner, all capacitors without exception will show a measurable amount regardless of the dielectric.

The maximum amount of charge is determined by the charging conditions and it is important to recognize that the maximum intrinsic stored charge can only be realized if the temperature during charging is equal to the highest temperature at which a real dipole or a virtual dipole relaxation process occurs in the dielectric. The organic dielectrics may show only trapping of ions or electrons, and the latter may be injected from the electrodes. It is also possible to inject holes. It follows that the charging temperature has to exceed the temperature at which the deepest traps (in terms of eV) will be activated and the carriers released.

Since part of the charge storage is due to ion diffusion which establishes double layers at boundaries between different microphases, this can arise in nonpolar dielectric films as well. Capacitors using linear polymer films of teflon, polystyrene and polyxylylene, for example, have small but finite stored charge due almost entirely to ions and the stored charge is thus a very sensitive measure of impurities. In teflon capacitors, for example, a difference in stored charge of 100 to 1 has been found between two different capacitors of the same type. Polystyrene is a special case in that over 95 percent of the stored charge comes from a sharp thermal current peak at 114°C and this is certainly ionic in character. Some linear polymers like Kapton film have an extremely high glass transition temperature and must be heated to over 250°C to charge them fully, thus, under normal conditions of use it will appear to have a lower dielectric absorption than it will intrinsically assume.

Capacitors with inorganic dielectrics, even those considered almost ideal such as Mica have a capability of storing large magnitudes of charge, but as noted above, the mechanisms are entirely different. Tantalum electrolytic capacitors are an interesting case because they can be made with a wet electrolyte and a solid semiconductor. In this instance, one has to consider an electrochemical potential as a possible driving force for current, but it would not be temperature dependent.

The presence of a large magnitude of stored charge gives rise to noise voltage spikes in high gain amplifiers since the capacitor acts like a current source. The charge transfer to the electrodes is found to take place during cooling or heating which introduces the possibility of added piezoelectric and pyroelectric effects which are not distinguishable from the stored charge due to the movement of charges or dipole relaxation.

We have shown[8] that stored charge can be controlled by appropriate TSD treatments of capacitors and if complete thermal clean-up is not entirely practical other methods of charge draining, such as the use of radiation at normal temperatures, can be used.

It should be mentioned that the capacitance noise in shielded cables used in very sensitive circuits is amenable to the same type of control. These effects are also found to lead to certain operational problems in ICs which can, likewise, be corrected where stored charge changes the operating point of a field affect transistor.

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NONDESTRUCTIVE, X-RAY INSPECTION OF CERAMIC-CHIP CAPACITORS FOR DELAMINATIONS

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Abstract

A radiographic method has been devised and successfully applied to the detection of delaminations in small ceramic-chip capacitors. The results indicate that this nondestructive technique is suitable for sampling or 100% screening of lots. The radiograph provides an integrated image of internal structure rather than a view of just one plane as in cross sectioning. It requires proper alignment of chips in the x-ray beam, and readily detects voids of at least 0.001-inch width that extend more than 30% of the depth of the capacitor. Life tests of radiographically graded parts showed a high correlation with physical-sectioning results and with capacitor failure rates.

Introduction

Ceramic-chip capacitors are being used in increasingly large quantities in hybrid microelectronic assemblies. These small monolithic devices consist of many thin layers of ceramic dielectric on which precious-metal electrodes have been deposited. Separations of layers (i.e., delaminations) create internal voids that have been a persistent source of problems. These voids, if sufficiently severe, can cause degraded performance or delayed failures at a rate significantly higher than for unflawed parts.

Examination of cross-sectioned samples from each lot or shipment is often used for quality assurance. The approach, however, is time-consuming, costly, and destructive, and consequently must be limited to a few samples. This limitation entails a high statistical risk that the small sample may fail to reveal that a lot contains a high proportion of parts with unacceptable delaminations.

An economical nondestructive method for 100% screening or for examining a statistically significant sample from each lot has long been sought. Cohen[1] reported on the use of liquid crystals to detect voids in large laminated structures by differences in thermal conductivity. Love[2] has reported limited success in using this approach for ceramic capacitors because of the small conductivity differences between the delaminated areas and the basic ceramic structure. For large ceramic capacitors, Love successfully applied specialized ultrasonic equipment not generally available to most part users. He has reported privately to the writers that the technique is not effective with small chip capacitors.

X-ray techniques have been employed widely to examine the internal structure and homogeneity of such objects as metal castings and large ceramic parts, as well as relatively small electronic parts, and to detect metallic contamination in semiconductor components. Their application to nondestructive examination of very small capacitor chips was explored by Aerojet ElectroSystems Company (AESC), and the resulting approach was found suitable for either 100% or large-sample screening.

Background

Decreased insulation resistance and short circuiting have been the two predominant modes of failure for ceramic-chip capacitors used in hybrid microelectronic arrays produced at AESC. Detailed failure analyses revealed one or more of the following conditions in a high percentage of cases: severe delaminations, ceramic rupture, and electrode misregistration.

This experience led, in 1973, to the practice of cross sectioning a small sample from each lot or shipment to evaluate the internal integrity of the ceramic structure. Accept/reject criteria were established, and lots were dispositioned on the basis of the number of defective units found.

The categories of rejectable defects include cracked electrodes with ceramic displacement, foreign matter causing ceramic rupture, electrode misregistration, and delaminations. The latter category encompasses ceramic separations creating voids that contain shattered electrode metalization, when such voids total (a) at least five extending less than half the planar length of the electrodes, or (b) at least two of greater length.

Cross sections of a typical acceptable capacitor and of one containing flaws are shown in Figure 1.*

Causes of Delaminations

In general, delaminations result from anomalous process-control conditions during the manufacture of capacitors from many thin stacked sheets of "green" ceramic-dielectric tape with screened conductors. The stacked sheets are cut into individual chips, which undergo firing to remove organic binders and other volatiles and to sinter the layers into a monolithic structure. Hamer[3] describes the processing steps in detail.

Too-rapid firing can cause escaping gases to force apart dielectric plates, creating voids. Dielectric ruptures can also occur during high-temperature sintering. Improper lamination or variations in ceramic-tape thickness can produce stresses that create voids or cracks in the dielectric. Other causes of delamination include the use of flawed tape containing large bubbles or contaminants, and the presence of foreign particles or nonhomogeneous dielectric materials that are incompatible with the ceramic or electrode materials. Piper[4] provides details on many of these anomalies.

Physics of Failure

The most common cause of ceramic-capacitor failure can be traced to an overstressed dielectric at a physically weak spot produced by some manufacturing nonuniformity. Defects of this type generally result in catastrophic infant-mortality failures and are usually screened by electrical tests and voltage conditioning. Not all manufacturing nonuniformities result in immediate failure, however. The most common form of long-term degradation of ceramic capacitors is evidenced by a reduction in insulation resistance. Although the capacitor body is a crystalline solid, it is possible for ions to move throughout the dielectric. This ion motion, as described by Payne,[5] can create non-ohmic behavior resulting in a time-dependent degradation.

*All photoreproductions in this paper are micrographs of cross-sectioned parts or of radiographs of parts.

Delaminations create conditions that can contribute to degradation. A void in the ceramic allows oxygen or other gases to change the equilibrium conditions of the dielectric. There is a tendency, when voltage is applied to the capacitor, for oxygen ions to float to the electrodes, pick up electrons, and become oxygen gas. If the capacitor has many delaminations and is not sealed, oxygen can escape. Continued loss of oxygen ions alters the characteristics of the dielectric until the device acts like a semiconductor. When the capacitor is biased, internal delamination may create a nonuniform field in the area of the defect and cause localized degradation of the dielectric.

This failure mechanism indicates a possible relationship between delaminations and the long-term degradation of insulation resistance that often occurs when such defects are present. The larger or more severe a delamination, the more likely it is to result in ultimate failure.

Cross-Sectioning Constraints

Cross sectioning to detect capacitor flaws has constraints that limit its usefulness. It destroys the samples and, for purely economic reasons, must generally be limited to a few parts from a lot or shipment. This creates a high statistical risk because small samples cannot adequately discriminate against lots with a high proportion of parts containing delaminations. For very small parts, sectioning is often limited to a single plane, which may or may not expose the delaminated area. Sequential grinding and polishing can be used, but is more costly and time-consuming. All these operations delay the dispositioning of the lot or shipment.

Radiographic Examination

The problems experienced with flawed capacitors led to the investigation of x-radiography as a screening tool. The degree to which x-rays penetrate a material is a function of its density and homogeneity. A void attenuates x-rays less than the surrounding area and projects a more heavily exposed (darker) image onto the radiographic film.

Figure 2 illustrates this concept, and Figure 3 defines the capacitor axes as they were oriented for radiography. Figure 4 reproduces typical images of unflawed and flawed capacitors x-rayed through the Y dimension to reveal delaminations in the X-Y plane.

Chips typical of those examined (all Type BX)[6] are depicted in Figure 5, which gives the range of capacitor sizes in this investigation. After experimentation, the conditions found to produce the best results with a Hewlett-Packard Faxitron 804 x-ray unit were as follows:

(1) Distance from x-ray source to film--36 inches

(2) Exposure factors--3 mA at 90 to 110 kV for 4 to 6 minutes, depending on capacitor depth (Y dimension)

(3) Film--Kodak Industrex R (Single Coated), processed with Kodak Liquid X-Ray Developer and Replenisher.

The size of the delaminations that can be detected radiographically is a function of the resolution attainable with the system used. To produce the sharpest images, the x-ray source should be as small as possible (a point source would be the ultimate) and be located as far from the object as practicable. The capacitor chips should be positioned as close to the film as possible, with their Y axes and the central ray perpendicular to the film. Satisfying these conditions enhances image definition (sharpness of outline, clarity of detail).

For the initial investigation, groups of chips were mounted on double-coated adhesive tape placed on top of the film holder as shown in Figure 6. Later in the study, to minimize handling and contamination, plastic tweezers were used to align the chips in the thin-plastic compartmentalized trays* in which they were delivered (see Figure 7).

To achieve the best image quality, a fine-grain single-emulsion film was chosen in preference to the more generally employed double-emulsion films (coated on both sides of the base). The developing time typically ranged from 4 to 5 minutes.

The delaminations recorded on the film are frequently not discernible to the unaided eye. For analysis, the radiographs were mounted on a light box and were viewed, by transmitted fluorescent light, through a binocular microscope (15 to 30X). Photomicrographs were made for record purposes and for comparison with subsequently cross-sectioned samples in the development of accept/reject criteria comparable to those for sectioned samples.

The experimental results showed that delaminations can appear slightly shorter on radiographs than on cross sectioning. This occurs because they tend to taper at their ends to a width (Z dimension) that is insufficient for radiographic detection. For this reason a 40% void-length criterion (X dimension) was chosen for radiography, as opposed to 50% for cross sectioning. That is, a capacitor was considered unacceptable if the film revealed (a) one delamination exceeding 40% of its length, or (b) five or more of lesser length. Figure 4 exemplifies radiographically acceptable and unacceptable conditions.

Off-Axis Sensitivity and Minimum-Detectable Size

Voids generally occur in the plane of electrode metalization as separations between adjacent ceramic layers. When the capacitor is aligned with its Y axis parallel to the central ray of the x-ray beam (perpendicular to the film), a delaminated area will project an image that most accurately represents the void (as illustrated in Figure 2). If the capacitor is tilted so that its Y axis is at a considerable angle to the central ray, narrow delaminations can be obscured because there is greater attenuation of the beam (see Figure 8).

Sensitivity to misalignment was investigated by using various tilt angles while x-raying a group of parts determined radiographically to have delaminations. Satisfactory results were obtained as long as the tilt did not exceed 12°. Beyond 12° the images of minor delaminations began to disappear and larger voids appreciably lost detail. Figure 8 presents typical images for 0, 12, and 18° tilt angles. A modicum of care must be taken, but alignment within ±12° has been found to present no difficulties.

Even with perfect alignment, detectability is limited by delamination-area depth and width (Y and Z dimensions, respectively), with depth the more important. Experimental evidence indicates that a void must exceed about 30% of the capacitor depth to be detected

*Approximately 2 inches square, holding 25 to 100 specimens.

reliably. Cross-sectioning experience indicates that delaminations tend to be fairly deep, while shallow ones occur infrequently. Although undesirable, shallow delaminations are less likely to cause failure, and the inability to detect them radiographically does not represent a severe reliability risk.

A very narrow delamination may not be detected if its width (Z) is less than the image resolution or if the misalignment angle is too great (which underscores the need for care in parts positioning). It was found in this investigation that delaminations as narrow as 0.001 inch in a properly aligned part can be detected consistently, provided they have sufficient depth.

Correlation with Cross Sectioning

X-ray examination is of value only if the results are highly correlated with the presence of delaminations. During this investigation and in applying the radiographic screening method, several thousand parts were x-rayed and subsequently cross-sectioned. Figures 9, 10, and 11 present examples of x-ray images and corresponding cross-section photomicrographs. The overall correlation in the study was greater than 99%.

Nearly all of the observed delaminations were found in a single cross section in the X-Z plane. Only occasionally were sequential grinding and polishing necessary to locate and expose a void shown radiographically. Figures 12, 13, and 14 reproduce radiographs (22X) of capacitor chips that contained a number of delaminations, together with Y-Z cross sections (22X) through the chips to show the corresponding void depth. To achieve a good estimate of delamination size and shape by cross sectioning alone, it would be necessary to take sequential sections in both X-Z and Y-Z planes. In contrast, radiographs display all delaminations provided they are at least 0.001 inch wide (Z) and extend over at least 30% of the depth of the part (Y), regardless of their location within the part.

When delaminations involved the displacement of several adjacent ceramic layers, sectioning indicated greater severity than shown in the corresponding radiographs. The suspected reason is breakage caused by the very high stresses that cross sectioning and polishing apply to the brittle, fragile ceramic in the delaminated area.

As noted earlier, radiographic images can suggest a shorter length (X dimension) than sectioning, because delaminations tend to taper at their ends to a width below the detectable 0.001 inch. Hence, the 50% void-length criterion for physical sectioning was reduced to 40% for radiography.

It was concluded that, within the resolution limits discussed above, a void revealed radiographically will be found in cross sectioning. The results indicated that radiography is highly effective in detecting delaminations and can be used as a 100% screen or to examine sufficiently large samples to minimize the statistical risks of accepting lots containing voids above some acceptable threshold. To provide added assurance, a small sample from a rejected lot can be sectioned to confirm the x-ray results.

Accelerated Life Testing

Theory and experience indicate that capacitors with severe delaminations tend to fail at a higher rate than those with small voids or none. To verify this premise, an accelerated life test was performed with samples graded on the basis of radiographic examination.

From a number of rejected lots* determined by cross sectioning to have excessive voids, 476 capacitors were randomly selected and x-rayed. Each radiograph was examined and the part was graded according to the radiographic criteria established earlier (i.e., unacceptable with one void >40% X or five or more <40% X). From this group, 200 capacitors were selected for the life test--125 with severe (rejectable) voids and 75 with voids of acceptable size.

The 200 parts were mounted on cards and were electrically tested for capacitance and dissipation factor at 1 kHz and 1 V, rms. Insulation-resistance measurements were made with a General Radio megohm-meter at 50 Vdc (twice the rated voltage) in accordance with Method 302 of MIL-STD-202,[7] at both 25 and 125°C. At 25°C the required insulation resistance was a minimum of 100 kilomegohms or 1000 megohm-microfarads, whichever was less, and at 125°C was 10 kilomegohms or 100 megohm-microfarads, whichever was less. All 200 sample parts met these initial electrical requirements.

The parts were then life-tested at 125°C, biased at 50 Vdc, each with a 100-kilohm resistor in series. The insulation resistance, capacitance, and dissipation factor were measured after 500 and 1000 hours. The resistance requirement at 125°C at these test points was 3 kilomegohms or 30 megohm-microfarads, whichever was less.

At 500 hours, eight parts had failed because of low insulation resistance and one had a short circuit. At 1000 hours, 12 more parts had low insulation resistance and one had shorted. All but the two short-circuited parts continued to meet the capacitance and dissipation-factor limits. Table 1 summarizes the results.

TABLE 1

Life-Test Results

Radiographic Grading*	Number Tested	Number of Failures**		
		0-500 Hours	500-1000 Hours	Total
Severe delaminations (major defects)	125	8***	12	20
Acceptable voids	75	1	1***	2
Total	200	9	13	22

*Confirmed by subsequent cross sectioning.
**Except as noted, all failures were due to lower-than-specified insulation resistance.
***One short-circuit failure in each case.

Twenty of the 22 failures occurred among the 125 parts judged radiographically to have severe delaminations. Subsequent cross sectioning confirmed the original defect grading. Examples are shown in Figures 10 and 11.

Two failures occurred among the 75 parts judged radiographically to have small, acceptable voids. One part had low insulation resistance at 500 hours and one was found to be short-circuited at 1000 hours. In the

*Purchased to MIL-C-55681A,[6] and voltage-conditioned at 125°C for 168 hours at 50 Vdc (twice the rated voltage), with 1-kilohm current limiting.

case of the former, sectioning revealed a single small delamination that involved severe ceramic displacement and rupture between two adjacent electrodes. This rupture (which cannot be detected radiographically) and the severe stresses applied during the life test caused the decrease in insulation resistance.

The short-circuited capacitor in the sample of 75 had been graded radiographically as having two delaminations extending less than 40% of its length (X). Sectioning revealed two delaminations exceeding 50% in length but of shallow depth (Y) in some locations, as well as several minor voids in the end-cap area that were not detected by x-ray examination. The observed shallowness could account for the radiographic misgrading in this case.

In summary, the life-test results showed that parts considered radiographically to have severe delaminations fail at a significantly higher rate than parts judged to have delaminations of acceptable size. The instance of the short-circuited capacitor that appeared radiographically to be acceptable suggests that the standard accept/reject criteria given earlier for x-ray examination could be tightened further if higher-reliability parts are required.

Conclusions

Delaminations are potentially detrimental to the reliability of ceramic-chip capacitors. The experimental results indicated that capacitor failures are clearly related to the number and severity of such voids. They also showed that delaminations large enough to cause failure can be detected radiographically and that x-ray grading has a high statistical correlation with subsequent cross-sectioning results.

The advantages of x-radiography for the detection of chip-capacitor delaminations are that the technique

- Is nondestructive
- Can be applied to large samples to reduce statistical risks
- Can be used for 100% screening
- Has a high correlation with physical cross sectioning
- Does not distort the delaminated area (whereas ceramic breakouts frequently occur in sectioning)
- Provides an integrated image of internal structure (rather than only one plane as in sectioning).

The limitations include

- The need to align capacitor X-Y planes within $\pm 12^{o}$ of the central ray for reliable detection of delaminations
- Difficulty in detecting shallow delaminations (less than 30% of capacitor depth)
- A minimum-detectable delamination width of 0.001 inch
- A void-image length less than the true length because the delamination tapers at its ends to a width less than 0.001 inch
- Costs related to special handling in aligning numerous parts and to skilled inspection of radiographs.

Experience has shown that only a modicum of care is necessary to ensure optimum alignment, and that shallow, narrow, delaminations ($Y < 30\%$, $Z < 0.001$ inch) and end-taper effects are of less significance than the gross defects revealed radiographically. The writers have found the radiographic approach effective in improving the reliability and quality of ceramic capacitors used in high-reliability microelectronic assemblies, and believe that the benefits to be gained far outweigh the limitations.

Acknowledgement

The authors wish to thank Larry E. Hess for his invaluable help in preparing, cross sectioning, and photographing samples.

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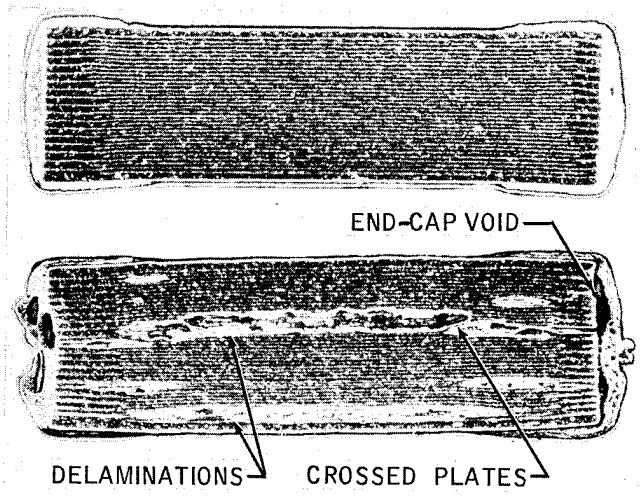


Figure 1. Cross Sections of Acceptable and Unacceptable Capacitors (22X).

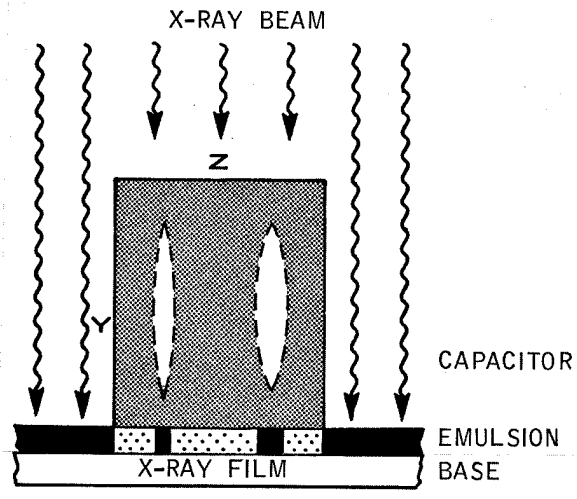


Figure 2. Capacitor Radiography, Schematic.

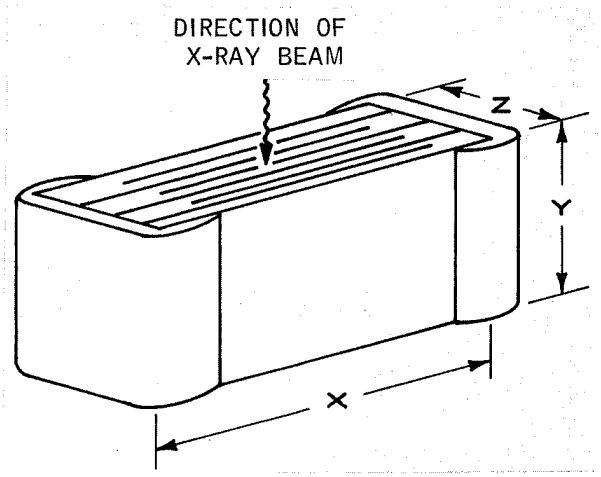


Figure 3. Axes as Oriented for Radiography.

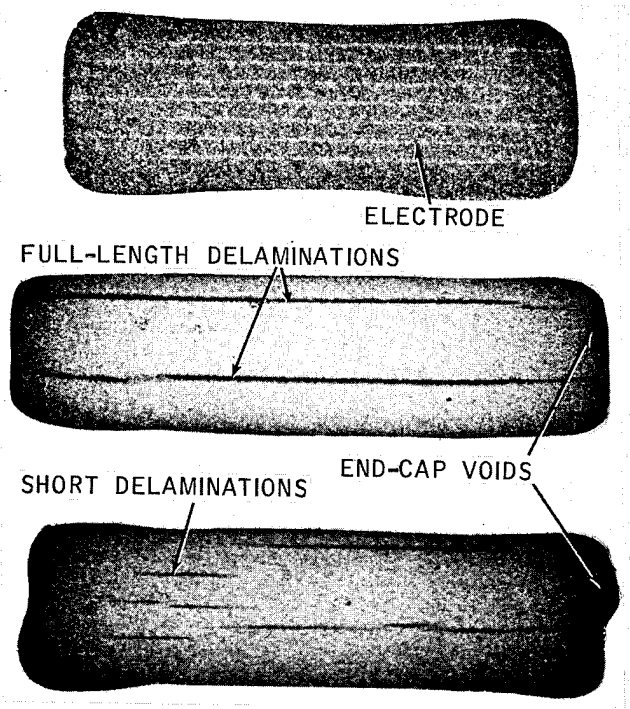
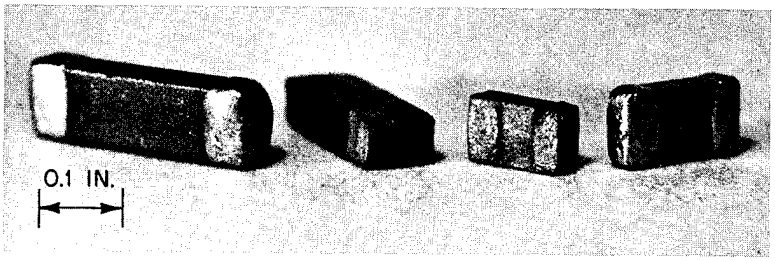


Figure 4. Radiographs of Acceptable and Unacceptable Capacitors (22X).



	DIMENSIONS, IN.			CAPACITY	NO. OF
	LENGTH (X)	DEPTH (Y)	WIDTH (Z)	μF	PLATES
MINIMUM	0.075	0.050	0.050	0.001-0.015	5-20
MAXIMUM	0.180	0.075	0.050	0.006-0.06	10-40

Figure 5. Typical Ceramic-Chip Capacitors and Dimensions.

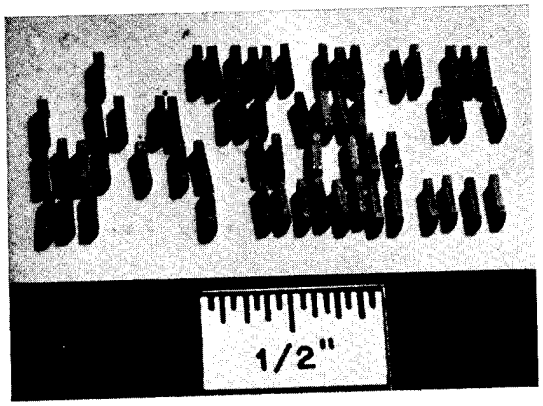


Figure 6. Capacitors Oriented on Double-Coated Adhesive Tape.

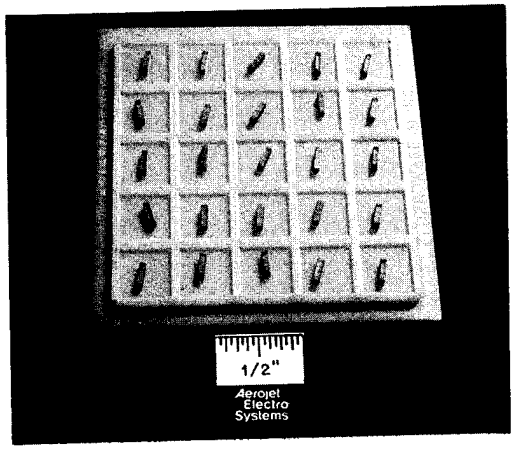


Figure 7. Capacitors Oriented in Plastic Tray.

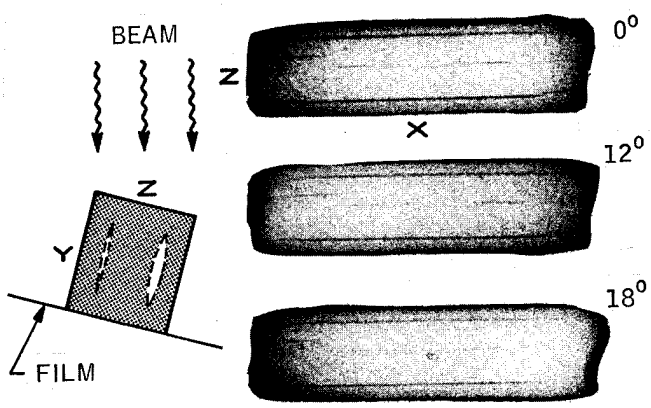


Figure 8. Effects of Orientation, Radiographs of a Typical Capacitor (14X).

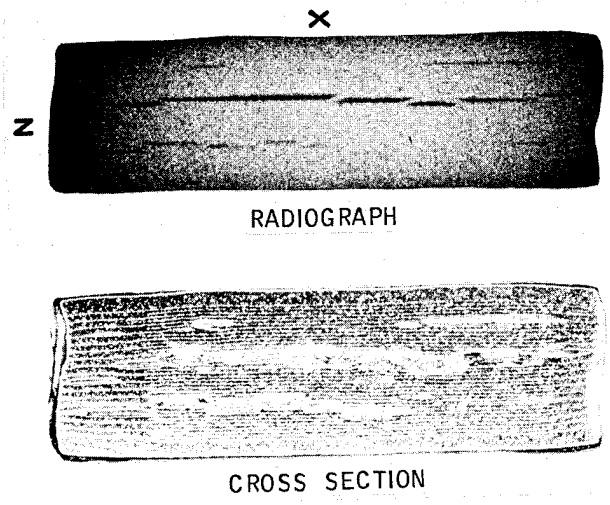


Figure 9. Length Correlation, Sample 4-2 (22X).

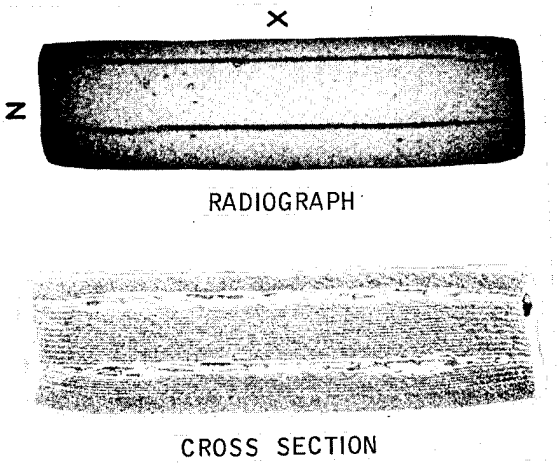


Figure 10. Length Correlation, Sample 3-18 (22X).

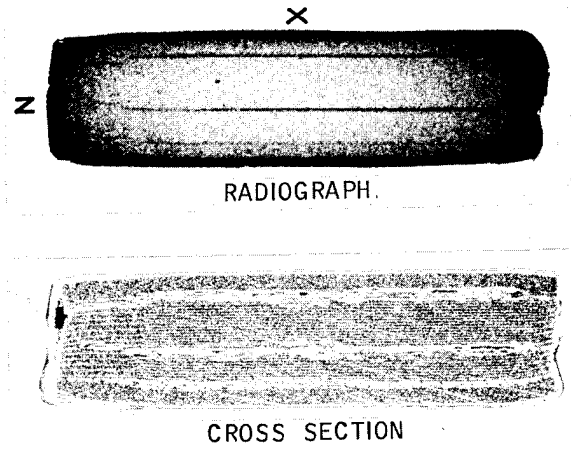


Figure 11. Length Correlation, Sample 1-19 (22X).

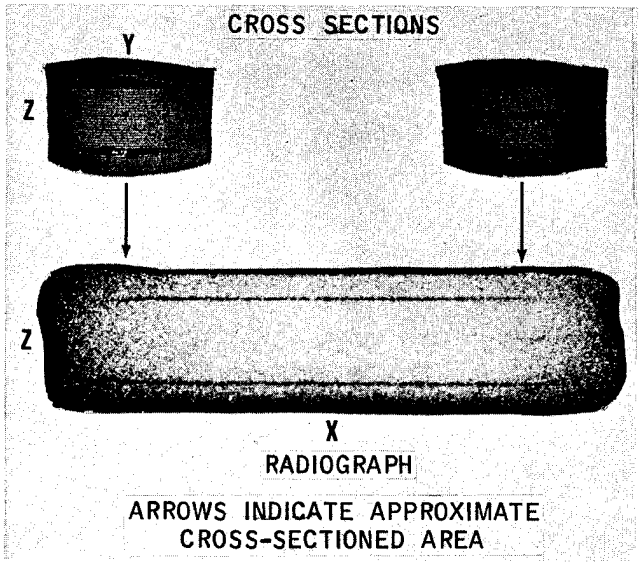


Figure 12. Depth Correlation, Sample 4-16 (22X).

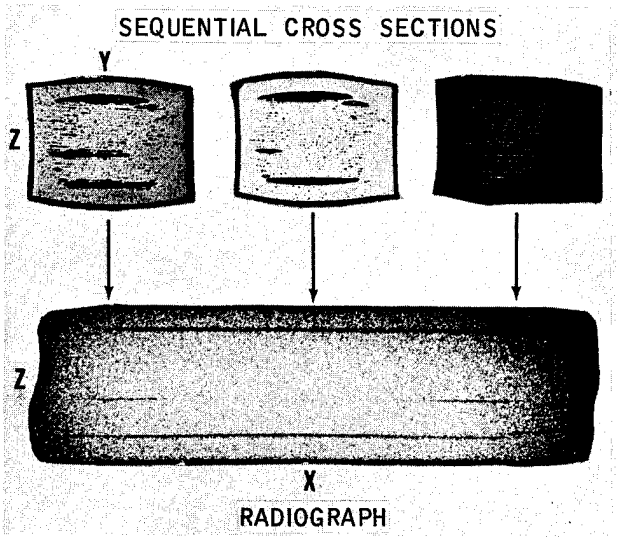


Figure 13. Depth Correlation, Sample 3-2 (22X).

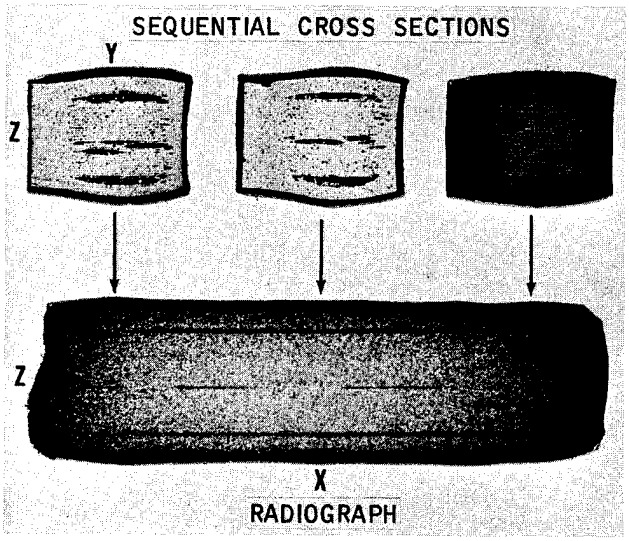


Figure 14. Depth Correlation, Sample 4-22 (22X).

FUSING MECHANISM OF NICHROME-LINKED PROGRAMMABLE READ-ONLY MEMORY DEVICES

G. B. Kenney*, W. Kinzy Jones**, and R. E. Ogilvie*

Introduction

The Programmable Read-Only Memory (PROM) consists of a two-dimensional matrix of nichrome (NiCr) fuses blown in a specific pattern to introduce a digital code. In this application, the reliability of the NiCr fuse can be considered to consist of two parts, that of the unfused and the fused resistor link. The reliability of unblown NiCr registors has been reported as excellent, when the resistors are properly fabricated and operated within well-defined specifications.[1,2,3]† The reliability of blown resistors is directly related to the probability of healing or "growback" occurring.[4] However, this can be minimized by fusing the resistors under proper blowing conditions. Although the reliability of fused NiCr resistors has been established, fusing mechanism has not, and is at present only speculation.

To obtain the experimental verification necessary to develop the fuse, an experimental technique[5] was developed using the transmission electron microscope (TEM). This technique was necessary because of the size of the fuse-gap region (less than 1 μm), and the available spatial resolution (less than 20Å) obtained in TEM analysis.

Analysis of commercial NiCr-linked PROM devices from four vendors, fused to the vendor's specification, was used to develop a unified fusing process. Although a rigorous approach is possible from magnetohydrodynamics, i.e., the unification of Maxwell's equations and fluid mechanics, the theory is based on the disintegration of liquid sheets (fluid dynamics) with effects of electron flux and potential used to explain the effects of geometry and certain phenomenological occurrences which are observed. The theory is based on the instability of a liquid sheet subsequent to nucleation of a void in the sheet. Upon melting, the void becomes an unstable hole in the molten film; as this hold grows, perturbation develops with a characteristic wavelength, as predicted by fluid mechanics. As the perturbations grow, the molten film disintegrates, leaving the characteristic structure in the gap region, as observed in the TEM. Observations and measurements from these photomicrographs are in good agreement with the calculated wave-perturbation wavelength.

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†Bracketed numerals refer to similarly numbered references in the List of References.

Theory of Fusing

Liquid-Sheet Disintegration

Liquid-jet disintegration has been the subject of theoretical and experimental investigations for 100 years, with the major theoretical analysis proposed by Lord Rayleigh in 1889.[6,7] Surface perturbations of all wavelengths are possible on the liquid jet; however, one perturbation with wavelength λ, characteristic of the liquid used, predominates and grows in amplitude. Since the growth rate is exponential with time, this wavelength grows more quickly than the others and is the only one observed. Rayleigh, considering only the capillary effects on a liquid cylinder, predicted that the characteristic wavelength which leads most rapidly to the disintegration of the cylindrical mass would be

$$\lambda = 4.509\ (2a)$$

where

a = radius of the cylinder

Weber[8] extended the theory to cover the effects of viscosity and obtained

$$\lambda = 2\pi\ [2(3Z + 1)]^{\frac{1}{2}}$$

where

$$Z = W/R$$

and

$$W \equiv \text{Weber number} = U\ (2\rho a/\gamma)^{\frac{1}{2}}$$

$$R \equiv \text{Reynolds number} = 2U\rho/\eta$$

where

U = velocity of the jet

η = coefficient of dynamic viscosity

From this it is seen that for nonviscous liquids $Z = 0$ and $\lambda = 4.44\ (2a)$, and for viscous liquids $Z \to \infty$ and $\lambda \to \infty$. This is in agreement with the earlier work of Lord Rayleigh.

The stability of thin fluid films was investigated to study the effect of liquid properties on the development of sheet disintegration. Surface tension, independent of all other properties, was found to have a profound effect upon the stability of the spray sheet. An increase in the surface tension leads to a reduction in the overall sheet-surface area, but also results in a larger perturbation-free zone. Therefore, the stability of the sheet is increased by an increase in surface tension.

The independent effect of viscosity is very similar to that of surface tension with one specific difference. Sheet stability also increases with viscosity; however, the

surface area of the sheet also increases in contrast to the effect of surface tension. These sheets with high viscosity are also found to have undisturbed rims. This behavior has been predicted by Weber[8,24] who showed that as viscosity increases, the growth rate of perturbations decreases.

No real stabilizing effect can be attributed to changes in density. However, the combined effect of increasing density and surface tension results in a very stable sheet devoid of major waves.

Two opposing forces are at work in the liquid sheet. The inertia—or expansion—force gives the particles in the sheet a radial velocity. The opposing force of surface tension imparts a velocity of contraction to the particles in the sheet. If the surface tension were zero, all of the particles would move out radially in the fan. However, since the surface tension is not zero, the particles follow a curved path inward toward the axis of the sheet. Since the edge of a liquid sheet is subjected to unbalanced surface forces, it contracts instantaneously, forming a thick cylindrical rim. This rim is analogous to a cylinder of liquid, and therefore obeys the same rules for disintegration that were specified by Rayleigh[6]. Since the wavelength of the perturbation on the surface of the cylinder is a function of surface tension, it is the surface tension that leads to disintegration of the edge of the sheet with the same wavelength as found on cylinders of the same liquid.

Dombrowski[9] states that, "In the disintegration of a sheet of liquid the formation of ligaments or threads is a necessary stage before the production of drops." He has also found that threads can be formed at any free edge or new boundary, such as the edge of a hole produced by a perforation in the film.

Therefore, a perturbation (with its characteristic wavelength) which forms on the cylindrical rim, grows into a drop as it is centrifuged radially outward, or as the cylindrical rim rolls or pulls back toward the axis of the sheet. Thus, as the rim is pulled in, the drop is left behind and necks out from the rim leaving a thread between itself and the rim. This thread eventually breaks up because it is itself a cylinder of liquid, and therefore subject to Rayleigh's laws of disintegration based on surface tension. As a result, a series of spherical particles of various sizes is produced by the disintegration of the free edge of the sheet or periphery of a hole.

Fusing Mechanism for Nichrome Resistors

Nichrome resistors are fabricated using various vapor-deposition techniques which are considered proprietary by the PROM vendor. The exact composition and thickness can vary between vendors; however, the thickness ranges between 150 Å and 250 Å and the composition ranges from a 50:50 to an 80:20 nickel-to-chrome ratio. After thermal processing in device fabrication, the environment of the resistor consists of the NiCr element and a Spinel (Cr_2NiO_4) sheath sandwiched between a layer of passivation and thermal oxide. Electrically, the resistor can be considered as two parallel resistor elements at room temperature: a low-resistance NiCr element with a metallic positive temperature coefficient of resistance (TCR), and a very high-resistance semiconductive oxide (Cr_2NiO_4) with a corresponding negative TCR. This model is used to discuss the high-temperature fusing effects.

The NiCr resistor is fused by pulsing an excessive amount of current to provide sufficient energy (Joule heating) to melt the neck region of the element. Upon melting, the molten sheet breaks up by a mechanism of hole growth. This necessitates the formation of a hole in the original void-free sheet; this hole must have a diameter greater than the thickness of the sheet to be unstable and grow.[10]

The nucleation of this hole, as a first step in the sheet-disintegration process, can occur in various ways.[11] Although electromigration (i.e., vacancy supersaturation) is possible, the hole is probably generated after the sheet is molten at the position of highest current flux. Because of observed segregation of the metallic components (nickel and chrome) in the gap region, the combined effects of the potential gradient on the ionic species, high current flux, and thermal gradient should be considered in the diffusional effects.

Another possibility is that a two-dimensional wave exists on the surface of the film. The waves should have a characteristic wavelength in both directions. The total surface area or total energy of the system is decreased as the amplitude of the waves increases. When the amplitude of the waves exceeds half of the thickness of the film, a hole is formed, thus leading to the disintegration of the film. However, regardless of the way in which this nucleation occurs, it is still a requirement for sheet breakup that a hole, with a diameter of the sheet thickness, be generated. The fusing mechanism, based on this principle, takes place as follows.

If the sheet is at a uniform temperature, the hole will grow symmetrically in all directions. However, in the case of a NiCr-resistor gap region, the temperature is not uniform and current flux must also be considered. The hole interrupts the continuity of the current-flux lines, and leads to current crowding between the edges of the circle and the near edges of the rectangular sheet. This current crowding leads to an increase in Joule heating in these regions. The surface tension of the liquid NiCr is inversely proportional to the temperature. Therefore, the top and bottom regions of the hole, as seen in Figure 1, having lower-than-average temperatures and higher-than-average surface tensions. The opposite is true of the edges which have higher temperatures and lower surface tensions. Since the rate of radial growth of the hole is inversely proportional to the surface tension, [12] the circle degenerates into an ellipse and

grows faster along its major axis than above its minor axis (see Figure 1).

As the hole begins to grow out from its original shape, as described previously, the edge of the film around the hole contracts and forms a cylinder. This cylinder is analogous to the Rayleigh jet, and as it thickens the characteristic perturbation develops on the rim. The amplitude of the perturbation grows until a drop forms on the surface of the rim. The diameters of the drop and the rim are approximately equal at this point. As the rim continues to contract, the drop is left behind in the hole connected by a NiCr thread, or finger (see Figure 2).

If the central gap region remains molten while the hole continues to grow to the edge of the sheet, the NiCr fingers will also pull back, form perturbations, and separate into individual spherical particles. If the central gap region cools quickly as the hole and rim pull back, the drops at the tips of the NiCr fingers will freeze in, or solidify. However, the rim will still remain molten until the conductive path across the sheet is opened. Since it is still molten, it will continue to pull back leaving a series of long fingers extending into the gap region.

Therefore, it is possible for two distinctly different structures to exist in different gap regions. The particular structure developed will depend on the temperature of the gap region; this will depend on the extent of current crowding, which is a function of resistor geometry. The more uniform the equipotential distribution within the gap region, which minimizes regions of high current divergence, the higher the probability of NiCr-finger formation. This is due to a larger sheet area at molten temperature when the hole is formed, and the more rapid movement of the hole and subsequent perturbation surfaces. In either case, the spacing between the fingers and the wavelength of the perturbation along the NiCr fingers should have the same value. Therefore, the spherical particles, which predominate in one case, should have the same spacing as that observed between the long fingers in the other case.

As considered previously, the total resistor consists of two regions, the NiCr sheet and a Spinel oxide phase. At the melting temperature of NiCr, the oxide phase has a resistivity of approximately 1 Ω-cm.[13] The oxide can thus conduct current to allow a momentary super-heating of the NiCr sheet. However, since the amount of Joule heat generated from this conduction is secondary to the primary NiCr conduction, it is unable to maintain conduction after the NiCr has fully fused. However, sufficient heat is generated for the oxide film to exceed its melting point and break up in the same way as does the NiCr sheet. The oxide film breaks up into a honeycomb structure in the hotter gap regions, whereas only a few holes form between the tips of opposite NiCr fingers where the final conduction of the fuse occurs.

Experimental Procedures

Preparation of thin sections of the metallization layer of semiconductors suitable for TEM analysis has previously been reported.[5] In analysis of PROM devices, the goal of sample preparation is a section of minimum thickness and maximum size, preserving the environment of the gap region. The maximum size is not limited by the sample-preparation technique, but rather by the 3-mm-diameter support grid accommodated by conventional electron microscopes.

Slight modifications have been made to the technique previously described, which result in samples of maximum size. Figure 3 is a photomicrograph of a standard section size produced for this analysis. Pure carbontetrafluoride is the reactant gas used in the plasma etcher to remove 85 to 90% of the passivation layer. Monitoring the removal rate or measuring the final thickness of the passivation layer is very difficult. This is usually accomplished by optically monitoring changes in color or by monitoring changes in resolution in the gap region using the scanning electron microscope (SEM). The sample is then ground from its back side to a thickness of less than 2 mils. The remaining silicon and 85 to 90% of the thermal-oxide layer must be removed using the plasma etcher, with the passivation surface and sides of the sample protected from further etching. This is done by placing the specimen on a drop of Dow-Corning DC 704 diffusion-pump oil which acts as a protective coating. The oil polymerizes after being subjected to the plasma etch for only 1 min. Thus, it also acts as a cement and holds the specimen in place on the glass slide. After the silicon has been removed, the sample becomes transparent. The thickness of the thermal oxide can then be monitored by noting the color changes undergone by the NiCr resistors as the thermal-oxide thickness decreases. When the NiCr resistors become light brown or tan, the thickness of the thermal-oxide coating is approximately 1500 Å.

The finished sample can be successfully removed from the glass slide by submerging the slide in a beaker of acetone. Since polymerized oil is soluble in acetone, the specimen will soon be floating freely. The sample can now be dipped from the beaker using a standard folding TEM grid. Extreme caution must be exercised because the sample tends to curl into a cylindrical shape. If necessary, it must be held flat with a pair of tweezers while the grid is folded and locked over it. This completes the process and the sample is ready for observation in either the SEM or the TEM. It should be noted that due to its fragility, extreme care should be exercised when working with the unsupported section.

Results and Discussion

Transmission Electron Microscopy

The Philips EM-300 TEM was used to examine the gap region of the fused NiCr

resistor. The EM-300 was operated at 100 kV and all photomicrographs were taken in the bright field mode. Nichrome resistors of four different geometric designs have been examined. Representative photomicrographs are given in Figure 4. All resistors were fused to the appropriate vendor's specifications. Since Vendors A and B exhibit the extreme of the model, the following discussion is limited to analysis of their structures. It should be noted that the odd appearance of Vendor D's fuse is due to a granularity in the passivation layer, which made sample preparation extremely difficult.

The fine features of the structure found in the gap region of the Type-A NiCr resistors are illustrated in Figures 5 through 8. There are certain features of the structure of the gap region that are characteristic of Type-A resistors:

(1) After the molten zone is formed, two interfaces appear to have developed, separating the resistor into two sections. These interfaces then appear to have pulled back forming an unstable meniscus. This unstable meniscus is characterized by the long fingers or rods of NiCr, which extend into the gap region.

(2) The fingers are characteristically arranged at specific intervals across the width of the resistor.

(3) The NiCr fingers also seem to have partially pulled back leaving elliptical and spherical particles between themselves and their sister fingers across the gap.

(4) White holes are usually found in the region between the ends of the NiCr fingers. These white spots are referred to as holes because they represent areas of high electron transmission where all of the nickel and chrome have been removed from these areas.

(5) Except for the white holes, a continuous light gray phase remains to outline the original position of the unblown resistor.

(6) The NiCr fingers on the emitter side of the gap are much longer and wider than those on the metal run side of the gap. The NiCr fingers on opposite sides of the gap are usually arranged in brother-sister pairs.

The structure found in the gap region of the Type-B NiCr resistors (see Figures 9 through 11) appears to be very different from that found in Type-A gap regions. Certain structural features of the gap region characteristic of Type-B resistors are:

(1) Dense spherical particles distributed throughout a major portion of the gap region. These particles are arranged with a specific spacing; that is, there tends to be common nearest-neighbor spacing.

(2) Spherical particles surrounded by an interconnected gray phase.

(3) White holes separating the gray phase and spherical particles. As previously discussed, white holes are areas of high electron transmission.

This honeycomb structure is common to all Type-B resistor-gap regions, and appears to be completely unrelated to the NiCr-finger structure found in Type-A resistor-gap regions. This point is considered later.

One of the most outstanding features of the Type-A resistor-gap region is the periodic spacing of the NiCr fingers. The average value of the spacing of the fingers is given in Table 1. The true spacing values were measured from Figures 5 and 7.

It is also observed that the NiCr fingers of the Type-A gap region have partially pulled back. In doing so, perturbations with specific wavelengths have developed on the surface of the NiCr fingers.

Table 1. Measured value of gap structure.

λ'	λ	δ
2410 Å (σ = 0.206)	2270 Å (σ = 0.256)	
2290 Å (σ = 0.235)	2170 Å (σ = 0.141)	
		2340 Å (σ = 0.113)
		1950 Å (σ = 0.087)

λ' = spacing between fingers

λ = wavelength of perturbation along surface of finger

δ = spacing between the spherical particles

σ = standard deviation

In several instances these perturbations have led to breakup of the fingers, resulting in formation of elliptical and spherical particles arranged at periodic intervals away from the tip of the finger. The wavelength of the perturbation of the finger equals the spacing between the resulting particles; this wavelength is also recorded in Table 1 as measured from Figures 5 and 7. It should be noted that the wavelength of the perturbation and equivalent spacing between the resulting particles is approximately equal to the spacing between the fingers.

As previously stated, the spherical particles found in the gap region of the Type-B

resistors are arranged with a specific spacing. The average value of this spacing has been measured from Figures 9 and 11 and is recorded in Table 1. A comparison of the values listed in Table 1 demonstrates that the spacing between the particles in the Type-B gap region is approximately equal to the spacing between the fingers in the Type-A gap region. This point will be examined in more detail in future discussions as it is the link that joins the Type-A and Type-B resistors together in one fusing mechanism.

Scanning-Transmission-Electron-Microscope Analysis (STEM)

Nondispersive X-ray spectroscopy was performed to determine the chemical composition of the different components found in the Type-A gap regions. A JEOL 100-C STEM was used, because with this instrument operating in STEM mode, X-ray data can be collected from spots having diameters of approximately 500 Å. This small spot size is essential since most of the components of the gap region have dimensions in this range. A Cambridge SEM was also used, in STEM mode, to duplicate the following results.

The nickel and chrome had segregated in the gap region. This chemical separation was found in all links analyzed. The nickel was found to have segregated toward the metal run side of the fused region (the shorter side of the finger structure). Conversely, the chromium segregated on the emitter side of the filament. The concentrations at the respective tips of the filaments were approximately twice that of the unfused resistor concentration. The concentration gradient decreased linearly from the tips to the end of the filaments, where the composition was equivalent to analysis away from the gap region.

No nickel or chrome was found in the white spots, and the gray region contained chrome with some nickel. However, due to the low court rate, the chemical analysis of the gray region was extremely difficult.

Analysis of Micro-Microelectron Diffraction Patterns

The atomic structure of the components of the Type-A and Type-B gap regions has also been investigated. Both the Philips EM-300 and the JEOL 100-C have proven to be ineffective in producing useful electron diffraction patterns of the gap region. However, the JEOL 200-C, with its 200-kV electron source, can produce micro-microelectron diffraction patterns of the components in the gap region. Also, a spot size of approximately 500 Å can be used to generate the micro-microelectron diffraction pattern. Therefore, patterns can be obtained from individual components within the gap region. A sequence of micro-microelectron diffraction patterns taken for one spot in the gray phase is given in Figure 12. Two patterns had to be taken, one being off-axis to obtain the outer diffraction rings. Analyses of the various phases previously described are:

(1) The NiCr phase—Both the body of the unfused resistor and the densified filaments and spherical particles were indexed as having the FCC nickel structure, consistent with the NiCr phase diagram for alloys over 50% concentration of nickel.

(2) The gray phase—A Spinel phase was indexed from this region. This is consistent with the lattice parameters for Cr_3O_4 and Cr_2NiO_4. Because of results from STEM analysis, the latter is the expected phase. This is also consistent with the oxide formed on oxidation of NiCr wire.

(3) The white holes—An amorphous pattern, void of crystalline structure was obtained. The pattern was equivalent to that produced in the glass region away from the fuse element. This region is identified as a region of amorphous SiO_2.

Experimental Verification of Unified Theory

The theoretical treatment of the fusing mechanism of NiCr resistors in PROM devices, as presented here, is discussed from the initial current pulse to the final freezing-in or solidification of the gap regions. All observations and measurements of the gap regions were made either before or after the resistor had been fused. Therefore, only the final structure of the gap region, as predicted by the theory, can be compared with the micrographs of the gap region.

The Type-A resistor-gap region is characterized by an arrangement of long NiCr fingers. This structure has been predicted to exist for a resistor whose central open region solidifies before the circuit has completely opened. This phenomenon would usually be associated with resistors having large gap regions where small equipoltention gradients exist. The resistor is melted by Joule heating in regions where current crowding occurs, that is, around the rim of the expanding hole. However, Joule heating does not occur along the length of the NiCr finger. Therefore, it is possible for the finger to quickly solidify while the rim of the hole is still contracting, producing elongated fingers. This does not mean that the NiCr fingers do not contract; they do. However, their contraction is controlled by the temperature in the gap region.

The spacing between the fingers and the wavelength of the perturbation along the fingers can be calculated using the equations of Rayleigh and Weber. The Rayleigh equation, based only on surface tension, predicts a value of approximately 3000 Å, which is in excellent agreement with the measured values given in Table 1. Weber's equation, which accounts for viscosity effects, predicts a value of approximately 3000 to 3600 Å, which is also in good agreement with the measured values from Type-A resistors.

The theoretical analysis was based on the assumption that a thin sheet existed in a homogeneous phase. Therefore, the existence of the gray phase and the subsequent white holes could not be predicted to exist. The

observation can be made that the white holes do exist between the ends of opposite fingers which correspond to the hottest region of the gap as the hole grows. It can then be assumed that the gray phase will break up when the temperature is sufficiently high.

It is observed that the fingers are longer on the emitter side of the gap of a fused Type-A resistor. This could be due to the effect of the force of the electric field in the resistor, which acts in the opposite direction from the electron flow. As a result, the electric field assists surface tension in pulling the rim of the hole back in the direction of the emitter base, simultaneously retarding the motion of the opposite side of the hole in the opposite direction.

The phenomenon of brother-sister pairs of NiCr fingers is due to the existence of identical waves on the opposite sides of the hole or gap. Since these waves will obviously have the same wavelength, they will also have the same nodal points since they are both terminated at the same point on the edges of the hole or gap. Thus, corresponding nodal points define the position of corresponding brother-sister pairs.

The Type-B resistor-gap regions are characterized by an arrangement of spherical particles. This structure has been predicted for a completely molten sheet. In this case, the hole forms and grows, leading to the production of fingers which also contract and break up. Therefore, the spacing measured between the particles should correspond to the value predicted by Rayleigh and Weber. Again, calculated values are in very good agreement.

The gap region of the Type-B resistors is hot enough for all of the NiCr fingers to disintegrate. Therefore, the gray phase might be expected to break up since the region appears to be hotter. This is indeed what has been observed and the characteristic honeycomb structure results.

As a result, the dissimilar Type-A and Type-B gap-region structures are not formed by different fusing mechanisms but by a variation in one general mechanism which is due to the temperature and size variation of the gap region produced. Therefore, resistors of a different design could possibly produce gap regions with a structure exhibiting features of both of the Type-A and Type-B gap regions, although the basic mechanism is operable in all cases.

Summary and Conclusions

The NiCr resistors used in PROM devices are fused or blown by pulsing an excessive amount of current through them. This leads to Joule heating in the narrow region of the resistor where the current crowding is most pronounced. The resistor then melts and pulls back to open the circuit, thus introducing the binary code to be used. It should be noted that the results have been obtained on devices which have a high reliability history.

From the theoretical treatment, observations, and measurements, it is concluded that:

(1) The formation of a hole prior to or immediately after melting is essential to the fusing mechanism. This hole could be produced by various methods.

(2) The hole grows into a flattened ellipse due to the asymmetric surface tension.

(3) As the hole grows, its rim thickens into an unstable cylinder which then disintegrates into a symmetrical system of NiCr fingers extending into the hole.

(4) The NiCr fingers will or will not disintegrate into elliptical and spherical particles depending upon the temperature and size of the gap region.

(5) One fusing mechanism, based on jet and sheet instability as illustrated by Rayleigh and Dombrowski, is operative.

(6) By changing the fusing conditions, the final structure of the gap region will appear to be quite different. However, this is only due to changes in the extent of the fusing process and not to changes in the fusing mechanism itself.

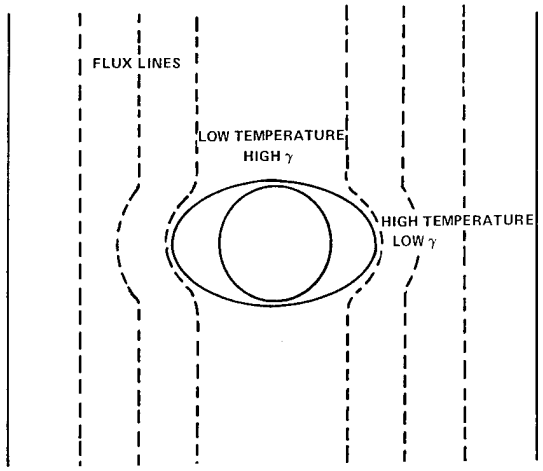


Figure 1. Current crowding and hole-growth direction.

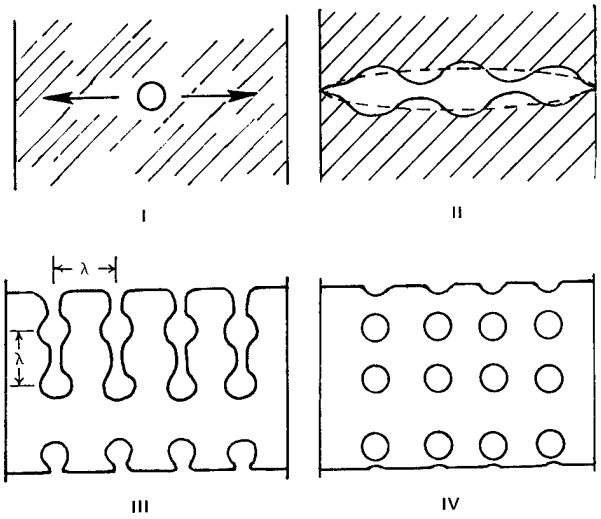


Figure 2. Progressive sheet disintegration.

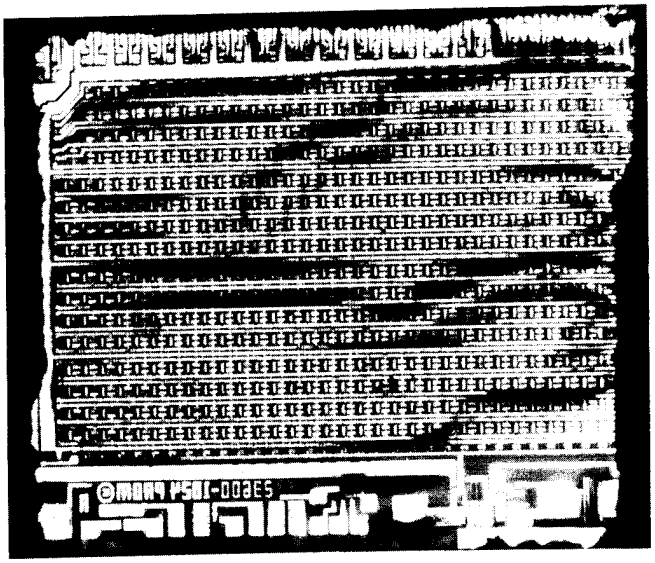


Figure 3. Photomicrograph of thin section.

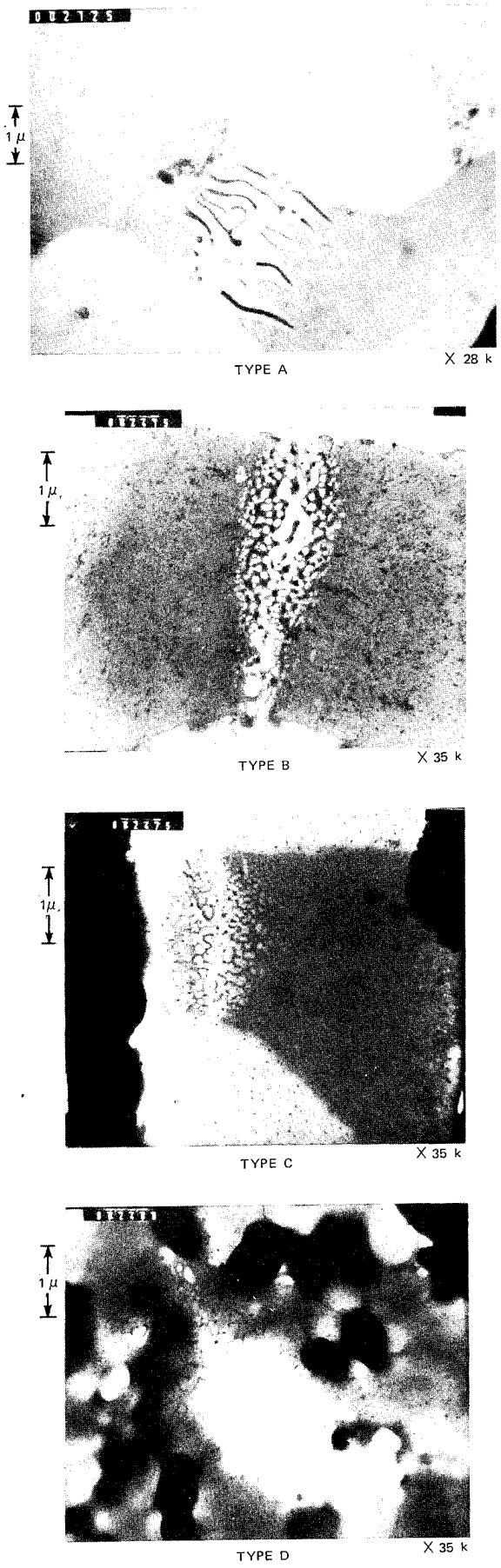
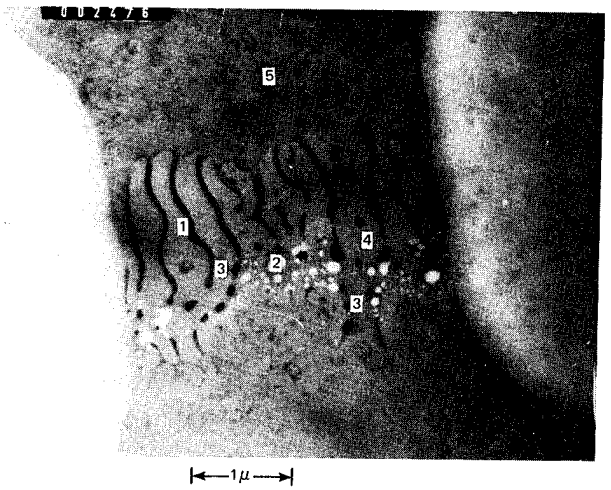


Figure 4. Fuse gaps of four commercial PROMS.



1. FINGERS
2. HOLES
3. ELLIPTICAL AND SPHERICAL PARTICLES
4. GRAY PHASE
5. EMITTER BASE SIDE OF GAP REGION

Figure 5. Gap region of fused Type-A resistor.

X 66,000

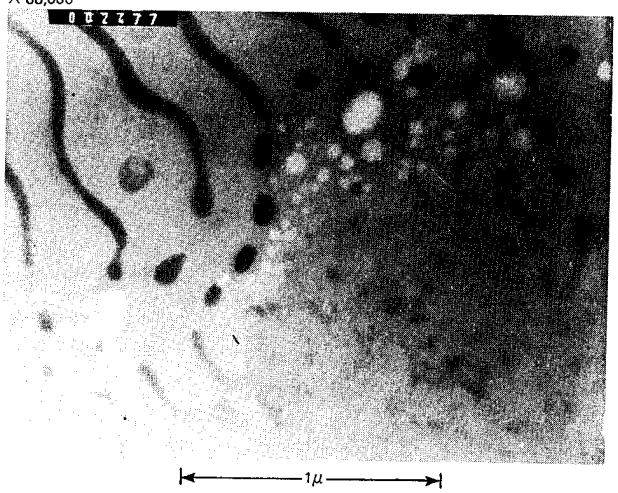
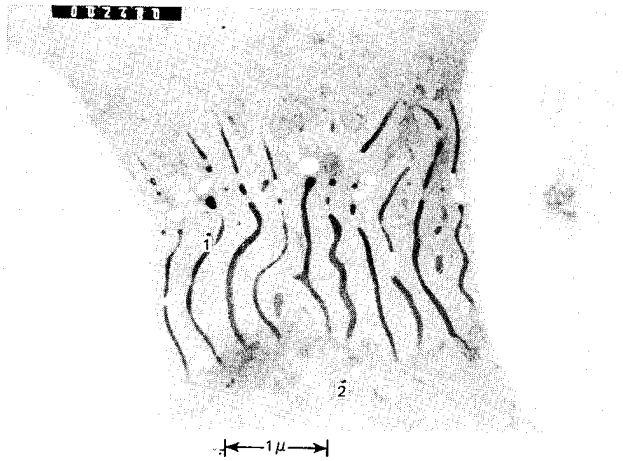


Figure 6. Higher magnification of Figure 5.



1. PERTURBATION WITH CHARACTERISTIC WAVELENGTH ALONG NiCr FINGER
2. EMITTER BASE SIDE OF GAP REGION

Figure 7. Gap region of fused Type-A resistor.

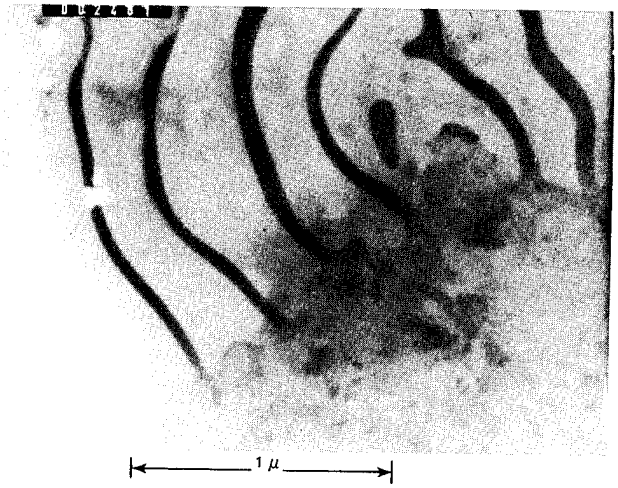


Figure 8. Higher magnification of Figure 11. Illustrates periodic spacing between the fingers.

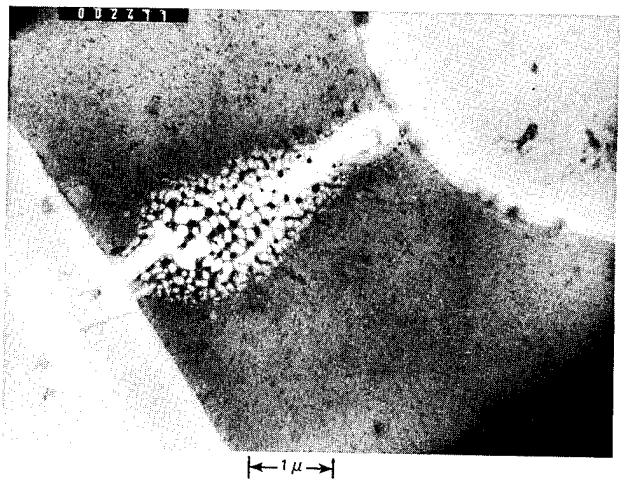
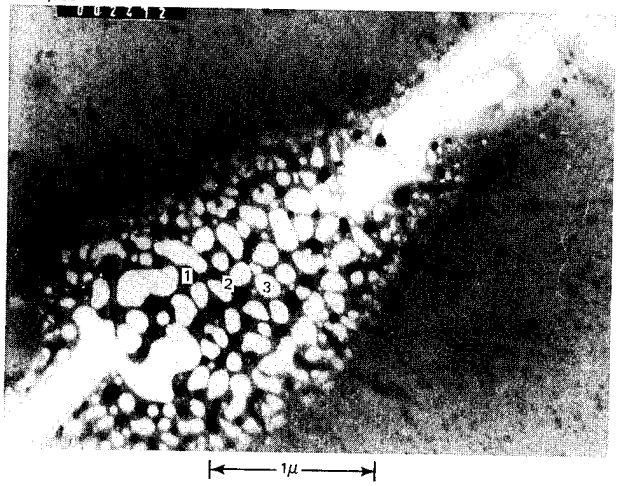


Figure 9. Gap region of fused Type-B resistor.

X 43,000



1. SPHERICAL PARTICLES
2. INTERCONNECTING GRAY PHASE
3. WHITE HOLES

Figure 10. Higher magnification of Figure 9.

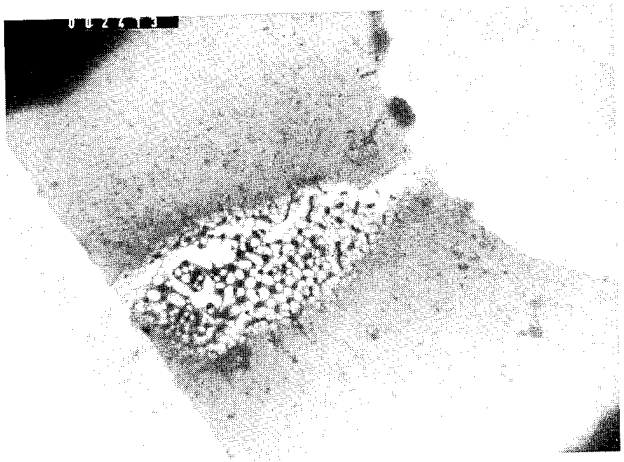
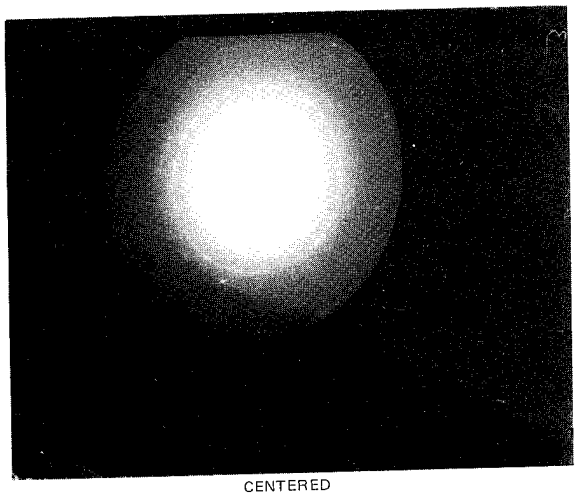


Figure 11. Gap region of another fused Type-B resistor.



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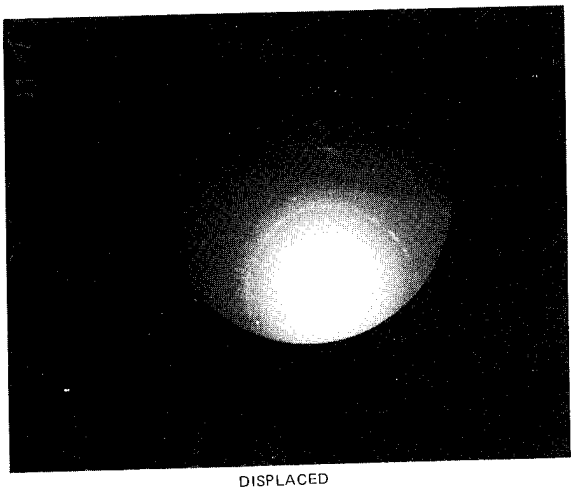

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Figure 12. Micro-microelectron diffraction patterns of gray phase in Type-A gap region.

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FUSING MECHANISM OF NICHROME THIN FILMS

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Introduction

Nichrome fusible link programmable read-only memories, PROM's, have been developed and utilized for over 7 years[1]. The physical mechanism of fusing these resistors has been generally described as melting[2], but only in the last 2 years, with the advent of a successful transmission electron microscopy technique[3], has detailed information on the structure of the programmed fuse gap become available. These observations, coupled with electrical and thermodynamic characterization of the fusing event, have led to a clearer understanding of this phenomena with concurrent definition of programming conditions for reliable operation of programmed PROM's.

Some Relevant General Properties of Nichrome

Fundamental to the mechanism of nichrome fusing are those physical properties that make it an excellent resistor material from a processing, design and applications perspective. It is no accident of history that nichrome is widely used for resistors on solid state devices.

To begin with, nichrome is a resistive material comprised of two transition metals - nickel and chromium. In transition metals, the outer electron shells contain only one or two electrons and some of the conduction electrons must come from inner shells. The inner shell conduction electrons are shielded by the outer shell resulting in a high scattering and trapping site density. Thus, transition metals are inherently less conductive than normal metals[4]. In the case of nichrome, an alloy effect[4] occurs to further enhance electron scattering. The result is that the resistance of the alloy is much higher than the arithmetic average of its two components[5] as illustrated in Figure 1.

The resistivity of nichrome makes it well suited for small geometry thin film resistors that are size compatible with high density fuse design requirements. Due to its high resistivity, the thickness of nichrome that is necessary to achieve a typical fuse resistance of 300 ohms is about 200Å. The small cross-sectional area of the nichrome resistor (as compared to polycrystalline silicon, for example) is an advantageous property for a fuse, as will be described later. There is also the elimination of step coverage problems where the metallization (aluminum) contacts the nichrome.

A consequence of the extensive electron scattering in nichrome is a short mean free path of the conduction electrons. For example, the mean free path in gold is 380Å[6] compared to an estimated 40Å for nichrome. As a consequence, films greater than 100Å thick have bulk resistivity properties (i.e., surface effects are not dominant). As Figure 2 shows, surface scattering effects which reduce conduction are absent by the time the resistor film is greater than 100Å[7] in thickness. The practical ramification of this property is reproducibility in the fabrication process. Because there is no dependence on surface effects to achieve the desired sheet resistivity, thin film resistors may be produced with excellent tolerance and stability[8].

The short mean-free path is also relevant to describing the fusing mechanism, discussed in the Mass Transport Models section.

Nichrome is a material that forms a self-limiting oxide skin. That is, the oxide of nichrome is known to be a coherent spinel[9,10], see Figure 3. It is postulated that in the course of processing nichrome resistors, this thin spinel sheath will form around the nichrome to a thickness of ≃20Å. This sheath serves to stabilize the resistors and is partly responsible for the excellent thermal stability (absence of $\Delta R(T)$ effects) of nichrome.[11]. This spinel may also be a factor in the fusing phenomena.

Microstructure Of A Programmed Nichrome Fuse

The technique of using transmission electron microscopy (TEM) to examine programmed fuse gaps was developed by Dr. Kinsey Jones at C. S. Draper Labs[3,12]. It is the only technique which mutually satisfies the requirements of sufficient resolution to analyze the gap and not destroy in sample preparation the structure to be analyzed. It is this latter point that has severely limited the utility of the scanning electron microscope (SEM) in endeavors to analyze programmed nichrome fuses. In depassivating devices, necessary with the SEM, microstructural details of the fuse gap are destroyed. Many interpretations of the fusing phenomenon based on SEM results have been erroneous or misleading because what was seen was an artifact of sample preparation.

Figure 4 illustrates schematically the utilization of transmission electron microscopy for fuse gap analysis. Of course, besides direct structure observation, composition of various phases may be ascertained by electron probing.

The microstructure of a programmed fuse gap in a PROM circuit via TEM is shown in Figure 5. The relevance of those programming conditions will be discussed further in following Sections, but Figure 5 is representative of the gap created in a nichrome fuse under programming power conditions specified[13] for PROM's.

The TEM photograph indicates the elemental distribution found by microprobing. The following observations are made:

a. The visual appearance indicates that the neck of the fuse was in the molten state during programming.

b. Mass transport of the nickel and chromium from the gap region has occurred.

c. There is an asymmetry to the melted nichrome distribution. That is, there is more densified nichrome on what was the cathode (negative) side of the fuse which suggests the molten nichrome moved in a direction opposite to electron flow during programming.

d. The gray phase (region C) of the gap which comprises the insulative separation of the two sides of the fuse is devoid of nickel and composed of oxides of silicon and chromium[14]. The typical separation is 0.6-1.0 microns. The resistance across the gap is >10 megohms and it will not break down, electrically or structurally to voltages in excess of 100 volts.

e. The white spots, dark spots and filaments are described by the fluid dynamics of a disintegrating liquid sheet[12]. Briefly, that model describes how minute discontinuities in a liquid sheet, perterbate into larger holes and finally into droplets and filaments because of surface tension effects. The structure looks similar to a "frozen splash".

Mass Transport Models

In the previous section, it has been demonstrated that programmed nichrome fuses melt and that mass transport takes place. But what is the mechanism, the driving force for mass transport? Table I lists the possibilities.

Table I

(1) Electromigration (Huntington & Grone[15]): Mass flux occurs under the influence of high current flow because electron collisions with atoms of the conducting medium provide a net motion vector in the direction of electron flow.

(2) Thermal gradient (Soret[16]): In the presence of a thermal differential, material will diffuse from the high temperature to the cold temperature region.

(3) Concentration gradient (Fick[17]): In an imbalanced distribution of concentration, mass will diffuse from regions of higher concentration to lower concentration.

(4) Field enhanced ionic mobility (Eyring and Jost[18]): Molten metals will ionize, lose electrons and become cations. In the presence of an electric field, they will be driven towards the cathode.

Considering each possible mechanism in turn:

(1) Electromigration - On the surface, this seems a most logical explanation for programming. It is known that the current densities in a fuse neck at programming are very high ($\sim 5 \times 10^7$ amps/cm^2) and it could be postulated that this electron flux sweeps the nickel and chromium from the gap. But empirical data and theoretical considerations show this not to be the case.

a. TEM of the fuse gap indicates the molten nichrome has moved in a direction opposite to electron flow.

b. Theoretical calculations of the kinetic energy of conduction electrons in nichrome demonstrate that because the mean-free path is short and the lattice binding energy is high (transition metals typically have high melting points), the electrons have insufficient energy to impart the mobility to the nickel and chromium atoms necessary for electromigration in the direction of electron flow.

However, general treatments of electromigration theory[15,24] identify two forces acting on atoms of the conducting medium. One is the aforementioned electron momentum ("electron wind") in the direction of electron flow. The other is the electrostatic force from the applied electric field that causes ions of the conducting material to move opposite to the direction of electron flow. See mechanism (4).

Obviously, the joule heating that leads to melting the fuse is coming from electron interaction with the nichrome film. There is no incongruity with the fact that this is not leading to electromigration such as observed in aluminum. Because the mean-free path is short, the energy exchanged per collision is small. But because electron scattering is a dominant factor in resistive materials, the frequency of collisions is high. Thus, thermal energy (lattice vibration) is added to the metal atoms. The electron collisions increase the amplitude of the atomic vibration and increase the temperature. This is why nichrome is an efficient material for converting electrical energy into thermal energy (toaster effect).

(2) Thermal Gradient - From an analysis of heat flow in a fuse, it has been shown (see the Transient Heat Flow Analysis section), Figure 6, that the temperature profile across a fuse neck is flat. The gradient occurs at the neck-to-fuse body interface. But the programmed gap occurs in a region where there is no temperature gradient. Further, this model would predict a symmetric distribution of mass, post-programming which is not observed. Temperature gradient does not cause the mass transport.

(3) Concentration Gradient - It has been shown in unprogrammed fuses that no concentration gradient exists. Laterally in the fuse film this is borne out by the TEM/probe analyses. That is, no nickel or chromium concentration variations are observed across an unprogrammed fuse. Vertically (distribution of nickel, chromium through a cross section of the resistor) it has been shown[20], from sputter etching Auger analysis that the nickel and chromium are distributed uniformly through the film (no concentration layering effects).

Because there is no concentration gradient initially, this is ruled out as a starting mechanism for fusing.

(4) Field Enhanced Ionic Mobility - Eyring and Jost[18] have observed that liquids have a fixed ratio between their energy as a liquid and the energy required for vaporization, see Figure 7. Stated simply, the principal is, the more cohesive the liquid, the more energy is required to transform it to the gaseous phase, and the ratio is a constant. This rule held for all types of liquids (gases, solvents, organics, etc.) except metals. But by accounting for ionization of molten metals and the subsequent reduction in atomic radii, see Table II, they found that metals obeyed the liquid: gas constant energy ratio. In other words, molten metals are ionic.

Footnote: Arguments have also been advanced that oxidization is the mechanism of fusing[19]. If this were so, the probe data, which discerns elemental presence, would not show nickel and chromium depletion in the gap region, i.e., mass transport, per se, would not have occurred. Because the TEM data clearly indicates mass transport, attention is focused here on identifying the driving force for that mass transport.

It follows then that these positive ions (they have given up outer shell electrons) will move in the presence of an electric field (from the programming pulse) toward the negative terminal, opposite to the direction of electron flow. This is consistent with the TEM observations and with some investigations of electromigration. For example, Wever[25] observed in copper, above 950°C, that mass flux was toward the cathode.

In summary, nichrome fuses program as follows: A programming pulse of sufficient power is applied across the fuse. Power dissipation in the fuse neck heats this region into the molten state and the nickel and chromium atoms become ionized. They move toward the negative side of the fuse and the liquid film begins to disintegrate. The film becomes electrically discontinuous and rapidly returns to the solid state, the final structure resembling a frozen splash described by fluid dynamics. The fuse gap consists of insulative oxides of silicon and chrome, with resistance >10 megohms.

Transient Heat Flow Analysis

The previous discussions dealt with the fusing event postfacto, describing the microscopic material structure created by programming. The dynamics of the fusing event can also be characterized. By modeling the fuse structure and its environment in terms of classical heat flow, the connection between electrical and material behavior of fuses can be established.

A computer thermal analysis program called "THEROS"[21] was used to calculate the dynamic temperature effects in a PROM-fuse structure as a function of applied power density.

This computer program can thermally model a multicomponent structure and calculate the temperature as a function of time for given power dissipation conditions. The program takes into account temperature dependent thermal properties of the various materials and models a 2-dimensional multi-material, multi-geometrical structure into a RC circuit network that can be analyzed by sophisticated transient circuit analysis programs. This approach is convenient because the differential equations that describe heat flow problems have the same form as differential equations for RC circuit networks. For example, specific heat is analogous to capacitance, thermal conductivity is analogous to the inverse of resistance, temperature is analogous to voltage and heat flow is analogous to current. By way of the "THEROS" heat flow to electrical analog program, the sophistication available with present circuit analysis programs can be utilized to solve complex heat flow problems without consuming hours of computer time and without the errors prevelant in more simplified calculations. For the heat flow model to be truly representative of the actual device, the immediate environment of the fuse must be completely accounted for. For example, the passivating oxide layer on top of the fuse will affect the heat flow and the subsequent structure of the programmed fuse. Programming a fuse without the passivating oxide[22] will result in a different structure than occurs in an actual PROM circuit.

The term "power density" is defined as the amount of power that is dissipated in the fuse neck region divided by the area of the fuse neck (watts/mil^2), see Figure 8. The concept of defining power density as power per unit surface area is applicable to thin film heat flow problems where the heat is dissipated through a surface. (The concept is analogous to defining current density as current per cross sectional area). Figure 9 shows a plot of the computer results giving the temperature in the center of the nichrome fuse that would be achieved if a constant power were applied for a time t. The curves show that the fuse can easily reach the melt temperature of nichrome[23] within microseconds for power densitities >2.5 watts/mil^2.

Figure 10 is a plot of the intercept of the time to reach the melt temperature (1450°C) vs. the power density. This theoretical prediction of the power density versus time to reach the melt temperatures compares well with experimental data on time to fuse. The data in Figure 10 was taken from test vehicle fuses, processed identically to circuit fuses, but free of interfacing circuitry. This allowed precise characterization of fuse-pulse interactions. The data matches for long fusing time but deviates for short fusing time. This difference can be accounted for by considering the definition of "time to fuse". The experimental data points represent total time to fuse which includes rise time of the programming pulse, time for the fuse to heat to sufficient temperature, and time of the actual fusing event. For example, Figure 11 shows a typical current trace for a fuse programmed under constant voltage conditions. The trace shows a fixed rise time, t_r (about 100 nanoseconds for this data), a response time, t_m, for the nichrome to reach the melt temperature, and a time for the fuse neck to enter the melt phase and program, t_f. Plotting the time defined as t_m shows excellent correlation with the theoretical prediction of the time to reach melt temperature. The difference between the theoretical prediction to reach melt and the actual time to fuse agrees with the measured values of t_r+t_f. Figure 10, therefore, shows that fusing follows a heat flow dependence that requires the nichrome to achieve melt. Proper PROM design necessitates taking into account thermal factors that affect the heat flow conditions in the neighborhood of the fuse. Concentrating power by optimum fuse geometry and ensuring sufficient power to the fuse will achieve fast, uniform programming.

For power density conditions below the programming threshold level, the fuse temperature as a function of power density into a fuse for a sustained pulse ($t \to \infty$) is shown in Figure 12. There is good agreement of the computer model with experimental data. The experimental data was derived from measuring the fuse resistance (at reduced current, avoiding I^2R heating) of an externally heated fuse and comparing that to the power necessary to generate the same resistance at an ambient temperature of 25°C. The agreement between model and experimental data is a further indication that the heat flow analysis is correctly projecting the temperature in the fuse.

It is also relevant to note the low power density on a fuse in the read mode, 5% of the threshold power density to melt the nichrome fuse. Test vehicle fuses were stressed at 1 watt/mil^2 which is 65% of the fusing threshold level and equivalent to a fuse temperature of 800°C. No failures occurred after 4000 hours of continuous operation. Thus, the designed power density for PROM operation in the read mode avoids the occurrence of unprogrammed fuses becoming open.

In summary, the power density versus time to program curve, Figure 10, is described well by the heat flow model and implies a single mechanism, melting, for fusing both fast and slow programming. High power programming (fast blow) approaches adiabatic heating

conditions and therefore gives a large melted region and a wide gap. Restricted power programming (slow blow) allows much of the heat to diffuse away taking longer for the fuse to reach melt.

Marginally Programmed Fuse

By grossly violating recommended programming procedures for fuses, it is possible to create a marginal fuse gap that may be subject to reverting state ("grow-back"). This anomaly was induced in a test vehicle fuse by restricting the power input to a value on the $t \to \infty$ asymptote ($\sim$1.5 watts/mil^2) of the power density vs. time to fuse curve (Ref. previous section, Figure 10). Under these conditions, a fuse was induced to program, become electrically discontinuous, after 5 minutes of sustained power. This effect, programming under an anomalously reduced power, was not found to be reproducible. Many fuses at this power density would not program after days.

This deliberately improperly programmed fuse was subsequently subjected to a slowly applied DC voltage ramp under current limited conditions (10M Ω resistor in series). At 12 volts, the fuse resistance dropped to $\sim$5,000 ohms. The TEM photograph of this fuse is shown in Figure 13. It is obvious from this photograph that the reduced power condition has resulted in a fuse that has marginally programmed. That is, the gap created after programming is very narrow (approximately a few hundred angstroms) and subject to a voltage breakdown effect.

Fuses programmed per the recommended power levels will program rapidly with a wide gap as illustrated in the Mass Transport Models section. These fuses can be subjected to more than 100 volts and will undergo no change in electrical or physical condition.

As indicated in Figure 13, if a restricted amount of power is applied to a fuse, it is possible to create a very narrow gap. Under the presence of high voltage and extreme current limiting, it is then possible to force a voltage breakdown across the gap. It is postulated that this voltage discharge results in the establishment of a low conductivity relink at one or a few points of closest approach in the marginally blown gap. This specific structure could not be confirmed with the TEM study because even the TEM did not have resolution to examine microstructure at $<$300 angstroms.

This mechanism of marginal programming is precluded from occurring in an actual PROM circuit because the programming specification, specifically the power and pulse widths, have been established to only generate well blown, wide gap fuses. That is, if the power actually reaching a fuse is lower than that required to blow the fuse properly, the fuse will not program in the time allotted for the programming pulse. The device, therefore, becomes a programming reject (won't program) and is scrapped.

In summary, the observation that a nichrome fuse can be marginally programmed has no connection with the reliability of the PROM circuit. Recall, to generate this anomaly, a power density four times less than the designed value and a program time $\sim 10^8$ times longer than the maximum specified programming time was required. Further, a voltage $\sim$10 times higher than the maximum that would be seen in an actual PROM, (with current limiting) was required to cause the relink.

Obviously, these observations and conclusions are based on nichrome fuses, PROM design, and control procedures as deployed by this manufacturer. Contentions by others that a specific fuse material, nichrome or something else, is more or less reliable must be interpreted in perspective of the manufacturer's technology and not necessarily be construed as being generally representative.

Life Test Results

Life testing data of programmed PROM's has been accumulated for several years of production. The data in Table III summarizes those results. The total sample base represents a multiplicity of designs and configurations (256, 512, 1024, 2048, and 4096 bit PROMS). These samples were selected from production runs that had passed the standard final test program and were programmed to data sheet programming procedure. The burn-in conditions are representative of typical applications (except for elevated temperature). The results indicate that the level of reliability of these PROM circuits is equivalent to circuits of similar complexity that do not utilize fusible links.

Summary

(1) Conduction electrons in nichrome have a short mean-free path. This maximizes I^2R heating and precludes electromigration in the direction of electron flow as a fusing mechanism.

(2) Transmission electron microscopy is the only effective analytical tool to characterize the programmed fuse gap structure.

(3) Nichrome fuses program by molten metal (nickel, chrome) ions moving in the presence of an electric field. The final structure resembles a frozen splash and is described by fluid dynamics.

(4) Thermal analysis coupled with empirical programmed fuse data indicate a threshold power density for fusing. If this power density is exceeded, which can be assured if the programming time utilized is as specified, the fuse gap will be wide and reliable. If this power density threshold is only matched, it is possible to create a marginal fuse.

(5) Life test results indicate programmed PROM reliability is equivalent to devices of the same complexity that do not utilize fusible links.

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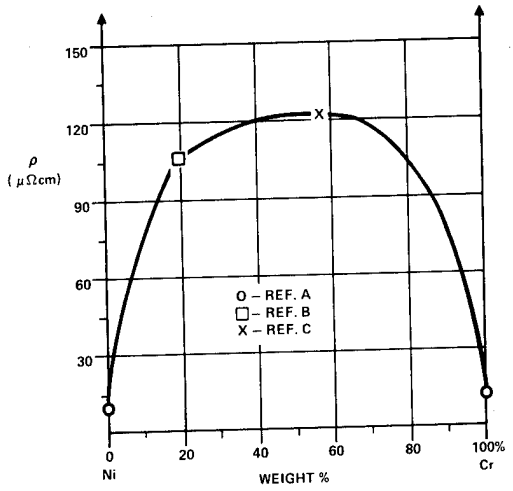
CONDUCTION PROPERTIES OF NICHROME

- NICKEL AND CHROMIUM ARE TRANSITION METALS.
- INNER SHELL ELECTRONS CONDUCT, OUTER SHELL SHIELDS. HIGHER RESISTANCE.
- ALLOY EFFECT ENHANCES SHIELDING/RESISTIVITY.

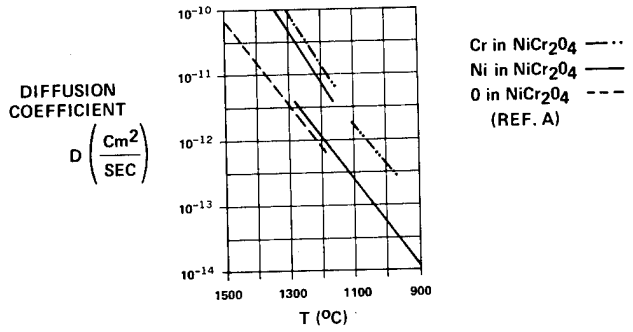


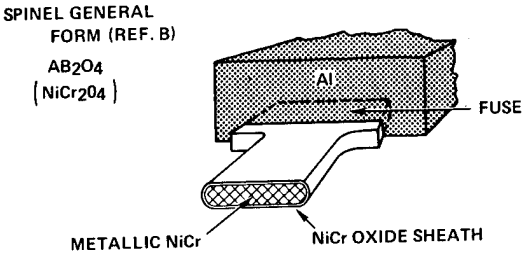
A – Handbook of Chemistry and Physics.
B – Thin Film Technology, R. W. Berry, et. al.
C – Japanese Metal Material Handbook, Y. Yamamoto, et. al.

Figure 1

OXIDATION OF NICHROME

- NiCr FORMS SELF LIMITING SKIN OXIDE
- SPINEL THICKNESS ≃ 20 Å
- PROMOTES RESISTOR STABILITY



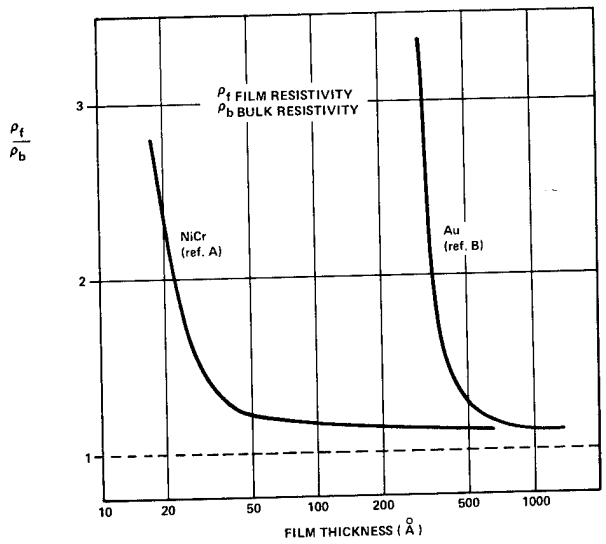


Ref. A – "Mass Transport in Oxides," NBS Publ. 296, (1968).
Ref. B – A. F. Wells, "Structural Inorganic Chemistry", Oxford Press (1950).

Figure 3

FILM VS. BULK PROPERTIES

- SHORT MEAN FREE PATH LENGTH OF ELECTRONS
- BULK RESISTIVITY IN THIN FILM
- GOOD FILM REPRODUCIBILITY



A – M. Nagata, et. al., Proc. Elec. Comp. Conf., 1969.
B – K. L. Chopra, Thin Film Phenomena, McGraw–Hill, 1969.

Figure 2

SCANNING TRANSMISSION ELECTRON MICROSCOPY ANALYSIS OF FUSES

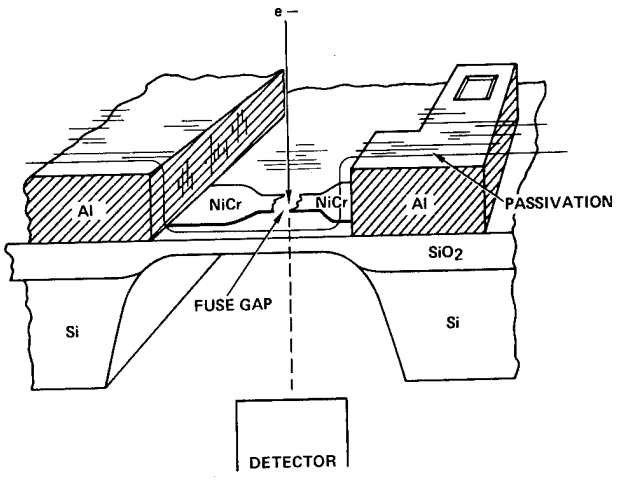
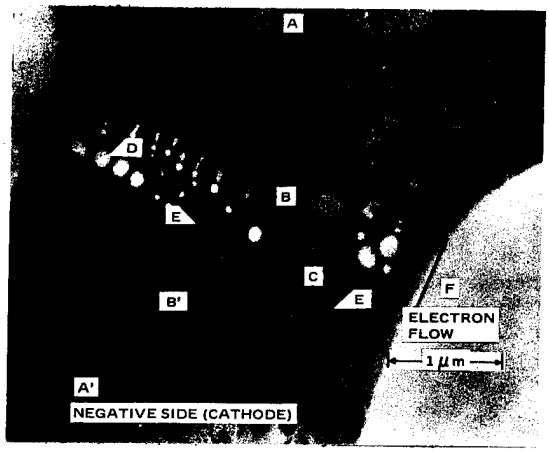


Figure 4

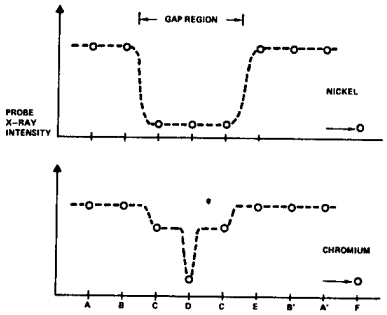
STEM PROGRAMMED FUSE

PROGRAMMING CONDITIONS:
POWER = 150 mW.
TIME TO FUSE = 2 μSEC.



POINT MICROPROBE ANALYSIS

A – NiCr
B – MELTED NiCr
C – SiO_2, CHROMIUM OXIDE
D – SiO_2
E – DENSIFIED NiCr
F – FIELD OXIDE (SiO_2)



NOTE: (A) "FROZEN SPLASH" EFFECT PROGRAMMING HAS MELTED NiCr IN GAP REGION.
(B) MASS TRANSPORT IN GAP.
(C) MASS ASYMMETRY TO NEGATIVE TERMINAL.

Figure 5

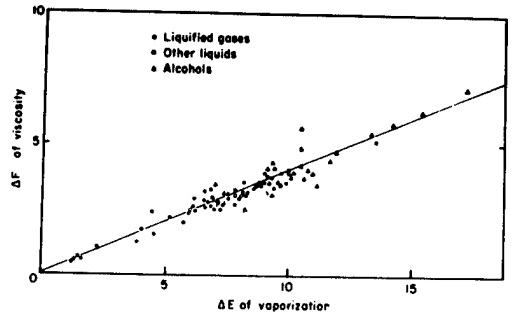


Fig. 11-24. Empirical relation between free energy of activation in liquids, ΔF, and energy of evaporation, ΔE, Rosevaere, Powell and Eyring.

Figure 7

TABLE II

Corrected ratio of energy of vaporization and activation for viscous flow

Metal	Average temp. °C.	ΔE_{vap} kcal.	ΔE_{visc} kcal.	$\frac{\Delta E_{vap}}{\Delta E_{visc}}$	$\frac{\Delta E_{vap}}{\Delta E_{visc}}\left(\frac{r_{ion}}{r_{atom}}\right)^3$
Na	500	23.4	1.45	16.1	2.52
K	480	19.0	1.13	16.7	3.41
Ag	1400	60.7	4.82	12.5	3.79
Zn	850	26.5	3.09	8.6	2.10
Cd	750	22.5	1.65	13.5	3.96
Ga	800	34.1	1.13	30.3	2.53
Pb	700	42.6	2.80	15.9	4.97
Hg	250	13.6	0.65	20.8	2.37
Hg	600	12.3	0.55	22.2	3.54
Sn	600	15.3	1.44	10.6	4.07
Sn	1000	14.5	1.70	8.6	3.30

TEMPERATURE PROFILE IN FUSE NECK FROM HEAT FLOW MODEL

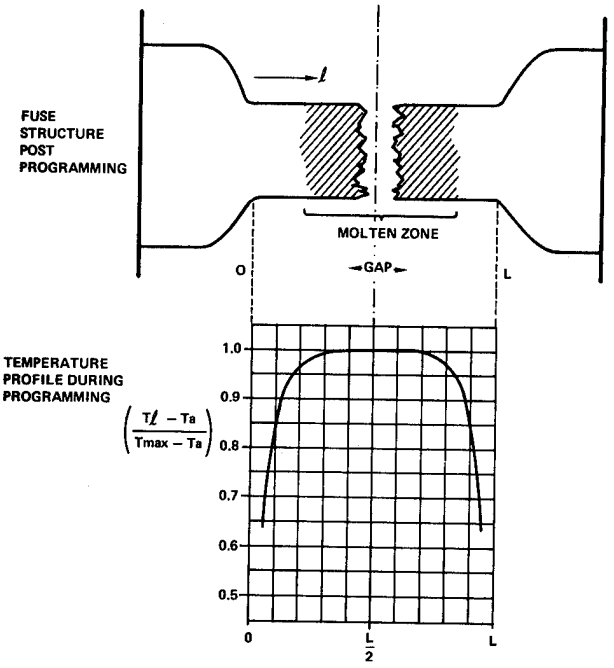
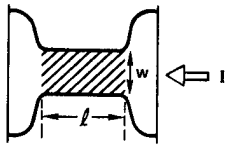


Figure 6

POWER DENSITY IN FUSE NECK REGION



$$\text{POWER DENSITY} = \frac{I^2 (\rho_s \ell / w)}{(\ell \cdot w)}$$

$\rho_s \ell/w$ = RESISTANCE OF THE FUSE NECK (OHMS)

ρ_s = SHEET RESISTIVITY OF NICHROME (OHMS/SQ)

$\ell \cdot w$ = AREA OF FUSE NECK (MIL.^{2})

ℓ = LENGTH OF FUSE NECK

w = WIDTH OF FUSE NECK

I = PROGRAMMING CURRENT ($I = V_F/R_F$)

Figure 8

DYNAMIC HEATING OF NiCr FUSE VS. POWER DENSITY

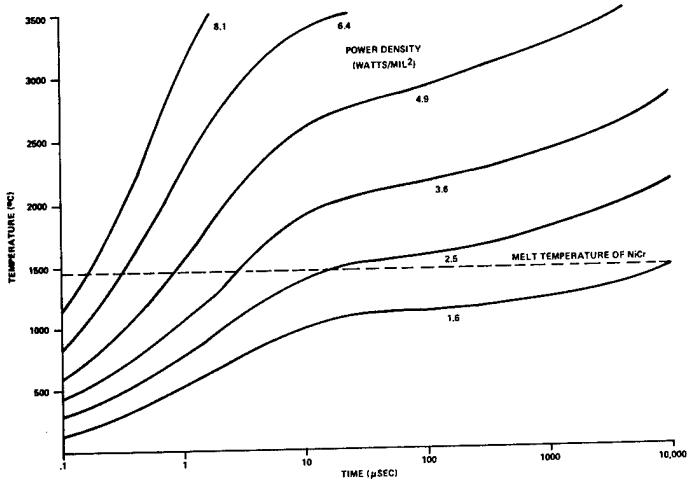
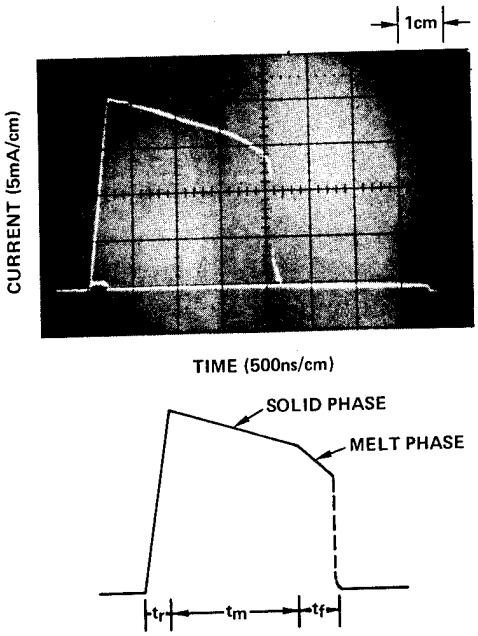


Figure 9

PROGRAMMING PULSE CHARACTERISTICS



t_r = RISE TIME OF PROGRAMMING PULSE

t_m = TIME FOR NiCr TO REACH MELT

t_f = TIME OF THE FUSING EVENT (IONIC MASS TRANSPORT)

Figure 11

POWER DENSITY VS. TIME TO FUSE

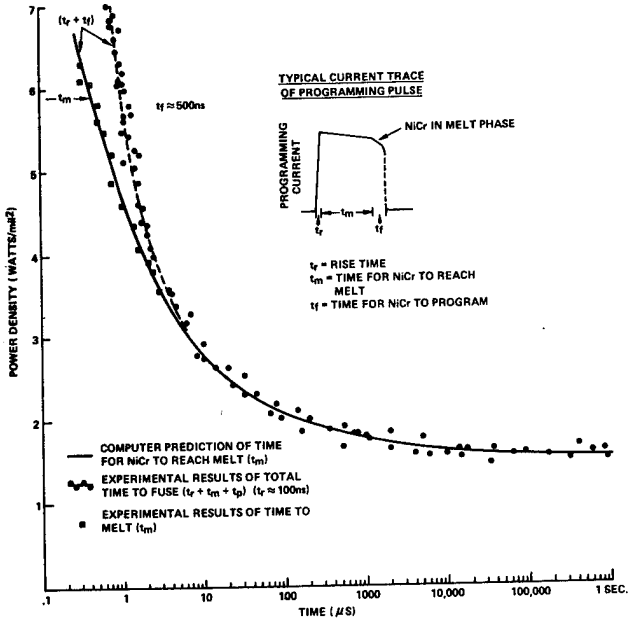


Figure 10

MAXIMUM FUSE TEMPERATURE VS. POWER DENSITY

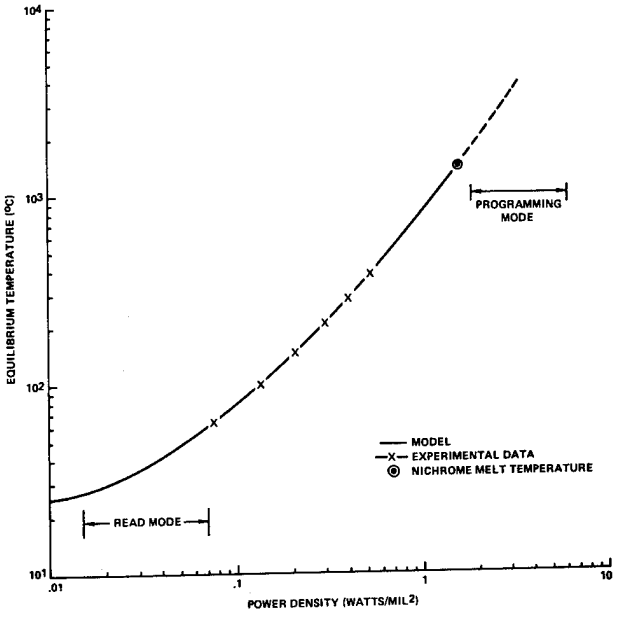
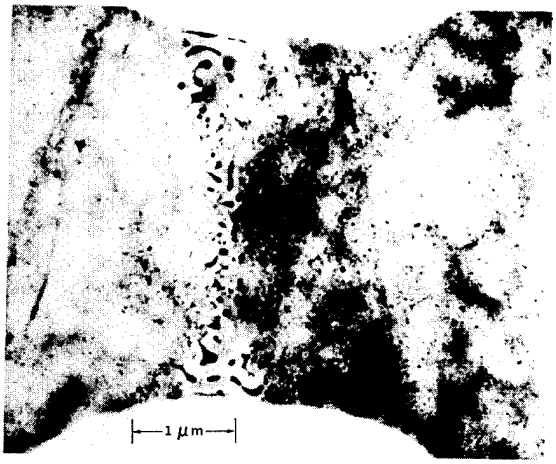


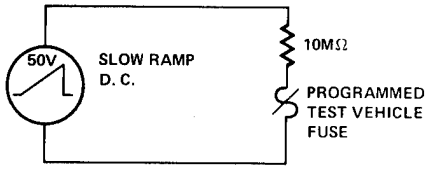
Figure 12

MARGINALLY PROGRAMMED TEST VEHICLE FUSE

PROGRAMMING CONDITIONS:
POWER DENSITY = 1.5 WATTS/MIL^2
TIME TO FUSE = 300 SEC.



FORCED RELINK OF MARGINALLY PROGRAMMED TEST FUSE



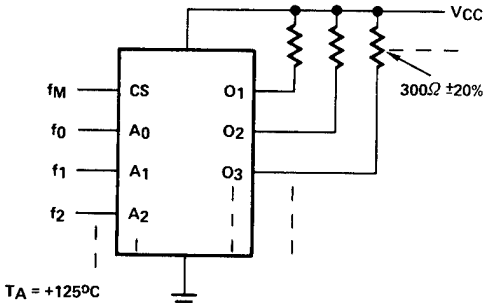
AT 12 VOLTS,
R_F DROPPED TO ≃5KΩ

Figure 13

OPERATING LIFE TEST RESULTS

	#DEVICES	#DEVICE-HRS	#FAILURES	ACTUAL FAILURE RATE	FAILURE RATE @ 60% C.L.(1)
ALL PROM TYPES	3840	9.030M	3(3)	0.03%/K HRS(4)	0.046%/K HRS(4)
				(MTTF - 3.3 x 10^6 HRS)	(MTTF - 2.15 x 10^6 HRS)
			DERATED TO 25°C	0.004%/K HRS	0.006%/K HRS
				(MTTF - 2.5 x 10^7 HRS)	(MTTF - 1.65 x 10^7 HRS)

BURN–IN SCHEMATIC



T_A = +125°C
V_{CC} = 5.5V
1MHz = $f_M = 2f_0 = 4f_1 = 8f_2 = \ldots$.

(1) C.L. (CONFIDENCE LEVEL)

(2) FUSE MATRIX: 50% PROGRAMMED RANDOM PATTERN AS PER PRESCRIBED PROGRAMMING PROCEDURE.

(3) NON-FUSE RELATED FAILURES

(4) SAME OR BETTER THAN MSI FAILURE RATES (REF. MDFR 1273 – ROME AIR DEVELOPMENT CENTER)

Table III

PROGRESS REPORT ON NICHROME LINK PROM RELIABILITY STUDIES

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Introduction

The basic element of the nichrome fusible-link Programmable Read-Only Memory (PROM) has been used for thin-film resistors in radiation-resistant integrated circuits for many years. Although the nichrome resistor has exhibited troublesome failure modes in the past, it has proven to be a reliable circuit element, provided that proper processing and packaging procedures are employed. In particular, nichrome resistors have failed because of electroplating,[1,2]* oxidation, [1,3] and formations causing poor contact to aluminum.[3,4] Electroplating and oxidation are correctable by hermetically sealing chips in a nitrogen ambient and in a package containing a minimum of glass, or by sealing packages at high temperatures during short periods of time. Electroplating and oxidation appear also to be eliminated by covering the integrated circuit with pin-hole and crack-free glassivation. High-contact resistance of aluminum to nichrome is minimized by good cleaning procedures, by relatively low-temperature processing after deposition of aluminum, or by exposing chips to high temperatures ($\geq$500°C) for short durations only.

Based on past history then, nichrome links to be used in programmable memories are potentially reliable, and attempts to accumulate reliability data by various users were made. Unfortunately, much of the data generated in the past is questionable, since customer programming conditions varied, programming specifications were volatile, and testing and screening of programmed parts was minimal, if performed at all. The total picture was further muddied by a lack of understanding of the fusing mechanism and by the reporting of a failure mode which appeared to be unique to the nichrome fusible-link PROM.[5] The fear caused by this regrow or revert failure mode was so pervasive that most changes of state were attributed to relinking, verified or not; analyzed or not. Further, if failure analysis was attempted, information was difficult to glean because of the submicroscopic nature of the failure mode and the destruction of evidence during test and analysis.

To clarify this situation, a study program was initiated to determine optimum programming conditions, test and burn-in requirements, and failure history. Coupled with an explanation of the fusing mechanism,[6,7] this report presents in-progress results of the study program including determined causes of the relinking mechanism found.

Controversy of Programming Conditions

At the outset of this study program, attempts were made to accumulate historical data. Surprisingly, it was found that programming conditions were not always known. When they were known, the conditions varied widely from vendors' specifications. For example, the manufacturers usually specify the rise time of the programming pulse to be from 1 to 200-μs. Yet, the regrow failure mode has been historically demonstrated by fusing links with rise times of seconds. Figures 1 to 3 are TEM photos depicting the character of such "slow blow" links. It is seen that the nichrome is minimally disturbed and exhibits miniscule gaps. On the other hand, Figure 4, typical TEM photos of links fused with 100-μs rise-time pulses, shows evidence of greater reaction and larger separation. These links blew on the rising portion of the applied pulse.

It became obvious that slow rise times of programming pulses limit the fusing current, and, therefore, limit the power delivered to the fuse link. It seemed inappropriate to do this, and it was, therefore, decided that parts programmed for this study would conform to the vendors' specified rise-times.

Curiosity, however, motivated an endeavor to determine how the ramp rate (voltage applied over unit time) might relate to the potential quality of a fused nichrome gap. For this purpose, test matrices of isolated nichrome links were fabricated by a manufacturer of nichrome link PROMs to his standard process at the time. Using the matrices, the time to fuse was measured as the ramp rate was varied. The results are given in Figure 5. It is seen that the time to fuse decreases exponentially with increasing ramp rate, reaching a minimum of about 250 ns for the composition and sheet resistivity of the nichrome tested.

The time to fuse was chosen as the dependent variable because the authors argue it is a parameter of first-order importance. The argument is simple: the faster energy is delivered to the link, the faster the link reacts, and less heat is conducted away by the surrounding silicon dioxide. Thermal studies at CSDL[8] have shown that only 1% of heat is conducted out through the nichrome and aluminum.

Carrying the argument further, the fusing model proposed here combines those of Kenney, Jones, and Davidson, et al. As the nichrome heats up, surface waves on the molten nichrome surface increase their amplitude, and the surface tension drops. As energy is rapidly delivered, the nichrome gets hotter and ionizes,

*Bracketed numerals refer to references in the List of References.

the surface tension decreases, and the surface area of the nichrome increases. At this point, a hole forms in the molten film and the nichrome begins separating. Speculation is divided as to the mechanism which generates the initial hole, either surface waves reaching an amplitude equal to the film thickness, or field migration of the charged ions. These are both self-consistent models but their relative magnitudes have not been experimentally determined. Then, once the gap forms, a plasma-like field migration of ions further segregates the nickel and chromium species. When a large enough gap is created by contraction of the cooling liquid, this plasma field migration is extinguished. Subsequently, the liquid nichrome sheet disintegrates into finger patterns as shown in Figure 4. If one could minimize surface tension and maximize field migration by inducing higher temperatures in the nichrome, then one might expect less residue material in the gap.

By inference, Figure 6, a link fused with a 20- to 30-ns rise time (but fused in the constant voltage part of the pulse), depicts the expected. That is, faster rise delivers proportionally more energy to the link and creates a less residue-filled gap. Unfortunately, this data is not yet considered conclusive since link geometries also varied. The geometry dependence, if any, will be determined as part of the ongoing study.

Although it was shown that the rise time of the programming pulse created important effects, other programming parameters required consideration. Next, how many pulses would be allowed? Although all vendors, at this time, suggest the use of multiple programming pulses, we concurred with the argument presented by Barnes and Thomas.[9] They suggest that fuses would react only in the direction of increased resistance. Therefore, less energy would be delivered during subsequent pulses making the quality of the fuse suspect. It was decided that only single programming pulses would be allowed.

Further, most manufacturers recommend 20% duty cycle during selection of links for fusing. Empirically, it was determined that a 20% duty cycle was yielding poorly due to under-programming. Based on the rationale that the chip was heating, the duty cycle was decreased to 10%, and V_{CC} was strobed, thereby decreasing the background temperature of the fusing circuitry. The programming yield on an in-house sample increased slightly.

Finally, two other programming variations will appear in the data. One, the current limit of the programming pulse, was initially inadvertently overly limited and was subsequently corrected. The other was a change in sequence of programming inspired by a recommendation from another agency.[10] The original suggestion was modified for ease of programming (see Figure 7), and selection is based on choosing the least resistive semiconductor paths for the first blows. This minimizes leakage paths and has greater yield impact as more links are programmed on the chip.

Yield and Reliability History

To understand part handling and flow, refer to Figure 8. A summary of a single vendor's fallout during this programming, assembly, and test flow is given in Tables 1 and 2. Reiterating, the parts were programmed to this vendor's specification except that only single-pulse programming was allowed, the duty cycle was decreased to 10%, and power strobing was instituted. The varied current limit and programming sequence conditions are listed separately.

Under-programming is defined as selected links not fusing, while over-programming occurs when unselected links fuse. Power strobe access time is a system application test. Under-programming, over-programming, and power strobe test are yield fallouts and have not been found, to date, to relate to reliability. Reviewing the yield parameters, it is observed that programming yield increased when partial programming along a base diffused-run was instituted. A further increase in programming yield is anticipated once full diffused-run sequence programming is implemented.

Table 3* lists all failures occurring during post-programming verify, burn-in, and system operation. Burn-in consists of a power-strobed sum-check operation at room temperature stressing each link for a total time of about 10 minutes. It is seen that the reverts appear to be the only reliability hazard generated as of this writing. Note, also, that most reverts occurred during burn-in, and one after burn-in. Laboratory data, however, shows that all reverts detected, to date, occur during the post-programming verify prior to burn-in.

Failure analysis of all these alleged regrow failures has revealed one processing procedure directly correlating to these failures. Discussion and analysis of these revert failures are given later in the discussion.

As an aside, it should be stated that in excess of 977,000 post burn-in PROM hours have been generated to date with one failure which was a revert. To calculate a failure rate at this time would be premature, since little time has been accumulated and corrective action is still being implemented.

Discussion of Reverts

Because of the submicroscopic nature of the revert failures, it was necessary to attempt to determine the physical size of possible bridging material in the gap of a fused link. Employing a blown link of a PROM with a measured resistance of greater than 10 megohms, a parallel external resistor was inserted into the circuit with point probes. This resistance was increased to determine the

*Data listed in Tables 1 through 3 was supplied to CSDL by J. K. Matthews of Raytheon Equipment Division. Raytheon is currently under contract to CSDL.

maximum resistance value which would ensure an output of "1". Note that for the PROMs tested, links are fused to create a "0". A revert then appears as a "1".

At V_{CC}=5.0 V, the critical resistance for a "1" was measured to be 3kΩ (see Figure 17). To ensure a "1" for V_{CC} less than 5.5 V, a critical resistance of 2.86kΩ was chosen. Powering the PROM at V_{CC}=5.5 V, with a 2.86-kΩ resistor inserted across the blown link, the "link" current was measured to be 480 μA.

Assuming the density, resistivity, and thickness of the nichrome bridge are the same as the original nichrome link, one can calculate the minimum width of the bridge, W, that would be required to support a "read" current of 480 μA and still not fuse.

$$W_{th} = \frac{I}{Jt} \qquad (1)$$

where

I = current through the bridge

t = thickness of the bridge (taken to be 200 Å)

J = current density necessary to blow the link

Various sources [5,11,12] indicate that the highest current density a link will tolerate prior to fusing is approximately 5×10^7 A/cm^2 for pulse widths greater than 10 μs. Using this value of current density as a rough approximation, the width of the bridge calculates to be 480 Å.

If the bridge is cylindrical, rather than a thin film, then

$$W_{cyl} = \left(\frac{4I}{J\pi}\right)^{1/2} \qquad (2)$$

Making the same set of assumptions for Eq.(1), W_{cyl} becomes 350 Å.

Fusing current densities have been calculated to be as low as 2×10^7 A/cm^2, which would make W_{th} max (Eq.(1))=1100 Å and W_{cyl} max (Eq.(2))= 875 Å. On the other hand, the density of the fused resolidified nichrome may increase,[6] thus potentially supporting higher current densities prior to fusing.

As stated earlier, this exercise was performed to determine magnifications necessary to view a filamentary bridge creating a regrow. The narrowest widths can only be seen with a minimum magnification of 15,000. If it were possible to remove the top glass layer without altering material in the fuse gap, these structures could be viewed with an SEM. The authors, however, have had better results with TEM samples prepared as previously reported.[13]

PROM Processing Procedures Contributing To Reverts

As shown in Table 2, eight verified revert failures have occurred to date. Additionally, seven verified revert failures occurred during post-programming verification tests of PROMs programmed at CSDL. All of these failures were exposed to reworked metal. Rework occurs when manufacturers choose to strip nichrome after the first deposition if resistivities, thickness, or registration of the metal are not within tolerance. Because of standard processing prior to stripping, the substrate thermal oxide is attacked such that a pedestal remains in the position of the removed nichrome link. Upon redepositing and redelineating, the second nichrome resistor tends to be misregistered relative to the first as depicted in Figure 9. The misregistration can appear as an X or Y translation, or both. Figure 10 is a TEM micrograph showing the misregistration and some discontinuity over the created silicon oxide step, the depth of which has been guessed to be anywhere from 20 to 100 Å. For a film of 100 to 200 Å, this represents a huge step. The rework procedure thus results in fabricating higher resistance links by a factor of 2 or more because of shadowing during deposition.

Rework can be viewed optically, as shown in Figure 11, where a ridge in the nonfused link is visible. Compare this with an unreworked nonfused link in Figure 12. Even the character of the fused gap appears different optically. Comparing the fused reworked links in Figure 13 to a typical non-reworked link shown in Figure 14, the reworked links show narrower gaps with and without a tendency to blow over the oxide step. The amount of material fused on the step is an indication of the resistance of the nichrome over the step. Very thin nichrome may have such a high resistance that it will not blow. Figures 15 and 16 show TEM micrographs of fused reworked links on a chip with a verified revert. Comparison of these to Figure 4 again shows characteristic differences which are still subject to interpretation. Based on previous arguments, one could speculate that the higher resistance would limit the delivered power, and, therefore, the amount of reacted nichrome, thus relatively amplifying surface-tension effects and minimizing the ion migration in the impressed field. The resistance might be so high that it would preclude any melting whatsoever.

Unfortunately, capturing a revert failure alive has been difficult. These failures have occurred only on reworked parts, but not necessarily on all reworked parts. Even then, only one or two links per chip revert. Often, the links refuse during debugging and verification. Hard failures, however, are in hand and are being TEM analyzed.

Discussion of Revert Mechanisms

Several theories of the revert mechanism have been forwarded. Thermal intermittents, arc-over, or ion migration in large impressed electric fields have been the most popular. The possibility of thermal intermittents caused by metal expansion across narrow gaps, however, had to be discounted. The reason is: reverts can be induced on probed reworked fused links, or slow-blow isolated test links with no heat generated. A pulsed voltage (15 to 30 V for 500 ns) impressed across these

links was sufficient to occasionally create a regrow. No correlation to elevated temperature has been found.

The high electric field is the most likely triggering force. The high field force could be created across small silicon oxide steps as in reworked parts, or across narrow gaps caused by excessively limited fusing currents.

It should be emphasized that the cosmetic appearance of the gap of a fast blown non-reworked link has not proven to be a good measure of its potential to revert. The only correlation to revert possibility found, to date, is the rework process, provided the fuse is blown properly. Furthermore, the appearance of reworked links in the area where fusing has occurred over the step resembles the gap of a slow-blow link. In particular, the average gap is very narrow in both cases. Nevertheless, if cosmetic comfort is required, typical gaps as shown in Figure 6 can be created. Whether the geometry or the circuit design allowing super fast rise time at the link, or both (or other factors), is the predominant effect, is not known at this time.

Recommended Programming and Screening Conditions for Nichrome Link PROMs

Although the PROM study program has not been completed, the following interim recommendations for finalizing a potentially reliable nichrome link PROM should be considered:

(1) Programming to the vendors's specification should be required as a minimum. These specifications have evolved empirically and are statistically oriented to programming yield. The only recommended exceptions are the single-pulse criterion, decreasing the duty cycle to 10%, and power strobing.

(2) Excess marginal low and high V_{CC} testing which has previously been reported,[14] and which has become part of some vendors' post-programming recommended testing should be performed. The intent is to detect marginally fused links. Referring to Figures 17 and 18 where the operating range is guaranteed between 4.5 and 5.5 V, the circuit threshold resistance for marginal "1" and marginal "0" can only be detected by exceeding the operating voltage range. The more the operating range of V_{CC} is exceeded, the larger the detectable variations in link resistance. Where the unprogrammed fuse will measure in excess of 10 megohms, a marginally fused link could be as low as several thousand ohms and still give a "0" output, or fuse to 1 kilohm and still give a "1" output. The exact values of threshold resistance depend on the circuit implementation. To detect a marginal "0", the authors have found that a V_{CC} level as low as 3.8 V is necessary, in line with some vendors' specifications. Detection of a marginal "1" may require a V_{CC} as high as 6 V. The reader should be warned that by decreasing V_{CC} to less than 4.0 V, a potential exists that good parts could be rejected as well as detecting marginally fused links. So far, this study has not shown that good parts were rejected; some bad parts have been rejected by the V_{CC} screen.

(3) Do not allow metal rework procedures if prior processing is such that a silicon oxide step can be created. The step can be detected by visual inspection of the chip at magnifications in excess of X300.

(4) PROMs should be statically burned in before and dynamically burned in after programming. Fortunately, most reverts occur rapidly. The data presented previously showed that most of the reverts occurred during the short stress times induced in the test-verify cycle. A few more, however, were generated during burn-in with one burn-in escape. Now here is the concern: a week of burn-in can be misleading. Depending on the pulse width and repetition rate, the total accumulated time on a link of a 1-k PROM can be amazingly small. For example, in this study, the total time in one 168-hour burn-in implementation was 6.56 minutes; in another, 19.7 minutes. The burn-in escape occurred after 70 minutes of total link time. In addition, elevated temperature does not appear to accelerate regrow. Nevertheless, it is believed that with:

   (a) Implemented corrective action relating to rework.

   (b) Proper programming.

   (c) Excess marginal V_{CC} testing.

   a 1-week room temperature burn-in post programming will be sufficient to detect reverts.

Table 1. PROM yield, sequential programming, April 1976.

I_{LIMIT}=200 mA		I_{LIMIT}=140 mA		
PART FALLOUT	%	PART FALLOUT	%	
58	11	76	10	Under-Programmed
13	2.6	36	4.8	Over-Programmed
-	-	1	0.1	Under- and Over-Programmed
13	2.6	10	1.3	Power-Strobed Access Time
1	0.2	10	1.3	Post-Programming Verify
7	1.4	3	0.4	Other
4	0.8	7	0.9	Burn-In Failure
-	-	1	0.1	System Failure
411	81	612	80.8	Total Surviving
507		757		TOTAL PROGRAMMED

Table 2. PROM yield, partial diffused-run programming, April 1976.

I_{LIMIT}=200 mA		I_{LIMIT}=140 mA		
PART # FALLOUT	%	PART FALLOUT	%	
102	7.2	18	4.2	Under-Programmed
46	3.2	11	2.5	Over-Programmed
-	-	10	2.3	Under- and Over-Programmed
9	0.6	-	-	Power-Strobed Access Time
12	0.8	1	0.2	Post-Programming Verify
-	-	-	-	Other
13	0.9	-	-	Burn-In Failure
-	-	-	-	System Failure
1242	87.8	393	90.8	Total Surviving
1416		433		TOTAL PROGRAMMED

Figure 1. Slow-blow nichrome link TEM (tr = 1 s)(X20 k).

Table 3. Burn-in failures.

SEQUENTIAL PROGRAMMING Part Fallout	PARTIAL DIFFUSED-RUN PROGRAMMING Part Fallout	REASON
2	5	Reverted Logic State
2	-	Glitching Output
6	7	Out of Specification Output Voltage
1	-	All "1"'s

Other

Incorrect Pattern
Parts Broken in Handling
Pattern Revision
Programming Station Failure

System Failure was a 0 → 1 Revert

Post-Programming Verify

- Allow Address Lines to Settle
- Apply V_{CC} = 4.0 Vdc
- Read Output Level

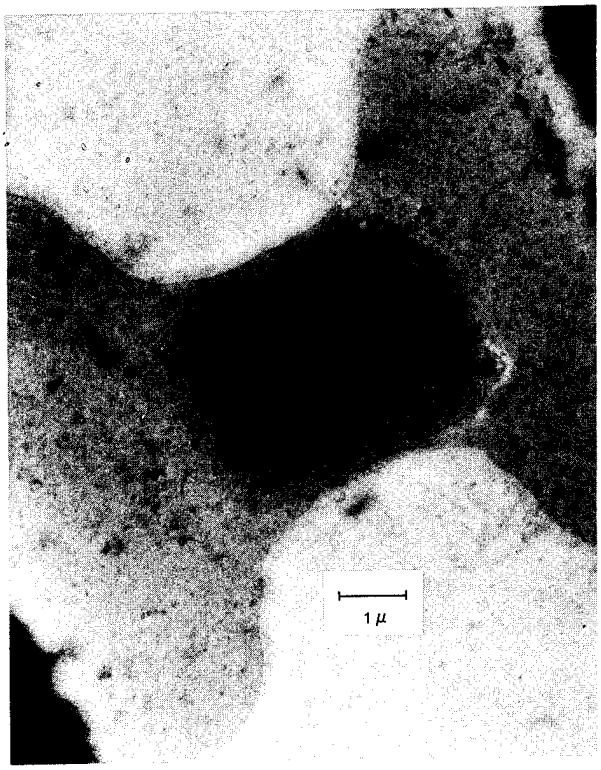

Figure 2. Slow-blow nichrome link TEM (tr = 1 s)(X17 k).

Figure 3. Slow-blow nichrome link TEM (tr = 1 s)(X13 k).

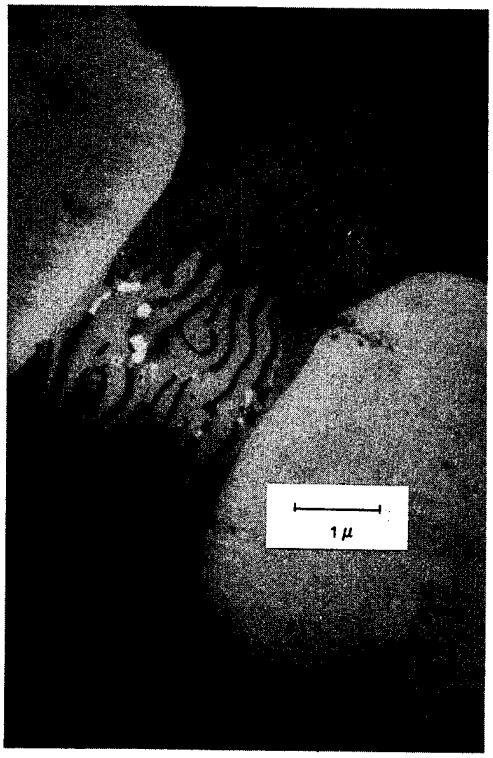

Figure 4b. TEM of nichrome link that blew on the rise (tr = 100 μs) (X28 k).

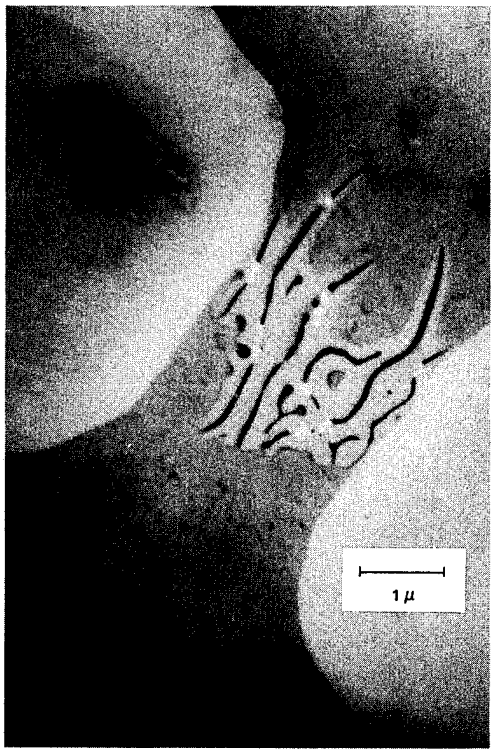

Figure 4a. TEM of nichrome link that blew on the rise (tr = 100 μs) (X28 k).

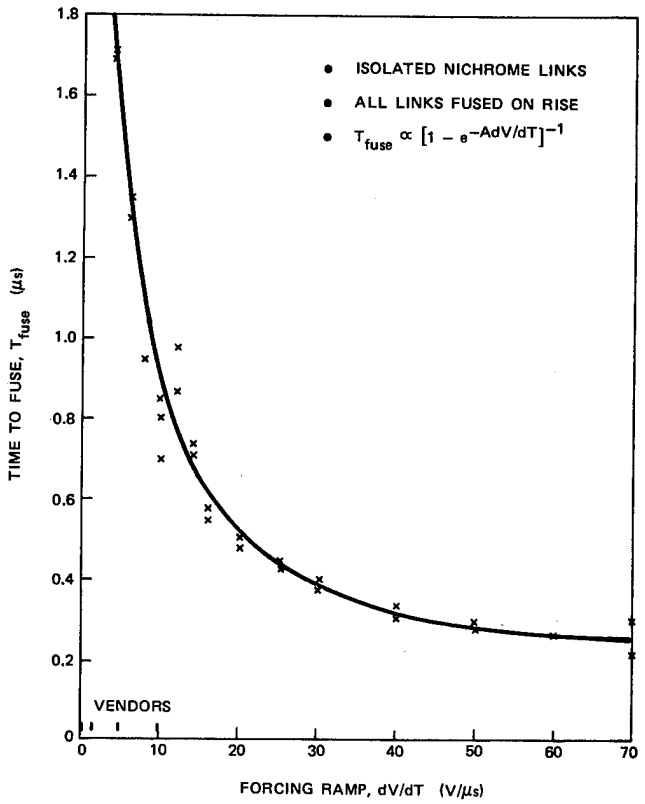

Figure 5. Exponentially decreasing time to fuse with increasing ramp rate.

Figure 6a. TEM of nichrome link that blew on the flat (20-ns rise)(X38 k).

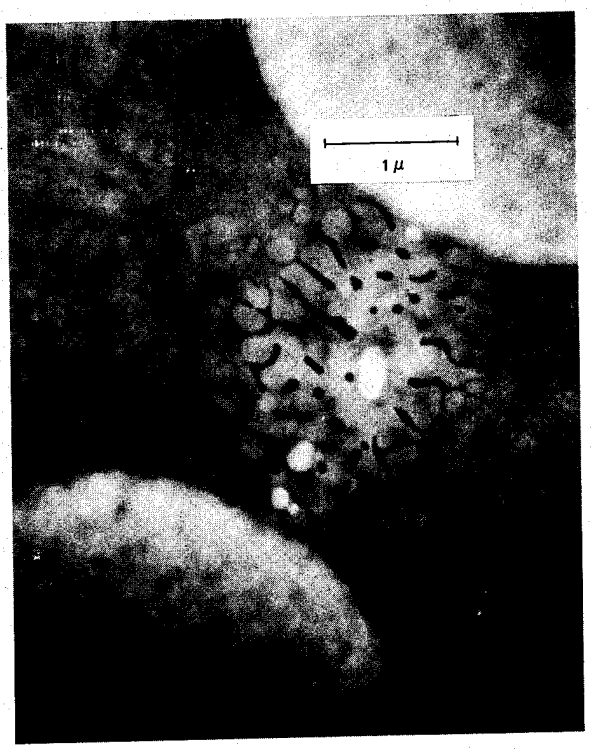

Figure 6b. TEM of nichrome link that blew on the flat (20-ns rise)(X34 k).

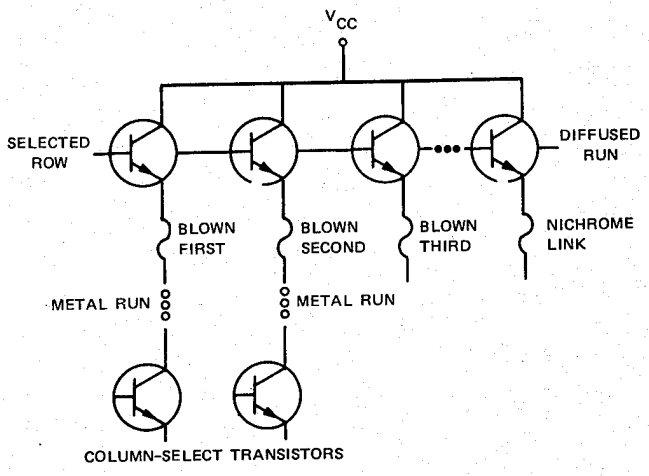

Figure 7. Programming along diffused run.

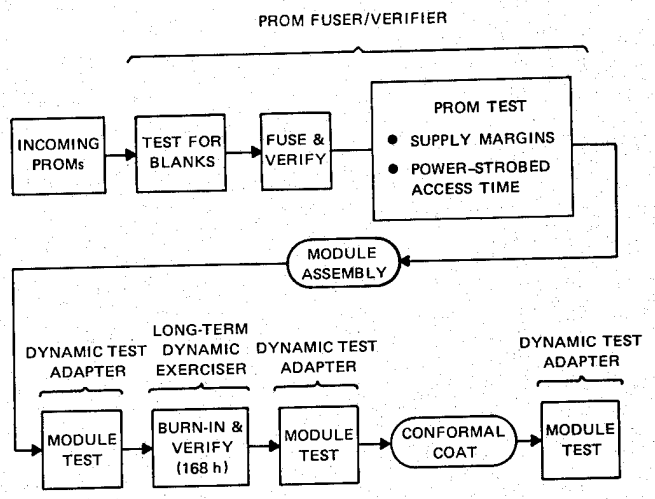

Figure 8. PROM flow diagram.

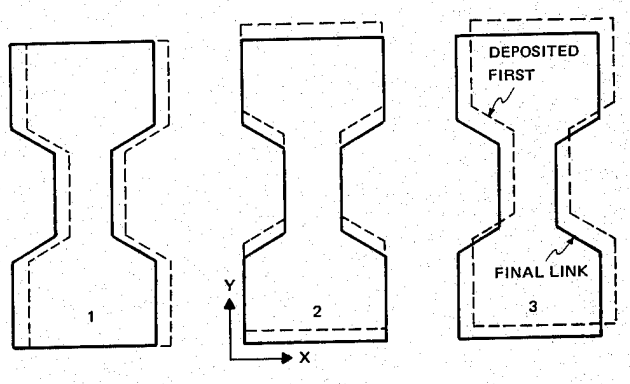

Figure 9. Reworked nichrome link misregistration.

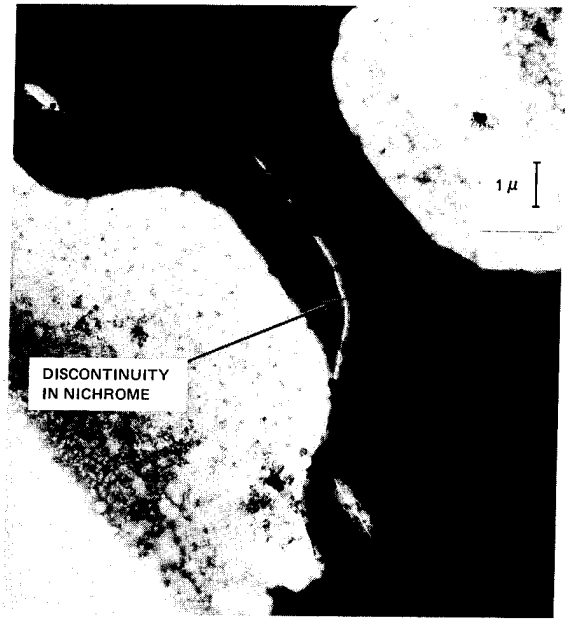

Figure 10. TEM of unfused reworked nichrome link (X12 k).

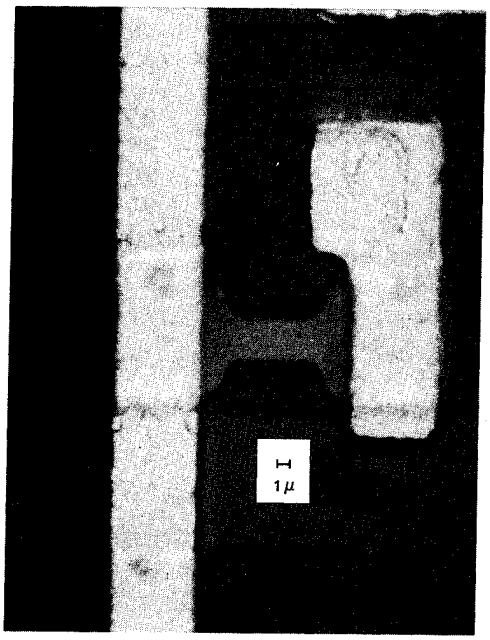

Figure 12. Photomicrograph of unfused unreworked nichrome link (X2 k).

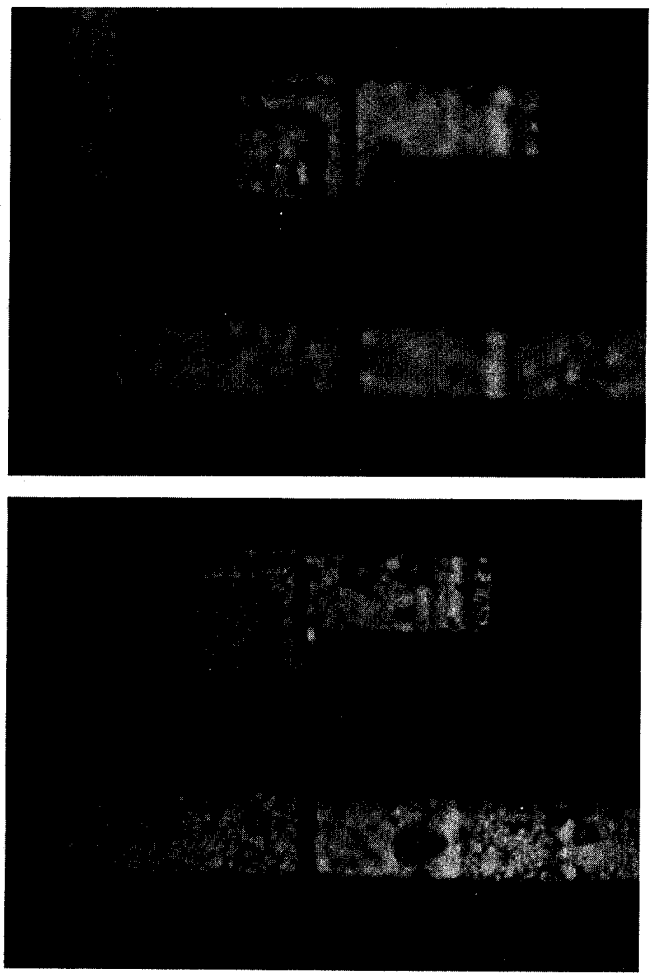

Figure 11. Photomicrographs of unfused reworked nichrome links (X2 k).

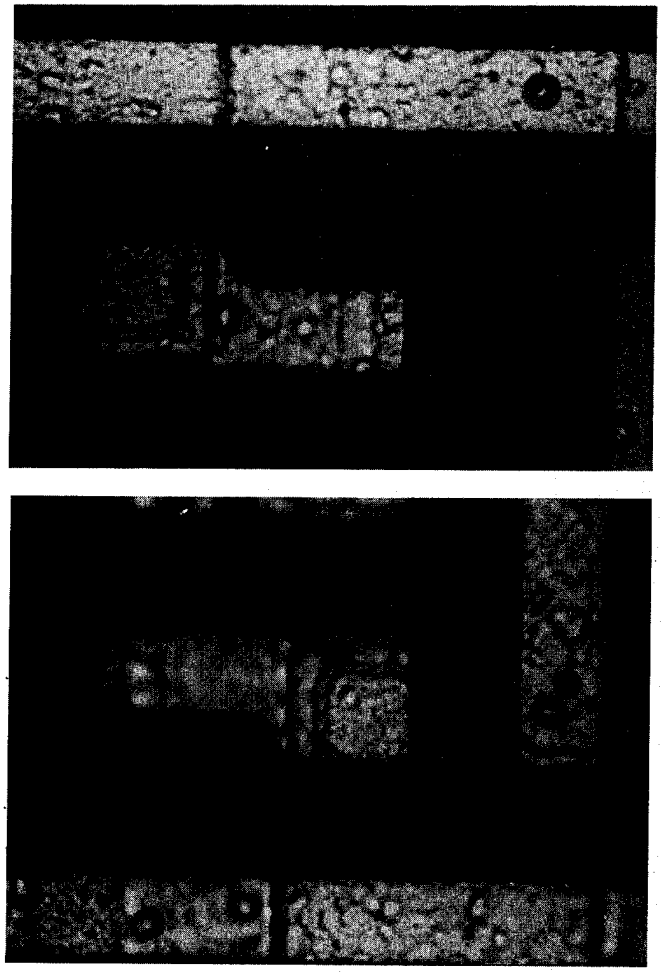

Figure 13. Photomicrographs of fused reworked nichrome links (X2 k).

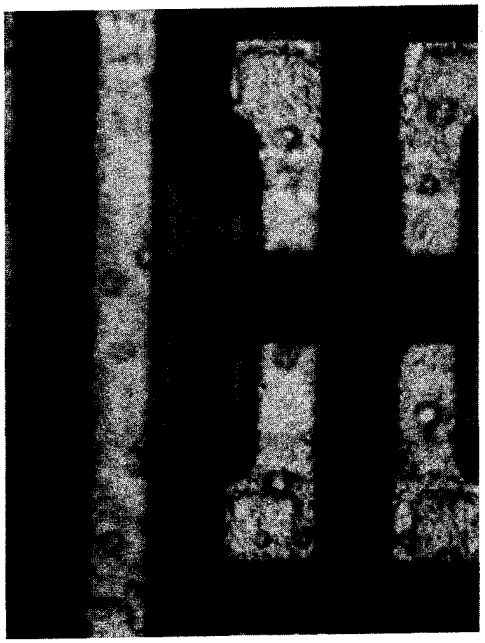

Figure 14. Photomicrograph of fused unreworked nichrome link (X2 k).

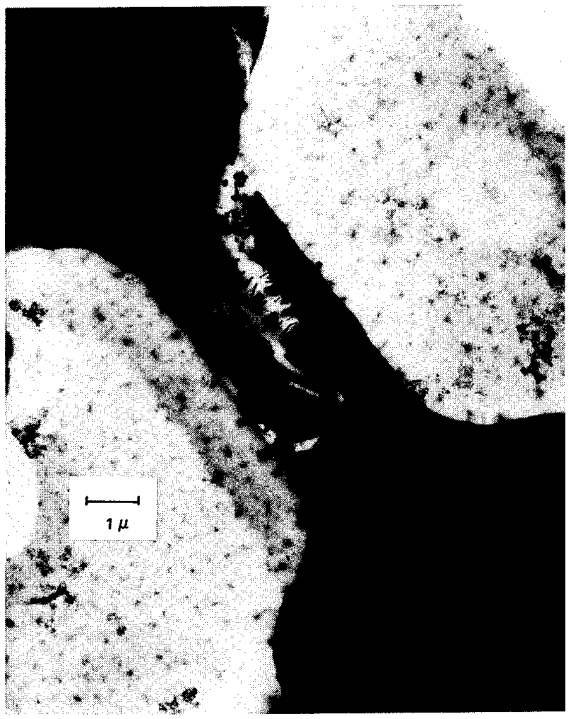

Figure 15. TEM of fused reworked nichrome link (X12 k).

Figure 16. TEM of fused reworked nichrome link (X16 k).

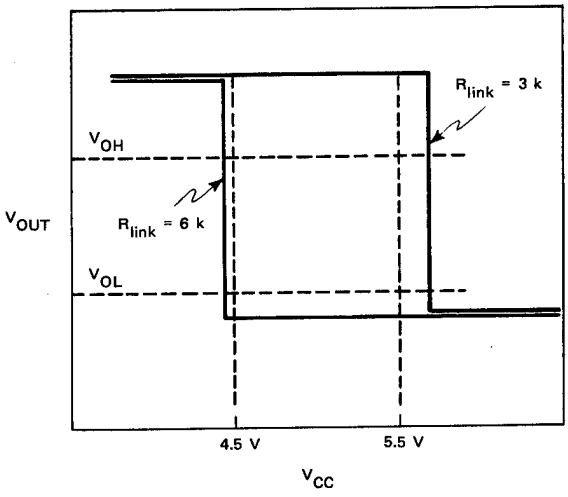

Figure 17. Detection of marginal links with high resistance.

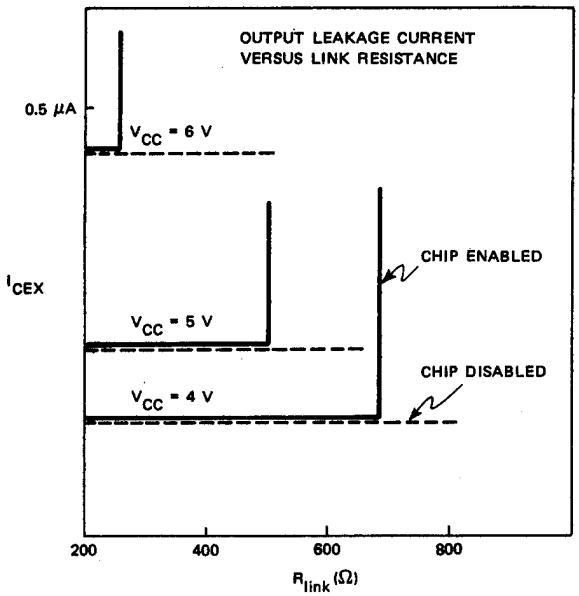

Figure 18. Detection of marginal links with low resistance.

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Acknowledgment

Many thanks to Stefan Solohub, Jr., who turned out samples for optical and SEM examinations and who did most of the electrical testing; W. Kinzy Jones, under whose direction samples were prepared for TEM analysis; George Kenney, who always managed to turn out TEM glossies; and Donald Powers, who designed and built the PROM fuses and programmed some parts used in the studies.

DEVELOPMENTS IN DUAL DIELECTRIC CHARGE-STORAGE (DDC) REPROM (REProgrammable Read Often Memories)

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Abstract

There has been an increasing interest in recent months in the dual dielectric metal insulator semiconductor (MIS) cell as a nonvolatile semiconductor memory element. A true nonvolatile semiconductor memory could replace the omnipresent magnetic memory because associated with it one also expects fast access capability as well as interface compatibility with other semiconductor logic circuits. Key features in such a semiconductor memory cell, then are; true nonvolatility, high-speed access capability and ease of write-erase operations. The development of the dual-dielectric charge-storage (DDC) cells have followed two parallel paths, both enjoying a limited success yielding commercial products. The first centers around the concept of the floating gate, an artificially created metallic charge-storage site located at the dual dielectric interface. The second uses the naturally occurring interfacial states existing at the dual-dielectric interface as the charge storage sites, as in metal-nitride-oxide-semiconductor (MNOS) memory transistors. The advantages and disadvantages of these two approaches to the realization of DDC cells is reviewed briefly. And then the concept of the interfacial dopants,[1] the heart of this paper, emerges as a particularly beneficial compromise between these two concepts, resulting in an optimum DDC cell, with true nonvolatility, yet with undemanding write-erase conditions.

It is shown in this paper that when suitable interfacial dopants such as W are introduced in a well-defined concentration range, the write-erase characteristics of dual-dielectric charge-storage cells are enormously improved. The upper limit of the dopant is dictated by its influence on the dielectric properties of the outer layer and is determined to lie at about $10^{15}/cm^2$ for Al_2O_3. Cells with $5x10^{15}/cm^2$ interfacial dopants showed marked increase in charge leakage. The lower limit is determined to lie at about $10^{14}/cm$ by comparison with cells with no interfacial dopants.

The improvement in write-erase characteristics of these cells is of such a magnitude as to allow using relatively thick SiO_2 layers (greater than 50 A) in these cells, which is mandatory for long memory-retention time (longer than 20 years at 100 C). (Detailed studies of retention time have been published separately.[2]) This study indicates that cells with thinner outer layers (approximately 300 A of outer layer and approximately 60 A of SiO_2) that would operate at gate-pulse voltages in the 25-V, 1-μs range, should be feasible.

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RELIABILITY STUDIES OF POLYSILICON FUSIBLE LINK PROM'S

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Abstract

Reliability aspects of polycrystalline silicon fusible link PROM's have been investigated and discussed in terms of manufacturing and accelerated lifetesting. Lifetest data indicate that the "grow back" failure made operative in nichrome fuse PROM's is not present in polysilicon fuses. Failure rates associated with the fuse structure are considerably below the inherent failure rate of the bipolar device.

Introduction

The purpose of this paper is to present reliability data on polysilicon fuse Bipolar Programmable Read Only Memories (PROM's). The paper is divided into the following sections: (1) a brief description of device operation, (2) a discussion of polycrystalline silicon fuse technology, (3) an overview of the operating failure mechanisms in PROMS, (4) a listing of the testing methods used to measure the reliability of PROM's, and (5) a discussion of the results of the reliability testing along with calculated failure rates.

Device Description and Operation

Intel's family of high density 1K, 2K, and 4K (open collector and tri-state outputs) PROMS were used in this study. The PROMS were sealed in 16 pin (1K and 2K) or 24 pin (4K) hermetic Cerdip packages. All units were 100% tested for hermeticity and AC and DC parameters.

The operation of each of the PROM devices is similar. Each cell consists of a transistor and a fuse connected by row and column select lines. The device also contains sense amplifiers and row and column decoders. Figure 1 shows a typical cell schematic and Figure 2 shows a scanning electron photograph of a single cell. During programming, the output state of the cell is changed by forcing a current of approximately 30 mA through the fuse, causing the fuse to melt and open.

Polycrystalline Silicon Technology

The fuse element in the PROMS is composed of polycrystalline silicon. At the appropriate stage of device processing, a polysilicon layer of approximately 3500 Å thickness is deposited using standard chemical vapor deposition techniques. This film is then selectively etched to the hour glass shape shown in Figure 3. Next the fuse is doped to the desired resistivity and the remaining manufacture follows the normal bipolar process to completion. A cross section of the cell structure is illustrated in Figure 4.

One novel aspect of the cell construction is shown in Figure 5. The surface passivation layer is removed from the active region of the fuse. The reason for this is two-fold. First, this exposes the fuse to the oxygen environment in the Cerdip package cavity. When the fuse blows, there is some silicon oxidation in the opened area which provides an additional dielectric barrier to inhibit regrowth. Also the absence of an encapsulating layer over the fuse aids in programming as the molten fuse is free to change shape (open) when subjected to the programming current pulse train. Exposure of the silicon fuse to the atmosphere is possible because of the hardness and corrosion resistance of silicon. This contrasts the situation for nichrome fuses where a protective surface layer is required.

Fuse dimensions are critical to both programmability and reliability. The fuse cross section must be small enough to be readily programmed yet not so small that the fuse will inadvertently program during a normal read operation. For reference, a current of 30 mA is typically used to burn out a fuse whereas the sensing current is nominally 2 mA. Below we will consider the temperature rise in the fuse associated with current flow in this range. First, however, we describe control of the fuse dimensions.

The polysilicon thickness is controlled to 3500 ± 400 Å. The width of the fuse is targeted at 2.2μ. However, as the fuse is patterned using normal photolithographic techniques there is always some variation in fuse width. Visual inspection of fuses on a number of wafers allows a determination of the expected size distribution. A typical histogram of fuse widths is shown in Figure 6. These data represent random measurements on 1K, 2K and 4K PROMS. The fuse widths follow a normal or Gaussian distribution and thus allow an estimate of what fraction of the fuses have a width greater than a certain minimum. For the data shown in Figure 6, 99.99% of all fuses are 1.0μ or wider. We shall show in a following section that fuse widths greater than 0.3μ are stable during device operations. As 0.3μ is considerably below the observed range of fuse widths, we conclude that adequate device fabrication technology exists such that programming during read operations should not represent a reliability hazard.

Programming of the polysilicon fuses occurs by a melting and "pull back" mechanism similar to that observed in standard wire element fuses. A scanning electron photograph of a blown fuse is shown in Figure 7. The "pull back" of silicon on one side of the fuse is clearly evident. It is interesting to note that the pullback always occurs toward the negative terminal of the fuse. The exact mechanism causing this phenomenon is not understood, although, it may be due to electromigration in the liquid state when the fuse is molten.

Simple heat flow calculations show that the programming current will readily melt the fuse in the notch area. For example, a 2μ wide fuse will melt in ~1 μsec during programming with a current of 30 mA. Conversely, the temperature rise expected in a similar fuse during a read operation is only about 20°C.

Prom Failure Mechanisms

The primary failure mechanisms in PROMS are (1) relinking or "grow back", (2) programming during read, and (3) non fuse related failures. Following is a brief discussion of each of these mechanisms.

The phenomenon of "grow back" has the effect of making a programmed fuse look like an unprogrammed fuse after some period of time. (1, 2, 3) This failure mode is nonexistant in polysilicon fuse PROMS because of the high activation energy for silicon migration (several eV) and the oxide layer which forms

when the fuse burns out. In some instances, marginally programmed fuses may give the appearance of "grow back". Resistive fuses under worst case temperature (high) and V_{CC} (low) conditions may appear unprogrammed. Fuses of this type can be screened by AC testing under the above conditions after the programming step.

Programming during read occurs when fuses are too narrow and, therefore, may be opened by the relatively low read current. As a test of fuse reliability as a function of fuse width a series of PROMS were purposely processed to give narrow fuse widths. For these PROMS the average fuse width was 0.8μ with minimum sizes below 0.3μ. Tests were run on unprogrammed PROMS and devices programmed with a checkerboard pattern. Appendix A describes the test details. The data in Table 1 show that program during read occurs only for very narrow fuses (less than 0.3μ in width). Targeting fuse widths greater than about 1.0μ makes this failure mode nonexistent for polysilicon fuse PROMS.

Non-fuse related failures are those not directly attributable to the fuse element. Included are specific failures in decoder and sense amps or gross failures such as metal defects, contamination, etc.

Table 1

Influence of Fuse Width on 1K PROM Reliability
1000 Hour, 125°C Dynamic Lifetest

Device	No. Units	Failures	Failed Fuse Widths
Narrow Fuse Unprogrammed	360	1	<0.3μ
Narrow Fuse Programmed	160	2	<0.3μ
Standard Fuse Programmed	1000	0	—

Reliability Testing

In this section we present data from four different types of lifetest on polysilicon fuse PROMS:

- 125/160°C Burn-In Monitors
- 85°C System Lifetests
- 125°C Dynamic Lifetests
- 250°C Drift Tests

Burn-in monitors are used to continuously track device production quality and examine infant mortality rates in a relatively large number of units. The data shown in Table 2 were obtained from a mixture of 1K, 2K and 4K devices. Units were unprogrammed and dynamically stressed where each cell is sequentially addressed and read (Appendix A).

Table 2

Cumulative Burn-In Monitor Results on Polysilicon Fuse PROMS - 48 Hour, Dynamic Burn-In

No. Units	Temp.	Failures	Cause
10,000	125°C	3	Fab Defects Non-Fuse Related
1,000	160°C	0	

In the 85°C systems lifetest devices are exercised in a manner similar to actual operating conditions with device functionality being continuously monitored (see Appendix A). Long term tests are conducted as well as cycling a 32 unit system through 1000 hour tests. The results of these studies are shown in Table 3.

Table 3

85°C Systems Lifetest on 1K PROMS

No. Units	Program State	Hours	Failures
32	50% Programmed	20,000	0
32	Unprogrammed	30,000	0
288	Unprogrammed	1,000	0

The 125°C Dynamic Lifetests are similar to the 85°C systems test except for test temperature and the fact that the devices are not continuously monitored for failures. In addition, access times were monitored on a sample basis to insure device stability. The results of these tests are shown in Tables 4 and 5. All units were programmed to a checkerboard data pattern and AC tested prior to lifetest. The PROMS were not burned-in prior to lifetest.

Table 4

1000 Hr., 125°C Lifetests on Silicon Fuse PROMS

DEVICE	NO. UNITS	ACCESS TEST 25°C, V_{CC} = 4.5V	FAILURES
1K PROM	1000	60 ns	0
2K PROM	900	80 ns	0
2K PROM	300	80 ns*	2 (1 marginally programmed fuse; 1 nonfuse related)
4K PROM	350	80 ns	0

*Initially tested at V_{CC} = 5.0V. Marginally programmed unit would probably have been screened with low V_{CC} test.

Table 5

Access Time Stability - 125°C Dynamic Lifetest

DEVICE	NO. UNITS	WAFER LOTS	AVERAGE ACCESS TIME*, ns INITIAL	500 HRS	1000 HRS
1K PROM	36	4	47.6	48.1	48.2
2K PROM	83	5	48.8	49.0	49.5
4K PROM	133	9	54.7	55.0	55.2

*Data taken at 25°C with V_{CC} = 4.5V

The 250°C high temperature bias test is used to detect failure mechanisms with high thermal activation energies. The static bias condition shown in Appendix A was employed and access times were measured (see Table 6). No device failures or significant access time degradations were observed.

Table 6

250°C Drift Test Results

DEVICE	NO. UNITS	WAFER LOTS	AVERAGE ACCESS TIME*, ns INITIAL	8 HRS	16 HRS
2K PROM	20	4	47.5	48.6	48.8

*Data taken at 25°C with V_{CC} = 4.5V

The results of the above tests are summarized in Table 7. Failure rate predictions at 75°C are made using an activation energy of 0.4eV. Although the 0.4 activation energy is typically used for bipolar devices, it should be noted that the appropriate activation energy for fuse related failure mechanisms is probably much higher. However, because of the lack of failures associated with fuses, it is apparent that any effort to ascribe a failure rate to the polysilicon fuses will be meaningless in that the fuse failure rate will be much lower than the inherent bipolar device failure rate.

Table 7

Failure Rate Predictions

Table 7: Failure Rate Predictions

TEMPERATURE°C	DEVICE HOURS	EQUIVALENT 75°C DEVICE HOURS	FAILURES	FAILURE RATE, %/1000 HRS 75°C, 90% CONFIDENCE LEVEL
85	1,888K	2,643K	0	
125	4,030K	19,747K	5	
160	48K	571K	0	0.04
250	0.32K	22K	0	
TOTAL	5778K	22,983K	5	

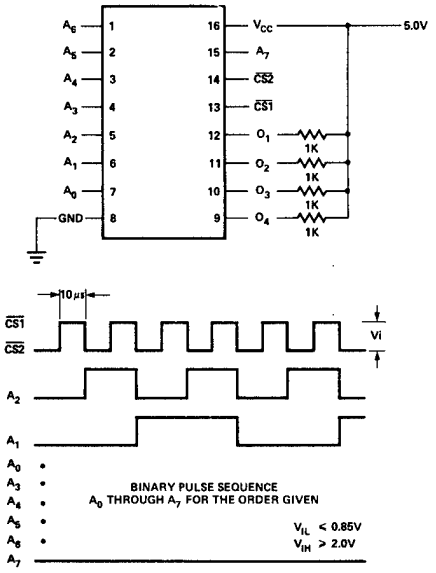
Summary

The reliability of polysilicon fuse bipolar PROMS has been discussed with respect to failure mechanisms and accelerated lifetesting. The data indicate that the polysilicon fuses do not impact the inherent reliability of the bipolar structure. 75°C failure rates are predicted to be 0.04% per 1000 hours at a 90% confidence level.

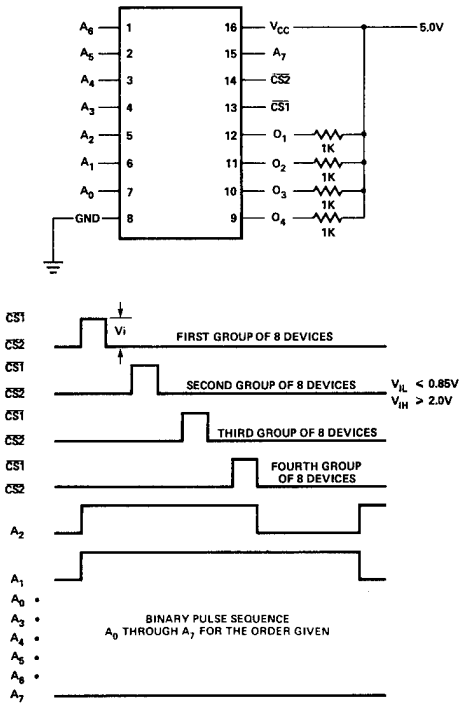
Appendix A

PROM Test Conditions

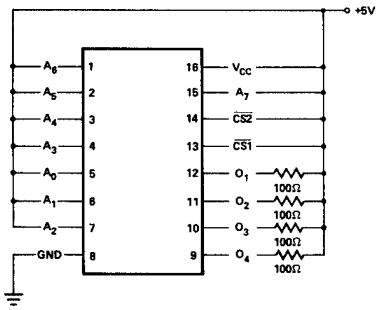
Dynamic Life Test Connections and Timing.



Rotating Life Test Connections and Timing.



HTB Configuration.



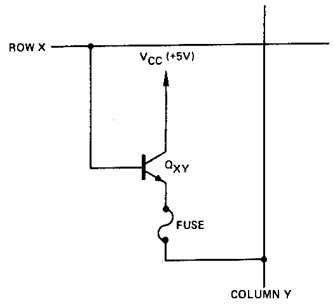


Figure 1
Schematic of PROM CELL

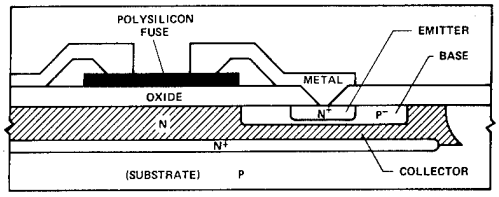


Figure 4
Cross Section of PROM CELL

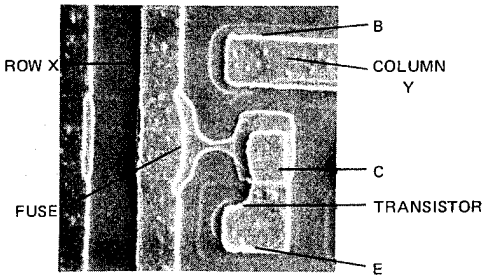


Figure 2
SEM Photograph of PROM CELL

Figure 5
Hole in Surface Passivation Over
Active Element of Fuse. Fuse is Blown

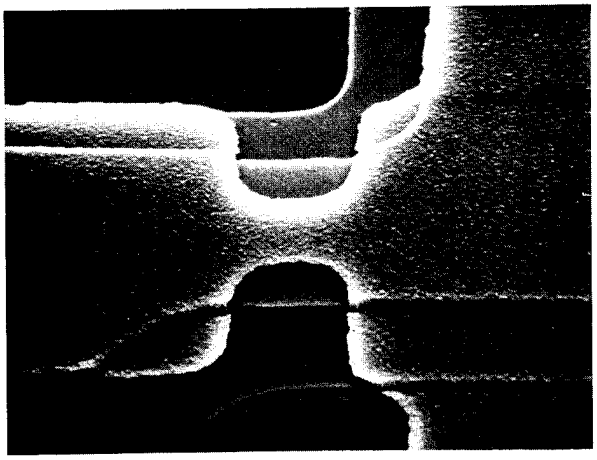


Figure 3
Polysilicon Fuse Shape

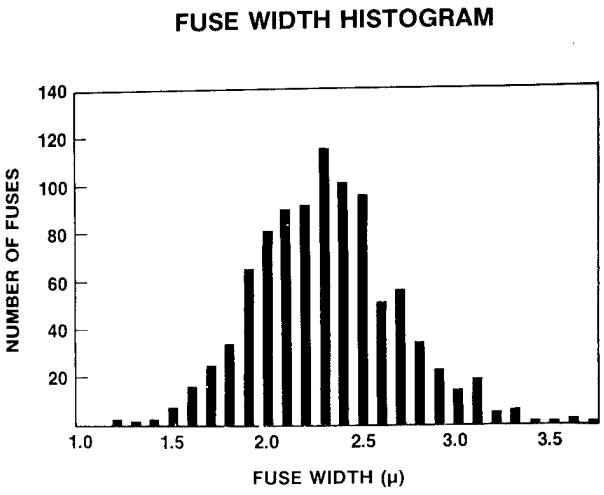


Figure 6
Fuse Width Histogram

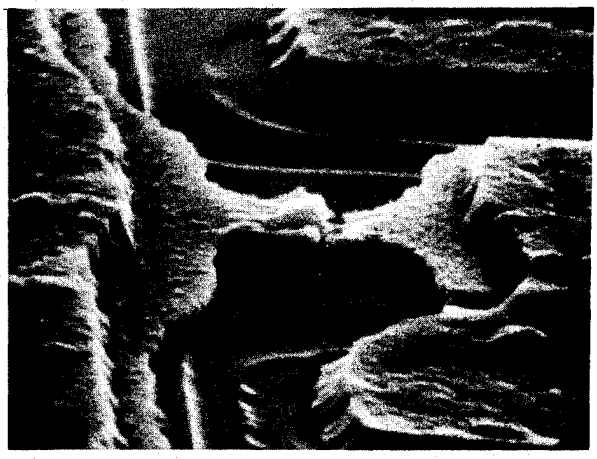


Figure 7
Side View of a Typical Blown Fuse

Acknowledgements

The authors would like to acknowledge helpful discussions with their many colleagues at Intel Corporation and also the invaluable experimental assistance provided by Nobuko Clark.

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FAMOS PROM RELIABILITY STUDIES

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ABSTRACT

Since the introduction of the FAMOS PROM structure and its implementation in a 2048 bit P-Channel MOS PROM, few device reliability data have been available. This paper presents data taken on both the P-Channel 2048 bit FAMOS PROM and the 8192 bit N-Channel FAMOS PROM.

The reliability studies undertaken fall into two categories, PROM retention tests and integrated circuit reliability tests. The combination of tests employed provide the basis for activation energy and failure rate calculations.

INTRODUCTION

The basic FAMOS PROM cell has been discussed in the literature[1] and is shown diagramatically in Figure 1. The memory cell is programmed by the transport of

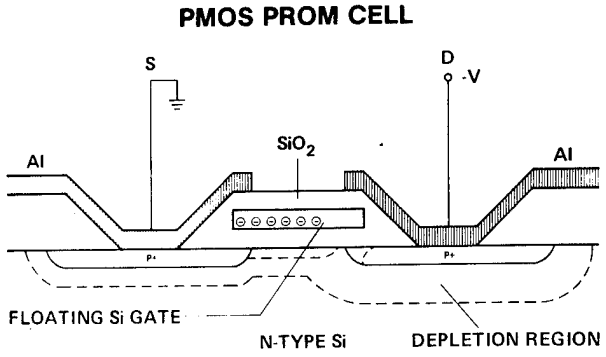

Figure 1

hot electrons from the vicinity of the drain junction to the floating gate. Once the electrons have been collected on the floating gate, the memory cell transistor assumes an "on" condition. The on or off (programmed or unprogrammed) condition can be detected through the use of a select transistor with row and column decode. This basic cell has been implemented in a 2048 bit PMOS PROM array, referred to as the 1702A.

A variation of the same basic FAMOS cell uses a two layer polysilicon process where the first layer forms the floating gate, and the second layer forms the select gate. Again cell operation depends on the transport of electrons to the floating gate where they are collected and used to offset the threshold voltage as measured with the top polysilicon gate. This basic single transistor memory cell has been implemented in a 8192 bit N-Channel FAMOS PROM referred to as the 2708. The basic memory cell is shown in Figure 2.

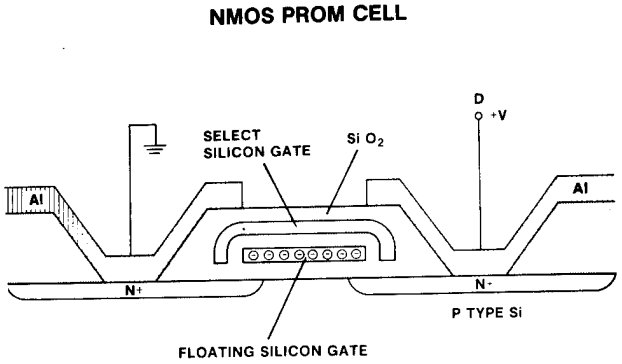

Figure 2

Both memory cells program the floating gate to a potential of about -12 Volts. At normal operating temperatures this programmed voltage remains indefinitely. The electrons are removed by illuminating the memory cell with ultraviolet light for five to ten minutes. The ultraviolet light produces a photocurrent from the floating gate back to the substrate thereby discharging the gate back to its original condition.

MEMORY CELL RETENTION

Cell charge loss characteristics were studied both on single FAMOS transistors on a test die and the PROM arrays previously described. The single transistor structure used is the N-Channel two layer polysilicon cell. By measuring the two terminal threshold voltage before and after programming, the offset voltage (V_{TP}-V_T) on the floating gate can be determined. Figure 3 shows the two terminal V_T bias configuration and the resulting IV characteristics. These parts were then baked at 200, 250 and 300°C to

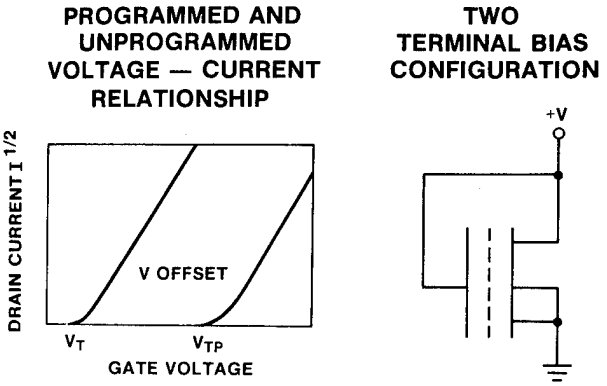

Figure 3

accelerate the charge loss. The degradation rate of programmed threshold voltage at the various temperatures is shown in Figure 4. Each data point represents the normalized average of ten individual transistor

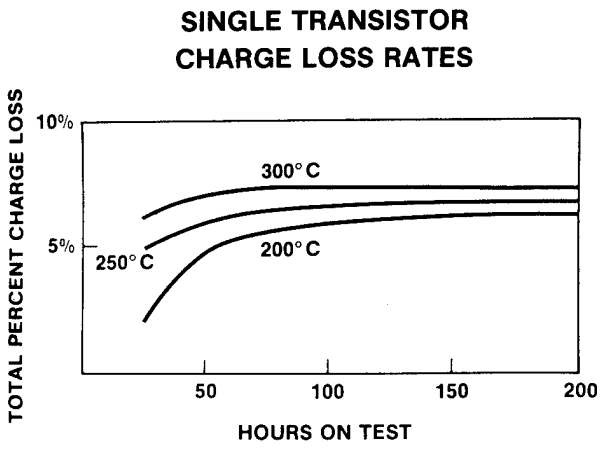

Figure 4

transistor readings. The degradation rates are plotted assuming an Arrhenius relationship, in Figure 5, yielding an activation energy of 0.8 eV

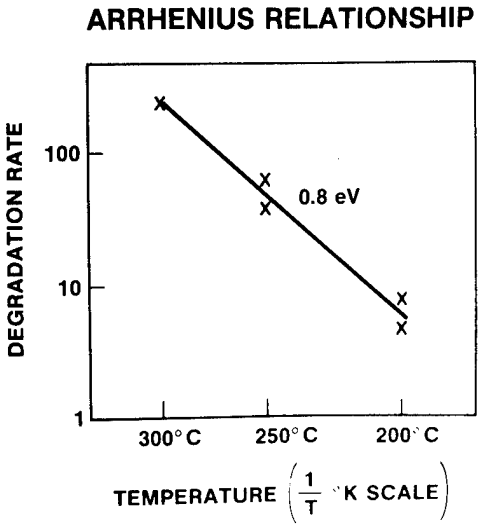

Figure 5

Cell retention in both the 2048 bit PMOS and the 8192 bit NMOS arrays were evaluated using high temperature bakes. A bit pattern was selected that programmed about 90% of the PROM cells but contained some unprogrammed bits in each row and column so a complete functional test could be performed. These parts were then baked at high temepratures and the cumulative percent failures plotted with time. Figure 6 shows the 250°C retention characteristics of the PROM and NMOS PROM arrays. Using the 0.8 eV activation energy derived from single transistor measurements, the time to 50% failure at 70°C is estimated at over 300 years.

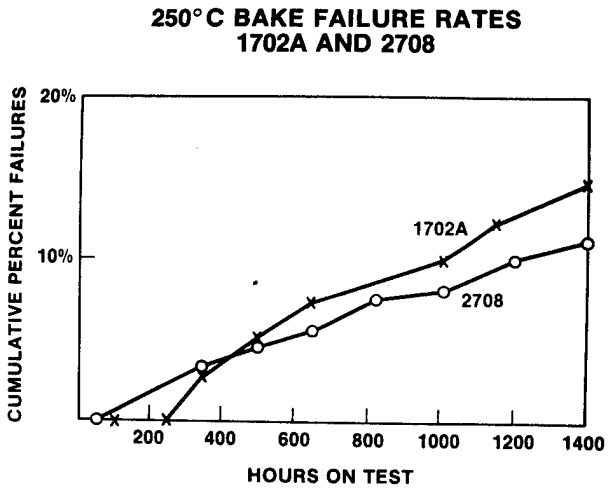

Figure 6

The useful life of most semiconductor products is between 10 and 20 years, and as a result the portions of Figure 6 past 100 hours at 250°C become unimportant to any real application of FAMOS technologies

LIFE TESTS

The electrical reliability of MOS LSI circuits is most realistically evaluated using MIL STD 883 condition D dynamic burn-in and life test. This was accomplished with the use of binary counters to genrate sequential address inputs. The address inputs of the individual devices were parallel wired on a printed circuit board with output load resistors at each device test socket. The chip select inputs were biased to enable the outputs. The printed circuits boards were then placed in an oven stabilized at an elevated temperature for the appropriate stress period. At each read point the entire oven is cooled down with all electrical signals still applied to maintain worse case stress conditions. The devices were then tested for complete functionality on a commercially available automatic tester. Samples of 1702A, 2048 bit PROMS, and 2708, 8192 bit PROMS were taken at various times throughout 1975 and placed on 125°C and 160°C operating life tests. These samples

1702 SINGLE BIT FAILURE

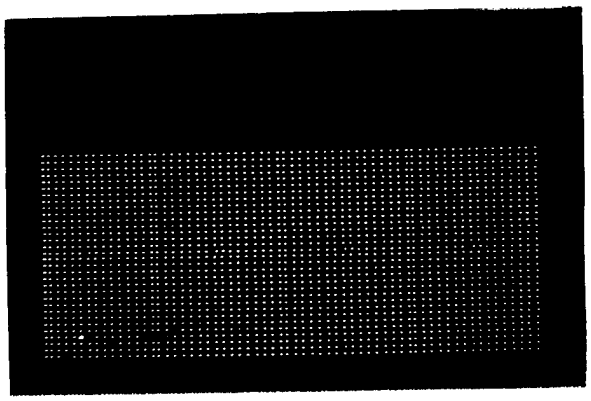

Figure 7A

2708 SINGLE BIT FAILURE

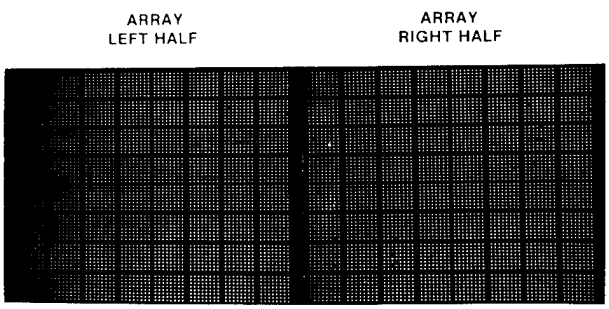

Figure 7B

received no special screening or preconditioning prior to the start of life tests. The units were programmed approximately 95% with the same data pattern as that used for retention bakes. The life test results are shown tabulated in Table A.

There were four functional failures in the 1702A test group at 125°C and two functional failures in the 2708 test group at 160°C. Each of these failures was caused by charge loss in a storage cell that resulted in a data pattern error. The errors observed were generally single bit errors although two and three bit errors have also been observed. Figures 7A and 7B show typical dot pattern displays of bits that failed on 1702A's and 2708's. The failed bit locations appear to be completely random. Close optical examination of the failed bit location confirmed there were no physical defects present that might have influenced the charge loss rate. In all cases the failed bit locations were reprogrammable indicating the failure mechanism was pure charge loss.

MOS PROMS require programming voltages well in excess of normal operating voltages and these high voltages are carried through each row and column during the programming operation. Each PROM goes through the programming operation twice, once during wafer test and once before final electrical test. The two programming steps use complimentary data patterns so each cell receives one program and erase cycle and each row and column receives two high voltage stress cycles. One would expect the programming operation to be a good screen for weak gate dilectrics because of the high voltage applied. The data in Table A strongly suggest this in indeed the case in as no failures due to shorted dilectrics were found.

Failure rate predictions were made by assuming the total device failure rate is equal to the sum of the failure rate contributions due to each failure mode.

Each failure mode was assumed to have temperature dependence. The life test data set for 1702A's and 2708's contain a number of failures due to charge loss but no failures due to all other MOS failure modes known to exist but not observed. The charge loss activation energy was determined to be 0.8 eV and the activation energy used for all other MOS failure modes not observed is 0.4 eV. Using the above relationship, the failure rates as a function of temperature were calculated. 60% and 95% confidence limits were used. Figures 8A and 8B show the predicted failure rates for the 1702A and 2708 respectively.

CONCLUSION

The FAMOS memory cell in application introduces a new failure mechanism, memory cell charge loss. The reliability studies reported in this paper were designed to evaluate the magnitude of risk associated with the floating gate PROM structures when these structures are implemented in the form of viable memory element.

OPERATING LIFE TEST RESULTS

DEVICE TYPE	TEMP.	SAMPLE SIZE	HOURS	FAILURES	FAILURE MODE
1702A	125°C	80	1000	0	
1702A	125°C	80	1000	1	Charge Loss
1702A	125°C	80	1000	1	Charge Loss
1702A	125°C	80	1000	1	Charge Loss
1702A	125°C	100	1000	1	Charge Loss
1702A	125°C	100	1000	0	
1702A	125°C	100	1000	0	
2708	160°C	64	2243	1	Charge Loss
2708	160°C	49	2028	0	
2708	160°C	51	2028	1	Charge Loss
2708	160°C	40	2830	2	Charge Loss
2708	160°C	80	1176	1	Charge Loss
2708	160°C	77	1176	4	Charge Loss
2708	160°C	79	984	1	Charge Loss

Table A

2708 FAILURE RATE PREDICTION

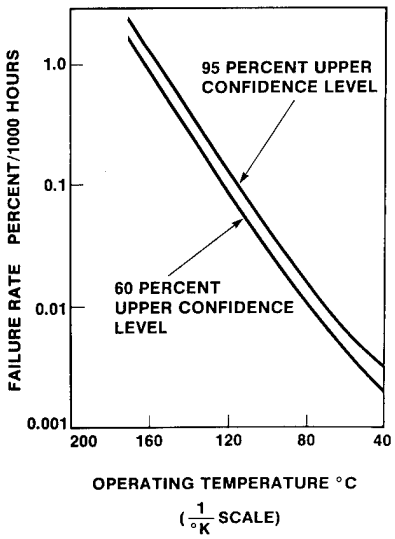

Figure 8A

1702A FAILURE RATE PREDICTION

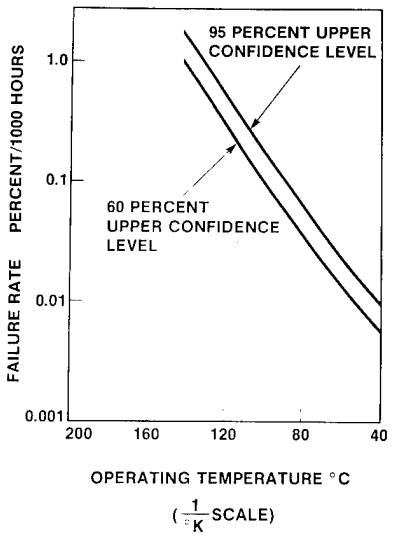

Figure 8B

LIFE TEST BIAS CONFIGURATION

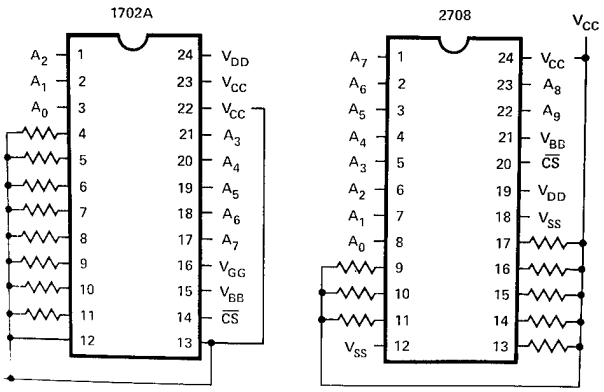

Figure 9

REFERENCE

1. "A Fully Decoded 2048 Bit Electrically Programmable MOS Read Only Memory", 1971 ISSCC, Philadelphia, February 17-19, 1971.

ELECTRICALLY SHORTED SEMICONDUCTOR JUNCTIONS UTILIZED AS PROGRAMMABLE READ ONLY MEMORY ELEMENTS

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Abstract

Occasionally a problem becomes a solution. In search of a reliable element to use as the electrically alterable storage element in a programmable read only memory (PROM), the well-known failure mode of the shorted semiconductor junction was studied. Since a shorted junction is easily produced and remains shorted indefinitely, it can be applied as a reliable PROM storage element.

This paper describes the programming technique and summarizes over four years of reliability characterizations performed on actual PROM devices produced using this technique.

Introduction

Since the development of the solid state semiconductor junction and subsequently, the bipolar transistor and integrated circuit, the phenomenon of avalanche breakdown has been extensively studied and documented. Indeed several practical applications have appeared using non-catastrophic avalanche breakdown such as avalanche diodes for voltage regulation and more recently microwave avalanching diodes used as microwave sources.[1]

Avalanche breakdown is not destructive to the junction as long as the avalanche current and the power dissipation are correctly limited to prevent thermal runaway. If the avalanche current is allowed to increase to a level where an excess of charge carriers is produced due to I^2R heating in the junction, secondary breakdown occurs generating additional excess charge carriers. If this process is allowed to continue, thermal runaway occurs and the temperature rapidly increases to the point where the materials comprising the junction no longer remain in the solid state. The junction is physically destroyed and becomes a resistive short circuit.[2-3]

This paper describes an application employing diodes which have been purposely shorted by secondary breakdown and thermal runaway. The paper also summarizes results of extensive reliability characterizations performed on actual devices designed and manufactured using this technique.

An Application for Shorted Junctions

It is intuitively obvious that a semiconductor junction once shorted by secondary breakdown and thermal runaway can never change back into a junction without expending a great deal of effort. Thus, the shorted junction would seem to be an ideal memory element for use in a field programmable read only memory device (PROM).

In early 1971 a PROM device was designed and fabricated using standard bipolar TTL memory technology with no extra processing operations. This device consists of an array of open-base NPN transistors of minimal area and the necessary addressing and interface circuitry.[4] The actual construction of a "bit" element is shown in Figure 1. A contact is made to the emitter and the collector is common to the collectors of the other "bit" elements. No connection is made to the base. Since 1971, 256, 1024, 2048 and 4096 bit PROMs, and a programmable logic array (FPLA) have been successfully designed and manufactured.

A portion of the diode matrix as manufactured (before any diode is programmed) is shown in Figure 2. After programming, the desired memory locations appear as single forward biased based-collector diodes. The base-emitter junctions have been electrically altered to form resistive shorts. The matrix after programming is shown in Figure 3. The shorted emitter-base diodes represent logic (1) and the open-base transistors are logic (0).

Programming

During the programming operation a high reverse current (avalanche) of 200 mA is forced into the desired emitter-base junction in short (7.5 μs) pulses. The 200 mA current is sufficiently large to initiate secondary breakdown and the pulse-width is long enough to allow the junction temperature to increase beyond the temperature where physical alteration of the junction occurs.

Actual programming employs a "pulse-sense-pulse" technique whereby the "resistance" of the junction is sensed at the end of each programming pulse and additional pulses are applied until the proper resistance is achieved. In this manner, very uniform programmed diodes are produced. Figure 4 shows a typical programming pulse sequence.

Physics of Programming

It was theorized that during programming, the base-emitter junction reaches a temperature sufficient to induce the migration of aluminum from the contact area to the junction causing a resistive short.[5] The wealth of literature available on the shorted-junction phenomenon [6-10] indicates shorting is caused by thermal charge multiplication and thermal runaway. As the avalanche current increases beyond the point where secondary breakdown is initiated, the current constricts into a narrow filament which forms a microscopic hot spot in the junction area. The current filament forms most easily in a location of electric field concentration. In the case of the emitter-base diode with an aluminum contact, the electric field is concentrated near the edges of the contact due to the presence of aluminum alloy locations.[11] As the programming pulse increases to 200 mA, thermal breakdown of the junction occurs. Aluminum from the contact area mixes with the silicon in the emitter contact and migrates to the junction; the voltage drops suddenly indicating the presence of a low resistance short. The process is thus, self-regulating because the power dissipation in the junction area also drops.

In order to properly characterize the programming technique, evaluation was undertaken to investigate

the actual physics of the shorting phenomenon.

Note that programmed diodes are not discernable from unprogrammed in surface views in either light or electron microscopy. This is consistent with theory since the shorting should be occurring beneath the surface of the silicon under the aluminum emitter contact. Figures 5 and 6 show surface views of the array using light and SEM microscopy. Sample devices were programmed and microsectioned in an effort to locate and analyze the material in the shorted region of the junction.

Samples of the 1024-bit PROM were microsectioned at an angle of 2° relative to the surface. Microsectioning at a shallow angle allows the subsurface filament of aluminum to be visible. Photomicrographs of programmed and unprogrammed diodes were made, Figures 7 and 8.

In all programmed diodes a white appearing material is visible extending from the emitter contact into the junction area. The material is visibly characteristic of the "white spear" effect extensively documented in the reference literature. In order to substantiate that aluminum has migrated to the junction, a sample which was sectioned was submitted to *x-ray dispersive analysis*. Results indicate that aluminum is indeed present (Figure 9). Since the x-ray microprobe technique is not particularly quantitative, the actual amount of aluminum present was not determined. However, the phase diagram for aluminum-silicon (Figure 10) indicates aluminum and 14% silicon form an eutectic at 555°C.[12] It is reasonable to assume that this temperature is reached in the current filament which forms during the programming operation. For comparison, an example of the white spear effect in a small geometry lateral transistor is shown in Figure 11.

For further verification that aluminum has migrated to the junction area, a sample was chemically etched with a common aluminum etchant (dil. HCL) which does not attack silicon. The white spear material was etched away leaving a crater in the junction area. A SEM photomicrograph was taken showing the cratering phenomenon (Figure 12). Normal aluminum "alloy pits" are also visible in this photo. Unprogrammed diodes are shown for comparison in Figure 13. No cratering is visible except for normal aluminum alloy pits.

Thus, the original hypothesis is correct. The current filament is localized at an alloy location below the emitter contact area and as the temperature increases during programming, aluminum mixes with the silicon and migrates to the junction causing a resistive short.

Reliability Characterizations, 1971-1976

Since the first devices were designed and manufactured, extensive reliability evaluations have been performed including:

1. Step-Stress Life $T_A = 125°C$
2. Freeze Life $T_A = -20°C$
3. Operating Life $T_A = 125°C$

Also, reliability data from the field is constantly recorded and reviewed.

Step-Stress Life Test

Since device programming occurs when a high current is forced into desired bit locations, it was felt that perhaps unwanted bits could be programmed during system operation due to inadvertent "glitches" in the system. A step-stress test was performed to determine if unwanted bits could program and what voltage level is necessary for unwanted programming. A sample of 26 units were programmed with 50% of the bit locations programmed. The devices were subjected to operating life test at $T_A = 125°C$. The supply voltage was started at a nominal +5 volts and subsequently increased 0.5 volts after each 168 hours on test. The devices were removed at each 168-hour time point and completely tested for compliance to specification. No failures occurred until a voltage of 9.5 volts at 1500 hours was reached. Significant failures occurred at 10.5 volts and 1840 hours total. Routine failure analysis was performed to determine if any unprogrammed bits became programmed. On all failures which occurred during the step-stress life test, one or more internal bond wires were blown open. The bond wires were subsequently replaced and the units were then retested. All units then functioned normally. No unwanted bits were programmed. Results of the step-stress life test are tabulated in Figure 14.

Freeze Life Test

A test has been adopted in the industry to subject devices to potentially damaging moisture effects. Any water present inside the hermetic package may condense on the chip surface at low temperatures and cause chemical activation of certain metallic constituents and subsequent corrosion and altering of the storage elements. The test is performed by cycling the ambient temperature between -20°C and +25°C while switching the applied voltage on and off.[13]

It was felt that the freeze life test was not pertinent to the avalanche induced migration programming technique since shorted junctions are not susceptible to corrosion. However, the test was performed in order to have documented data available to insure compliance with the industry standard. 26 units were programmed 50% and subjected to the freeze life test. No failures occurred after 1,000 hours.

Routine Life Test Evaluation

Since 1971 samples have been routinely procured from shippable product and subjected to life test, both static and dynamic at $T_A = 125°C$ and nominal supply voltage. Samples include a 256, 1024, 2048 bit PROM, and a programmable logic array (FPLA). To date 2912 devices have been life tested a minimum of 1,000 hours with several samples exceeding the 10,000 hour time point. The average sample size is 129 units. The total cumulative device hours equal 10.44×10^6. The life test summary is shown in Figure 15. All devices subjected to life test were programmed to a standard truth table (approximately 50% bits programmed). Routine failure analysis was performed on every reject which occurred during these evaluations. The occasional failure was typical of those normally found with any standard bipolar TTL memory device. However, there has been no occasion of a programmed bit which reverted to unprogrammed. In fact, there has never been a bit-related failure in a total of 6.47×10^9 bit-hours of life testing.

Field Data

Field data is the ultimate indicator of device reliability. Feedback from customers in the field indicate there has never been a bit-related failure out of billions of programmable bits shipped since 1971.

Summary

The shorting junction phenomenon, which has plagued the semiconductor industry since its birth, has been successfully applied to a memory application where a simple and reliable technique was needed. Programmable read only memory devices were designed and manufactured using standard bipolar TTL technology. The memory element consists of an open base transistor, whose emitter-base junction is electrically altered to form a resistive short due to secondary breakdown and thermal runaway. Extensive physical evaluation has shown that shorting occurs due to aluminum migrating to the junction in a small, high temperature current filament, which follows the path of highest field strength. The reliability related points are:

1. The shorted junction is inherently hermetic as it lies beneath the glassivation, aluminum, and N+ diffusion.

2. Current is forced through the element before and after programming to assure that the element has been properly programmed.

3. Each bit is operated at a current which is 1/400 of the programming current.

4. No special material depositions or controlled etches are required in manufacturing.

Finally, results of extensive reliability evaluations and field data further confirm the theoretical hypothesis that a programmed bit is irreversible.

Once again, simplicity in design, application, and manufacture has yielded a reliable extension of semiconductor technology.[14]

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[1]S. K. Roy, B. Som, and B. B. Pal, "Dependence of the Read Diode Characteristics on the Current Multiplication Factor in the Avalanche Zone," *Proc. IEEE,* July, 1975.

[2]Kiyoshi Demizu and Yoshimichi Yamamoto, "Second Breakdown of IC Structured Power Transistors," *IEEE Trans. Elect. Dev.*, June, 1975.

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[9]Henry Domingues, "Transient Temperature Rise in Silicon Semiconductor Devices," *IEEE Transactions on Electron Devices,* January, 1975, pp 20-22.

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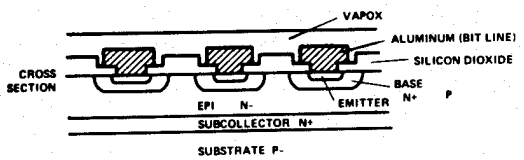
[13]Vincent C. Kapfer, John J. Bart, "Thin Film Nickel-Chromium Resistor Failures in Integrated Circuits," *10th Annual Proc. Reliability Physics,* 1972, pp 176.

[14]J. Rizzi, L. Fagan, "Electrically Alterable Integrated Circuit Read Only Memory Unit and Process of Manufacture," *U.S. Patent No. 3,742,592,* July 3, 1973.



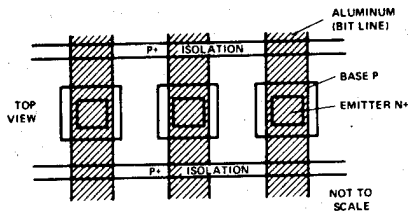


Figure 1

Bit Element Construction

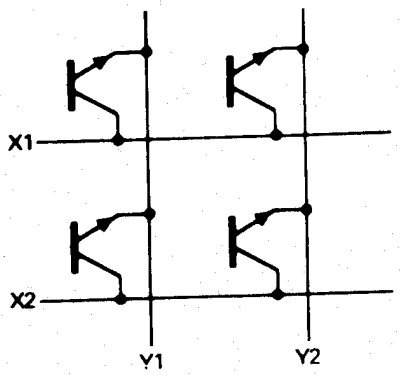


Figure 2

Unprogrammed Array

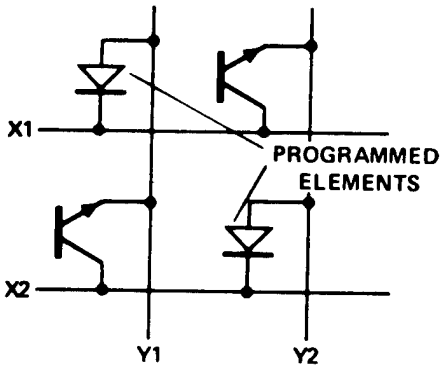


Figure 3

Array After Programming

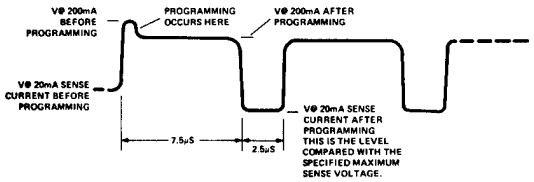


Figure 4

Programming Pulse Sequence

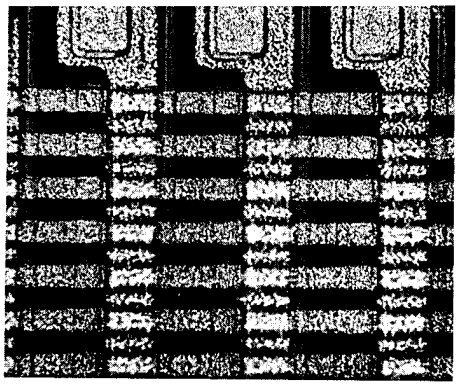


Figure 5

Surface view of array, light microscopy.
Every other bit is programmed.

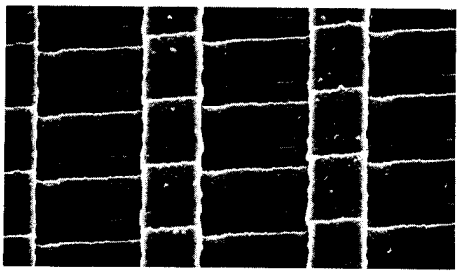


Figure 6

Surface view of array, SEM. Every other
bit is programmed.

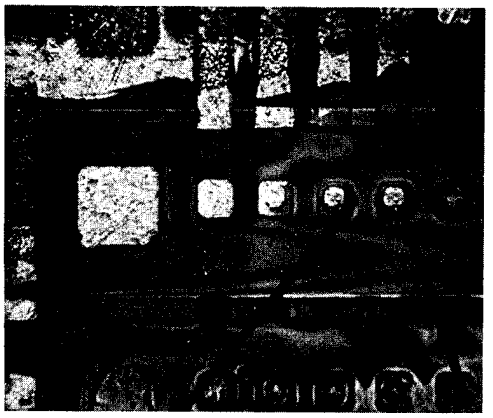


Figure 7

Photomicrograph showing microsection at 2°.
Bit elements are visible.

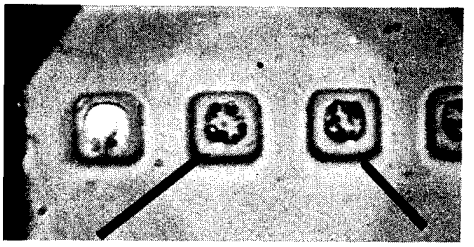


Figure 8

Higher magnification showing "white spear"
effect in programmed diodes.

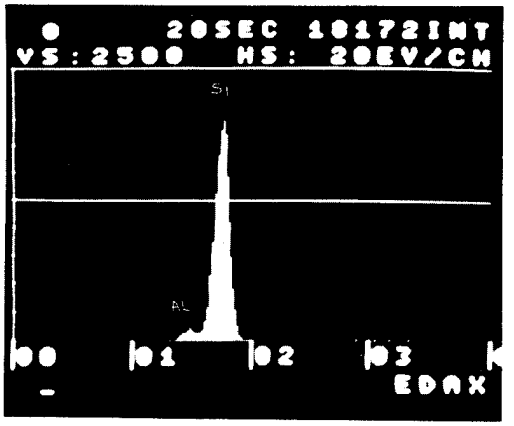


Figure 9

X-ray microprobe results showing aluminum
present in white spear.

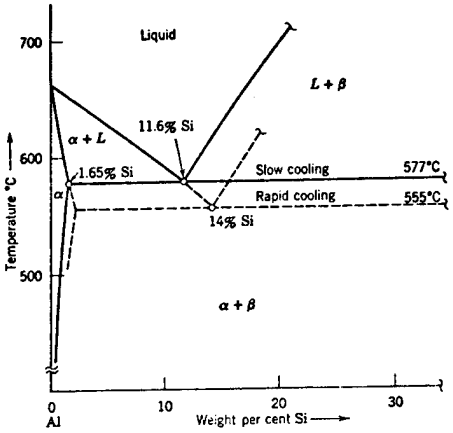


Figure 10

Phase diagram of Al-Si mixture.

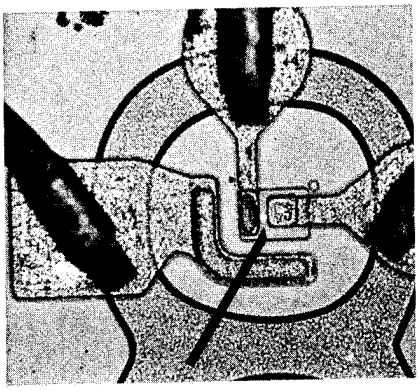


Figure 11

Lateral transistor which was shorted to demonstrate white spear effect.

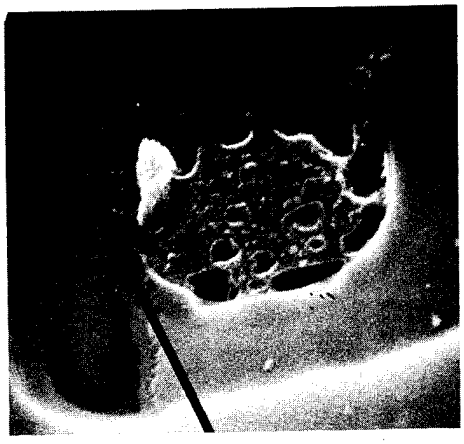


Figure 12

SEM photo showing cratering in junction area on programmed diode. Al was removed by chemical etching.

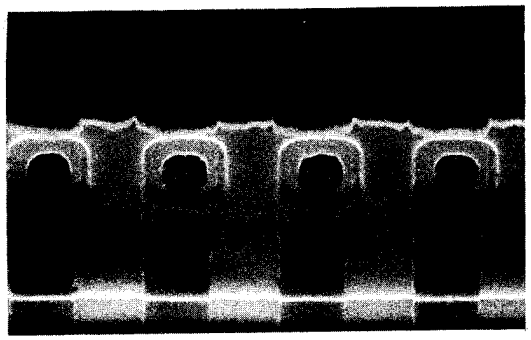


Figure 13

SEM photo of unprogrammed diodes showing normal Al alloy pits. Al was removed by etching.

Test Point	Test Time, Hours	Supply Voltage	Quantity	Failures
0	0	5.0	26	0
1	168	5.5	26	0
2	340	6.0	26	0
3	500	6.5	26	0
4	668	7.0	26	0
5	840	7.5	26	0
6	1,000	8.0	26	0
7	1,168	8.5	26	0
8	1,340	9.0	26	0
9	1,500	9.5	26	1
10	1,668	10.0	25	5
11	1,840	10.5	20	16

NOTE: Rejects were rebonded and subsequently passed all electrical tests.

Figure 14

Step Stress Life Summary
$T_A = 125^oC$

DEVICE TYPE	QUANTITY TESTED	CUMULATIVE DEVICE HOURS x 10^6	CUMULATIVE BIT HOURS x 10^9
256-Bit PROM	1,354	6.19	1.58
1024-Bit PROM	1,147	3.67	3.76
2048-Bit PROM	385	0.50	1.02
FPLA	26	0.08	0.11
Totals	2,912	10.44	6.47

NOTE: Not a single bit related failure has ever occurred during life testing.

Figure 15

Operating Life Test Summary
$T_A = 125^oC$

A RELIABILITY ASSESSMENT OF BIPOLAR PROMS

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Summary

Design factors affecting the reliability of Schottky T^2L PROMs are discussed with special attention to the high voltage programming circuitry and fuse design. Key process controls during nichrome deposition, fuse delineation (masking) and subsequent processing environments have been developed as a result of device failure analysis. Approaches to functional and AC testing before actual programming are detailed with respect to the use of additional test "bit" and "word" lines and device design layout. One pulse programming of extra test fuses in each device is used as a special manufacturing screen to remove would be failures. "User" liabilities involved in programming, testing and Hi-Rel processing are explored with emphasis on long term reliability.

Introduction

Any total assessment of integrated circuit reliability starts with device design and its compatibility with established wafer fabrication processes. Design and wafer processing factors must be constantly referred to in the continuing reliability study further on in the manufacturing cycle, i.e., assembly, testing, and screening. This comprehensive approach is even more important when investigating the reliability of Programmable Read Only Memories (PROM).

As well as being large scale integrated circuits, (LSI) PROM's were the first IC devices to be shipped to the user incompletely manufactured and incapable of having been 100% tested since field programmability actually defines the functionality of the device. In the unprogrammed state the output level of the PROM, depending on design, is initially either all highs or lows for every addressable location. Programming subsequently changes some of these locations to hold the opposite of the original logic level. Thus programming becomes the final manufacturing step, and therefore the final testing of the device must be performed after field programming by the user. In practice this is most often accomplished in the same equipment used to program the device. These factors, of course, raise additional reliability questions. A total assessment of PROM reliability should therefore take into account:

1) Circuit design
2) Wafer processing
3) Packaging and assembly
4) Pre-programming tests and screens
5) Programming
6) Post-programming tests and screens

Circuit Design

Programming of all PROM's manufactured today depend on a method of selecting a programmable element and changing it through the use of a high voltage pulse. Although this paper deals with nichrome fusible link bipolar PROM's, much of what is discussed can be extrapolated to other technologies since high voltage programming is common to all.

The key point to remember in PROM design is that the device must not only work at the normal voltage supply levels, 4.5 - 5.5 volts for TTL, but also function at the higher programming voltage levels, typically 20-30 volts. Only the programming path need be tolerant of high voltages and currents. However, since most design approaches involve a fully decoded memory array matrix, figure #1, to minimize external pins to the outside world, one finds that much of the circuitry must consider the potential reverse bias leakages and breakdowns at the higher voltages experienced during programming. The first available PROM was a 256 bit device organized 32 words by 8 bits (output), figure #2. Note that there is no decoding of the array matrix in the output direction. The programming pulse does not have to be multiplexed through additional decoding circuitry. It is this factor that simplified the design of the device and the subsequent 64x8 (512 bit) device. It should be mentioned that most of the significant voltage drops during programming have occurred once the word decode circuitry is reached through the memory array matrix. When larger circuits were designed, such as the 512x4 (2048 bit) device, figure #3, additional output decoding circuitry tolerant of programming voltages became necessary for chip layout and geometry reasons.

Current trends in TTL LSI circuitry are moving towards the Schottky process instead of the gold diffused process. This approach uses the Schottky barrier diode as a clamp across the base-collector region to avoid saturation and minority carrier storage in the transistor, as well as the attendant recovery delay, see figure #4. One of the drawbacks with the Schottky diode clamp is that edge effects around the metal-semiconductor periphery cause higher field strengths which cause soft reverse breakdowns of the Schottky barrier diodes. Extension of aluminum over the thermal oxide around the contact cut provides field plate protection which tends to minimize the field effects from the edge of the metal-semiconductor junction. When designing PROM's, however, much higher reverse biases are experienced in the course of high voltage programming. Field plate geometries are not

sufficient to protect against losing valuable programming current through soft, leaky Schottky reverse bias junctions. A P-type guard ring around the edge of the metal-semiconductor junction is used so that the reverse breakdown now takes on the characteristic of the higher base-collector junction, BV_{cbo}. This guarded Schottky clamped transistor structure, reflected in figure #5, provides an adequate solution to any soft breakdowns encountered during high voltage PROM programming.

Numerous design factors effect parasitics and in PROM's they may significantly limit programming current. "Epi"-resistors are frequently employed in the design of devices using a thin epitaxial Schottky bipolar process. They provide a convenient source of small geometry, high value resistors taking advantage of the higher sheet resistivity of the lightly doped epitaxial layer and the lack of isolation requirements. Minimum geometry epi-resistors are narrow and normally used at TTL biases. However, they may tend to pinch off to an extremely high resistance at the high voltages used during programming causing the original circuit design to become non-functional. This is due to the width of the charge depletion region increasing with higher reverse biases across the isolation-epi PN junction. PROM design must consider this pinch off effect specifically throughout the programming path. Isolation diffusions are a source of parasitics. The diffusion widths must be large enough to prevent parasitic NPN action where large programming currents result in large substrate currents.

Actual component, transistor, diode, etc., geometry is also important in that it must be compatible with the large currents and voltages encountered during programming. For example the multiplex transistors in the output decode at the head of each bit line, figure #1, funnel all the programming current to the fuse. The base drive for this device comes from another overlapping high voltage pulse on the program pin, figure #6. This leads to an overall design requirement, that voltage drops in the circuitry to the nichrome fuse, be conserved to provide, as much as possible, adequate programming current margins.[1] One of the chief areas of concern with PROM's is assuring sufficient current to open fuses reliably.[2] For this reason, voltage drops, due to word line resistance are important. Note that in figure #7, the high resistivity of the common collector epi tub which serves as the word line in the array matrix is circumvented by using, in parallel, a lower sheet resistivity N+ diffusion and a metal shorting bar between two back-to-back memory cells. Even using these techniques the word line length may become too long, especially in the larger memories such as the 4096 bit PROM, figure #8. Here the array matrix has been split to reduce word line resistance. This technique, however, increases chip area but avoids the other alternative of going to a multilevel metalization system. Although the latter approach improves the ease of controlling voltage drops within the circuit, one pays the penalty in the more complex processing required, the associated yield effects, higher costs and the additional failure modes and reliability problems which are well documented with multi-level metalization.[3] As an example, figures #9 and #10 contrast two 1024 PROM designs. In the first a single array is used with single level metalization resulting in a chip size of 7035 mil^2. The split array, still using single level metalization, requires a chip size of 8288 mil^2, an 18% increase over the single array.

Nichrome fuse resistance plays a significant role in determining what programming current is required to open the fusible link. The lower resistance value fuse makes designing the circuit over wider threshold margins easier but a penalty is paid in the increased programming current requirements. Higher programming currents typically mean double layer interconnect systems, i.e., dual-level metal. The effect of nichrome fuse geometry on PROM reliability and on the fuse programming mechanism has been reviewed in some detail using new analytical techniques in conjunction with Scanning Transmission Electron Microscopy, STEM.[4-7]

The PROM's referenced all use a collector-base, CB, diode cell in series with the nichrome fuse, figure #1 and #7. There are other design approaches using transistors, i.e., the emitter-follower cell. The major advantage of the CB diode design is the absence of active emitter area. It is well known that emitter-base junction leakage and breakdowns (shorts) are a major failure mechanism in bipolar IC's. Pinholes and other oxide defects in the more susceptible, thinner thermal oxide grown over N+, emitter diffusion areas as well as bulk defects such as "pipes" also contribute to wafer process yield losses. Thus the use of the CB diode cell, with its characteristically high reverse breakdown voltage not only improves the design reliability picture but also proves to be more produceable. The impact of this cell design is realized when one looks at a large PROM such as the 4096 device in figure #8. Not only is the array matrix composed of collector-base diodes but so is most of the word decode and output decode circuitry. In contrast this device, an 18,600 mil^2 chip, has less active emitter area than a 54S181 TTL MSI device (4-bit ALU), a chip less than 40% the size of the LSI PROM.

It is significant that most of these design considerations, i.e., metalization techniques, active emitter area, etc., are not taken into account in the MIL-HDBK-217B[8] reliability prediction models. Therefore caution should be used when trying to extrapolate such failure rate calculations from one design to another.

As a PROM is shipped unprogrammed and additional testing is required after programming, it is important that the design incorporate measures to correlate with and assure field programmability and the functioning of the programmed device over the whole operating spectrum of specified temperatures and power supply tolerances, i.e., V_{CC}. To do this an extra test word line and a test

bit line are introduced at the respective ends of the array, figure #1 and #8. This extra circuitry allows the unprogrammed device to be tested functionally, checking internal thresholds and the decoding circuits. In earlier designs this circuitry was only available through additional bonding pads at the wafer probe testing level. The assembled package with its restriction on the number of external pins to the outside world did not permit access to this extra circuitry. This was overcome in later designs by multiplexing the extra test bit and word lines to existing normal address pins through the use of Zener diodes within the input circuitry. Since high voltages are used to enable this extra circuitry (via Zener breakdown), the test word and bit lines become invisible at TTL input voltage levels and therefore do not interfere with normal device operation. The absense of nichrome fuses in some locations along the test word and bit lines simulate blown fuses and provide a standard functional program easily interrogated during factory testing. Later on,the remaining test fuses may be programmed at the package level to assure field programmability prior to shipment.

During the design phase it is important to remember that device operation and programmability must be assured over the entire distribution of wafer processing variables, i.e., diffusion sheet resistivities, beta, fuse resistance, reverse biased junction characteristics, etc. In earlier designs marginal circuit performance, specifically programmability, figure #11, was traced to the fact that a process distribution variable, the fusing current, partially overlapped the current capable of being supplied by the circuit design. The result was that some percentage of the units would fail to program or program slowly requiring wide pulses. This was rectified by establishing a minimum design margin current criterium. During the initial production stages, and periodically thereafter, one must characterize the design-process compatibility by careful sample selection of lots reflecting process variable extremes.

Wafer Processing

High voltage programming requirements figured heavily in the design phase of PROM's and it is only natural that they play an important part in the actual wafer processing. Obviously the reverse bias leakages and breakdowns of the various PN junctions are key process control points. In reality these measurements are used at wafer inspection gates to screen out marginal wafers as well as for process control monitoring. Additional tests for beta and other discrete device characteristics are performed on a special test chip made out of the normal device by using mask options.

The major difference in PROM processing is the nichrome metal deposition and the subsequent masking step. Otherwise the wafers undergo the same processing as other non-nichrome LSI products such as ROM's, RAM's, and Computer Logic Chips.

Nichrome is deposited in a thin film, $\sim$175Å, by conventional vacuum deposition equipment. Controls for such deposition processes and the following masking steps are well documented.[9] During nichrome deposition from an evaporative source, care must be exercised to control the temperature since vapor pressures of the nickel and chromium components vary widely with changes in the temperature. Thus, even though initial source composition is controlled, one may end up with a variety of thin film compositions without the proper temperature control. The fine structure of the fuse is determined by many deposition variables, specifically rate of deposition, substrate temperature, residual oxygen, vacuum pressure, etc. Test specimens placed along side actual wafers during each deposition are used to automatically control deposition time by directly measuring the sheet resistivity since it is a more sensitive parameter and measures film thickness indirectly.

The small geometry nichrome fuse is more reproduceably defined through a reverse lifting process rather than the conventional etching technique, figure #12. Using the lift technique, photo resist is applied to the wafer prior to the nichrome deposition; the pattern is exposed after alignment with the applicable mask; the develop cycle removes the resist where the fuse is to be placed, and then the nichrome is deposited. After deposition, ultrasonic action in a suitable photoresist stripping reagent, e.g., J-100, dissolves the remaining photoresist under the unwanted nichrome, lifting it away. The nichrome deposit is left on the SiO_2 substrate due to its excellent adherence to the thermal oxide. Separation of the film is usually at the point indicated in figure #12. However, if the process is not adequately controlled it could separate above this point leaving a flap of nichrome sticking up some 7000Å above the surface. A SEM photo, figure #13, shows such a nichrome flap. Subsequent aluminum deposition may form a void or tunnel around the fuse periphery where the flap shadows the metal deposition. This void will enlargen during the etching of the metal interconnect pattern as in figure #14. Control of this critical "lifting" process is easily monitored using the SEM. An acceptable fuse before and after metal deposition is shown in figures #15 and #16.

Since nichrome is a thin film, surface effects play a large part in defining the fuse structure. Reactions that are not important, or that do not occur in bulk nichrome, become significant in the thin film structure due to the higher free energy associated with surface chemical and physical phenomena. Both ESCA, Electron Spectroscopy for Chemical Analysis,using X-Ray photoelectrons[10], and Auger Electron[11] spectroscopy have shown that subsequent process steps play a significant role in determining nichrome structure and its contact to the aluminum interconnect metalization. Other studies have shown that moisture levels in the lifting reagent can attack thin nichrome films.[12] The metal etch used in removing unwanted aluminum metalization over the fuse may also attack the nichrome. Usually an oxidizing agent, such as

nitric acid, is added to the metal etch reagent to passivate the nichrome against attack. However, the very process of passivation involves oxidation of the surface of the nichrome and, considering its thin nature, any shift in fuse characteristics as a result of the altered surface structure must be monitored.

Subsequent high temperature processing after nichrome deposition may also alter the fuse structure, e.g., alloying ohmic contacts, special stabilizing anneals, silox (glassivation) deposition.[12,13] All such effects must be monitored throughout the processing using the applicable fusing current vs. fuse resistance criteria established for the specified process-design. Reliable nichrome to aluminum contact may also be checked during these measurements by checking fuse resistance linearity at low voltage levels.

Assembly - Packaging Factors

As many PROM's are LSI circuits, special attention should be given to reliable and adequate chip attach techniques. When attaching a large chip, say >10,000 mil^2, to a metalized ceramic substrate, there is seldom enough gold to form an adequate volume of gold-silicon eutectic material to result in the desired void free chip attach. Therefore one must supply additional eutectic material in the form of a small gold-silicon preform. This will help in reaching the optimum thermal dissipation capability that a particular package and chip size allows. The θ_{JA} (Junction to ambient temperature coefficient) or θ_{JC} (Junction to case temperature coefficient) of the device is critical in reliability calculations determining the acceleration of failure rates due to the dependence on junction temperature.[8]

The reliability of thin nichrome films vs. dry hermetic packaging has received wide attention via the use of nichrome resistor structures, similar to fuses, in radiation hardened dielectrically isolated circuits.[12-15] Paulson[12] has reviewed the mechanism of moisture attack on nichrome. Hermetic packages, using devitrified (crystalized) high lead content glasses, were found to have residual moisture levels high enough to condense out at low temperatures inside the cavity forming a thin film over the chip. If the device was then biased (functioning) under this low temperature condition, electrolytic attack might occur; specifically anodic dissolution would take place when two areas on the circuit (bonding pad and a fuse in the case of a PROM) were connected by the water film and a potential difference of at least 2.5 volts existed. Although the SiO_2 glassivation was thought to prevent moisture from reaching the nichrome fuse which it covers, there is always the chance that a small invisible crack or pinhole may permit the condensed water vapor to contact the nichrome film below. Devitrified glasses, commonly used in sealing Cer-DIP packages, are particularly sensitive to this phenomena of high residual moisture content in the package cavity. The source of the moisture comes from water strongly bonded in the glass which was formed when an organic binder was burned off during the manufacture of the raw assembly piece parts. This binder is used to hold the glass particles together until subsequent firing in a furnace can fuse the glass together. Later during IC package sealing, this glass first melts to form a hermetic seal and then undergoes a phase transformation called devitrification where the glass assumes a more ordered crystalline structure. It is during this latter process that most of the latent moisture is evolved and trapped in the cavity.

One approach to avoid the residual moisture is to use a vitreous seal which does not crystallize after sealing and therefore does not precipitate out as large amount of moisture as in the devitrifying seals. These vitreous glasses are often sealed in air to prevent reduction of lead oxide to metallic lead and can therefore contain appreciable moisture if the air is not carefully dried.

Cerdip packages used for commercial temperature ranges, 0° - $70^{\circ}C$, are not affected by this phenomena since the moisture never condenses out in a biased mode especially considering that chip temperatures are some 20° - $30^{\circ}C$ in excess of the ambient temperature outside the device. Vitreous seals could be used on military temperature ranges if residual moisture levels could be proven low enough or as an alternate approach, the chip can be made moisture proof by using a redundant silicon oxide barrier to reduce the possibility of a glassivation flaw exposing a nichrome thin film. The "freeze-out" test specified in the MIL-M-38510/201 detail specification[16] on the 512 bit PROM, provides one method to determine whether or not residual moisture is attacking nichrome. The water drop test, in the same document, determines the integrity of the glassivation. It is important to note, however, that most single layer glassivation techniques using deposited SiO_2 are not much more than scratch protection barriers. Visual inspection for small glassivation flaws is virtually impossible; so a better solution for military temperature range PROM's is to avoid residual moisture in the first place. This is accomplished by using the well known gold-tin, 80:20, Au/Sn, solder seals. These are of proven reliability in side-brazed dual-in-line configuration as well as in the ceramic-filled glass flatpacks. The sealing environment can use very dry nitrogen or forming gas (N_2/H_2 mixtures) with furnace profiles that result in very dry hermetic packages.

Pre-programming Testing and Screening

As discussed under circuit design, functional testing, making use of a pre-programmed test word and bit line, and the subsequent test fusing provide the manufacturing screens used to correlate with field programming and subsequent device performance. These tests are used in conjunction with standard DC parametric tests. The latter can be performed either before test fusing or afterwards. However, functional testing using the extra test circuitry can only be performed before all the test fuses have been programmed. Thus no meaningful functional

test can be performed on an unprogrammed part once it has been test fused.

Further refinements in these pre-programming screening tests can be made. One involves restricting test fusing such that only devices in which all fuses blow on the very first pulse are passed. Another involves stressing the normal array at high voltages to screen out would be leakage (figure #1) after test fuse programming. This is done by applying the highest voltage pulse that the device will see in the field on every bit line while selecting all the already open fuse locations on the test word line. If any marginal leakage or other circuit problems pull down the unselected word lines in the normal array such that random bits are programmed, these will become visible when the array is scanned for marginal or blown fuses in the subsequent enabled output leakage test. This provides an excellent method to screen out potential over blows, devices which program in random unselected locations.

Temperature test correlation has been one of the most debated subjects when considering LSI testing. PROM's are no exception. Generally the digital integrated circuit manufacturer employs a correlation technique that uses an extended V_{CC} voltage range for D.C. and functional tests at room temperature, $\sim 25^{o}C$, instead of the normal V_{CC} specified limits at both temperature extremes. The correlated V_{CC} values run well below and above normal minimum and maximum values respectively and depend on such design factors as the number of V_{BE} and V_{CE} drops, etc., in the circuit. A typical device might use 4.3 volts V_{CC} @ $25^{o}C$ to correlate with normal functionality at 4.75V and $0^{o}C$, figure #17. This technique is very effective for commercial temperature range SSI, MSI and most LSI circuits. However, the military temperature range presents a problem. SSI circuits correlate fairly well using the extended V_{CC} technique, however, this approach starts to fail with some of the MSI and many LSI circuits. The reasons involve the inability of increased V_{CC} voltage performance to correlate with increases in internal circuitry leakage experienced at high temperatures. Surface leakage, exponentially increases with temperature and can not be predicted at the high temperatures that military device specifications require, $+125^{o}C$ ambient. At the low end, $-55^{o}C$., beta and resistor value combinations prove to be too complex in large circuits to correlate with a V_{CC} voltage drop.

It becomes clear that to guarantee actual military temperature range performance to pass the Group A LTPD's referenced in MIL-STD-883A,[17] test method 5005.3, LSI PROM's must be 100% temperature tested D.C. and functionally. Two questions arise, why functionally, [18] and how do we meet this requirement on an unprogrammed PROM? If one looks at an LSI circuit under D.C. test it is immediately apparent that as little as 5% of the actual circuitry is being exercized, typically, only the input and output devices. One must also test the array and all the logic circuitry involved in decoding that array thereby guaranteeing internal thresholds as well as those visible at inputs and outputs. On an unprogrammed PROM the best way to accomplish this is to perform 100% temperature screening before test fusing such that the test bit line and word line are used along with its pre-programmed pattern. This checks both the output (bit) decode and the address (word) decode circuitry. After test fusing this becomes impossible to perform since no pattern remains to be interrogated. Testing the actual array at both temperature extremes is accomplished by performing the I_{CEX} or V_{OH} leakage tests at every address location with the circuit enabled. Since all bits should be in the high state in an unprogrammed device, the output should be off (high). If the circuit was designed in the reverse manner so that the output is low for an unprogrammed bit, V_{OL} should be tested at every address location. In the latter case although low V_{CC} and low temperature should be worst case conditions for V_{OL}, it is important to check both sets of extremes as the enable circuit may be sensitive at the high temperature and V_{CC} extreme causing a malfunction in which the outputs are disabled and reflect a high, off, logic state.

Temperature testing 100% unprogrammed PROM's both D.C. and functionally, prior to test fusing has been able to easily guarantee tightened LTPD levels for Group A tests (classes A and B) performed after subsequent screening and programming. These include both D.C. tests at temperature extremes, subgroup #2 and #3, and functional tests, subgroup #8.

Of course this temperature testing does not replace the MIL-STD-883A, Class B, final testing after the burn-in screen. Figure #18 summarizes a successful approach to military, "883" screening of both unprogrammed and programmed PROM's. Note that initially all parts go through the pre-test fuse temperature testing. After successful completion of one pulse test fusing, high voltage array stress and blank verification for extra bits (which may have resulted from the first two operations), the devices follow the normal screening flows with the following modifications. When factory programming is required, it is performed prior to any burn-in. All burn-in must be dynamic, condition "D".[2] This assures that the maximum amount of internal circuitry is exercized, and in the case of a programmed device, that each programmed fuse is stressed. Final electricals should include 100% functional temperature testing for already programmed devices and for unprogrammed circuits the quasi-functional array test via output monitoring with the chip enabled.[18] Following these flows we have found excellent field performance specifically in the case of unprogrammed class "B" parts. The combination of test fusing, array stress and burn-in are very effective in removing would be infant mortality failures on unprogrammed devices as well as improving field programmability

Programming

Many investigators have researched the effects of pulse width, rise time and number

of programming pulses on programmed fuse reliability.[2,6,7,19-22] It is now well known that fuses requiring long program pulses and blowing on the dwell or flat of the pulse, have an increasing propability of failure via growback.[2] This longer time corresponds to lower programming current requirements, figure #19, and reflects a non-adiabatic fusing mechanism. Fast, adiabatic fusing results when programming times are held below 1.0 msec. Blowing the fuse on a fast rise-time guarantees high programming currents, i.e., high dEp/dt conditions, where Ep represents the programming energy. This has been shown to favor wide separations of conductive material, nichrome, in the gap of blown fuse.[2,6] The wider the gap, the higher the dielectric breakdown of the gap. Experimental data suggest that growback is nothing more than the dielectric breakdown of the nickel and chrome oxide matrix found in the gap under the influence of very high potential fields originating from the close separations of the two conductive sides of the blown fuse under biased conditions, i.e., circuit operation.[2,23] Such field strengths may approach 10^7 volts/cm for separations of $\leq 100\text{Å}$ during normal circuit operation where a worst case potential of 3.0 volts exists across a blown fuse.

To eliminate the possibility of slow programming a re-definition of program pulse timing is necessary. The PROM circuits discussed here use a program pin (enable) pulse, figure #6, and an output pin pulse. The program pin pulse supplies the necessary base drive for the output decode (bit line) multiplex transistor through which the actual programming current is directed from the output pin, figure #1. It is important that the program pin pulse dwell overlap the rise and fall of the output pulse, figure #21. The output pulse is very short, $<80\mu$sec., and almost sawtooth in shape, emphasizing programming on the rise time. The dwell, in fact is only long enough to make oscilloscope presentations easy to read, calibrate and verify that there are no voltage spikes exceeding V_{OUT}. Verification is performed after each pulse at correlated V_{CC} thresholds. Both extremes should be checked to guarantee the specified spectrum or window of device functional operation between the V_{CC} and temperature limits. Although the correlated V_{CC} levels shown in figure #21 are for the commercial PROM, they have proven to be adequate for military temperature/V_{CC} range devices, so long as the parts have seen prior 100% temperature testing prior to test fusing. Redundant 100% D.C. and functional testing at temperature after programming is recommended as an option only where higher confidence levels are necessary than those attainable with the LTPD sample sizes used in the Group A subgroup testing.

Programming, the final manufacturing step, must be controlled. Programming equipment should be calibrated routinely and ideally under actual device programming conditions. This can be performed using a storage scope and two DC current probes clamped over external wires to the program pin and output pin respectively. Each time a new board or programming module is put into the equipment the whole system should be checked. Both timing and voltage levels should be checked against referenced specifications.

Programming yield is a measure of the manufacturer's success in correlating with circuit performance during field programming using the special tests previously outlined, i.e., test bit/word lines, test fusing, array stress, etc. It is also indirectly proportional to memory size. That is, a 4K memory will usually reflect poorer programming yields than a 2K device, etc., figure #22. This is nothing more than a reflection of the large amount of untested active circuit area on larger memories. Programming yields tend to vary over a range. Some lots may be high, some low depending on many random variables, but all should fit into a given range 90% of the time. Low programming yields do not necessarily mean poor reliability. One may conclude poor screening correlation at the factory as a result of low programming yield but an understanding of why the parts failed to program or over program is required before any effects on reliability may be extrapolated.

Conclusions

PROM reliability as in other IC devices is a composite of design, wafer process, assembly/package, screening and testing factors. Its LSI aspect requires a thorough understanding of the first two of these areas but field programmability brings into focus new and unique considerations in the assessment of integrated circuit reliability. Uppermost in the mind of the user must be the facts that the devices have not finished being processed and final tested until after programming and verification. If these steps are performed properly, the devices will reflect the same types of failure rates as the masked programmed ROM's. In general, failure rates have been found to be two or more orders of magnitude better than MIL-HDBK-217B estimates and many times better than devices smaller in chip size due to the simple approach used in designing the memory cell array.

Infant mortality levels are similar to MSI circuits, typically one percent or less and easily qualify for the MIL-STD-883A/MIL-M-38510 percent defective allowables, PDA's, of 5% for class "A" and 10% maximum for class "B". New programming approaches have reduced fuse related failure modes to an insignificant level. Typical infant mortality failures are due to circuit leakage problems similar to MSI bipolar digital devices or the normal packaging/manufacturing workmanship escapes, i.e., wire bonding, etc.

Military grade devices are easily defined but require additional screening considerations. The class "B" unprogrammed part is definitely a reality through specially correlated 100% temperature testing prior to test fusing. Test fusing, the high voltage array stress, and dynamic burn-in reduce infant mortality to less than one in one thousand devices. Beyond that requirement level, further system or board level conditioning under bias should meet the most stringent class "B" requirements.

Field programmability using nichrome fuses, is a reliable technique if one is aware of the special considerations required in performing the final programming and testing of PROM's. The nichrome fusible link has become the standard in all high performance programmable bipolar logic. The field Programmable Logic Array (FPLA) figure #23, is only the first of many standard LSI logic building blocks which will use this technique.

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[18] Note: MIL-STD-883A, test method 5004.3 does not require 100% screening for functional test at temperature, only 100% DC tests.

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[22] T.M. Donnelly and W.W. Powell, "Reliability Evaluation of PROM's", Final technical report RADC-TR-75-278, Feb. 1976.

[23] Results of unpublished work performed at MMI.

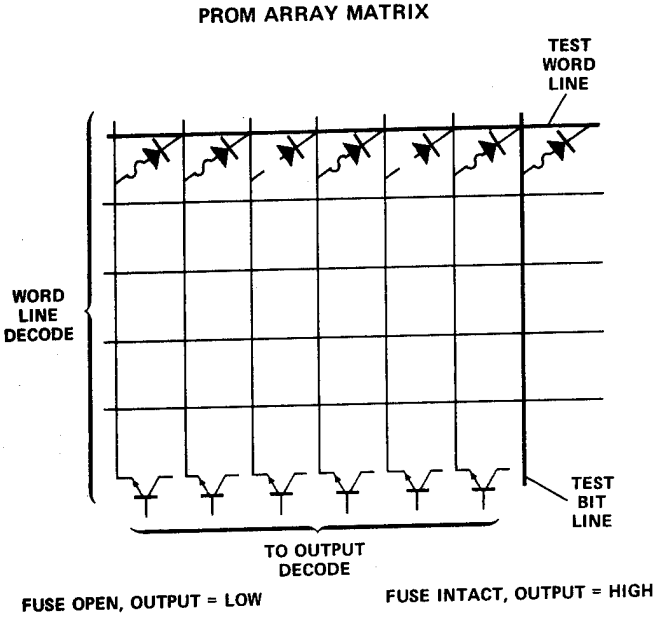


FIGURE #1

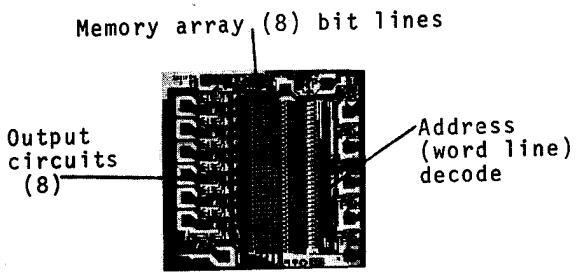


FIGURE #2

256 (32x8) bit PROM

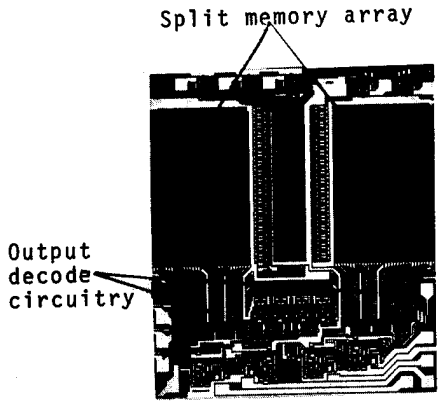


FIGURE #3

2048 (512x4) bit PROM

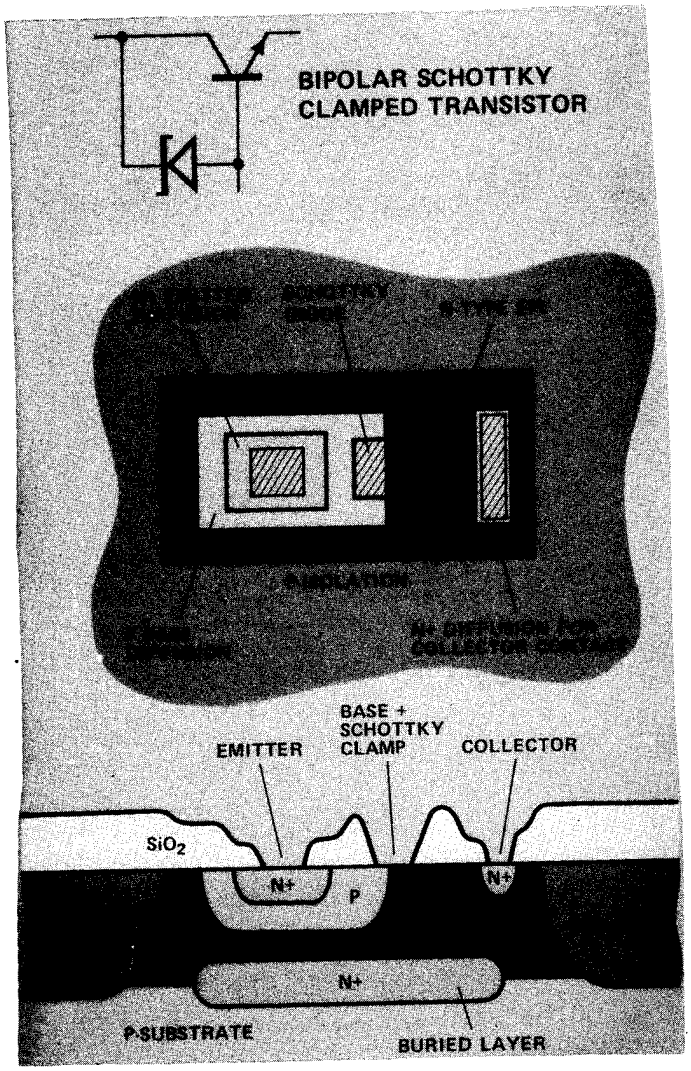


FIGURE #4

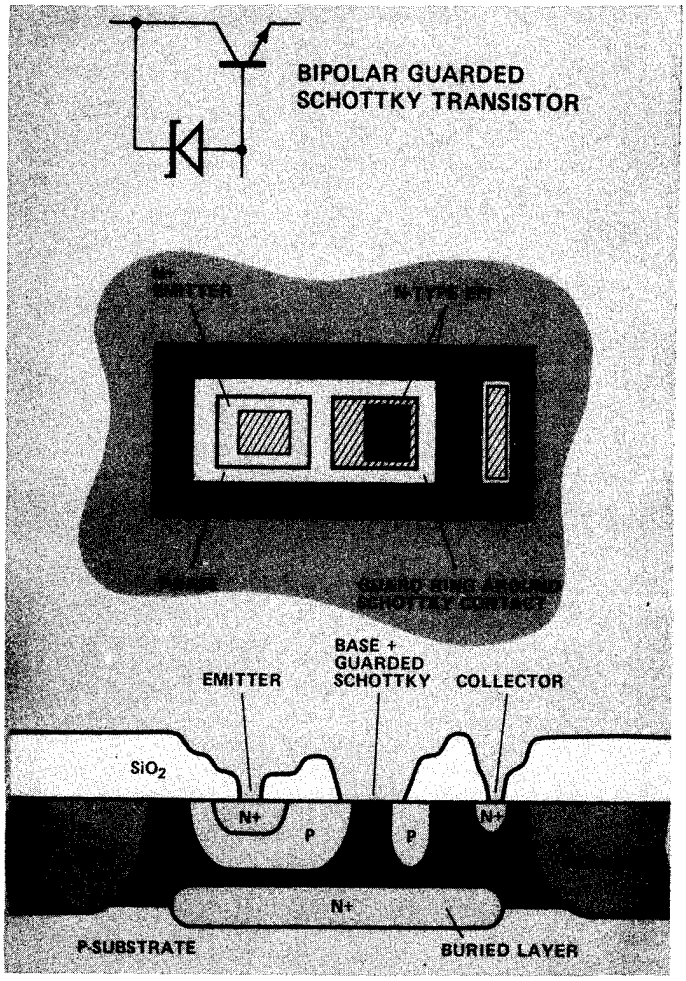


FIGURE #5

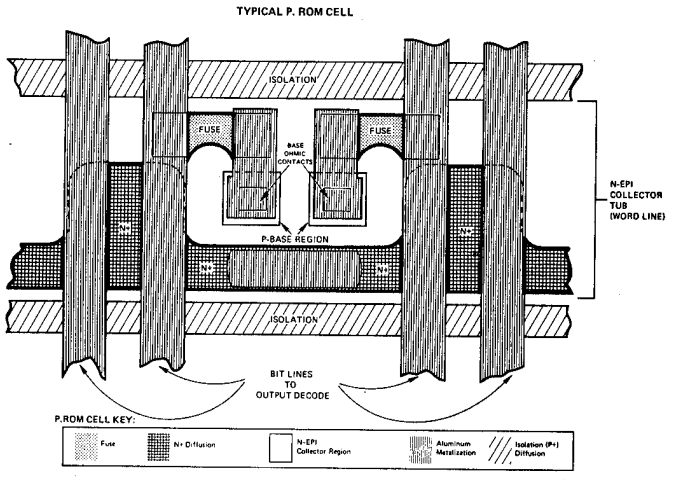


FIGURE #7

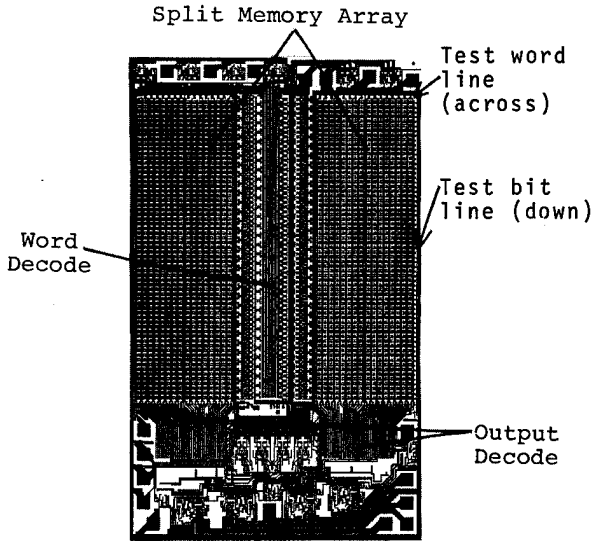


FIGURE #8
4096 (1024x4) bit PROM

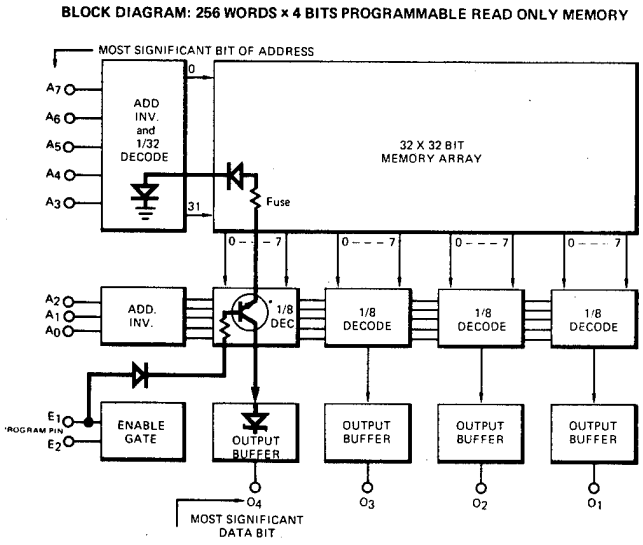


FIGURE #6

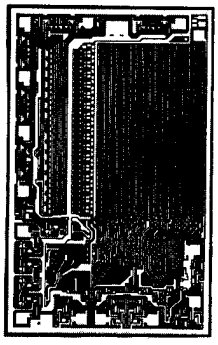


FIGURE #9
1024 (256x4) bit PROM
Single Array

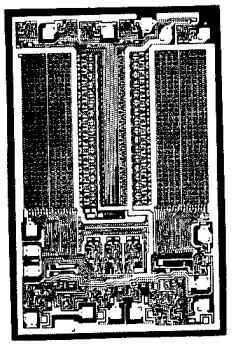


FIGURE #10

1024 (256x4) bit PROM
Split array

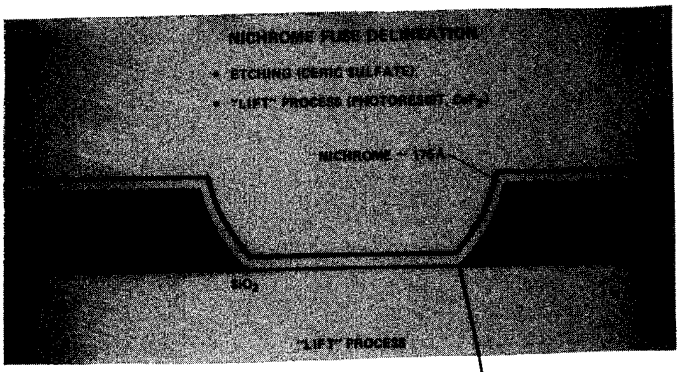
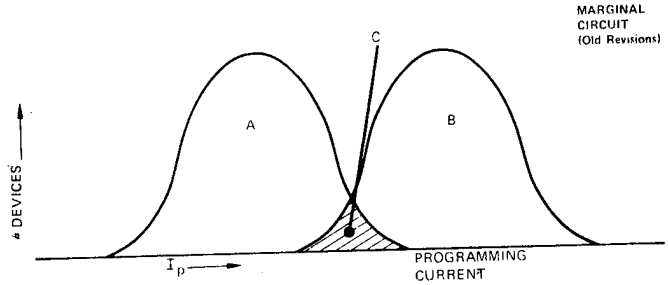


FIGURE #12

Normal
separation point

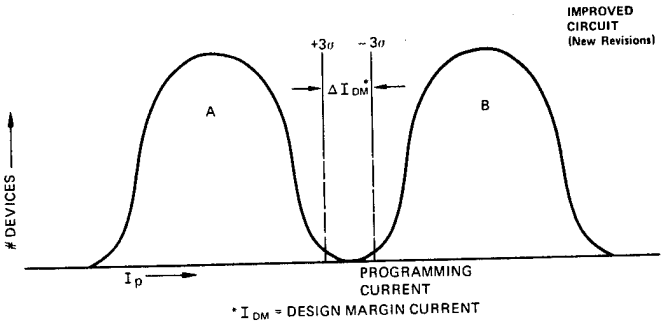
CIRCUIT DESIGN REQUIREMENTS FOR
PROGRAMMING CURRENT



A. DISTRIBUTION OF REQUIRED PROGRAMMING CURRENT FOR THE FUSES OVER ALL DEFINED PROCESS VARIATIONS.

B. DISTRIBUTION OF PROGRAMMING CURRENT AVAILABLE TO THE FUSE AND LIMITED BY THE DEVICE CIRCUITRY OVERALL DEFINED PROCESS VARIATIONS.

C. OVERLAP AREA WHERE PROGRAMMING CURRENT IS LIMITED TO THE FUSE PRODUCING FUSES WITH A HIGHER PROBABILITY OF "GROW BACK" AND A NUMBER OF FUSES THAT WON'T PROGRAM.



*I_{DM} = DESIGN MARGIN CURRENT

FIGURE #11

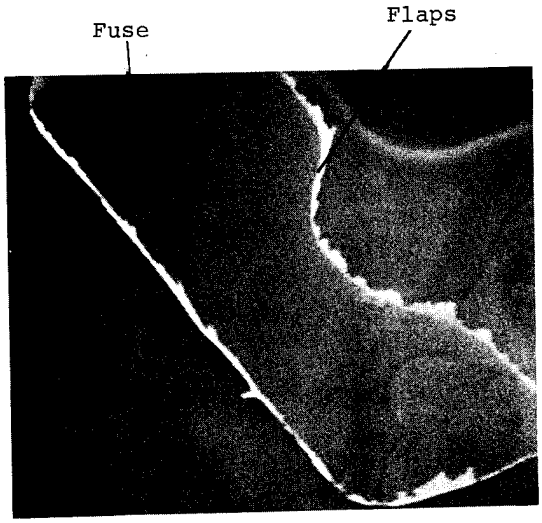


FIGURE #13

Nichrome fuse with flaps

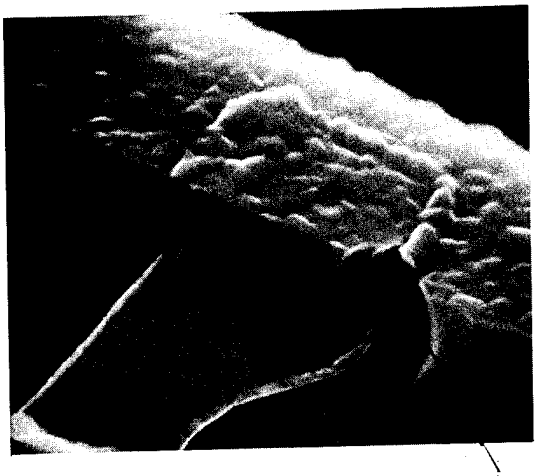


FIGURE #14

Nichrome fuse with flaps
after metal deposition/etch

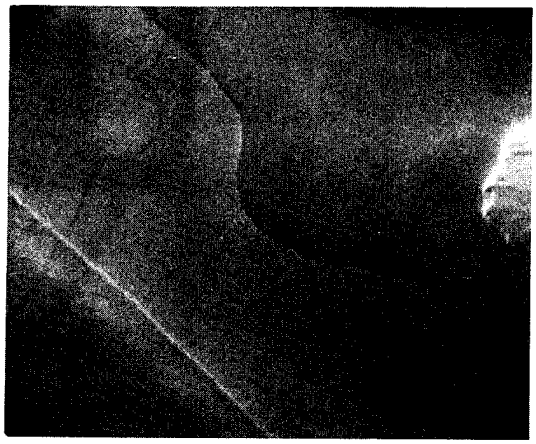


FIGURE #15

Nichrome fuse without flaps

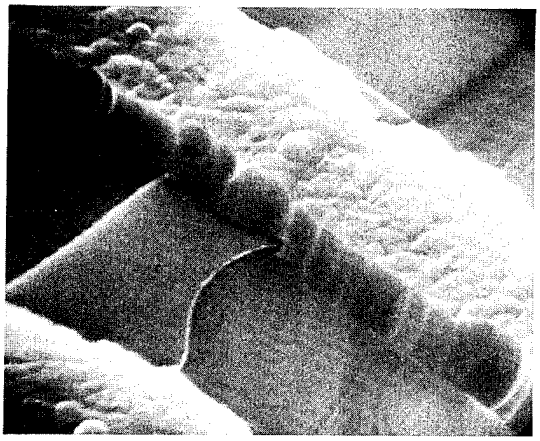


FIGURE #16

Nichrome fuse without flaps
after metal deposition/etch

FUNCTIONAL TEMPERATURE TEST CORRELATION

	COMMERCIAL	MILITARY
STANDARD		
TEMPERATURE & V_{CC} RANGES	0 → 70°C. 4.75 -5.25 V.	-55° → +125°C. 4.5 -5.5 V.
CORRELATED	@ 25°C. 4.3 -6.0 V.	@ 25°C. 3.8 -7.2 V.
CORRELATION ACCURACY		
SSI	99%+	97-99%
MSI	98-99%+	90-97%
LSI	97-98%	85-95%

FIGURE #17

STANDARD HI-REL 5004 SCREENING

MIL-STD-883 FLOW	METHOD	883C PROM/FPLA Unpro.	883C PROM/FPLA Prog.	883B PROM/FPLA Unpro.	883B PROM/FPLA Prog.
INTERIM TEST DC & FUNCTIONAL @ -55°C, +25°C, +125°C; AC @ +25°C	DATA SHEET LIMITS	√	√	√	√
TEST FUSE/ARRAY STRESS/VERIFY	1 PULSE	√	√	√	√
PROGRAM/VERIFY	CUSTOMER PROGRAM	–	√	–	√
BURN-IN 160 HR. @ 125°C	1015.1 COND. D	–	√	√	√
FINAL ELECTRICAL, DC, FUNCTION -55°C, +25°C, +125°C; AC @ 25°C	DATA SHEET LIMITS	–	√	√	√
LOT ACCEPTANCE GROUP A-SUB. 1, 2, 3, 7, 8, 9	5005	√	√	√	√

FIGURE #18

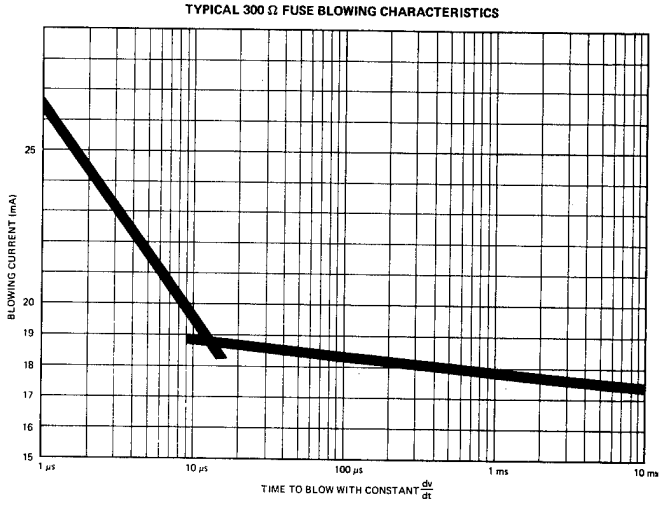


FIGURE #19

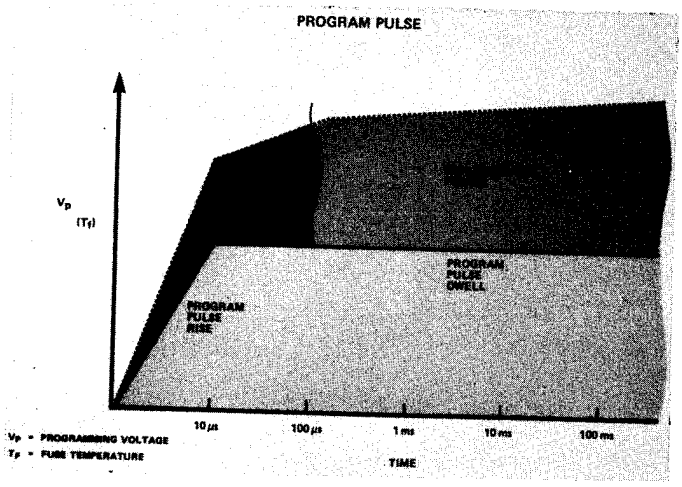
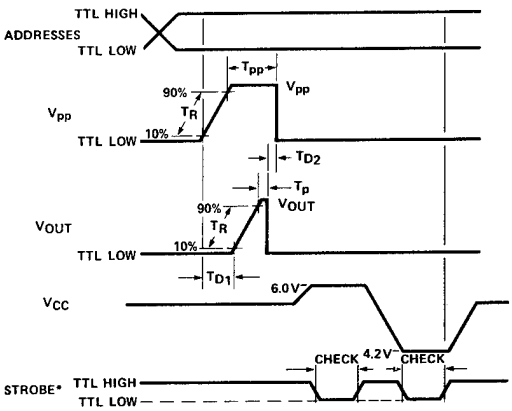


FIGURE #20

PROGRAMMING TIMING



T_R 0.4 V/μs ± 15%
T_{pp} 95 ± 15μs
T_p 7 ± 1μs
T_{D1} 80 ± 10μs
T_{D2} 100ns minimum

NOTE: OUTPUT LOAD = 0.2mA DURING 6.0V CHECK
OUTPUT LOAD = 12mA DURING 4.2V CHECK

FIGURE #21

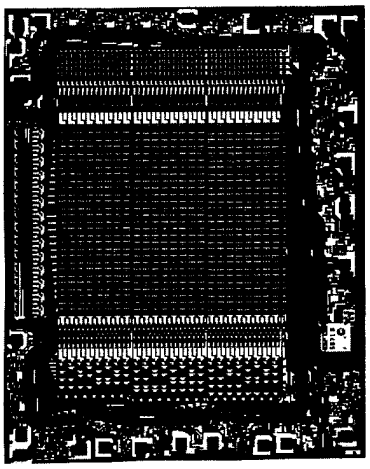


FIGURE #23

Field Programmable Logic Array (FPLA) using nichrome fusible links

PROM PROGRAMMING YIELDS

P/N	TOTAL BITS	ORGANIZATION	AVE. % YIELD	RANGE
5330/1-1	256	32 X 8	99	95-100
5300/1-1	1024	256 X 4	97	91-99
5305/6-1	2048	512 X 4	95	88-98
5335/6-1	2048	256 X 8	92	82-95
5340/1-1	4096	512 X 8	90	80-95
5350/1-1	4096	1024 X 4	92	86-95
5380/1-1	8192	1024 X 8	80	70-85

FIGURE #22

DYNAMIC PERMEABILITY METHOD FOR EPOXY ENCAPSULATION RESINS

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Introduction

Water vapor permeability through semiconductor encapsulation is one of the fundamental contributors to device failures. Such permeation accelerates ionic mobility, changes the dielectric properties of the encapsulant and contributes to chip corrosion. To evaluate candidate encapsulation materials and develop improved materials requires an adequate permeation test criteria and an understanding of the effects of formulation and processing variables on permeability. Unfortunately, standard permeability tests suffer from being very time consuming to perform, limited in use at higher temperatures and difficult to measure small permeation rates accurately. The purpose of this paper is to describe the use of a dynamic permeability test which overcomes these limitations and demonstrate its application to the evaluation of epoxy molding compounds developed for encapsulation markets.

Limitations of Existing Tests

All the older permeability methods have serious drawbacks which prohibit their use in evaluating thermosetting molding compounds at high temperatures. The standard cup methods, such as ASTM E-96 which require sealing the edges of the specimen to a container, do not have adequate sensitivity and are subject to errors caused by leaks which are very difficult to detect. They usually take many weeks or even months to obtain sufficient data on low permeability materials.

Other methods which measure differences in pressure or volume such as ASTM D-1434 (Dow cell) depend on degassing of the polymer and isolating the cell for a period of time to observe whether it has been degassed. Mercury is used in the monometer for measuring the pressure change which limits its use to non-reactive gasses and restricts its use at elevated temperatures because of the hazards of mercury vapor. It also is time consuming since measurements must be made until a linear plot is obtained.

Methods which use electrical moisture detectors such as the method published by Hadge, Riddell and O'Toole are sufficiently sensitive, are approximately 10 times more rapid than cup tests and can be used on materials in thicknesses typical of molded parts. Although this type device solves many of the measurement problems, it is still limited to only a moderate temperature range and may be poisoned by reactive outgassed products.

The dynamic method described in this paper overcomes all of the limitations of the previous methods. Its advantages are:

1. Measures permeability as a function of temperature,
2. Measures permeability on materials in thickness typical of molded parts,
3. May be used with any permeant and at any temperature by careful selection of cell material of construction,
4. Reaches equilibrium conditions rapidly, usually within an hour for most materials,
5. Measures permeability and diffusion coefficient directly.

Summary of Method

The polymer sample is clamped into a cell as shown schematically in Figure 1 and both sides of the cell are purged with nitrogen. The gas on the lower side of the cell passes through a thermal conductivity detector which is connected to a potentiometric recorder. When the recorder stabilizes at the baseline for the nitrogen carrier gas the polymer is known to be degassed. The nitrogen carrier gas in the upper half of the cell is then replaced with the water vapor or permeant gas and the rate at which the permeant passes through the polymer is indicated on the recorder. The detector is calibrated for the permeant by direct injection of a known amount before and after each permeability test. The resulting recorder trace is used to calculate permeability, diffusion and solubility coefficients.[2]

Experimental Details

Equipment

The equipment shown schematically in Figure 1 is similar in several respects to a gas chromatograph except that the permeability cell replaces the usual gas sample valve and column. The apparatus was constructed of 316 stainless steel. Connections were made with 1/8" tubing to minimize the volume and the 4 way valve has straight through flow to prevent mixing and restriction in the valve. The volume of the permeability cell is approximately 5 cc. The sample is clamped between the stainless steel flanges which creates the primary seal between the polymer sample and the metal. A 1/8" Viton-A o-ring is used to insure against leakage.

The detector system is a thermoconductivity cell with thermistor bead detectors (made by Gow-Mac Instrument Co., Madison, NJ). These glass coated beads have high sensitivity and are resistant to most compounds, especially at the low concentrations present in the carrier gas stream. Detection limit is around 1 PPM in the carrier gas. Any other gas chromatograph detector or other specialized detector could be used.

Sample Preparation

The epoxy samples were transfer molded and post cured using standard thermoset molding techniques. Discs were molded 4-1/4" diameter and 20 mils thick.

Procedure

Measurements are made isothermally and the effects of temperature on permeability obtained by running at several temperatures. Water vapor was generated in a round bottom flask connected to the permeability cell with heated lines. This approach provides water vapor at atmospheric pressure independent of cell temperature.

Calibration of the detector is performed in a simple manner for each test run. Injection of 1 microliter of water directly into the carrier gas stream

produces a known relationship between volume of permeant and unit area of the recorder trace produced during a permeability test. The advantages of the calibration procedure are that it is direct, eliminates instrumental variables such as detector temperature and current, is independent of the carrier gas and the thermal conductivity of the permeant and eliminates the need to measure the carrier gas flow rate.

Figure 2 shows a typical permeation curve as observed on the recorder. Initially both parts of the cell are purged with the carrier gas (usually helium or nitrogen) until a stable baseline is obtained. This indicates that the polymer sample is outgassed. To start the test the carrier gas in the upper part of the cell is replaced with the water vapor, point A. Permeation is indicated on the recorder and continued until a steady state is reached, point B. By putting the carrier gas back into the upper side, a desorption curve can be obtained which is a duplicate of the adsorption curve. The permeability is obtained from the steady state portion and the diffusion coefficient from the slope of the adsorption or desorption curve.

In some cases the permeability is too small to be directly observed, as with a thick sample of lower temperature. The permeated gas can then be accumulated in the cell by using the 4-way valve. After a measured length of time the amount of gas can be determined by sweeping the collected gas over the detector.

The test is very rapid compared to other permeability test methods. One sample can be run per day since it must come to constant temperature and be degassed. Typical testing times to reach steady state permeability are about 2 hours at 90°C and as low as 20 minutes at 165°C. These results have led us to standardize our routine material evaluations on 20 mil samples at 145°C. Thus, both adsorption and desorption curves are run and a reference curve is obtained in a couple of hours. The amount of water vapor is not at the limit of the detector sensitivity so that the effect of baseline drift is minimal. Usually the sample is replaced and degassing is done overnight.

Reproducibility of permeability measurements made by retesting the same specimen show standard deviations of approximately 1% of the mean on permeability values and 2 to 3% for diffusion and solubility values. Since variations due to molding are significantly larger, the test is sufficiently precise to investigate molding parameters.

Calculation of Results

Permeability

The permeability coefficient is directly obtained from the steady state portion of the curve. The permeability coefficient, P, can be expressed as:

$$P = \frac{Q \times l}{p \times A \times t}$$

Q = amount of gas through film, ml (volume of gas is at 0°C and 1 atm pressure)

l = thickness, mils

A = area, inch^2

t = time, minutes

p = pressure across film, atm

All data in this report is given in units for P of:

ml·mil/100 in^2·24 hours·atm

Alternate unit for P can be obtained by:

(1.04×10^{-6}) P = g H_2O·mil/24 hours·100 in^2·mm Hg

(6.0×10^{-13}) P = ml·cm/cm^2·sec·cm Hg

The measured permeation, Q, in ml/min is multiplied by sample thickness, detector attenuations, and a calibration factor which includes sample area and time conversion into hours. The pressure must also be included if the water vapor is not at 1 atm.

Diffusion and Solubility Coefficients

Expressions for calculating the diffusion coefficient have been theoretically derived. They start with Fick's first and second laws of diffusion.

$$P = -D\frac{(DC)}{(DX)}$$ where P = ml/sec and C = concentration (2)

$$\frac{DC}{DT} = D\frac{(D^2C)}{DX^2} \quad (3)$$

These equations apply only if diffusion is the rate controlling step, rather than the sorption of the gas into the polymer surface and D is independent of concentration (3, 4, 5).

The usual approach to calculating diffusion coefficient is to use the derivation from Fick's Laws in terms of the time lag from exposure to the permeant to the initial observation of permeant passing thru the polymer sample,

$$D = l^2/_{6\emptyset}$$ where $\emptyset$ = time lag or time for the initial observation of gas passing through the polymer film. (4)

However, a precise value for $\emptyset$ is difficult to obtain experimentally with accuracy since the curve begins gradually and some time is required to purge the carrier gas from the cell with the sample gas. For this reason, a better approach was obtained based on the linear ascending portion of the cruve. This derivation allows the diffusion coefficient to be calculated from an expression for D obtained from a normalized permeation rate equation,

$$D = 0.176\, l^2 \frac{(\Delta s)}{(\Delta t)} \frac{(l)}{(s^\infty)} \quad (5)$$

The $\frac{\Delta s}{\Delta t}$ is the slope of the linear portion of the ascending curve and s^∞ is the steady state signal on the recorder.

Other variations of the theoretical equations can be used to determine whether D is independent of the concentration, but this is also indicated if the experimental absorption curve has a linear portion.

By assuming the diffusion is independent of the concentration:

$$P = D(C_2 - C_1)/l$$ where P = ml/sec/cm^2 (6)

If Henry's law (C = Sp) for gas solubilities is obeyed, i.e., the gas is in equilibrium with the solution at the polymer surface and the solubility is not a function of the concentration.

$$P = D\,S\,(p_2 - p_1)/l$$ where S = Henry's Law Constant (7)

Thus, for unit pressure differential and unit thickness, P becomes the permeability coefficient and is related to D and S:

$$P = DS \tag{8}$$

The units for D are cm^2/sec, the units for S are ml vapor/cm^3·cmHg, and the units for P are ml·cm/cm^2·sec·cmHg.

Thus, the permeation, diffusion and solubility coefficients are readily determined from the experimental data.

The temperature dependence of these coefficients follow an Arrhenius type equation, for example, in the case of diffusion:

$$\ln D = \ln D_o - \frac{\Delta E_D}{RT} \tag{9}$$

where E_D is the activation energy for diffusion.

This makes:

$$E_P = E_D + E_S \tag{10}$$

since P and S both follow the Arrhenius equation. Plots of log P vs. 1/T are useful in analyzing experimental data since linear plots should be obtained. Also, the best straight line can be drawn through all the data points and consistent results obtained. This is especially valuable in calculating the solubility coefficient since a small scatter in the P and D results have a relatively large effect on the scatter of the solubility results. The best values for solubility are obtained by using values of P and D from the plotted data.

Applications

The dynamic permeability test method has been used successfully to rank various Allied encapsulation grade epoxies and competitive epoxies and silicones as shown in Figure 3. The Arrhenius plot in Figure 3 of log permeability vs. temperature shows greater resistance to water vapor permeability of PLASKON® * MX-2342, an encapsulation grade epoxy molding compound, as compared to a competitive epoxy and silicone material. This relationship has been confirmed by semiconductor manufacturer's end-use life test at high humidities and temperatures on encapsulated electronic components.

The effect of the glass transition, Tg, is significant especially with permeants with small molecular dimensions as compared to the hole size in the polymer matrix. The step in the Arrhenius plot at Tg is expected and predicted by proposed diffusion theory.[6] One of our approaches to developing improved materials is to increase the glass transition temperature beyond the end-use temperature range of encapsulated devices. The experimental epoxy shown in Figure 3 shows one formulation whose permeability is flat to 190°C.

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*Registered trademark, Allied Chemical Corporation

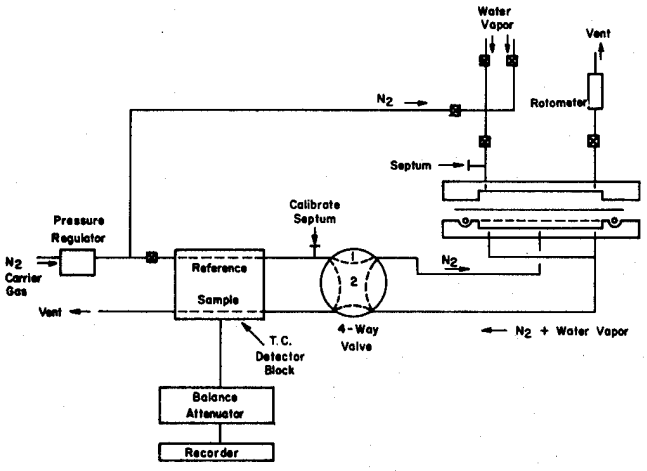
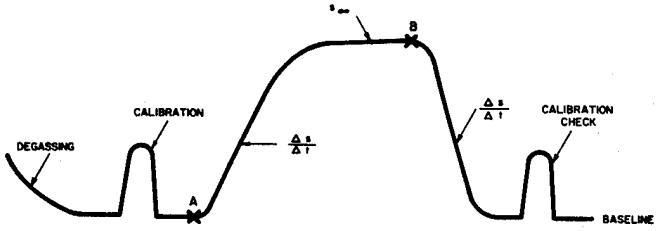


Fig. 1

PERMEABILITY APPARATUS

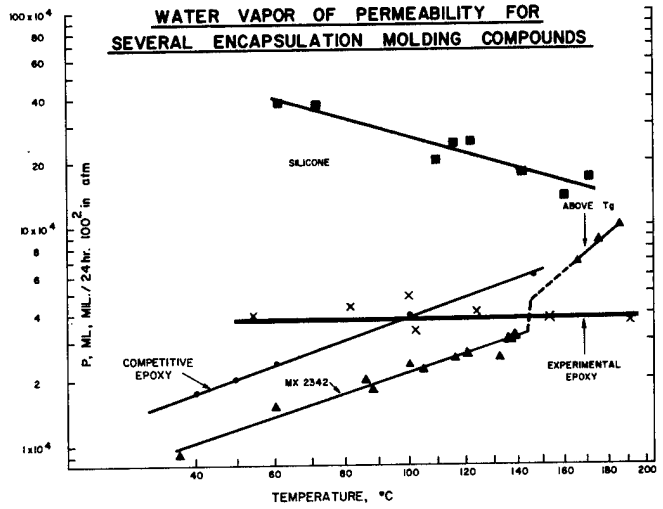


A: START WATER VAPOR IN UPPER PART OF CELL.
B: START CARRIER GAS IN UPPER PART OF CELL.
$\frac{\Delta s}{\Delta t}$: LINEAR REGION ON ASCENDING AND DESCENDING CURVE FOR DIFFUSION COEFFICIENT
s_∞: STEADY STATE FOR PERMEABILITY.

Fig. 2

TYPICAL PERMEABILITY CURVE

Fig. 3


WATER VAPOR OF PERMEABILITY FOR
SEVERAL ENCAPSULATION MOLDING COMPOUNDS
100 x 10⁴
80
60
40
20
10 x 10⁴
8
6
4
2
1 x 10⁴
P, ML., ML./24 hr. 100² in atm
SILICONE
ABOVE Tg
COMPETITIVE
EPOXY
MX 2342
EXPERIMENTAL
EPOXY
40
60
80
100
120
140
160
180
200
TEMPERATURE, °C

A STUDY OF PARASITIC MOS FORMATION MECHANISM IN PLASTIC ENCAPSULATED MOS DEVICES

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Abstract

With a view to preventing the formation of parasitic MOS in plastic encapsulated MOS devices, we studied the mechanism of the formation and found that parasitic MOS is due not only to surface mobile charge on oxidized silicon but also to bulk charge in plastic materials. Concerning an epoxy resin for semiconductor use, which is the most widely used material for plastic encapsulation, the behavior of bulk charge under pressure was investigated by electrical measurement and that under application of high voltage dc was also investigated electrically and by EPMA analysis. As a result, it was established that the majority of the mobile charge is actually certain ions with a negative charge and containing chlorine, rather than electrons or dipoles.

It was further confirmed that parasitic MOS formation is extremely scant in MOS devices encapsulated with the same type of epoxy resins with little hydrolyzable chloride ion, and hence that minimizing the ionizable component in plastic materials is highly effective in preventing parasitic MOS formation.

Motion of charge along the interface between silicon oxide layer and plastic could not be clarified. However, it is thought that parasitic MOS formation due to this motion can be prevented by providing an appropriate guard ring.

Introduction

In MOS devices sensitive to surface effects, accumulation of charge on the surface silicon oxide layer will cause an inversion layer or channel to form in the silicon beneath the oxide layer, as though a metal electrode with dc voltage were provided on the oxide layer. This phenomenon, called parasitic MOS, is known as a possible cause of misoperation of MOS devices.

According to our experience, parasitic MOS forms more readily in plastic encapsulations than in hermetic seals. This report deals with the mechanism of parasitic MOS formation dependent on the properties of plastic materials. In the study, we used an epoxy resin for semiconductors, which is the most popular plastic material for encapsulation.

Concerning the surface charge motion on silicon oxide layers, there are the analytical and experimental studies of Shockley et al.[1,2] Cases where conditions vary have been reported by Schlegel et al.[3] For a case where there is epoxy resin on the silicon oxide layer, we measured the charge motion and inversion layer formation using a model MOS device, and compared the results with measurements for a device without epoxy resin. The comparisons revealed that the bulk charge in the epoxy resin contributed greatly to inversion layer formation. The methods of analysis with the model MOS device and identification of mobile charge in the epoxy resin will be described.

Behavior of Charge in Plastic Encapsulations

As for the behavior of surface mobile charge on a silicon oxide layer, it is thought that surface potential distribution varies with time t as in Fig. 1 and the inversion layer also varies. Shockley et al., on the assumption that total density of surface mobile charge is independent of time and distance, analyzed the behavior and derived the following equation:

$$\frac{\partial V}{\partial t} = \frac{1}{C_0 R_\square} \frac{\partial^2 V}{\partial x^2} \tag{1}$$

for which the solution is:

$$V = V_0 \operatorname{erfc}\left(\frac{R_\square C_0 x^2}{4t}\right)^{1/2} \tag{2}$$

This indicates that an inversion layer induced by surface mobile charge is formed in proportion to the square root of time t.[1]

On the other hand, Schlegel et al. assumed that the total density of surface mobile charge varies with the surface potential of the oxide layer, and derived the following equation:[3]

$$\frac{\partial V}{\partial t} = \frac{\mu}{2} \frac{\partial^2 V^2}{\partial x^2} \tag{3}$$

for which the solution is:

$$V = V_0 f\left(\frac{x^2}{\mu V_0 t}\right) \tag{4}$$

where μ is the mobility of surface charge. In the final analysis, equation (4) also indicates that distance x is in proportion to the square root of time t.

Meanwhile, in order to investigate the motion of surface charge on a silicon oxide layer in the case of plastic encapsulations, we designed a test device (I) based on the model shown in Fig. 2. Using an n-type silicon substrate, we performed p-type diffusion at MOS detector A (to form a source and drain). Then, a thermal oxide layer with a thickness of 8,000Å was formed. And upon this layer a 1μm thick aluminum electrode is formed by vacuum evaporation and photo etching. Distance x between the V_G electrode and MOS detector A was varied in the range of 8μm to 150μm. When these test devices are encapsulated in epoxy resin and a V_G of -40V is applied at 110°C, charge (negative in this case) accumulates on the silicon oxide layer. When the surface potential becomes larger than the V_{th} of the silicon oxide layer, an inversion layer is formed in the n-type silicon, and when the

inversion layer reaches point A, the current I_{SD} across the source and drain at A increases abruptly. Therefore, the time from V_G application to increase of I_{SD} at A means the time t for the inversion layer formation to reach a distance of x from electrode V_G. In this way, it was found that distance x over which an inversion layer forms in an epoxy resin encapsulation is proportional to $t.^{0.8\sim1}$ This relationship is obviously different from the theoretical value $x \propto t^{1/2}$ stated above (Fig. 3). These results suggest that in making an epoxy resin encapsulation, inversion layer formation, viz., parasitic MOS formation, occurs at an early stage because accumulation of additional charge is superposed on the accumulation of charge along the silicon oxide layer (or along the interface between the oxide layer and epoxy resin).

To isolate and confirm this phenomenon, we made a new test device (II) (Fig. 4) by providing a guard ring (ground electrode) on the silicon oxide layer between electrode V_G and MOS detector A in test device (I). In test device (II), it is presumed that the charge motion from electrode V_G toward A along the silicon oxide layer (or along the interface between oxide layer and epoxy resin) is blocked by the guard ring. Measurements under the same conditions as for test device (I), i.e., at 110°C and V_G=-40V, are presented in Fig. 5.

In the region near the guard ring, an inversion layer is not easily formed, presumably because the charge is absorbed by the guard ring. The farther the site is removed from the guard ring, the more the inversion layer tends to form at the rate of $x \propto t$.[1] From this fact, it is inferred that the charge goes beyond the guard ring by proceeding in the epoxy resin, thereby accumulating on the surface on the other side of the guard ring and causing an inversion layer to form.

From the above, it is considered that, in a plastic encapsulated MOS device, not only the charge accumulation in accordance with $x \propto t^{1/2}$ along the silicon oxide layer but also the charge accumulation on the device surface via the interior of the plastic material contribute to inversion layer formation, viz., parasitic MOS formation.

Transverse Electric Field Effect (TEF Effect)

The charge motion along the interface between silicon oxide layer and epoxy resin can be blocked by the guard ring, as shown above. The problem, then, would be to block the bulk charge motion in the epoxy resin. Generally, charge motion viz., electric conduction, in a plastic material is due to electron motion, ion motion, or orientation polarization of dipoles. To find which of these phenomena is predominant, the following experiment was conducted.

It is known that when a plastic material is subjected to mechanical pressure, intermolecular distance shortens, with the result that an increase in electron mobility, viz., that in electronic conduction, occurs due to overlapping of electron wave functions, and at the same time a reduction in free volume causes a decrease in ion mobility and dipole orientation polarization, viz., that in ion conduction and polarization current. Therefore, depending on whether electric conductivity increases or decreases when pressure is applied, it will be known whether the carrier is electrons (when it increases), or ions or dipoles (when it decreases). Using a model as shown in Fig. 6, we applied a uniaxial pressure to test device (III) and investigated the pressure dependence of the electric conductivity in the epoxy resin. Test device (III) was made by forming a 0.5μm thick thermal oxide layer on a 1Ωcm n-type silicon substrate, then, by vacuum evaporation, forming two 75mm-long 1μm-thick Al electrodes (#1 and #2) facing each other and spaced 10μm. Across the two electrodes a voltage of V_m=50V was applied and the variation of current I_m due to pressure application was measured by means of a vibrating reed electrometer (10 minute values were used for I_m). The sample temperature was 140°C, or lower than the 160°C glass transition temperature of the plastic material (epoxy resin) used.

Measurements (Fig. 7) revealed a heavy drop in the electric conductivity of the epoxy resin resulting from pressure application. This suggests that the charge carrier is either ions or dipoles rather than electrons.

Next, to separate ions and dipoles and to investigate the polarity of the charge carrier, the TEF effect of this epoxy resin was measured.[4] The TEF effect is a method we had previously used in determining the polarity of a charge carrier in dc conduction in an insulator. We got a hint from the fact that the polarity of the charge carrier in a semiconductor can be found simply by using the Hall effect.

Fig. 8 is a sectional diagram of a specimen used in measuring the TEF effect. The specimen was made by encapsulating test device (III) with epoxy resin, and then providing a 1μm thick Al electrode #3 by vacuum evaporation on the epoxy resin over a 1mm thick piece of epoxy resin.

At 140°C, a dc voltage V_t was applied for the intended period across electrode #3 and the silicon substrate of test device (III). When the specimen cooled to 90°C, a dc bias V_m of 50V (ohmic conduction region) was applied across electrodes and current I_m at the time was measured by means of a vibrating reed electrometer. The measured I_m consists of the current component of the C-R cable equivalent circuit I_{CR} and the absorption current component I_a, which are given as:

$$I_a \propto t^{-\alpha} \tag{5}$$

$$I_{CR} = \frac{V_m}{RL} + \frac{2V_m}{RL} \Sigma(-1)^n \exp\left[-\frac{\pi^2 n^2 t}{CRL^2}\right] \tag{6}$$

where α is constant (=1.0∼2.0); C and R are respectively capacitance and surface resistivity per unit area of the silicon oxide layer of test device (III). L is the length of the gap between electrodes #1 and #2, and t is the time. In equation (6), Shockley's short circuit model is used. When $t \gg 0$, then I_a and the second term in equation (6) can be neglected, and I_m is reduced to V_m/RL. In this experiment, the 10 minute value of I_m was measured.

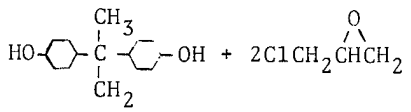
The results are shown in Fig. 9. The solid line shows the variation of I_m in relation to the time of application of V_t=-2.5kV and V_t=+2.5kV at 140°C. The broken line represents a case where V_t=0, indicating that I_m undergoes no change simply by subjecting the specimen to high temperature (140°C). Solid line ABC shows a carrier depletion in the region of test device (III) by a bias of $V_t>0$, and ADE a carrier accumulation there by a bias of $V_t<0$. In this case, therefore, the polarity of the charge carrier is negative. Moreover, occurrence of such a clear depletion and accumulation of charge suggests a motion of negative ions rather than a polarization by dipole orientation.

True Nature of Charge

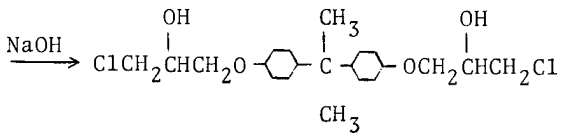
If the charge carrier is ions, their presence can be confirmed by analytical procedures. Aluminum foil electrodes of 20μm thickness were applied to both sides of an epoxy resin disk of 0.8mm thickness and 30mm diameter, and a dc bias was applied under conditions corresponding to the TEF effect, viz. 140°C, 3×10^4V/cm, 240 hours. When the specimen cooled to room temperature, the bias was cut off, the electrodes were removed, and their contact surfaces were examined with an electron probe microanalyzer. From the plus and minus electrodes, about the same amounts of Si, O, Al, Fe and Ca were detected. In addition, a large amount of Cl was detected in the positive electrode, and a trace amount of Na in the negative electrode.

Then, the epoxy resin was cut in half and the cross section was scanned with the EPMA to examine the transverse distribution of Cl and Na. The results are presented in Fig. 10. For Na, no uneven distribution was found. For Cl, however, a marked accumulation was observed over a distance of about 100μm from the positive side and a depletion over about 100μm from the negative side. Drops in Cl level correspond to the points where silica powder was mixed as a filler. From these results, it is presumed that the negative ions in epoxy resin which cause parasitic MOS formation are either Cl^- or other ions containing Cl.

The reason why a large amount of ionizable Cl is contained in epoxy resin is thought to be that Cl in epichlorohydrin is retained, as well-known, in epoxy resin during the epoxy resin synthesis process shown below for a typical epoxy resin (bisphenol A epoxy):[5]

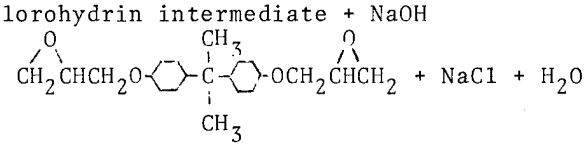


Bisphenol A Epichlorohydrin



Chlorohydrin intermediate

Chlorohydrin intermediate + NaOH



Bisphenol A Epoxy (n=0)

The epoxy molding compound for semiconductors used in this study contained 3,000 to 4,000ppm Cl (by fluoro X-ray analysis), of which about 1,500ppm was hydrolyzable chloride ions (by titration).

Meanwhile, in MOS devices encapsulated with a similar epoxy molding compound containing 700ppm Cl and 300ppm hydrolyzable chloride ions, parasitic MOS did not readily form, corroborating the finding in the present study.

Conclusions

This study was carried out for the purpose of clarifying the mechanism of and finding a preventive method for parasitic MOS formation in plastic encapsulated MOS devices. In our experiments we used epoxy resin, which is one of the generally used plastic material for encapsulation. If the results with the models used are applicable to actual phenomena, then the following conclusions may be drawn:

1. In plastic encapsulated MOS devices, accumulation of charge on the device surface, which often causes parasitic MOS formation, is due not only to charge motion in accordance with $x\propto t^{1/2}$ along the interface between silicon oxide layer and plastic material, but also dominantly to bulk charge motion in the plastic material. The total charge motion in a plastic encapsulation can be expressed by $x\propto t^{0.8\sim1.0}$ where x is the reach of charge and t denotes time.
2. The major carrier of the mobile charge in the epoxy resin used in the study is not electrons or dipoles but certain ions with a negative charge. It is highly possible that Cl is involved in these ions.
3. Therefore, a guard ring alone cannot be expected to prevent parasitic MOS formation effectively. Mobile ion components in the plastic material must be minimized and further improvement must be made in electrode design.

In our experiment, we have not been able to determine the possible effects of dipoles; nor have we given due consideration to Na or other positive ions. We plan to pursue these points further.

References

1. W. Shockley, H.J. Queisser, and W.W. Hooper, "Charges on oxidized silicon surfaces," Phys. Rev. Letters, vol. 11, pp.489-490, 1963.
2. W. Shockley, W.W. Hooper, H.J. Queisser, and W. Schroen, "Mobile electric charges on insulating oxides with application to oxide covered silicon p-n junctions," Surface Sci., vol. 2, pp. 277-287, 1964.

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4. S. Nishida, Y. Wakashima, and H. Inayoshi, "Measurement of transverse electric field effects on dc conduction in epoxy resin" Japan J. Appl. Phys., vol. 12, No. 1, pp. 147-148, 1973.

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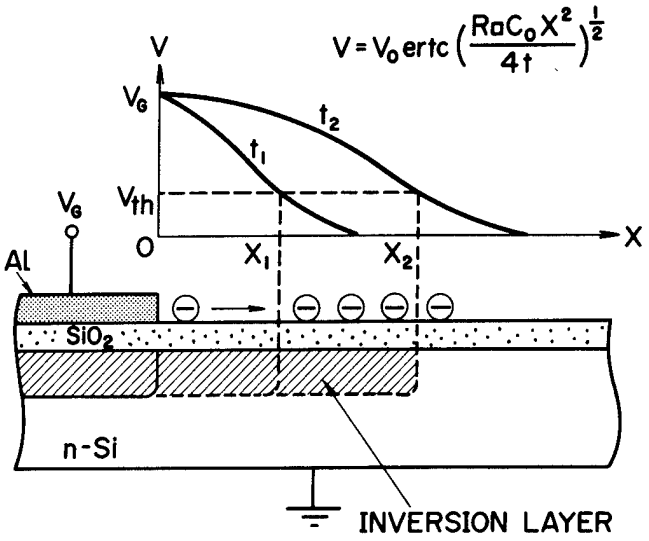

Fig. 1. Inversion Layer Formation by Surface Charge on SiO_2

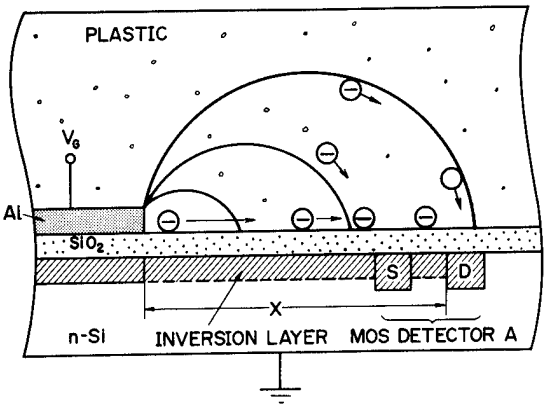

Fig. 2. Plastic Encapsulated MOS Device (Test Device [I])

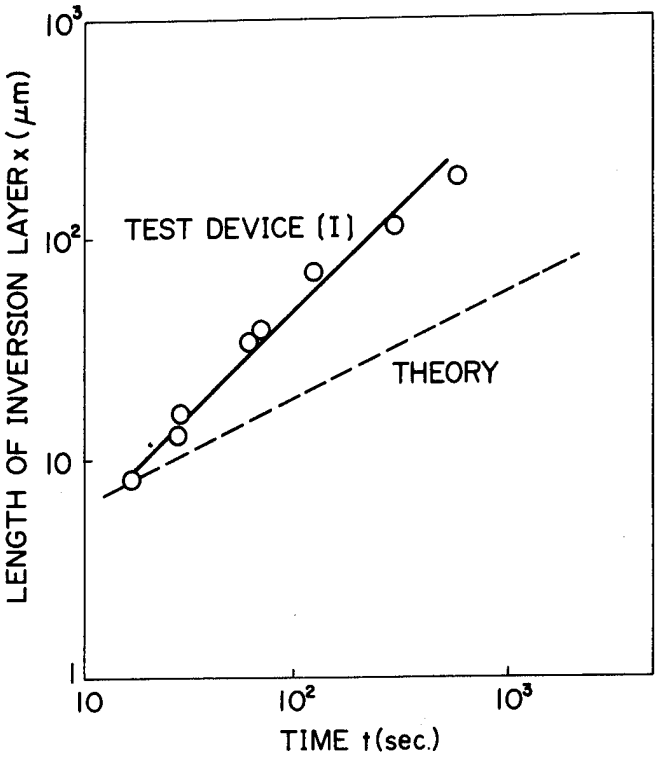

Fig. 3. Inversion Layer Formation in Plastic Encapsulated MOS Device

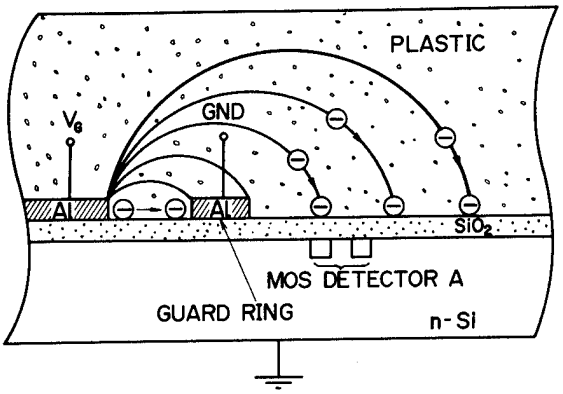

Fig. 4. Plastic Encapsulated MOS Device with Guard Ring (Test Device [II])

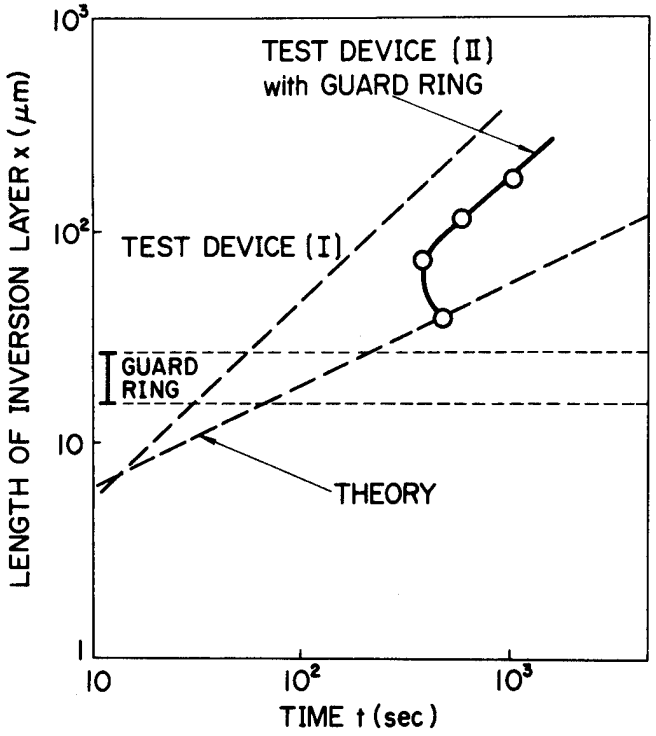

Fig. 5. Inversion Layer Formation in Plastic Encapsulated MOS Device with Guard Ring

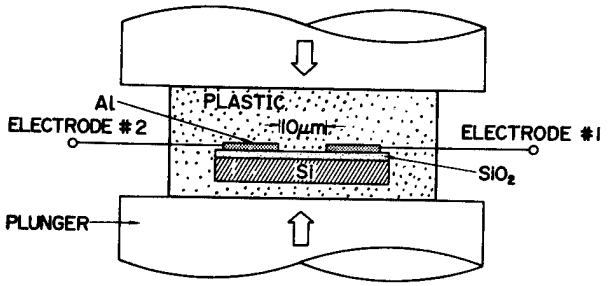

Fig. 6. Experimental Set-up of Uni-axial Pressure Effect

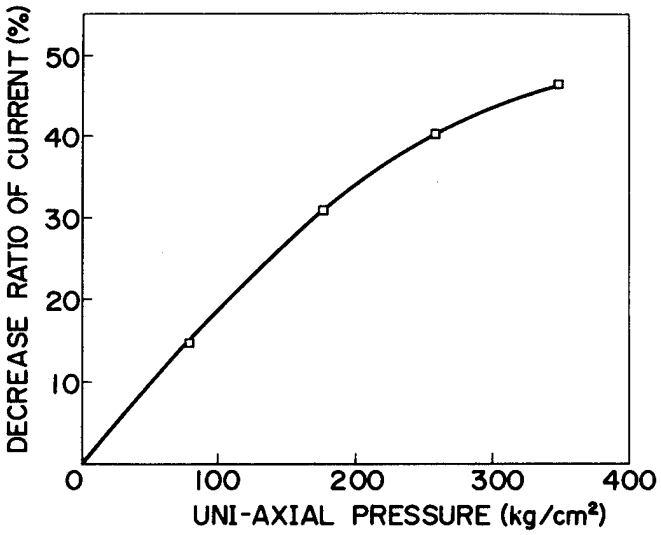

Fig. 7. Variation of Current by Uni-axial Pressure (140°C)

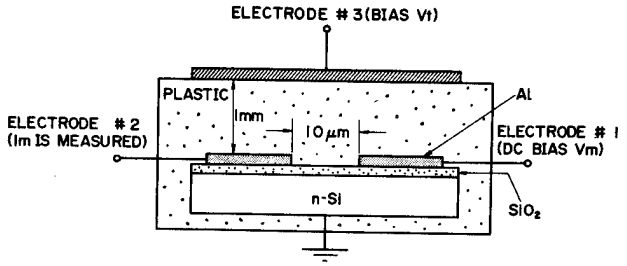

Fig. 8. Schematic Electrodes Arrangement of Specimen. Length of the 10μm Gap Between Electrodes #1 and #2 is 7.5cm.

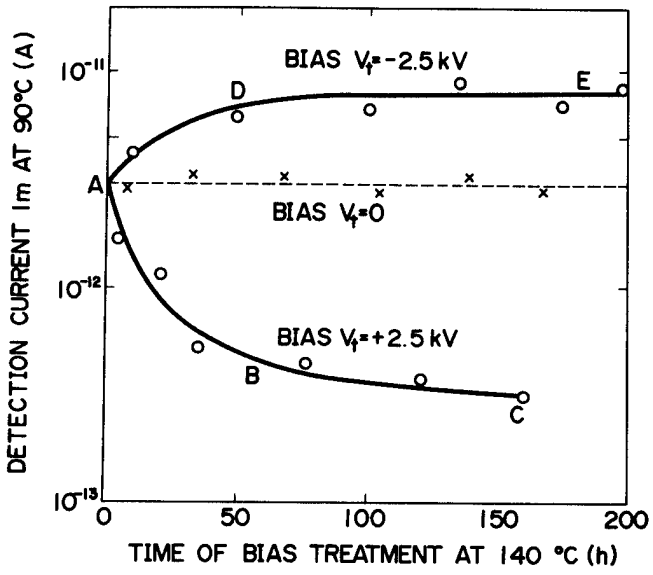

Fig. 9. Variation of Detection Current Measured Between Electrodes #1 and #2 with Bias (Curved Solid Lines) and Without Bias (Broken Line)

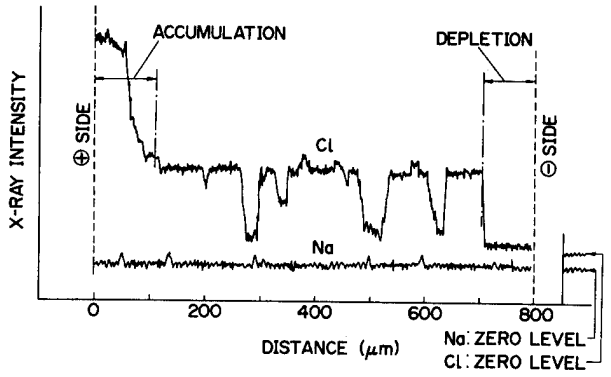

Fig. 10. Distribution of Cl and Na After B.T. Treatment (by Electron Probe Micro-analyzer)
(B.T. Treatment; 140°C, 2.5kV/0.8mm, 240h)

POLYIMIDE PASSIVATION RELIABILITY STUDY

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Summary

Special n-channel FET memory chips with non-random, purposely etched passivation defects are used to ascertain the effect of incompletely cured polyimide on the product's functional reliability. Polyimide is applied to the chip's surface and cured at 300°C for five minutes. This cure results in approximately 95% linkage formation as ascertained from IR spectrum analysis. Subsequently, the product is broken into four groups and further "cured" at 225°C for 0 (controls), 5, 25, and 50 hours, respectively. These samples are then put on life stress at 40, 85, and 130°C. For the control case, cumulative percent fail versus time data for steps in stress temperature is shown to have an Arrhenius model dependency with a ΔH of 1.1 eV. However, recovery of the failed cells under stress conditions (with bias applied) indicates the failure mechanism to be other than classical surface inversion. Data is presented showing the inverse dependency of the additional cure on cumulative percent fail. Explanation of this phenomena is attributed to dipoles that are associated with incompletely cured polyimide (potential linkages), aligning in the preferential E-field direction, thus inducing an image charge (an electron) at the silicon surface (quasi inversion). Degree of cure is ascertained from dissipation factor measurements performed on metallized silicon test wafers which have 2 - 4 μm polyimide films on their upper surfaces. Aluminum dot and mercury probe techniques are compared. Curves of dissipation factor versus cure time and temperature obtained via the latter technique are presented that illustrate two distinct phases of the polymerization/solvent expulsion process. The initial phase represents the disappearance of the linkage associated dipoles. The second phase is accounted for by the expulsion of molecular water which is a by-product of the polymerization process. Extended life stress reliability data (10K power on hours at 85°C) obtained from the previously mentioned special array chips is presented showing that polyimide in direct contact with the silicon surface does not invert same if fully cured (as defined by dissipation factor methods). In addition, it was found from dissipation factor data that a hot plate is superior to an oven for final cure.

Introduction

In recent years, various applications have been found for polyimides (PI) in the integrated circuit field, among which are chip passivation [1] as well as intermetal insulation [2]. For the former, a concern is manifest if PI is allowed to be in intimate contact with the chip's surface, especially if the PI is in a less-than-fully-cured state. One may hypothesize that dipoles associated with the unformed polymer linkages will align themselves under E-field urging, such that the positive dipole species is closest to the silicon. This would lead to inversion of the surface of P-type silicon (n-channel devices) and, hence, produce unwanted leakage.

The purpose of this study was to address the "dipole" concern and, if it was found to be real, develop a method of monitoring degree of PI cure to insure consistent reliability.

Dissipation Factor

In the following text, we will extensively refer to the "dissipation factor" or "measure of dielectric loss" as a means of determining the degree of polyimide cure. Hence a brief set of definitions regarding the subject is in order and follows.

Any lossy dielectric may be modeled by an ideal capacitance, C, in parallel with a resistor, R, whose value is dependent upon orientational polarization or permanent/quasi-permanent dipole moments. Further, consider this parallel combination to have impressed a voltage, V, as illustrated in Figure 1.

Figure 2 depicts the relationship between apparent power, P_{ap}; imaginary power, P_i, and real power, P_r.

We define the dissipation factor as the ratio of real power to imaginary power or:

(1) $$\text{Dissipation Factor} = \frac{P_r}{P_i} .$$

From Figure 2 it is immediately seen that this ratio is simply the tangent of the angle delta or:

(2) $$\frac{P_r}{P_i} = \tan \delta .$$

But, from Figure 1, P_r and P_i may be expressed as:

(3) $$P_r = \frac{V^2}{R} \quad \text{and} \quad P_i = \frac{V^2}{(\frac{1}{\omega C})}$$

Substituting (3) into (2) yields:

(4) $$\tan \delta = \frac{1}{\omega RC} .$$

where

R and C are measured values
ω = constant = $2\pi \times 10^6$ for our experiment.

Now let us assume the area, A, of the plates of the capacitor (and resistor) are much greater than

the electrode spacing, ℓ, hence

$$(5)\quad R = \frac{\rho\ell}{A} \text{ and } C = \frac{\varepsilon A}{\ell}$$

where

ρ = resistivity of the "lossy" dielectric
ε = resistivity of the "lossy" dielectric
Substituting (5) into (4) yields

$$(6)\quad \text{Tan } \delta = \frac{1}{\omega\rho\varepsilon} \text{ or}$$

$$(7)\quad \tan \delta = \frac{\sigma}{\omega\varepsilon}$$

where

$$\sigma = \frac{1}{\rho}$$

Hence, one may conclude that from sample to sample small variations in the interelectrode spacing and cross-sectional area cancel and what is observed is the basic physical properties of the media.

Dissipation Factor Methods

Evolution of dissipation factor measurements followed two stages:

Aluminum dots and

Mercury probe.

The following discussion concerns itself with these stages and reasons for their evolution.

Aluminum Dots ... Stage 1 (Figure 3)

Starting with a silicon wafer (used as a carrier) blanket aluminum which was used as a signal plane (lower capacitor plate) was deposited. Next, a thin film of PI was spun on (thickness was 1.2 to ~8.0 µm) the wafer. Aluminum dots of 762 µm (30 mil) diameter were then deposited on the PI film (capacitor "upper" plate). Removing a small area of the PI located at the periphery of the wafer allowed the underlying aluminum signal plane to be contacted. Contact was made to the aluminum dots on the upper surface with a small movable probe. The probes were connected (coaxial cable) to a Boonton Electronics capacitance bridge Model 75A-S8 that permitted capacitance and resistance measurements to be taken (at 1 MHz). In using this method, care must be taken to "null" stray capacitance and conductance, otherwise appreciable error will result. This may be accomplished by raising the movable "dot probe" just above the aluminum dot's surface, and adjusting the bridge to zero. The dot is then contacted and the capacitance/resistance values measured. The data thus obtained was substituted into Eq. (4) and corresponding dissipation factors calculated. At this point the shortcoming of this approach should be mentioned. As the PI cures (linkage form), molecular water is a by-product. The aluminum dot is much larger than the PI thickness and may, hence, have a "masking" effect or impede the removal of this water, thereby leading to altered dissipation factor data. This supposed limitation was eliminated by use of a mercury probe and discussion of same follows.

Mercury Probe ... Stage 2 (Figure 4)

The same vertical structure (as described in stage 1) minus the aluminum dots was utilized. Contact to the signal plane is as previously described while contact to the upper surface is now via a movable mercury probe (mercury diameter also ~762 µm). The probes were then connected (coaxial cable) to a Hewlett-Packard Automatic Capacitance Bridge Model 4270A and corresponding capacitance/conductance data obtained. The mercury probe, because of its 90-degree relationship to the signal plane, presents essentially zero stray conductance. However, stray capacitance must be measured and subtracted from the obtained readings. A comparison performed between the two techniques resulted in virtually a one-to-one correspondence (tan δ = 0.0082 aluminum dots, tan δ = 0.0081 for mercury probe; average over five readings each on the same wafer).

Polyimide Cure A La' Dissipation Factor

As suggested by the manufacturer, polyimide undergoes three basic curing stages: 130°C initial, 200°C intermediate, and 350°C final. Initial and intermediate cures are performed to allow the polymer to harden to a sufficient degree of facilitate normal manufacturing operations (handling and etching) while final cure renders the substance virtually impervious to chemical attack. An accurate method of specifying the degree of cure is the dissipation factor approach. Using the mercury probe techniques data was collected for 2 µm PI and a plot was made of dissipation factor vs time in minutes on a hot plate for temperatures of 320°C, 340°C, and 360°C (see Figure 5). Hot-plate temperature was monitored using a thermocouple attached to a silicon control wafer. Note that for time equals zero (initial plus intermediate cures) all dissipation factor readings are 0.024. From this starting point, the shapes of the curing curves are readily apparent. For 360 and 340°C, tan δ essentially arrives at a minimum value and remains constant after an elapsed time of five minutes, while the 320°C cure reaches the same value after approximately 30 minutes (end point not shown on curve). It should be noted that IR techniques failed to discern any difference between the beginning and end of this high temperature exercise. The equipment used was calibrated to register a change of 5%. Therefore, one concludes that the difference in IR readings for the final cure is insufficient to detect the changes that the above method readily discerns (above 95% cure).

Hot Plate vs Oven Cure

An experiment was also performed to compare oven vs hot plate cures (same temperatures). It was observed that the oven produced consistently higher dissipation factors than the hot plate for times as long as 30 minutes. The oven-cured wafers were then placed on the same temperature hot plate (350°C) and a corresponding lowering of the dissipation factor was observed (same value as wafers cured on hot plate only). This effect is thought to be due to the thermal gradient across a wafer placed upon the hot plate which would tend to migrate the molecular water formed during linkage formation toward the wafer surface and, hence, into the atmosphere. No such gradient is present in the oven (uniform wafer temperature).

Reliability Test Site Description

The basic test site described by the author and R. G. Berger in a paper [3] presented at the 1975 IEEE Reliability Physics Symposium was the test vehicle also used for this study. In essence it consists of an n-channel FET memory array chip that was processed such that holes to the silicon were generated in critical cell locations (Figures 6 and 7). These holes were subsequently filled with PI. Figure 8 illustrates the basic FET flip-flop memory cell. Note that the dashed resistor (and associated leakage current) is a direct function of the PI-induced inversion layer.

Reliability Data Correlation

The experiment was conducted to ascertain the effect of not fully cured PI on the product's functional reliability. The previously mentioned test vehicle with etched quartz holes filled with PI was cured at 300°C (hot plate) for five minutes (insufficient temperature and time to result in "fully" cured PI) and subsequently flip-chip module mounted. The modules were then split into four groups of equal size (160 holes each) and "cured" at 225°C for 0 (controls), 5, 25, and 50 hours, respectively. This low temperature was necessary, as the PbSn pads melt at approximately 250°C. Post cure, the three additional cure groups were stressed at 130°C, while the controls were stressed at 40, 85, and 130°C. Readouts were performed with the results shown in Figures 9 and 10. A "fail," for our purposes, was defined as a memory array cell, lying on the etched hole pattern, that did not function. It is seen (Figure 9) that upon completion of the 50-hour cure at 225°C, resulting in fully cured polyimide (see next section), the greatest stress reliability was obtained. On the 5-hour cure line in the past 40-hour region, the slope of the curve goes from zero to a decidedly negative value, thus indicating the polyimide is curing under stress (130°C prolonged time "cure"). The 40°C control cell showed no fails while 85°C and 130°C results are shown in Figure 10. The "recovery" of the 130°C cell is readily apparent. From a comparison of the time-to-fail of the 50% points, a ΔH for this phenomena was calculated to be 1.1eV which is in perfect agreement with earlier inversion-related work [3].

Dissipation Factor to Stress Data Correlation

Five wafers with approximately 4 μm PI and aluminum dots were placed in the same oven as per above (225°C) and dissipation factor measurements taken in the 0- to 50-hour range. Readings are shown in Figure 11. Upon completion of the 50 hours at 225°C, average dissipation factors of the five test vehicles were well within the fully cured range (Figure 5). The initial leveling off and subsequent decrease of this curve is believed to be composed of two phases. The constituents of the first phase are: (1) Dipoles associated with the uncured PI (open intermolecular linkages) and (2) dipoles associated with the molecular water that forms as a result of the complete polymerization of the PI (disappearance of intermolecular linkages). The initial decrease and subsequent leveling off of this curve is believed to be due to the disappearance of the PI-associated dipoles, hence leaving only the molecular water component. The final decrease would then be attributed to the removal of the water component.

The time/temperature related failure mechanism can be explained by dipoles that are associated with incompletely cured PI, aligning in the preferential E-field direction with the positive dipole species closest to the silicon surface. This dipole-associated charge then induces its image (an electron) at the silicon surface and behaves as if it were an ionic species with a mobility dependency (actually it would be that of a dipole rotational mobility). As a check, the substrate voltage was varied and found to control the fail (i.e., a failed cell would perform properly with a more negative normal substrate bias). The "recovery" process can now be explained by the curing (disappearance of dipoles and associated image charge) of the PI at 130°C for prolonged periods of time.

Long-Term Reliability Study

PI test site modules, as previously described, were placed at 85°C life stress for 10K POH. As controls, test sites with the induced quartz defects, but minus the PI were also included. Approximately 1000 defects of each type were considered. Figure 12 shows the results of the study. Note that both types of test sites were processed through the same line at the same time, hence, they should have the same amount of residual contamination contained within the defects. Residual ionic contamination is the cause of fail for the non-PI chips. Earlier work [3] has shown that this level, if mobile, will lead to very high percent cell fails in a short period of time at 85°C. Sodium levels in the PI were in the 7 to 10 ppm range. However, again as shown in Figure 12, the non-PI chips failed at least 6 times more often in the same time frame as the PI chips, even though the Na levels in the PI were very high. One, therefore, concludes that PI must at least reduce the mobility of positive ionic species contained within its molecular structure.

Conclusions

The conclusions of this study follow:

1. Dissipation factor is a viable tool for ascertaining the degree of polyimide cure.
2. Not fully cured polyimide behaves as ionic contamination (dipole related). The associated ΔH for this mechanism is 1.1 eV.
3. Sodium and residual ionic contamination is for practical purposes immobile in fully cured polyimide.

Acknowledgments

The author wishes to express his appreciation to all workers who have made this study possible. Special contributions were made by Stan Macie for his assistance throughout the program; Ron Westman for his interest; probing questions, and encouragement; and Dr. Ron Uttecht for providing the test samples. Thanks are also in order for Russ Berger and, again, Stan Macie for earlier polyimide related work. All mentioned above are from the IBM Essex Junction, Vermont facility.

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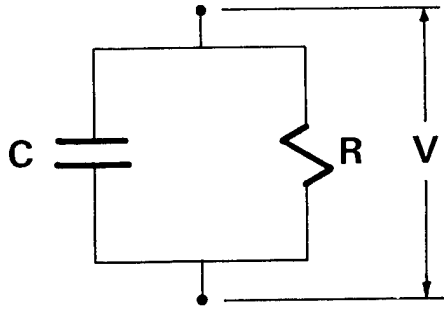

Figure 1. Circuit Model.

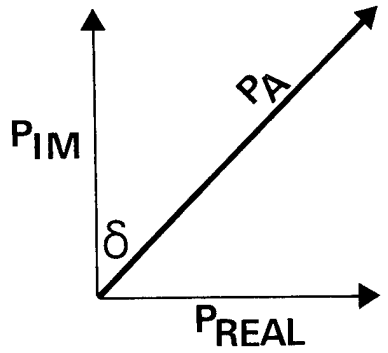

Figure 2. Power Diagram.

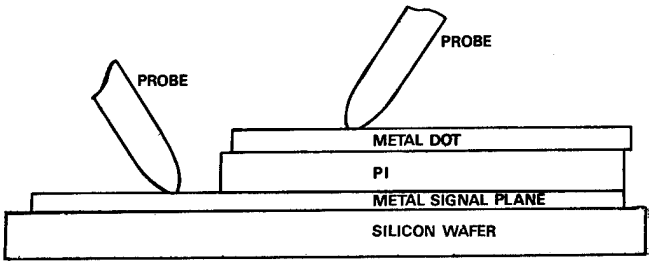

Figure 3. Metal Dot Technique Schematic.

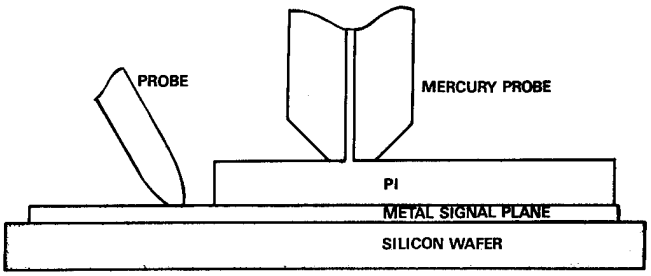

Figure 4. Mercury Probe Technique Schematic.

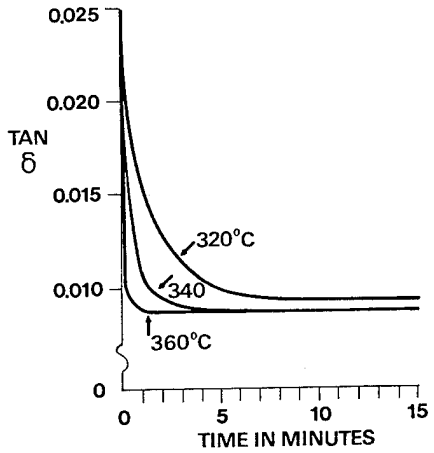

Figure 5. Tan δ Vs. Time in Minutes on Hot Plate for 320°, 340°, 360° C Cures.

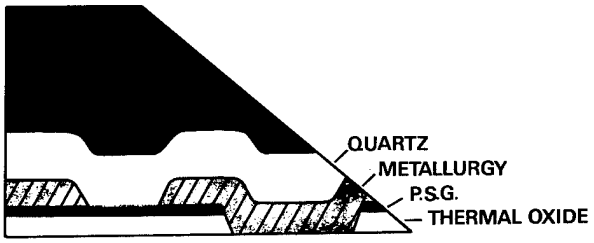

Figure 6. Normal Structure-No Etched Holes.

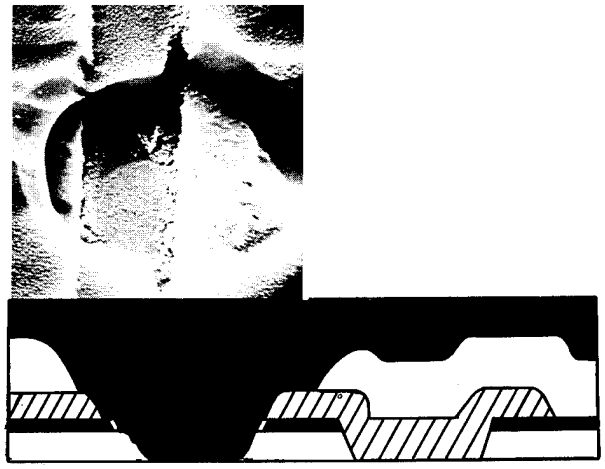

Figure 7. P.S.G. & Thermal Oxide Gone, Silicon Exposed.

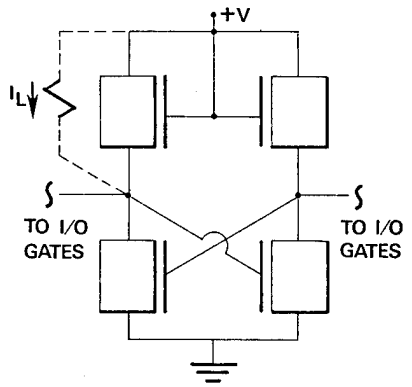

Figure 8. Cell with Inversion-Induced Resistor.

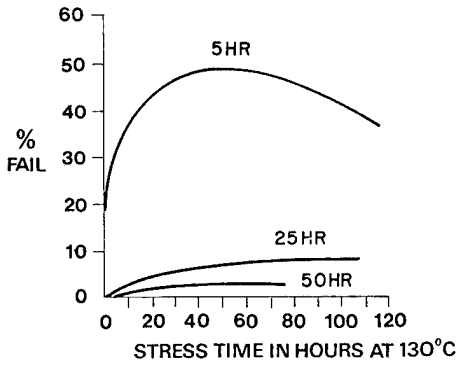

Figure 9. Additional Cure: % Fail Vs. Time at 130° C.

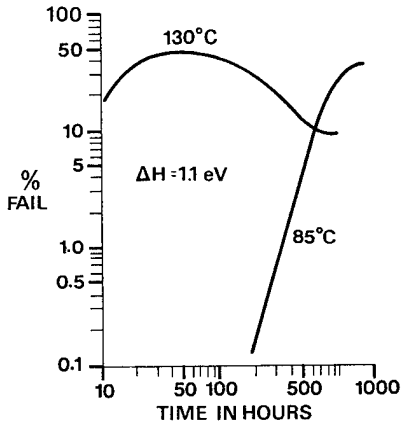

Figure 10. % Fail Vs. Time 85°C & 130° C Controls.

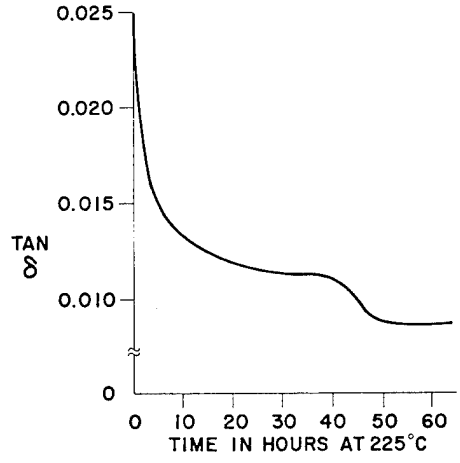

Figure 11. Tan δ Vs. Time at 225° C.

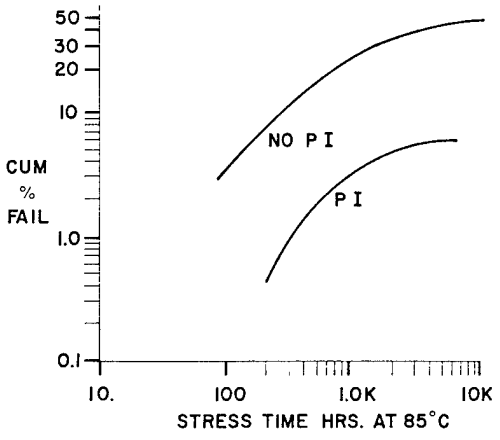

Figure 12. Cum % Fail Vs. Time at 85° C for Fully Cured and No PI.

THERMALLY STIMULATED DISCHARGE EFFECTS IN POLYMER ENCAPSULANTS

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Abstract

Regions of polymer encapsulant formulations are frequently exposed to high temperatures and high electric field strengths when used in encapsulation of semiconductor devices. The technique of thermally stimulated discharge is used to study effects of these polarizing fields on various epoxy compounds. The dependence of the unique discharge curve shapes found for these systems on chemical composition is noted. New methods of analysis are presented. Desirable polarization properties for an epoxy encapsulant are defined, and an approach to the development of systems exhibiting these desirable properties is outlined.

Introduction

Accelerated reliability tests subject polymer encapsulants to high temperatures at strong fields (e.g., high temperature reverse bias testing, HTRB) in an effort to simulate long term device operating requirements. The unfortunate part of this is that such testing requires large amounts of time and the use of live devices. Since this is both costly and time consuming, it would be expedient to develop more rapid procedures by which encapsulant candidates could be screened.

In an attempt to solve this problem, we have initiated a study to develop a quick and inexpensive screening procedure by which HTRB live device testing results might be predicted. As a part of this study, we have adopted the technique of thermally stimulated discharge (TSD) to investigate the molecular level phenomena occurring in a polymer encapsulant under accelerated testing conditions.

The Thermally Stimulated Discharge (TSD) Technique

Many dielectric polymer substances can be made to exhibit dynamic thermal charge relaxation phenomena. The usual dielectric absorption measurements use just such an effect. Figure 1 may be used to demonstrate the processes occurring in a dielectric which give rise to these relaxation phenomena. When a polymer is subjected to strong electric fields at high temperatures and then cooled while maintaining the field (a procedure called poling), long-lasting oriented arrays of separated charges can be formed. Such substances and their charge arrays are called electrets. To effectively apply an electret, its relaxation time must be long in comparison to the time scale of measurement. Commercial utilization of electrets has thus depended heavily on their room temperature stability.

Basically, there are two mechanisms by which the electret structure occurs. One is by actual dipolar charge separation (or orientation) occurring within the polymer molecule. The other is customarily attributed to the separation of free carrier species, under the action of the applied field. These species may originate from either impurity sources or from unreacted fragments of the chemical composition.

Thermally stimulated discharge (TSD) is a procedure whereby these formed electrets are heated and allowed to relax (depole) at a fairly rapid rate. Constituting mainly displacement charge movement, current is measured as it flows between probes connected to the oppositely polarized surfaces of the dielectric sample while the material is heated. The current levels so detected when plotted against temperature give thermograms having a structure representative of the relaxation processes occurring within the sample and indicating the energy levels required to activate the relaxation.

Figure 2 is a typical thermogram so generated exhibiting the general structural properties peculiar to a particular phenolic cured epoxy encapsulant. Note in particular the peaked nature of the curve and the other ways in which the current levels change as a function of temperature.

One of the favorable aspects of these measurements is that they are easily performed, and a TSD apparatus can be self fabricated from materials available in most laboratories without large capital equipment expenditures. Again these are qualities desirable for the initiation of a new testing procedure. Figure 3 shows a schematic of the basic equipment presently used to form the TSD charge separations. It consists of an experimental chamber which is capable of applying strong electric field strengths through a wide range of temperatures. In the present apparatus a silicone oil bath is used with an immersion heater and an immersed cooling coil. Other authors (1-5) have developed apparatus with TSD capabilities over a much wider temperature range. However, here we desired only to replicate the temperature ranges commonly encountered by our systems in HTRB testing.

The samples used in these experiments were transfer molded discs approximately two inches in diameter and about three millimeters thick. The sample surfaces are first coated with gold contacts. Following this they are suspended between spring loaded holders in a silicone oil bath as shown. A variable 75 kV DC power supply is then used to apply a voltage of 5,000 V/mm of sample thickness. Voltages on this order are generally standard for TSD work and in the present case are believed to be fairly representative of the field strengths encountered by encapsulants in the vicinity of P-N junctions, particularly under HTRB testing. Figure 4 details the poling procedure in terms of heating and field. The voltage is applied and the temperature is raised from room temperature to 150°C where it is held for 30 minutes. Afterward the sample is cooled to room temperature while the field remains on. In this way electrets are formed and are frozen into the bulk of the material. During poling, the movement of charge and the limited conductivity of the sample causes current to flow. This is noted at several points during the process, though no thermogram is made due to experimental complications and the ambiguity of displacement current and actual sample conductivity.

Now the sample is ready for depolarization (i.e., the release of the formed electrets). Figure 5 depicts the apparatus used in this part of the experiment, and again details the thermal history. Here the oil bath is heated at a constant rate of from 2 to 4°C per minute. A picoammeter is attached across the former poling electrodes, and the thermogram current output is recorded using a strip chart recorder on which the direct read temperature is noted at 5°C intervals.

Testing Program

Upon beginning the study we intended only to develop a screening procedure for HTRB testing. However, it soon became clear that TSD studies could improve our total understanding of physical and chemical processes in polymer encapsulants and even give hints concerning encapsulant failure mechanisms. We now believe that a number of previously knotty problems may be illuminated using the technique, and considerable insight into the mechanisms involved in encapsulant generated device failure may be developed. Among these are the problems of the various degenerative types of ionic mobility, of external field control as applied to the encapsulated chip, of specific transport processes as they occur in an encapsulant, and generally, of the physical behavior of the polymeric composition at the molecular level. A special advantage may be in the development of control mechanisms for interdictive impurities occurring at the dielectric-semiconductor interface.

Application to Epoxy Encapsulants

Generally, it is found in HTRB reliability studies that anhydride cured epoxy systems are more reliable than are phenolic cured systems. Figure 6 depicts representative thermograms for phenolic and for anhydride cured specimens. The TSD thermogram for the anhydride system does not exhibit the charge storage nor the charge relaxation (structure) that the phenolic systems exhibit. No thermograms were taken in which current levels higher than on the order of 10^{-8} amp were observed, and nearly all the systems tested gave thermograms which exhibited some sort of TSD structure. We wanted to delineate as to which of the previously mentioned charging mechanisms, freely mobile carrier species or dipolar molecular charge separation, is responsible for the large peaks in most of the phenolic cured systems. This would be of particular interest to us since it would allow us to adjust the formulation chemistry and thus control the effect. For purposes of demonstration, we shall look at a particular representative system. Such a system is an epoxy incorporating an epoxy cresolic novolac resin with a phenolic novolac hardener and an amine catalyst. Since the microscopic theory of dielectrics would predict that TSD curve shapes which are due to orientation of the individual polymer molecules should remain essentially unchanged if the mobile charge carriers were removed, it seemed to us that the easiest way to differentiate between the two mechanisms would be to remove the mobile species from the samples and to then run TSD measurements on the remaining material. To do this samples were poled at 150°C for periods of four hours or more to give the free carriers time to drift to the surface under the action of the applied field. Following poling, the sample surfaces were slowly abraded away in such a manner as to minimize surface heating as much as possible. After this the sample surfaces were recoated with gold contacts and a discharge thermogram was made before repoling. Then the samples were repoled (150°C for 30 minutes) and another dicharge thermogram was taken. Figure 7 gives the results obtained for our typical system. Here we see that after surface removal no further TSD structure could be detected. Even succeeding polarizations and depolarizations were in most cases unable to create nonzero TSD profiles. The conclusion to be drawn from this is that the thermogram structure is primarily caused by mobile charge carriers in the epoxy matrix, although occasionally a small amount of residual TSD structure is observed. This residual structure is attributed to a relatively small amount of molecular poling. Being a subject of some contention, the identity of the mobile species is not yet well understood. And trapping effects within the polymer bulk are believed to add severely to the complexity of the situation. Indeed, the protean nature of the possibilities due to the chemical reaction makes investigation of these species highly complicated. Fortunately, identification of the individual transport factors, as we shall soon see, is not a sine qua non to the present investigation. However, indications to date are that the governing factors in the TSD structure are the availability of reaction fragments and the size of these fragments.

Live Device Correlation

Up to now we have discussed TSD citing its viability for general polymer investigations and stating that it might serve as a screening test for HTRB. Centering our attention now on anhydride cured epoxy systems, we present in Figure 8, four thermograms taken for a series of these; all are identical in composition except for catalyst and flameout ingredients. Notice that systems B, C, and D all offer fairly flat, featureless TSD curves. On the other hand system A shows a greater increase in current level, especially at the higher temperatures. Table 1 gives live device data for a test matrix of transistors using these systems. Looking at the number of failures after 140 hours it is immediately obvious that system A was much worse than the others in live device performance. This is especially true for leakage current data, but also holds for gain. Keeping the TSD curves of Figure 8 in mind, this sort of data is indicative of the correlations seen between HTRB live device testing and TSD results. The lower part of Table 1 shows the differences between the four formulations. From this it appears that it is the combination of the changes of catalyst and flameout ingredient that generates the substantial changes in the TSD data. Such results support the idea that reaction fragments are prime contributors to TSD behavior.

Table 2 develops the correlation between live device data and TSD further. This shows a comparison of TSD charge storage (proportional to the area under the TSD curve) against leakage current change for a series of mixed p-n-p and n-p-n transistors. Here again we see a direct correlation between TSD results and HTRB leakage current results. This figure especially demonstrates the dramatic increase in leakage current with TSD and gives some indication of the sensitivity of TSD as an indicator for HTRB results.

To date we have not had a great deal of live device test data on phenolic cured epoxy systems, though we have studied them extensively using TSD. We are, however, hoping to acquire such data at an early date.

Desirable Encapsulant Properties

Based on the above results, it seems clear that the most desirable TSD property for an encapsulation candidate is a flat, featureless TSD curve. A slight overall increase in curve height with increasing temperature does not appear to greatly affect live device performance so long as the curve shape remains fairly flat. This has been observed to be true for both phenolic cured and anhydride cured systems. This type of curve shape is typical for anhydride systems, which are known for their improved HTRB device performance.

From our surface removal results we may readily assume that the purest materials available should be used in formulations. Further, and more importantly, chemical ingredients should be carefully chosen to minimize the possibility of unreacted species forming as freely mobile charge carriers. If unavoidably formed, action should be taken to limit to the greatest extent possible their migration through the reacted polymer matrix.

Direction

Several lines of investigation using TSD are suggested by results to date. In one program we are studying the individual components of encapsulant formulations. From this we are hoping to develop an understanding of the physical and chemical processes occurring as these components are combined to form finished systems. Another study entails the use of TSD to study the dielectric-semiconductor surface interaction. In the present phase of the project we are attempting to identify causative factors for poor reliability performance. The preliminary findings using this approach have been outlined above. We have found that in many cases it is the interaction between chemical species that provides the most important contribution to TSD structure.

Summary

Accelerated reliability tests of semiconductor devices frequently subject polymer encapsulants to high electric field conditions for long periods of time. Good examples of these high field conditions are the fringing fields associated with bipolar devices. Simultaneously, the encapsulated devices are subjected to temperatures as high as 200°C. Following this, the devices are allowed to cool sometimes with and sometimes without the electric field applied. This treatment gives rise to the possibility of forming electrets or oriented arrays exhibiting charge separation within the polymer matrix.

The method of thermally stimulated discharge in which these oriented arrays are frozen into the polymer bulk and then released has been used to study various organic macromolecular substances. This paper applies the technique particularly to epoxy encapsulants for semiconductor devices. The technique itself is described and a discussion of typical discharge curve shapes is presented. After this the curve shapes found for a number of different epoxy systems are given. The curves are found to have several unique features. Some of these are shown to be dependent on the nature of the basic chemistry of the epoxy formulation. Experimental evidence is cited showing the identification of specific facets of the data with specific charge separation mechanisms. New interpretive methods are advanced.

The experimental data can be summarized by Table 3. This indicates the relative performance characteristics of anhydride versus phenolic cured epoxy encapsulants. Also, the direct correlation between HTRB leakage current results and TSD current is demonstrated. Dependence of TSD performance on reaction fragment size has also been indicated.

Finally, the data are projected to indicate what the desirable polarization properties of an epoxy encapsulant must be. Experimental evidence shows the validity of this projection. A series of experiments detailing procedure for optimizing a polymer encapsulant on the basis of polarization effects is proposed. From this study choices of epoxy systems optimized for desirable polarization effects can be made.

Acknowledgements

The author wishes to thank Dr. John Sparapany for his suggestions and his encouragement in this study. Henry Harris is also to be thanked for his assistance in the TSD experiments.

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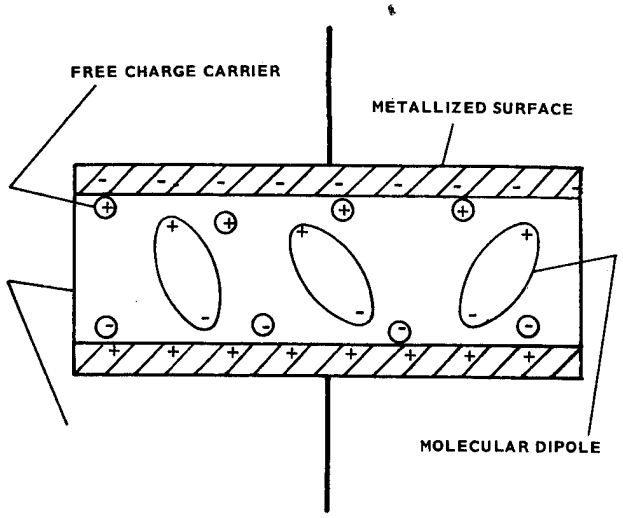


Figure 1. Formation of a Polymer Electret

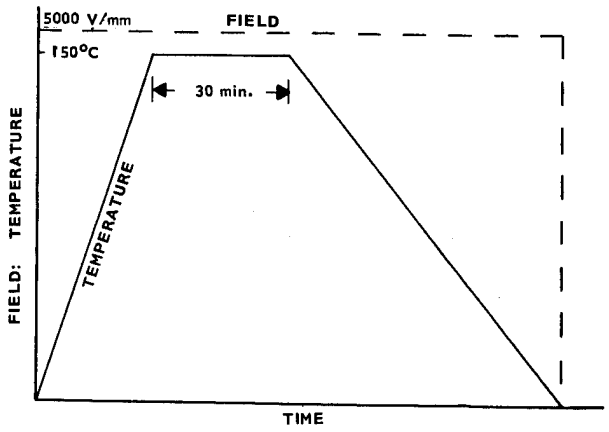


Figure 4. Poling Procedure

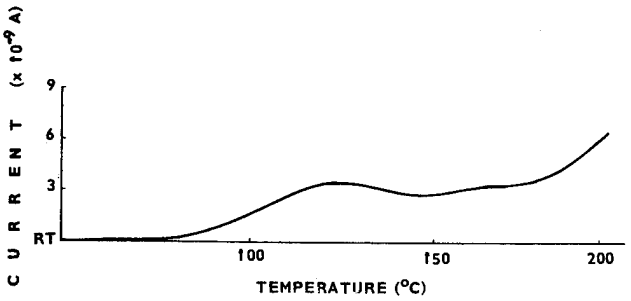
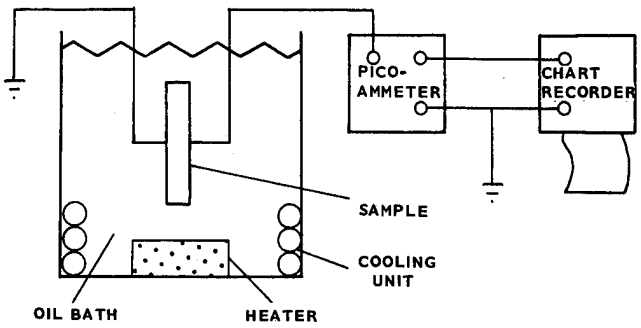


Figure 2. TSD for a Typical Polymer System



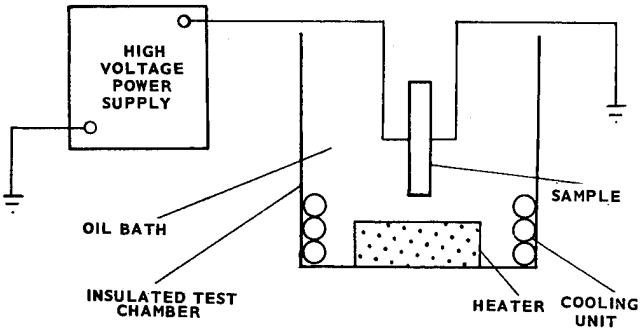


Figure 3. Poling Apparatus

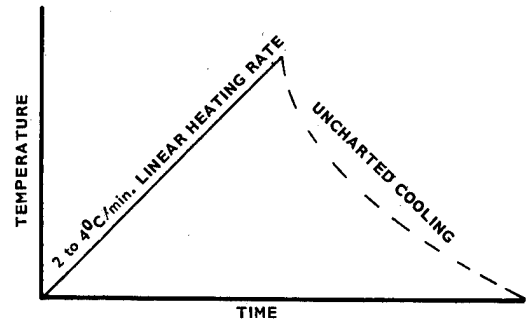


Figure 5. Thermally Stimulated Discharge

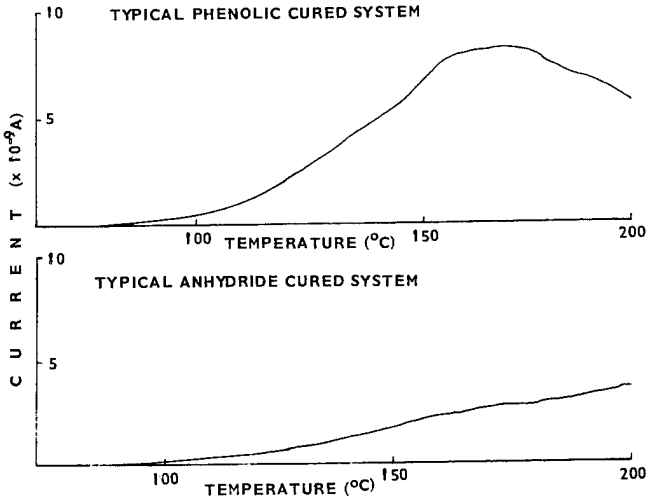


Figure 6. Comparison of Phenolic and Anhydride Cured Systems, Indicating the Generally Better Characteristics of Anhydride Cured Systems.

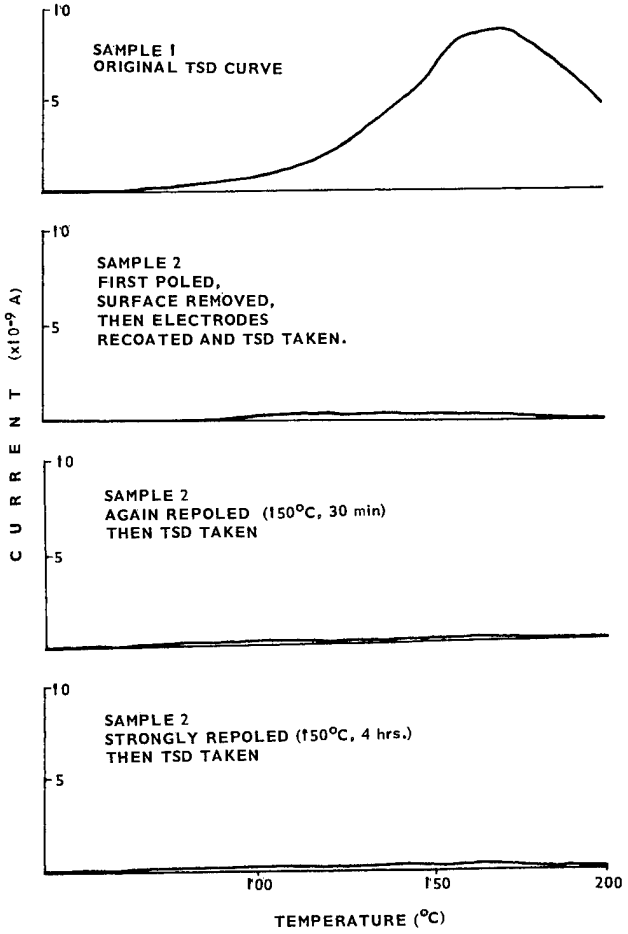


Figure 7. Effects of Surface Removal.

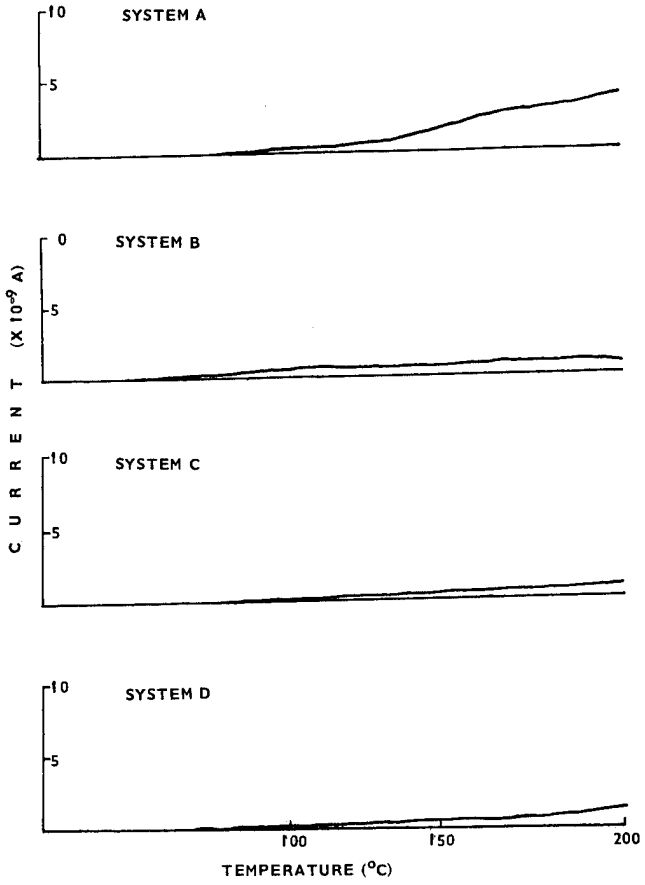


Figure 8. Comparison of Anhydride TSD's.

Table 1. Transistor Data; HTRB (150°C); 140 Hour Data

	A	B	C	D
No. of Devices	15	15	15	15
Avg. Beta (Initial)	106	112	88	88
Avg. Beta (140 Hours)	139	105	78	85
No. Failures (> 30% Shift)	12	0	1	0
Avg. Leakage Current (Initial)	21×10^{-9}	96×10^{-9}	124×10^{-9}	122×10^{-9}
Avg. Leakage Current (140 Hrs.)	193×10^{-6}	479×10^{-9}	333×10^{-9}	176×10^{-9}
No. Failures (> 10^{-6})	15	0	0	0

	Catalyst	Flameout Ingredients
System A	1	1
System B	2	1
System C	1	2
System D	1	None

Table 2. Comparison of Anhydride Systems
Exposed to HTRB (150°C, 40 V) for 140 Hours

System	Measured TSD Charge ($\times 10^{-7}$ Coul)	Initial Current	Current After 140 Hours HTRB	Change in Leakage Current
A	9.3	333 nA	124 nA	-209 nA
B	38.3	2 nA	193 uA	192 uA
C	49.0	33 nA	194 uA	193 uA
D	66.2	17 nA	1.2 mA	1.2 mA
E	100.0	128 nA	2.8 mA	2.8 mA

Table 3. Typical Leakage Current Results

System	Hardener	Measured TSD Charge ($\times 10^{-7}$ Coul)	- NPN Transistors - % Leakage Current Change After Exposure To HTRB @ 150°C, 40 V For 48 Hours
A	Anhydride	4.4	13
B	Anhydride	9.1	105
C	Phenolic	64.8	7,490
D	Phenolic	107.6	11,240

EXTENDED TEMPERATURE CYCLING OF PLASTIC AND CERAMIC I/C's WITH THERMAL SHOCK PRECONDITIONING

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SUMMARY

The purpose of this investigation was to determine if liquid-liquid thermal shock preconditioning would affect subsequent long-term temperature cycling performance of ceramic and/or plastic dual-in-line packaged devices or ceramic or metal flat packages.

Three levels of preconditioning were investigated, each followed by three levels of temperature cycling to form a 3x3 balanced matrix, analyzed by an Analysis of Variance. Fifteen cycles of preconditioning were used (as required to process Class A 38510 parts), followed by up to 3,000 cycles of temperature cycling.

This investigation showed that there was no significant thermal-shock/temperature cycling interactions, but that a wide range of life response was observed between and within package types. This experiment increases our knowledge of device behavior when subjected to extended temperature cycling and allows direct comparisons between plastic and ceramic dual-in-line packages. End of life was observed for several of the samples.

The results indicated that there was no significant interaction between the levels of preconditioning used and the subsequent extended temperature cycling used, regardless of package type or material used.

For DC electrical failures, there was no independent effect due to temperature cycling, nor independent effect due to thermal shock preconditioning for any of the package types. There was a very strong independent effect due to thermal shock with respect to both indicated and confirmed fine leak failures within the black ceramic dual-in-line packages only. The white ceramic sidebraze package passed all leak testing without a single hermeticity failure.

A strong independent vendor-to-vendor effect was observed within the indicated fine leak analysis of ceramic dual-in-line packages, between ceramic flat package vendors and between plastic device vendors when analyzed for DC electrical failures. A strong vendor vs. temperature cycle interaction was observed within the DC electrical analysis of plastic dual-in-line devices. Vendors 1 and 4, both constructed using 1.5 mil diameter gold wire, sustained significantly fewer failures than did Vendors 2 and 3, built with 1.0 mil gold ball bonds. The heavier bonding did hold up longer in extended temperature cycling of these plastic devices.

Within the dual-in-line ceramic samples, all using ultrasonic bonding with 1 mil wire, the direction of wire bonding was observed to have a pronounced effect upon failure mode. 89% of the failures occurred at the first bond made, whether to the die or to the post. The failure mechanism was wireflex. Plastic devices, all using gold wire, failed most often for grain boundary fracture, almost always located some 3 to 10 mils above the bond to the die, rather than at the heel of the bond.

By package type, 52% of the plastic packages failed, compared to 41% of the ceramic DIP and only 7% of the flat packages within the 3,000 cycle life.

This work was supported by Contract No. F30602-72-C-0251, with RADC, Rome, New York.

INTRODUCTION

This test sequence was designed to investigate what effect, if any, a 15-cycle liquid to liquid preconditioning thermal shock would have on the subsequent performance of the devices subjected to extended air to air temperature cycling. The devices would be evaluated on package integrity and circuit integrity.

All environmental test conditions are per MIL-STD-883. Parts were preconditioned with 15 cycles of Method 1011A or 1011B or 1011C, and then subjected to 3,000 temperature cycles per Method 1010B or 1010C or 1010D. The results were arranged in a balanced design matrix having three rows (Temperature Cycling Levels - Factor C), three columns (Preconditioning Thermal Shock - Factor S), and from three to five values per cell (Vendors - Factor V). See Figure 1.

Data Analysis

The three-way analysis of variance was used to analyze the interaction test results:

Factor C - Temperature Cycling (B, C, and D) are fixed levels.

Factor S - Thermal Shock (A, B, and C) are fixed levels.

Factor V - Vendors are fixed levels (but could also be considered random levels).

The mechanics of conducting a three-way Anova are adequately covered in references. This type of analysis partitions for each factor, the individual contributions to the cell values with an estimate of their relative effect; i.e., the mean square (MS) values. It then compares each factor variance against a random error variance to obtain an "F" value. Comparison of the calculated "F" value with the critical value at α confidence yields the results of the analysis. In this paper, a "statistical significance at 1%" means there is only a 1% chance that all levels of the factor in question are equal (accept the null hypothesis).

Discussion - Choice of Variable to be Used in Analysis

To simplify the data analysis and allow comparisons of effects of temperature cycling and thermal shock, a search was made for a single number or figure of merit which could be used. One was found and used in all data analysis of the interaction matrix results.

Figure of Merit

The typical failure response to long term thermal cycling consisted of an offset time period plus a failure period. See Figure 2. The offset period is the number of thermal cycles from zero to the last readout with zero failures (OA) and represents the time period of trouble-free service prior to start of failure. The failure period starts with the last zero readout and continues from there (ABCDEF). The offset period varies from none, for one vendor, to very long (for several months). In some cases, no failures were found throughout the entire test period, these samples representing the best performance. It is believed that a long offset period is the most important characteristic to have, since this represents the period of "trouble free service". It also represents the "warrantee period" response, or period when the expected failure rate is very low.

The failure period also has varying characteristics. In one case, only one failure is found followed by several readouts with zero failures (ABCD) - very low failure rate. In other cases, the failures occur all at once going from zero failures (at point A) to 100% failures on the very next readout (point B). A response in between is shown as ABCDEF. It is felt that low failure rate (low slope) is better than high failure rate.

Truncated "Z" Values (Z*)

It became evident that the test results would have to be truncated at some point; therefore, 3,000 cycles was chosen as the upper truncation point and all data was based on a maximum test time of 3,000 cycles. Numbers went from 0 (no failures through 3,000 cycles) to high number (large number of failures - high failure rate - early failures). This Z* number is proportional to the area below the curve; referenced from 3,000 cycles. (Point G would be the 3,000 cycle end point).

These Z* numbers will be used throughout the interaction matrix analyses. (Area of $\triangle$AFG.)

$Z^* = \frac{1}{2}$ (P%) (3,000 - A (cycles)/1000)
where P% = % failure @ 3,000 cycles

A = last readout cycles with zero failures

Z^* (Fig. 2) = $\frac{1}{2}$ (60)(3000-1500)/1000 = 45

Hermetic Dips (DC Electrical - Z* Values)

The 3x3x4 Anova is shown in Table 1. The matrix values are given in Table 2. Since no interactions are significant, the variation due just to temperature cycles-Factor C mean square is tested against the pooled residual mean square. This comparison is not significant; that is. there is no significant independent degradation due to Temperature Cycling alone in this experiment.

The interactions in CxV, Cycles vs. Vendors, is almost significant due to the same sample results - sample 3, 3, 3 = 125 and sample 3, 3, 4 = 159.37. These results indicate Vendors 10 and 11 both showed higher failure rates when subjected to Method 1011C Thermal Shock Preconditioning, and Method 1010D, Extended Temperature Cycling, than did any of the other vendors.

All four suppliers used 1 mil diameter aluminum wire and ultrasonic bonding. The failure modes, Table 3, were heel breaks at the bond to the die (BD - Break at Die) for Vendors 8 and 9, and predominately heel breaks at the post bond (BP - Break at Post) for Vendors 10 and 11. This difference in bonding sequence; Vendors 8 and 9 bonded die first and post last. Vendors 10 and 11 bonded post first and die last. The mechanics of bonding subjects the first bond to flexure as the bonding needle routes the wire to the final bond location. Each flexure of the bond "work hardens" it, making it more brittle and subject to failure. Consequently, subsequent expansion - contraction of the bonded wire when the devices are subjected to Temperature Cycling causes the first bond to fail first. All samples had comparable 1 mil aluminum wire with ultrasonic bonds. Vendor 11, only, had gold plated Kovar posts.

A comparsion between Vendors 10 and 11 (both bonded post to pad) would indicate additional failure rate due to the presence of gold aluminum intermetallic in the post bond only. This additional weakening of the bond shows up strongly in Temperature Cycle Method 1010D (-65°C to 200°C), Row 3, where 15 BP failures were obtained for Vendor 11 vs. 2 BP and 1 BD for Vendor 10. The abnormally high failure rates (Z* values) in samples 3, 3, 4 (Vendor 11)

were due to the very early BP failures (100, 500, 1000, 1500, and 2000 cycles) compared to most other samples which did not show failures until after 1000 cycles. Sample 3, 3, 3 (Vendor 10) also had early failures (30, 1000 cycles) for the cell, causing a high failure rate (Z*) values.

As will be shown later, Vendor 11 (sidebraze) had a perfect hermeticity record but the combination of gold-aluminum posts and post-to-pad bonding led to reduced electrical performance (opens) compared to the other in this test.

The 2, 4, 4 matrix (not shown) specifically run to compare the effect of preconditioning against no preconditioning, showed no significant differences between any main effects or interactions. Therefore, it can be concluded that 15 cycle preconditioning Thermal Shock (1011A, B, or C) does not significantly alter subsequent electrical performance to Temperature Cycling on hermetic DIP devices.

Hermetic Dip (Leak Test Results - Z* Values)

The three-way analysis of variance for leak test failures was quite different from that for electrical failures. Two situations were analyzed:

1. Indicated Fine Leak Failures (Tables 4 and 5)

2. Confirmed Fine Leak Failures (Tables 6 and 7)

In both cases there was a significant effect due to the preconditioning thermal shock.

Taking the indicated Helium Leak Anova first, the residual error term was pooled with those of C, C x S, and C x V, to obtain the new values below the line. Testing this pooled residual against the S x V interaction showed this interaction to be highly significant at 0.5%. Therefore, the value obtained for a particular vendor was dependent upon which preconditioning column it was in. Here, both Vendor 10 and Vendor 13 had higher failure rates (higher Z* values) than expected, whereas Vendor 11 (Sidebraze) had a perfect record - no indicated leakers in 3000 cycles. All other vendors had consistently higher failure rates when subjected to Preconditioning Thermal Shock 1011C than to levels 1011B or 1011A. The Z* number for 1011C is nearly 4X the number for 1011B! This high value is statistically significant at 2.5%.

A study of the Vendor averages indicates that Vendor 11 is best and Vendor 9 is next. Vendor 9 also had a very strong package on the torque test sequence. Vendor 8 and 10 have similar packages and used essentially the same sealing glass, but Vendor 10 has more helium trapping problems. Vendor 13 also has a trapping problem. It is of interest that the extended temperature cycling following the preconditioning had very little effect on the hermeticity outcome even at much higher temperature extremes than those used for the preconditioning. The temperature cycling performance does not depend upon the level of thermal shock preconditioning.

The confirmed Helium Leakers Anova simplifies the problem of confirming helium leakers further. Indicated helium leakers were left on test until they became gross leakers, verified by the red dye test. Those fine leak devices which never failed gross leak were considered unconfirmed helium leakers. The results are presented in Tables 6 and 7. Again, pooling the non-significant terms to obtain a better overall estimate of residual variance and testing for significance of differences between levels of Factor S (Preconditioning Thermal Shock) yields significant difference at 0.1% due to the preconditioning level chosen. The difference between response to Method 1011C and Method 1011B is even greater than in the previous case for indicated fine leakers. The most dramatic shift in Z* values occurs in all the lower stress levels, such as Method 1010B and 1011A. (Comparing Indicated with Confirmed Helium Leakers - Tables 5 and 7)

At lower levels of preconditioning, approximately 20% of the indicated helium leakers are confirmed whereas for Preconditioning Thermal Shock, Method 1011 C, 69% of the indicated leakers were confirmed.

The same general pattern holds for Temperature Cycling; 14.48% of 1010B, 63.4% of 1010C, and 74.9% of 1010D values were confirmed.

When comparing vendors, the results are: Table 8

Vendor	% Confirmed
8	56.17%
9	74.16% Best CDIP
10	60.48%
11	100% Sidebrazer-Solder Seal Lid
13	36.64% Large 40-Lead DIP

The percent confirmed correlates well with the absolute value of Z*; i.e., the lower the Z* (lower failure rate) the greater the percent confirmed. This is due to less helium trapping by the stronger packages and better glass-to-metal and glass-to-ceramic bonding. The only gross leakers obtained were with Vendor 10 to the highest levels - 1011C Preconditioning plus 1010D Temperature Cycling.

The major observations made for these matrix tests are:

1. Thermal shock preconditioning has a highly significant effect on helium leak performance with Method 1011C causing a significant failure rate for this failure mode. It has little effect on bond strength.

2. Extended temperature cycling has the most effect on bond failures with an

increasing failure rate with an increase in level or an increase in number of cycles. It has little effect on leak test results.

3. Vendor 10 has the best bonding but weakest package. Vendor 11 had the best leak test performance but highest bond failure rate due to putting the first bond on the post and having a gold-aluminum post bond with intermetallics causing additional weakening of bond strength.

Flat Packages

Vendors 5, 6, and 7 are flat packages with Vendor 5 being metal flat with gold ball bonds, and Vendors 6 and 7 Cerflats with aluminum-ultrasonic bonds. There were no leak test failures for the flat packages. The small flat packages have excellent hermeticity performance throughout the entire test program. The Interaction Matrix for DC Electrical is shown in Table 9 and Table 10.

Using a pooled value for the residual, there is a significant difference between Vendors at 2.5%. This difference is obviously between Vendor 6 and Vendor 7. Vendor 7 had no DC electrical failures nor any bond failures in the entire 3000 cycles. There is no significant interaction in this test. All the differences observed were due to vendor-to-vendor differences.

There is a pattern of increasing failure rate with increasing Temperature Cycling Level (Factor C) but no similar trend associated with Thermal Shock Preconditioning.

The flat packages showed the best overall performances, as a group, to the interaction matrix testing. This package style is clearly the best "Hi-Rel" package for all the environments studied in this program.

Plastic Packages

Plastic package performance to the interaction matrix was varied. Some Vendors did very well; others did poorly.

Tables 11 and 12 cover the plastic results. Pooling the residual with those factors underlined gave the error mean square below the line. Testing the C x V interaction against this term showed C x V to be significant at 0.1%. Therefore, the value obtained for temperature cycling depended very strongly upon which Vendor was under consideration.

Since the C x V interaction is significant, the Factor C (Temp Cycle Levels Effect) and V (Between Vendors Effect) had to be tested against the interaction mean square, not the pooled residual. This testing established a significant difference between Vendors while the Temp Cycle Levels Effect became non-significant (NS). The most surprising performance was Vendor 4 Phenolic with a perfect record - no DC electrical or intermittent failures even through 3000 Temperature Cycles of Condition D (-65°C/+200°C). The reason is thought to be: the Phenolic package had a glass transition point above 200°C whereas the other three epoxy packages had glass transition points less than 150°C. This Vendor also used 1.5 mil gold thermal compression wire bonding. Vendors 1 and 3 used the same plastic, epoxy "B", but had different wire bonding systems. Vendor 1 uses 1.5 mil diameter gold thermal compression wire bonding; Vendor 3 used 1.0 mil gold ball bonding.

The poorest performance was given by Vendor 2 who had a plastic with the lowest glass transition point and 1.0 mil gold ball gonding.

The results show clearly (see C x V matrix). Through Temperature Cycling Condition C (-65°C/+150°C) 1.5 mil gold T/C bonding showed excellent performance compared to 1.0 mil gold ball bonding. Test Condition D is too much for all except Vendor 4. (Note: Vendor 4 does not make phenolic packaged I/C's at this time. The samples used throughout these tests were engineering run samples.)

The failure modes for the plastic devices were intermittents first and verified DC electrical second. It sometimes took quite some time for a repeating intermittent to become a hard failure. When the failure was analyzed, the most common failure mode was grain boundary fracture (GBF) in the gold wire some 2 to 10 mils above the bond to the die, (LD), at the lowest intermetallic interface between the gold wire and the aluminum pad metal. This failure mode is due to Kirkendall Voiding in the Au_5Al_2 region following fatigue cracking in the bond due to the thermal cycling.

There was no independent effect due specifically to the preconditioning thermal shock.

Failure Modes by Vendor and Readout

Table 13 shows which vendors had which failure modes throughout the entire test program.

In general, the higher the temperature cycling stress, the more bond failures were noted. The higher the thermal shock stress, the more indicated fine leak failures were noted. The first five categories contain 89% of the failures obtained. These were all related to wire bonds or fine leak failures. The remaining 11% of the failures were for a variety of failure modes - mostly die related. The test program did pick up a total of 8 oxide defects and pinholes under the metal failures which is 2.9% of the failure or 1.0% of the devices (8/792).

The test plan was hardest on plastic where 53% of the plastic population sustained failures but of these 53%, 85% were associated with Vendors 2 and 3, using 1 mil ball bonds. Hermetic flat packages were clearly the best overall performers with only

7% of the flat package population sustaining failures and the failure modes obtained were more random in nature. The hermetic dual-in-lines sustained failures in 37% of its population with 58.9% of these due to wire bond failures and 33.6% due to fine leak failures.

Table 14 presents the same data by failure mode vs number of temperature cycles. Attempts have been made to determine an acceleration factor for temperature cycling levels vs failure mode but due to the limited sample size in each cell (n = 8 per Vendor), the relationship obtained was just too crude to document. In general, the higher the stress condition, the sooner failures are obtained. The main conclusion here is that the overall test plan caused plastic (mostly 1 mil ball bond) to fail early - 30 to 2K cycles while hermetic wire bond failures were not detected until much later, 500 to 3K cycles. Indicated helium leak, all CDIP only, were very widely scattered with a relatively large number detected after first readout and additional failures detected all the way to 3K cycles.

The majority of the other failures detected occurred pretty much at random. Thermal cycling did pick up some oxide defect and pinhole failures but only after extensive cycling. Either the product was free of these failure modes or the temperature cycling is not very effective in accelerating these failure modes.

Overall Conclusions:

The overall conclusions from analysis of the interaction results are these:

1. Thermal shock preconditioning generated fine leak failures.

2. Extended temperature cycling was more effective in causing wire bond failures - much less effective in causing leak test failures.

3. There was no interaction between the preconditioning thermal shock (15 cycles) and the subsequent extended temperature cycling performance. The temp cycle performance did not care what 15-cycle preconditioning (if any) was used.

4. The largest difference, considering all package styles and failure modes, was Vendor-to-Vendor differences. This testing shows the importance of evaluating each Vendor on his own merits and being careful of generalization across Vendors making common package styles.

5. Flat packages showed the best overall performance and the lowest overall average Z* value. This fact was true considering both package integrity and wire bond integrity.

6. Plastic packages can perform as well as hermetic in thermal cycling applications, but were highly Vendor dependent at these stress levels.

7. Hermetic dual-in-line (CDIP construction) may be convenient to use but showed greater failure rates and far greater variation from cell to cell than did the flat packages. They are particularly susceptible to package failure due to their design, i.e., uneven masses of ceramic between top and bottom, heavy lead frame reducing amount of bonding glass around the frame, large torque forces exerted by the lead frame on the lid when the leads are compressed during insertion into the board.

8. Dual-in-line sidebraze showed excellent package integrity but weaker interior post bonding reliability, due to the use of a gold/aluminum structure combined with post to pad bonding.

9. For the same temperature cycling stress levels, plastic devices failed much earlier than did hermetic devices for bond related failure modes.

Acknowledgment

I would like to acknowledge Mr. Marv Carpenter for his extensive efforts in carrying out this test program.

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INTERACTION MATRIX TEST PLAN

N = 8 (EACH VENDOR)

4 (CERDIP), 3 (FLATS), 4 (PLASTIC DIPS)

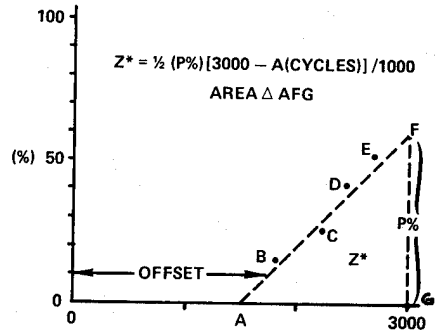
TEMPERATURE CYCLING	PRECONDITIONING THERMAL SHOCK		
RO: 30, 60, 100, 500, 1000, 1500, 2000, 2500, 3000	1011A 15c 0/+100°C	1011B 15c −55/+125°C	1011C 15c −65/+150°C
1010B −55/+125°C	J	M	Q
1010C −65/+125°C	K	N	R
1010D −65/+200°C	L	P	S

CONTROL SAMPLES: TEST GROUPS C, D, AND E. (NOT SHOWN)

D7085

FIGURE 1

THERMAL CYCLES ACCUMULATIVE % FAIL vs THERMAL CYCLES



D7086

FIGURE 2

ANOVA TABLE: CDIPS — DC ELEC.

(Z* VALUES)

SOURCE OF VARIATION		DF	MEAN SQUARE	F	SIG
TEMP CYCLE LEVELS	−C	2	3049.26	2.78	–
PRECON THER-SHOCK	−S	2	534.63	–	–
VENDORS	−V	3	631.71	–	–
CYCLES vs SHOCK	−CxS	4	1664.94	2.63	–
CYCLES vs VENDORS	−CxV	6	2016.57	2.26	–
SHOCK vs VENDORS	−SxV	6	1154.48	1.83	–
RESIDUAL ERROR		12	631.86		
TOTAL		35			
POOLED RE		33	1097.96		

D7087

TABLE 1

ANOVA: CDIPS — DC ELEC.

(Z* VALUES)

		V8	V9	V10	V11	$\bar{S}$	$\bar{C}$
CB	SA	31	25	0	3	15	12 ←
	SB	37	6	0	0	11	
	SC	31	6	0	0	9	
CC	SA	19	91	3	19	33	22 ←
	SB	25	9	19	37	23	
	SC	9	12	6	12	10	
CD	SA	31	31	0	62	31	43 ←
	SB	12	9	19	47	22	
	SC	6	12	(125)	(159)	76	
	$\bar{V}$ =	23	23	19	38		26

SA = 26 | SB = 18 | SC = 32

D7088

TABLE 2

FAILURE MODE vs BONDING DIRECTION

	UPBOND (V8, V9) N = 144		DOWNBOND (V10, V11) N = 144	
FAILURE MODE	#	%	#	%
BREAK – BOND TO DIE (BD)	32	94	2	6
BREAK – BOND TO POST (BP)	1	3	28	85
OTHER	1	3	3	9

D7089

TABLE 3

ANOVA TABLE: CDIPS — INDICATED HELIUM

(Z* VALUES)

SOURCE OF VARIATION		DF	MEAN SQUARE	F	SIG
TEMP CYCLE LEVELS	−C	2	78.75	–	
PRECON THER-SHOCK	−S	2	5784.98	(4.43)	2.5%
VENDORS	−V	4	2326.86	(1.78)	
CYCLES vs SHOCK	−CxS	4	110.94	–	
CYCLES vs VENDORS	−CxV	8	446.62	–	
SHOCK vs VENDORS	−SxV	8	1304.62	3.49	0.5%
RESIDUAL ERROR		16	440.39		
TOTAL		44			
POOLED RE		30	374.10		

D7090

TABLE 4

ANOVA: CDIPS — INDICATED FINE LEAK

(Z* VALUES)

		V8	V9	V10	V11	V13		
CB	SA	0	0	0	0	30	6	19
	SB	19	12	16	0	0	9	
	SC	36	6	94	0	80	(43)	
CC	SA	0	0	0	0	30	6	24
	SB	74	0	0	0	5	16	
	SC	75	12	74	0	89	(50)	
CD	SA	19	9	0	0	45	15	23
	SB	6	0	28	0	30	13	
	SC	19	56	112	0	15	(41)	
		(28)	11	(36)	0	(36)		22

SA = 9	SB = (13)	SC = (45)

D7091

TABLE 5

ANOVA TABLE: CDIPS — CONFIRMED HELIUM

(Z* VALUES)

SOURCE OF VARIATION		DF	MEAN SQUARE	F	SIG
TEMP CYCLE LEVELS	–C	2	895.56	2.01	
PRECON THER-SHOCK	–S	2	4179.85	8.49	0.1%
VENDORS	–V	4	605.70	1.36	
CYCLES vs SHOCK	–CxS	4	547.97	1.23	
CYCLES vs VENDORS	–CxV	8	394.02	–	
SHOCK vs VENDORS	–SxV	8	500.43	1.12	
RESIDUAL ERROR		16	445.36		
TOTAL		44			
POOLED RE		42	492.55		

D7092

TABLE 6

ANOVA: CDIPS — CONFIRMED FINE LEAK

(Z* VALUES)

		V8	V9	V10	V11	V13		
CB	SA	0	0	0	0	0	0	3
	SB	0	0	0	0	0	0	
	SC	36	6	0	0	0	8	
CC	SA	0	0	0	0	0	0	15
	SB	9	0	0	0	0	0	
	SC	56	0	74	0	89	(44)	
CD	SA	19	9	0	0	0	6	17
	SB	0	0	9	0	15	5	
	SC	19	56	112	0	15	(40)	
		(15)	8	(22)	0	(13)		12

SA = 2	SB = (2)	SC = (31)

D7093

TABLE 7

% CONFIRMED FINE LEAK vs VENDOR

VENDOR	% CONFIRMED	COMMENT
8	56	
9	74	BEST CDIP
10	60	
11	100	S/B – SOLDER SEAL
13	37	LARGE 40 LEAD DIP.

D7094

TABLE 8

ANOVA TABLE: FLAT PACKS — DC ELEC.

(Z* VALUES)

SOURCE OF VARIATION		DF	MEAN SQUARE	F	SIG
TEMP CYCLE LEVELS	–C	2	279.11	1.67	
PRECON THER-SHOCK	–S	2	51.33	–	
VENDORS	–V	2	621.67	4.95	2.5%
CYCLES vs SHOCK	–CxS	4	144.50	–	
CYCLES vs VENDORS	–CxV	4	97.01	–	
SHOCK vs VENDORS	–SxV	4	13.69	–	
RESIDUAL ERROR		8	166.64		
TOTAL		26			
POOLED RE		24	125.62		

D7095

TABLE 9

ANOVA: FLAT PACKS — DC ELEC.

(Z* VALUES)

		V5	V6	V7		
CB	SA	0	19	0	6	2
	SB	0	0	0	0	
	SC	0	0	0	0	
CC	SA	0	25	0	8	5
	SB	0	9	0	3	
	SC	9	6	0	5	
CD	SA	12	0	0	4	13
	SB	3	31	0	11	
	SC	16	54	0	23	
		4	16	0		7

SA = 6	SB = 5	SC = 9

D7096

TABLE 10

ANOVA TABLE: PLASTIC — DC ELEC.

(Z* VALUES)

SOURCE OF VARIATION		DF	MEAN SQUARE	F	SIG
TEMP CYCLE LEVELS	–C	2	30930.08	(2.15)	NS
PRECON THER-SHOCK	–S	2	204.53	–	
VENDORS	–V	3	158546.99	(11.04)	1%
CYCLES vs SHOCK	–CxS	4	67.00	–	
CYCLES vs VENDORS	–CxV	6	14364.22	71.46	0.1%
SHOCK vs VENDORS	–SxV	6	199.15	–	
RESIDUAL ERROR		12	246.00		
TOTAL		35			
POOLED RE		24	201.00		

D7097

TABLE 11

ANOVA: PLASTIC — DC ELEC.

(Z* VALUES)

		V1	V2	V3	V4		
CB	SA	0	247	219	0	116	115
	SB	0	250	225	0	119	
	SC	0	275	166	0	110	
CC	SA	0	273	234	0	127	134
	SB	0	285	280	0	141	
	SC	0	275	267	0	136	
CD	SA	270	295	273	0	210	211
	SB	267	294	298	0	215	
	SC	239	297	298	0	209	
		86	277	251	0		154

SA = 151	SB = 158	SC = 151

D7098

TABLE 12

FAILURE MODE BY VENDOR

	PLASTIC				FLAT			CPIP				
FM	1	2	3	4	5	6	7	8	9	10	11	
GBF	21	55	55									131
BD	1					3		18	14	1	1	38
BP		1							1	4	24*	30
I-He L								14	7	15		36
LD		10			1							11
CORR		1	4							4		9
OX DEF						4			1			5
PIN H			1		1	1						3
GL										3		3
Au AL					2						*	2
SUB S						2						2
OPEN M		1	1									2
CHIP						1						1
CRACK		1										1
US DAM						1						1
TOTAL	22	69	61	0	4	12	0	32	23	27	25	275
	53%				7%			37%				

D7099

TABLE 13

FAILURE MODE BY READOUT

	# TEMPERATURE CYCLES											
FM	30	60	100	500	1K	1.5K	2K	2.5K	3K	T	% of	N
GBF	25	8	8	52	36	1	1			131	45.5	288
BD				2	5	9	3	7	12	38	4.8	792
BP			1	2	1	4	5	7	10	30	3.8	792
I-He L	15	4	1	1	1	3	4	3	4	36	7.1	504
LD	5		4	1					1	11	1.4	792
CORR	2		1		4		2			9	1.1	792
OX DEF				1			3		1	5	0.6	792
PIN H					2		1			3	0.4	792
GL	3									3	0.6	504
Au AL			1			1				2	0.5	432
SUB S					1		1			2	0.3	792
OPEN M			2							2	0.3	792
CHIP					1					1	0.1	792
CRACK				1						1	0.1	792
US DAM					1					1	0.2	432
TOTAL	50	12	18	60	52	18	20	17	28	275		

D7100

TABLE 14

BASIC INTEGRATED CIRCUIT FAILURE ANALYSIS TECHNIQUES

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ABSTRACT

This tutorial is a review of several basic analytical techniques used to perform failure analysis on integrated circuits. Included are methods for failure verification, package opening, and electrical die probing. "Secrets" for obtaining ac measurements above 1MHz are discussed along with techniques of microsurgery for isolation of integrated components. A detailed presentation of the metallurgical technique of angle lapping is included along with an error correction scheme to aid in precise junction depth measurements. Chemical formulas for staining silicon and selectively removing silicon oxides and metallization are revealed.

INTRODUCTION

Integrated circuit failure analysis is a constant challenge due to continual changes in device design, manufacturing processes, and circuit complexity. To meet this challenge, a working knowledge of the fundamental techniques is required. From the fundamentals, new techniques can be developed to meet specific needs as they arise.

Successful analysis techniques should be easily reproducible with a minimal amount of effort. They should not alter the circuit performance or mask the actual failure mode. They should help the analyst uncover the origin of failure without destroying any evidence in the process.

A successful analysis depends on a successful analyst. The analyst must be proficient in electronics, semiconductor technology, component testing, materials, and reliability physics. However, the real key to producing an accurate failure analysis is a well devised plan of attack coupled with the use of a few basic analytical techniques.

FAILURE VERIFICATION

The first step in every analysis is verification of the failure. Overlooking this step usually results in disaster. A detailed review of the circumstances surrounding the failure, the chip construction technology, and electrical design is time well spent.

Performing a few simple curve tracer tests usually uncovers a good percentage of the failures associated with the device inputs and outputs. A minimum test involves checking continuity and voltage breakdowns of all inputs and outputs with respect to the substrate and power supply pins. If the measured characteristics are not as expected after studying the circuit design and device parasitics, a comparison with a "good" unit will confirm a failure.

A bench test is constructed to duplicate the failure exactly as it appears in the system. The test is then simplified to isolate the single or small group of parameters which cause the failure. This not only aids in pinpointing the failure mode, but allows for a workable layout during electrical die probing. Additional electrical tests narrow the failure to a small functional block on the die.

At this point in the analysis, a procedural flow chart is formulated to guarantee that all suspected locations are investigated during the microscopic analysis which follows. This flow chart is revised as additional information is gathered.

TECHNIQUES FOR PACKAGE OPENING

Integrated circuits are supplied in hundreds of package types, each requiring a special opening technique. In general, a package should be opened in a manner to inflict the least amount of damage to the internal components. A most frustrating experience is opening a package to discover the die cracked, bonding wires broken, or the failure symptoms "cured".

Metal lid packages are the easiest to open. The recommended technique involves "sawing" into the edge of the seal at a corner with a razor blade tool. Once a cut is made, the lid is pried off as shown in Figure 1. An alternate technique for solder sealed metal packages uses a "hot cap desealer" made from a large soldering iron equipped with a vacuum head (see Figure 2). The device is momentarily placed on the hot iron ($510^{o}C$) and the vacuum pulls the lid off. If the circuit can withstand this thermal shock, the "hot cap de-sealer" is the fastest method. Welded metal packages require thinning the lid by sanding or cutting the edges by grinding. When sanding or grinding, it is imperative that the package only be thinned. The lid can then be pried off without introducing unwanted particles into the package cavity.

Ceramic dual-in-line packages are opened using an end cutting pliers whose face has been ground flat. The glass seal is placed in the jaws of the pliers. The seal is broken by the application of force on the handles or with a light blow from a hammer as shown in Figure 3.

Ceramic flat packs are opened by applying a light compressive stress to the lid. The package is placed in a vise with the lid facing downward. The lid is given a light "tap" with the edge of a file (Figure 4).

Round metal cans are opened with a miniature pipe cutter as shown in Figure 5. A low speed diamond cutting wheel or mill works equally well if the cut is stopped before entering the package cavity. The lid is then pried off.

Plastic packages are the most difficult to open due to the fact that strong bases and acids are required to chemically dissolve the material. Silicones dissolve readily in tetramethylguanidine at $80^{o}C$ in about 20 minutes or after several hours using "Uresolve Plus" at $100^{o}C$. Epoxy packages require the use of concentrated acids that have been boiled for 1 to 2 hours to remove any moisture which would attack the aluminum metallization on the die. A technique for removing epoxy is given below. Similar techniques have been previously reported in the literature.[1,2]

REMOVAL OF EPOXY MATERIAL

1. Mill or grind a slot in the package above the wire bonds and die. Remove enough material to expose the bonding wires.

2. Solder the leads together using a heavy buss wire or encase the leads and base in a castable ceramic.

This is done to provide mechanical support after etching.

3. Vacuum bake the package for several hours at 100°C to remove any moisture.

4. Boil concentrated nitric acid or concentrated sulfuric acid for several hours to remove any moisture.

5. Immerse the dry package in the boiling acid. Sulfuric acid takes 15-30 seconds. Nitric acid requires from 1 to 15 minutes.

6. Immerse in room temperature acid for several seconds.

7. Wash in methyl alcohol for several minutes.

8. Examine the die and immediately etch again (step 5) if required. Care must be taken not to induce any moisture on the package during handling.

9. When sufficient material has been removed, wash the package for 5 minutes in deionized water followed by a final methyl alcohol rinse.

For this technique to be successful, it is important to use methyl alcohol as the intermediate rinse. Water is only used when the etching is complete. If an elastomer is used to cover the die and bonding wires, hot "Uresolve Plus" usually removes the coating.

ELECTRICAL DIE PROBING

In many cases, probing is required to locate a failed component on the die. To accomplish this, electrical contact is made to the die metallization using a very sharp "needle-like" tungsten probe attached to a precision micromanipulator. The tool is geared to provide a large reduction in movement of the operator's hand. Figure 6 shows several micromanipulators stationed around an optical microscope. The microscope is capable of magnifications up to 500 times with a working distance of about 7mm.

Most integrated circuits are manufactured with a hard glassivation layer over the die surface. The probe needle must penetrate this glassivation before electrical contact is made. Often, several repeated attempts are needed to break through the glassivation under the probe tip. At other times, etching the glassivation is the only solution.

Once contact has been made to the metallization, voltages on internal nodes can be measured. Care must be taken to avoid bumping the probe station or its table while the probes are making contact to the circuit. The smallest movement may cause damage to the soft die metallization. It is important to shield the die from the microscope illumination as the induced photocurrents can alter the circuit performance.

If probing is to be done at frequencies below 1MHz, most interconnections are considered electrically short and unshielded wire can be used. At higher frequencies, special precautions must be taken to control the signal transimssion characteristics with respect to reflections and crosstalk.[3] Conductor lengths must be reduced to less than 10cm whenever possible. An isolated "single point" grounding system is recommended along with special low capacitance coaxial cables. All signal generators should be terminated at the device under test. Short micromanipulator tips (isolated with a non-conducting sleeve) significantly reduce line lengths. A small interconnection superstructure attached directly to the probe tips accomplishes signal distribution and output loading with minimum distortion.

To illustrate the fact that a probe station can reproduce fast ac signals, the input pin of the TTL gate of Figure 7 was driven with the upper waveform in Figure 8. The driving signal, as measured through the micromanipulator with a FET probe, reproduces the original waveform with very little distortion.

MICROSURGERY

Advances in LSI technology make component probing particularly difficult at times. Metallization line widths are approaching 2μm and the use of multi-level interconnect systems is increasing. Because of this, care must be taken while isolating components to avoid any damage to the surrounding circuitry.

The most common technique for cutting metallization is to scratch it open with a sharp probe. However, this usually leaves a thin film of metal residue in the area of the scratch. To remove this unwanted film, it is necessary to either fuse it open with a controlled voltage overstress or chemically etch it away. A curve tracer is adequate for applying a low voltage overstress (usually less than 3 volts) across the opening to be fused. A careful circuit analysis must be made to guarantee that the fusing voltage does not damage the circuit after the metal opens. If aluminum metallization is used, freshly scratched metal can be removed with a 3 to 5 second etch in the same buffered HF solution used to etch silicon dioxide (25 ml of HF, 56 g ammonium fluoride, and 75 ml of water). The solution only attacks freshly scratched metallization. An alternate procedure[4] uses a weak solution of sodium hydroxide, however, this slowly attacks all exposed aluminum.

Ultrasonic cutting is the most accurate and reproducible technique for separating metallization proposed to date[5]. All that is required is a sharp probe attached to a standard ultrasonic horn. To illustrate this fact, the horn from an ultrasonic wire bonding machine was fit with a tungsten probe. Figure 9 shows an aluminum metallization run separated with this technique. An amazing fact is that ultrasonic power can be used to cut metal stripes buried under several layers of glassivation, as in the case of a two-level metal device. Figure 10 shows a cut made on a polysilicon interconnection buried under 2μm of glassivation. Using conventional cutting techniques, a polysilicon run is almost impossible to open.

A metal interconnection is often opened by mistake. The damage can easily be repaired using an ultrasonic wire bonded "micro-bridge" as shown in Figure 11. To construct a "micro-bridge", a sharp probe is used to puncture a hole in the die glassivation over the area to be bonded. The die is placed in an ultrasonic cleaner for a few seconds to remove any loose glass particles from the hole. Then, a flat ribbon wire is bonded to the glassivation over the hole. The bonding action drives a spear of aluminum down through the hole. It is important that ribbon wire be used as a round wire may not form a bond with the glassivation. Figure 12 shows a typical ribbon wire bond to a 6.4μm metal stripe. This technique has also proven useful for bringing an internal node to an external package pin for measurement or excitation.

PROBE FABRICATION

Needle sharp probes can be made from tungsten wire in a matter of minutes. The procedure involves constructing an electrochemical cell using a sodium hydroxide electrolyte. Figure 13 illustrates this simple cell. Current flows from the tungsten probe to the copper cathode causing dissolution of the tungsten metal. To create a pointed tip, the probe is repeatedly immersed and removed from the solution at a one second rate. This method is ideal for sharpening broken tips.

If many probes are to be made, etching becomes a very time consuming process. Excellent results have been obtained using an acetylene torch to oxidize the tips. The technique involves cutting tungsten wire stock into pieces about 1 cm longer than the desired probe length. The wire is oxidized by waving it back and forth in the flame. When the wire is thinned to a sharp point, as illustrated in Figure 14, the pressure of the escaping gas blows the residual end away.

ANGLE LAPPING

Angle lapping is a necessary technique for construction evaluation and failure analysis. Accurate diffusion depth and oxide thickness measurements can be taken due to the fact that the die is sectioned at a shallow angle. Hidden diffusion faults can also be discovered since cross-sectioning reveals another dimension, depth, to the analyst.

To prepare a device for angle lapping, a small drop of clear epoxy is placed on the die. The epoxy protects the die from the harsh environment which follows. Excess package material is ground away before the device is mounted on the angle block with wax. It is necessary to mount the die parallel to the face of the angle block if accurate depth measurements are to be calculated. Figure 15 shows a lapping block and its holders.

After mounting, the die is lapped using 3/0 emery paper until the leading edge of the beveled section is near the area to be checked. The final lapping is performed with polishing alumina on a glass plate as shown in Figure 16. A drop of liquid detergent added to the alumina helps to lubricate the slurry.

The N-type diffusions are identified using an electroless copper sulfate solution. A drop of the solution (6% copper sulfate, 2% hydrofluoric acid (48%)) is placed on the die and illuminated with a high intensity light. When the solution dries, N-type regions will have been plated with copper. The copper decoration can be removed with a small amount of additional polishing.

Semiconductor junctions are defined by a one second etch in a silicon stain (5 parts nitric acid, 3 parts hydrofluoric acid (48%), 3 parts acetic acid). Figure 17 shows a die after staining.

There are two basic methods for finding the actual depth of stained junctions. A dual-beam interferometer is ideal for measuring lapped surfaces and thin films. However, junction depths can be calculated using a standard optical microscope and the following procedure. Each measured distance must be multiplied by the sine of the lapping angle used. The accuracy of these measurements is dependent upon the die being mounted parallel to the lapping block. Figure 18 illustrates the general case where the die is incorrectly mounted in its package. To compensate for this inaccuracy, an alternate technique is used. The package must be turned 180^{o} and beveled far enough to get a comparison of at least one measurement.

The two measurements, m_1 and m_2, depend on the angles a and b, and on the junction depth x

$$m_1 = x \csc (a + b)$$

$$m_2 = x \csc (a - b)$$

Eliminating the error angle, b, from these equations gives the exact junction depth as

$$x = \frac{2 m_1 m_2 \cos a \sin a}{\sqrt{(m_2 - m_1)^2 \sin^2 a + (m_1 + m_2)^2 \cos^2 a}} \quad (1.1)$$

Since the angles a and b are usually small, a useful approximation is found by expanding the trigonometric functions and retaining only terms of lowest order in a, yielding[6]

$$x \cong \tfrac{1}{2} r (m_1 + m_2) \sin a \quad (1.2)$$

$$\text{where } r = 1 - \left[\frac{m_1 - m_2}{m_1 + m_2}\right]^2$$

Equation 1.2 introduces less than 1 percent error for lapping angles below 14 degrees. Because all depths cannot be compared by lapping from both sides of the die, these measurements are corrected by multiplying by the ratio, x/m.

Angle lapping is ideal for pinpointing hidden diffusion faults. Figure 19 shows what appears to be an N+ emitter diffusion defect over a diffused P-type resistor. This fault was uncovered after removal of the die metallization. Lapping and staining verified the fact that the observed defect was "pinching" the resistor. This is shown in Figure 20.

ETCHING SEMICONDUCTOR MATERIALS

As seen in the previous example, selective removal of materials is often required to locate the cause of failure. This may involve etching the glassivation, die metallization, and thermal oxides to expose a defect.

Table 1 is a listing of common chemical etchants used for integrated circuit failure analysis. References 2, 4, 7, and 8 contain others. Removal times and temperatures will vary with each vendor and technology. It is a good idea to experiment with several etching techniques before determining the one best suited to a particular application. With the help of a scanning electron microscope, etchants can be chosen which do the least amount of damage to the remaining layers.

As always, care must be taken when using strong chemicals to avoid personal injury. Protective clothing should be worn at all times and etchants should only be used in areas with adequate ventilation.

SUMMARY

Several basic techniques were presented to provide a foundation for integrated circuit failure analysis. Included were methods of package opening, electrical probing, microsurgery, angle lapping, and selective etching. The laboratory procedures described have proven useful in daily analysis of failures from a wide cross-section of semiconductor technologies.

ACKNOWLEDGEMENT

The author is indebted to the staff of the Semiconductor Failure Analysis Laboratory at the Naval Weapons Support Center for their technical contributions.

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TABLE 1

COMMON ECHANTS USED FOR FAILURE ANALYSIS OF INTEGRATED CIRCUITS

Material	Etchant	Comments
Aluminum (1)	Phosphoric Acid	Rapid, 50°C
(2)	1g Potassium Hydroxide 100ml Water	Slow
Gold	1 part Hydrochloric Acid 3 parts Nitric Acid	
Nichrome	6g Ceric Sulfate 10ml Nitric Acid 90ml Deionized Water	55°C
Platinum	1 part Hydrochloric Acid 3 parts Nitric Acid	
Silicon (1)	4 parts Hydrofluoric Acid 4 parts Nitric Acid 2 parts Water	
(2)	3 parts Hydrofluoric Acid 5 parts Nitric Acid 3 parts Acetic Acid	
Silicon Monoxide	40% Ammonium Fluoride (aqueous) 2% Sodium Hydroxide (aqueous)	Mix to give pH of 9 50°C
Silicon Dioxide	25ml Hydrofluoric Acid 56g Ammonium Fluoride 75ml Water	
Silicon Nitride	Phosphoric Acid	Use condenser 180°C
Titanium	Sulfuric Acid	80°C

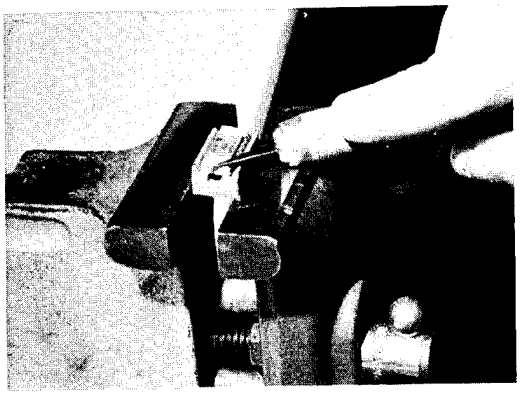

FIGURE 1. Opening metal lid dual-in-line packages with a razor blade tool.

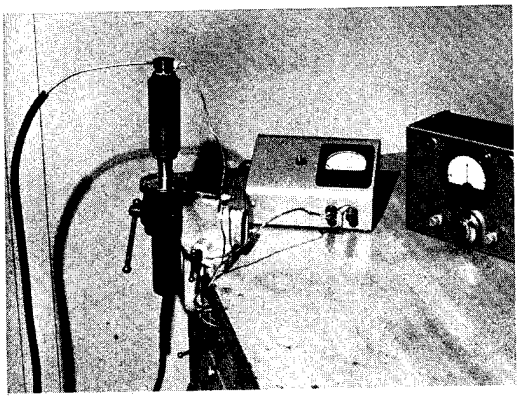

FIGURE 2. "Hot cap de-sealer" made with a large soldering iron.

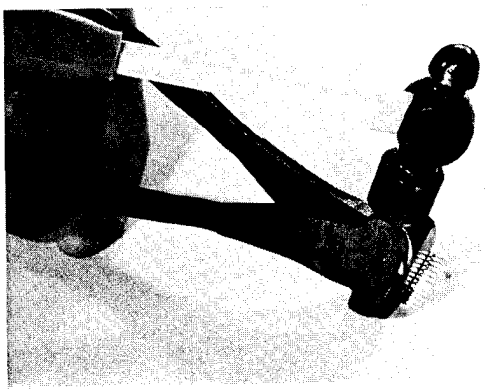

FIGURE 3. Opening ceramic dual-in-line packages with an end cutting pliers.

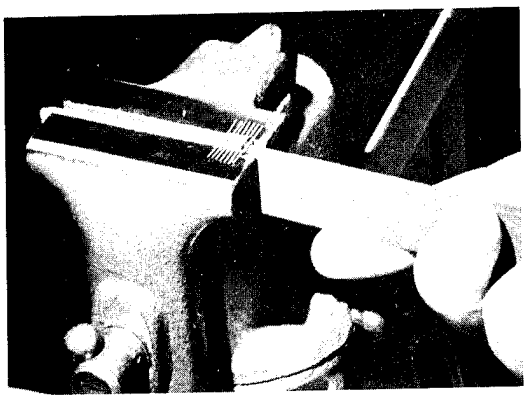

FIGURE 4. Technique for opening ceramic flat packs.

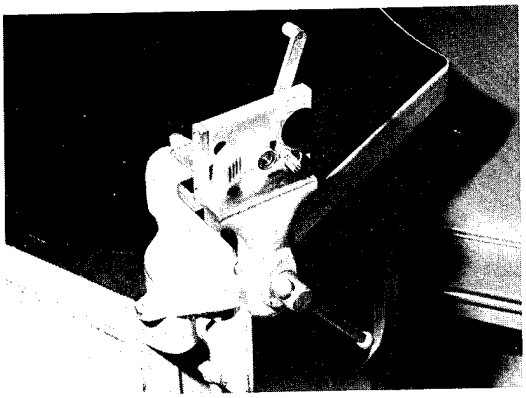

FIGURE 5. Miniature pipe cutter used for opening round metal cans.

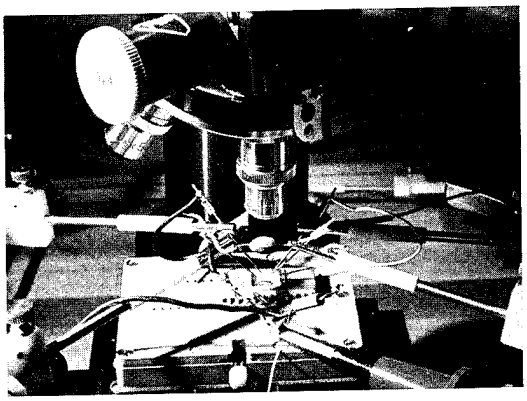

FIGURE 6. Micromanipulator probe station.

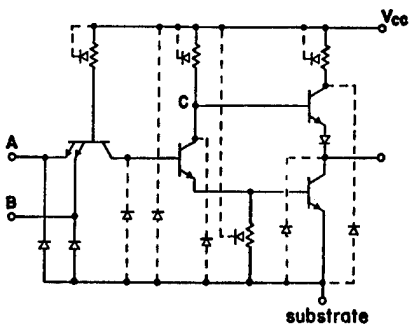

FIGURE 7. Schematic diagram of a TTL NAND gate. Several of the diode parasitics are outlined.

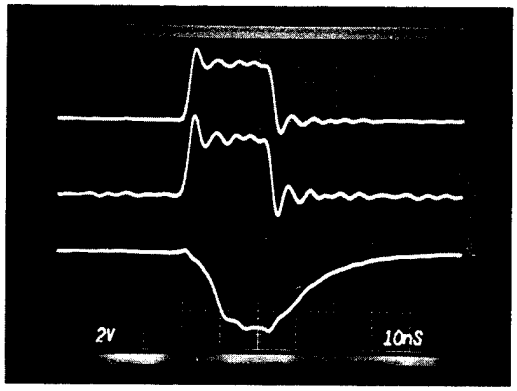

FIGURE 8. Waveforms measured on the circuit of Figure 7. (TOP) Injected signal at input A. (CENTER) Input A measured through the micromanipulator probe. (BOTTOM) Waveform at point C.

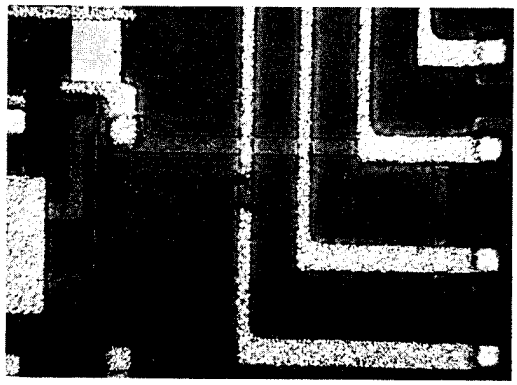

FIGURE 9. An ultrasonically cut aluminum metal run (6.4 μm width).

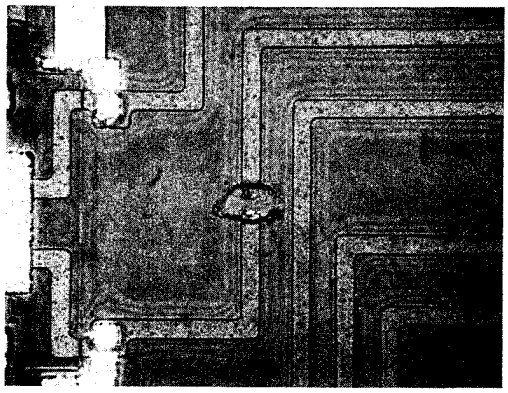

FIGURE 10. A polysilicon interconnection (12.7 μm width) cut with an ultrasonic probe.

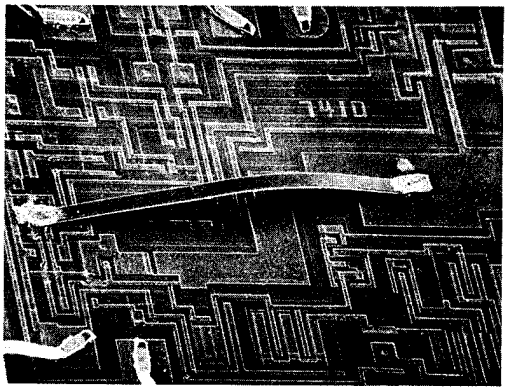

FIGURE 11. Circuit repair using an ultrasonically bonded ribbon wire "micro-bridge".

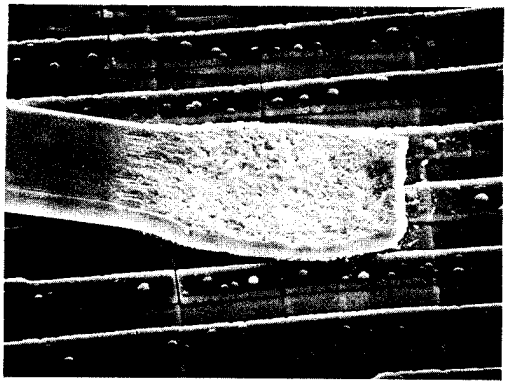

FIGURE 12. Ultrasonic ribbon wire bond to a glassivated metal stripe.

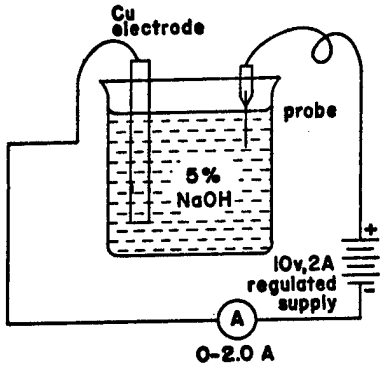

FIGURE 13. Electrochemical cell used for probe fabrication.

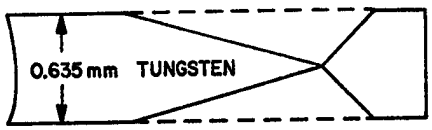

FIGURE 14. Tungsten wire "oxidized" to a sharp point.

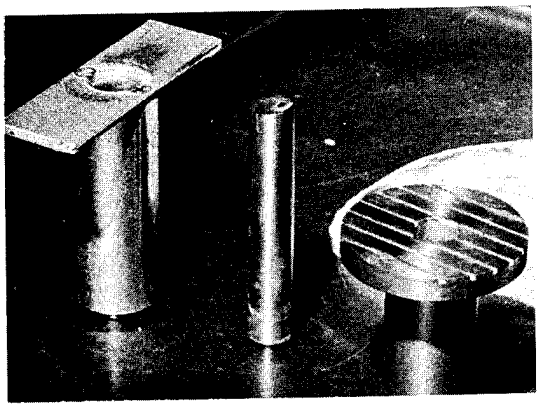

FIGURE 15. Angle lapping tools. Pictured from the left are, the angle block microscope holder, the angle block, the lapping holder for the angle block.

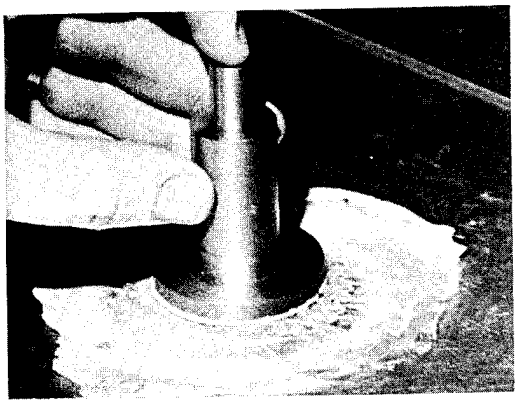

FIGURE 16. Final lapping using 0.3 μm polishing alumina on a glass plate.

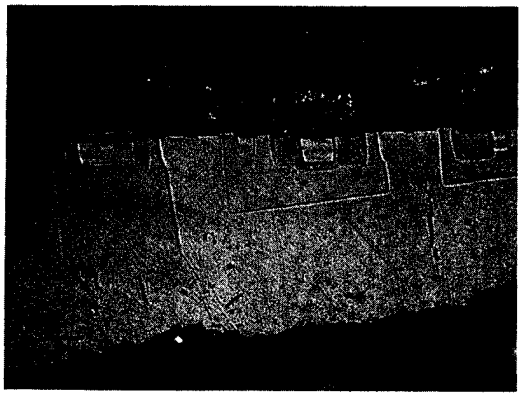

FIGURE 17. An angle lapped die after staining.

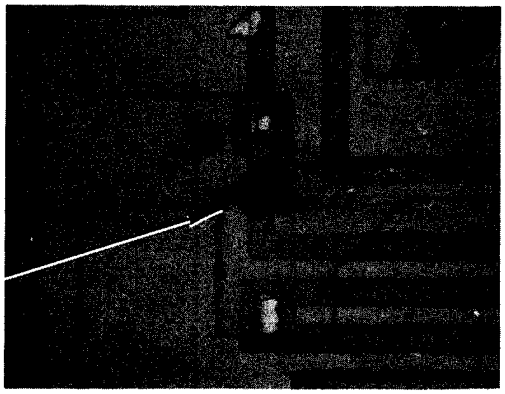

FIGURE 19. Diffusion defect over a P-type resistor.

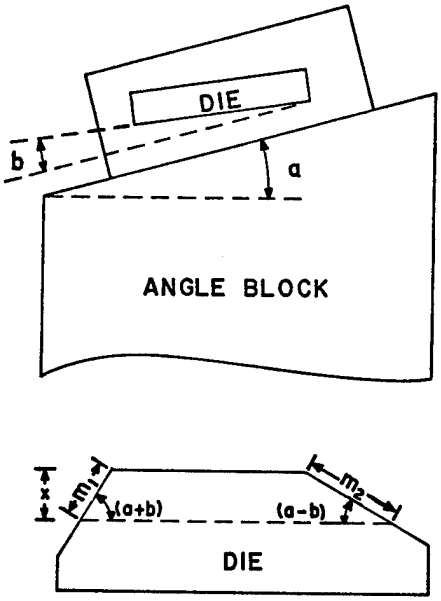

FIGURE 18. The general case where a die is mounted non-parallel to the package bottom. To correct, the die is turned 180 degrees and a comparison measurement is taken.

FIGURE 20. Angle lap of the resistor "pinched" by the N-type defect.

HERMETICITY AND PARTICLE IMPACT NOISE TEST TECHNIQUES

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Summary

Factors to be considered in selecting a hermetic seal test technique are reviewed and discussed. These include package size and condition as well as the objectives of the testing. Also factors which may contribute to result error and wrong conclusions are examined. Why they cause error and the type of results one should be suspicious of are discussed.

The effects of shock levels, vibration level and frequency on particle detection using the impact noise technique are reviewed. Also methods of attaching devices to the transducer are discussed.

Positive actions that can be taken to improve the results of hermeticity and particle detection test are also pointed out.

Text

The choice and proper use of that choice of test techniques for failure analysis is critical. Pick the wrong technique or use the right technique wrong and the result can be to implement a solution to a problem which doesn't exist while the real problem continues in production. This paper addresses some factors to be considered when choosing the test technique so that time spent solving non problems can be minimized. It also points out some pitfalls to be avoided when using the techniques selected.

Hermetic seal testing should be conducted early in the failure analysis process to prevent plugging of leak paths during handling. Further, the fine leak testing should be done prior to gross leak testing because of this plugging possibility. If the device is a fine leaker, the hole would be less than one micron in diameter even if it were a nice single pipeline (see Figure 1). Odds are good that it will be more than a single path, therefore the holes will be even smaller.

The hole size also means that pressure vessels, device carriers, fluids, etc., used for leak detection must be kept clean. Grease, rust or other materials can plug the hole and mask a hermetic seal failure, leaving the analyst wondering how that moisture got in the package.

The fine leak test may be conducted using helium and a mass spectrometer (Figure 2) or krypton 85 (Figure 3) and a scintillation crystal (Figure 4). There are other gases which work as well but these are the two for which commercial equipment is readily available.

The leak range which can be tested is dependent on the free internal volume of the package, the pressure used, the time pressure is applied, the delay time from pressure removal to read and the tracer gas concentration. Figure 5 shows that for larger packages the range is broad and that it becomes more narrow as the free volume decreases. This continues until the pressurization time must become quite long in order for the range of the leak test to overlap the range of the gross leak test. The gross end cut off is moved deleteriously by the storage pump down cycle of the radioisotope equipment. This results from reducing the activation tank pressure to essentially minus one atmosphere at the end of the bomb cycle so that the krypton 85 discharge into the atmosphere can be minimized. The length of time required to complete the storage cycle determines the extent of the negative effect, so it's very important to minimize this time. Preferably the store cycle will not be allowed to exceed two minutes. This is accomplished by a good maintenance program on the equipment and by using filler blocks in the activation tank when testing partial loads of devices. The filler blocks must be inert as far as sorbtion of the tracer gas is concerned. The same type degradation of the detectable range can occur with helium testing if the device carrier has a large free volume which must be pumped for a relatively long period of time prior to reaching the spectrometer's "test" pressure. This pump down time is kept to a minimum through the use of device holders with very little free space around the device and by a good equipment maintenance program.

These same pitfalls can also affect the quantitative data being sought by the test in that excessive pumping will reduce the amount of gas available to be read. This results in leak rates appearing to be lower than the actual value.

Surface contamination such as potting compound, grease, glue off of tags, etc., can also contribute to false results by causing the device to appear to be a leaker. The radioisotope method provides a means to measure this by counting the beta which does not have sufficient energy to penetrate most device cases. Since the beta makes up more than 99 percent of the krypton emission, a device with surface contamination will give a much higher reading on a Geiger Mueller tube than in the scintillation crystal. One must know, however, that the device case does shield this beta because there are some materials being used which do not. This is particularly true with some of the thin lid IC's. For instance, 40 percent of the beta from krypton 85 will penetrate a 0.003 inch thick kovar lid. Sixty percent of the Kr 85 beta will penetrate the 0.004 to 0.005 inch lids typically used on the 1/4 inch by 1/4 inch ceramic IC package. Kovar which is 0.005 inch or thicker effectively eliminates

this beta as do most of the ceramics which are greater than 0.008 inch in thickness.

There are also some ceramics which "get" or absorb the tracer gases and cause the devices to read at some rate. An open package of exactly the same type must be evaluated and a desorbtion curve plotted in order to factor out this background.

For accurate quantitative data all of the test conditions must be calculated and adhered to. Figures 6 and 7 show the formulas used for helium and radioisotope testing. The strict use of these will provide good quantitative data into the upper 10^{-7} atm cc/sec or lower 10^{-6} range. The data then becomes suspect as the leak progresses toward the more gross because the flow assumptions of the formulas are no longer true.

If the previously mentioned precautions are taken, the equipment maintained and calibrated at proper intervals and the personnel doing the testing are well trained, either of these techniques can be used with good results.

There are three common techniques in use for gross leak testing, bubble, weight gain, and dye penetrant. Unlike the fine leak techniques discussed, these do not provide the same type results. The bubble and dye methods provide go-no go information while possibly identifying the leak entrance point. The weight gain technique provides qualitative data, can give quantitative data, but does not help in locating the hole. Therefore it would seem that one has to decide which is more important, to determine that it's a gross leaker of some specific rate or that it's a probable gross leaker with identified leak entrance point(s).

Actually one can do both quite easily, by weighing the device, pressurizing it, reweighing, then immersing in an elevated temperature bath. This sequence performs both weight gain and bubble, providing a rate and a location. Figure 8 shows the fill rates at various pressures for FC-78. FC-72, FC-77 and PP-1 could be expected to flow at about the same rate, close enough for all practical purposes. By using this information to determine the bomb time and pressure and handling the devices carefully, the leak rate can be determined unless it's greater than 10^{-2} atm cc/sec. In that case the device will probably fill completely in less time than can be programmed for pressurization.

The dye penetrant technique was mentioned earlier because it can be a valuable tool to use when ready to delid. With four atmospheres differential, Zyglo will flow through a 2 to 3×10^{-6} hole in trace quantities. This technique can be used to confirm weight gain or bubble identified leaks or sometimes to find leaks which have escaped the other methods. This is particularly true on very small packages where the detectable ranges of the fine and gross techniques barely touch one another.

Fluids must be kept clean for each of these techniques. The back fill liquid for weight gain or bubble must be filtered before each use. The bath fluid should be filtered frequently. The streams are fine and short in some cases and can be lost among particulate matter. The jars in Figure 9 are equipped with filtering lines which allow the hot fluid to be pumped through a one micron filter. New fluid cannot always be assumed to be clean. It should be examined and/or filtered prior to use.

The observer for the bubble technique must be alert from entrance into the bath until exit. Very gross leakers are missed sometimes because the bubbling has ceased by the time the device reaches the observation depth.

Another common problem is the selection of the wrong wait period from removal from pressurization fluid to immersion in the indicator fluid or reweighing. Too short a time, typically less than two minutes, can cause a false indication on either bubble or weight gain. On bubble it's by random bubbling, usually from several places. On the weight gain test it's indicated by the device losing weight rapidly while being weighed. One can also wait too long before testing after removing the device from the pressurization fluid. Typically, within 2 to 5 minutes after removal works best, but this window has to be narrowed for devices with small internal volumes. The correct time is best determined by testing a package with a large ($\geq$ 0.01 inch) hole in it. Each package type and material must be evaluated.

Magnifiers must be used for bubble observation. They should magnify the device at least 3 times, but the magnification must also be low enough so that all of the device can be observed.

Valid hermeticity data can be secured by:

A. Choosing the right technique

B. Keeping everything clean

C. Being observant and curious

D. Keeping equipment well maintained and calibrated

The recommended techniques are:

A. If the package is clean, use helium or radioisotope followed by the weight gain/bubble technique

B. If the package is contaminated, use radioisotope followed by the weight gain/bubble technique

Follow these with dye penetrant testing if possible, particularly in the case of the package with external contamination.

Testing for particles by "listening" for them during vibration has several names. These are:

A. ALPD - Acoustical Loose Particle Detection

B. PIND - Particle Impact Noise Detection

C. PIANT - Particle Impact Acoustical Noise Test

D. PIN - Particle Impact Noise Test

These are all the same thing done on the same type equipment. The basic equipment required is shown in Figures 10 and 11. It consists of a vibration system to shake the device, a transducer to detect the noise generated by a loose particle, a filter/amplifier and means to listen to and look at the amplifier output signal.

This test technique can provide useful information for failure analysis purposes although its primary use is for screening. It can also provide some indication of the size of the particle by the magnitude of signal observed. This is shown in Figure 12. Note that there are minimum and maximum levels for a given mass. This variance is caused by the way the particle strikes the case and its shape. The closer its shape is to a sphere, the closer the output will be to a uniform level. The skill required to translate this signal to a correct analysis can be developed but not in all people. It requires some of the instincts that make a good mechanic or good electronics technician.

There is a great deal of discussion and dissention over the vibration level and frequency, the shock level and how to apply the shock. Because of this these items need to be examined and discussed. The points made are based on more than 12 years use experience with the technique. A paper on this technique by Texas Instruments authors was published in the 1965 Institute of Environmental Sciences Annual Technical Meeting Proceedings.

The vibration level required is enough g's to move the particle and keep it bouncing. Correlation studies conducted with two other companies show no significant difference in signal from a specific device even though one of these companies runs at 5 g and the other runs at 10 g. This is shown in Figure 12. The fact that one company uses 5 g successfully while others use up to 12 g successfully supports the idea that the range works. The guideline for this should be that it's at least 5 g and that it's low enough to minimize noise from the vibrator. Five g minimum is used because test runs at 3 g have failed to yield good results on devices known to contain particles. The maximum will be dependent on the shaker and its condition. If the flextures or suspension is good and the armature or guide doesn't rub one might go up to 20 g and have the noise level below 20 millivolts.

The frequency must cause the particle to have maximum travel within the device and provide a large number of pulses per unit time. The optimum frequency will vary for different package configurations but will be in the 30 Hz to 90 Hz range for all practical purposes. The particle tends to follow the package, but out of phase with it in this range, providing full rebound. Very low frequencies do not provide enough signals per unit time and higher frequencies cause the particle displacement to be reduced providing less signal on impact. For most applications, 65 Hz seems to be quite satisfactory.

The attachment medium should be one which will minimize particle noise signal attenuation and extraneous noise. There are two mediums available which do this, Permacel P-50 double face tape and Dunegan AC-V9 couplant. The P-50 and AC-V9 are compared in Figure 13. The Sperry HV-50A4084 couplant attenuates the signal slightly more than the other two but is water soluble and might be considered if the interest is only in large particles. The P-50 is preferred because no degreasing is necessary and it holds well. Other tapes which have been evaluated have not worked. Tape must be changed after 50 devices are tested and more frequently in some cases. The latter is true with failure analysis type testing because the devices usually contaminate the tape.

Particles tend to stick and must be knocked loose. This knocking loose is a basic requirement of this test technique. This is called "shocking" the device and much has been said and many ways proposed to do this. The fact that it's called shock makes one want to specify a g level and a time duration which in this case is a mistake. The whole purpose of hitting the device is to dislodge (unstick) the particle without damaging the package or the device within. The force required thus varies from package to package. Figure 14 shows the results of several different ways of doing this. Note that tapping the device on the table top immediately prior to testing and tapping it with the finger during test was as much or more effective than the g level controlled techniques. In each of the test groups shown the rejects were put back into the sample after each test run.

A feel for how hard the device must be struck can best be developed by packaging known particles in the package of interest and determining what's required to free the particle when it sticks. What can be done with regard to tapping the device is also controlled to some degree by the package configuration. A thin lid hybrid or a ceramic cannot be thumped with the same vigor as a large stud power package.

If g level numbers are essential to one's peace of mind, the range will be from 50 g to 500 g. Direction must be dependent on what part of the package is accessible. To restate, the tap must be hard enough to loosen the particle, not hard enough to damage the package or device and be administered immediately before and during vibration.

Observation should be made by visual and audio methods during testing. It has been observed that either visual or audio signal may occur without the other one, although in most cases they will be simultaneous.

Fifty millivolts per centimeter is the normally used oscilloscope setting used.

The time on vibration should be short, on the order of 5 seconds. The particle will either bounce on start-up or immediately after tapping during vibration. Several short test runs with removal of the device from the vibrator between each one offer a much higher probability of particle detection than does one lengthy run.

One can get valid results from hermetic seal and particle detection testing if the equipment is understood, the objective of the test is understood and the pitfalls mentioned in the previous discussions avoided.

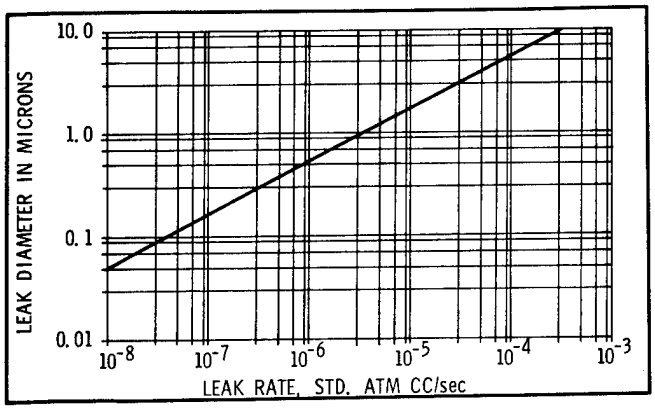

Figure 1. Hole size relative to leak rates.

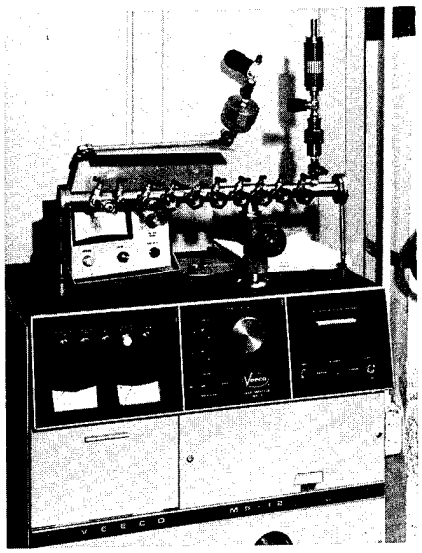

Figure 2. Mass spectrometer used for helium testing.

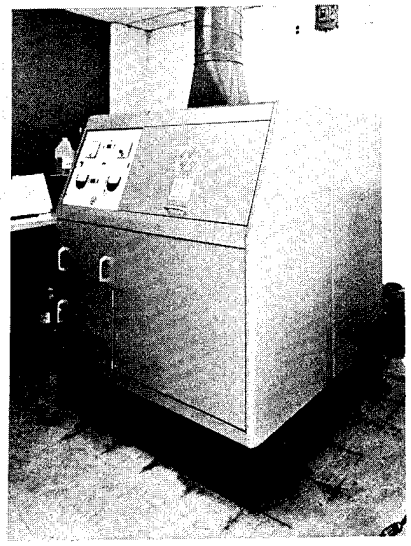

Figure 3. Radioisotope pressurization unit.

Figure 4. Radioisotope counting stations.

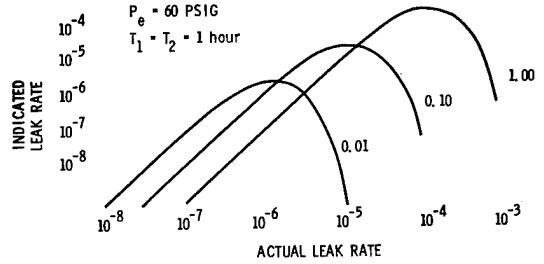

Figure 5. Effect of package size on leak rate range sensitivity.

$$R = \frac{LP_E}{P_o}\left(\frac{M_A}{M}\right)^{1/2}\left\{1 - e^{-\left[\frac{Lt_1}{VP_o}\left(\frac{M_A}{M}\right)^{1/2}\right]}\right\}e^{-\left[\frac{Lt_2}{VP_o}\left(\frac{M_A}{M}\right)^{1/2}\right]}$$

where

- R = the measured leak rate of tracer in atm cm^3/sec
- L = the equivalent standard leak rate in atm cm^3/sec
- P_E = the pressure of exposure in atmospheres absolute
- P_o = the atmospheric pressure in atmospheres absolute
- M_A = the molecular weight of air
- M = the molecular weight of the tracer gas
- t_1 = the time of exposure of P_E in seconds
- t_2 = the dwell time between release of pressure and read out, in seconds
- V = the internal volume of the package in cm^3

Figure 6. Formula for helium test.

$$Q = \frac{R\left(P_o^2\right)}{SKT\left(P_e^2 - P_i^2\right)}$$

where

- Q = measured leak rate in atm cm^3/sec
- R = counts per minute above background
- P_o = atmospheric pressure in atmospheres absolute
- S = specific activity of the tracer gas in microcuries per atmospheric cm^3
- K = counting efficiency in counts per minute per microcurie
- T = pressurization time in seconds
- P_e = exposure pressure in atmospheres absolute
- P_i = internal pressure of device being tested in atmospheres absolute

Figure 7. Formula for radioisotope test.

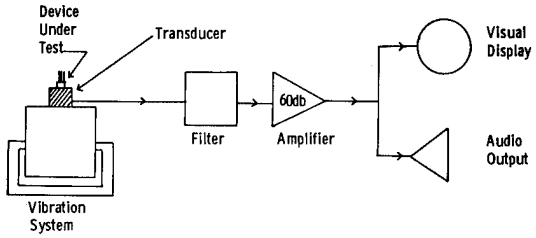

Figure 10. PIND test equipment.

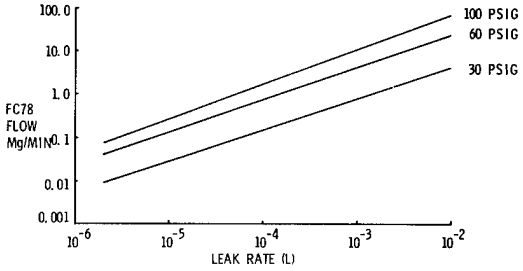

Figure 8. Fill rate in milligrams per minute using FC-78.

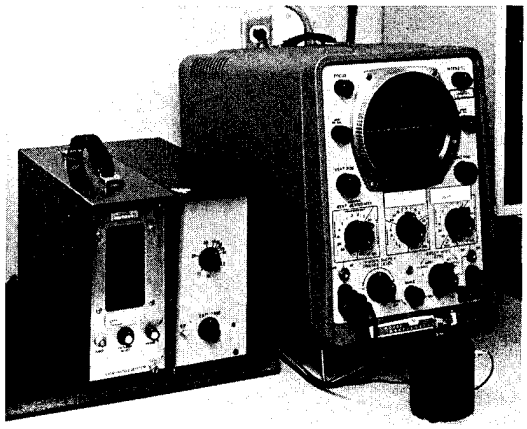

Figure 11. PIND test setup.

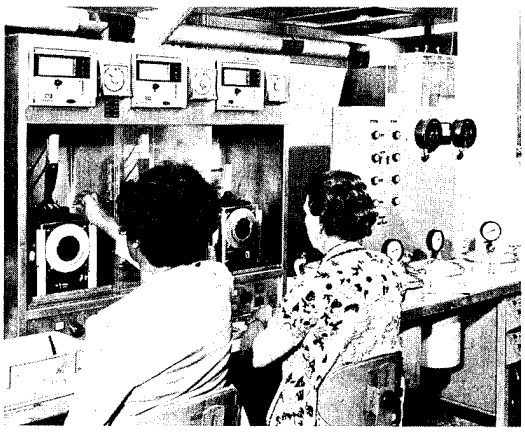

Figure 9. Gross leak test apparatus.

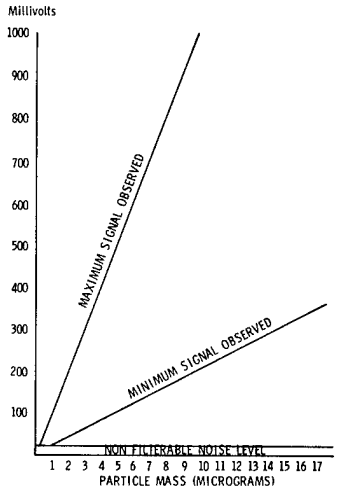

Figure 12. Noise signals from various masses.

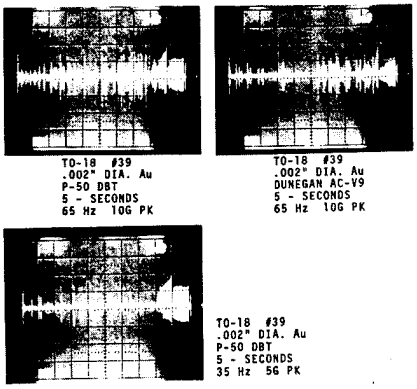

Figure 13. Noise signals at different frequencies, G levels and coupling.

TEST CONDITIONS	QUANTITY	% FAIL
CR-V-CR-V	2400	2.25
TT-V-FT-V	2400	3.58
V	400	40.25
CR-V-CR-V	400	45.5
TT-V-FT-V	400	63
V	400	37.5
CM-V-CM-V	400	49.5
TT-V-FT-V	400	54.25
TT-V-FT-V	200	65
TT-V-CR-V	200	50.5
TT-V-CM-V	200	64

V = Vibrate
CR = Condensaire with rubber tip
CM = Condensaire with metal tip
TT = Table top
FT = Finger tap

Figure 14. Test results using different shock methods.

AN IMPROVED APPROACH TO LOCATING PINHOLE DEFECTS IN MOS AND BIPOLAR INTEGRATED CIRCUITS USING LIQUID CRYSTALS

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Summary

Routine failure analysis of dielectric defects using nematic liquid crystals is possible with the method described in this paper. The refinements on previously described implementations result in excellent definition of the pinhole site.

The paper discusses the principle involved in liquid crystal pinhole detection and details a practical liquid crystal fixture and device preparation.

The influence of cell voltage polarity is illustrated and shown to be an important factor in achieving satisfactory results.

The effectiveness of using dark field illumination and polarized light is shown and compared with the conventional bright field illumination used by prior authors. CMOS, MOS capacitor, and bipolar device analyses are included.

Results are presented in sufficient detail to allow the reader to easily implement the technique in his own laboratory.

Introduction

This paper describes a liquid crystal technique for locating pinholes in thin and thick oxide regions of MOS and bipolar integrated circuits for the purposes of failure analysis. Variations and improvements on previously reported liquid crystal pinhole detection techniques are fully discussed.

Background

Fundamental to the operation of MOS and bipolar semiconductor devices is the formation and maintenance of a defect free insulating layer of SiO_2 over the device surface. In both MOS and bipolar technologies, thick SiO_2 is used over large areas of a device to insulate the metal conductors from the underlying silicon substrate as the metal runs traverse the surface, interconnecting active and passive component regions of the device. This "field" oxide has a nominal thickness of 10,000 Å. Because both process induced and voltage stress induced defects are less likely to occur in regions of thick oxide, field oxide defects are not common.

The proliferation of MOS structures in integrated circuits has increased the incidence of oxide defect problems, since MOS devices depend on relatively large areas of conductor-covered thin oxide in order to function. In MOS transistors, these gate oxides are about 1,000 Å thick. MOS capacitors, which often appear in bipolar op amp integrated circuits, have a thin oxide dielectric whose typical thickness is also about 1,000 Å. The thinness of the active region oxide and the extensive conductor coverage of the thin oxide contributes to making MOS structures more susceptible to process related oxide defects and to voltage induced pinhole shorts than bipolar structures. Figure 1 depicts a typical MOS device cross-section indicating the various material layers of interest.

The Failure Analysis Problem

Historically, the RADC approach to oxide pinhole defect location has been to follow a meticulous procedure to verify that a suspected defect was indeed an oxide fault. Usually an attempt was also made to identify the cause of the fault as either process or electrical overstress induced. A typical procedure previously used at RADC would include the following steps:

1. Terminal Electrical Measurements - Primarily pin to pin measurements used to identify or verify shorts from external pin connections to the silicon substrate. Frequently, a functional test will help locate the section of the circuit that must contain the defect.

2. Visible Light Microscopy - Analysis to detect darkening or other disturbances in the conductor or glass layers which are often indicative of a short through the underlying SiO_2 insulating layer to the silicon substrate.

3. Selective Conductor Removal and Electrical Die Probing - Isolating the suspected region from the rest of the circuit by physically scribing open the conductor stripes and confirming that the short exists under that particular section of conductor by using micromanipulator probes. This step limits the area which must be examined in detail in subsequent steps.

4. Exposure of the Suspect Oxide - Enabling the failure analyst to thoroughly study the suspect oxide under the optical microscope, to attempt precise location and verification of the oxide defect and perhaps establish the defect mechanism. This step involves chemical removal of the glassivation and conductive layers from the device surface.

5. Iterative Cleaning and Optical Analysis - To separate artifacts (dirt, dust, discolorations, etc.) from real oxide defects. Suspect artifacts are noted and the surface cleaned repeatedly with observations after each cleaning step to determine if the "defect" is washed away. A stationary "defect" in a suspect region is then "confirmed" as the site of an oxide pinhole.

6. SEM (Scanning Electron Microscope) Analysis - To provide confirmation of suspect pinhole defects which are often at or beyond optical resolution limits. SEM analysis may also help in attributing the mechanism of failure to processing or electrical stress applied to the device, since it can yield a highly magnified view of the pinhole structure.

The procedure just described is both tedious and often uncertain. With larger, more complex MOS integrated devices becoming more common, a new approach had to be found.

The Liquid Crystal Solution to the Failure Analysis Problem

A simple, quick, positive method for locating oxide pinholes can be devised using nematic liquid crystals. The first application of liquid crystals for

this purpose was reported by Keen[1, 2, 3] and the technique further developed by Ebel and Engelke[4]. Heilmeir, Zanoni, and Barton[5, 6] provide a thorough treatment of liquid crystal theory and characteristics.

The liquid crystal technique has been successfully used at RADC for about two years with variations and improvements being implemented to render it a more practical failure analysis tool.

Referring back to the previous section, the liquid crystal technique eliminates the need for procedure steps 2, 3, 5 and sometimes 6. Terminal measurements are still used to identify the failure mode and to localize the area of interest, the suspect oxide is still exposed for examination by removal of covering layers of glassivation and metal, and a new step is added: Viewing of the device under test in a liquid crystal cell. Since the identification of pinholes is positive, SEM verification is not required and the SEM is used only when the morphology of the defect is of interest.

The simplicity, speed, and positively confirmed results obtainable using this technique justify the enthusiasm expressed by prior authors.

1. The Basic Liquid Crystal Cell

In its simplest form the liquid crystal technique requires a cell as shown in Figure 2. The device under study is prepared for examination by removing glassivation and metallization layers, thus exposing the oxide areas of interest. A drop of liquid crystal material* is placed on the device surface. A glass slide, with a transparent conductive coating on its surface, forms the top of the cell. A voltage is impressed across the cell between the back surface of the device under study (silicon substrate) and the conductive coating on the glass slide. The liquid crystal material is very slightly conductive ($\rho = 10^{11}\ \Omega$-cm) and where there are openings in the insulating oxide, charge flows through the liquid crystal. This current results in localized turbulence in the liquid crystal molecules. The external manifestation of this turbulence is a localized dynamic scattering of light shining on the cell. When viewed through the glass slide with a microscope, the turbulence at the openings in the oxide layer appears dark against a light background when bright field illumination is used and bright against a dark background when dark field illumination is used. The turbulence appears as vortices when seen through the microscope.

The vortices extend laterally beyond the edges of the openings in the oxide making the holes in the insulating SiO_2 layer appear larger than they actually are. This "magnification" enables one to view submicron defects which are at or below the limits of optical microscopy.

The display exhibits a voltage threshold of a few volts below which no turbulence is seen. The turbulence increases with increasing voltage above the threshold level.

The optical effect is also dependent upon the cell spacing, the vortices increasing in width with increasing cell thickness and the motion in the vortex slowing down.

A good display requires that the cell thickness be on the order of 10-20 microns. Lack of parallelism between the surface of the device being analyzed and the brass slide results in either a non-uniformity in the turbulence from one region of the device to another or the shorting of the edge of the device to the conductive coating and consequent shorting of the liquid crystal cell.

2. A Practical Liquid Crystal Fixture

The previous reports published on this technique formed the liquid crystal cell by using either a glass slide floated on a drop of liquid crystal on the device surface or a glass plate held in position over the device by a micromanipulator. We have devised a method of fixturing which makes possible precise control of parallelism of the cell components and the cell spacing. The result is an excellent, stable display of the oxide defects in the device under analysis.

The liquid crystal fixture we developed is shown in the photographs of Figures 3 and 4. It consists of a fixed position, level glass slide, a mechanism for independently leveling the device under study and an elevating mechanism for setting the spacing of the cell. The whole assembly rests on the microscope stage with the elevating controls protruding down through a hole in the stage. The microscope X-Y stage controls move the whole assembly on the microscope stage and the normal microscope focus knobs are used for course and fine focusing. Either a focusing optics or focusing stage microscope may be used.

The leveling of the device under test is accomplished by means similar to a standard microscope leveling stage. A ball bearing acts as a pivot point for the upper plate of the assembly (see Figure 5). The device under study is suspended from this plate by way of the L-shaped bracket and elevating mechanism. Adjusting the two knurled nuts moves the L-shaped bracket, the elevating mechanism and the device under study, until the device is leveled. The fine and course knobs on the elevating mechanism are used to adjust the cell spacing.

The contact to the glass slide's conductive coating is made by two brass rails on the lower plate of the assembly. Spring clips from the lower plate hold the glass slide firmly in contact with the brass rails. The surface of the brass rails is machined to be level with the microscope stage, assuring that the glass slide will always be level.

To level the specimen, the glass slide is slid out sideways on the brass rails and the elevator operated so that the device under test protrudes through the objective window in the top plate of the fixture. The leveling procedure is illustrated in Figure 6. After level has been obtained, a single drop of MBBA is applied with a metal rod directly to the device surface. The device is then lowered to below the level of the brass rails and the glass slide slid back into place. The device is elevated until the MBBA wets the slide and the voltage is turned on across the cell. The final adjustment of spacing is accomplished while viewing the liquid crystal turbulence through the microscope. When the desired effect is obtained, the spacing is adjusted properly.

Examples of a CMOS (Complementary MOS) device, with a pinhole in a gate oxide, are shown in Figures 7, 8 and 9. Figures 10, 11 and 12 are illustrative of analysis performed on bipolar devices with a MOS capacitor, again exhibiting a pinhole. Examples of both bright and dark field illumination are shown. In all the displays, the regions of oxide defects and contact cuts are immediately obvious when viewed

*MBBA: N-(p-Methoxybenzilidene)-p-butylaniline, Eastman Kodak Co., Rochester, NY.

through the microscope since they display moving vortices in the liquid crystal. Spurious spots and lines, that are not defects and which exhibit no motion, can be surpressed by polarizing the incident light to the microscope. This is not so important in the actual analysis but is primarily useful for photographic purposes where the motion of the vortices is frozen and "noise" is not so easily ignored. Figure 13 illustrates very clearly the improvement in photographed displays when the incident light is polarized. The greatest improvement is seen to be for dark field optics where scattering from dirt, etc., lowers the signal to noise ratio in the photograph drastically. (The effect of polarization of incident light is also seen in the other photographs but less dramatically.)

Figure 14 is a high magnification photomicrograph of contact cuts on a bipolar device. Its purpose is to illustrate the effect of cell voltage polarity on the display that is seen. Positive voltage on the conductive coating of the glass slide appears to confine the display more closely to the contact cut areas than does negative. Reference to other figures where pinholes are shown indicates that pinholes are displayed smaller when negative voltage is applied to the conductive coating and in some cases the pinholes are not visible at all. Polarity of the voltage across the cell appears to be an important consideration in achieving a successful display of oxide defects.

Practical application of the liquid crystal technique to locate a pinhole for SEM analysis is shown in Figure 15. The coordinates of the pinhole on the device surface are found from Figure 15A so that the SEM operator may quickly locate the site of the defect at high magnification without excessive searching. SEM photographs of a submicron pinhole are seen in Figure 15B and 15C at 2,600X and 13,000X, respectively (original magnification).

The power supply used consists of a 22½ volt battery, a 5 megohm potentiometer, a 1 megohm current limiting resistor, a polarity reversal switch and an on/off switch. The components fit in a mini-box which can be seen to the right in Figure 4. The schematic of the supply is shown in Figure 16.

3. Specimen Preparation

In order to use the fixture described, the device must either be removed from the package and mounted on a small metal slide or the package must be cut away so that the semiconductor die is the highest projection left on the package base. Examples of specimens prepared both ways are shown in Figure 3, on the sides of the top plate of the liquid crystal fixture. A device is also shown in the test fixture, mounted atop the elevator mechanism.

Contact to the back of the substrate is made by cementing the demounted die to the small metal slide with conductive epoxy. For packages with a conductive epoxy or eutectic die bond to a metal base, contact is made directly to the metal package base. For ceramic packages, contact is made by painting a conductive stripe from the gold die bond pad on the ceramic base, around the package edge and across the package bottom.

The preparation of a MOS device for gate oxide pinhole analysis requires successive chemical strip of the top deposited glassivation layer and, in turn, removal of the interconnect aluminum metal. This operation requires careful control to prevent unwanted etch damage to the MOS gate regions under investigation. A special measurement technique was used to insure a degree of glassivation etch control with the known etch rate of the chemical agents* used. (The etch rate was established from manufacturer's data and by experiment on sample devices.) A surface profile measuring instrument (Dektak**) was used to determine the topography (thickness) of the MOS surface structure; i.e., deposited glass layer, aluminum interconnect stripes, and thermal oxide (SiO_2) layer relative to the underlying silicon surface. It was determined that the deposited glass top layer of the MOS device exhibited greater deposition thickness (approx. 30%) in regions overlying the aluminum internconnect stripes. This differential glass thickness proved troublesome to cope with in a normal glass etch cycle. A second profile trace following a normal glass strip revealed >2500 Å of glass remaining over the aluminum interconnect stripes. Additional etching to remove this residual glass layer would etch the thermal oxide (SiO_2), undercutting the gate metal and possibly damaging the gate oxide. An extended glass etch could also generate pinholes in the gate oxide or obscure interpretation of latent pinhole shorts already present by etching through pinholes in the gate metallization. Instead, the devices were subjected to an aluminum etch***. The residual glass layer masks the aluminum and tends to inhibit the etch rate somewhat. In time, however, undercutting of the aluminum takes place, resulting in complete removal of the aluminum and generally, detachment of the overlying glass.

An alternate technique was evaluated to speed up the above lengthy etch cycle. In this method an ultrasonic energy cleaner is used to fracture and lift off the residual glass tunnel that may remain after a partial glass-Al etch. It was discovered that ultrasonic agitation, if continued for an extended time, (30-45 min.) would generate an abundance of oxide faults in the thin gate oxide. In practice, a short ultrasonic agitation cycle (10 sec to 1 min.) was quite effective.

Preparation of the device for analysis in the SEM requires that all the MBBA liquid crystal material be cleaned off the surface. Acetone is a suitable solvent for this purpose.

4. Safety

Previous authors have warned that MBBA contained compounds which might stimulate cancer. Eastman Kodak has advised us[7] that an earlier researcher had apparently mistaken the name of an MBBA constituent, benzylidene, for benzidene, which is a recognized carcinogenic agent. Their review of all available information concerning possibly carcinogenic action by chemicals failed to reveal any report of carcinogenicity for MBBA. As with any chemical, due care should be exercised in its use.

Limitations and Problems

The technique and fixturing we describe is not a panacea for all oxide defect failure analysis problems. Two major deficiencies for which we have not found a suitable answer are the inability to test (1) silicon on sapphire devices and (2) silicon gate devices. The former cannot be tested because we have not been able to devise a way to make contact to the back of the silicon islands as is required to form the liquid

*Siloxide Etchant, Transene Company, Inc., Rowley, MA. Q-etch Glassivation Etch: 100 parts NH_4F (40% sol.), 30 parts H_2O, 22 parts H.F. (49% sol.)
**Dektak, Sloan Technology Corp., Santa Barbara CA
***B-etch aluminum etch: 2 parts H_2O, 1 part HNO_3, 1 part CH_3OOH, 16 parts H_3PO_4

crystal cell. The later cannot be tested since we know of no way of removing the polysilicon gate conductor without destroying the integrity of the gate oxide.

There are four minor problems in using our approach: (1) the device must either be out of the package or the package cut away; (2) the fixture is somewhat sensitive to vibration since the spacing is so small and undamped springs are used in the assembly of the top and bottom plates of the fixture; (3) gas bubbles are sometimes generated in the cell after prolonged viewing with the power on; and (4) still photography is not able to adequately capture the full impact of the moving vortices as seen by the human eye directly through the microscope.

Conclusions

Despite any shortcomings mentioned, we have found this technique and fixturing provides a quick, positive, practical method of performing failure analysis for oxide pinhole defects. It is non-destructive of the thermal oxide and has possible application for in-process, as well as failure analysis applications. It allows a failure analyst to quickly locate the region of interest for the SEM operator, saving an extensive search operation on the SEM.

Changes in fixturing and experiments using combined nematic and cholesteric liquid crystals[6] will evolve and probably result in further refinements. As can be judged from the photographs, very little improvement is necessary, since the technique as we use it provides a satisfactory failure analysis tool.

Acknowledgements

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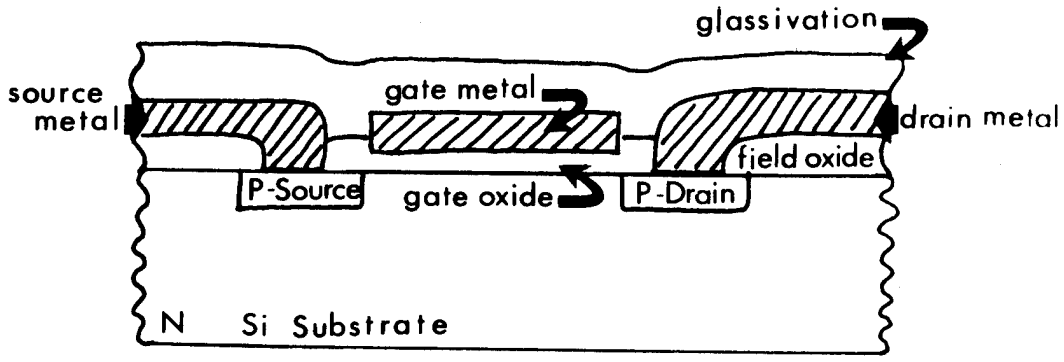


Figure 1 - Typical P-MOS Transistor Cross-section. The glassivation is deposited SiO_2. The field and gate oxide are thermally grown SiO_2.

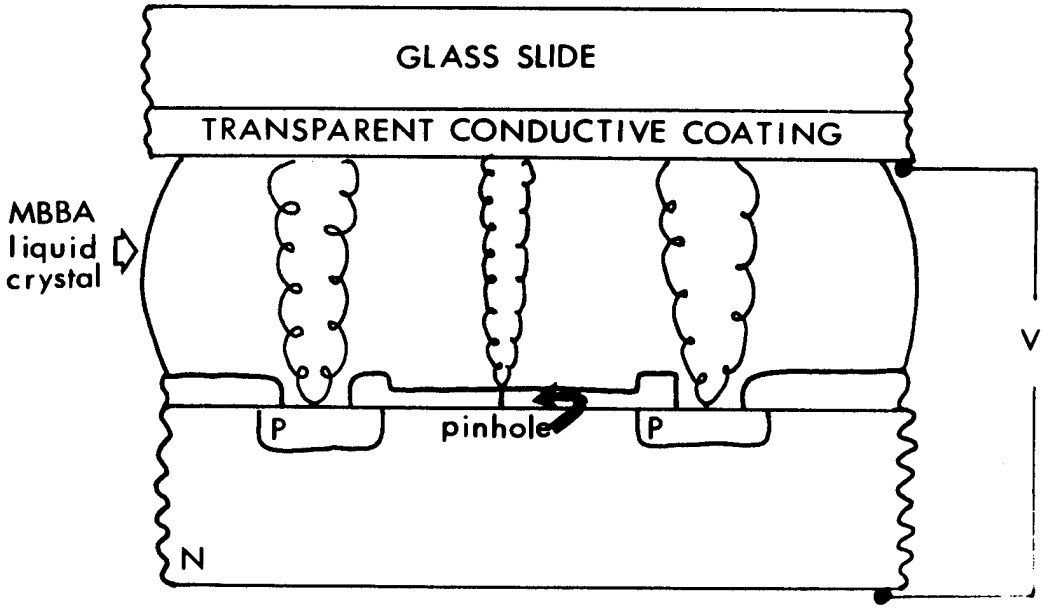


Figure 2 - Basic Liquid Crystal Cell. The cell is illuminated and viewed from the top through a microscope. The large oxide openings are contact cuts made to allow the conductor to make contact to source and drain regions.

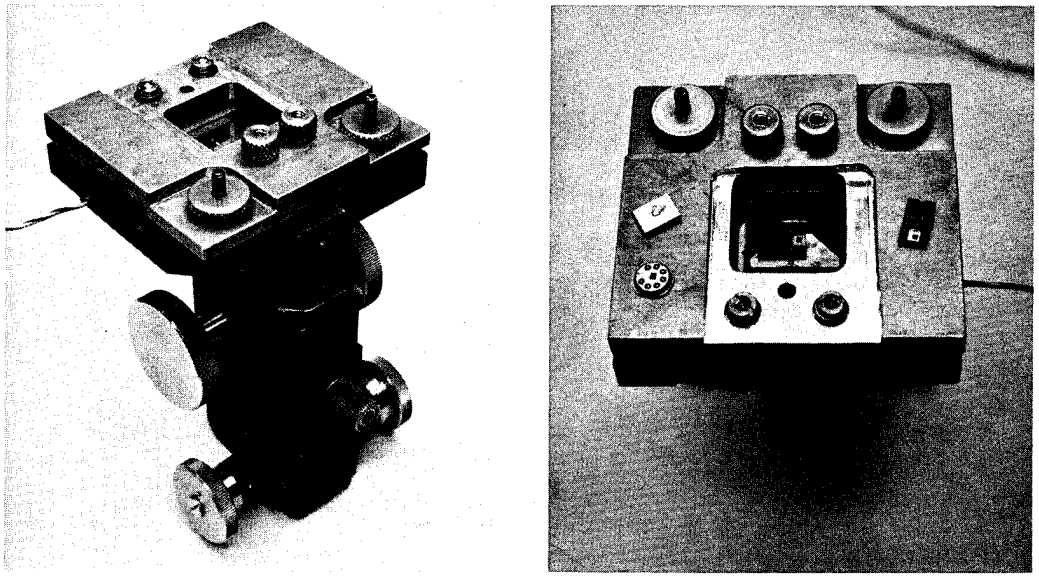


Figure 3 - Liquid crystal fixture, demounted. Also shown are devices prepared for testing.

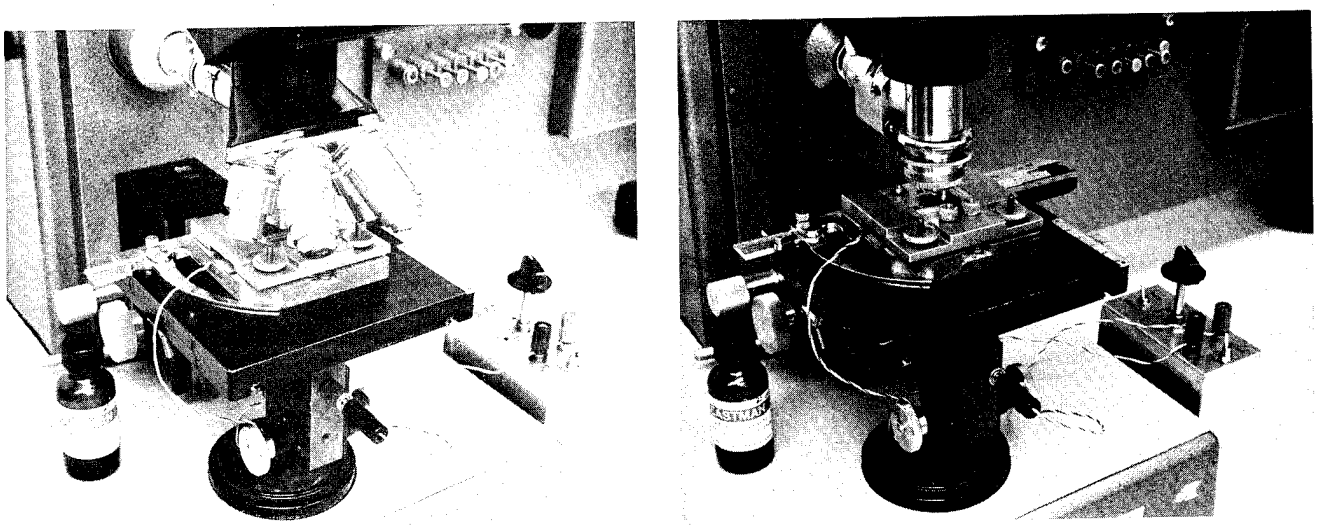
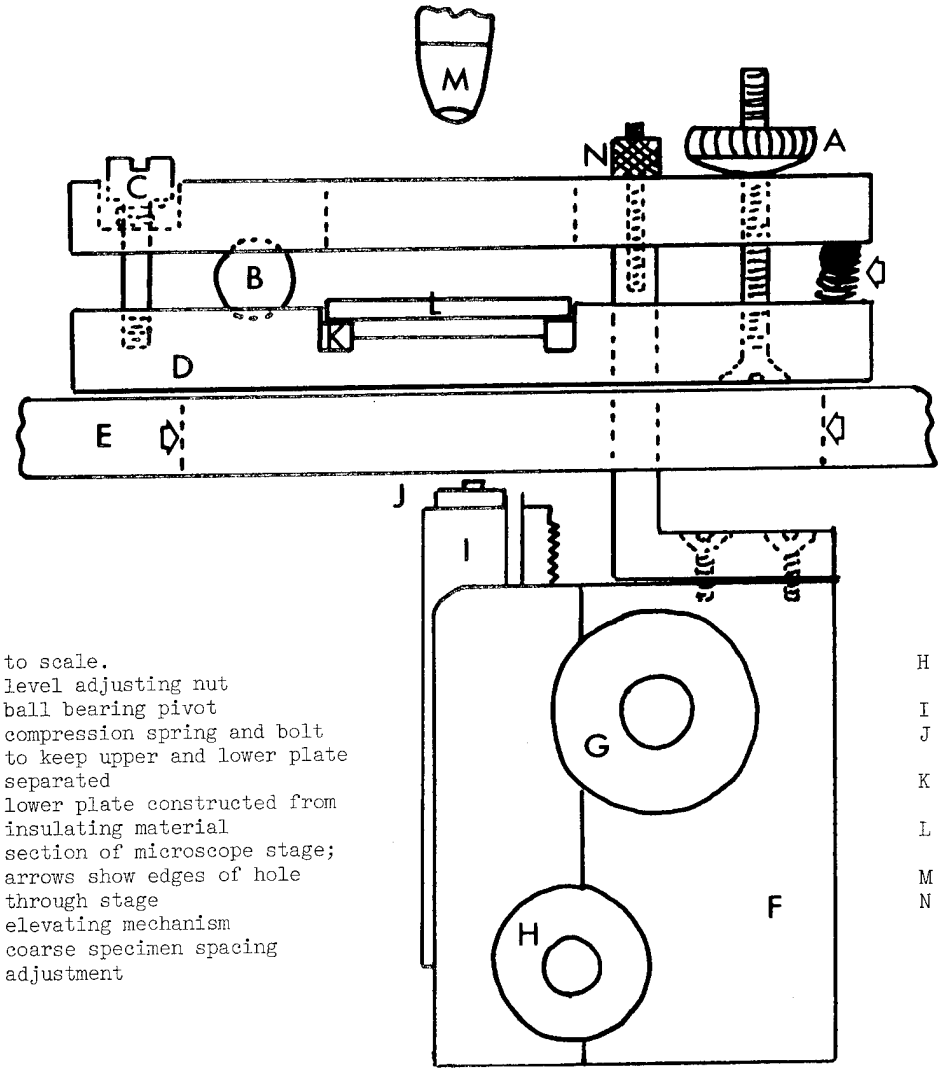


Figure 4 - Liquid crystal fixture in place on metallograph stage; left, bright field optics; right, dark field optics.

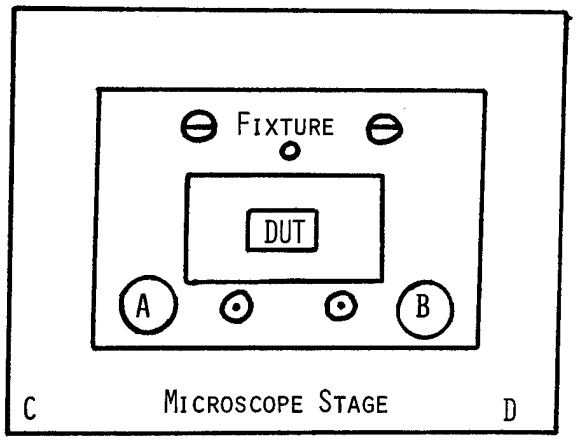


Helper springs to aid springs at C.

Not to scale.
A - level adjusting nut
B - ball bearing pivot
C - compression spring and bolt to keep upper and lower plate separated
D - lower plate constructed from insulating material
E - section of microscope stage; arrows show edges of hole through stage
F - elevating mechanism
G - coarse specimen spacing adjustment

H - fine specimen spacing adjustment
I - specimen elevator
J - specimen mounted on metal slide
K - brass rails machined parallel to stage
L - conductively coated glass slide
M - microscope objective
N - knurled nut for ease of removal of fixture from microscope stage

Figure 5 - Liquid Crystal Fixture Schematic



Liquid crystal stage mounted on microscope stage.

Device under test as viewed through eyepieces of the microscope.

Step 1. Focus on the DUT at the corner labeled 2 at approximately 200 X magnification.

Step 2. Using the microscope stage X-Y controls, traverse to the corner labeled 4.

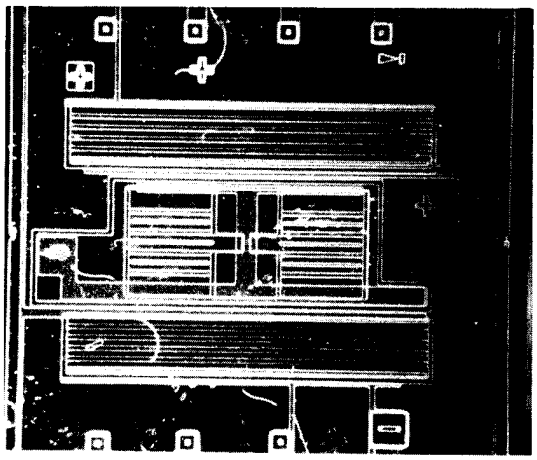
Step 3. Do not refocus. Push down or pull up on the corner of the microscope stage at the corner labeled D and note which direction produces better focus. Turn the leveling nut B clockwise or counterclockwise (down or up) direction as needed to produce a focussed image at corner 4. Return to step 1 and repeat until corners 2 and 4 stay in focus after simple traverse of the stage.

Step 4. Using the microscope stage X-Y controls, traverse to the corner labeled 1. Focus using the microscope focus controls.

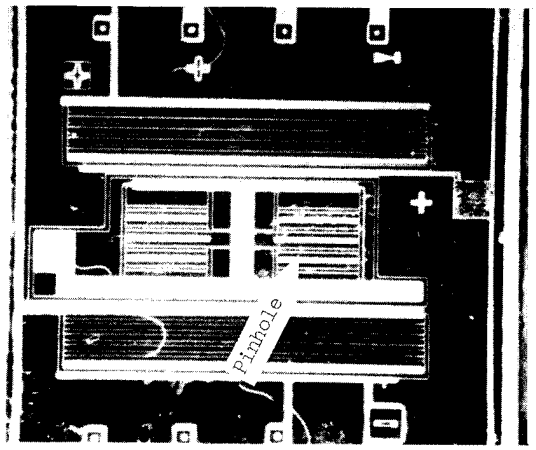
Step 5. Using the microscope stage X-Y controls, traverse to the corner labeled 3.

Step 6. Do not refocus. Push down or pull up on the corner of the microscope stage at the corner labeled C and note which direction produces better focus. Turn the leveling nut A clockwise or counterclockwise (down or up) direction as needed to produce a focussed image at corner 3. Return to step 4 and repeat until corners 1 & 3 stay in focus after simple traverse of the stage.

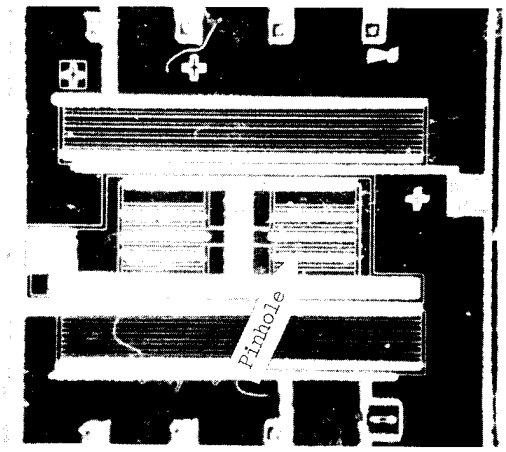
Figure 6 - Leveling Procedure



0 volts, 1 sec. exposure, 82 X magnification.



+17 volts, 1 sec. exposure, 82 X magnification.



-17 volts, 1 sec. exposure, 82 X magnification.

Figure 7 - CMOS device viewed through liquid crystal cell without polarizer, dark field illumination. Large illuminated areas are contact cuts. A pinhole is visible at the second gate of the lower n-channel transistor. Other bright spots which are not pinholes are also seen. See text and following figures.

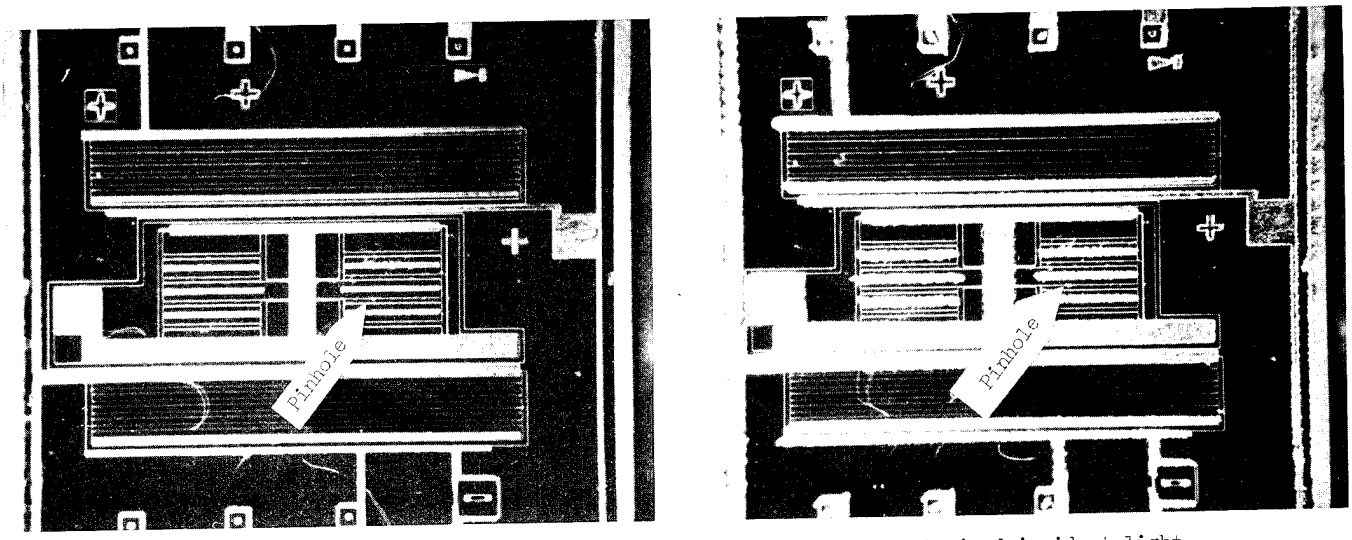


Figure 8 - CMOS device viewed through liquid crystal cell with polarized incident light. Spurious bright spots are greatly reduced. See text. Left: +17 volts; right: -17 volts. 82 X, 2 sec. exposure.

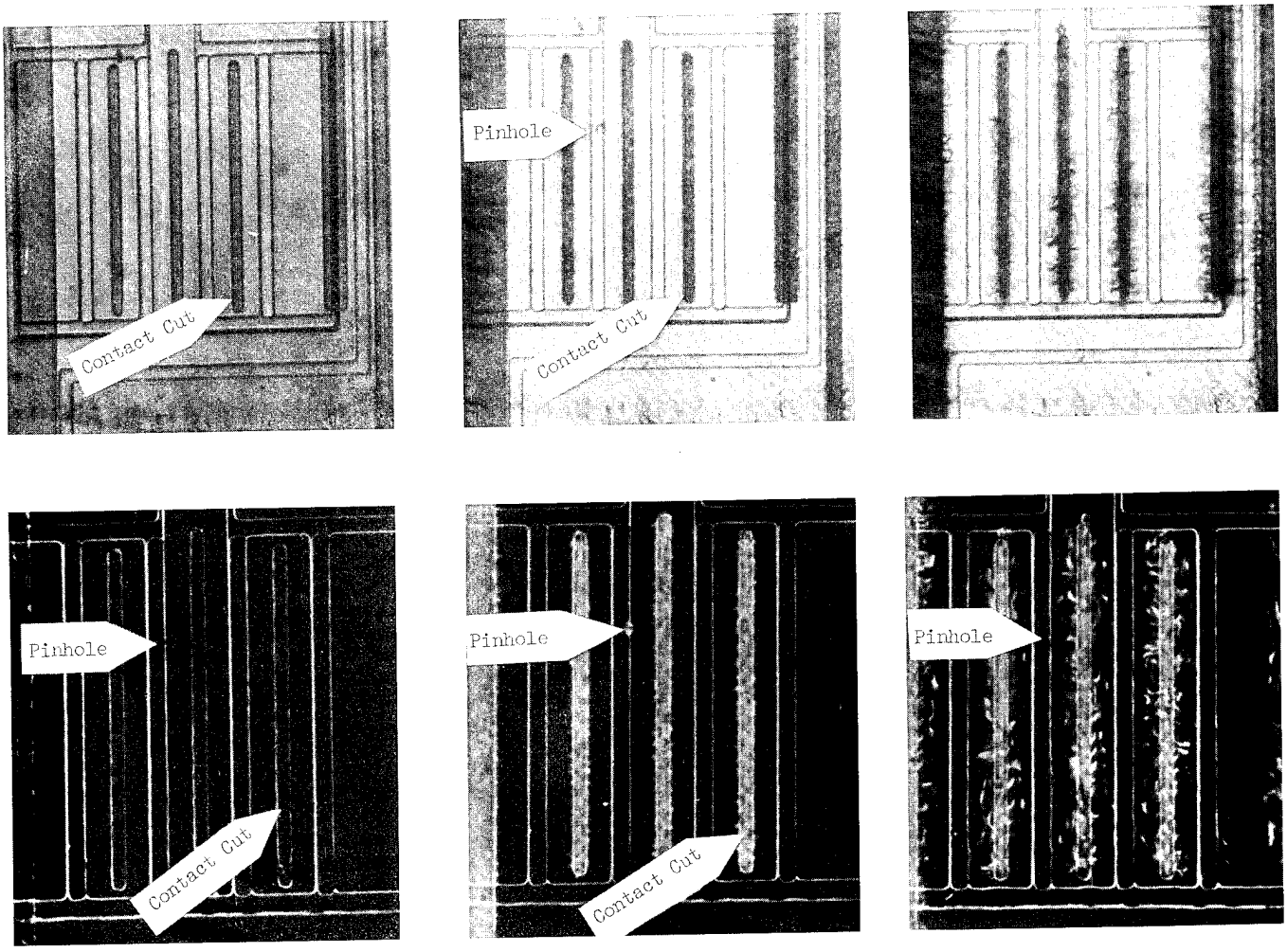


Figure 9 - CMOS device viewed through liquid crystal cell. Top left to right, bright field, 0 volts, +18.4 volts, -18.4 volts; ½ sec. exposure, 185 X. Bottom left to right, dark field, 0 volts, +16.4 volts, -16.4 volts; 3 sec. exposure, 204 X; green filtered incident light.

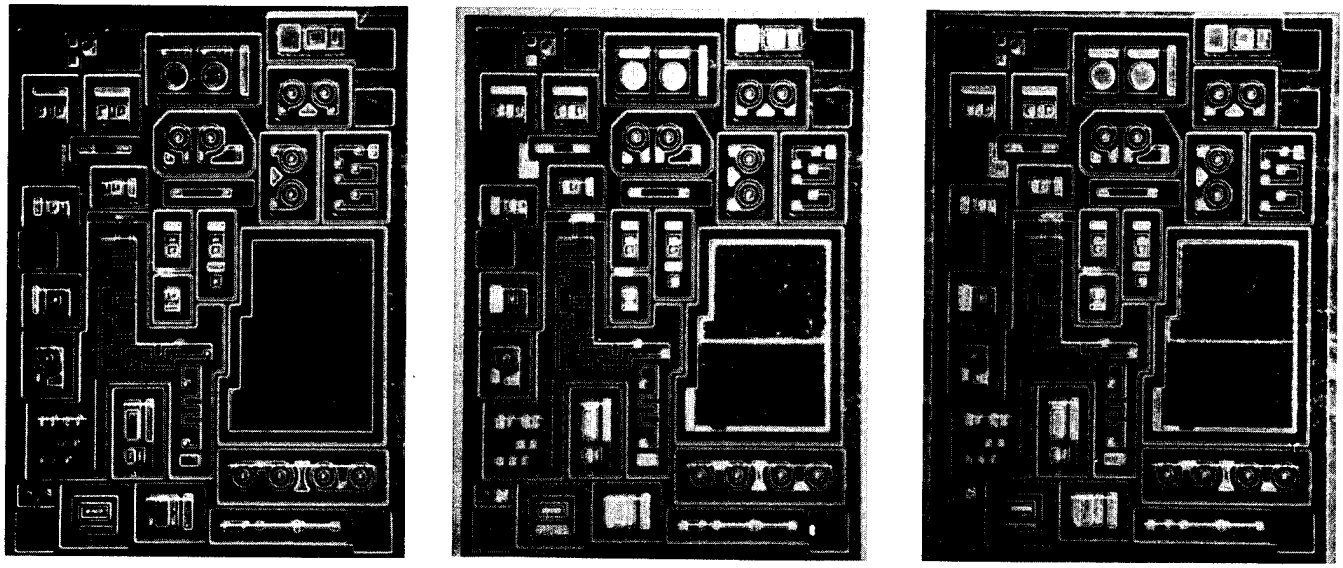


Figure 10 - Bipolar device with MOS capacitor viewed through liquid crystal cell with polarized incident illumination, dark field. Left to right, 0 volts, +21 volts, -21 volts; ½ sec. exposure, 50 X. Capacitor was metallized on the bottom half only.

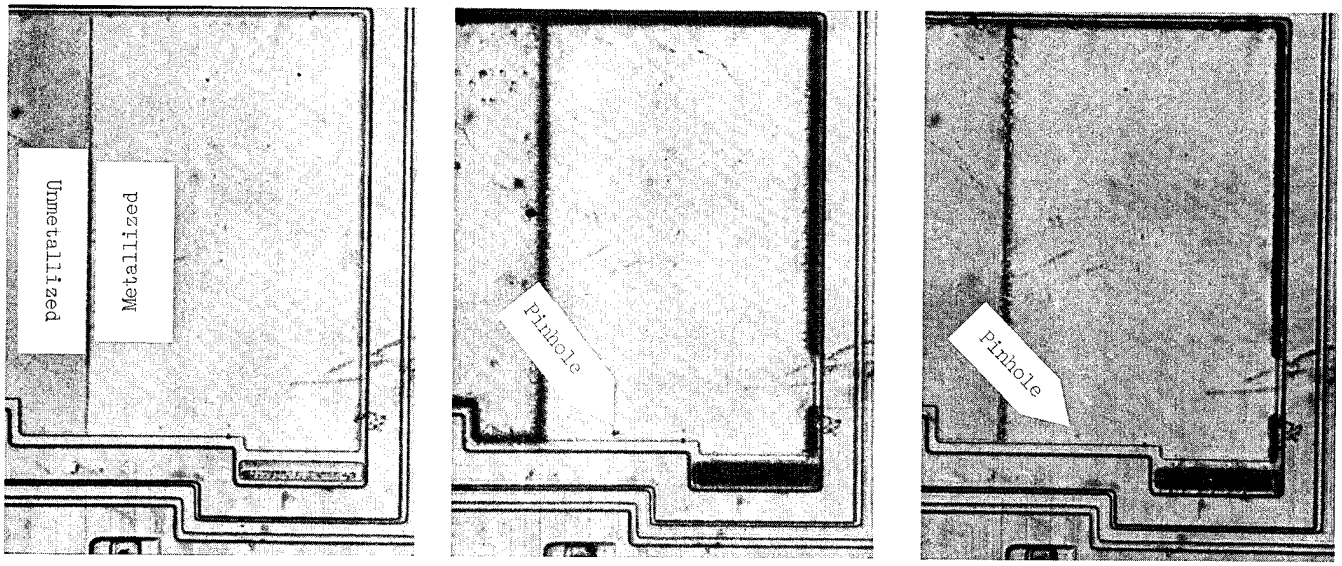


Figure 11 - MOS capacitor viewed through liquid crystal cell. Left to right, bright field, 0 volts, +21 volts, -21 volts; 3 sec. exposure, 150 X, green filtered illumination. The capacitor was metallized only to the right of the vertical line indicated. The metallization covered the edge of the thin oxide along the bottom of the capacitor and on the right side where a metal stripe connected the capacitor to other elements of the device. Where the metallization did not cover the thin oxide, etching of the thin oxide occurred during glassivation removal. A pinhole defect is seen at the lower edge of the capacitor.

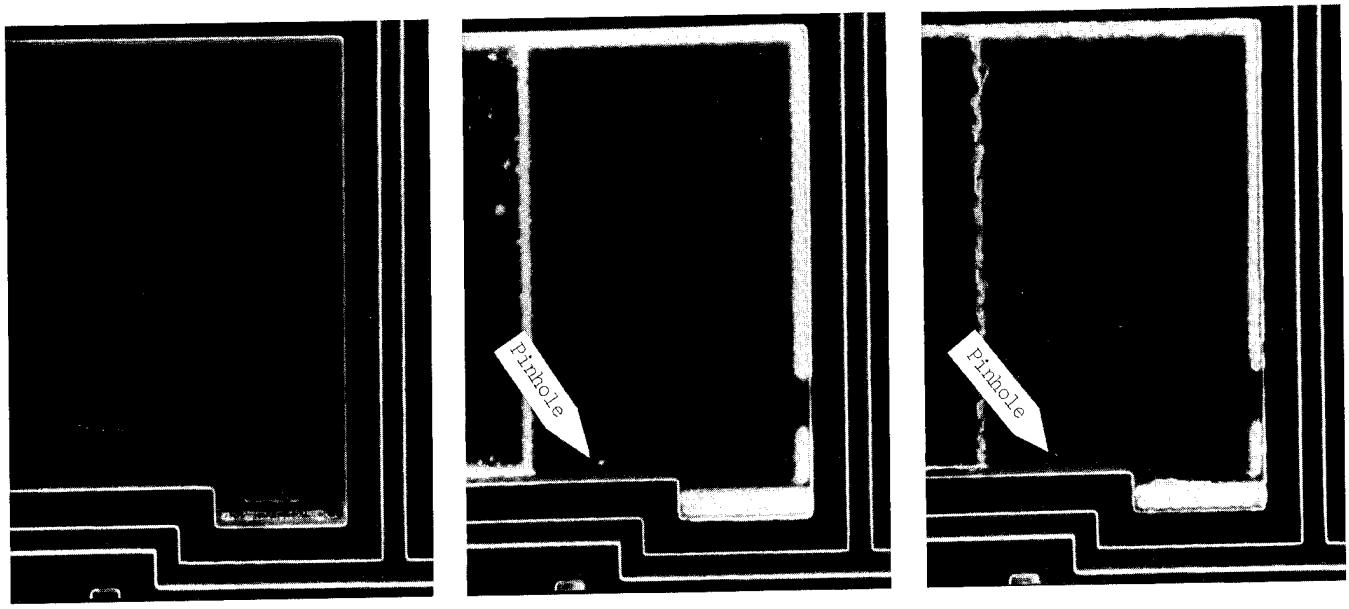


Figure 12 - MOS capacitor viewed through liquid crystal cell. Left to right, dark field, 0 volts, + 21 volts, - 21 volts; ½ sec. exposure, 150 X, polarized incident illumination.

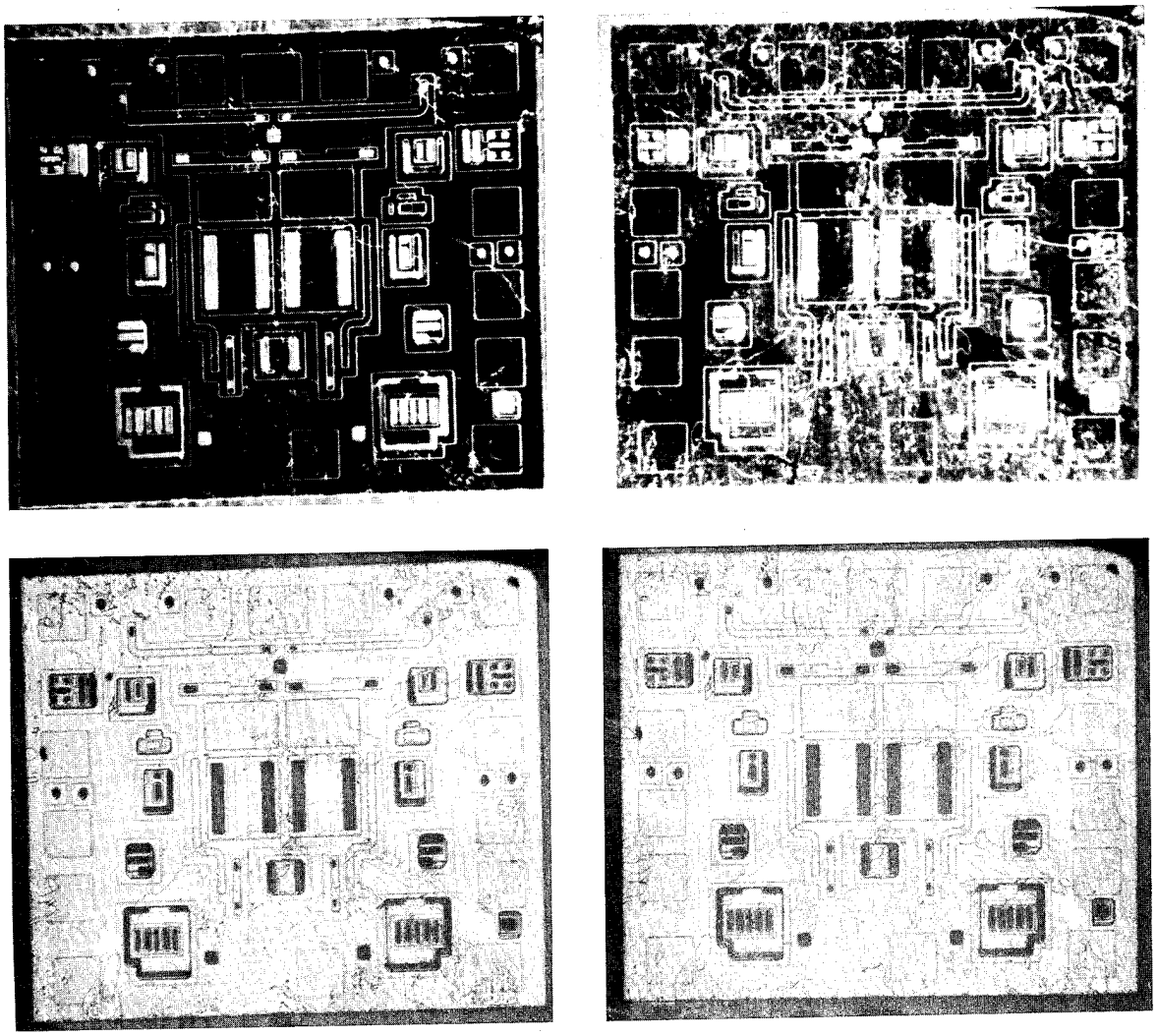


Figure 13 - Comparison of displays seen using polarized vs. non-polarized incident light. Dark field, green filter: top left, polarized light, +14.2 volts, 3 sec. exposure, 81 X; top right, non-polarized light, +14.2 volts, 1 sec. exposure, 81 X. Bright field, green filter: bottom left, polarized light, +16.7 volts, 1 sec. exposure, 82 X; bottom right, non-polarized light, +16.7 volts, ½ sec. expsoure, 82 X.

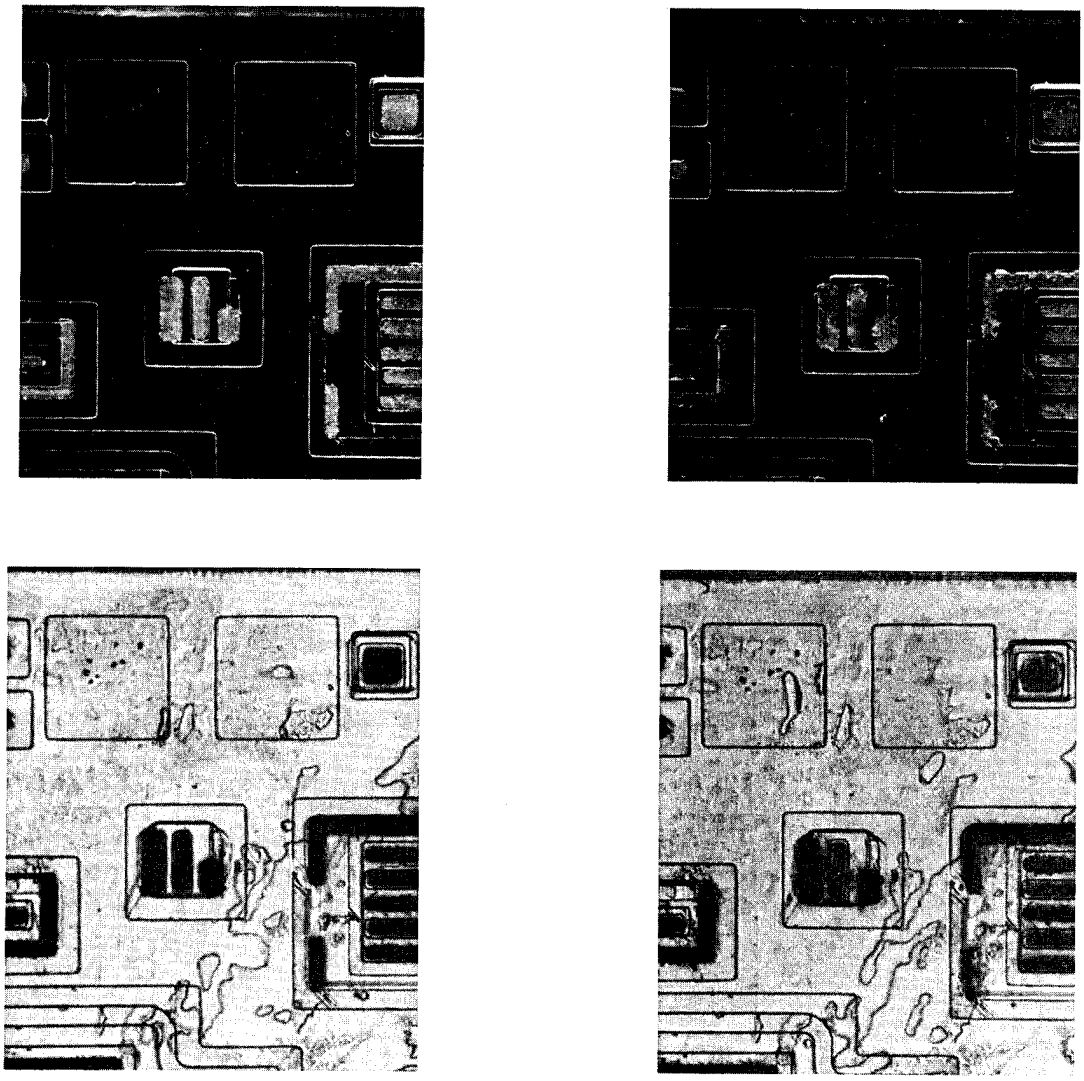
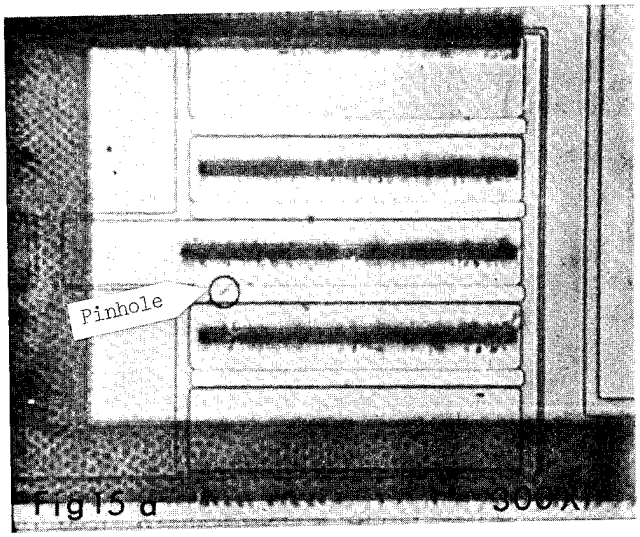
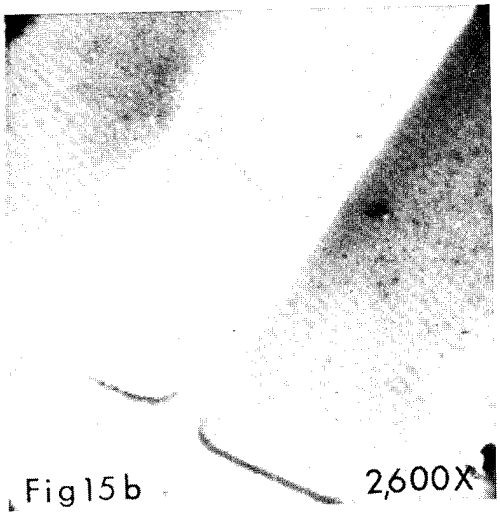


Figure 14 - Comparison of displays seen at high magnification at contact cuts using positive vs. negative polarity voltage to the conductive coating on the glass slide. Dark field, polarized incident light, green filter, 6 sec. exposure, 240 X, top left, positive voltage to conductive coating; top right, negative voltage to conductive coating. Bright field, polarized incident light, green filter, 3 sec. exposure, 240 X, bottom left, positive voltage to conductive coating; bottom right, negative voltage to conductive coating.





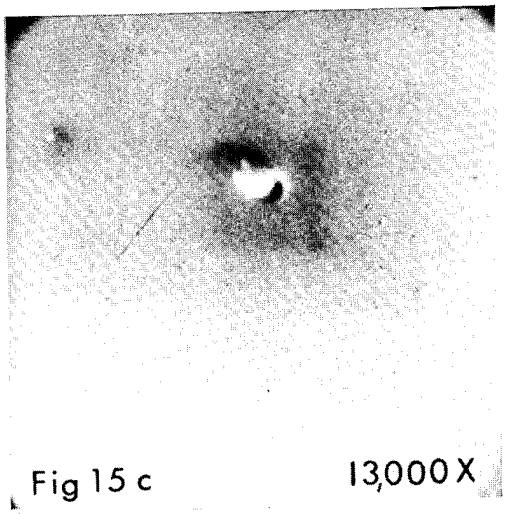


Figure 15 - Submicron Pinhole Detection Capability; a) liquid crystal at 300 X, b) SEM at 2,600 X, c) SEM at 13,000 X.

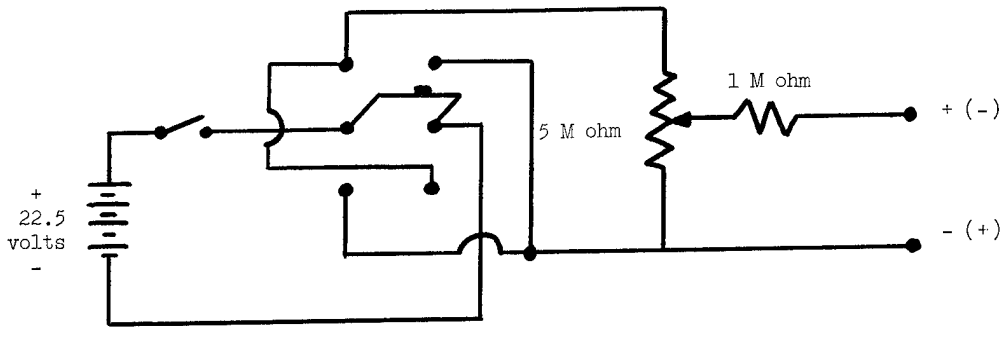


Figure 16. - Power Supply

NONDESTRUCTIVE SEM STUDIES OF LOCALIZED DEFECTS IN GATE DIELECTRIC FILMS OF MIS DEVICES

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A nondestructive technique to identify localized defects in the gate dielectric of MOS devices has been developed. The technique is based upon electron beam induced conductivity modulation which gives rise to a relatively large increase in gate current under an applied bias when the beam scans a localized defect area. Measurements on devices with low gate breakdown voltage have been made and correlated with regions where subsequent catastrophic gate breakdown occurred. A circuit description and physical model of the technique is presented.

Introduction

Electrically weak regions in gate dielectrics of MOSFETs contribute significantly to device failures and hence impact reliability and yield of MOS/LSI. A rapid nondestructive technique to detect localized weak regions in the gate dielectric would provide an invaluable tool to determine the nature of such defects and hence provide a better understanding of device failure. One such technique can be implemented with a scanning electron microscope and is described here. This technique is simple, nondestructive, namely, allows the gate metal to remain undisturbed, and provides several advantages over some of the more commonly used techniques.

Several methods to determine localized defects in dielectric films have been reported in the literature[1]. The most commonly used are (i) optical microscopy, (ii) electrolytic copper decoration[2], (iii) Nematic liquid-crystal light scattering in an electric field[3], (iv) standard dielectric breakdown and (v) self-healing dielectric breakdown[4]. These techniques are either non-discriminatory between electrically active and non-active defects (optical microscopy) or limited in resolution(>10μ for nematic liquid-crystal light scattering), or limited to dielectric films on a monolithic bulk semiconductor structure (ii and iii), or are destructive (iv and v). We propose an electron beam enhanced gate leakage current measurement technique (EBEGC) as a means of nondestructively determining electrical weak regions in MOS gate dielectrics. The major advantages of this technique are:

(i) It is a nondestructive determination of weak regions in a gate dielectric.
(ii) The weak regions can be determined in a manner where the device structure is unaltered.
(iii) The resolution is better than 1 μm and is limited by the beam voltage and gate metal thickness.

The technique can also be used to determine the relative weakness of different defects in the gate dielectric and hence allow a quantitative mapping of the localized defects.

Principal of Operation

The secondary electron, backscattered electron, Auger electron and x-ray emission from a sample in a SEM can be used to obtain microscopic topological details of the sample surface. In the case of electronic materials, however, the interaction of the electron beam with the bulk material can be used to determine some electronic properties such as diffusion lengths and lifetimes of minority carriers[5], electric field profiles at semiconductor p-n junction via EBIC[6] or variations in the resistivity[7] of the material, These measurements are based upon the generation of excitons (hole-electron pairs) under the influence of the high energy electron beam.

The EBEGC results from the generation of charge carriers by the electron beam in an electrically stressed region of the gate insulator. The magnitude of variation in the EBEGC of a region is in general dependent on the local electrical field. The presence of defects which result in a high localized electric field would thus cause a relatively larger change in the EBEGC. A map of the beam enhanced current through the gate insulator as it is scanned by the beam would then show the presence of localized gate defects.

In order to detect the relative change in current one needs to make electrical contact to the insulating layer. Thus, the normal gate oxide of a finished MIS transistor or capacitor is ideally suited for this type of study since one can make contact to the body and the gate metal of these devices. The thickness of the gate metal layer would determine the beam voltage since the beam electrons must penetrate through to the gate insulator. For a 1 μm thick gate metallization a 20 Kev beam would suffice. The spreading and intensity loss in such a metallic layer would limit the spatial resolution of the EBEGC technique to approximately 1 μm. Variations in the gate metal thickness could affect the results but these variations are quite obvious from a surface examination.

As the electron beam scans the gate area the leakage current is modulated by the characteristics of the point at which the beam is directed. This modulation can then either be displayed directly on a CRT of the SEM or mixed with the secondary electron signal to give an indication of the variation of beam enhanced leakage current over the gate area.

Experimental Technique

The instrumentation required for measurement of the electron beam enhanced gate current (EBEGC) consists of a bias source, a current to voltage converter and a mixer. Figure 1 is a block diagram of the EBEGC system. The mixing amplifier allows the simultaneous display of both the EBEGC signal and the normal high resolution secondary electron signal. Thus the details of the EBEGC signal can be spatially related to the device structure. The mixing amplifier also allows the operator to vary the gain and offset of the input signals which enables a relative control of the intensity of the EBEGC signal and the secondary electron signal. Thus one can adjust the contrast between these signals to obtain an optimum CRT display. The bias supply and current to voltage converter are shown schematically in Figure 2. The bias supply can be operated in either of two modes, namely, a constant voltage or constant current. In the constant voltage mode (0-20V) (cf. Fig. 2a), the current through the device is monitored and an equivalent voltage signal is obtained from the current to voltage converter. This voltage serves as an input signal and is fed to the mixing amplifier. The current sensitivity is switch selectable from 10^{-8}A to 10^{-4}A for a one volt full scale output. In the constant current mode a

fixed current is forced through the gate insulator and the voltage developed across the gate serves as an input signal and is fed directly to the mixing amplifier. This circuit is illustrated in Figure 2b. The polarity of the bias applied to the gate of an MIS device can also be selected externally. A front-panel LED is used to indicate amplifier overload. This enables the operator to avoid false indications caused by amplifier overload and signal clipping.

Results and Discussion

Defects in gate dielectric films of MIS devices which enhance the electric field in its vicinity such as pin holes, thin spots, particulate impurities and sharp edges due to device geometry of the gate insulator can be detected by the EBEGC technique.

We illustrate the use of EBEGC to detect weak spots in the gate insulator due to the silicon edge[8] commonly encountered in MIS transistor on silicon on sapphire (SOS). The electric field in the gate insulator at the silicon island edge is expected to be higher than the rest of the gate area due to the geometry as shown in Figure 3. When the electron beam scans such a high field region, one detects a larger beam induced current due to the higher drift velocity of the generated carriers in the electric field. Figure 4(a) is a secondary electron micrograph of an MIS/SOS transistor. The EBEGC signal-mixed with the secondary electron signal of this transistor is shown in Figure 4(b). It can be seen from these micrographs that the EBEGC signal is enhanced at the silicon island edge. Figure 4(c) is a secondary electron micrograph of the MIS/SOS transistor shown in Figure 4(a) after a catastrophic gate failure. The correlation between the device gate failure and the EBEGC signal is obvious from Figure 4(b) and 4(c). Figures 5(a) and 5(b) are another example of the correlation between the EBEGC signal seen as a bright spot in Figure 5(a) and eventual gate failure seen in Figure 5(b).

The presence of semiconductor junctions under the gate insulator can also give rise to an enhanced current in the EBEGC mode, under appropriate gate bias condition. Unlike the EBIC current, which is measured directly across the junction, this junction current is detected through the gate of the MIS transistor. Figure 6(a) is an EBEGC picture of a p-channel MNOS/SOS transistor where the terminals of the transistors are connected as shown in the inset in the figure. Under a positive bias the channel region is accumulated with majority carriers and the carriers generated near the drain-substrate and source-substrate junctions can be detected as a current through the insulator. However when the channel region of the MIS transistor is inverted by applying a negative gate bias the p+n junction between the source-substrate and drain-substrate at the semiconductor surface is eliminated by the presence of holes in the channel region. Figure 6(b) is an EBEGC micrograph of the p-MNOS/SOS transistor under a negative gate bias. It can be seen that the semiconductor junction can no longer be detected. In the presence of semiconductor junctions one can therefore minimize the junction current by an appropriate bias on the gate insulator. The effect of the gate bias on the junction current can conversely be utilized to determine uniformity of channel formation in a MIS transistor.

Conclusions

A nondestructive technique based upon the electron beam enhancement of the gate leakage current (EBEGC) of a MIS device has been developed to study localized defects in the gate dielectric. The resolution of this method is determined by the beam spreading within the gate metal and gate insulator. Thus for a beam voltage of 20 KeV, 1 μm thick metallization and $\leq$5000Å of gate insulator one can obtain a resolution of approximately 1 μm. Experimental results were presented to show weak gate areas at silicon island edges encountered on SOS devices by the use of this technique. The presence of semiconductor junctions under the insulator were also found to yield a signal in this mode but, under appropriate gate bias one could eliminate this signal. It was suggested, however, that the presence of this signal could be utilized to determine uniformity of channel formation in an MIS transistor as a function of bias.

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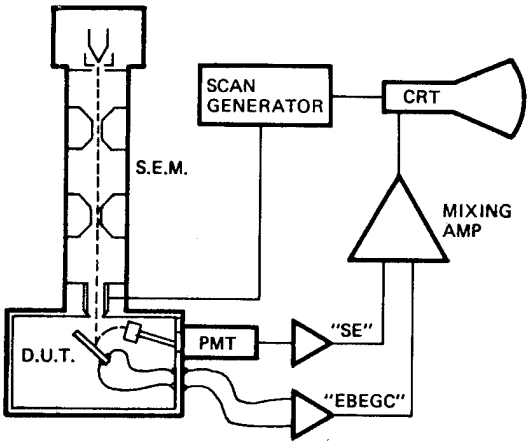


Figure 1. Block Diagram of EBEGC System

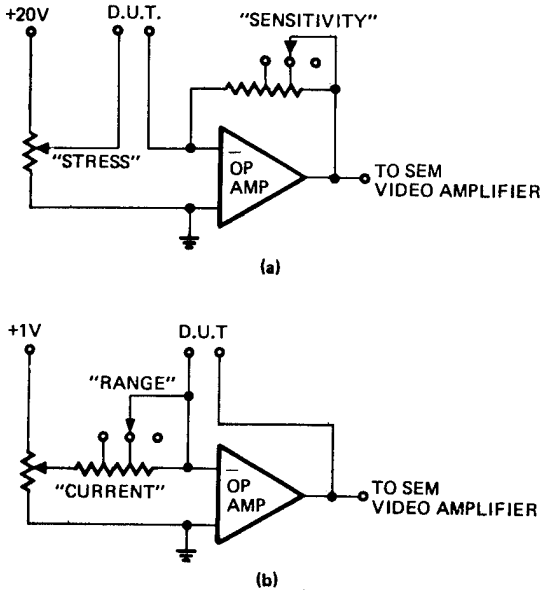


Figure 2. Simplified Circuit of EBEGC Electronics for (a) the Constant Voltage Mode, and (b) the Constant Current Mode

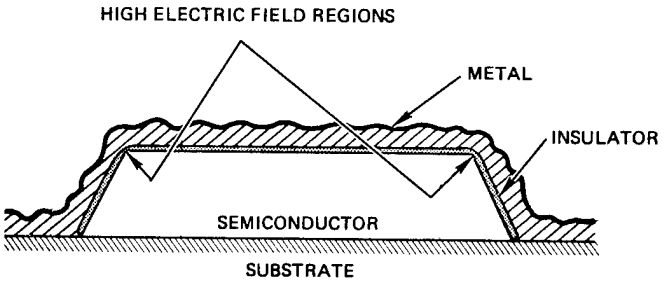
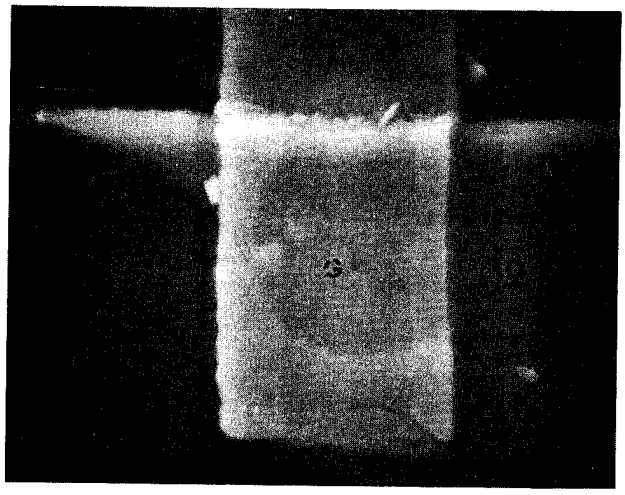
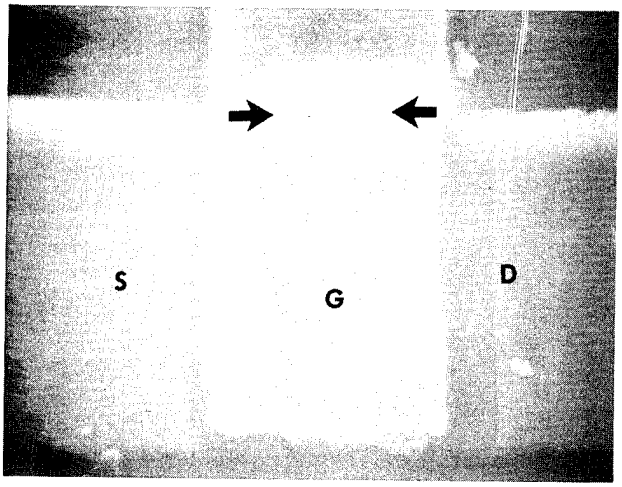


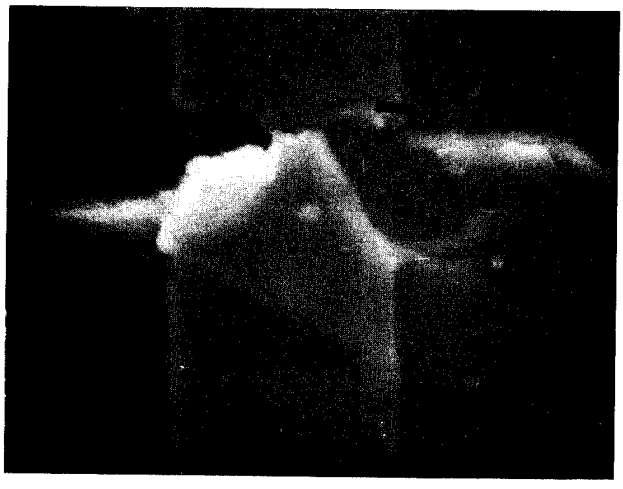
Figure 3. Cross-Section View of the Gate Region of an MIS Transistor on an Insulating Substrate. The high electric field regions in the gate dielectric are as shown.



(a)

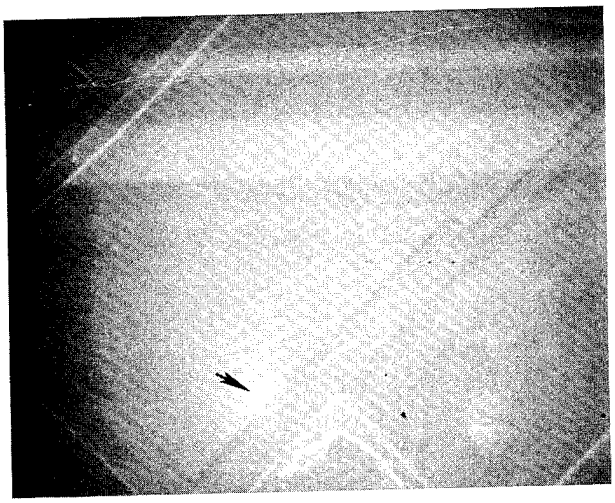


(b)



(c)

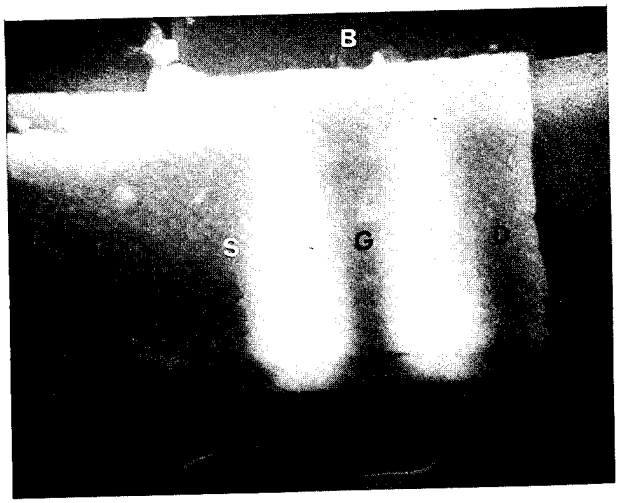
Figure 4. p-MOS/SOS Transistor with Weak Gate Dielectric. (a) Secondary Electron Micrograph of Surface Source, Gate, and Drain are Identified. (b) EBEGC Signal Mixed with Secondary Electron Signal Showing Location of Weak Region. (c) Same Device after Catastrophic Failure of the Gate Dielectric.

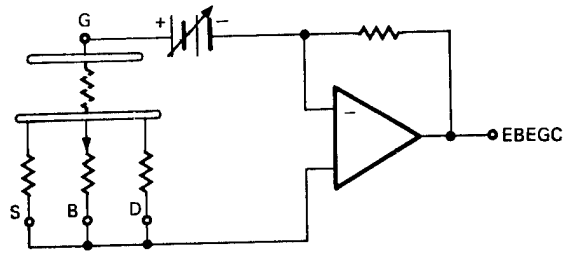


(a)

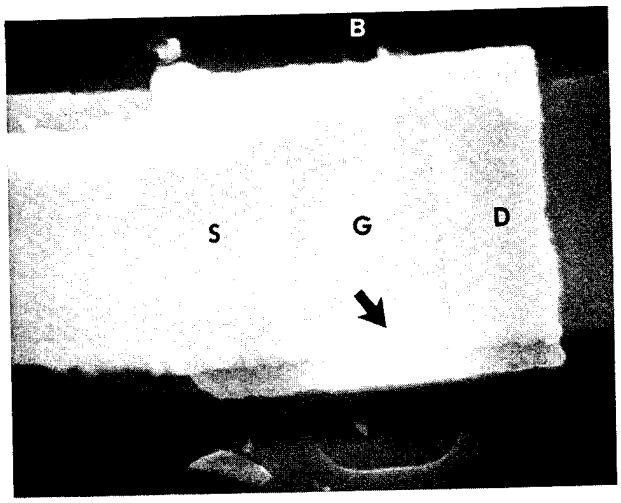
(b)

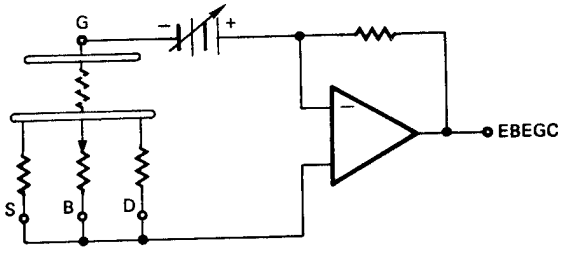
Figure 5. (a) MOS Capacitor with EBEGC and Secondary Electron Signals Indicating Weak Region Near Substrate Contact. (b) The Capacitor after Catastrophic Failure. Energy was Sufficient to Open the Initial Breakdown Area and Induce Secondary Breakdown.





(a)





(b)

Figure 6. p-Channel MNOS/SOS Transistor with (a) Positive Gate Bias, EBEGC Signal is Dominated by Current Induced in Junctions. (b) Negative Gate Bias Eliminates the Junction Currents and Shows High Field Region at Bottom of the Gate Area. The Equivalent Circuit Connection of the Transistors Are Shown in the Insets.

NEW FAILURE ANALYSIS TECHNIQUES FOR BEAM LEAD AND MULTI-LEVEL METAL INTEGRATED CIRCUITS

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ABSTRACT

The ultra-sonic probe was invented to go where conventional probes could never go and to do what conventional probes could never do. Special problems related to "isolation cutting" of titanium-platinum-gold interconnects are essentially eliminated. Electrical node probing through deep insulation glass on multi-level metal I/C's is now possible. In addition, the ultra-sonic probe makes possible a new, fast and accurate technique for measuring oxide thickness over selected circuit components.

Isolation cutting, electrical node probing and glass thickness measurements are all techniques advanced in the "state-of-the-art" with the application of this new, simple, and low cost instrument.

INTRODUCTION

Beam lead devices, or any micro-circuit which employs a hard multi-layer metal system such as titanium-platinum-gold presents special problems to the failure analyst. Due to the hardness of these metals, "isolation cutting" is impossible with a conventional probe. Up to now, laser beams have been the only practical way to isolate these devices. The newly developed "ultra-sonic probe" allows one to accomplish this task effectively without the high capital investment necessary for a laser system. In addition, the probe offers superior performance over conventional probes for failure analysis of multi-level metal circuits (circuits with insulation glass between levels of metal).

For example, first level metal can be buried under 30,000 angstroms of glass on three level metal devices. With this amount of glass present, conventional node probing techniques require substantial needle pressure to "scratch" through the glass and make contact with the metal. A very sharp needle and a great amount of operator skill are required to put the needle on target without disturbing circuitry not under investigation.

Isolation, another valuable analysis technique, is even more difficult to accomplish with conventional probes. Cutting a metal run through 30,000 angstroms of glass can be almost futile.

To sum it up, conventional probing techniques on multi-layer and multi-level metal integrated circuits are, at best, cumbersome and results are often not satisfactory due to undesired circuit damage. In contrast, the "ultra-sonic probe" through its ultrasonic motion gives excellent "target contact" through deep glass, and in addition, it lends itself to cutting hard multi-layer metal systems.

The new probe is also an excellent device for measuring glass thickness over selected circuit components. Through the ultra-sonic scrubbing action of the needle, it is possible to lap a concave hole in the glass down to the pure silicon. Color fringes clearly visible along the outer edges of the subjected area make it possible to measure glass thickness under a microscope by simply counting the fringes for conversion to an oxide thickness table.

ULTRA-SONIC PROBE CONSTRUCTION

Figure 1 shows the probe and its components. Mount a "wirebond transducer" onto a custom designed bracket that allows the transducer to pivot through both horizontal and vertical angles of ± 45 degrees. The bracket should be designed to insure electrical contact between the transducer shank and the bracket mounts. Mount this assembly onto an XYZ micro-manipulator using an appropriate electrical insulator between the bracket and

manipulator. Install a flexible conductor to the bracket for attachment to electrical measurement devices. Replace the "wirebond needle" on the end of the transducer with a custom needle mount. The needle mount should be designed to align the probing needle along a line parallel to the transducer's shank. Connect a compatible ultra-sonic generator with a variable power output control to the transducer. A foot switch should be installed for convenient on-off control.

PROBE APPLICATION

Isolation Cutting

Figures 2 and 3 depict titanium-platinum-gold metal stripes isolated using the ultra-sonic probe. Figure 4 shows a first level metal interconnect cut on a three-level aluminum device.

For best results, maintain the ultra-sonic energy at a minimum effective level and apply slight vertical pressure to the needle. A standard probing needle can be used, provided it extends no more than one-half inch outward from the needle mount. Move the needle back and forth over the run to be cut in either the "X" or "Y" direction (moving in a direction parallel to the direction of the ultra-sonic motion minimizes cut width). The isolation procedure in Figures 2, 3 and 4 required from thirty seconds to one minute to completely isolate the metal systems depicted. Single level aluminum metal can be isolated instantly using this probe (see Figure 5).

Ultra-sonic Node Probing

Electrical node probing through deep insulation glass can be extremely satisfactory provided the ultra-sonic energy to the probe is maintained at a minimum effective level (see Figures 6 & 7). A curve tracer attached between the probe and device substrate will indicate when penetration to the metal is complete.

Oxide Thickness Measurements

Present methods for measuring oxide thicknesses are effective, however, most techniques include cross-section analysis which is slow and costly. The ultra-sonic probe is fast, inexpensive and a very accurate method for determining glass thicknesses over selected circuit components. Applying the ultra-sonic needle to a subject glass area and "scrubbing" a concave hole down to pure silicon displays visible color fringes which can be correlated to glass oxide thickness under a white light microscope (see Figure 8). Course resolution of this technique is approximately 200 angstroms.

Scrubbing the hole is best accomplished by using a blunted needle with a fair amount of pressure and the ultra-sonic energy turned up moderately high. The needle's length from the mount should be extended to over three-fourths inches. This allows for wider needle swing. Under these conditions, manipulator movement in either the "X" or "Y" direction will give the desired scrubbing effect.

SUMMARY

In conclusion, conventional probes are not effective for cutting and probing multi-level metal devices. The ultra-sonic probe overcomes this problem by permitting the probe needle to penetrate through the deep insulation glass. Additionally, the ultra-sonic probe makes possible the cutting of multi-layer hard metal interconnects such as titanium-platinum-gold employed on some single level high reliability devices. Fast, accurate glass thickness measurements over selected circuit components is a bonus application of the probe.

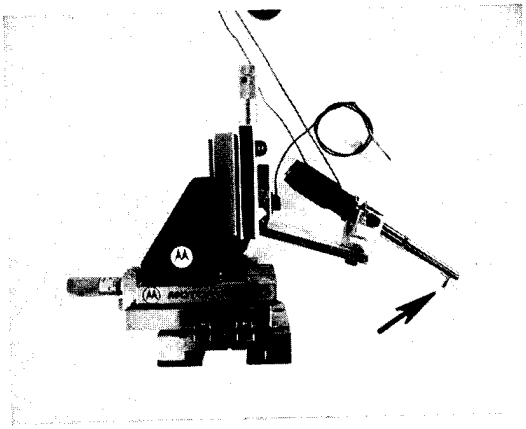

FIGURE 1

Ultrasonic probe is a powerful new tool for integrated circuit failure analysis. (Note mounting attachment for probe needle at end of transducer.)

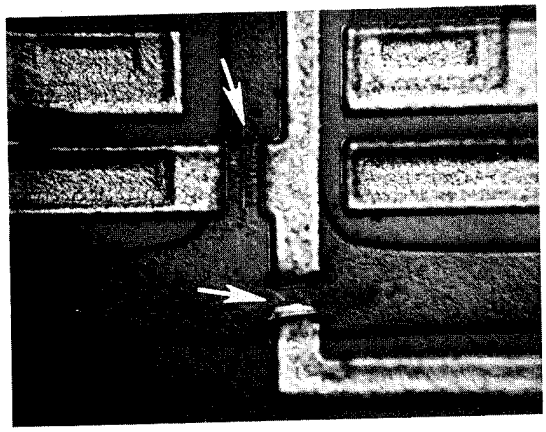

FIGURE 2

Failure analysis is now practical for devices employing the "hard" multi-layer metal systems. Beam lead devices (titanium-platinum-gold interconnects) can be isolated instantly using the ultrasonic probe.

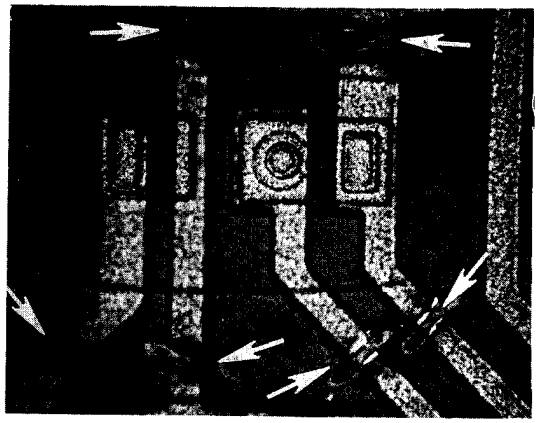

FIGURE 3

This figure depicts a ti-plat metal system and a completely isolated transistor. The ultrasonic action of the needle easily removes the hard titanium and platinum from the cuts.

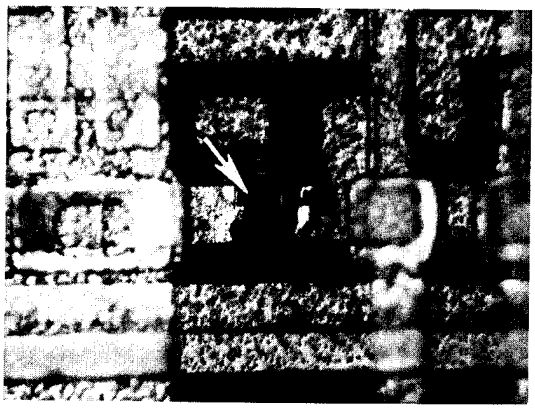

FIGURE 4

Photo shows ultrasonic probe cut on first metal run under 30KÅ of insulation glass. Note cut is in a tight area with no damage to surrounding components (3-level metal device).

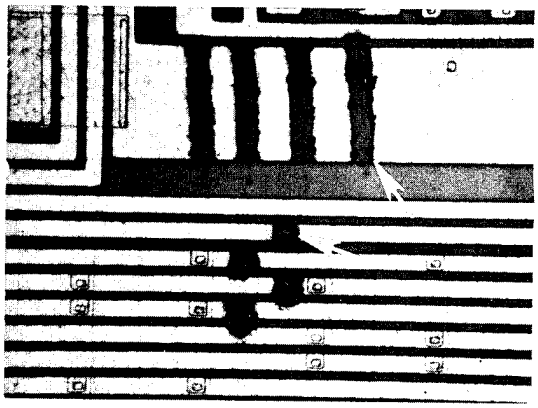

FIGURE 5

Ultrasonic probe is effective for isolation cutting of single level metal. Light needle pressure permits accurate and controllable probe movements.

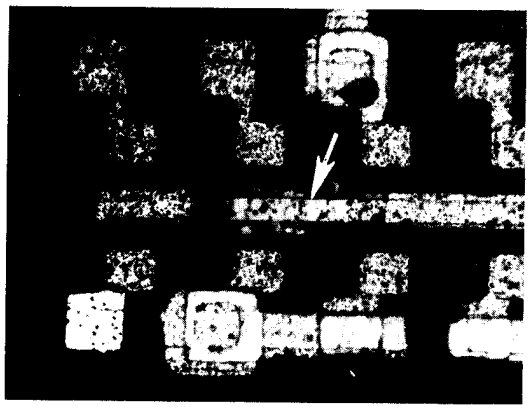

FIGURE 6

Arrow points to subjected area after node probing first metal on a 3-level metal device. Photograph was taken after top metal was removed. No excessive glass damage resulted from application of the ultrasonic energy.

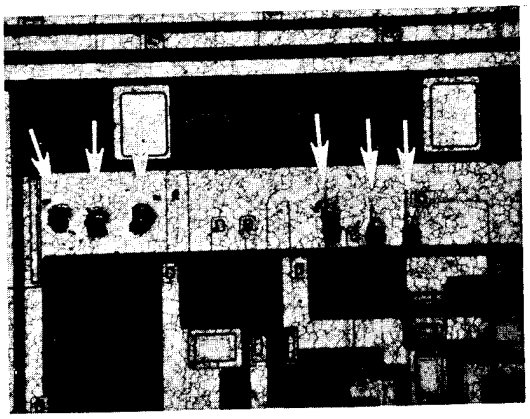

FIGURE 7

Node probing metal through passivation is more effective using ultrasonic energy. The same needle was used to make all 6 probe marks above. The 3 on the left resulted with ultrasonic energy applied, while the 3 on the right resulted without using ultrasonic energy. Note the long probe skid marks at the right which is indicative of poor target contact.

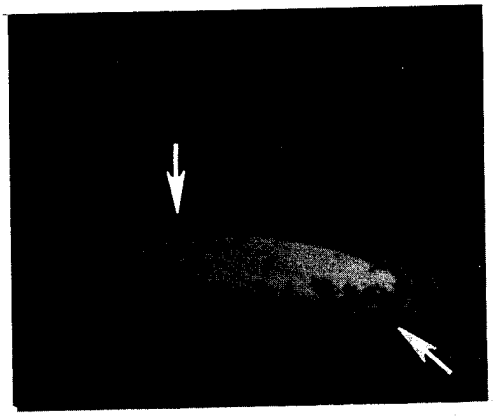

FIGURE 8

Photo shows a die pad area prepared for measuring glass thickness. By combining the color of the "flat" oxide with the number of color fringes, a quick reference to an oxide color chart will reveal the exact thickness.

MICROCIRCUIT PACKAGE GAS ANALYSIS

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ABSTRACT

A method for accurately measuring the ambient gas hermetically sealed within the cavity of microelectronic package is described. Design consideration for the opening chamber are discussed. The type of mass spectrometer and its operation are detailed for those who might be selecting one as a detector. Finally, the pumping system and an automated data analysis system are considered in detail.

Once assembled, the gas analysis system must be accurately calibrated. The various methods used for calibration are discussed, followed by section which relates the analysis results to the assembly and sealing of the microcircuit package.

INTRODUCTION

A search of the literature indicates that as far as could be determined, a documented paper on the design and operation of a package analysis system for measuring the gas ambient of an integrated circuit package is not available. The author has co-authored a paper which discusses the correlation obtained between several analysis systems and pointed out the need to know what was surrounding the chip for the life of the device [1]. More recently the potential and demonstrated deleterious effect of moisture inadvertantly sealed into the microcircuit was presented and will be published this fall [2].

This paper is intended to provide the analyst with detailed information on the design and operation of a gas analysis system. It will also provide information relating to the interpretation of the gas analysis results.

The gas analysis system layout is shown in Fig 1. A detail of the opening chamber is given in Fig 2.

PACKAGE OPENING CHAMBER

In designing a mass spectrometer packaging opening system, a decision must be made as to whether a static sample or dynamic flow technique is to be employed. In the following discussion, the relative merits and disadvantages of the two techniques will be described. Both techniques require a vacuum chamber which can be baked out prior to opening the package. It is essential to remove moisture adhering to the outside surfaces of the microcircuits as well as the walls of the vacuum chamber. The more moisture present as background the more difficult it is to detect small additions (10-100ppm) of moisture to ambient background as the package is opened.

As in any vacuum, the time required to remove moisture from the walls of the system is an exponential function and for low moisture backgrounds, it requires extended bakeout times at elevated temperatures. Typically, the temperature and time are 125°C for 24-48 hrs.

The system must be fabricated from vacuum quality stainless steel with copper gasket seals. Welding of the vacuum assembly must be done from the inside with care taken to remove any scale from the weld and polished to permit inspection for small fissures which could serve as virtual leaks which will increase the time necessary for cleanup after opening the microcircuit package.

All precautions should be taken to insure a completely leak free system. The package opening system shown in Fig 2 allows the mounting of 20 packages of varying types on a circular disk which may be indexed one at a time under the tool steel puncturing pin. A sharpened tool steel needle ground to an included angle of 30° and then case hardened by heat quenching has provided a long lasting puncturing device for both metal and ceramic packages. It is also important to use a bellows drive assembly to obtain an almost burst-free linear motion as a satisfactory method for puncturing the circuit package without damaging the electronic chip. If the bellows assembly threads are well lubricated with a high temperature molysulfide grease, it will permit the operator a feel for when the package lid has been encountered.

Details of the indexing ratchet mechanism are not shown in the assembly drawing. The package opening chamber has a non-contaminating metal diaphragm pressure sensor for giving a positive indication that the hermetic seal has been broken and may also be used to give a relative indication of the absolute quantity of gas present in the cavity Since each package is opened into the same volume, it is only necessary to know the volume of the inside of the package and the opening pressure rise in order to calculate the number of micrograms of each component present in the cavity. The theoretical pressure inside the package can be obtained if the seal temperature is known and the gas is assumed to be 100% N_2. The presence of condensible species such as water and freon or adsorptive species such as carbon dioxide, or reactive species such as oxygen make these absolute measurements only good approximations. However, the reporting of the contents of the package by % volume/volume is quite adequate for failure analysis requirements, providing the analyst recognizes the volume/volume results obtained on packages that have only small residual quantities of gas may be very inaccurate since the relative percent of a small quantity of gas may be greatly influenced by background gases and random fluctuations present in every vacuum system.

The package opening system should also provide a method of venting to the atmosphere as well as evacuating quickly after loading. An important feature of the roughing system is that it be oil free.

A well trapped mechanical pump is adequate, however, a turbomolecular pump is nearly ideal since it may be operated for short times at atmospheric pressure and at the same time possesses an ultimate vacuum of 10^{-9} torr. If the turbo pump is used only for roughing, it is not necessary to heat the line from the opener to the turbo pump as long as the roughing valve is located within the heated oven. The oven is also a critical part of the package opener. If cooler areas are present around the opening chamber, vacuum valves or connecting tubing, these surfaces will act as cryogenic pumps. The more condensible species, such as oils and moisture are trapped and do not exit along with the not so easily condensed species such as nitrogen, oxygen and hydrogen. It is therefore necessary to heat the opening chamber and control valves uniformly. This may be done with heating tapes wrapped with insulation and aluminum foil. A better method which produces more uniform results is obtained by installing the complete opener, pressure sensor, vacuum valves and ballast chamber inside a circulating air bakeout oven. The temperature of the oven is a compromise between the minimum temperature needed to desorb all specie quickly and a maximum temperature that will inhibit chemical reactions which alter the gas constitutents before they have a chance to be detected. One hundred degrees centigrade is indeed a satisfactory but non-ideal compromise since moisture is still slow to desorb from the walls of the system and yet oxygen reacts quickly with copper o-rings and the chrome in the stainless steel at this temperature.

Another important feature of the system is the method of obtaining a pressure drop from the opening chamber to the mass spectrometer. One might be tempted to use a leak valve to control the pressure, as in the static sampling method. Although this seems logical, it presents a major difficulty in allowing the equal sampling of the moisture and other gases at the same time. Moisture is selectively retained in the package opener by the separating action of the leak valve. For small packages, 1/4 x 1/4" flat packs and dual-in-line packages, a package opener volume of 1 liter connected to the mass spectrometer through a 3' long 3/8" diameter stainless steel line gives the proper pressure drop in the opener so that the gas may be sampled under dynamic flow conditions without the use of a leak valve. The added advantage of this method is that it allows an accurate way to determine the opener background gases without changing the system conductance. Since not all of the specie leave the punctured package at the same rate, see Fig 3, it is important to sum the components during the dynamic flow pump out period. Another phenomena has been observed which was somewhat distressing at first (Fig 4). The moisture peak detected by the mass spectrometer after opening is sometimes less than the background value determined before opening. The amount of depression depends on the amount of moisture in the background compared to the moisture in the package. A plausible explanation considers the decrease in the outgassing of moisture from the walls of the opener as the total pressure inside the opening chamber rises by many orders of magnitude after opening the package. The proper measuring pressure is important as will be seen later. Ideally, for larger volume packages, it would be desirable to non-selectively pump away excess gas and then measure the remaining gas without the use of a leak valve. Some range extension can be obtain through the use of an evacuated, clean ballast tank. The removal of a portion of the excess gas by the use of a vacumm pump is not feasible since the pump will not remove each of the gas components equally. For the very large package, there is no alternative but to sample the gas through a pressure reducing orifice or valve that has been calibrated and corrected for the unequal sampling rate. This involves inserting a large package with known water content and determining the loss ratio for moisture.

MASS SPECTROMETER

There are several types of mass spectrometers which may be employed as detectors in gas analysis systems. Quadrupole mass filters have recently been developed to a point that they have sufficient sensitivity and resolution to take advantage of their lower cost and smaller size. While several laboratories are using the magnetic sector spectrometers, it is difficult to justify the higher cost even though the resolution is much better than the quadrupole. If one has a magnetic sector instrument with a helium separator, it is feasible to attach a package puncturing device to the separator making it an ideal way to measure gas in large packages. For the smaller microcircuits, it is advisable to utilize the direct dynamic flow sampling technique described earlier.

A mass range of 2-100 m/e (mass to charge ratio) is sufficient for a failure analysis system with maybe an optional extension in mass to 250 m/e if one is interested in organic solvent identification.

Some problems should be pointed out in the electron multiplier detectors used with quadrupole instruments. The 14 stage beryllium copper detectors degrade quickly with use. Typically, the gain in our multiplier drops from 10^6 to 10^4 during several months use. However, the noise background becomes extremely good, normally less than 2 mv at 3 KV and the multiplier remains relatively stable for the duration of its life. Sensitivity factors for the various specieschange quite dramatically after exposure of the multiplier to air. Daily calibration is therefore recommended. One other problem was found with the beryllium copper multiplier and that is the non-linearity in gain for pressures of greater than 10^{-5} torr. This change in gain is temporary,recovering in a matter of seconds. The thin film detectors, while more stable over the life of the multiplier, have a pressure overload change in gain which may take several minutes to recover. In the case of package analysis this would extend over the entire sampling period and hence make an accurate analysis impossible. The physical basis for this instability has not been experimentally verified. Since the short term gain loss is liveable, the beryllium-copper multiplier is recommended for use in gas analyzers which see large changes in pressure during the opening process. Some of the non-linearities observed at high pressures (10^{-5} torr range) are due to the measurable change in ionization cross section of the various gases, their isotopes, and multiply-ionized fragments.

One method utilized to increase the dynamic range of a gas analysis system is to let the major peak, such as the nitrogen molecule at mass 28 saturate, and then measure an isotope at mass 29 which has a stable ratio to mass 28. One can gain almost two orders of magnitude dynamic range by using this technique. One should not use mass 14, however, since the raio of this doubly ionized molecule of nitrogen to mass 28 is very pressure sensitive making quantitative analysis impossible.

PUMPING SYSTEM

An ideal pump would remove all gas species equally from atmospheric pressure to ultra-high vacuum quickly without generating any contamination of its own. Unfortunately, there are not any pumps with such characteristics and therefore a compromise is in order. The turbomolecular pump is well suited for roughing out the system after loading since it does pump from atmospheric pressure to an ultra high vacuum with contaminant removal enhanced by a pumping speed which increases as the mass of the molecule becomes larger. It is therefore highly recommended as a roughing and clean up pump. The mass spectrometer should be pumped by a separate high capacity pump. In this case, it may be a toss up between an ion pump and the turbo pump. The ion pump is particularly well suited as a non-contaminating pump for holding the mass spectrometer at low pressures when the opener is not in use. It does have several drawbacks. Most ion pumps have titanium sublimators which assist in pumping noble gases. Trapped gases buried under the titanium layer will regurgitate during pressure changes. These bursts are indistinguishable from the gas coming from the opener. This difficiency may be satisfactorily overcome by limiting the conductance between the pump and the mass spectrometer so that back diffusion of regurgitated species is more difficult while at the same time equalizing the pumping speeds for hydrogen, oxygen, and argon with repect to nitrogen. The ion pump has the additional advantage over the turbopump in that it will maintain a high vacuum in the mass spectrometer even though power is lost for several hours. This can be accomplished with the turbopump but not without the considerable expense of purchasing an electrically operated vacuum shutoff valve.

COMPUTER ANALYSIS SYSTEM

While manual analysis of mass spectra for package analysis is possible, it is very tedious, time consuming and error prone. In addition, one would have to accept an accuracy of no better than 10%. Utilizing computer automation, accuracies of .1% have been routinely obtained. The computer system to be described was designed to take data on-the-fly, have a sensitivity of 10 ppm, an accuracy of .1%, require no operator interpretation or manipulation, and permit a high throughput of packages during analysis. It is limited in analysis since it cannot reduce spectra which have overlapping fragments. For the common species found in microcircuit packages, this compromise has proven satisfactory. The addition of spectrum stripping software to the system would increase the cost of the system by some 10% and it was not seen as cost effective. Many trade-offs can be made. With the advent of microprocessors, it is likely that the data handling will become more cost effective. Trade-offs which need to be made because of cost limitations will be pointed out during the discussion which follows.

The computer system consists of a control station at the mass spectrometer to start and stop the data taking. Data is fed into the computer on two low noise coax cables. The computer interface consists of an inverter for the mass intensity signal, and a multiplexer for combining the data into mass peak, and mass number pairs. The multiplexed analog data is then converting to a digital value by a high speed A/D converter, concerting on command at a clock rate of 17 KHz or one data point every 33 μ sec. The paired digital data is then stored on-the-fly into two core data buffers which operate in a tail chasing mode via the direct memory access channel on the 32K core memory. As one buffer fills with data pairs, another buffer previously filled with data pairs from an earlier portion of the spectra is being analyzed by a level one software program. The level one software first averages eight raw data points and stores the result in a separate core buffer and then looks at the averaged data for the start of the sweep, establishes a baseline value for analog spectra, determines when a peak is approaching by an up parameter measurement, verifies that a peak has passed by a down parameter check, determines the peak center and then digitally averages the data at the top of the peak.

To overcome non-linearities in the ramp voltages of the quadrupole, the level one program will generate its own ramp voltage-mass number by an operator initiated calibration procedure. Once this calibration has been accomplished, the level one program will report out the spectra upon demand after the one second data taking interval. The mass intensity for each peak is in millivolts and the mass number is in tenths of mass units. The level one program was purchased from the mass spectrometer manufacturer.

A level two program processes the raw data following the dynamic flow analysis period. Background components are determined by averaging ten scans of data immediately prior to opening each package. After opening, the computer then integrates the pump out curve for each specie. The total integrated intensity for each specie is then multiplied by the relative sensitivity factor for that specie. The relative percent by volume of each specie can then be computed by taking the ratio of the sensitivity corrected data for each specie to the total summed intensity of all species.

CALIBRATION

One of the most difficult tasks in making a gas analysis facility operational is the development of an accurate and reproducible calibration system. The major problem is associated with the difficulty in maintaining the calibration source integrity from the mixing container, usually at or above atmospheric pressure, during the pressure drop into the mass spectrometer which normally operates at pressure of 10^{-5} torr and lower.

For the gases such as nitrogen, hydrogen, oxygen, and carbon dioxide, a simple leak valve using a pressure regulator on a research grade mixture of gases works satisfactorily if several precautions are taken. A dynamic flow of calibration gas should be established. This method will assure that the walls of the vacuum chamber will come to equilibrium with the flowing gas. Holding-chambers at elevated temperatures are to be avoided. Especially in the case of oxygen which will react quickly with the chamber walls during the time the source mixture is being analyzed. It is also recommended that mixture ratios of 10% or greater be utilized to insure that the walls of the system will quickly come into dynamic equilibrium. If the mixture ratio is less than 1% it can sometimes take hours to establish equilibrium. The above comments are particularly pertinent to oxygen. The dynamic flow technique also has the advantage of minimizing background effects. In a static system one must accurately determine the outgassing rate for each specie and make corrections for the contribution of species coming from the walls of the system. This is not necessary if a constant source of calibration gas is supplied to the analyzer.

Another precaution should be mentioned. Depending on the pumping system being used, a method for equalizing the pumping rate should be employed. This can be a fixed orifice in the pump port or a partially closed gate valve. Hydrogen when pumped by ion pumps containing titanium sublimators has a highly variable pumping speed depending on the partial pressure of hydrogen and the history of previously buried gas species. A 10% hydrogen mixture in nitrogen, leaked into the ion pump for short periods of time at pressures no greater than 10^{-7} torr is sufficient to determine the relative sensitivity factor for hydrogen.

The same precautions apply to argon, helium and neon, with the added warning that ion pumping speeds for these gases are much lower, increasing the chance of overloading the pump and making an accurate calibration impossible. To avoid overloading the pump, a mixture ratio of 1% is adequate for the noble gases.

If a diffusion pump or a turbomolecular pump is used in place of the ion pump the same comments made on flow equilibrium apply. The selective pumping and overloading effects are still present but not as critical as for the ion pump system.

The most difficult specie to calibrate accurately, is the moisture. Moisture leaked into the mass spectrometer from atmospheric pressure is adsorbed by the dehydrated walls of the vacuum chamber. It is therefore very important to assure that the walls are brought to equilibrium, and that a dynamic flow of the moisture mixture is maintained. This is illustrated graphically in Fig 5. The difference between moisture and the previously mentioned gases is that the sticking coefficient for moisture is orders of magnitude higher. The net result is that once you have calibrated your system for moisture you have also negated any cleanup bakeout done in preparation for package analysis. Several investigators using this technique perform the calibration for moisture after the packages have been analyzed. While useful on a manually computed analysis, it will not work on the real-time automated system.

For the automated system, a molecular beam generation system was developed. Gas at atmospheric pressure is expanded into a 3 stage differentially pumped system forming a true sample at reduced pressure. The design and operation of this system is beyond the scope of this paper. An internal report describing the system is available from the author upon request. (DE-69-2)

INTERPRETING THE GAS ANALYSIS RESULTS

The interpretation of data obtained by the gas analysis of package ambients is quite complex.

To begin such a discussion, it is necessary to consider possible reactions which may proceed at the elevated bakeout temperature of 100°C.

1. Outgassing can occur from the materials within the package.
   a. Glass sealing frit outgasses moisture and carbon dioxide.
   b. Gold plating outgasses hydrogen.
   c. Die attach organics outgas water and organic solvents such as xylene.
2. Kovar reacts with oxygen.
3. Oxygen will react with the sealing frit and the ceramic cases.
4. Moisture will react with the aluminum or other metals present within the cavity.

Therefore, the gas ambient of the package is not a static system and it is quite likely that many changes have taken place since the package was sealed. Of course, if the package had been sealed with 99.9% nitrogen, few of the reactions would have occurred.

One of the most dramatic changes which occurs in the package ambient takes place immediately after seal. If the seal is made in dry nitrogen (5 ppm moisture) and parts are used which have not been baked out, the ambient in the package changes from 5 ppm to 5000 ppm moisture within a matter of seconds. This desorption of moisture from the ceramic or metal parts continues for several days reaching moisture contents greater than 15,000 ppm even though the package was sealed in a dry atmosphere. This effect has been observed by mass spectrometry analysis as well as direct measurement by the use of miniature moisture sensors [3]. This simple effect and the widespread use of unbaked parts has contributed greatly to the high incidence of moisture activated integrated circuit failures.

The outgassing of moisture from the interior walls of the package also affects the interpretation of the reported moisture content, since the mass spectrometer cannot distinguish between the moisture which was in the vapor state at the moment of opening the package, and the moisture which desorbs from the package walls after opening. It is fair to say that the reported moisture at 100°C is always greater than the amount actually in the ambient. This fact becomes important if one wants to relate the measured moisture back to the dew point. To calculate the dew point, several assumptions are required. One, is that all the moisture in an enclosed volume must remain in the vapor state since dew point concerns only the molecules of moisture in a volume of gas. It has nothing to do with the container in which it is stored. Therefore, if one cools this volume of gas, the dew point is reached when the moisture molecules can no longer all remain in the vapor state. At this point, liquid water forms. However, in the process of cooling a package containing moisture, some of the moisture is adsorbed on the walls of the package. Thus, the point at which the liquid water forms inside the package is always lower than the dew point calculated from the relative percent moisture at 100°C. This depression is dependent on the percent of ambient adsorbed moisture which is related to the wall material, the rate at which the package is cooled and the total quantity of moisture present within the cavity in relation to surface area. As an example, see Fig 6, if a package has 1.5% moisture at 100°C in the ambient within a small cerdip cavity, it takes only a small percentage of the ambient water to bring the walls to equilibrium at 25°C, therefore, the correction for the dew point under these conditions is only several degrees centigrade. However, if 500 ppm moisture were present in the same size package ambient at 100°C, it would take almost 95% of that ambient moisture to satisfy equilibrium conditions at 25°C. The dew point would then drop from -27°C to -55°C. A rather drastic depression to say the least. This discussion illustrates the problem of trying to relate relative percent moisture to dew point in a closed container whose walls are being cooled and adsorbing moisture from the ambient.

Once the secondary reactions which are going on inside the package are defined, it is possible to understand the relation of moisture to the activation of failure mechanisms. Fig 7 is a nomograph which converts parts per million moisture to dew point at constant pressure. It does not take into account moisture removed from the ambient by the walls of the package. If one neglects this adsorbed moisture, the

nomograph indicates that packages containing less than 6000 ppm (0.6%) moisture will not condense a liquid, since the dew point is below 0°C. If the measured moisture content is 500 ppm, the frost point is -27°C. At this point, few chemical reactions occur and the absolute quantity of moisture present is very small. Although it is difficult to prove experimentally, the amount of adsorbed moisture present on the semiconductor chip is probably insufficient to provide any significant ionic mobility.

Other conclusions can be drawn from relating other species appearing in the package with moisture. A 5-10% volume of hydrogen may indicate that an electrolytic reaction has taken place within the cavity. Higher hydrogen content points to intentionally filling the package with a reducing atmosphere.

Trace quantitites of helium (<500 ppm) indicate a fine leak below the detectability limit of the helium leak detection apparatus and may indicate a marginal seal. Quantities of FC-78 (Gross Leak Test Fluid) are strong evidence of a temperature activated gross leak which may not have been detected during gross leak tests. The presence of 1% argon indicates the leakage of air into the dry box, the sealing furnace, or a fine leak which has allowed the package to equilibrate with its environment. Oxygen present within the cavity unless greater than 25% is usally not a good indicator since it reacts with many materials. Large quantities of oxygen are probably intentionally added to the ambient at the time of seal to keep the lead in the sealing glass in an oxidized state. Carbon dioxide is very often found in ceramic packages in the range of 1-5% and is associated with the glass sealing reaction, or outgassing from the ceramic.

In blind tests, it has been possible to determine whether liquid N_2 or bottled N_2 gas was used on off shore assembly plants by accurately measuring trace quantities of argon present in the nitrogen. It has also been possible to separate a group of devices into respective date codes by noting small changes in the mass spectra fingerprint.

Trace quantities of organics are difficult to identify if the mass range is limited to 2-100 m/e. However, if one knows that a particular organic solvent such as xylene might be present, it is relatively easy to match the strip chart of the unknown with a small sampling of the suspect solvent.

CONCLUSIONS

A gas analysis system has been described which can be used to monitor the performance of a sealing system, or provide the failure analyst with critical data on the ambient surrounding the electronic chip. Problems involved in the design, calibration, and operation of the system were discussed with suggested trade-offs and possible consequences.

The establishment and operation of accurate gas analysis facilities in the analytical service companies and microelectronic industry will provide a means for eliminating one of the major factors blocking the realization of failure free electronics. We have come a long way in solid state electronics, but the electron tube manufacturers provided a cleaner working ambient.

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[1] D. E. Meyer and R. W. Thomas, "Moisture in SC Packages," Solid State Technology, Sept 1974, pp 56-59.

[2] R. W. Thomas, "Moisture Myths and Microcircuits," IEEE Transactions Parts, Hybrids, and Packaging, Sept 1976.

[3] V. Cordasco, "Control of Microcircuit Contamination," RADC-TR-75-317, Final Technical Report AF30602-74-C-0203, March 1976.

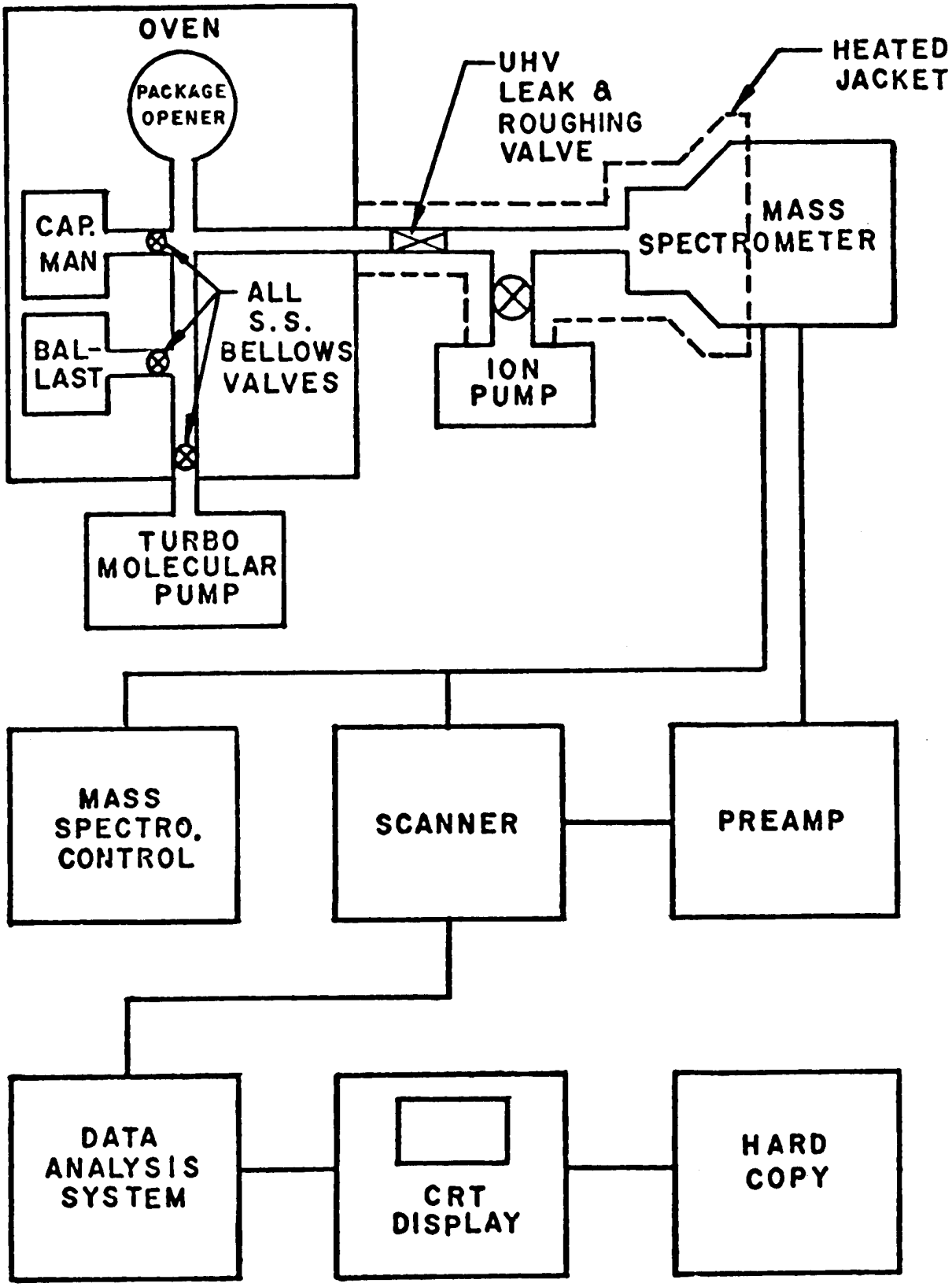


FIG. 1. I.C. GAS ANALYSIS SYSTEM

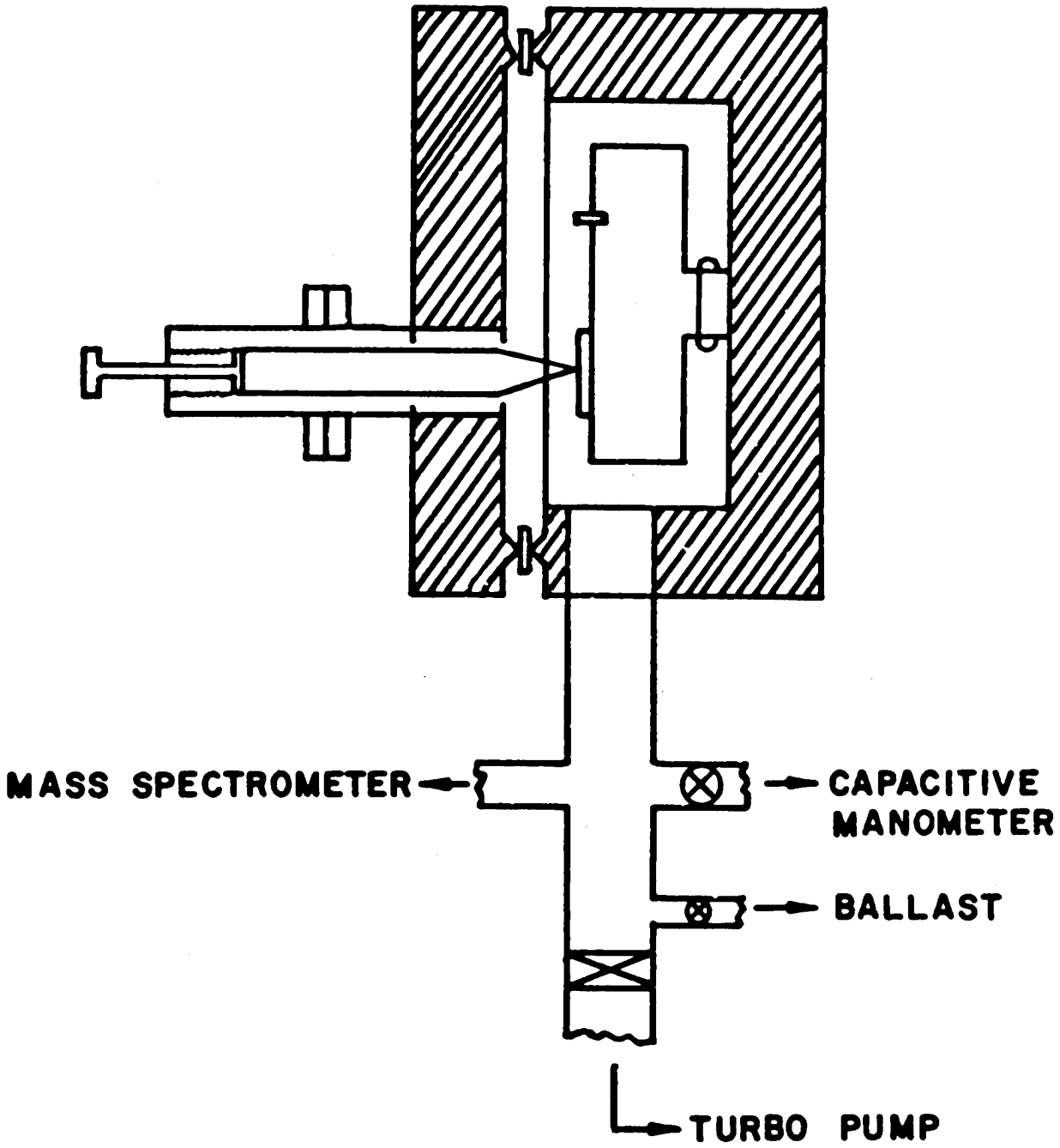


FIG. 2. PACKAGE OPENER

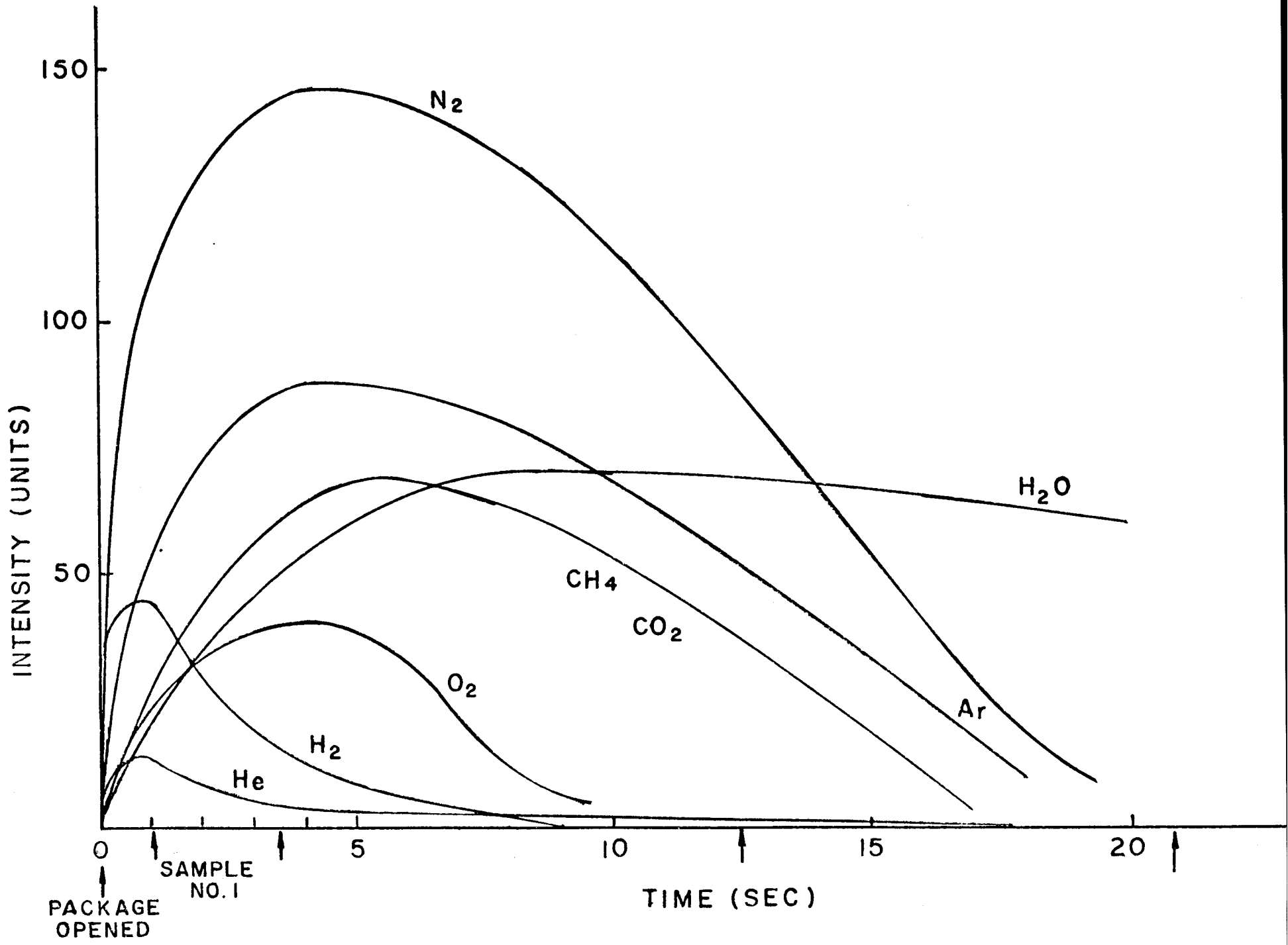
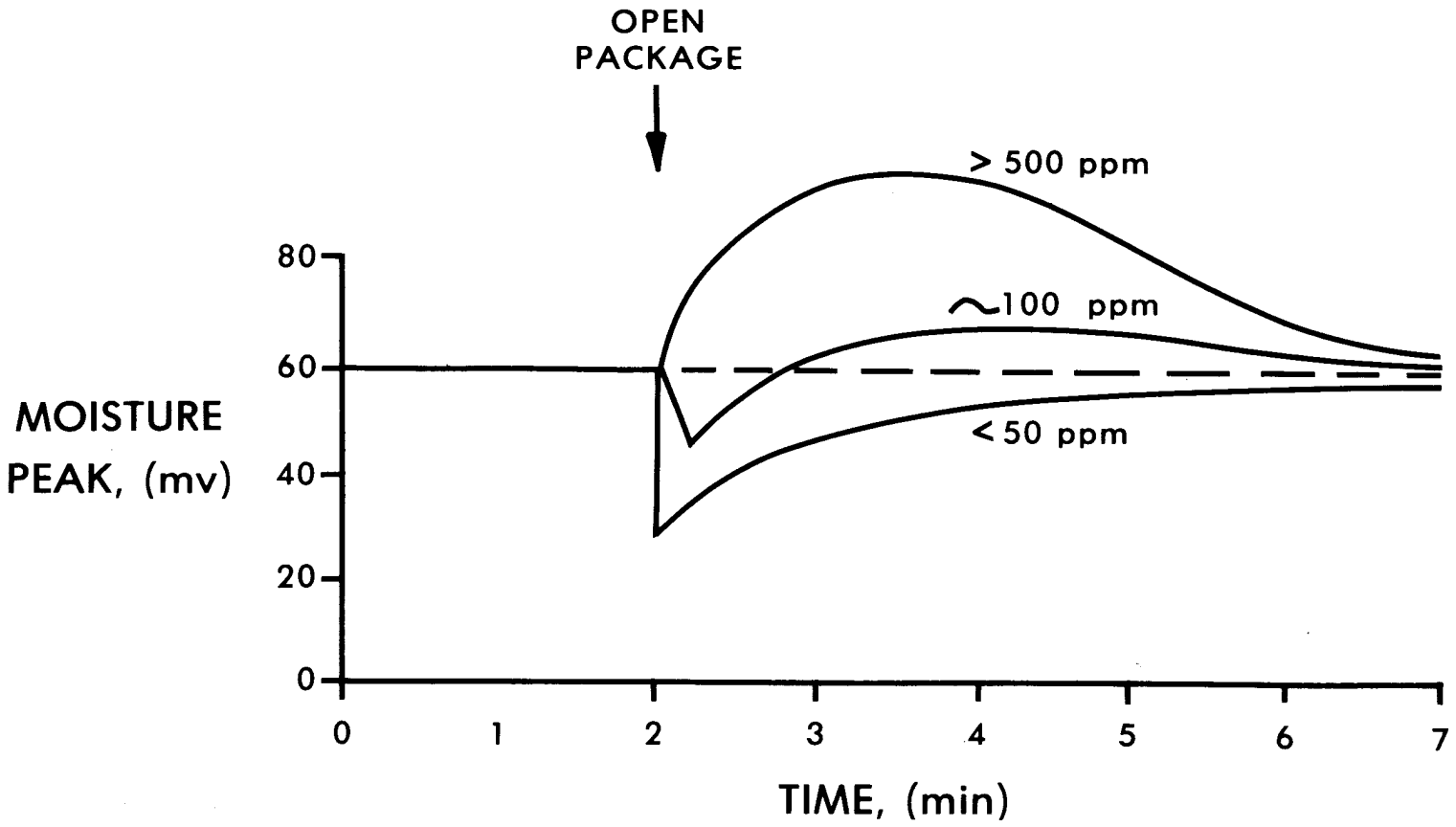
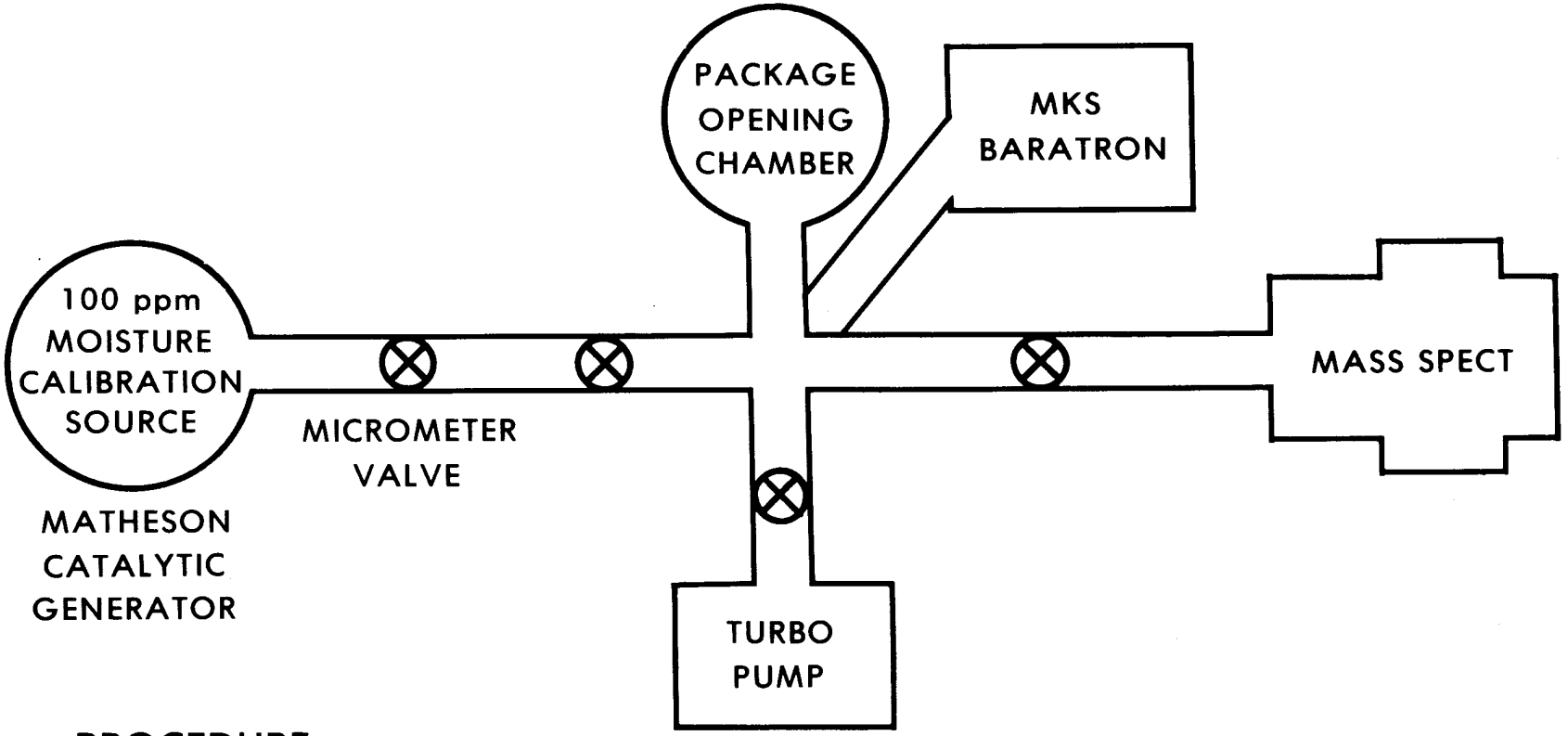

150
100
50
INTENSITY (UNITS)
N2
H2O
CH4
CO2
O2
Ar
H2
He
0
5
10
15
20
SAMPLE NO. 1
PACKAGE OPENED
TIME (SEC)

FIGURE 3



BACKGROUND DEPRESSION vs PACKAGE MOISTURE CONTENT

FIGURE 4



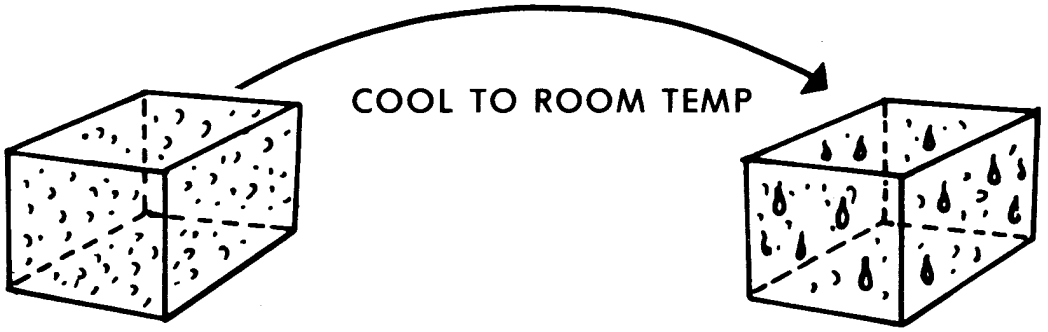
PROCEDURE:

- LEAK IN SOURCE AFTER EVACUATION — — — — — 100 ppm MOISTURE NOT DETECTABLE
- LEAK IN SOURCE SLOW RATE WHILE PUMPING (5 min) — — 100 ppm MOISTURE NOT DETECTABLE
- LEAK IN SOURCE HIGH RATE WHILE PUMPING (30 min) — — 80 ppm DETECTED

FIGURE 5

THEORETICAL ASSUMPTIONS

1. VOLUME .01cc
2. ISOTHERM DATA FOR Au
3. PACKAGE HERMETICALLY SEALED
4. Au WALLS



100°C

MOISTURE VAPOR STATE

500 ppm

DEW POINT= -27°C

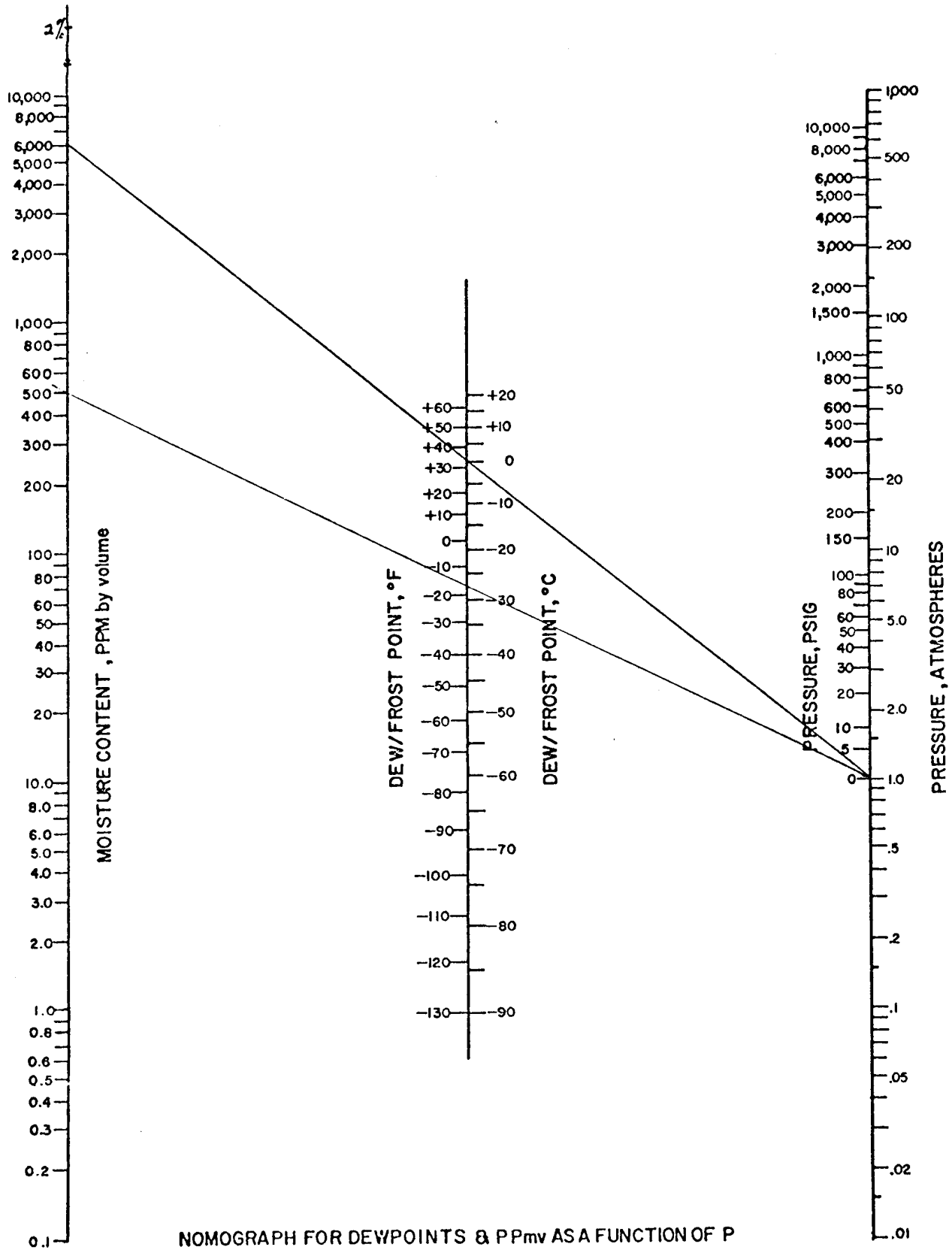
25°C

MOISTURE IN VAPOR STATE

22 ppm

DEW POINT= -55°C

FIGURE 6



NOMOGRAPH FOR DEWPOINTS & PPmv AS A FUNCTION OF P

FIGURE 7

SURFACE ANALYSIS BY ISS AND SIMS

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ABSTRACT

Two surface analysis techniques utilizing ion beams, Ion Scattering Spectrometry (ISS) and Secondary Ion Mass Spectrometry (SIMS) will be discussed. These techniques use a low-energy (1-5 keV) noble gas ion beam to determine elemental and chemical surface analysis of a wide variety of materials. Both ISS and SIMS are sensitive to the first monolayer of atoms. This, combined with charge neutralization to prevent beam wander, surface electric fields, etc., provide for composition depth profiles with monolayer resolution on such materials as glasses, semiconductors, and polymeric coatings.[1] The use of recently developed ion guns to generate high-brightness, small-diameter ion beams allows imaging ISS and SIMS analysis for applications requiring high spatial resolution. Principles of the technique as well as several illustrative examples of ISS and SIMS surface analysis will be presented.[2]

References

1. See, for instance, William L. Harrington, "Low Energy Ion Scattering Spectrometry Studies of Si, SiO_2, and Related Materials"
NBS Special Publication 400-23
ARPA/NBS Workshop IV
Surface Analysis for Silicon Devices, held at Gaithersburg, Maryland, April 23-24, 1975

2. To receive copies of recent publications and applications notes on the use of ISS and SIMS for Surface Analysis, or if interested in receiving a bibliography on the subject, please write directly to the author.
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HIGH SPATIAL RESOLUTION AUGER ELECTRON SPECTROSCOPY (AES) IN A DIFFUSION-PUMPED SEM

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Summary

High spatial resolution Auger electron spectroscopy in an SEM is presented, and aspects of vacuum requirements for AES in a diffusion-pumped SEM are discussed.

The vacuum system of a Cambridge Stereoscan* was rebuilt. Auger spectra recorded after 45 minutes of electron bombardment demonstrated that the carbon buildup due to the polymerization of hydrocarbon molecules can be prevented by using the gas-jet technique. Auger data taken in an unmodified Cambridge Stereoscan, using only the gas-jet technique, is also presented.

The spatial resolution of the SEM operating in the Auger mode is a function of necessary beam current, lens aberrations, and gun brightness. In the existing SEM equipped with a LaB_6 electron gun, beam diameters of 0.4 μm containing 4×10^{-7} A at 20 kV were obtained. This allowed the recording of greyscale Auger images with less than 0.5 μm spatial resolution in 400 sec.

An SEM-Auger technique for determining the composition profiles of thin films (> 1000 Å thick) is described. The technique makes use of the small escape depth of Auger electrons combined with the magnification of cross sections obtained by angle sectioning.

The method is illustrated in the determination of a composition profile of the phosphorus concentration in an SiO_2 layer deposited on a single-crystal silicon substrate.

To examine the effectiveness of an RF sputter-cleaning process on small via holes, SEM-Auger spectroscopy showed the removal of carbon and fluorine residue left behind from a previous chemical-etching step. However, Auger spectra taken after RF cleaning indicated the presence of silicon, suggesting sputter deposition of silicon during RF cleaning.

*Trademark of Cambridge Instrument Company, Inc.

THE USE OF HIGH ENERGY ION BEAMS FOR SURFACE AND THIN FILM ANALYSIS

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Introduction

The object of this brief review is to introduce the subject of surface and thin film analysis by the use of high energy ion beams. This field has grown considerably in recent years and there is a large literature concerning both techniques and applications. References will be given which illustrate both principles and applications. The principal technique is that of Rutherford backscattering, and we will only cursorily touch upon the other techniques such as ion induced nuclear reactions or ion induced X-rays.

General Principles

Ion scattering experiments[1,2] have been performed at energies which can be classified loosely as high (1-2 MeV), medium (100-400 keV), and low (0.5-10 keV). The low energy regime is the subject of a separate paper at this meeting, and we will not consider it further. Essentially, the technique consists of bombarding a target with a monoenergetic, collimated beam of ions and obtaining an energy spectrum of the particles scattered, typically, through angles greater than 90°. Energy spectra thus obtained may contain information on topics such as surface impurities at tract levels and near surface or thin film compositional profiles. If channeling or blocking techniques are employed information can be obtained on surface disorder or structure.

The scattering events are binary collisions between the ions and individual target atoms and for the high-energy, and generally for the medium-energy, regimes the backscattering is Rutherford in which the bare nuclei of ion and target interact. This makes quantitative interpretation[3] of the scattered yield unusually simple. Moreover the collisions are elastic and this permits simple identification of atoms at a surface by the energy of the backscattered ions. In effect the energy scale becomes a mass scale for target atoms at the surface, with higher energy indicating larger mass.

The ions travel in essentially straight trajectories through the solid until a close collision with a target atom backscatters them. The ion, however, will lose energy to the electrons of the solid during its entrance and emergent path. Since these energy loss rates have been calculated and measured quite accurately, the energy scale of the backscattered spectra can also be used as a depth scale. It is worth emphasizing that compositional depth profiles in thin layers may thus be obtained from a single spectrum without recourse to sputtering.

Choice of the analyzing ion depends on such factors as mass and depth resolution and ^4He particles present the best compromise.

Protons and deuterons will induce nuclear reactions with sizable cross sections in most of the light nuclei for bombarding energies in the vicinity of 1 MeV. Impurities such as B, C, N or O can therefore be detected in the near surface region. Energetic ion beams can also be used to generate characteristic X-rays. This technique with its excellent mass resolution can be combined with Rutherford scattering with its superior depth resolution for surface or thin film analysis.[3]

Applications and Limitations

a) Surface Analysis. The backscattering technique is ideally suited for detecting, for example, heavy mass impurities on Si.[2] Using 2 MeV He ions and solid state detectors the limit of sensitivity for detecting Au on Si will be $\sim 10^{11}$ atoms/cm^2. These limits represent the optimum conditions for impurity detection. Moreover because scattering cross sections are known the absolute number of impurity atoms can be determined without recourse to calibration methods. The limitations are firstly that with solid state detectors the technique is not truly surface sensitive, with depth resolution being $\sim$200 Å. Depth resolution primarily depends on the energy resolution of the detecting or analyzing system and can be improved to $\sim$10-20 Å by use of magnetic or electrostatic analyzers. Little has been done in this area besides demonstrating that such resolution is obtainable. This is probably because of the inherent utility and simplicity of the solid state detectors. The poorer resolution of the surface barrier detectors also causes a loss in mass resolution for the heaviest masses. Moreover it is very difficult to detect light impurities on a heavy substrate as the spectra will be completely dominated by substrate scattering unless channeling is used to reduce the substrate scattering. This problem of course, does not exist with low energy scattering.[4]

Most backscattering configurations employ beam spot sizes of approximately 1 mm in diameter. This defines the lateral resolution of the system and is a definite limitation in many practical applications. Recent work,[5] however, has shown it possible to produce and use MeV ion beams with lateral resolution of several microns.

It has been demonstrated[6] that low energy ion scattering can be useful for surface structure analysis by making use of the shadowing phenomena. Recently, however, it has been shown[7] that high or medium energy ion scattering can be used to investigate such phenomena as surface structure or relaxation by making use of surface channeling or blocking techniques.

b) Thin Film and Near Surface Compositional Profiling. Rutherford backscattering is now widely used as a tool for profiling thin films and near surface regions.[8] Composition profiles can be obtained quantitatively and non-destructively. Virtually all other techniques employ surface sensitive techniques which rely upon sputtering to section the films or surface of interest. Sputtering is destructive but probably a more severe limitation is that sputtering mechanisms in alloys or at interfaces are not understood. Sputter sectioning can, and probably will, change the surface composition of the material under study. The sputter sectioning plus surface techniques, however, possess great advantages in such areas as elemental sensitivity and the best approach to a problem is to combine backscattering with a surface sensitive technique.[9,10]

We will list those areas in which backscattering has made a particular contribution to the understanding of thin film phenomena. (The subject of detection and location of implanted species by energetic ion beams will not be discussed but that historically

is where the field originated.) Several recent conferences[11,12,13] have covered this area and all references are contained there.

1) Insulating Films. Composition and impurity content of such films as Al_2O_3, SiO_2 and Si_3N_4.

2) Metal-Metal Interdiffusion. Profiles in such systems as Al-Au, Cu-Au and Pd-Au.

3) Metal-Semiconductor Reactions. Silicide formation and metal + compound semiconductor reactions.

4) Metal-Dielectric Reactions. Mainly metal-SiO_2 reactions.

5) Solid State Epitaxy. Diffusion and epitaxial growth at interfaces of Si and Ge through metal films.

6) Superconducting Films. Stoichiometric and impurity analysis of such high T_c thin films as Nb_3Ge.

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M.M.E. Beguwala is a Member of the Technical Staff in the Electronics Research Division of Rockwell International. He is engaged in the study of electrical properties of MIS transistors, capacitors and MIS, p-n and Schottky barrier diodes. His present assignment is to study the charge transport, charge storage, the mechanisms responsible for charge retention and device endurance and reliability of MNOS memory devices.

Dr. Beguwala graduated magna cum laude in engineering from the University of California at Los Angeles in June 1967. He received his MS in electrical engineering in February 1969 and his PhD in electrical engineering in January 1975 from the University of Southern California, Los Angeles.

Dr. Beguwala is a member of the IEEE, American Physical Society and the Electrochemical Society. He has also been elected to membership in Sigma Xi, Eta Kappa Nu and Tau Beta Pi honor societies. He has been cited several times on the Dean's List during his academic career. Dr. Beguwala has published papers in the field of charge transport and charge storage in semiconductor junction devices and filed a patent for a novel process to incorporate dopants at the interface of two similar or dissimilar insulators.

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From 1964 to 1972 he was a Member of the Technical Staff at Bell Laboratories, Murray Hill, N.J., where he carried out research and development on solid-state devices. At Bell Laboratories he was a Supervisor in the Semiconductor Device Laboratory from 1966 to 1972, concentrating on the physics and applications of the silicon-silicon dioxide system, including charge-transfer devices. In June 1972 he joined Bell-Northern Research, Ottawa, Ontario, Canada, as Manager of the Electronic Materials and Processes Laboratory, and in November 1973 he was appointed Vice-President, Technical Development, at Microsystems International Limited, Ottawa, Canada. In October 1974 he returned to Bell-Northern Research as Manager, Silicon Technology Laboratory where he is responsible for the development and administration of silicon integrated circuit technology programs for Northern Electric and Bell Canada.

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9 years in Electromechanical Relay Engineering as a designer and as an engineering manager.

3 years in Component Engineering on capacitors, resistors, and other passive components including 2 years as Group Head.

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W.R. Brockhoff holds a B.S. degree in Electrical Engineering from Arizona State University, Tempe, Arizona in 1968. In 1968 he joined Texas Instruments as Quality Assurance Engineer, Minute-Man Program. In 1969 he joined Fairchild Semiconductor as Quality Assurance Engineer, Integrated Circuits. In 1971, he joined Intersil Semiconductor, where he is currently Manager of Reliability. Mr. Brockhoff is a member of the IEEE.

BURNHAM. JOHN

Dr. Burnham with a PhD in Physical Chemistry from Stanford University has more than 35 years experience in components, materials, and processes involving the manufacture of pulseforming networks, capacitors, resistors, magnetics, and mercury batteries. He has been responsible for research programs involving the development of high-voltage insulation, magnet wire insulation, high dielectric constant ceramics, and thin film dielectrics. Before joining Hughes, Dr. Burnham was with Sprague Electric Company for ten years as Assistant Research Director and Chief Engineer, and with Ti-Tal, Inc., for 18 years as President and Chief Engineer, and engineering consultant to General Electric Company, I.T.T., Fansteel Metallurgical Corp., Lenkurt Electric, and Stanford Research Institute.

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He is currently Manager of Reliability for Aerojet ElectroSystems Company, Azusa, Ca. He joined Aerojet-General Corporation in July 1959 and formerly served as a member of the Corporate Reliability Staff, Head of Reliability for the Avionics Division. From 1946 to 1948 he was with RCA, Camden, N.J., as a Quality Engineer and from 1948 to 1959 was with the U.S. Army Signal Supply Agency, Philadelphia, as a Quality Assurance Specialist.

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Dr. Cunningham is presently Vice President Semiconductor Operations at Advance Memory Systems, Inc., Sunnyvale, Ca. This position includes responsibility for Circuit Design, Product and Process Engineering, QA, Production Control, Manufacturing and Plant Facilities for all integrated circuit activities of the company. Dr. Cunningham joined AMS in mid 1974. Dr. Cunningham was formally Vice President, Operations for Cal-Tex Semiconductor, Santa Clara. He held this position for just under two years. Prior to this position, he was with Texas Instrument, Inc., for eleven years in various engineering and management positions. His last assignment was Manager of the Advanced Process Technology Facility in the MOS Department. He has published in Electromechanical Technology, the Journal of Electrochemical Society, Solid State Electronics, Microelectronics and Reliability, the Electronic Engineer, and Electronics. Dr. Cunningham has been granted 17 patents dealing with semiconductor technology and thin film deposition. His education includes Ph.D, M.A. and B.A. degrees in Inorganic Chemistry from the University of Texas.

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From 1962 to 1968, he worked with the Bell Telephone Laboratories in Holmdel, New Jersey and Naperville, Illinois in the area of memory circuit design. In 1968, he joined the System Products Division of IBM in Hopewell Junction, New York where he has been involved with circuit design and device analysis. He is currently working on the electrical design of packaging systems for high speed logic.

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DELANEY, ROBERT H.

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Since joining the IBM System Products Division, East Fishkill, N.Y., in 1969, he has worked in several areas of advanced FET development including silicon gate FET's, high-voltage FET's, and FAMOS devices.

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Mr. Doyle was born on October 26, 1938 in Rome, New York. He received his B.S. degree in Electrical Engineering from the University of Dayton, Ohio, in January 1961, and has additional graduate credits in mathematics and engineering management from Syracuse University, New York. Affiliated with the Rome Air Development Center (RADC), Air Force Systems Command (AFSC) since 1961, he has extensive experience in the area of reliability physics related to failure mechanisms in microelectronic devices, reliability stress testing and MIL-STD-883 screening techniques.

Currently, Mr. Doyle heads the RADC System Support Failure Analysis Activity providing reliability support to Air Force Systems on a quick reaction basis involving advanced device technology evaluations, part field failure analysis and general microcircuit procurement reliability requirements for high-reapplications.

Mr. Doyle is a member of Tau Beta Pi, National Engineering Honor Society, has authored numerous technical reports in the reliability physics field and presented several papers at both national and regional symposiums on selected reliability topics. He was a lecturer at the General Electric Co. Advanced Engineering Course and has given several tutorials in the failure analysis techniques and applications area.

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Bill Fitch is currently the Manager of Motorola Bipolar Integrated Circuit Reliability Engineering, a position he has held since mid-1970. Prior work includes Reliability Engineering on Minuteman II as Minuteman R & QA Program Manager. For most of 1967 and 1968, he was responsible for I/C In-Process Quality Assurance and Failure Analysis.

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Mr. Griffith holds degrees in Physics from Marietta College (Ohio) and the State University of New York. His master's thesis delt with transport properties of soft carbons (graphitizable) at temperatures below 4.2K, and the research toward a PhD dissertation was on the topic of ionization enhanced diffusion using the electron beam technique for measuring variations in minority carrier lifetimes.

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HARMAN, GEORGE

George Harman is a senior research scientist at the National Bureau of Standards. He has an M.S. in physics from the University of Maryland and has been at NBS for 20 years. Earlier, he published a number of papers on such subjects as electroluminescence, and semiconductor contacts. He switched fields to form an NBS bonding group in 1968, when the orientation of his division changed towards problems of the semi-conductor device industry. He has recently published a number of specialized reports on bonding, and given numerous papers on that subject, four of which have been at this conference. In October 1972 he received the Department of Commerce silver medal for work in the field of interconnection bonding. He is a senior member of the IEEE and a member of the American Physical Society, Sigma Pi Sigma, and ISHM.

HEWLETT, FRANK W. JR.

Frank W. Hewlett, Jr. (S'69-M'71) was born in Richmond, Va., on February 4, 1945. He received the B.S. and M.S. degrees in electrical engineering, and after doing research in microelectronics, the Ph.D degree from the University of Florida, Gainesville, in 1966, 1967, and 1971, respectively.

As a member of the Technical Staff of Bell Laboratories, he worked in a computer-aided design group for one year. In 1972 he joined a bipolar silicon integrated circuit group with Bell Laboratories, Allentown, Pa., where he designed the first I^2L chip intended for manufacture at Allentown, and designed and fabricated the Schottky I^2L device. (IEEE Journal of Solid State Circuits, Special Issue on Memory and Logic, October, 1975).

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Ronald W. Jocher is a member of the Mechanical Reliability Group in the Interconnection Technology Laboratory. He holds an associate degree in Electronics Technology from R.C.A. Institutes (1967). He joined Bell Laboratories in 1967, doing work on antenna systems. Present assignments include the design of reliability testing devices and reliability evaluation of printed circuit product.

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Mr. Johnson received his Bachelor's degree from California State University at Fullerton in 1973, and is presently completing his Master's degree including courses in integrated electronics and independent research utilizing scanning microscopy. He has recently co-authored a patent application and publication pertaining to ion-milled Al O and is a member of the Southern California Electron Microscopy Society.

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Dawon Kahng was born on May 4, 1931, in Seoul, Korea. He studied at Seoul University from 1949-1950. After serving with the Korean Marine Corps he returned to Seoul University in 1953 and received the B.Sc. degree in physics in 1955. He was granted the M.Sc. and Ph.D. degrees in electrical engineering from Ohio State University, Columbus, Ohio, in 1956 and 1959, respectively. He became a U.S. citizen in 1964.

While at Ohio State University he was engaged in teaching as well as in the study of diffusion of impurities into silicon through a growing oxide layer. He joined Bell Laboratories, Murray Hill, in October 1959, and worked on feasibility studies of MOS transistors and hot electron devices, and on silicon epitaxial film doping profile studies. Since 1964 he has been supervising groups concerned with the development of Schottky barrier high-frequency diodes, studies of large gap and ferroelectric semiconductors, luminescence in the visible and charge coupled devices. More recently, he has been concerned with development of nonvolatile semiconductor memories and associated silicon tegrated circuits.

Dr. Kahng is a member of Sigma Xi and Pi Mu Epsilon. He is a Fellow of the IEEE and a Life Member of the Korean Physical Society. He has co-authored more than thirty-five technical articles including a book chapter, and holds twenty-two U.S. patents. He is a recipient of the 1975 Stuart Ballantine Medal of the Franklin Institute.

KENNEY, GEORGE B.

George B. Kenney is currently working on his Ph.D. in Economic Materials Technology at MIT. He has worked in the areas of electron-optic applications in analysis of PROMs and plated wire and economic modeling of materials flow.

KOBLINSKI, A.N.

A.N. Koblinski is a technician in the Product Development Laboratory at Motorola Semiconductor Products in Phoenix, Arizona. His previous work includes research and development in hybrid electronics and thin film metallization. He holds several patents, including a basic patent on beryllium-aluminum thin film metallization.

KOSSOWSKY, RAM, DR.

Dr. Ram Kossowsky received a BSc degree in Mechanical Engineering from Technion Haifa in 1957, and MSc and PhD degrees in Metallurgy from the University of Pennsylvania in 1961 and 1963, respectively.

Dr. Kossowsky joined the Westinghouse Research Laboratories in 1966 as Senior Scientist in the Solid State Department. From 1970 he has been a Fellow Scientist in the Metallurgy Department specializing in materials characterization, mechanical properties, correlation of structure and properties. Dr. Kossowsky has recently been assigned the technical direction for the Physical Metallurgy Section and the Electron Optics Lab.

LAHTI, J.N.

J.N. Lahti is a member of the Interconnection Technology Laboratory at Bell Laboratories. He supervises the Electrical Reliability Group in that organization. After receiving the Ph.D. degree in Electrical Engineering in 1965 from the University of Washington, he joined the staff of Bell Laboratories. Since that time he has been engaged in studies of deep space and military communications problems; and since joining the Interconnection Technology Laboratory, he has been responsible for supervising work on the electrical characterization and reliability of printed wiring products. Dr. Lahti is a member of the IEEE and Sigma Xi.

LANDRY, EDWARD F.

Edward F. Landry is a member of the Electrical Reliability Group. After joining Bell Laboratories in 1953 he was subsequently engaged for nearly 20 years in military applications of microwave systems and components. Since joining the Reliability Group his primary responsibility has been the development of data acquisition and data processing techniques.

LORIGAN, ROBERT P.

Robert P. Lorigan received a B.S. degree from Sul Ross State University, Alpine, Texas in 1973. He joined the Materials Research Laboratory of the Semiconductor Products Division of Motorola, Inc. in February, 1974. He has been involved in the study of aluminum corrosion, R.F. sputtered beryllium, and resistor materials as applied to semiconductor technology. Mr. Lorigan is a member of Alpha Chi National Honor Society.

LORO, A.

A. Loro graduated from London University in 1952 with a B.Sc. Hons, Special Chemistry degree. He worked in England as an investigator with British Non-Ferrous Metal Research Assoc. and as a research chemist with G.V. Planer Ltd. before emigrating to Canada in 1957 to join the semiconductor department of the Northern Electric Company. He has remained in the semiconductor field specializing in process technology and more recently device failure analysis. He is presently employed by Bell-Northern Research in Ottawa. He is holder of 27 patents.

MARQUES, ANTHONY M.

Anthony M. Marques received a B.S. from R.P.I., an M.S. from Syracuse U., and is doing graduate work at M.I.T., all in physics. He worked at Rome Air Development Center in the reliability physics and failure analysis of semiconductor devices, and at NASA — Goddard (for Sperry Rand) in the failure analysis of electronic components. Presently he is at The C.S. Draper Laboratory, Inc., concerned with the overall reliability of PROMs. Professional societies include the A.P.S. and the I.E.E.E.

MARTIN, BYRON D.

Byron D. Martin was born in Washington, D.C. He received the BA in physics from Johns Hopkins University, Baltimore, MD and the Ph.D. in physics from Ohio State University, Columbus, Ohio. Dr. Martin worked in solid state physics at the National Bureau of Standards in Washington, DC and Battelle Memorial Institute, Columbus, Ohio. He joined IBM in 1968 at Endicott, NY. At IBM he has worked in ultrasonic bonding, laser materials, and packaging. He is presently a development engineer at East Fishkill, NY.

RODRIGUES DE MIRANDA, WILLIAM R.

William R. Rodrigues De Miranda has been associated with Honeywell's Hybrid Facility for the past three years. He is responsible for process controls, failure analysis/corrective action, and device reliability. For the past two years, Mr. Miranda has developed and implemented plans for a number of investigations on physical and electrical characteristics of wire bond metallurgy. These plans included provisions for correct statistical interpretation and sample size designs. He also worked as Reliability Work Director on the Minuteman program. Prior to his work at Honeywell he was with Raytheon where he spent four years on the Poseidon Captive Line program as Product Assurance engineer and semiconductor vendor liaison manager.

Mr. Miranda received his BS in Electrical Engineering from the Hogere Technische School in Eindhoven, Netherlands, in 1957. He has attended Illinois Institute of Technology for post graduate work and followed a number of courses in semiconductor technology, statistics, reliability engineering and management techniques. He is a member of IEEE, ASQC and ISHM and has written a number of technical papers on integrated circuits and reliability. He is an ASQC Certified Reliability Engineer.

NEWSOME, JAMES L.

James L. Newsome received his Bachelor of Electrical Engineering degree in 1969 from the Georgia Institute of Technology. He has been with the Aerospace Division of Honeywell since 1969 and is presently a work director in the Product Assurance Laboratory. In this capacity he is responsible for directing all failure analyses performed by the Lab. and overseeing the operation of the Division's Scanning Electron Microscope.

NISHI, K.

K. Nishi was born in Tokyo, Japan, on July 12, 1946. He received the Bachelor of Engineering degree in Physics in 1970 and received the Master of Science in Chemical Physics in 1972 from Waseda University. His research involved optical and electrical measurement of the irradiated polymers by the electron beam and the y ray.

Since 1972 he has been a member of the technical staff of Semiconductor & IC Div., Hitachi, Ltd., Japan, and has been engaged in the development of high reliability resin package for semiconductor devices.

He is a member of the Japan Society of Applied Physics.

NISHIDA, S.

S. Nishida was born in Japan on March 30, 1936. He received the B.Sc. degree in Physics from the Kyushu University, Japan, in 1958.

Since 1958 he has been a member of the technical staff of Hitachi, Ltd., Japan.

OGILVIE, ROBERT E.

Robert E. Ogilvie is a professor of Materials Science and Engineering at MIT.

OSWALD, RUDOLPH G.

Dr. Rudolph G. Oswald is currently responsible for the Advanced Development and Process Control activities in the Hybrid Microelectronic Facility of Honeywell's Aerospace Division. Personnel under his direction develop new processes, implement new equipment, and provide assistance in generation of process controls and documentation.

He received his PhD in Solid State Physics at the University of Tennessee. His prime areas of interest are in wire bond metallurgy, vacuum technology and thick and thin film metallizations. He is actively involved in ISHM and is the present President of the Southeastern Region of the American Vacuum Society.

OIEN, M.A.

M.A. Oien joined Bell Laboratories in 1967 after completing his doctorate in Engineering Mechanics at Cornell. For the past three years he has worked on problems related to multilayer board processing and reliability evaluation as a member of the Mechanical Reliability Group in the Interconnection Laboratory at Bell Laboratories.

PARTRIDGE, JAYNE

Jayne Partridge received a BA in physics from Boston University in 1958. From 1959 to 1963 she was employed by Sylvania, Semiconductor Division where she worked at trouble shooting process problems and reliability physics. In 1963, Ms. Partridge joined MIT Instrumentation Lab (now MIT Draper Lab) where she was responsible for the development, evaluation, selection, and reliability of the semiconductor parts used in the Apollo Guidance Computer. She received NASA and MIT achievement awards for this effort.

She is a senior member of the IEEE and is a past General Chairman of the Reliability Physics Symposium.

PAULSON, WAYNE M.

Wayne M. Paulson received a B.A. in physics and mathematics from Luther College, an M.S. in metallurgy from Iowa State University and a Ph.D. in Materials Science from Northwestern University. He is currently a Senior Scientist in the Product Development Laboratory of Semiconductor Products Division, Motorola, Inc. His current research involves the development and reliability of thin film materials for semiconductors. He is a member of the American Society for Metals and the American Vacuum Society.

PEDERSEN, RICHARD A.

Richard A. Pedersen was born in Farmington, Minnesota on October 2, 1940. He received the B.S. and M.S.E.E. degrees from the University of Minnesota in 1962 and 1964, respectively.

After doing research work on superconducting thin films at Minnesota, he joined Bell Laboratories in 1964. At Bell Labs, he was engaged in high frequency transistor development and development of silicon integrated circuits. In 1968 he was promoted to Supervisor of the Bipolar Digital Integrated Circuits Group at the Bell Telephone Laboratories in Allentown, Pennsylvania.

In 1970 he joined Honeywell, Inc., at the Solid State Electronics Center in Minneapolis, where he was involved in design of bipolar memory and high speed logic. In 1971 he rejoined Bell Labs and is now Supervisor of the Bipolar SIC Development Group doing development of bipolar LSI structures and circuits.

PLATTETER, DALE

Dale Platteter received his BSEE degree from the University of Wisconsin in 1972. Since then he has been with the Naval Weapons Support Center, Crane, Indiana. He is currently engaged in the analysis of semiconductor circuits for the TRIDENT Missile Program.

POTTER, HAROLD CLAUDE

Harold Claude Potter is a Member of the Technical Staff with the Microwave Device Department at Bell Telephone Laboratories, Reading, Pa.

A native of Waukegan, Illinois, Mr. Potter received the B.S. degree in 1963 from the Illinois Institute of Technology, the M.S. in 1964 from the University of Illinois and the PhD in 1970 from Cornell University.

Since joining Bell Laboratories in June 1963, he has worked at the Reading location and is presently invovled in IMPATT diode design and development.

Mr. Potter has published two articles on surface properties of metal and alloy single crystals.

He is a member of the American Physical Society and the American Association for the Advancement of Science.

RESTRICK, R.C., III

R.C. Restrick, III is a member of the Interconnection Technology Laboratory at Bell Laboratories. After receiving a Ph.D. in Electrical Engineering from the University of Michigan in 1968, he joined Bell Laboratories and continued his work in coherent image processing. There he has worked on image processing, imaging systems, electrical characterization of interconnection media, the acquisition and processing of printed circuit reliability data, and automatic testing of printed circuits. Dr. Restrick is a member of the IEEE and Sigma Xi.

RIDDELL, MALCOLM M.

Malcolm M. Riddell earned a B.S.M.E. from Fairleigh Dickinson University and has done graduate work in polymer engineering and science at Stevens Institute of Technology. He has more than ten years industrial experience in engineering properties and testing, processing, applications research and technical service on a broad variety of plastics and reinforced plastics both thermoplastics and thermosets. He has published papers and lectured on new materials, testing mechanics and failure mechanisms and in general on the engineering properties of plastics. He is a voting member of ASTM, Vice-Chairman of Plastics Committee D-20 and Section Chairman, and active in SPE Engineering Properties and Structure Division. He is currently Technical Manager of the Thermoset Business Group, Allied Chemical, Specialty Chemicals Division, Toledo, Ohio.

ROSENBERG, STUART J.

Stuart J. Rosenberg received his B.S. degree in applied math, engineering (elec.) and physics from the University of Wisconsin, May 1975. Mr. Rosenberg joined Intel Corporation in 1975 as a reliability project engineer working on Bipolar and dynamic RAM integrated circuits. Since March 1976, Mr. Rosenberg has been the Quality Assurance, Reliability representative for Intel in Europe.

RUDY, DONALD A.

Donald A. Rudy is a member of the Interconnection Technology Laboratory of the Bell Laboratories at Whippany, New Jersey. He holds an MA in Biophysics from Harvard University and a Ph.D. in Physics from Washington University. Before joining the Bell Laboratories he did research in acoustical properties of paramagnetic materials. Present work includes electrical and mechanical reliability studies on multilayer printed circuit boards, and electrochemical studies of copper electroplating systems. He is a member of The American Association of Physics Teachers, The Electrochemical Society, The American Electroplaters Society and Sigma Xi.

SIMMONS, W.J.

Mr. Simmons has a B.S.E.E. degree from The University of Missouri. Since joining Hughes in 1961, Mr. Simmons has specialized in microwave devices and electron tube component engineering. Improved reliability in Hughes space programs has resulted from his in-depth microwave semiconductor failure analyses and appropriate manufacturer corrective action. In addition to varactors and step recovery diodes, he has instituted the necessary quality controls and testing to secure silicon Schottky barrier mixer diodes and germanium tunnel diodes for use in long life space programs. He has helped to determine techniques, by use of the scanning electron microscope (SEM) and microprobe analysis, to evaluate the possible degradation due to metalization defects and surface contamination on microwave transistors. For certain low usage microwave items he has been instrumental in establishing degradation parameter limits by use of step-stress testing. This approach is presently being used to establish the MTBF of IMPATT diodes for a space application.

As a microwave component specialist he has worked on all types of programs at Hughes.

His area of responsibility also includes electromechanical, passive and active microwave components and electron tubes (from magnetrons and traveling wave tubes to photomultiplier and cathode-ray tubes). In his present position he is responsible for two component specialists involved with RF transistors, signal processing devices (balanced mixers, switches, and phase detectors), electron tubes and all microwave components. For three years prior to joining Hughes, Mr. Simmons designed and developed UHF and VHF transceivers at Collins Radio Company.

SPANO, JOHN D.

John D. Spano has ten years experience in the I.C. manufacturing industry, including three years as an I.C. Failure Analyst specializing in LSI. Presently, he is a Quality Assurance Process Control Engineer with the Bipolar IC Wafer Process Operation. His responsibilities include monitoring 'on-going' wafer processing parameters in the diffusion, photoresist, metalization and electrical probe operations.

John is also responsible for analyzing processing anomalies as they relate to product reliability.

SPRIGGS, SPENCER

Spencer Spriggs received the B.S. degree in Physics (1952) from the University of Redlands in California. His professional background includes material evaluation, thin-film investigations, and process development in support of hybrid microelectronics.

He is a Reliability Specialist on the Technical Staff of Aerojet Electro-Systems Company, Azusa, Ca. His current responsibilities include environmental testing, component reliability and failure analysis, and characterization studies to establish hardware reliability.

Mr. Spriggs holds six patents and has four pending in the area of thin-film microelectronics. He is joint author of ten papers on microelectronics and failure analysis, and is a member of the American Physical Society and the International Society for Hybrid Microelectronics, as well as a Senior Member of the American Vacuum Society.

SMITH, JACK S.

Jack S. Smith holds a B.S. degree from Clarkson College and an M.S. degree from Syracuse University both in Physics. Mr. Smith has worked in the areas of reliability physics and radiation effects on semiconductor devices at Rome Air Development Center. In 1976 he joined the Lockheed Palo Alto Research Laboratory where he is currently engaged in research on oxide degradation mechanisms.

SMITH, RONALD C.

Ronald C. Smith has been employed in the Reliability Engineering Department of Intel Corporation since 1970. He has worked extensively in the general area of PROM and dynamic MOS RAM reliability. Currently Mr. Smith is a Group Leader responsible for product reliability and failure analysis of MOS RAM integrated circuits.

TALADA, DONALD D.

Donald D. Talada entered the U.S. Air Force in May 1966. Through the Airman's Education and Commissioning Program he received a B.S.E.E. degree from Oklahoma State University in July 1972, and was commissioned a Second Lieutenant in the U.S. Air Force in November 1972. He received a M.S.E.E. from the Air Force Institute of Technology in June 1974, and since that time has been assigned to the Reliability & Compatibility Division of the Rome Air Development Center.

THOMAS, EDWARD F.

Edward F. Thomas graduated from Northeastern University, Boston, Massachusetts, in 1963 with a B.S.E.E. Since that time, he has been with NASA's Goddard Space Flight Center as a member of the Quality Assurance Division. His initial activities involved the failure analysis of semiconductor devices. During the past seven years, Mr. Thomas has been conducting investigations into the mechanisms of degradation and failure in electronic parts, most recently in the area of optoelectronic devices.

VANDERKOOI, N.

N. Vanderkooi received a PhD in Physical Chemistry at Wayne State University. He has been with Allied Chemical Corporation since 1957 working in physical measurement, electron spin resonance, GC analysis,pyrolysis and process development. He is currently engaged in chemistry and physical properties of condensation polymers.

WAKASHIMA, Y.

Y. Wakashima was born in Tokyo, Japan, on June 24, 1940. He received the B.Sc. degree in Applied Physics in 1965 from the College of Science, Tokyo, Japan.

He has been a member of the technical staff of Semiconductor & Integrated Circuits Div., Hitachi, Ltd., in Tokyo, and has been engaged in the development of plastic encapsulating processes for semiconductors.

WEBSTER, S.L.

Mr. Webster, holding a B.S. in Electrical Engineering from UC at Berkeley, has been with the Hughes Aircraft Company since 1953. He has specialized in component and reliability engineering and has made creditable contributions to the development of programs for statistical data reduction and analysis, evaluation and screening of high reliability component parts, and failed parts analysis. He has been directly involved in the GIDEP data program since 1963, with particular responsibilities as Contrator Data Coordinator. Mr. Webster has produced a number of specification and evaluation techniques for selecting components for use in high reliability space systems.

Since February 1974 Mr. Webster has been Head of the Passive Component Section of the Components and Materials Laboratories.

WINCHELL, II, VERN H.

Vern H. Winchell II is presently with Motorola's Semiconductor Research and Development Laboratory where he has specialized in wire bonding and related assembly studies for the past 2 years. Previously, he worked 6 years with Honeywell prior to receiving his M.S. ('68) and Ph.D. ('70) degrees in Metallurgy and Materials Science from the University of Denver.

WOODARD, JOHN

John Woodard received his Ph.D. from Penn. State. He has been with HYSOL for the past year and a half where his interests have centered around the physical processes occurring in exposy Encapsulants.

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