# Complementary 2-D MESFET for Low Power Electronics

**Interim Report # 3**

**Air Force SBIR Phase I**
**Contract Number: F33615-95-C-1679**


**June 28, 1995**

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# (AirForce SBIR Contract F33615-95-C-1679)

## Phase I Interim Report #3

As detailed in the Phase I proposal, the project has four major tasks. These are 1) assessment of the p-channel 2-D MESFET device fabrication, 2) development of a p-channel 2-D MESFET model and implementation of the model into AIM-SPICE, 3) circuit simulations of complementary 2-D MESFET circuits using AIM-SPICE and comparison with conventional circuits, and, 4) analysis of manufacturability and technology insertion issues. This report summarizes progress in each task area through 28 JUN 95.

### Task 1: Assessment of p-Channel Device Fabrication

The assessment of the p-channel 2-D MESFET device fabrication is underway. Heterostructure modeling of a prospective AlGaAs/InGaAs/GaAs structure was completed and an order was placed for growth of the wafer. Once the wafer is delivered, the p-channel device fabrication will commence.

### Task 2: Development of p-Channel 2-D MESFET Model

The development of a p-channel 2-D MESFET model is underway. The new p-channel model is similar to the n-channel model and uses realistic values for the hole mobility, saturation velocity and Schottky barrier height. The model has been implemented into AIM-Spice and is presently being used simulate the current-voltage characteristics of p-channel 2-D MESFETs. Simulated 0.5 micron width p-channel 2-D MESFET $I_d$ - $V_{ds}$ and $I_d$ - $V_{gs}$ characteristics are shown in Fig. 1 and 2, respectively. The simulations indicate that devices fabricated on the designed structure should yield devices which are in the proper range of peak current and threshold voltage for use in complementary 2-D MESFET circuits. The model is now being used to simulate low power complementary 2-D MESFET logic circuits.

### Task 3: Complementary 2-D MESFET Circuit Simulations

Circuit simulations of complementary 2-D MESFET circuits are just getting underway and will be reported in the next Report.

### Task 4: Manufacturability and Technology Insertion Issues

A comprehensive technology analysis of complementary 2-D MESFET circuits will be performed throughout the duration of the Phase I project. It will serve to summarize the main advantages of a complementary 2-D MESFET over existing technologies and to address any potential barriers to insertion of the complementary 2-D MESFET technology into the large scale IC manufacturing environment.

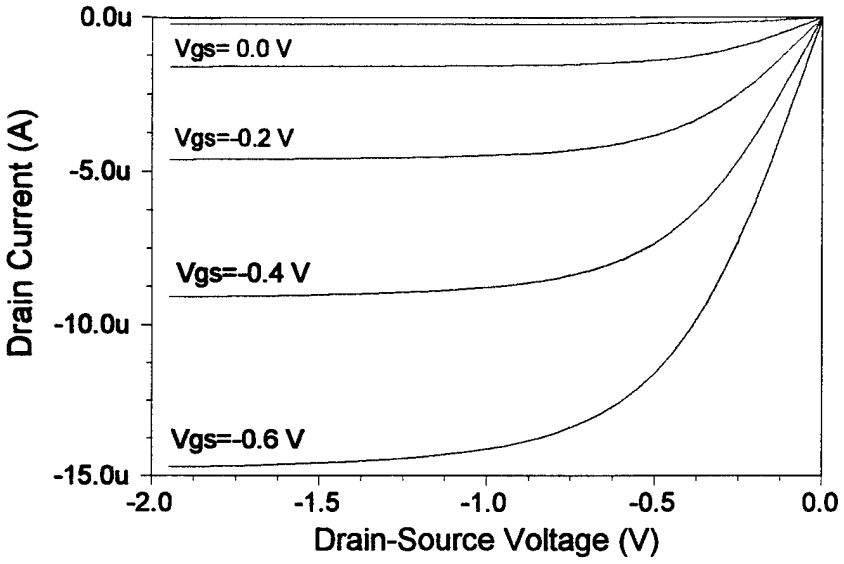


*Fig. 1. Simulated $I_d$ vs. $V_{ds}$ characteristics of p-channel 2-D MESFET ($L_g$ x $W_0$ = 0.5 x 0.5 μm).*

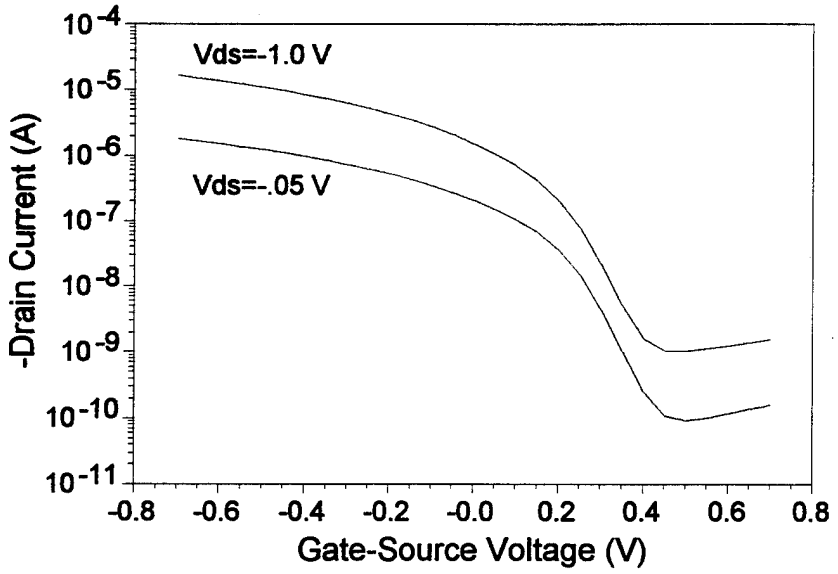


*Fig. 2. Simulated $I_d$ vs. $V_{gs}$ characteristics of p-channel 2-D MESFET ($L_g$ x $W_0$ = 0.5 x 0.5 μm).*

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