Frequency Control Devices

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The objective of the program was to explore advanced concepts in the design and manufacture of frequency control devices. The program was designed to lead to low cost mass production, high performance components, increased levels of communication system circuit integration, and a significant size reduction of radios and other communication system elements. The proposed approach was to adapt advanced microelectronic material processing, piezoelectric thin films, and micro-machining of single crystal plates to achieve wafer scale integration and production of a wide class of frequency control devices.

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1.0 PROJECT OVERVIEW

1.1 Summary

The objective of the program was to explore advanced concepts in the design and manufacture of frequency control. devices. The program was designed to lead to low cost mass production, high performance components, increased levels of communication system circuit integration, and a significant size reduction of radios and other communication system elements. More specifically, **the objective was to decrease the size and extend the frequency range** of frequency control components by a factor of at least 100 so that they can be combined with integrated circuit chips to increase the functionality of communication systems.

The proposed approach was to **adapt advanced microelectronic material processing, piezoelectric thin films, and micro-machining of single crystal plates** to achieve wafer scale integration and production of a wide class of frequency control devices.

1.2 Background

Over the last few decades major advances have been made in the miniaturization of computer electronics and digital signal processing through the implementation of Very Large Scale Integration (VLSI) circuit techniques. Unfortunately, the same level of advancement has not been made in communication circuits and systems. The problem is that, unlike digital systems, Radio Frequency (RF) systems have not realized the same levels of integration and size reduction at the component level. This is due to the required mixture of diverse technologies; transistor integrated circuits and frequency control components. There is a significant lack of commonalty in the fabrication techniques and sizes of those technologies that has impeded the evolution of RF communications systems technology.

The nature of the problem to be addressed by this project is illustrated in Figs 1.1 and 1.2. In Fig. 1.1a a portion of a digital circuit is illustrated. The digital VLSI chips are densely packed and are directly connected to each other with very few passive components. The ratio of the number of transistors to the number of passive components in the system is enormous due to high levels of chip integration and functionally.

In contrast, a typical RF circuit, Fig. 1.1b, is composed of a mixture of integrated circuits or individual transistors and passive frequency control elements. The frequency control components define the ranges of frequencies processed and insure circuit stability. Consequently, every electronic communication system requires frequency control devices for preselection filtering, oscillator control, spur reduction, spectrum definition, and channelization.

High frequency RF analog active circuits have experienced increased levels of integration and functionally as a result of microelectronic VLSI and Microwave Monolithic Integrated Circuit (MIMIC) development. efforts and advances in materials processing. However, the passive circuit elements required for frequency control have evolved slowly along a different path employing a processing technology that is somewhat stagnant. As a result, the impact of MIMIC on overall RF system size and cost is considerably reduced over what could be achieved if frequency control components kept pace with MIMIC evolution.

At the current state of the art there is a diminishing rate of return on the further increase in RF chip functionality through denser microelectronic processing because of the need for
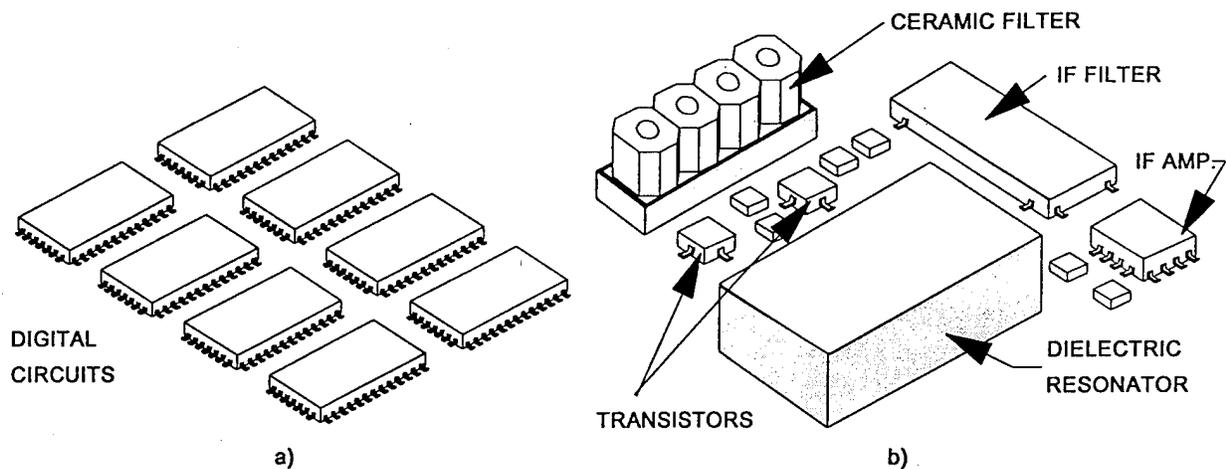
Fig. 1.1 Schematic layouts of representative circuits; a) Digital, b) High frequency analog. The VLSI digital circuit packages are all directly interconnected and require very few external components. The radio frequency circuit has relatively few transistors compared to the number of passive frequency control components.

intermediate filters or other passive elements within the circuit chain. Hypothetically reducing the size and cost of the active circuits to zero in a radio receiver only impacts the overall system by a small percentage of cost and size because of the dominance of frequency control and other passive elements. **What is needed is a new miniature frequency control technology that is truly compatible with MIMIC system concepts.** To that end, a new approach to the development of frequency control components was investigated here.

1.3 Microelectronics Materials Processing

Conventional frequency control devices are largely incompatible with microelectronic processing techniques for two reasons. First, conventional devices are too large for mass production wafer processing and second, they use materials and fabrication techniques that are incompatible with microelectronic processing. The size issue is perhaps the most important from a fabrication standpoint because it rules out wafer processing and handling constraints. Surface Acoustic Wave (SAW) device fabrication, at higher frequencies where devices are small, employs wafer scale processing.

There are two critical steps to the implementation of wafer processing for frequency control devices; First, the frequency control devices must be miniaturized to dimensions comparable with IC's, and Second, the required device fabrication steps must be made compatible with microelectronic processing methods. In short, **frequency control device technologies must be made compatible with integrated circuits in size and manufacturing methods** yet the processing details have to adapt to the special needs of piezoelectric materials.

The potential impact is illustrated in Fig. 1.2 where a 100 mm diameter silicon wafer containing many filters is compared to the size of a single ceramic filter. The size of thin film filters is significantly reduced by the wavelength scaling achieved through the use of acoustic waves.

2

INTEGRATED RF CHIPS

SILICON WAFER

TFR DEVICES

IC AREA

CERAMIC FILTER
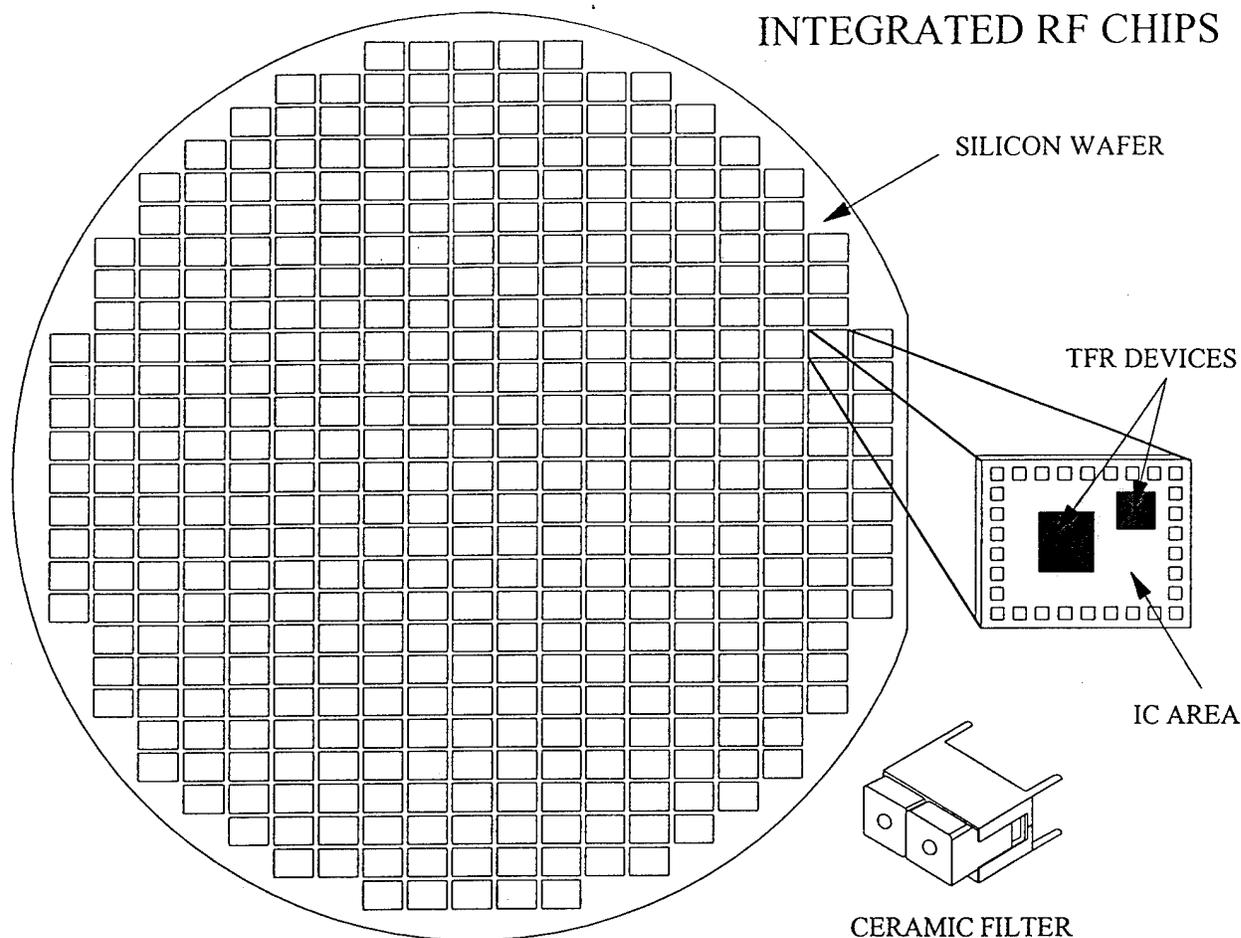
Fig. 1.2 Illustration of a 100 mm diameter silicon wafer containing over 400 communication integrated circuits made possible by the miniaturization and integration of thin film acoustic signal processing devices. A single 900 MHz ceramic filter is shown for size comparison.

However, the ability to fabricate such small acoustic devices at microwave frequencies requires the application of microelectronic materials processing and handling techniques. The illustration suggests an integrated filter and an IC chip but it must be clear that wafer processing would have considerable utility for discrete devices as well.

1.4 Miniaturization and Higher Frequencies

Microwave acoustic devices are scaled according to wavelength in order to achieve a particular frequency of operation. The only flexibility in the size scaling is afforded by material velocities and different modes of vibration. The traditional constraint has been the technology used to fabricate devices and the ability of that technology to obtain device dimensions of interest. The array of filter technology indicated in Fig. 1.3 represents a range of conventional electromechanical devices employing a variety of mechanical modes of vibration [1]. At low frequencies compliant modes are used in order to keep the device size small and at high frequencies stiffer modes (higher velocity) are used to keep the devices from becoming too small. Here small and large are size concepts that are only meaningful relative to the methods used to fabricate the devices.

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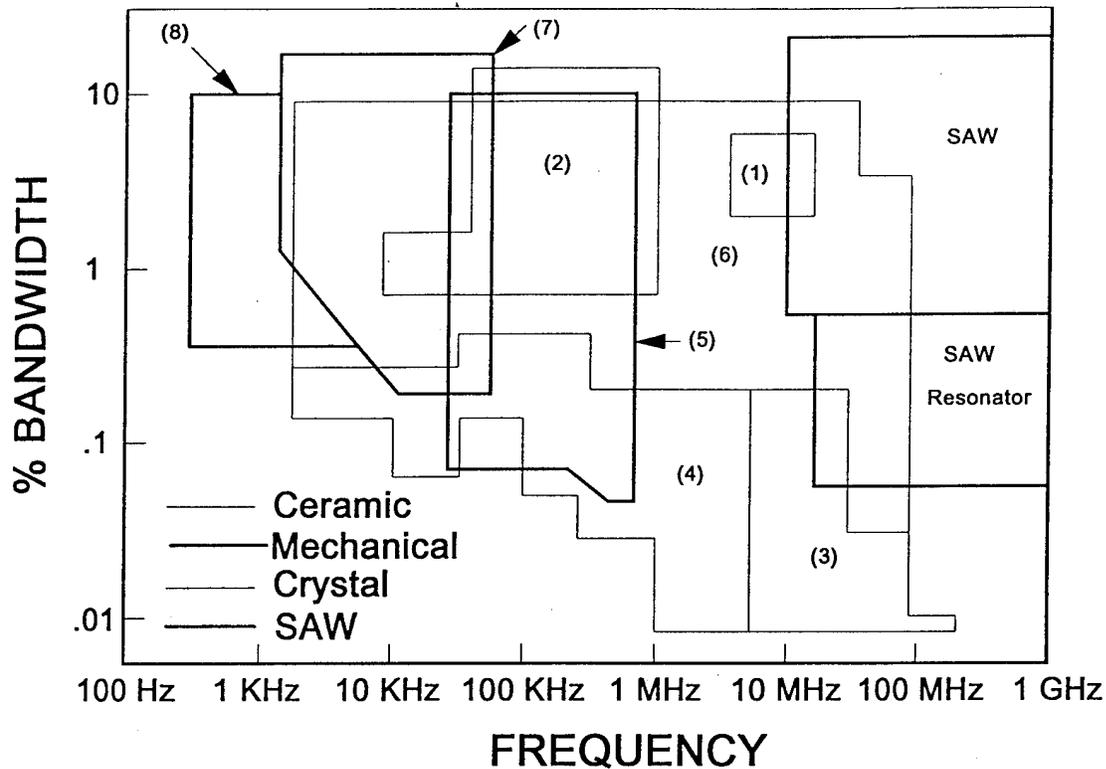
Fig. 1.3 Frequency chart of acoustic filter technology (from R.A. Johnson [1]) showing frequency and percentage bandwidth for conventional filter technologies. The general types are bounded by the line types. (1) Ceramic monolithic ladder, (2) PZT ceramic ladder and tuning fork, (3) Monolithic crystal filter, (4) Narrowband crystal lattice, (5) Disk flexure, torsional rod, extensional rod multi-resonator mechanical filters, (6) Wideband crystal lattice, (7) Flexure-bar mechanical filters, (8) Tuning fork mechanical filters.

With the limited exception of SAW devices none of the technologies represented in Fig. 1.3 have taken advantage of advances in manufacturing brought about by wafer processing and micro-machining. A review of current technology for microwave frequency sources [2] compares the various microwave acoustic technologies and fabrication constraints and points to some technology trends.

In Fig. 1.4 device frequencies are estimated in terms of what could be obtained with thin films and state of the art microelectronic material processing. Consequently, traditional resonator configurations are moved higher in frequency by the dimensional scaling allowed by micro-machining. Thus a ladder filter implemented with thickness mode resonators at 21.5 MHz could be implemented with flexural or extensional mode resonators sufficiently scaled in size. The result would be an IF filter hundreds of times smaller and of dimensions comparable with IC chips. Alternatively, the availability of high Q thickness mode resonators at VHF/UHF could allow the movement of the IF to higher frequencies while achieving the same required bandwidth. For example, 150 KHz bandwidth filters have been demonstrated at 1.6 GHz using thin films [3].

Currently system designers have little choice beyond the filter technologies of Fig. 1.3 for frequencies below 2 GHz. Relatively large ceramic filters are available at UHF and digital

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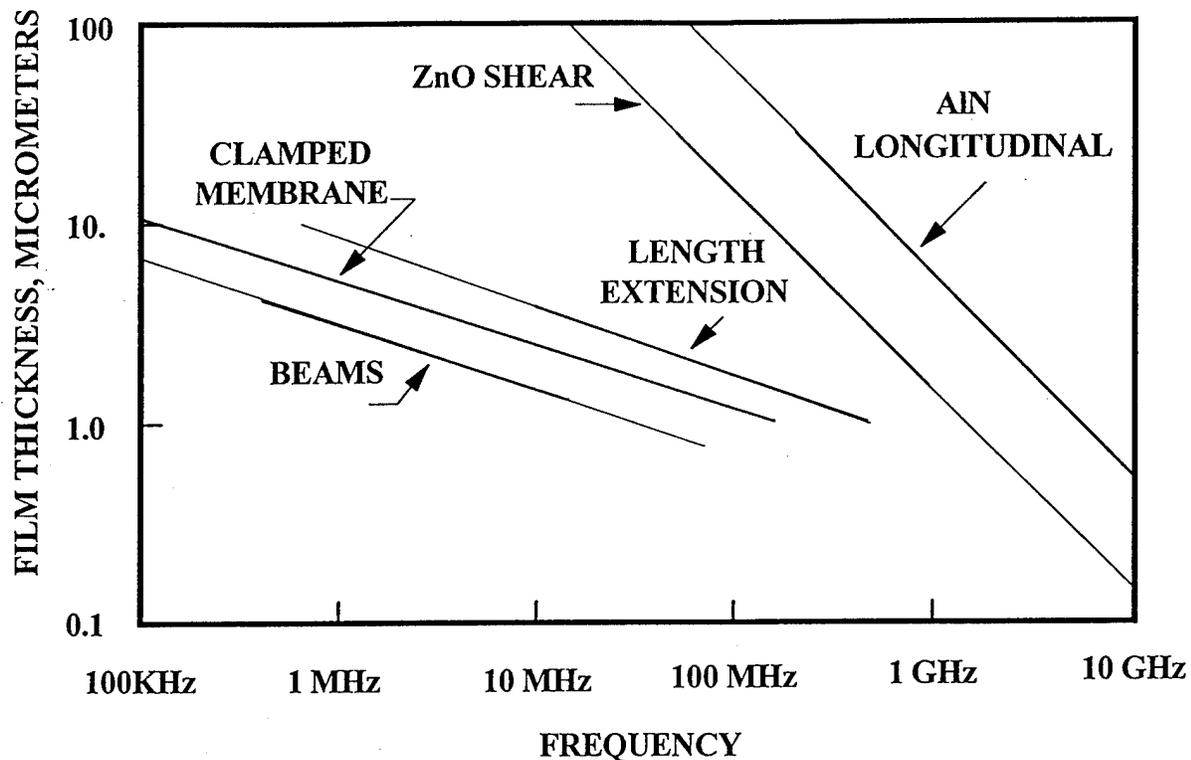
Fig. 1.4. Frequency chart of possible filter technologies implemented with thin film processing. The more compliant the mode of vibration the lower the resonant frequency for a given film thickness. The highest frequencies are obtained with longitudinal modes using a refractory material like AlN and the lowest frequencies are from the flexural modes of beams. AlN shear and ZnO longitudinal are between the AlN and ZnO thickness mode lines.

processing is being implemented at baseband frequencies. SAW devices provide some relief at VHF but become increasingly expensive as 1 GHz is approached. For many filter applications SAW devices provide marginal performance.

The impact of a new thin film and thin plate technology would be the implementation of **ultraminiature** frequency control devices at current frequencies of interest and devices at **higher frequencies** not attainable by traditional technologies.

1.5 Towards Integrated RF Systems

Obtaining device miniaturization and higher frequencies are not necessarily sufficient goals in themselves. A lesson learned from digital circuits is that miniaturization leads to increased levels of system functionality. Computer systems haven't gotten so much smaller as more capable. Within the RF context a much slower evolution has taken place. Future radios could cover 30 MHz to 2 GHz in the same size box with increased functionality to handle GPS, satellite communications, video, FAX, digital data, and, of course, all voice modes.

The evolution to increased functionality and performance in RF systems can only come with higher levels of integration enabled by the miniaturization of frequency control components through innovative concepts.

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1.6 Impact on DoD Systems

The demonstrated feasibility of a new class of high performance ultra-miniature devices and the availability of such devices at frequencies unattainable by traditional frequency control technologies will have a significant impact on DoD communication and other RF systems. The new devices will allow increased levels of functionality in overall systems and give designers the opportunity to implement optimized subsystems not previously practical. Component miniaturization and RF circuit integration will allow a greater density in RF circuits and allow wider frequency ranges to be handled at reduced power consumption.

2.0 OBJECTIVES AND GENERAL APPROACH

The overall objectives of this program are to demonstrate the feasibility of advanced concepts; 1) to reduce the size of frequency control components by a factor of 100 or more, 2) to make miniature high performance resonators and filters available at significantly higher frequencies than currently available and, 3) to integrate frequency control devices with active circuits in a manner that optimizes individual material properties and fabrication methods. The specific objective of two tasks is to make available single crystal materials, having superior acoustic properties, in thin plate form for novel device structures at UHF and microwave frequencies.

The general approach is to bring advanced microelectronic and micro-machining processing techniques to bear on a selected group of device fabrication problems. The detailed individual tasks have been chosen to address the most critical technical problems and to be complementary with other Company initiatives carried out with current or proposed DoD SBIR contracts and with initiatives proposed to other government agencies. Only microwave acoustic devices are to be studied because of the size scaling offered by this technology over electromagnetic techniques or the higher acoustic device performance over lumped element LC devices. The SAW technology is viewed as relatively mature at VHF and UHF, with devices too large in lateral extent for integration with IC's, having characteristics uniquely suited for transversal filtering and consequently marginal filter performance for many applications.

Within the microelectronic industry significant advances have been made in plasma and chemical etching [4-5] that will be adapted to two problem areas in device fabrication, 1) Controlled thinning of crystal plates, and 2) Lateral high resolution definition of device geometries for high frequency scaling.

The impact of ultraminiature devices is significantly reduced if they are too small to handle in a manufacturing environment. Accordingly an important task is to demonstrate the feasibility of wafer scale processing and handling of miniature components such that hundreds of devices are processed in parallel on a single wafer even though the materials may be dissimilar.

The following section details the various tasks designed to demonstrate the advanced device and processing concepts summarized above.

3.0 RESEARCH TASKS AND RESULTS

3.1 Work Summary

Research and development was carried out over a three year period on advanced concepts in materials processing and device topologies for microwave acoustic frequency control devices.

The goal was to greatly extend the frequency range of crystal resonators and to miniaturize resonators and filters.

Several novel crystal plate fabrication techniques were investigated in an attempt to find a practical method of fabricating quartz and other crystal resonators for UHF. One approach investigated was to mount miniature quartz blanks onto silicon wafers having micro-machined recessed pockets to automatically limit the polishing process. Another, more promising, approach investigated was to bond a large piezoelectric wafer to a support substrate and then polish the piezoelectric substrate to the required thickness. Techniques for bonding and controlling the polishing depth were examined and resonators evaluated for thickness uniformity.

A novel plasma etching and trimming technique that directly and automatically produces the correct resonant frequency was designed and demonstrated at HF using quartz wafers. A plasma etching system was designed for a wide range of etch plasma frequencies and substrate types.

3.2 Novel Plate Polishing Technique

3.2.1 Background

Quartz and other piezoelectric plates have been polished to dimensions required for VHF-to-microwave frequencies using chem-mechanical or etching techniques in a number of studies [6-7]. The problems encountered are thickness control, handling of the blanks after the desired thickness has been obtained, and subsequent packaging. Currently quartz crystal blanks can be polished to 60 MHz (25 micrometer thickness) using standard chem-mechanical polishing techniques and then etched to higher frequencies in selected regions.

Chemical etching and plasma processing techniques in general have produced thinned quartz membranes supported by the original quartz blank in the inverted mesa configuration. Because a substantial portion of the quartz is used as a supporting structure these techniques leave a relatively large device overall. In addition, the recessed membrane precludes the use of a chem-mechanical polish to smooth the surface roughness due to faceting and defects. A system of mounting a small quartz blank onto a wafer carrier has been reported [8] but also lacks a means of automatically stopping or limiting the thinning process.

For VHF devices it is relatively difficult to grow piezoelectric films having the required thickness and surface finish control. Slow growth techniques, such as sputter deposition are impractical for VHF thickness mode devices, and rapid growth techniques, such as chemical vapor deposition and vapor transport produce thick films that are heavily faceted and unsuitable for bulkwave or SAW device fabrication without further processing. A controlled polishing technique offers some distinct advantages.

3.2.2 Task Objective

The objective of this task was to demonstrate the feasibility of new chem-mechanical polishing techniques for producing thin crystal blanks to produce fundamental thickness mode resonators and other devices in the UHF range. The process was to be compatible with single crystals as well as VHF thin films that require surface finish polishing.

3.2.3 Approach and Results

The initial proposed approach involved taking thin (25 micrometers or less) crystal blanks having preprocessed metal electrodes on one side, etching the resonators (100 micrometers in diameter) from the blank and then mounting them on a silicon wafer as shown in Fig. 3.1. The crystal plates were to be eutectic or adhesive bonded to the wafer carrier using infrared heating (silicon is transparent to IR whereas quartz adsorbs within a depth of 10 micrometers) and then polished to the required thickness.

The mounting technique of Fig. 3.1c optionally allows the blank to be rigidly bonded to the carrier and therefore provides a very firm support for the subsequent polishing action to allow the fabrication of very thin (1 micrometer) plates of quartz and other piezoelectric materials. The via would be formed using a chemical etch common to silicon processing, such as KOH or EDPW.

The rational of the initial approach was to draw upon existing commercial supplies of thin quartz and polishing technology and to preserve as much quartz as possible from the original thin blank. However, the handling of such small crystals is difficult and significantly departs from the economies of wafer scale processing.

Alternate approaches were investigated wherein an entire quartz wafer was to be bonded to a suitable substrate, reduced to the desired thickness, and then resonator die separated from the carrier wafer. Four possible techniques were investigated for polishing quartz die down to thicknesses sufficient for operation in the UHF region. The techniques are similar and all avoid the problems associated with handling, cleaning, and mounting individual thin quartz die for subsequent polishing. The techniques are illustrated on the following pages.

The first technique is shown in figure 3.2. A Si wafer is used as a carrier for the quartz. Pockets are etched in the Si wafer using KOH or EDPW leaving bonding pads. A quartz wafer is metallized and the electrode patterned on the bottom as shown in the insert. The quartz wafer is then aligned with the Si and bonded to it. Anodic , fusion, or direct bonding could be used for this process. It may be necessary to oxidize the Si wafer prior to the bonding step. After bonding a dicing saw is used to isolate each quartz die. AlN is then deposited over the entire wafer. This will act as polishing stop after the lapping process brings the quartz thickness within range for the polishing step. Depending on the thickness of the AlN it could also serve as a means of sealing the die. The AlN layer could be metallized to give a visual indication of the polishing termination point. After polishing the topside metal electrodes would be patterned. A series connected electrode will be employed in order to bring the electrodes to the top surface.

Prior to implementing the first technique experiments were conducted in direct wafer bonding of quartz to silicon and quartz to quartz. Initial experiment were conducted with 75 mm diameter silicon and quartz wafers sent to Dr. U. Gösele at the School of Engineering at Duke University. The first wafer was heat treated to increase the bonding strength. It was ramped up to 200°C at a rate of 1°C per minute followed by a 1 hour soak and then a ramp down at the same rate. The wafer broke into numerous pieces and many of the pieces were delaminated. The quartz wafer was evidently too thick to allow strain relief during the heat treatment. The second wafer was mounted on a chuck and lapped in an effort to reduce the thickness prior to heat treatment. The wafers delaminated during the lapping process. At this point an effort was made to bond thinner quartz wafers to Si in house. This was successful. Quartz wafers of 0.25 mm and 25 micrometer thickness were bonded to Si wafers with vias.

POLISHING CONCEPTS

BOND CRYSTAL IN WAFER POCKET

POLISH TO REQUIRED THICKNESS

POLISH STOP

CRYSTAL

WAFER CARRIER

a)

CRYSTAL

WAFER CARRIER

SMALL AIR GAP OR RIGID BOND

PROTECTED SURFACE

b)

BOND CRYSTAL IN WAFER POCKET

CRYSTAL

WAFER CARRIER

c)

FORM VIA

CRYSTAL

ETCHED VIA

d)
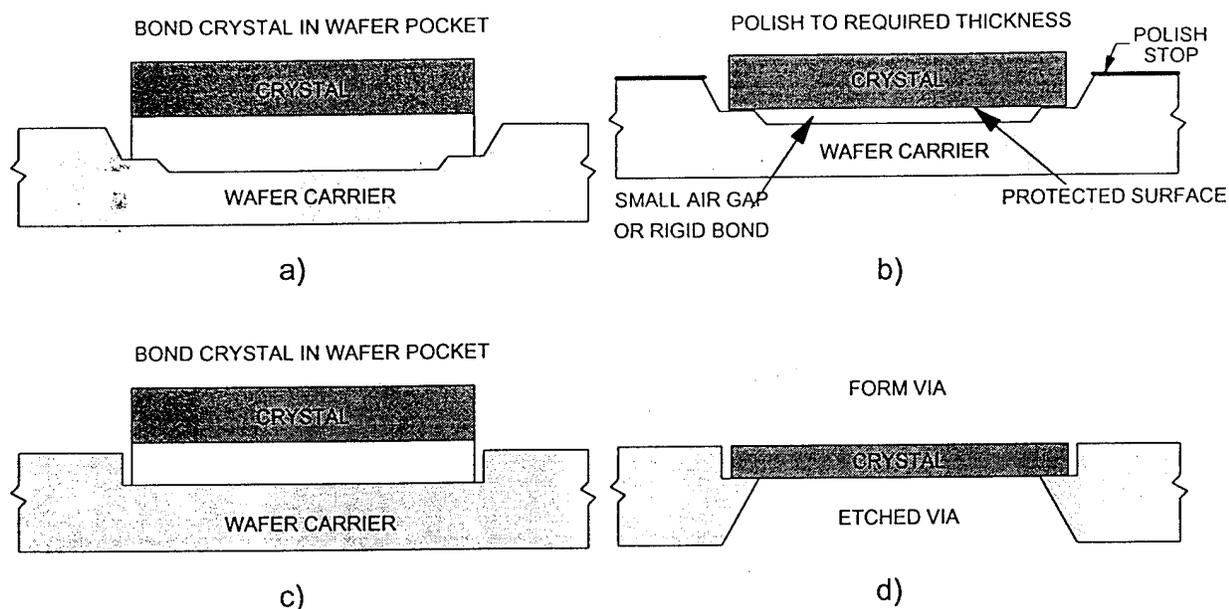
Fig. 3.1 Concept for polishing of prefabricated acoustic crystals. The wafer acts as a carrier for the thin crystal blanks which are never removed from the carrier since the carrier eventually becomes part of the package. The carrier surface, properly protected from the chemical and mechanical actions of the polishing materials becomes the automatic stop for the polishing process. The silicon wall may be etched vertical or angled as desired. a) and b), system where there is an air gap under the crystal, c) and d) system where the crystal is bonded to the carrier and a subsequent via etch used to free the bottom side.

The 0.25 mm thick wafer was 4.8 mm x 2.5 mm while the 25 micrometer thick wafer was 13 mm in diameter. The wafer with the 25.4 micrometer thick quartz survived heat treatment but the 0.25 mm wafer cracked in three places. Both remained bonded. The wafer with the thinner quartz was successfully polished down to 15 micrometers using SITON but during subsequent polishing to thin it down to 10 microns the quartz became delaminated from the silicon substrate.

Thermal expansion mismatches between silicon and quartz precluded complete processing of 0.25 mm thick quartz wafers bonded to silicon substrates. Using thinner, 100 micrometer thick, quartz wafers did not improve the situation.

It was concluded that quartz to silicon bonding could not be accomplished with the techniques investigated.

In order to eliminate thermal expansion mismatches between the silicon and quartz, quartz to quartz bonding experiments were attempted. Wafers were bonded and cycled to 200°C and 400°C but in both cases the bonding was insufficient and the wafers could be pried apart.

In an effort to reduce the bonding temperatures, Figure 3.3 illustrates a slightly different approach. Here a Au-Sn eutectic is used to bond the quartz to the Si wafer. First the backside of the quartz wafer is patterned for the bottom resonator electrode. Next both the
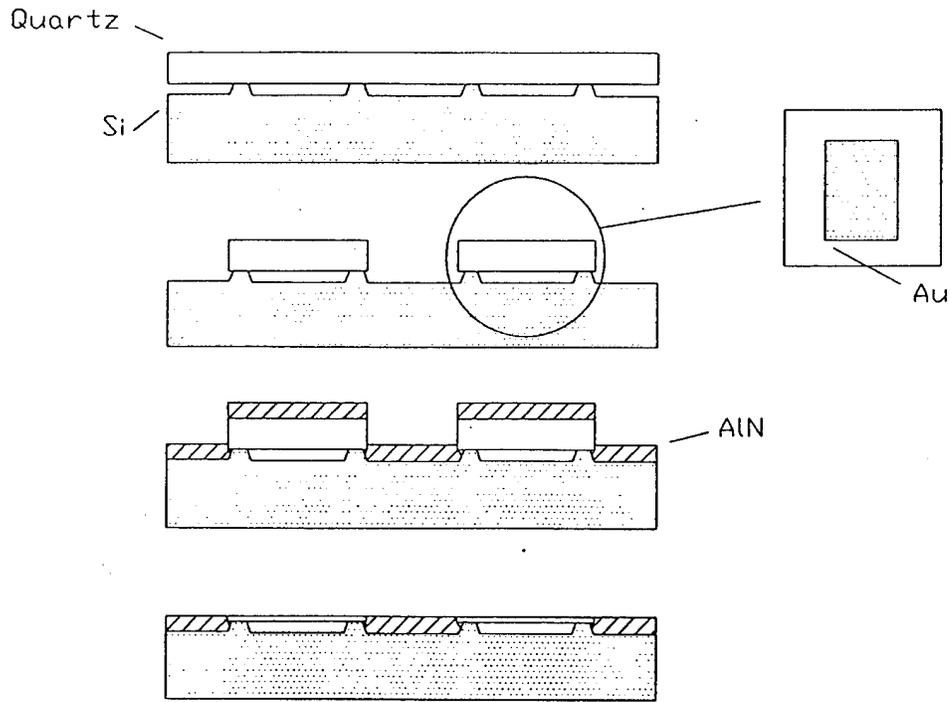
Fig. 3.2 Wafer bonding system for quartz. a) Quartz is bonded to mesas etched in silicon, b) quartz is sawed into die, c) AlN is deposited over wafer, d) quartz polished to AlN stop.
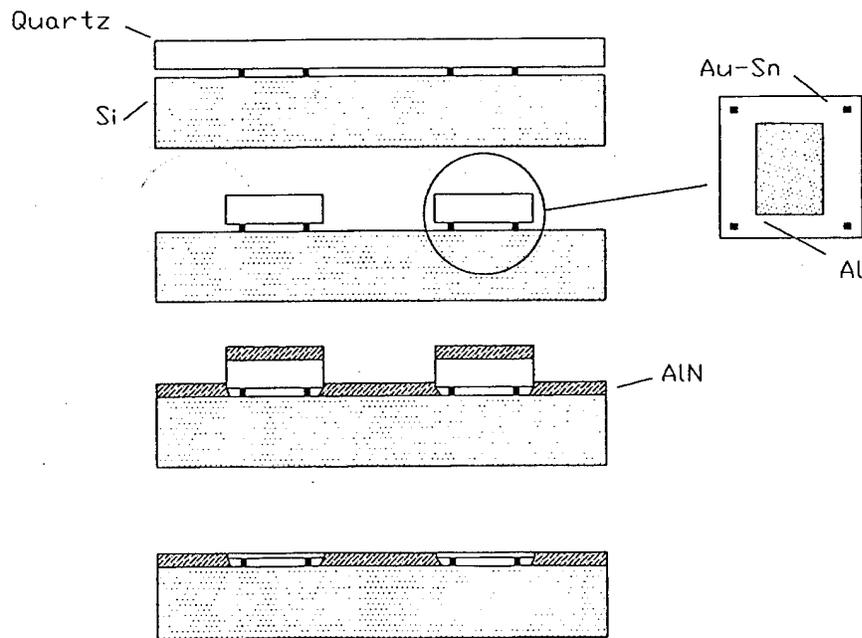
Fig. 3.3 Eutectic bonding of quartz. a) Quartz is bonded to Au-Sn pads formed on a silicon wafer, b) quartz is sawn into die, c) AlN deposited over wafer, d) quartz polished to AlN stop.
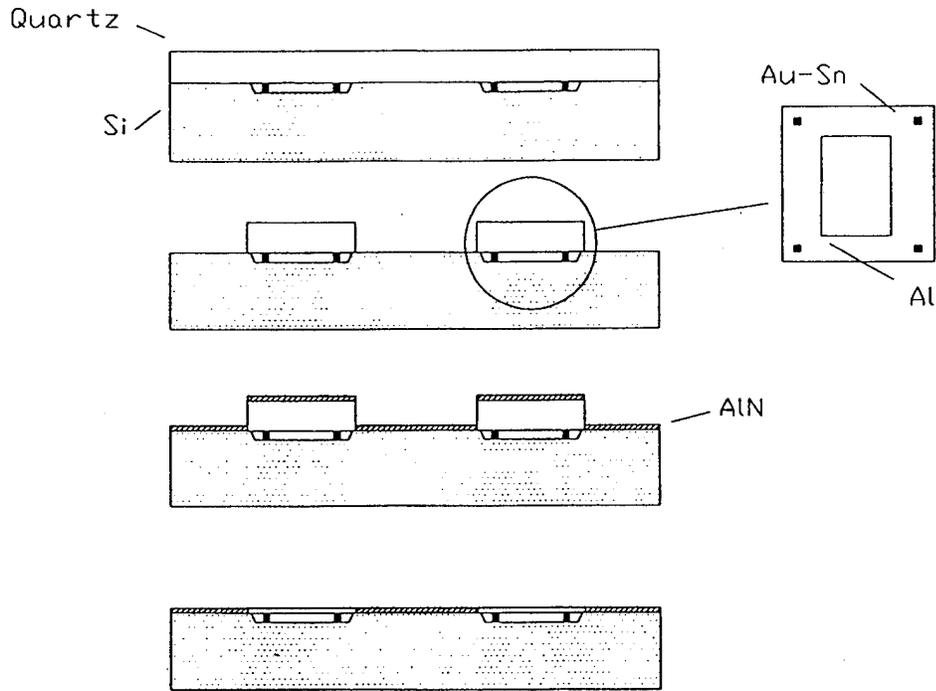
Fig. 3.4 Wafer bonding system for quartz. a) Quartz is eutetic bonded to mesas etched in silicon, b) quartz is sawed into die, c) AlN is deposited over wafer, d) quartz polished to AlN stop.
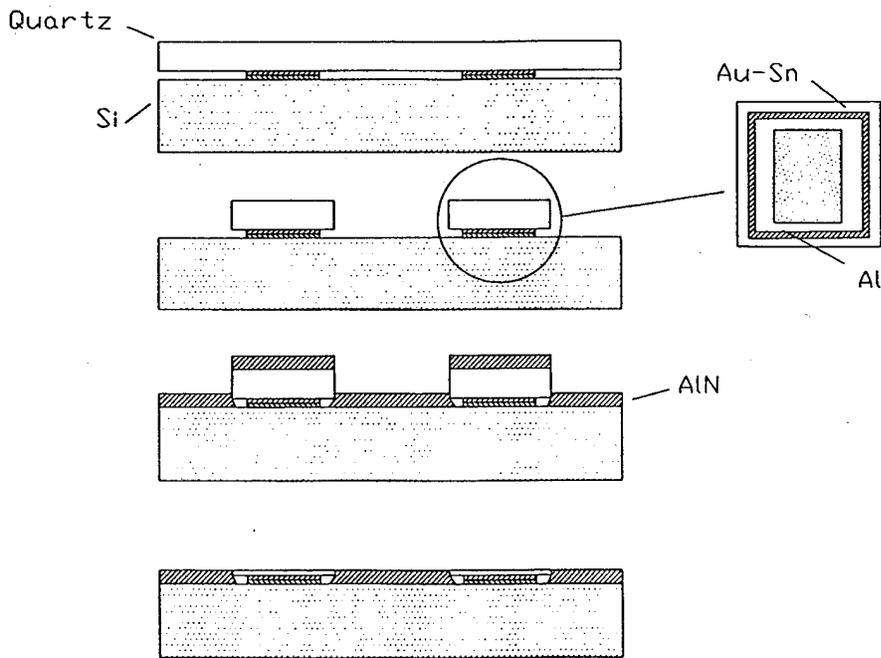
Fig. 3.5 Wafer bonding system for quartz. a) Quartz is eutetic bonded to silicon, b) quartz is sawed into die, c) AlN is deposited over wafer, d) quartz polished to AlN stop.

quartz and the Si wafers are patterned with consecutive Au, Sn, and Au depositions in an E-beam evaporator using a liftoff technique. The last Au deposition will prevent the Sn from oxidizing and insure a low bonding temperature. After deposition the quartz and Si wafers are aligned and bonded. A good Au-Sn eutectic bond can be achieved at 260 degrees C. The rest of the process is the same as described above.

Figure 3.4 shows a variation of the previous technique. The major difference is that the Quartz wafer sits directly on the Si wafer assuring good planarity. This is accomplished by first etching recesses in the Si wafer and then proceeding as outlined above.

Figure 3.5 represents a process that is an extension of figure 3.2. Instead of having bonding posts the die are sealed by the Au-Sn eutectic.

Several attempts were made at low temperature bonding of Si and quartz in preparation for wafer thinning. A 75 mm diameter Si (100) wafer was used as the carrier substrate. The wafer was masked with a patterned Al film and recesses were etched in the Si using RIE. After etching the Al film was removed. The etched Si wafer was then metallized in a three hearth E-beam evaporator with 700 angstroms of Cr, 700 angstroms of Au, 2 microns of Sn, and 1500 angstroms of Au in that order without breaking vacuum.

The starting quartz was a 75 mm in diameter by 0.5 mm thick 36° cut wafer polished on one side. It was metallized on the polished side with 700 angstroms of Cr and 1.0 micron of Au as shown in Figure 3.4. The quartz and Si wafers were then clamped together in a jig and placed in a vacuum chamber which was pumped down to 10^{-6} Torr. The wafers were heated with a quartz lamp to 265C for 10 minutes and then allowed to cool down.

The results were inconsistent and only partial bonding occurred. In the parts of the wafer where complete bonding took place the bond was sufficiently strong to tear loose chunks of Si when separation was attempted. In other areas no bonding at all occurred.

A lower temperature bonding technique was investigated towards the end of the project using epoxy. The goal was to demonstrate that thin quartz plates could be fabricated without cracking of the quartz when the quartz became thin during polishing. The procedure was to bond a quartz to a silicon wafer having etched mesas. The mesa tops were in direct contact with the quartz to insure a planarity between the bottom of the silicon carrier and the top of the quartz. Thus when the silicon wafer was mounted to the polishing block the block surface, mesa interface, and quartz surface against the polishing pad were all parallel. This procedure avoided the wedge bond previously encountered between the quartz and silicon.

Starting from a 0.25 mm thick quartz blank it was possible to polish the quartz down to 10 microns thickness with good thickness uniformity. This puts the quartz in the range for subsequent RIE without significant loss of planarity. The result is shown in cross-section in Fig. 3.6 in general had better than 10% thickness uniformity across the 75 mm diameter wafer.

In the future, the quartz would be isolated from the epoxy with quarter wavelength reflectors.

3.2 Plasma Thinning and Frequency Trimming

3.2.1 Background

Significant advances have been made in plasma processing for etching and deposition in microelectronic device fabrication. To a limited extent plasma processing has been applied to

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SILICON

EPOXY

QUARTZ

GLUE
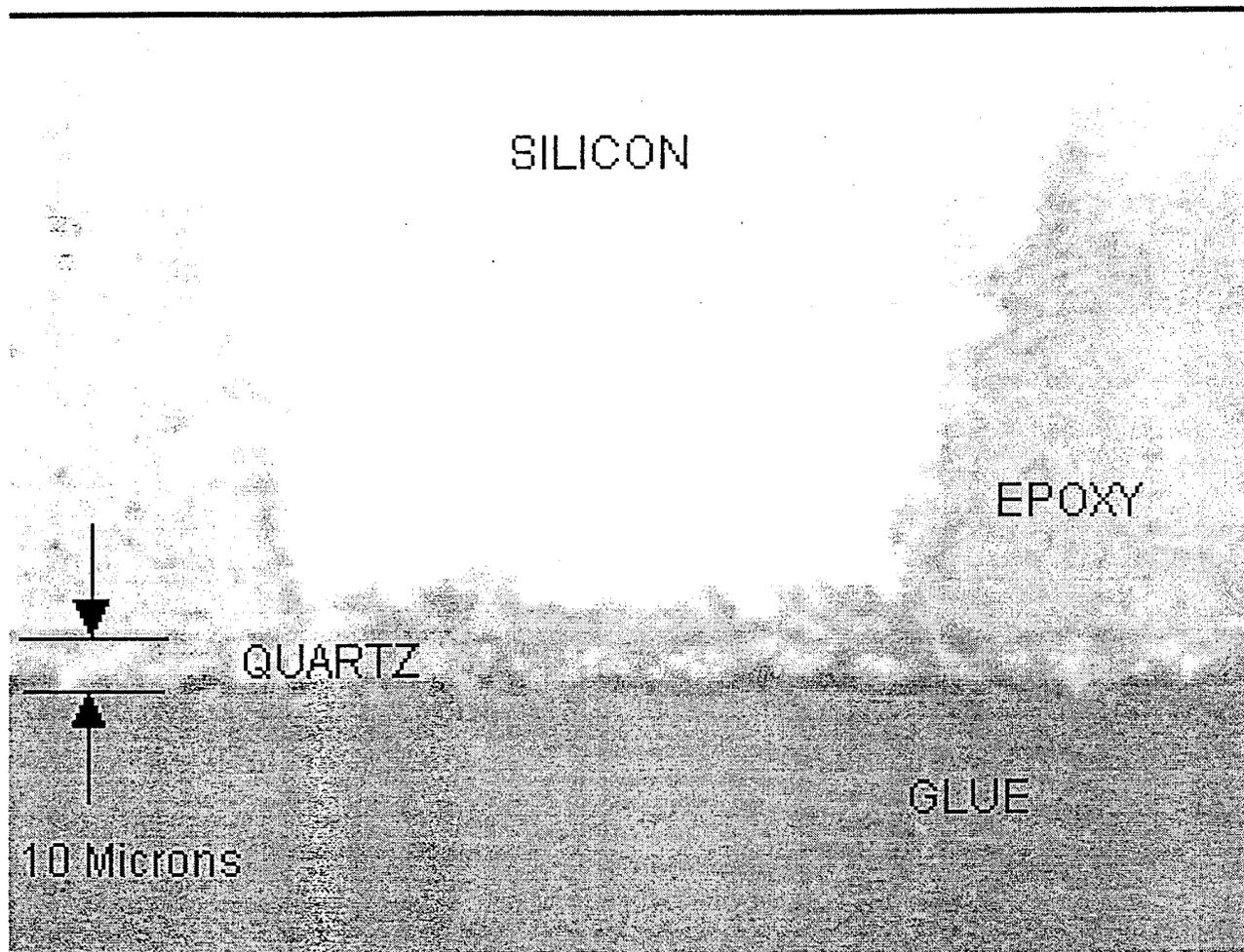
10 Microns

Fig. 3.6. Cross-section of bonded polished quartz wafer. The light region is the silicon mesa, the region adjacent to the silicon is the bonding epoxy, the lighter region against the epoxy and silicon mesa is a 10 micron thick quartz plate, and the lower area is the mounting adhesive used for edge polishing. Raggedness of the edges is due to epoxy breaking away from the edges during edge lapping.

crystal resonators [9-11] but without satisfactory control of the resonant frequencies. A plasma processing method is proposed here that should produce large area UHF crystal plates with precise control of frequency and be suitable for automatic trimming of resonators and filters fabricated on wafers.

Consider the plasma etching system drawn schematically in Fig. 3.7. Here a crystal wafer is placed between capacitor plates similar to a typical parallel plate plasma or reactive ion etching (RIE) system. It is desired to control the resonant frequency of the crystal by etching the plate in the gas plasma to reduce its thickness and raise the resonant frequency to some predetermined value. Assume for example that the frequency of the RF generator is set to a desired resonant frequency that is above the resonant frequency in the crystal, i.e. the crystal plate is too thick for the desired frequency. In the presence of the gas plasma the surface of the crystal is eroded by the action of the plasma and the crystal becomes thinner, thus raising its resonant frequency towards the fixed generator setting.

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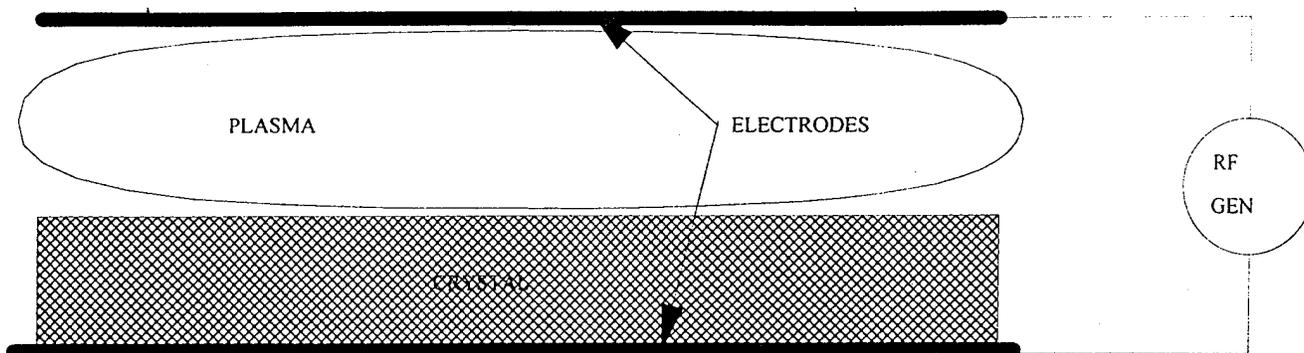
Fig. 3.7 Parallel plate plasma etching system having a crystal resonator placed upon one electrode and in proximity to the RF plasma.

The etch rate of the crystal is dependent upon the rate of ion impingement and energy imparted to the surface and hence the RF current and power. The RF current is controlled by the impedance of the parallel plate capacitor which includes the crystal. Under conditions where the crystal is away from mechanical resonance the crystal appears as a normal dielectric and the voltage across the crystal is determined by a simple series capacitor impedance relationship.

As the thinning crystal approaches the condition where it is in parallel resonance at the generator frequency the impedance of the crystal increases rapidly and consequently the current and etch rate decrease. The effect is to automatically stop the etching process at the generator frequency rather than at a predetermined thickness thought to be appropriate for properties of the crystal.

If a series resonance condition is approached with further thinning, the voltage across the crystal decreases and the current supplied by the RF generator increases dramatically, limited largely by the external drive impedance of the RF system. Maximum etch rate is obtained at series resonance, but as the plate continues to get thinner the crystal thickness moves away from the series resonance condition toward higher resonant frequencies. It will be important to limit or stop the thinning process at the parallel resonance condition.

If the plasma conditions and electrode bias are changed from an etching to a deposition condition then the resonator plate grows in thickness and the resonant frequencies shift downward. If the generator frequency is below the plate's resonant frequencies then series resonance is approached first as the plate thickens. The deposition rate would be a maximum at series resonance. With increasing thickness during deposition the parallel resonant frequency of the plate would be moved down toward the generator frequency and the deposition rate would significantly decrease.

The plasma etch rate has been modeled for this system with some reasonable approximations. Assume that the etch or deposition rate is proportional to the magnitude of the RF power and that the external circuit impedance is low. Under these conditions the voltage across the crystal is determined by the low impedance external source and constant voltage drop nature of a plasma discharge.

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The differential equation for thickness is given by;

$$\frac{da}{dt} = r\frac{|V|^2}{|Z|} \quad (1)$$

where V is the voltage, Z circuit impedance, a the thickness, r a proportionality constant and t is time. In (1) Z is evaluated at the RF generator frequency f_g and the absolute value is used assuming no external resonances. Eqn. (1) is more easily solved for time as a function of thickness. The differential expression for time becomes;

$$dt = \frac{1}{r|V|^2}|Z(\phi(\alpha))|d\alpha \quad (2)$$

where,

$$\alpha = \frac{V}{2f_p} , \quad \phi(\alpha) = \frac{\pi f_g}{2 f_p}$$

where V is the velocity. Using the frequency normalization for thickness α suggested above, (2) may be integrated to give t as a function of the parallel resonant frequency f_p ;

$$t = \frac{1}{R}\int_{\alpha_o}^{\alpha}\left|1 - K^2\frac{\tan\phi}{\phi}\right|\frac{d\alpha}{\alpha^3}, \quad (3), \quad \phi = \frac{\pi}{2}\frac{1}{\alpha}, \quad \alpha = \frac{f_p}{f_g}$$

where α_o is a normalized parallel resonant frequency corresponding to the initial plate thickness, α is the normalized frequency corresponding to the thickness at time t and the convenient normalization frequency is the RF generator frequency, f_g. The coefficient R is a normalized deposition or etching rate. The impedance of the crystal is assumed to be of the form plotted in Fig. 3.8a as used analytically in the integrand of (3).

The general results of this modeling are shown in Fig. 3.8b. The etching proceeds at a uniform rate, indicated by the initial slope of the curve, causing the resonant frequency of the plate to increase toward the generator frequency. The change of resonant frequency with time then levels off when the current decreases as parallel resonance is approached. Etching proceeds slowly during parallel resonance, due to decreased plasma current, causing a slow drift towards series resonance where etching proceeds very rapidly. Finally etching continues at a rate determined by the simple dielectric capacitance of a plate that is getting thinner (and hence the current increases).

The deposition process is almost the mirror image of the etching process with the RF generator set to a frequency below parallel resonance of the plate. Deposition occurs at a normal rate until series resonance where the current increases and then levels off during parallel resonance where the current is minimum.

Because the etching process automatically approaches the parallel resonant frequency of the crystal, a high degree of planarization of a crystal blank or wafer would occur. Suppose there was a thickness variation across the wafer. Setting the generator to a frequency higher than the parallel resonant frequency of the thinner region would cause greater etching in thicker regions until parallel resonance is obtained. Etching would occur on a localized basis until the entire wafer reached the parallel resonant condition assuming that the parallel resonant etch rate is sufficiently slow to prevent the drift of the first trimmed regions into series resonance.

The effects of thickness non-uniformity are illustrated in Fig. 3.9 where initial wafer non-uniformities of 5% and 10% were modeled. By programming the RF generator to shift

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a) (left graph)

AMPLITUDE vs FREQUENCY

FREQUENCY axis: 0.50 0.60 0.70 0.80 0.90 1.00 1.10 1.20 1.30 1.40 1.50

b) (right graph)

FREQUENCY vs TIME

FREQUENCY axis: 0.80 0.84 0.88 0.92 0.96 1.00 1.04 1.08 1.12 1.16 1.20

TIME axis: 0.00 0.07 0.14 0.21 0.28 0.35 0.42 0.49 0.56 0.63 0.70
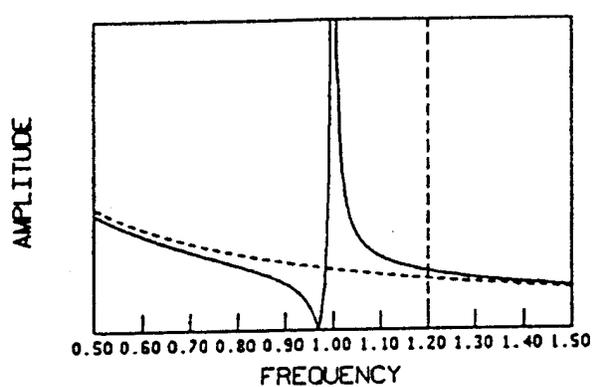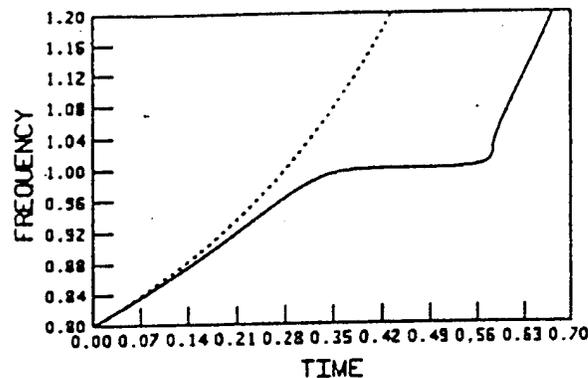
Fig. 3.8 Basic nature of the etching process using parallel resonance as an automatic stop point. Etching proceeds at a normal rate until parallel resonance is obtained where the drop in current causes the etch rate to decrease. The slow drift during parallel resonance moves the crystal into series resonance where the current is higher and therefore so is the etch rate. Beyond series resonance the crystal etches normally approaching the characteristics of a simple dielectric shown in the dashed line. a). Impedance characteristics of a crystal resonator versus frequency normalized by the crystal's parallel resonant frequency. Around series and parallel resonance the crystal's impedance departs from a normal capacitor relationship (dashed line) and goes through impedance extremes determined by the Q of the material. The vertical dashed line at 1.2 is a reference for the RF generator used in crystal etching. b) The etching characteristics of a resonator having a Q of 20,000 and an initial parallel resonant frequency that is 0.8 that of the RF generator. The frequency axis is normalized to the generator frequency and the time axis is scaled according to the etch rate.

upward in frequency towards the end of the first parallel resonance condition the wafer would be moved out of the first region's parallel resonance and away from the danger of drifting into

series resonance. The effect of a step in RF generator frequency is equivalent to starting the curves from zero time but now with the relative thickness variations much reduced. This procedure would provide for an effectively wider time band at parallel resonance at the new generator frequency setting. In this manner the system could be programmed to planarize a wafer in steps and get a high degree of thickness precision and resonator frequency uniformity.

The characteristics of the plasma are such that as current is reduced to near the point of extinction the plasma departs from the constant voltage relationship and the current decreases and the plasma may extinguish. A simple experiment conducted with a series connected quartz crystal, neon bulb, and RF generator showed that the bulb's plasma could be made to extinguish when parallel resonance was reached and that large currents were drawn if the RF generator was set at the series resonant frequency.

3.3.2 Task Objective

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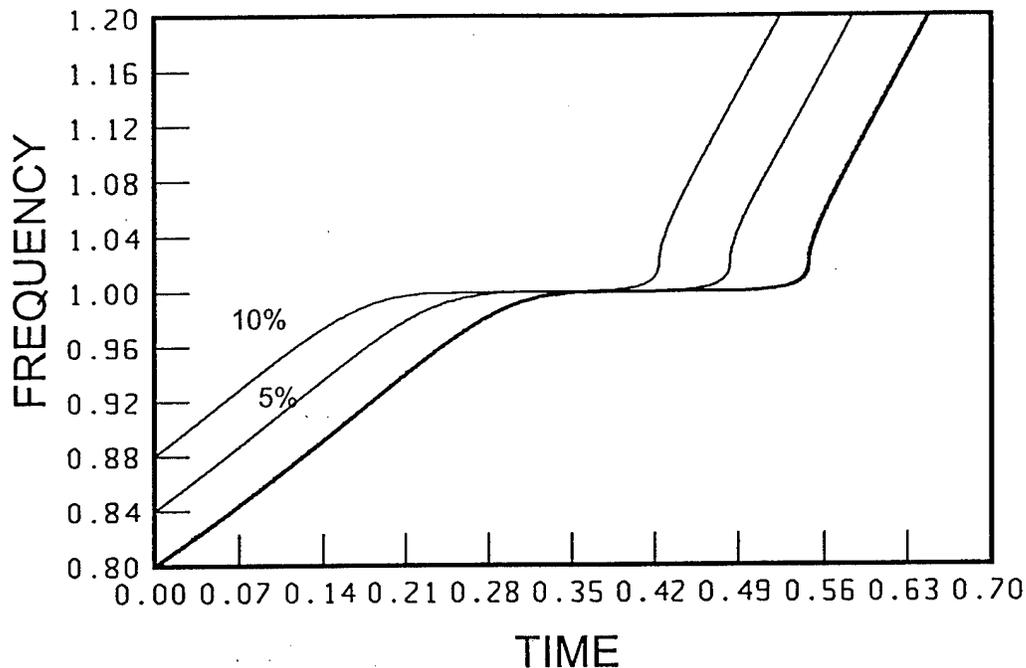
Fig. 3.9 Etching characteristics of regions of a crystal wafer having thickness variations. The thinner portion of the wafer (higher initial resonant frequency) will reach parallel resonance first and drift upward slowly toward series resonance. Meanwhile the thicker portions of the crystal (lower initial resonant frequency) will attempt to catch up with a faster etch rate. The result is a range of time where the entire wafer is at substantially the same thickness. If during this time the RF generator is raised slightly in frequency the effect would be the same as starting at zero time but with a much closer frequency tolerance and eventual wider time interval during parallel resonance.

The objective of this task is to demonstrate the feasibility of a unique plasma etching process that automatically defines resonant frequencies. A secondary objective is to demonstrate the thinning and trimming process on large area wafers containing many resonators.

3.3.3 Approach

The approach was to design and build a small plasma etcher that was capable of a wide range of frequencies as opposed to using a commercial system constrained to just one frequency. The overall system design in cross-section is shown in Fig. 3.10 and detail of the cathode assembly shown in Fig. 3.11.

For simplicity of design and low cost, mostly off-the-shelf UHV components were used. The chamber is a 20.3 cm (8 inch) stainless steel cross with 26 cm (10.25 inch) Conflat flanges. This provides the necessary maximum RF shielding since etching is conducted at frequencies well outside the ISM frequency bands. To the right is a viewport for access to the chamber for loading wafers. The wafers are placed on a aluminum table (cathode) which is attached to the water cooled RF feed. This is shown more clearly in Fig. 3.11. The RF feed is coaxial with water cooling to the table via the copper heat sink screw attachment. The table as well as the ground shield is designed to be replaceable to accommodate various wafer sizes.
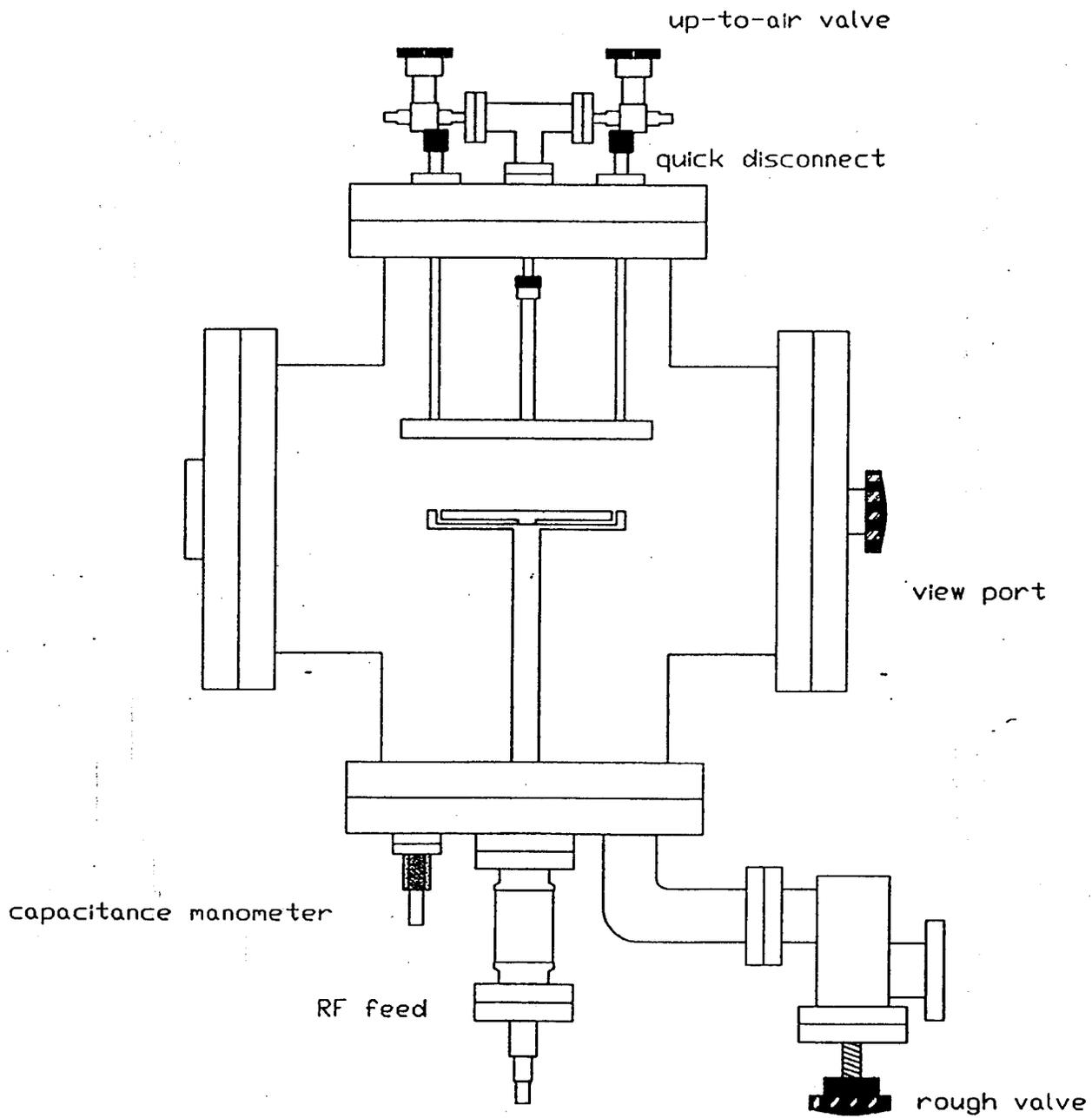
Fig. 3.10. Section view of RIE system.

up-to-air valve

quick disconnect

view port

capacitance manometer

RF feed

rough valve

0.635 (0.250 in)

0.9525 (0.375 in)   13.97 (5.5 in)

aluminum table   0.3175 (0.125 in)
Al   SS

(every 60 degrees)   4-40 cs   weld   1.905 (0.75 in) SS

copper heatsink   braze

1.27 (0.5 in) copper

0.9525 (0.375 in) SS

16.51 (6.50 in)

Heli-arc or TIG welded

25.4 (10.25 in) Flange

8.89 (3.500 in)

sleeved butt joint brazed

1.27 (0.5 in) SS

19.685 (7.750 in)
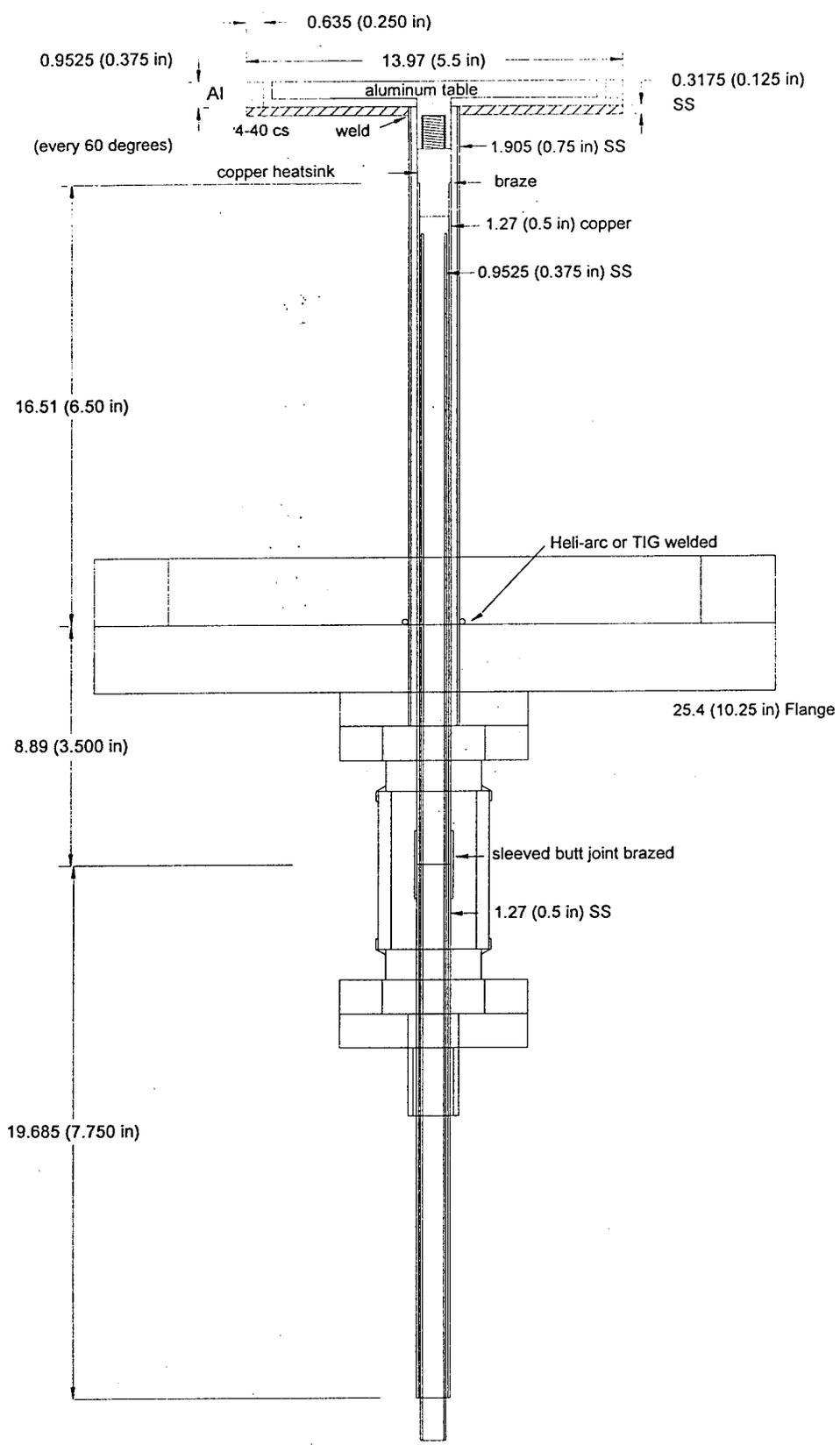
Fig. 3.11. Cathode assembly.

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The chamber pressure is monitored by a capacitance manometer. The pressure is regulated manually by use of the roughing valve. Gas flow rates are controlled by two mass flow controllers connected to the two up-to-air valves on the top of the chamber. The system was designed to use two different gases which are mixed in the top tee and flow into a shower head anode. The shower head can be raised or lowered to allow for adjustment of the substrate to anode distance. The chamber pumping is done with a rough pump having Fomblin oil.

The initial demonstration of the self limiting RIE was successful. A small diameter 1.3 cm cathode and accompanying ground shield were constructed for the purpose of etching 1.3 cm diameter quartz crystals. The matching network was modified to match the plasma impedance using a modified antenna tuner. Initially a 4.83 cm x 2.54 cm x 203 micrometer AT quartz wafer was placed on the cathode for etching. A 100 watt Kenwood HF (1.6-30 MHz) transceiver was used to drive the plasma through the matching network. The parallel resonant frequency of the wafer was measured to be 7500.78 KHz by observing plasma extinguishment at parallel resonance. By rocking the generator frequency across the resonant frequencies, parallel and series resonance could be observed. At series resonance the plasma became more intense and moved closer the surface of the quartz while at parallel resonance the dark space increased significantly, lifting the plasma off the resonator. With higher power the plasma did not extinguish at parallel resonance.

Using FREON (CF4) the 1.3 cm diameter cathode region of the larger wafer was etched. Using another crystal having metalization on the cathode side, the automatic stopping of the etching process at parallel resonance was observed. The signal generator (transmitter) was placed a few KHz above the parallel resonance of the crystal and the crystal was allowed to etch to the point where the parallel resonant frequency was equal to the generator frequency. At parallel resonance the plasma extinguished demonstrating the automatic etching stop. The process was repeated by resetting the generator to a higher frequency and allowing the crystal to continue etching. It was necessary to set the generator power to a level that would allow the plasma to extinguish at parallel resonance (approximately 2 watts).

Gas pressure was maintained in the 20 to 100 mTorr range to assure sufficient energy for reactive ion etching. The overall power density was equivalent to 125 watts for a 100 mm diameter wafer which is in the range for normal RIE of silicon wafers.

An effort was made to measure the etch rate and produce a curve similar to that in Fig. 3.8 using an optical interferometer as shown in Fig. 3.12. The monochromatic light source from the HeNe laser produces interference fringes due to the path difference between the top and bottom surfaces of the transparent wafer. This results in a sinusoidal output which follows the cosine law,

$$A = 1 + a\cos(\frac{2\pi\eta t}{\lambda\cos\theta}) \text{ where}$$

a = amplitude after refracting through the crystal

λ = wavelength of light

η = refractive index of crystal

t = thickness of crystal

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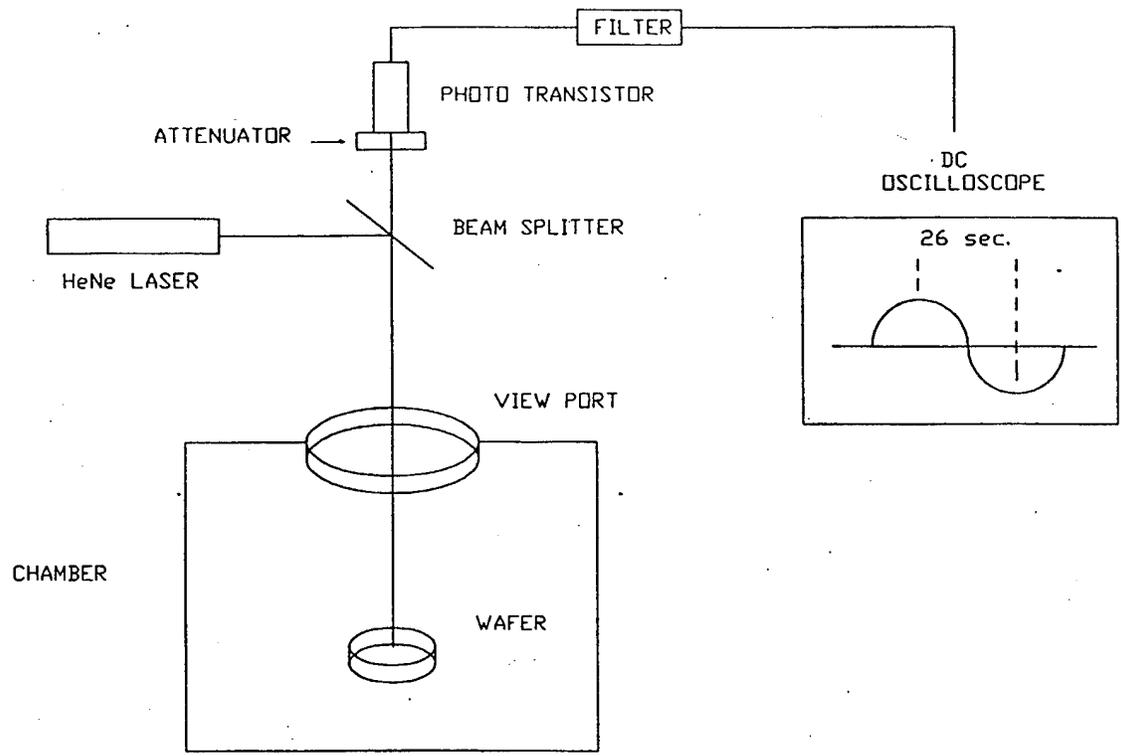
Fig. 3.12. Block diagram of interferometer used for determining etch rate.
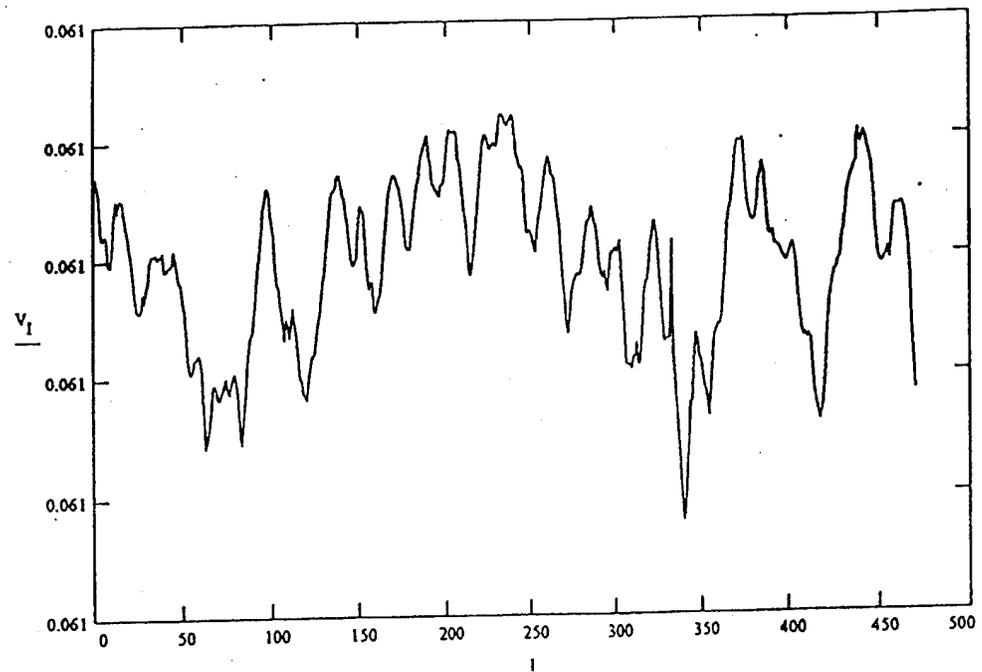
Fig. 3.13 Detector output versus time showing optical interference due to changing film thickness

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θ = angle of incidence.

Alternate constructive and destructive interference is produced as the thickness of the wafer is changed during etching

The technique described above was verified experimentally. A 5 cm quartz wafer with metallized circular patterns on the bottom was used as the substrate. A RF power source operating with a power level of 1.8 watts at 13.56 MHz was used and CH4 was employed as the reactive species gas. A consistent sinusoidal output was observed from the interferometer during the etching process with a periodicity of 26 seconds. Extinguishing and re-igniting the plasma produced no instability in the output. A plot of detector voltage versus time is shown in Fig. 3.13. The data was too noisy to obtain etch rate data.

Plasma etching at UHF was initiated using a miniature version of the original plasma etcher. This was necessary in order to keep the cathode size within reason and to allow for efficient matching of the generator to the plasma load. The new cathode assembly is shown in Fig. 3.14 consists of nominal 4.4 cm components including a standard cross and ports. The matching network consists of a half wave coaxial resonator fed off center for impedance matching. One end of the resonator constitutes the cathode in the vacuum chamber and the end outside the vacuum is open circuited to allow for a DC bias to be established within the plasma. A similar design using a quarter wave coaxial resonator short circuits the DC bias.

The position of the input tap along the resonator allows impedance matching to a 50 source.

A considerable effort was directed towards improving the profiles of the etched quartz. It was found necessary to pattern an electrode on the quartz side in contact with the anode in order to assure a uniform potential across the quartz. Without the electrode it was found that the machining marks on the cathode post were replicated on the top of the quartz wafer. Although undesirable, the results showed the extent to which the etching was being controlled by series impedance of the circuit since air gaps under the quartz created by groves in the cathode post constitute low capacitance high impedance paths for RF current.

The geometry above the crystal was also changed in an effort to planarize the etch profile. A 5/8" anode was installed above the coaxial cathode. It's configured so that the cathode to anode distance is adjustable. The anode produces a more perpendicular electric field distribution above the crystal rather than the fringing fields that extend to the edge of the crystal.

Quartz blanks 1.3 cm in diameter with a 0.635 cm diameter aluminum electrode on the back side were etched using the new configuration and the results were encouraging. The attached plots show the etching profiles before, Fig. 3.15 and after, Fig. 3.16 the design change. The plots were made using an Alpha Step 200. The lateral scan was over a distance of 10,000 microns.

An ECHIP SDE program was set up to optimize the etching process. The three variables were power, cathode to anode distance, and plasma pressure. There were 14 trials including 5 replicate runs. The power was varied from 3 to 6 watts, the pressure from 20 to 80 millitorr, and the wafer to anode spacing from 0.32 to 0.64 cm. Quartz wafers 0.5 mm thick were diced up and thinned down to 127 micrometers prior to RIE. The back sides were metallized. Some of the results are shown in Figs 3.17 and 3.18. The RIE parameter space affected the etch profile but not as significantly as previous alterations of the anode and cathode geometries.

VIEW PORT

QUARTZ WAFER

1.33 " CONFLAT FLANGE (TYPICAL)

PUMPING PORT

VIEW PORT

QUATER-WAVE RESONATOR

RF INPUT

N-TYPE TEE

CAPACITIVELY SHORTED STUB
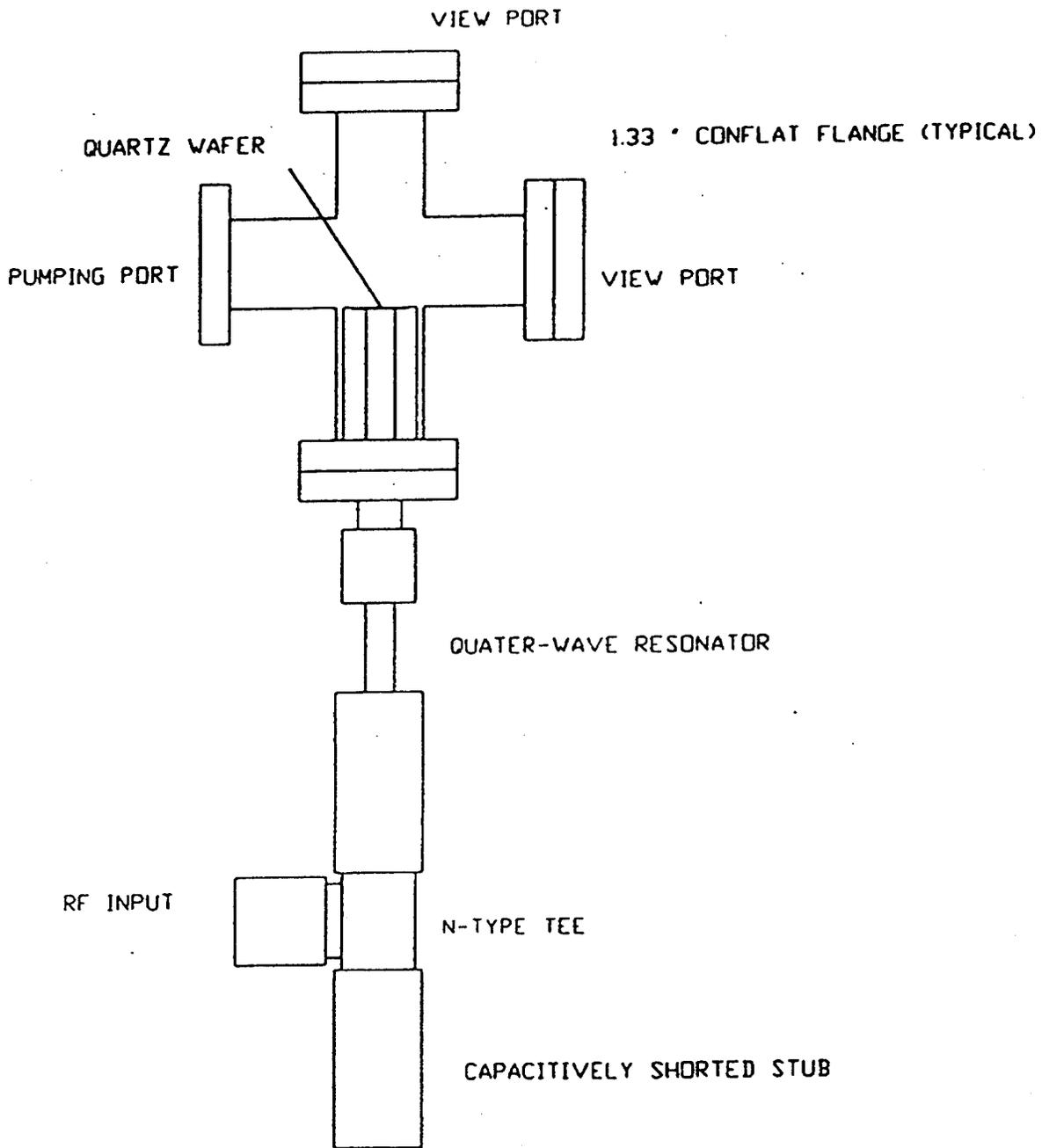
Fig. 3.14 Miniature plasma etcher for UHF quartz crystals. The cathode consists of a half-wave coaxial resonator fed off center for impedance matching to 50 ohm generator. The chamber consists of nominal 1.75 inch UHV components.
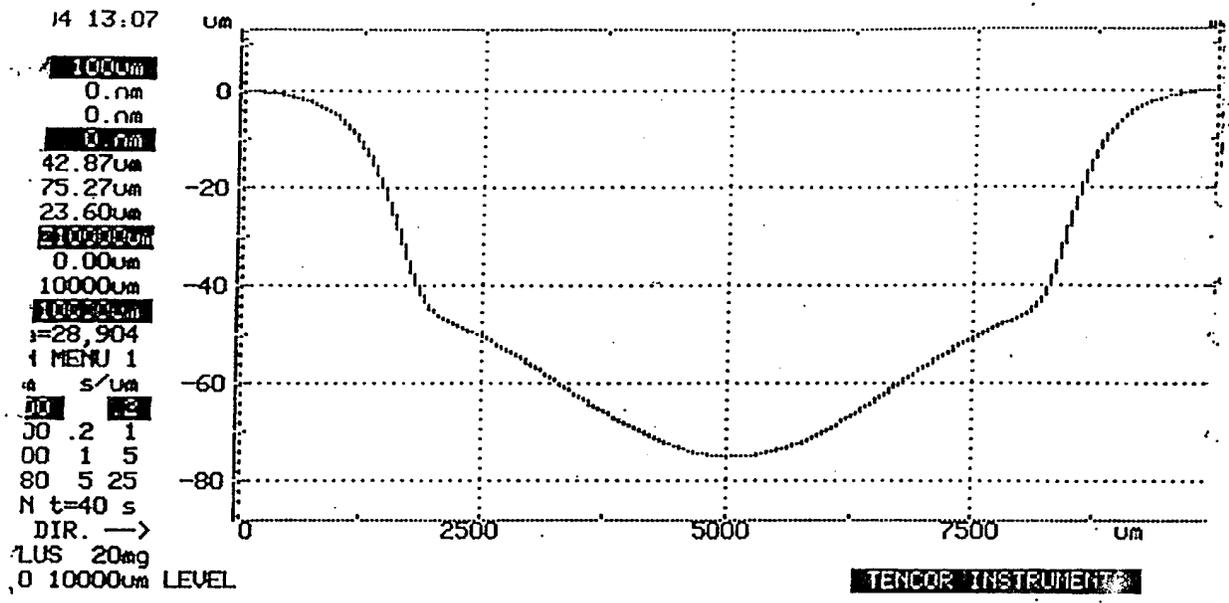
Fig. 3.15 Plasma etching profile before adding an anode above the crystal.
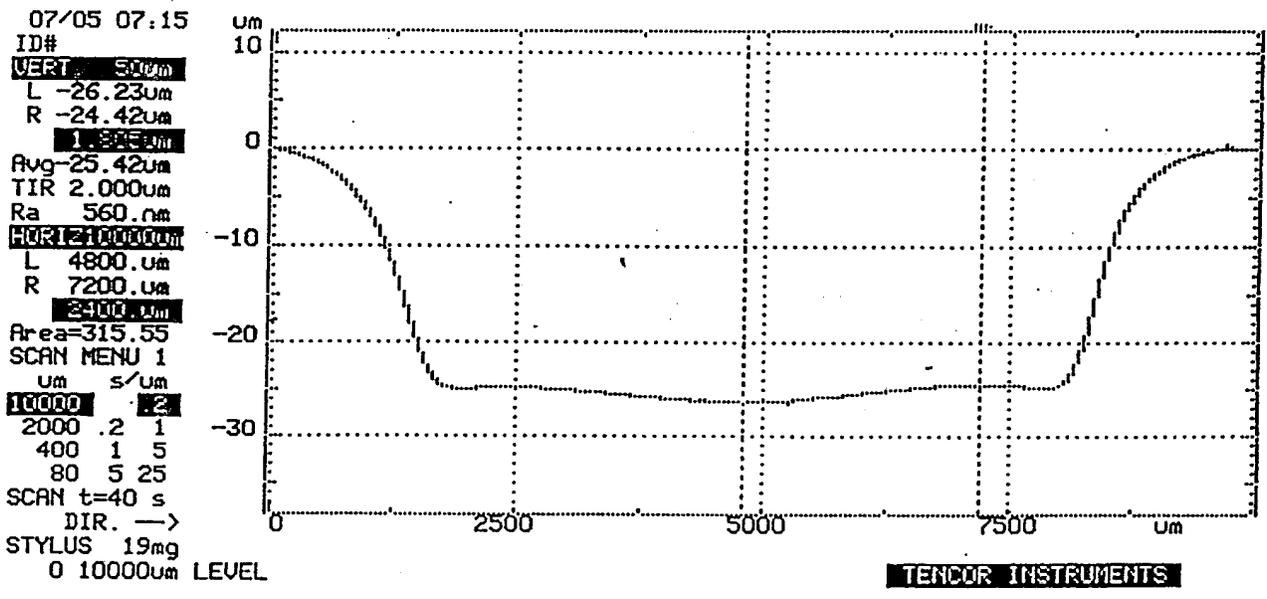
Fig. 3.16 Plasma etching profile after adding an anode above the crystal.

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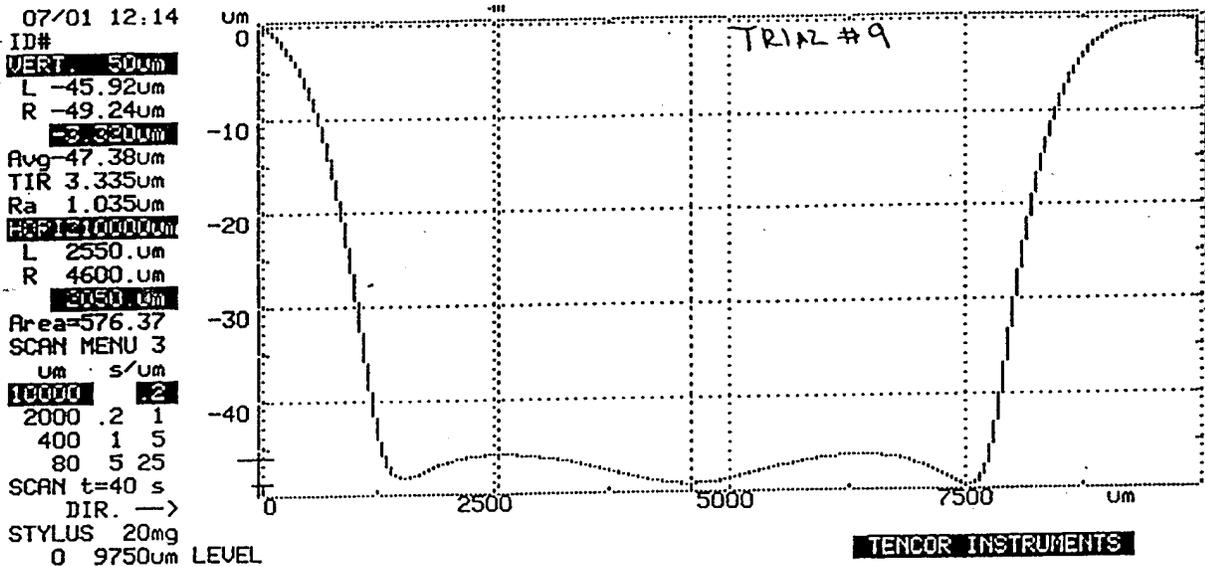
Fig. 3.17 Etch profile after the 9 th trial.
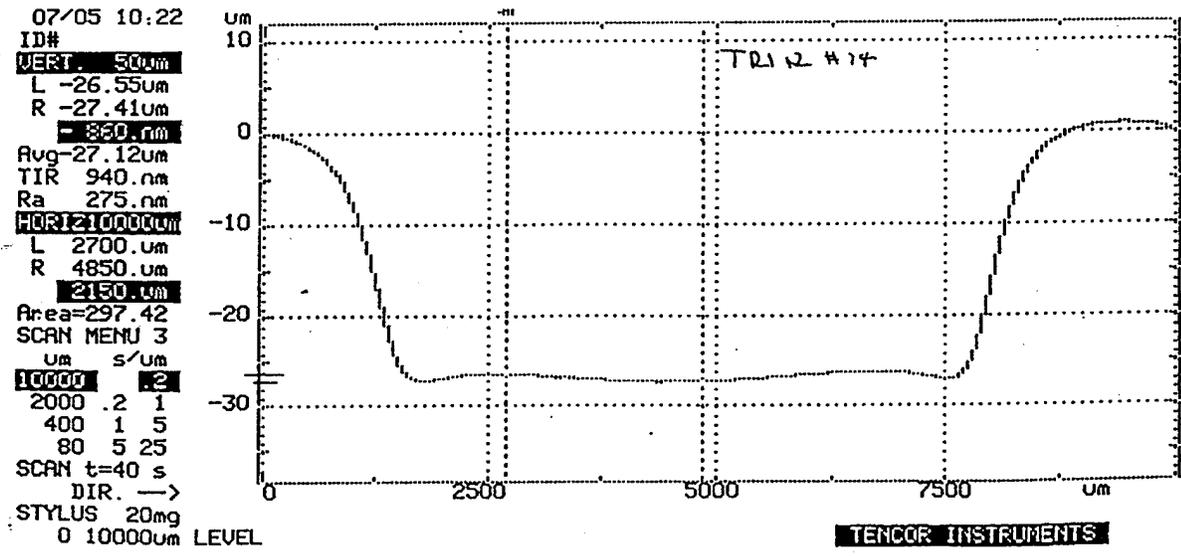
Fig. 3.18 Etch profile after the 14 th trial.

The etch profiles of the replicated runs were quite consistent.

The resonators fabricated by RIE operating in the 350 MHz range have been very fragile and thus difficult to handle or measure. It was suggested by Dr. John Vig that chemically etching the crystals prior to RIE might result in more robust structures.

A saturated solution of ammonium biflouride was heated to 88 C in a Teflon beaker and 60 MHz quartz blanks were etched in the bath. After etching the blanks exhibited greatly

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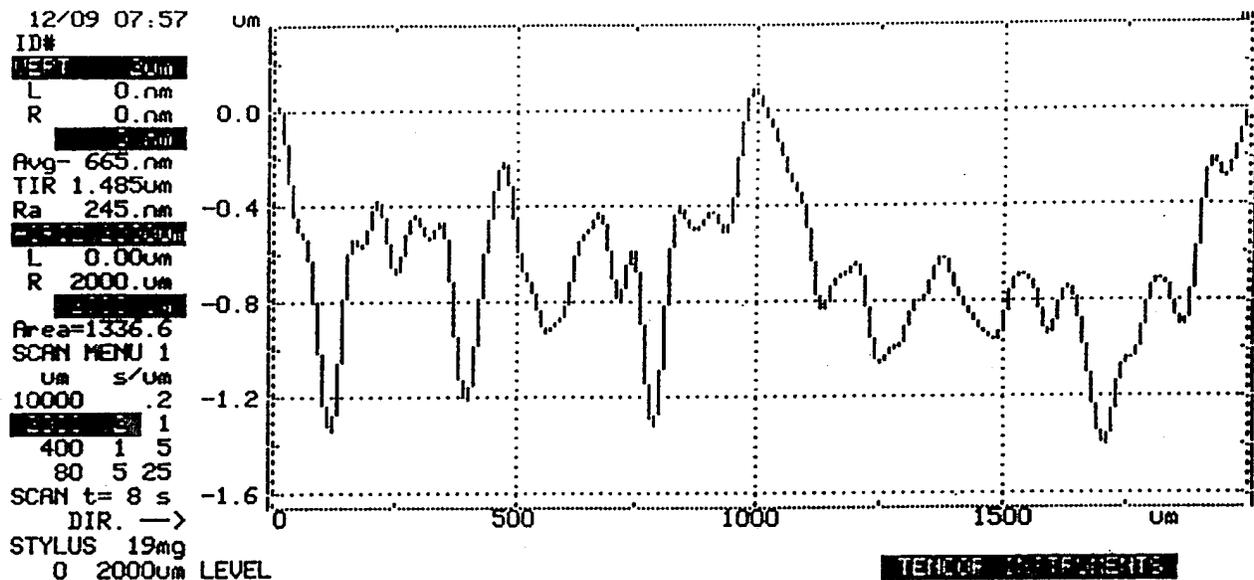
Fig. 3.19 Thickness profile of a chemically etched 60 MHz quartz blank.

increased strength as predicted. The blanks, however, appeared from Alpha Step profiling to be rougher after the etching than before, Fig. 3.19, having a peak value of approximately 1.3 micrometers.

The same process was used to etch cultured swept AT quartz 203 micrometer blanks from P. R. Hoffman. They also became rougher after etching. They even appeared frosted to the naked eye. An RCA clean was performed on the crystals prior to etching.

4.0 WORK SUMMARY

4.1 Novel Polishing Techniques

Two approaches were implemented for thinning piezoelectric crystals for use in the UHF range. Both approaches were designed to maximize yield and facilitate handling. In the first case several 1.3 cm diameter 25 micrometer thick quartz crystals were bonded to a Si wafer prior to thinning. In the second case full size (75 mm x 0.38 mm) quartz wafers were bonded to Si or quartz and subsequently thinned. In order to achieve high yield a very uniform bond was required. Direct wafer bonding results in a very uniform bond but attempts at this were unsuccessful. Thermal expansion mismatch caused the quartz/Si wafers to break and strong bonds could not be achieved for quartz/quartz.

Use of a Au/Sn eutectic for bonding was also unsuccessful even for bonding quartz/quartz. The thermal expansion differences between the eutectic and the quartz again caused the wafers to break.

The final bonding procedure attempted worked quite well. It involved the use of epoxy as the bonding material and etched mesas in Si as the planarizing support. The quartz was polished from 380 to 10 micrometers thickness with good thickness uniformity across the entire wafer. Final device fabrication using this technique would require the thinned piezoelectric to be isolated from the support wafer by acoustic isolators or the bonding material removed from

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immediately under a resonator region. The ideal approach would be to keep the quartz attached to the support substrate to avoid handling thin piezoelectric plates.

Thinning of the mounted piezoelectric plate beyond the initial polished thickness of 10 microns or so can be done with plasma etching with good control.

For purposes of volume production and ease of handling the use of a host wafer for the thinned quartz is a must. Selection and implementation of a suitable bonding technique to accomplish this is key to the success of this approach. Unless direct wafer bonding can be achieved the low temperature epoxy technique or variation described above might be a good starting position for further development. The combination of bonded plate wafer scale thinning combined with localized plasma trimming should be a practical alternative to total inverted mesa style resonator fabrication. In addition, the bonded wafer approach is very applicable to materials other than quartz, such as lithium niobate, that are not suitable for inverted mesa fabrication.

We anticipate further developing this process for the fabrication of lithium niobate ladder filters for UHF and microwave frequencies where isolation from the bonding region is achieved through quarter wave reflector layers deposited on the piezoelectric wafer prior to bonding to the wafer carrier.

4.2 Plasma Etching

The concept of a self limiting RIE was successfully demonstrated on quartz. This was done, however, under very narrow operating conditions where the generator frequency was set so that relatively little etching was required for the crystal to reach resonance and at low power levels to insure automatic stopping at parallel resonance. At faster etching rates with higher power the plasma did not extinguish at parallel resonance. The low K^2 of quartz no doubt contributes to this problem since series and parallel resonance are very close together. Even though the plasma does not go out under these conditions the plasma dark space does still increase and lift the plasma off the resonator as it goes through parallel resonance. In this case an optical system could be used to monitor the dark space and shut off the plasma when resonance occurs.

5.0 Conclusions and Summary of Accomplishments

Techniques were investigated for producing high frequency quartz resonators. The mounting of small quartz die onto silicon substrates and subsequent thinning for high frequency resonator operation proved more difficult than employing the conventional inverted mesa geometry wherein the thin quartz resonator is supported by the bulk of the wafer.

A novel technique was demonstrated for plasma thinning quartz plates such that the frequency of etching can be used as an indicator and control mechanism of the desired resonator frequency.

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