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13. ABSTRACT (Maximum 200 words)

This final technical report outlines the development of Vertical-Cavity Surface-Emitting Lasers (VCSELs) for use in high-speed parallel data links. During this contract, Optical Concepts has produced VCSELs with greatly improved performance, and has developed packaging technologies for VCSELs.

VCSELs have been developed that operate at greater than 5 GHz with sub-milliamp threshold currents. With low turn on delays, these devices have demonstrated GHz data rates with no pre-bias.

VCSEL arrays have been incorporated into high-speed, parallel, fiber coupled packages. Optical Concepts has demonstrated packages using both top and bottom emitting VCSELs, and has developed an integrated microlens technology to ease packaging tolerances.

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vertical-cavity surface-emitting lasers; laser arrays; high speed; data links

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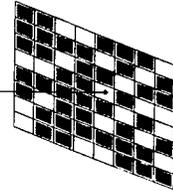
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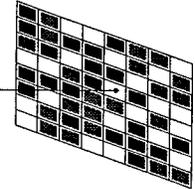
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Optical Concepts, Inc.

VERTICAL CAVITY SURFACE EMITTING LASERS FOR OPTICAL SIGNAL PROCESSING AND OPTICAL COMPUTING APPLICATIONS

FINAL REPORT

Table of Contents

Table of Figures

Statement of Problem Studied

The development and fabrication of prototype vertical cavity surface emitting laser (VCSEL) arrays, packaged with optical fiber ribbons to form high speed data links.

Summary of Most Important Results

- Development of sub-milliamp threshold laser arrays.

- Incorporation of lasers into high-speed fiber-coupled parallel transmitters.

- Demonstration of gigabit/line data rates using these VCSEL arrays.

- Development of microlenses integrated with VCSELs

List of Technical Reports and Publications

REPORTS:

VERTICAL CAVITY SURFACE EMITTING LASERS FOR OPTICAL SIGNAL PROCESSING AND OPTICAL COMPUTING -

1ST ANNUAL REPORT - JANUARY 28, 1994

VERTICAL CAVITY SURFACE EMITTING LASERS FOR OPTICAL SIGNAL PROCESSING AND OPTICAL COMPUTING -

2ND ANNUAL/FINAL REPORT - DECEMBER 30, 1994

PUBLICATIONS

- F. H. Peters, G. D. Robinson, M. G. Peters, D. B. Young and L. A. Coldren, "Small Electrically Pumped Index-Guided Vertical-Cavity Lasers", IEEE Photon. Tech. Lett. 6 (10) (1994)

- J.W. Scott, B.J. Thibeault, D.B. Young, and L.A. Coldren, "High Efficiency Sub-Milliamp Vertical Cavity Lasers With Intra-Cavity Contacts" IEEE Photonics Technology Letters, 6 (6) pp. 678-680. (1994)

- J.W. Scott, B.J. Thibeault, C.J. Mahon, L.A. Coldren, and F.H. Peters, "High Modulation Efficiency of Intra-Cavity Contacted Vertical Cavity Lasers" Applied Physics Letters, 65 (12) pp. 1483-1485. (1994)

- J.W. Scott, F.H. Peters, B.J. Thibeault, D.B. Young, L.A. Coldren, and F.H. Peters. "2.488 Gbit/s optical data transmission with linear arrays of intra-cavity contacted vertical cavity lasers" in European Conference on Optical Communications, 1994. Geneva, Switzerland.

- J.W. Scott, B.J. Thibeault, C.J. Mahon, F.H. Peters, D.B. Young, and L.A. Coldren. "Intra-cavity contacted vertical cavity laser arrays optimized for low current, high speed interconnects" in 14th IEEE Int. Semiconductor Laser Conference, 1994. Maui, Hawaii, USA.

List of Participating Scientific Personnel

Principal Scientist: Dr. Frank H. Peters

Dr. Frank H. Peters was the principal investigator and directed all research effort on the program. He was assisted by Gerald Robinson, Dr. Jeffrey W. Scott and Dr. Vijaysekhar Jayaraman. Gerald Robinson was responsible for wafer processing, device fabrication and testing. Dr. Jeffrey W. Scott performed device modeling, and fabrication on the high speed devices. Dr. Scott also performed device evaluation and characterization and analysis to confirm that device performance agreed with the models for the VCSEL devices. Dr. Vijaysekhar Jayaraman participated in technical discussions on device design and performance.

The resumes of the personnel involved in the program are listed below.

While working on this program, under a subcontract to the University of California at Santa Barbara (UCSB), Jeffrey W. Scott completed the requirements for a Ph.D. EE recently conferred by UCSB.

Resumes of Key Personnel

VIJAYSEKHAR JAYARAMAN

Vijay Jayaraman received his MSEE. and BSEE from the Massachusetts Institute of Technology in 1985 and the Ph.D. EE. from the University of California at Santa Barbara in September 1993. 1988-1993 - Graduate Research Assistant, Department of Electrical and Computer Engineering, University of California at Santa Barbara: Developed grating based long-wavelength semiconductor lasers. Work included setting up system to make fine-period diffraction gratings, crystal growth of long wavelength InGaAsP/InP compounds, and processing and testing of broad-area and ridge-waveguide lasers. In addition, work required theoretical analysis of complex multi-section laser structures. This work led to the proposal and demonstration of the first widely tunable "sampled grating" lasers. The sampled grating approach has since been employed by many other research groups world-wide, and currently holds the world record for semiconductor laser tuning range.

Applied holographic fabrication technique developed for grating-based lasers to fabrication of quantum structures. These included quantum wires, quantum boxes, and lateral potentials in the GaAs/AlGaAs, InGaAs/InP, and InAs/AlSb material systems.

1985-1988 - Staff Member, Massachusetts Institute of Technology Lincoln Laboratory, worked in the Optical Communication Group on the development of a satellite-to-ground free space optical heterodyne communications link.

Dr. Jayaraman joined Optical concepts in January 1994 as Principal Scientist working in the development of long wavelength IR VCSELs.

FRANK H. PETERS

Frank Peters received his Ph.D. in Engineering Physics, McMaster University, Hamilton, Ontario, Canada in 1991. His thesis work developed spatially resolved and polarization resolved electroluminescence in 1.3 uM semiconductor lasers. This results of this research revealed important information strain, scattering and absorption in the active region of lasers. The results were correlated with the spectral output and performance of lasers. A theoretical model was developed which allows device designers to design lasers with predicted spectral outputs and superior performance and efficiency. Dr. Peters has received many scholastic awards and fellowships and has published over 30 papers in recognized technical journals.

1991 to 1993 - Post Doctoral Researcher, ECE Department, University of California, Santa Barbara, CA. Studying the electrical and optical properties of vertical cavity surface emitting lasers (VSCEL). Development of VCSELs for high speed and high power applications with an emphasis on optoelectronic packaging of devices.

1993 to 1994 - Principal Scientist at Optical Concepts Inc. Lompoc, California.

GERALD D. ROBINSON

Gerald D. Robinson retired from Rockwell International 1965 - 1989 where he was a member of the technical staff. He headed the optoelectronics processing laboratory for process development, fabrication, and packaging GaAs fiber optic integrated receivers and transmitters. Responsible for development and fabrication of high electron mobility, HEMT, MBE, INP and GAAS Ternary and quamtermary super lattice structured microwave and millimeter wave integrated circuits. Developed processes for fabricating mocvd grown laser diodes and fabricating mocvd grown laser diodes. Also responsible for process development of planar, multiple implanted digital integrated circuits. Prior to joining Rockwell, he was employed by MRDC, Anaheim, CA, where he headed the processing laboratory for successful transfer of GaAa IC process into pilot line facility. He also developed thin film hybrid circuit processing procedures for the fabrication of x-band radar receivers for the F-111 Aircraft.

Gerald Robinson joined Optical Concepts, Inc, in January 1993, and is currently developing processing procedures for fabrication of high temperature semiconductor devices and ICs. He is also developing procedures for lift-off of semiconductor active layers, devices and ICs for Van Der Waal bonding to thermally conductive substrates. Mr. Robinson has recently developed processes for the fabrication of photolithographically defined planar microlenses for vertical cavity surface emitting lasers (VCSELs).

JEFFREY W. SCOTT

Jeff W. Scott received the B.A. in Physics from the University of California at Berkeley in 1983. From 1983 to 1987, he was employed at Harris Microwave Semiconductor Corporation in Milpitas California, as a R&D process engineer for GaAs Monolithic Microwave Circuits (MMICs). Since 1987 he has been pursuing the advanced degree program at the University of California at Santa Barbara (UCSB), College of Electrical and Computer Engineering. In 1989, he received the MSEE in Solid State Electronics. He has recently (December, 1994) completed the requirements for the Ph.D. EE degree in Solid State Electronics under Professor Larry A. Coldren, Director of the Optoelectronics Center at UCSB. His thesis centered on GaAs Based Vertical Cavity Surface Emitting Lasers (VCSELs).

1. Introduction

Vertical Cavity Surface Emitting Laser (VCSEL) technology is a rapidly growing field. In the last few years GaAs based vertical cavity surface emitting lasers have demonstrated excellent properties. Lasing above 100°C, modulation bandwidths to greater than 8 GHz, output power stability over a 70°C range and single mode operation above 1 mW, have been demonstrated simultaneously in index-guided structures. Modeling work has shown these properties to be within the control of the device designer. These properties indicate that vertical cavity surface emitting lasers can be used as sources for optical communications. In spite of the positive qualifications of VCSELs, they have not yet penetrated commercial markets. The primary reasons for this are centered around growth, reliability and packaging of VCSELs. The purpose of the Phase II effort was to fully develop low power, high-speed VCSELs, to solve the packaging and yield problems, and to demonstrate a potentially low cost, high-speed parallel data link using VCSELs.

During the first year of the Phase II contract, the majority of the device development was completed, yield and packaging issues were initiated, and final system designs were begun. During the first year, Optical Concepts developed low power high-speed top emitting VCSELs with modulation bandwidths above 8 GHz and bottom emitting devices with sub milliamp thresholds which produce over 1 mW of optical power. Improved fabrication procedures were developed to improve device yield, and new packaging procedures for laser and fiber arrays which take advantage of their unique laser beam qualities are under development.

The final year of the Phase II contract has seen the completion of packaged and optical fiber pigtailed vertical cavity surface emitting laser arrays, utilizing both top emitting and bottom emitting VCSELs, and the performance evaluation of different geometry's of lasers. Bottom emitting laser arrays were flip chip bonded onto subcarriers, and both top and bottom emitting devices were pigtailed. Bit error rate measurements were made on top emitting VCSELs at rates

up to the equipment limit of 3 Gbps, packaged high-speed lasers were measured operating in excess of 6 GHz, and bottom emitting devices were demonstrated with integrated microlenses.

2. Background

Vertical cavity surface emitting lasers (VCSELs) out perform in-plane lasers in many respects, and this makes them attractive for high-speed, low cost data links. Their low divergence circular beam relaxes fiber-coupling tolerances compared to in-plane lasers. In-plane lasers require microlenses or lensed fibers to achieve results commensurate with VCSELs coupled into cleaved fibers. VCSELs have threshold currents typically below 2 mA and can be modulated at over 5 GHz frequencies at under 5 mA of drive current. This compares with bias currents of 30-100 mA for in-plane lasers. Low operating currents for VCSELs makes them ideal for low power consumption laser arrays that can be easily heat sunk. The fabrication of arrays of VCSELs on the surface of the laser substrate makes them ideal for flip chip bonding techniques. This also facilitates electrical interconnection to the laser arrays and heat sinking. Another advantage of VCSELs is that they can exhibit inherent single mode operation in a simple device structure. In comparison, DFB in-plane lasers initially require gratings, regrowth and optical coatings on cleaved facets to ensure single mode operation.

A bottom emission, index-guided VCSEL is shown in Figure 2.1a. A typical cavity design is shown in Figure 2.1b along with the optical standing wave pattern as a function of the distance from the substrate. The plot shows the field as resonant inside the cavity with the optical power decaying due to the semiconductor reflectors on either side. Light is extracted into the substrate with roughly 1% of the light coupled out for each round trip oscillation. The inset of Figure 2.1b shows three 80 Å $In_{0.2}Ga_{0.8}As$ quantum wells where the electrical current is converted into light. Quantum efficiencies of at least 30% are typically observed for these devices.

Vertical cavity surface emitting lasers have a single longitudinal mode due to their short cavity. They can, however, have many lateral modes. An index-guided structure has the advantage of

electrical isolation

+

Upper mirror stack
and optical waveguide

Figure 2.1a

990 nm Vertical Cavity Laser Design

Distance [μm]

Figure 2.1b

Optical Spectra

Figure 2.2a

Modulation Response
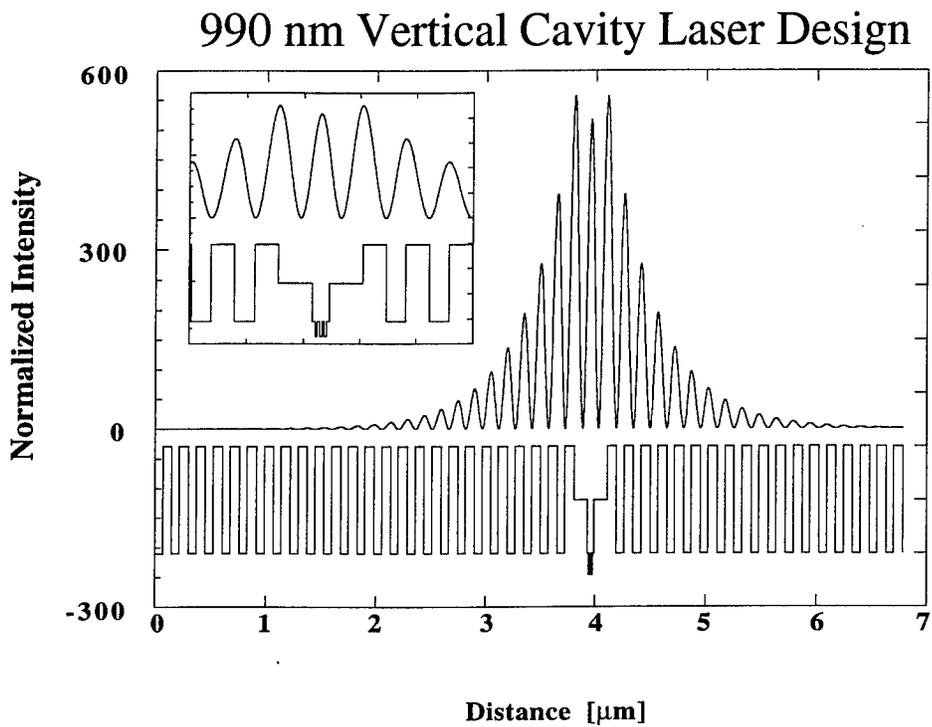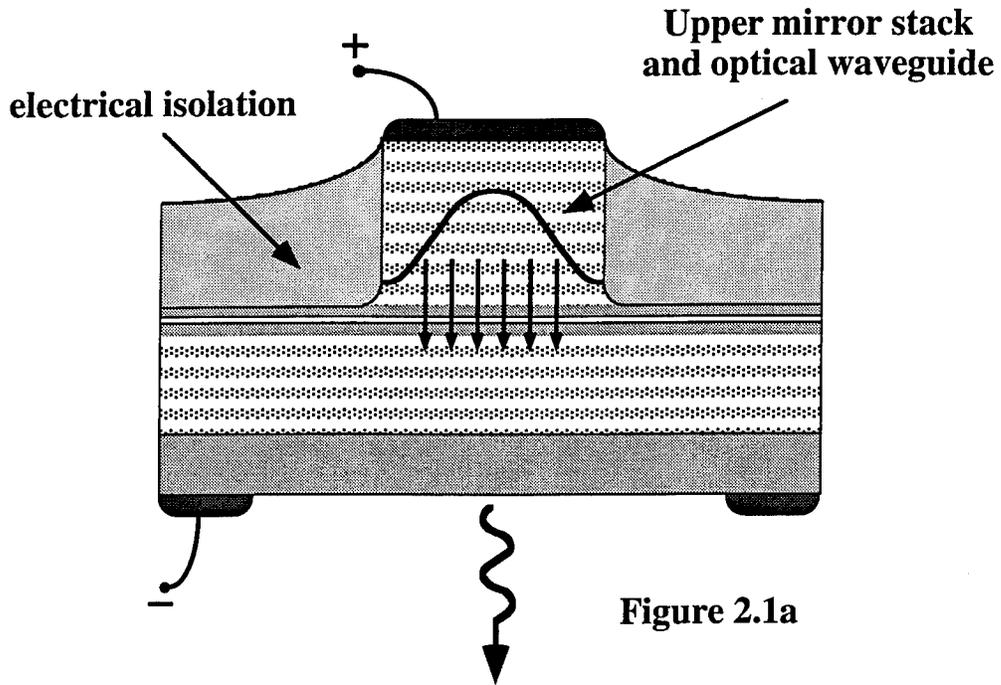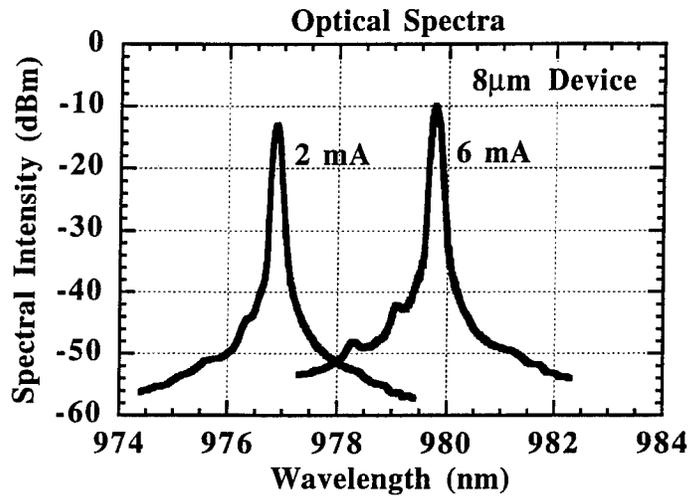
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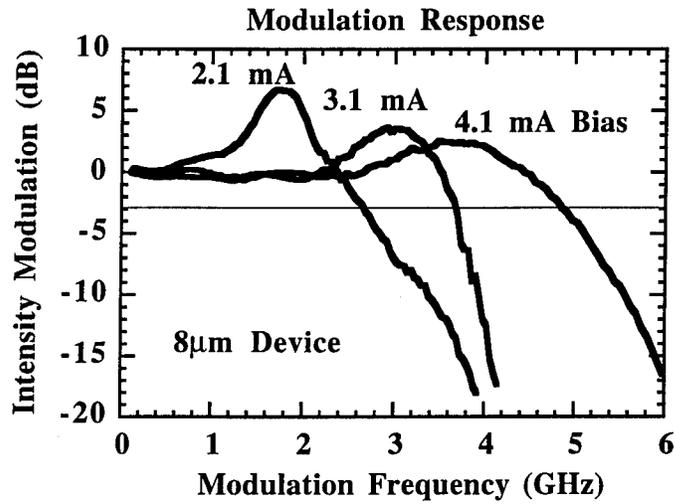
High Temperature Operation
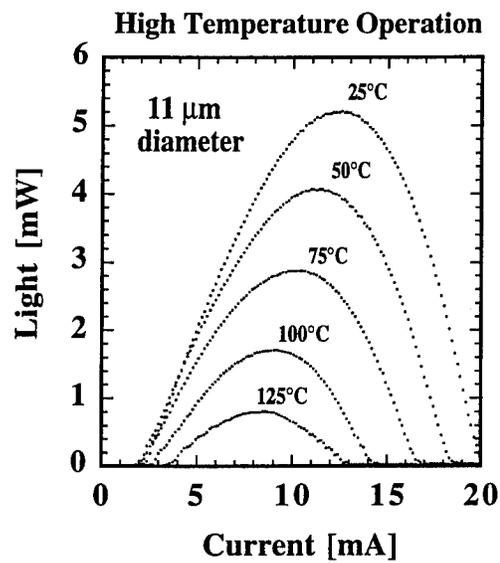
Figure 2.2c

well defined lateral modes. Structures less than 10 μm tend to have single mode operation due to the higher surface-scattering losses of the higher order lateral modes (Figure 2.2a). In addition, temperature compensation can be achieved in the device by offsetting the cavity mode to the long wavelength side of the peak quantum well gain. As the device heats up, the gain moves into resonance, compensating for the lower peak gain which results from carriers thermalizing to higher energy states. The net effect is a stabilized threshold and output powers as shown in Figure 2.2c, making it possible to develop packaged links without thermoelectric coolers or temperature compensation circuits.

Vertical cavity surface emitting lasers are capable of operating at microwave frequencies. A typical laser, as is shown in Figure 2.1a, can be fabricated with more than 2 μm of polyimide insulation layer separating the contact pad from the n material. The RC time constants for a 50 μm diameter contact pad and 500 Ω series resistances are above 10 GHz. Hence, VCSELs can be designed into high performance microwave optoelectronic packages similar to those common for high-speed detectors. Due to the small size of the lasers, they operate at high-speeds under low bias (Figure 2.2b). The high modulation efficiency is a result of the high differential gain of the InGaAs quantum wells and the small modal volume due to the short cavity.

Vertical cavity devices have very low current thresholds and power requirements. The key to the low threshold structure is the high Q cavity formed by the multilayer mirrors grown around the active multiple quantum well structure as shown in Figure 2.1b. The mirrors have reflectivities greater than 99.5% which have resulted in VCSELs with very low current thresholds, typically below 2 mA. This eliminates the need for high current driver circuitry within the optoelectronic package.

InGaAs VCSELs emit a nearly collimated beam of light with typical wavelengths near 1.0 μm. The divergence angle for single mode devices with diameters between 5 and 10 μm is no larger than 6°. Because of this small divergence angle, simple butt-coupling of multimode fibers leads to coupling efficiencies greater than 90%. This coupling efficiency approaches 100% with anti-reflection (AR) coated fibers. For bottom emission VCSELs, the divergence angle within the substrate is only 2° because of the index of refraction for the GaAs substrate. This means that

very little expansion of the optical beam has taken place by the time the light exits from the substrate, greatly assisting efficient fiber coupling.

In summary, index-guided vertical cavity surface emitting lasers have demonstrated the modal, electrical, thermal and modulation characteristics that make them ideal for low power, short haul, high-speed data link applications. In particular, the interface of arrays of lasers with both fiber arrays and with integrated circuits is much simpler than in the case of in-plane lasers. We report below on the progress of this program in the development of packaged VCSEL arrays for data link applications.

3. Initial Phase II Objectives

The stated objectives of the Phase II program were to develop and fabricate prototype vertical cavity surface emitting laser (VCSEL) arrays, packaged with either optical waveguides or optical fiber to form data transmission systems. Initially the specific objectives were:

1. Device Objectives: Perform Simulation, modeling, design and mask fabrication for GaAs VCSELs emitting at 820-850 nm for compatibility with silicon and GaAs detectors.

2. Device Fabrication: Perform necessary material growth, wafer processing, device fabrication, packaging and testing of GaAs VCSEL arrays.

3. Waveguide Technology: Develop compatible processes for polyimide optical waveguides in hybrid multi-chip modules, for interfacing and fan out applications.

4. Fiber Optic Technology: Design and fabricate hybrid packages with hermetically sealed multi-fiber optic interfaces.

5. Demonstration: Perform test, evaluation and assessment of devices derived from task 1 through 4.

Based on our research, the initially specific objectives have evolved into what we believe is the most direct route towards a successful product. The objectives will be discussed in the following subsections.

3.1 Device Objectives

Once all the costs of packaging were taken into consideration, it became apparent that the material costs of the lasers and detectors were a small fraction of any final product. As a result, we feel that it is not advantageous to pursue shorter wavelength VCSELs, but rather to continue to develop VCSELs emitting near 1 μm for compatibility with InGaAs detectors. These VCSELs also have properties that cannot be matched by shorter wavelength devices, such as their temperature insensitivity.

One of the major advantages of VCSELs is their ability to operate over large temperature ranges. Using such devices, no thermoelectric cooling is necessary, greatly reducing the packaging costs. This extended temperature operation has only been demonstrated for longer wavelength (~1 μm) InGaAs lasers. This is largely due to the material composition of the mirrors used for the devices. An InGaAs VCSEL emitting near 1 μm can be designed with binary (GaAs/AlAs) mirrors while a VCSEL operating at much shorter wavelengths requires AlGaAs/AlAs mirrors so that the mirror absorption is minimized at those wavelengths. These mirrors cause two problems for the VCSELs. First, the thermal conductivity of GaAs is much higher than for AlGaAs, and secondly there must be more mirror periods since the refractive index step in the mirror is smaller than for the binary mirrors. The result is that thermal resistance of VCSELs with binary mirrors is much lower than for VCSELs emitting at shorter wavelengths. Thus, one of the greatest advantages of epitaxially grown VCSELs would be reduced by choosing shorter emission wavelengths.

Very efficient VCSELs have been fabricated emitting at 1 μm. This emission wavelength is compatible with high-speed InGaAs/InP detectors. For high performance data links, both detectors and emitters would be flip chip or wire bonded to silicon or GaAs control circuitry.

The cost of detector arrays is minimal due to the large number of detector arrays possible per wafer. Thus, VCSELs emitting near 1 μm and InGaAs detectors will be the devices of choice for the data link.

3.2 Device Fabrication

During Phase II, high performance top emitting and bottom emitting VCSELs were grown and fabricated. The results will be outlined in the Section 4. During the first year, all material was grown by UCSB, and during the second year all material was grown at Sandia National Laboratories according to the subcontracts. Initially it was our intent to transfer wafer growth technology to a commercial supplier, and to reproduce our current VCSEL results with commercially grown material. However, as a result of our investigations we conclude that there is no adequate source for VCSEL material commercially, so it is necessary to produce our own source of material for commercial viability.

All VCSELs fabricated by Optical Concepts have been index-guided pillar structures (Figure 2.1). During Phase II, other geometries of VCSELs have been investigated so that the best fabrication and device geometry would be chosen. Very efficient gain-guided VCSELs have recently been produced[1]. These devices exhibit thermal lensing which helps for the production of high single mode powers. Unfortunately, thermal lensing causes more problems than advantages. As the thermal lens forms, the initial differential efficiency is very high due to the improving overlap between the optical field and the gain region. However, the thermal lens continues to squeeze the optical field, and the overlap between the gain and optical field will start to decrease, resulting in a decreasing differential efficiency. As a result it is highly questionable whether ion implanted, gain-guided VCSELs are appropriate for high-speed data links. Certainly, they are not appropriate for analog links since their behavior is nonlinear, and the thermal time constant, on the order of one microsecond, can lead to pattern dependent effects which degrade link performance. These uncertainties have encouraged the continued

development of index-guided structures, whose properties are appropriate for both analog and digital data transfer.

As an aid to our device comparison, we have examined gain-guided VCSELs fabricated at Sandia National Laboratories. The comparisons between the different VCSEL structures will be made in Section 4.

3.3 Waveguide Technology

The development of polyimide waveguide technology that is compatible with VCSEL technology has been deemed to be beyond the scope of the Phase II investigation, and has been replaced by a concentrated effort toward the fiber optic technologies. As the lasers mature and become proven in a production environment, they will warrant a reconsideration of incorporation in multichip modules. The extensive costs and developmental level of multichip technology makes this collaborative work best left for the future.

3.4 Fiber Optic Technology

Since optical fibers can easily be coupled with VCSELs, development was required for the coupling of fiber optic ribbons with VCSEL arrays. This was a major focus of the second half of Phase II. Two fiber alignment schemes have been suggested: the coupling of fiber ribbons to a glass window for hermetic packages, and the coupling of fiber ribbons directly to bottom emitting VCSELs. For the first coupling scheme, microlenses external to the hermetic seal will be used to focus the light from the VCSELs into the optical fibers. For both coupling schemes, control of the fiber ribbon will be necessary for coupling. During the course of the Phase II investigation, it has become evident that the most immediate market for VCSEL arrays requires the arrays to be low cost. As a result our fiber coupling effort was directed toward the low cost method of direct butt-coupling between lasers and fiber ribbons.

3.5 Demonstration

The following section will outline many of the results obtained by Optical Concepts during Phase II. Both low and high-frequency measurements have been made on top emission and bottom emission devices.

3.6 Additional Tasks

A number of additional tasks were required after the first year of investigation for the completion of the project. The first additional task was centered around packaging technologies, since any successful product must be reliable and in a package. Therefore, a large effort has been made to ensure high packaging yield. The second task was an investigation into driver circuitry appropriate for a high-speed data link.

4. Results

During the first half of Phase II we concentrated on vertical cavity surface emitting laser (VCSEL) development. As a result, we have fabricated VCSELs that operate at record modulation efficiencies, and also devices with near record threshold currents that produce more output power than existing devices with equivalent thresholds. Even with these achievements, there is still much room for the devices to be optimized for better performance. In parallel with our device research, we are in the process of developing packaging technologies that are critical for any successful product. Initially the material growth technology will be described, including enhancements made by Optical Concepts. This will be followed by fabrication, device results, packaging technologies, packaging design and finally system designs.

4.1 Vertical Cavity Surface Emitting Laser Designs

During the Phase II program, design work was done for two types of vertical cavity surface emitting lasers (VCSELs), intra-cavity contacted VCSELs and etched post VCSELs. The design philosophy behind the first structure, the intra-cavity contacted laser, was to place both contacts on the top surface of a semi-insulating GaAs substrate. This flexible design allows for top or bottom emission and wire bond or solder bump contacts. The semi-insulating substrates make the parasitic capacitance of all these configurations very low, realizing the maximum flexibility in packaging without compromising the lasers' the high-speed capability.

At the same time, considerable effort was made in refining the design of the etched post VCSEL. During the phase II contract most of the refinements were made in the fabrication of the devices, as described in a following section. The collaboration with the University of California at Santa Barbara and Sandia National Laboratories did produce significant improvement in reducing the resistivity of the distributed Bragg reflectors (DBRs), resulting in higher performance devices.

4.1.1 Material Growth Technology

Growth of vertical cavity structures places stringent demand on the accuracy and uniformity of the epitaxial technique. In the case of InGaAs lasers operating at wavelengths near 1 μm, a 1% deviation from the designed thickness results in a 10 nm shift in operating wavelength. For temperature stabilized operation, the offset between the Fabry-Perot cavity mode and the room temperature photoluminescence peak of the quantum wells should fall within 10 nm of design across the wafer. It is necessary, then, to have a highly uniform and accurate growth system. Both metal organic chemical vapor phase epitaxy (MOVPE) and solid source molecular beam epitaxy (MBE) systems can be designed to achieve the required uniformity. To achieve accurate growth it is very helpful to incorporate *in-situ* control. Optical Concepts used MBE to produce its first prototype devices and has been developing growth control techniques in collaboration with UCSB. The high-frequency top surface emission devices discussed in section 4.1.2 were the first devices to be grown at UCSB using *in-situ* control. The technique, based on the optical reflectance spectrum, can be adapted to either MBE or MOVPE systems. In this section the

specific growth conditions used will be outlined, followed by a description of the *in-situ* control setup. Finally the experimental results of an optically monitored growth will be presented and discussed.

The growth is done in a Varian Gen II MBE system with the wafer under rotation. All layers except the active region were grown at 600°C at a growth rate of ~1 μm / hr. The pseudomorphic InGaAs quantum wells are grown at 520°C to minimize indium evaporation. Five second smoothing pauses are used on either side of the quantum wells. The entire structure is grown with an over pressure of cracked arsenic. High energy electron diffraction (RHEED) is used to calibrate the rates prior to growth. All the aluminum alloys are formed using digital superlattices, allowing furnace temperatures to be held constant for repeatability. By maintaining constant furnace temperatures, the growth repeatability is improved. Nevertheless, RHEED has its limitations due to the decay of the signal strength with increasing island growth. The introduction of *in-situ* control improves the accuracy, leading to a manufacturable process.

Our technique is a modification of the approach developed by Chalmers[2] at Sandia. In his approach, growth is interrupted when the bottom mirror and ~95% of the central cavity are complete. The wafer is cooled and moved to an optical port. White light is reflected off the surface and the reflectance spectra is analyzed. By comparing with the theoretical curve, one can determine the deviation from design and adjust the remaining growth to compensate. The entire process of cooling, measurement and repositioning the wafer takes about 1 hr. Since the active region growth is complete and the interruption occurs in heavily doped p-type material, the effects of unintentional impurity incorporation is minimal. We have simplified this technique by taking advantage of the pyrometer optical port, allowing optical monitoring of the wafer surface *in the growth position*. Measurements are made while the substrate temperature is ~200°C, so that the entire time from interruption to resumption of growth is under 20 min without moving the wafer. In addition to minimizing surface contamination and furnace drift during measurement, this technique is applicable to any MBE system having an axial pyrometer port. The pyrometer reads signals primarily in the infra-red, and thus the temperature reading becomes

Wafer in
Growth Position

MBE
Pyrometer Port

Lens

Tungston
Source

1x2 Coupler

Multimode
Fiber

Spectrum

Optical
Spectrum
Analyzer

Spectrum
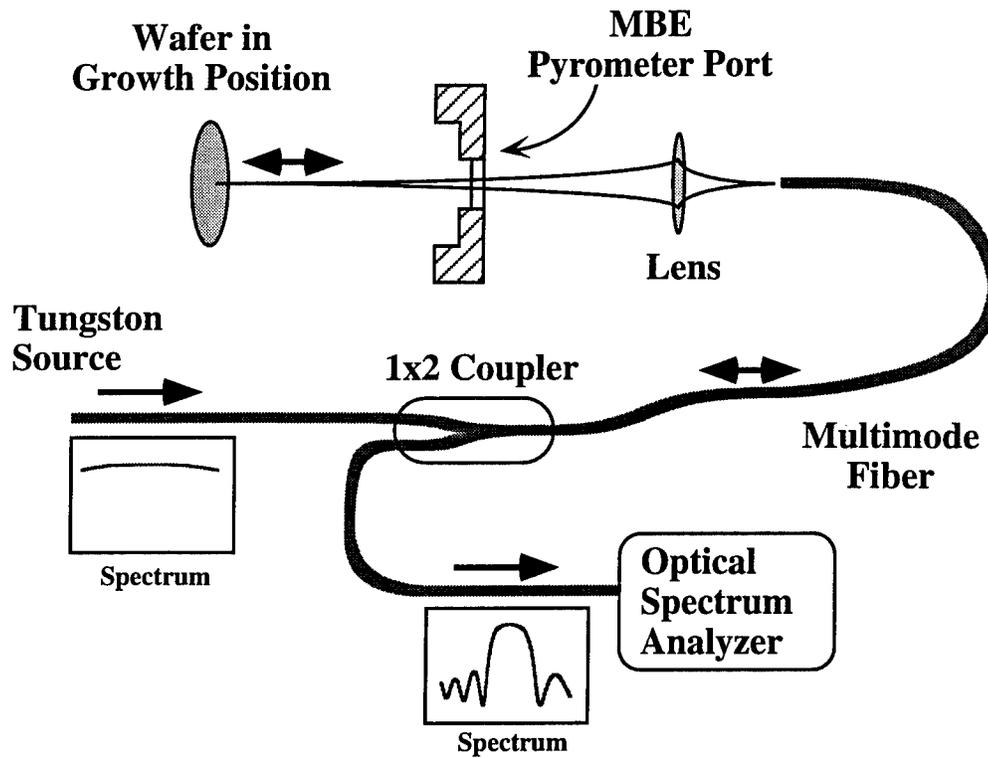
Figure 4.1a

inaccurate once infra-red distributed Bragg reflectors (DBRs) are grown on the surface. There is, therefore, no loss in control if the port is used for optical access during growth.

The *in-situ* apparatus used is depicted in Figure 4.1a. White light is launched down a multimode fiber, passed through one arm of a 1x2 fiber coupler and positioned in front of the optical port. Free space optics are then used to capture the diverging beam and focus it on the wafer surface. The light spectrum is modulated by the surface reflectivity and the reflected beam retraces its path back to the fiber coupler. The signal is coupled into the other fiber output and connected to an optical spectrum analyzer. It is a simple matter, then, to compare the expected spectrum with the signal and make corrections to the growth if necessary. By using optical fiber, the modifications to the MBE system are minimal.

The control procedure used will now be described. First, RHEED is used to set the initial growth rates. Next, the first 10 periods of the bottom mirror are completed and the growth is interrupted. The wafer is cooled to 200°C which can be measured by a thermocouple. The reflectance spectrum is taken and compared with the calculated spectrum at 25°C as shown in Figure 4.1b. Comparing the mirror band edge resonance near 1100 nm, the difference is 12.5 nm. It is preferable to make comparisons on the long wavelength side of the spectrum where the effects of above-band absorption can be avoided. Earlier *in-situ* spectral measurements on VCSEL material showed that the optical spectrum shifts 0.84 Å/°C. Thus the 175°C temperature difference corresponds to a 14.7 nm shift. The measured spectrum is therefore 2.2 nm shorter than design and hence needed no correction. Growth was resumed until the bottom mirror and all but 390 Å of the optical cavity were grown. The wafer was again cooled to 200°C and the spectrum was taken. The data and calculated spectrum at 25°C are shown in Figure 4.1c. The cavity modes differ by 11.3 nm. Again, including the expected shift, the growth is determined to be short by 3.4 nm. Having determined the optical mode was within design tolerances, the growth was completed.

After growth, the wafer was removed and cleaved for processing and analysis. The measured and calculated spectrum at the center of the wafer taken by a spectrophotometer are shown in
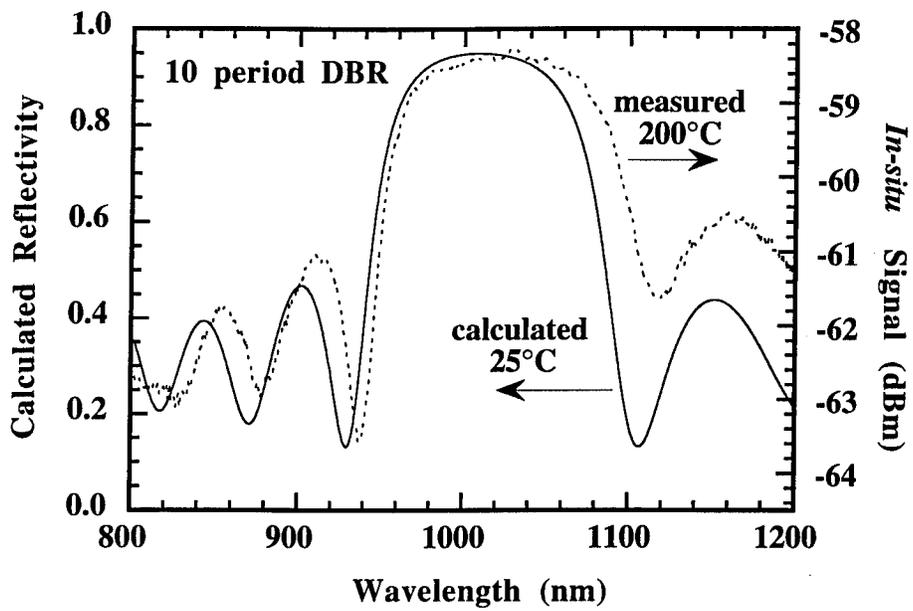
Figure 4.1b
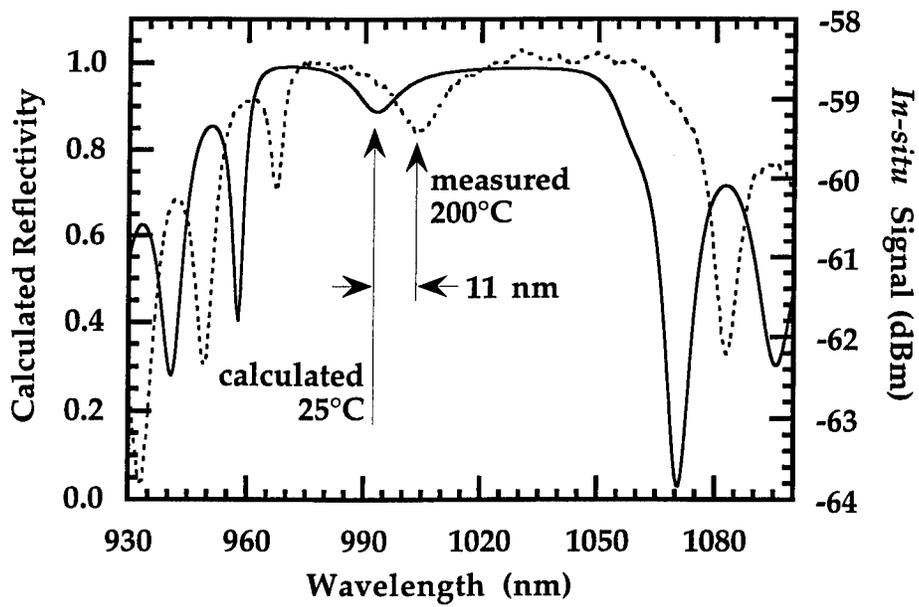
Figure 4.1c
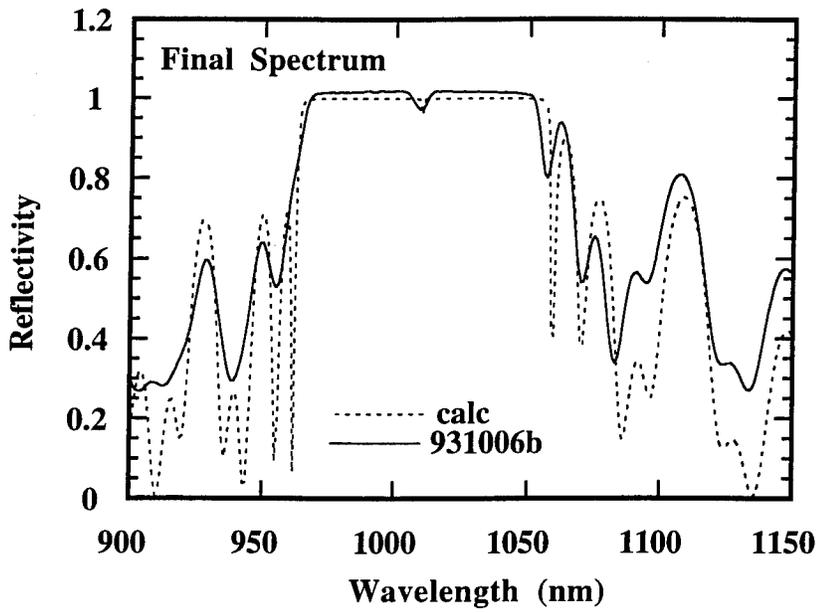
Figure 4.1d
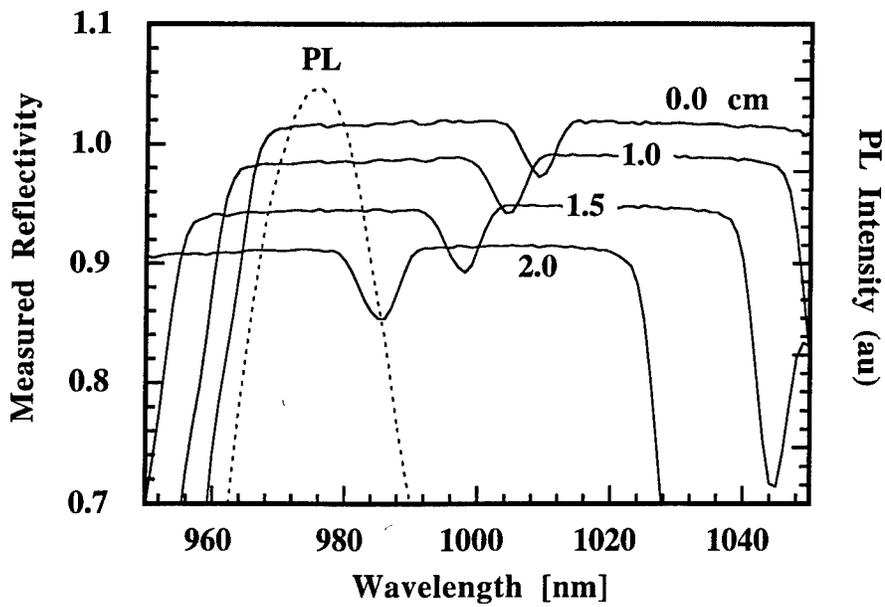
Figure 4.1e

Figure 4.1d. The measured cavity mode is at 1009 nm, 1 nm short of the design value of 1010. The upper mirror was removed from a piece 1.5 cm from the center to measure the room temperature photoluminescence (PL) signal. The PL signal and the measured reflectivity spectra at various radii are shown in Figure 4.1e. The PL peak is at 975 while the cavity mode varies from 1009 nm at the center to 985 nm at a radius of 2 cm. A 3% growth variation is typical for the Varian Gen II system. As a research tool, this variation allows the study of a variety of gain offsets between the gain peak and the cavity mode. State of the art MBE systems for 4 inch wafers have a growth variation in the range of 1%. Combined with this control technique, these systems are sufficient to repeatably produce high performance VCSEL material. During Phase II Optical Concepts attempted to work with material growth companies to develop this capability commercially. Unfortunately, due to the infancy of the commercial VCSEL market, material growth companies were not willing to invest the time and energy to make the necessary improvements in their material growth capabilities. As a result Optical Concepts is currently in the process of developing its own growth facilities to assure an available supply of acceptable material.

4.1.2 Intra-Cavity Contacted Design

The intra-cavity contacted design allows the use of ring contacts by placing thin p-type and n-type layers within the optical cavity to distribute current. This design bypasses the distributed Bragg reflectors and makes it possible to have both contacts on the top surface of a semi-insulating GaAs substrate. The result is a very low capacitance device which can be scaled to very small diameters. The small modal volume and low capacitance yield a high-speed, sub-milliamp threshold laser which is ideal for low current, high-speed data link applications.

A schematic of the structure fabricated during this program is shown in Fig. 4.1f. The inner ring contacts the p-type layer, the outer ring contacts the n-type layer. The current constriction blocks the shunt path, forcing the current into the optical mode. The constriction can be fabricated using grown-in or implanted blocking layers, a wet oxidation process, or a selective wet etch as was done here. The top mirror was made using an undoped semiconductor distributed Bragg

active region

current constricting
undercut

＋

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Semi-insulating GaAs
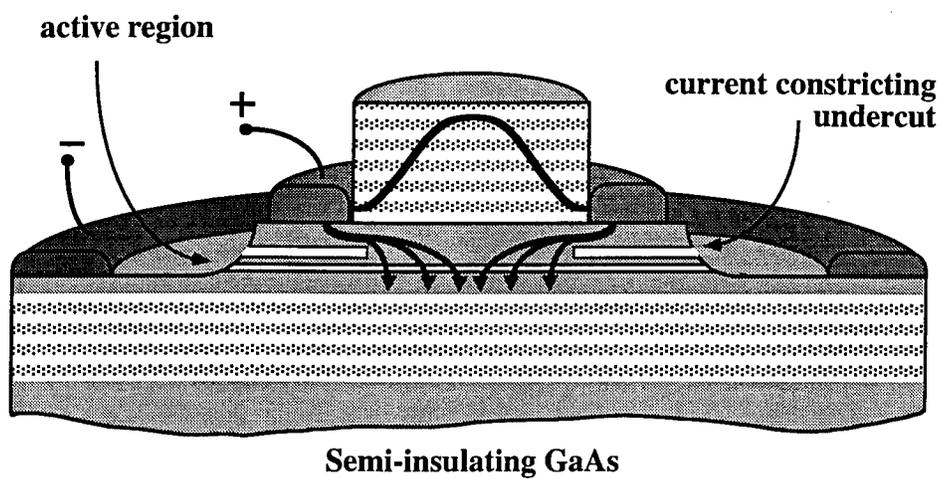
Figure 4.1f

reflector, although it could also be made using dielectric layers. The design of the intra-cavity layers, including a high-performance single-mode current-apertured structure, have been patented by Optical Concepts (US Patent No. 5,343,487.)

The main advantages of the intra-cavity structures are in the realization of efficient, high-speed small-diameter VCSELs. Emission can be from either the top or bottom, depending on the respective mirror reflectivities. The ring contacts ensure that the ohmic contact areas are sufficient to provide a reliable, low resistance contact even for very small lasers. The current constriction avoids introducing surface recombination or damage in the active region. The design has the potential for high reliability, although more work remains to be done in this important area.

Detailed device models for the current flow and current-to-light properties of these laser have been developed which allow the analysis of potential designs prior to fabrication. The models allow the prediction of such properties as the threshold current vs. temperature, optical and power conversion efficiencies and variation in device performance with size. These design tools reduce the number of experimental runs required to realize a desired set of device characteristics.

4.1.3 Etched Post Vertical Cavity Surface Emitting Lasers

4.1.3.1 Wafer Design

A schematic showing the design of a typical MBE grown bottom emitting vertical cavity surface emitting laser (VCSEL) is shown in Figure 2a. The structure is made by positioning an active cavity between two quarter wave DBR mirrors. As with the top emitting device, three 80 Å $In_{0.2}Ga_{0.8}As$ quantum wells are positioned around 80 Å GaAs barriers. On either side of the quantum wells are 100 Å GaAs smoothing layers before the carrier confinement layers. At this point the design diverges from the top emitting device. The carrier confinement layers are made up of $Al_{0.5}Ga_{0.5}As$ on both sides of the quantum wells, with thicknesses such that the total active cavity is one wavelength. The active region is doped $1x10^{18}$ cm^{-3} part way into the confinement layers, and the rest of the active region is undoped.

The MBE grown bottom emitting device is grown with an 18-20 period GaAs/AlAs p-doped top mirror followed by a GaAs layer designed to phase match the reflectivity with a top gold contact, increasing the total reflectivity of the top mirror to ~99.9%. The bottom mirror is made up of 17.5-19.5 periods of GaAs/AlAs layers. Since the current must pass through both mirrors, the mirrors are linearly graded from one binary to the next using 20 Å digital alloys over 180 Å. The doping profile is also modulated so that the doping is 1×10^{18} cm^{-3} in the layers and 5×10^{18} cm^{-3} at the interfaces. This improves the conductivity of the mirrors with only a small increase in the optical absorption. To reduce this absorption, the first four mirror periods are only heavily doped at interfaces located at a null in the optical standing wave. This growth procedure (initially done in 1992) resulted in the highest output powers achieved in VCSELs[3] to date. Other mirrors, such as AlGaAs/GaAs mirrors, have been grown with better electrical characteristics than the binary mirrors but at the expense of a higher thermal impedance. Since the bottom emission devices are intended to be flip-chip mounted, the ternary mirror systems were not developed. Instead, delta doping and carbon sources were investigated as methods of reducing the voltage drop across the DBR mirrors.

During the second year of the Phase II effort, two improvements occurred in DBR mirror technology. The first improvement was the development of low resistance mirrors by careful bandgap engineering. At UCSB, delta doping in p-type AlGaAs/GaAs DBRs was successfully demonstrated. A pair of delta dopings creates an electric dipole which compensates for a linear grade in the bandgap. The delta doped heterointerfaces in the p-mirror have a flat valence band, resulting in greatly reduced mirror resistance. In the MBE system the p-type dopant, beryllium, has limited incorporation into AlAs at standard growth temperatures, resulting in dopant segregation. As a result, successful delta doped mirrors are produced in only AlGaAs/GaAs DBRs. The penalty is that thicker mirrors are required for a given reflectivity and that the optical penetration and associated free carrier losses increase for the AlGaAs mirrors. The segregation effect has been confirmed by low resistance AlAs/GaAs mirrors that were grown at reduced temperatures. The increased optical losses, however, of the low temperature mirrors were unacceptable.

The second major improvement during the last year is the demonstration by Sandia National Laboratories that very high quality epitaxial material can be grown using MOVPE instead of MBE. The Sandia material uses carbon as the p-type dopant, that has high saturation levels and low diffusivity compared with beryllium. As a result material from Sandia has produced the lowest voltage and highest efficiency VCSELs to date. Further more the scientists at Sandia have fully developed flat valence bands in the p-DBR through careful bandgap engineering similar in nature to the UCSB design. The difference is that the carbon doping is assured of incorporating as designed, so that continuous parabolic grading and uniform doping sheets have been used. The impressive reduction in mirror resistance make the intra-cavity and etched pillar structures comparable with respect to device resistance. It is the packaging and reliability which will determine what structure will ultimately be most useful.

Vertical cavity surface emitting lasers operate at high-speed under low bias. This has not yet been fully optimized, therefore this property has been investigated. The question asked is how fast can a VCSEL operate at a minimum input power. This is an important issue for a high data rate package. If there is no active temperature control, then it is important that the devices will still operate at the required speed, even if the temperature increases. One interesting result that has come out of studying the modulation bandwidth of VCSELs is the conclusion that it is desirable to use the highest possible cavity finesse.[4] This is significant for a number of reasons. To begin with, in existing VCSELs the goal has been to obtain the highest possible output power by decreasing the cavity finesse. This was the case for the devices whose very high relaxation oscillations were measured and for the devices which showed the high modulation current enhancement factor of 5.7 GHz/$\sqrt{mA}$. It has been shown that the most important characteristic of a VCSEL to achieve high modulation is the effective modal volume.[5] By reducing this as much as possible, the relaxation oscillation frequency can be maximized for a given input current. A reduced modal volume can be accomplished in two ways. First, the area of the active region can be minimized, and secondly the penetration depth into the mirrors should be minimized.

The first method of reducing the active region, minimizing the active area, is the simplest initially but comes with some inherent problems. Although it is straight forward to make small

devices, they do not necessarily work, due to size dependent loss mechanisms. Therefore it is necessary to minimize all size dependent loss mechanisms such as surface scattering and diffraction.

The penetration depth has not been fully optimized in vertical cavity structures to date. Typically it has been desirable to ensure that the vertical cavity design structure can also be fabricated into an in-plane laser for material characterization. This has required that the active area forms a waveguide for an in-plane laser, and often means that the active area is thicker than necessary. This can be easily demonstrated using GaAs based VCSELs which have been extensively studied. Figure 4.1g shows the active area and first few mirror periods of a typical structure. The active area is one wavelength in length so that the peak of the electric peak is situated over the quantum wells. This requirement can also be accomplished using a zero phase cavity where the quantum wells are situated inside the mirrors themselves. This structure can be seen in Figure 4.1h. Here the effective length of the active region has been significantly reduced. Secondly, the penetration depth into the mirrors is minimized by maximizing the refractive index step in the DBR mirrors. This is a good reason to use binary GaAs/AlAs mirrors, although the long term stability of the relatively reactive AlAs remains a concern.

The next important change that is necessary to increase the modulation bandwidth of the devices is to increase the bias that can be applied to the structures. The most practical ways to do this are to decrease the losses (resulting in heat generation) and to improve the heat flow from the device. Decreasing the losses in a device is probably the most important aspect of vertical cavity design. Increasing the heat flow from a device is based on two parameters: the thermal conductivity of the material and the length of the heat flow. GaAs/AlAs mirrors have much better thermal conductivity than AlGaAs/GaAs mirrors. The length of the heat flow can be minimized by flip chip bonding the device (described in the next section), or by substrate removal. Optical Concepts is currently developing a flip chip bonding capability for maximum heat flow from VCSELs, and has experience in substrate removal technology.

Standard VCSEL

Figure 4.1g

Reduced Cavity VCSEL
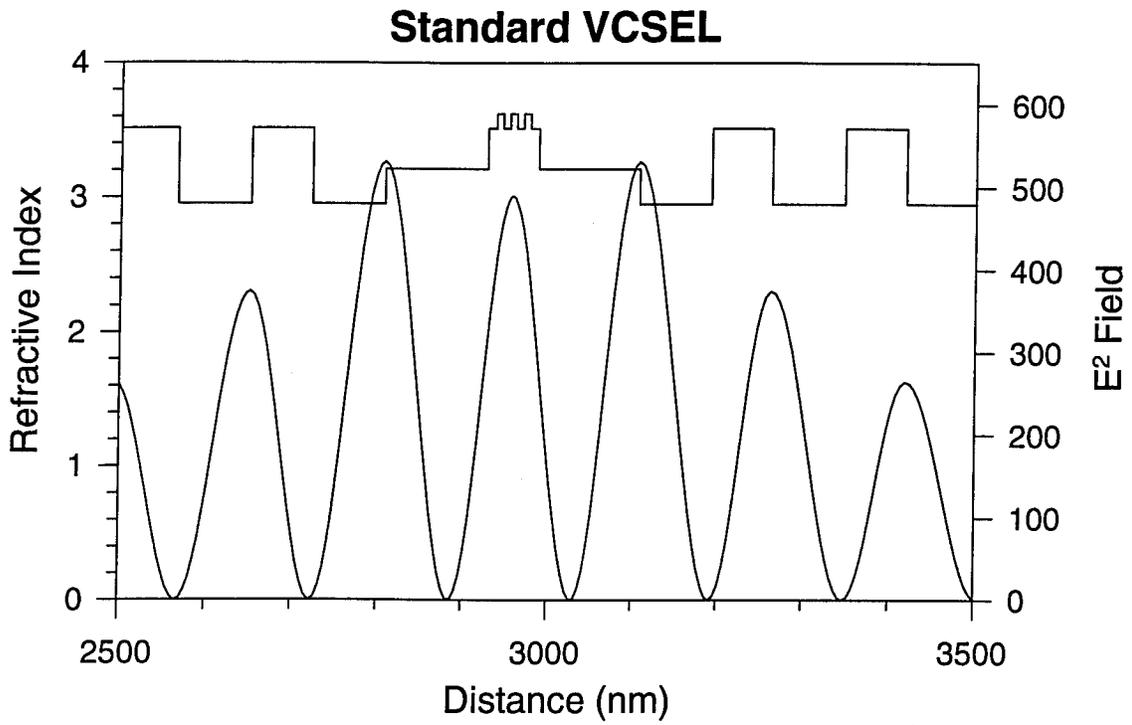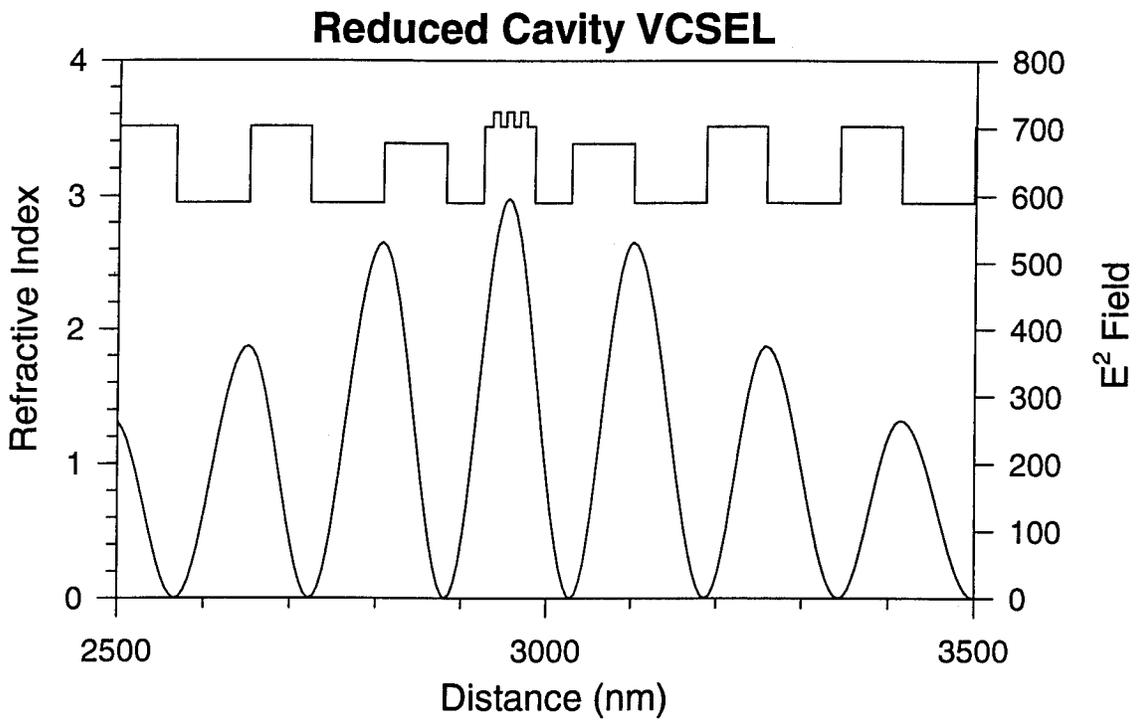
Figure 4.1h

The last important issue is the inherent speed limitations of the package and device. Devices on conductive substrates can have a significant parasitic capacitance under the bonding pads, and therefore it is important to minimize the resistance of the device. For pillar contacted devices, it is possible to greatly reduce the parasitic capacitance by raising the contact pad away from the surface with an insulator, although here the problem becomes reducing the thermal resistance of the mirrors. There must be a trade off between active-layer volume, thermal conductivity and the mirror resistance.

4.1.3.2 Fabrication

This section describes in detail the current fabrication methods for bottom emitting etched post vertical cavity surface emitting lasers (VCSELs) which have evolved during the Phase II effort. The procedures for the fabrication of VCSELs have been designed to utilize conventional III-V processing equipment in a class 1000 clean room environment. These procedures incorporate established techniques whenever possible or modified techniques when necessary to accommodate unique requirements. Process procedures which have been developed to facilitate fabrication of VCSEL arrays include double resist lift-off processes, an improved n and p-type ohmic contact process, and a microlensing procedure.

The fabrication sequence for the bottom emission devices is simpler than the intra-cavity structures, although the solder bump process adds to the process complexity. The simplicity of the process leads to very high yields, an important issue for manufacturing low cost arrays. The most critical point is the formation of the top contact which acts as electrical contact, optical reflector and a self-aligned etch mask for the formation of the optical waveguide. Furthermore, single transverse mode operation can be achieved by using device diameters below 8 µm. We have, therefore, focused on developing a self-aligned alloyed ring contact and developing metallization compatible with the solder bump process. The fabrication of the laser shown in Figure 4.1i is described below. To facilitate the description, the dimensions given will be for an 8 µm diameter device.

Ti/Au/Ni reflector

InGaAs active region

Au/Zn/Au contact

p-GaAs/AlAs mirror

solder barrier

SiNx

GaAs substrate

n-GaAs/AlAs mirror
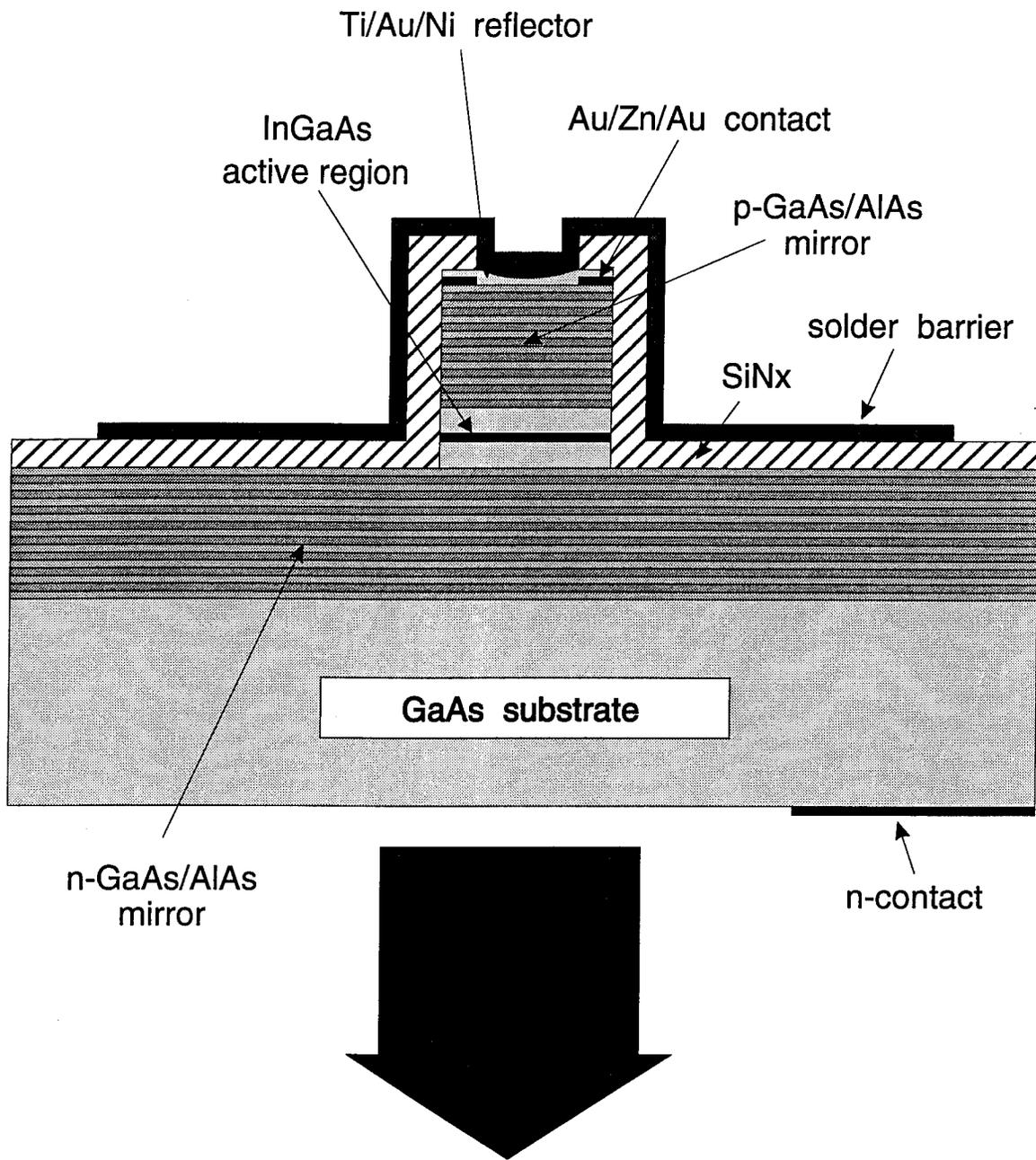
n-contact

Figure 4.1i

The first step in the process is to form the top contact. This begins by depositing the p ohmic metal on the surface using a liftoff mask to leave a 4 μm hole. Then an 8 μm dot of Ti/Au/Ni is deposited by liftoff, keeping the Ti to a minimum thickness to make use of the high reflectivity of the Au in the center where the optical mode is strong. Next, a highly selective cyanide gold etch is used to etch off the p ohmic in the field using the Ni as an etch mask. This procedure leaves an 8 μm dot on the surface with nickel on the surface to act as an etch mask in the Cl reactive ion etch (RIE) with a 2 μm ring contact of Au/Zn/Au underneath to make electrical contact. The next step in the process is the definition of the optical waveguide by low pressure RIE. A HeNe laser is reflected off the surface and the signal is used to monitor the etch depth. The device is etch into the cladding just above the active region, constricting the current injection while avoiding exposed active surfaces. After etching, the lasers are encapsulated with PECVD silicon nitride, isolating the field and protecting the waveguide surface. A 4 μm window is opened in the center of the top by CF_4 plasma etching to allow electrical connection.

Once the lasers are complete, they must be prepared for the solder bumps. Using a thick liftoff mask, a Ti/Pt/Au metallization is deposited in a 30 or 50 μm dot. To ensure step coverage, the evaporation is done at an angle with the substrate rotating. The processing now turns to the backside. The Indium solder bumps (2-4 μm thick) are then deposited by evaporation and liftoff. The wafer is lapped and polished, and then n-type ohmic contacts are deposited in a bar pattern allowing for die separation and light emission. Finally, the n and p ohmics are alloyed simultaneously.

Many variations to this process are possible including the generation of both p and n contacts on the top side. Variations will be explored as time and results indicate the most promising path. In any case, Optical Concepts is using devices generated with the above process to define the package sequence and study the contact reliability.

4.2 Device Performance

4.2.1 Intra-Cavity Contacted Laser Performance

This section presents the measured characteristics of the intra-cavity contacted VCSELs shown in Figure 4.1f. First, the DC characteristics such as LI, IV and spectral measurements are shown. The smaller lasers have sub-milliamp threshold currents and single transverse mode operation while the larger 15 μm multimode lasers have a threshold current density of 1 kA/cm^2 and external quantum efficiency of 46%. While the DC properties of VCSELs are fairly well known, there is much less data on their high-speed properties. Using the unique configuration of these intra-cavity contacted lasers, high-speed measurements can be made on wafer. The issues of packaging and the associated parasitics are avoided by high-speed probing so that very clean measurements are made.

The high-speed characterization begins with small signal scattering parameter measurements using a vector network analyzer. From the S_{11} measurements an equivalent circuit for the 7 μm laser is constructed. From the S_{21} measurements the modulation response and carrier transport limits are determined. The 7 μm diameter laser has a 3 dB bandwidth in excess of 8 GHz at a bias of only 4 mA. The 3 dB electrical bandwidth vs. the square root of current above threshold is plotted for the various diameter devices. The slope of the plot yields the Modulation Current Efficiency Factor (MCEF) and is shown to agree with theory. The 7 μm diameter laser has a very high value of 5.7 GHz/√mA, higher than any in-plane laser reported to date.

After the microwave measurements, large signal modulation of the lasers is used for Gigabit/s digital data transmission. For the first time, on-wafer probed high-speed Bit Error Rate (BER) measurements have been made. The BER measurements of varying diameter laser arrays show that all the lasers are capable of data transmission at 3 Gbit/s, the maximum rate of the test equipment, with no error floor. One promising application of these high-speed laser arrays is to extend computer buses off the board using multimode graded index fiber arrays. Sixty-four electrical channels operating at 100 MHz could be multiplexed up to 8 channels at 1.6 Gbit/s

with commercial GaAs circuits and then transmitted in parallel using the laser arrays, making maximum use of the optical links while avoiding complicated microwave circuits. Such a link has an aggregate data rate in excess of 13 Gigabit/s. For such applications it would be desirable to use simple on/off modulation of the lasers to minimize the complexity of the driver and receiver circuits. Thus, further measurements were made at 1.6 Gbit/s on the sub-milliamp 7 μm lasers under full on/off modulation conditions. The sensitivity of the BER performance was made for variations between devices and variations of substrate temperature. The laser arrays showed remarkable uniformity, indicating promising application in this area.

The layer structure and doping of the experimental devices are shown in Figure 4.2a. The active region is formed from three 80Å $In_{0.2}Ga_{0.8}As$ quantum wells with 80 Å GaAs barriers. On either side are 100 Å GaAs smoothing layers before the carrier confinement layers. Below the active region is a $Al_{0.25}Ga_{0.75}As$ n-type confinement layer followed by a $Al_{0.1}Ga_{0.9}As$ n-type intra-cavity contact layer. Above the active region is an $Al_{0.5}Ga_{0.5}As$ p-type confinement layer, a AlAs current constriction layer and a $Al_{0.1}Ga_{0.9}As$ p-type intra-cavity contact layer. A selective wet etch is used to etch the current constriction layer to force the current into the optical waveguide. The p-type intra-cavity contact layer consists of a 1λ thick p- layer below a 1.25λ thick p+ layer. The DBR mirror layers are formed from $AlAs/Al_{0.1}Ga_{0.9}As$ pairs, each layer 1/4 optical wave thick. The lower mirror consists of 28.5 periods while the upper mirror consists of 15 periods. The center wavelength of the reflectors and cavity mode were designed for 1010 nm to provide a 20 nm offset from the gain peak on the majority of the wafer. $Al_{0.1}Ga_{0.9}As$ was used instead of GaAs to allow efficient optical pumping of the laser in other experiments.

Along with the layer structure, Figure 4.2a shows the doping profile as shaded regions. The dopants were set back 500 Å from either side of the active region. The n+ Si doping density was $2x10^{18}$ cm^{-3}. The Al content on the n side was kept below 30% to avoid DX center compensation. The p dopant used was Be. The heavily shaded p+ doping density was $4x10^{18}$cm^{-3} while the lightly doped p- was $2x10^{17}$ cm^{-3}. The p+ layer is used to distribute the current while the p- layer acts to diffuse the injected current to reduce current crowding. All doped heterointerfaces used a parabolic grading to minimize the barrier to majority carrier flow
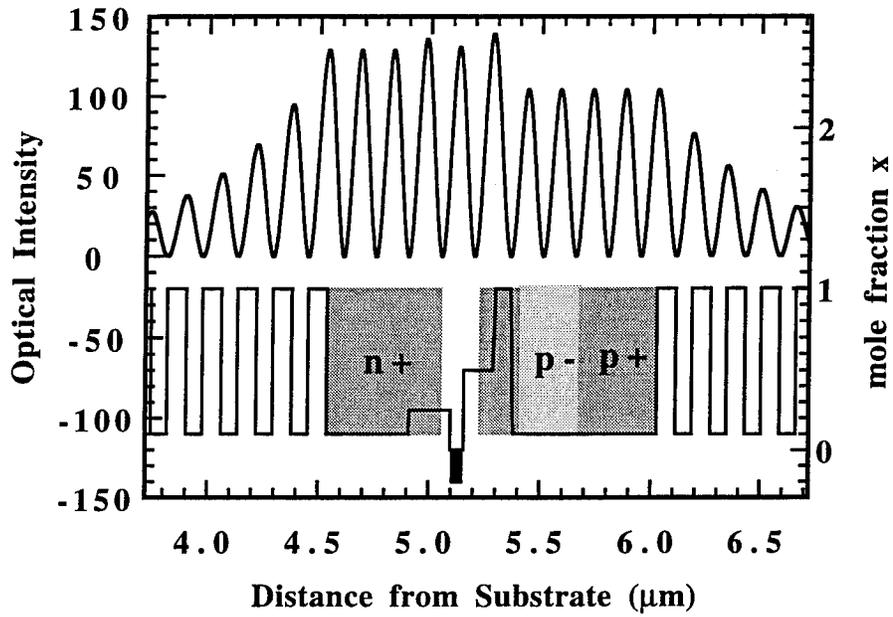
Figure 4.2a
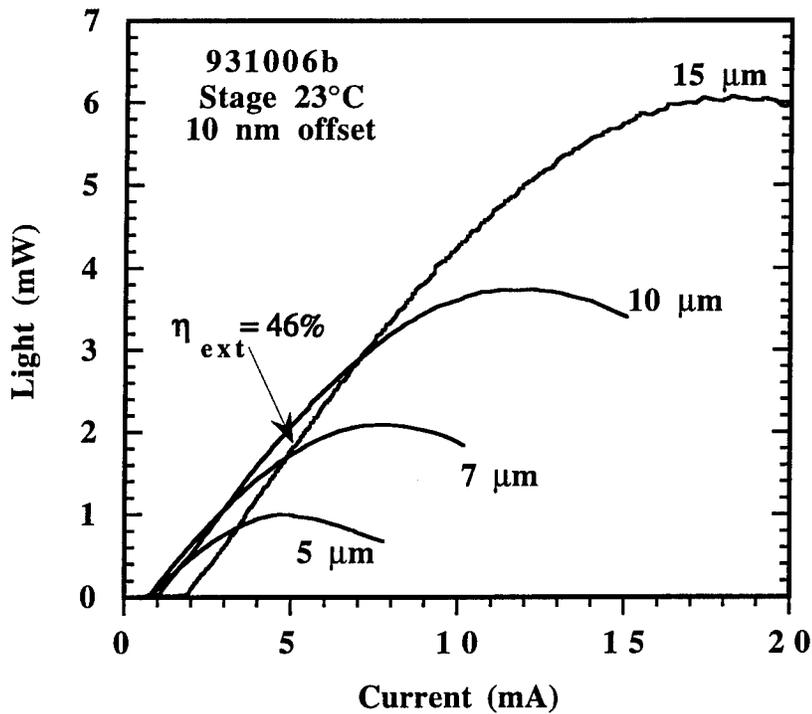
Figure 4.2b

[6] . The DBR mirrors and substrate are undoped. The entire VCSEL structure was grown on a semi-insulating substrate.

The calculated longitudinal standing wave pattern, normalized to the field emitting from the top surface, is also shown in Figure 4.2a. The optical losses are presumed to be dominated by free carrier losses, taken to be 5 cm^{-1} per 10^{18} cm^{-3} for electrons and 11.5 cm^{-1} per 10^{18} cm^{-3} for holes. The threshold gain, determined using a transmission matrix approach, is predicted to be 1500 cm^{-1} or equivalently a round trip gain of 1.32%. The relative standing wave amplitude, at the quantum wells of 131, yields an effective transmission coefficient of 0.87% for the upper surface. The optical efficiency, defined as the fraction of photons generated that escape the device, is thus calculated to be 0.66. Assuming an internal efficiency of 0.8, a typical value in our experience, the expected external quantum efficiency is 52%. Modeling has shown, however, that limited optical overlap with carriers injected near the periphery of the device leads to additional losses. The measured external differential efficiency of 46% indicates that the optical modeling is effective in predicting the device performance.

Lasers with four waveguide diameters were fabricated: 5, 7, 10 and 15 μm. The lasers were fabricated into two kinds of arrays. In the high density arrays, all four sizes were repeated in close proximity to allow direct comparison between devices. Although the lasers are high-speed devices, the probe pad configuration is not suited to high-speed testing. The high-speed arrays used 2x18 arrays of a single diameter laser on 250 μm centers. This makes them suitable for coupling into standard multimode ribbon fiber arrays. In addition, each laser is accessed using a 600 μm long tapered coplanar transmission line to make the transition from the two ring contacts to 75 μm pitch, ground-signal-ground probe pads compatible with a high-frequency electrical probe. The transmission lines provide both controlled electrical connections and remove the probe/bonding pads back from the lasers making the fiber access more convenient. The DC and pulsed measurements were made on the high density arrays. The microwave and digital measurements were made on the high-frequency arrays. We begin with the low frequency measurements.

4.2.1.1 Low Frequency Performance

The LI characteristics of the four laser sizes are shown in Figure 4.2b. The lasers have very linear LI characteristics, showing little non linearity due to current crowding. The 5 and 7 μm diameter lasers have sub-milliamp threshold currents. The measured threshold currents were 0.76, 0.72, 0.99 and 1.8 mA for the 5, 7, 10 and 15 μm diameter devices respectively. The maximum output powers are 1, 2.1, 3.7 and 6 mW while the differential efficiencies are 31, 38, 43 and 46% respectively. The variation in external efficiency indicates that the size dependent losses are significant. This is not surprising given the large number of processing steps during which the waveguide sidewalls were exposed. One would expect that the higher order transverse modes would be suppressed in the smaller devices and this is indeed the case. The IV characteristics of the four device sizes are shown in Figure 4.2c. The lasers had operating voltages between three and four volts for most of the LI curve. Given that the photon energy is 1.24 eV, this indicates that there is significant room for improvement. The active region's resistance properties are far from optimized. The drive voltage for more optimized devices should be nearly half of the measured value. This alone would result in a doubling of the thermally limited output power. Also indicated are the voltages and differential resistance at peak power. The power conversion efficiencies of the 10 nm offset lasers are shown in Figure 4.2d with maximum values of 6.5, 10, 12 and 12.8% respectively. Most importantly, the maximum efficiencies are achieved at very low power levels. For example, at a 3 mA bias the 7 μm laser produces 1 mW of optical power at an input power of only 10 mW. These high efficiencies at low power levels are essential for high density interconnect applications. While the performance is quite good, they could be much better. If the drive voltages were halved the efficiency would double, which would make the devices some of the most efficient VCSELs to date.

The optical spectrum of the lasers at various bias currents was measured using an Anritsu Optical Spectrum Analyzer with a 0.1 nm resolution. The measured spectra for the four device sizes are shown in Figure 4.2e. Each plot has a 60 dB vertical scale and a 12 nm horizontal scale. Due to heating, the spectrum shifts to longer wavelengths with increasing bias. While the short cavity
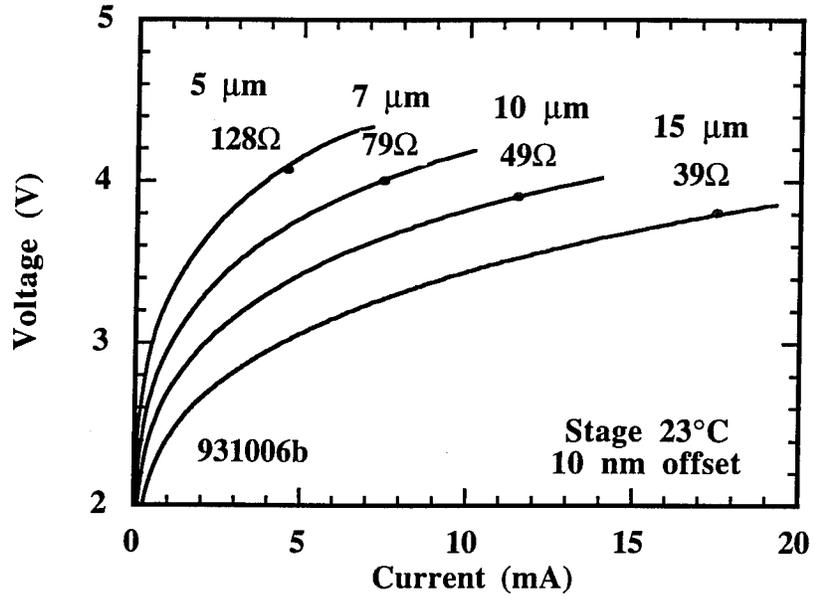
Figure 4.2c
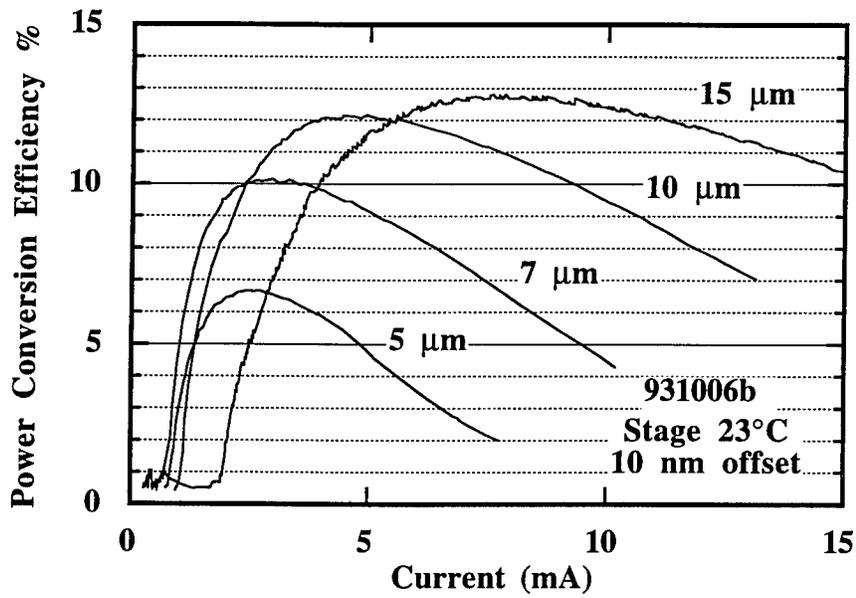
Figure 4.2d
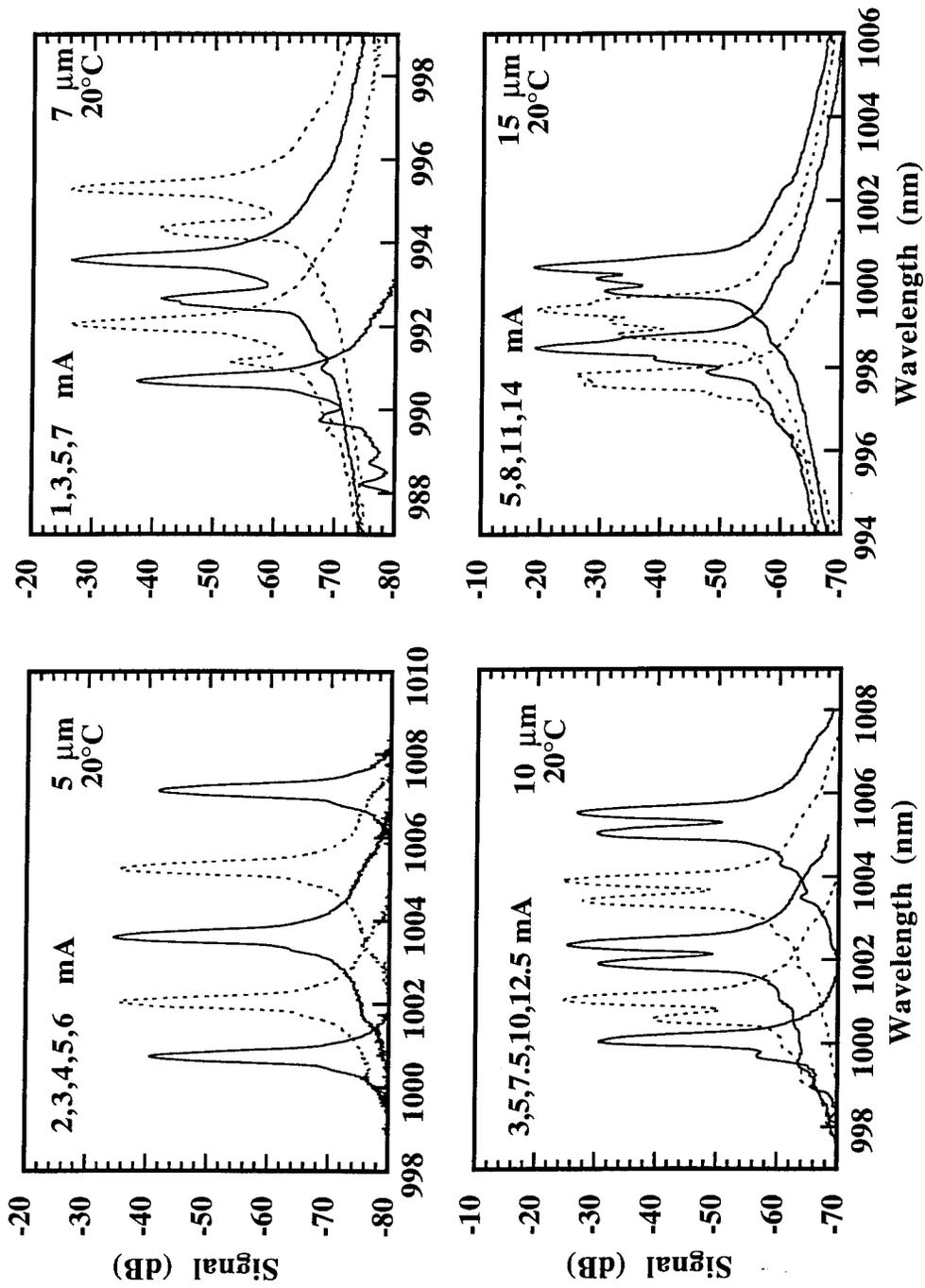
Figure 4.2e

forces a single axial mode pattern, there are many possible transverse modes. The higher order transverse modes occur on the short wavelength side of the fundamental mode. As can be seen in the figure, the lasers' transverse mode properties vary from single mode to multimode. As the cavity diameter gets wider, the mode spacing becomes less, varying from a 2.0 nm spacing for the 5 μm diameter lasers to 0.19 nm for the 15 μm laser. The higher scattering and diffraction losses of the smaller devices provide a mode discrimination so that they lase in a single transverse mode. The Mode Suppression Ratio (MSR) of the 5 μm laser is 41 dB while the 7 μm has an MSR of 15 dB. The 10 μm laser starts with a single transverse mode but, due to spatial hole burning, a second order mode lases at power levels above 1.5 mW. The two competing modes result in a far field pattern which shifts between two lobes and a single lobe. The 15 μm laser begins lasing in a two lobe far field pattern, and evolves into a four lobe "clover" pattern at higher power levels. A current apertured design could be used to allow higher single mode powers if desirable.

The spectrum in Figure 4.2e can be used to estimate the lasers' thermal impedance. To determine the shift in wavelength with temperature, a 7 μm laser was held at a constant bias while the stage temperature was varied. The measured shift, $d\lambda/dT$, is 0.73 Å/°C. The lasing wavelength shift of the four devices as a function of dissipated power is shown on the left in Figure 4.2f. The data points are from the spectra shown in Figure 4.2e while the solid lines are the curve fits. The slopes are 3.32, 1.94, 1.44 and 0.83 Å/mW. Dividing by the measured $d\lambda/dT$ gives thermal impedances of 4.53, 2.65, 1.96 and 1.13°C/mW for the 5, 7, 10 and 15 μm diameter lasers respectively. The mode separation can be used to accurately determine the waveguide diameter. From the wavelength spacing between the fundamental and the next higher transverse mode of 2.0, 0.92, 0.49 and 0.19 nm, the waveguide diameters are calculated to be 4.4, 6.6, 9.2 and 14.8 μm respectively. Using these calculated diameters, the thermal impedances are plotted vs. the inverse radius to compare with the simple formula for thermal impedance of a uniform temperature disk on a semi-infinite substrate. As shown on the right in Figure 4.2f, the agreement is quite good using an effective thermal conductivity of 0.038 mW/°Cμm.
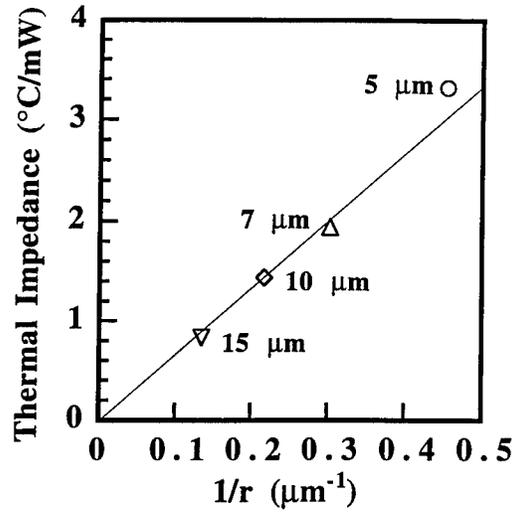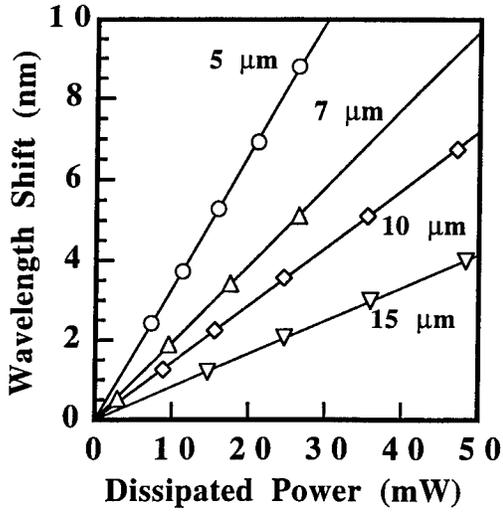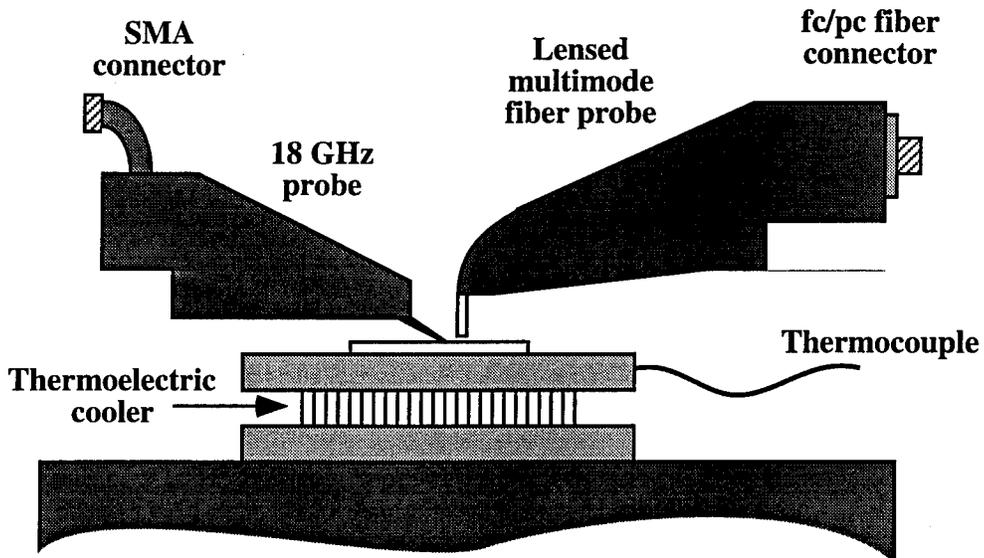
Figure 4.2f

Figure 4.2g

The effective thermal conductivity of the mirror layers can be approximated by the geometric mean of the high and low index materials. As shown in Figure 4.2a, the mirror layers were made from $Al_{0.1}Ga_{0.9}As$ and AlAs so that the only GaAs in the laser were the barriers cladding the quantum wells. This design makes it fairly easy to achieve efficient optical pumping of the structure. Unfortunately, the use of the ternary $Al_{0.1}Ga_{0.9}As$ significantly increases the thermal impedance. The thermal conductivities are calculated to be 0.091 for AlAs and 0.014 for $Al_{0.1}Ga_{0.9}As$ resulting in a geometric mean of 0.036 mW/°Cμm, in good agreement with the measured value. In future designs GaAs would be used for the high index material. Its thermal conductivity of 0.044 mW/°Cμm would give an effective thermal conductivity of 0.063 mW/°Cμm, two times higher than the experimental value. The output powers of the lasers would be expected to double with this change alone!

4.2.1.2 Microwave Response

One attractive feature of intra-cavity contacted VCSELs is that emission is from, and both contacts are on the surface of a semi-insulating GaAs substrate. This makes it possible to make high-speed measurements on wafer using the techniques developed for monolithic microwave integrated circuits. The experimental setup is shown schematically in Figure 4.2g. The sample is held by vacuum onto a temperature controlled stage. An 18 GHz Cascade probe is used for electrical connection. The light is captured by a lensed multimode fiber 50 - 100 μm above the surface. Both probes are mounted on xyz stages for positioning. The entire setup was mounted on an optical isolation table for stability. Two kinds of S parameter measurements were made. The S_{11} measurements provide information on the input impedance. The S_{21} measurements show the modulation response of the laser. Careful calibration is required for both measurements. For the S_{11} measurements, a calibration substrate is used to set the reference plane at the probe tips. The calibration substrate has open, short and laser trimmed 50 Ω loads which match the coplanar transmission line probe tips. For the S_{21} measurements, a through calibration is used, connecting all the microwave cables together in series with the two network ports. In addition, the amplifier and photodetector responses must be measured and subtracted from the data. The detector used was a 25 GHz New Focus detector which uses a top surface illuminated InGaAs detector and has

a multimode fiber input. A cascaded pair of 18 dB, 20 GHz New Focus amplifiers were used to compensate for the low responsivity of the detector (~0.1 A/W) and the power loss in the laser. With the above test system, the laser properties could be measured quite rapidly.

The magnitude of the reflection coefficient varies by less than 0.5 dB from 1 to 15 GHz, with input impedances near 250 Ω for the 7 μm diameter device at 3 mA bias. To characterize the coplanar transmission lines, open, short and ~100 Ω loaded test lines were measured. The data matched the theoretical characteristics of a transmission line with a 55 Ω characteristic impedance. From the shorted line the series resistance is determined to be 1.2 Ω. From the open termination the line is determined to have a phase of 22 degrees at 15 GHz. Using this model for the coplanar transmission lines, an equivalent circuit for the laser can be constructed to match the measured data. Given the particularly good performance of the 7 μm laser, we modeled its input impedance at a representative bias of 3 mA. An admittance Smith chart plot of the S parameters for the laser and the open, shorted and loaded transmission lines is shown in Figure 4.2h as scanned from 0.5 to 15.5 GHz. As can be seen in the figure, the reflection coefficient does not follow a constant resistance curve. To get good agreement, it was necessary to use the device model shown in Figure 4.2i. The series resistance is 150 Ω while the parasitic shunt capacitance is 30 fF. The junction resistance is 110 Ω in parallel with a diode capacitance of 80 fF. Even with the relatively high resistances, the capacitance values are so low that the laser is not RC limited. The two time constants are determined by the effective resistance seen looking out of the capacitors. In a $Z_O = 50$ Ω test system, the time constant associated with the parasitic capacitor is given by $\tau_p = C_p(Z_O/(R_s+R_d)) = 1.3$ ps while the time constant associated with the diode capacitor is given by $\tau_d = C_d(R_d/(R_s+Z_O)) = 5.7$ ps. Thus the RC limited bandwidth is 28 GHz, well above the maximum modulation bandwidth measured.

The S_{21} data for the 7 μm laser is shown in Figure 4.2j. Shown are the experimental data as dashed lines and the theoretical fit as solid lines. The laser had a threshold of 0.85 mA. The normalized modulation response can be written as [7] :
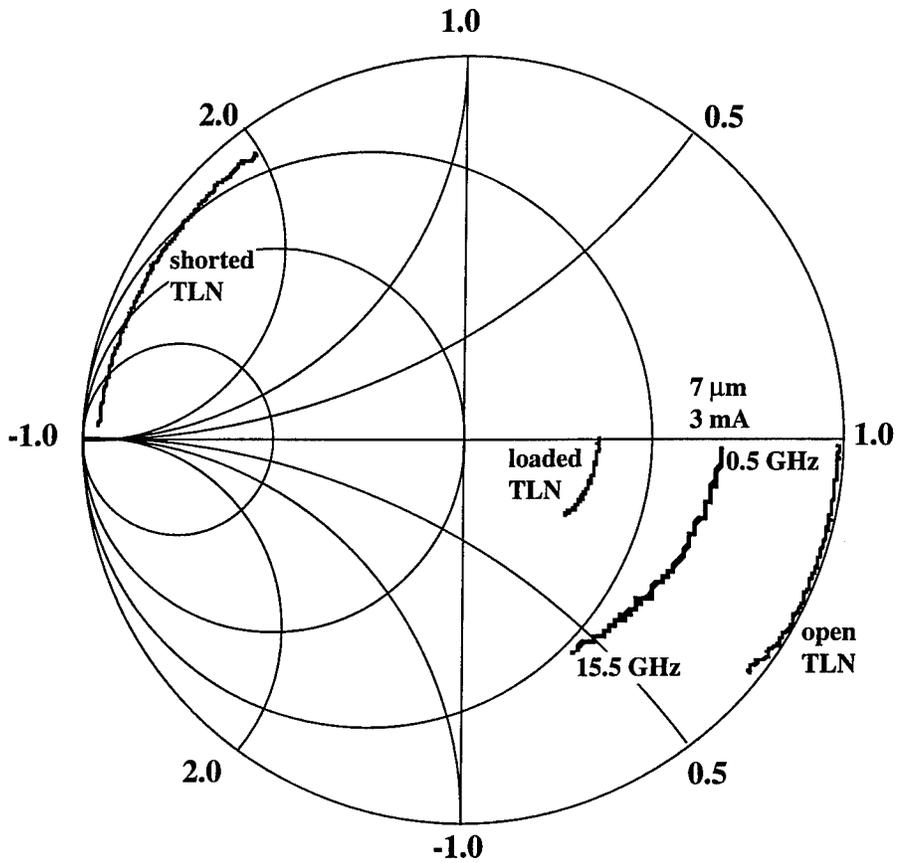
S$_{11}$ plotted on a Smith chart. Shown are the data for the 7 μm laser at a 3 mA bias and the data for open, shorted and load terminated coplanar transmission lines

Figure 4.2h

Small Signal Equivalent Circuit
(7 µm laser, 3 mA bias)

55Ω TLN

R_s

C_p

C_d

R_d

$C_p = 0.03$ pF

$R_s = 150 \ \Omega$

$C_d = 0.08$ pF

$R_d = 110 \ \Omega$

Figure 4.2i

Small Signal Modulation Response

Response (dB) vs Frequency (GHz)

4.0 mA

2.5

1.5

1.0

931006b, 20°C
7 µm diameter
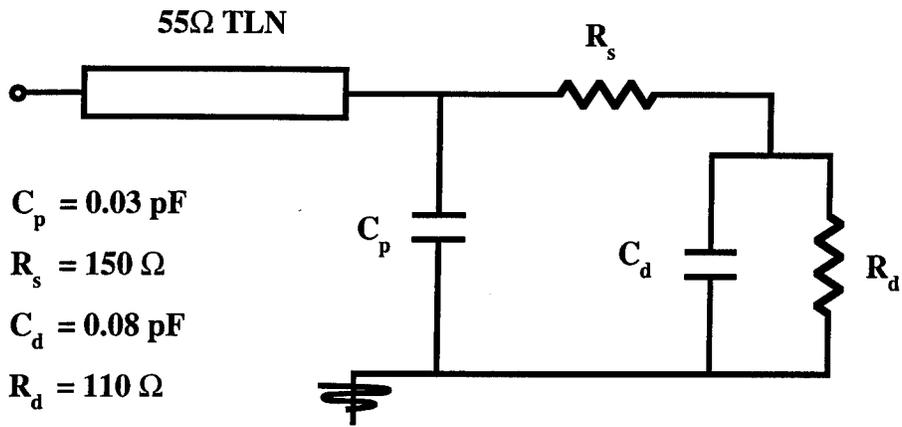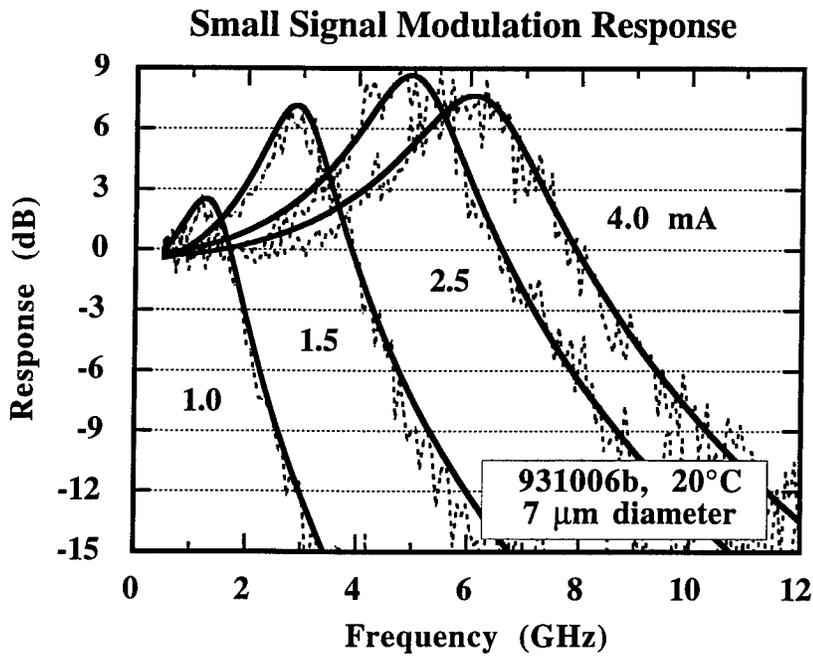
Figure 4.2j

$$\frac{L}{I}(f) = C_0 + \frac{1}{1 + \left(jf / f_p\right)} \frac{1}{1 + \left(jf / f_r\right)^2 + \left(jf / f_d\right)} \tag{1}$$

where L and I are the small signal light output and modulation current respectively, f is the modulation frequency, f_r is the relaxation oscillation frequency, f_d is the damping frequency, f_p is a single order parasitic rolloff frequency and C_0 is an offset to account for normalization error. The damping frequency is defined here as $f_d = 2\pi(f_r)^2 / \gamma$, where γ is the damping rate. A maximum 3 dB electrical bandwidth of 8.5 GHz is observed at an injection current of only 4 mA. At higher drive currents the modulation response showed little change, indicating that as the junction temperature rose the effective threshold current was increasing and the differential gain was decreasing. Note that the relaxation oscillation peak showed little dampening, indicating that higher speeds should be possible by improving the thermal and electrical designs. The parameters used in the curve fits are shown in Table 1. The fit of Equation (1) at 4 mA has a relaxation peak at 6.3 GHz and a damping frequency of 19 GHz indicating an intrinsic bandwidth in excess of 27 GHz. For a good fit it was necessary to include a parasitic roll off at 9 GHz. The parasitic rolloff may be due to transport effects [7] associated with the 500Å doping setbacks in the AlGaAs cladding the active region. The modulation response of the 7 μm laser at 4.5 mA of drive current has been taken at stage temperatures varying from 15°C to 60°C. The 3 dB bandwidth varied from 9.3 to 6.0 GHz respectively with little change in the threshold current.

Table 1. Parameters used in the curve fits shown in Figure 4.2j.

	f_r (GHz)	f_d (GHz)	f_p (GHz)	C_o (dB)
1.0 mA	1.46	2.01	9.00	-0.78
1.5 mA	3.00	7.59	9.00	-0.65
2.5 mA	5.10	16.0	9.00	-0.23
4.0 mA	6.30	18.9	9.00	-0.38

In the absence of damping and parasitics, the 3 dB bandwidth of a semiconductor laser under small-signal direct-current modulation is proportional to the square root of injected current above

threshold. To characterize low-threshold high-speed lasers Chen et. al. [8] have suggested the modulation-current efficiency factor (MCEF) as the figure of merit, defined as:

$$MCEF = f_{3dB} / \sqrt{(I - I_{th})} \qquad (2)$$

where $f_{3\,dB}$ is the 3 dB bandwidth of the laser under direct current modulation, I is the bias current at which the modulation bandwidth is measured and I_{th} is the threshold current of the laser. For applications such as high bandwidth computer interconnects, the laser should provide the highest bandwidth at the lowest current, and thus the optimal laser will have a low threshold current and a high MCEF. In the absence of damping and parasitics, the 3 dB bandwidth of a semiconductor laser under direct current modulation can be written as [8] :

$$f_{3dB} \cong 1.55\, f_r = \frac{1.55}{2\pi} \sqrt{\frac{v_g G' P}{\tau_p}} \qquad (3)$$

$$= \frac{1.55}{2\pi} \sqrt{\frac{v_g G' \eta_i}{q V_{opt}} (I - I_{th})} \qquad (4)$$

where f_r is the resonance frequency, v_g is the group velocity, G' is the differential gain, τ_p is the photon lifetime described in chapter 2, η_i is the internal efficiency, q is the electronic charge and V_{opt} is the modal volume. The modulation current efficiency factor, Equation (2), can thus be expressed in terms of the internal parameters:

$$MCEF = \frac{1.55}{2\pi} \sqrt{\xi_{enh} \frac{v_g G' \eta_i}{q V_{opt}}} \qquad (5)$$

where we have introduced the enhancement factor, ξ_{enh}, into the equation. In the case of a VCSEL the electric field at the quantum wells is nearly doubled due to their location at the peak of the strong standing wave in the cavity, resulting in an enhancement of the stimulated emission rate. In Equation (5) this periodic gain enhancement factor must be included, a value of 1.83 for

our device structure. Historically, comparisons of laser modulation efficiency have been based on output power. However, modern high-speed in-plane lasers use facet coatings to optimize performance while VCSEL mirror reflectivities vary with the number of mirror periods. With varying output coupling, the relationship between output power and internal field strength vary from device to device. Figures of merit based on output power can be misleading by showing higher values for lower external efficiency lasers. More meaningful comparisons can be made from benchmarks based on injected current rather than output power.

The 3 dB bandwidth as a function of the square root of the current above threshold for the various laser diameters are plotted in Figure 4.2k. The slope yields the modulation current efficiency factor. Equation (5) would suggest that the modulation efficiency would be inversely proportional to the device diameter. The trend towards higher modulation efficiency was observed down to the 7 μm device which displayed the highest MCEF of 5.7 GHz/√mA, higher than any in-plane semiconductor laser. For comparison, Chen et. al. recently reported [8] record levels of 5 GHz/√mA, with previous values of 2-3 GHz /√mA in high-speed bulk lasers and 2-4 GHz/√mA in high-speed quantum well lasers. The surface emitting lasers reported here have not been optimized for high-speed other than to minimize the device parasitics. In fact, they were optimized for high quantum efficiency. Lasers with higher mirror reflectivities would operate at a lower threshold gain, resulting in a higher differential gain.

The modal volume of a VCSEL is quite small, although the cavity length of these lasers have an additional micrometer compared to many vertical cavity structures, to allow for the intra-cavity contacts. From the calculated standing wave pattern in Figure 4.2b, the effective length is determined to be 2.2 μm. The transverse mode is mostly contained in a mode diameter of 6 μm. By multiplying the modal area by the effective length, the modal volume V_{opt} is calculated to be 6.22×10^{-11} cm^3. An estimate of the internal efficiency which includes both the injection efficiency and spatial hole burning effects can be made by dividing the measured external efficiency of the 15 μm laser, 46%, by the calculated optical efficiency of 66% yielding an internal efficiency η_i of 0.7. The plane wave threshold gain of the cavity has been calculated to
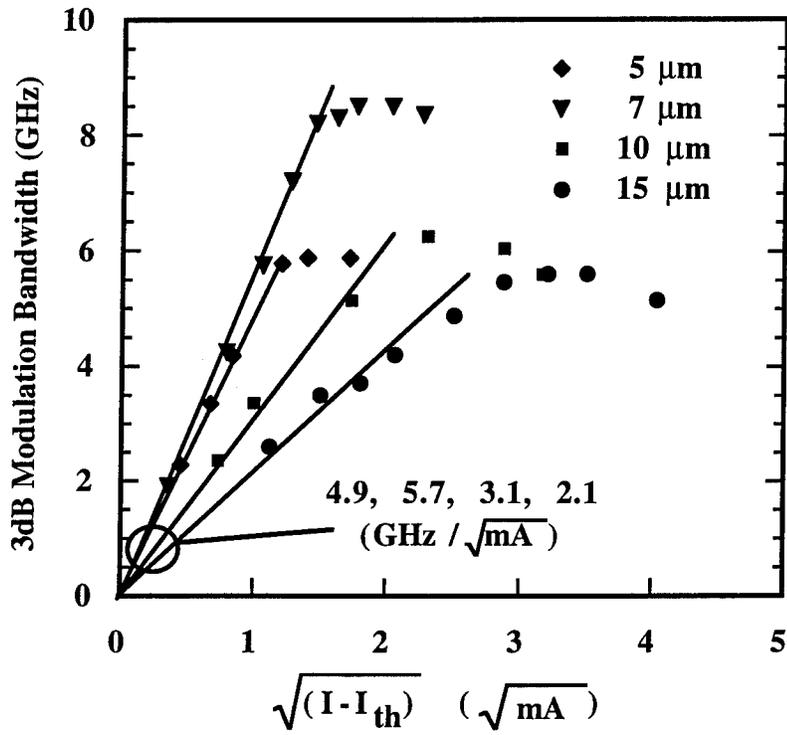
Figure 4.2k
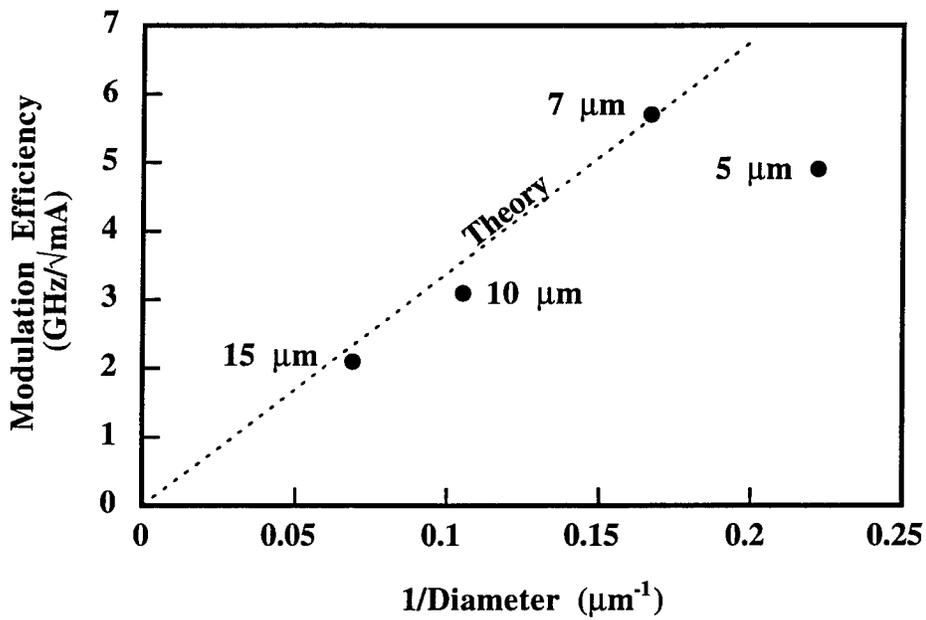
Figure 4.2l

be 1500 cm^{-1}. The theoretical differential gain G' is 5.4×10^{-16} cm^2 at that point on the quantum well gain curve. Using the above values along with a group index of 4 in Equation (5) yields a predicted MCEF for the 7 μm laser of 5.6 GHz/√mA, in good agreement with the measured value of 5.7 GHz/√mA. Dividing out the diameter, the MCEF can be expressed as:

$$MCEF = \frac{33.6 \, GHz/\sqrt{mA}}{D(\mu m)}$$

(6)

where D is the device diameter. This theoretical line is plotted in Figure 4.21, showing good agreement except for the 5 μm laser. The quantum wells in that device are driven very hard due to the higher optical losses of the very small waveguide and the relatively high mirror transmission. The result is that the wells are biased to saturation levels so that the differential gain is much lower, reducing the MCEF for this device. Cavity designs optimized for high-speed would use a higher reflectivity output coupler to keep the differential gain higher at the expense of reduced external efficiency. In such a design modulation current efficiency factors in excess of 7 GHz/√mA appear quite possible to achieve. Returning to Figure 4.2k, it is clear that all the lasers are capable of GHz modulation at low bias currents. In the next section, their high modulation efficiency will enable high-speed digital data transmission at low current levels.

4.2.1.3 Digital Data Transmission

This section presents results of an investigation of the system performance of the linear arrays of intra-cavity contacted, top-emitting VCSELs. The system performance experiments were chosen from the perspective of demonstrating compatibility with digital logic circuits under varying environmental conditions. To this end, measurements of the laser's temperature insensitivity and device-to-device performance variations were made under identical drive conditions.

A block diagram schematic of the set-up employed to perform the optical data transmission experiment is shown in Figure 4.2m. Light from the laser is coupled into the multimode fiber (50μm core diameter/125 μm cladding diameter) via a Cascade optical probe mounted on an xyz stage. As the Cascade microwave probe (which supplies the laser bias and modulation signals) is

HP 3 Gbit/s
BER
Test Set

DC bias
to laser

lensed
multimode
fiber probe

30 meters of
graded index
multi-mode fiber

high-frequency
probe

variable
attenuator

3GHz low
pass filter

variable
attenuator

3x 20dB
gain stages

25GHz ν_{focus}
Photodiode
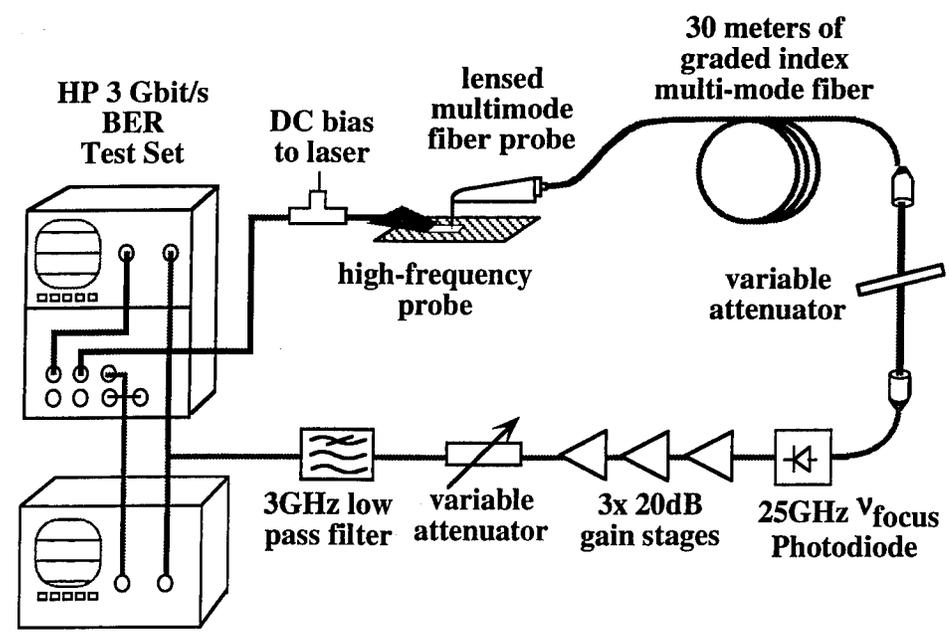
Sampling Scope

Figure 4.2m

Bit Error Rate

- 15 μm
- 10 μm
- 7 μm
- 5 μm
- - - - Theory

10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}

2.488 Gbit/s
2^7-1, NRZ

-20 -19 -18 -17 -16 -15 -14 -13

Received Signal Power (dBm)

Figure 4.2n

also mounted on an xyz stage, the data transmission performance of different devices on the wafer could be quickly and conveniently evaluated. The wafer itself is mounted on a tem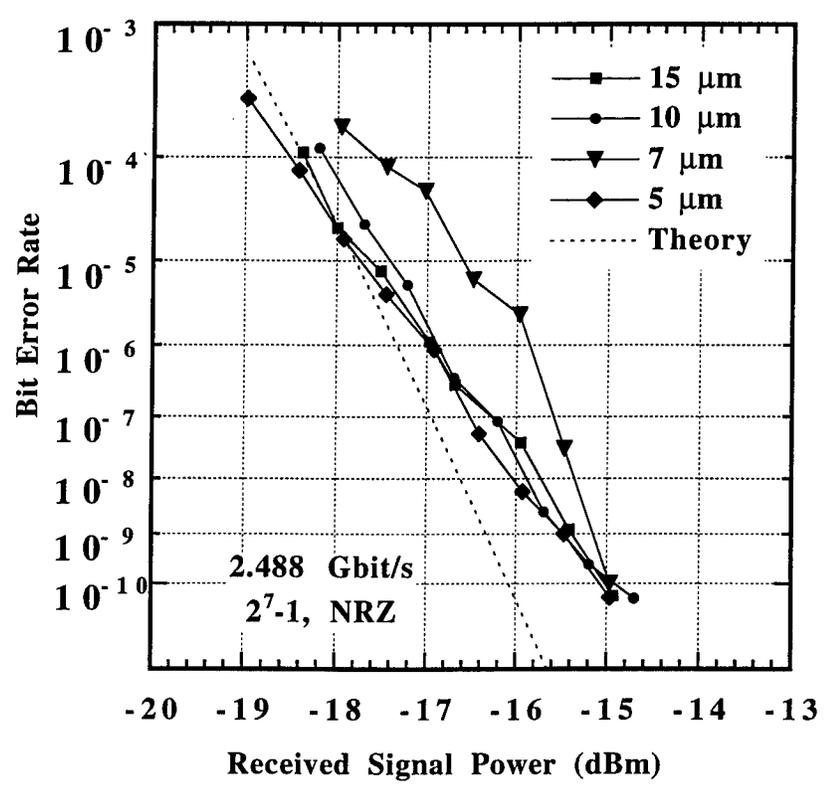perature-controllable vacuum chuck as shown in Figure 4.2g. This flexible measurement setup exhibited excellent stability in spite of the use of wafer probes for the electrical and optical coupling, indicating the potential for automated testing in a manufacturing environment. Bit error rate (BER) measurements were performed at 2.488 Gbit/s for all device sizes. The corresponding BER curves are shown in Figure 4.2n. Thermal noise in the front end limits the receiver sensitivity to -18 dBm at a BER of 10^{-9}. For the 2.488 Gbit/s measurements, the lasers were biased so that the zero logic level was slightly above threshold, introducing an extinction ratio penalty of 1.4 dB. For comparison, the theoretical curve taking into account thermal noise, amplifier noise and finite extinction ratio is shown as well. All devices could be operated at 3 Gbit/s, the limiting bit rate of the test equipment used, with no additional penalty. Optical coupling efficiency into the lensed multimode fiber, held 50 to 100 µm above the surface, was greater than 80%. There were several fc/pc connectors in the link while the coupling efficiency of the free space optical attenuator was ~ 50%. It is interesting that all the lasers, from the single mode 5 µm device to the multimode 15 µm device, showed no error floor. An eye diagram of the 5 µm laser at a received optical power of -14 dBm (50†µW) is shown in Figure 4.2o. High light levels are on the lower part of the plot. The zero is one division from the top. From the above experiments, it is clear that the lasers are capable of multi Gigabit data rates at very low current levels.

In order to evaluate the performance of the VCSELs for board to board interconnects, BER curves were measured at stage temperatures of 20°C, 40°C and 60°C under full on/off modulation. On/off modulation is an attractive feature for the simplified implementation of data links. The bias and drive conditions were identical in each case. A bit rate of 1.6 Gbit/s was chosen as representative of the bit rates employed in these applications. As can be seen from the BER curves shown in Figure 4.2p, no appreciable degradation in BER performance can be observed, indicating the robustness of VCSELs in environments with large temperature gradients/ variations. For these and the following experiments, the lasers were biased at an

Eye Diagram of 5 μm Laser at 2.488 Gbit/s
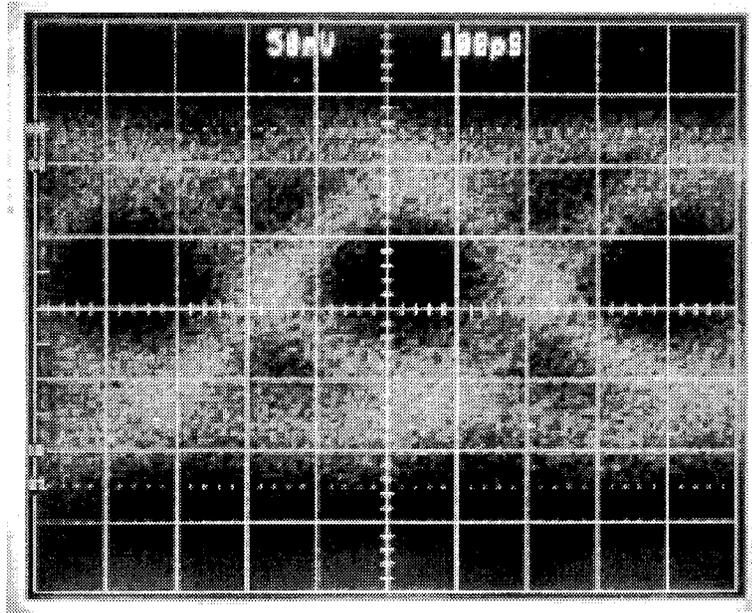
(received signal power -14 dBm)

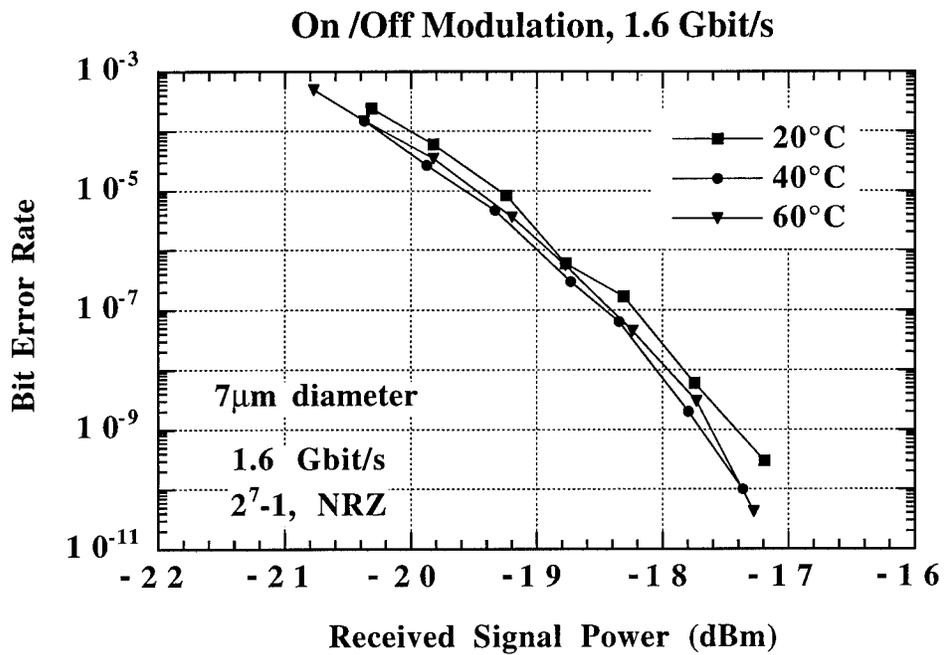## Figure 4.2o

On /Off Modulation, 1.6 Gbit/s
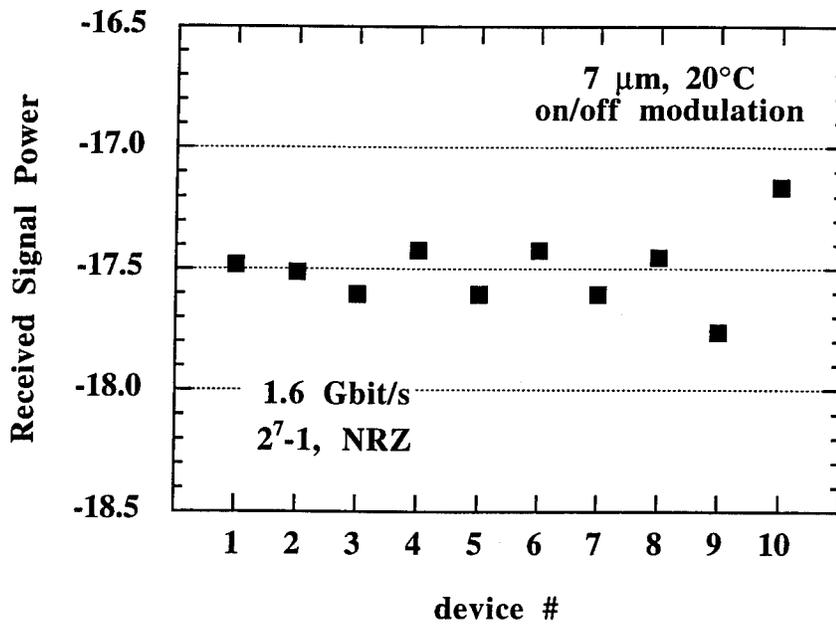

Figure 4.2p

Variation from Device to Device

Figure 4.2q

average current of 3 mA with a modulation signal amplitude of 1 V peak to peak into 50 Ω. This was sufficient to ensure that the lasers were driven well below threshold in the zero state . No additional penalty due to turn on delay was observed with this on/off modulation condition due to the low threshold current. Finally, a block of 10 devices in an array of 7 μm devices were each used as transmitters in the optical data link to evaluate the uniformity of the device performance under the same identical operating conditions. The received optical power required to obtain a BER of 10^{-9} was first recorded for device #1 in the array. The optical and microwave probes were displaced laterally to the next device in the array and, under identical operating conditions, the received optical power required to achieve a BER of 10^{-9} was recorded. This procedure was repeated for all 10 devices. Figure 4.2q plots the received optical power for a BER of 10^{-9} for each device. The total spread in received optical power is less than 0.6 dB, clearly illustrating the uniformity of the devices' performance. Combined with a well controlled gain-offset growth for temperature-stabilized output power, these BER characteristics indicate that it should be possible to develop VCSEL based parallel data links using simplified electronics and without temperature control. Such a data link holds promise of providing very low cost, high bandwidth networks.

In summary, measurements of intra-cavity contacted, top-surface emitting VCSELs have shown output powers greater than 1 mW, 3 dB bandwidths in excess of 8 GHz and gigabit data rates at bias currents of only a few milliamps and power consumption below 10 mW. The advantages of semi-insulating substrates enabled all the laser characterization to be made with wafer level probing. Measurements of the thermal and electrical properties indicate that significantly higher speeds and efficiencies will be achieved as the laser designs are improved.

4.2.2 Bottom Emitting Vertical Cavity Surface Emitting Lasers

Bottom emitting VCSELs have proven to be successful devices in laboratory conditions. They have produced 113 mW CW output power, lased CW at 140°C, and operated at 5 GHz. What remains to be done in terms of device development, before the devices can be successful in commercial ventures, is to show that the devices can operate reliably and to demonstrate capabilities for high-speed data transfer. Since the basic structures have already been proven,

manufacturability and yield issues have been addressed in the first half of Phase II. The predominant weakness in bottom emitting VCSELs is the top metallization, which has not been ohmic.

In a bottom emitting VCSEL, the top metallization serves the dual purpose of a top mirror and an electrical contact. The thickness of the top DBR mirror can be decreased by relying on the reflectivity of the evaporated metal layer, and this improves the conductivity of the mirror stack. Typically there is a large voltage drop across the top DBR mirror of a VCSEL, so it is advantageous to reduce the thickness and the resistance of the mirror. To provide the best possible mirror, a cold contact is required, but this causes an extra voltage drop since the contact is not ohmic. Alloyed contacts tend to reduce the reflectivity of the top metal, resulting in poorer performance for the VCSELs.

In an effort to solve this problem, alloyed ring contacts with non-alloyed central reflecting metallization have been tested. Since the optical mode is concentrated towards the center while the largest area is near the periphery, alloyed ring contacts were expected to perform well. This proved to be a good solution. Figure 4.2r shows the output power characteristics of three VCSELs fabricated together from the same location on a wafer. The ripple in the data is a result of interference from the back of the substrate, which will be eliminated with an anti-reflection coating on the backside. The laser with the cold contacts has the highest differential efficiency, but does not produce the most output power. This is due to the extra heat caused by the non-alloyed contacts. The device with the fully alloyed contacts has better electrical characteristics, and therefore operates at higher bias currents. Its differential efficiency is much worse than the device with no alloyed contacts. The device with ring contacts provides the best alternative. The differential efficiency is almost identical to the device with cold contacts, but the increased conductivity of the contact results in an increase of the total output power.

For bottom emitting VCSELs with the highest efficiencies [9], the high efficiencies were produced for devices with diameters of 20-30 μm. The efficiency of smaller devices declines very rapidly, more than a factor of two when the radius of the device is reduced from 20 μm to ·

Comparison of top contact metallization

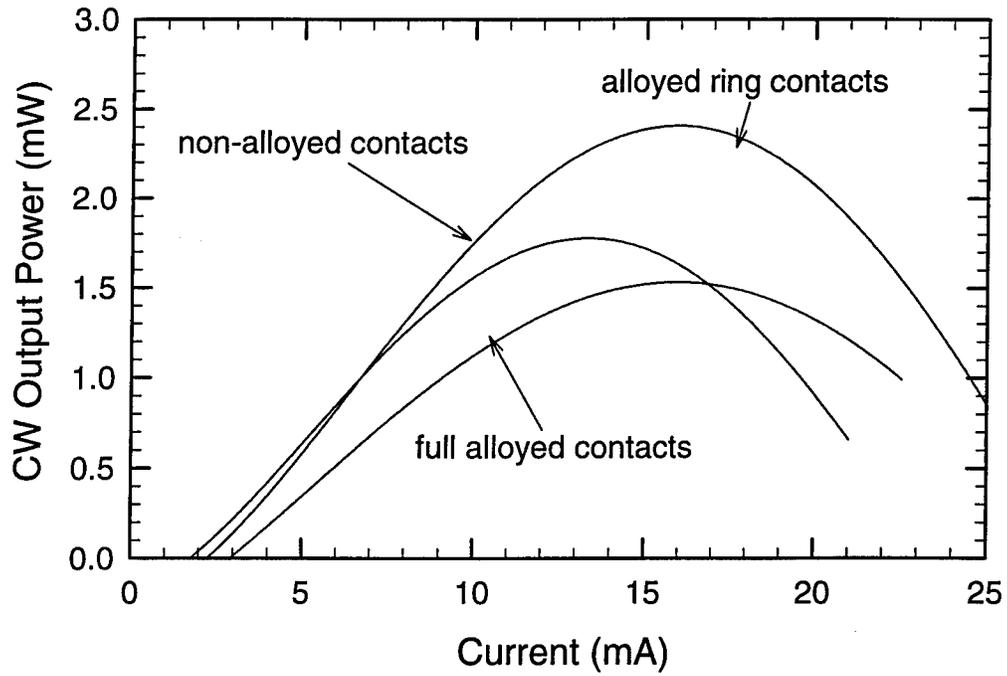**CW Output Power (mW)** vs **Current (mA)**

- non-alloyed contacts
- alloyed ring contacts
- full alloyed contacts

Figure 4.2r

VCSELs with alloyed ring contacts

CW Output Power (mW) vs **Current (mA)**

- 7 µm diameter
- 3 µm diameter

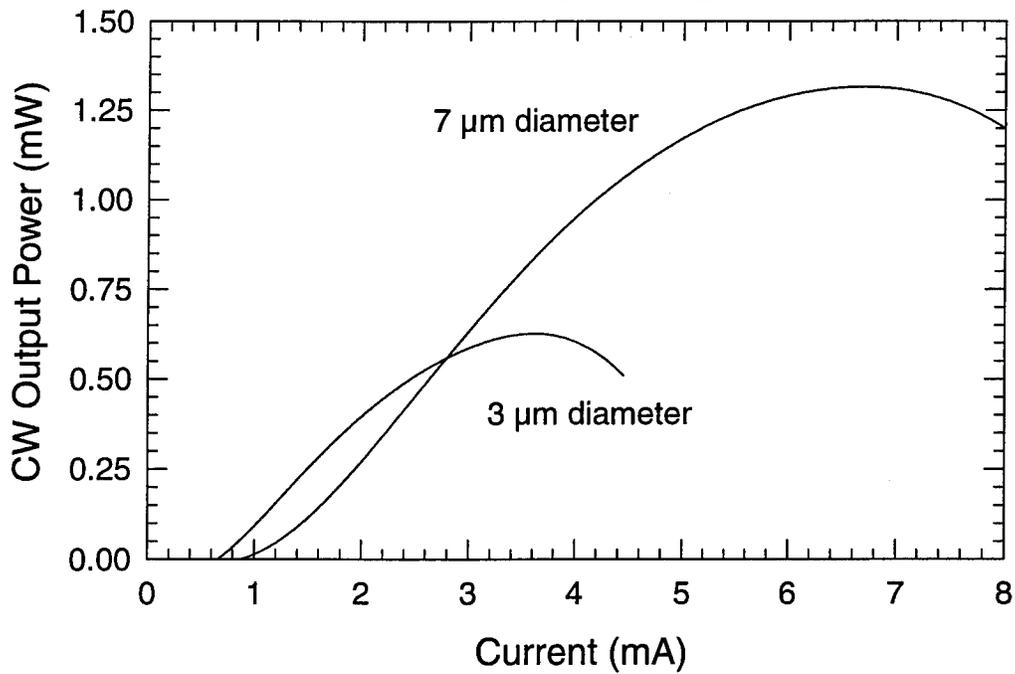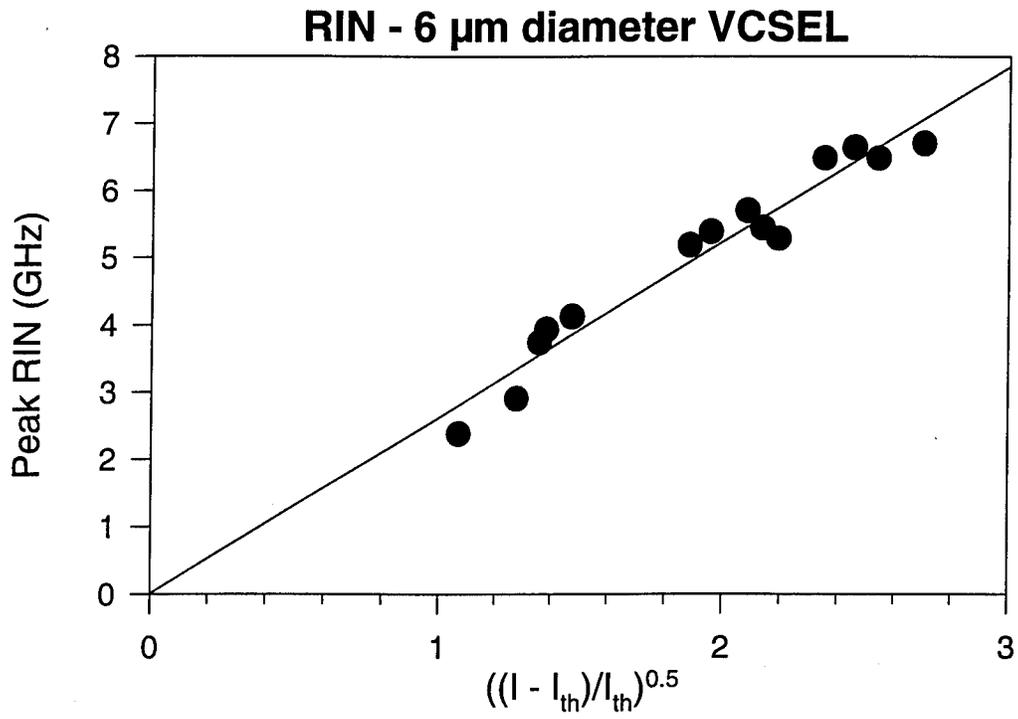**Figure 4.2s**

10 μm. Also, the yield of the devices suffers when the size of the devices decreases. At the beginning of the Phase II effort, it was typical of a 70 μm diameter VCSEL to have a near 100% yield, a 20 μm VCSEL to have a 90% yield, about 75% for a 10 μm VCSEL and 10% or lower for a 4 μm VCSEL. This was primarily due to the poor quality of the metallization. Therefore, once the ring contact process proved to be useful, it was coupled with the ohmic contact research and new VCSELs were fabricated. The test wafer used for this process was not world class, but even so, the results are noteworthy.

Devices fabricated with ohmic ring contacts have demonstrated near 100% yields for all sizes of devices, even devices with 4 μm diameters. This is a significant result already. What is more encouraging is the efficiencies of the devices. Our initial results showed only a 25% decrease in the efficiency of 20 μm diameter devices to 4 μm diameter devices. Since the test wafer was not exceptional, the large devices are not particularly good while the 4 μm devices are the best devices of that size ever produced. Figure 4.2s shows light verses current curves for 4, 8 and 20 μm diameter VCSELs with alloyed ring contacts. These results are significant in that there is virtually no change in the differential efficiency as a function of diameter. The 4 μm diameter device produces over 600 mW with a threshold current of about 600 mA. The threshold current of the device is as good as the best ultra-low threshold VCSELs that produce much smaller peak output powers. The 8 μm device produces over 1 mW of output power with a threshold current of under 1 mA. These devices will be used to test the flip chip bonding technology being developed by Optical Concepts.

The relative intensity noise (RIN) was measured for standard top contacted GaAs devices. This was done for both devices that had been heat sunk and for those that had not. The non heat sunk device that was measured was a 6 μm diameter VCSEL that operated single frequency, while the heat sunk device was a multi lateral mode 12 μm VCSEL. This device was chosen because it was the smallest reliable heat sunk device produced. The metallization previously used on smaller devices could not stand up to the stresses inherent in the soldering process.

For typical GaAs VCSELs with top contacts, 6 μm is the largest diameter which ensures single

RIN - 6 μm diameter VCSEL

$$((I - I_{th})/I_{th})^{0.5}$$

Figure 4.2t

12 μm diameter VCSEL

— 25°C

········· 0°C

Current (mA)

Figure 4.2u

Relative Intensity Noise - 25°C
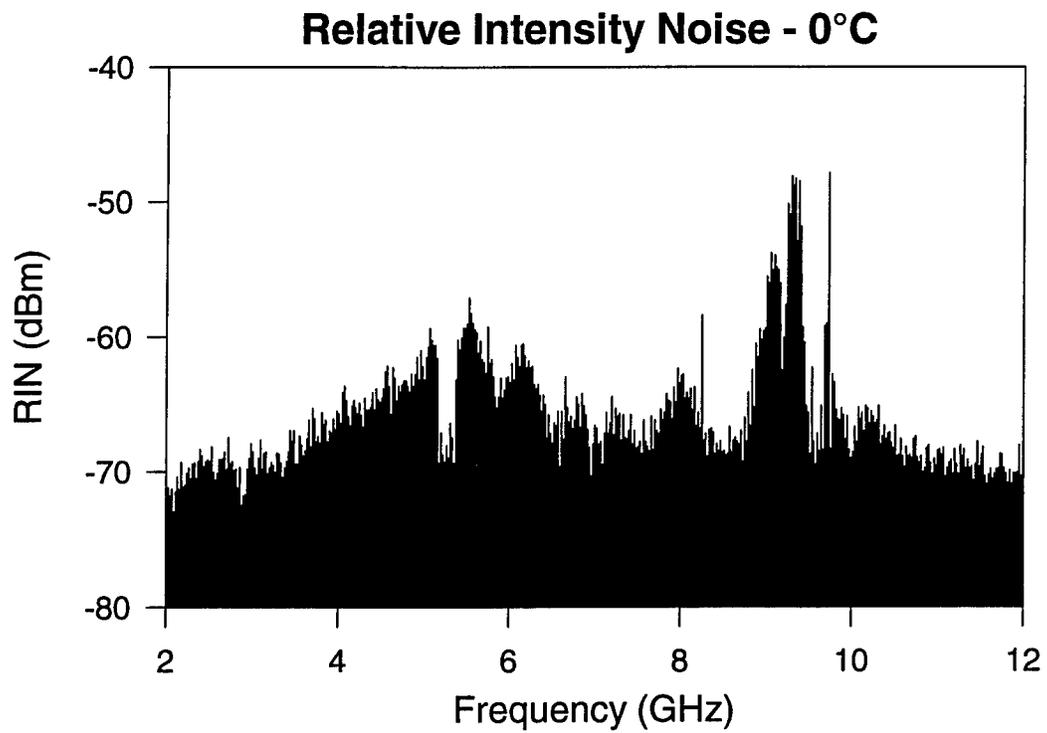

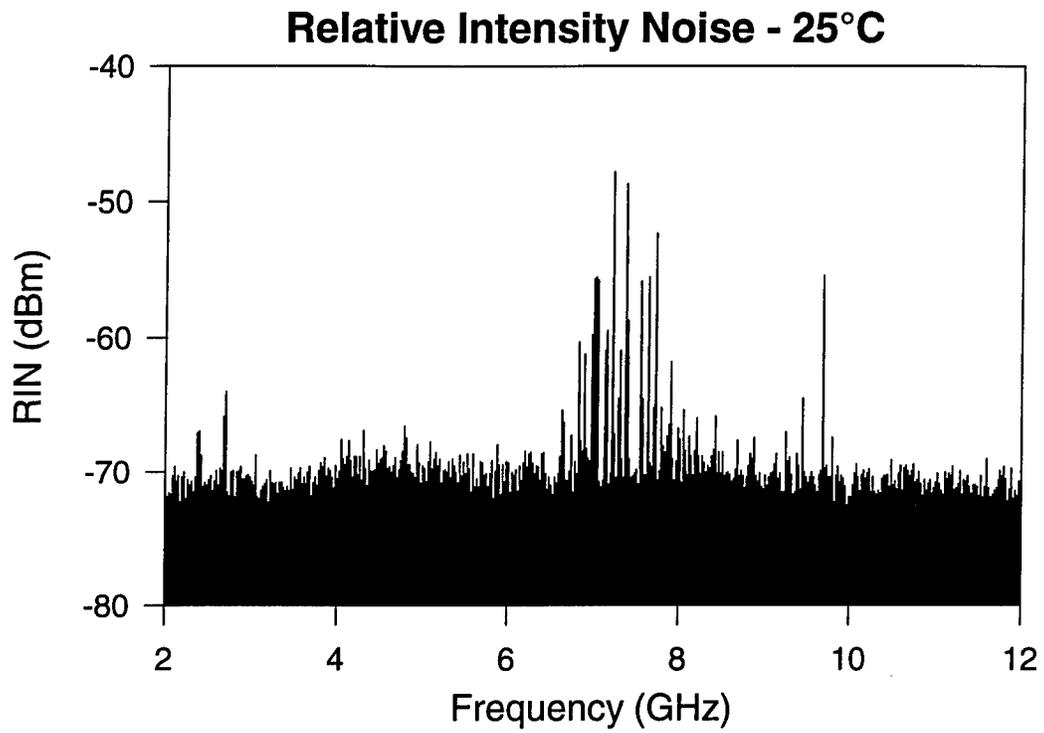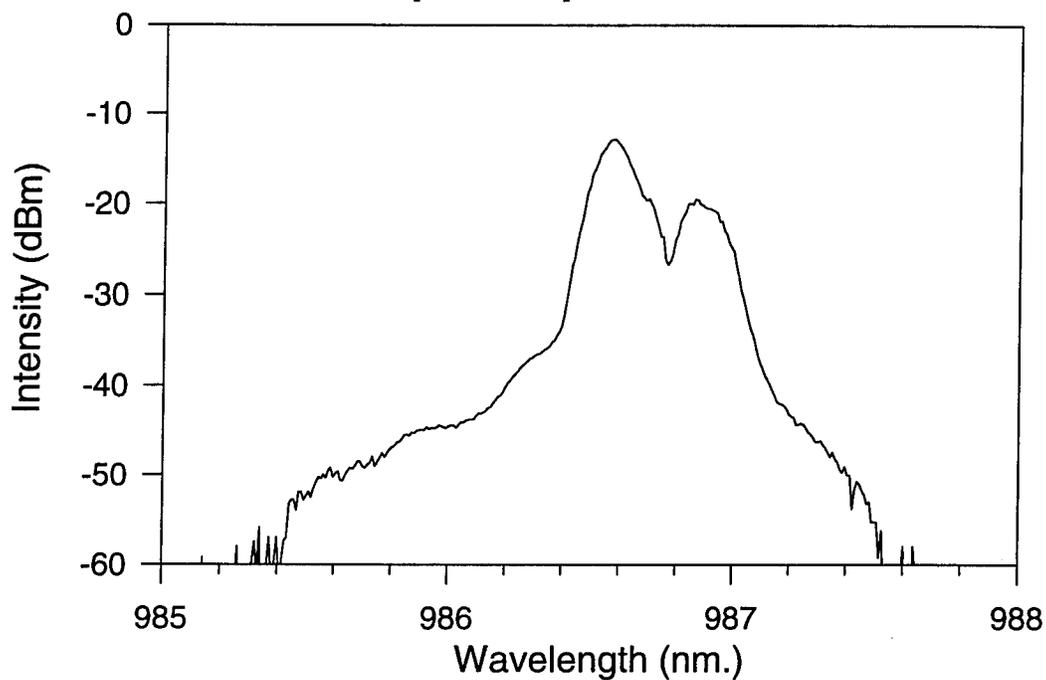## Relative Intensity Noise - 0°C
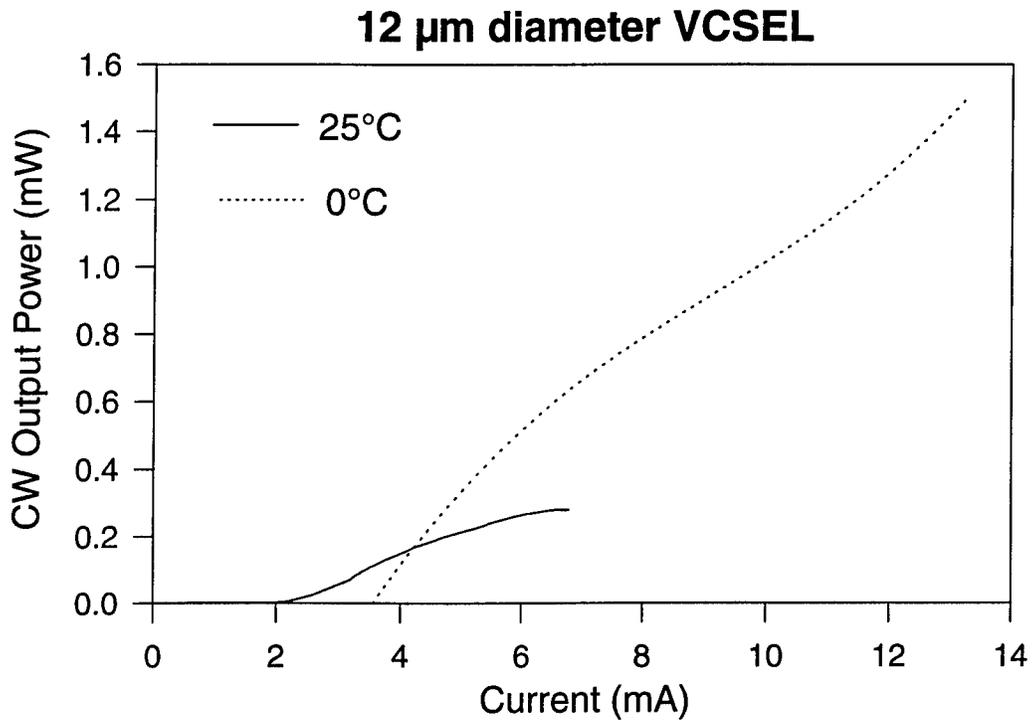
Figure 4.2v

Optical Spectra - 25°C

A

Optical Spectra - 0°C

B
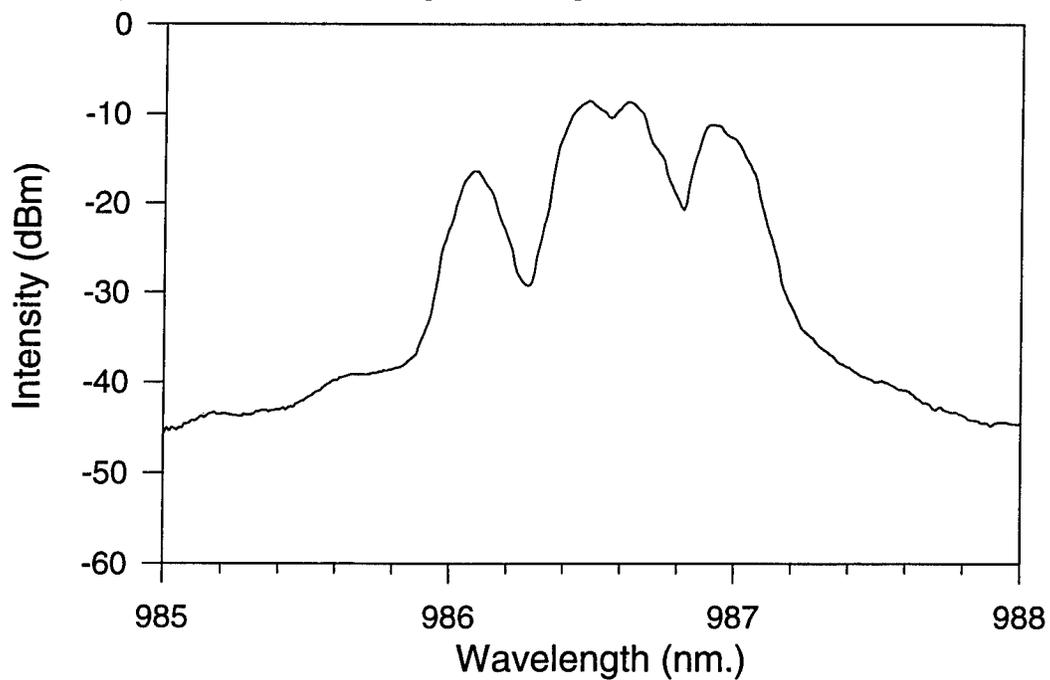
Figure 4.2w

frequency operation over the entire bias range. Figure 4.2t shows the RIN as a function of bias for a 6 µm device with GaAs/AlGaAs mirrors. The slope of the curve is not nearly as high as have been measured for devices with GaAs/AlAs mirrors.

The relative intensity noise peaks for larger devices are typically smaller than those of the 6 µm device shown. However, once the device was heat sunk it was capable of operating at higher bias points which produced RIN peaks at higher frequencies. The device was cooled from 25°C to 0°C and the output power and RIN peaks were monitored. Figure 4.2u shows the light vs. current curves of the 12 µm device at the two temperatures. As one can see, even though the threshold current increased at lower temperatures, the device was able to operate at higher bias, and produced much more output power. Initially the device was biased at about 6 mA at 25°C and the RIN was measured as shown in Figure 4.2v. Then as the temperature was lowered, the bias was increased to the laser so that the junction temperature would be constant. This was done by monitoring the emission wavelength of the device. Figure 4.2w shows the laser spectra at the two temperatures. At 0°C the RIN peaks increased from below 7 GHz to about 9 GHz. When measured, this was the highest CW RIN peaks measured for a VCSEL, and this was done using a relatively poor device. This result demonstrates the significance of effective heat sinking. The temperature difference between a package and the active region of the device should be minimized, otherwise the performance of the devices will suffer.

4.3 Fabrication Technology Development

4.3.1 Microlens Technology

OCI staff have developed a technique for forming microlenses directly on GaAs substrates, potentially eliminating the need for planar microlens arrays. The technique incorporates conventional photolithography for the formation of poly (dimethylgutarimide) (PMGI) circular patterns on the substrate side of back emitting VCSEL arrays. When the PMGI is heated to 250°C, it reflows forming a perfect lens. Initial investigation of this technique applied to

VCSELs indicate that this procedure may provide an inexpensive, very efficient microlensing procedure which substantially simplifies the packaging arrays.

Vertical cavity surface emitting lasers arrays with their small beam divergence angle and separation of the laser from the surface are a breakthrough from a packaging perspective. The small divergence angle simplifies optical coupling since a lens with a low numerical aperture can be used. In comparison, in-plane lasers require a much higher numerical aperture for efficient coupling. A backside emission VCSEL offers another great advantage in optical coupling because the laser is removed from the backside of the substrate. This makes it a good candidate for fabricating microlenses directly onto the substrate. Such a lens would eliminate the need for external microlens arrays and the associated alignment during packaging.

Optical Concepts has fabricated such microlenses onto GaAs substrates and has also put such lenses onto the backsides of VCSEL arrays, in collaboration with both UC Santa Barbara and Sandia National Labs (Figure 4.3a). The initial microlenses are made from cured PMGI which has an index of refraction similar to quartz at 630 nm. These microlenses can easily be fabricated and have the appropriate light transmission properties to work well as a microlens [10,11].

The microlens process was done initially on a GaAs substrate. First, multiple layers of PMGI are spun onto the GaAs substrate. The PGMI is then developed into cylinders using deep UV, and the GaAs is etched to form a step used to contain the PMGI during reflow. Once reflow has taken place the PMGI lenses are complete.

To improve the focal length of the microlenses and to accommodate microlenses which can be used in hermetic packages, the PMGI microlenses have been used as templates for the formation of microlenses in GaAs. Once the PMGI microlenses were formed, the PMGI was nonselectively etched away leaving microlenses in the GaAs. Since the index of GaAs is ~3.5, this means that the radius of curvature can be much larger than what is required for PMGI microlenses for the same focal length. Microlenses fabricated into GaAs have been made and are nearly identical in appearance to the PMGI microlenses. GaAs microlenses are shown in
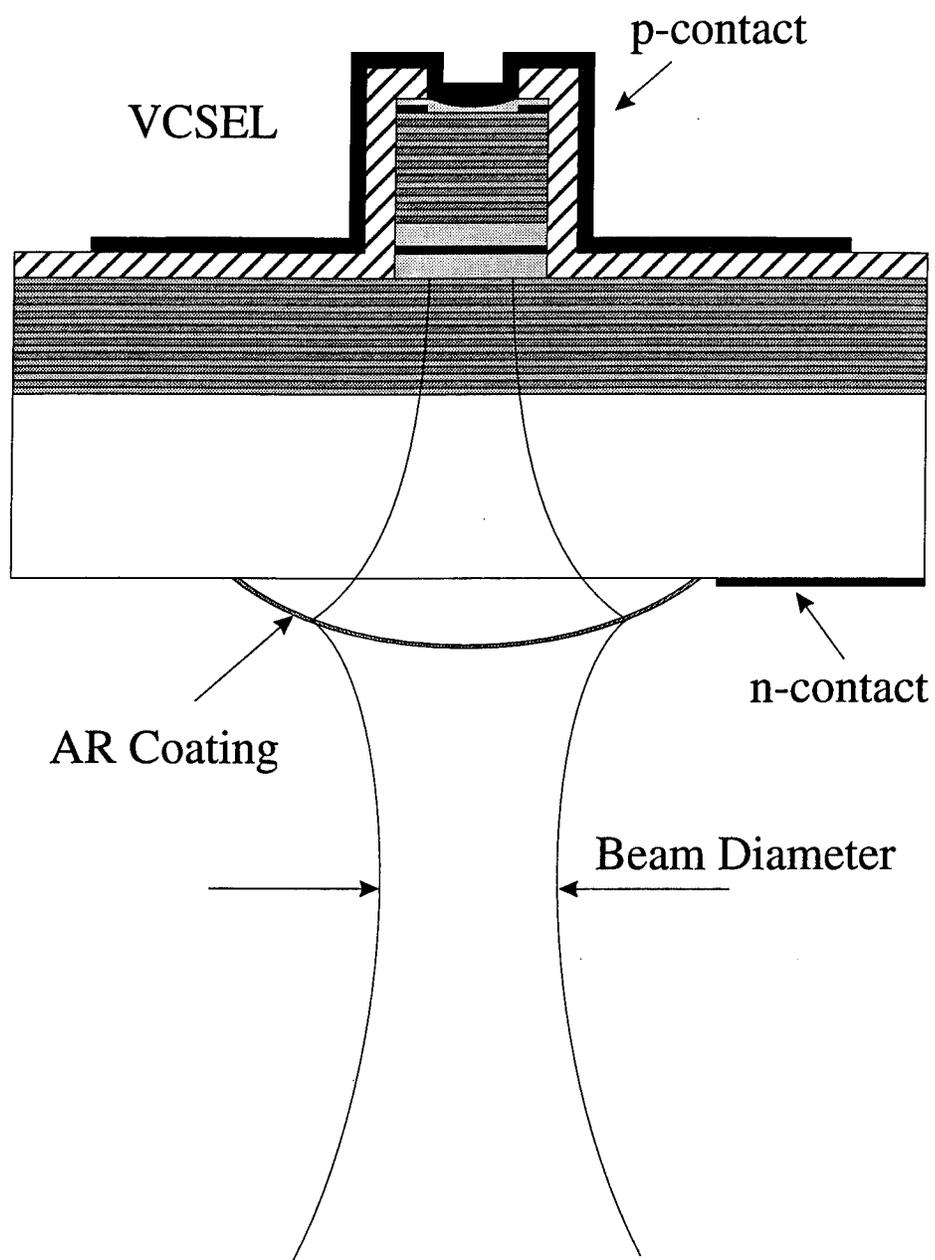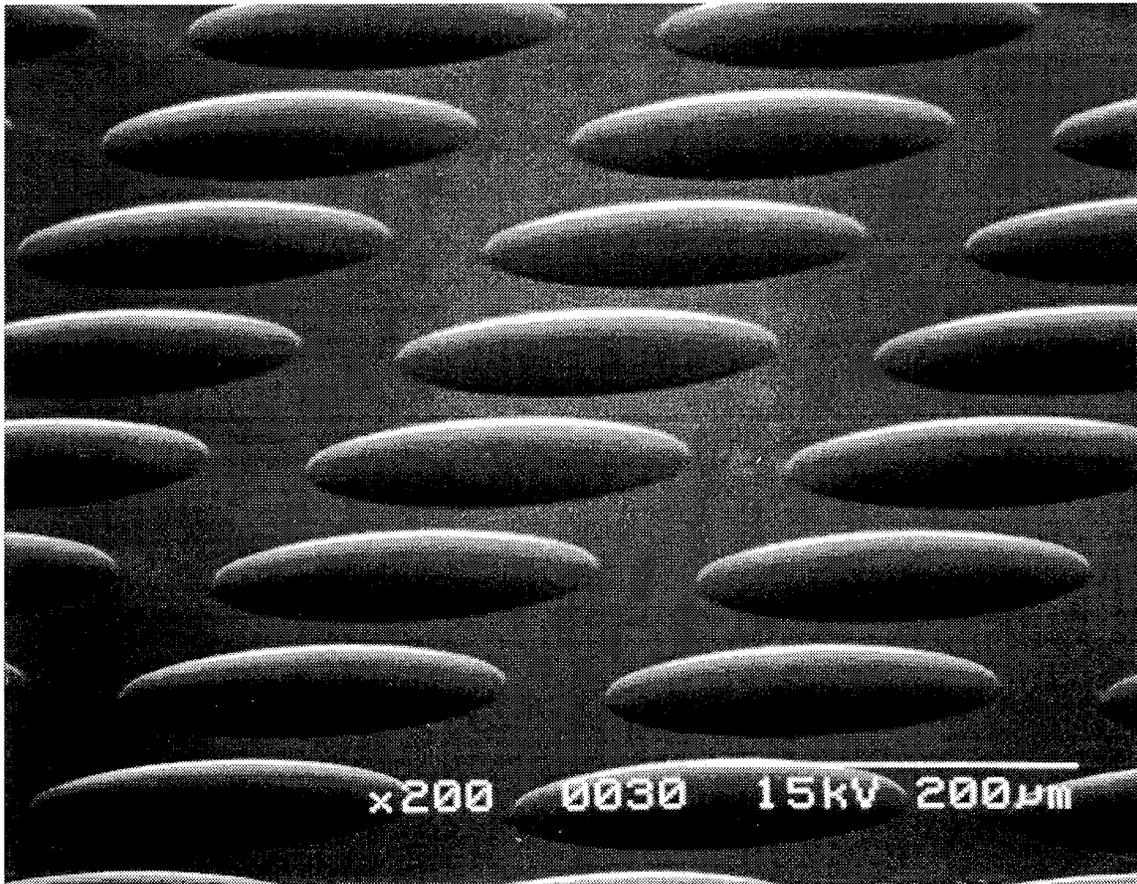
Figure 4.3a

GaAs Microlenses

Figure 4.3b

Figure 4.3b. These lenses greatly reduce the already low divergence of the emission from the VCSEL. Figure 4.3c shows the beam diameter of a VCSEL as a function of distance from the exit aperture.

For accurate lens formation in GaAs, it is necessary to quantify the different etch rates of the PMGI and the GaAs. This material-dependent etch rate has been measured and can be seen graphically in Figure 4.3d. We would like to be able to make microlenses for various applications which may require small or large focal lengths (or radii of curvature). The lower limit of radius of curvature (ROC) of a curved etched GaAs surface was found to be around 4 μm. Some applications such as free space interconnect systems require microlenses with rather long ROC. Because the etch rate of GaAs is about 2 to 3 times higher than PMGI, the ROC of the PMGI mound has to be even longer. It is useful to know the upper limits of ROC in PMGI lenses. Figure 4.3e shows some of the initial results of creating large ROC lenses in GaAs.

For potential manufacturing of microlenses it is useful to know the limitations of the technology. It has been found that the reflow time of the PMGI mounds greatly affects the subsequent shape of the PMGI lens. Therefore, it is concluded that the reflow time should be kept short, close to the minimum time to obtain a paraboloidal shape to prevent loss of material. Possibly reflowing at lower temperatures would give a less severe material loss. It is also necessary to use a constrained reflow to control the shape of the lens, since at least the diameter is fixed.

Based on our investigations, we feel that the technology used for the formation of microlenses provides sufficient control for incorporation into the manufacturing phase.

4.3.2 Ohmic Contacts

VCSELs require both n and p-type ohmic contacts. Conventional contacts to p-type III-V compound semiconductors incorporate AuZnAu contacts whereas n-type contacts incorporate Ni/AuGe eutectic/Ni/Au contacts. Although these materials form satisfactory ohmic contacts, the alloy temperatures, ~38°C for p-type and ~420°C for n-type, are incompatible with each other. When both types of contacts are required for a device, a compromise in alloy temperature

Effect of Microlens on Beam Width
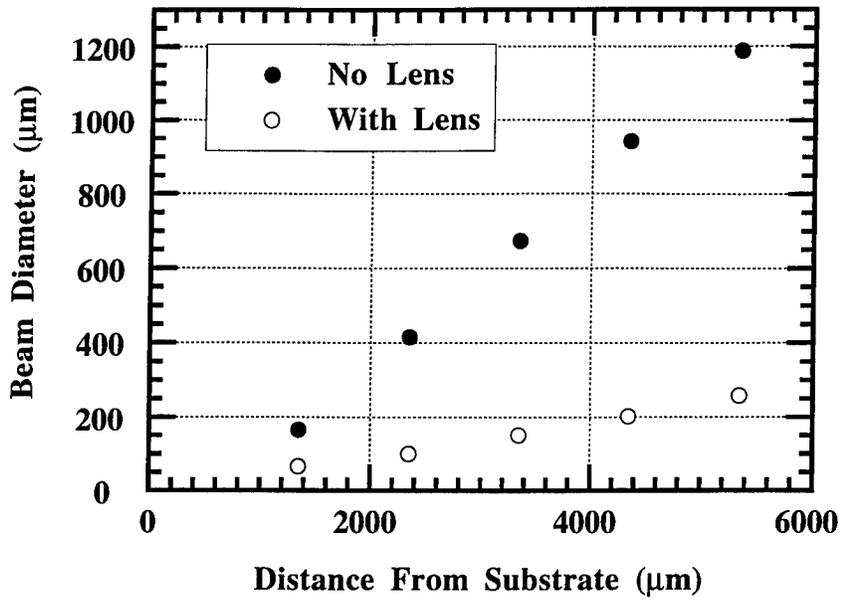
Figure 4.3c

Radius of Curvature vs initial PMGI thickness
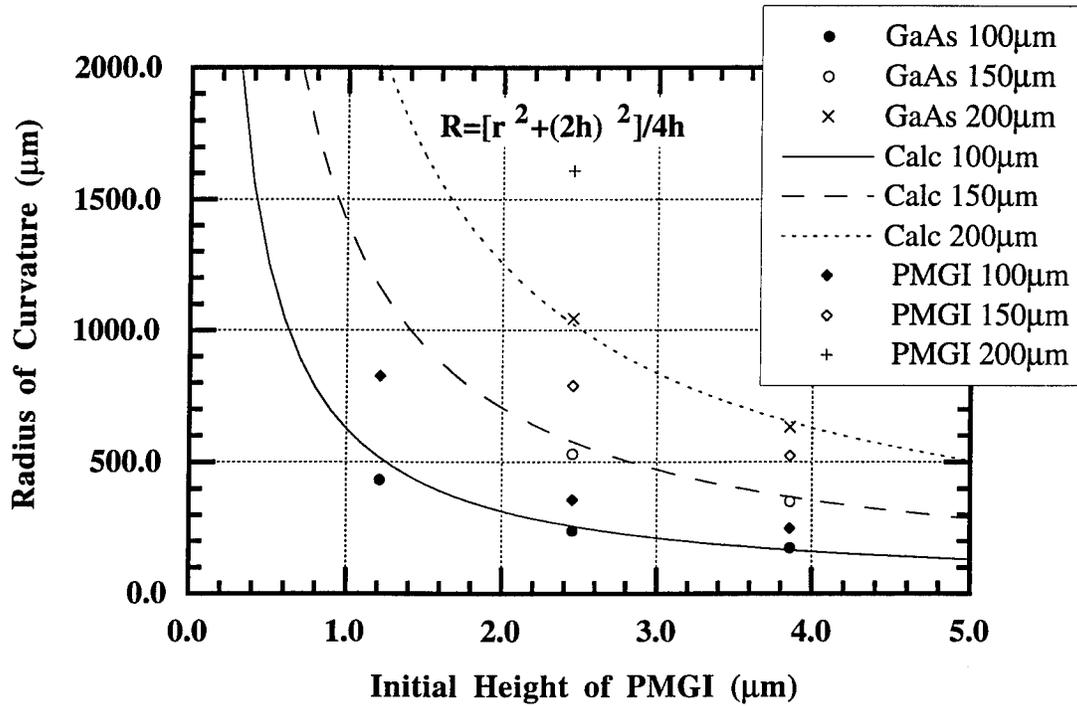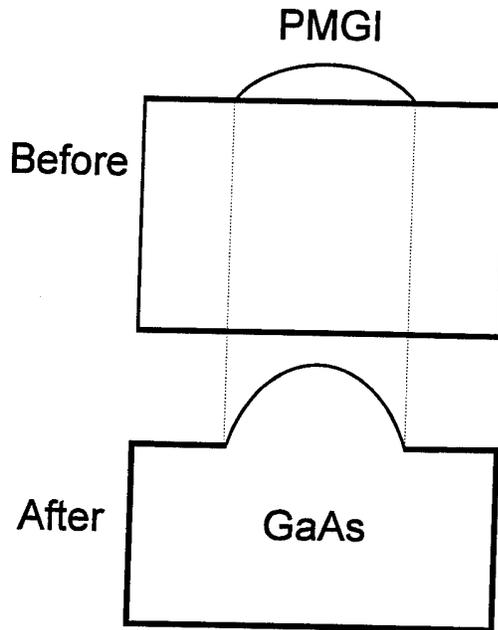
$$R=[r^2+(2h)^2]/4h$$

Figure 4.3e

PMGI

Before

GaAs

After

Vertical Etch Rates in Cl_2 RIE

Etch Rate (Å/min) vs Pressure (mT)

Legend:
- ● GaAs @ 350 V
- ■ PMGI @ 350 V
- ▲ GaAs @ 100 V
- ▼ PMGI @ 100 V
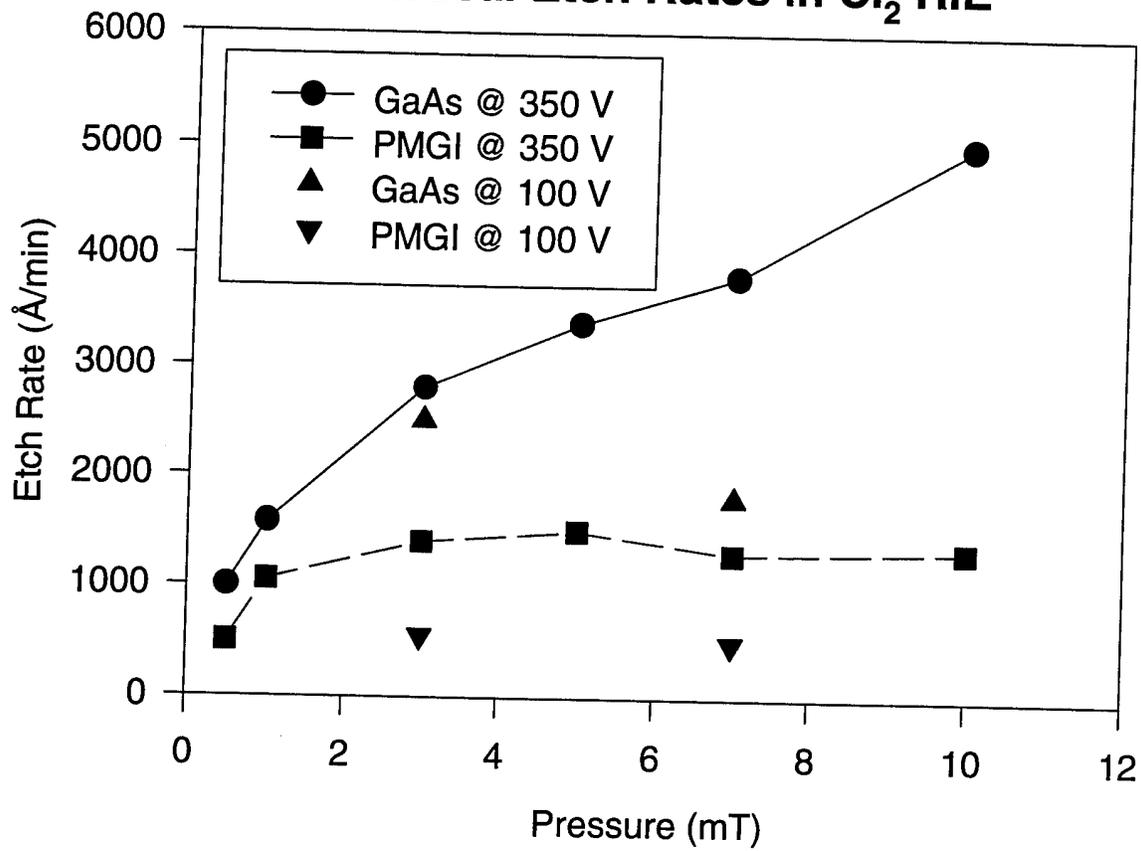
Figure 4.3d

results in less than optimum results. The alloy temperature required to form ohmic contacts to both p and n-type material results in over alloying of the p-type contact and under alloying of the n-type contact.

In an attempt to find a more compatible ohmic metal system, a comprehensive study was performed. The intent was to find ohmic metal systems, pre-metalization semiconductor surface preparation and alloying procedures which would result in satisfactory contact resistance, R_c, for both p and n-type materials when alloyed simultaneously. Preparation of the semiconductor surface prior to ohmic metalization and subsequent alloying is known to play a significant role in the quality of the resultant ohmic contact. Figure 4.3f shows the effect of various pre-metal preparation procedures. The three samples shown were from the same substrate and were processed identically with the exception of the pre-metalization treatment. As the results indicate, the buffered oxide etch/hydrochloric acid (BOE/HCl) treatment provides the lowest R_c values. This procedure has been implemented as a standard processing procedure for both n and p-type GaAs. Figure 4.3g shows the results of a Ni/Ge/Au/Ni/Au, (50 Å / 170 Å / 300 Å / 200 Å / 2000 Å) metal system for n-type material. Note that an R_c of 0.093 ohm-mm was obtained at an RTA anneal temperature of 400°C. Figure 4.3h shows the results of a Au/Zn/Au, (50 Å/120 Å/1000 Å) metal system for p-type material. Note that an R_c value of 0.15 ohm-mm was obtained at an RTA anneal at 400°C. These systems were formed on p and n-type material identical to that of the VCSEL structure. Thus, the metallization process has been simplified by permitting simultaneous alloying of both types of material, and has been utilized in the fabrication of VCSELs.

For a sense of scale, consider a 2 μm alloyed ring contact to an 8 μm diameter bottom emission device. The resulting contact resistance is estimated to be 5 ohms for the best p-type contact. The small area of the devices makes it imperative to have low contact resistance.

OHMIC CONTACT RESISTANCE
vs. SURFACE PREPARATION
Ni/AuGe/Ni/Au
RTA - 420 C / 20 sec.

BOE+HCl   Rc = 0.11 ohm-mm
HCl   Rc = 0.14 ohm-mm
NH4OH   Rc = 0.26 ohm-mm

n+ GaAs

y = 1.1138 + 1.2505x R= 0.99949
y = 1.4364 + 1.2473x R= 0.99914
y = 2.6225 + 1.1777x R= 0.99974
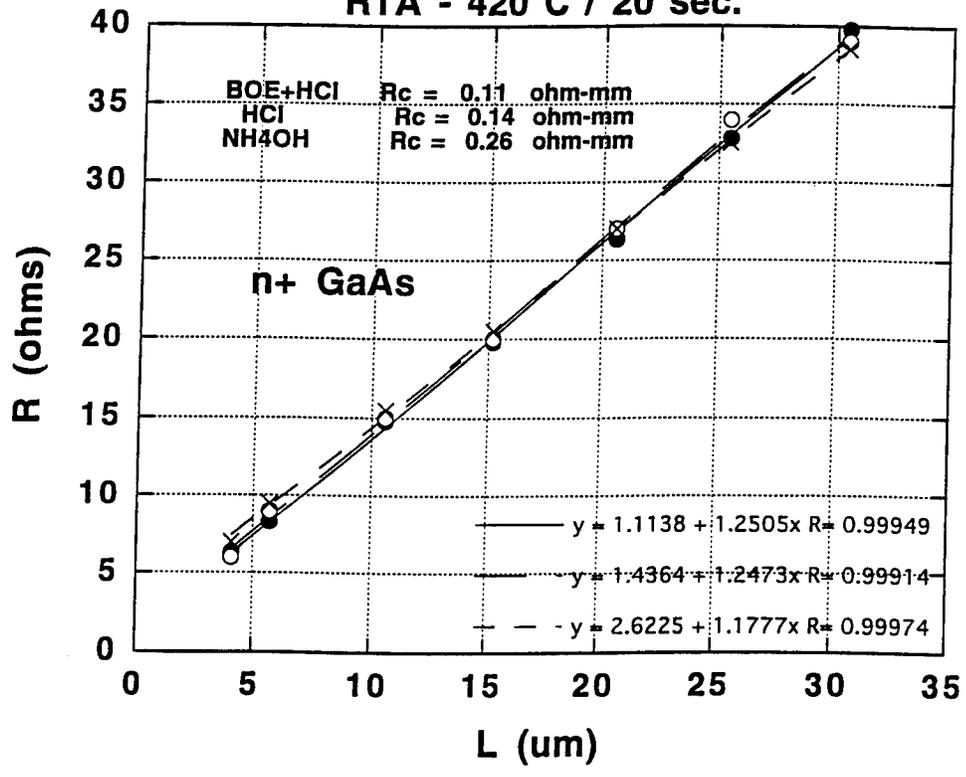
Figure 4.3f

OHMIC CONTACT RESISTANCE
vs.
RTA ALLOY TEMP. @ 20 sec.

Rc (390) = 0.184 ohm-mm
Rc (400) = 0.093 ohm-mm
Rc (410) = 0.242 ohm-mm
Rc (420) = 0.234 ohm-mm
Rc (430) = 0.177 ohm-mm

Ni/Ge/Au/Ni/Au
n+ GaAs

y = 2.3416 + 1.0602x
y = 2.4234 + 1.0593x
y = 1.8433 + 1.0942x
y = 1.77 + 1.0984x
y = 0.92862 + 1.15x

R (ohms) vs. L (µm)
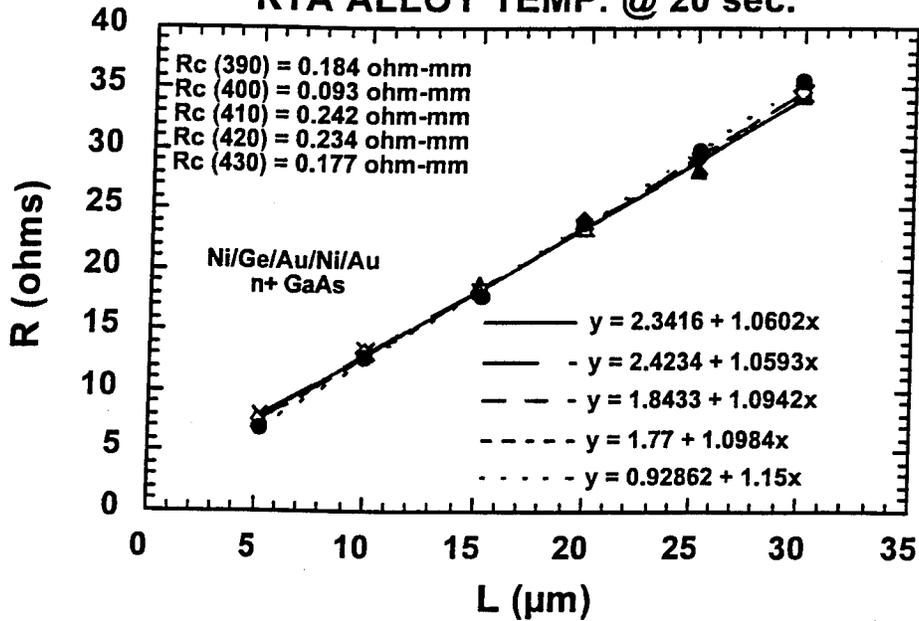
Figure 4.3g

OHMIC CONTACT RESISTANCE
vs.
RTA ANNEAL TEMP. @ 20 sec.

400 C, Rc = 0.15 ohm-mm
410 C, Rc = 0.26 ohm-mm
420 C, Rc = 0.23 ohm-mm
430 C, Rc = 0.24 ohm-mm

AuZnAu, 50A/120A/1000A
p+ on S.I. GaAs

y = 1.5194 + 1.3599
y = 2.5939 + 1.3226x
y = 2.339 + 1.3577x
y = 2.4207 + 1.3505

R (ohms) vs. L (µm)

Figure 4.3h

4.3.3 Double Resist Process

The process for fabricating VCSEL arrays incorporates conventional contact photolithographic equipment. Initial photolithography and subsequent metal lift-off is performed on a planar surface of the substrate. As the process progresses, mesas are formed by chlorine reactive ion etching (RIE) creating a stepped structure where conventional photolithography is precluded. To circumvent this problem a novel double resist procedure was developed. This procedure incorporates two dissimilar positive photoresists, Kodak 820 and AZ series, to planarize irregular structures while creating an undercut profile for clean metal lift-off. Two procedures have been developed for metal lift-off; one for planar substrates, and one for planarization and lift-off from irregular substrates. Both procedures incorporate 820/AZ resists. For planar surfaces 820 with a viscosity of 27 cp and AZ4110 is used. For irregular surfaces with up to 3 μm steps, 820-100 cp and AZ4210 is used. The configuration for planar surfaces permits clean lift-off of evaporated metals and dielectrics with thicknesses to 1 μm. The other configuration permits p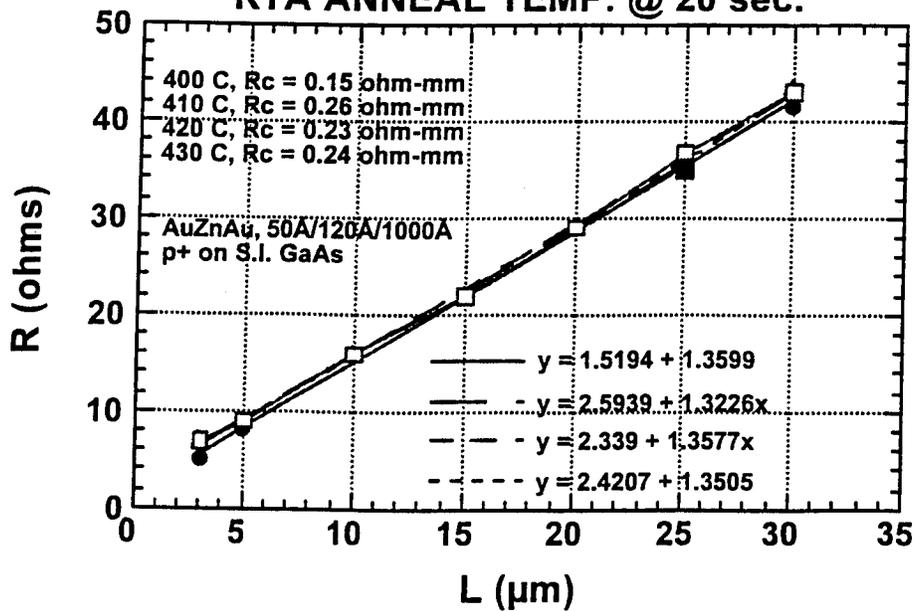lanarization of irregular substrates, ea., mesas, and clean lift-off of evaporated metals and dielectrics with thicknesses to 3 μm.

The recent acquisition by UCSB of a Deep UV (DUV) flood exposure system, will facilitate planarization of irregular surfaces and subsequent metal lift-off. The process, transferred from OCI to UCSB, incorporates conventional positive photoresist and photo-sensitive poly (dimethylgutarimide), PMGI, which serves a dual purpose as a planarization and lift-off medium. Multiple layers of PMGI are spin applied to irregular surfaces, ea., VCSEL arrays. The PMGI is then reflowed at 250°C to form a planar surface. As many as 10 layers at 1.1 μm/layer have been applied and reflowed to 5 μm VCSEL mesa arrays providing a planar surface. Conventional contact photolithography is used to define an imaging layer of photoresist applied to the PMGI. The resulting pattern is exposed to DUV at 254 nm which polymerizes the PMGI. The PMGI is then developed in a developer which does not attack the positive photoresist imaging layer. Over-development of the PMGI creates a controlled undercut of the photoresist resulting in a profile ideal for lifting thick layers of evaporated metal.

4.4 Vertical Cavity Surface Emitting Laser Packaging Technologies

Vertical cavity surface emitting lasers can now produce considerable optical power at low bias at high data rates, however they are not yet used for any real application. For this to occur, it was necessary that certain packaging issues be addressed and solved. During Phase II Optical Concepts has addressed the issues of flip chip bonding of VCSELs for electrical and thermal conduction, and the optical coupling of light from VCSELs into optical fiber.

4.4.1 Flip chip Bonding

For effective low cost high-density electrical connections, flip chip bonding of devices is a very useful technique. Optical Concepts is investigating three different flip chip bonding processes for VCSEL arrays. One process is the standard solder bump bonding, the second is a solderless polymer flip chip technology, and the third is a new approach being developed by Optical Concepts in collaboration with UCSB. The solder bump bonding process has become an industry standard but is an involved process with many metalization layers and is mechanically brittle. The solderless polymer flip chip technology is a simplified two step process with an electrical bond that is more elastic than a solder bond. The new approach being undertaken by Optical Concepts is similar to the conventional solder bump bonding process but could possibly result in a environmentally sealed active device array. A critical component to successful solder bonding of devices is the metalization of the contacts.

4.4.1.1 Solder Bumps on Vertical Cavity Surface Emitting Lasers

Initial experiments with solder bump technology have been performed by Optical Concepts in collaboration with UCSB. Three different types of solder have been used with various degrees of success: AuSn, PbSn and In solders. Each of the solders have different properties some of which may cause problems with VCSELs. If the contacts have a solder connection there are some potential problems that result. In initial experiments AuSn solder was not acceptable. It did provide a good mechanical contact, but since the solder is hard it destroyed the weak contact to the top of the laser. In solder on the other hand is a ductile solder and therefore does not destroy

the top contact. It does leech away the gold metallization, and therefore requires a solder barrier. This poses an entirely different problem. The only evaporated metals currently available in our subcontracted facilities to make solder barriers, such as nickel and tungsten, are highly stressed after evaporation. This means that the solder barrier layers themselves may destroy the weak top contact. Even with the potential problems, this was the only workable solution since the AuSn solder did not work.

Using nickel as a solder barrier, both PbSn and In solders were successfully used in bonding VCSELs onto diamond substrates. The PbSn solder initially appeared to be the best solder since the solder process was very simple with 100% yield and good mechanical strength. Unfortunately, the lasers degraded over a period of hours as their top contacts slowly peeled off, presumably due to the additional stress caused by the solder. In solder was much more difficult to use, but for devices which were successfully bonded, the reliability was excellent. Bonding such devices onto diamonds has produced the highest CW VCSEL powers to date[3,12].

Indium solder has also been used to successfully bond a 1X18 VCSEL array onto a sapphire substrate, using nickel as a solder barrier. This was performed by using a makeshift alignment procedure, relying on the transparency of GaAs, silicon and sapphire to infrared light. A standard CCD video camera was focused on the substrate metallization. A silicon substrate was used to block stray visible light, and a infrared light source was used to shine through the VCSEL and contact substrates. Figure 4.4a shows a picture of the VCSEL wafer and contact substrate before alignment. While not practical in the long term for low cost packages due to the large amount of required manual labor, this process provided useful experience in mounting VCSELs.

4.4.1.2 Optical Concepts Flip Chip Bonding

The novel flip chip bonding technology Optical Concepts is working to develop for VCSEL arrays is a self aligned process that shows promise as being a environmentally sealed package. This process initially incorporated deep UV sensitive poly (dimethylgutarimide) (PMGI) and conventional positive photoresist for the precise formation and mating of evaporated solder
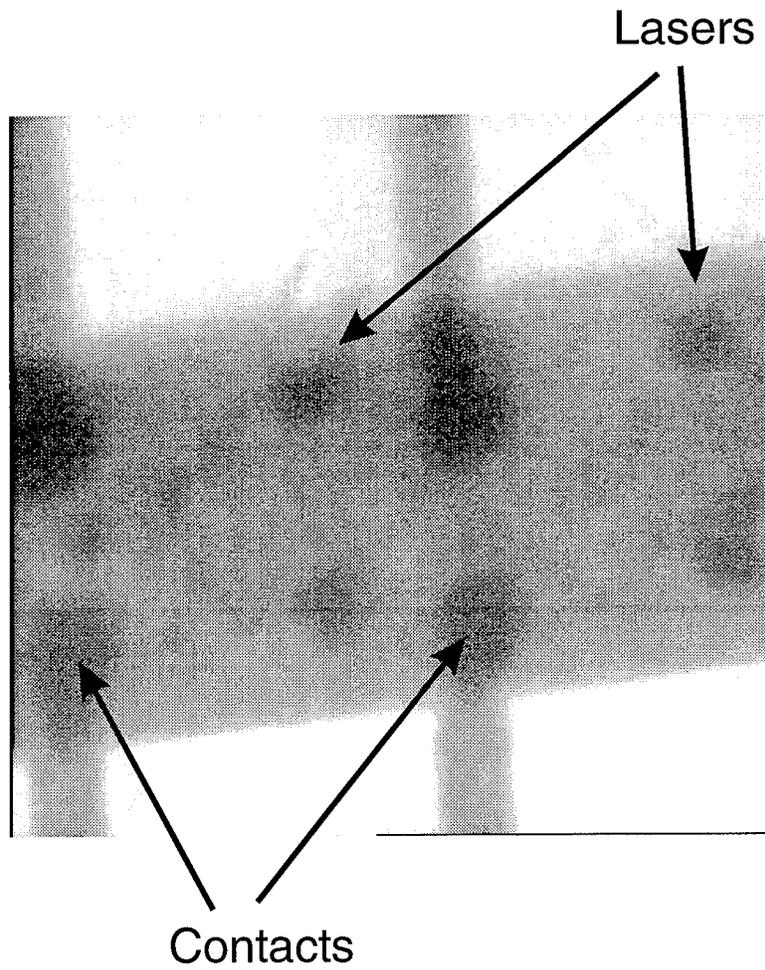
Infrared Alignment

Figure 4.4a

bumps on VCSEL arrays to solder bumps on a dissimilar substrate. PMGI has received wide use in the semiconductor industry for planarization and double resist liftoff processes. When cured PMGI exhibits excellent electrical and mechanical properties similar to that of a glass and undergoes a glass transition at 189°C. The PMGI is used with photoresist to define solder bumps on both the substrate and the device array. The photoresist and the PMGI are lifted off from the VCSEL array leaving only the solder bumps, while the photoresist is removed from the substrate leaving both the PMGI and the solder bumps (Figure 4.4b). The hole in the PMGI serves to aid the alignment of the solder bumps. Once alignment is reached, the bumps on the VCSEL array will literally fall into place (Figure 4.4c). The substrate is then heated to melt the solder and reflow the PMGI. Once cooled, the solder bumps provide the electrical and thermal conduction while the glass-like PMGI provides mechanical support (Figure 4.4d).

This process has three inherent advantages over conventional solder bump techniques. In conventional solder bump bonding the alignment is somewhat difficult, requiring expensive alignment equipment. The PMGI based solder bump process provides a built in alignment once the coarse alignment is accomplished. Also, in conventional solder bump technology, epoxy is backfilled around the solder bumps for structural support. This is required due to the small size of the solder bumps. By using the PMGI process, the PMGI automatically takes the place of the backfilled epoxy in providing structural support for the chip. Lastly, the PMGI provides a seal around the VCSEL circuitry separating the laser from the environment.

During the first year of Phase II this procedure looked extremely promising. Early in the final year of Phase II, Shipley discontinued production of PMGI, which was picked up by another company. The new PMGI, unfortunately, has properties that are not appropriate for the self aligned process. In particular, the present PMGI cracks once exposed to acetone during removal of the photoresist. As a result we are proceeding in two directions with this process. We are working with the manufacturer of the PMGI who at this time is willing to adjust their process. Also, we are investigating other materials to be used in the same way as the PMGI. Ideally, we would like to use a material that is appropriate for inclusion in a hermetic package.
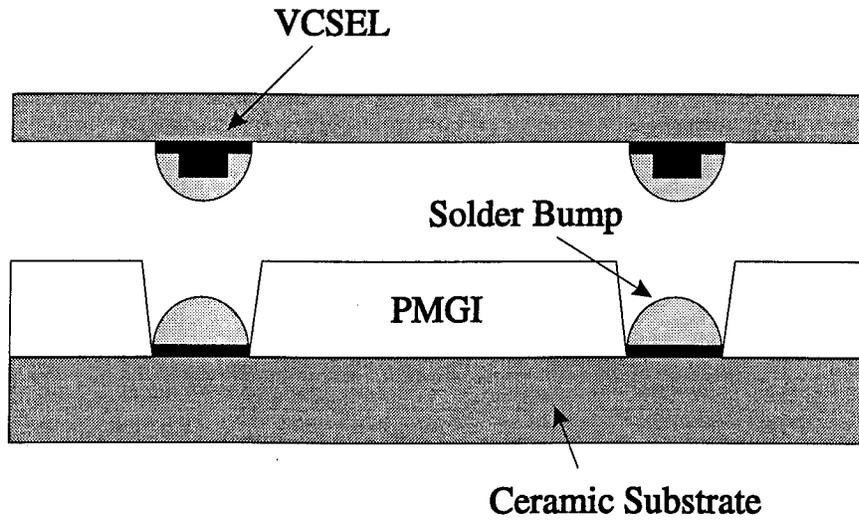
VCSEL

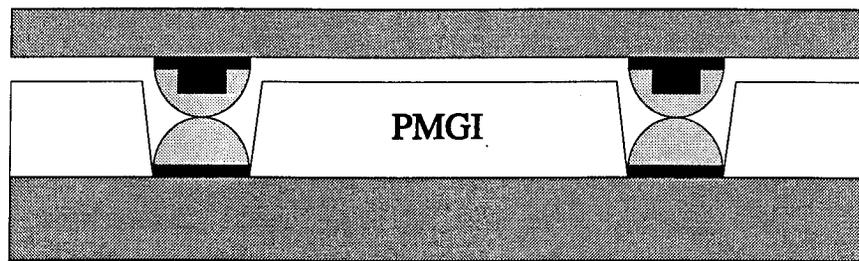Solder Bump

PMGI

Ceramic Substrate

Figure 4.4b

PMGI

Figure 4.4c

PMGI
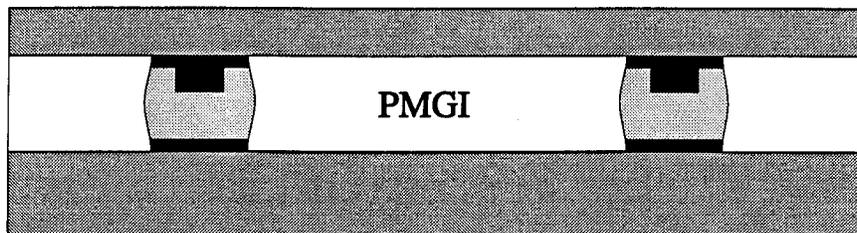
Figure 4.4d

4.4.1.3 Solderless Polymer Flip Chip Process

The commercially available solderless polymer flip chip technology has been developed by Epoxy Technology Inc. The electrical bond is made with an IR curable silver epoxy with a volume resistivity in the range of 0.1-0.4x10-3 W-cm that is mechanically compliant. The degradation temperature of the polymer epoxy and dielectrics used in the process is 400°C with a continuous operating temperature range of -55°C to 200°C. These resistivity and temperature ranges should prove adequate for many of the packaging applications Optical Concepts is considering. The above method may be appropriate on the long term once large volumes of devices are being produced. Unfortunately, since this requires that devices are sent to Epoxy Technologies for the bonding, it removes from Optical Concepts the desired process control and creates an unwanted dependency on an outside company. Thus, even though the process may be acceptable, it will not be pursued in this program.

4.4.1.4 Specialized Equipment for Solder Flip Chip Bonding

For Optical Concepts to optimize the flip chip process, there are two pieces of equipment which will be necessary: a dedicated thermal evaporator, and an alignment fixture.

As mentioned earlier, the metallization is a critical aspect of the solder bump process. At present Optical Concepts is limited to only a few metal sources for solder barriers and ohmic contacts. There are possible refractory ohmic metallization schemes with which Optical Concepts has experience that should provide good reflectivity ohmic contacts that are stable even at high temperatures. Optical Concepts hopes to develop such metallization schemes fully in the future. Also there are metal layers which will provide low stress solder barriers, a necessary component for high reliability devices and, a dedicated thermal evaporator would be used to develop these solder barriers.

In sections 4.4.1.1 and 4.4.1.2, two different bonding schemes were discussed, both of which require careful alignment. At first, transparent sapphire substrates have been used to make alignment possible. Since then, Optical Concepts staff have used an infrared mask aligner to

position laser arrays on opaque substrates such as silicon and aluminum nitride. This procedure works, although the yield is not sufficient for manufacturing. In the long term, it will be necessary to have an alignment fixture for mounting VCSEL arrays.

4.4.2 Fiber Optic Coupling

Optical fiber ribbons are currently made from single and multimode fibers. The separation between the individual fibers is 250 μm at present; new fiber ribbons are being developed with 140 μm spacings. Existing fiber ribbons can be purchased for both 12 and 18 elements. For the 18 element fiber ribbon, the total ribbon housing is ~5 mm which is comparable to existing electrical telephone lines. The advantage of the vertical cavity technology centers on the parallel possibilities of the devices. The largest (18 fiber) fiber ribbons are the most appropriate, allowing for a 16 bit parallel data path per package; unfortunately, there are no commercially available connectors for the 18 fiber ribbons. For this reason we have adapted the 12 fiber ribbons and connectors made by USCONEC. This provides 8 bit parallel data transfer plus 4 overhead bits.

Fiber coupling to VCSEL arrays is remarkably easy due to the low divergence of the laser emission. We have demonstrated pigtailed arrays using four different types of VCSEL arrays: intra cavity contacted top emitting devices, gain-guided top-emitting devices, large-area flip chip mounted bottom emitting devices and small-area flip chip mounted bottom emitting devices. The fiber coupling procedure is as follows:

Initially, the fibers are actively aligned to the laser array. Then the fiber ribbon is backed away from the laser package using a precision micrometer stage, and epoxy is applied to the laser package. Finally, the fibers are brought back down into the package according to the appropriate measurement made by the micrometer. Once the epoxy has hardened, the devices are fully pigtailed. Because of the ease with which this pigtailing was accomplished, we believe it is possible to automate the procedure for manufacturing. It should be noted, that using this procedure the actual fiber coupling is a passive alignment made based on micrometer settings.

4.4.2.1 Passively Aligned Fiber Ribbons

Once our decision was made early in the final year of Phase II to use the USCONEC fiber ribbon connector, it seemed appropriate to attempt to utilize the USCONEC housing for passive alignment. The USCONEC housing uses two precision alignment pins which could potentially be coupled to the laser package. For this coupling to be feasible we investigated precision machined holes. The result was that existing commercial laser, mechanical and ultrasonic machining companies could not meet the dimensional requirements with only one exception which was a division of IBM. The IBM division was interested in selling the entire laser machining equipment rather than providing machining services. Although the IBM laser machining system may be appropriate for manufacturing, it was certainly out of question for the Phase II investigation.

Recently in cooperation with the University of California at Santa Barbara, Optical Concepts has developed a much less expensive approach for making precision alignment holes. Figures 4.4e and 4.4f show the procedure. Oversized alignment holes are made in the host substrate (that can be anything from aluminum nitride to copper), and the holes are filled with a snap curing epoxy. Next alignment pins are held by a precision housing which a mold release is applied. The pins are then inserted into the oversized alignment holes and the epoxy is cured. After curing, the pins can be removed, leaving precision alignment holes in the host substrate.

Using bottom emitting VCSEL devices, metallization and solder bumps can be added to the host substrate, aligned to the precision holes. Once the devices are flip chip mounted on the host substrate, the pins can be inserted providing the necessary alignment for efficient multimode fiber ribbon coupling. Due to the recent nature of this procedure, no fully pigtailed packages have been made in this way at the time of this report; however, Optical Concepts is actively continuing the development of this process.
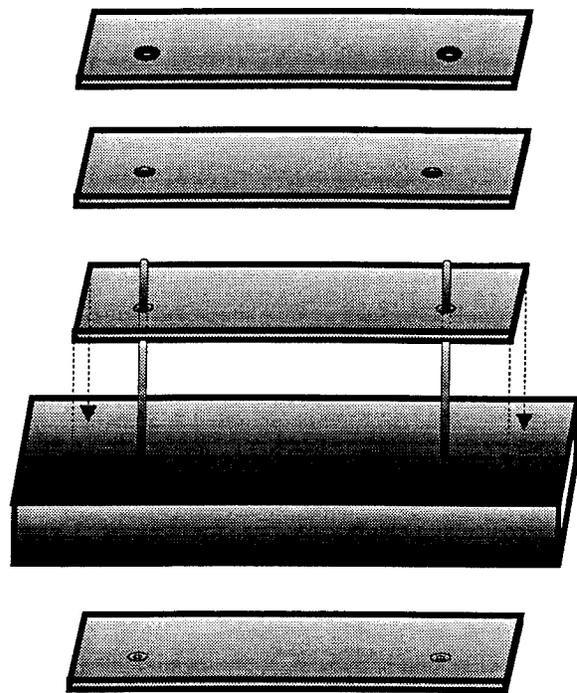
Substrate with drilled holes 2X
diameter of alignment pins.

Fill holes with thermo setting
heat conductive epoxy.

Apply mold release to alignment pins.
Insert pins from alignment block into
uncured epoxy. Place onto hotplate
and cure epoxy.

Remove pins from cured epoxy.

Figure 4.4e
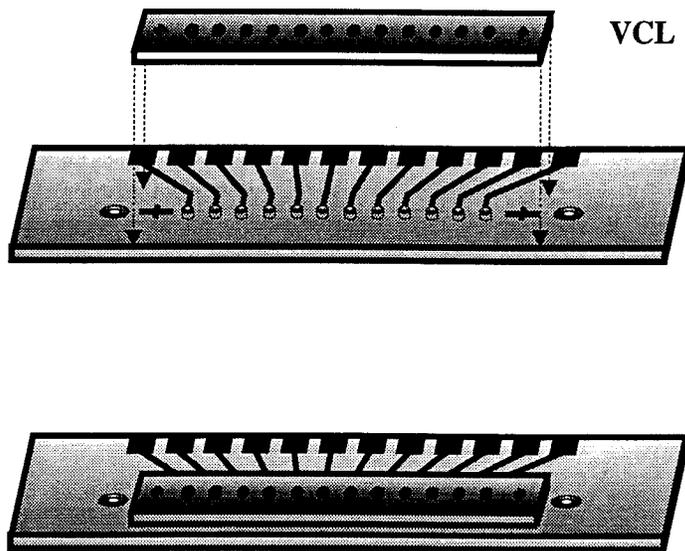
VCL array with solder bumps.

Metal pattern with solder
bumps aligned to precision
alignment pin holes formed
with epoxy.

Flip chip VCL array to
substrate using flip chip bonder.

Figure 4.4f

4.5 Vertical Cavity Surface Emitting Laser Package Designs

The packaging of the devices is a critical step to achieve the maximum performance. Two different packaging schemes were investigated, a hermetic packaging design and a low cost package. Market research conducted during the first year of Phase II showed that the most important market would be for a low cost package, operational at hundreds of MHz to a few GHz, rather than a more expensive, higher performance hermetic package. As a result during the second half of the Phase II effort Optical Concepts produced prototypes of the low cost package and left the more expensive package in the design stage for later development.

4.5.1 High Performance Hermetic Package

The goal of the hermetic package design is to provide the highest reliability and speed possible. We believe that the package outlined below has very little risk, relying on conventional packaging techniques such as wire bonding and all optical alignment, external to the package. Taking advantage of the high-speed and beam qualities of these laser arrays, it is expected to provide higher aggregate bandwidth at lower cost than most high-speed sources. Considering the temperature stability, parallel data path and full on/off modulation capabilities of the lasers, the link will greatly reduce the complexity and cost of the controlling electronics. In the final product, some degree of multiplexing using custom ICs may be used to enable the transfer of 32 to 64 bits on 8 to 16 fibers. In this program, we have studied the packaging technologies necessary to make this data link, but have opted to make prototypes using a less stringent design. Also, integration with ICs is outside the scope of this program but definitely in the product development plans.

The ring contacted devices are fabricated on semi-insulating GaAs/AlAs mirrors using intra-cavity contacts. This allows for interconnects and bonding pads to be deposited on the GaAs substrate without increasing the parasitic shunt capacitance. The output beam is directed through a window, with the fiber coupling done after the package is sealed. Using multimode fiber and the low beam divergence of the lasers, very high coupling efficiencies can be achieved for fiber-

to-laser separations of up to 10 mil (250 µm) which allows such external coupling schemes. The advantage of this scheme is that the hermetic sealing can be done using conventional processes. Device reliability remains a key area of future work, and the hermetic-packaged wire-bonded devices allow a study of the lasers' degradation properties without introducing the additional uncertainties of flip-chip contact stresses or epoxy outgassing. While the low cost plastic package described below is the preferred long term solution, the hermetic package is the lowest risk design in the near term.

4.5.2 Low Cost High-speed Computer Interconnect

The goal of the low cost package is to produce a low cost, volume manufacturable high-speed parallel data link. Bottom emitting devices have the simplest fabrication sequence and are therefore the least expensive to produce. The initial prototype packages contained 1X12 VCSEL arrays; however, ultimately, the package will also contain custom silicon or GaAs driver circuitry. The VCSEL devices were flip chip bonded onto an aluminum nitride submount in order to provide the thermal and high-speed electrical connections. This was done according to the procedure outlined in Section 4.4.1. Then, following the procedure laid out in Section 4.4.2, multimode fibers were actively aligned with the VCSELs. At this point the package is essentially complete, and this is the state of the prototypes. The final step would then be to encapsulate the entire package in plastic, providing a better strain relief for the fibers.

A schematic of the package design is shown in Figure 4.5a. The VCSELs are mounted onto the AlN submount with either flip chip bonding for bottom emitting devices, or wire bonding for top emitting devices. The submount is inside a single sided butterfly package with wire bonds between the package and the submount. With the pins coming out only one side of the package, the package can then be mounted as shown in Figure 4.5b. This initial design is attractive from a prototyping perspective because it is relatively inexpensive to produce. No polymer waveguide technology or angle polished fibers are required for the light to exit at right angles to the electronics board, rather the corner is turned by the package itself, and a relatively simple butt-coupling of optical fibers is performed.
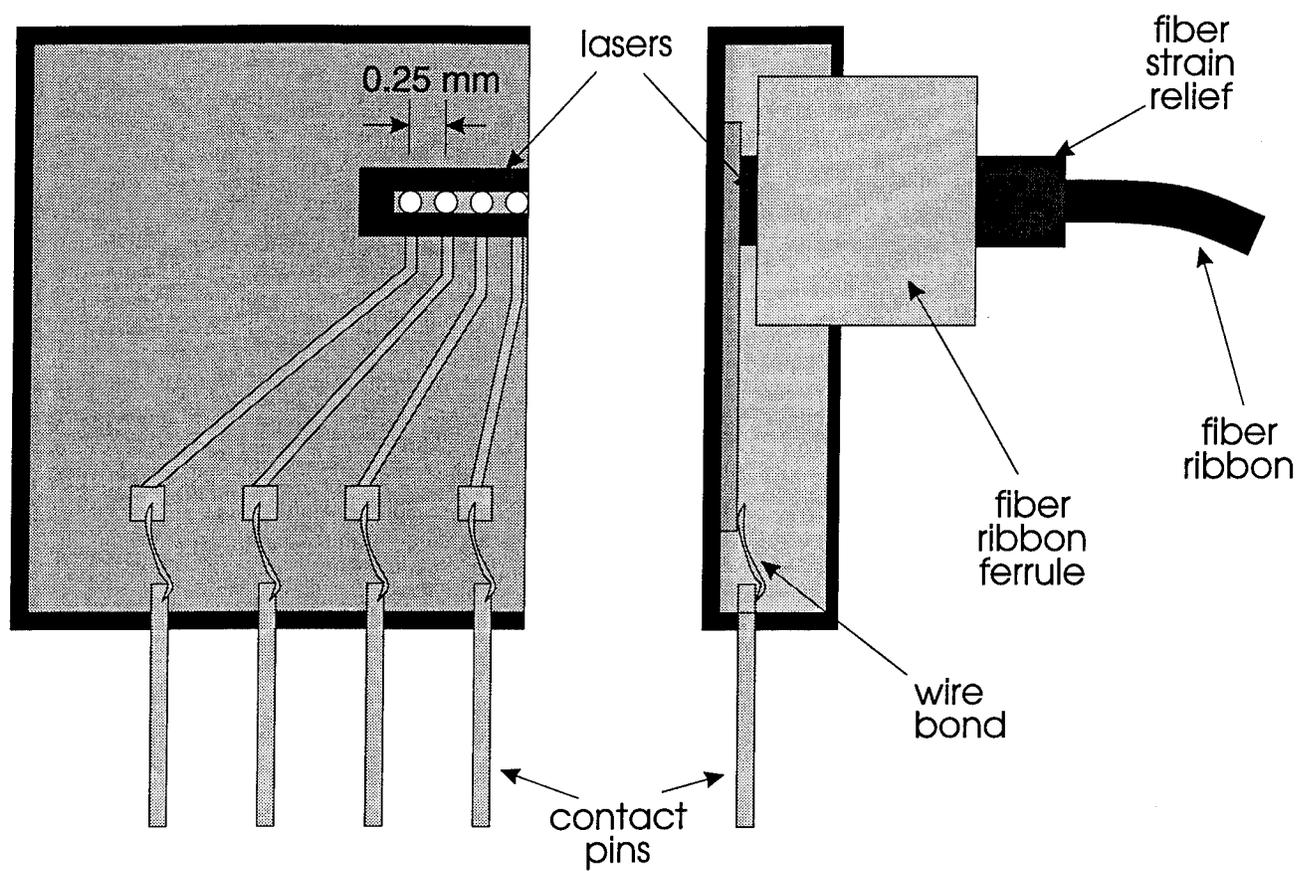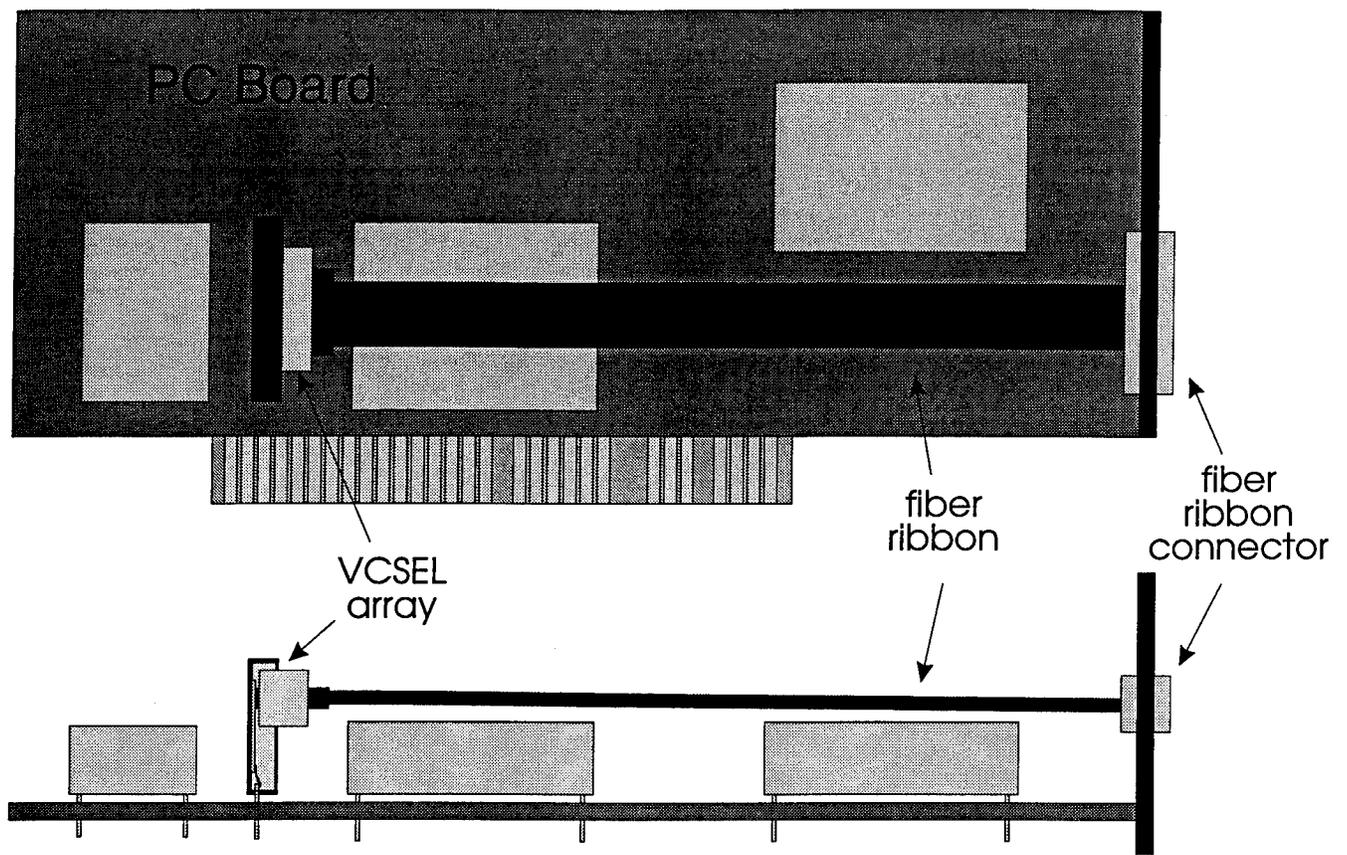
Bottom Emitting VCSEL Packaging Schematic

Figure 4.5a

Figure 4.5b

4.5.3 Prototype Device Arrays

The actual prototypes developed during Phase II were a variation of the low cost design. Aluminum nitride submounts were made using material from Film Microelectronics Inc. The material was delivered metallized on 3" square substrates, laser scribed to be easily broken into individual parts. A custom mask was designed and purchased from Precision Photo Mask for the fabrication of the submounts. Due to high expense of custom packages when purchased in small quantities, Optical Concepts chose an available butterfly package which was then cut in half to form two single sided packages. The resulting package can be seen in its various stages of development in the following Figures. Figure 4.5c shows the bare package with the aluminum nitride subcarrier. The subcarrier was designed to accept both top emitting wire bonded device arrays (Figure 4.5d) and flip chip mounted bottom emitting device arrays (Figure 4.5e). Figure 4.5f shows the subcarrier installed inside the package with a flip chipped VCSEL array mounted on the subcarrier. The next figure, Figure 4.5g shows a close up view of the flip chip mounted VCSEL array. Once the fibers were epoxied onto the package, the package appears as shown in 4.5h. At this point additional epoxy is used for additional strain relief for the fiber ribbons, and the prototype package is complete. This package design has aided us in the development of the relevant packaging technologies: wire bonding, metallization, solder bumps, flip chip bonding and fiber alignment. In this regard it has been highly successful.

## 4.6 Receiver/Transmitter VLSI Design

During the final year of Phase II, we have initiated the development of interface circuitry for VCSEL arrays through a consultant. The consultant's report is included in Appendix A.

4.7 Packaged Device Performance

Optical Concepts has completely packaged and pigtailed four types of VCSEL arrays: intra-cavity contacted top emitting, gain-guided, large multimode bottom emitting and small single
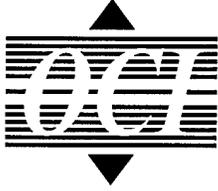
Aluminum Nitride
VCSEL array subcarrier

Bare VCL Array Package
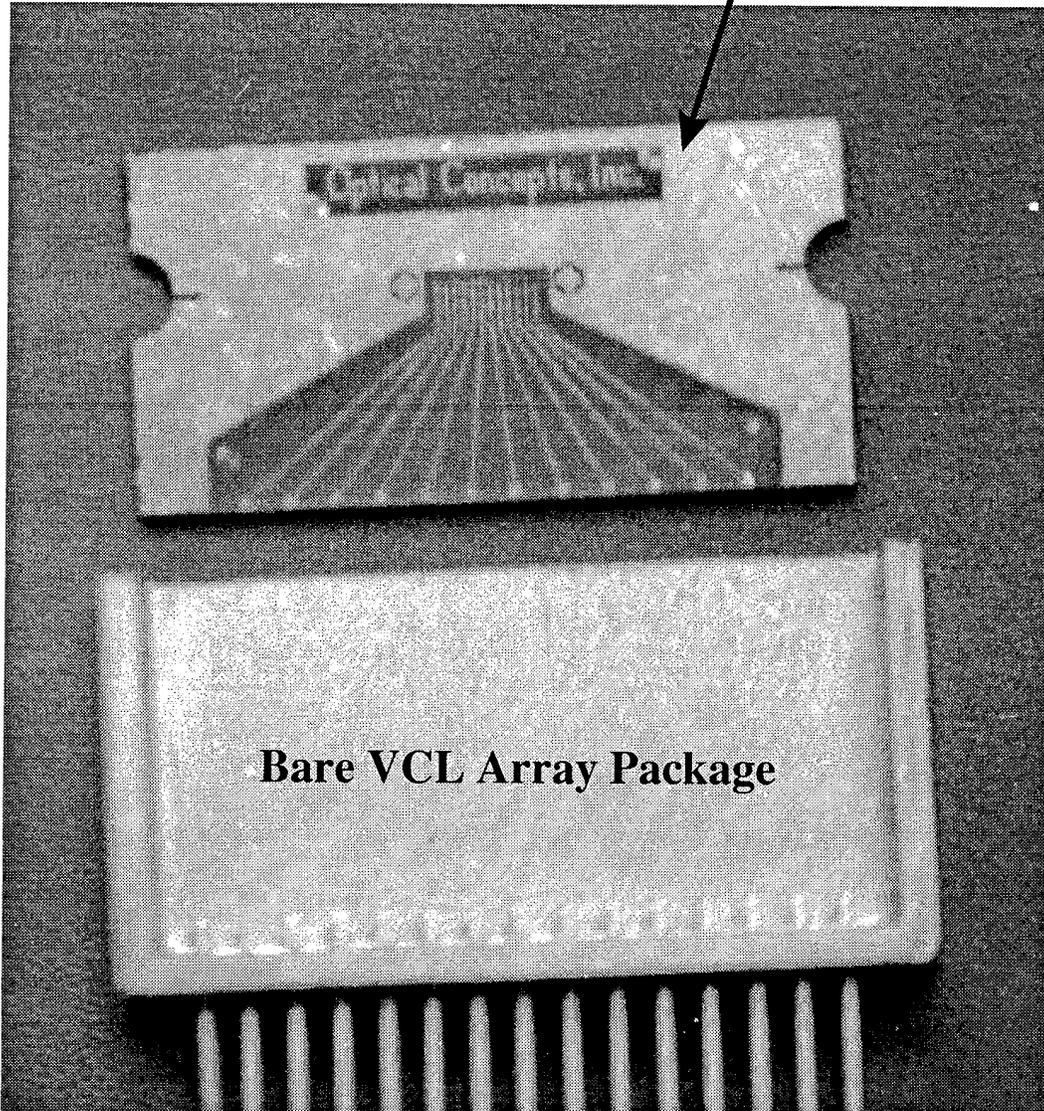
Close up of VCSEL Array Package

Figure 4.5c

7 μm diameter VCSEL

250 μm
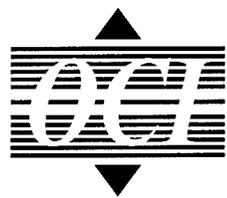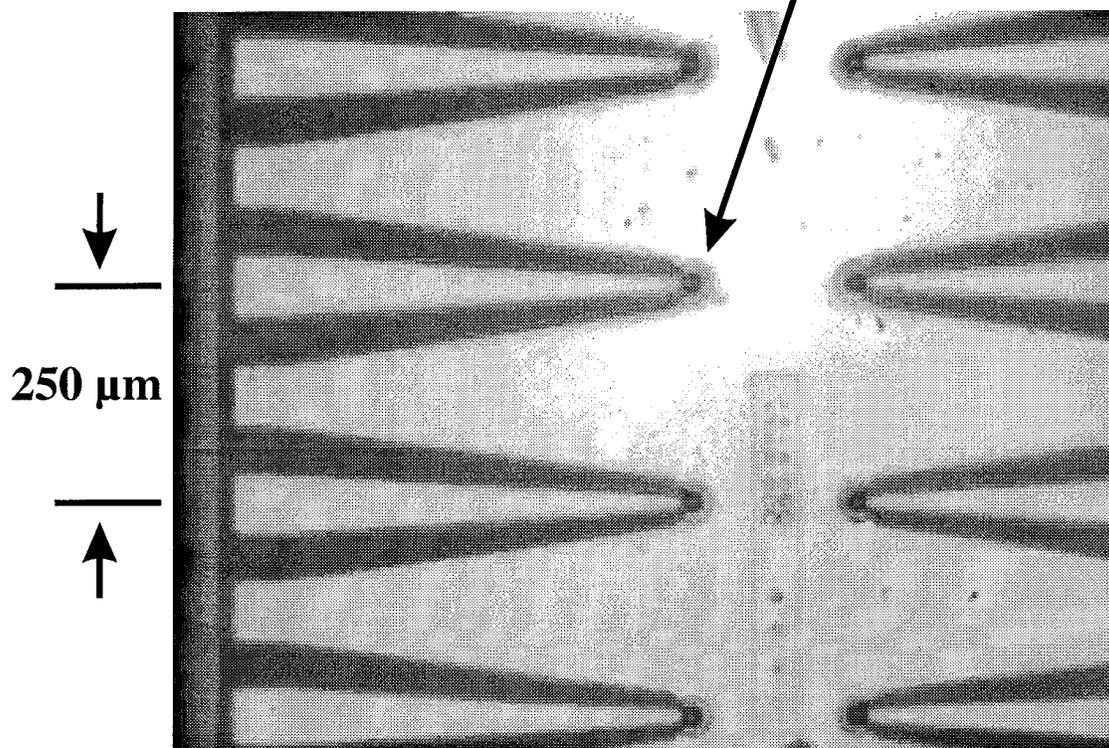
**Close up of Top Emitting
VCSEL Array**

Figure 4.5d
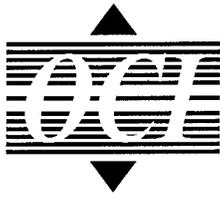
Spontaneous Emission
from 10 µm diameter VCL

250 µm
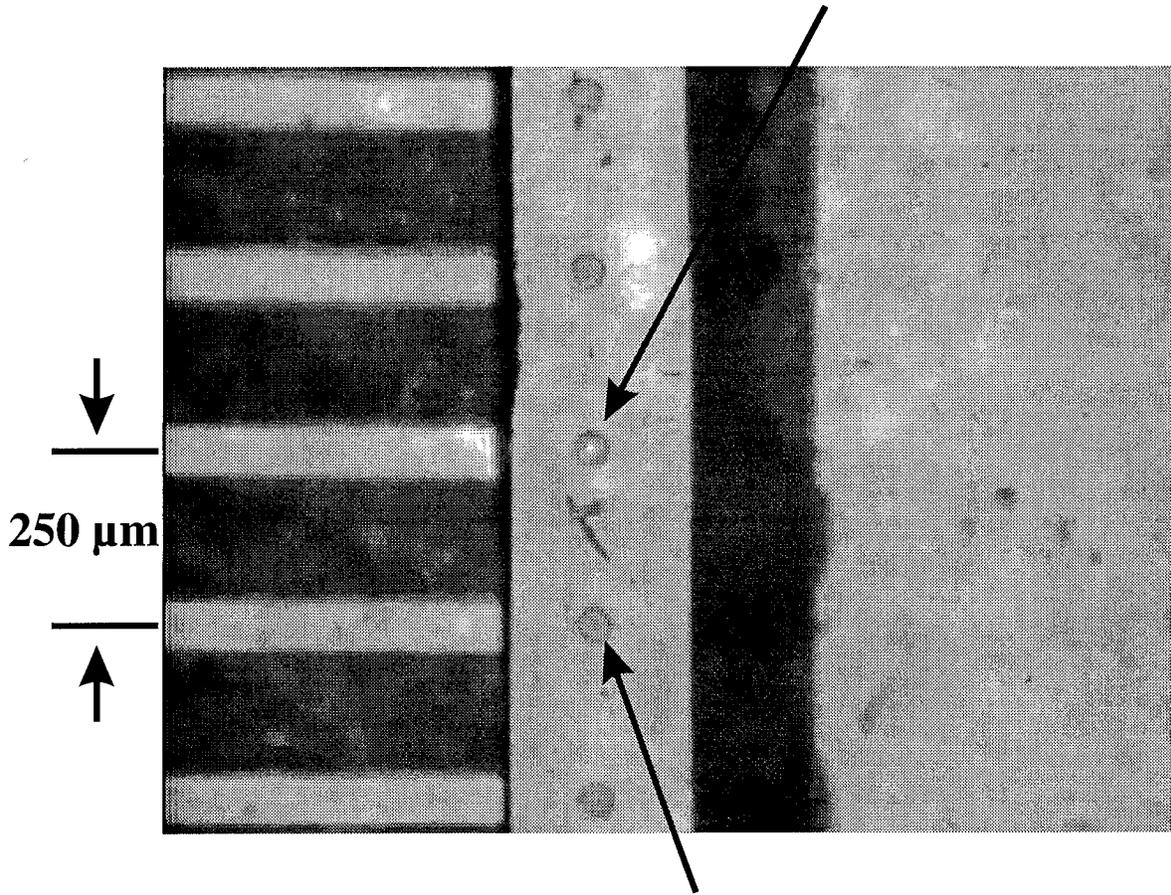
50 µm diameter
window in back
side metalization

Close up of Bottom Emitting VCSEL Array

Figure 4.5e

VCSEL array

Bottom Emitting VCSEL Array Package

Figure 4.5f

Flip Chip Mounted
Bottom Emitting VCSEL Array

Figure 4.5g

Optical Fiber Ribbon

VCSEL Array Package

Figure 4.5h

mode bottom emitting lasers. The packaging yields some valuable information into the potential performance of a complete link.

4.7.1 Intra-Cavity Contacted Vertical Cavity Surface Emitting Lasers
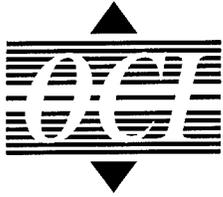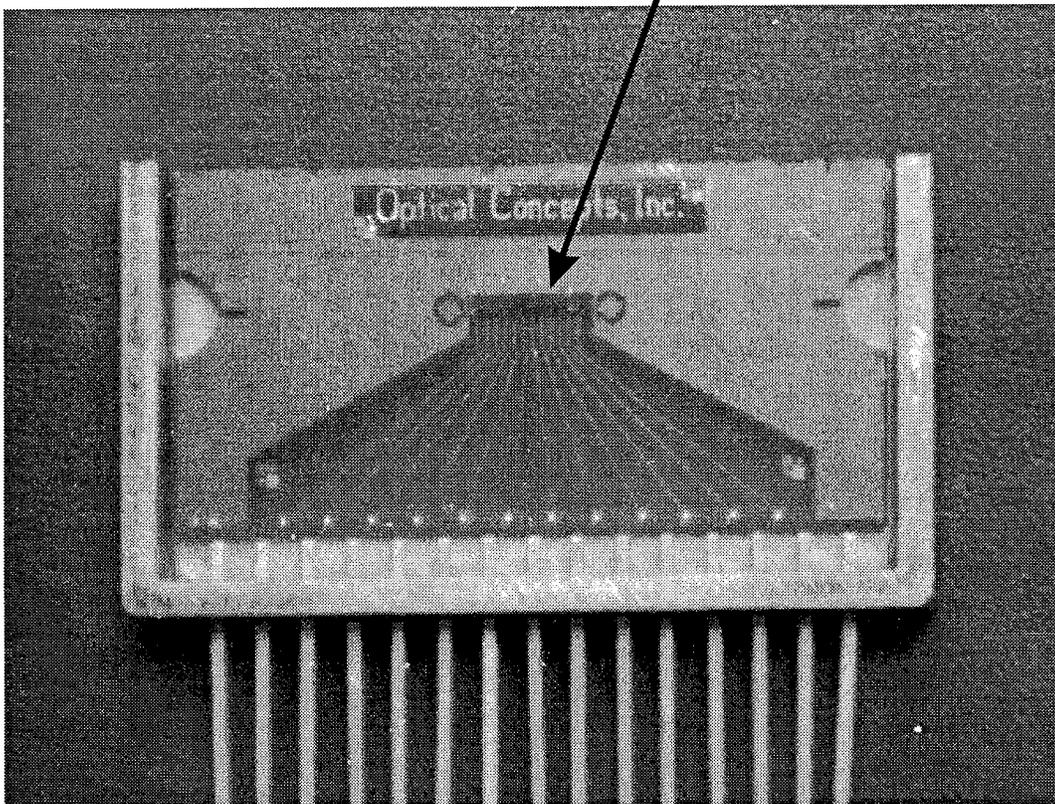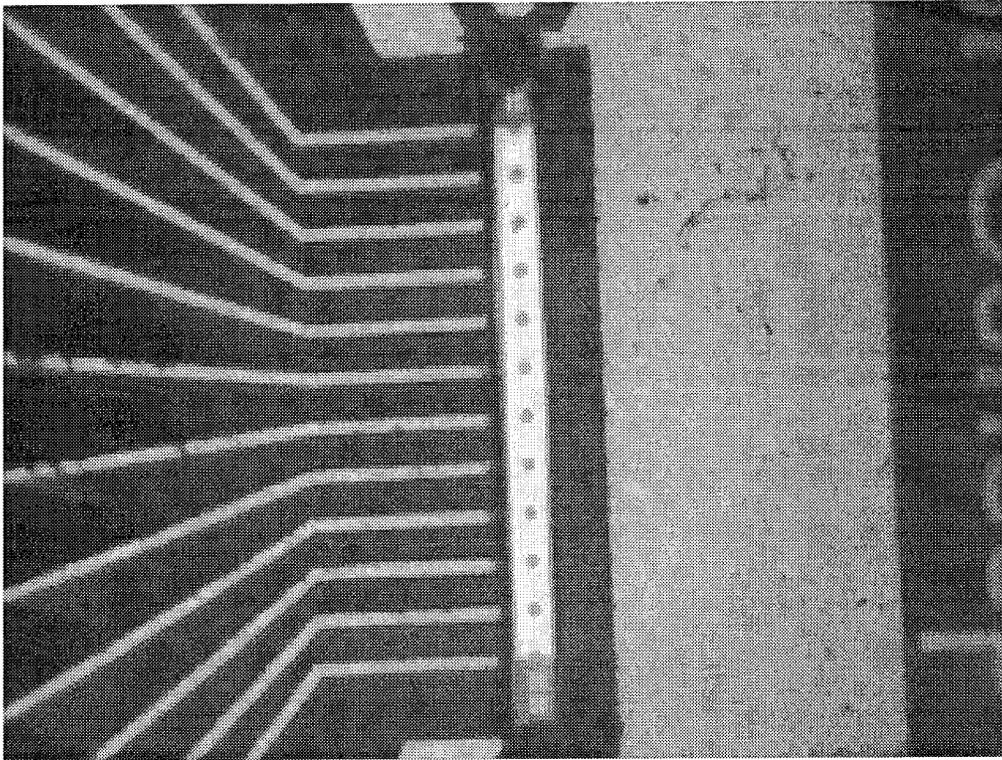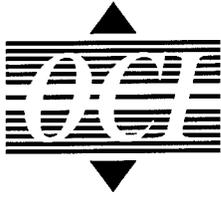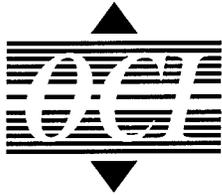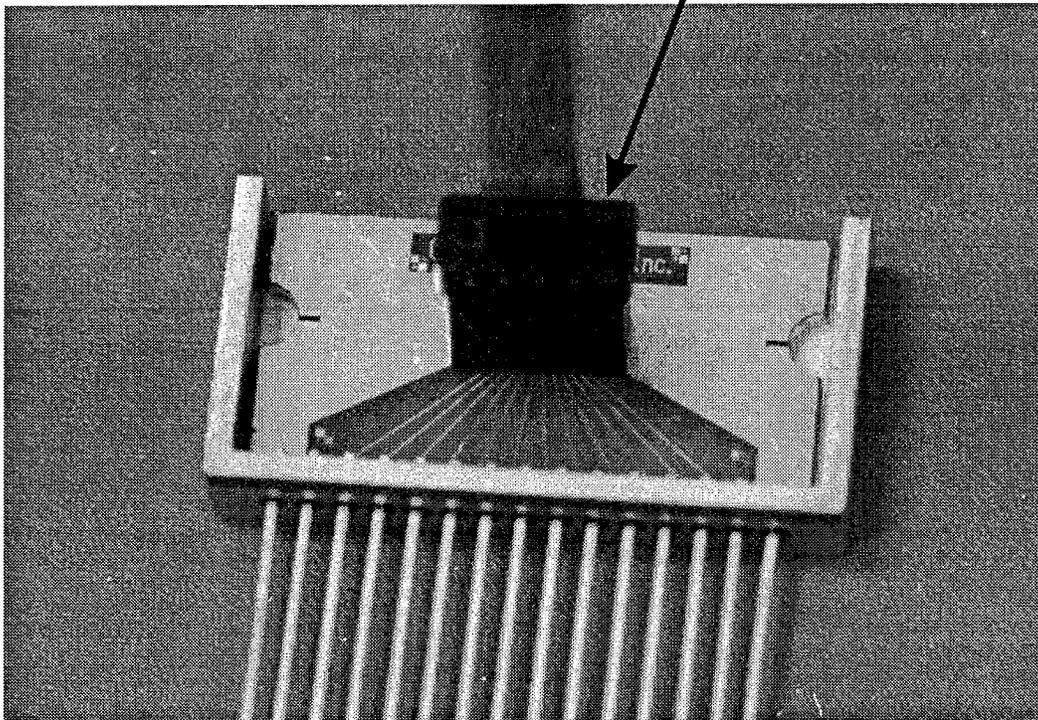
Intra-cavity contacted devices with diameters of 5 μm, as described in Section 4.2.1, were fully packaged and measured. The packaging sequence for the top emission devices is described in the previous section. Since the intra-cavity contacted top emission devices use the semiconductor/air interface as part of the exit mirror, it was anticipated that the direct butt fiber coupling of the device arrays might alter their performance. To investigate this, we tested the devices before and after the fiber coupling. Figures 4.7a and 4.7b show the light vs. current curves before and after fiber coupling. It is noticeable that the device properties across the array were less uniform after the fiber coupling than before, and that the threshold currents and output powers increased. This is consistent with the design of the given devices.

The intra-cavity contacted devices were optimized for high output powers, and as a result the reflections at the semiconductor/air interface become a significant part of the output mirror. Since the semiconductor/epoxy interface is less reflecting than the semiconductor/ air interface, the output coupling of the devices increases (resulting in greater maximum output powers), and this requires more gain for threshold to be reached. In general the greater the output coupling of the exit mirror, the more sensitive the devices will be to external changes. This phenomenon can be seen by examining in-plane semiconductor diode lasers. These devices have mirror reflectivities of about 30% and are extremely sensitive to any optical feedback. VCSEL by contrast have mirror reflectivities of greater than 90% and are highly insensitive to external optical feedback.

The design of manufacturable intra-cavity devices would need to be less sensitive to external changes than the devices as measured in order to eliminate the partial non-uniformities in performance as seen in Figure 4.7b. By adding extra mirror periods, two potential problems would be solved. First, the differential efficiency would decrease, making the light vs. current

Packaged Top-emitting VCSELs

Figure 4.7a

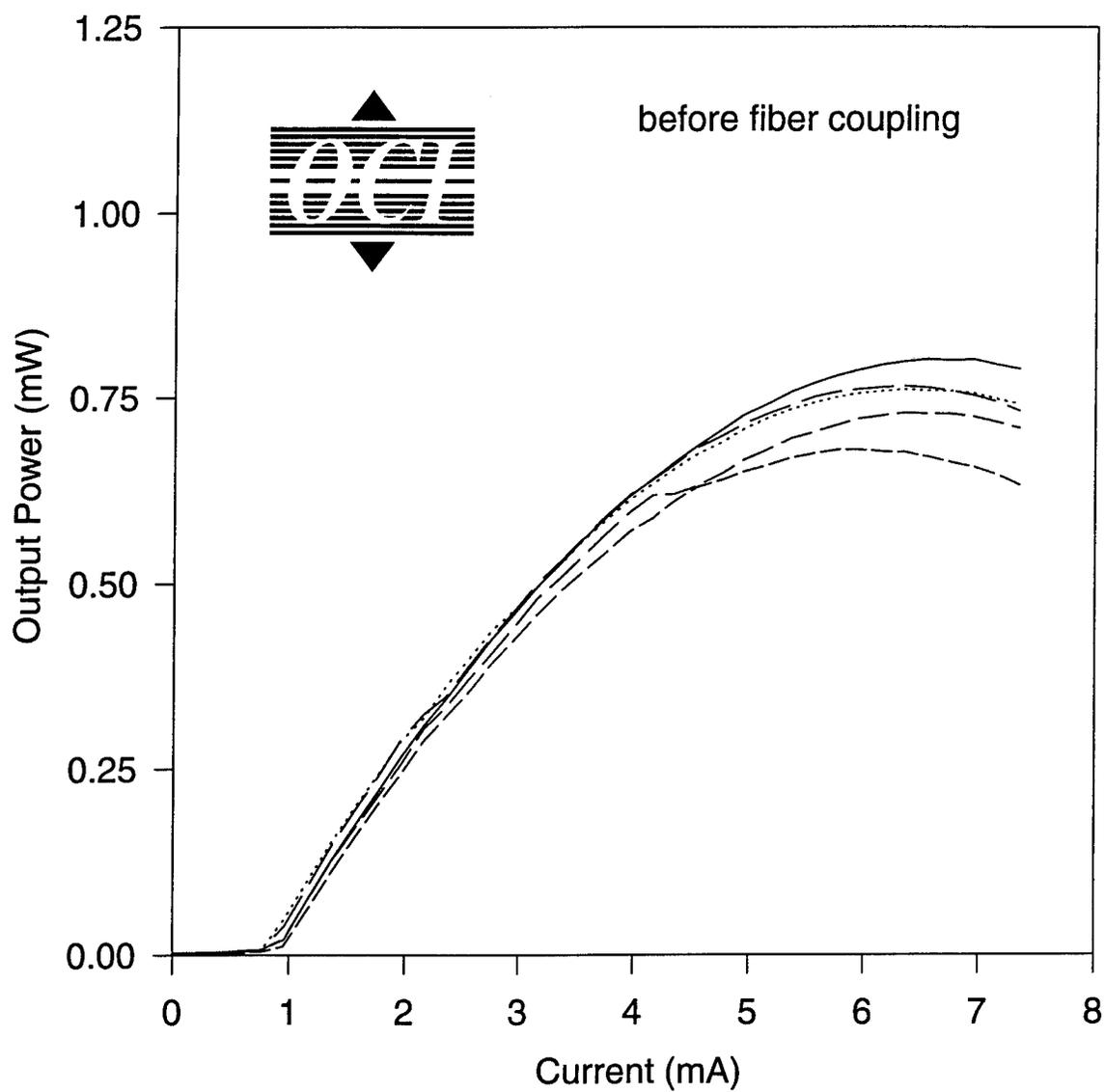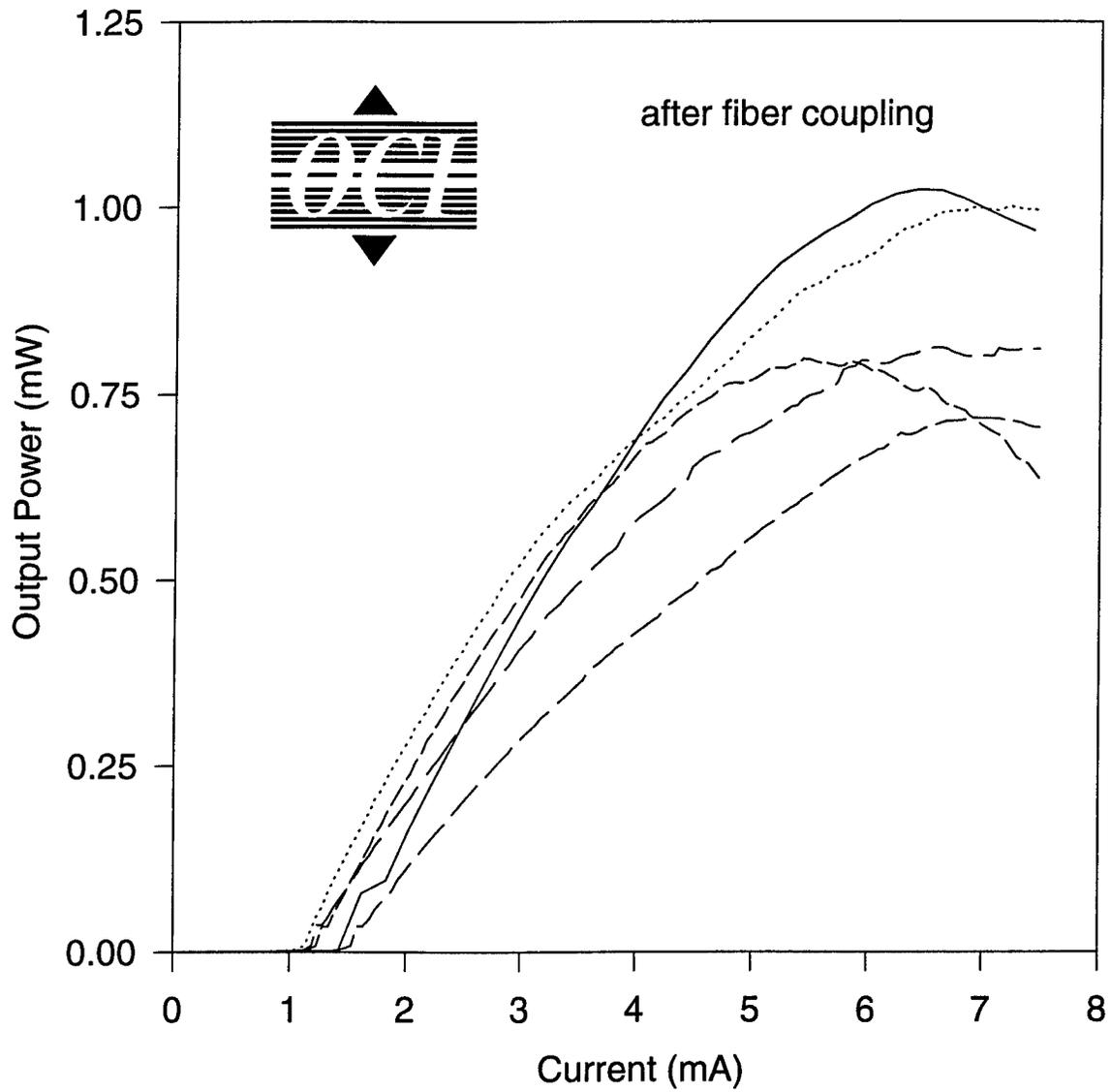# Packaged Top-emitting VCSELs

after fiber coupling

Figure 4.7b

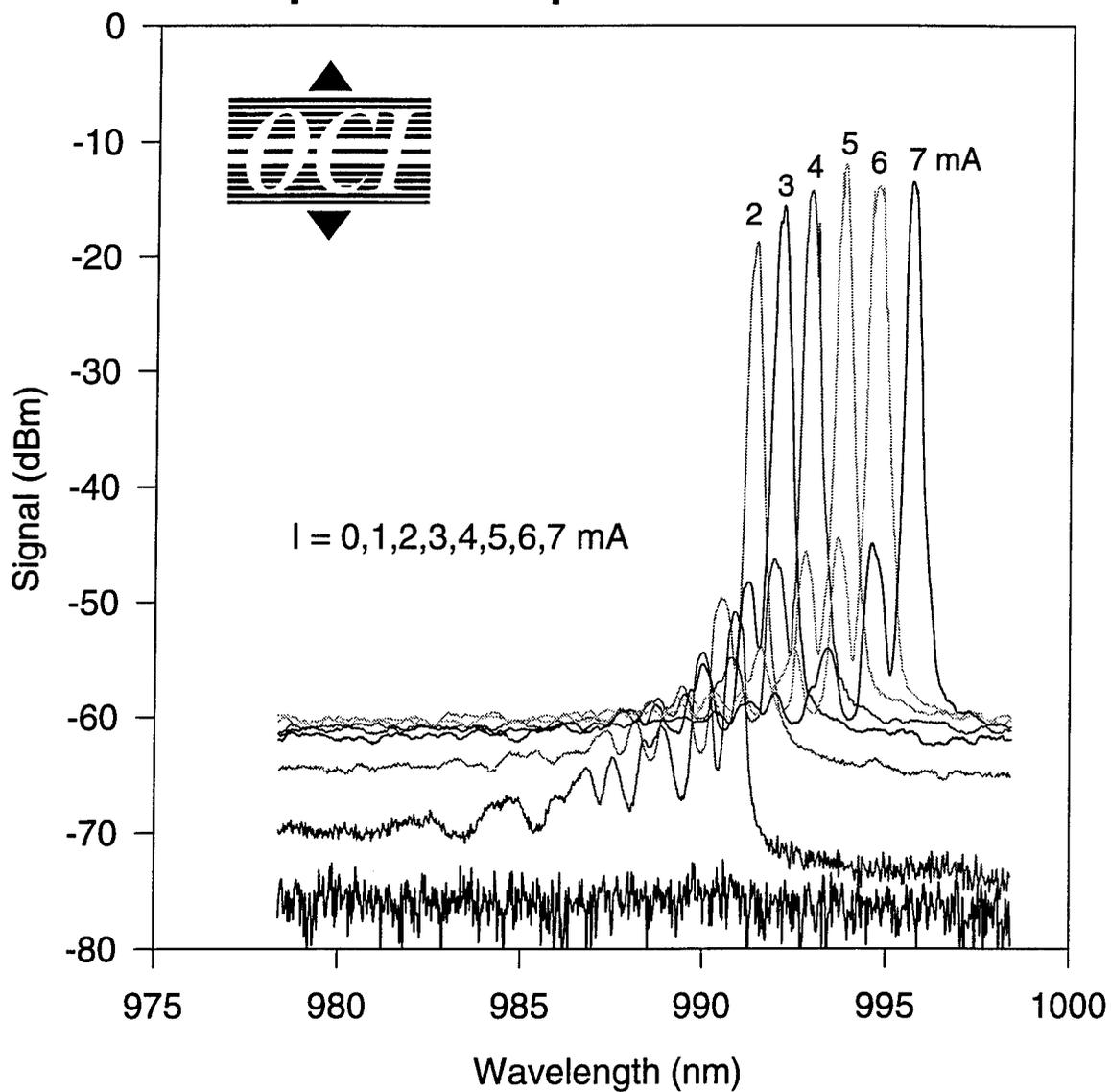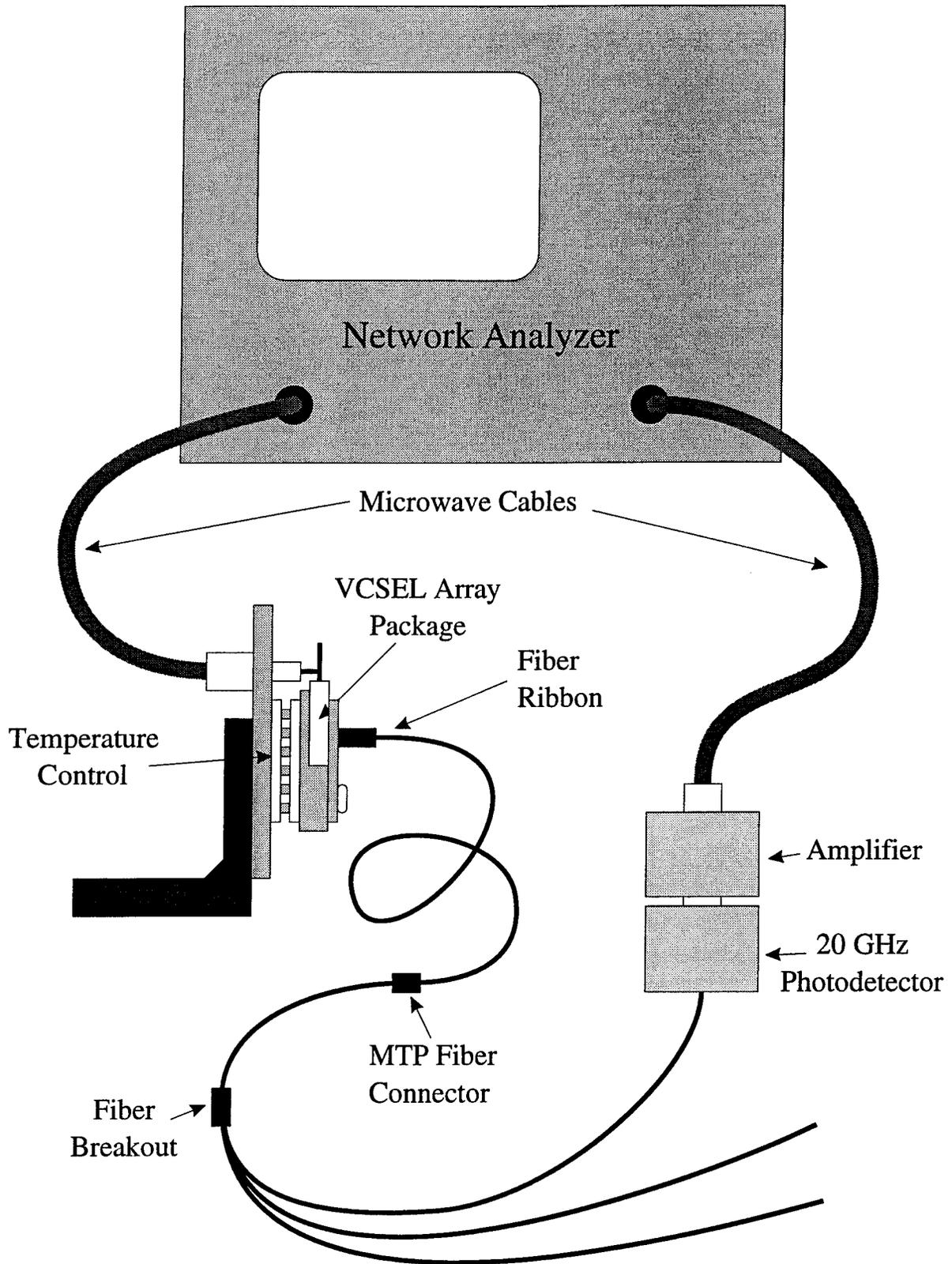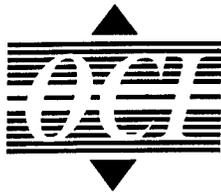# Spectra for 5 µm diameter VCSEL

I = 0,1,2,3,4,5,6,7 mA

Figure 4.7c

Figure 4.7d

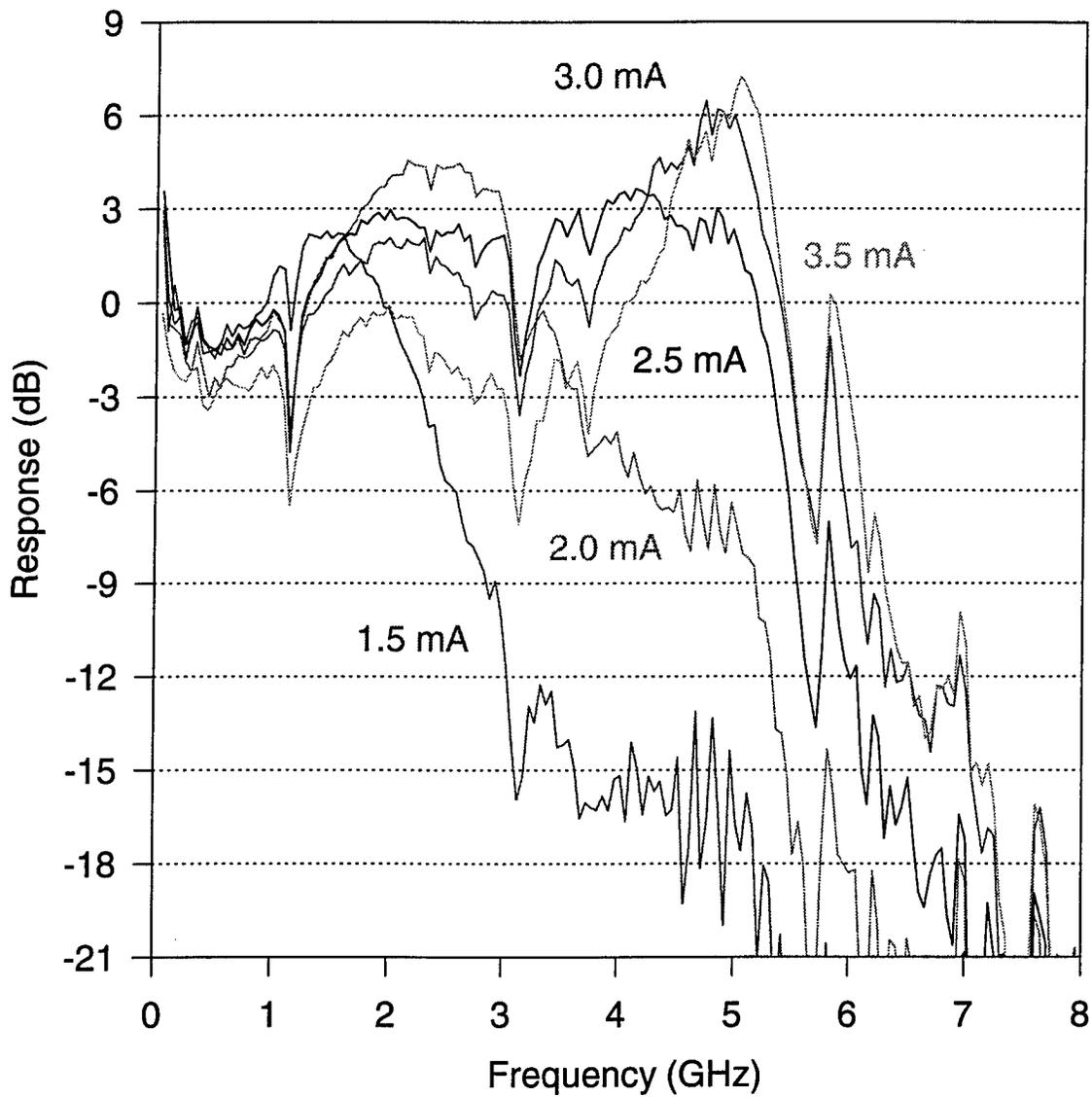# 5 μm diameter Top Emitting VCSEL

High Frequency Response

Figure 4.7e

characteristics much more uniform across the device array, and second the extra mirror periods would serve to ensure only negligible changes in device performance after fiber coupling. This second point was proven by the next packaged VCSEL arrays to be discussed.

After the completed packages were made, additional tests were performed on the device arrays. Figure 4.7c shows the optical spectra coupled into the fiber as a function of the input power. One can see that the second lateral mode stays greater than 30 dB below the fundamental mode over the entire useful bias range.

Microwave measurements were then performed on the fully packaged devices. This was done as shown in Figure 4.7d. A 13.5 GHz HP network analyzer was used in conjunction with a 20 GHz New Focus photodetector and microwave amplifier. Individual devices were tested using a fiber ribbon to FC-PC individual fiber adapter from USCONEC. The adapter was connected to the pigtailed VCSEL array using USCONEC MTP press fit fiber ribbon connectors. The microwave response of the lasers in the package was almost identical to the response of the lasers when tested in the manner discussed in Section 4.2.1.2. The response of Figure 4.7e shows some high-frequency resonances at 1.2 and 3.2 and 5.5 GHz, which are assumed to be due to elements in the package design and are currently under investigation. These resonances are not critical for initial application requiring VCSEL arrays, since the first anticipated applications will operate at speeds from 100 MHz to 1 GHz per channel.

4.7.2 Gain-guided VCSELs

Optical Concepts received some complete VCSEL arrays from Sandia National Laboratories as part of our sub-contract. The devices were 25 μm diameter top emitting gain-guided VCSELs operating at 980 nm. These VCSEL arrays were packaged and measured in the same manner as the intra-cavity contacted VCSELs.

The typical fiber coupled output of the devices is shown in Figure 4.7f. Here, one can also see the high quality of the epitaxial material as demonstrated by the very low threshold and drive voltages. The optical spectra from the devices is shown in Figure 4.7g. The multimode nature of

25 µm diameter Gain-Guided VCSEL
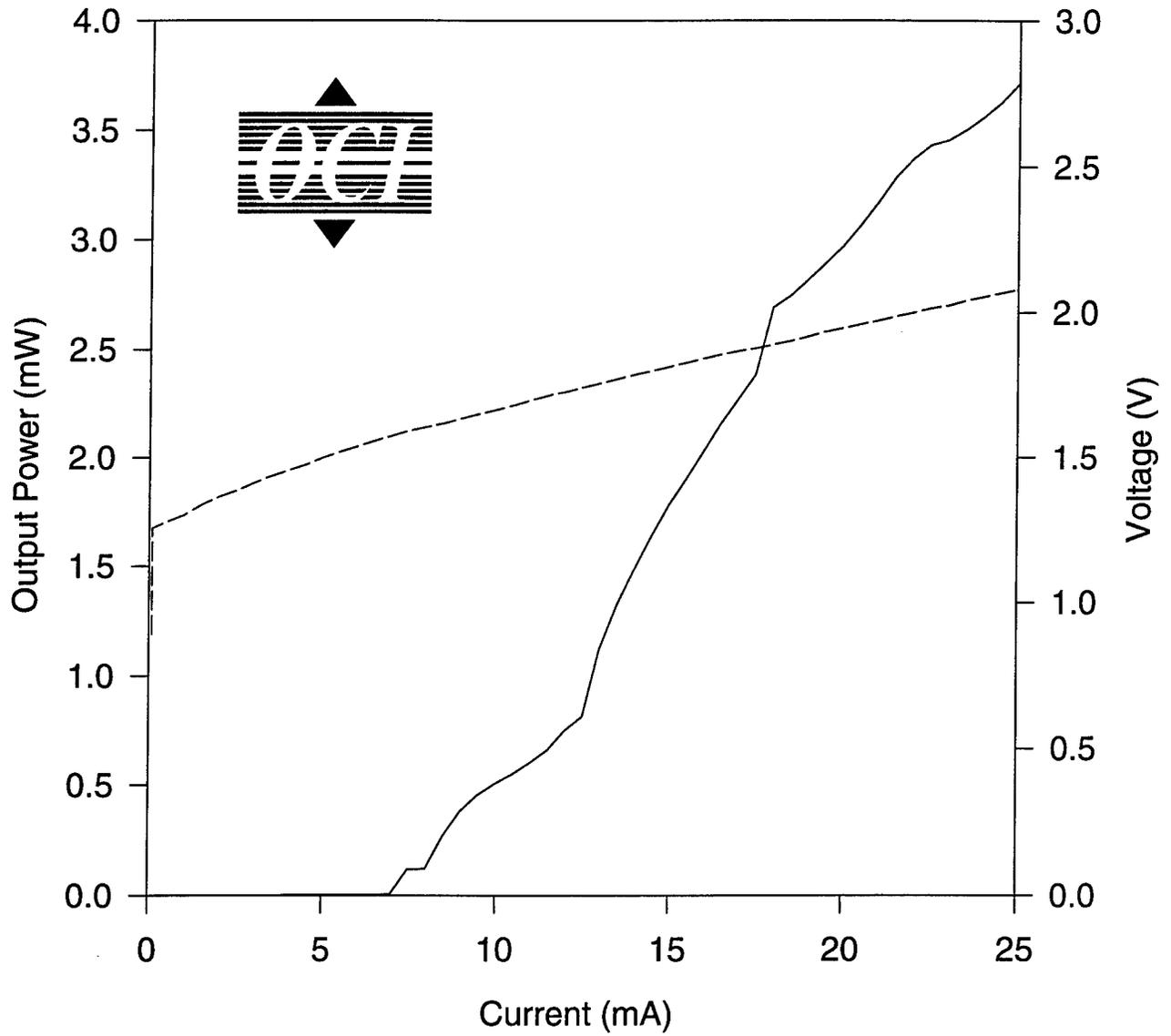
Figure 4.7f

Spectra from 25 µm diameter gain-guided VCSEL

Figure 4.7g

High Frequency Response

25 µm diameter gain-guided VCSEL
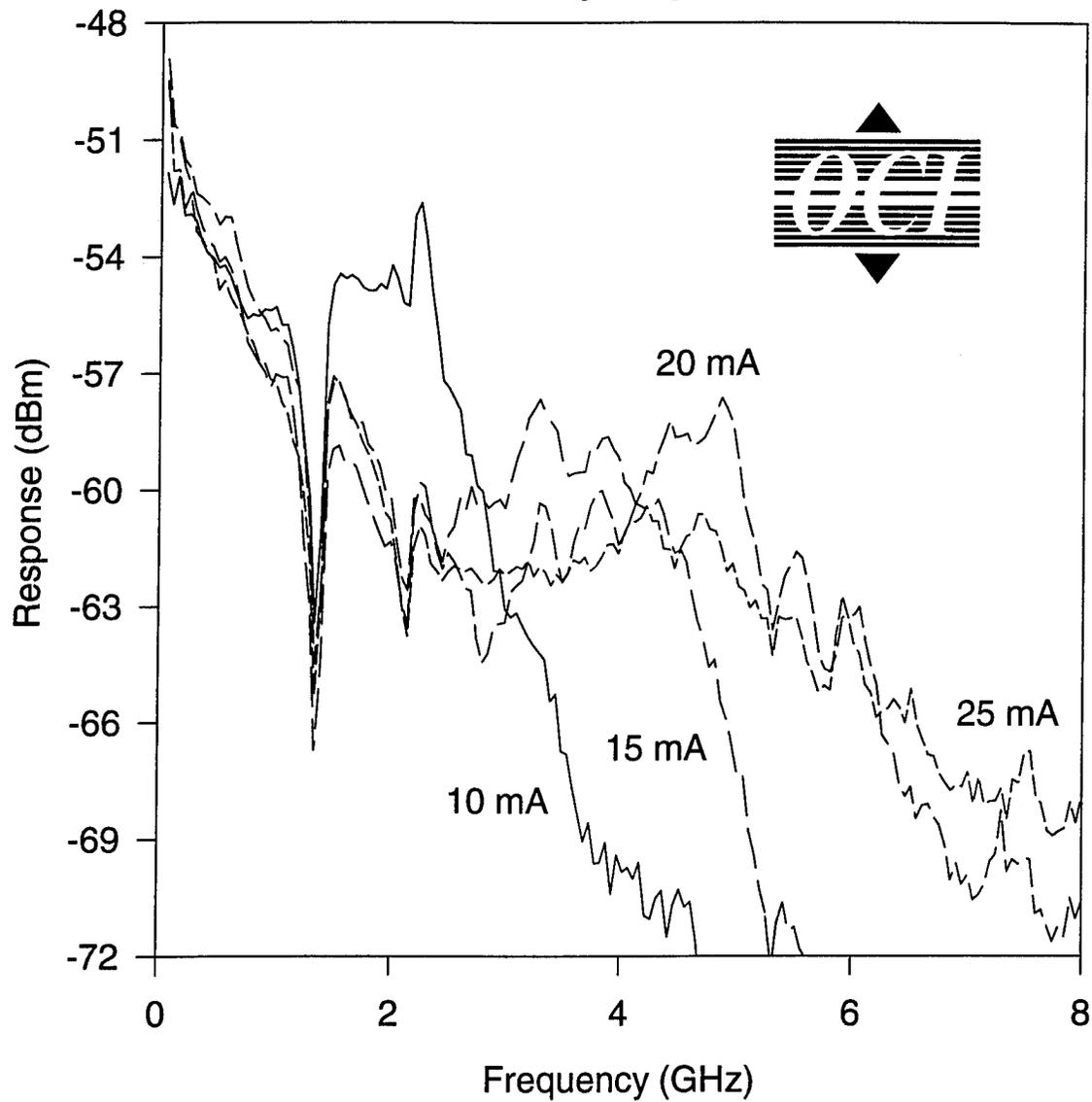
Figure 4.7h

the devices is evident from the broad spectra. Due to the large size of the devices, the frequency separation between lateral modes is much smaller than the resolution of the optical spectrum analyzer, and thus one only measures the envelope of the optical spectrum.

It was expected that the high-frequency response of the gain-guided devices would not be as good as the index-guided devices due to the large parasitic capacitance existing as part of the fabricati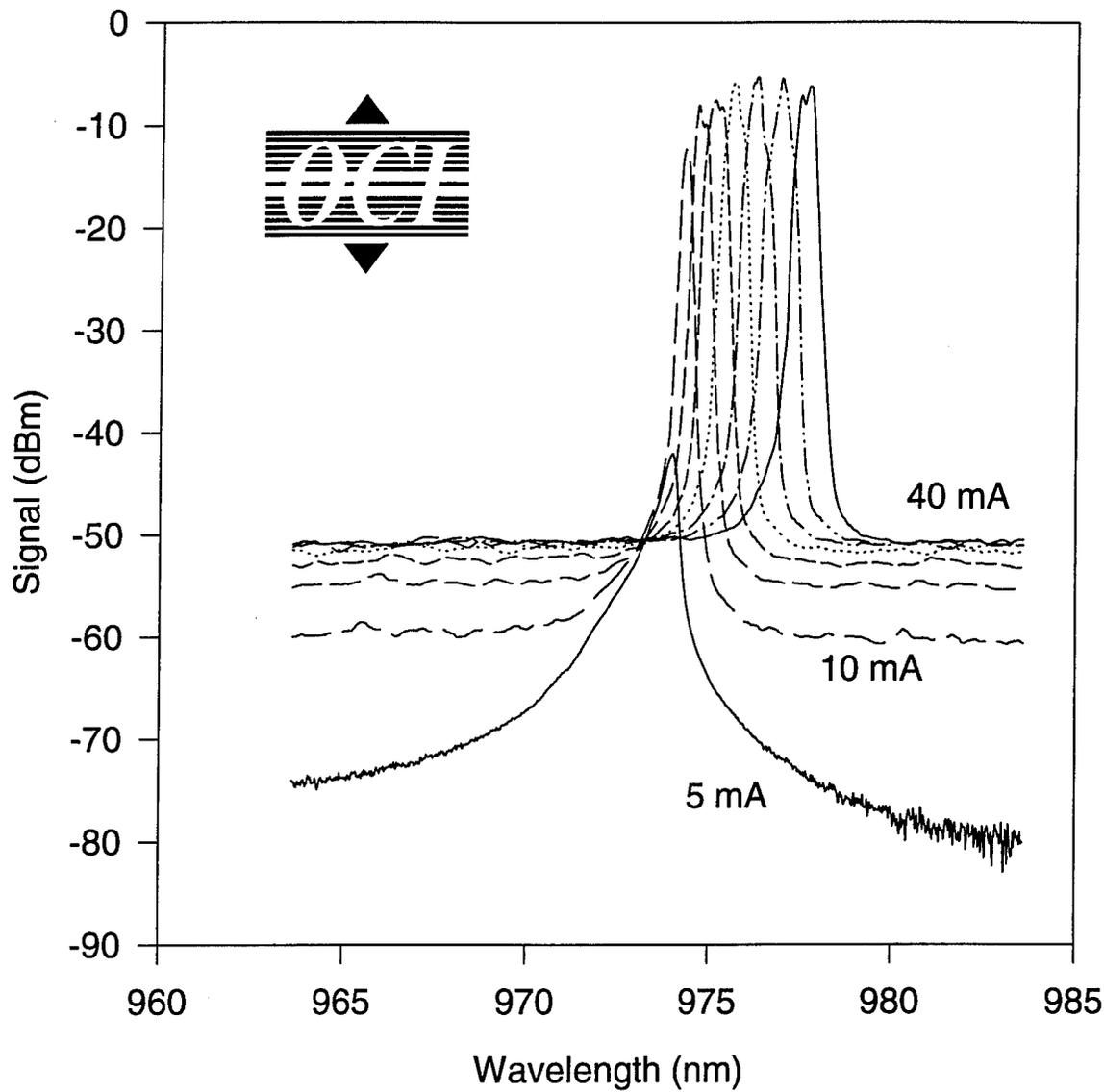on sequence (Sandia also fabricated device arrays using a method to eliminate the capacitance, so the problem is not a generic problem of gain-guided devices, but rather of the devices received). This can be seen in the microwave response of the Sandia devices shown in Figure 4.7h

4.7.3 Bottom Emitting Vertical Cavity Surface Emitting Lasers

We have packaged and pigtailed both small area and broad area etched-pillar bottom-emitting VCSELs. As with the gain-guided devices, the large area bottom emitting VCSELs operate multi-lateral mode as seen in Figure 4.7i. Even relatively small etched pillar devices operate in more than one lateral mode as can be seen from the spectra of a 10 μm diameter VCSEL as seen in Figure 4.7j. Using our present fabrication of etched pillar bottom emitting devices, only devices with diameters less than 8 μm operate in the fundamental mode over the entire operating range. For example, Figure 4.7k shows the spectral output of a 7 μm diameter VCSEL. Once lasing is established, the next highest lateral mode remains 30 dB below the fundamental mode.

The etched pillar devices operate at higher speeds than the gain-guided devices, primarily because the RC-limits of the devices are much higher than the gain-guided devices. Figures 4.7l and 4.7m show the microwave response of both multimode and single mode etched pillar bottom-emitting VCSELs. As with the intra-cavity contacted devices these devices operate much faster than necessary for the initial applications. The single mode bottom emitting devices operate as fast as can be expected considering the parasitic capacitance from the metallization and the solder bump. This is a positive sign for future applications since the solder bump can easily be reduced from 50 μm diameters to 10-20 μm diameter, greatly decreasing the

30 μm diameter bottom emitting VCSEL
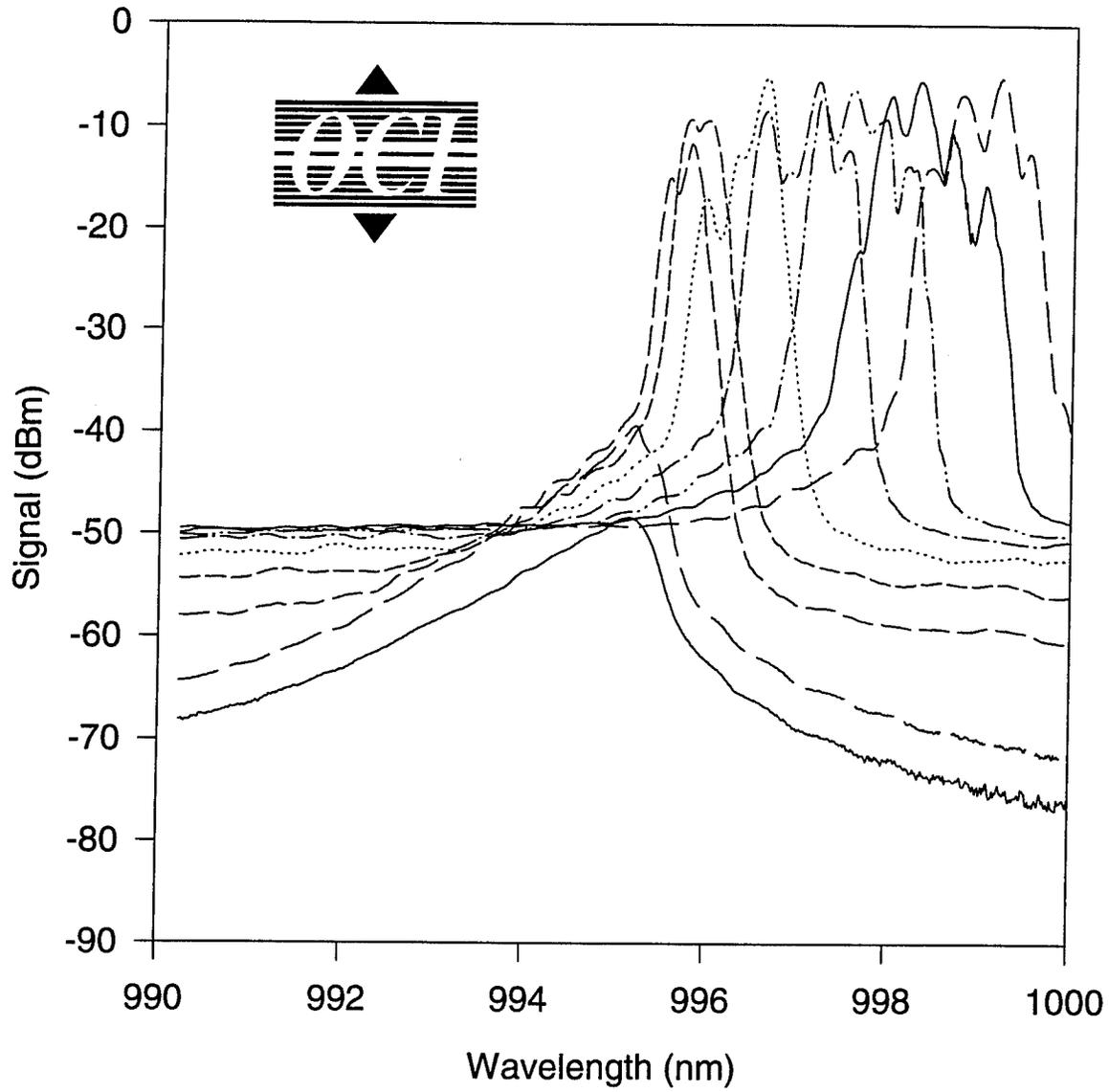
Figure 4.7i

10 μm diameter bottom emitting VCSEL

Figure 4.7j

7 µm diameter bottom emitting VCSEL

I = 1,3,5,7,9,11 mA
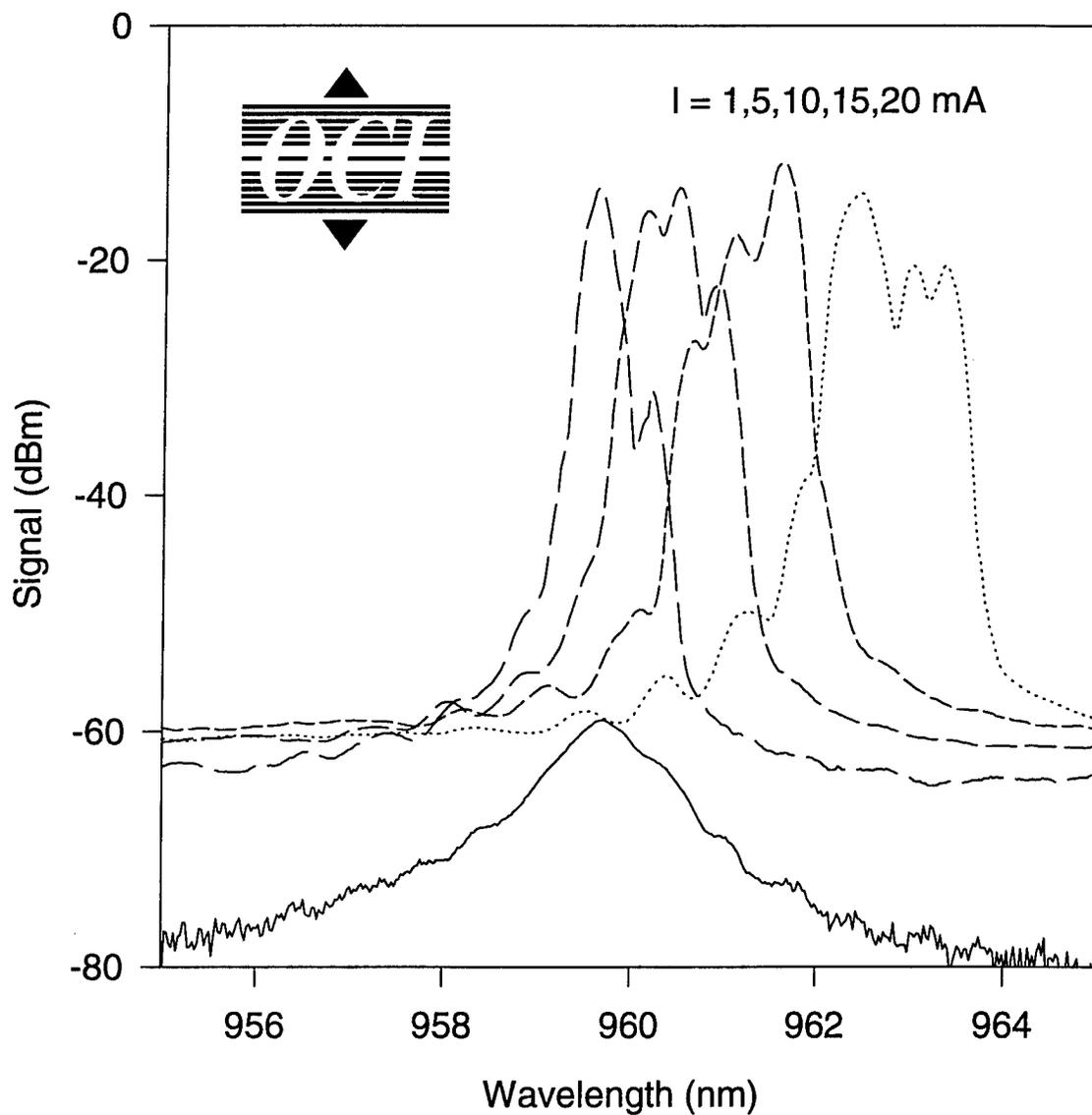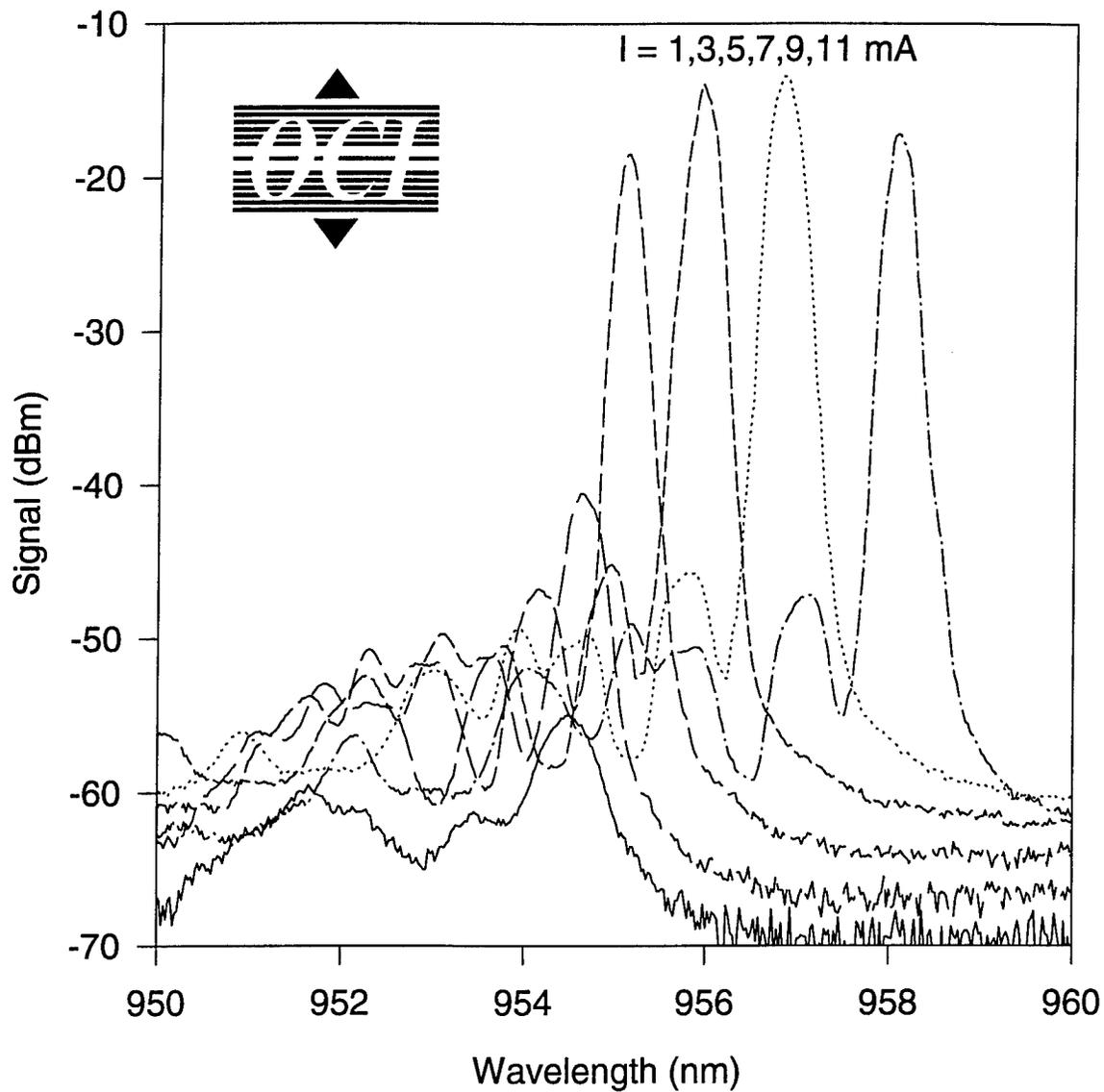
Figure 4.7k

Multi-Mode bottom emitting VCSEL

S$_{21}$ Microwave Response
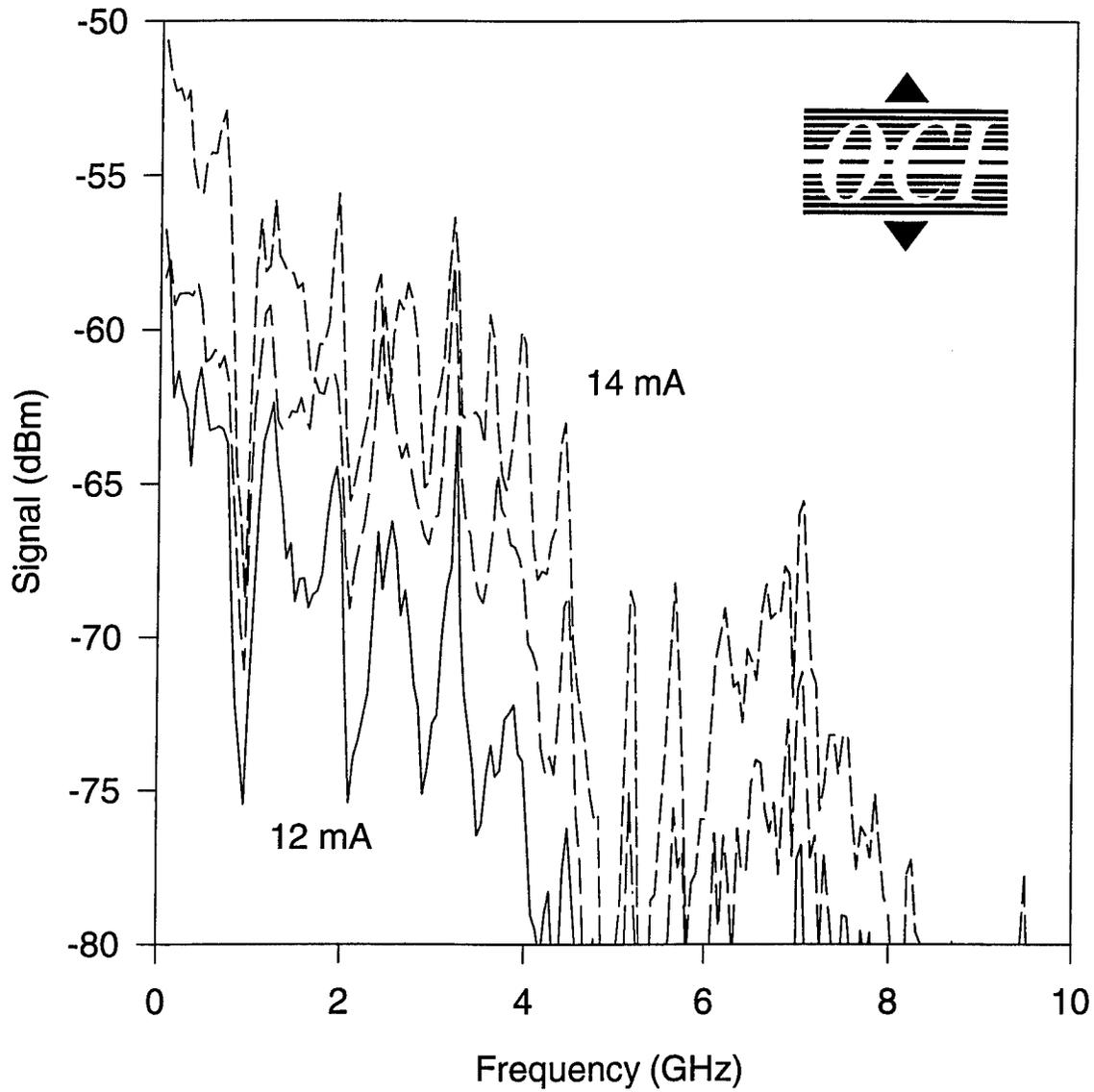
Figure 4.71

Single-Mode bottom emitting VCSEL

S$_{21}$ Microwave Response
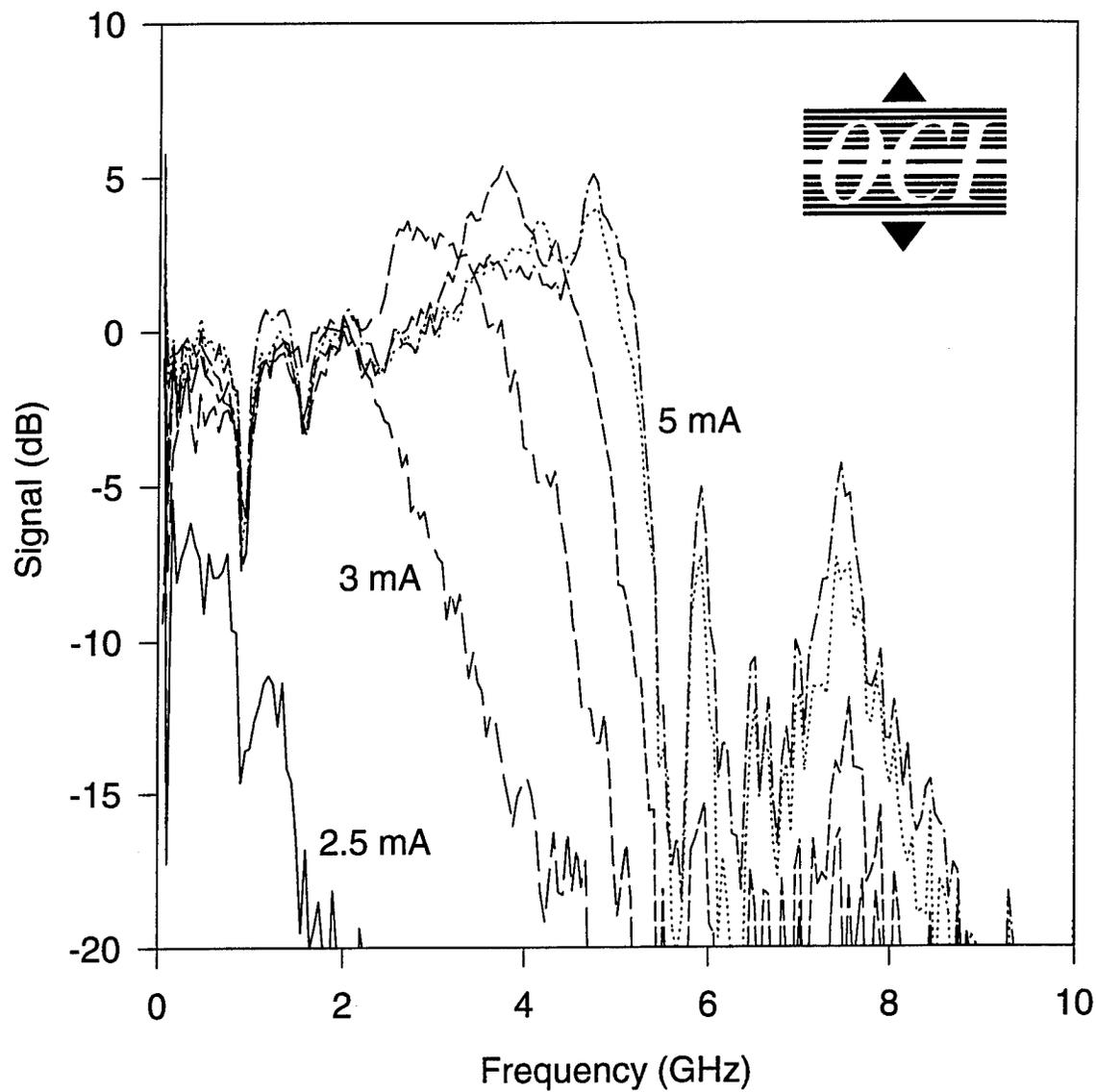
Figure 4.7m

capacitance of the contact pad. Also, by fabricating bottom emitting VCSELs from low voltage material as demonstrated by the Sandia devices, the low resistance of the device would also increase the RC-limit.

4.8 Manufacturability of VCSEL Links

Through this Phase II program we have investigated the technologies necessary in the manufacturing of high performance parallel data links using vertical cavity surface emitting lasers (VCSELs). During the two years, we have developed a number of new technologies to increase both the performance and yield of VCSELs. As a result of our investigation we feel confident that VCSEL array links can and should be inexpensively manufactured. The following subsections will describe the various manufacturing technologies in relation to VCSEL arrays link modules.

4.8.1 Fabrication

Two different VCSEL fabrication schemes were investigated during the Phase II investigation: top emitting intra-cavity contacted VCSELs and etched post bottom-emitting VCSELs.

4.8.1.1 Manufacturing Intra-Cavity Lasers

The processes used to fabricate the intra-cavity contacted lasers are mostly conventional GaAs procedures; the main differences are the mesa structure formation by Cl reactive ion etching and the current constriction etch. The fabrication sequence has been developed for repeatability and uniformity. As such, it could be transferred to a manufacturing environment with a high probability of success. It would be preferable, however, to modify the structure for easier fabrication. In particular, the use of a dielectric stack for the top reflector would simplify the fabrication considerably.

In its current form, both mirrors are grown epitaxially. A chlorine reactive ion etch done at low pressures, ~1 mtorr, is used to etch the top mirror to form the vertical waveguide. A combination

of nickel and sacrificial silicon masks are used to produce both the waveguide and the p mesa in a single etch step. This is shown in Figure 4.8a below. The e-beam evaporated silicon etches at a rate approximately 3.5 times slower than GaAs, so that a 0.3 μm thick silicon layer produces a 1 μm thick mesa. The nickel mask does not etch at all, leaving a vertical waveguide in the center of the p-mesa. The nickel is deposited on top of an organic material, PMGI, for removal after the etch. This process has been used for several years with consistent, repeatable results.

The next step is the undercut etch. The central waveguide is protected in photoresist and then a sequence of aluminum oxide removal followed by selective etching in an HCl solution forms the undercut as shown in Figure 4.8b. This procedure also has proven consistent, with an etch time of approximately 45 seconds for a 5 μm undercut. It remains, however, to measure the uniformity when scaled from 2 cm square samples to a full wafer. The initial results look promising and give no cause for concern.

The remaining process steps for ohmic and interconnect metal are similar to standard MESFET processes, other than that extra thick liftoff masks must be used due to the 3 μm tall mesa in the center of the laser. One could expect, then, that the device fabrication could be directly transferred to production. In addition, the semi-insulating substrate allows bond pads or solder bump pads to be placed in any configuration, well away from the device, avoiding potential reliability problems associated with packaging stresses.

With further process development, the device fabrication could be simplified by replacing the top semiconductor mirror with a dielectric stack. Quarter wave stacks of TiO_2/SiO_2 are commonly used in the optical coating field for reflectivities greater than 99%. This strain-compensated dielectric system can be deposited using ion beam assisted evaporation techniques at substrate temperatures below 200°C. Optical Concepts is currently working with an commercial source of optical thin films and has demonstrated mirror reflectivities of 99.6% using this system. The advantage of this approach is twofold. First, the device fabrication without the top mirror is simplified, making the fabrication sequence similar to a detector array while reducing epitaxial growth time. Second, the post fabrication opens the possibility of current apertured designs.
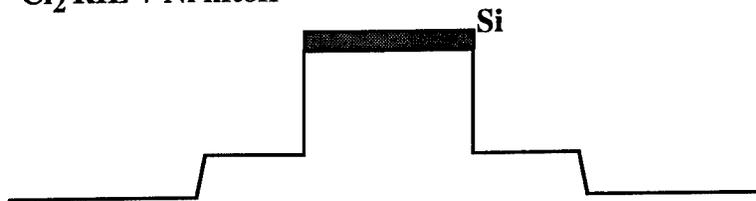
• Ni / PMGI / Si + O_2 RIE

Ni

PMGI

Si

• Cl_2 RIE + Ni liftoff

Si

Figure 4.8a

• **Photomask and Selective Etch**

Photoresist

undercut
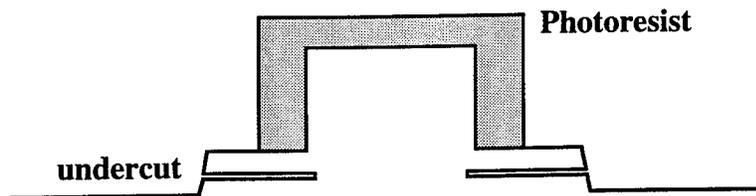
Figure 4.8b

In a current apertured design, the current constriction is formed using a current blocking layer which does not constrict the optical mode. Thus, current can be funneled into the center of the waveguide, optimizing the modal overlap and ensuring single mode operation. One potential approach is to replace the AlAs undercut with a n-type current block and then use ion implantation or diffusion to type convert the blocking layer in the center of the laser, producing a current funnel. The dielectric mirror with a larger diameter is deposited on top once the fabrication is complete. This improved design, patented by Optical Concepts (US Patent No. 5,343,487), promises higher output powers, sub-milliamp thresholds and single transverse mode operation. We intend to develop this design aggressively, yet too many uncertainties remain to be resolved to make production plans on this advanced design.

In summary, the prospects look very good to transfer the intra-cavity contacted laser process to a manufacturing environment. With the flexibility of having both contacts on the surface of a semi-insulating substrate, the lasers provide the largest number of options for packaging including top or bottom emission and wire bond or flip chip contacting.

4.8.1.2 Bottom Emitting Index-guided Devices

The simplicity of the bottom emitting etched post VCSEL immediately lends itself toward manufacturing. During the Phase II effort we have refined the fabrication of these devices to the point of achieving near 100% yields. Since it is the entire package that is ultimately important, this means that the good yield must be kept through the packaging sequence. Ensuring a high yield package adds additional complexity to the initially simple structures through the addition of anti-reflection coatings, plating, solder barriers and flip chip bonding. After more than a year of developing methods of packaging bottom emitting VCSELs, we have made some changes to our fabrication and are considering more changes for the future.

As mention in Section 4.4.1, proper metallization was a major issue in order for the VCSEL to be reliably soldered to a host substrate. The two initial problems were having proper adhesion of the metal to the insulator and providing a solder barrier. The solutions to the problems have been discussed previously. The final problem which is presently being solved is the purely mechanical

problem relating to the breaking of single mode devices during flip chip bonding. This is primarily a packaging issue and will be discussed at length in a later section, however there is a change in our fabrication that may eliminate or at least reduce the problem.

Based on recent work performed at UC Santa Barbara, we have begun to add a thick layer of plated-gold to the top of the VCSEL structure. There are two potential benefits of this procedure. First, the plated-gold is a better thermal conductor than the soft indium solder, and therefore the thick gold provides a better thermal path than the solder, for the heat generated in the top mirror and active region. Secondly, the plated-gold tends to be somewhat porous, and this provides a certain amount of strain relief during the bonding procedure. As a result we are adding this final procedure to our fabrication.

4.8.2 Packaging Technologies

The packaging issues are normally very different for top emitting and bottom emitting devices. This does however depend on the final package design. Using our current designs the top emissions structures only require the use of epoxy plus wire bonds, whereas the bottom emitting devices require flip chip bonding.

Wire bonding of devices is very straight forward and causes no significant yield problem. This procedure can easily be fully automated, although it requires very high volumes to justify the high cost of the necessary automated equipment. The use of thermal epoxy to make contact to the back of a top emitting VCSEL is very simple with no foreseeable yield problems, and the use of the transparent epoxy for fiber coupling has caused no difficulties for the number of pigtailed packages we have made. The only packaging technology we feel requires more of an effort to achieve acceptable yields is flip chip bonding.

4.8.2.1 Flip-Chip Bonding

During this investigation we have been somewhat handicapped in our development of a good flip chip technology. The dedicated equipment designed for this purpose costs upwards of one hundred thousand dollars, and as a result we will not have access to this type of equipment until

after the end of the contract. This means that many of our perceived problems in flip chip bonding may simply be a result of the lack of the proper tools. In any event our research into this manufacturing technology has been profitable from the perspective of an additional safety factor, i.e. if we can develop a reliable process using the equipment at hand, this should translate into a more reliable process once the correct equipment is available.

So far, we have made two approaches toward flip chip bonding. The first was the painstaking approach of using probes to push a chip around a host substrate until the two were aligned and then providing heat to reflow the solder. Although this approach worked, it also took hours per package and required a host substrate that was transparent to IR light.

The second approach used a IR mask aligner for initial alignment. Using this approach, pressure was applied between VCSEL array and host substrate. There are a number of difficulties with this approach. The most significant difficulty was that the device array and host substrate could not be made parallel, and this resulted in devices at one end of the array being broken and devices at the other end operating. This was the case for all but the largest bottom emitting devices that are less easily broken due to their size. Equally problematic was the fact that no heat could be applied at the IR mask aligner, so the flip chip arrays were extremely fragile until additional material was applied for mechanical strength. If heat could be applied, the procedure may well have been more successful since it would then have been possible to release the vacuum before pressure was applied to the device array. Then, the reflow of the solder would have completed the alignment procedure.

As a result of our investigations, flip chip bonding has become our only remaining critical packaging issue to be solved before high yield bottom emitting VCSEL array packages can be completed.

4.8.3 Other Reliability Issues

Many of the materials utilized in our fabrication (such as PMGI) and our packaging (such as the epoxies and solders) may be potential problems for long term reliability. We are therefore

proceeding to initiate long term life testing of our device arrays. This long-term testing will ultimately decide the most desirable fabrication and packaging methods.

5. Conclusions

The goal of this program has been to develop vertical-cavity surface-emitting lasers (VCSELs) and complementary technologies for the formation of high-speed parallel data links. To this end the program has been highly successful. Sub-milliamp threshold laser arrays have been incorporated into a high-speed fiber-coupled parallel transmitter. Gigabit data rates have been demonstrated using these devices. Perhaps most importantly, we are currently entering into a privately funded Phase III program.

At the beginning of this contract VCSELs were primarily novelties of research and educational institutes. During the course of the Phase II investigation we have played an active role in developing VCSEL technology, developing close working relationships with some of the leading research institutions in the field. In particular, joint programs with University of California Santa Barbara and Sandia National Laboratories have enabled Optical Concepts to stay involved with some of the most important technological advantages. At both institutions, Optical Concepts has been a key participant in the development of comprehensive device models and has provided addition commercial focus to the research programs.

During the Phase II investigations the laser characteristics have changed dramatically. Our program with UC Santa Barbara has resulted in very low-threshold, high-frequency index-guided VCSELs, while the group at Sandia has reduced the drive voltage from the 6-8 Volt range to below 2 Volts, dramatically improving the power conversion efficiency and maximum output power. Combined with the geometrical advantages of low beam divergence and array configurations, these changes in device characteristics provide a number of significant advantages of existing laser communications systems. Because the present generation of VCSELs operate at low input power levels, they are well suited to parallel data links where thermal management is an important issue. Furthermore, the lasers demonstrated in this program

operate at Gigabit data rates at current levels of only a few milliamps with negligible turn on delays. Low bias currents and on/off modulation opens the possibility of simplified, low power driver and receiver circuitry. The high frequency measurements presented in this report are the first which show good agreement between the theory and high frequency experimental data for varying device diameters. Additionally, we have developed design tools which enable accurate prediction of laser properties such as threshold current, external efficiency and modulation efficiency.

Recognizing that it is important to transfer the technology from the research to the manufacturing environment, we have endeavored to develop reliable VCSELs that can be manufactured on a wafer scale and packaged for as low a cost as possible. This desire promoted an extended development of appropriate fabrication techniques and contact metallization. The intra-cavity contacted devices allow the use of standard alloyed contacts and wire bonds on the top surface without compromising the lasers' optical properties or high frequency performance. Alloyed ring contacts have been developed which provide good electrical and optical properties for the bottom emission lasers.

Prototype packages appropriate for high speed VCSEL data links have also been developed. We have demonstrated packaging schemes for both top and bottom emitting VCSELs. The top emitting lasers were wire bond contacted and permanently butt coupled to fibers. The bottom emitting lasers were flip-chip bonded for electrical contact. This technology includes the development of appropriate solder barriers and infra-red alignment techniques. To ease the fiber coupling tolerances, procedures for fabricating integrated microlenses on the backside of the semiconductor substrate have been developed. Packaged fiber coupled arrays of the index-guided lasers, both top and bottom emission, have been demonstrated with bandwidths greater than 5 GHz at drive currents of only a few milliamps. These VCSEL transmitters show great promise as an important product in the short-haul data communications market.

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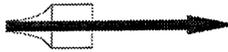
APPENDIX A

IC DESIGN

FOR:

LASER DRIVERS

RECEIVER AMPLIFIERS

COMPUTER / NETWORK INTERFACE