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January 16, 1995

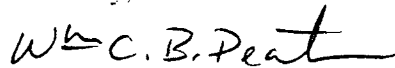
Dr. Alvin M. Goodman
Program Officer, Code 312
Office of Naval Research
800 North Quincy Street
Arlington, VA 22217-5000
TEL: (703) 696-4845

Dear Dr. Goodman:

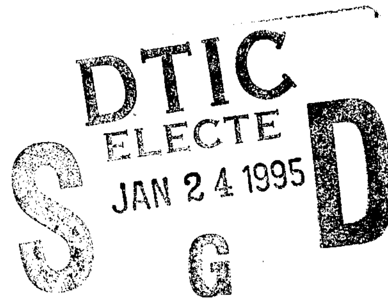
Please find enclosed Progress Report #3 entitled "Novel Field Effect Transistors for Low Power Electronics" summarizing the status of our research under ONR STTR Contract #N00014-94-C-0260. Also enclosed is invoice #SA3-11695. If you should have any questions regarding either the report or the invoice, please don't hesitate to call me at the number above.

Thank you for your interest and support of Advanced Device Technologies, Inc.

Sincerely,



William C.B. Peatman
President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Novel Field Effect Transistors for Low Power Electronics

Progress Report # 3

NAVY STTR Phase I
Contract Number: N00014-94-C-0260

January 16, 1995

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Novel Field Effect Transistors for Low Power Electronics
(ONR STTR Contract N00014-94-C-0260)

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I. Phase I Technical Objectives

The primary objective of this Phase I project is to determine the extent of the significant reduction in power consumption of integrated circuits which may be achieved by utilizing a novel sidegate FET technology. The new FET technology promises to eliminate the Narrow Channel Effect (NCE) which is one of the primary factors limiting the minimum power consumption of integrated circuits. By eliminating the NCE, we will be able to scale the device size dramatically and reduce the power consumption by an order of magnitude. The project will assess the power, speed, circuit design, processing, and manufacturability of the new FET technology for both digital and analog circuit applications. In particular, we will extract device parameters from the new ultra-low power FETs fabricated at UVa, develop device models, incorporate these models into a new SPICE package (AIM-Spice), simulate different logic families including DCFL and SCFL, and compare the predicted performance with the standard DCFL and SCFL logic. We will also analyze the gate current leakage and subthreshold slope as the primary factors limiting the noise margins at low power supplies, establish the minimum required bias voltage for reliable operation, and analyze the factors determining the threshold voltage changes from device to device as well as other factors which may limit the yield and integration scale.

II. Phase I Progress Report #3

As detailed in the Phase I proposal, the project has five major tasks. These are 1) 2-D MESFET (discrete) device fabrication, 2) detailed device evaluation and optimization for next iteration of device design and fabrication, 3) parameter extraction using AIM-SPICE to generate and refine AIM-SPICE 2-D MESFET models, 4) 2-D MESFET DCFL and SCFL logic circuit simulations using AIM-SPICE and comparison with conventional circuits, and 5) analysis of manufacturability and technology insertion issues. This report summarizes the progress in each task area since the second Progress Report of 11/28/94.

Task 1: Device Fabrication

In the last report, we reported devices having record unit width transconductance for a 1 micron wide FET (295 mS/mm at room temperature). Since that time, the device fabrication has been focussed on developing a new gate level dry etch process using the Cl-RIE at UVA. This work has been successful and a sample batch of devices (not electrically active) were fabricated to demonstrate the new capability. A scanning electron micrograph of the device, given in Fig. 1, shows the excellent gate definition (after etch and plate) and alignment between ohmic and gate levels. The channel dimensions (the 2-d electron gas region between the two opposing gate contacts) are nominally 0.5 x 0.5 micron ($W_0 \times L_g$) while the source/drain spacing L_{DS} is 2.7 micron. This represents a significant improvement in device scaling, compared with previous devices, and such scaling will be important for achieving higher performance (high speed, lower power) devices.

There are several batches of 2-D MESFETs in progress which will be completed by the end of this Phase I contract. These devices will provide additional data for parameter extraction and device modeling. In addition, a new maskset was designed which will permit fabrication of both discrete devices (for noise measurements), single-stage inverters and 3-stage inverter chains. The inverter devices will greatly facilitate the parameter extraction and comparison with the AIMSPICE circuit simulation.

Task 2: Evaluation, Optimization, Design

Additional evaluation of the devices reported last time included the measurement of the series resistance and estimate of the intrinsic transconductance. To estimate the source and drain series resistances R_s and R_d for the 1 micron wide device, we measured the drain current of 1 µm (27.9 µA) and 3 µm (15.3 µA) channel length devices at $V_{DS} = 0.05$ for $V_{GS} = 0.5$ V (i.e. in the linear region with nearly fully conducting channel). Assuming ohmic behavior so that $R_s + R_d = V_{DS}/I_D$, we extrapolated the measured resistances to zero channel length and obtained $R_s + R_d = 1050\ \Omega$. Due to the source/drain symmetry, we obtain $R_s = 525\ \Omega$ which agrees well with the calculated spreading resistance assuming the2-d gas conductivity and the geometry of the device shown in Fig. 1. The *intrinsic* transconductance , G_m' is larger than the extrinsic G_m measured earlier (295 mS/mm) by the factor $(1 - G_m(R_s + R_d))^{-1}$ so we estimate the peak G_m'

value to be 427 μS (427 mS/mm) which is, to our knowledge, the highest unit-width transconductances (both extrinsic and intrinsic) yet reported for FETs of these channel widths. These results offer further evidence that the narrow channel effect, which is a serious limitation to the minimum power consumption in conventional FETs, is practically eliminated in this device.

Task 3: 2-D MESFET AIM-SPICE Modeling

Last time, the 2-D MESFET inverter transfer characteristic was presented showing the excellent agreement between measured data and the universal HFET model of AIMSPICE. Since that time, we have developed an accurate capacitance model based on extracted I_D - V_g data of the 0.5 micron wide device used in the inverter measurements. Fig. 2 shows the fit between the data and the model over several decades in the capacitance. The new capacitance model was implemented into AIMSPICE and will continue to be improved as new data is obtained.

Task 4: 2-D MESFET DCFL and SCFL Circuit Simulation

The I-V and C-V AIMSPICE models were used in the transient response simulation of a 3-stage 2-D MESFET ring oscillator which is shown in Fig. 3. The simulation was performed using the parameters of the 0.5 micron device of the inverter transfer characterization reported last time. The total delay was 52 ps (17 ps/stage) at V_{DD}= 0.8V and 48 ps (16 ps/stage) at V_{DD}= 1.6V. The delay and power per gate were calculated using the equations

$$t_d = \frac{1}{2Nf} \quad (1)$$

and

$$P_d = \frac{V_{dd} I_d}{N} \quad (2)$$

The results include a delay of 8.7 ps and power of 9.25 uW per gate at V_{DD}= 0.8V or a power-delay product of less than 0.1 fJ. This result represents a very substantial reduction in the power-delay product compared to the state-of-the-art. The main reason for such a reduction in the power-delay product are the elimination of the narrow channel effect (thereby allowing much narrower, lower current devices) and the use of the heterodimensional 3-d/2-d Schottky contact which has lower capacitance than the equivalent parallel plate device.

Task 5: Manufacturability and Technology Insertion Issues

A comprehensive technology analysis of 2-D MESFET circuits will be performed toward the end of Phase I project. It will serve to summarize the main advantages of the 2-D MESFET over existing technologies and to address any potential barriers to insertion of the 2-D MESFET technology into the large scale IC manufacturing environment.

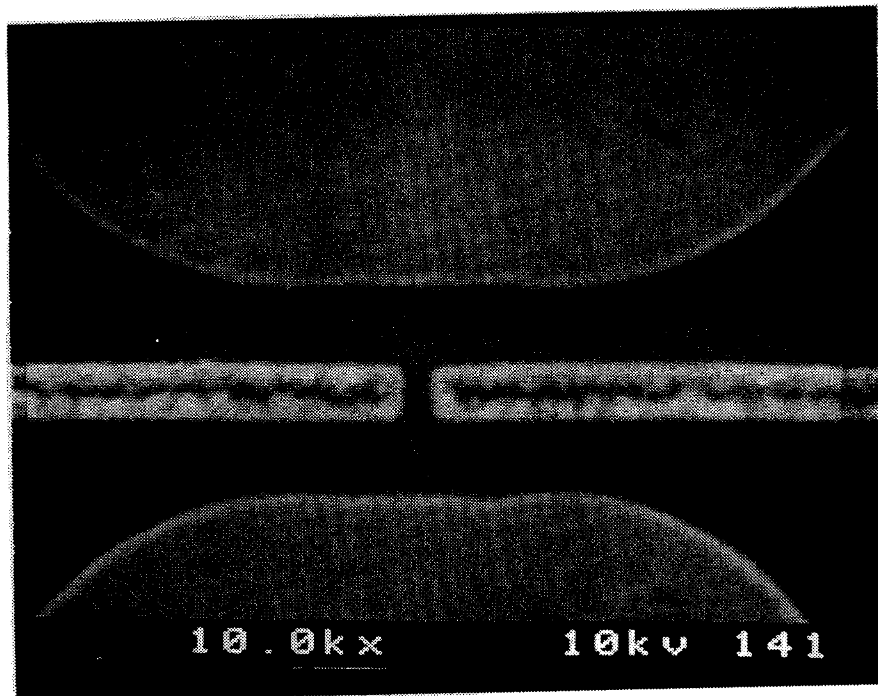

Fig. 1.Scanning electron micrograph of a nominally 0.5 micron by 0.5 micron channel 2-D MESFET.

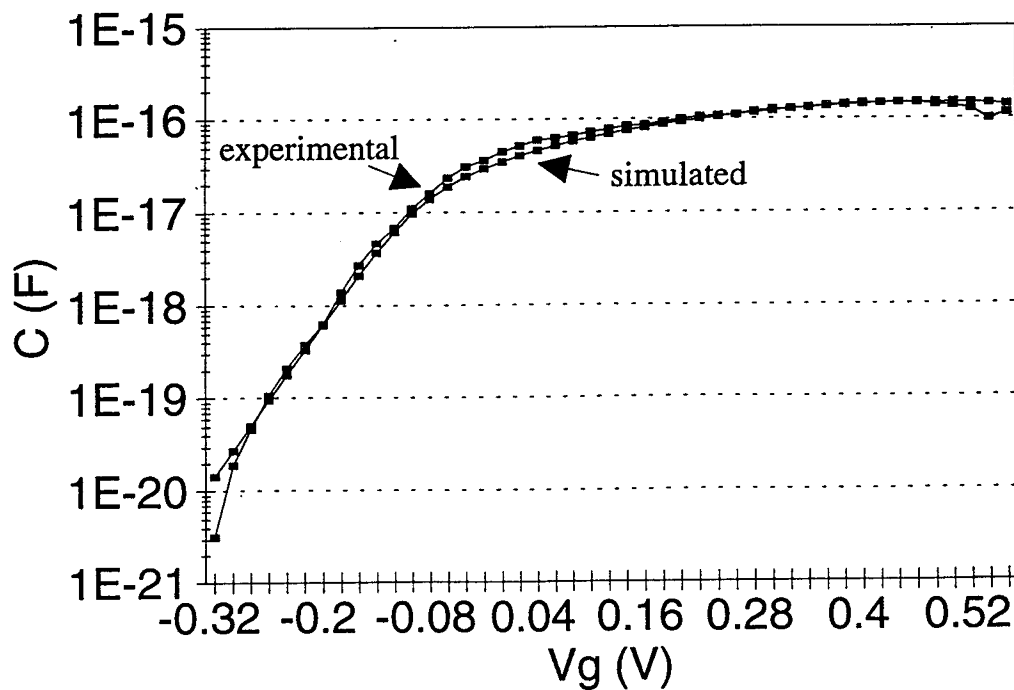

Fig. 2 Simulated capacitance-voltage characteristic of 0.5 micron 2-D MESFET.

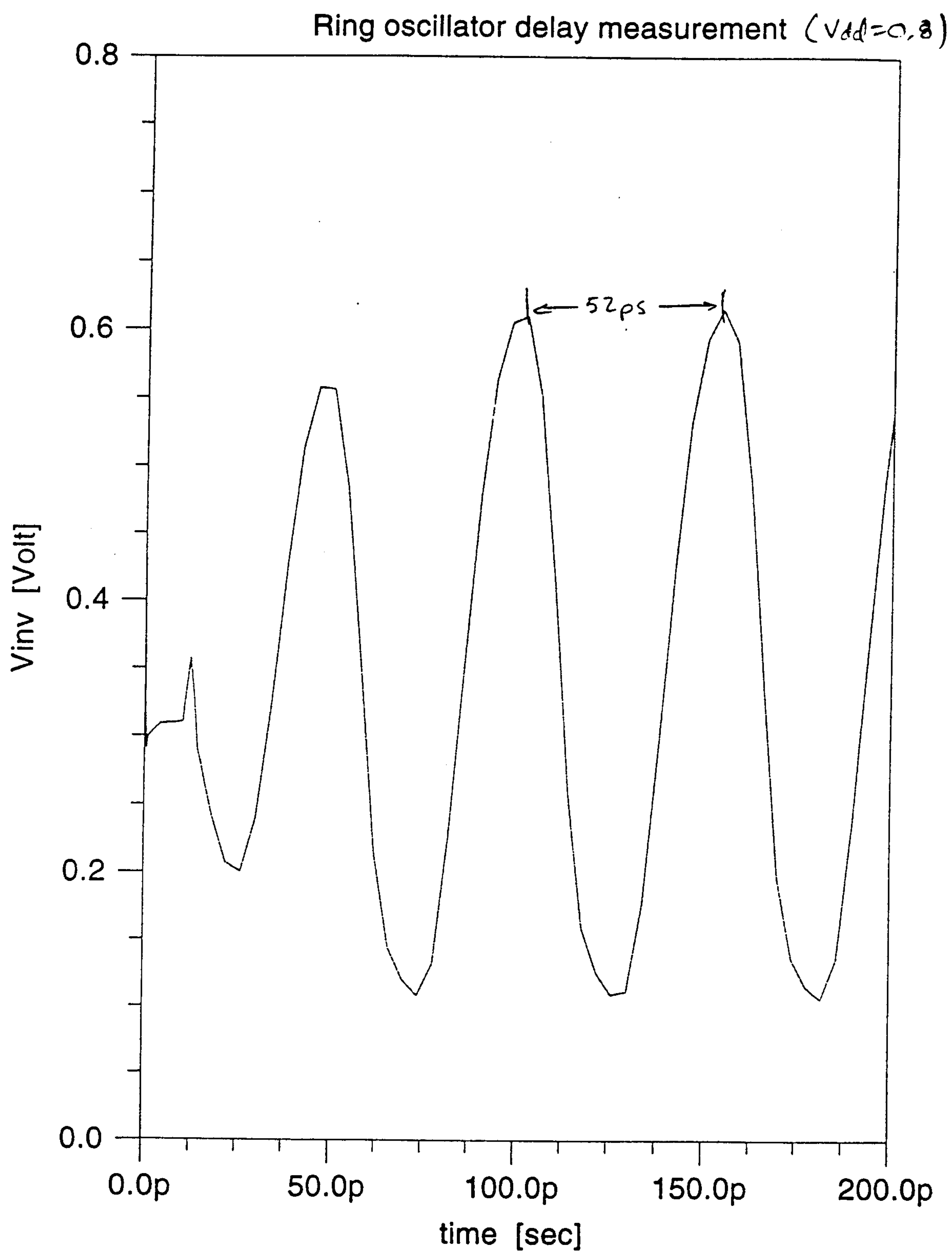

Fig. 3. AIMSPICE transient response of a 3-stage 2-D MESFET ring oscillator.

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