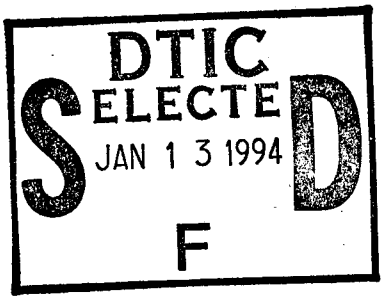
FINAL REPORT

SBIR PHASE II

"ELECTRONICALLY STEERABLE AGILE BEAM ANTENNA"

Contract DAAE07-87-C-R102

USA TANK AND AUTOMOTIVE COMMAND



October 30, 1989

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13. ABSTRACT *(Maximum 200 words)*

The Electronically Steerable Agile Beam Antenna (ESABA) was developed under Phase I/II of the Small Business Innovative Research (SBIR) Program. The goal of the project is to develop a rugged antenna that transmits real-time analog video from an unmanned robotic vehicle (RV) to a manned command center (CC). The ESABA uses a Very High Frequency (VHF) phased array to determine the direction of the incoming VHF command link from the CC. The ESABA then electronically switches the radio frequency (RF) microwave signal carrying the video from the video transmitter to one of eight circular-polarized, helical antennas. The advantages of the ESABA approach over a conventional mechanical system are: 1) better reliability because there are no moving parts; 2) better link margin because of circular-polarized, helical design; and 3) better performance because reacquisition of the direction to the CC can be done electronically in milliseconds.

14. SUBJECT TERMS

Antenna; Microwave; very high frequency (VHF);
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I. INTRODUCTION

I.A. BACKGROUND

The Army Tank and Automotive Command (TACOM) is developing robot vehicles for reconnaissance into hazardous areas. The vehicle is controlled remotely by an operator who can see the terrain in which the vehicle is operating as well as hear engine noises to help in the control of the robot. The operating terrain is monitored by several video cameras, some of which are specialized. The video and other data are transmitted from the vehicle (RCV) to the base station (RCC) by four channels in the frequency band of 1700 to 2500 MHz. This link is called the microwave link. Data used to control the vehicle are transmitted from the base station (RCC) to the vehicle on a VHF link at 225 to 235 MHz.

Early AGVT robots used a mechanically pointed horn type microwave antenna to relay the video and other data to the base station. The antenna had to be pointed both in azimuth and elevation towards the base station. It used a signal from the RCC to track the base as the vehicle maneuvered. The mechanical system was cumbersome and had no potential to use reflected signal propagation if the line of sight path was lost. TRA proposed to TACOM that an electrically steerable agile beam antenna (ESABA) could be constructed that would have no movable mechanical parts and would have the potential for reflected signal linking. Further, since the antenna would be controlled electronically, tracking the base station would occur very fast, allowing for rapid vehicle turns and rapid signal reacquisition.

TRA was awarded a SBIR Phase I contract to prove the feasibility of the idea. The details of this work are included as Appendix X.E. Briefly, a four antenna azimuthal array operating at 440 MHz was built. A dedicated computer controlled a PIN switch which caused the array to electronically sweep in a circular azimuthal pattern. When a radio signal was heard, the computer would determine in which quadrant the signal was strongest and route radio communication to that sector. Upon completion of the communication, the scanning would resume until the next signal was heard. The prototype antenna worked well and was tested in one of the local canyons. The antenna could switch from a direct down canyon path to a stronger reflected signal if the direct path was weaker due to intervening obstructions. Because of the success of the Phase I feasibility study and hardware TRA was awarded a Phase II contract to develop two prototype ESABA antenna systems. This work started in late August 1987, was delayed for four months due to federal budget delays, and was completed at the end of October 1989 ahead of schedule considering the four month delay.

I.B. PURPOSE OF ESABA AND ADVANTAGES

The purpose of the ESABA is to provide TACOM with a more effective steerable microwave antenna for the robot vehicle (RCV). The ESABA has several advantages:

1. The ESABA is a completely electronic antenna and has no moving parts to wear out, break, or jam.

2. The ESABA antenna system is designed to have an equal or better gain than the mechanical horn antenna that it replaces. Thus it will provide a better link margin.

3. If for some reason the base station (RCC) "beacon" signal is lost, for example the vehicle goes behind an obstruction, reacquisition of the video signals by the RCC will be much faster because the robot, with its rapid electronic scanning in azimuth, will be able to find the RCC in milliseconds.

4. The ESABA allows for the use of reflected signals as the communication link when the direct line of sight signal is lost as the RCV passes behind an obstruction, since the ESABA directs the microwave link at the strongest RCC signal.

I.C. SYSTEM BLOCK DIAGRAM

Figure 1 shows the ESABA system block diagram. Four end fed half wave length dipole whip type antennas form a phased array. This array of four antennas can be configured by switching and phasing into eight different directional antennas. Each of these antennas covers a separate 45 degree sector in azimuth. Only one of the eight antennas is active at any one time but all eight are formed at up to 2500 times per second, depending upon the signal strength response time (see Section V.B.1). This scanning allows the RCV ESABA computer to determine in which of the eight sectors the RCC is and thus in which sector to direct the video.

The switching and phasing board electronically creates the eight different VHF array antennas which are used in a direction finding mode. The switching and phasing board is controlled by the ESABA system computer. Received RF is passed through to the VHF ESABA dedicated receiver (IMSCO Model ADX-MR).

The VHF receiver listens to the RCV control signals sent by the RCC. Signal strength information is sent from the receiver to a signal strength converter on the CPU board.

The signal strength converter provides level shifting, gain adjustment and filtering. This processed signal is then converted into digital information by an A/D converter and accessed by the

ESABA dedicated computer.

The ESABA computer controls the configuration of the eight VHF antennas and compares the strength of the received RCC signal in each of the eight sectors. This sector/signal strength information is used to control a single pole eight throw microwave PIN switch. The PIN switch thus routes the video data to one of eight helical microwave antennas that is pointing to the RCC at that moment.

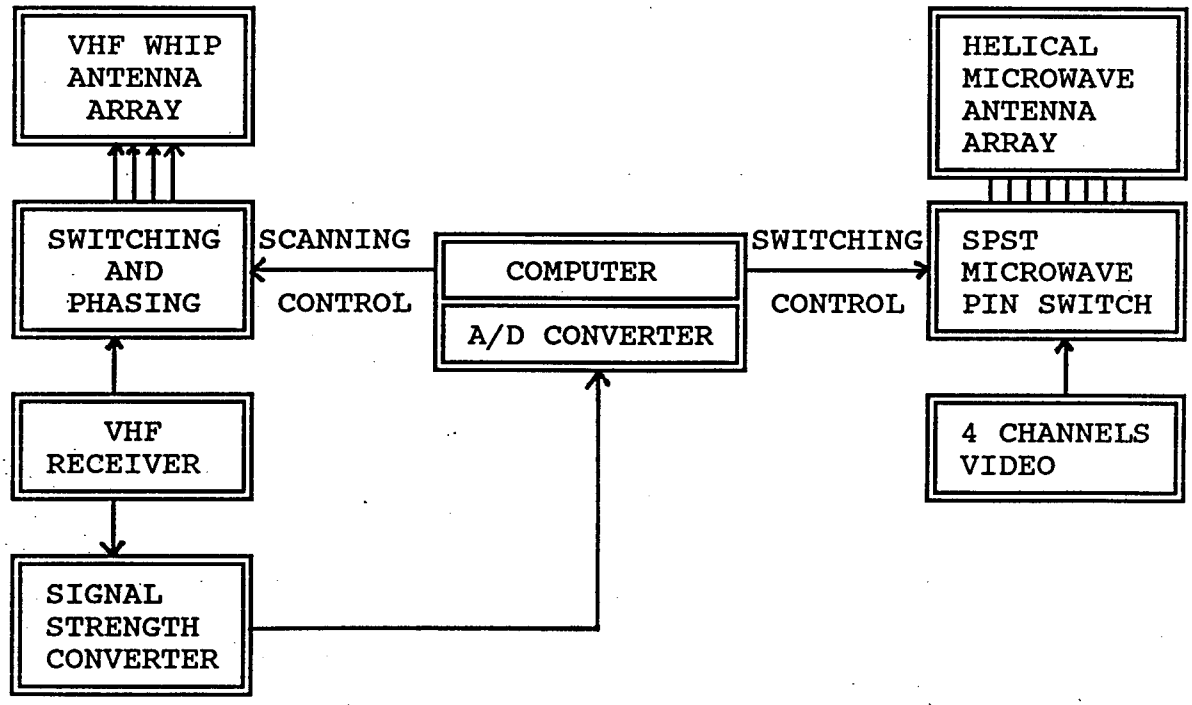


FIGURE 1
SYSTEM BLOCK DIAGRAM

II. VHF LINK

II.A. OVERVIEW

II.A.1. PURPOSE OF VHF LINK

The purpose of the VHF link is to allow the ESABA system to find the direction of the RCC from the RCV. Since the RCV is continually moving through the terrain this information is constantly changing especially during RCV turns.

II.A.2. THEORY OF THE PHASED ARRAY

A single vertical antenna radiates a radio wave equally well in all azimuthal directions. Two vertical antennas can be spaced at various distances and fed in various phase relationships to produce azimuthal radiation patterns that vary in strength. In Figure 2a we see that if two antennas are located in the same place (0 degrees separation) and fed in phase their radiated waves superpose and produce a wave that has twice the amplitude of either single wave.

Figure 2b shows the case of separating the two antennas by 1/4 wavelength (90 degrees of phase) and feeding them in phase. In the direction of interest one gets a signal that is somewhat greater in amplitude than the individual signals due to superposition. This superposed signal is lower in amplitude than the superposed signal shown in Figure 2a.

Figure 2c shows antennas A1 and A2 separated by 1/4 wavelength but this time fed minus 90 degrees out of phase. Note that the individual waves superpose to provide twice the signal in the direction of interest.

In Figure 2d the antennas are still separated by 1/4 wavelength but we have reversed the phase of the feeding signals to plus 90 degrees. Note that the superposed signals completely cancel. Here one is "looking" at the same array as in 2c but from the back of the array where the array is fed as in 2c,that is antenna 1 is fed at 0 phase and antenna 2 is fed at minus 90 degrees phase.

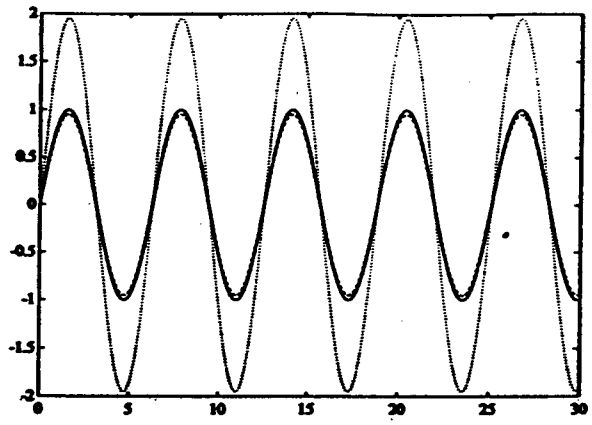


FIGURE 2A

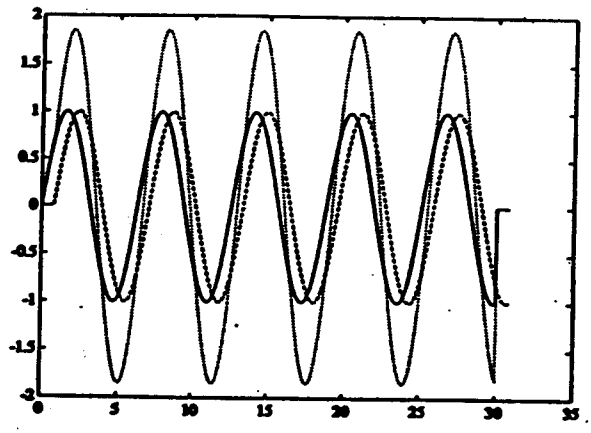


FIGURE 2B

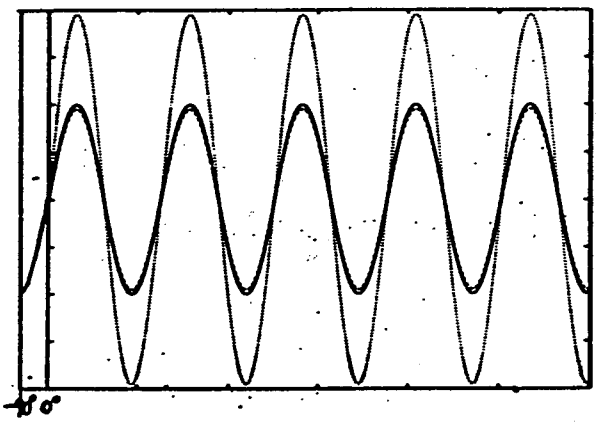


FIGURE 2C

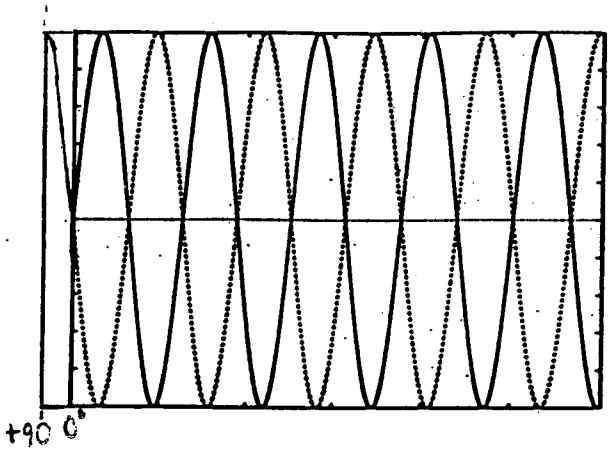


FIGURE 2D

FIGURE 2
TWO ELEMENT RADIATION PATTERNS

Figure 3 shows the azimuthal radiation pattern from the two antennas separated by 1/4 wavelength with A1 fed at 0 degrees phase and A2 fed at minus 90 degrees. A strong 2X (3 dB) signal is radiated in the 0 degree direction and no signal is radiated in the back, 180 degree direction. A similar but even stronger forward radiation pattern can be formed by spacing three antennas in a straight line each spaced at 1/4 wavelength and fed at 0 degrees, -90 degrees and -180 degrees.

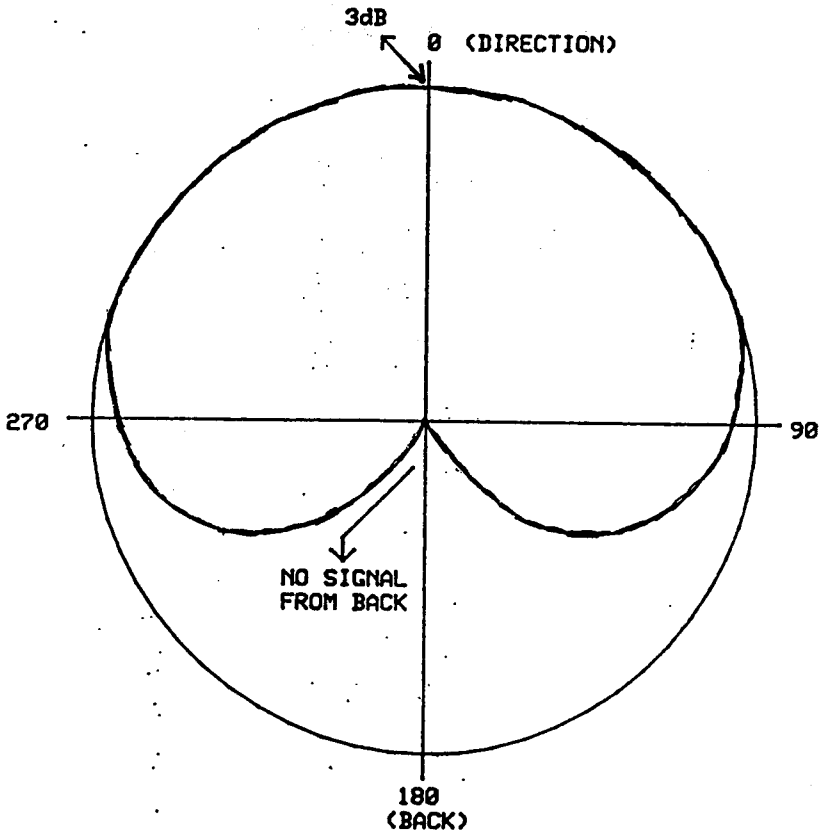


FIGURE 3
AZIMUTHAL PATTERN FROM TWO ANTENNAS

Figure 4 shows how directional (gain) antenna arrays can be formed from four single antennas spaced on the corners of a 1/4 wavelength square. In Figure 4a two opposite antennas are fed at -90 and the other opposite antennas at 0 and -180 degrees respectively. This produces strong radiation in the 315 (NNW) direction. Figure 4b shows two adjacent antennas fed at 0 degrees and the other two adjacent antennas fed at -90 degrees. Now a strong pattern is generated in the 0 degree (N) direction and no signal is radiated off the back of the antenna array.

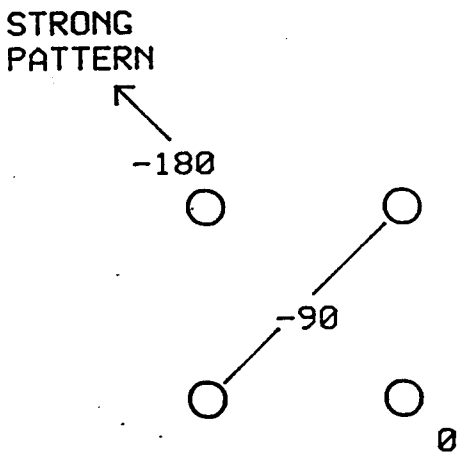


FIGURE 4A

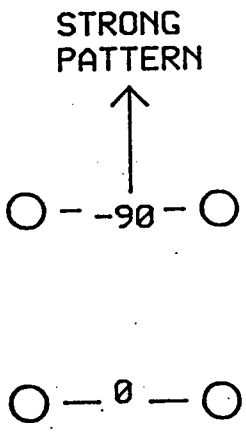


FIGURE 4B

FIGURE 4
DIAGONAL AND BROADSIDE RADIATION PATTERNS

Figure 5 shows how eight different directional patterns can be formed by four antennas spaced 1/4 wavelength and fed with different phasing. This is basically how TRA can sample radio signals from eight sectors of azimuth. Because the antennas that comprise the array interact the radiation patterns actually obtained differ slightly from those computer generated. Figure 6 shows computer generated radiation patterns for the 0,-90 and 0,-90,-180 fed four square arrays.

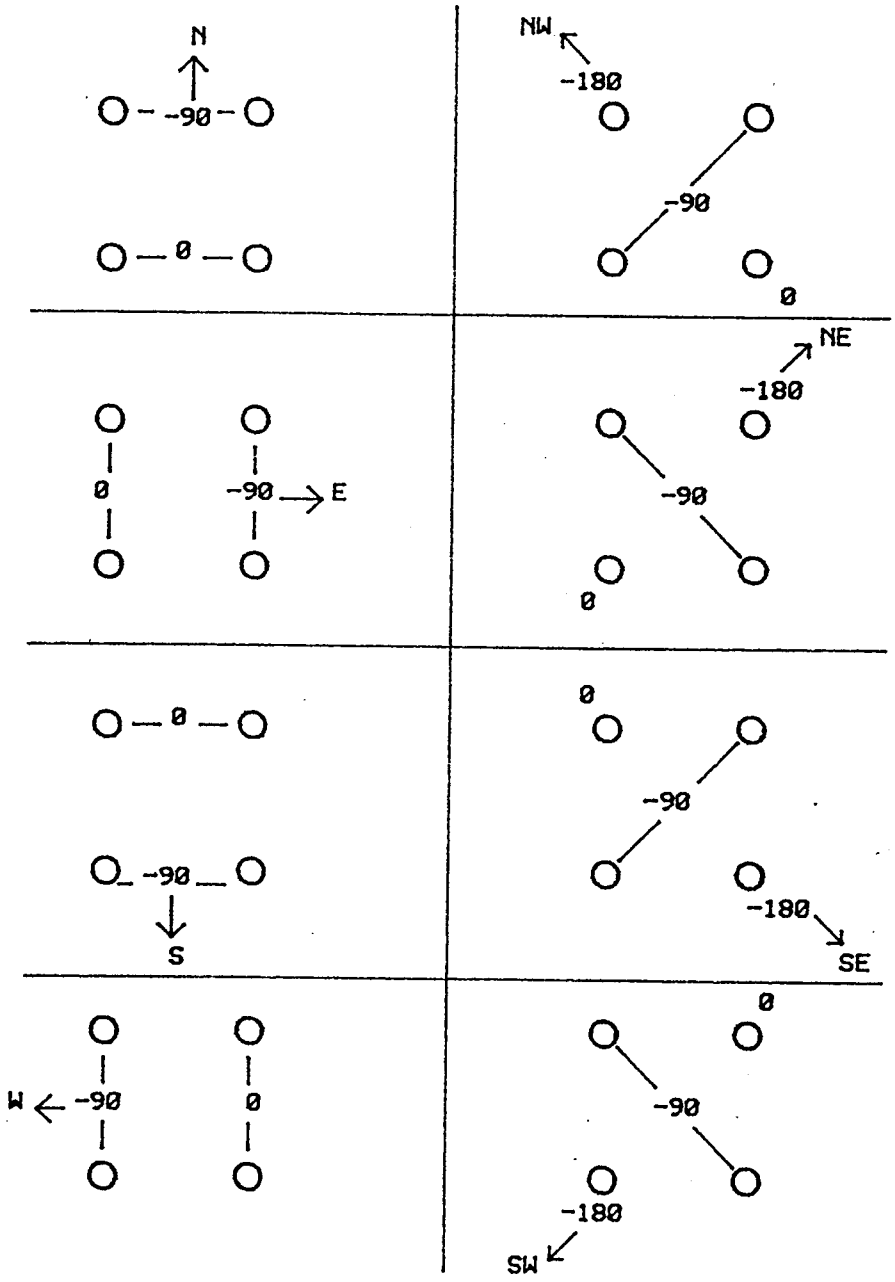


FIGURE 5
DIRECTIONAL PATTERNS FROM FOUR ELEMENT ARRAY

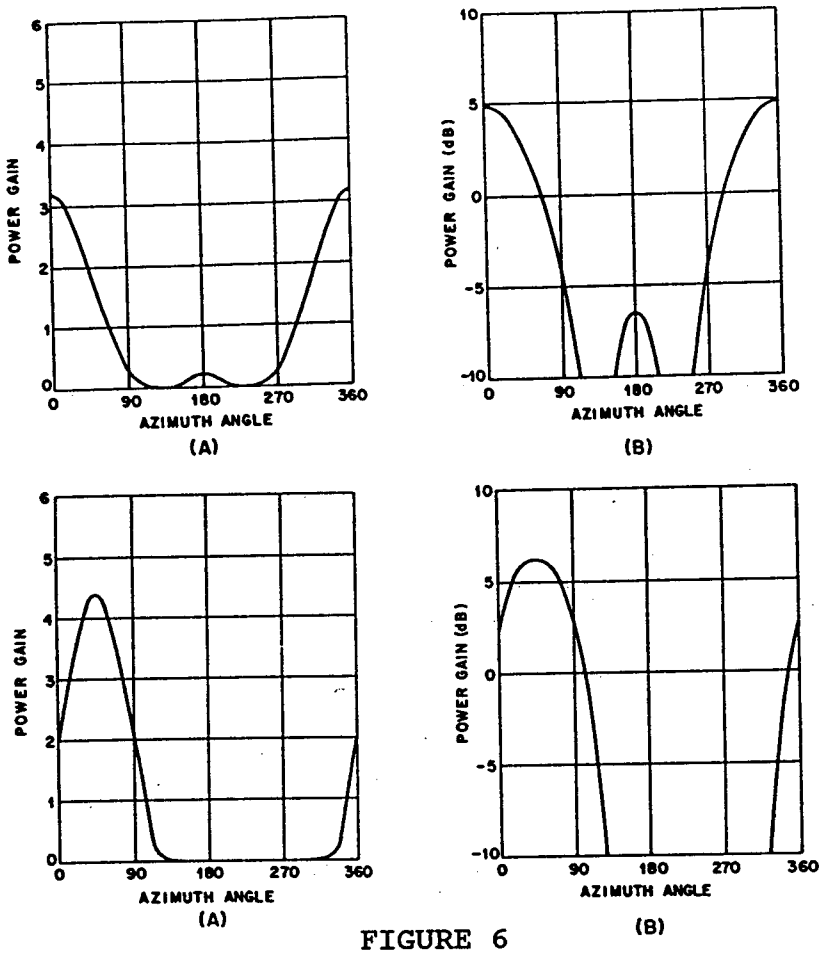


FIGURE 6
COMPUTER GENERATED DIRECTIONAL PATTERNS

II.B. PHASING BOARD (PB)

II.B.1. REQUIREMENTS AND THEORY OF THE PHASING BOARD

The phasing and switching board, as its name suggests, fulfills multiple functions. The board switches the individual antennas, changes the phase to the array, provides proper impedance matching and divides the RF power equally among the antennas comprising the array. Figure 7 shows the block diagram for the PB. Starting at the receiver, the signal is split by a Wilkinson power divider. The two 70 ohm 1/4 wavelength cables provide impedance matching and the 100 ohm resistor absorbs any reflected power from antenna mismatch.

Next are two switches S1 and S2 that provide either straight through routing of RF or routing through a quarter wave section of 50 ohm transmission line. The quarter wave section provides 90 degrees of phase shift as needed. The straight

through configuration introduces no phase shift. The output of the switches S1 and S2 is further split, impedance matched by additional Wilkinson power dividers and fed to switches S3,S4,S5 and S6. Again these switches can introduce no phase shift or 90 degrees of shift.

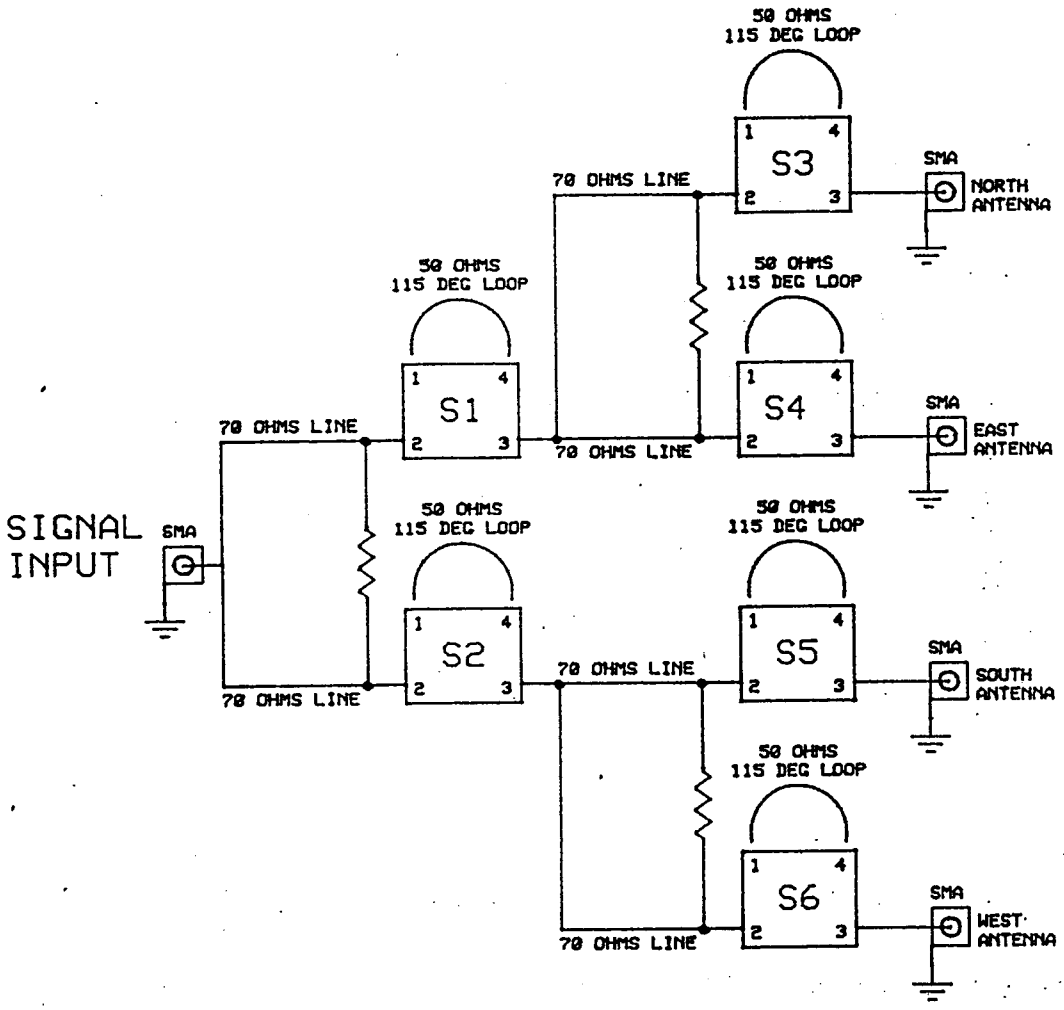
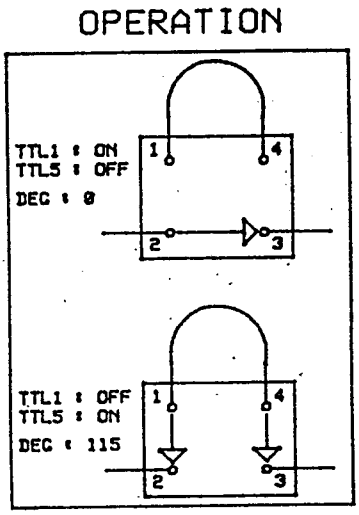


FIGURE 7
BLOCK DIAGRAM OF PHASING BOARD

As an example let us program the system to provide the pattern shown in Figure 5 (SE). Antenna A1 (N) needs 0 shift so both S1 and S3 route straight through . Antenna A2 (E) needs -90 degrees so S4 routes through the additional quarter wave 50 ohm line. Antenna A3 (S) needs -180 degrees of shift so both S2 and S5 route through the quarter wave sections. Antenna A4 (W) needs only -90 degrees, obtained by the S2 routing with S6 straight through. By selecting the correct combination of routing all the eight configurations of Figure 5 can be obtained.

Figure 8 illustrates the construction of the electronic routing switches. Mechanical relays could have been used but could not operate at the speed needed and would arc and wear quickly. The straight through and -90 degree delay configurations are shown in Figure 8a. The actual schematic is shown below in Figure 8b.



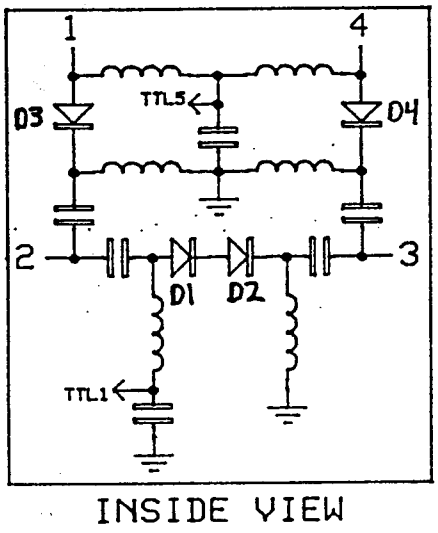


Figure 8a

Figure 8b

FIGURE 8
A PIN SWITCH IN THE PHASING BOARD

In the straight through mode, PIN (P doped,Intrinsic, N doped) diodes are biased on by TTL1 set positive. The DC blocking capacitors pass RF while the RF blocking inductors pass the DC. Thus RF passes from port 2 to port 3. At the same time diodes D3 and D4 are reversed biased (negative at TTL5) to block the RF from ports 1 and 4 and thus preventing the RF from passing through the quarter wave shifter.

To route the RF through the section of quarter wave transmission line D1 and D2 are reversed biased (TTL1 negative)thus blocking the RF from passing from port 2 to port 3. Diodes D3 and D4 are forward biased (TTL5 positive) allowing the RF to traverse the quarter wave section. While only one diode is needed at D1/D2, two are used to preserve the phase symmetry of the switch since two diodes are needed at D3/D4. Figure 9 presents the TTL signals needed to form the various antenna arrays.

PHASING BOARD DRIVER PATTERN CODES FOR EACH DIRECTION	D1	D2	D3	D4	D5	D6	D7	D8
S1 : PA0	-	-		+	+	+	+	+
$\overline{S1}$: PA1	+	+	+	-	-	-	-	-
S2 : PA2	+	+	+	+	-	-	-	+
$\overline{S2}$: PA3	-	-	-	-	+	+	+	-
S3 : PA4	-	+	+	+	+	+	-	-
$\overline{S3}$: PA5	+	-	-	-	-	-	+	+
S4 : PA6	+	+	-	-	-	+	+	+
$\overline{S4}$: PA7	-	-	+	+	+	-	-	-
S5 : PB0	+	+	-	-	-	+	+	+
$\overline{S5}$: PB1	-	-	+	+	+	-	-	-
S6 : PB2	-	+	+	+	+	+	-	-
$\overline{S6}$: PB3	+	-	-	-	-	-	+	+
65C22 PORT A CODE	99	A9	69	6A	66	A6	96	9A
65C22 PORT B CODE	06	0A	09	09	09	0A	06	06

FIGURE 9
LOGIC LEVELS TO DRIVE PHASING BOARD

II.B.2. MEASURED VALUES FOR THE PHASING BOARD

MEASURED PHASE SHIFTS THROUGH THE PHASING BOARD :
Figure 10 shows the phase shift through the board for different configurations of the switch. Note that TRA designed the phase shift to be 0, -110 and -220 degrees rather than the 0,-90 and -180 as discussed earlier. This difference compensated for the interaction of the antennas as mentioned earlier. The figure shows that the worst case phase errors are less than 10 degrees.

CABLE #1

	N	E	S	W
N	-219	-114	-2	-109
NE	-106	-110	1	2
E	-110	-222	-108	-1
SE	-4	-111	-111	-6
S	0	-108	-220	-113
SW	4	2	-110	-110
W	-106	-2	-112	-221
NW	-110	-7	-7	-111

CABLE #2

	N	E	S	W
N	-220	-115	-5	-110
NE	-107	-110	0	0
E	-110	-222	-110	-4
SE	-5	-112	-113	-8
S	-1	-109	-221	-114
SW	3	1	-110	-110
W	-107	-4	-114	-223
NW	-110	-8	-8	-113

FIGURE 10a
MEASURED PHASED SHIFTS THROUGH PHASING BOARD

CABLE #3

	N	E	S	W
N	-219	-113	-3	-109
NE	-106	-110	1	2
E	-110	-221	-108	-2
SE	-4	-111	-111	-7
S	0	-108	-220	-114
SW	4	2	-110	-110
W	-106	-3	-112	-222
NW	-110	-7	-7	-112

CABLE #4

	N	E	S	W
N	-219	-115	-4	-110
NE	-108	-110	0	1
E	-111	-221	-108	-4
SE	-5	-111	-112	-8
S	-2	-108	-220	-115
SW	3	1	-112	-111
W	-107	-4	-114	-221
NW	-110	-8	-9	-113

FIGURE 10b
MEASURED PHASED SHIFTS THROUGH PHASING BOARD

The measured VSWR, S_{21}, and isolation for prototype #1 is shown below. Measured values for both prototypes are included with the Operations Manual shipped with each prototype.

VSWR

	PROTOTYPE #1
ANT 1	2.8:1
ANT 2	3.0:1
ANT 3	2.3:1
ANT 4	2.2:1
ANT 5	2.8:1
ANT 6	2.5:1
ANT 7	2.9:1
ANT 8	2.5:1

S_{21}

	PROTOTYPE #1
ANT 1	-2.8
ANT 2	-3.6
ANT 3	-1.6
ANT 4	-1.8
ANT 5	-2.6
ANT 6	-2.2
ANT 7	-3.2
ANT 8	-2.9

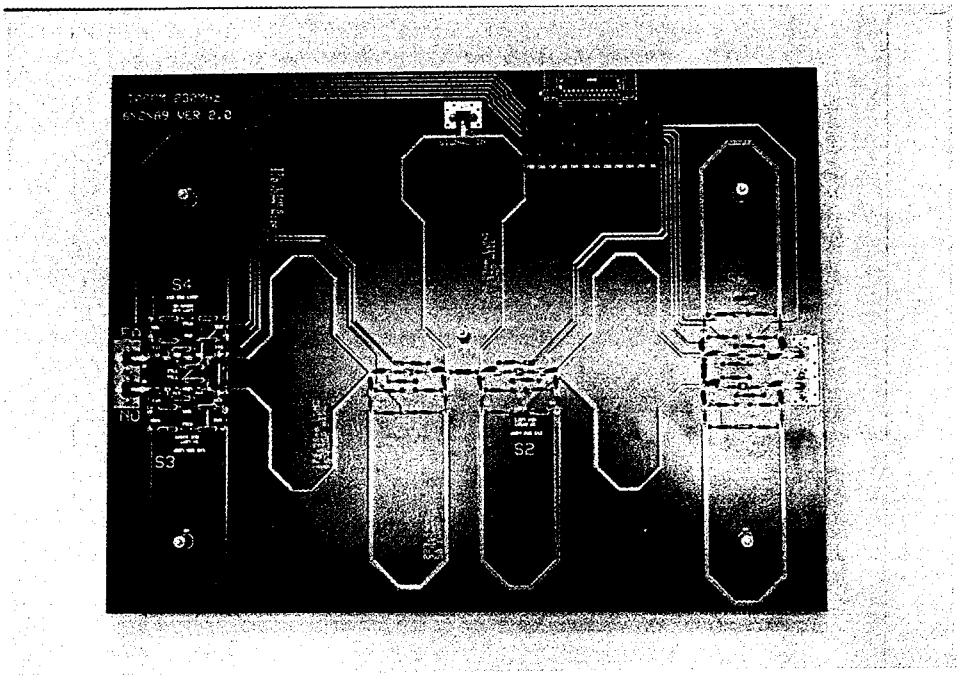
ISOLATION

PROTOTYPE #1

BETWEEN LEGS 1 AND 2.....-16 dB
BETWEEN 1 OR 2 AND ALL OTHER LEGS.....-25 dB
BETWEEN LEGS 3 AND 4.....-16 dB
BETWEEN 3 OR 4 AND ALL OTHER LEGS.....-25 dB
BETWEEN LEGS 5 AND 6.....-14 dB
BETWEEN 5 OR 6 AND ALL OTHER LEGS.....-20 dB
BETWEEN LEGS 7 AND 8.....-15 dB
BETWEEN 7 OR 8 AND ALL OTHER LEGS.....-25 dB

II.B.3. PICTURE OF THE PHASING BOARD

The Phasing Board is shown in Photograph 1.



PHOTOGRAPH 1
PHASING BOARD

II.C. PHASING BOARD DRIVER (PBD)

II.C.1. REQUIREMENTS AND THEORY OF PHASING BOARD DRIVER

The phasing board driver circuitry was not designed for the same fast switching speed as the microwave switch driver. This was due to two reasons : (1) There is no reason for very fast switching times on the VHF signal as the maximum scan rate of the VHF antenna is set by the signal strength output of the radio and there is no signal "glitching" to consider as there is with the microwave signal, and (2) the LR time constant of the phasing board is the critical determinant of the VHF switching time.

The phasing board driver was, however, designed to provide twelve reasonably fast independent dual level outputs which can change state simultaneously. The first stage of the phasing board driver is two 74573 latches. In order to reconfigure the phasing board driver the microcontroller first performs two independent writes to two eight bit ports of the 65C22 PIO device. A separate PIO pin then transfers these two bytes simultaneously to the output of the 74573 latches. The latch outputs are routed to 75150 devices which convert the 0 or 5 volt outputs to +12 or -12 volts. The outputs of the 75150 devices are routed to a push - pull arrangement of RF NPN/PNP transistors which provide current gain. The output current passes through a current limiting resistor and leaves the board through a connector. The 68 ohm output resistors limit the current provided to the PIN diodes to the desired 100 mA.

II.C.2. MEASURED VALUES FOR PHASING BOARD DRIVER

Measured output current : 103 mA

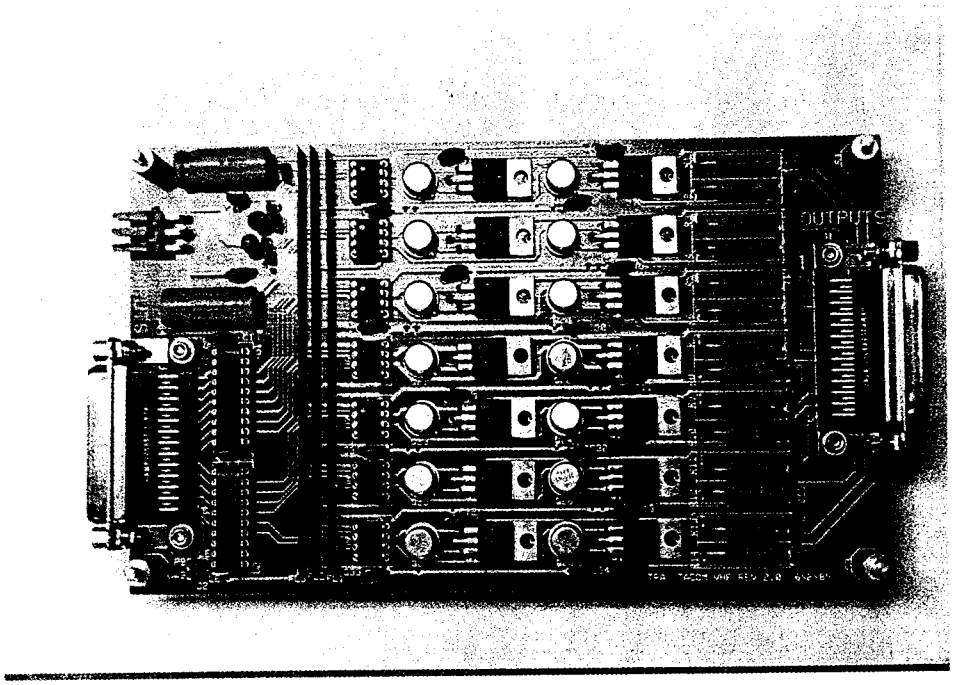
Measured switching time, no load
- Forward bias to backward bias : 40 ns
- Backward bias to forward bias : 40 ns

Measured switching time, phasing board as load
- Forward bias to backward bias : 215 microseconds
- Backward bias to forward bias : 47 microseconds

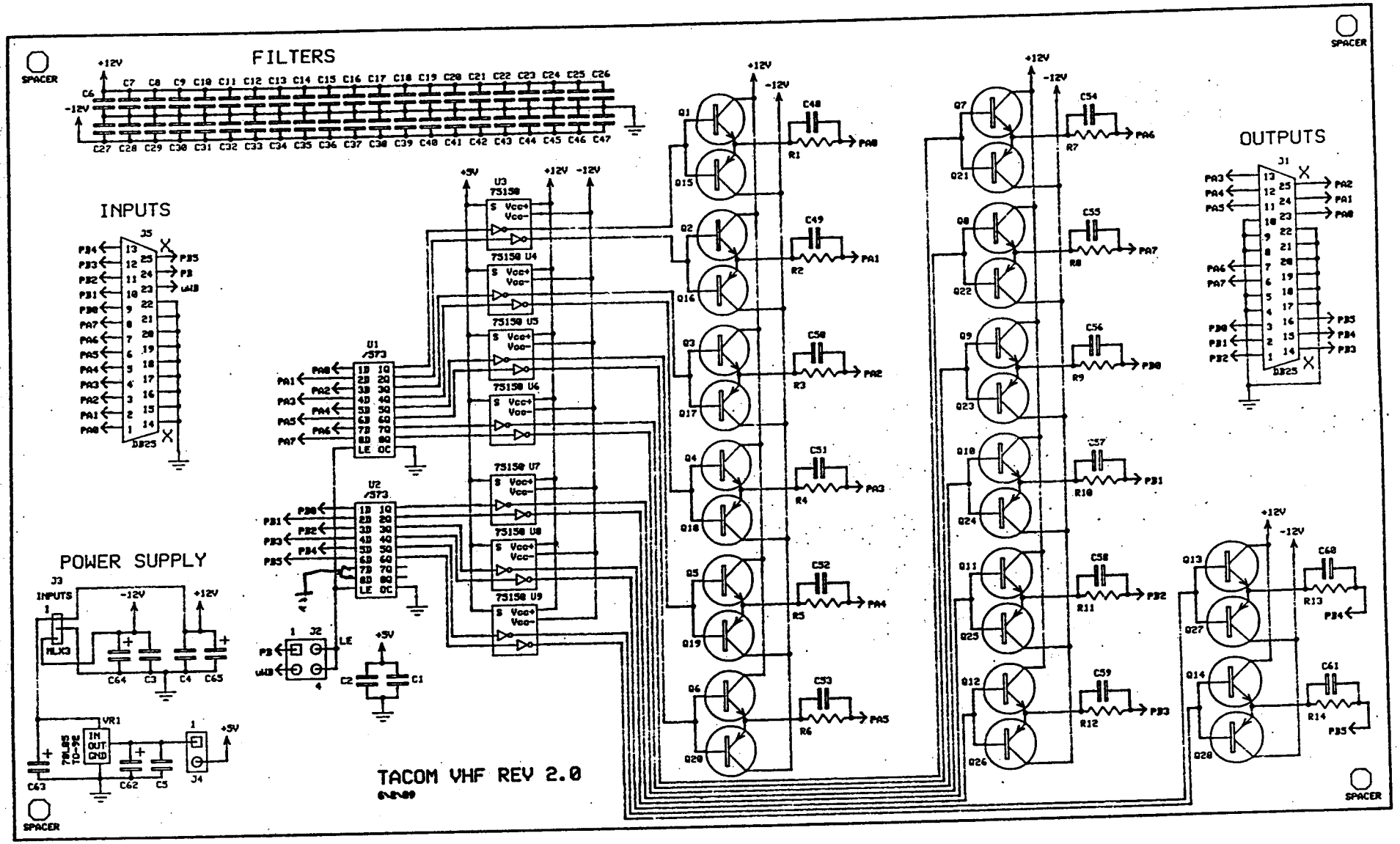
II.C.3. PICTURE AND SCHEMATICS OF PHASING BOARD DRIVER

The schematic of the phasing board driver circuitry is shown in Figure 11.

A photograph of the phasing board driver is shown in Photograph 2.



PHOTOGRAPH 2
PHASING BOARD DRIVER



Schematic of Phasing
Board Driver
Figure 11

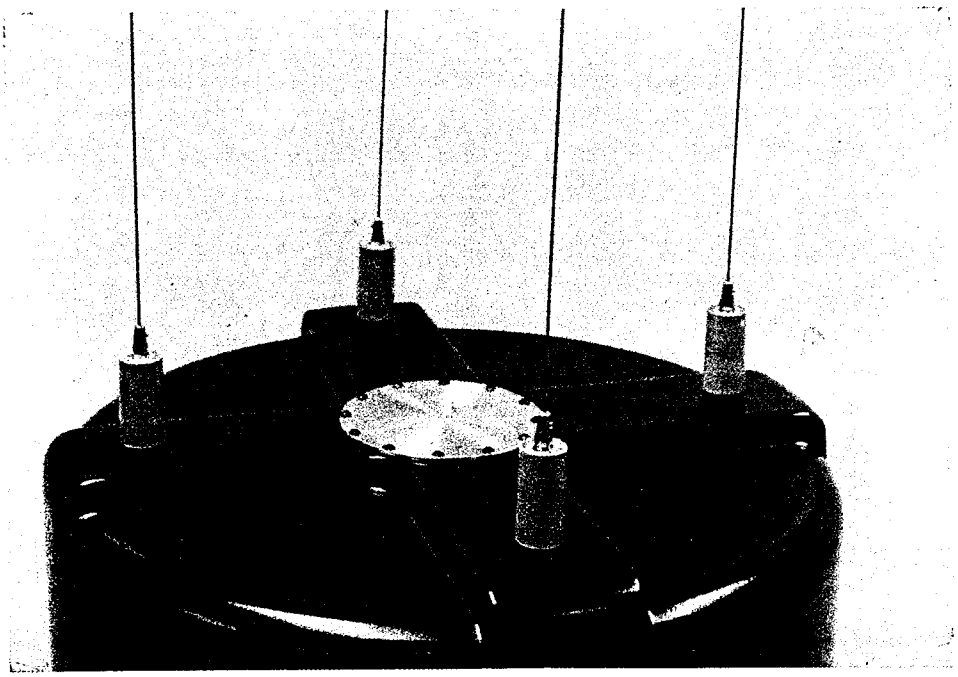
I.D. WHIP ANTENNAS

II.D.1. TYPE

Larsen brand end fed half wave dipole antennas were selected for the 230 MHz phased array. The antennas consist of a half wave radiator and a discrete component matching device. The dipole antenna does not require a ground plane and the array is thus suitable for mounting atop the array with minimum effect on the radiation pattern of the helical array. Center fed dipole antennas would require a central supporting structure that would interfere with the phasing of the four radiators. Thus the best solution was obtained with the end fed dipoles.

During vehicle motion there will be some swinging movement between the four whip antennas. Computer calculation reveals that the radiation pattern is relatively insensitive to such motion as long as the spacing stays within the limits of 0.167 to 0.33 wavelengths. Hence, a spacing of 0.25 wavelengths was chosen. The whip antennas are trimmed to the center frequency of 230 MHz but since the whips are replaceable any frequency in the 225-235 MHz band can be optimized. The whip antennas are affixed to the top of the helical antenna dome which is reinforced. Their cables are routed down through the central mast along with the cables for the microwave helical antennas.

2. PICTURE OF WHIP ANTENNAS



PHOTOGRAPH 3
WHIP ANTENNAS

II.E. VHF SYSTEM TEST

II.E.1. VHF PHASED ARRAY ANTENNA PATTERNS

Figures 12 through 19 show the measured antenna radiation patterns produced by the phased antenna array. The patterns are quite uniform and more than adequate to provide the direction finding needed for the ESABA system.

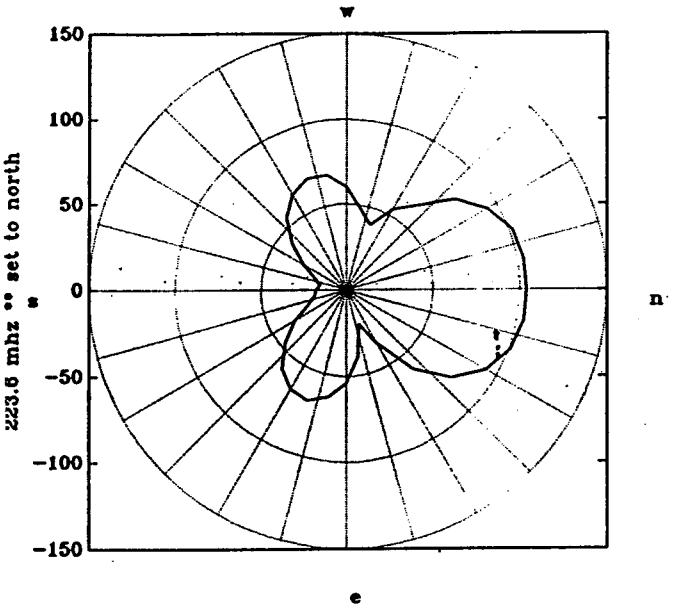


FIGURE 12

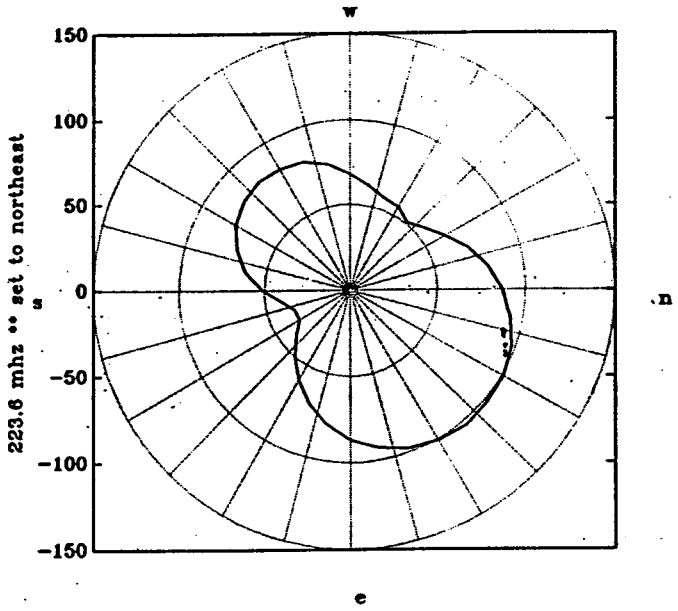


FIGURE 13

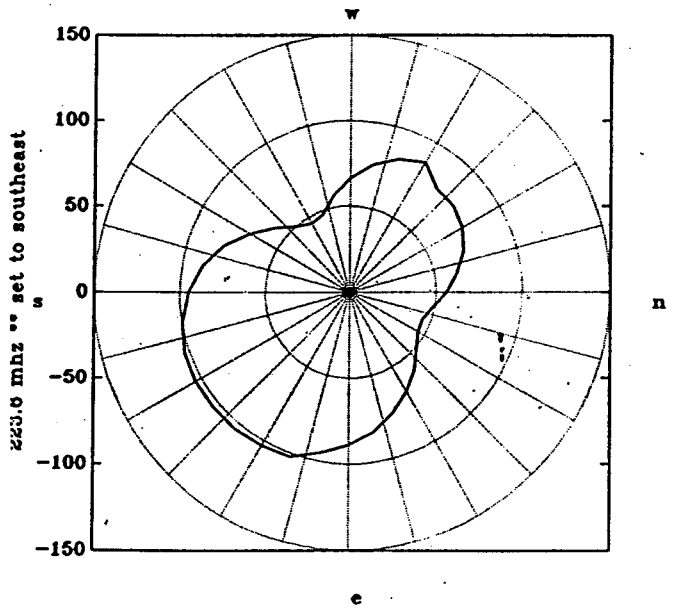


FIGURE 14

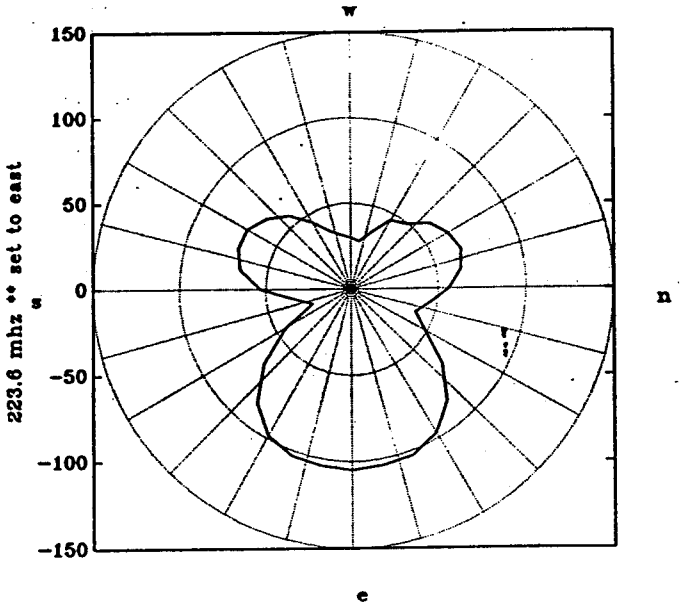


FIGURE 15

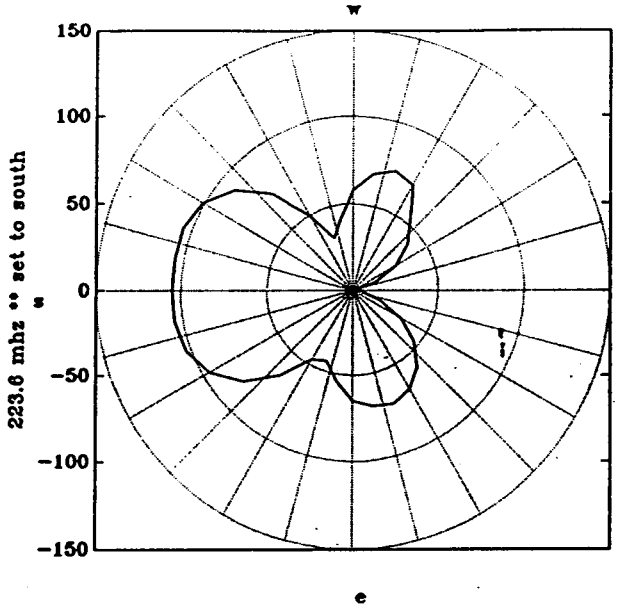


FIGURE 16

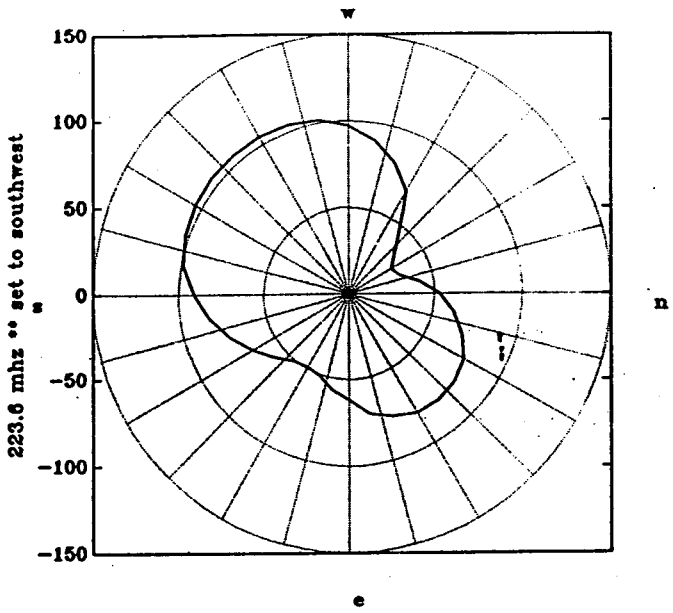


FIGURE 17

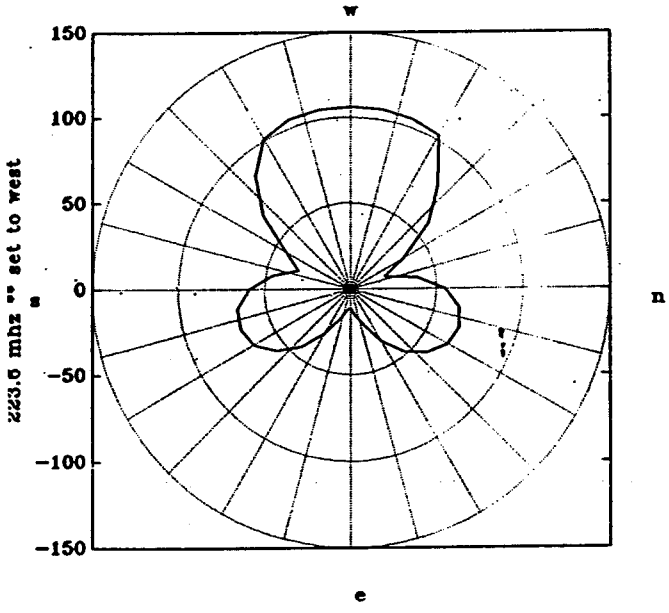


FIGURE 18

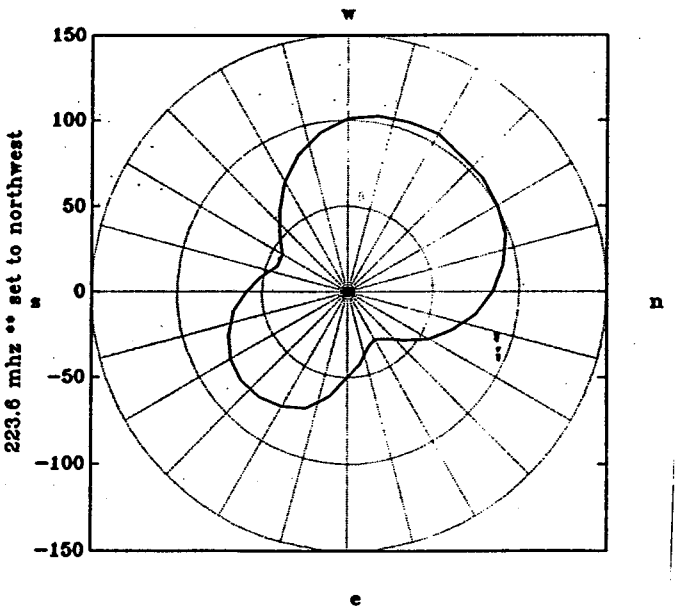
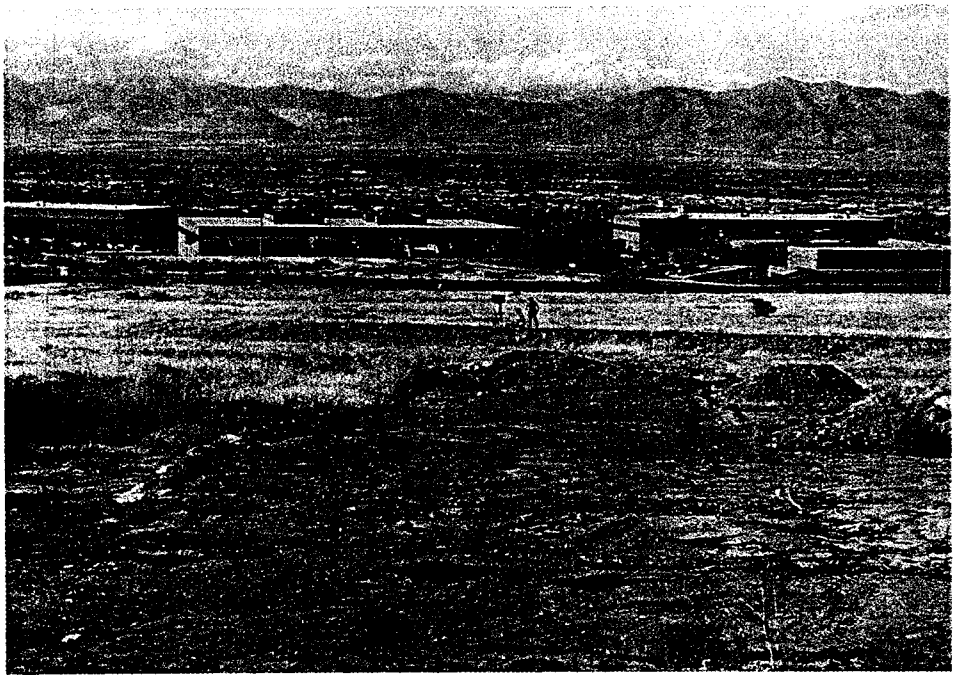


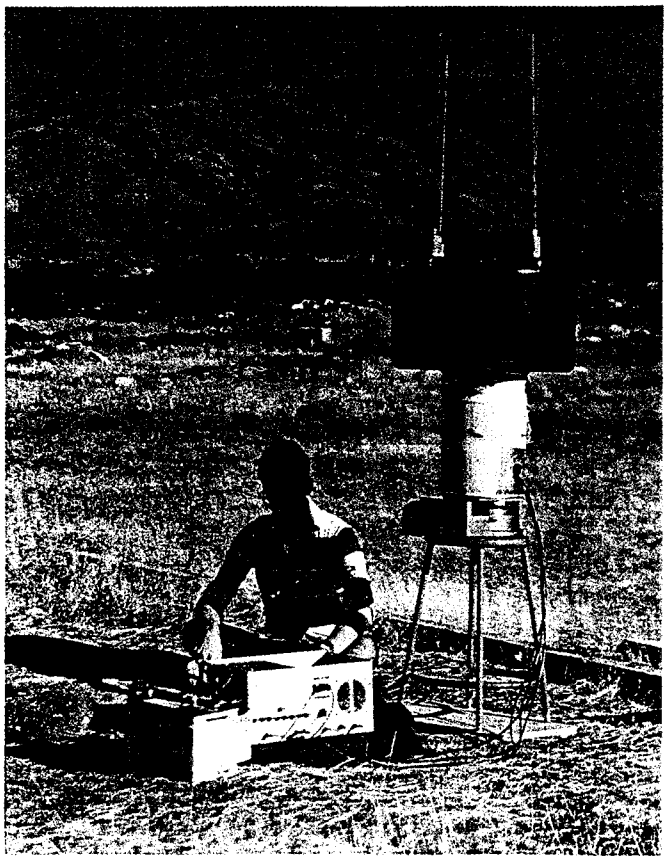
FIGURE 19

II.E.2. PICTURES OF VHF ANTENNA TEST RANGE

Photograph 4a shows the VHF antenna test range used by TRA. Figures 12 through 19 above were obtained in this location. Photograph 4a shows the range as seen from the transmitter. Photograph 4b was taken during final system test.



PHOTOGRAPH 4a
ANTENNA TEST RANGE



PHOTOGRAPH 4b
VHF SYSTEM TEST

III. MICROWAVE LINK

III.A. OVERVIEW OF THE MICROWAVE LINK

The microwave link in many respects was the most difficult component of the ESABA system. Firstly, the antenna system has to operate over a 40% bandwidth (1700-2500 MHz), which is very wide for any gain antenna system. Secondly, the microwave antennas had to provide circular polarization so as to minimize multipath flutter. Thirdly, since the phased array can only resolve eight sectors, the microwave antenna array must transmit in the same eight sectors, thus fixing the beamwidth. Fourthly, the PIN switch has to transition very rapidly so as to minimize video glitching during switching. Finally, the PIN switch has to carry up to 40 watts of RF power from the RCV's video transmitters. Single pole eight throw with this power handling capability are not commercially available.

TRA chose the axial mode monofilar helical antenna. This antenna was invented by John Kraus in 1946. It is a travelling wave type of antenna with wide band width and whose gain and beamwidth can be adjusted by altering the number of turns. Further, the antenna produces circular polarization. It is the only antenna that fits the requirements.

The microwave PIN switch requirements presented great difficulties. Although single pole multiple throw switches are available their power handling capability is of the order of one watt continuous. TACOM's requirement was for up to 40 watts. Additionally, switching has to occur very rapidly so as to minimize glitching of the video signal. If only a single video signal was being transmitted, switching could be done during flyback between frames. However, up to four independent video channels will be transmitted from the RCV.

III.B. HELICAL ANTENNAS

III.B.1. REQUIREMENTS AND THEORY

1. TRA chose the axial mode helical antenna because it ideally suited the requirements of beamwidth, and bandwidth. A six turn helix of circumference equal to one wavelength has a half power beamwidth of 45 degrees, exactly that needed for transmitting into the eight sectors that the phased array can resolve. The axial ratio for this antenna is very close to 1 over the wide frequency range needed. This means that the circularity will remain good throughout the microwave band. The 6 turn helix has realistic gain of about 15 dBi. Since there is a 3 dB ripple in azimuth where the half power points overlap, the array should have at least 12 dBi gain at any point in azimuth. Further, the RCV will be able to pitch +/- 22.5 degrees and still have 12 dBi on axis gain in elevation.

The eight individual helical antennas used in the array are stacked in a 4 over 4 configuration. This stacking is convenient and produces a compact structure. The mounting cube faces also function as a reflector for each helix. The upper and lower cubes are displaced 45 degrees from each other so as to provide eight sector coverage.

Note that the helical antennas generate right circular polarized waves. When such a wave is reflected from a conductive surface polarization is reversed. Thus a right circular polarized receive antenna will not respond to the reflected wave but only the direct wave. This prevents multipath flutter. The ESABA system has the potential for using reflected signal paths with the ability of the RCC to switch polarization of the receive antenna as follows.

Suppose the RCV is transmitting and drives behind an obstruction, losing direct line of sight contact with the RCC. If there is a reflective object, such as a rock face or building nearby, the RCV's phased array will find the reflected path is the strongest and will attempt to route the microwave signal via the reflector. Since the reflection changes polarization the RCC will not receive the microwave unless its receive antenna can change polarization. In future RCC receive antennas it would be desireable to build in this polarization switching capability as was apparently originally proposed.

III.B.2. MEASURED VALUES OF HELICAL ANTENNAS

Figure 20 illustrates a typical radiation pattern for a unit helical antenna. The boresight axial ratio is 1.05 with some deterioration (to 1.26) at the half power points. The pattern is symmetrical about boresight. Figures 21 through 24 show that the antennas suffer little degradation of performance when stacked in the array. Figures 21 and 22 compare the radiation patterns of adjacent top and bottom antennas when in the array at 2.2 GHz. Note that the -3dB (half) power points exceed 45 degrees. Figures 23 and 24 show a similar result at 1.7 GHz. These measurements suggest that the stacking does not degrade individual performance.

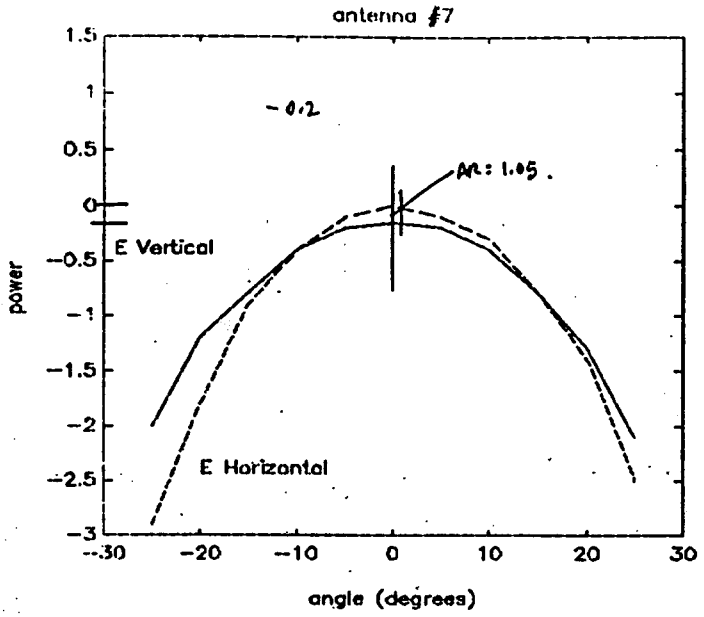


FIGURE 20
TYPICAL RADIATION PATTERN FROM HELICAL ANTENNA

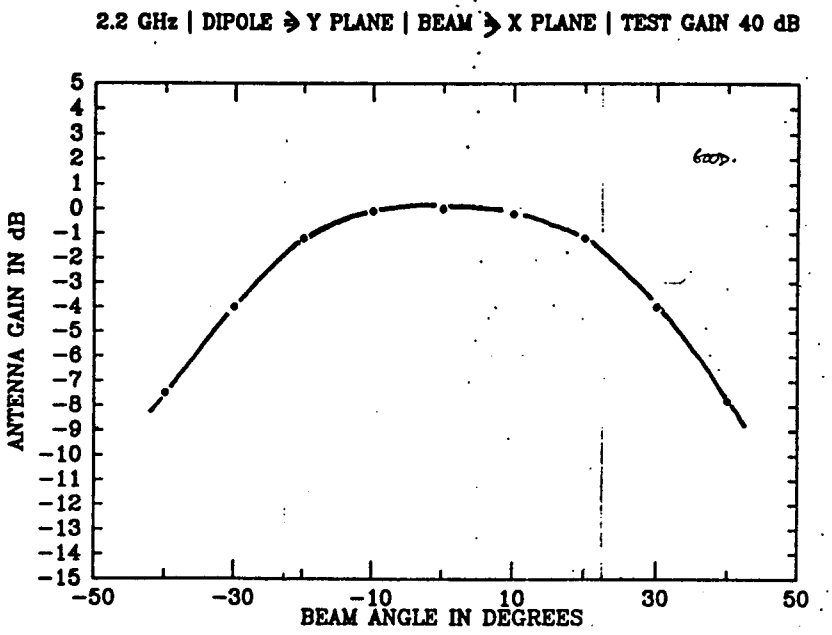


FIGURE 21
RADIATION PATTERN, 2.2 GHZ, TOP HELICAL

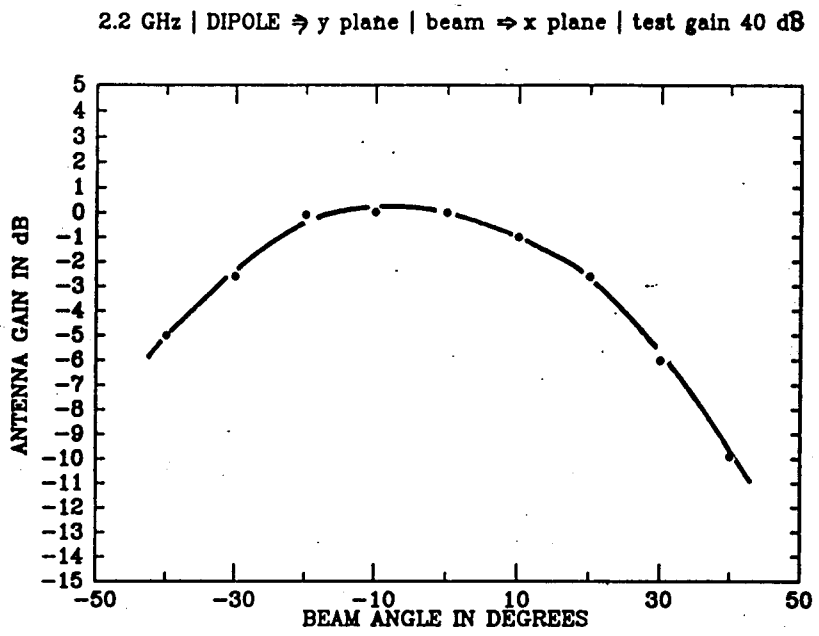


FIGURE 22
RADIATION PATTERN, 2.2 GHZ, BOTTOM HELICAL

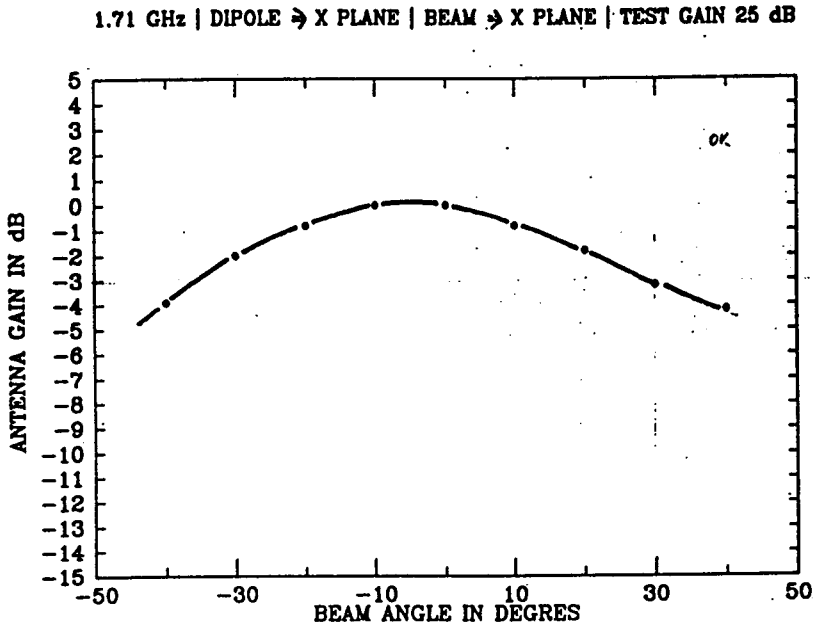


FIGURE 23
RADIATION PATTERN, 1.71 GHZ, TOP HELICAL

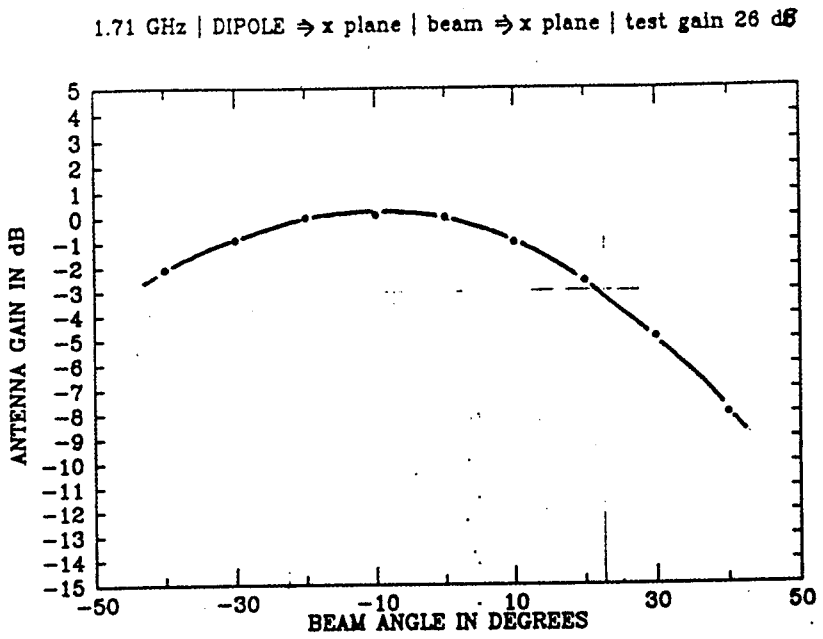
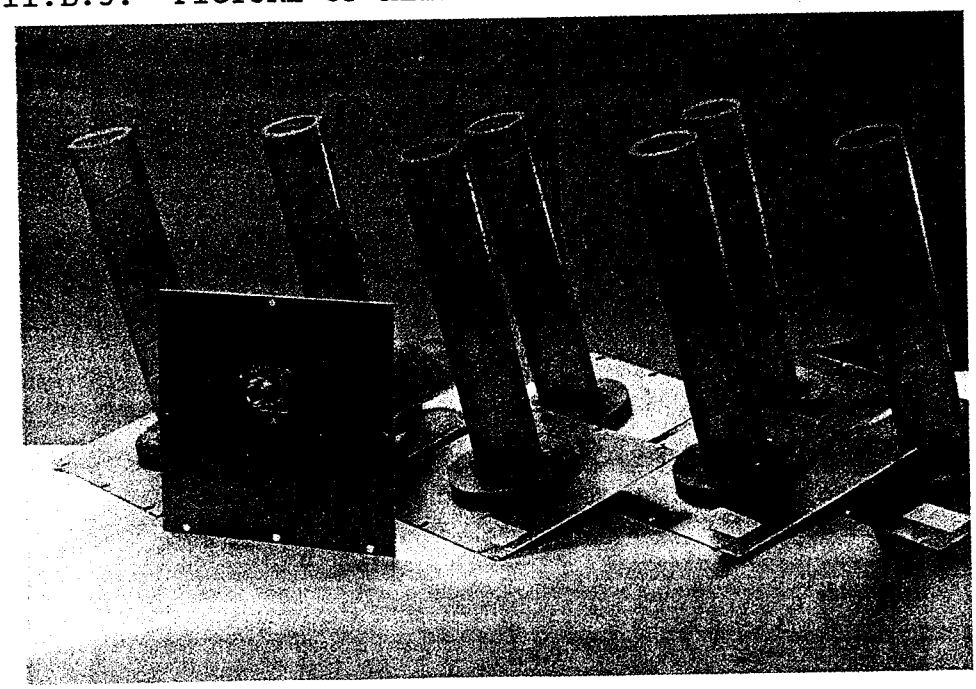


FIGURE 24
RADIATION PATTERN, 1.71 GHZ, BOTTOM HELICAL

III.B.3. PICTURE OF HELICAL ANTENNAS



PHOTOGRAPH 5
HELICAL ANTENNAS

III.C. MICROWAVE SWITCH BOARD (UWSB)

III.C.1. REQUIREMENTS AND THEORY

The microwave switch board needs to switch 40 watts of RF (frequency multiplexed from up to 4 transmitters) to one of the eight helical antennas depending on information from the phased array antenna. The switch is driven by the microwave driver board which in turn is controlled by the microcontroller. TRA chose to design a branched switch after it was determined from computer simulation that that design would be more efficient than spoke type design (see Figure 25). Simulation showed that the branched design was superior with respect to loss and isolation.

The power handling requirement precluded the use of the PIN diodes as direct switches as they were in the Phasing Board receive switch. TRA chose a shunt type switch whose operating principle can be seen in Figure 26. The switch is based on the fact that a quarter wavelength transmission line "inverts" impedance. That is if one end of a quarter wave line is shorted, the other end presents an open (high impedance) and vice versa. In Figure 26 PIN diodes at A and C are spaced one quarter wavelength from the switch input at B. If the diode at A is turned on it effectively shorts A to ground. A signal entering at B "sees" high impedance. The PIN diode at C is reverse biased and creates an open at point C thus a signal at B "sees" a normal transmission line (50 ohms in our design) when looking at C. With high impedance one way and matched impedance the other way the signal is conducted towards C. The structure forms a single pole double throw switch.

This type of switch design has another advantage over the through diode switch. The diodes do not pass any RF so the power handling capacity of the switch is much greater. When diode A is conducting virtually no RF enters the leg from B. When diode at C is off no RF passes through it since the RF "prefers" the lower impedance transmission line path.

The switch that TRA designed actually has two quarter wave sections in series in each leg of the switch to increase the isolation. A novel approach was taken in mounting the diodes. Holes were drilled in the microstrip line at the quarter wave points and the diodes were mounted in these holes and grounded to the ground plane. This preserved the symmetry of the shunted transmission line and provided good heat sinking for the diodes. Because of the width of the microstrip transmission line, full width homemade DC blocking capacitors were fabricated to prevent impedance bumps. The Milar film was tested to 5000 volts.

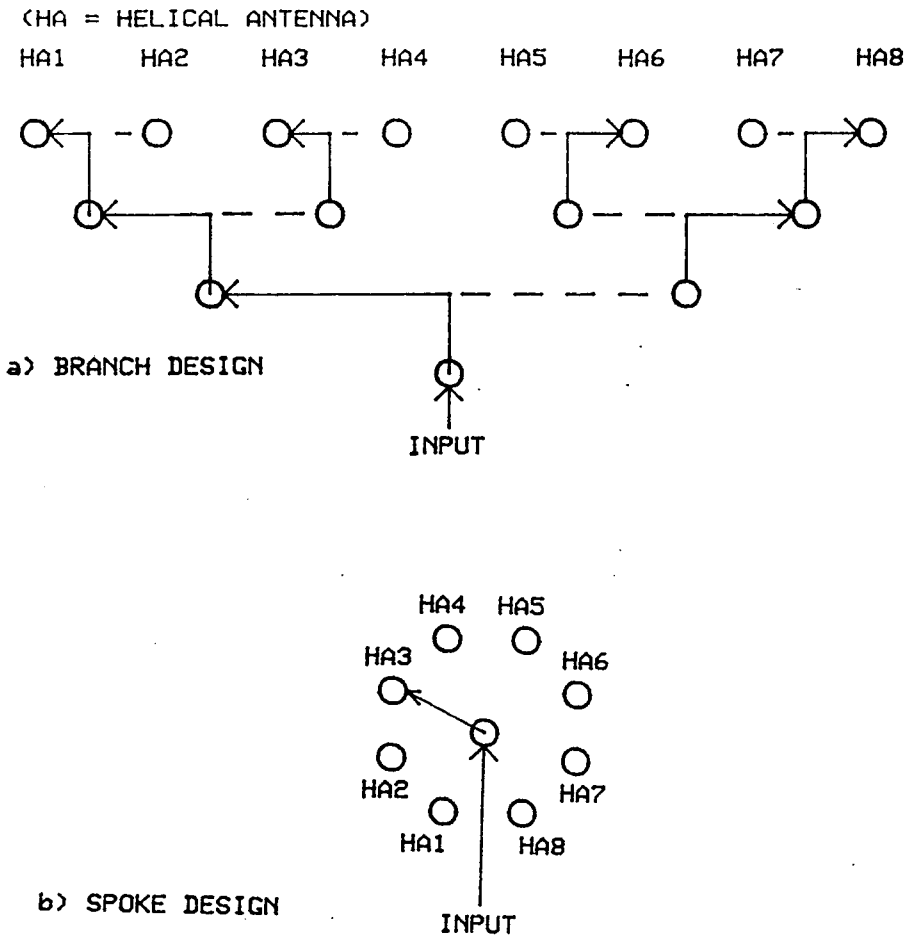


FIGURE 25
BRANCHED AND SPOKE DESIGN OF MICROWAVE SWITCH

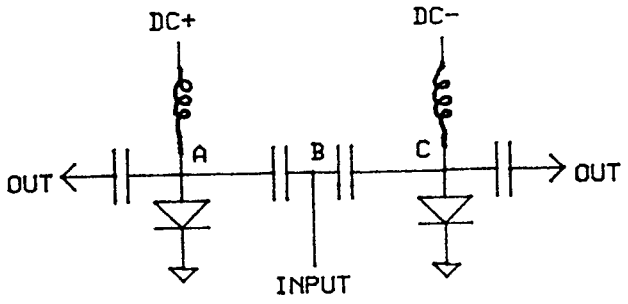


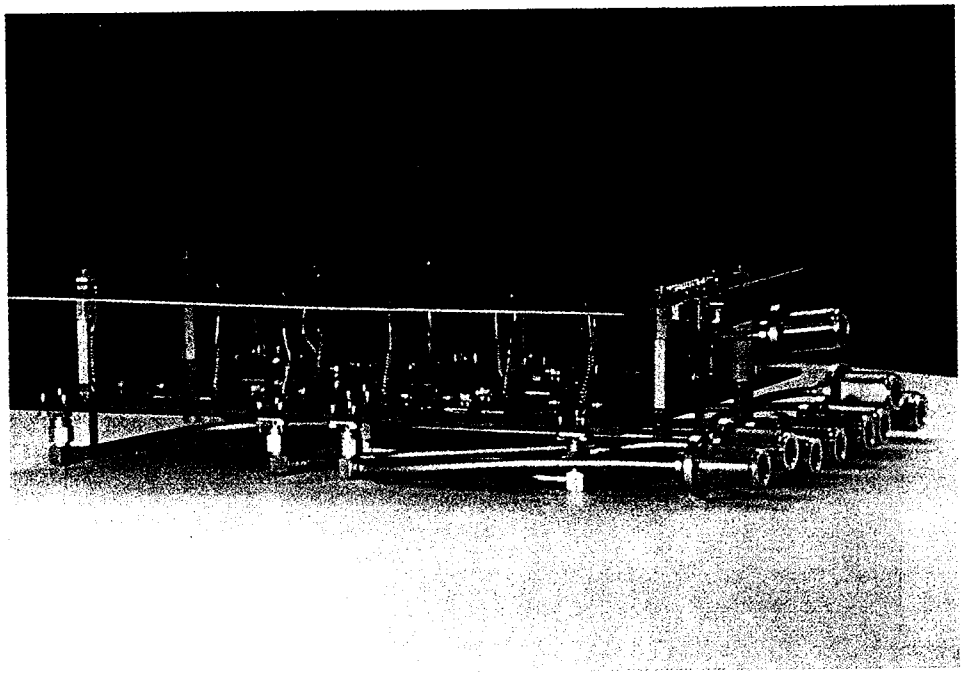
FIGURE 26
SHUNT TYPE DESIGN OF MICROWAVE SWITCH

III.C.2. MEASURED VALUES FOR THE MICROWAVE SWITCH BOARD

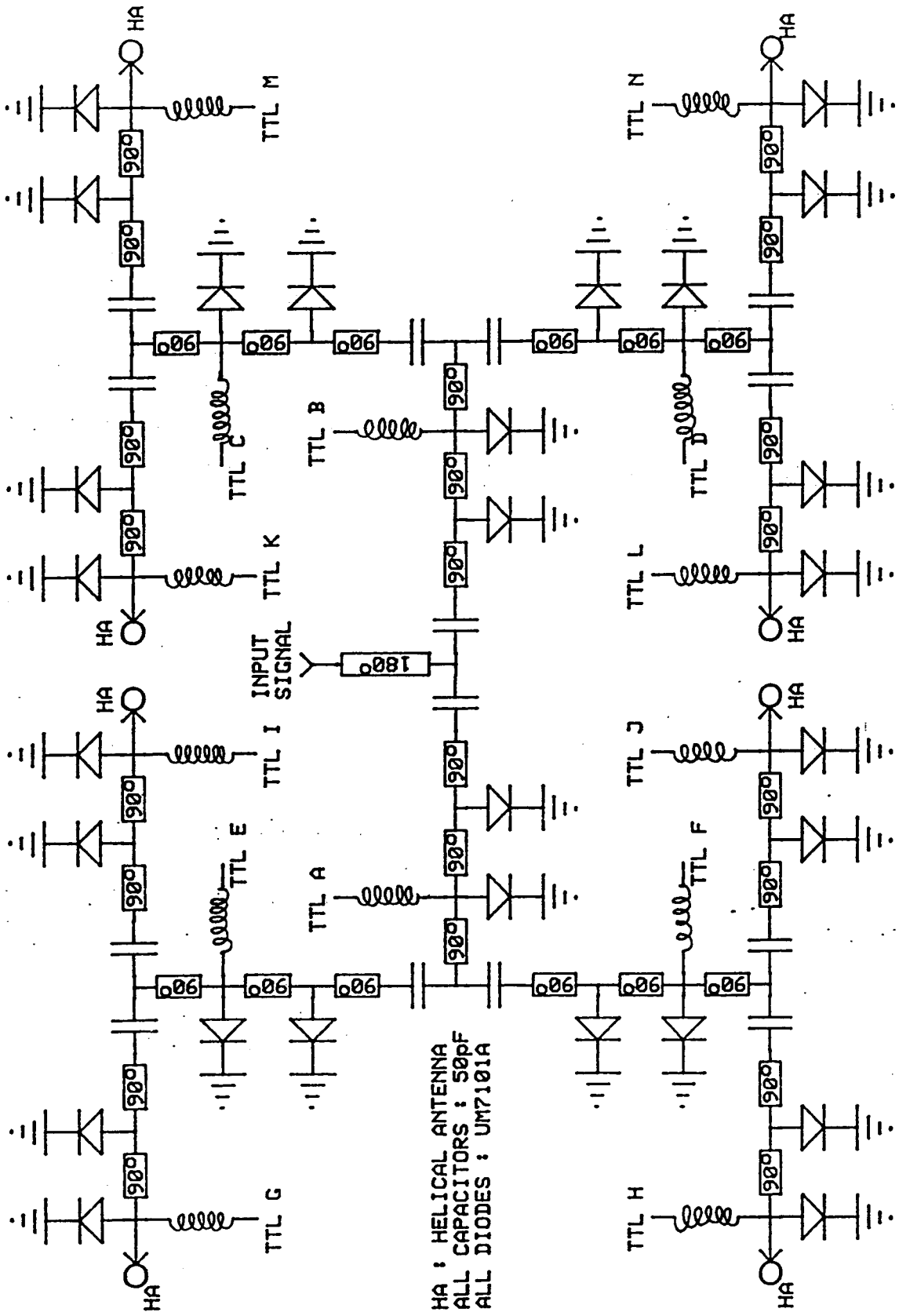
Exact measured values of VSWR, S_{21}, and isolation for each prototype are included in the Operations Manual included with each prototype.

Typical VSWR values for the microwave switch board are 2.6:1 in the low band (1.71 - 1.8 GHz) and 1.8:1 in the high band (2.2 to 2.45 GHz). Typical S_{21} values are -2.5 dB (-3.7 dB worst case) in both bands. Typical isolation is 20 to 25 dB, with 15 dB worst case.

III.C.3. PICTURE AND SCHEMATICS OF MICROWAVE SWITCH BOARD



PHOTOGRAPH 6
MICROWAVE SWITCH BOARD



Schematic of Microwave Switch Board
FIGURE 27

A copy of the layout artwork used in making the microwave switch board is shown below. This image was reduced 25% in order to fit on the page.

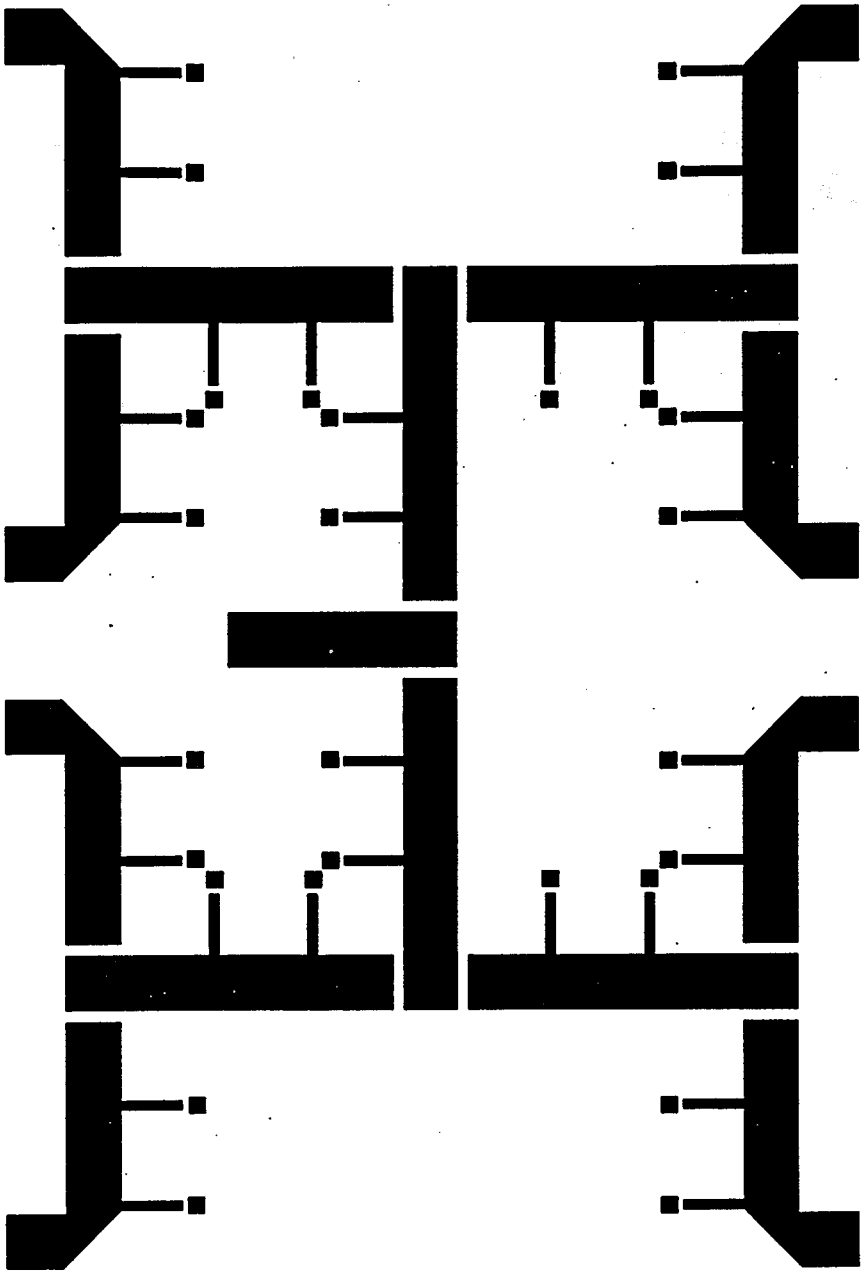


FIGURE 28
ARTWORK FOR MICROWAVE SWITCH BOARD

III.D. MICROWAVE SWITCH DRIVER BOARD (uWSDB)

III.D.1. REQUIREMENTS AND THEORY

The microwave switch driver board was designed to provide fourteen dual level outputs which can simultaneously switch the PIN diodes on the microwave switch board as fast as possible. Fast switching is needed to minimize "glitches" in the video signal when the ESABA system changes microwave antennas.

In order to turn a PIN diode "on" a charge $Q = I_{DC} * \tau$ is applied to the diode, where I_{DC} is the steady state "on" current and τ is the mean life time of the minority carriers. The amount of time needed to provide the charge Q can be shortened by applying a current spike, I_{pk}, for an optimum period given by $t = \tau * I_{DC} / I_{pk}$ before reducing the current output to I_{DC}. If the current spike is maintained longer than this duration then an excess charge will be placed on the PIN diode and the turn off time of the diode will be lengthened since this excess charge has to be removed for turn off. Conversely, optimum turn off time will occur when a large peak current in the opposite direction of I_{pk} is achieved.

The National Semiconductor DH0035 PIN diode driver device is specially manufactured to provide the current levels and timing intervals needed for optimum PIN diode switching, and one of these devices has been incorporated into each channel of the microwave switch driver board.

As with the phasing board driver the microwave switch board driver was designed so that all fourteen of the PIN diode bias outputs switch simultaneously. In order to effect a change in the microwave switch driver board output configuration the ESABA microcontroller first does two separate writes to the 65C22 PIO. A separate PIO output then causes this configuration to latch across the two 74HC573 devices on the driver board simultaneously. The outputs of the 74HC573's are routed to 74240/74244 devices which provide the differential higher current outputs needed by the DH0035 devices, and the DH0035 devices then provide the current and timing relationships as discussed above.

The logic levels used by the microwave switch driver board are shown in Figure 28. Note that because of different construction methods the logic levels are different between the two prototypes. As documented in Section V.B.1, the software is alerted to this difference by the setting of DIP switch 2 on the CPU board.

PROTOTYPE #1
MICROWAVE BOARD DRIVER PATTERN CODES FOR EACH DIRECTION

	D1	D2	D3	D4	D5	D6	D7	D8
A : PA4	-	-	+	+	+	+	-	-
B : PA5	+	+	-	-	-	-	+	+
C : PB4	+	+	-	-	+	+	+	+
D : PA6	+	+	+	+	-	-	+	+
E : PA1	-	-	+	+	+	+	+	+
F : PB1	+	+	+	+	+	+	-	-
G : PA2	-	+	+	+	+	+	+	+
H : PB2	+	+	+	+	+	+	-	+
I : PA0	+	-	+	+	+	+	+	+
J : PB0	+	+	+	+	+	+	+	-
K : PB5	+	+	-	+	+	+	+	+
L : PA7	+	+	+	+	+	-	+	+
M : PB3	+	+	+	-	-	+	+	+
N : PA3	+	+	+	+	+	+	+	+
65C22 PORT A CODE	16	13	20	20	68	E0	10	10
65C22 PORT B CODE	00	00	30	18	00	00	06	03

PROTOTYPE #2
MICROWAVE BOARD DRIVER PATTERN CODES FOR EACH DIRECTION

	D1	D2	D3	D4	D5	D6	D7	D8
A : PA4	-	-	+	+	+	+	-	-
B : PA5	+	+	-	-	-	-	+	+
C : PB4	+	+	-	-	+	+	+	+
D : PA6	+	+	+	+	-	-	+	+
E : PA1	-	-	+	+	+	+	+	+
F : PB1	+	+	+	+	+	+	-	-
G : PA2	+	-	+	+	+	+	+	+
H : PB2	+	+	+	+	+	+	-	+
I : PA0	-	+	+	+	+	+	+	+
J : PB0	+	+	+	+	+	+	+	-
K : PB5	+	+	-	+	+	+	+	+
L : PA7	+	+	+	+	+	-	+	+
M : PB3	+	+	+	-	-	+	+	+
N : PA3	+	+	+	+	+	+	+	+
65C22 PORT A CODE	13	16	20	20	68	E0	10	10
65C22 PORT B CODE	00	00	30	18	00	00	06	03

("+" is a digital 0 and "-" is a digital 1)

FIGURE 29
LOGIC LEVELS FOR MICROWAVE SWITCH DRIVER BOARD

III.D.2. MEASURED VALUES FOR THE MICROWAVE SWITCH DRIVER BOARD

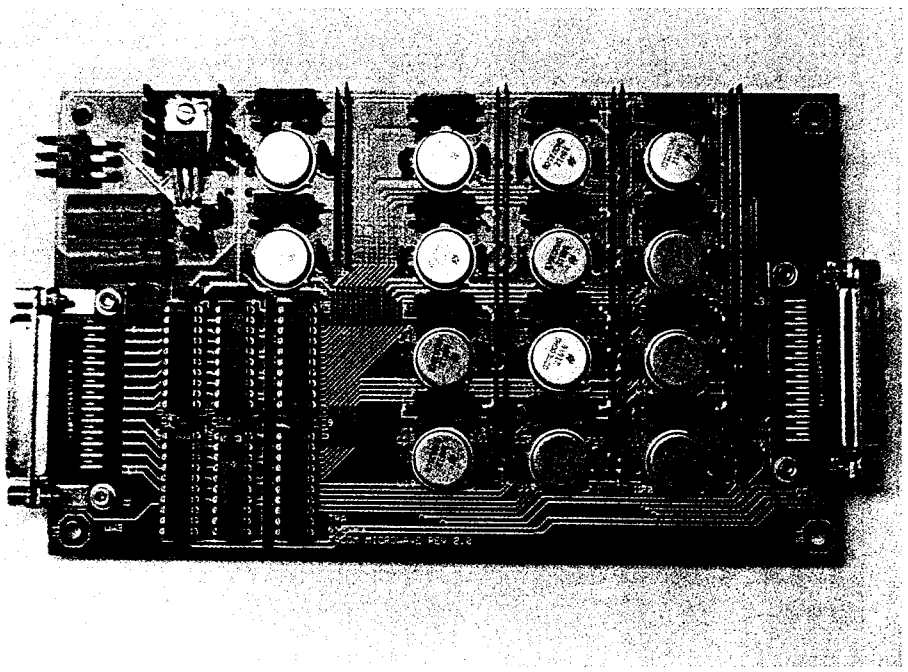
Measured output current : 200 mA

Measured switching time, no load
Forward bias to backward bias : 40 ns
Backward bias to forward bias : 10 ns

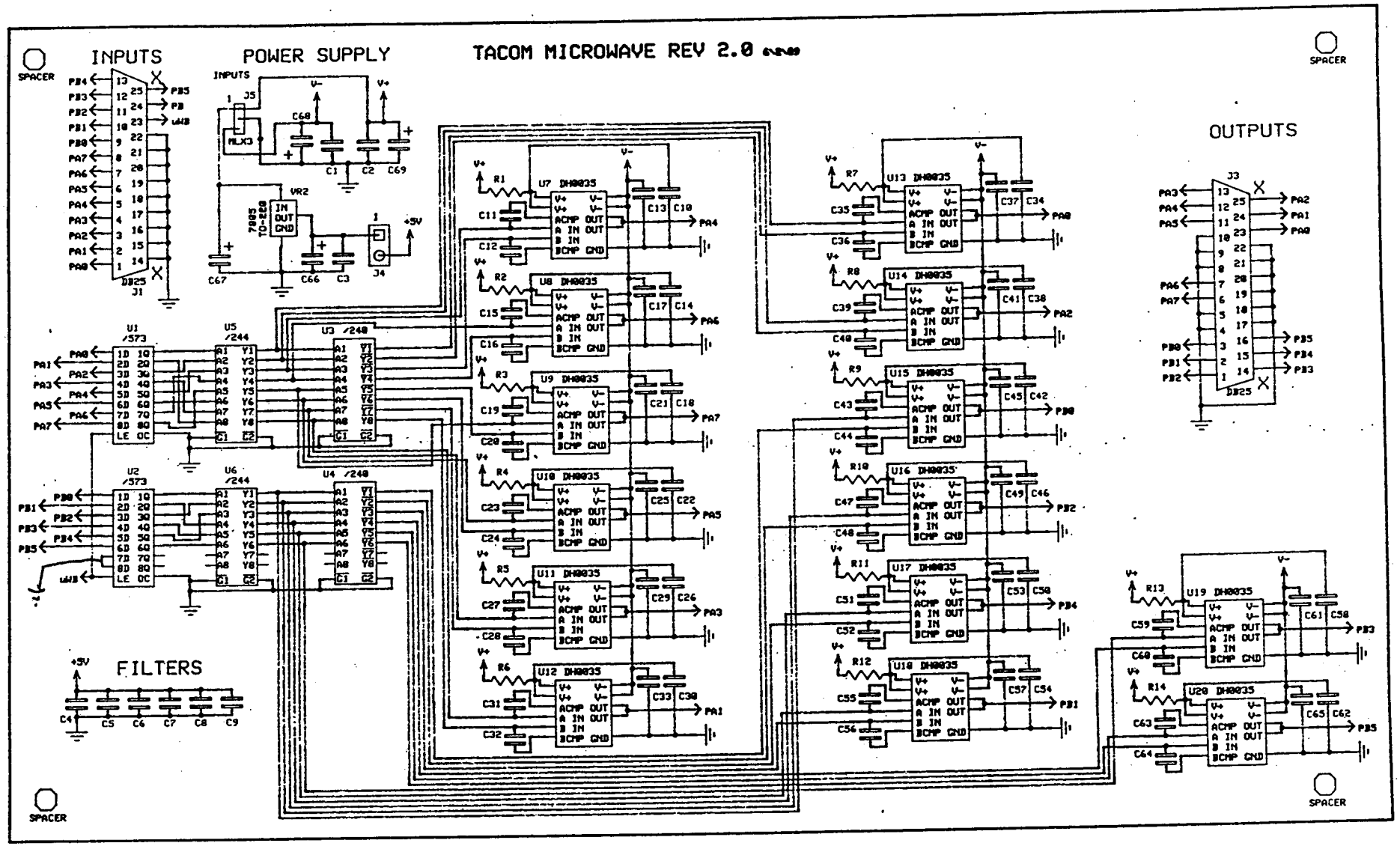
Measured switching time, microwave switch as load
Forward bias to backward bias : 160 ns
Backward bias to forward bias : 10 ns

The above measured values are typical. Exact parameters for each prototype are included in the Operation Manual shipped with each prototype.

III.D.3. PICTURE AND SCHEMATICS FOR THE MICROWAVE SWITCH DRIVER BOARD



PHOTOGRAPH 7
MICROWAVE SWITCH DRIVER BOARD



Schematic of Microwave
Switch Driver Board
Figure 30

IV. MICROCONTROLLER AND RADIO

IV.A. OVERVIEW

The microcontroller board (uCB) controls and directs system operation. As shown in the system block diagram of Section I.C., the uCB controls both the microwave switch board and the phasing board and controls which particular sector is chosen for both the VHF and microwave links.

In actual operation the radio presents a voltage proportional to the strength of the VHF signal it is receiving in a particular sector. The uCB uses a 10 bit A/D converter to capture this information. The signal strength in each of the eight sectors is captured in this way. The uCB analyzes this information to determine the direction of the RCC, and the uCB may decide to change the current sector in which the microwave video signal is being transmitted. The actual logic used in making this decision is detailed in Section V.B.1.

IV.B. MICROCONTROLLER

IV.B.1. GENERAL SPECIFICATIONS

The microcontroller board (uCB) is based on a Motorola MC68HC11A1 microcontroller. This device has 512 bytes of on chip EEPROM, parallel I/O, two types of serial I/O (SCI and SPI), 8 bit A/D channels, sophisticated 16 bit timers, Computer Operating Properly (COP) Watchdog system, etc.

The uCB features :

---Three memory sockets (Can accommodate any device up to 64kx8 by reprogramming the PLD device)
---10 bit serial A/D converter (Linear Technology LTC1091)
---PLD (Programmable Logic Device) allows flexible control signals and decoding
---On-board voltage regulation and inverting allows operation from a single +12 V supply
---Analog ground plane and separate analog voltage regulation.
---On board DIP switch allows control of scan speed and operation modes.
---Parallel output lines allow control of phasing board driver and microwave switch board driver.
---Separate connector allows a debugging module to be connected. The debugging module has an LCD display for error messages, LED's for visual indication of VHF and microwave sector position, DIP switch for operational mode selection, and a reset switch.
---The DC signal strength in circuitry includes voltage

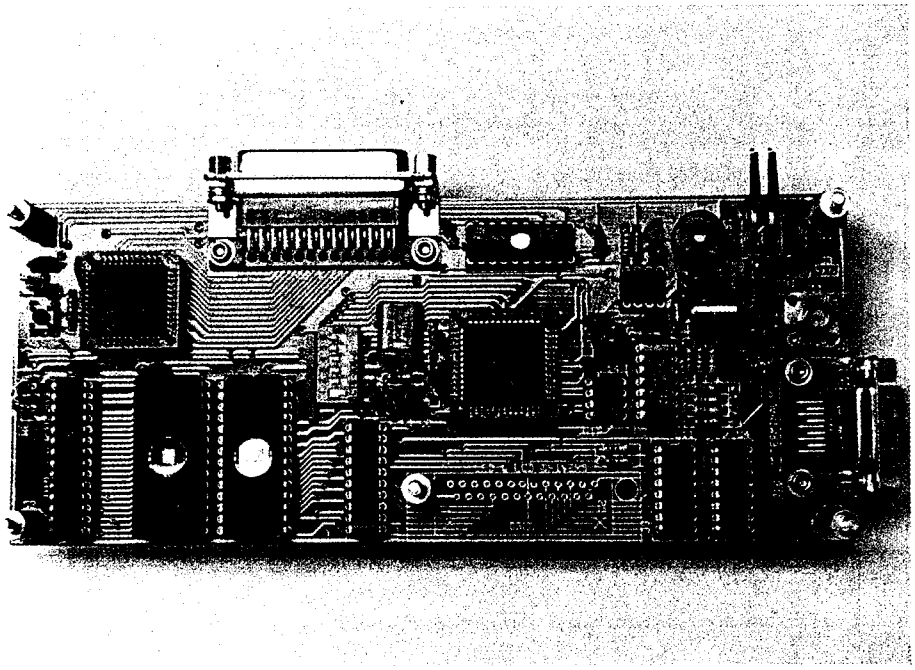
scaling and DC level shifting and low pass filter.
---On board buzzer for diagnostic purposes.
---RS-232 communication.

IV.B.2. PLD PROGRAM LISTING

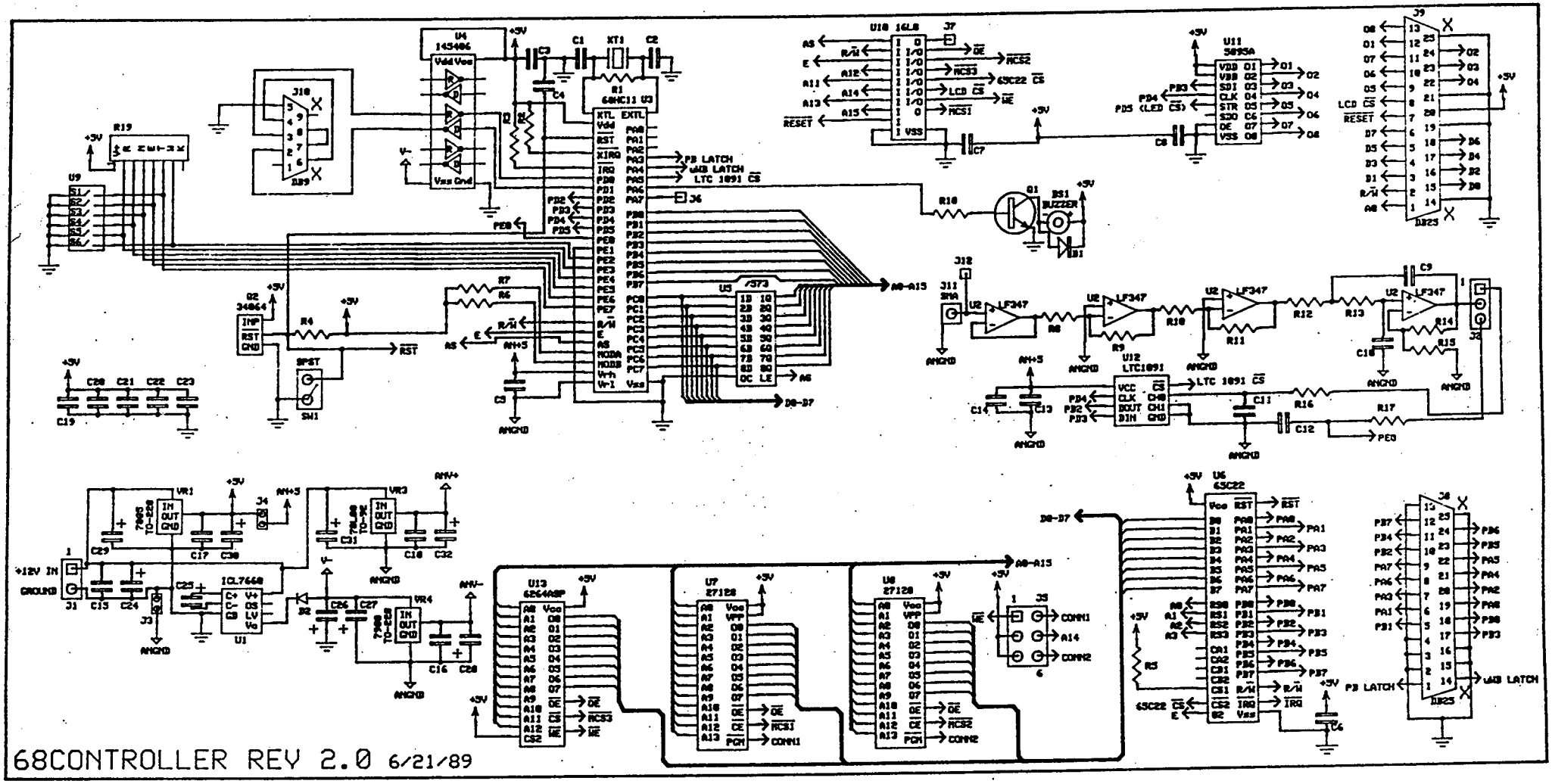
```
*IDENTIFICATION
 TACOM CONTROLLER BOARD DECODER    TACOMVF4
      This version is for a 16V8
 TOM MCLAUGHLIN
 Technical Research Associates, Inc.   7/19/89
*X-NAMES
 E,              ! 68HC11 CLOCK LINE
 RW,             ! 68HC11 READ/WRITE LINE
 RES,            ! RESET LINE
 AS,             ! 68HC11 ADDRESS STROBE LINE
 ADR[11..15];       ! TOP 5 LINES OF 16 BIT ADDRESS BUS
*Y-NAMES
 MCS[1..3],         ! THREE MEMORY SELECT LINES
 IO[1..2],          ! SELECT LINES FOR 65C22 (IO[1]), LCD (IO[2])
 OE,             ! OUTPUT ENABLE FOR MEMORY CHIPS
 WE;             ! WRITE ENABLE FOR MEMORY CHIPS
*RUN-CONTROL
 LISTING = PLOT , EQUATIONS , FUSE PLOT , NET , PINOUT;
 PROGFORMAT = JEDEC;
*FUNCTION-TABLE
 $  RES , AS , E , (ADR[15..11]) : ((MCS[1..3] , IO[1..2]));
; ================================================================
   0  , - ,  - ,      -              :   111 11   ; DISABLED
     1  , 0 ,  1 , 01CH..01FH        :   011 11   ; E000-FFFF (U7)
     1  , 0 ,  1 , 18H..1BH          :   101 11   ; C000-DFFF (U8)
     1  , 0 ,  1 , 10H..13H          :   110 11   ; 8000-9FFF SOCKET
     1  , - ,  - , 014H              :   111 01   ; 65C22 AT A000
     1  , 0 ,  1 , 015H              :   000 01   ; LCD at A800
 REST                                :   111 11   ; NOTHING SELECTED
 $  E , RW : ((OE , WE));
; ================================================================
   1 , 1  :   0 1; OE ACTIVE
     1 , 0  :   1 0; WE ACTIVE
 REST       :   1 1; BOTH OE AND WE INACTIVE
*PAL
 TYPE = GAL16V8_C7;
*PINS
 ADR[15]  = 8,
 ADR[14]  = 6,
 ADR[13]  = 7,
 ADR[12]  = 4,
 ADR[11]  = 5,
 MCS[1]          = 12,
 MCS[2]          = 17,
 MCS[3]          = 16,
```

```
 IO[1]           = 15,          ! SELECT FOR 65C22 AT A000H
 IO[2]           = 14,          ! SELECT FOR LCD AT A800H
 OE              = 18,
 WE              = 13,
 E               = 3,
 RW              = 2,
 AS              = 1,
 RES             = 9;
*END
```

IV.B.3. PICTURE AND SCHEMATICS OF MICROCONTROLLER BOARD



PHOTOGRAPH 8
MICROCONTROLLER BOARD



Schematic of Microcontroller
Board
Figure 31

IV.C. RADIO

IV.C.1. GENERAL SPECIFICATIONS

The VHF scanning radio is receive only and is an IMSCO Model ADC-MR. Radio specifications are given in the Operations Manual included with each prototype.

IV.C.2. MEASURED VALUES

The radios included in the TRA ESABA prototype have been modified to provide a DC voltage proportional to the received VHF signal strength. In testing in September 1989 at TRA the response time of this signal was 5 milliseconds, although IMSCO was working to improve this performance at the time this final report was written in October 1989. This response time restricts the scanning speed to 25 Hz (5 ms per sector times 8 sectors is T = 40 ms, f = 1/T = 25 Hz). The TRA ESABA is capable of 2500 Hz or better, so this response time does degrade system performance.

IV.C.3. INTERFACE WITH MICROCONTROLLER AND PHASING BOARD

The role of the IMSCO VHF receive only radio can be seen in the block diagram of Section I.C. When the microcontroller sets the phasing board driver and phasing board to configure the four element phased array to "point" in a particular direction, the IMSCO radio receives the VHF signal present in this sector. The signal strength output from the radio presents a voltage proportional to this signal strength to the microcontroller board. The signal is passed to a level shifting / gain circuit, through a two pole low pass filter, and then to the 10 bit A/D converter. The signal is digitized and recorded for further analysis.

IV.C.4. SCHEMATICS OF RADIO

(SEE OPERATIONS MANUAL)

V. SOFTWARE

V.A. OVERVIEW

The system software is divided into two main areas : the main program written in assembly language and a Forth monitor with various system test and debugging aids.

V.B. MODE SELECTION

V.B.1. DIP SWITCH SELECTION OF OPERATION MODES

The mode of operation, i.e., the program executed, is set using the DIP switch found on the CPU board. This board is the top board in the smaller aluminum compartment next to and on the same level as the radio. Once the cover of the aluminum box is removed, the 6 position DIP switch is easily seen.

The mode of system operation is set as follows :

DIP SW #1....OFF	Load "normal" operation assembly program "TACMAIN" and begin operation
DIP SW #1 ...ON	Load Forth monitor and Forth system test aids.
DIP SW #2 ...ON	Use with TRA ESABA Prototype #1.
...OFF	Use with TRA ESABA Prototype #2.

DIP switches 3,4, and 5 set the scan speed for the main program TACMAIN. A scan speed of 25 Hz means that 5 milliseconds is spent in each sector (5 ms times 8 sectors = 40 ms, 1/T is 25 Hz). As of October, 1989 the IMSCO radio signal strength output response time of 5 ms restricts system operation to 25 Hz. The TRA ESABA is capable of operating at 2500 Hz, if the radio response time could be improved to about 300 microseconds.

SW #3	SW #4	SW #5	
ON	ON	ON	SCAN AT 4 HZ (TEST MODE)
ON	ON	OFF	SCAN AT 25 HZ
ON	OFF	ON	SCAN AT 50 HZ
ON	OFF	OFF	SCAN AT 100 HZ
OFF	ON	ON	SCAN AT 200 HZ
OFF	ON	OFF	SCAN AT 300 HZ
OFF	OFF	ON	SCAN AT 400 HZ
OFF	OFF	OFF	SCAN AT 2500 HZ

DIP SW #6 ...ON FUTURE EXPANSION
...OFF

V.B.2. COMPUTER OPERATING PROPERLY (COP) WATCHDOG ACTIVATION

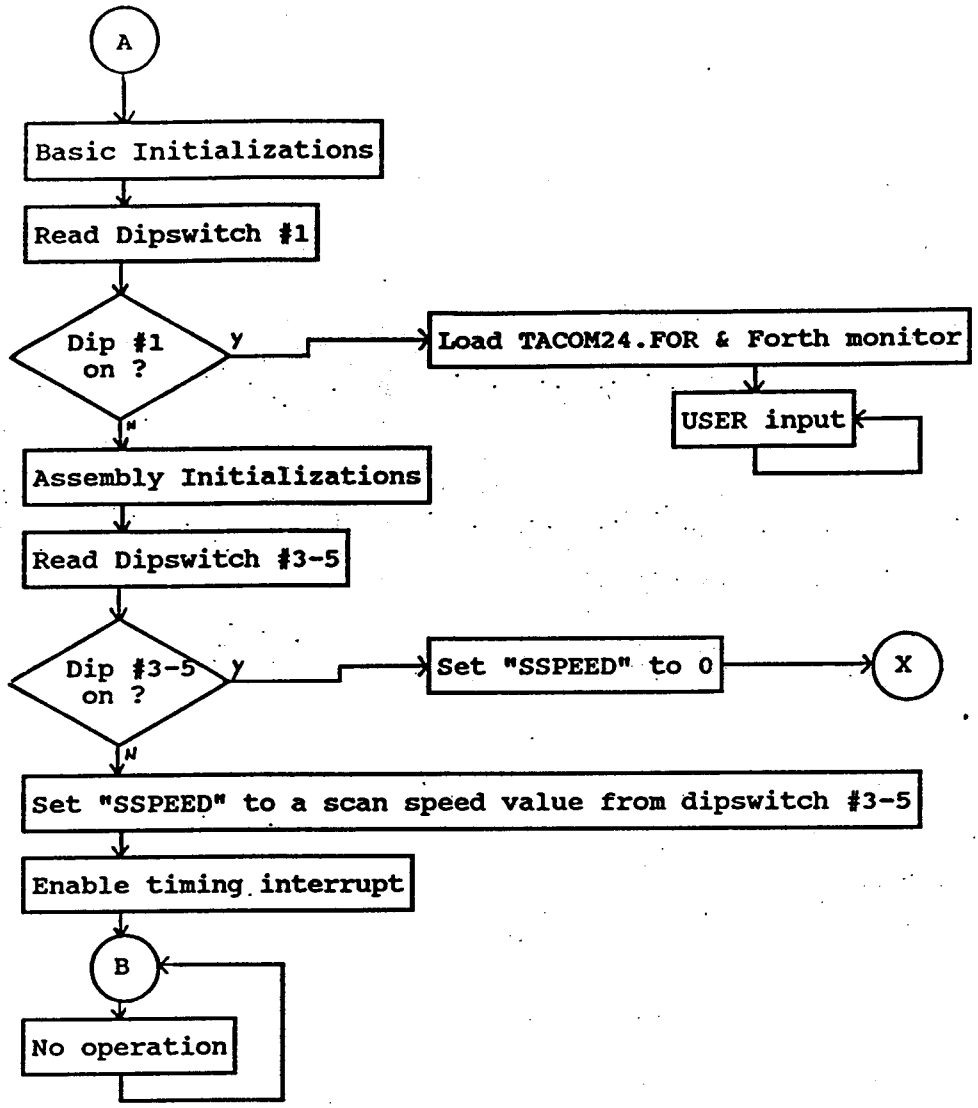
The Motorola 68HC11 family has a Computer Operating Properly (COP) watchdog timer which provides protection from software failures. When activated, the COP timer is set to 65 milliseconds. If the timer is allowed to time out, then a system reset is performed and the software program is restarted. In normal operation the ESABA software periodically resets the COP timer to prevent this occurrence. If the ESABA program somehow fails or gets lost, then this timer reset will not occur and a general system reset will restore system operation.

It is not possible to activate or deactivate the COP timer in software. Unfortunately, an activated COP timer interferes with the Forth monitor and the Forth test and debugging aids built into the ESABA system. For this reason TRA has shipped the ESABA system with 68HC11 devices which have deactivated COP timers. This will allow TACOM access to the test modes of the Forth monitor. If added protection from software failure is desired, TRA has also included 68HC11 devices with the COP timers activated. These devices will then need to be installed in the ESABA CPU board. This operation is simple enough for any electronic technician to perform.

V.C. MAIN PROGRAM

V.C.1. FLOW CHART OF MAIN PROGRAM

"TACMAIN5.ASM" assembly language program flowchart.



Basic Initializations
-set prescaler to 1
-set "OPTION" to 89H
-set stack ptr to FFH
-set system ram to 0000H
 & system regs to B000H
-set phasing & microwave
 antennas to D2
-init I/O ports & A/D line

Assembly Initializations
-set "FLAG","COUNT1","COUNT2" to 0
-set "BESTSS","WINSS" to 0
-set "DCODEN","WINDIR","BESTD" to D2
-set "UPA","UPB" to D2 for microwave
 antenna settings
-set OC2 to leave PA0-7 alone
-clear pending OC2F interrupts

FIGURE 32a
FLOW CHART OF MAIN PROGRAM

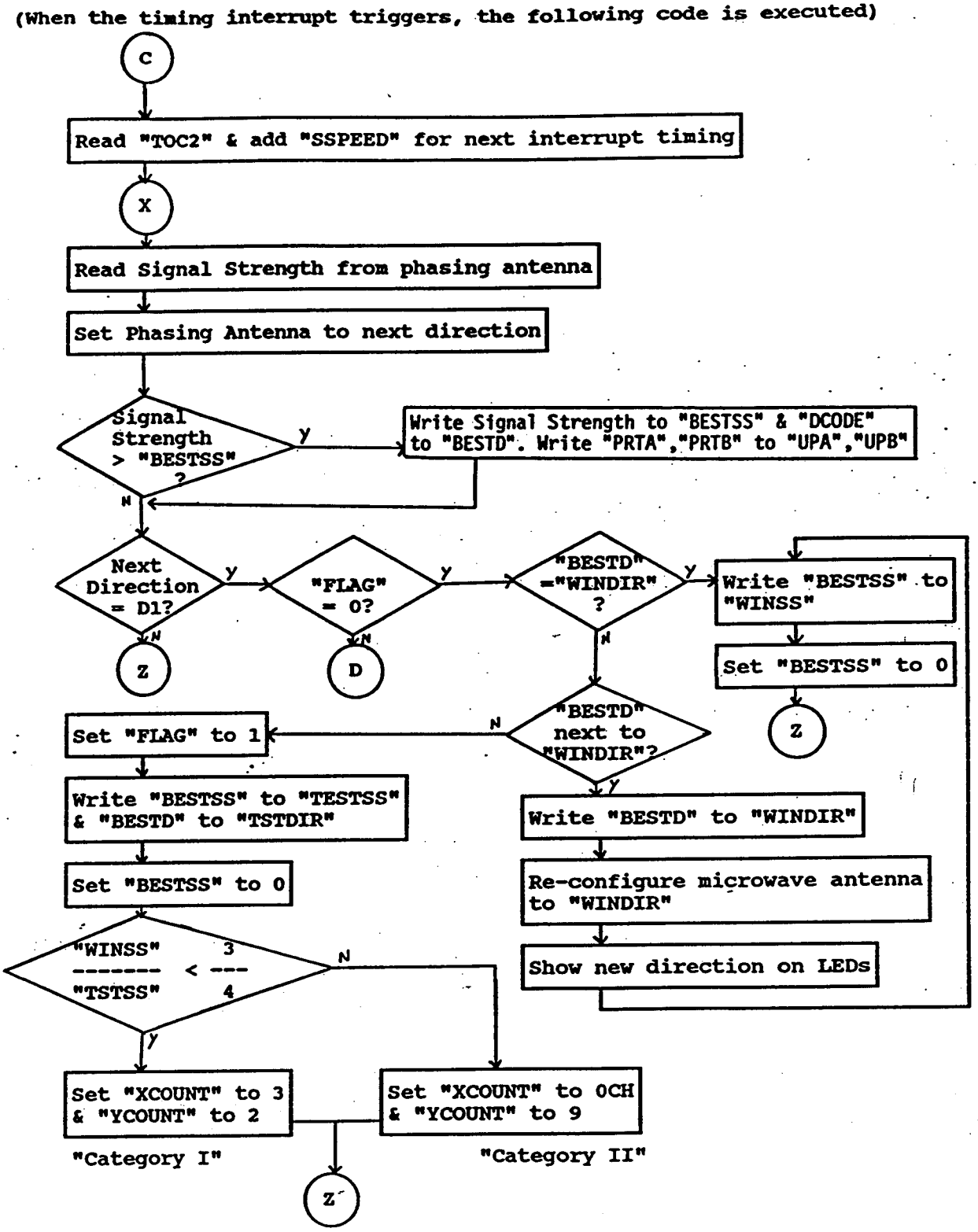


FIGURE 32b
FLOW CHART OF MAIN PROGRAM

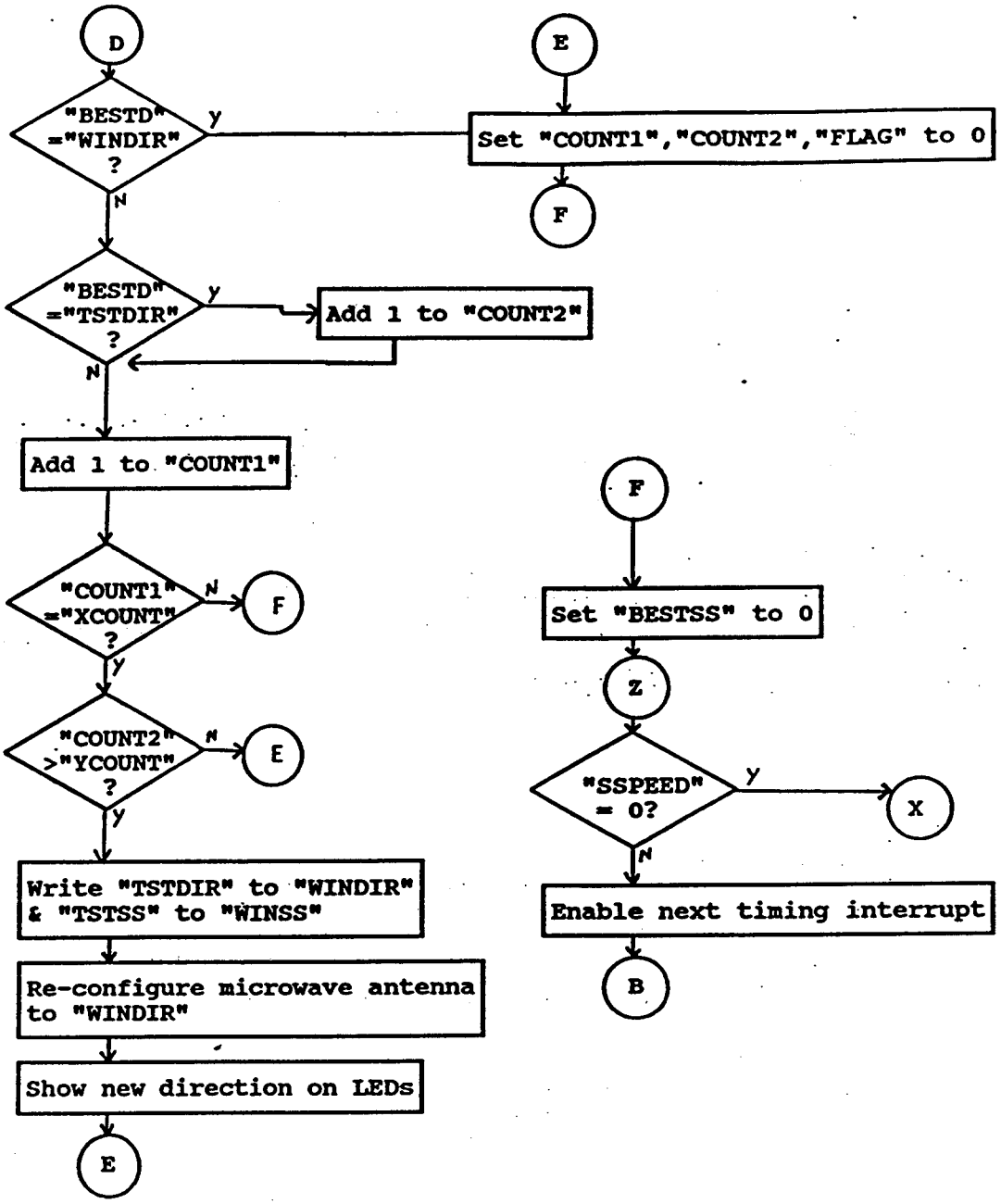


FIGURE 32c
FLOW CHART OF MAIN PROGRAM

V.C.2. EXPLANATION

The main program TACMAIN is an assembly language program and is the "normal operation" program. It is run when the DIP switch #1 is in the OFF position as detailed in Section V.B.1.

The main program directs the ESABA system to sample the VHF signal strength in each of eight sectors. The microwave video channels are then directed out of the appropriate helical antenna based upon these signal strength readings. See the system block diagram in Section I.C.

The main program could be made to be comparatively simple...it could always direct the video channel to the sector with the strongest received VHF signal. In an environment with significant multipathing, however, this could lead to undesirable and rapid switching of the microwave signal. The maximum rate of rotation of the vehicle should be considered before "skipping sectors" and routing the video signal in a radically different direction. Since each VHF and video sector is 45 degrees wide, we define "skipping a sector" as any switch in which the new direction is 90 degrees or more from the currently active direction.

The switching strategies for configuring the microwave antenna have been divided into two cases :

CASE 1 : The VHF signal strength is strongest in the currently active sector, or in one of the two sectors adjacent to the currently active sector.

The "currently active sector" is the sector in which the microwave antenna is currently configured. It is to be expected that vehicle rotations will cause one of the antennas adjacent to the currently active sector to become the "best" sector to transmit the video signal. Therefore, in the situation of Case 1 the microwave antenna sector used will be dictated by the direction of the strongest signal received on the VHF link.

CASE 2 : The new VHF signal strength reading shows a "skipped sector", in that the VHF signal strength reading is in a sector which is not the currently active sector nor one of the sectors adjacent to the currently active sector.

The software has been designed to guard against skipping sectors. It is not possible for the vehicle to turn fast enough that an entire sector has been skipped since the last signal strength sampling. However, the ESABA system cannot endlessly refuse to acknowledge that the best VHF signal is in a radically new direction. It

would also seem that the actions of the ESABA system should differ depending upon whether the signal strength in the radically new direction is much stronger, or only slightly stronger, than the signal strength in the currently active sector.

Case 2 therefore has been further subdivided into two categories in the software :

CASE 2, CATEGORY 1 : The new direction of the VHF signal is much stronger than the signal strength of the currently active sector.
Note : "much stronger" is here defined as when SS_o / SS_n < .75, where SS_o is the "original" signal strength in the currently active sector and SS_n is the signal strength in the new or latest sector.

ACTION OF THE ESABA SYSTEM IN CASE 2, CATEGORY 1 :
Scan all directions three times. If all three scans agree that the new direction is correct, then configure the microwave antenna to the new sector. If all three scans do not agree on a single sector, then the microwave antenna is not reconfigured.

CASE 2, CATEGORY 2 : The new direction of the VHF signal is slightly stronger than the signal strength of the currently active sector.
Note : "slightly stronger" is here defined as when SS_o / SS_n > .75.

ACTION OF THE ESABA SYSTEM IN CASE 2, CATEGORY 2 :
Scan all directions twelve times. If the new direction is repeated 10 out of 12 times, then reconfigure the microwave antenna to the new direction.

V.C.3. MAIN PROGRAM CODE LISTING

The main program code listing is included in Appendix IX.A.

V.D. FORTH MONITOR AND SYSTEM TEST AIDS

V.D.1. OPERATION

The setting of DIP switch #1 on the microcontroller board determines whether the ESABA system boots up into its "normal" operation or into the Forth monitor. In "normal" operation the ESABA begins execution of the assembly language program which scans the VHF sectors and configures the microwave link

to the appropriate antenna. However, the Forth monitor included with the system provides a convenient means to debug and test the ESABA system, as well as provide manual control of ESABA operation.

If DIP switch #1 is set to "on" and the system turned on or reset, the ESABA system comes up into the Forth monitor. At this point a terminal connected to the microcontroller RS232 port has access to many Forth words.

V.D.2. FORTH WORDS

FORTH WORDS PROVIDING MANUAL CONTROL OF THE ESABA SYSTEM

D1P	Set VHF phased antennas to direction 1
D2P	Set VHF phased antennas to direction 2
D3P	Set VHF phased antennas to direction 3
D4P	Set VHF phased antennas to direction 4
D5P	Set VHF phased antennas to direction 5
D6P	Set VHF phased antennas to direction 6
D7P	Set VHF phased antennas to direction 7
D8P	Set VHF phased antennas to direction 8
D1M	Set microwave antennas to direction 1
D2M	Set microwave antennas to direction 2
D3M	Set microwave antennas to direction 3
D4M	Set microwave antennas to direction 4
D5M	Set microwave antennas to direction 5
D6M	Set microwave antennas to direction 6
D7M	Set microwave antennas to direction 7
D8M	Set microwave antennas to direction 8

FORTH WORDS PROVIDING DEBUG AND TEST FUNCTIONS FOR THE ESABA SYSTEM

SCANALL	This word shows the A/D reading for all eight VHF sectors.
SCANDIR	This word returns "D1" if this sector has the strongest VHF signal, etc.
Q	Returns "D1=" and then this sector A/D readings until another key is pressed.
W	Returns "D2=" and then this sector A/D readings until another key is pressed.
E	Returns "D3=" and then this sector A/D readings until another key is pressed.
R	Returns "D4=" and then this sector A/D readings until another key is pressed.
T	Returns "D5=" and then this sector A/D readings until another key is pressed.
Y	Returns "D6=" and then this sector A/D readings until another key is pressed.

U — Returns "D7=" and then this sector A/D readings until another key is pressed.

I — Returns "D8=" and then this sector A/D readings until another key is pressed.

SCANNING — This Forth word is a simplified Forth version of the "normal" operation main program. It will cause the ESABA system to scan the signal strength in each of the eight VHF sectors and configure the microwave antenna according to the winning sector. Additionally, it will drive the LED's on the optional debugging module so as to indicate the current microwave antenna sector. The scan speed in this mode can be easily changed by writing different values to the Forth variable DEL-VAR.

V.D.2. FORTH PROGRAM LISTING

The Forth program listing is included in Appendix IX.B.

VI. POWER MODULE

VI.A. POWER REQUIREMENTS

The power available to the ESABA system is 24 to 32 volts DC (28 volts nominal).

The power requirements of the ESABA system are as follows:

MICROWAVE SWITCH / MICROWAVE SWITCH DRIVER :

PIN diodes positive biased : Eleven out of fourteen channels on at a time, 150 mA per channel = 1.65 amps, +12 VDC, = 19.8 watts.

Pin diodes negative biased : Three out of fourteen channels negative biased at a time, 50 mA per channel (through DH0035 devices), = 150 mA, -12 VDC, = 1.8 watts.

VHF PHASING BOARD / PHASING BOARD DRIVER :

PIN diodes positive biased : Five out of twelve channels on at a time, 100 mA per channel = 0.5 amps, +12 VDC, = 6 watts.

Pin diodes negative biased : Seven out of twelve channels negative biased at a time. Since the current path is through the PIN diodes, power is consumed only during the switching transients.

MICROCONTROLLER BOARD

Approximately 100 mA at 12 VDC = 1.2 watts.

(The microcontroller board generates its own minus voltages)

RADIO

Approximately 500 mA at 12 VDC = 6 watts.

FAN

Approximately 220 mA at 24 VDC = 5.3 watts.

POWER TOTALS : >>>>>>>>>>>>

+12 VDC .....2.75 amps
-12 VDC .....150 mA
+24 VDC .....220 mA

The power in is 28 VDC nominal (24 to 32 volts). The +12 VDC and -12 VDC are generated by the DC to DC converters in the ESABA power module, while the +24 VDC needed by the fan is produced by a voltage regulator.

The power consumed is 40.1 watts. (2.9 * 12 + 0.22 * 24 = 40.1)

The +28 VDC current and power required is then 1.77 amps

and 49.6 watts.

[CALCULATIONS....
The +12 and -12 VDC current totals 2.9 amps and 34.8 watts. With 80% efficiency in the DC to DC converters this translates to 1.55 amps of +28 VDC (43.5 watts).

The +24 VDC current totals 0.22 amp. Since this voltage is generated by a voltage regulator this translates to 0.22 amps of +28 VDC (6.2 watts).

TOTAL +28 VDC CURRENT NEEDED IS 1.55 + 0.22 = 1.77 amps
TOTAL +28 VDC POWER REQUIRED IS 43.5 + 6.2 = 49.7 watts.]

The measured power consumption by the ESABA unit was slightly lower than the calculated value above. The measured current using 24 VDC was 1.3 amps or 31.2 watts.

VI.B. POWER MODULE SPECIFICATIONS

The power module is made up of two DC to DC converters and one voltage regulator :

WESTCOR VI-121 DC to DC Converter
Input voltage range : 20 to 56 VDC
Output voltage and current : +12 VDC , 4.16 amp
Operating temperature range : -40^{o} to 85^{o} C

The modules in the ESABA system powered by the Westcor VI-121 are :
(1) +12 VDC to microwave switch driver board
(2) +12 VDC to phasing board driver

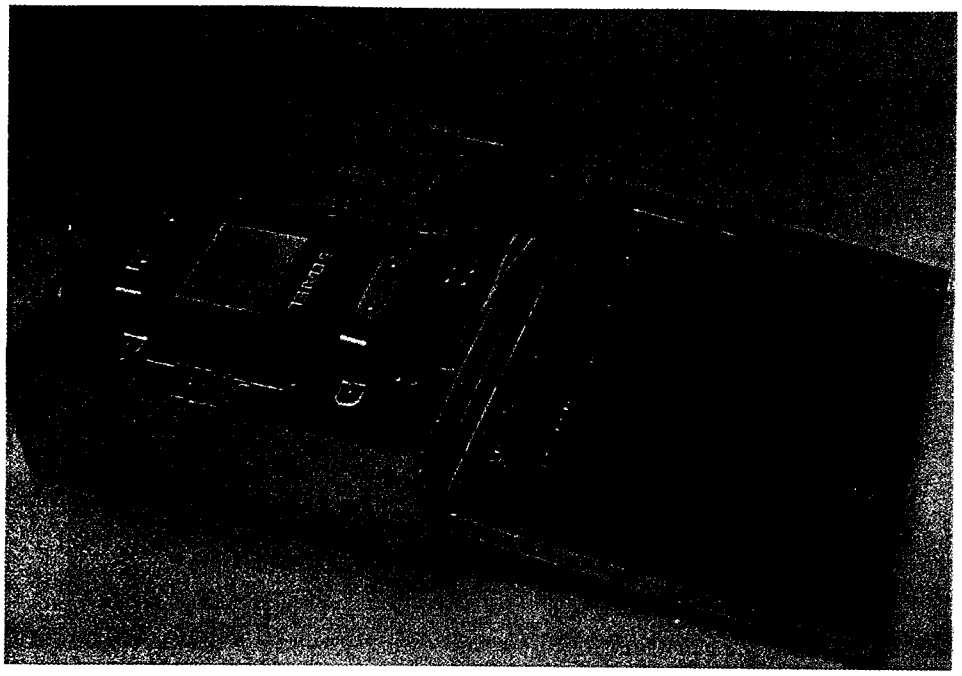
DATEL BPS-12/1250-D24 DC to DC Converter
Input voltage range : 18 to 36 VDC
Output voltage and current : +12 VDC , 1.25 amp ,
: -12 VDC , 1.25 amp
Operating temperature range : -25^{o} to 71^{o} C

The modules in the ESABA system powered by the Datel BPS-12/1250-D24 are :
(1) +12 VDC to microcontroller board
(2) +12 VDC to radio
(3) -12 VDC to microwave switch driver board
(4) -12 VDC to phasing board driver

TEXAS INSTRUMENTS 7824 Voltage Regulator

The only module in the ESABA system powered by the TI 7824 is the fan.

VI.C. POWER MODULE PICTURE



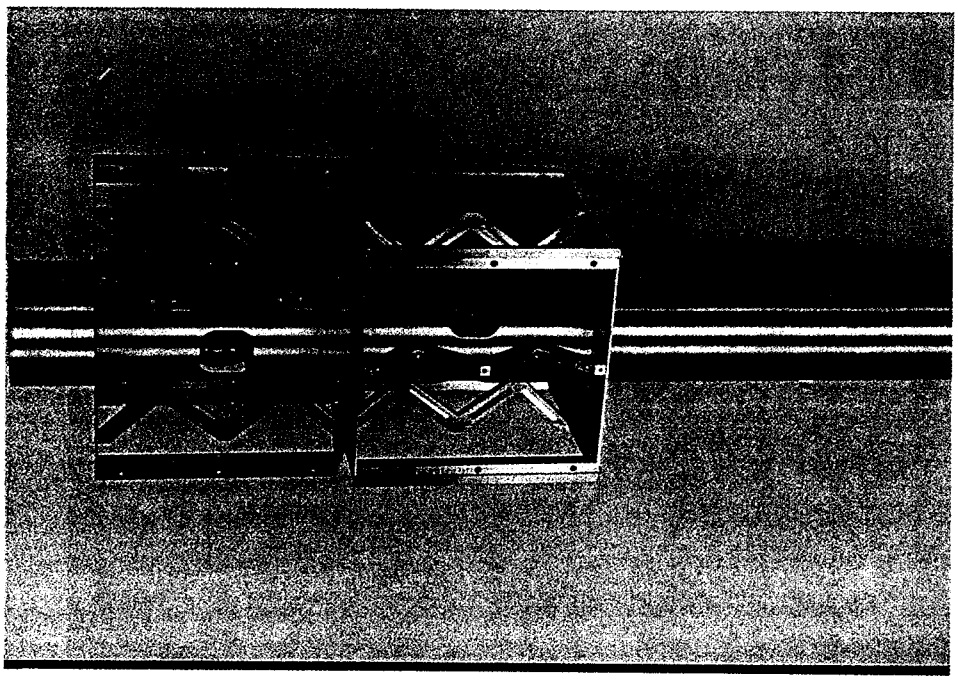
PHOTOGRAPH 9
POWER MODULE

VII. MAST AND DOME STRUCTURE

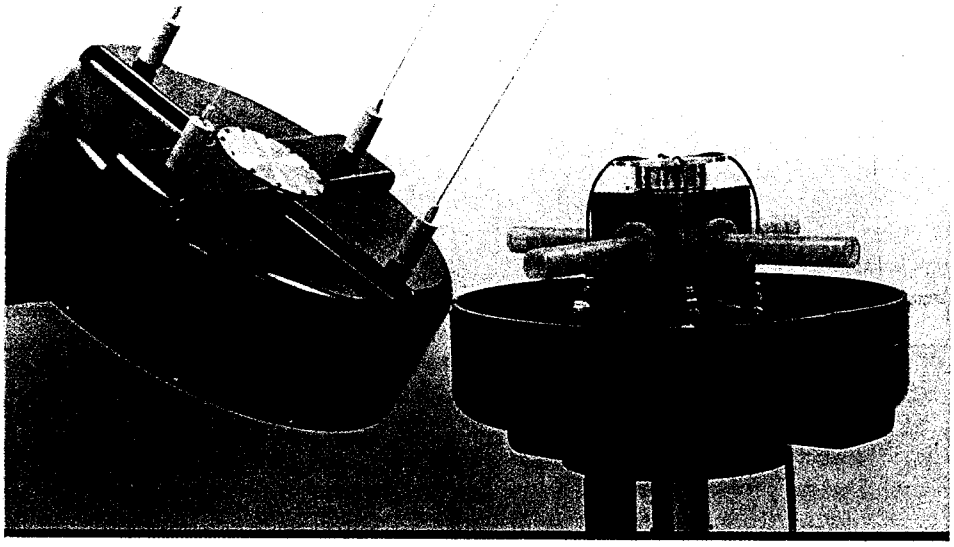
VII.A. MAST AND DOME STRUCTURE

The mast support for the helical antennas, dome, and whip antennas was constructed in two pieces for ease of installation and easy modification of the height of the dome.

The inner structure of the upper mast is shown in Photograph 10. A view of the finished dome is shown in Photograph 11. A six foot section of 3" O.D. pipe machined to fit into the upper mast assembly is included with each prototype. This six foot section can be cut to size and mounted on the test vehicle by TACOM. The upper mast assembly and dome can then be attached to this section with four bolts. See the Operations Manual for further details.



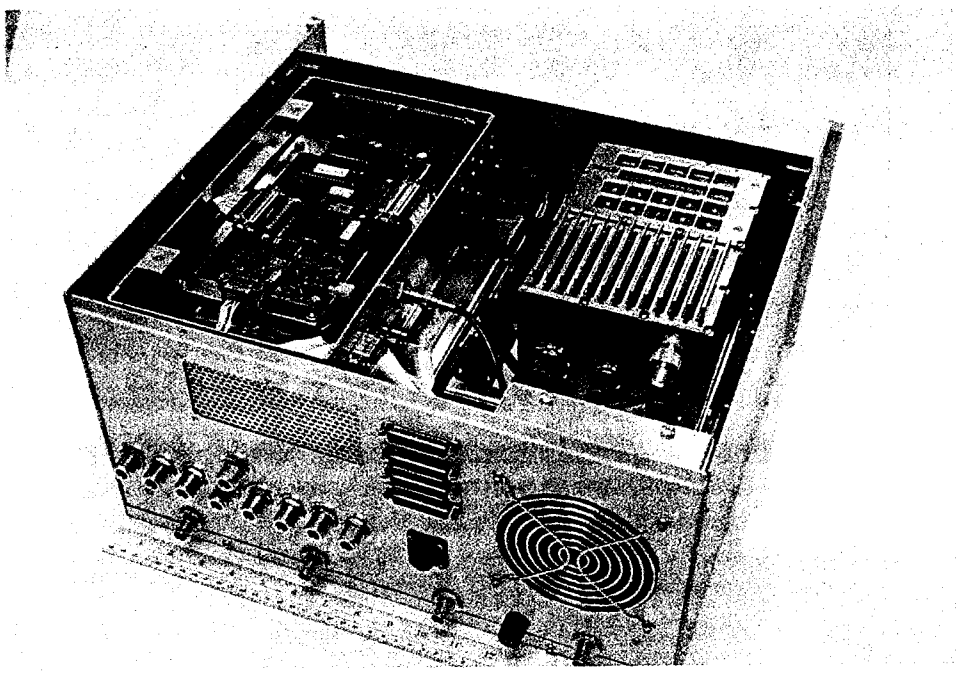
PHOTOGRAPH 10
INNER STRUCTURE OF THE UPPER MAST



PHOTOGRAPH 11
DOME ENCLOSURE

VII.B. 19" RACK SYSTEM ENCLOSURE

A photograph of the 19" rack enclosure housing the ESABA electronics is shown in Photograph 12.



PHOTOGRAPH 12
19" RACK ENCLOSURE

VIII. SYSTEM PERFORMANCE

VIII.A. SYSTEM PERFORMANCE AND THE REQUIREMENTS OF THE CONTRACT

The ESABA system meets the performance criteria set forth in the contract.

VIII.B. SYSTEM PERFORMANCE AND AREAS OF FUTURE IMPROVEMENT

There are areas which can be improved upon in any successive versions of ESABA. These include :

(1) The insertion loss of the microwave PIN switch can likely be improved from its present 4 dB. Since the 40% bandwidth called for in the contract is very wide, it is possible that a better switch could be designed by using two switches, one for the high band and one for the low band. If TACOM requests additional ESABA units, TRA will also reexamine the commercial market. It is possible that recent developments in commercial switches would allow a commercial switch to be used.

(2) It might be advisable to include a stepped attenuator which can be controlled by the system microcontroller in a successive version of ESABA. TRA's field testing showed that a very strong VHF signal could "swamp" all sectors of the phased array, and that adding an RF attenuator could then allow the VHF phased array to identify the direction of the transmitter. Since TRA could not test the behavior of the microwave signal in the field, it is not clear if the microwave antennas would be similarly "swamped". Field tests with a microwave transmitter / receiver in place will need to be done to answer this question.

(3) The insertion loss through the PIN switch is about 4 dB. This loss cancels most of the 5 to 6 dB gain of the phased array antenna. A LNA can be easily and inexpensively added in series with the VHF receiver if additional gain is required.

(4) As discussed in Section III.B.1 adding the capability of switching polarization at the RCC will allow the ESABA unit to take advantage of reflected signals. Without switchable polarization it is possible that the VHF phased array will try to use a strong reflected signal and direct the microwave signal inappropriately in some instances.

(5) A manual over-ride feature could be easily added to a future version of ESABA to allow the RCC direct control over the sector in which the microwave signal is transmitted.

(6) Potentially, the ESABA can interface with the inertial guidance computer on board a RCV and use that information to control the video link.

IX. APPENDICES

IX.A. MAIN PROGRAM CODE LISTING

TACMAIN5.DOC (10\24\89)

** The EPROM labeled "TACMAIN5" has burned into it four programs as follows:
- TACOMxx.HEX : C000H - CDFFH
- TACOMxxR.HEX : CF00H - CFFFH
- TACMAIN5.HEX : D000H - D4FFH
- MNTR-2-3.HEX : E000H - FFFFH

Adapt following vectors:
- RESET
- TOC2
- CLOCK TIMER
- COP MONITOR

** The TACMAIN5.ASM will read the dip switch upon a reset or a powering up of the board and do the following:

DIPs#	STATUS	ACTION TAKEN
1	on	Load Forth Monitor and TACOMxx.
1	off	Scan at assembly language speed.
2	on	Use uwave switch box #1 antenna settings.
2	off	Use uwave switch box #2 antenna settings.
3 4 5	on on on	A complete scan at a speed of 4Hz.
3 4 5	on on off	" " " " " of 25Hz.
3 4 5	on off on	" " " " " of 50Hz.
3 4 5	on off off	" " " " " of 100Hz.
3 4 5	off on on	" " " " " of 250Hz.
3 4 5	off on off	" " " " " of 750Hz.
3 4 5	off off on	" " " " " of 1500Hz.
3 4 5	off off off	" " " " " of about 2500Hz.

** U3 socket will have a CPU. It is an MC/XC68HC11A1.
** U13 socket will have a 6264ASP RAM. (8000H - 9FFFH)
** U8 socket will have a 62256 RAM. (0100H - 7FFFH)
** U7 socket will have a 27C128 EPROM labeled "TACMAIN5". (C000H - FFFFH)
** The clock monitor and cop timer are enabled. If the system clock stops working or the program is corrupted, the system will reboot itself. The cop timer will function only if the CPU is marked as having an active cop timer.

```
*********************************************************************
* TACMAIN5.ASM   ( Tacom assembly language main program )           *
* October 26, 1989              ( FOR NEW BOARDS  REV 2.0 )         *
* the cop timer is reloaded periodically                            *
* antenna scanning test routines; scan speed is user-set            *
* each sector/direction is scanned at a user-set speed              *
* Vectors to set: TOC2, COP Monitor, Clock Monitor, & RST           *
* TOC2:FFE6,7/COP  Monitor:FFFA,B/Clock Monitor:FFFC,D/RST:FFFE,F   *
* D1 = ANTENNA #1. D2 = BETWEEN ANTENNA #1 & #2. D3...D8 = CW       *
*********************************************************************

*****EQUATES *****
* 65C22 PORT ADDRESSES
REGB    EQU     $A000   ;PORTB I/O.
REGA    EQU     $A001   ;PORTA I/O.
DDRB    EQU     $A002   ;PORTB I/O CONTROL REGISTER.
DDRA    EQU     $A003   ;PORTA I/O CONTROL REGISTER.

* 68HC11 ADDRESSES
PORTA   EQU     $B000   ;PORTA.
PORTD   EQU     $B008   ;PORTD.
DDRD    EQU     $B009   ;PORTD CONTROL REGISTER.
PORTE   EQU     $B00A   ;PORTE.

* TIMER OUTPUT CAPTURE REGISTERS
TOC2    EQU     $B018   ;TIMER OUTPUT CAPTURE REGISTER 2.
TCTL1   EQU     $B020   ;TIMER CONTROL REGISTER 1.
TMSK1   EQU     $B022   ;TIMER INTERRUPT MASK REGISTER 1.
TFLG1   EQU     $B023   ;TIMER INTERRUPT FLAG REGISTER 1.
TMSK2   EQU     $B024   ;TIMER INTERRUPT MASK REGISTER 2.

* SERIAL PERIPHERAL INTERFACE REGISTERS
SPCR    EQU     $B028   ;SPI CONDITION REGISTER.
SPSR    EQU     $B029   ;SPI STATUS REGISTER.
SPDR    EQU     $B02A   ;SPI DATA REGISTER.

* MISCELLANEOUS ADDRESSES
CHIPRAM EQU     $0000   ;ON CHIP RAM OF 256 BYTES.
INITR   EQU     $103D   ;INIT REGISTER.
OPTION  EQU     $B039   ;A/D CONTROL & CLOCK MONITOR.
COPRST  EQU     $B03A   ;COP TIMER REGISTER.
RSTVEC  EQU     $FEC0   ;START OF NORMAL RESET VECTOR (FORTH).

* PATTERNS FOR PHASED ARRAY ANTENNA DIRECTIONS
PAD1    EQU     $99     ;PHASED ANTENNA PORT A D1.
PAD2    EQU     $A9
PAD3    EQU     $69
PAD4    EQU     $6A
PAD5    EQU     $66
PAD6    EQU     $A6
PAD7    EQU     $96
PAD8    EQU     $9A
PBD1    EQU     $06     ;PHASED ANTENNA PORT B D1.
PBD2    EQU     $0A
PBD3    EQU     $09
PBD4    EQU     $09
PBD5    EQU     $09
PBD6    EQU     $0A
PBD7    EQU     $06
PBD8    EQU     $06

* PATTERNS FOR MICROWAVE ANTENNA DIRECTIONS
MAD11   EQU     $16     ;MICRO WAVE PORT A D1; SWITCH #1.
MAD12   EQU     $13     ;MICRO WAVE PORT A D2; SWITCH #2.
MAD21   EQU     $13     ;SWITCH #1.
MAD22   EQU     $16     ;SWITCH #2.
MAD3    EQU     $20
MAD4    EQU     $20
MAD5    EQU     $68
MAD6    EQU     $E0
MAD7    EQU     $10
MAD8    EQU     $10
MBD1    EQU     $00     ;MICRO WAVE PORT B D1.
MBD2    EQU     $00
MBD3    EQU     $30
MBD4    EQU     $18
MBD5    EQU     $00
MBD6    EQU     $00
MBD7    EQU     $06
MBD8    EQU     $03

* VARIOUS DATA BYTES FOR STORAGE
DIPDAT  EQU     $9FC0   ;DIP DATA.
BESTSS  EQU     $9FC1   ;STORE BEST SIGNAL STRENGTH.
BESTD   EQU     $9FC3   ;STORE BEST DIRECTION.
ADDATA  EQU     $9FC4   ;A/D DATA STORED HERE.
DCODE   EQU     $9FC6   ;DIRECTION CODE.
PRTA    EQU     $9FC7   ;USED BY ASSEMBLY LANGUAGE FOR STORAGE OF PORTB.
PRTB    EQU     $9FC8   ;USED BY ASSEMBLY LANGUAGE FOR STORAGE OF PORTB.
TEMPY   EQU     $9FC9   ;TEMPORARY BYTE FOR STORAGE OF ANYTHING.
WINDIR  EQU     $9FCB   ;DIRECTION OF STRONGEST SIGNAL.
WINSS   EQU     $9FCC   ;STRENGTH SIGNAL OF STRONGEST SIGNAL.
TSTDIR  EQU     $9FCE   ;TEMPORARY STRONGEST DIRECTION.
TSTSS   EQU     $9FCF   ;TEMPORARY STRONGEST SIGNAL STRENGTH.
```

```
COUNT1   EQU      $9FD1    ;TEMPORARY COUNTER 1.
COUNT2   EQU      $9FD2    ;TEMPORARY COUNTER 2.
FLAG     EQU      $9FD3    ;FLAG TO SHOW KIND OF SCANNING ROUTINES.
XCOUNT   EQU      $9FD4    ;INSIDE COUNTER.
YCOUNT   EQU      $9FD5    ;OUTSIDE COUNTER.
UPA      EQU      $9FD6    ;STORE UWAVE ANTENNA PARAMTER FOR PORTA.
UPB      EQU      $9FD7    ;STORE UWAVE ANTENNA PARAMTER FOR PORTB.
DIP2     EQU      $9FD8    ;STORE DIP#2 STATUS.
SSPEED   EQU      $9FD9    ;SPEED OF SCANNING.
DCODEN   EQU      $9FDB    ;STORE NEW DIRECTION CODE.
TEMPP    EQU      $9FDC
TEMPPP   EQU      $9FDD

TOUCH    EQU      $9FDF

         ORG $2000

*****BASIC INITIALIZATIONS *****
START    LDS #$FF ;LOAD STACK POINTER WITH $FF.
         LDAA #$0B
         STAA INITR          ;SET UP SYSTEM SO ON-CHIP RAM IS AT
                             ;$0000 AND 64 REGISTERS IS AT $8000.
         LDAA #$80;POWER ON THE A/D AND CLOCK MONITOR.
         STAA OPTION         ;INITIALIZE SYSTEM.
         LDAA #$00
         STAA TMSK2          ;SET PRESCALER AT 1 FOR OUTPUT CAPTURE TIMING.
         STAA TCTL1          ;SET UP OC2 TO LEAVE 68HC11 OUTPUTS PA ALONE.
         JSR STRTUP          ;INIT ALL PORTS, A/D,.
         LDAA #PAD2          ;LOAD REG A WITH PATTERN FOR PORTA D2.
         STAA PRTA           ;STORE IT IN PRTA.
         LDAA #PBD2          ;LOAD REG B WITH PATTERN FOR PORTB D2.
         STAA PRTB           ;STORE IT IN PRTB.
         JSR SENDPA          ;CALL SUBROUTINE SENDPA TO SET PHASED ANTENNA.
         JSR READIP          ;GET STATUS OF DIP #2.
         ANDA #$40
         CMPA #$40           ;IF DIP2 IS OFF, GOTO GOON.
         BEQ SW2N
         LDAA #MAD21
         JMP GOON
SW2N     LDAA #MAD22
GOON     STAA UPA ;STORE IT IN UPA.
         LDAA #MBD2          ;LOAD REG B WITH UWAVE PATTERN FOR PORTB D2.
         STAA UPB ;STORE IT IN UPB.
         JSR SENDUA          ;SET UWAVE ANTENNA FOR D2.

* DEBUGGING ROUTINE HERE *
         LDAA #$00
         STAA TEMPP
         STAA TEMPPP
         JMP ALSCAN          ;TEMPORARY DEBUGGING INSERTION.

*****READ DIP SWITCH AND SELECT PROGRAM TO RUN *****
;SELPRO  JSR READIP
;        LDAA DIPDAT         ;PUT DIP DATA IN REG A.
;        ANDA #$80           ;"AND" IT TO GET BIT 7 (DIP #1).
;        CMPA #$00           ;IS IT ON ?
;        BEQ LOADTM          ;YES - GOTO LOAD TACOM AND THEN FORTH MONITOR.
;        JMP ALSCAN          ;NO - GOTO ASSEMBLY LANGUAGE SCANNING.
;        JMP SELPRO

*****LOAD THE TACOM PROGRAM BEFORE LOADING THE FORTH MONITOR *****
* COPY ROM'S CONTENTS (TACOMXXR.HEX) TO ON-CHIP RAM *
;LOADTM  LDY #CHIPRAM        ;LOAD RAM POINTER WITH 0000H.
;        LDX #$CF00          ;LOAD REG X WITH 256B-RAM ADDRESS IN ROM.
;LOOP2   LDD X
;        STD Y
;        INX
;        INX
;        INY
;        INY
;        CPX #$D000          ;IS ROM POINTER D000H ?
;        BEQ CONT4           ;NO - GOTO LOOP2. YES - GOTO CONT4.
;        JMP LOOP2
;CONT4   JMP RSTVEC          ;GOTO NORMAL FORTH RESET.

*****ASSEMBLY INITIALIZATIONS *****
ALSCAN   LDAA #$00
         STAA FLAG           ;SHOW CONDITION OF SCAN ROUTINES.
         STAA COUNT1
         STAA COUNT2         ;SET BOTH COUNTERS TO ZERO.
         LDAA #$02
         STAA WINDIR         ;STORE 0000 0010 AS DIRECTION CODE FOR D2.
         STAA DCODEN
         STAA BESTD
         JSR SENDLED         ;LIGHT UP THE D2 LED.
         LDD #$0000
         STD WINSS           ;SET WINSS AT ZERO. (SIGNAL STRENGTH = 0.)
         STD BESTSS          ;DO THE SAME FOR BESTD.
         JSR READIP
         LDAA DIPDAT
         ANDA #$40
         STAA DIP2 ;STORE STATUS OF DIP#2 IN DIP2.
         JSR SETSS           ;READ DIP #3-5 AND DETERMINE SCAN SPEED.
         LDD SSPEED
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        CPD #$0000          ;ARE DIPS #3-5 OFF?
        BNE ENINTS          ;NO - ENABLE INTERRUPT TIMING.
        JMP BYPASS          ;YES - BYPASS INTERRUPT TIMING.
ENINTS  LDAA #$40
        STAA TFLG1          ;CLEAR POSSIBLE PENDING OC2F INTERRUPTS.
        STAA TMSK1          ;ENABLE OUTPUT CAPTURE TIMING INTERRUPT.
        CLI                 ;ENABLE INTERRUPT CAPABILITY OF SYSTEM.
LOOPY   NOP
        NOP
        NOP
        NOP
        JMP LOOPY           ;WAIT FOR INTERRUPT.


        ORG $3000

STINT   LDD TOC2 ;READ IN TOC2 INTO REG D.
        ADDD SSPEED         ;ADD SSPEED FOR NEXT INTERRUPT TIMING.
        STD TOC2 ;STORE NEW VALUE FOR NEXT INTERRUPT.

BYPASS
* DEBUGGIN ROUTINE HERE
        LDAA WINSS
        CPD #$00FF
        BNE HAHA
        LDD #$0000
        STD WINSS
HAHA
* END OF DEBUGGING ROUTINE *
        LDAA DCODEN
        STAA DCODE
        JSR READAD          ;GET SIGNAL STRENGTH OF PRESENT DIRECTION IN REG D.
        STD TEMPY           ;STORE TEMPORARILY IN TEMPY.
        LDAA DCODE
        LSLA                ;SHIFT DIRECTION CODE LEFT FOR NEXT DIRECTION TO SCAN.
        BCC LP10 ;WAS PREVIOUS BIT 7 A 1?
        ORAA #$01;YES - SET BIT 0 TO 1. NO - GO ON.
LP10    STAA DCODEN         ;STORE NEW DIRECTION IN DCODEN.
        CMPA #$01
        BEQ SCAND1          ;NEW DIRECTION D1?
        CMPA #$02
        BEQ SCAND2          ;D2?
        CMPA #$04
        BEQ SCAND3          ;D3?
        CMPA #$08
        BEQ SCAND4          ;D4?
        CMPA #$10
        BEQ SCAND5          ;D5?
        CMPA #$20
        BEQ SCAND6          ;D6?
        CMPA #$40
        BEQ SCAND7          ;D7?
        CMPA #$80
        BEQ SCAND8          ;D8?
        JMP STOPIT          ;CORRUPTED DCODE.
SCAND1  LDAA DIP2
        CMPA #$40           ;IF DIP2 IS ON, GOTO SW2ON1.
        BEQ SW2ON1          ;IF DIP2 IS OFF, GOTO SW2OF1.
SW2OF1  JMP Q12
SW2ON1  JMP Q11
SCAND2  LDAA DIP2
        CMPA #$40           ;IF DIP2 IS ON, GOTO SW2ON2.
        BEQ SW2ON2          ;IF DIP2 IS OFF, GOTO SW2OF2.
SW2OF2  JMP Q22
SW2ON2  JMP Q21
SCAND3  JMP Q3
SCAND4  JMP Q4
SCAND5  JMP Q5
SCAND6  JMP Q6
SCAND7  JMP Q7
SCAND8  JMP Q8

TESTSS  LDD TEMPY           ;GET NEW SIGNAL STRENGTH IN REG D.
        CPD BESTSS          ;IS NEW SS HIGHER THAN BESTSS?
        BLS LP11 ;NO - GOTO LP11. YES - INSERT NEW SS IN BESTSS.
        STD BESTSS
        LDAA DCODE
        STAA BESTD          ;STORE DIRECTION CODE IN BESTD.
        JSR LOADUA          ;STORE NEW UWAVE ANTENNA SETTINGS IN UPA,B.
LP11    LDAA DCODEN
        CMPA #$01           ;IS DCODEN SET FOR D1?
        BEQ TSTFLG
        JMP ENABI           ;ENABLE NEXT INTERRUPT.
TSTFLG  LDAA TEMPP
        CMPA #$00
        BEQ TEM0
        CMPA #$01
        BEQ TEM1
        CMPA #$02
        BEQ TEM2
        CMPA #$03
        BEQ TEM3
        CMPA #$04
        BEQ TEM4
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            CMPA #$05
            BEQ  TEM5
            CMPA #$06
            BEQ  TEM6
            CMPA #$07
            BEQ  TEM7
            CMPA #$08
            BEQ  TEM8
            CMPA #$09
            BEQ  TEM9
            CMPA #$0A
            BEQ  TEMA
            CMPA #$0B
            BEQ  TEMB
TEM0        LDAA #$01
            STAA TEMPP
            JMP CONTT
TEM1        LDAA #$02
            STAA TEMPP
            JMP CONTT
TEM2        LDAA #$03
            STAA TEMPP
            JMP CONTT
TEM3        LDAA #$04
            STAA TEMPP
            JMP CONTT
TEM4        LDAA #$05
            STAA TEMPP
            JMP CONTT
TEM5        LDAA #$06
            STAA TEMPP
            JMP CONTT
TEM6        LDAA #$07
            STAA TEMPP
            JMP CONTT
TEM7        LDAA #$08
            STAA TEMPP
            JMP CONTT
TEM8        LDAA #$09
            STAA TEMPP
            JMP CONTT
TEM9        LDAA #$0A
            STAA TEMPP
            JMP CONTT
TEMA        LDAA #$0B
            STAA TEMPP
            JMP CONTT
TEMB        LDAA #$00
            STAA TEMPP
            JMP CONTT
CONTT

            LDAA FLAG
            CMPA #$00           ;IS FLAG CLEAR?
            BEQ  FLGCLR         ;YES - GOTO FLGCLR ROUTINE.
            JMP FLGSET          ;NO - GOTO FLGSET AND TEST FOR STRONGEST DIRECTION.
FLGCLR      LDAA WINDIR
            CMPA BESTD          ;IS BESTD SAME DIRECTION CODE AS WINDIR?
            BNE NXTST1          ;NO - TRY NEXT TEST.
            LDD BESTSS
            STD WINSS           ;YES - PUT NEW SS IN WINSS.
            LDD #$0000
            STD BESTSS          ;STORE ZERO IN BESTSS.
            JMP ENABI
; ROTATE BESTDR ONCE IN BOTH DIRECTIONS AND COMPARE WITH WINDIR.
NXTST1      LDAB BESTD          ;PUT BESTD IN REG B.
            CLC                 ;CLEAR CARRY FLAG.
            ROLB                ;ROTATE REG B LEFT ONCE.
            BCC TST1 ;CARRY FLAG CLEAR? YES - GOTO TST1. NO - GO ON.
            ORAB #$01           ;PUT A 1 IN BIT 0.
TST1        CBA                 ;IS NEW DIRECTION CODE IN B EQUAL TO WINDIR IN REG A?
            BNE TST2 ;NO - GOTO TST2. YES - GO ON.
            JSR NEWDIR          ;SET UWAVE ANTENNA AND NEWxxx PARAMETERS.
            JMP ENABI
TST2        LDAB BESTD          ;PUT BESTD IN REG B.
            CLC
            RORB
            BCC TST3
            ORAB #$80           ;PUT A 1 IN BIT 7.
TST3        CBA                 ;IS NEW DIRECTION CODE IN B EQUAL TO WINDIR IN REG A?
            BNE SETFLG          ;NO - GOTO SETFLG. YES - GO ON.

            JSR NEWDIR          ;SET UWAVE ANTENNA AND NEWXXX PARAMATERS.
            JMP ENABI
SETFLG      LDAA #$01
            STAA FLAG           ;SET FLAG TO SHOW CATEGORY 1/2 TESTING.
            LDAA BESTD
            STAA TSTDIR         ;GET BESTDR AND STORE IN TSTDIR.
            LDD BESTSS
            STD TSTSS           ;GET BESTSS AND STORE IN TSTSS.
            LDD #$0000
            STD BESTSS          ;SET BESTSS TO ZERO.
            LDD TSTSS           ;GET TSTSS IN REG D FOR ARITHMETIC OPERATION.
            LSRD                ;SHIFT REG D RIGHT TWICE.
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          LSRD
          STAB TEMPY+1        ;STORE (BESTSS / 4) IN TEMPY.
          ADDD TEMPY          ;ADD TEMPY TO ITSELF.
          ADDD TEMPY          ;ADD TEMPY TO STEP ABOVE FOR (TEMPY * 3).
          CPD WINSS           ;(WINSS/TSTSS) <= (3/4) ?.
          BLO CATEG2          ;YES - GOTO CATEG1. NO - GOTO CATEG2.
CATEG1    LDAA #$03
          STAA XCOUNT
          DECA
          STAA YCOUNT
          JMP ENABI
CATEG2    LDAA #$0C
          STAA XCOUNT
          LDAA #$09
          STAA YCOUNT
          JMP ENABI

FLGSET    LDAA BESTD
          CMPA WINDIR         ;IS NEW STRONGEST DIRECTION EQUAL TO WINDIR?
          BNE LP12 ;NO - GOTO LP12. YES - RE-INIT FLAG, COUNTERS &
                              ;RETURN TO ENDLESS LOOP WAITING FOR NEXT INTERRUPT.
          JMP REINIT          ;REINIT COUNTERS, FLAG, AND BESTSS.
LP12      CMPA TSTDIR         ;IS NEW STRONGEST DIRECTION EQUAL TO TSTDIR?
          BNE LP13 ;NO - GOTO LP13. YES - INCREMENT COUNT2 BY 1.
          LDAA COUNT2
          INCA
          STAA COUNT2
LP13      LDAA COUNT1
          INCA                ;INCREMENT # OF TIMES THIS SECTION HAS HAPPENED.
          STAA COUNT1
          CMPA XCOUNT         ;IS COUNT1 EQUAL TO XCOUNT?
          BEQ CONT2
          LDD #$0000
          STD BESTSS          ;SET BESTSS TO ZERO.
          JMP ENABI
CONT2     LDAA COUNT2
          CMPA YCOUNT         ;IS COUNT2 GREATER THAN YCOUNT?
          BLS LP14 ;NO - GOTO LP14. YES - GO ON.
          JSR NEWDIR1         ;SET UWAVE ANTENNA AND WINXXX PARAMETERS.
LP14      JMP REINIT          ;RE-INIT COUNTERS, FLAG, AND BESTSS TO ZERO.

************************************************************
*****END OF MAIN PROGRAM -- SUBROUTINES START HERE *****
************************************************************

*****SEND-LEDS SECTION *****
* THIS LIGHTS UP AN LED CORRESPONDING TO THE DIRECTION *
SENDLED   LDAA #$53;CODE TO INITIALIZE THE SPI CONDITION REGISTER.
          STAA SPCR
          LDAA SPSR           ;CLEAR SPIF BIT BY READING IT IN.
          LDAA WINDIR         ;GET WINNING DIRECTION CODE DATA.
          STAA SPDR           ;SEND TO SPI DATA REGISTER.
LP6       TST SPSR ;LED DATA DONE SENDING?
          BPL LP6             ;NO - GOTO LP6. YES - GO ON.
          LDAA #$20;TOGGLE CS LED LINE HIGH.
          STAA PORTD
          LDAA #$00;TOGGLE CS LED LINE LOW.
          STAA PORTD

* DEBUGGING ROUTINE HERE *
          LDAA TEMPPP
          CMPA #$00
          BNE TOGLO
TOGHI     LDAA #$01
          STAA TEMPPP
          LDAA PORTA
          ORA #$10 ;TOGGLE THE uWB LINE HI.
          STAA PORTA
          JMP CCONT
TOGLO     LDAA #$00
          STAA TEMPPP
          LDAA PORTA
          ANDA #$EF           ;TOGGLE THE uWB LINE LOW.
          STAA PORTA
CCONT
          RTS                 ;RETURN TO CALLING SUBROUTINE.

* SUBROUTINE TO TAKE THE WINNING DIRECTION AND CONFIGURE THE TRANSMITTING *
* UWAVE FOR THAT DIRECTION *
SENDUA    LDAA UPA ;LOAD REG A WITH DATA IN UPA.
          STAA REGA           ;WRITE IT TO PORTB (65C22).
          LDAA UPB ;LOAD REG B WITH DATA IN UPB.
          STAA REGB           ;WRITE IT TO PORTB (65C22).
*         LDAA PORTA
*         ORA #$10 ;TOGGLE THE uWB LINE HI.
*         STAA PORTA
*         ANDA #$EF           ;TOGGLE THE uWB LINE LOW.
*         STAA PORTA
          RTS                 ;RETURN TO CALLING ROUTINE.

* SUBROUTINE TO SET THE PHASED ARRAY ANTENNA FOR A DIRECTION *****
*****SEND-AB (SEND TWO BYTES OF DATA TO PORTB & PORTB ON THE 65C22) *****
SENDPA    LDAA PRTA           ;LOAD REG A WITH DATA IN PRTA.
          STAA REGA           ;WRITE IT TO PORTB (65C22).
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        LDAA PRTB           ;LOAD REG B WITH DATA IN PRTB.
        STAA REGB           ;WRITE IT TO PORTB (65C22).
*       LDAA PORTA
*       ORA #$08 ;TOGGLE PB LATCH HI.
*       STAA PORTA
*       ANDA #$F7           ;TOGGLE PB LATCH LOW.
*       STAA PORTA
        RTS                 ;RETURN TO CALLING ROUTINE.

* SUBROUTINE TO READ THE SIGNAL STRENGTH FROM THE A/D LINE *
* THE RESULT WILL BE LEFT IN REG D *
* DEBUG ROUTINE TO LOAD REG D WITH PRESET VALUE.
READAD
* DEBUGGING ROUTINE HERE *
*       JSR READIP
*       LDAA DIPDAT
*       ANDA #$04
*       BEQ BANK1
        LDAA TEMPP
        CMPA #$00
        BEQ GBANK0
        CMPA #$01
        BEQ GBANK1
        CMPA #$02
        BEQ GBANK2
        CMPA #$03
        BEQ GBANK3
        CMPA #$04
        BEQ GBANK4
        CMPA #$05
        BEQ GBANK5
        CMPA #$06
        BEQ GBANK6
        CMPA #$07
        BEQ GBANK7
        CMPA #$08
        BEQ GBANK8
        CMPA #$09
        BEQ GBANK9
        CMPA #$0A
        BEQ GBANKA
        CMPA #$0B
        BEQ GBANKB
        JMP READAD
GBANK0  JMP BANK0
GBANK1  JMP BANK1
GBANK2  JMP BANK2
GBANK3  JMP BANK3
GBANK4  JMP BANK4
GBANK5  JMP BANK5
GBANK6  JMP BANK6
GBANK7  JMP BANK7
GBANK8  JMP BANK8
GBANK9  JMP BANK9
GBANKA  JMP BANKA
GBANKB  JMP BANKB
BANK0   LDAA DCODE
        CMPA #$01
        BEQ B0D1
        CMPA #$02
        BEQ B0D2
        CMPA #$04
        BEQ B0D3
        CMPA #$08
        BEQ B0D4
        CMPA #$10
        BEQ B0D5
        CMPA #$20
        BEQ B0D6
        CMPA #$40
        BEQ B0D7
        CMPA #$80
        BEQ B0D8
        JMP STOPIT
B0D1    LDD #$0054
        JMP RETAD
B0D2    LDD #$0032
        JMP RETAD
B0D3    LDD #$0054
        JMP RETAD
B0D4    LDD #$0034
        JMP RETAD
B0D5    LDD #$00FF
        JMP RETAD
B0D6    LDD #$0055
        JMP RETAD
B0D7    LDD #$0022
        JMP RETAD
B0D8    LDD #$0087
        JMP RETAD
BANK1   LDAA DCODE
        CMPA #$01
        BEQ B1D1
        CMPA #$02
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```
        BEQ  B1D2
        CMPA #$04
        BEQ  B1D3
        CMPA #$08
        BEQ  B1D4
        CMPA #$10
        BEQ  B1D5
        CMPA #$20
        BEQ  B1D6
        CMPA #$40
        BEQ  B1D7
        CMPA #$80
        BEQ  B1D8
        JMP  STOPIT
B1D1    LDD  #$0054
        JMP  RETAD
B1D2    LDD  #$0033
        JMP  RETAD
B1D3    LDD  #$0023
        JMP  RETAD
B1D4    LDD  #$0065
        JMP  RETAD
B1D5    LDD  #$00FF
        JMP  RETAD
B1D6    LDD  #$0033
        JMP  RETAD
B1D7    LDD  #$0022
        JMP  RETAD
B1D8    LDD  #$0066
        JMP  RETAD
BANK2   LDAA DCODE
        CMPA #$01
        BEQ  B2D1
        CMPA #$02
        BEQ  B2D2
        CMPA #$04
        BEQ  B2D3
        CMPA #$08
        BEQ  B2D4
        CMPA #$10
        BEQ  B2D5
        CMPA #$20
        BEQ  B2D6
        CMPA #$40
        BEQ  B2D7
        CMPA #$80
        BEQ  B2D8
        JMP  STOPIT
B2D1    LDD  #$0054
        JMP  RETAD
B2D2    LDD  #$0033
        JMP  RETAD
B2D3    LDD  #$0023
        JMP  RETAD
B2D4    LDD  #$0065
        JMP  RETAD
B2D5    LDD  #$00FF
        JMP  RETAD
B2D6    LDD  #$0033
        JMP  RETAD
B2D7    LDD  #$0022
        JMP  RETAD
B2D8    LDD  #$0066
        JMP  RETAD
BANK3   LDAA DCODE
        CMPA #$01
        BEQ  B3D1
        CMPA #$02
        BEQ  B3D2
        CMPA #$04
        BEQ  B3D3
        CMPA #$08
        BEQ  B3D4
        CMPA #$10
        BEQ  B3D5
        CMPA #$20
        BEQ  B3D6
        CMPA #$40
        BEQ  B3D7
        CMPA #$80
        BEQ  B3D8
        JMP  STOPIT
B3D1    LDD  #$0054
        JMP  RETAD
B3D2    LDD  #$0032
        JMP  RETAD
B3D3    LDD  #$0054
        JMP  RETAD
B3D4    LDD  #$0034
        JMP  RETAD
B3D5    LDD  #$00FF
        JMP  RETAD
B3D6    LDD  #$0055
        JMP  RETAD
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```
B6D3    LDD #$00FF
        JMP RETAD
B6D4    LDD #$0034
        JMP RETAD
B6D5    LDD #$0012
        JMP RETAD
B6D6    LDD #$0055
        JMP RETAD
B6D7    LDD #$0022
        JMP RETAD
B6D8    LDD #$0043
        JMP RETAD
BANK7   LDAA DCODE
        CMPA #$01
        BEQ B7D1
        CMPA #$02
        BEQ B7D2
        CMPA #$04
        BEQ B7D3
        CMPA #$08
        BEQ B7D4
        CMPA #$10
        BEQ B7D5
        CMPA #$20
        BEQ B7D6
        CMPA #$40
        BEQ B7D7
        CMPA #$80
        BEQ B7D8
        JMP STOPIT
B7D1    LDD #$0054
        JMP RETAD
B7D2    LDD #$0032
        JMP RETAD
B7D3    LDD #$00FF
        JMP RETAD
B7D4    LDD #$0034
        JMP RETAD
B7D5    LDD #$0032
        JMP RETAD
B7D6    LDD #$0055
        JMP RETAD
B7D7    LDD #$0013
        JMP RETAD
B7D8    LDD #$0032
        JMP RETAD
BANK8   LDAA DCODE
        CMPA #$01
        BEQ B8D1
        CMPA #$02
        BEQ B8D2
        CMPA #$04
        BEQ B8D3
        CMPA #$08
        BEQ B8D4
        CMPA #$10
        BEQ B8D5
        CMPA #$20
        BEQ B8D6
        CMPA #$40
        BEQ B8D7
        CMPA #$80
        BEQ B8D8
        JMP STOPIT
B8D1    LDD #$0054
        JMP RETAD
B8D2    LDD #$0032
        JMP RETAD
B8D3    LDD #$0043
        JMP RETAD
B8D4    LDD #$0034
        JMP RETAD
B8D5    LDD #$0014
        JMP RETAD
B8D6    LDD #$0055
        JMP RETAD
B8D7    LDD #$00FF
        JMP RETAD
B8D8    LDD #$0043
        JMP RETAD
BANK9   LDAA DCODE
        CMPA #$01
        BEQ B9D1
        CMPA #$02
        BEQ B9D2
        CMPA #$04
        BEQ B9D3
        CMPA #$08
        BEQ B9D4
        CMPA #$10
        BEQ B9D5
        CMPA #$20
        BEQ B9D6
        CMPA #$40
```

```
        BEQ  B9D7
        CMPA #$80
        BEQ  B9D8
        JMP  STOPIT
B9D1    LDD  #$0054
        JMP  RETAD
B9D2    LDD  #$0032
        JMP  RETAD
B9D3    LDD  #$0032
        JMP  RETAD
B9D4    LDD  #$0034
        JMP  RETAD
B9D5    LDD  #$0012
        JMP  RETAD
B9D6    LDD  #$0055
        JMP  RETAD
B9D7    LDD  #$00FF
        JMP  RETAD
B9D8    LDD  #$0043
        JMP  RETAD
BANKA   LDAA DCODE
        CMPA #$01
        BEQ  BAD1
        CMPA #$02
        BEQ  BAD2
        CMPA #$04
        BEQ  BAD3
        CMPA #$08
        BEQ  BAD4
        CMPA #$10
        BEQ  BAD5
        CMPA #$20
        BEQ  BAD6
        CMPA #$40
        BEQ  BAD7
        CMPA #$80
        BEQ  BAD8
        JMP  STOPIT
BAD1    LDD  #$0054
        JMP  RETAD
BAD2    LDD  #$0032
        JMP  RETAD
BAD3    LDD  #$0023
        JMP  RETAD
BAD4    LDD  #$0034
        JMP  RETAD
BAD5    LDD  #$0032
        JMP  RETAD
BAD6    LDD  #$0055
        JMP  RETAD
BAD7    LDD  #$00FF
        JMP  RETAD
BAD8    LDD  #$0032
        JMP  RETAD
BANKB   LDAA DCODE
        CMPA #$01
        BEQ  BBD1
        CMPA #$02
        BEQ  BBD2
        CMPA #$04
        BEQ  BBD3
        CMPA #$08
        BEQ  BBD4
        CMPA #$10
        BEQ  BBD5
        CMPA #$20
        BEQ  BBD6
        CMPA #$40
        BEQ  BBD7
        CMPA #$80
        BEQ  BBD8
        JMP  STOPIT
BBD1    LDD  #$0054
        JMP  RETAD
BBD2    LDD  #$0032
        JMP  RETAD
BBD3    LDD  #$0054
        JMP  RETAD
BBD4    LDD  #$0034
        JMP  RETAD
BBD5    LDD  #$0014
        JMP  RETAD
BBD6    LDD  #$0055
        JMP  RETAD
BBD7    LDD  #$00FF
        JMP  RETAD
BBD8    LDD  #$0043
        JMP  RETAD
RETAD   STD  TEMPY
        RTS

        LDAA #$53;CODE TO INITIALIZE THE SPI CONDITION REGISTER.
```

```
        STAA SPCR
        LDAA SPSR           ;CLEAR SPIF BIT BY READING IT IN.
        LDAA PORTA          ;PUT PORTA DATA INTO ACC.
        ANDA #$DF
        STAA PORTA          ;PORTA BIT 5 GOES LOW.
        LDAA #$68;CODE TO BEGIN A/D OPERATION.
        STAA SPDR
LP4     TST SPSR ;A/D DATA READY TO READ IN?
        BPL LP4             ;NO - GOTO LP4. YES - GO ON.
        LDAA SPDR           ;PUT A/D DATA INTO ACC.
        ANDA #$03           ;GET BITS 0 & 1 FOR MSB DATA.
        STAA SPDR           ;BEGIN NEXT A/D OPERATION.
LP5     TST SPSR
        BPL LP5
        LDAB SPDR           ;PUT A/D DATA INTO REG B. (LSB)
        STD ADDATA          ;STORE 10-BIT A/D RESULT IN ADDATA.
        LDAA PORTA          ;PUT PORTA DATA INTO ACC.
        ORAA #$20
        STAA PORTA          ;PORTA BIT 5 GOES HI.
        RTS                 ;RETURN TO CALLING ROUTINE.

* SUBROUTINES TO CONFIGURE THE PHASED ARRAY BOARD FOR A DIRECTION *
*****Q1 - Q8 SECTIONS *****
* EACH QX SECTION SENDS OUT CERTAIN PATTERNS TO THE PHASED ARRAY *
* ANTENNA FOR A PARTICULAR DIRECTION *
* D1 DIRECTION WITH SPECIAL SETTINGS FOR UWAVE SWITCH #1.
Q11     JSR LOADCP          ;RELOAD THE COP TIMER.
        LDAA #PAD1          ;LOAD REG A WITH PATTERN FOR PORTA D1.
        STAA PRTA           ;STORE IT IN PRTA.
        LDAA #PBD1          ;LOAD REG B WITH PATTERN FOR PORTB D1.
        STAA PRTB           ;STORE IT IN PRTB.
        JSR SENDPA          ;CALL SUBROUTINE SENDPA TO SET PHASED ANTENNA.
        LDAA #MAD11         ;LOAD REG A WITH UWAVE PATTERN FOR PORTA D1.
        STAA PRTA           ;STORE IT IN PRTA.
        LDAA #MBD1          ;LOAD REG B WITH UWAVE PATTERN FOR PORTB D1.
        STAA PRTB           ;STORE IT IN PRTB.
        JMP TESTSS
* D1 DIRECTION WITH SPECIAL SETTINGS FOR UWAVE SWITCH #2.
Q12     JSR LOADCP
        LDAA #PAD1
        STAA PRTA
        LDAA #PBD1
        STAA PRTB
        JSR SENDPA
        LDAA #MAD12
        STAA PRTA
        LDAA #MBD1
        STAA PRTB
        JMP TESTSS
* D2 DIRECTION WITH SPECIAL SETTINGS FOR UWAVE SWITCH #1.
Q21     JSR LOADCP
        LDAA #PAD2
        STAA PRTA
        LDAA #PBD2
        STAA PRTB
        JSR SENDPA
        LDAA #MAD21
        STAA PRTA
        LDAA #MBD2
        STAA PRTB
        JMP TESTSS
* D2 DIRECTION WITH SPECIAL SETTINGS FOR UWAVE SWITCH #2.
Q22     JSR LOADCP
        LDAA #PAD2
        STAA PRTA
        LDAA #PBD2
        STAA PRTB
        JSR SENDPA
        LDAA #MAD22
        STAA PRTA
        LDAA #MBD2
        STAA PRTB
        JMP TESTSS
Q3      JSR LOADCP
        LDAA #PAD3
        STAA PRTA
        LDAA #PBD3
        STAA PRTB
        JSR SENDPA
        LDAA #MAD3
        STAA PRTA
        LDAA #MBD3
        STAA PRTB
        JMP TESTSS
Q4      JSR LOADCP
        LDAA #PAD4
        STAA PRTA
        LDAA #PBD4
        STAA PRTB
        JSR SENDPA
        LDAA #MAD4
        STAA PRTA
        LDAA #MBD4
        STAA PRTB
```

```
        JMP TESTSS
Q5      JSR LOADCP
        LDAA #PAD5
        STAA PRTA
        LDAA #PBD5
        STAA PRTB
        JSR SENDPA
        LDAA #MAD5
        STAA PRTA
        LDAA #MBD5
        STAA PRTB
        JMP TESTSS
Q6      JSR LOADCP
        LDAA #PAD6
        STAA PRTA
        LDAA #PBD6
        STAA PRTB
        JSR SENDPA
        LDAA #MAD6
        STAA PRTA
        LDAA #MBD6
        STAA PRTB
        JMP TESTSS
Q7      JSR LOADCP
        LDAA #PAD7
        STAA PRTA
        LDAA #PBD7
        STAA PRTB
        JSR SENDPA
        LDAA #MAD7
        STAA PRTA
        LDAA #MBD7
        STAA PRTB
        JMP TESTSS
Q8      JSR LOADCP
        LDAA #PAD8
        STAA PRTA
        LDAA #PBD8
        STAA PRTB
        JSR SENDPA
        LDAA #MAD8
        STAA PRTA
        LDAA #MBD8
        STAA PRTB
        JMP TESTSS

* SUBROUTINE TO LOAD UPA,B WITH UWAVE ANTENNA SETTINGS *
LOADUA  LDAA DCODE      ;USE DCODE TO DETERMINE DIRECTION.
        CMPA #$01       ;D1?
        BEQ UAD1
        CMPA #$02       ;D2?
        BEQ UAD2
        CMPA #$04       ;D3?
        BEQ UAD3
        CMPA #$08       ;D4?
        BEQ UAD4
        CMPA #$10       ;D5?
        BEQ UAD5
        CMPA #$20       ;D6?
        BEQ UAD6
        CMPA #$40       ;D7?
        BEQ UAD7
        CMPA #$80       ;D8?
        BEQ UAD8
        JMP STOPIT      ;CORRUPTED DCODE. START OVER.
UAD1    JSR READIP      ;GET STATUS OF DIP #2.
        LDAA DIPDAT
        ANDA #$40
        BEQ SW2ON5      ;DIP #2 ON? YES - GOTO SW2ON5. NO - GOTO SW2OF5.
SW2OF5  LDAA #MAD12     ;LOAD REG A WITH PARAMETERS FOR D1 SWITCH #2.
        JMP CONT5       ;CONTINUE AT CONT5.
SW2ON5  LDAA #MAD11     ;LOAD REG A WITH PARAMETERS FOR D1 SWITCH #1.
CONT5   STAA UPA ;STORE IT IN UPA.
        LDAA #MBD1
        STAA UPB
        RTS
UAD2    JSR READIP      ;GET STATUS OF DIP #2.
        LDAA DIPDAT
        ANDA #$40
        BEQ SW2ON3      ;DIP #2 ON? YES - GOTO SW2ON3. NO - GOTO SW2OF3.
SW2OF3  LDAA #MAD22     ;LOAD REG A WITH PARAMETERS FOR D2 SWITCH #2.
        JMP CONT3       ;CONTINUE AT CONT3.
SW2ON3  LDAA #MAD21     ;LOAD REG A WITH PARAMETERS FOR D2 SWITCH #1.
CONT3   STAA UPA ;STORE IT IN UPA.
        LDAA #MBD8
        STAA UPB
        RTS
UAD3    LDAA #MAD3
        STAA UPA
        LDAA #MBD3
        STAA UPB
        RTS
UAD4    LDAA #MAD4
        STAA UPA
```

```
        LDAA #MBD4
        STAA UPB
        RTS
UAD5    LDAA #MAD5
        STAA UPA
        LDAA #MBD5
        STAA UPB
        RTS
UAD6    LDAA #MAD6
        STAA UPA
        LDAA #MBD6
        STAA UPB
        RTS
UAD7    LDAA #MAD7
        STAA UPA
        LDAA #MBD7
        STAA UPB
        RTS
UAD8    LDAA #MAD8
        STAA UPA
        LDAA #MBD8
        STAA UPB
        RTS

*****SUBROUTINE TO READ THE DIP SWITCH *****
READIP  LDAA PORTE          ;PUT PORTE DATA INTO REG A.
        ANDA #$FC           ;MASK OUT BITS 0 & 1.
        STAA DIPDAT         ;STORE IN DIPDATA BYTE.
        RTS

* SUBROUTINE TO RELOAD THE COP TIMER.
LOADCP  LDAA #$55
        STAA COPRST
        LDAA #$AA
        STAA COPRST         ;COP TIMER IS NOW RELOADED.
        RTS

* SUBROUTINE TO INIT ALL PORTS, A/D, RAM TABLE *
STRTUP  LDAA #$38
        STAA DDRD           ;PORTD: ALL OUT EXCEPT RxD = PD0.
        LDAA #$FF
        STAA DDRA           ;INIT 65C22 PORTA TO OUTPUTS.
        LDAA #$FF
        STAA DDRB           ;INIT 65C22 PORTB TO OUTPUTS.
        LDAA #$00
        STAA PORTD          ;SET PDx LOW.
        LDD #$0000
        STD WINSS           ;STORE 0000H IN WINSS.
        RTS                 ;RETURN TO CALLING ROUTINE.

* SUBROUTINE TO SET UWAVE ANTENNA AND NEWXXX PARAMETERS *
* FROM BESTXX PARAMETERS *
NEWDIR  LDD BESTSS
        STD WINSS           ;STORE STRONGEST SIGNAL STRENGTH IN WINSS.
        LDAA BESTD
        STAA WINDIR         ;STORE STRONGEST DIRECTION IN WINDIR.
        JSR SENDUA          ;SET UWAVE ANTENNA TO STRONGEST DIRECTION.
        JSR SENDLED         ;SHOW NEW DIRECTION ON THE LEDS.
        RTS

* SUBROUTINE TO SET UWAVE ANTENNA AND NEWXXX PARAMETERS *
* FROM TSTXXX PARAMETERS *
NEWDIR1 LDD TSTSS
        STD WINSS           ;STORE STRONGEST SIGNAL STRENGTH IN WINSS.
        LDAA TSTDIR
        STAA WINDIR         ;STORE STRONGEST DIRECTION IN WINDIR.
        JSR SENDUA          ;SET UWAVE ANTENNA TO STRONGEST DIRECTION.
        JSR SENDLED         ;SHOW NEW DIRECTION ON THE LEDS
        RTS

* SUBROUTINE TO STOP THE SYSTEM. THE CLOCK MONITOR WILL RESET THE SYSTEM *
STOPIT  TPA                 ;MOVE CONDITION CODE REG TO REG A.
        ANDA #$EF           ;CLEAR BIT 7 TO ENABLE THE STOP.
        TAP                 ;MOVE NEW VALUE BACK TO CONDITION CODE REG.
        NOP
        STOP

* SUBROUTINE TO RE-INIT THE COUNTERS, FLAG, AND BESTSS TO ZERO *
REINIT  LDAA #$00
        STAA COUNT1
        STAA COUNT2
        STAA FLAG
        LDD #$00000
        STD BESTSS          ;SET BESTSS TO ZERO.
        JMP ENABI

* SUBROUTINE TO READ DIPS #3-#5 AND DETERMINE THE SCANNING SPEED.
SETSS   JSR READIP
        LDAA DIPDAT
        ANDA #$38           ;GET DIPS #3-#5.
        CMPA #$00
        BEQ HZ4
        CMPA #$08
        BEQ HZ25
```

```
        CMPA #$10
        BEQ  HZ50
        CMPA #$18
        BEQ  HZ100
        CMPA #$20
        BEQ  HZ200
        CMPA #$28
        BEQ  HZ300
        CMPA #$30
        BEQ  HZ400
        LDD  #$0000
        JMP  HZRET
HZ4     LDD  #$F424
        JMP  HZRET
HZ25    LDD  #$2710
        JMP  HZRET
HZ50    LDD  #$1388
        JMP  HZRET
HZ100   LDD  #$09C4
        JMP  HZRET
HZ200   LDD  #$04E2
        JMP  HZRET
HZ300   LDD  #$0341
        JMP  HZRET
HZ400   LDD  #$0271
HZRET   STD  SSPEED
        RTS

* SUBROUTINE  TO ENABLE  THE NEXT TIMED INTERRUPT.
ENABI   LDD  SSPEED
        CPD  #$0000          ;ARE DIPS. #3-5 OFF?
        BNE  ENINS           ;NO - ENABLE  NEXT INTERRUPT  TIMING.
        JMP  BYPASS          ;YES - BYPASS NEXT INTERRUPT  TIMING.
ENINS   LDAA #$40
        STAA TFLG1
        STAA TMSK1           ;ENABLE  OUTPUT CAPTURE  TIMING INTERRUPT.
        RTI                  ;GOTO ENDLESS  LOOP AND WAIT FOR INTERRUPT.
        END
```

IX.B. FORTH PROGRAM CODE LISTING

```
HEX
8004 1C !
50 1E !
8060 22 !
FORGET TASK
8080 DP !

( **FORTH CODE FOR TACOM PROJECT **ALL BOARDS REV 2.0 **)
( ************** TACOM24.FOR **********)
(                 10/26/89                )
(        BURNED INTO EPROM AT C000H       )
( D1 = ANTENNA #1 / D2 IS BETWEEN ANTENNA #1 & #2      )
( D3...D8 IS CW ie. D3 IS ANTENNA #2                   )

( ************ADDRESSES **************************)
( 65C22 ADDRESSES )
A000 CONSTANT REGB
A001 CONSTANT REGA
A002 CONSTANT DDRB
A003 CONSTANT DDRA

( 68HC11 PORT ADDRESSES )
B000 CONSTANT PORTA
B008 CONSTANT PORTD
B009 CONSTANT DDRD
B00A CONSTANT PORTE
B028 CONSTANT SPCR          ( SPI CONDITION REGISTER )
B029 CONSTANT SPSR          ( SPI STATUS REGISTER )
B02A CONSTANT SPDR          ( SPI DATA REGISTER )
B026 CONSTANT PATCL         ( BIT 7 IS DDRA7 )

( SERIAL I/O ADDRESSES )
B02B CONSTANT BAUD

( A/D ADDRESSES )
B030 CONSTANT ADCTL
B033 CONSTANT ADR3
B034 CONSTANT ADR4
B039 CONSTANT OPTION

( ************PATTERN BITMASKS **********************)
( STORAGE LOCATIONS FOR PORTA & PORTB TO SET PHASED ARRAY ANTENNA )
99 CONSTANT PAD1   ( PHASED ANTENNA PORT A D1 )
A9 CONSTANT PAD2
69 CONSTANT PAD3
6A CONSTANT PAD4
66 CONSTANT PAD5
A6 CONSTANT PAD6
96 CONSTANT PAD7
9A CONSTANT PAD8
06 CONSTANT PBD1   ( PHASED ANTENNA PORT B D1 )
0A CONSTANT PBD2
09 CONSTANT PBD3
09 CONSTANT PBD4
09 CONSTANT PBD5
0A CONSTANT PBD6
06 CONSTANT PBD7
06 CONSTANT PBD8

( STORAGE LOCATIONS FOR PORTA & PORTB TO SET UWAVE ANTENNA )
16 CONSTANT MAD11  ( MICRO WAVE PORT A D1 SWITCH #1 )
13 CONSTANT MAD12  ( MICRO WAVE PORT A D1 SWITCH #2 )
13 CONSTANT MAD21
16 CONSTANT MAD22   ( MICRO WAVE PORT A D8 SWITCH #2 )
20 CONSTANT MAD3
20 CONSTANT MAD4
68 CONSTANT MAD5
E0 CONSTANT MAD6
10 CONSTANT MAD7
10 CONSTANT MAD8
00 CONSTANT MBD1   ( MICRO WAVE PORT B D1 )
00 CONSTANT MBD2
30 CONSTANT MBD3
18 CONSTANT MBD4
00 CONSTANT MBD5
00 CONSTANT MBD6
06 CONSTANT MBD7
03 CONSTANT MBD8

( ************VARIOUS DATA STORAGE ****************)
9FC0 CONSTANT DIPDAT    ( DIPSWITCH DATA )
9FC1 CONSTANT LOOPS     ( NUMBER OF TIMES TO SCAN 1 DIRECTION )
9FC2 CONSTANT BEST      ( STORE STRONGEST SIGNAL LEVEL )
9FC4 CONSTANT WINA      ( WINNING DIRECTION'S PORT A BITMASK )
9FC5 CONSTANT WINB      ( WINNING DIRECTION'S PORT B BITMASK )
9FC6 CONSTANT WINDIR    ( WINNING DIRECTION )
9FC7 CONSTANT CHKSUM    ( USED FOR UPLOADING IN HEX FORMAT )
9FC9 CONSTANT DEL-VAR   ( DELAY VARIABLE )
9FCB CONSTANT ADDATA    ( A/D DATA IS STORED HERE )
9FCD CONSTANT DATAA     ( STORAGE TO PUT LED CODE )
9FD0 CONSTANT UNUSED
```

```
( ************FILL CONSTANTS WORDS ***************)***
( FILL STORAGE LOCATIONS WITH CORRECT BITMASKS )
: FILL-VARCON          ( FILL CONSTANTS WITH DEFAULT VALUES )
    06 LOOPS C! 200 DEL-VAR ! FFFF BEST ! ;

( ************MISC WORDS ************************)*****
: DEL       DEL-VAR @ 0 DO 1 0 DO LOOP LOOP ;  ( DELAY )
: BAUD-300   35 BAUD C! ;    ( USED FOR UPLOADING IN HEX FORMAT )
: READIP   PORTE C@ ; ( LEAVE DIP STATUS ON STACK )

( ************A/D WORDS ************************)*****
( LEAVE A/D RESULT ON STACK )
: READAD   53 SPCR C!        ( INIT SPCR )
        SPSR C@ DROP      ( CLEAR SPIF BIT )
        PORTA C@ DF AND PORTA C! ( CS GOES LOW )
        68 SPDR C!        ( INITIATE TRANSFER )
        BEGIN SPSR C@ 80 AND IF 0 ELSE 1 THEN UNTIL  ( TEST IF RCVR DONE )
        SPDR C@ 03 AND ADDATA C!    ( STORE MSB OF DATA IN ADDATA )
        SPSR C@ DROP      ( CLEAR SPIF BIT )
        00 SPDR C!        ( INITIATE TRANSFER )
        BEGIN SPSR C@ 80 AND IF 0 ELSE 1 THEN UNTIL  ( TEST IF RCVR DONE )
        PORTA C@ 20 OR PORTA C!       ( CS GOES HI )
        SPDR C@ ADDATA 1+ C!    ( STORE LSB OF DATA IN ADDATA )
        ADDATA @ ;

( ************ANTENNA FUNCTION WORDS ***************)***
: SET-REGS-OUT    FF DDRB C! FF DDRA C! ;
: TOG-PB        PORTA C@ DUP 08 OR PORTA C! F7 AND PORTA C! ;
: TOG-UWB       PORTA C@ DUP 10 OR PORTA C! EF AND PORTA C! ;
: OUTA         REGA C! ;
: OUTB         REGB C! ;
: OUTPB        OUTB OUTA TOG-PB ;
: OUTUWB       OUTB OUTA TOG-UWB ;

( ************LED WORDS ************************)*****
: OUTLED  DATAA C! 53 SPCR C! SPSR C@ DROP DATAA C@ SPDR C!
       BEGIN SPSR C@ 80 AND IF 0 ELSE 1 THEN UNTIL
       20 PORTD C! 00 PORTD C! ;

( ************FIX DIRECTION WORDS ***************)***
( PHASED ANTENNA )
: D1P   PAD1 PBD1 OUTPB 01 OUTLED ;
: D2P   PAD2 PBD2 OUTPB 02 OUTLED ;
: D3P   PAD3 PBD3 OUTPB 04 OUTLED ;
: D4P   PAD4 PBD4 OUTPB 08 OUTLED ;
: D5P   PAD5 PBD5 OUTPB 10 OUTLED ;
: D6P   PAD6 PBD6 OUTPB 20 OUTLED ;
: D7P   PAD7 PBD7 OUTPB 40 OUTLED ;
: D8P   PAD8 PBD8 OUTPB 80 OUTLED ;
( MICROWAVE ANTENNA )
: D1M   READIP 40 AND IF MAD12 MBD1 ELSE MAD11 MBD1 THEN OUTUWB ;
: D2M   READIP 40 AND IF MAD22 MBD2 ELSE MAD21 MBD2 THEN OUTUWB ;
: D3M   MAD3 MBD3 OUTUWB ;
: D4M   MAD4 MBD4 OUTUWB ;
: D5M   MAD5 MBD5 OUTUWB ;
: D6M   MAD6 MBD6 OUTUWB ;
: D7M   MAD7 MBD7 OUTUWB ;
: D8M   MAD8 MBD8 OUTUWB ;

( ************CHIRPING ROUTINE ***************)*****
: CHIRPS   0 DO PORTA C@ DUP 40 OR PORTA C! BF AND PORTA C! LOOP ;

( ************SCAN ************************)*******
( THE RADIO EMITS A VOLTAGE OUTPUT THAT HAS AN INVERSE RELATIONSHIP )
( TO THE STRENGTH OF THE SIGNAL LEVEL )
: SCANNING
    D1P DEL READAD BEST ! READIP 40 AND IF MAD12 WINA C!
       ELSE MAD11 WINA C! THEN MBD1 WINB C! 01 WINDIR C!
    D2P DEL READAD DUP BEST @ < IF BEST ! READIP 40 AND
       IF MAD22 WINA C! ELSE MAD21 WINA C! THEN
       MBD2 WINB C! 02 WINDIR C! ELSE DROP THEN
    D3P DEL READAD DUP BEST @ < IF BEST ! MAD3 WINA C!
       MBD3 WINB C! 04 WINDIR C! ELSE DROP THEN
    D4P DEL READAD DUP BEST @ < IF BEST ! MAD4 WINA C!
       MBD4 WINB C! 08 WINDIR C! ELSE DROP THEN
    D5P DEL READAD DUP BEST @ < IF BEST ! MAD5 WINA C!
       MBD5 WINB C! 10 WINDIR C! ELSE DROP THEN
    D6P DEL READAD DUP BEST @ < IF BEST ! MAD6 WINA C!
       MBD6 WINB C! 20 WINDIR C! ELSE DROP THEN
    D7P DEL READAD DUP BEST @ < IF BEST ! MAD7 WINA C!
       MBD7 WINB C! 40 WINDIR C! ELSE DROP THEN
    D8P DEL READAD DUP BEST @ < IF BEST ! MAD8 WINA C!
       MBD8 WINB C! 80 WINDIR C! ELSE DROP THEN
       WINA C@ WINB C@ OUTUWB ;

( ************DUMP FORTH CODE AS INTEL HEX FORMAT ***)
: LP   9000 0 DO 1 0 DO LOOP LOOP ;
: CE   DUP A < IF 30 ELSE 37 THEN + EMIT ;          ( CONVERT AND EMIT )
: 2.R  FF AND 10 /MOD CE CE ;
: 4.R  0 100 UM/MOD 2.R 2.R ;
: INTEL-DUMP                                  ( addr count --- )
   LP
   BAUD-300
   OVER + SWAP          ( CONVERTS ADDR & COUNT TO UPPER, LOWER ADDR )
```

```
   BEGIN   CR
      2DUP 20 + MIN   ( MAKE NEXT LINE OF OUTPUT UP TO 32 BYTES LONG )
      SWAP          ( BRING UP START ADDRESS, MOVE DOWN END ADDRESS )
      ." :"                              ( BEGIN THE RECORD )
      2DUP -                  ( FIND OUT # OF BYTES IN THIS RECORD )
      DUP CHKSUM !                        ( BEGIN CHKSUM COMPUTATION )
      2.R          ( PRINT # OF BYTES IN RECORD IN TWO DIGIT FIELD )
      DUP 100 /MOD + CHKSUM +!          ( ADD START ADDRESS TO CHKSUM )
      DUP 4.R            ( PRINT START ADDRESS IN FOUR DIGIT FIELD )
      ." 00"          ( PRINT RECORD TYPE, NO NEED TO ADD TO CHKSUM )
      >R DUP R>                    ( MAKE START STOP #S FOR DO LOOP )
      DO
         I C@ 2.R              ( PRINT HEX BYTE IN TWO DIGIT FIELD )
         I C@ CHKSUM +!                          ( UPDATE CHKSUM )
      LOOP
      CHKSUM C@ NEGATE 2.R  ( PRINT CHKSUM NEGATED TWO DIGIT FIELD )
      2DUP =
   UNTIL              ( KEEP GOING TILL LINE END IS = TO BLOCK END )
   CR ." :00000001FF" CR                      ( TACK ON END RECORD )
   2DROP ;

( ************START-UP THE BOARD FUNCTIONS *********)
: INITALL  80 OPTION C!              ( POWER UP A/D CAPABILITY )
        38 DDRD  C!                          ( INIT PORT D )
        SET-REGS-OUT    D1P D1M          ( SET ANTENNAS TO D1P )
        FILL-VARCON                    ( FILL VAR CONSTANTS )
        2 CHIRPS  ;                ( SIGNIFY BOARD IS READY )

( ********SCAN AND SHOW A/D READING FOR A DIRECTION SEVERAL TIMES **)
( ********DO ON ALL 8 DIRECTIONS AND REPEAT **********************)*****
: DELA     3000 0 DO LOOP ;
: SHOWAD   READAD DELA DECIMAL . HEX CR ;
: SCANALL  INITALL READAD DROP CR BEGIN
        D1P LOOPS C@ 0 DO ." D1= " SHOWAD LOOP CR
        D2P LOOPS C@ 0 DO ." D2= " SHOWAD LOOP CR
        D3P LOOPS C@ 0 DO ." D3= " SHOWAD LOOP CR
        D4P LOOPS C@ 0 DO ." D4= " SHOWAD LOOP CR
        D5P LOOPS C@ 0 DO ." D5= " SHOWAD LOOP CR
        D6P LOOPS C@ 0 DO ." D6= " SHOWAD LOOP CR
        D7P LOOPS C@ 0 DO ." D7= " SHOWAD LOOP CR
        D8P LOOPS C@ 0 DO ." D8= " SHOWAD LOOP CR
        ?TERMINAL UNTIL ;

( ******SCAN ALL DIRECTIONS CONTINUOUSLY *************)**
: SCAN  INITALL BEGIN SCANNING ?TERMINAL UNTIL ;

( ******SCAN AND SHOW STRONGEST SIGNAL ***************)***
: SCANDIR  INITALL BEGIN
        SCANNING
        WINDIR C@ 01 = IF ." D1" CR ELSE THEN
        WINDIR C@ 02 = IF ." D2" CR ELSE THEN
        WINDIR C@ 04 = IF ." D3" CR ELSE THEN
        WINDIR C@ 08 = IF ." D4" CR ELSE THEN
        WINDIR C@ 10 = IF ." D5" CR ELSE THEN
        WINDIR C@ 20 = IF ." D6" CR ELSE THEN
        WINDIR C@ 40 = IF ." D7" CR ELSE THEN
        WINDIR C@ 80 = IF ." D8" CR ELSE THEN
        WINDIR C@ OUTLED ?TERMINAL UNTIL ;

( FOR FIELD TESTING PURPOSES TO ENABLE EASIER A/D READING )
: Q  INITALL D1P BEGIN ." D1= " SHOWAD ?TERMINAL UNTIL ;
: W  INITALL D2P BEGIN ." D2= " SHOWAD ?TERMINAL UNTIL ;
: E  INITALL D3P BEGIN ." D3= " SHOWAD ?TERMINAL UNTIL ;
: R  INITALL D4P BEGIN ." D4= " SHOWAD ?TERMINAL UNTIL ;
: T  INITALL D5P BEGIN ." D5= " SHOWAD ?TERMINAL UNTIL ;
: Y  INITALL D6P BEGIN ." D6= " SHOWAD ?TERMINAL UNTIL ;
: U  INITALL D7P BEGIN ." D7= " SHOWAD ?TERMINAL UNTIL ;
: I  INITALL D8P BEGIN ." D8= " SHOWAD ?TERMINAL UNTIL ;
```

APPENDIX IX.C.

PARTS LIST WITH VENDOR AND COST DATA

REPORT " BY CODE AND COST "
FROM DATABASE...PARTSUSE PRINTED ON Nov 1, 1989 AT 1:17 pm

CODE OF ASSEMBLY	DESCRIPTION OF ITEM	NUM PER ASM	VENDOR	VENDOR STOCK NUMBER	MANUFACTURER	COST	TOTAL
ANT_HELICAL	ANTENNA...HELICAL TYPE	8	TRA			$ 50.00	$ 400.00
	CONNECTOR...N TYPE SOLDER CONNECTION FLANGE MOUNT	8	PASTERNACK	PE4013	PASTERNACK	$ 3.25	$ 26.00
Total:							$ 426.00
ANT_WHIP	ANTENNA...WHIP TYPE	4	LARSEN ELECTRONICS	NLA-220	LARSEN	$ 50.00	$ 200.00
Total:							$ 200.00
BIASB	D25 MALE PC MOUNT TYPE (RIGHT ANGLE)	1	ARROW	9215PRP	AMP	$ 8.30	$ 8.30
Total:							$ 8.30
CABLE_PB1	N MALE CLAMP TYPE CONNECTOR TO RG-58	1	PASTERNACK	PE4081	SAME	$ 3.25	$ 3.25
	BNC FEMALE BULKHEAD CONNECTOR	1	PASTERNACK	PE4078	PASTERNACK	$ 4.25	$ 4.25
	SMA MALE CLAMP TYPE RIGHT ANGLE CONNECTOR FOR RG-58	1	PASTERNACK	PE4029	PASTERNACK	$ 14.25	$ 14.25
	RG-58 COAX CABLE	1	KIMBALL		BELDEN	$ 1.00	$ 1.00
	BNC MALE CRIMP TYPE CONNECTOR TO RG-58	1	PASTERNACK	PE4016	PASTERNACK	$ 1.60	$ 1.60
Total:							$ 24.35
CABLE_PB2	SMA MALE CLAMP TYPE RIGHT ANGLE CONNECTOR FOR RG-58	4	PASTERNACK	PE4029	PASTERNACK	$ 14.25	$ 57.00
	CONNECTOR REDUCER...PL259 TO RG-58 (SIMILAR TO R.S. 278-206)	4	RADIO SHACK	278-206		$ 0.50	$ 2.00
	BNC MALE CRIMP TYPE CONNECTOR TO RG-58	4	PASTERNACK	PE4016	PASTERNACK	$ 1.60	$ 6.40
	BNC FEMALE BULKHEAD CONNECTOR	4	PASTERNACK	PE4078	PASTERNACK	$ 4.25	$ 17.00
	PL259 (UHF) TYPE FEMALE CONNECTOR	4	RADIO SHACK	278-205		$ 1.40	$ 5.60
	RG-58 COAX CABLE	1				$ 5.00	$ 5.00
	PL259 RIGHT ANGLE MALE-FEMALE CONNECTOR	4	NEWARK	46N7371	SPC	$ 5.88	$ 23.52
Total:							$ 116.52
CABLE_PBD1	D25 MALE CRIMP TYPE (STRAIGHT)	2	ARROW	9215PD9	AMP	$ 1.23	$ 2.46
	D25 FEMALE CRIMP TYPE (STRAIGHT)	3	ARROW	9215PEA	AMP	$ 1.23	$ 3.69
Total:							$ 6.15

REPORT " BY CODE AND COST "
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CODE OF ASSEMBLY	DESCRIPTION OF ITEM	NUM PER ASM	VENDOR	VENDOR STOCK NUMBER	MANUFACTURER	COST	TOTAL
CABLE_PM1	CIRCULAR TYPE 4 PIN FEMALE CONNECTOR	2	ARROW	9215PFZ	AMP	$ 1.52	$ 3.04
	CIRCULAR TYPE 4 PIN MALE CONNECTOR	2	ARROW	9215PF5	AMP	$ 2.06	$ 4.12
		1	DIGIKEY	WM2101	MOLEX	$ 0.18	$ 0.18
Total:							$ 7.34
CABLE_PM2		2	DIGIKEY	WM2101	MOLEX	$ 0.18	$ 0.36
	CIRCULAR TYPE 4 PIN MALE CONNECTOR	2	ARROW	9215PF5	AMP	$ 2.06	$ 4.12
	CIRCULAR TYPE 4 PIN FEMALE CONNECTOR	2	ARROW	9215PFZ	AMP	$ 1.52	$ 3.04
Total:							$ 7.52
CABLE_PM3	CIRCULAR TYPE 4 PIN MALE CONNECTOR	1	ARROW	9215PF5	AMP	$ 2.06	$ 2.06
	CIRCULAR TYPE 4 PIN FEMALE CONNECTOR	1	ARROW	9215PFZ	AMP	$ 1.52	$ 1.52
	CIRCULAR 3 PIN FEMALE CONNECTOR	1	IMSCO	MS3116F8-36	BENDIX		$ 0.00
Total:							$ 3.58
CABLE_PM4	CIRCULAR TYPE 4 PIN FEMALE CONNECTOR	2	ARROW	9215PFZ	AMP	$ 1.52	$ 3.04
	CIRCULAR TYPE 4 PIN MALE CONNECTOR	2	ARROW	9215PF5	AMP	$ 2.06	$ 4.12
Total:							$ 7.16
CABLE_RADIO1	CIRCULAR 8 PIN FEMALE CONNECTOR	1	IMSCO		BENDIX		$ 0.00
	D25 FEMALE CRIMP TYPE (STRAIGHT)	1	ARROW	9215PEA	AMP	$ 1.23	$ 1.23
Total:							$ 1.23
CABLE_uCB1	D25 FEMALE CRIMP TYPE (STRAIGHT)	3	ARROW	9215PEA	AMP	$ 1.23	$ 3.69
Total:							$ 3.69
CABLE_uCB3	D9 FEMALE CRIMP TYPE (STRAIGHT)	2	ARROW	9215PD6	AMP	$ 1.16	$ 2.32
	D9 MALE CRIMP TYPE (STRAIGHT)	1	ARROW	9215PD5	AMP	$ 1.16	$ 1.16
	D25 MALE CRIMP TYPE (STRAIGHT)	1	ARROW	9215PD9	AMP	$ 1.23	$ 1.23
Total:							$ 4.71

REPORT " BY CODE AND COST "
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CODE OF ASSEMBLY	DESCRIPTION OF ITEM	NUM PER ASM	VENDOR	VENDOR STOCK NUMBER	MANUFACTURER	COST	TOTAL
CABLE_uCB4	SMA MALE CLAMP TYPE RIGHT ANGLE CONNECTOR FOR RG-58	1	PASTERNACK	PE4029	PASTERNACK	$ 14.25	$ 14.25
	CIRCULAR 8 PIN FEMALE CONNECTOR	1	IMSCO		BENDIX		$ 0.00
	BNC MALE CRIMP TYPE CONNECTOR TO RG-58	1	PASTERNACK	PE4016	PASTERNACK	$ 1.60	$ 1.60
	BNC FEMALE BULKHEAD CONNECTOR	1	PASTERNACK	PE4078	PASTERNACK	$ 4.25	$ 4.25
Total:							$ 20.10
CABLE_uWSB1	N TYPE MALE CLAMP TYPE CONNECTOR TO RG-214	16	PASTERNACK	PE4132	PASTERNACK	$ 4.25	$ 68.00
	LOW LOSS SF214 COAX	1	TIMES WIRE AND CABLE			$ 40.00	$ 40.00
Total:							$ 108.00
CABLE_uWSB2	LOW LOSS SF214 COAX	1	TIMES WIRE AND CABLE			$ 40.00	$ 40.00
	N TYPE MALE CLAMP TYPE CONNECTOR TO RG-214	2	PASTERNACK	PE4132	PASTERNACK	$ 4.25	$ 8.50
Total:							$ 48.50
CABLE_uWSBD1	D25 FEMALE CRIMP TYPE (STRAIGHT)	4	ARROW	9215PEA	AMP	$ 1.23	$ 4.92
	D25 MALE CRIMP TYPE (STRAIGHT)	2	ARROW	9215PD9	AMP	$ 1.23	$ 2.46
Total:							$ 7.38
DIV_PLANE		1				$ 20.00	$ 20.00
Total:							$ 20.00
DOME		1				$ 300.00	$ 300.00
Total:							$ 300.00
FAN		1	ARROW		COMAIR-ROTRON	$ 40.00	$ 40.00
Total:							$ 40.00
PB	SMA FEMALE CONNECTOR, FLANGE MOUNT, SOLDER CUP TERMINAL	5	PASTERNACK	PE4000		$ 4.75	$ 23.75
	1000nF METALLIZED POLYESTER CAP	12	DIGIKEY	E2105		$ 0.75	$ 9.00
	PRINTED CIRCUIT BOARD	1	TRA			$ 250.00	$ 250.00
	10uH RF CHOKES	36	DIGIKEY	M8025	J.W. MILLER	$ 1.79	$ 64.44
	1500pF DISC	24	DIGIKEY	P4114		$ 0.94	$ 22.56

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CODE OF ASSEMBLY	DESCRIPTION OF ITEM	NUM PER ASM	VENDOR	VENDOR STOCK NUMBER	MANUFACTURER	COST	TOTAL
PB	PIN DIODE	24	HP	5082-3168		$ 0.83	$ 19.92
	100 OHMS, METAL OXIDE, 1Watt	3	DIGIKEY	P100W-1		$ 0.15	$ 0.45
	HEX SPACERS	10	DIGIKEY	J213		$ 0.45	$ 4.50
	D25 MALE CRIMP TYPE (STRAIGHT)	1	NEWARK	44F8681		$ 8.30	$ 8.30
Total:							$ 402.92
PBD	4.7uF TANT	1	JAMECO	TM4.7/35		$ 0.40	$ 0.40
	250uF ELECTROLYTIC	2	ARROW ELEC.	6816KQG		$ 0.99	$ 1.98
	NPN RF TRANSISTOR	14	NEWARK	MRF475		$ 13.12	$ 183.68
	POWER DISTRIBUTION STRIPS (.15uF)	3	ROGERS CORP.	QV-2 20.2.1(.15)		$ 3.64	$ 10.92
	10uF TANT	1	JAMECO	TM10/35		$ 0.59	$ 0.59
	0.1uF DISC	22	JAMECO	DC.1/50		$ 0.15	$ 3.30
	D25 MALE PC MOUNT TYPE (RIGHT ANGLE)	1	ARROW	9215PRP	AMP	$ 8.30	$ 8.30
	20-PIN MACHINE PIN DIP	2	DIGIKEY	C7220		$ 1.36	$ 2.72
	PRINTED CIRCUIT BOARD	1	TRA			$ 250.00	$ 250.00
	TRI-STATE OCTAL D-TYPE LATCH	2	JAMECO	74HC573		$ 0.89	$ 1.78
	HEX SPACER	8	DIGIKEY	J213		$ 0.45	$ 3.60
	PNP RF TRANSISTOR	14	ARROW ELEC.	1439CJW		$ 3.45	$ 48.30
	330pF DISC	14	JAMECO	DC330/50		$ 0.10	$ 1.40
	DUAL RS-232 VOLTAGE TRANSLATOR	7	ARROW ELEC.	2413ANQ		$ 0.89	$ 6.23
	5V REGULATOR, TO-92	1	JAMECO	78L05		$ 0.29	$ 0.29
	68 OHMS, 2W	14	DIGIKEY	P68W-2		$ 0.18	$ 2.52
	8-PIN MACHINE PIN DIP	7	DIGIKEY	C7208		$ 0.56	$ 3.92
Total:							$ 529.93
PM	POWER SUPPLY...DC TO DC CONVERTER	1	WESTCOR	VI-121-I	WESTCOR	$ 253.00	$ 253.00
	POWER SUPPLY...DC TO DC CONVERTER	1	ELCOM	BPS-12/125 0-D24	DATEL	$ 169.00	$ 169.00
Total:							$ 422.00
RACK_BOX		1	ARROW	1685BGG	BUD	$ 144.55	$ 144.55
Total:							$ 144.55
RADIO	VHF,UHF RADIO	1	IMSCO	ADC-MX,MR	IMSCO	********	$ 5,950.00
Total:							$ 5,950.00
uCB	28-PIN SKINNY DIP	1	JAMECO	28-PIN		$ 2.00	$ 2.00

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CODE OF ASSEMBLY	DESCRIPTION OF ITEM	NUM PER ASM	VENDOR	VENDOR STOCK NUMBER	MANUFACTURER	COST	TOTAL
				SKINNY D			
	A/D	1	MARSHALL	LTC1091		$ 11.00	$ 11.00
	D9 MALE PC MOUNT TYPE (RIGHT ANGLE)	1	ARROW	9215PRJ	AMP	$ 6.16	$ 6.16
	32Kx8 CMOS EPROM, 150ns	2	ARROW	2413BPL		$ 8.88	$ 17.76
	44-PIN PLCC SOCKETS	1	ARROW	9422BE7		$ 2.40	$ 2.40
	PRINTED CIRCUIT BOARD	1	TRA			$ 250.00	$ 250.00
	D25 MALE CRIMP TYPE (STRAIGHT)	2	NEWARK	44F8681		$ 8.30	$ 16.60
	47K OHMS, 1/4W	1	JAMECO	R47K		$ 0.05	$ 0.05
	1.8K OHMS, 1/4W	1	JAMECO	R1.8K		$ 0.05	$ 0.05
	2.2K OHMS, 1/4W	3	JAMECO	R2.2K		$ 0.05	$ 0.15
	3.3K OHMS, 1/4W	2	JAMECO	R3.3K		$ 0.05	$ 0.10
	68HC11A1 CPU	1	BELL	68HC11A1		$ 18.00	$ 18.00
	3K OHMS, 1/4W	1	JAMECO	R3K		$ 0.05	$ 0.05
	NPN GENERAL PURPOSE	1	JAMECO	2N3904		$ 0.12	$ 0.12
	510 OHMS, 1/4W	1	JAMECO	R510		$ 0.05	$ 0.05
	8-PIN BUSSED SIP, 5.6K	1	NEWARK	81F9204		$ 0.31	$ 0.31
	PCB SMA CONNECTOR	1	PASTERNACK	PE4000		$ 4.74	$ 4.74
	220 OHMS, 1/4W	1	JAMECO	R220		$ 0.05	$ 0.05
	QUAD BIFET OP-AMP	1	DIGIKEY	LF347N		$ 1.20	$ 1.20
	0.1u DISC	18	JAMECO	DC.1/50		$ 0.15	$ 2.70
	4.7K OHMS, 1/4W	5	JAMECO	R4.7K		$ 0.50	$ 2.50
				SPEAKER		$ 3.00	$ 0.00
	22p DISC	2	JAMECO	DC22/50		$ 0.10	$ 0.20
	PAL	1	ARROW	16L8		$ 2.60	$ 2.60
	8-PIN MACHINE PIN DIP	1	DIGIKEY	C7208		$ 0.56	$ 0.56
	10M OHMS, 1/4W	1	JAMECO	R10M		$ 0.05	$ 0.05
	4.7u TANTALUM	4	JAMECO	TM4.7/35		$ 0.45	$ 1.80
	10u TANTALUM	6	JAMECO	TM10/35		$ 0.59	$ 3.54
	50 PIV, 1A	2	JAMECO	1N4001		$ 0.10	$ 0.20
	0.01u DISC	2	JAMECO	DC.01/50		$ 0.10	$ 0.20
		1	BELL	MC34064	MOTOROLA	$ 3.00	$ 3.00
	8Kx8 SKINNY RAM	1	MARSHALL	HM6264ASP-120		$ 9.00	$ 9.00
	6-POSITION DIPSWITCH	1	JAMECO	206-6		$ 1.09	$ 1.09
	16-PIN MACHINE PIN DIP	2	DIGIKEY	C7216		$ 1.08	$ 2.16
	8-BIT, SI, LATCHED DRIVERS	1	NEWARK	UCN5895A		$ 2.86	$ 2.86
	5V REGULATOR, TO-220 CASE	1	JAMECO	7805T		$ 0.45	$ 0.45
	8V REGULATOR, TO-92 CASE	1	NEWARK	MC78L08AC		$ 2.00	$ 2.00
	14-PIN MACHINE PIN DIP	1	DIGIKEY	C7214		$ 0.94	$ 0.94
	-8V REGULATOR, TO-220 CASE	1	JAMECO	7908T		$ 0.49	$ 0.49
	MINI SPST	1	DIGIKEY	P9954		$ 0.26	$ 0.26
	TRI-STATE OCTTAL D-TYPE LATCH	1	JAMECO	74HC573		$ 0.89	$ 0.89
	VERSATILE INTERFACE ADAPTER	1	MARSHALL	R65C22J3E		$ 8.00	$ 8.00
	20-PIN MACHINE PIN DIP	2	DIGIKEY	C7220		$ 1.36	$ 2.72
	27K OHMS, 1/4W	1	JAMECO	R27K		$ 0.05	$ 0.05
	8MHz CRYSTAL	1	JAMECO	CY8		$ 1.19	$ 1.19

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uCB	52-PIN PLCC SOCKET	1	ARROW	9422BFA		$ 2.44	$ 2.44
	CMOS RS232 DRVR-RCVR	1	JAMECO	MC145406P		$ 2.95	$ 2.95
	28-PIN MACHINE PIN DIP	2	DIGIKEY	C7228		$ 1.92	$ 3.84
Total:							$ 389.47
uCB_BOX		1	GUDGELLS			$ 50.00	$ 50.00
Total:							$ 50.00
uWSB	CONNECTOR...N TYPE...FEMALE SOLDER CONNECTION BULKHEAD FEEDTHROUGH TO SEMIRIGID CABLE	9	HUBER SUHNER	24 N 50-3-14/133	HUBER SUHNER	$ 10.94	$ 98.46
	PIN DIODE , MADE BY UNITRODE	28	HALL MARK	UM7101A	UNITRODE	$ 13.00	$ 364.00
	PRINTED CIRCUIT BOARD	1	TRA			$ 250.00	$ 250.00
	CONNECTOR...SMA TYPE...MALE CLAMP RIGHT ANGLE TO RIGID CABLE	9	HUBER SUHNER	16 SMA 50-3-3c/111	HUBER SUHNER	$ 8.40	$ 75.60
	CAPACITOR...10 pF CHIP TYPE	28	ATC	100B100FP500X	ATC	$ 5.62	$ 157.36
	SMA FEMALE CONNECTOR, FLANGE MOUNT, SOLDER CONNECTION TERMINAL	9	PASTERNACK	PE4000	PASTERNACK	$ 4.75	$ 42.75
	SUBSTRATE FOR MICROWAVE BOARD	1	ROGERS CORP	RT/DUROID 5880 .125"	ROGERS CORP	$ 233.92	$ 233.92
Total:							$ 1,222.09
uWSBD	22pF DISC	14	JAMECO	DC22/50		$ 0.10	$ 1.40
	3.3uF TANT	1	JAMECO	TM3.3/35		$ 0.29	$ 0.29
	10uF TANT	1	JAMECO	TM10/35		$ 0.59	$ 0.59
	PRINTED CIRCUIT BOARD	1	TRA			$ 250.00	$ 250.00
	220pF DISC	14	JAMECO	DC220/50		$ 0.10	$ 1.40
	0.1uF DISC	37	JAMECO	DC.1/50		$ 0.15	$ 5.55
	TRI-STATE OCTAL D-TYPE LATCH	2	JAMECO	74HC573		$ 0.89	$ 1.78
	HEX SPACER	8	DIGIKEY	J213		$ 0.45	$ 3.60
	D25 MALE CRIMP TYPE (STRAIGHT)	2	NEWARK	44F8681		$ 8.30	$ 16.60
	POWER CONNECTOR	1					$ 0.00
	250uF ELECTROLYTIC	2	ARROW ELEC.	6816KQG		$ 0.99	$ 1.98
	TRI-STATE OCTAL DRIVER INVERTER	2	JAMECO	74S240		$ 1.39	$ 2.78
	20-PIN MACHINE PIN DIP	6	DIGIKEY	C7220		$ 1.36	$ 8.16
	5V REGULATOR, TO-220 CASE	1	JAMECO	7805T		$ 0.45	$ 0.45
	HEAT SINK FOR TO-220 CASE	1				$ 0.20	$ 0.20
	TRI-STATE OCTAL DRIVER	2	JAMECO	74S244		$ 1.19	$ 2.38
	PIN DIODE DRIVER	14	BELL	DH0035CG		$ 19.11	$ 267.54

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CODE OF ASSEMBLY	DESCRIPTION OF ITEM	NUM PER ASM	VENDOR	VENDOR STOCK NUMBER	MANUFACTURER	COST	TOTAL
			INDUST.				
	43 OHMS, 3W	14	DIGIKEY	P43W-3		$ 0.41	$ 5.74
	POWER DISTRIBUTION STRIPS (.15u)	11	ROGERS CORP.	QV-2 20.2.1(.15)		$ 3.64	$ 40.04
Total:							$ 610.48
uWSB_BOX		1	GUDGELLS			$ 50.00	$ 50.00
Total:							$ 50.00
Total:							$ 11,131.97

APPENDIX IX.D.

TRA CAPABILITY GUIDE

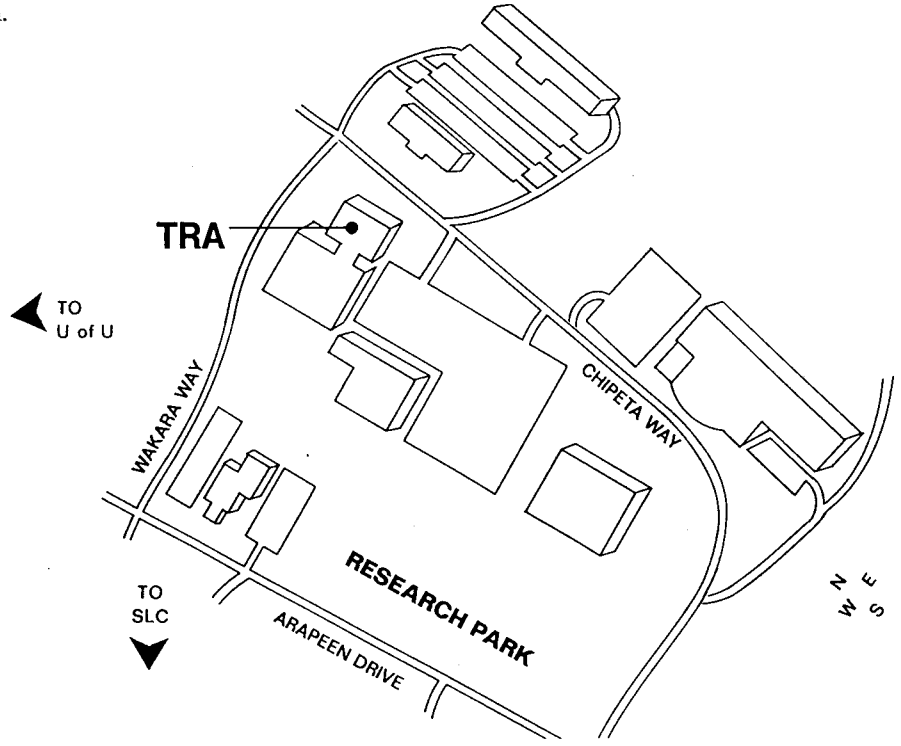
Technical Research Associates (TRA) was organized in 1983 to develop and commercialize new technologies. TRA is one of the most successful companies in the United States in obtaining research funding through the Small Business Innovation Research program sponsored by the federal government. As an outgrowth of the work performed by TRA researchers under this and other programs, the Company has developed and maintains the commercial rights to technologies in the areas of medical devices, materials strengthening, biotechnology, and communications. TRA has been successful in the commercial marketing of these products and technologies.

The Company's corporate offices and research laboratory facilities are located in the University of Utah Research Park, Salt Lake City, Utah.

tra

Technical Research Associates, Inc.
410 Chipeta Way, Suite 222
Salt Lake City, Utah 84108-1209
(801) 582-8080

Research
Product Development
Engineering Services
Process Trouble Shooting
Contract Manufacturing
Product Evaluation



The Company's offices and laboratory facilities are located in Research Park on the edge of the Wasatch mountains adjacent to the University of Utah and Fort Douglas.

tra

Technical Research Associates, Inc.

TRA MANAGEMENT

Charles D. Baker, PE, President and CEO. *Education:* Electrical Engineer, Long Beach College; Medicine, Boston University; Mechanical Engineering, West Coast University; Professional Manufacturing Engineer, CA. *Experience:* Program Management, Engineering Management, Technology Transfer, Medical Device Design, Materials & Processing Engineering, Electromechanical Packaging, Government & Industrial Standards, Spacecraft Hardware Design, Polymer Processing. *Publications:* Eleven patents and twenty-six publications in fields of expertise. *Associations:* Member ASME, SME, Rotary International and Salt Lake Chamber of Commerce.

Jeffrey R. Clark, CPA, Financial Vice President. *Education:* BS Accounting, Brigham Young University; MBA Management, Brigham Young University; CPA, Texas. *Experience:* Financial Forecasting and Budgeting, Accounting Systems Design, Accounting Management, Computer Programming, Corporate Taxation, Federal Government Contract Administration, Subcontractor and Project Management.

Joseph K. Weeks, MS, Marketing Vice President and Manager Materials Division. *Education:* BS, MS, Chemical Engineering, University of Utah. *Experience:* Product and Process Development of metal-matrix composites, reinforced with continuous and nano-sized ceramic reinforcements. Ceramics, cemented carbides. Kinetics and catalysts. Photochemical etching. Emulsion explosives. *Publications:* One patent and 17 publications in fields of expertise. *Associations:* Member AICHE and ASM International MRS.

Gail Bowers-Irons, BS, Manager Biotechnology Division. *Education:* BS Chemistry, University of Utah. *Experience:* Biotechnology, Waste Water Treatment and Analysis, Analytical Chemistry, Polymer Extraction and Separation. *Publications:* One patent pending and eight publications in field of expertise.

Owen D. Brimhall, BS, Manager Bioengineering Division. *Education:* BS Mechanical Engineering, Brigham Young University. *Experience:* Product Development, Design of medical implants and instrumentation. Blood separation methods, applications of ultrasound. Design and Fabrication of research instrumentation and prototypes, CAD, Commercial Art, Drafting, Electronic Technician. *Publications:* Four patents and seven publications in field of expertise. *Associations:* Member ASME, Professional Engineer, Utah (1st half complete).

Thomas J. McLaughlin, BS, Program Manager, Communications/Electronic Development. *Education:* BS, BSEE Electrical Engineering, University of Utah. *Experience:* Microprocessor/Digitalk Design, Analog Electronics, Assembly Language Programming, Acoustics, and Control Systems. *Publications:* Four patents and two publications in field of expertise.

tra

Technical Research Associates, Inc.

TRA KEY PERSONNEL

Kameron Behzadian, ME, Mechanical Engineer. *Education:* BS, ME, Mechanical Engineering, University of Utah. *Experience:* Vibration, acoustics, strength of materials, stress and fatigue analysis, fluid mechanics.

Nathalie Chevreau, PhD, Research Scientist. *Education:* BS Organic Chemistry, MS Inorganic Chemistry, PhD, Solid State Inorganic Chemistry, University of Bordeaux, France. *Experience:* Solid state inorganic chemistry, chemical and physical properties of materials, synthesis and characterization of barium ferrites for high density magnetic recording applications, techniques for the preparation of colloidal sols of various oxides. *Publications:* One patent pending and ten publications in field of expertise.

Chantal Gensse, PhD, Senior Scientist. *Education:* BS Geochemistry, Doctorat Chemistry, University of Paris; PhD, Ceramic Engineering, University of Illinois. Experience: Ceramic Precursors, Ultra Fine Powders, Sol-Gel Processes, Ceramic Processing. *Publications:* One patent pending, 9 publications and communications.

Allen D. Labrecque, PhD, Research Scientist. *Education:* BA, Genetics Cytology, MA Molecular and Genetic Biology, PhD, Human Anatomy/Physiology, University of Utah; OD Optometry, New England College, Boston. *Experience:* Human Histology, Enzyme Technology and Cell Culture, Endocrine Tumor Biology, Ocular Biology, Refraction and Contact Lenses. *Publications:* Eleven papers in field of expertise. *Associations:* Member Sigma Xi, AAAS, Tissue Culture Association, American Optometric Association.

James E. Messinger, Electrical Engineer. *Education:* University of Utah 1981-1986, Electrical Engineering. *Experience:* Digital and analog design, computer programming, microprocessor applications, biomedical instrumentation. *Publications:* Two papers, one patent.

Robert W. Okey, PE, Civil Engineer. *Education:* BS Agricultural Engineering, Iowa State College; BS, Civil Engineering, MS, Civil and Sanitary Engineering, University of Washington. *Experience:* Waste management design or analysis problems, laboratory studies of treatability or biodegradability, detailed field studies of waste character and origin, stream studies and environmental impact studies. *Publications:* Three patents and seventy papers in field of expertise. *Associations:* Adjunct Professor, University of Utah; American Society of Civil Engineers; Professional Engineer.

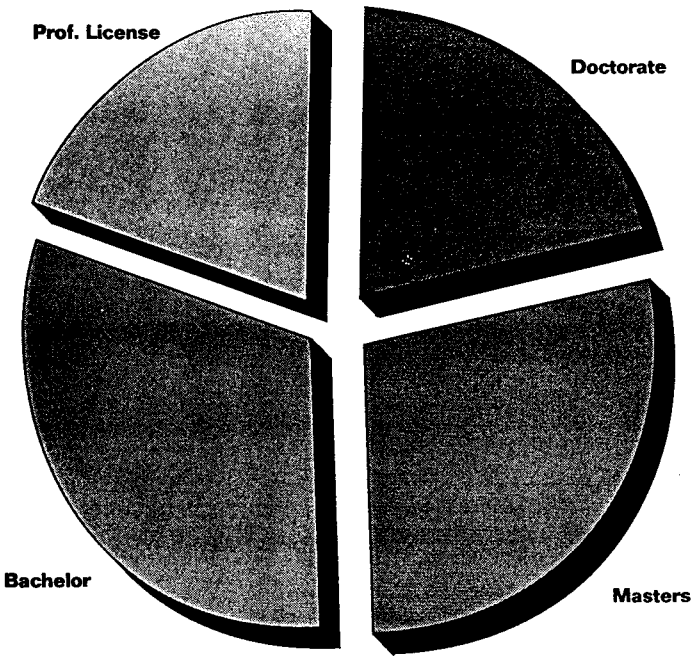
Robert J. Pryor, BS, Biologist. *Education:* BS Cellular Biology and Genetics, University of Utah. *Experience:* Application of microorganisms to biorecovery of metals and paint degradation. Operation and laboratory analysis using SEM, EDAX and optical microscopy.

Dilip N. Ghosh Roy, PhD, Senior Scientist. Education: BS Mechanical Engineering, University of Jadaupar; MS Mathematics, University of Jadaupar; PhD, Astronautical Sciences, Northwestern University, Illinois. *Experience:* Plasma physics, lasers and light scattering. *Publications:* Forty-five publications, one book and one review article in field of expertise.

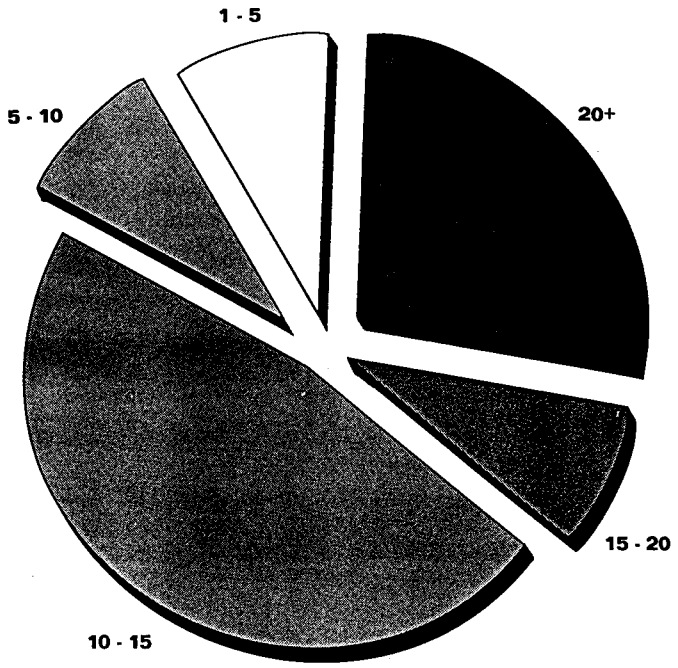
Sam L. Sparks, PhD, Senior Scientist. *Education:* BSEE, Electronic Engineering, California State Polytechnic University; PhD, Physiology and Biophysics, University of Washington. *Experience:* Human and Animal Sensory Physiology, Electrical Circuit Analysis, Mathematic Modeling, Project Management, Corporate Management, and Personnel Test Developer. *Publications:* Two patents, one pending, and two publications in field of expertise. Amateur Extra Class radio license (KD7K).

TRA STAFF CAPABILITIES

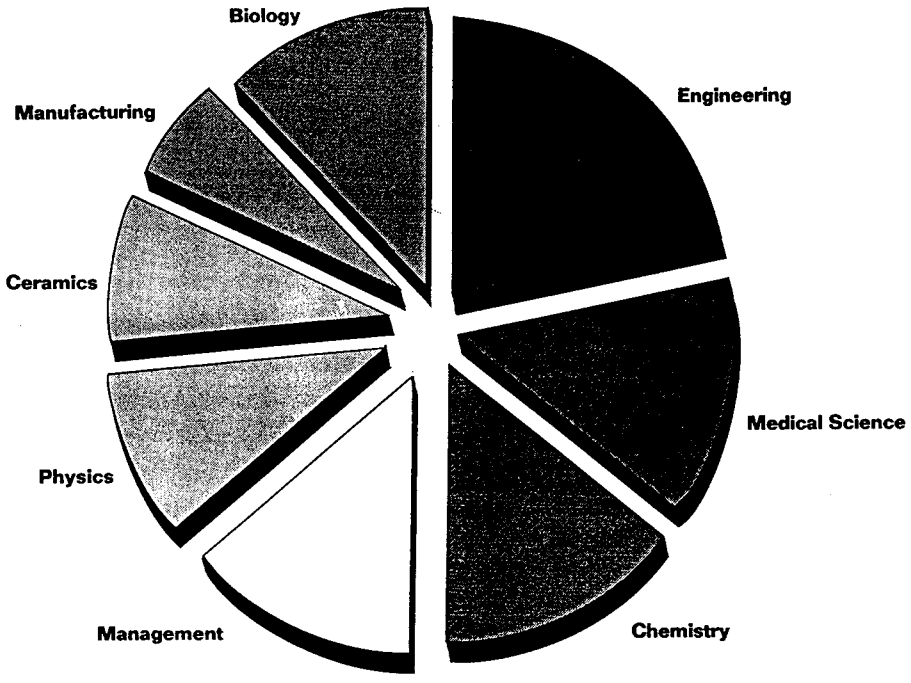
TRA has an experienced staff with an established and respected performance record. Following is a summary of TRA's staff capabilities:



EDUCATION

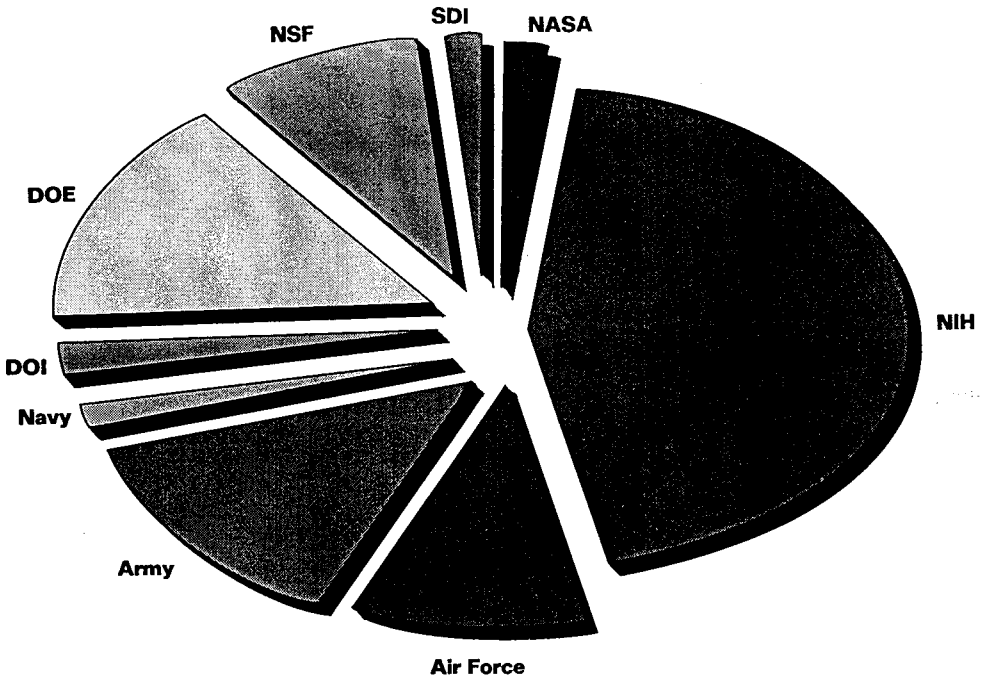


YEARS EXPERIENCE

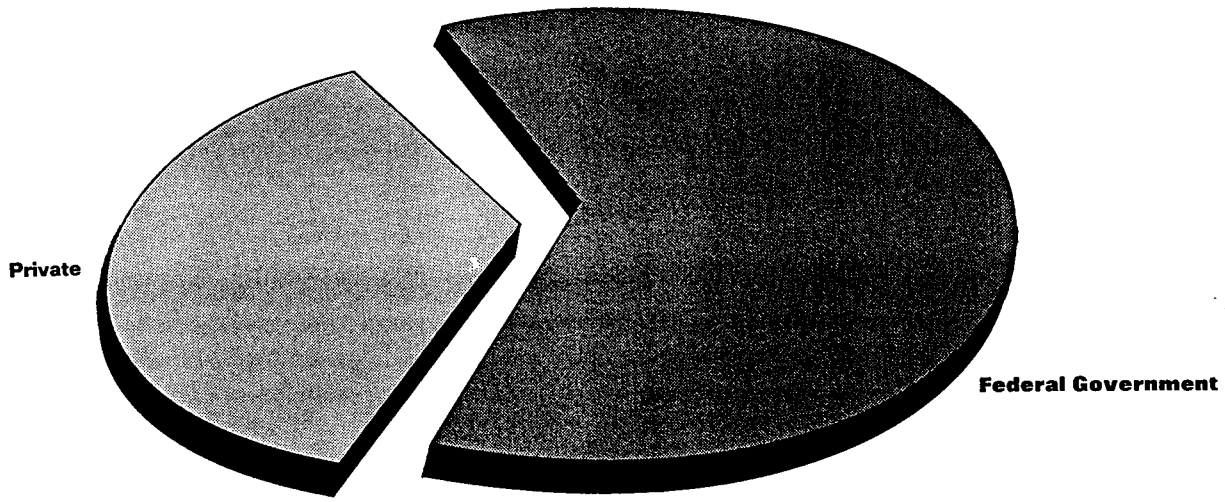


BACKGROUND

TRA CONTRACT RESEARCH EXPERIENCE
1983-1988



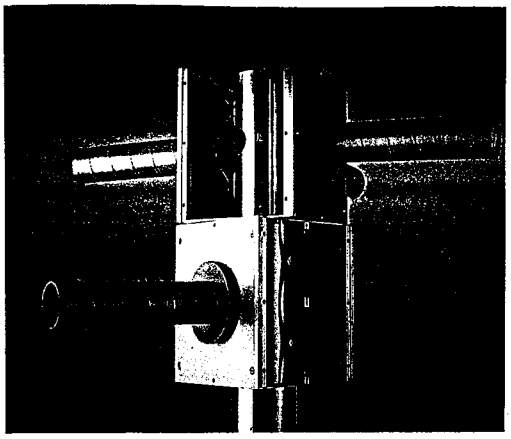
GOVERNMENT SPONSOR BREAKDOWN



SPONSOR SOURCE

tra

Technical Research Associates, Inc.



Computer-controlled antenna being developed by TRA to enhance the mobility and range of robotic vehicles.

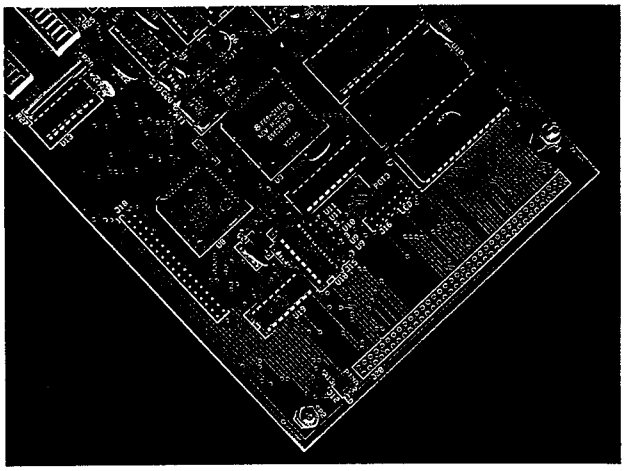
ELECTRONICS AND COMMUNICATIONS

Major Programs:

Computer Controlled Antenna Systems: TRA has completed a contract with the U.S. Army to supply an antenna system that substantially increases the range and mobility of robotic vehicles. Commercial applications include equipping U.S. Forest Service, Fire and Police vehicles with "smart" antenna systems that will increase range and enhance received signals.

Ultrasound Control Systems: TRA has developed several control systems for specialized ultrasound separation systems. These microprocessor based particle separation systems have applications in many medical and industrial areas.

Instrumentation: Microprocessor based instrumentation has formed the core of numerous TRA projects, including a computer controlled agile beam antenna, computer controlled bioreactors, and various computer controlled medical devices. The use of programmable logic devices has enabled TRA to reduce board size and complexity in recent projects. TRA has extensive experience in biomedical instrumentation, data acquisition, imaging devices, and filtering and amplification of low-level and biological signals. TRA's designers are proficient in assembly and high-level programming, and in design and layout of printed circuit boards on an internal CAD system. In the communications field TRA recently designed and built a computer controlled VHF phased array and a 2 GHz eight throw PIN diode switch.



Circuit developed by Company researchers to direct TRA's computer-controlled antenna.

Equipment Available:

Electronics

1. Compilers/assemblers for 68HC11, 8096, 8051, Z80, 6805 and PIC16C54
2. Logic analyzer (Orion Unilab) support for compiler/assemblers
3. Programmable logic device programmer/software
4. PCB design and layout software
5. Analog simulator software
6. Full range of electronic test equipment

Microwave/RF Design

1. HP8410 network analyzer 100 MHz to 18 GHz
2. 2 GHz frequency counter
3. Touchstone microwave CAD software

Thomas J. McLaughlin, Program Manager
410 Chipeta Way, Suite 222 ▪ Salt Lake City, Utah 84108-1209 ▪ (801) 582-8080 ▪ FAX (801) 582-8182

TRA PRODUCT DEVELOPMENT FACILITIES

TRA was established in 1983 by five engineers and scientists from the University of Utah Research Institute. The company has grown to a company of forty and is recognized for outstanding innovative work and unusual success in the commercialization of products from research.

TRA is engaged in the development of products through research in four specific disciplines: Bioengineering, Materials Improvement, Biotechnology and Communications. Each of these commercially important areas is heavily supported by grant and contract awards from both the federal government and the business community. TRA has received research and development contracts from NIH, NSF, DOE, SDI, Army, Navy, Air Force and NASA. Many of these development contracts have been carried to commercialization through contract extension, license, royalty and outright sale. As a result, the company has product license agreements with companies in the USA, Japan and Canada. TRA is currently preparing for the commercial introduction of a strengthened metal product and is engaged in the marketing of several environmentally safe metals-extraction processes utilizing biotechnology.

TRA continues to improve the capability of its facilities through acquisition of new equipment, expanding and modifying laboratory space, and training of staff members. As an example, in 1988-89 TRA acquired two specialized microscopes for examination of metallographic samples and evaluation of biological specimens, a Hewlett Packard gas chromatograph/MS, and a Milton Roy UV-VIS spectrophotometer.

Computer Services

Computers: 80386, 80286 and MacIIcx systems, laser printers, scanners, flatbed and pinch-roller type plotters

Software: CAD systems, schematic capture and printed circuit board layout software, analog and digital simulation software, assemblers, compilers, mathematical modelers

Development Shop

Digital milling machine
12" swing lathe
36" brake and roll former
Drill presses
Tool grinders
Band saw
Combined pressure/vacuum chamber
Bead blaster
Hand tools, bits, end mills, etc.
Measuring and inspection equipment
Polymer processing equipment

Research and Development

Laboratory Space (Sq. Ft.)

Bioengineering	800
Materials	900
Biotechnology	700
Communications	300
Computer Services	300
Development Shop	500
Storage	400
Research Personnel	4300
Administration	1300
Total	9500

APPENDIX IX.E.

PHASE I FINAL REPORT

Phase I Objectives

The overall Phase I objective will be to design, build and test an ESABA that operates in the 440 MHz. amateur band and provides a steerable beam for maintenance of AX.25 protocol digital communications from a moving vehicle. The following tasks are proposed to achieve this goal in the 6 month Phase I period:

Task 1. Design and construct a phased four element vertically polarized 440 MHz. antenna array. The vertical elements will operate over a ground plane.

Task 2. Design and construct a PIN diode switching and phasing assembly. The PIN diodes will allow rapid (less than 10 microsecond) RF switching by a dedicated microprocessor. The phasing assembly will contain power splitters (Wilkinson type) and phasing (delay) lines.

Task 3. Write assembly language routines for the microprocessor to allow manual steering of the beam as well as a simple automatic sweep. A simple single board Z-80 microcomputer will be used as the controller.

Task 4. Modify a commercially available FM transceiver for operation with the system. Modifications will include signal level output (for subsequent A/D conversion) and adaptation of the transceiver to a packet (digital) terminal node controller (TNC).

Task 5. Test the system in manual mode. Complete any required adjustments and debugging.

Task 6. Design, build and test four bit A to D flash converters (conversion times less than 0.1 microseconds), and interface the converters between the transeiver and microcomputer. The converters will provide 16 level measurement of signal strength in each of four quadrants of beam direction.

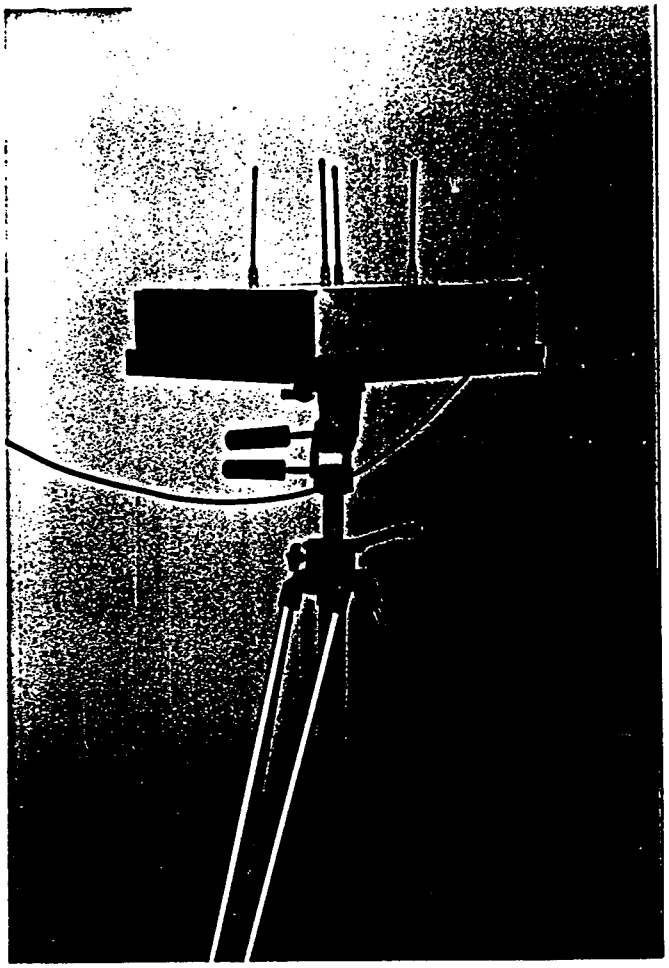
Task 7. Write and debug software for quadrant level detectors and a rapid scanning algorithm. The algorithm will determine the quadrant with the highest signal strength and point the beam in that quadrant. Periodically the beam will sweep through all four sectors in order to determine if the antenna beam should be directed to another quadrant due to vehicular movement.

Task 8. Test the entire system in a moving vehicle and over terrain which results in a marginal communications link.

Task 9. Write final report. The deliverable will be the final report containing system performance data and recommendations for Phase II development work.

Task 1.

The first task was to design and construct a four element, vertically polarized 440 MHz antenna array. As was indicated in the Phase I proposal, four quarter wave vertical antennas over a ground plane and placed at the corners of a square (0.25 wavelengths on a side) would have a cardioid shaped radiation pattern if driven suitably. The proposed array was constructed and is shown in Photograph 1.



Photograph 1

A chassis box was mounted beneath the ground plane to contain the phasing and switching assemblies as well as the on board computer, sample and hold, and power supply circuitry. The purpose of the phased array was not to construct the ultimate antenna but to provide proof of concept of the ESABA system as a hole.

Note on additional work done.

The principal investigator had the opportunity to visit an AGVT

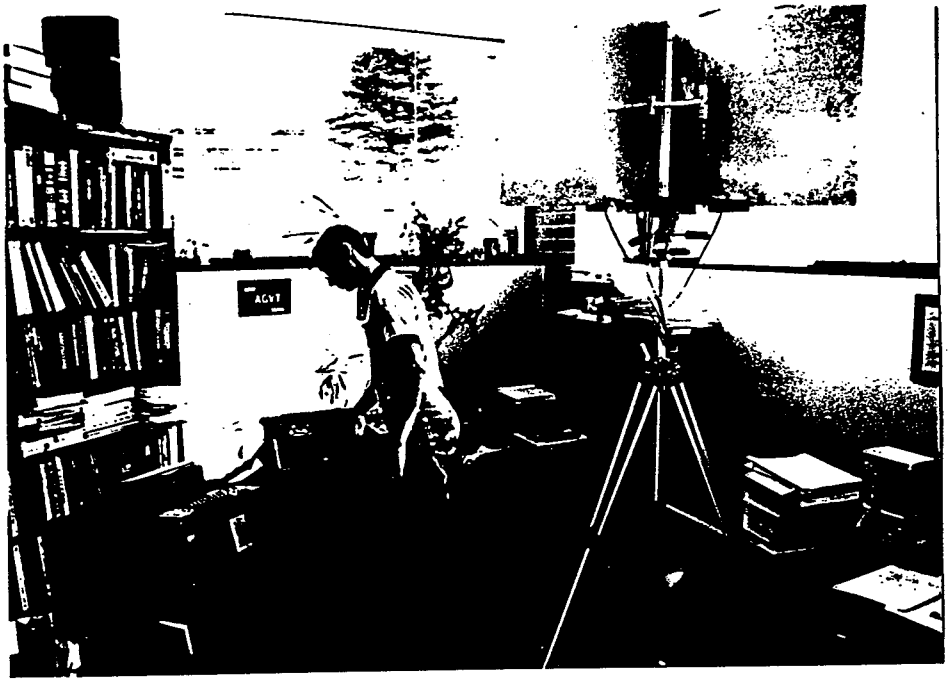
demonstration in January at the Martin Marietta Facility. During this visit it became apparent that the phased array built above would not provide the gain (directivity) equivalent to that of the mechanically steered antenna currently mounted on the vehicle. Thus TRA felt that a different approach also be investigated. Corner reflector antennas have the desireable features of easy construction, high front to back ratios, relatively high gain (to about 17dBi) and easy configuration as a switched array. Photograph 2 (below) and Figure 3 (page 7) show a cardboard model of a six over six array of 60 degree corner reflectors scaled to a frequency of 2.0 GHz.

Photograph 2

It is estimated that an array of this size would provide a gain of about 10dB per corner reflector, a gain equivalent to the single horn antenna currently in use. As can be estimated from the photograph, the size of the entire array is similar to the overall size of the horn and its gimbal assembly. The corner array antenna offers the additional advantage of increased survivability. If one corner unit is hit the other 11 antennas

can still provide only slightly reduced performance. In fact if six antennas in the array were disabled in random position the robotic vehicle might successfully operate with the remaining six antennas. This style of antenna would be switched but not phased.

The actual proof of concept antenna that was built is shown in Photograph 3. Recall that the Phase I radio system operates at 440 MHz so that the size of the 4 corner reflector array is almost 5 times larger than a similar antenna designed to operate at 2 GHz. Scaled drawings of the phased array and the switched 4 corner array are included as Figures 1 and 2 respectively.



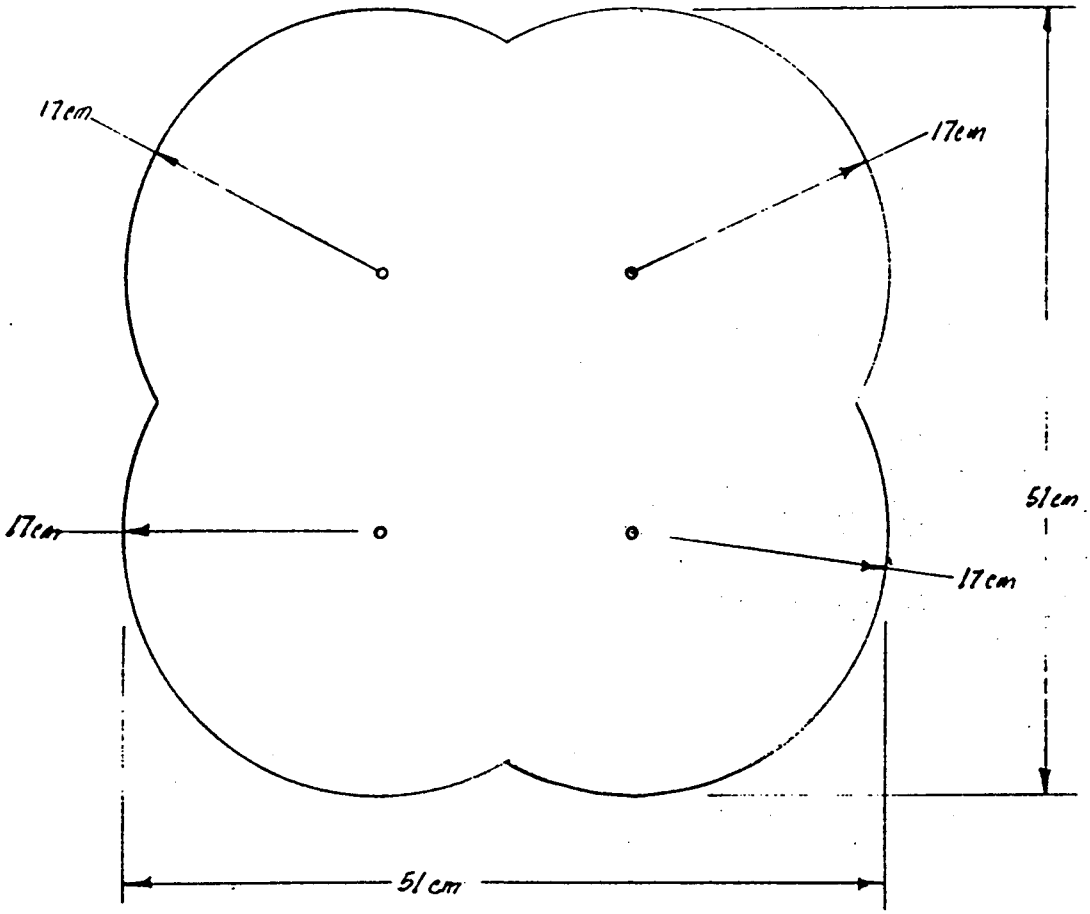
Photograph 3

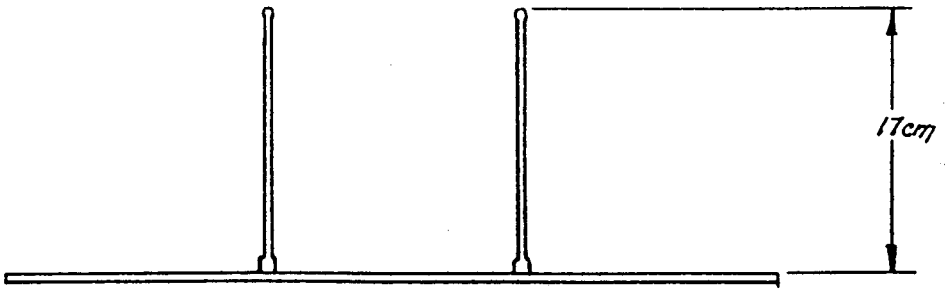
Task 2

Task 2 includes the design and construction of the PIN switching and phasing assemblies for the phased array as well as the additional task of designing and building the switcher for the corner array. The schematic for the phasing, Wilkinson power splitter and impedance matcher is illustrated in Figure 4. The device was built as illustrated in Figure 5. The phasing assembly shown produced measured phase shifts shown in Table 1.

Table 1 Phase angle, degrees

Port	Measured	WRT Ref.	Desired
B	130	0	0
A	20	-110	-110
D	35	-95	-110
C	-90	-220	-220

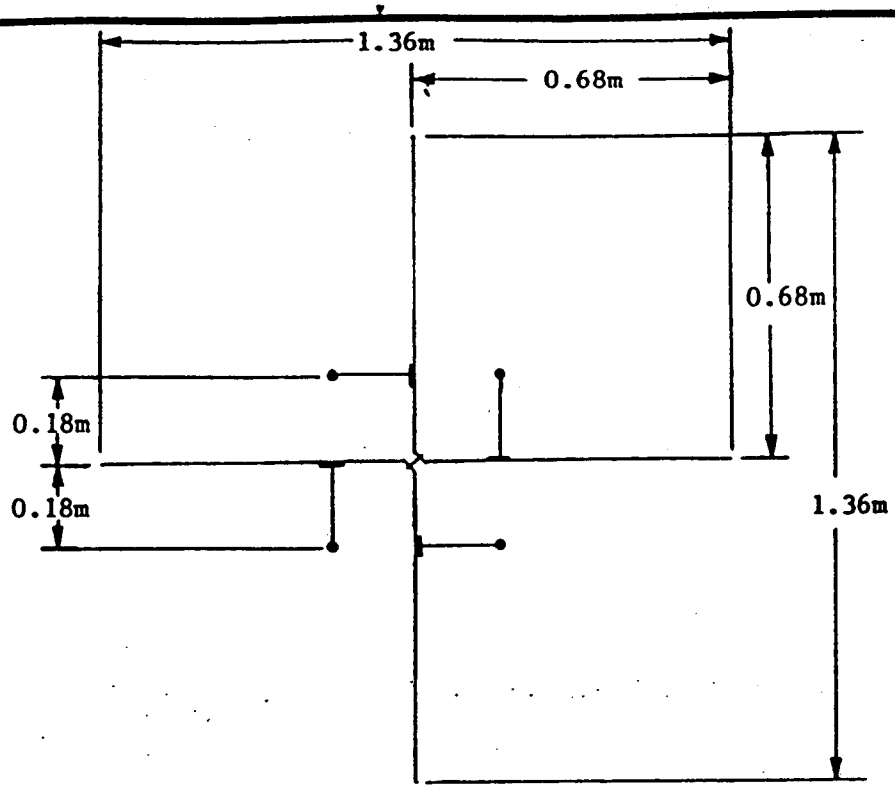




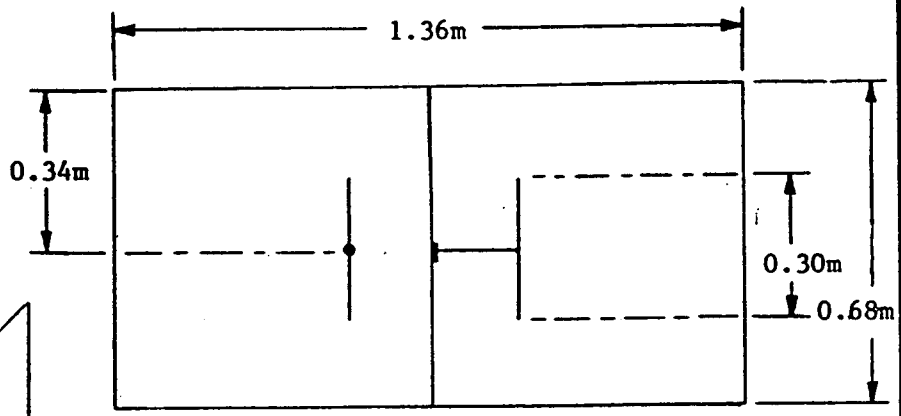
PHASED ARRAY

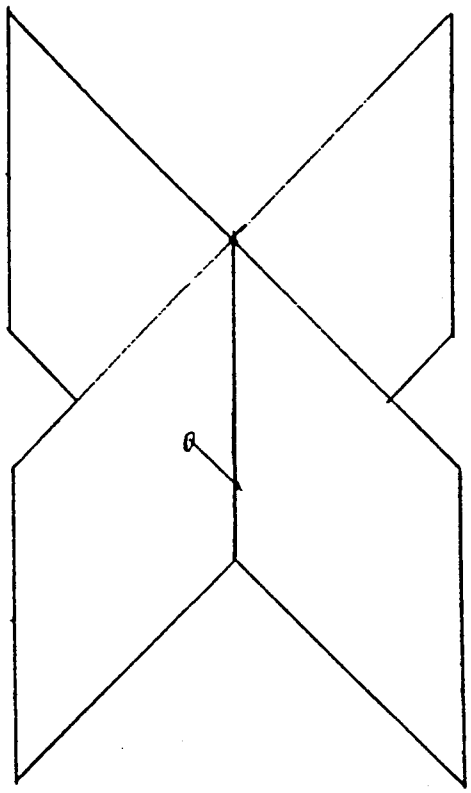
SIZE	CODE IDENT NO.	DRAWING
	FIG. 1	
SCALE		SHEET

TOP VIEW



SIDE VIEW





SIZE	CODE IDENT NO.	DRAWING
	FIG. 2	CORNER REFLECTOR ANTENNA
SCALE		SHEET

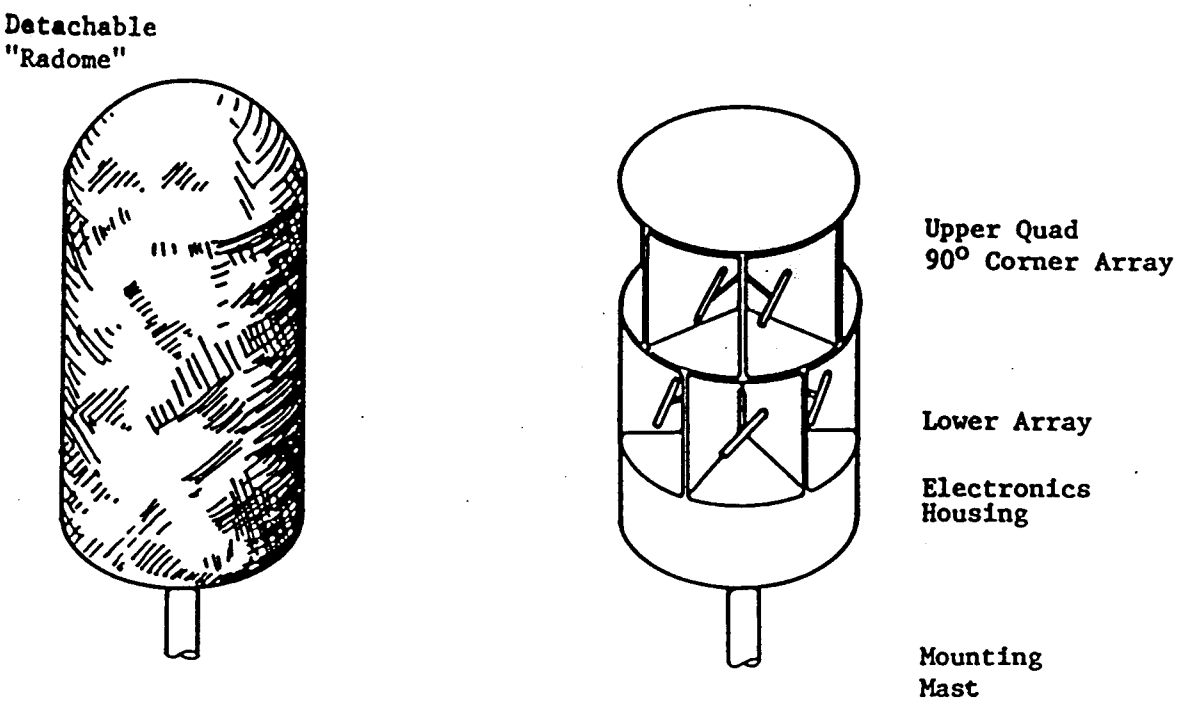
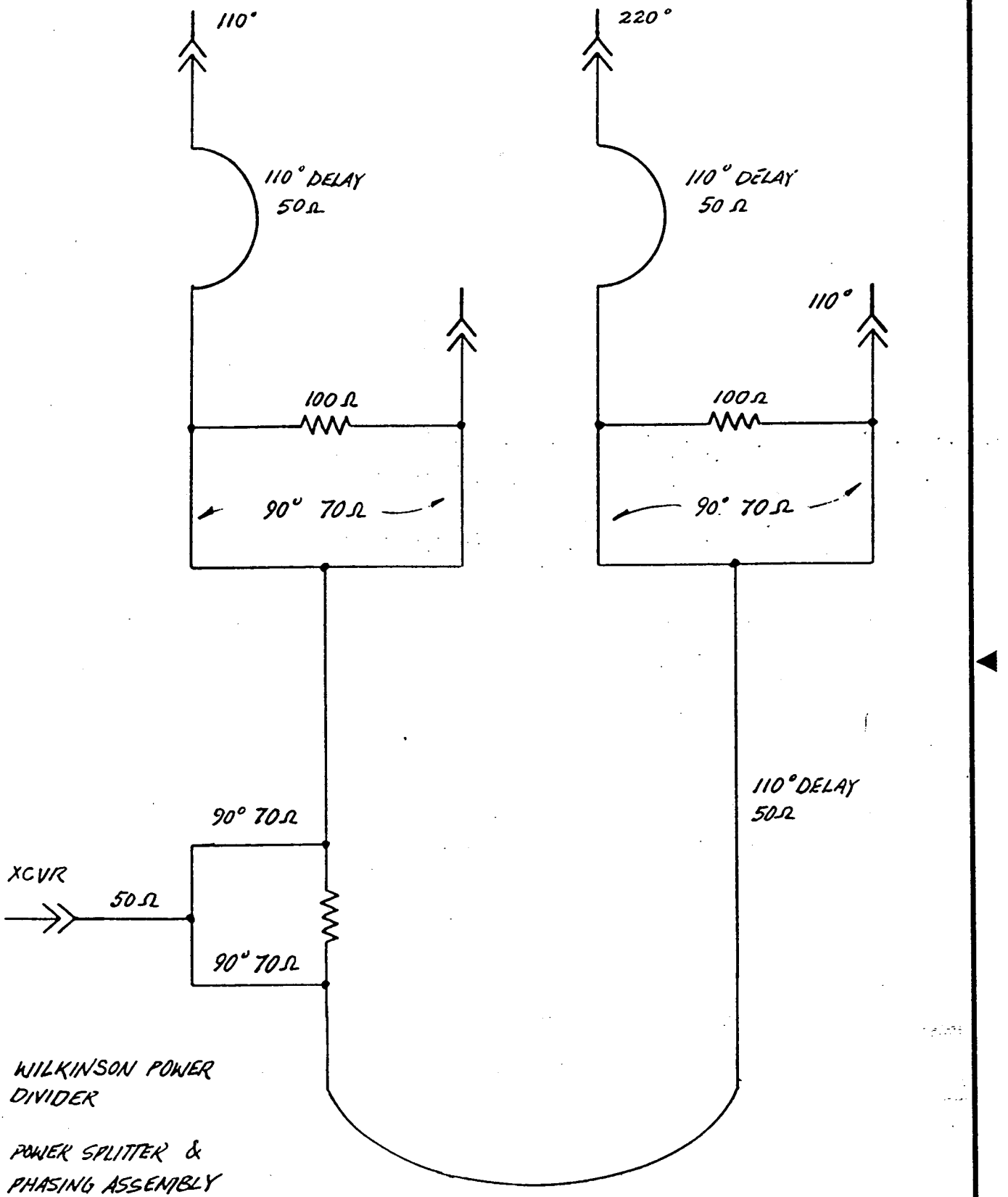

Detachable
"Radome"
Upper Quad
90° Corner Array
Lower Array
Electronics
Housing
Mounting
Mast

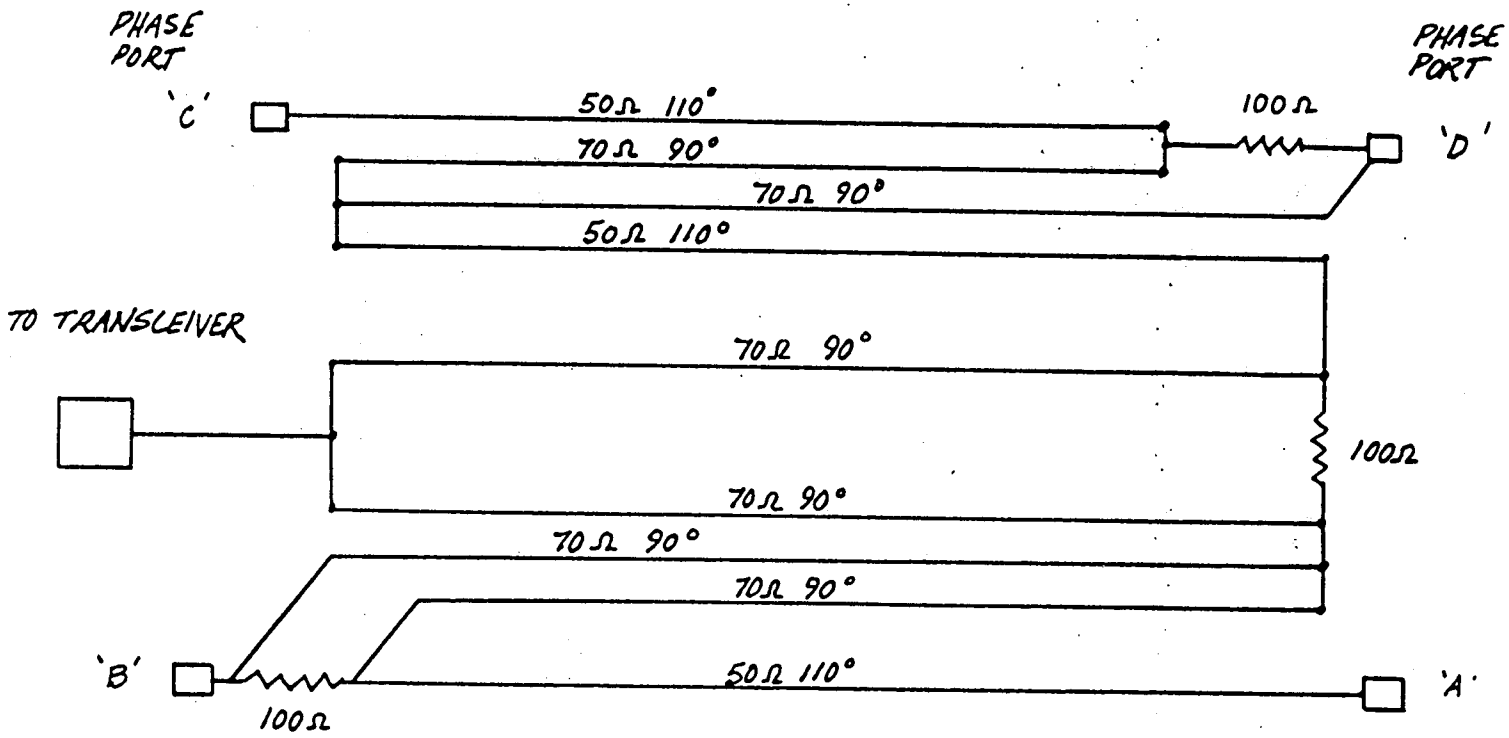
FIGURE 3



WILKINSON POWER DIVIDER

POWER SPLITTER & PHASING ASSEMBLY

SIZE	CODE IDENT NO.	DRAWING
	FIG. 4	
SCALE		SHEET



ALL LINES COAX. SHIELD TO GROUND

90Ω 110° LINES 13.7cm

70Ω 90° LINES 13.4cm

PHASING LINE SUBASSEMBLY / WILKINSON POWER DIVIDER

FIG. 5

The 15 degree deviation of port D should result in a slight skewing of the beam but should not affect the overall proof of concept.

The PIN switcher used to switch the phased array is shown in Figure 6 which illustrates the actual circuit diagram of the switch and Photograph 4 shows the constructed switch.

An additional PIN switch was constructed to switch the four corner reflector array. The principle of the switched corner reflectors is illustrated in Figure 7. The schematic of the switcher is shown in Figure 8 and the device is illustrated in Photograph 5.

Task 3

Software routines for manual control and preliminary tests.

Manual control of the antenna system was implemented so that an operator can type in "Q1" to set the system to quadrant 1, "Q2" to set the antenna to quadrant 2, etc. Since this "manual" mode does not require fast execution, this software was written in the computer language Forth and burned into the system EPROM. The Forth code written for this project is in the software appendix under the heading "Forth Code".

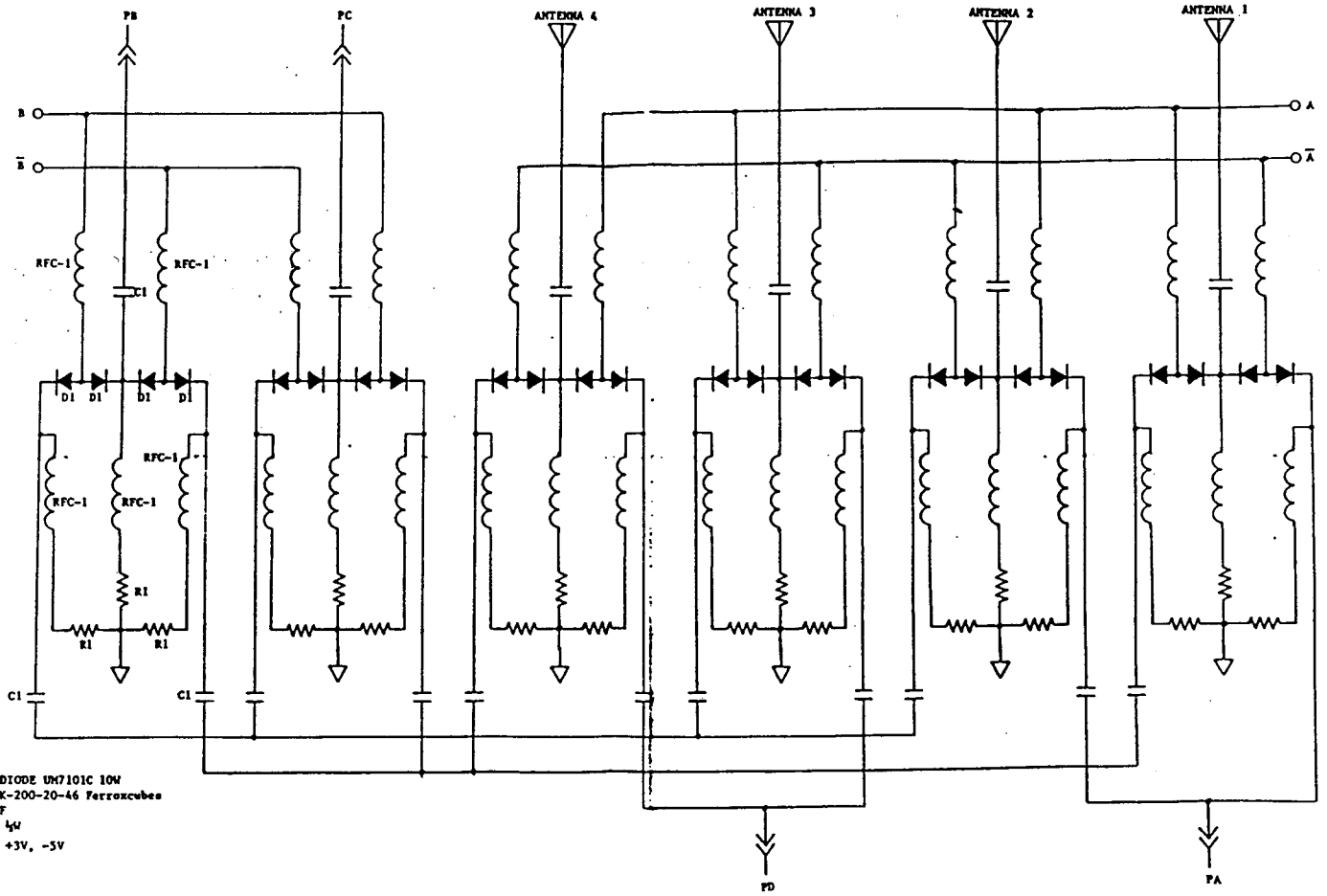
The final system software includes assembly language routines which incorporate "automatic sweep" functions. This software will be discussed under Task 7.

Task 4

This task includes the modification of the commercially manufactured 440 MHz transciever and the design and construction of an interface circuit between the transciever and the sample and hold circuit. The low battery indicator circuit was altered to produce a more realistic assessment of battery condition. Details of the modification are not included here since they are not relevant to the project.

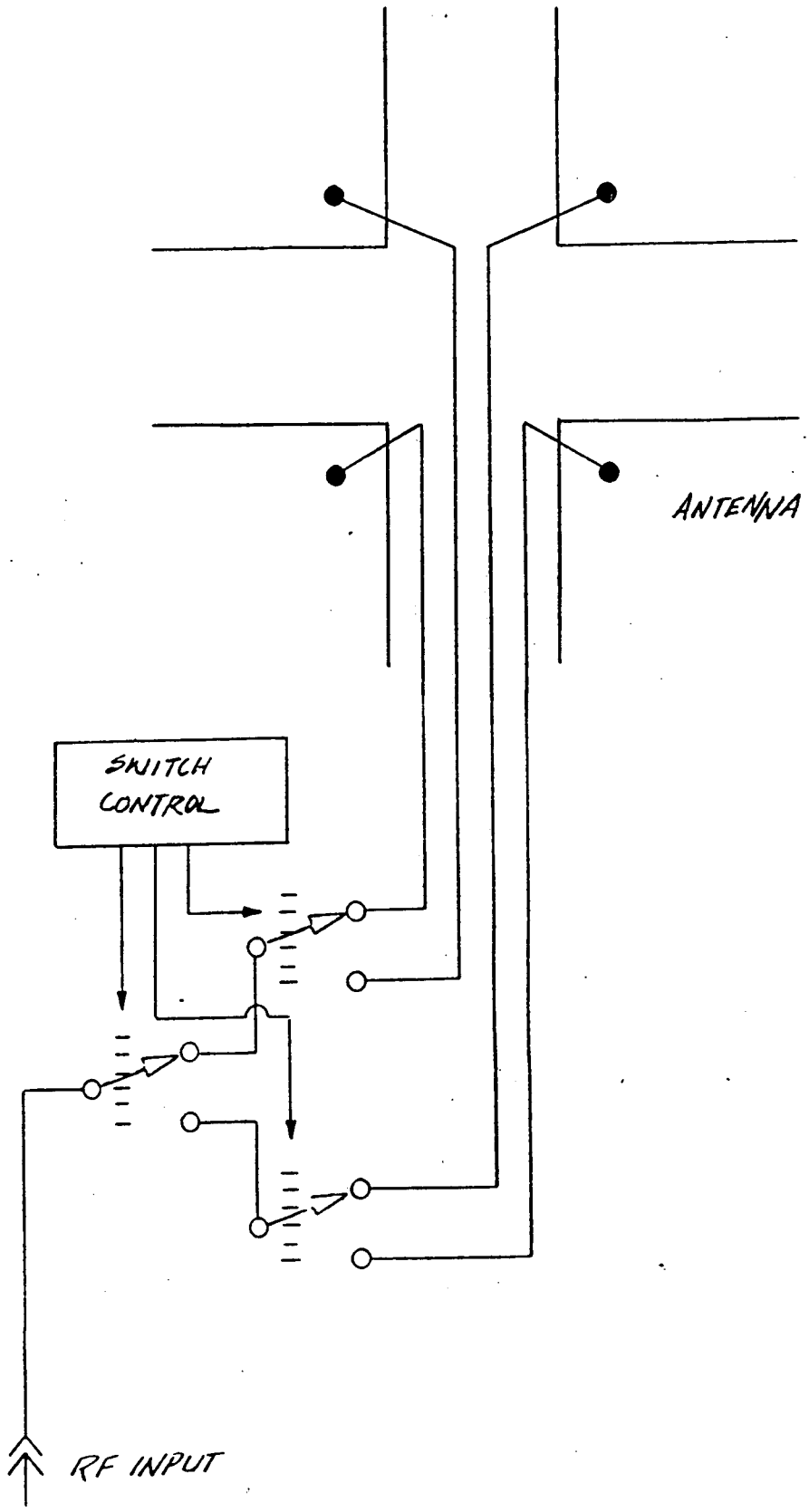
Figure 9 shows the schematic of the IF amplifier and level converter circuit. The input to the amplifier connects to a LM358 voltage follower installed in the radio which in turn connects to pin 5 (455 kHz input) of the MC 3357P IF IC. The LM358 acts as a buffer between the radio and the outside world. In addition the squelch line was brought out of the radio. The level converter produces a DC signal whose amplitude is proportional to RF input signal strength. This signal is used by the sample and hold

PIN DIODE SWITCHING CIRCUIT



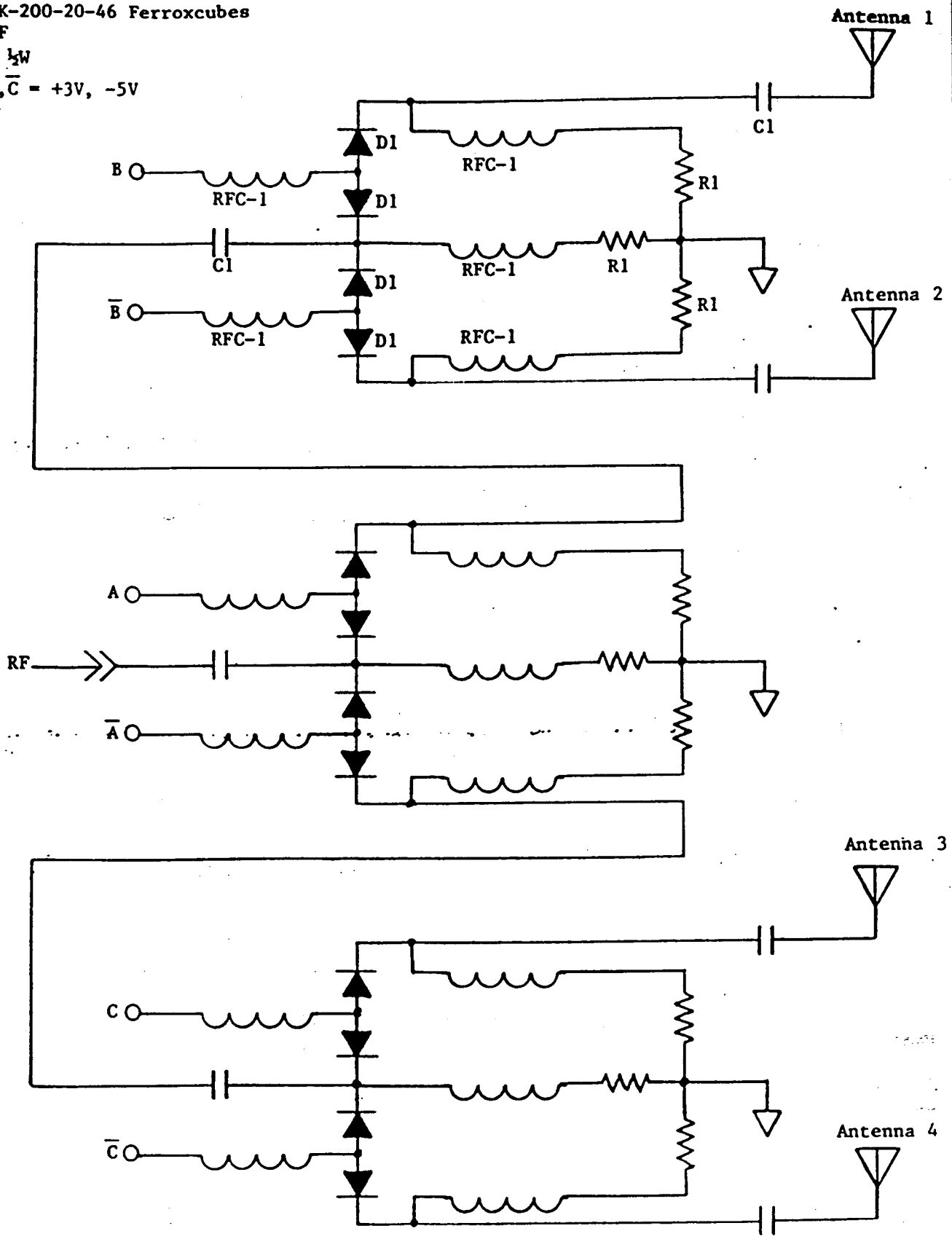
D1 = PIN DIODE UM7101C 10W
RFC-1 = VK-200-20-46 Ferroxcubes
C1 = 471pF
R1 = 68Ω, ¼W
A, $\overline{A}$, B, $\overline{B}$ = +3V, -5V

FIG. 6

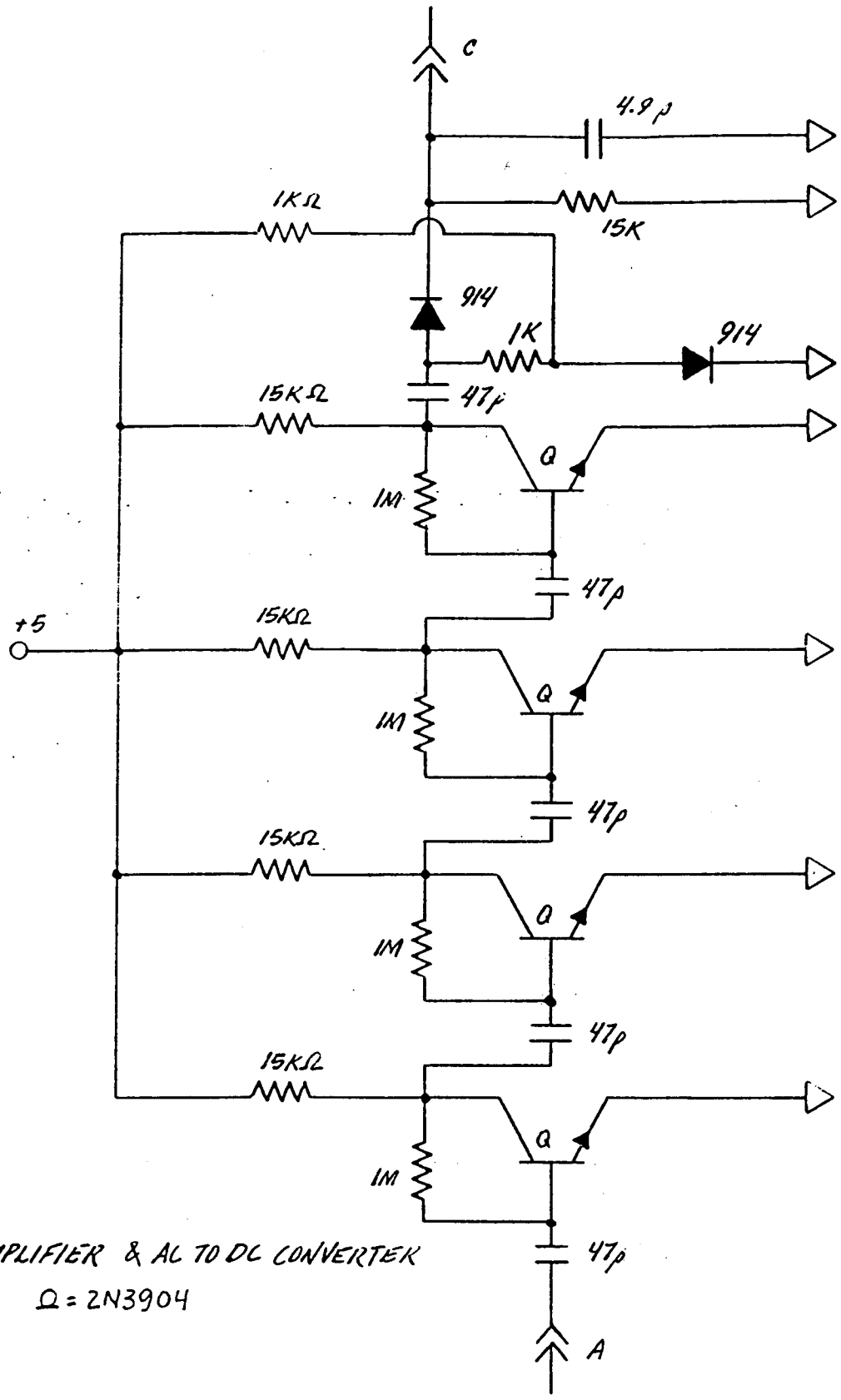


SIZE	CODE IDENT NO.	DRAWING NO.
	FIG 7	
SCALE		SHEET

D1 = PIN DIODE 5082-3379
RFC-1 = VK-200-20-46 Ferroxcubes
C1 = 471pF
R1 = 68Ω, ½W
A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$ = +3V, -5V



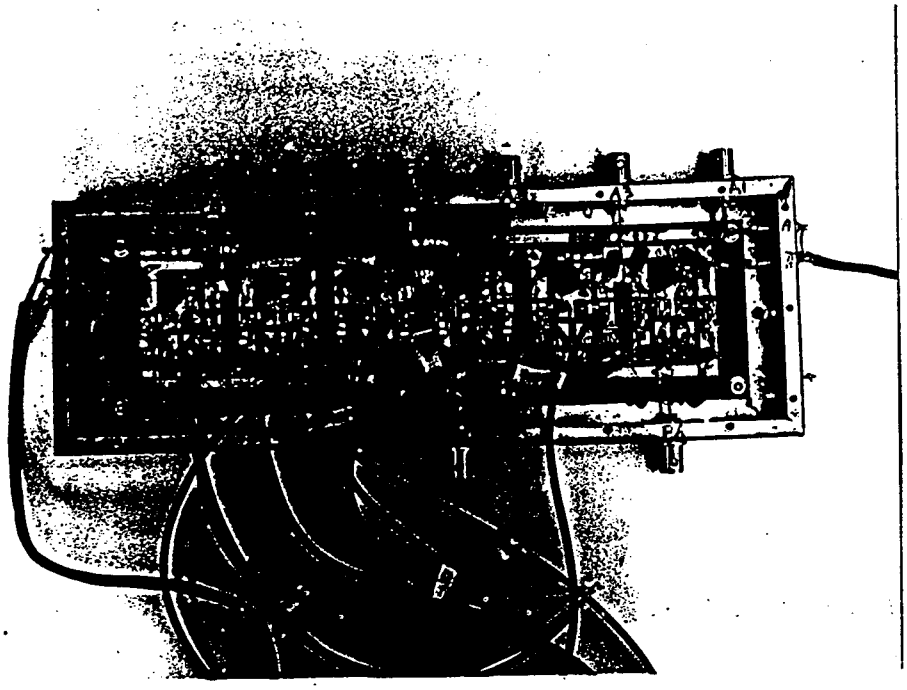
SIZE	CODE IDENT NO.	DRAWING NO.
	FIG. 8	PIN DIODE SWITCH CIRCUIT
SCALE		SHEET



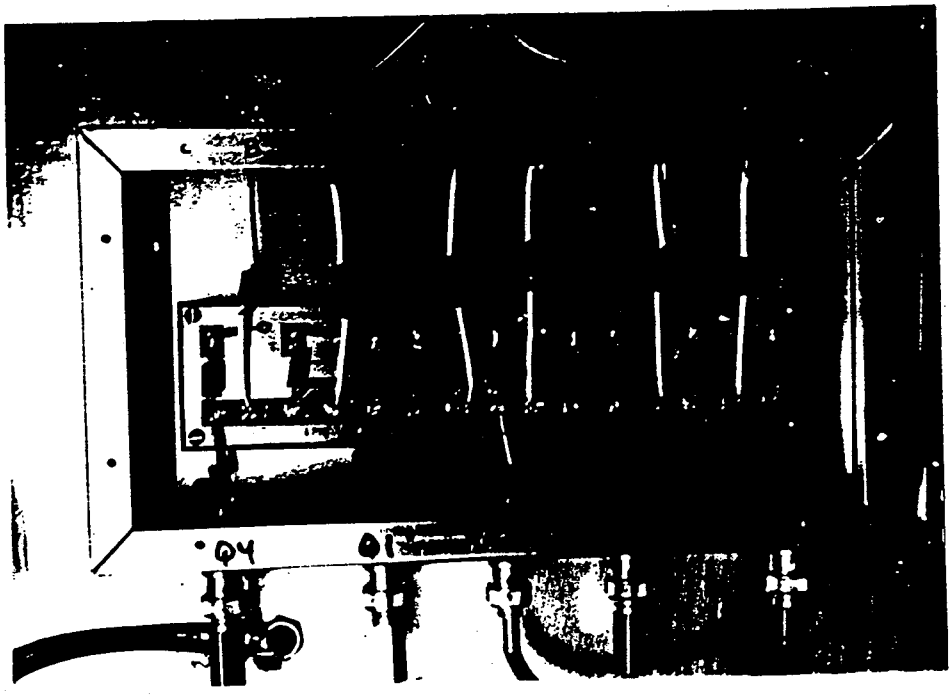
IF AMPLIFIER & AC TO DC CONVERTER

Q = 2N3904

SIZE	CODE IDENT NO.	DRAWING NO.
	FIG. 9	
SCALE		SHEET



Photograph 4.



Photograph 5.

circuitry to evaluate in which quadrant the RF signal is strongest.

One additional modification to the terminal node controller (TNC) was made: a push to talk (PTT) line was brought out to interface with the sample and hold/computer system.

Task 5

Task five comprises the testing in manual mode of the system so far constructed. Figure 10 shows the overall phased array system in block form.

Figure 11 shows the phased array antenna directivity pattern with the phasing assembly attached. This pattern, though not ideal, shows that the phased array produces directivity adequate to provide proof of concept of the switched system. The slight skewing of the directivity results from the 95 degree phase angle (rather than the 110 degree desired) of phasing port D.

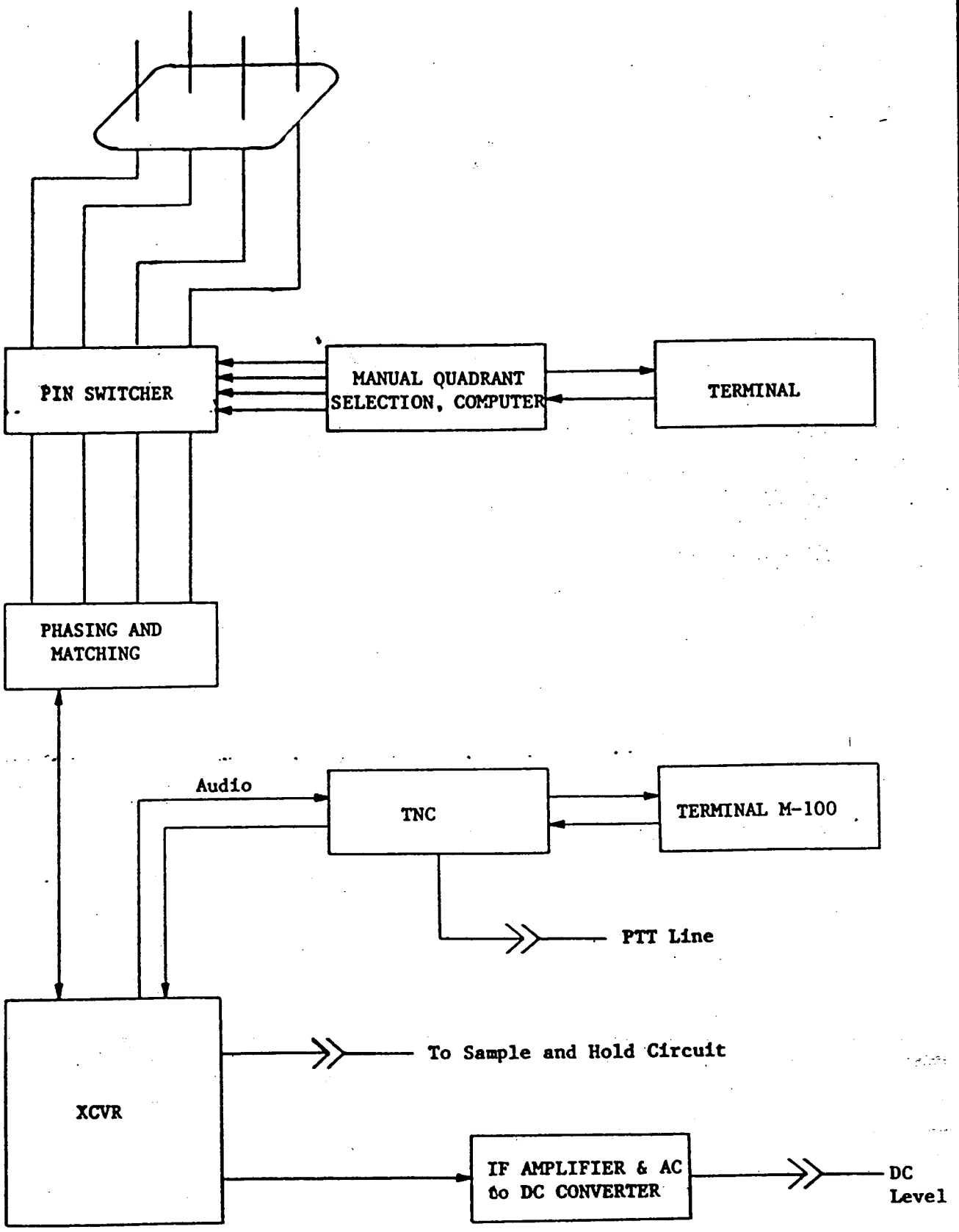
Figure 12 shows the directivity of the four corner array. As can be seen the four corner array has a much cleaner directivity and is also suitable to demonstrate proof of concept.

The PIN switchers were tested and found to be switching properly. The PIN switch for the phased array must not introduce any additional phase shift in the already shifted signals. Considerable circuit modification was necessary to correct the phase shift introduced by the uneven switch numbers during each quadrant configuration. This switching and phasing assembly introduced variable phase shift during the switching operation. This shift caused beam skewing. Empirical adjustment of the phase shift would correct this problem which is worse at higher frequencies (>100 MHz) but was not done due to time limitations and the need for a higher gain antenna system. Operation of the phased array and the PIN switcher were demonstrated to Steven Schehr during his visit to TRA.

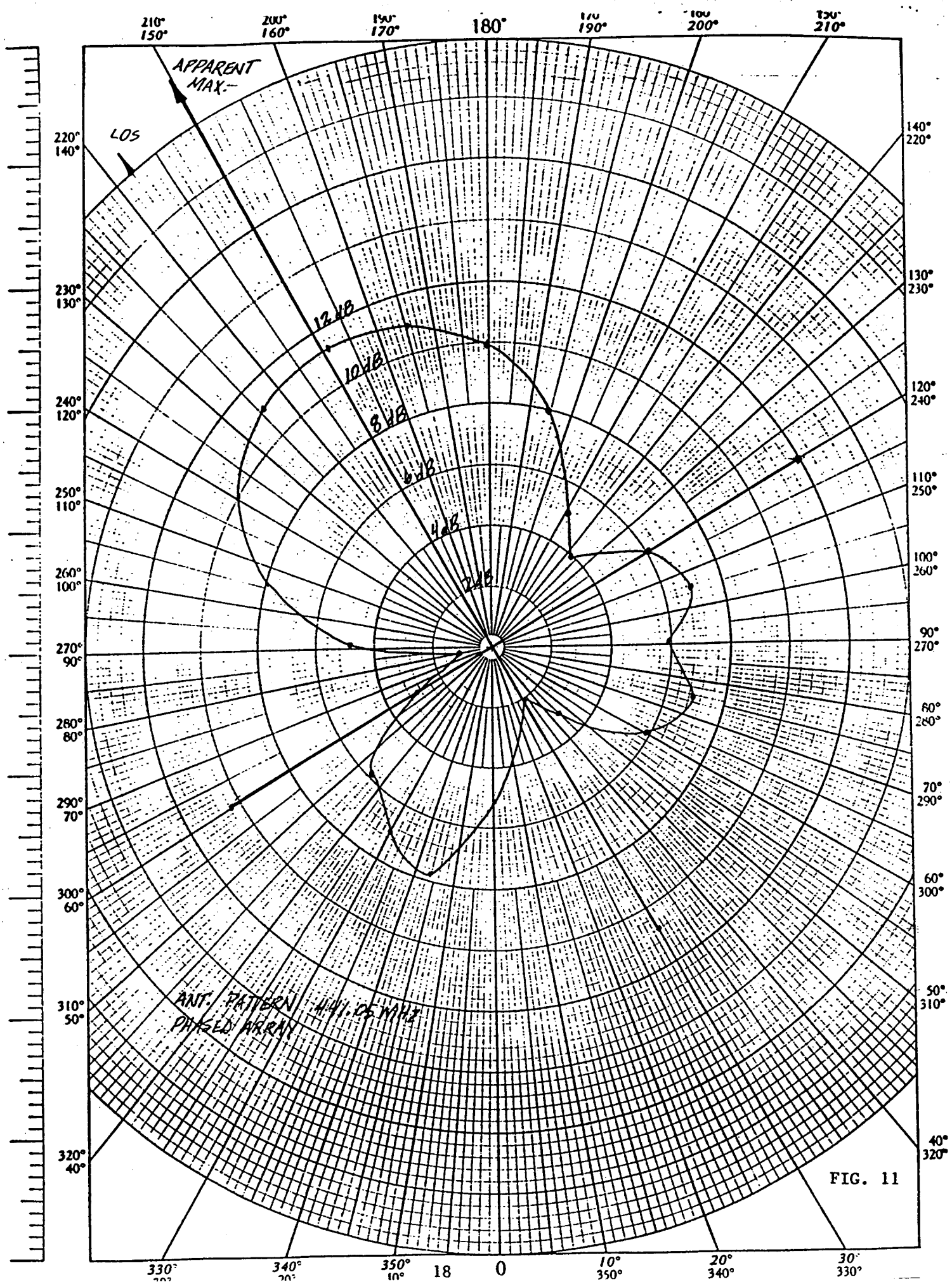
The PIN switcher for the four corner array did not have this problem since phase shift through the switch would have no effect at the individual antenna. Estimated loss through the switch was 1.5 dB but again during this proof of concept work no attempt was made to minimize loss.

The software to operate the system in the manually switched mode obviously worked as we were able to operate the system and complete the above demonstration.

Photograph 6 shows the amplitude of the DC level which corresponds to the RF amplitude of the signal. The signal source was the 9th harmonic of 49.005556 MHz from a signal generator. The pulse on the lower trace is the switching voltage for



SIZE	CODE IDENT NO.	DRAWING NO.
	FIG. 10	
SCALE		SHEET


APPARENT MAX.
LOS
12dB
10dB
8dB
6dB
4dB
2dB
ANT. PATTERN 441.05 MHz
PHASED ARRAY
180°
0
18
FIG. 11

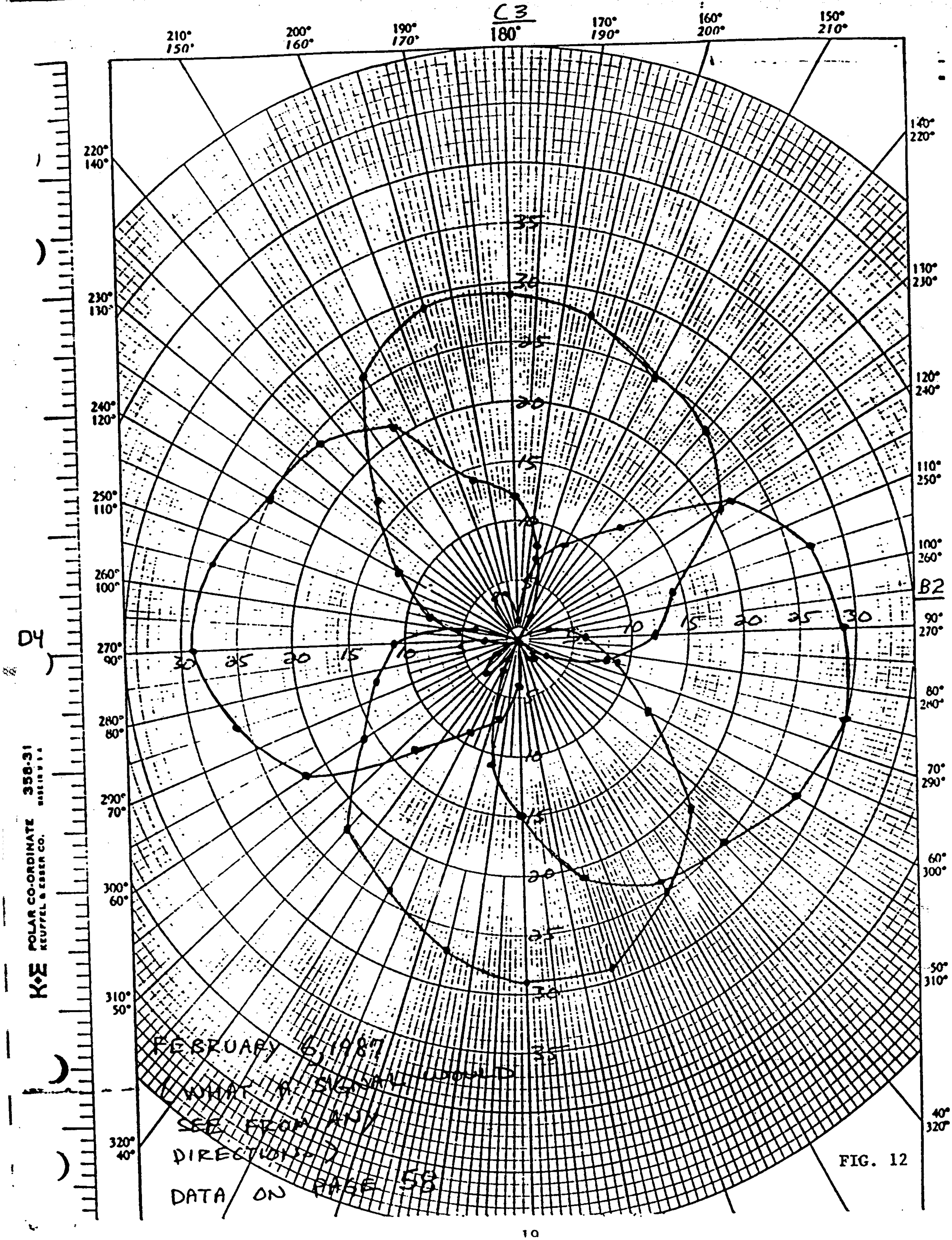
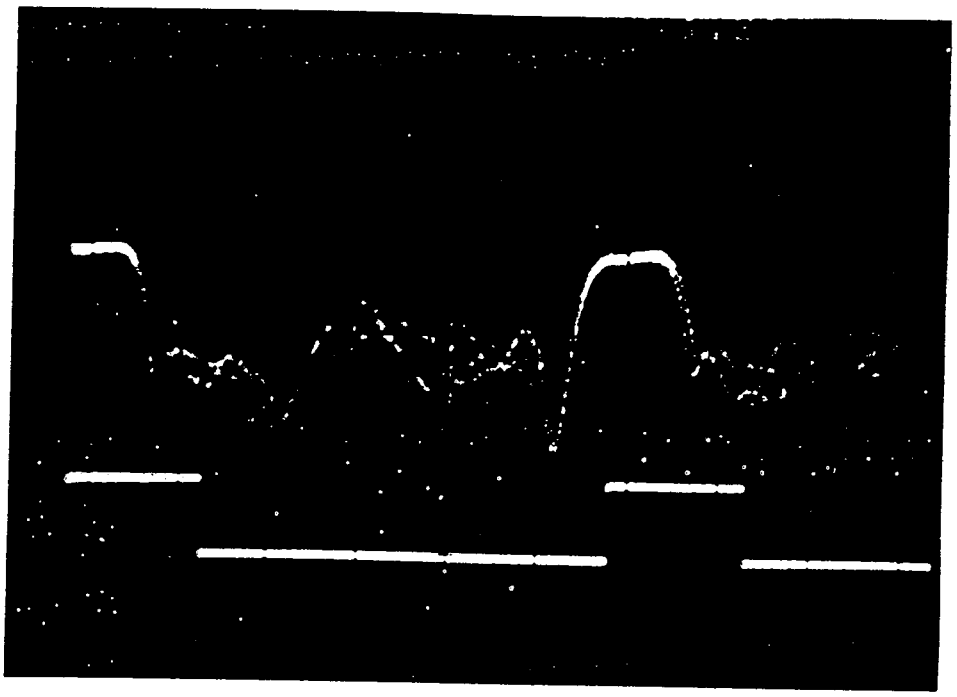

C3
B2
D4
FEBRUARY 6 1987
(WHAT A SIGNAL WOULD
SEE FROM ANY
DIRECTION)
DATA ON PAGE 58
K+E POLAR CO-ORDINATE 358-31
KEUFFEL & ESSER CO.

FIG. 12



Photograph 6.

quadrant 1 with quadrants 2,3 and 4 equally interspersed. The highest DC level on the upper trace is displaced with respect to its quadrant switching signal because of the time delay of the signal through the reciever. In the photo the strongest signal appears in quadrant 4. This time delay could be reduced, if necessary, by converting the RF or IF signal to DC earlier in the radio.

TASK 6

Sample and Hold Circuitry

One approach in designing the hardware for this project is to have flash A/D converters convert the sampled RF signal and then set the antenna system to the appropriate quadrant based on these A/D values. Reading and then processing A/D values requires significant CPU time, however. Since a design goal in this project was for the antenna system to lock in on a received signal as quickly as possible, it was decided to use high speed comparators and hard wired logic circuitry to minimize CPU activity. In the circuit shown in Figure 13, once the RF signal is sampled the CPU need do only one read and one write operation to set the system to the quadrant with the strongest received signal.

The system computer "scans" for a microwave signal by writing to a PIO. Each write is decoded by logic circuitry so as to bias the PIN diode switches to connect the "scan radio" to a particular antenna. Figure 14 shows the circuitry which converts the logic circuitry TTL outputs to the necessary voltage and currents to drive the PIN diodes. To connect to antennas 1,2,3... the computer writes 0001, 0010, 0100,... Each successive write connects the scan radio to a different antenna. If the scan radio detects a signal exceeding a set minimum level then an internal squelch line will toggle and this transition will be detected by the computer. Now, the computer brings high the "sample and hold enable line", which is the PIO line common to the four AND gates to the right of the sample and hold chips, and writes the pattern 0001, 0010,... as before. Each write enables one of the sample and hold chips, and the next successive write "holds" the voltage on this chip's input. The sample and hold voltage inputs are all connected to a rectified and amplified DC signal level brought out of the scan radio. After the signal level in each of the quadrants has been sampled, the high speed comparators compare the results. The logic circuitry connected to these outputs will provide the "winner" and this result is latched. If sector 3 contains the strongest signal then the logic circuitry will produce the pattern 0100 to the input PIO. This is just the format the computer needs to configure the system to sector 3, so it needs to do only one read and one write operation to configure the antenna and lock in.

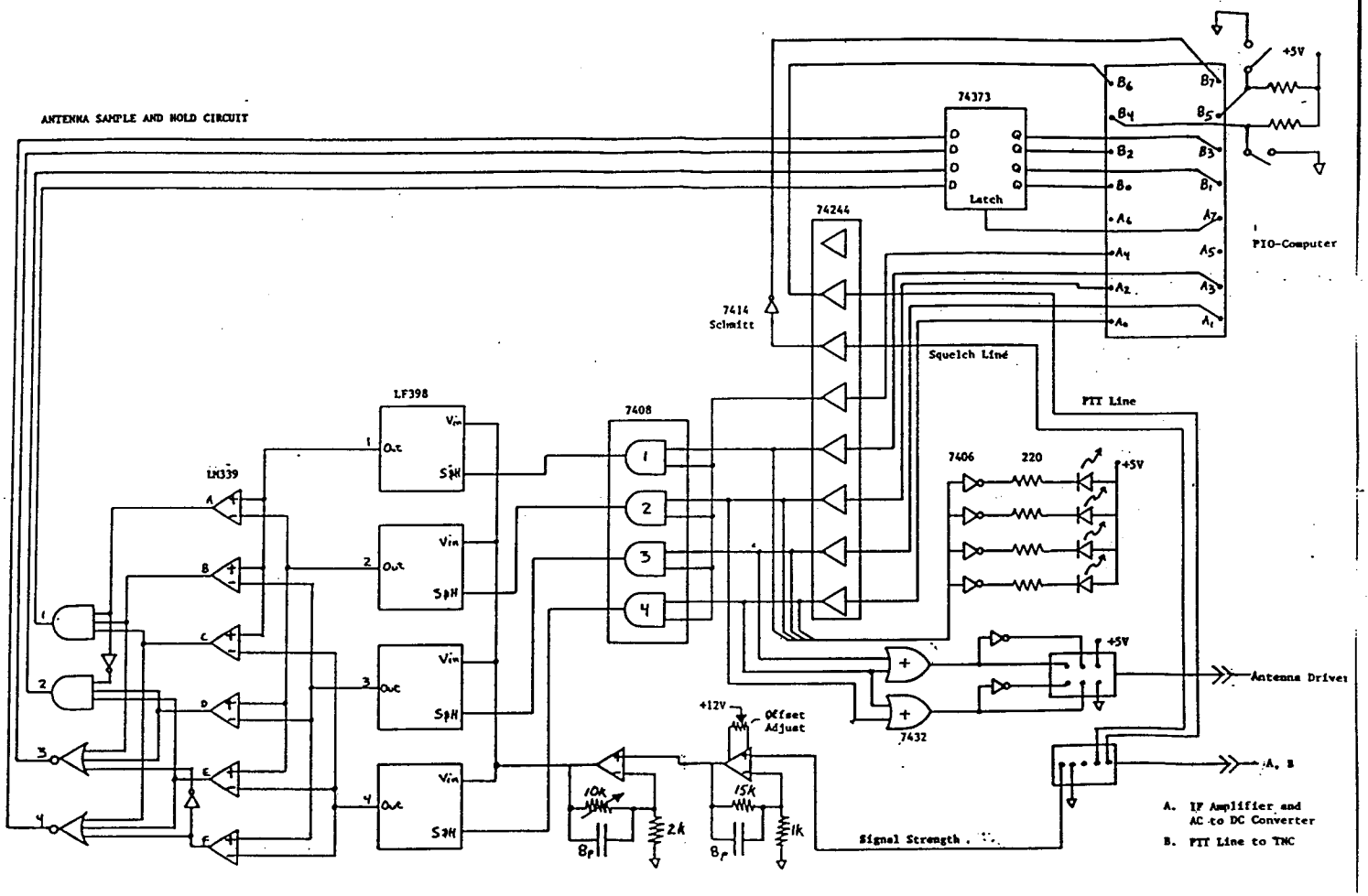
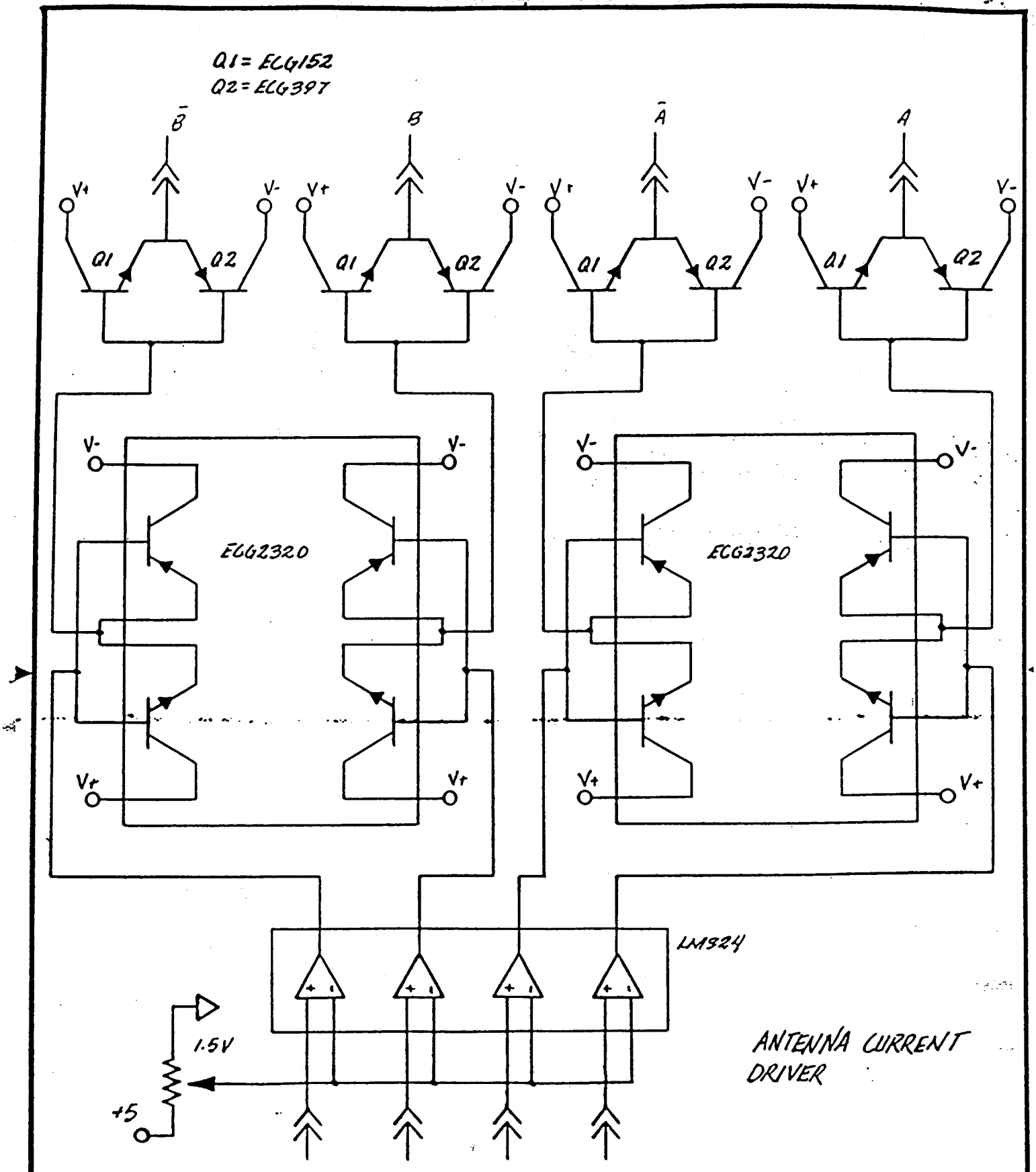

ANTENNA SAMPLE AND HOLD CIRCUIT
74373
Latch
74244
7414
Schmitt
PIO-Computer
+5V
Squelch Line
PTT Line
LF398
LM339
7408
7406
220
7432
Antenna Driver
Offset
Adjust
+12V
10K
2k
15K
1k
Signal Strength
A. IF Amplifier and AC to DC Converter
B. PTT Line to TNC

FIG. 13



SIZE	CODE IDENT NO.	DRAWING NO.
	FIG. 14	
SCALE		SHEET

The computer re-reads the PIO to record in memory the result of the lock-in operation.

The above hardware provides very fast scan and lock-in capabilities. The above circuitry allows a system to sample signal strength and lock in on the strongest signal in about 10 microseconds. However, the RF chokes used in the PIN diode bias circuitry present significant inductance to the DC bias transistors, and this factor presently limits system operation to about 200 microseconds per quadrant.

TASK 7

System Software

The system software falls into four functional areas.

1) Assembly Language Two Way Communication Software

The assembly program "Twoway4" is listed in the Software Appendix. This program provides :

(a) Rapid scanning for received signals.
(b) Rapid lock-in to the sector with the strongest received signal.
(c) Efficient control of two-way communications.

The flow chart for this program is shown in Figures 15 and 16.

From figures 15 and 16, we see that if a signal is received and "locked in on" in quadrant x, then the answering transmission will also be sent in quadrant x. If it is desired to contact another radio station, then a trial transmission will be sent in a quadrant. If no reply is detected then the re-try transmission will be broadcast in a different quadrant. This process will continue until a reply is obtained. Any reply will insure that the next transmission will occur in the quadrant which best received this reply.

Particular care was spent in optimizing the assembly code which allows the system to "lock in on" the quadrant with the strongest received signal. The software sets the antenna system to a particular quadrant, waits for the PIN diode bias circuitry and radio circuitry to stabilize, and then tests to see if a received signal is present. If a signal is present, then the signal level is immediately sampled in this quadrant before sampling in the other sectors. This technique increases the needed code, but speeds system execution.

The system scan rate is stored in RAM. If "Twoway4" is

TWO-WAY PROGRAM

FLOW CHART

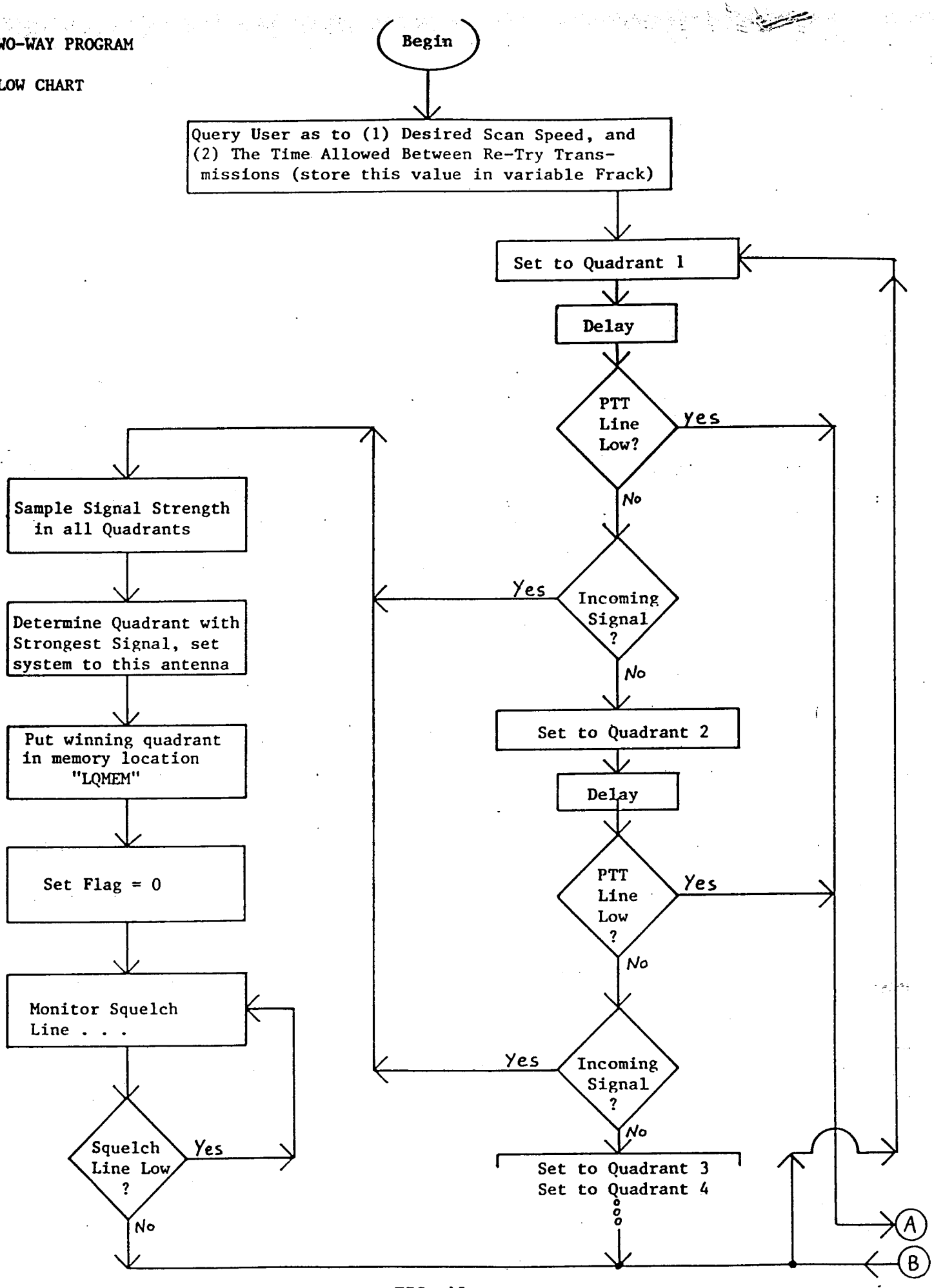


FIG. 15

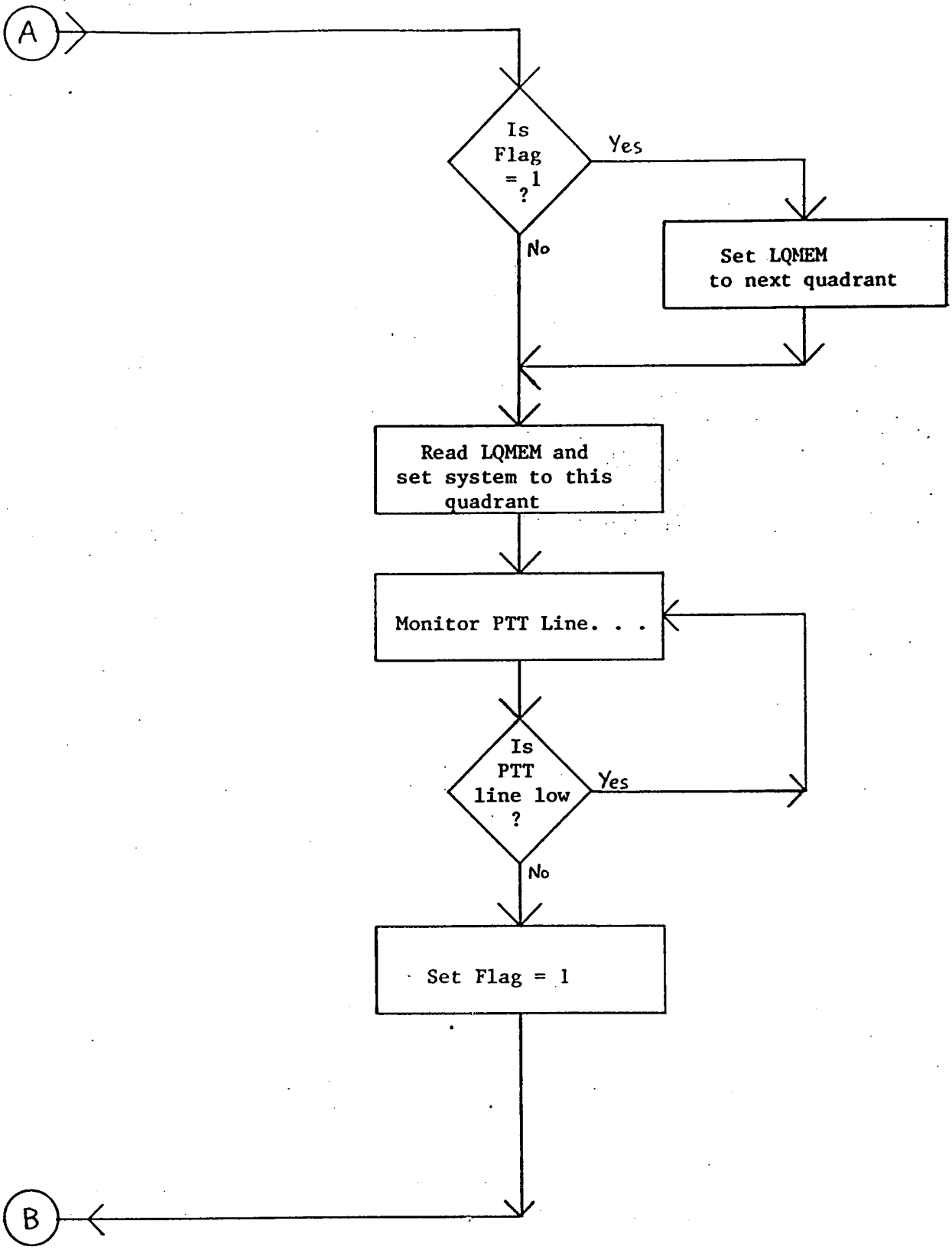

A
Is Flag = 1 ?
Yes
No
Set LQMEM to next quadrant
Read LQMEM and set system to this quadrant
Monitor PTT Line. . .
Is PTT line low ?
Yes
No
Set Flag = 1
B

FIG. 16

accessed via the Forth code, then the user is queried as to the value of this scan rate factor. "Twoway4" can also be run merely by toggling a switch on the system enclosure which is connected to the computer NMI input. In this case the scan rate factor is automatically initialized so that the scan rate is 200 microseconds per quadrant.

2) Forth Code

A single 27128 EPROM on the system computer board contains a complete Forth language kernel and auxiliary functions. This monitor allows Forth source code written on an MSDOS computer to be downloaded and compiled on the antenna system board. This feature was used extensively in the debugging phase of the system hardware.

A listing of the Forth code which was burned into EPROM in the final software version is provided in the Software Appendix. This code provides the following capabilities.

(a) Manual control of the antenna system is gained by typing "Q1" to set the antenna system to quadrant 1, etc.

(b) Access to various assembly language routines is gained by typing the program name. The Forth code queries the user for system parameter initializations and then sends computer execution to the appropriate assembly code.

3) NMI Software

The antenna system was designed to operate autonomously without access to terminal communication to the on board computer. After system power is applied, a switch can be thrown on the system enclosure. This switch is connected to the computer NMI interrupt pin. The on board computer is vectored to location 9F00H on NMI interrupts, which is the location of program "Readip4". This software reads a dipswitch on the sample & hold card and does a jump to different assembly programs depending on this reading.

The listing for "Readip4" is in the Software Appendix.

4) Quadrant Tracking Software

This software is called "Lockin". It samples quadrant strengths about ten times a second, and locks in on the quadrant with the strongest signal after each sampling. If an RF source is in a particular direction, then the system LED's will reveal which quadrant the signal is strongest in. An interesting demonstration of system operation is gained by running "Lockin" while rotating the system antenna. As antenna #1, antenna #2, etc. are swept past the direction of the RF source one can observe LED #1, LED #2, etc. light up in succession.

The listing for the "Lockin" program is also provided in the Software Appendix.

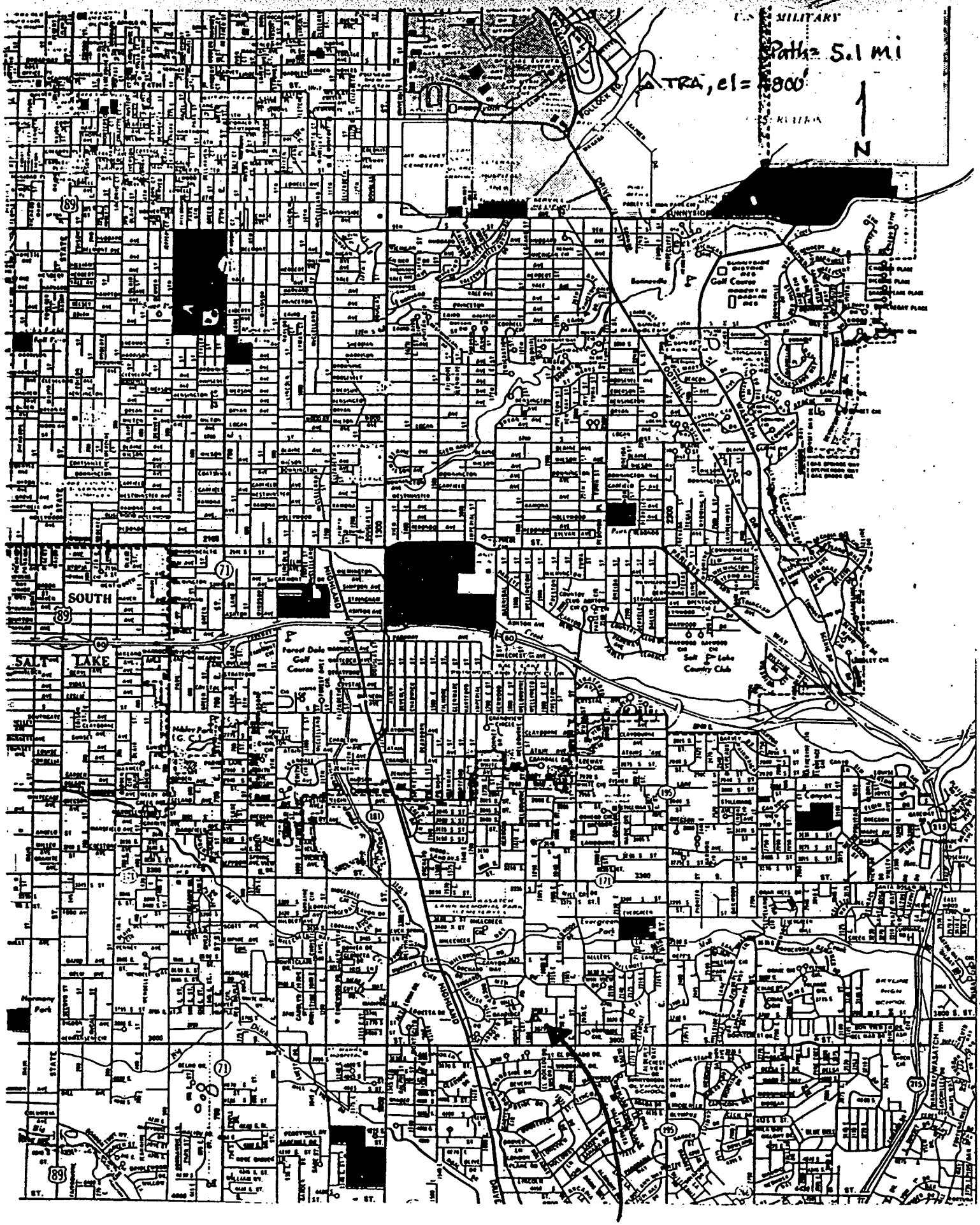
Task 8

Task eight is to test the entire system.

The four corner reflector system was first tested over a 5.12 mile path between TRA and the principal investigator's house (map of path is shown as Figure 17). The PI's packet station, consisting of equipment similar to that used at TRA, was operated both in the station mode and in the digipeat mode. The digipeat mode allowed an RF loop to be established. The loop allowed a packet, generated at TRA, to be repeated by the PI's station and sent back to TRA. Thus testing of the system could be done by a single operator. The test link was done using FM and a digital rate of 1200 baud. The estimated EIRP at the digipeater was about 5 watts and the EIRP at TRA was estimated at 2 watts. The path was almost line of sight with a building just blocking the LOS path. The digipeater antenna was at a height of 6 m and just cleared the roof of the house. The corner array at TRA was at a height of 2 m and located on a tripod which allowed rotation of the array. The TRA end of the test setup is illustrated in Photograph 3.

Tests of the corner system were successful and one test was observed by Dr. John Clark and Richard Salter of RAND and Ed Hill and Dan Bush of General Dynamics. The antenna could be rotated (as it would rotate if mounted on a moving vehicle) and would successfully locate the LOS quadrant to the digipeater. A brick supporting column (seen in photo 3) near the antenna produced a strong multipath signal and if the scanning sequence was such that if the quadrant selected for transmission occurred before the LOS quadrant, the digipeater could hear the transmission reflected from the post. However, the TRA ESABA system would still select the LOS quadrant during receive scan and lock. The system was scanning at a rate of 1250 Hz (800 microseconds per 360 degree scan). By selecting the appropriate TXDELAY on the TNC the system could successfully lock in and decode a single 1200 baud packet.

A second more critical test of the corner array was carried out over a non-line of sight path. Figure 18 is a topographic map of the test location. Photographs 7 and 8 show the view westward from the canyon test location. At the Box Elder location the ESABA always selected the unit antenna that pointed westward down the canyon. Photograph 9 shows this location. At another location, just below Tracy Wigwam, the ESABA often selected quadrants that were directed towards the canyon walls, suggesting that reflected signals were stronger than those from (non-LOS) directly down the canyon. The transmit power for these tests was higher than those described above. The digipeater was transmitting at 5W (transceiver out) and the antenna was at the same height as before. Estimated EIRP was 25 W. The field transceiver was generating 2.5 W out, with an estimated EIRP of



RF Loop route map

FIG. 17

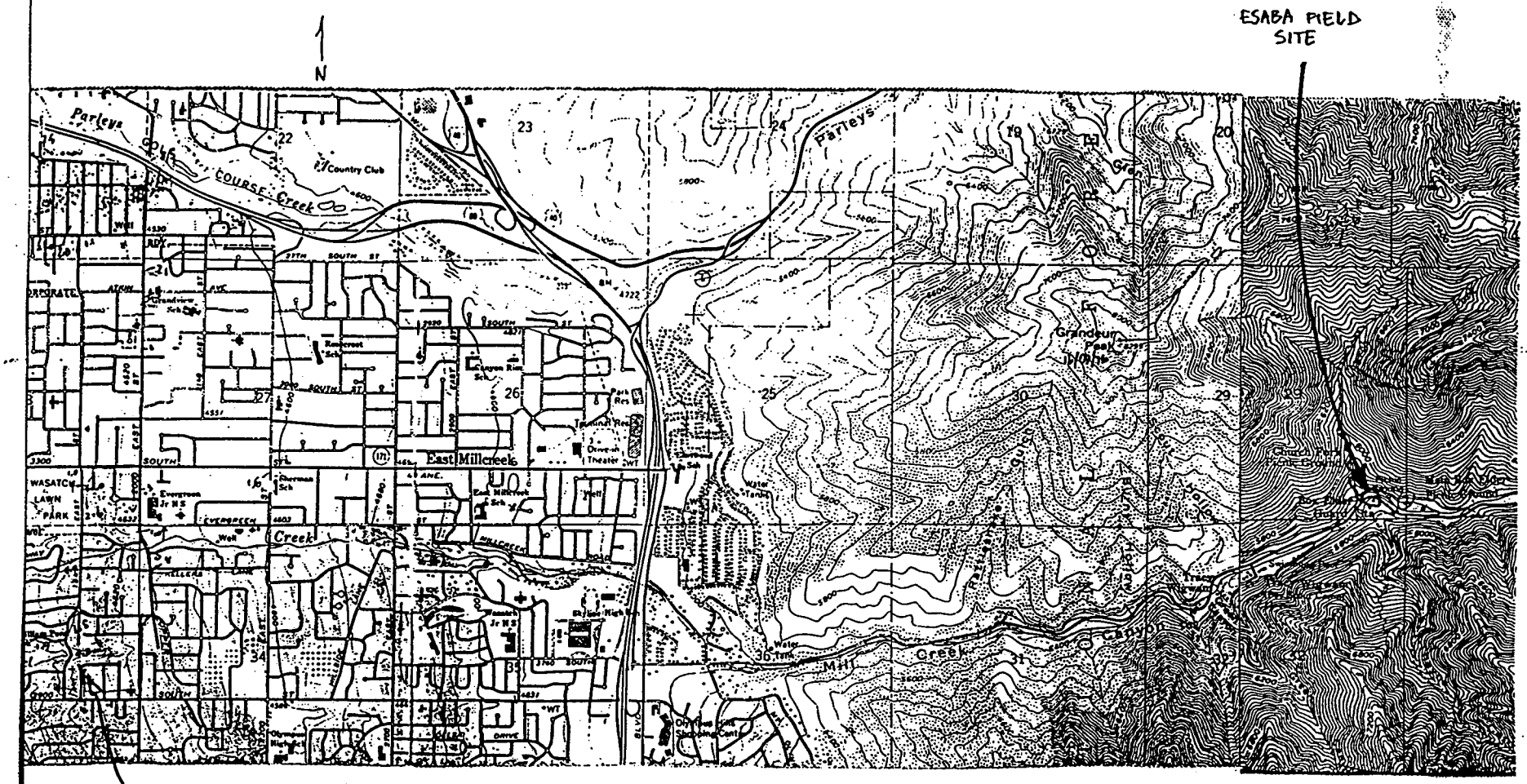
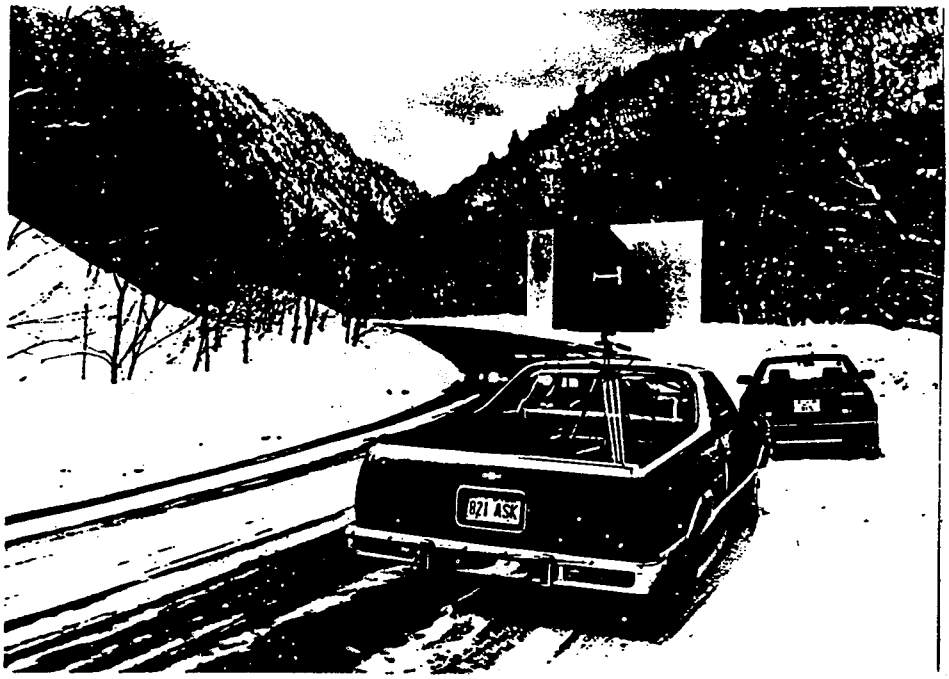
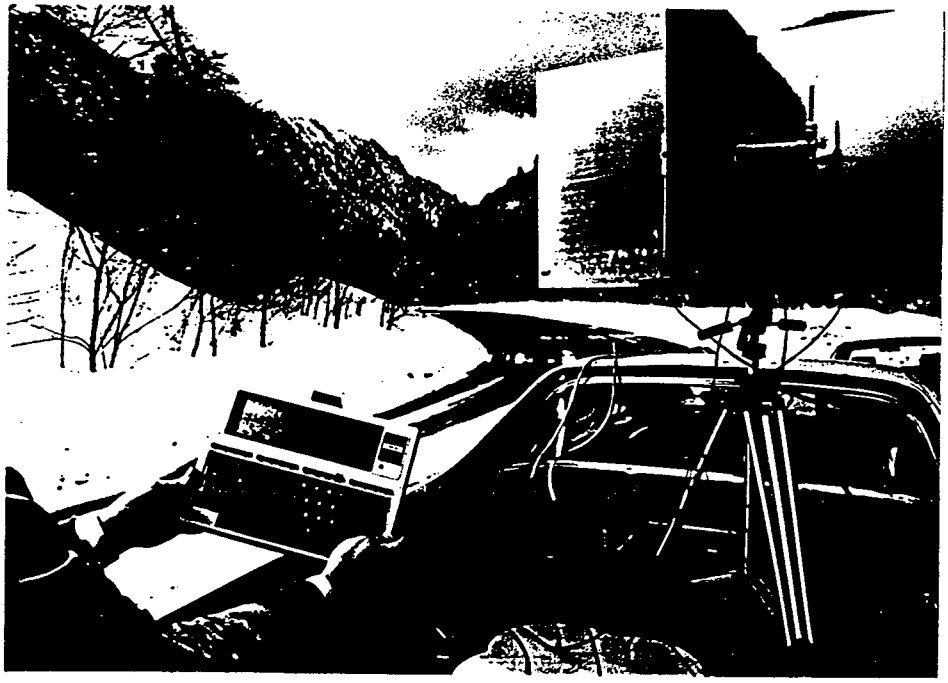


FIG. 18

13.3" => 5.04 MILES LOS



Photograph 7.



Photograph 8.

Photograph 9.

25 W. Trees and building obstructions were in the path to the mouth of the canyon. The total one way path was slightly over 5 miles. The system operated in both the one way connect and RF loopback modes.

These tests of the corner array ESABA clearly demonstrate proof of concept of the system.

Task 9

Task nine is the production of this final report.

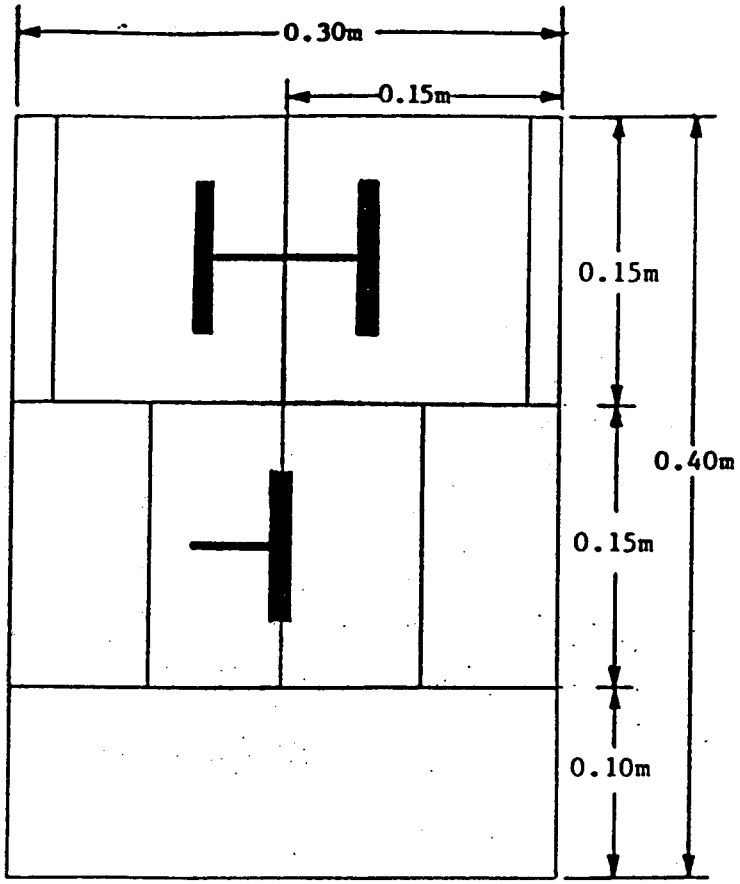
Outline of proposed future program

With the successful completion of the Phase I feasibility study TRA feels that the ESABA concept would enhance the RF communications link between the robotic vehicle and the RCC. TRA envisions an ESABA based on a six over six, 60 degree, corner array. A model, scaled to 2 GHz, of this antenna is shown in Photograph 2 and dimensioned in Figure 19. The cylinder at the bottom of the array would contain the PIN switchers and associated electronic components. The on board computer, power supplies, sample and hold and radio would be located inside the robot vehicle for protection. The antenna could be mounted on an extensible mast so it could be raised above obstructions to enhance the communication link, Figure 20. A similar system could be located on the RCC.

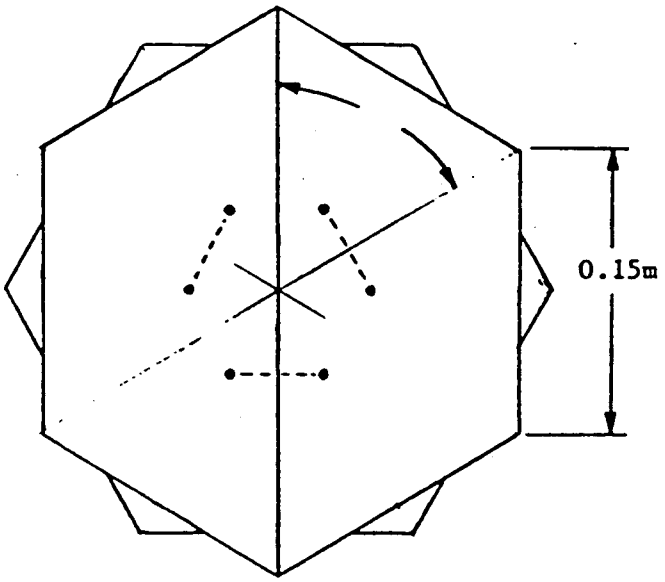
The proposed system could operate on a continuous sample mode outlined in Figure 21. A dedicated receiver would be multiplexed to the antenna system, and the ESABA would operate in a continuous scan mode continually evaluating signal strength in all sectors. The computer could then configure other PIN switchers to direct the RF (on other frequencies) to the appropriate unit antenna. As the vehicle moved the ESABA would continually maintain the best link to the RCC. The RCC similarly equipped with ESABA would follow the robot. In fact the same antenna could simultaneously, by the use of different receivers, switchers and transmitters operating on different frequencies (again multiplexed), maintain simultaneous communications with several robot vehicles.

The proposed ESABA has additional advantages. A second robot could be configured to act as a full duplex repeater between a forward robot, perhaps out of line of sight of the RCC, and the RCC. Several mobile repeaters could form a flexible communications network with the potential for decoy operation. Another advantage of the proposed system is increased survivability of the antenna. The currently employed horn could be destroyed by a single hit while the 6/6 array has multi hit

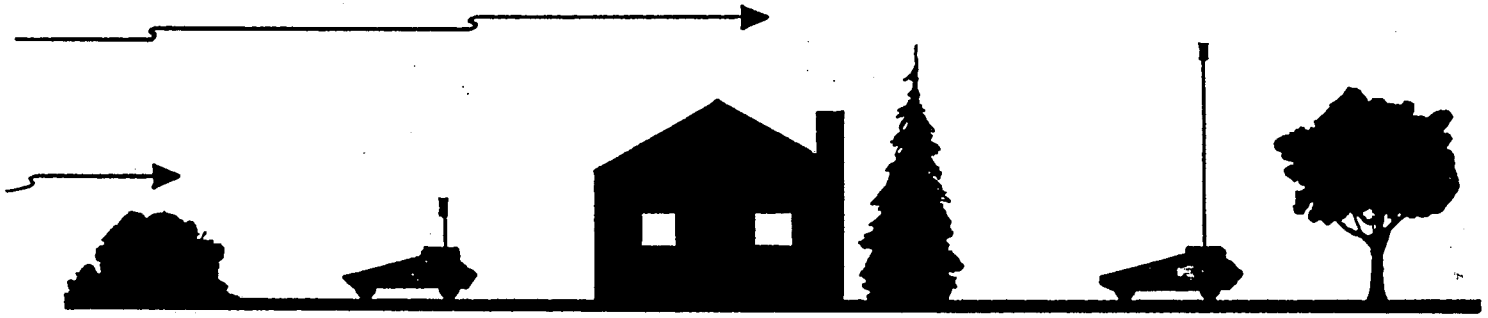
SIDE VIEW



TOP VIEW



SIZE	CODE IDENT NO.	DRAWING NO. PROPOSED
	FIG. 19	SIX OVER SIX ARRAY
SCALE 1:4		SHEET



A robot vehicle with a scanning antenna on a boom

FIG. 20

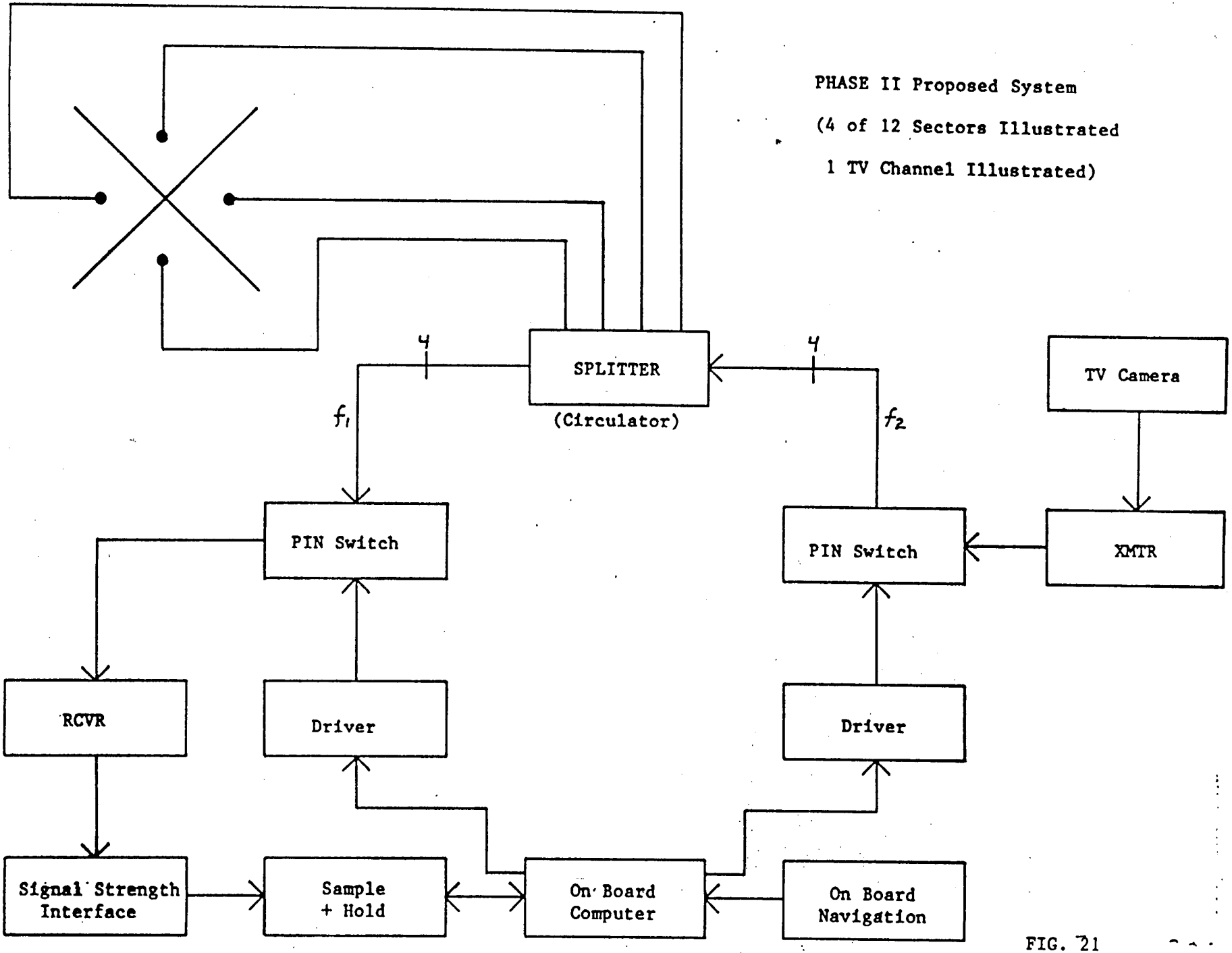

PHASE II Proposed System
(4 of 12 Sectors Illustrated
1 TV Channel Illustrated)
4
4
SPLITTER
(Circulator)
f_1
f_2
TV Camera
PIN Switch
PIN Switch
XMTR
RCVR
Driver
Driver
Signal Strength Interface
Sample + Hold
On Board Computer
On Board Navigation

FIG. 21

survivability. Further, the ESABA is smart and can independently locate the RCC. Thus the robot could awaken from a sleep or autonomous mode and quickly establish communications with the RCC. The ESABA also takes advantage of multipath signals. If the robot moves behind an obstruction and a significant reflected signal exists the antenna will be configured to take advantage of that path even if only for a few seconds. Further for about a doubling of the antenna size (2 feet high and diameter) gains approaching 17dBi can be obtained.

TRA feels its ESABA concept can significantly enhance battlefield communications and is particularly suited to the AGVT program. Phase II would provide for the development of ESABAs for the RCC and one or more robots. The ESABA would be installed on the vehicle and the RCC and field evaluated.