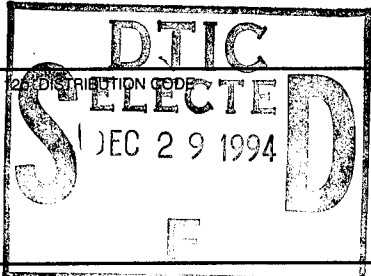


# REPORT DOCUMENTATION PAGE

Form Approved  
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE <p style="text-align: center;">June 1994</p>	3. REPORT TYPE AND DATES COVERED <p style="text-align: center;">Professional Paper</p>
4. TITLE AND SUBTITLE <p style="text-align: center;"><b>MICROWAVE CHARACTERIZATION OF SUB-MICRON N- AND P- CHANNEL MOSFETS FABRICATED WITH THIN FILM SILICON-ON-SAPPHIRE</b></p>		5. FUNDING NUMBERS <p>PR: EEB3 PE: 0602234N WU: DN313033</p>
6. AUTHOR(S) C. E. Chang, P. M. Asbeck, P. R. de la Houssaye, G. Imthurn, G. A. Garcia, and I. Lagnado		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Command, Control and Ocean Surveillance Center (NCCOSC) RDT&E Division San Diego, CA 92152-5001		8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Naval Command, Control and Ocean Surveillance Center (NCCOSC) RDT&E Division San Diego, CA 92152-5001		10. SPONSORING/MONITORING AGENCY REPORT NUMBER
11. SUPPLEMENTARY NOTES		
12a. DISTRIBUTION/AVAILABILITY STATEMENT <p style="text-align: center;">Approved for public release; distribution is unlimited.</p>		
13. ABSTRACT (Maximum 200 words) <p>This paper reports on microwave characteristics for n- and p- MOS transistors fabricated with thin-film Silicon-on-Sapphire technology. The gates were defined with I-line optical lithography, and ranged down to 0.5 μm (drawn dimension). The f<sub>t</sub> values of the transistors reach 22 GHz for the n-channel structures and 21 GHz for the p- channel devices. The PMOS results are significantly higher than found with other Si or III-V technologies, and can potentially lead to high performance complementary microwave circuits. Small signal transistor models are similar to the ones for GaAs FETs. Dependence of model parameters on gate length were determined.</p> <p style="font-size: 2em; font-weight: bold; margin-top: 20px;">19941227 106</p> <p style="font-size: 0.8em; margin-top: 20px;"><del>Public Release in Full</del> <i>IEEE MTT-S International Microwave Symposium Digest, vol. 1, pp. 405-408, May 1994.</i></p>		
14. SUBJECT TERMS A/D converters in SI and GAAS electronic devices ion beam technology VLSI/VHSI circuits		15. NUMBER OF PAGES
		16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT <p style="text-align: center;">UNCLASSIFIED</p>	18. SECURITY CLASSIFICATION OF THIS PAGE <p style="text-align: center;">UNCLASSIFIED</p>	19. SECURITY CLASSIFICATION OF ABSTRACT <p style="text-align: center;">UNCLASSIFIED</p>
20. LIMITATION OF ABSTRACT <p style="text-align: center;">SAME AS REPORT</p>		

UNCLASSIFIED

21a. NAME OF RESPONSIBLE INDIVIDUAL P de la Houssaye	21b. TELEPHONE (include Area Code) (619) 553-3912	21c. OFFICE SYMBOL Code 553
---	--	--------------------------------

Accession For	
NTIS CRAND	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By	
Distribution/	
Availability Codes	
Dist	Avail and/or Special
A-1	

# Microwave Characterization of Sub-micron n- and p- channel MOSFETs Fabricated with Thin Film Silicon-On-Sapphire

C.E. Chang, P.M. Asbeck  
Electrical and Computer Engineering Department  
University of California, San Diego  
La Jolla, CA 92093-0407

P.R. de la Houssaye, G. Imthurn, G.A. Garcia, & I. Lagnado  
Naval Command, Control, and Ocean Surveillance Center Research, Development, Test, and Evaluation Division (NRaD) 553  
San Diego CA 92152-7633

### Abstract

Microwave characteristics are reported for n- and p- MOS transistors fabricated with thin-film Silicon-on-Sapphire technology. The gates were defined with I-line optical lithography, and ranged down to 0.5  $\mu\text{m}$  (drawn dimension). The  $f_t$  values of the transistors reach 22 GHz for the n-channel structures and 21 GHz for the p-channel devices. The PMOS results are significantly higher than found with other Si or III-V technologies, and can potentially lead to high performance complementary microwave circuits. Small signal transistor models are similar to the ones for GaAs FETs. Dependence of model parameters on gate length were determined.

### Introduction

The evolution of digital Si MOSFET technology has resulted in sub-micron gate length devices which exhibit high microwave gain.<sup>1,2</sup> These devices may be considered for use in Si monolithic microwave integrated circuits (MMICs); however, the conductive properties of the bulk Si substrates and the high capacitance in some SOI technologies which use a thin isolation oxide on a conductive Si substrate prevent the realization of high-Q passive elements typically associated with MMICs. On the other hand, the sapphire substrate used in SOS is ideally suited for MMIC applications due to its insulating properties and high thermal conductivity as compared to the SiO<sub>2</sub> layers used in SIMOX or BESOI.

Fully depleted thin-film SOS FETs exhibit well behaved I-V curves, good sub-threshold characteristics, reduced hot-electron effects, radiation hardness, and higher breakdown voltage than thick-film SOS. We report here that digital thin-film SOS devices based on a 0.5  $\mu\text{m}$  written gate length, exhibit  $f_t > 20$  GHz for both p- and n-channel devices. These results are the highest ever shown for SOS FETs fabricated with optical lithography and are comparable to the best ever reported for electron-beam processed structures.<sup>3</sup> Unlike typical devices fabricated by III-V, bulk Si, or other SOI technologies, the  $f_t$  of the thin-film SOS PMOS approaches the NMOS  $f_t$  for short gate lengths. This opens up a new possibility for complementary microwave amplifiers. The technology is also promising for the co-integration of microwave and VLSI digital ICs.

In this work, we characterize the microwave performance of digital thin-film SOS devices, determine the variation of the small signal model elements as a function of gate length for both the n- and p- channel devices, and compare the thin-film SOS performance with competing III-V and Si technologies.

### Fabrication Technology

A cross section of an SOS MOSFET representative of those used for this work is diagrammed in fig. 1. Fabrication of the high quality single crystal Si films on sapphire is accomplished using an amorphization implant and solid phase re-growth process described elsewhere.<sup>4</sup> The Si films correspond to (100) planes, and are deposited on (1 $\bar{1}$ 02) sapphire surface. The result is a 100 nm Si film

with low defect density despite the lattice mismatch between Si and sapphire at the interface. An I-line stepper is used to define the 380 nm thick polysilicon gate on top of the 25 nm thick gate oxide, resulting in a minimum controlled gate length of 0.5  $\mu\text{m}$ . The effective gate length ( $L_{g,eff}$ ) varies uniformly from the center to the edge and is about  $0.15 \pm 0.05 \mu\text{m}$  smaller than the drawn gate length ( $L_g$ ), as measured by the Moneda algorithm on adjacent test devices.  $L_{g,eff}$  is similar for adjacent n- and p- channel devices in the same die. The gate length reduction is due to a combination of undercutting during the gate etch and diffusion of the source/drain implants under the gate. The source/drain regions are formed by implantation, which is self-aligned to the gate. A 100 nm oxide sidewall spacer is formed next to the gate and TiSi<sub>2</sub> is formed on all exposed silicon surfaces. In this process, the regions outside of the spacer become silicide, almost to the sapphire interface; this tends to reduce  $R_d$  and  $R_s$ .

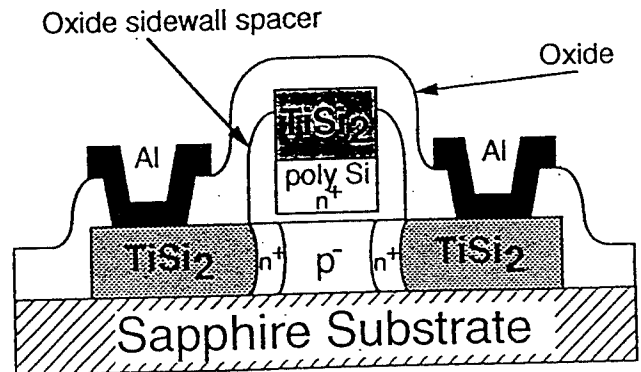


Fig. 1: Cross sectional diagram of a thin-film SOS MOSFET with self-aligned ohmic contacts and a silicide gate

The enhancement mode devices have  $V_t$  around 0.7 V for the NMOS and -0.9 V for the PMOS. Various gate lengths were fabricated on the same wafer using the same doping profile; thus, the devices were not optimized for a specific gate length. The digital SOS MOSFETs with the silicide/polysilicon gate tend to have high gate resistance which reduces the power gain and increases the noise at microwave frequencies; however,  $R_g$  can be reduced with an Al overlay.<sup>3</sup>

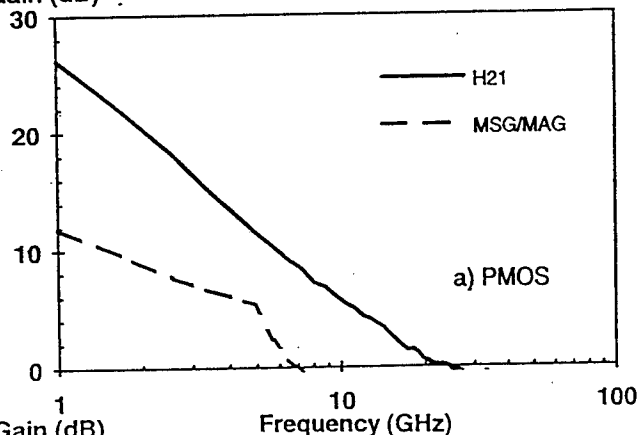
An important feature of the thin-film SOS technology is the high  $f_t$  of the PMOS as compared to that of bulk Si or other SOI technologies. The enhancement is believed to result from the strain due to the silicon/sapphire interface which splits the valence band degeneracy and reduces the hole effective mass. As a consequence, the hole mobility is increased.<sup>5,6,7</sup>

### Microwave Characterization

For microwave characterization, standard n- and p-channel digital MOSFETs were fabricated with co-planar microwave pads which can be probed with 100  $\mu\text{m}$  pitch co-planar microwave probes. These microwave devices were fabricated side-by-side with LSI digital circuits such as CMOS 16 x 16 multipliers and memory circuits, demonstrating the possibility of this technology for low-power combined microwave and digital ICs. The s-parameters were measured with a HP 8510B network analyzer from 1 to 40 GHz. Typical  $h_{21}$  and MAG/MSG plots which were used to obtain the figures-of-merit are shown in fig. 2a and 2b. The low pad parasitic capacitance of the sapphire substrate does not significantly degrade the measured results; thus, de-embedding the pad parasitics to determine the device performance (as used in bulk Si, SIMOX, and BESOI) is not required for SOS.

Table 1 lists the as-measured performance of the devices. In thin-film SOS technology, with the 0.5  $\mu\text{m}$  optically defined gate, the  $f_t$  for the PMOS is 21 GHz, which is close to the 22 GHz  $f_t$  for the NMOS. The measured  $L_{g,eff}$  of the PMOS is 0.3  $\mu\text{m}$  while the measured  $L_{g,eff}$  for the NMOS is 0.35  $\mu\text{m}$ . The high performance of the PMOS raises the possibility of high-speed, low-voltage, and high-efficiency class A/B or class B power amplifiers.

Gain (dB)



Gain (dB)

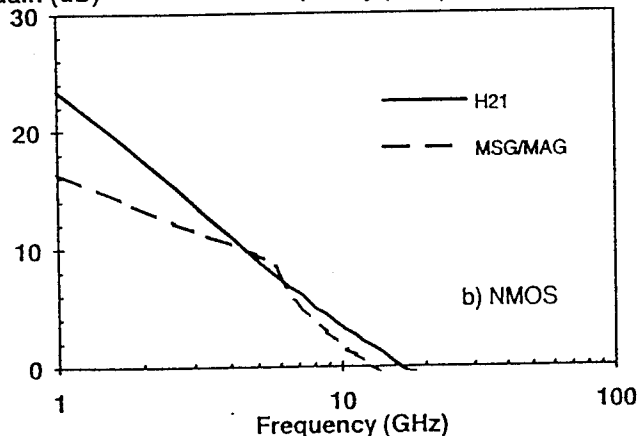


Fig. 2: Measured  $h_{21}$  and MAG/MSG is shown for a)  $L_g = 0.5 \text{ mm}$  (drawn) PMOS b)  $L_g = 0.7 \text{ mm}$  (drawn) NMOS

The  $f_t$  vs.  $L_{g,eff}$  is plotted for both types of devices in fig. 3. For saturated carrier velocities, simple analysis predicts a  $L^{-1}$  scaling for  $f_t$  vs.  $L_{g,eff}$ . For non-saturated carrier velocities, the gradual channel model predicts a  $L^{-2}$  trend. The  $f_t$  vs.  $L_{g,eff}$  for the NMOS behaves as  $L^{-1.05}$  which implies that the carrier velocities are largely saturated. On the other hand, the  $f_t$  vs.  $L_{g,eff}$  for the PMOS shows an  $L^{-1.3}$  trend. This implies that the carrier velocity in the PMOS is

saturated for only part of the channel length. Since the hole velocity saturates at a higher electric field than for electrons, a shorter gate length is needed for the PMOS to exhibit strong saturation effects. These results indicate that thin-film SOS CMOS is capable of achieving significant microwave performance with sub-micron gates.

Device	$L_g$ ( $\mu\text{m}$ )	$V_{ds}$ (V)	$V_{gs}$ (V)	$f_t$ (GHz)	$f_{max}$ (GHz)
NMOS	0.5	2.5	2.5	22	11
NMOS	0.7	3.5	3.5	15	13
NMOS	1.0	3.0	3.0	8	11
PMOS	0.5	-4.0	-3.0	21	7
PMOS	0.7	-4.0	-3.0	12	10
PMOS	1.0	-4.0	-2.0	6	8

Table 1: Measured  $f_t$ ,  $f_{max}$ , and bias for the digital NMOS & PMOS

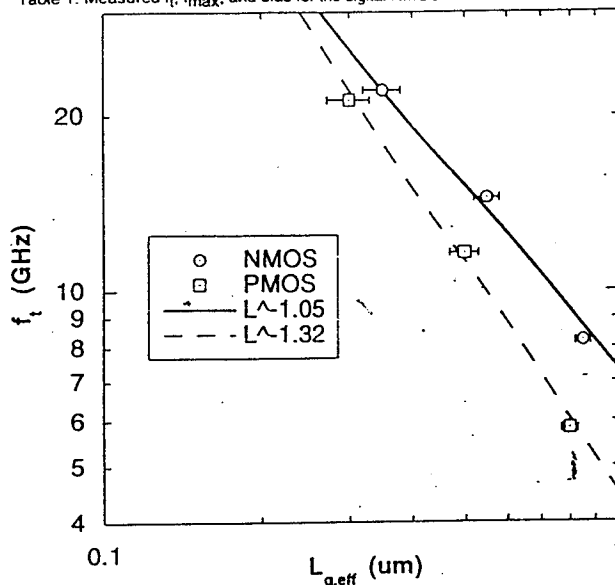


Fig. 3: Measured  $f_t$  vs.  $L_{g,eff}$  for the NMOS and PMOS

### Microwave Modeling

The measured device s-parameters were fitted to the small signal model shown in fig. 4 with the aid of EEsof's LIBRA. Due to the insulating properties of sapphire, the SOS MOSFET small signal model is the same as for GaAs MESFETs on semi-insulating GaAs. Open pad patterns without the device were measured to determine the values of the pad parasitic capacitance for the small signal model and to verify that the parasitic capacitance does not significantly affect the as-measured  $f_t$  and  $f_{max}$ . The models were derived from measurements at biases for maximum  $f_t$  and  $f_{max}$  as listed in table 1.

The typical fits achieved between the small signal model and the measured s-parameter data are illustrated in fig. 5a and 5b. Table 2 contains the extracted parameters for the NMOS and the PMOS for various gate lengths. Due to the self-aligned silicidation process,  $R_s$  and  $R_d$  are quite low for all the devices at 2 ohms (0.1 ohms-mm). Due to the insulating properties of sapphire and the shielding properties of the inverted thin-film Si, the feedback capacitance,  $C_{ds}$ , is quite small.  $C_{gd}$  does not scale with gate length and differences among the measurements are due to the various  $V_{gs}$  and  $V_{ds}$  values used in biasing the device.

The variations of the parameters  $C_{gs}$ ,  $R_g$ ,  $\tau_m$ , &  $g_m$  as  $L_{g,eff}$  is changed are plotted in figs. 6a and 6b. Both  $C_{gs}$  and the  $g_m$  delay,  $\tau_m$ , scale as  $L^{-1}$  for both the NMOS and the PMOS.  $R_g$  vs.  $L_{g,eff}$  scales with L for both device types.  $R_g$  for the PMOS (average  $R_g$  of 5.5 ohms/square) is close to the  $R_g$  for the NMOS (6.3 ohms/square). Under the gradual channel model,  $g_m$  vs.  $L_{g,eff}$  scales as  $L^{-1}$ . For the saturated velocity model,  $g_m$  is constant. In the NMOS, there is a weak scaling of  $g_m$  with inverse L which suggests that the majority of

the channel is in the carrier velocity saturation regime as suggested by the  $f_t$  vs.  $L_{g,eff}$  results. In the PMOS case,  $g_m$  vs.  $L_{g,eff}$  scales as  $L^{-\gamma}$ , where  $\gamma$  is less than 1 but higher than for the n-channel MOSFET which suggests that a smaller part of the channel is in the velocity saturation region. The PMOS results are consistent with the  $f_t$  vs.  $L_{g,eff}$  results. It is expected that the PMOS will eventually follow the NMOS trend as the gate length continues to shrink since the hole velocity will saturate at higher electric fields obtained with shorter gates at constant drain bias.

The high  $R_g$  of the digital MOSFETs with the silicide gate limits the microwave gain,  $f_{max}$ . Fortunately, the gate resistance in the digital process can be reduced with an Al overlay on the gate silicide.<sup>3</sup> Small signal modeling showed that the Al overlay would (by reducing  $R_g$  by a factor of 10 or more) result in an increase of  $f_{max}$  to around 40 GHz as shown in fig. 7. These results show that digital devices with high  $f_t$  can also achieve high  $f_{max}$  with the Al overlay.

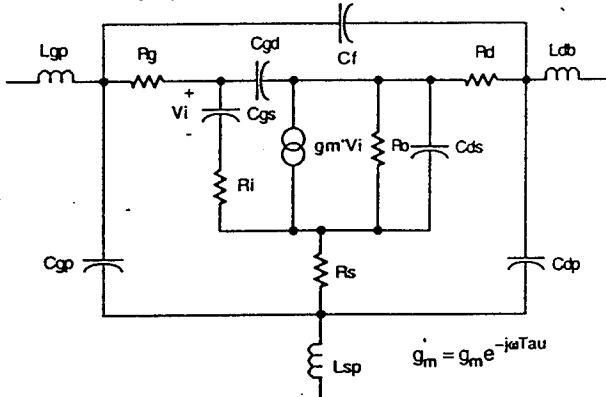


Fig. 4: Small signal MOSFET model (with pad parasitics)

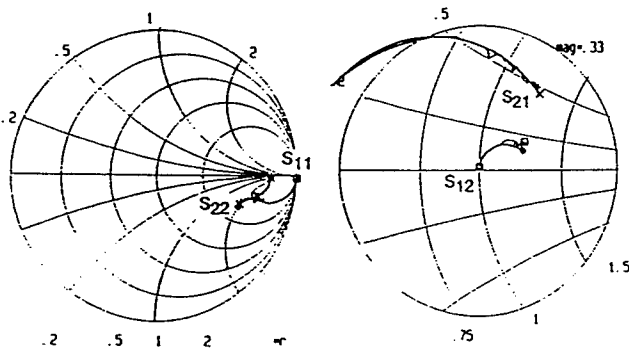


Fig. 5: Measured data vs. small signal model for a 0.5 mm NMOS a)  $S_{11}$  and  $S_{22}$  b)  $S_{12}$  and  $S_{21}$

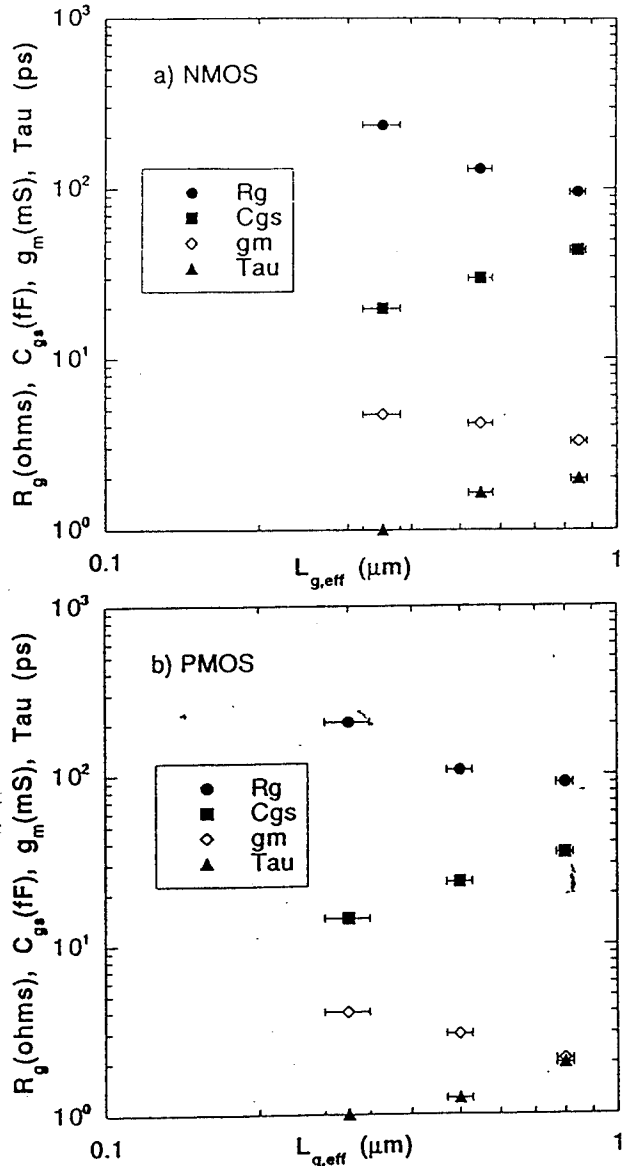


Fig. 6:  $C_{gs}$ ,  $g_m$ ,  $\tau$ , and  $R_g$  as a function of  $L_{g,eff}$  for a) NMOS, b) PMOS

	NMOS 1.0 $\mu\text{m}$	NMOS 0.7 $\mu\text{m}$	NMOS 0.5 $\mu\text{m}$	PMOS 1.0 $\mu\text{m}$	PMOS 0.7 $\mu\text{m}$	PMOS 0.5 $\mu\text{m}$	
$L_g$	50	50	50	50	50	50	pH
$R_g$	96	130	236	90	107	206	$\Omega$
$C_{gs}$	44	30	20	35	24	14	fF
$R_i$	65	70	79	60	58	67	$\Omega$
$C_{gd}$	17	14	14	22	16	14	fF
$R_o$	2200	1100	490	1580	670	177	$\Omega$
$C_{ds}$	0.01	0.012	0.03	0.01	0.02	0.028	fF
$R_s$	2	2	2	2	2	2	$\Omega$
$L_s$	0.02	0.02	0.02	0.02	0.02	0.02	pH
$R_d$	2	2	2	2	2	2	$\Omega$
$L_d$	86	55	40	85	62	13	pH
$G_m$	3.27	4.15	4.7	2.11	2.96	4.0	mS
$\tau$	1.98	1.64	1	2	1.25	1	ps

Table 2: Small signal model parameters extracted from the measured results

### Thin-Film SOS Comparison

The  $f_t$  values obtained by the digital thin-film SOS devices are compared to the state-of-the-art in Si and III-V FETS in fig. 8. The digital thin-film SOS devices with optically defined gates have performance similar to the microwave thin-film SOS devices fabricated with electron-beam lithography.<sup>3</sup> For the n-channel device, the state-of-the-art microwave SIMOX process (MICROX) results in a  $f_t$  of 23.6 GHz based on a gate length of 0.25  $\mu\text{m}$ .<sup>8</sup> The  $f_t$ 's similar to the results obtained with the SOS process; however, the gate length in the MICROX device is smaller. In comparison with the state-of-the-art bulk Si devices, the  $f_t$  of the thin-film SOS devices is lower due to the reduced electron mobility in SOS films; however, the comparison in performance is complicated by the fact that the bulk Si results are de-embedded and the SOS results are not de-embedded. Furthermore, the thin-film digital SOS MOSFET oxide thickness is not optimized for a specific gate length and is significantly thicker than that of the other devices especially at short gate lengths. The  $f_t$  vs.  $L_{g,eff}$  for both thin-film SOS and bulk Si NMOS scale as  $L^{-1}$ . The Si  $f_t$ 's are lower than the state-of-the-art III-V n-channel FET results.

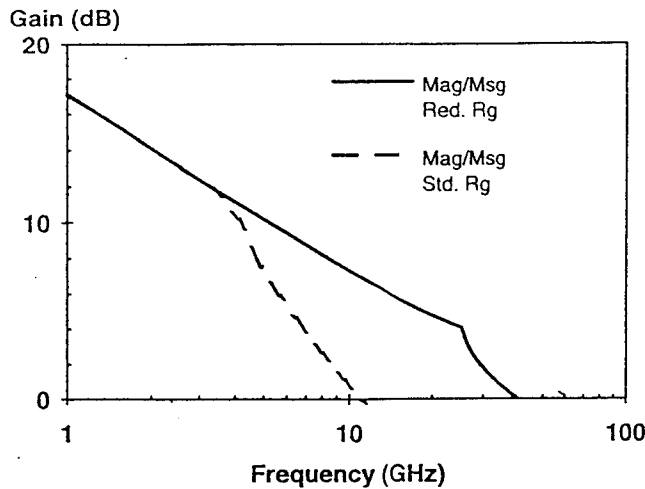


Fig. 7: Modeled  $f_{max}$  (std.  $R_g$ ) and extrapolated  $f_{max}$  with  $R_g$  reduced by a factor of 10 (red.  $R_g$ ); for example, with the Al overlay.

In bulk Si, the PMOS devices have significantly lower  $f_t$ 's than the n-channel counterparts for the same gate length. In thin-film SOS (both the digital and microwave), the PMOS have  $f_t$ 's that approach the NMOS for short gate lengths of 0.4  $\mu\text{m}$  or less. As compared to MICROX,  $f_t$  for a 0.25  $\mu\text{m}$   $L_g$  PMOS is 9.2 GHz which is lower than the thin-film SOS results.<sup>8</sup> The  $f_t$  of the thin-film PMOS is significantly higher than that of the either bulk Si or other SOI PMOS. The  $f_t$  vs.  $L_{g,eff}$  of both the bulk Si PMOS and the thin-film SOS PMOS have the same slope.

Like S.I. GaAs, the sapphire substrate used in SOS has many advantages for MMIC applications. For power devices, both wafers have similar thermal conductivity (0.42 W/cm<sup>2</sup>C for sapphire and 0.46 W/cm<sup>2</sup>C for GaAs). Sapphire has slightly lower dielectric constant (9.3 to 11.5 versus 13.1 for GaAs). Although microstrip transmission lines are difficult to form on sapphire due to the difficulty in etching back-side vias, co-planar transmission lines can be used, which do not require back side vias and wafer thinning. Both substrates should be able to yield high-Q and low-loss passive elements such as capacitors, inductors, and transmission lines. The large sapphire wafers (6 inches) can also potentially increase the throughput.

#### Conclusion

The measured and modeled results show that thin-film silicon on sapphire technology has achieved both n and p channel devices capable of high microwave gain, with  $f_t > 20$  GHz for optically defined gates. Small-signal models similar to those for GaAs FETs provide an accurate description of the SOS MOSFET characteristics. It is expected that the formation of an optically defined T-gate (by an Al overlay on the silicide/polysilicon gate) can significantly improve  $f_{max}$  and extend the frequency range of application. The sapphire substrates exhibit excellent microwave characteristics as compared to either bulk Si or many SOI substrates, and can utilize the same coplanar structures typically used in III-V MMICs. High performance NMOS combined with high performance PMOS in thin-film SOS technology can potentially lead to high-speed & high-efficiency power amplifiers as well as other high-speed and low-power microwave circuits. With thin-film SOS, microwave circuits can be fabricated using a proven low-power and high-speed digital LSI technology. This combination of features may be valuable in high-volume and low-cost portable communication applications.

#### Acknowledgments

The authors would like to acknowledge B. Offord, J. Ruthberg, G. Kelley, and members of the NRaD Microelectronics Lab for their assistance in this work. This work was supported by the ONR 6.2 Microelectronics Block at NCCOSC RDTE DIV.

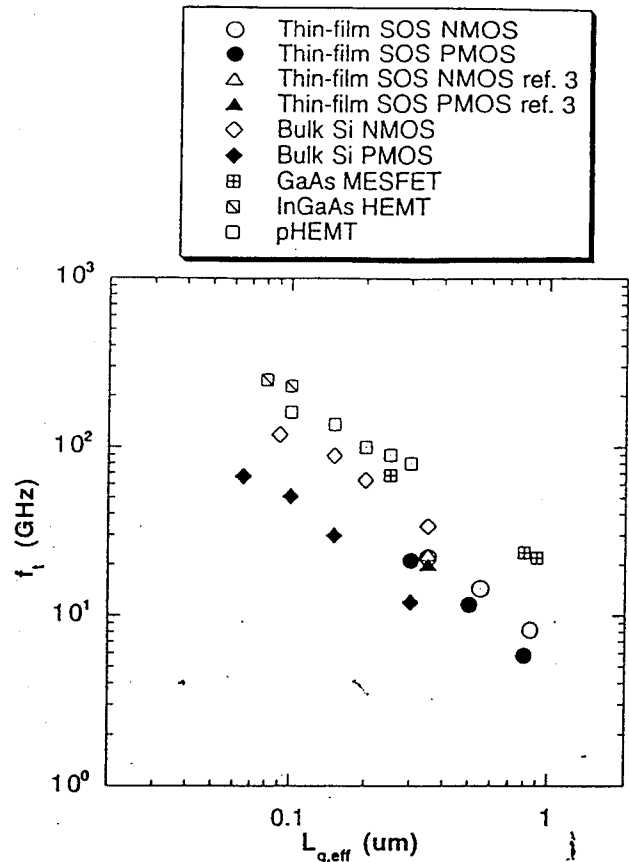


Fig. 8:  $f_t$  vs.  $L_{g,eff}$  for a variety of III-V and Si technologies

#### References

1. R. Yan, K. Lee, D. Jeon, Y. Kim et al, "89 GHz  $f_t$  room-temperature silicon MOSFETs," IEEE Electron Device Letters, 13, May 1992, pg. 256.
2. K. Lee, R. Yan, D. Jeon, Y. Kim et al, "0.1  $\mu\text{m}$  p-channel MOSFET with 51 GHz  $f_t$ ," IEDM Technical Digest, 1992, pg. 1012.
3. A. Schmitz, R. Walden, L. Larson, S. Rosenbaum, R. Metzger, J. Behnke, and P. Macdonald, "A Deep-Submicrometer Microwave/Digital CMOS/SOS Technology," IEEE Electron Device Letters, 12, Jan. 1991, pg. 16.
4. R. E. Reedy, G.A. Garcia, "Thin (100 nm) SOS for application to beyond VLSI microelectronics", Material Research Society Symposium Proceeding, 107, pg. 365, 1988.
5. M. Roser, S. Clayton, P. de la Houssaye, G. Garcia, "High-Mobility Fully-Depleted Thin-Film SOS MOSFET's," 1992 Device Research Conference, pg. BA-4.
6. A. Hughes, "Stress-induced anisotropy in the electrical properties of  $\text{Si}/\text{Al}_2\text{O}_3$ ," Journal of Applied Physics, 46 (7), July 1975, pp. 2849.
7. H. Schlotterer, "Mechanical and electrical properties of epitaxial Si films on spinel," Solid-state Electronics, 11, 947, 1968.
8. M. Hanes, A. Agarwal, T. O'Keefe, M. Hobgood, et al, "MICROX-an all silicon technology for monolithic microwave integrated circuits," IEEE Electron Device Letters, 14, May 1993, pg. 219.