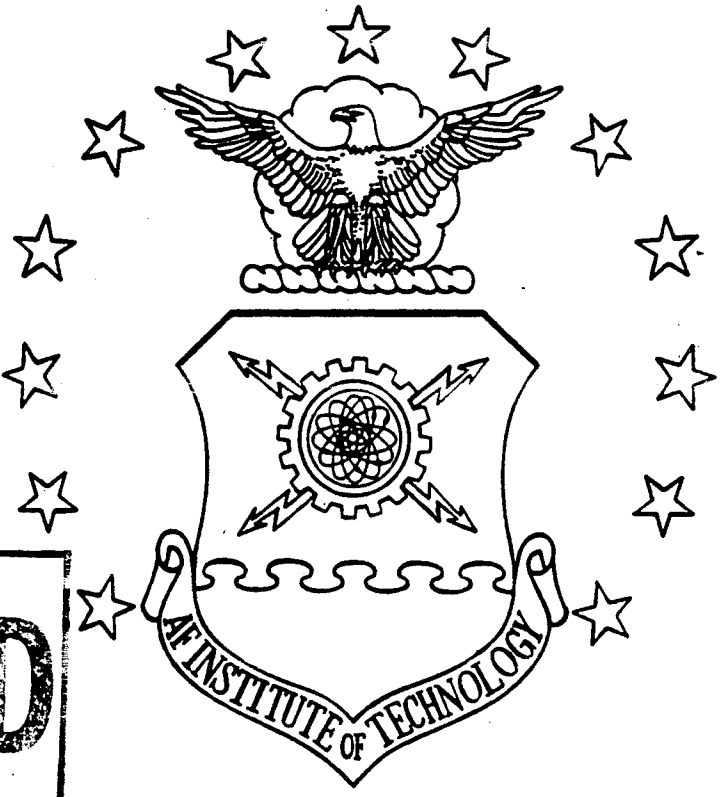

TOTAL IONIZING DOSE EFFECTS IN MOSFET DEVICES AT 77 K

THESIS

Kevin J. Daul, Captain, USAF

AFIT/GAP/ENP/94D-01

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY
AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

AFIT/GAP/ENP/94D-01

TOTAL IONIZING DOSE EFFECTS IN MOSFET DEVICES AT 77 K

THESIS

Kevin J. Daul, Captain, USAF

AFIT/GAP/ENP/94D-01

The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U. S. Government.

AFIT/GAP/ENP/94D-01

TOTAL IONIZING DOSE EFFECTS IN MOSFET DEVICES AT 77 K

THESIS

Presented to the Faculty of the Graduate School of Engineering
of the Air Force Institute of Technology
Air University
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Nuclear Engineering

Kevin J. Daul
Captain, USAF

December 1994

Preface

MOSFET technology is currently used extensively in the majority of electronic systems. When a MOSFET is exposed to ionizing radiation, the resulting effects from this radiation can cause severe degradation of the device performance and of its lifetime. This research investigated total ionizing dose effects on MOSFET devices, which utilized different oxide processes, while operating at 77 K.

I would like to express my thanks and appreciation to a number of people who assisted and supported me during the course of this project. Special thanks goes out to my faculty advisor, Major Paul Ostdiek, for his support and assistance throughout this research. In addition, I would also like to thank Dr. Bright and Captain Jeff Martin for their assistance and advice. I would also like to thank Mr. Lewis Cohn of the Defense Nuclear Agency, for sponsoring this research. Invaluable support and assistance was provided by Mr. Steven Clark and Mr. Patrick Cole of the Naval Surface Warfare Center during the experimental stages of this thesis. Furthermore, I would like to thank Mr. Jim Pickel of Maxwell Laboratories S-cubed division for his assistance during this research. Perhaps most of all, I would like to thank my wife Susan, and daughters Ambrosia and Kellsie, for their understanding and patience throughout the entire project.

Kevin J. Daul

Table of Contents

page

List of Figures

List of Tables

Abstract

Total ionizing dose effects on thermal oxide and reoxidized nitrided oxide (RNO) MOSFET devices operating at 77 K were studied. The MOSFETs were immersed in liquid nitrogen and irradiated, using a ^{60}Co source, up to 1 Mrad(Si) at a dose rate of 107 rads(Si)/sec. Drain current-gate voltage characteristics were obtained and used to determine threshold voltage and transconductance. At 77 K the subthreshold slopes indicated no observed buildup of interface states in any of the transistors. Furthermore, all transistors experienced very little change in the transconductance. Typical negative shifts in threshold voltage as dose increased were observed in all of the thermal oxide devices. The threshold voltage shifts of the RNO devices were typically less than those for thermal oxide devices.

TOTAL IONIZING DOSE EFFECTS IN MOSFET DEVICES AT 77 K

I. Introduction

The metal oxide semiconductor field effect transistor (MOSFET) is used extensively in digital circuit applications and is considered to be the core of integrated circuit design. By operating MOSFETs at cryogenic temperatures it may be possible to improve the efficiency or optimize some desirable characteristic of a device compared to operating at higher temperatures. There are several advantages of operating MOSFETs and integrated circuits at low temperatures. These advantages include: faster switching speeds due to increased mobility and decreased electrical resistance; increased reliability due to exponential slow down of thermally activated processes such as diffusion, electromigration, and chemical reactions; improved noise behavior due to reduced thermal noise; and greater packing density due to improved heat removal (1; 2). Furthermore, operation at low temperatures may be necessary if the semiconductor devices are to be used in conjunction with a system that operates at cryogenic temperatures.

As just mentioned, there are several reasons for using MOSFETs at cryogenic temperatures. However, ionizing radiation induced degradation effects in MOSFETs are a major concern. Ionizing radiation produces electron-hole pairs in the gate oxide. In a

thermal oxide the electrons are relatively mobile and are readily swept out of the oxide through the gate for a positive gate bias. The holes are relatively immobile and, under a positive applied gate potential, undergo a stochastic hopping transport process through the oxide to the oxide-semiconductor interface. Some of these holes will be captured in trapping sites near this interface, producing a negative shift in the threshold voltage. Additional interface states can also be generated during this process. This buildup of interface states occurs over a relatively long period of time and is a strong function of the electric field applied in the oxide. These radiation-generated interface states can cause additional shifts in threshold voltage as well as a reduction in carrier mobility.

Electronic systems that utilize MOSFETs may have to operate in environments consisting of low temperatures and ionizing radiation. Examples of these systems include, satellite systems, weapon systems, instrumentation for nuclear power plants, and detectors used in high energy physics experiments. Satellite systems require certain electronic components that must operate at cold temperatures while being exposed to ionizing radiation. For example, the signal processing electronics used for infrared focal plane arrays operate in a cryogenic/vacuum system. Infrared focal plane arrays are of importance to the military since they are used on Air Force surveillance and seeker systems. The military needs satellites for meteorological, communication, and navigation operations, as well as for surveillance and command-and-control operations. These operations are essential to the national security of this country. Many weapon systems also contain electronic components that may encounter severe radiation environments. Instrumentation and detectors that are used at nuclear power plants and at

experimental facilities can encounter similar environments that a satellite or weapon system may experience.

Satellites are exposed to naturally occurring ionizing radiation while passing through the Van Allen radiation belts. In addition to this natural environment, satellite systems, as well as weapon systems, may be exposed to a nuclear-enhanced environment created from the detonation of nuclear weapons.

Recently, in order to improve the hardness of MOSFETs to ionizing radiation, researchers have begun using nitrided oxides and reoxidized nitrided oxides (RNO) for the gate oxide. Nitrided oxides and RNO have demonstrated a reduction in threshold voltage shift after total ionizing dose, as well as suppressing the formation of radiation generated interface states, at both room and cryogenic temperatures (3-7). Furthermore, studies have found that nitrided oxides and RNO are superior to thermal oxides in terms of better process yield, greater dielectric strength, improved resistance under electrical stress, and better resistance to the diffusion of dopants or contaminants (4; 8). The oxide growth process is critical to the total dose hardness of nitrided oxides and RNO. Specifically, the time and temperature of the nitridation and reoxidation play a critical role in the susceptibility to total dose damage.

Ionizing radiation effects may degrade MOSFET performance and the useful lifetime of the device may be severely limited. Degraded MOSFET performance can have an adverse effect on total system performance. Thus, it is necessary to have electronic components exposed to an operational environment continue to function properly. Furthermore, MOSFETs need to be reliable and dependable when exposed to

low temperatures and ionizing radiation. Recently, nitrided oxides and RNO have been shown to be superior to thermal oxides in radiation hardness, offering promise in their future use.

This research investigates total ionizing dose effects in MOSFET devices, fabricated using different oxide processes, while operating at 77 K. Devices utilizing both thermal oxide and RNO processing were studied up to total doses of 1 Mrad(Si). The specific radiation effects that were investigated are threshold voltage shifts and changes in transconductance. These changes can be used to predict the performance of similar devices exposed to similar environments. Therefore, the goal of this study is to further the understanding of ionizing radiation effects and oxide processing in MOSFET devices operating at 77 K.

This first chapter provided an introduction into the problem of radiation effects in MOSFETs. The next chapter gives a select review of the literature in the area of total dose effects in MOS devices. Then, chapter 3 discusses the theory of basic MOSFET device physics, and of total dose effects. Included in this chapter are concepts involving charge generation, transport, and trapping in the gate oxide, as well as the creation of interface traps at the Si-oxide interface. Chapter 4 provides a description of the experimental research that was performed. This chapter contains descriptions on the test devices, equipment, and procedures used for this research. The results of the experimental research are presented and discussed in chapter 5. The final chapter, chapter 6, summarizes the research and offers recommendations and comments regarding future work into this area of study.

II. Literature Review

This chapter contains a review of the literature on the total dose effects in MOSFETs. The vast amount of information that has been published in this area is beyond the scope of this effort, so only the material directly related to this research is presented here. There are three major areas, each area comprises its own section, that are reviewed in this chapter. The first section contains a review on the important features of hole transport in both thermal and reoxidized nitrided oxides. The second section presents material on the concepts involved with the trapping of charge in oxides. The third section reviews the literature which deals with the formation of interface states at the Si-oxide interface.

2.1 Literature Review of Hole Transport

2.1.1 Review of Hole Transport in SiO_2. The 1970's saw a relatively large scale investigation into the hole transport properties in SiO_2. An important focal point of this investigation was the dispersive features of hole transport in SiO_2. This section presents several representative experiments which were taken from the literature which illustrate several important characteristics of hole transport in thermal oxides.

Much of the research into hole transport in SiO_2, performed by Boesch, McLean, and colleagues (9-13), consisted of irradiating MOS capacitors with a pulsed electron source. Flat band voltage shifts versus the time after the radiation pulse as a function of temperature and electric field were determined. Only negative flatband voltage shifts were observed due to the net positive charge induced in the oxide layer.

Boesch and McLean proposed that radiation generated electrons, due to their relatively high mobility, are swept out of the oxide while the radiation generated holes are left remaining near their point of generation. This results in rigid negative shifts along the voltage axis in the capacitance-voltage or current-voltage characteristics of the devices compared to their preirradiation characteristics. The voltage shift is proportional to the first spatial moment of the radiation-induced charge distribution relative to the gate. As the holes execute their relatively long transport toward the negative electrode, the changing charge distribution is reflected in the time dependence of the voltage shifts. The holes are collected at the negative electrode, resulting in the relaxation of the flatband voltage toward its preirradiation value.

From these experiments (9-13) it was observed that in every case the recovery, or hole transport, is very dispersive in time. This large dispersion was attributed to a wide distribution of individual hole transit times across the oxide layers. The effects of temperature and oxide field on hole transport in SiO_2 are shown in Figures 2-1 and 2-2 respectively. A feature common to all of the data is that changes in temperature and field did not have much effect on the shape of the recovery curves. Rather, the major effect of

changes in these parameters is simply to produce a translation of the curves along the time axis. This means that only the time scale for the transport is affected and not the amount of dispersion. Both Boesch and McLean successfully employed a stochastic model of hole transport based on the Continuous-Time Random Walk (CTRW) formalism of Montroll and Weiss to describe the time dispersion of their data (14).

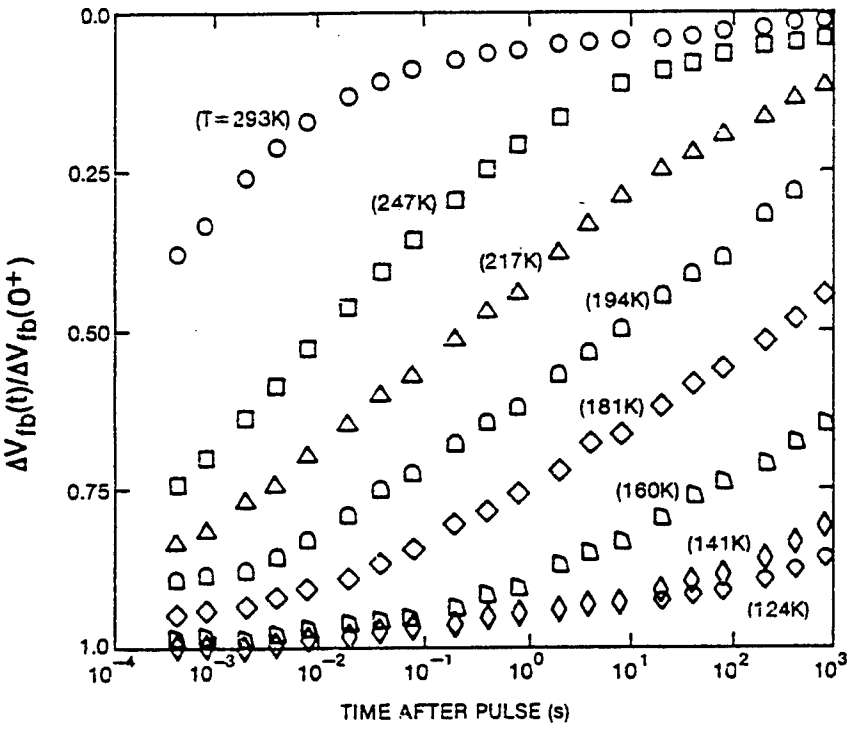

Figure 2-1. Flatband voltage recovery data following pulsed LINAC electron irradiation of 96.5 nm wet-grown oxide capacitor under 1 MV/cm oxide field for series of temperatures between 124 and 293 K. The data are normalized to the initial flatband voltage shift immediately after the radiation pulse (10).

As a result of the strongly temperature-activated nature of the transport, it was seen that very little transport occurred at low temperatures until relatively long times on the scale of the experiments. For example (see Figure 2-2), at 79 K and for a field of 3 MV/cm, the recovery only begins after 10 seconds and was not complete up to the longest measurement time of 1000 seconds (13). In addition, for fields less than 2 MV/cm, essentially no recovery took place for times of the order of thousands of seconds.

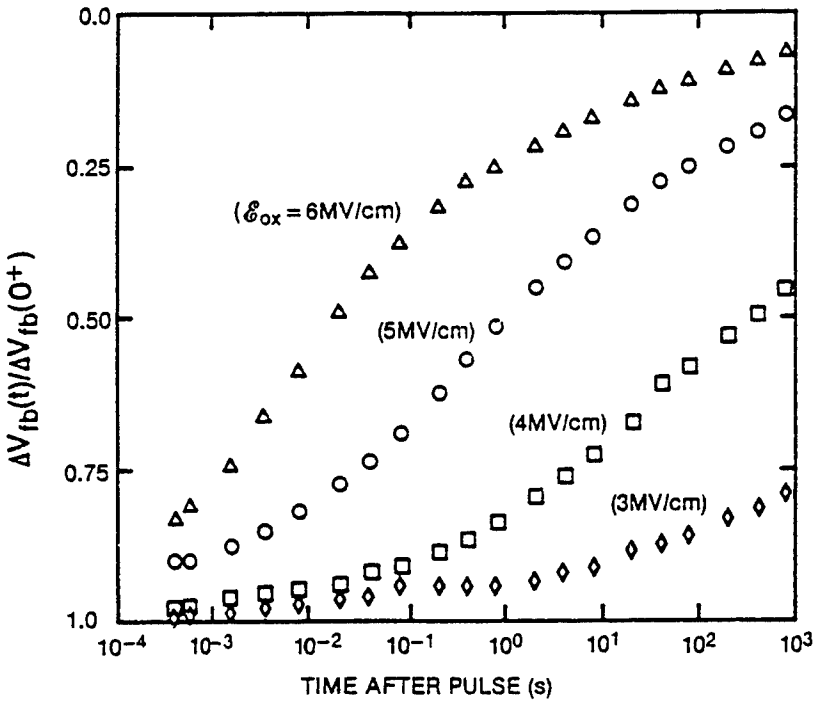

Figure 2-2. Normalized flatband voltage recovery data following pulsed LINAC electron-beam exposure for 96.5 nm oxide at 79 K and for oxide fields from 3 to 6 MV/cm (13).

2.1.2 Review of Hole Transport in RNO. Very little information on hole transport in reoxidized nitrided oxides (RNO) has been published. However, in 1991 Boesch and Dunn measured the charge generation and hole transport in both reoxidized nitrided oxides and radiation-hard thermal oxides (TO) (15). They measured these processes as a function of temperature from 77 to 295 K and applied fields from 1 to 5 MV/cm using pulsed irradiation and fast time-resolved current-voltage measurement techniques. It was determined that the radiation-generated charge yield in TO and RNO are essentially equal. In addition, the hole transport in RNO is qualitatively similar to that in TO. However, the temperature and field dependence of hole transport in RNO is quantitatively different from the dependencies in TO. It was observed that hole transport in RNO at low fields and near room temperature is significantly retarded with respect to that in TO, while the transport in RNO at 77 K for applied fields between 2 and 5 MV/cm is accelerated with respect to that in TO.

2.2 Literature Review of Trapped Charge

This section is concerned with the published literature regarding the microscopic nature of hole traps in TO, charge traps in RNO, and interface states. These areas of study are relatively new and there is still some uncertainty into exactly which microscopic point defects are responsible for the trapping of charge.

2.2.1 Review of Hole Traps in Thermal Oxides. Several microscopic point defects have been observed in irradiated TO (14; 16-18). The most important defect in thermal oxides has been determined to be the E' center (14; 16-18). The E' center was identified by Lenahan and Dressendorfer (17) to be the primary hole trap in TO. They showed a strong correlation between the E' center and radiation-induced positive charge for thermal oxides by using electron spin resonance (ESR) measurements. The E' center is a trivalent silicon defect associated with an oxygen vacancy in the SiO_2 structure. Figure 2-3(a) is a schematic diagram of the E' center in SiO_2. In addition to identifying the microscopic nature of the hole traps, the ESR measurements showed that the E' centers are concentrated near the Si-SiO_2 interface.

2.2.2 Review of Charge Traps in RNO. In 1992 Yount et al. (19) used ESR to study the radiation-induced point defects in thermal oxides, nitrided oxides (NO), and reoxidized nitrided oxides. It was determined that nitridation reduces the density of radiation-induced E' centers, and creates bridging nitrogen center precursors. A schematic diagram of a bridging nitrogen center is shown in Figure 2-3(b). A bridging nitrogen center is a nitrogen atom bonded to two silicon atoms, leaving two nitrogen bonds available for trapping charge. It is suggested that these bridging nitrogen centers

are probably electron traps, but this has not been conclusively proven. The reoxidation results in a reduction of the bridging nitrogen centers and an increase in the amount of E' centers. These E' centers were determined to be neutral (not positively charged as in thermal oxides) and did not seem to play an important role in hole trapping in RNO. The E' center in RNO is shown in Figure 2-3(c). It is currently uncertain as to which defect center does play an important role in hole trapping in RNO.

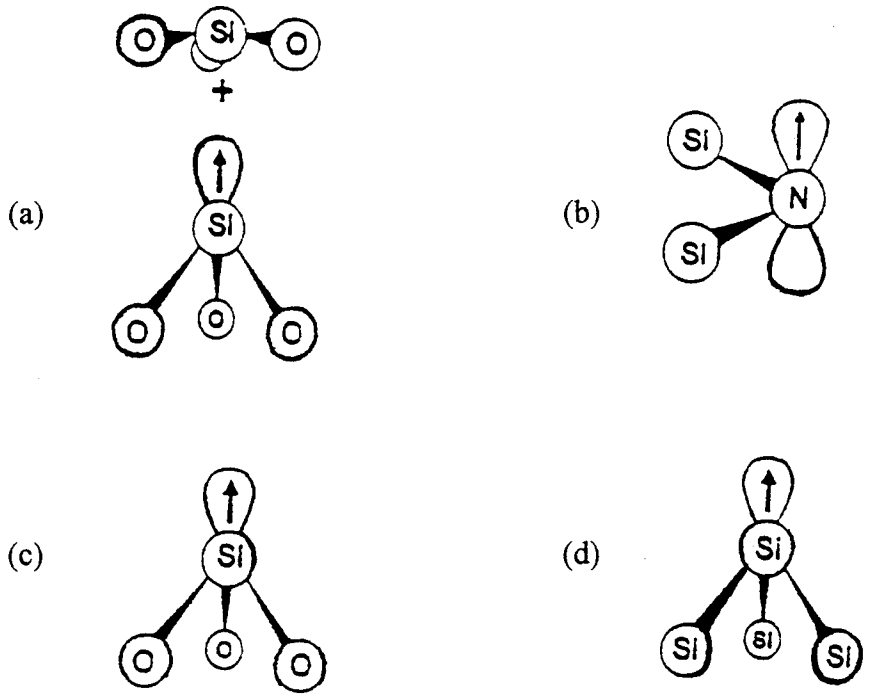

Figure 2-3. Schematic diagram of: (a) positive E' center in SiO_2; (b) bridging nitrogen center; (c) neutral E' center in RNO; (d) P_b center. The arrows indicate the direction of Jahn-Teller distortion (19).

2.2.3 Review of Trapped Charge in Interface States. ESR was used once again by Lenahan and others to identify the P_b center and associate it with the radiation-induced interface state (16; 18). Figure 2-3(d) is a schematic diagram of the P_b center. The P_b center was identified as an interface trap defect composed of a trivalent silicon bonded to three silicon atoms at the Si-oxide interface. Lenahan and Dressendorfer (17; 20) determined that the number of observed P_b centers correlated to the number of interface traps measured using capacitance-voltage measurements during irradiation and during post irradiation anneals.

2.3 Literature Review of Interface Trap Generation

In recent years, a great deal of electrical and microscopic information about radiation-induced interface traps has been obtained. Based on this information several models have been proposed to explain the generation of interface traps following exposure to ionizing radiation. The most accepted models are variations of a two-stage hydrogen transport model. Based on the results of several time-dependent and field-dependent experiments, it was determined that a positive ion (probably H^+) is responsible for the formation of interface states (21; 22). One common feature among almost all of the models is that they begin with the transport and /or trapping of radiation-generated holes.

This section is divided into three subsections. First, a description of the two-stage hydrogen model in SiO_2 is discussed. Second, experiments which support the two-stage hydrogen model in SiO_2 are presented. Third, a review of interface state formation in both TO and RNO is presented.

2.3.1 Review of Two-Stage Hydrogen Model in SiO_2. Svensson was the first to propose a two-stage hydrogen model for the buildup of interface traps (4). In the first stage of his model, radiation-generated holes react with some hydrogen containing species in the oxide causing the release of neutral hydrogen. The free hydrogen atoms diffuse to the Si-SiO_2 interface in the second stage, and break Si-H bonds at the interface to create the interface traps.

Winokur (23) modified this two-stage model to suggest that hydrogen ions, H^+, were released instead of neutral hydrogen. The first stage determines the saturated value of interface traps (i.e. the peak value of interface traps), and occurs during the period of charge generation and hole transport through the oxide. The saturated value is related to the production of electron-hole pairs in the oxide. Then, in the second stage, the liberated H^+ ions undergo a dispersive hopping transport which controls the rate of interface formation. The H^+ ions that reach the interface can break Si-H bonds at the interface creating the interface traps. This two stage hydrogen transport model is now believed to be the main process for radiation-induced interface state buildup.

In the previously described hydrogen transport model H^+ ions were released as holes transport through the oxide. In this model, an increase in electric field increases the energy a hole imparts to the oxide lattice as it transports through the oxide, causing more H^+ to be released. This would produce more interface traps with increasing field. This increase is true up to a point and then the interface trap buildup follows an approximate $E^{-1/2}$ field dependence.

A model to account for this field dependence was proposed by Shaneyfelt et al. (24). This model was called the hole-trapping/hydrogen transport $(HT)^2$ model. In this model the number of holes trapped determines the total number of interface traps (i.e. the saturated value) that buildup at a given electric field. Because the number of holes trapped scales as $E^{-1/2}$, the saturated value of interface trap buildup will follow the same field dependence. The $(HT)^2$ model involves, for positive gate bias, hole trapping near the Si-oxide interface, and the release of mobile H^+ ions near the interface. The H^+ ions transport to the interface and react to form interface traps. In the $(HT)^2$ model, H^+ transport is the rate limiting process.

2.3.2 Review of Experiments Supporting Two-Stage Hydrogen Model in SiO_2. A set of field switching experiments performed by Saks (25) supports a type of two-stage hydrogen model. Interface trap formation was measured using charge pumping on MOSFETs irradiated at 78 K and subjected to 20 minute isochronal anneals up to 350 K.

It was concluded that interface traps are produced during the annealing by two different processes at widely separated temperatures. The small process (< 10% of the total buildup) occurred around 120 K and was dependent on gate bias. The large process (> 90% of the total buildup) occurred between 200 and 300 K and was strongly dependent on gate bias. Saks proposed that the small process was caused by the reaction of radiation-induced neutral hydrogen with an interface state precursor at the Si-SiO_2 interface to produce an interface trap. He further suggests that the large process is caused by the reaction of radiation-induced neutral hydrogen and holes to produce H^+, which drifts to the interface region in response to the applied field, and reacts at the interface to produce the interface traps.

Shaneyfelt (24) performed a study of radiation-induced interface trap buildup rates in wet and dry oxides (20 nm to 100 nm) for both positive and negative bias irradiations followed by positive bias anneals. The observed buildup rates were consistent with the predictions of the $(HT)^2$ model. For the case of positive bias during irradiation and anneal, he observed that the time-dependent buildup of interface traps is nearly independent of oxide thickness for both wet and dry gate oxides. For the case of negative gate bias during irradiation and positive bias anneal, he observed a thickness dependence for both the wet and dry oxides. These thickness dependencies suggest that the way in which hydrogen is incorporated in the oxide during processing may play a key role in determining whether H^+ is released in the bulk of the oxide or near the interface.

The details of the mechanisms for the buildup of interface traps still needs to be resolved. It is apparent that hole transport and/or trapping either in the bulk of the oxide or near the interface is important for interface formation. In addition, the release of hydrogen also seems to be involved in one way or another with the buildup of interface states.

2.3.3 Review of Interface State Formation. It has been demonstrated that the formation of interface states is suppressed in thermal oxides at low temperatures. Saks et al. (25; 26) measured the formation of interface traps in thermal oxides using a charge pumping technique on MOSFETs irradiated at temperatures ranging from 78 to 285 K. They found that interface states are not formed by radiation at the low temperatures in thermal oxides. However, when the MOSFETs were warmed up to 295 K after irradiation at 80 K, interface states then formed with approximately the same density as would have been observed for irradiation at 295 K. They concluded that the process of interface state formation is not eliminated at 80 K, but rather is effectively frozen out. Based on the current understanding of interface state formation (two-stage hydrogen models), it seems that the reason why Saks et al. did not observe any interface state formation is because at 80 K the hydrogen ions would be immobile, and therefore incapable of transporting to the interface and reacting to form interface states.

Dunn and Wyatt (6) performed an experiment in which p-channel MOSFETs with 37 nm reoxidized nitrided oxides were irradiated using 10 keV X-rays at room temperature. These devices exhibited only a -1.45 V shift in the midgap voltage after

irradiation up to 55 Mrad(SiO_2). Furthermore, no change in subthreshold slope was measured, even at this extremely high dose. This indicates that the interface state generation was completely suppressed in the reoxidized nitrided oxides.

Terry et al. (7) exposed nitrided oxide devices to 1.5 MeV electrons up to a total dose of 1 Mrad(Si) at room temperature. They did observe a very small distortion of the capacitance-voltage curve at 1 Mrad(Si). This is attributed to a very small buildup of interface states. They suggested that the suppression of interface state generation in the nitrided oxides may be related to the buildup of nitrogen near the insulator-silicon interface.

Bhat and Vasi (5) irradiated reoxidized nitrided oxide MOS capacitors at room temperature with a ^{60}Co source at a dose rate of 380 krad(Si)/hr up to 2.2 Mrad(Si). They observed very little interface state generation even at such high dose levels. They suggest that this implies that hydrogen does not play a role in interface state generation in RNO and the transport of H^+ ions is inhibited due to the oxynitride layer near the Si-SiO_2 interface. They conclude that the major interface state component in thermal oxides (H^+ transport) is suppressed in RNO and the small buildup is due to trapped hole recombination. Trapped hole recombination suggests that radiation-generated holes get trapped near the Si-oxide interface and are converted into interface traps by electron injection. Electrons tunnel from the substrate to annihilate the trapped holes producing a structural change at the interface and resulting in a weak or dangling silicon bond that acts as the interface trap (36; 39).

III. Theory

MOSFETs are unipolar devices since current is transported predominately by carriers of one polarity only, holes in a p-channel device and electrons in an n-channel device. The MOSFET consists of a silicon substrate, an insulator (gate oxide) region, and a conducting gate. It is a four terminal device with an n-channel device consisting of a p-type semiconductor substrate terminal, source and drain terminals which are heavily doped n^+ regions, and a gate terminal. The gate is formed by placing a metal contact onto the insulator. Heavily doped polysilicon can be used instead of a metal to form the gate. Figure 3-1 is an example of a n-channel device. A p-channel device would consist of a n-type semiconductor substrate with the source and drain being heavily doped p^+ regions. This chapter provides a description of the different types of MOSFETs, threshold voltage, MOSFET operation, transconductance, ionizing radiation, total dose effects on MOSFETs, bias effects, and concepts involving different oxide processes.

3.1 Types of MOSFETs

There are basically four types of MOSFETs. There are n-channel enhancement mode and depletion mode devices as well as p-channel enhancement and depletion mode devices. In the enhancement modes the semiconductor substrate is not inverted directly

under the oxide with zero applied gate voltage. In the depletion modes the substrate is inverted directly under the oxide for zero applied gate voltage.

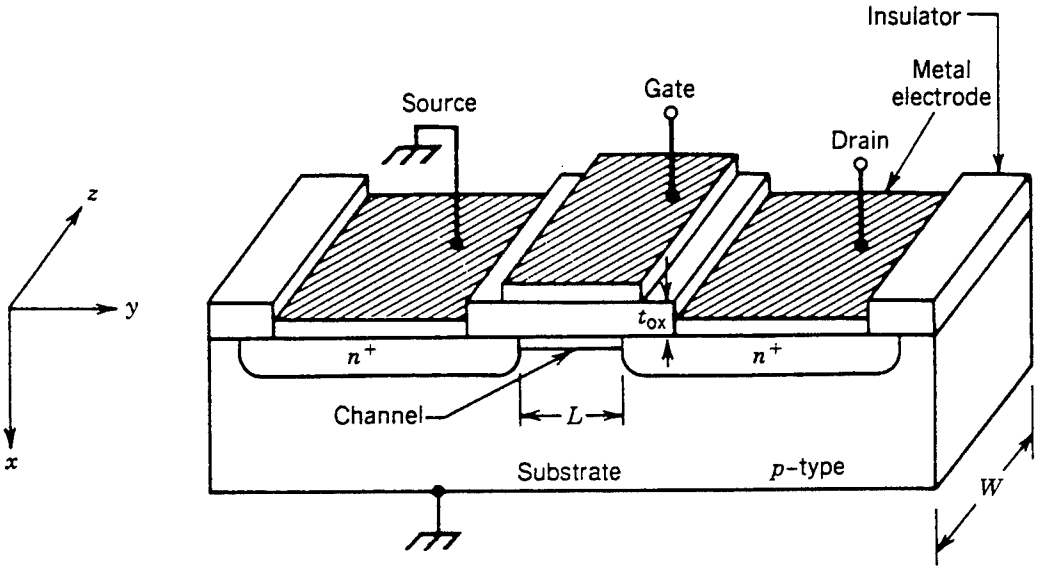

Figure 3-1. Cross-section of a simplified n-channel MOSFET showing the basic elements (14:4).

For the n-channel enhancement (normally off) MOSFET a positive gate voltage induces an electron inversion layer, which forms the channel between the n-type source and drain regions. In an n-channel device the electrons will flow from the source to the drain region. If an n-channel exists at zero gate bias then a negative bias must be applied to the gate in order to deplete carriers in the channel, reducing the channel conductance. This is the n-channel depletion (normally on) MOSFET. The n-channel can be an electron inversion layer or an intentionally doped n-region. In the p-channel enhancement mode

MOSFET a negative gate voltage needs to be applied to create an inversion layer of holes which forms the channel between the p-type source and drain regions. A positive gate voltage is needed to "turn off" the p-channel depletion mode device since a p-channel exists for zero gate voltage. Holes flow from the source to the drain in a p-channel device.

In an n-channel device the concentration of electrons in the channel increases with increasing gate voltage so the magnitude of the current for a given drain voltage can therefore be modulated by changing the gate voltage. A p-channel device is similar except the concentration of holes in the channel increases with a negative increase in voltage. The gate voltage that is required to cause appreciable current to flow is called the threshold voltage and is described next.

3.2 Threshold Voltage

In order to understand the threshold voltage consider a p-type semiconductor substrate where a positive gate voltage is applied. An energy band diagram of such a device is shown in Figure 3-2. The surface of such a device has been inverted from a p-type to an n-type region so that there is an inversion layer of electrons at the oxide-semiconductor interface. E_{Fi} is the intrinsic Fermi level and E_F is the Fermi level. E_c is the conduction band energy and E_v is the valence band energy. ϕ_s is the surface potential and is the difference between E_{Fi} measured in the bulk semiconductor and E_{Fi}

measured at the surface.

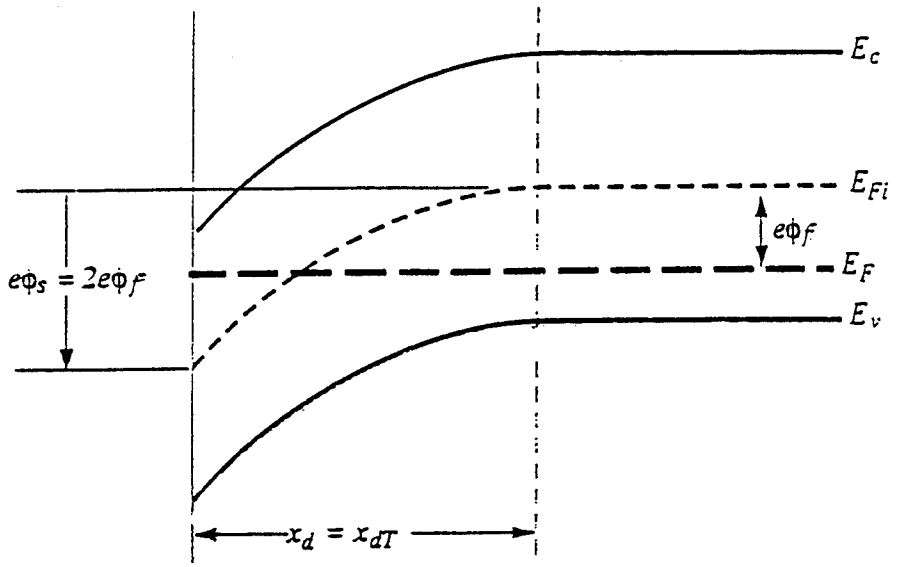

Figure 3-2. An energy-band diagram for a p-type semiconductor at threshold inversion (27: 497).

The bulk potential, ϕ_f, is the difference between the intrinsic Fermi level and the Fermi level and is expressed by (27)

$$\phi_f = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right) \tag{3-1}$$

N_a is the acceptor doping concentration and n_i is the intrinsic carrier concentration. The intrinsic carrier concentration is strongly dependent on temperature and is given by (27)

$$n_i^2 = N_C N_V \exp\left[\frac{-E_g}{kT}\right] \qquad (3\text{-}2)$$

The Boltzmann constant, k, is 1.38×10^{-23} J/K, T is the temperature, and q is the electronic charge. E_g, the bandgap energy, increases as temperature decreases and is about 1.17 eV at 77 K for silicon (30). N_c and N_v are the effective densities of states in the conduction band and valence band respectively. Figure 3-2 shows the case for which $\phi_s = 2\phi_f$ so that E_F at the surface is as far above E_{Fi} as E_{Fi} is above E_F in the bulk semiconductor. The concentration of electrons at the surface is the same as the hole concentration in the bulk semiconductor. This condition is known as inversion and the gate voltage that creates this condition is defined as the threshold voltage, V_T. The threshold voltage can be looked at as being the gate voltage required to cause an appreciable current to flow.

The threshold voltage is a function of several parameters including semiconductor material, oxide material, temperature, and semiconductor doping. The threshold voltage is a very important parameter which must be within the voltage range of a circuit's design. Since the threshold voltage is the point at which the transistor "turns on", any shifts in V_T could prevent the device from being turned on with the operable circuit

voltages. The equation which represents the threshold voltage is presented here without any derivation. The threshold voltage is expressed by (14; 27)

$$V_T = 2\phi_f + \phi_{ms} + \frac{1}{C_{ox}}(Q_{sd} - Q_{ox} - Q_{it}) \qquad (3\text{-}3)$$

where $Q_{sd} = 2(qN_a \varepsilon_s \phi_f)^{1/2}$, and is the maximum space charge density per unit area of the depletion region,

ε_s is the permittivity of the semiconductor,

Q_{ox} is the trapped oxide charge,

Q_{it} is the interface trapped charge, and is discussed in a further section,

$C_{ox} = \varepsilon_{ox}/d_{ox}$ is the oxide capacitance per unit area, where ε_{ox} is the permittivity of the oxide and d_{ox} is the oxide thickness,

and ϕ_{ms} is the metal-semiconductor work function difference.

Positive trapped oxide charge will cause negative shifts in the threshold voltage for both n-channel and p-channel devices, whereas negative trapped oxide charge produces positive threshold voltage shifts. The interface trapped charge can cause either positive or negative shifts in the threshold voltage depending on the type of carrier present in the interface trap. Later sections present a more detailed discussion on both the trapped oxide charge and interface trapped charge and their effects on threshold voltage. The temperature dependence of V_T mainly arises from the temperature dependence of the

bulk potential which in turn is caused primarily by the strong temperature dependence of the intrinsic carrier concentration. Therefore, the threshold voltage will increase as the temperature of a device decreases since ϕ_f increases as temperature decreases.

3.3 MOSFET Operation

This section describes the basic operation of a MOSFET. To understand the basic operation of a MOSFET an n-channel enhancement mode device is used as an example. When the gate voltage, V_G, is less than the threshold voltage, the channel region contains very few electrons and many holes. Under these conditions no appreciable current can flow between the source and drain. When the gate is biased so that inversion occurs ($V_G > V_T$), a significant number of mobile electrons are present in the channel region producing a conduction channel for electrons, which connects the source and drain regions. The conduction channel is the gray region in Figure 3-3(a). The number of mobile electrons, and therefore the channel conductance, increase with increasing gate voltage. It is therefore possible to modulate the source-drain conductance by changing the applied gate voltage.

Next look at the effect of drain bias, V_D, after the inversion channel has been formed. For small applied drain voltages the conduction channel will behave as a simple resistor, so that the drain current, I_D, will be directly proportional to V_D. This is called

the linear region of operation. As V_D is increased the potential drop along the channel due to the channel current starts to negate the inverting effect of the gate which means

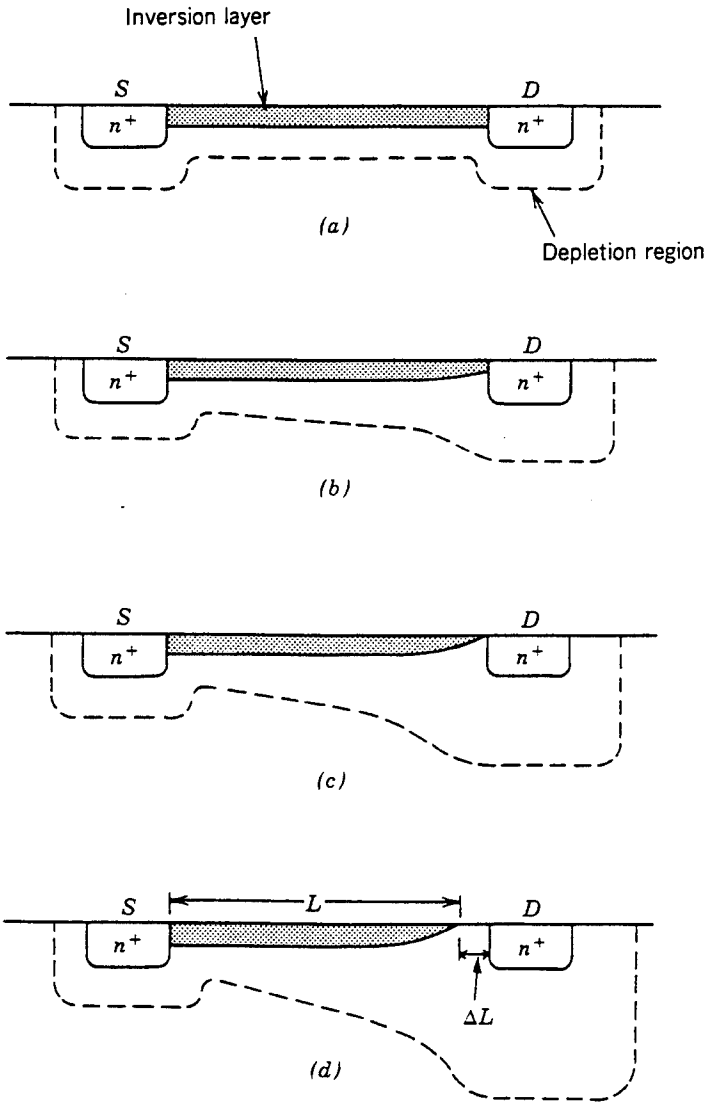

Figure 3-3. Diagram of an n-channel MOSFET showing the conduction channel after the device is turned on: (a) $V_D = 0$; (b) $V_{Dsat} > V_D > 0$; (c) $V_D = V_{Dsat}$; (d) $V_D > V_{Dsat}$ (14:24).

that the induced inversion charge density near the drain also decreases. Therefore the inverted channel narrows near the drain and the number of channel electrons decreases as shown in Figure 3-3(b). In addition, the conductance of the channel at the drain decreases which means that the slope of the I_D-V_D curve will decrease. The greatest increase in the depletion region width, which corresponds to the greatest decrease in number of channel electrons, occurs near the drain terminal. When V_D increases to the point where the potential drop across the oxide at the drain terminal is equal to V_T, the induced channel inversion charge is zero at the drain terminal. This is referred to as "pinch off" because the normal conduction channel disappears next to the drain, this is shown in Figure 3-3(c). When the channel pinches off, current saturation occurs so that the slope of the I_D-V_D curve is approximately zero. This region is referred to as the saturation region. For drain voltages greater than the pinch off voltage, V_{Dsat}, the pinched-off portion off the channel widens from just a point into a depleted channel section, ΔL, and the drain voltage in excess of V_{Dsat} is absorbed almost entirely across ΔL, as shown in Figure 3-3(d). Electrons will enter the channel at the source, travel through the channel to the point where the charge goes to zero and then get injected into the depleted region where they are swept by the electric field to the drain.

3.4 Transconductance

The transconductance, gm, is the change in drain current with respect to the corresponding change in gate voltage and is given as

$$gm = \frac{\partial I_D}{\partial V_G} \tag{3-4}$$

The transconductance is also referred to as the transistor gain.

For an n-channel MOSFET operating in the nonsaturation region we have (28)

$$gm = \mu_n C_{ox} \frac{W}{L} V_D \tag{3-5}$$

The transconductance in the saturation region is given by (28)

$$gm = \mu_n C_{ox} \frac{W}{L} (V_G - V_T) \tag{3-6}$$

Where W and L are the channel width and channel length respectively. It is observed from the above equations that the transconductance is proportional to the effective carrier mobility, μ_n, in the channel. The carrier mobility will vary with applied gate voltage and the temperature. For temperatures down to 77 K, both the electron mobility and hole mobility in silicon will increase as the temperature is lowered (1; 2; 27; 28). This

increase in mobility is due to a decrease in phonon scattering as temperature is lowered (27; 28). Since the mobility increases with decreasing temperature the transconductance will also increase as the temperature decreases.

The carrier mobility also depends on the carrier scattering due to oxide and interface charge (14). Ionizing radiation can cause trapped oxide charge and interface state buildup. The interface states cause a distortion, change in slope, in the characteristic I_D-V_G curve (14; 27; 29; 30), thus, a change in the transconductance is observed. At 77 K very few, if any, radiation-generated interface states build up at the Si-oxide interface (25; 26; 31; 32), which is discussed in more detail in section 3.6.3. Therefore, at 77 K any change in the transconductance can be attributed to the mobility dependence on carrier scattering due to the radiation-generated trapped charge in the oxide. The next section discusses ionizing radiation, specifically the ionizing radiation resulting from the decay of ^{60}Co to stable ^{60}Ni.

3.5 Ionizing Radiation

As a charged particle, such as an alpha or a beta particle, passes through matter it will occasionally approach close enough to an atom (or molecule) for the electrical interaction to be sufficient to completely remove an orbital electron from the atom. This complete removal of an electron from the atom is called ionization. What is left of the atom, after the electron is removed, is a positively charged ion. Therefore, an electron

and ion are formed, and the combination of the two particles is called an ion pair. Gamma rays and x-rays do not carry any electrical charge; however, as they pass through matter these rays still cause the ejection of electrons. These ejected electrons are electrically charged and can produce considerable ionization (i.e., create electron/hole pairs).

Ionizing dose from gamma rays, which are produced in the decay of ^{60}Co to stable ^{60}Ni, can be used to simulate operational environments encountered by MOSFETs. Gamma rays are quanta of electromagnetic radiation with wavelengths ranging from 10^{-13}m to 10^{-11}m (29). Gamma rays occur in a radioactive change when a nucleus is formed in an excited state. The excess energy of this excited nucleus is released as gamma radiation. In the decay of ^{60}Co to stable ^{60}Ni two gamma rays of 1.17 and 1.33 MeV are released (33; 34).

There are three principle ways in which gamma rays interact with an absorbing material. These interactions are; the photoelectric effect, the Compton effect, and pair production. At low energies the photoelectric effect dominates the other interactions. As the photon energy increases the Compton effect becomes the dominate form of interaction. For very high energy gamma rays, minimum of 1.02 MeV, pair production occurs. All three interactions are ionizing processes in that electron/hole pairs are produced. Gamma rays from ^{60}Co interact with a MOSFET primarily by Compton scatter. This is due to the energy of the gamma rays and the nature of the interacting materials, mostly Si and SiO_2. Figure 3-4 is a diagram of a Compton interaction. It

shows a gamma ray making an elastic collision with an electron of the absorbing material. In the collision, part of the energy of the incident gamma ray is transferred to the electron. Another (scattered) gamma ray of lower energy then moves off in a new direction, so that it is scattered from its initial path. Both the recoil electron and scattered gamma ray can produce more ionization. The average energy of the gamma rays from ^{60}Co is 1.25 MeV and the Compton cross section for these gamma rays in Si and SiO_2 is 0.06 cm^2/g which is 0.999 of the total interaction cross section (33; 34). In Si and SiO_2, because of similar cross sections, an equal number of electrons will be produced. The range of these electrons can be several millimeters since it is dependent on the energy of the electron.

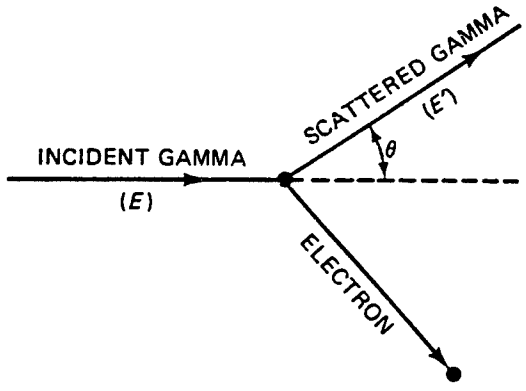

Figure 3-4. Diagram showing a Compton Interaction (33).

This section described the ionizing radiation that can be used to simulate the operational environment of MOSFETs. The absorption of this radiation by the MOSFET materials is referred to as the ionizing dose. The next section discusses the total dose effects of this ionizing radiation on MOSFETs operating at cryogenic temperature.

3.6 Total Dose Effects

The gate oxide is the most sensitive part of a MOSFET to ionizing radiation. The basic radiation-induced processes are presented in Figure 3-5. In the first process, gamma rays (ionizing radiation) interact with the oxide material producing electron-hole pairs. In the presence of an electric field, either internal or applied, these radiation generated electrons and holes can move through a material. The generated electrons are much more mobile than the holes, and are swept out of the oxide within a few picoseconds. However, a certain fraction of the electrons and holes will recombine within the first picosecond (34). The amount that recombine depends on the applied electric field and on the energy and type of ionizing radiation. The holes which escape this initial recombination are relatively immobile and remain near their point of origin, producing a negative threshold voltage shift. However, over a period of time extending to about one second at room temperature and to tens of thousands of seconds at cryogenic temperatures, the holes undergo a stochastic hopping transport through the oxide in response to any electric field present (9-13).

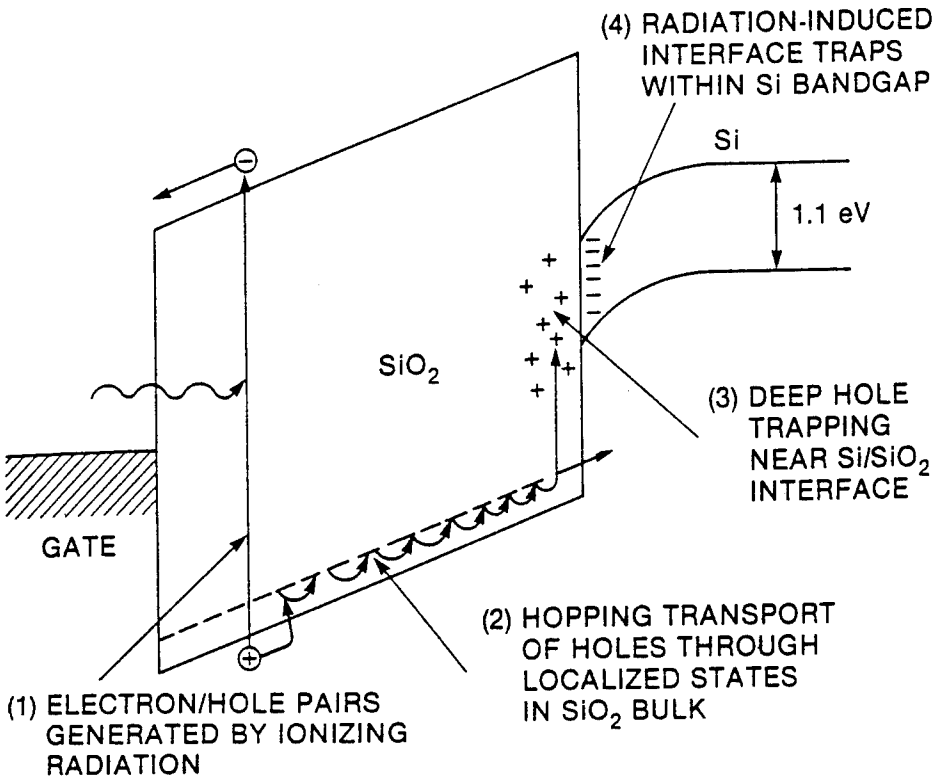

Figure 3-5. The basic ionizing radiation-induced effects in MOS structures, for a positive applied gate bias (34: 89).

3.6.1 Hole Transport. The second process shown in Figure 3-5 is the transport of the holes, under positive applied bias, to the Si/oxide interface by the hopping transport. This

hole transport is temperature activated and very dispersive in time, and gives rise to a short-term, transient recovery in the voltage shift (9-13). A Continuous Time Random Walk (CTRW) model is used to describe hole transport in the oxide (9-13; 34). The specific intersite charge transfer hopping mechanism is a polaron-like hopping of the holes between localized, energetically shallow trap states having a random spatial distribution (9; 10; 13). Polaron is the term given to the situation in which the charge carrier (in this case a hole) interacts with the lattice, inducing a distortion near the carrier. As the carrier moves through the lattice it carries the distortion with it. The hopping is a phonon-assisted tunneling transition between two localized trap sites.

The radiation response is a function of a disorder parameter, α, and a characteristic transit time. The disorder parameter, which describes the dispersion, is proportional to the density of localized states and has a value between zero and one (12; 34). The smaller the value of α, corresponding to a lower density of hopping sites, the more dispersive the transport becomes. The characteristic transit time depends strongly on oxide thickness, temperature, and electric field.

Dispersive charge transport is directly attributed to a wide distribution of transit times of the individual carriers through the material. Some carriers will transit the material very rapidly through a succession of rapid hops, while other carriers are immobilized at some point for relatively long periods of time (10; 12; 13; 34). Dispersive transport is non-Gaussian and has the feature of an apparent time-dependent mobility or a thickness-dependent mobility. As a carrier travels further it has a greater chance of finding itself in a trapping site where the next hop is a relatively far away site,

resulting in longer waiting times between hops. These long waiting times are due to the random spatial distribution of the traps. Therefore, the effective mobility of the carriers decreases with time so that the average transit time of carriers through the material varies superlinearly with thickness.

Hole transport is temperature activated, and the activation energy is temperature dependent. There are two distinct temperature regions: a high-temperature region in which the transport is strongly activated, and a low-temperature region in which the transport becomes essentially nonactivated. The transition temperature from activated behavior to nonactivated behavior is given by (34)

$$T_T = \frac{T_D}{\nu} \tag{3-7}$$

where T_D is the Debye temperature and is approximately 600 K for SiO_2, and ν is a numerical factor, depending primarily on the phonon spectra of the solid, and is about 4 for SiO_2 (34). Therefore, T_T is approximately 150 K for SiO_2. The transition temperature for a given material increases with increasing density of localized sites. Therefore, in SiO_2 at temperatures below 150 K the hole transit time is much greater then transit times above 150 K. Thus, there is very little hole transport below T_T until extremely long times so that the holes are essentially frozen in place very near their point of origin.

Hole transit time is strongly dependent on the electric field strength. At low field strengths the hole transport is relatively long compared to times at high field strengths. At low temperatures holes are relatively immobile unless a large electric filed is present. For example, in SiO_2 at 80 K and for $E_{ox} = 3$ MV/cm, the transport only begins after about 10 s, but for $E_{ox} < 2$ MV/cm, essentially very little transport takes place for times on the order of thousands of seconds (13). It has been shown that hole transport is a complex function of several variables including the applied electric field, temperature, and oxide thickness. The next section discusses the trapping of the charge within the oxide.

3.6.2 Trapped Charge. For positive gate voltages the holes move toward the Si-oxide interface where some become captured in long-term trapping sites, while the others flow into the silicon substrate. This long-term trapping of the holes is illustrated as the third process in Figure 3-5. A hole trap is a neutral oxide defect that can capture a hole and retain it for long periods of time. Based on electron spin resonance (ESR) spectroscopy studies, the microscopic structure of the trapped holes has been determined to be the E' center (16-18). The E' center is a trivalent silicon defect associated with an oxygen vacancy in the oxide structure. The Si-oxide interface region is characterized by local strain associated with the sudden change in material composition and the presence of oxygen vacancy defects (strained Si-Si bonds). A hole that encounters a strained bond, may break the bond and recombine with one of the bonding electrons. The resulting

positively charged structure relaxes into the E' center, with one of the silicon atoms retaining the remaining electron from the broken bond.

The radiation generated holes encounter a distribution of hole traps that starts at the Si-oxide interface and extends several nanometers into the oxide (16-18). Up to this point, two types of radiation-induced defects in the oxide (trapped oxide charge and interface traps) have been discussed. Oxide traps that are very close to the interface can transfer charge back and forth from the silicon relatively easily. These near interfacial oxide traps behave like interface traps, and are called border traps (4). For the purpose of this study, border traps are considered to be identical to interface traps, which are addressed in the next section. Depending on the density and the hole capture cross-section of the hole traps a fraction of the holes incident on the trap distribution will be captured. The remainder continue into the Si and eventually recombine. The hole trap densities depend on the oxide and device processing. The efficiency of hole capture by the traps is a function of the electric field in the oxide. The effective hole trap cross section has been observed to vary as the inverse square root of the electric field ($E^{-1/2}$) in the oxide for fields above about 1 MV/cm (34; 35). The trapped holes cause a negative threshold voltage which can last for several hours to years. This effect dominates the other radiation damage processes such as negative charge trapping and interface trap buildup effects. Interface traps, their buildup, and their effect on MOSFETs will be covered in the next section.

Most of the holes which get captured by hole traps within 2 to 5 nm of the silicon are removed by a tunneling process thought to be primarily responsible for the long-term annealing of the threshold voltage shift (4; 14). Electrons from the silicon tunnel to, and recombine with, the trapped holes contained in the distribution of traps near the Si-oxide interface. In addition, electrons which are generated in the oxide, either within the distribution of hole traps or between the distribution and the silicon, are swept through the distribution of traps for positive gate voltages. Some of the electrons will recombine with the trapped holes. This recombination depends on the density of trapped holes and the electron capture cross-section of trapped holes. The radiation generated holes and their long-term trapping produce negative threshold voltage shifts. The electron and trapped hole recombination, and the tunneling process reduce this threshold voltage shift.

For negative applied gate voltages, the radiation generated holes move toward the gate terminal. Now the holes can become trapped near the oxide-metal interface. The trapped charge in this region near the oxide-metal interface has less effect on the threshold voltage. This difference is due to the fact that the threshold voltage shift not only depends on the amount of trapped charge, but also on the location of the charge. The shift in threshold voltage due to oxide charge is (14)

$$\Delta V_T = -\frac{1}{C_{ox}} \int_0^{d_{OX}} \frac{x}{d_{ox}} \rho(x) dx \qquad (3\text{-}8)$$

Where x is the distance from the oxide-metal interface to the trapped charge and $\rho(x)$ is the spatial distribution of the oxide charge density. It needs to be made clear that this trapped charge can be either positive or negative. Trapped charge located near the oxide-metal interface produces a minimum threshold voltage shift where as that same charge placed at the Si-oxide interface produces a maximum threshold voltage shift. In most cases the trapped oxide charge tends to be in the form of a sheet charge (14). For a sheet charge located a distance x from the oxide-metal interface the shift in threshold voltage due to the oxide charge is

$$\Delta V_T = -\frac{x}{d_{ox}}\frac{Q_{ox}}{C_{ox}} \tag{3-9}$$

There are two main reasons why radiation generated electrons usually do not play a significant role in the irradiation response of MOSFETs. First, the electrons are highly mobile in comparison to the holes for all electric fields and temperatures, and therefore are swept out of the oxide very quickly (34). Second, due to the relatively low concentration and small capture cross section of electron traps, the amount of electron trapping in SiO_2 is up to six orders of magnitude less than for hole trapping (34). Therefore, in SiO_2, the hole trapping will dominate any effects associated with electron trapping. However, in nitrided oxides and reoxidized nitrided oxides, electron trapping can have a significant effect.

Radiation-generated holes at low temperatures are immobilized near their point of origin in the oxide bulk. The holes are not trapped at defect sites in the oxide, as is the case for long-term hole trapping observed at room temperature, but are trapped in polaronic states that have a very low effective mobility at low temperatures. It will be pointed out that the term effective mobility is both time and oxide thickness dependent. The holes stay trapped, causing negative V_T shifts, for minutes to hours. These polaronic hole traps can be emptied by raising the oxide temperature to a level at which the polarons become reasonably mobile or by applying a large electric field.

3.6.3 Interface States. Ionizing radiation can generate additional interface states (or traps) which can lead to shifts in the threshold voltage. The radiation-generated interface traps are shown as the fourth process in Figure 3-5. Interface traps are electronic energy levels located at the Si-oxide interface that can capture or emit electrons (or holes). The electronic levels are due to the lattice mismatch at the interface, disconnected chemical bonds, or impurities (14; 27). The occupancy of the interface traps is determined by Fermi statistics. The net charge of these interface traps is a function of the position of the Fermi level in the bandgap.

The two types of interface traps are donor traps and acceptor traps. A donor trap is an interface trap that is neutral when filled with an electron and positively charged when empty. The donor trap can be looked at as being neutral if the Fermi level is above the state and is positively charged if the Fermi level is below the state. An acceptor trap is negatively charged when filled with an electron and neutral when empty. The acceptor

trap is negatively charged if the Fermi level is above the state and is neutral if the Fermi level is below the state. Usually interface traps below the middle of the silicon band gap (midgap) are donor-like and those above are acceptor-like, this point is discussed in more detail later in this section (27; 36).

An example of the energy band diagram for a p-type semiconductor in accumulation is shown in Figure 3-6(a). There is a net positive charge trapped in the donor states. As the gate voltage is increased, the Fermi level corresponds to the intrinsic Fermi level at the surface, this is known as the midgap condition. The energy band diagram for the midgap condition is shown in Figure 3-6(b). For the midgap condition all of the interface states are neutral. Figure 3-6(c) shows the energy band diagram for the inversion condition. There is now a net negative charge in the acceptor states. Thus, the charge of the interface state is a function of the applied gate voltage. In other words the charge depends on the energy band bending. The presence of interface states causes the threshold voltage to shift by some amount and direction depending on the gate voltage being applied.

As with the trapped oxide charge defect center, ESR spectroscopy has been used in order to identify the interface trap defect center. Based on ESR spectroscopy studies, the microscopic structure of interface trap defect center has been determined to be the P_b center (16; 17). The P_b center is an interface trap defect composed of a trivalent silicon bonded to three silicon atoms at the Si-oxide interface. The P_b center is similar to the E' center except that the P_b center is back bonded by three silicon atoms instead of three

oxygens.

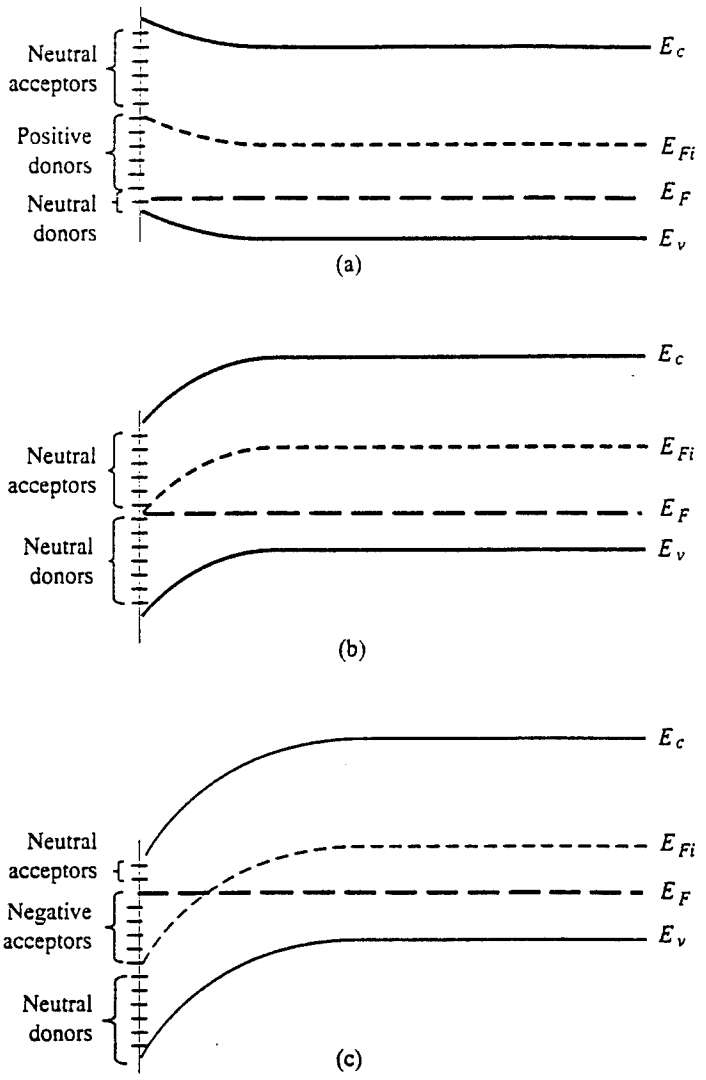

Figure 3-6. Energy-band diagram for a p-type semiconductor showing the trapped charge in the interface states when biased (a) in accumulation, (b) at midgap, (c) at inversion (27: 521).

The distribution of P_b centers is peaked at midgap and decreases toward both the conduction band and valence band edges. In the lower part of the band gap, the P_b center is a donor-like, positively charged interface state defect. As the Fermi level moves toward midgap, the positively charged P_b centers accept an electron and become paramagnetic and neutral. As the Fermi level moves from midgap towards the conduction band edge, the P_b center picks up another electron, becoming negatively charged and again diamagnetic. In the upper part of the band gap the P_b center is therefore an acceptor-like negatively charged interface state defect. The P_b center is paramagnetic only when it has an unpaired spin (one electron). Therefore, interface traps below the middle of the silicon band gap are donor-like and those above midgap are acceptor-like.

For an n-channel device the interface traps are predominately acceptor traps since for a positive bias the energy bands will bend down, and the Fermi level will be above several acceptor states. These negatively charged acceptor traps will produce a positive shift in threshold voltage. In the n-channel device the negative charge from the interface traps compensates the positive charge from trapped holes. In a p-channel device the interface traps are predominately donor states. The positively charged donor states will cause a negative shift in the threshold voltage. The positively charged interface traps of a p-channel device add to the positive charge from the trapped holes producing a larger net threshold voltage shift.

Presently there is uncertainty in exactly how interface traps buildup at the Si-oxide interface. Several models have been proposed over the years with the two most accepted being a hydrogen transport model and a trapped hole recombination model. One common feature among almost all of the models is that they begin with the transport and /or trapping of radiation-generated holes. The hydrogen transport model is described next followed by a description of the trapped hole recombination model.

A two-stage hydrogen model was developed where in the first stage radiation-generated holes react with some hydrogen containing species in the oxide causing the release of hydrogen ions (23; 36-38). This first stage determines the saturated value of interface traps and occurs during the period of charge generation and hole transport through the oxide. Then, in the second stage, the liberated H^+ ions undergo a dispersive hopping transport, similar to the hole transport previously described, which controls the rate of interface formation. The H^+ ions that reach the interface can react to form interface traps. It is almost certain that H^+ is the ion causing interface buildup, but the nature of the hydrogen containing species in the oxide, the chemical reaction which produces the H^+, and the resulting spatial distribution of the H^+ ions through the oxide, are all uncertain.

Once the H^+ ions have reached the interface they can react with H-Si trap precursors and electrons from the substrate to produce silicon dangling bonds (interface traps) and neutral H_2. This reaction is given by (38)

$$H^+ + e^- + H - Si \equiv Si \rightarrow H_2 + \bullet Si \equiv Si \qquad (3\text{-}10)$$

where $H - Si \equiv Si$ is a silicon atom bonded to a hydrogen atom and back bonded to three silicon atoms, and $\bullet Si \equiv Si$ represents a silicon atom with a dangling bond back bonded to three silicon atoms.

This two stage hydrogen transport model is believed to be the main process for radiation-induced interface state buildup, where the first stage determines the saturated value of the traps and the hopping transport of H^+ ions (second stage) determines the time scale of interface state buildup. In the previously described hydrogen transport model H^+ ions were released as holes transport through the oxide. In this model, an increase in electric field increases the energy a hole imparts to the oxide lattice as it transports through the oxide, causing more H^+ to be released. This would produce more interface traps with increasing field. This increase is true up to a point and then the interface trap buildup follows an approximate $E^{-1/2}$ field dependence (24; 35).

A model to account for this field dependence is a hole-trapping/hydrogen transport $(HT)^2$ model (35). In this model the number of holes trapped determines the total number of interface traps (i.e. the saturated value) that buildup at a given electric field. Because the number of holes trapped scales as $E^{-1/2}$, the saturated value of interface trap buildup will follow the same field dependence. This model involves, for positive gate bias, hole trapping near the Si-oxide interface, and the release of H^+ ions near the interface. The H^+ ions transport to the interface and react according to Equation

(3-10) to form interface traps. In the $(HT)^2$ model, H^+ transport is the rate limiting process.

The trapped hole recombination models suggest that radiation-generated holes get trapped near the Si-oxide interface and are converted into interface traps by electron injection. It is proposed that electrons tunnel from the substrate to annihilate the trapped holes producing a structural change at the interface and resulting in a weak or dangling silicon bond that acts as the interface trap (36; 39). In this model the conversion of trapped holes to interface traps is the rate limiting step. The temperature effects of interface state buildup will be covered next.

The formation of interface traps depends on the transport and/or trapping of holes as well as the transport of H^+ through the oxide. At low temperatures the holes and H^+ ions will be immobile due to the nature of their transport. Therefore, at low temperatures the buildup of interface states is greatly restricted. As the temperature is raised, some of the holes and H^+ ions will become thermally detrapped. It is only after this detrapping occurs that any significant interface traps will buildup.

Almost all of the interface trap models begin with the transport and/or trapping of the radiation-generated holes. These holes either interact in the bulk of the oxide or in a narrow interfacial region. The release and transport of hydrogen ions is involved in most of the interface trap buildup. Whether H^+ ions are released in the bulk oxide or in the interfacial region is uncertain at this time.

3.7 Bias Effects

Throughout this document several bias (electric field) effects have been discussed. However, two additional concepts involving applied gate bias are presented here. The threshold voltage shift is a function of the amount of trapped charge and is therefore a function of the applied gate voltage. For small values of gate voltage (low electric field), some radiation generated electrons and holes recombine in the oxide. At low temperatures, electrons escaping recombination are swept out while the remaining holes are immobile. As the field is increased, a larger fraction of electrons escape recombination leaving an increasingly larger amount of positive charge. Thus, the threshold voltage shift at a given dose increases with increasing applied voltage up to a point (about 2 MV/cm) (40; 41). At still higher fields, the holes become mobile which results in less positive charge in the oxide and thus a decrease in threshold voltage shift with increasing bias is observed (40; 41).

A positive biased gate results in a larger negative shift in threshold voltage compared to a negative biased gate. For a positive biased gate the radiation generated holes move toward the Si-oxide interface, and become trapped near the interface. For a negative biased gate the radiation generated holes move toward the gate, and become trapped near the gate. Holes trapped near the Si-oxide interface have a much larger effect on the threshold voltage shift than the holes trapped near the gate.

3.8 Oxide Processes

Until recently most of the work dealing with oxides has been concerned with thermal SiO_2 since this has been the most commonly used technology in MOSFETs. However, alternatives to thermal oxides include nitrided oxides (NO) and reoxidized nitrided oxides (RNO), which have several advantages over thermal oxides. These advantages include greater radiation hardness, higher dielectric strength, improved resistance against the diffusion of dopants or contaminants, and improved resistance under electrical stress (8; 42; 43). This thesis is concerned with the total radiation dose effects to thermal oxides compared to RNO.

Thermal oxides are produced by the reaction of a silicon surface with an oxidizing agent such as dry oxygen or steam. Typically, NO devices are formed by exposing an oxidized silicon wafer to an ammonia (NH_3) ambient (44). The nitridation of a thermal oxide results in the addition of nitrogen throughout the oxide with peaks in the nitrogen concentration at the Si-oxide interface and oxide surface (oxide-gate interface) (6). Figure 3-7 shows the depth profile of nitrogen concentration in thermal oxide, nitrided oxide, and reoxidized nitrided oxide based on Auger Electron Spectroscopy (AES) measurements. The RNO are formed by reoxidizing the nitrided oxide in a high temperature oxygen environment (44). Reoxidizing the nitrided oxide reduces the surface nitrogen peak and the nitrogen content in the bulk, and leaves a somewhat reduced peak at the Si-oxide interface (6). An important point to mention is that the oxide growth process is critical to the total radiation dose susceptibility of NO

and RNO. Specifically, the time and temperature of the nitridation and reoxidization play a crucial role in total radiation dose hardness of these oxides.

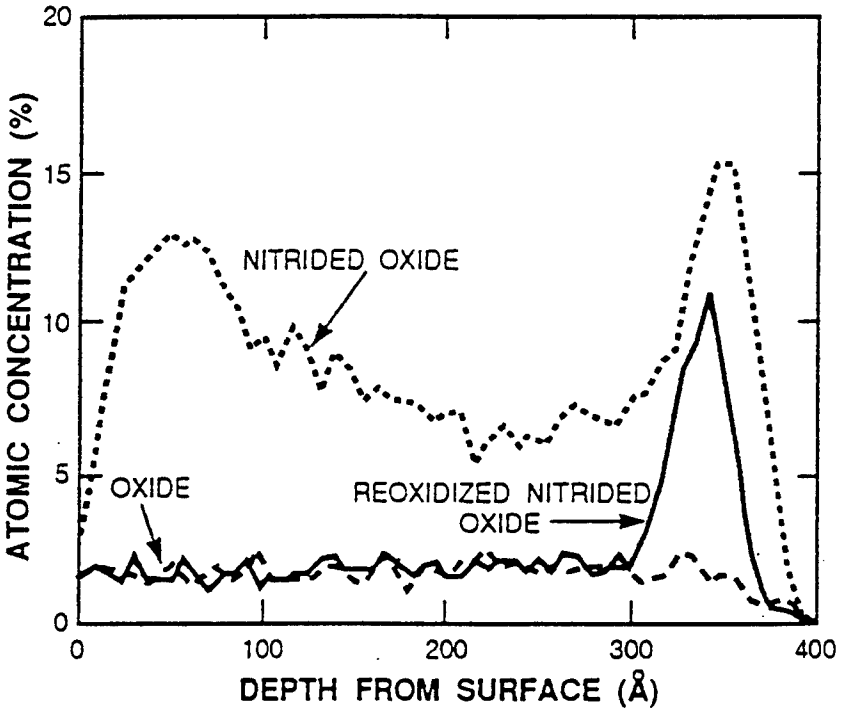

Figure 3-7. Depth profile of nitrogen concentration in the thermal oxide, nitrided oxide, and reoxidized nitrided oxide based on Auger Electron Spectroscopy measurements (6).

Hole transport in RNO is qualitatively similar to transport in thermal oxides, but quantitatively different in thermal and field activation dependencies (15). As with hole

transport in thermal oxides, hole transport in RNO is dispersive in time and the time scale is strongly temperature and field dependent. The dispersion parameter, α, in the transport process for both types of oxides is the same. However, there is a difference in the temperature and electric field dependencies of hole transport for the two types of oxides. Hole transport in RNO is significantly retarded at low fields and at temperatures near room temperature compared to the transport in thermal oxides. However, at 77 K and at moderate fields (2 to 5 MV/cm), the hole transport in RNO is accelerated when compared with thermal oxides (15). RNO devices have been observed to have a lower hole trap energy compared to thermal oxides, and therefore more response to field-activated hole transport (3).

ESR measurements have been used to study the microscopic nature of point defects in NO and RNO. From these measurements it is determined that nitridation reduces the number of E' centers generated by irradiation while introducing a large number of radiation-induced bridging nitrogen centers (19). Bridging nitrogen centers are a nitrogen atom bonded to two Si atoms, leaving two nitrogen bonds which are available to trap charge. It is believed that these bridging nitrogen defects play an important role in electron trapping in NO and RNO. Reoxidation results in a small increase of radiation-generated E' centers and a large decrease in the radiation-induced bridging nitrogen centers (19). The E' centers introduced by reoxidation are electrically neutral when paramagnetic and therefore very different from those in thermal oxides.

The E' centers in RNO, unlike those in thermal oxides, are not the dominant hole traps (19). E' centers in RNO are single dangling bonds and not vacancies as in thermal oxides.

Recall that E' centers in thermal oxides are holes trapped in oxygen vacancies and are heavily concentrated near the Si-oxide interface. In a nitrided oxide the E' centers are reduced by nitridation and uniformly distributed throughout the oxide. Nitridation also produces bridging nitrogen centers which are heavily concentrated near the gate. Reoxidation causes a small increase in the number of E' centers, which are distributed throughout the RNO with a peak in concentration near the gate. In addition, reoxidation reduces the number of bridging nitrogen centers, especially near the gate, producing a uniform concentration throughout.

Nitridation results in a large number of electron traps (bridging nitrogen centers) concentrated near the gate and near the Si-oxide interface. The negative trapped charge will produce a positive shift in the threshold voltage. In addition, nitridation reduces the number of hole traps (E' centers) especially at the Si-oxide interface. Reoxidation reduces the number of electron traps while increasing the number of hole traps, especially near the gate. However, the concentration of electron traps is significantly larger and the concentration of hole traps is substantially reduced in RNO compared to thermal oxides.

Very little if any radiation-generated interface states are present in RNO (5-7; 45). It was proposed that hydrogen ions released in the bulk of the oxide or near the Si-oxide interface (which are responsible for most of the interface trap buildup in thermal oxides) can not penetrate the high nitrogen concentration layer near the Si-oxide interface and create any interface traps (5). The presence of the nitrogen-rich layer near the Si-oxide interface in RNO blocks the transport of hydrogen ions to the interface (5). Therefore, RNO will show very little buildup of interface states and no delayed buildup. It is uncertain whether the nitrogen-rich layer near the interface provides a physical barrier or whether the hydrogen gets chemically bonded in this layer. From studies of thermal oxides it is suspected that low temperature operation would only enhance the lack of radiation-generated interface buildup in RNO.

IV. Experimental

Total ionizing dose testing of the transistors was performed at the Naval Weapons Support Center (NWSC), Crane, Indiana. The transistors were irradiated at 77 K in a Shepherd ^{60}Co test cell at a dose rate of approximately 107 rads(Si)/sec. The test devices were fully immersed in liquid nitrogen throughout the cold temperature testing. A Keithley transistor parameter measurement system was used for the measurement and collection of data.

This chapter is divided into two sections, an equipment section and a procedure section. The first section describes the MOSFET devices and the major equipment which was used in this research. The next section discusses the procedure and methods that were used to perform the experimental work.

4.1 Equipment

This section covers the equipment that was used in performing the experimental work of this project. Included within this section are descriptions of the test devices, Shepherd ^{60}Co test cell, cryogenic dewar, Keithley transistor parameter system, and thermoluminescent dosimeters (TLDs).

4.1.1 Test Devices. The transistors that were tested in this project were supplied by the NWSC. The transistors, which were manufactured using the TRW process, consisted of both n-channel and p-channel variants. The gate oxide thickness, d_{ox}, of all the transistors was 150 Å. For every device, both the length and width of the gate was 50 μm. The substrate doping concentration of the n-channel devices was 4×10^{16} cm^{-3} and 1×10^{16} cm^{-3} for the p-channel devices. Three different oxide processes were explored including a thermal oxide (TO) process, and two different reoxidized nitrided oxide (RNO) processes. The oxide permittivity for the RNO devices was approximately 3.63×10^{-13} F/cm. The first RNO process, referred to as RNO1, consisted of a rapid thermal nitridation (RTN) step which lasted for 60 seconds at a temperature of 1050 °C in an NH_3 ambient environment. The second RNO process, RNO2, also used a RTN, but the RTN was done for 60 seconds at a temperature of 1150 °C in an NH_3 ambient environment. Both of the RNO processes went through a rapid thermal reoxidation step for 60 seconds at a temperature of 1050 °C in an oxygen ambient. Six different test chips, each one consisting of 10 transistors, were used. The six different test chips are:

1. N-channel Thermal Oxides (NTO).
2. N-channel RNO1 (NRNO1).
3. N-channel RNO2 (NRNO2).
4. P-channel Thermal Oxides (PTO).
5. P-channel RNO1 (PRNO1).

6. P-channel RNO2 (PRNO2).

The test chips were mounted onto 24 pin sockets which were mounted to a circuit board.

4.1.2 Shepherd Test Cell. The transistors were irradiated using a Shepherd 484 ^{60}Co test cell located at the NWSC, at a dose rate of approximately 107 rads(Si)/sec. The determination of this dose rate will be discussed in the second section. The Shepherd 484 is a completely self-contained irradiation facility designed to irradiate electronic components. This system consists of a model 81-22 pneumatically operated irradiator, containing three ^{60}Co source rods, mounted to a shielded irradiation tunnel, which has two access doors. A diagram of the test cell is shown in Figure 4-1.

The shielded irradiation tunnel is permanently mounted to the model 81-22 irradiator. The irradiation tunnel is fully accessible through two completely shielded doors, which are fully interlocked. The primary door provides access to the full tunnel, while the side door provides tunnel access approximately 12 inches from the source rods. An access port for running circuit cables is built into the top of the irradiation tunnel. Inside the irradiation tunnel is a moveable mounting cart for the positioning of the transistors.

In order to gain access to the irradiation tunnel, the source rods must be in the shielded (OFF) position and a door interlock button must be pressed while releasing the door latch. The experiment mounting cart can then be set up and positioned. After the

experiment is set up the access doors must be fully shut in order to position the source rods in the irradiate (ON) position. The Shepherd 484 has several safety features

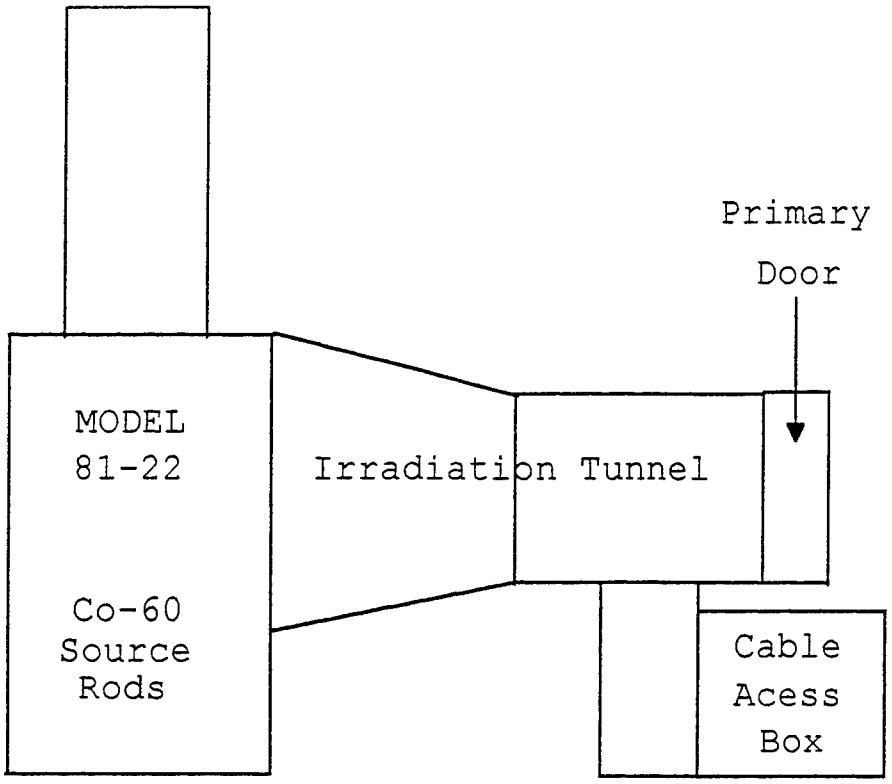

Figure 4-1. Diagram of the Shepherd 484 ^{60}Co irradiator.

including shut-off mechanisms in the event of electrical failure, interlock systems, and external trip monitors.

4.1.3 Cryogenic Dewar. A simple stainless steel cryogenic dewar, filled with liquid nitrogen (LN), was used to keep the test devices at 77 K. The circuit board holding the test devices was immersed in the LN throughout the cold temperature testing. The circuit board and cables fit tightly into the dewar so that there was no motion of the test devices or cables, and therefore no change in the dose rate at the devices.

4.1.4 Keithley Transistor Parameter System. The Keithley transistor parameter system is an integrated system consisting of a Keithley 707 switching matrix, four Keithley 236 Source Measure Units (SMUs), and a control computer. This system was used for the measurement, collection, and storage of all data taken during the testing. By using this system, the radiation testing, which is described in detail in the next section, was fully automated. A block diagram showing the configuration of the experiment is shown in Figure 4-2.

The test chips are mounted onto a circuit board which gets immersed into the dewar filled with LN. Tri-axial cable connects the test chips to the Keithley transistor parameter system. Using this testing setup, up to 16 transistors could be tested at the same time. The SMUs can source voltage from ± 100 μV to ± 110 V, and measure current from ± 10 fA to ± 1 A, or can source current and measure voltage. For this experiment the SMUs were used to source voltage and measure current. Compliance limits can be used to protect external circuitry or test devices. Setting an appropriate current compliance can prevent excessive power dissipation in a device. The computer

controls the parameter system as well as the positioning of the source rods during testing.

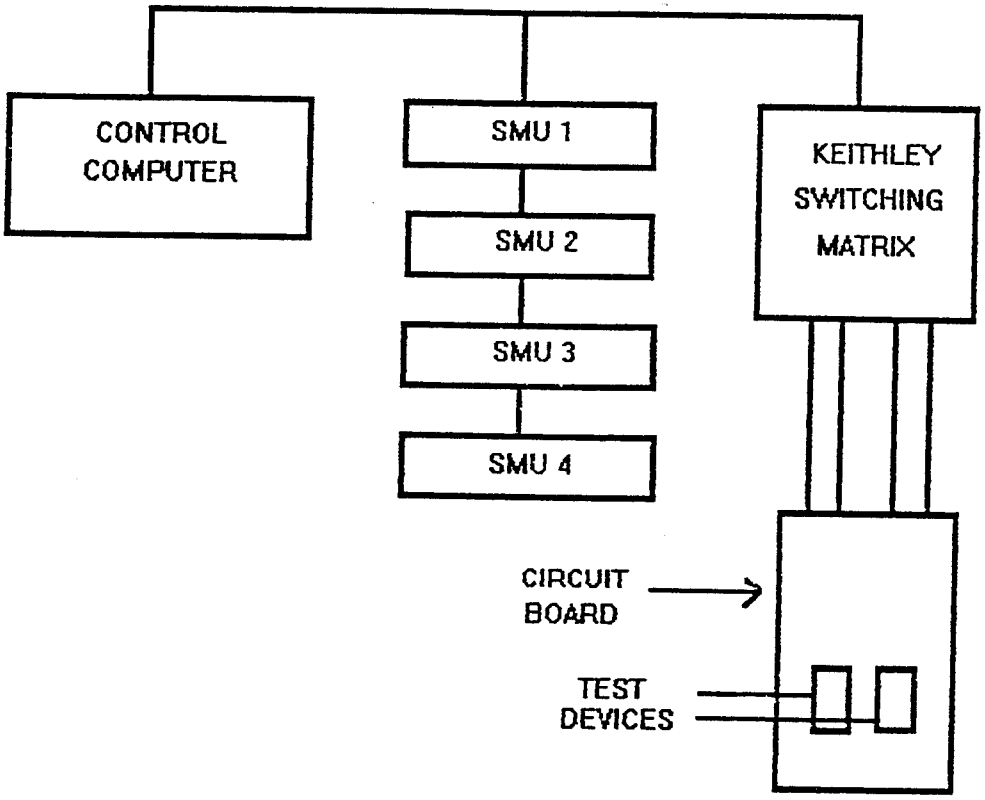

Figure 4-2. Block diagram showing the configuration of the experiment.

4.1.5 Thermoluminescent Dosimeters. Manganese activated Calcium Flouride, CaF_2:Mn, thermoluminescent dosimeters (TLDs) were used to determine the dose rate of

the Shepherd ^{60}Co irradiator. The dosimetry procedure is described in the next section. Thermoluminescent materials consist of a crystalline insulator material with added dopants which introduce trapping centers within the band gap. Ionizing radiation creates electrons and holes which become captured in the traps, and the density of filled traps is proportional to the dose absorbed by the material. The trapped carriers are released by heating the material so the dose can be measured. As the temperature of the material is raised the trapped electrons (or holes) can gain enough thermal energy so that they are liberated from the traps. The liberated electrons (or holes) can then recombine with a trapped hole (or electron), emitting a photon in the visible region which is the basis of the TLD signal. The integrated light output is proportional to the density of filled traps, and therefore to the absorbed dose in the TLD material. To determine rad(Si), the absorbed dose in the TLD material is multiplied by the ratio of the density of TLD material to the density of silicon.

4.2 Experimental Procedures

This section discusses the testing and measurement of the test devices. Included in this section is a description of the dosimetry work that was done to determine the dose rate of the Shepherd ^{60}Co irradiator and a discussion on the total dose testing.

4.2.1 Dosimetry.

In order to determine the dose rate of the Shepherd ^{60}Co irradiator, a dosimetry study using CaF_2:Mn TLDs was performed. Four CaF_2:Mn TLDs were mounted in aluminum foil to make a TLD package. These TLD packages (i.e. eight TLDs) were immersed into the LN filled dewar and exposed simultaneously for two minutes. during irradiation testing. The results of the TLD irradiation are presented in Table 4-1. An average dose rate of 113.0 rads(Si)/sec was obtained from the data in Table 4-1. An additional TLD package, four TLDs, was exposed for 123.6 seconds in NSWC's Gammacell 220, a NIST calibrated ^{60}Co source, to use as a standard for calibrating the TLD results. The results of the TLD irradiation in the Gammacell 220 are presented in Table 4-2. An average dose rate of 52.4 rad(Si)/sec was determined from the data in Table 4-2. Based on a December 1991 NIST calibration, and allowing for decay, it was determined that the actual dose rate in the Gammacell 220 should be 49.77 rad(Si)/sec. Therefore, the calibration TLD package showed that the actual dose rate was 0.95 times the measured values in Table 4-1. Therefore, the actual dose rate of the Shepherd ^{60}Co irradiator is 107.4 rads(Si)/sec and was assumed to remain constant throughout all of the testing due to the 5.3 year half life of ^{60}Co.

Table 4-1. Results of the TLD irradiation in the Shepherd irradiator.

Package 1 TLD #	Dose (rads Si)	Package 2 TLD #	Dose (rads Si)
1	1.614 E +04	1	1.312 E+04
2	1.294 E +04	2	1.326 E +04
3	1.503 E +04	3	1.214 E+04
4	1.452 E+04	4	1.135 E+04

Table 4-2. Results of the TLD irradiation in the Gammacell 220.

Package 1 TLD #	Dose (rads Si)
1	6.654 E+03
2	6.850E+03
3	6.571E+03
4	5.838E+03

4.2.2 Total Dose Testing. The testing of the transistors was spread over three days with 16 transistors being tested each day. Eight n-channel thermal oxide (NTO), and eight

n-channel RNO1 (NRNO1) transistors were tested on the first day. On the second test day the eight p-channel thermal oxide (PTO) and the eight p-channel RNO1 (PRNO1) transistors were tested. On the third test day the eight n-channel RNO2 (NRNO2) and the eight p-channel RNO2 (PRNO2) transistors were tested.

Throughout all of the testing the source and substrate terminals were grounded in order to prevent charge buildup within the device. All of the tests were conducted in a similar manner. First, before being irradiated, the test devices were mounted onto the circuit board and placed into the empty dewar. Pre-radiation measurements of the devices were then made at room temperature, this will be referred to as pre-rad warm testing. A suite of measurements were conducted, and are described as follows. First, for n-channel devices, the drain voltage is set to 0.1 V on the first transistor and the gate voltage, V_G, on this transistor is swept from -2.0 V to +3.0 V in 0.05 V increments. The drain current, I_D, the substrate current, I_{sub}, and the source current, I_s, are all measured at each value of the gate voltage. Second, the drain voltage is set to 1.0 V on this first transistor and the gate voltage is swept again and current values are measured. After both sweeps of this first transistor are done the next transistor goes through this process, which is repeated until all 16 of the transistors are swept. For p-channel devices the drain biases are -0.1 V and -1.0 V, and the gate voltage is swept from -5.0 V to 0.0 V in 0.05 V increments. While a transistor is being swept, all other transistor gates and drains are left floating, so that there was no external field in the oxide or in the channel. To reiterate

the measurement process, the first day of testing is used as an example, and is presented next.

On the first test day, the pre-rad warm testing started with the first NTO transistor, designated 1NTO. Recall that both the NTO and NRNO1 transistors were tested on this first day. The drain bias was set to 0.1 V on transistor 1NTO and the gate voltage was swept from -2.0 V to +3.0 V in steps of 0.05 V, for a total of 100 data points. All of the currents were measured and recorded for each value of V_G. After this was complete the drain bias was set to 1.0 V, the gate was swept again over the same interval, and the currents were measured at each gate bias. While 1NTO was being measured all the other transistors were left floating. After the measurements were made on 1NTO, the next transistor, 2NTO, went through the same process. This process of sweeping each transistor continued until the last transistor 20NRNO1 was tested.

The drain biases of 0.1 V and 1.0 V were used since these correspond to operation in the linear and saturation regions respectively. From these sweeps the I_D-V_G characteristics of the transistors are obtained for each drain bias. This I_D-V_G data can be used to determine the threshold voltage, trapped oxide and interface charge densities, and transconductance. The analysis of the data is discussed in Chapter 5.

After the pre-rad warm testing was complete the dewar was filled with LN, completely covering the test devices. During all of the radiation testing, the dewar was filled with LN approximately every hour to ensure that the test devices always remained covered completely. After filling the dewar with LN, pre-radiation measurements of the

devices were made at 77 K, this is referred to as the pre-rad cold condition. The suite of measurements at this pre-rad cold condition was made in the same manner as the previously described procedure for pre-rad warm testing.

Once the suite of measurements were completed at pre-rad cold, the source rods of the Shepherd ^{60}Co irradiator were placed in the irradiate position. The devices were exposed to a total dose of 1.0 Mrad(Si) with measurements, similar to those just described, taken at 100 krad(Si), 200 krad(Si), 500 krad(Si), and at 1.0 Mrad(Si). Tables 4-3, 4-4, and 4-5 list the devices tested on the first day, second day, and third day respectively, along with the applied gate bias during irradiation. During the irradiation the drain terminal was grounded, so no channel carrier effects are expected. After the 1.0 Mrad(Si) measurements were made an attempt was made to take post-radiation measurements at room temperature, however several problems were encountered during the post-rad warm measurements. All of the problems that have an effect on the data are discussed next.

During the first day of testing it was discovered after about 3 minutes into the irradiation, which corresponds to about 20 krads(Si), that the test devices (NTO and NRNO1) were not biased, rather they were all grounded. This was corrected immediately and the testing continued. Therefore, the NTO and NRNO1 devices were biased for approximately 3 minutes less than the devices tested on other days. There was also a problem on the final test day which resulted in the loss of all data for two of the PRNO2 devices, so that only six of these test devices were used. The problem was with the cable connecting transistors 16PRNO2 and 17PRNO2.

Table 4-3. Test devices and their bias during irradiation on the first test day.

N-channel Thermal Oxide	Applied Gate Voltage (V)	N-channel RNO1	Applied Gate Voltage (V)
1NTO	-1	11NRNO1	-1
2NTO	-3	12NRNO1	-3
3NTO	-5	13NRNO1	-5
4NTO	5	14NRNO1	5
7NTO	1.25	17NRNO1	1.25
8NTO	2.5	18NRNO1	2.5
9NTO	3.75	19NRNO1	3.75
10NTO	0	20NRNO1	0

The post-rad warm measurements were made on the NTO and NRNO1 devices the next morning. There is no way of determining the exact amount of time in which these devices had to anneal at room temperature since they were left in the LN dewar after the irradiation. This meant that after irradiation the LN would boil off until the devices were no longer covered by the LN. The devices would then heat up to room temperature and anneal until the next morning at which time the post-rad testing was done. This same procedure was not done for the devices tested on the other days, rather a heat gun was used to heat the devices immediately after the total dose test. Furthermore, the exact temperature was never determined for any of the devices tested throughout the entire project. Therefore, there is no way to compare any of the post-rad warm data.

However, the post-rad annealing of the devices was not an issue for this project, and is left for future study.

Table 4-4. Test devices and their bias during irradiation on the second test day.

P-channel Thermal Oxide	Applied Gate Voltage (V)	P-channel RNO1	Applied Gate Voltage (V)
3PTO	5	11PRNO1	1
4PTO	-5	12PRNO1	3
5PTO	-1.25	13PRNO1	5
6PTO	-2.5	14PRNO1	-5
7PTO	-3.75	15PRNO1	-1.25
8PTO	0	18PRNO1	-2.5
9PTO	3	19PRNO1	-3.75
10PTO	1	20PRNO1	0

Table 4-5. Test devices and their bias during irradiation on the third test day.

N-channel RNO2	Applied Gate Voltage (V)	P-channel RNO2	Applied Gate Voltage (V)
1NRNO2	. 1	11PRNO2	1
2NRNO2	3	12PRNO2	3
3NRNO2	5	13PRNO2	5
4NRNO2	-5	14PRNO2	-5
5NRNO2	-1.25	15PRNO2	-1.25
6NRNO2	-2.5	16PRNO2	-2.5
7NRNO2	-3.75	17PRNO2	-3.75
8NRNO2	0	18PRNO2	0

In addition to the post-rad annealing of the devices another difference in the radiation testing of the devices occurred. The total time required to complete the suite of measurements varied between test days. A suite of measurements on the first day of testing took approximately 55 minutes, so that each transistor took about 3.4 minutes to be swept. The time that it took to complete a suite of measurements for the remaining four groups of devices was about 27 minutes, or about 1.7 minutes for each transistor to be swept. This reduction in measurement time is attributed to a change in the current compliance from 1 nA on the first test day, to 10 nA on the second test day. Therefore, the NTO and NRNO1 (first day) devices had an extra 84 minutes, exposed to no radiation or applied bias, to anneal at 77 K throughout the total dose testing up to 1.0 Mrad(Si). The question arises as to how much annealing occurred in the NTO and NRNO1 devices during this extra 84 minutes. Since the devices are at 77 K with no applied bias, where the holes are relatively immobile, it is probably safe to assume that very little annealing took place.

V. Results and Discussion

The results of the experimental testing are presented, analyzed, and discussed in this chapter. Unless otherwise noted, this chapter assumes that the experimental data collected throughout this research was accurate and precise within the presented error. This chapter is divided into four sections. Drain current-gate voltage (I_D-V_G) curves were generated from the data and were used to determine the threshold voltage and the transconductance. I_D-V_G curves along with the threshold voltage shifts, ΔV_T, are discussed in the first section. Plots of the transconductance as a function of the applied gate voltage are presented in the second section. The third section contains a discussion on the effects of gate bias during irradiation. The fourth section discusses the radiation hardness of the devices.

5.1 Threshold Voltage Shift

5.1.1 Drain Bias Effects. From the measured data, I_D-V_G curves were generated for every transistor at the two different drain biases. Each of the figures containing the I_D-V_G curves shows a family of curves for each of the different test conditions. Figures 5-1 and 5-2 show the I_D-V_G characteristics of transistor 9NTO for drain biases of 0.1 V and 1.0 V, respectively. The applied gate bias for this transistor during irradiation was

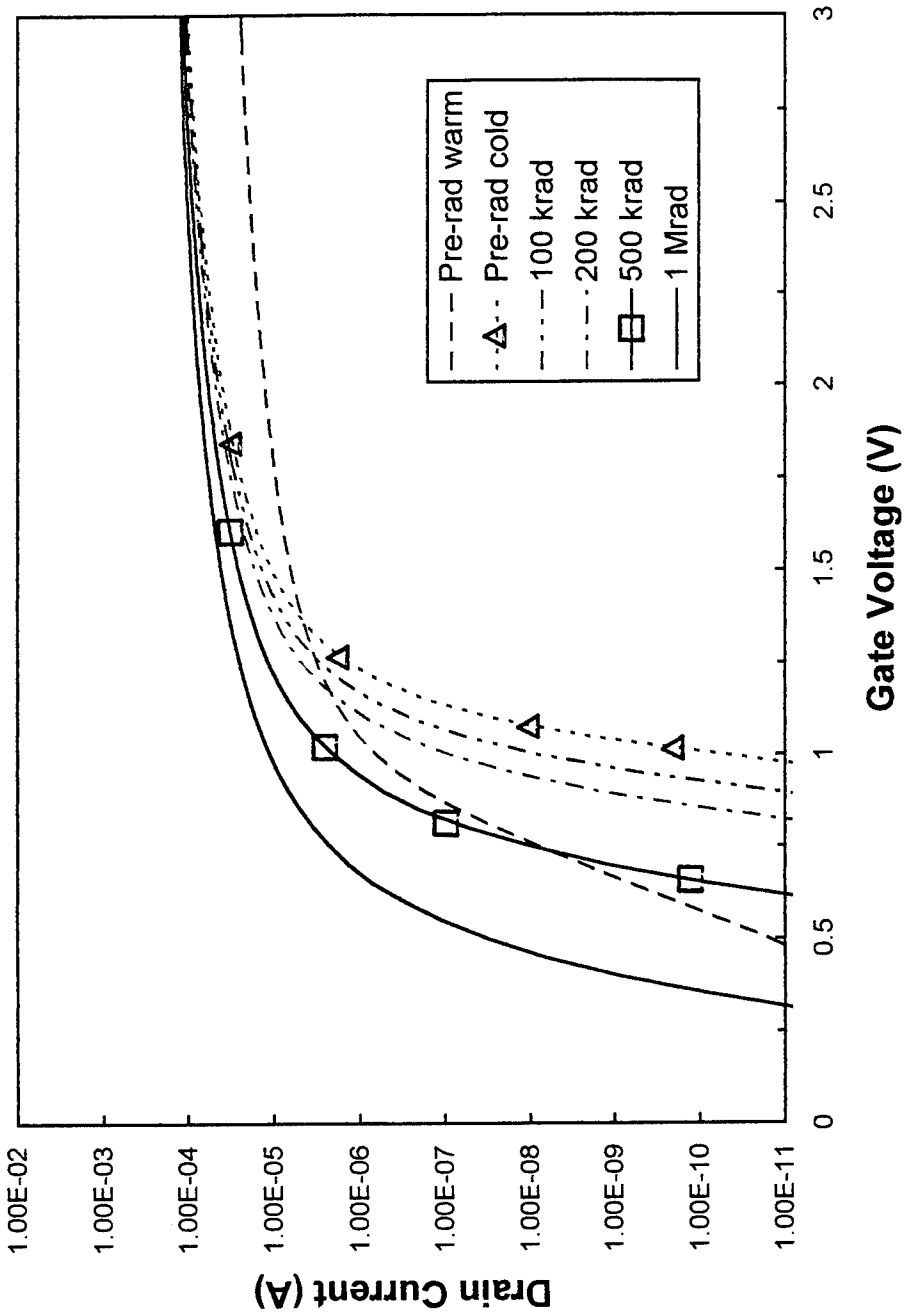

Figure 5-1. I_D-V_G characteristics of transistor 9NTO, V_D = 0.1 V, gate bias during irradiation was +3.75 V.

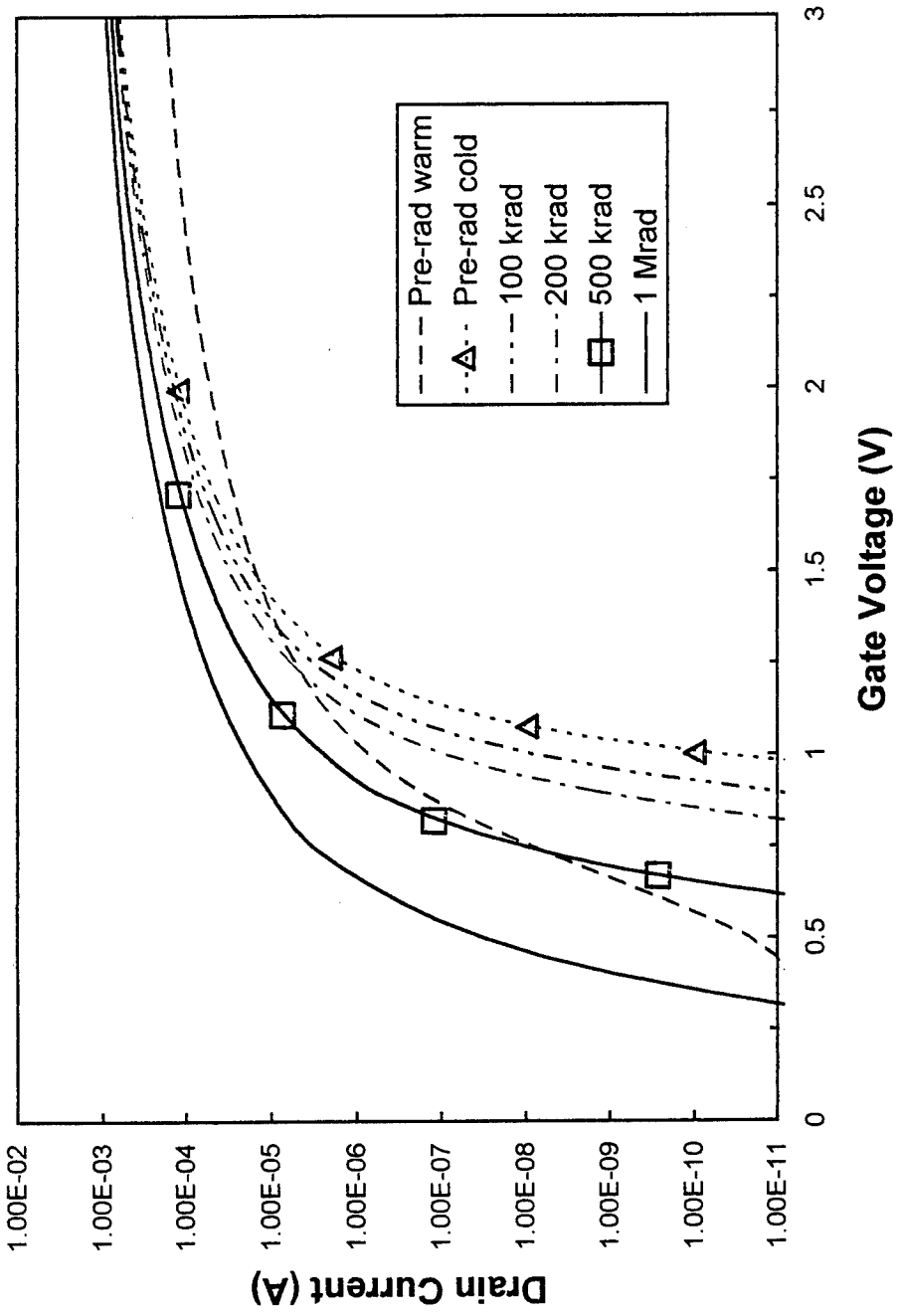

Figure 5-2. I_D-V_G characteristics of transistor 9NTO, V_D = 1.0 V, gate bias during irradiation was +3.75 V.

+3.75 V. It is observed from the two figures that there is no difference in the subthreshold characteristics between the two drain bias cases. However, there is a difference in the characteristics above threshold, in particularly the magnitude for which I_D peaks. These results can be expected since the drain bias should only have an effect on the drain current above the threshold voltage (14: 30). Therefore, in the subthreshold regime the drain current increases with gate voltage but is independent of drain bias. These drain bias characteristics were observed for all but one of the transistors (1NRNO2). For transistor 1NRNO2 there is a slight shift in the I_D-V_G characteristics between the 0.1 V and 1.0 V drain bias conditions. It is uncertain as to exactly why this one device behaved this way, but it may be due to a problem with the data from this device. Since the subthreshold characteristics do not change with drain bias the threshold voltage shift will not change with drain bias. Therefore, for a given test condition, any shift in V_T is the same no matter what drain bias is used. The determination of the threshold voltage from the I_D-V_G data is discussed next.

5.1.2 Threshold Voltage Determination. The threshold voltage was determined as the value of the gate voltage which produces a drain current of 50 nA. This first method for determining V_T was compared to a second method which is determined as follows. The square root of the drain current is plotted versus the gate voltage. The linear part of this curve is extrapolated to zero current, and the voltage intercept is the threshold voltage. After comparing these two methods it was determined that even though both methods

provided very close results, the first method typically provided more conservative estimates of the threshold voltage shift. Since this first method produces larger threshold voltage shifts it was used throughout this project in determining ΔV_T. In addition, a study performed by Cole at NSWC compared these different methods for determining the threshold voltage (47). From this study it was concluded that this first method resulted in larger shifts in V_T compared with the second method which supports the results determined in this project.

5.1.3 N-Channel Transistors. Next, look at the shifts in the I_D-V_G curves of Figure 5-2 for the different test conditions. By cooling the transistor from the pre-rad warm condition to the pre-rad cold condition there is an observed shift of the I_D-V_G curve in the direction of positive gate voltage. This shifting of the I_D-V_G curve will be referred to as simply a positive shift in V_T, since a shift in the I_D-V_G curve corresponds to the same shift in V_T. This positive shift can be attributed to the strong temperature dependence of the threshold voltage. As discussed in Chapter 3, as the temperature of a transistor is lowered the magnitude of the threshold voltage increases.

In addition to the positive V_T shift there is also an increase in the slope of the of the I_D-V_G curve when going from room temperature down to 77 K. This increase in the slope of the I_D-V_G curve is due to an increase in the carrier mobility which results in an increase in the transconductance of the transistor as the temperature is lowered. The shift in V_T and increase in the I_D-V_G slope was observed for every transistor when cooling

from pre-rad warm to pre-rad cold. Therefore, these points will not be mentioned again in this chapter.

As the device in Figure 5-2 is irradiated there is an observed shift of the I_D-V_G curve in the negative gate voltage direction (i.e. negative V_T shift). This negative shift is due to the trapping of radiation-generated holes in the oxide. The radiation-generated electrons will be swept out of the thermal oxide with very few ever becoming trapped. However, the holes are relatively immobile and a large number will become trapped in the thermal oxide. This trapped positive charge (holes) will cause the negative shifts in the threshold voltage. Recall from Chapter 3 that positive trapped charge will cause negative shifts in V_T and negative trapped charge will cause positive shifts in V_T (see section 3.6.2 for a detailed discussion on this). As the total radiation dose is increased up to 1 Mrad(Si) we see further negative shifts in the threshold voltage, so that as the dose increases so does the amount of trapped positive charge in the oxide. Figure 5-3 shows the threshold voltage shift versus total radiation dose for the NTO transistors. The error bars shown in Figure 5-3 are due to the uncertainty in the dose rate of the Shepherd test cell. Every NTO device exhibited negative shifts in V_T as the total dose increased. The effects of the gate bias during irradiation is not discussed now, but rather in the third section of this chapter.

As mentioned in Chapter 3, interface states can cause positive or negative shifts in V_T depending on the gate bias. However, there should be almost complete suppression of any radiation-generated interface states at 77 K. In order to determine if

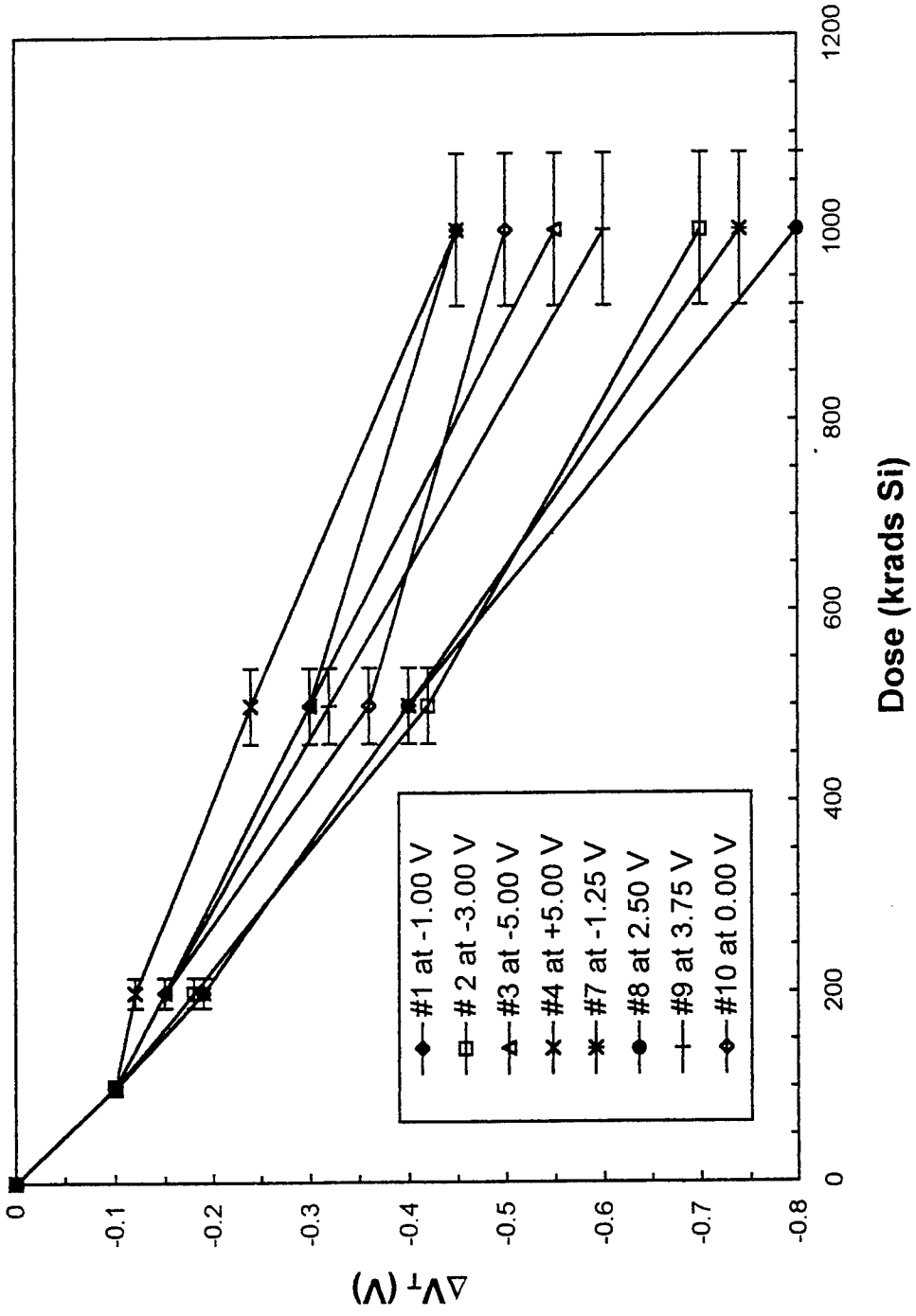

Figure 5-3. Threshold voltage shift versus total dose up to 1 Mrad(Si) for the NTO transistors. The legend lists the transistor number and its gate bias during irradiation.

there were any radiation-generated interface states, the change in subthreshold slope, ΔS (mV/decade), was calculated. From ΔS the change in mean interface trap density, ΔD_{it}, following irradiation was determined by (14; 30)

$$\Delta D_{it} = \frac{C_{ox}\Delta S}{kT\ln(10)} \tag{5-1}$$

In addition, the shift in threshold voltage, ΔV_{Nit}, based on interface charge was calculated using (14; 30; 45)

$$\Delta V_{Nit} = \frac{\Delta S \phi_f}{\left(\frac{kT}{q}\right)\ln(10)} \tag{5-2}$$

It was determined from Equations (5-1) and (5-2) that there was no significant change in interface trap density or in threshold voltage due to a change in interface state charge for any of the irradiated transistors. Therefore, any change in the threshold voltage can be attributed to trapped charge, positive or negative, in the gate oxide.

Figure 5-4 shows the I_D-V_G curves for transistor 12NRNO1, which was biased (gate bias) at -3.0 V during irradiation. From Figure 5-4 it is seen that this NRNO1 device shows similar characteristics to the thermal oxide devices. The threshold voltage

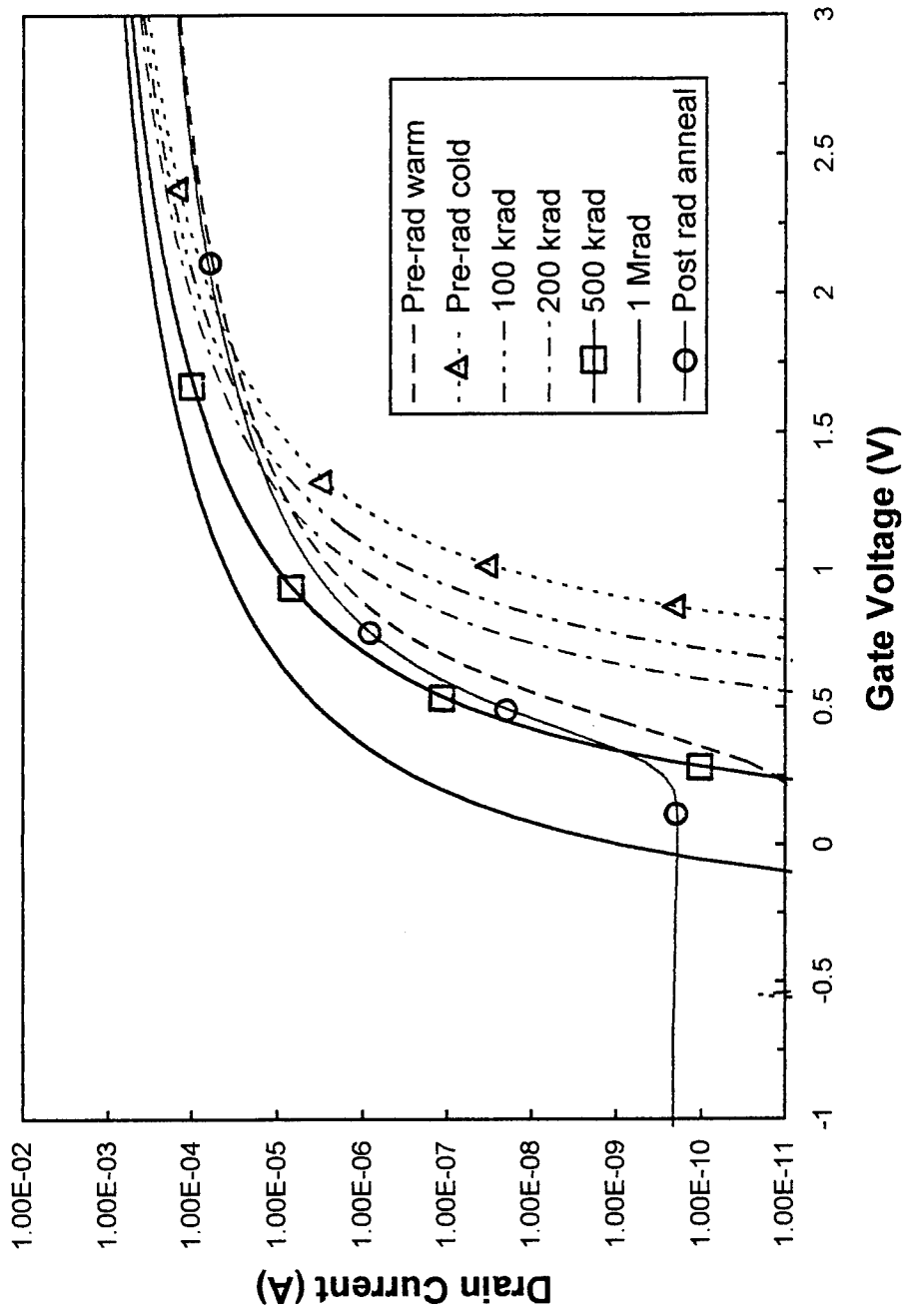

Figure 5-4. I_D-V_G characteristics of transistor 12NRNO1, V_D = 1.0 V, gate bias during irradiation was -3.00 V.

shift versus dose for the NRNO1 transistors is plotted in Figure 5-5. The NRNO1 devices were similar to the NTO devices since both types of devices displayed negative threshold voltage shifts as the total dose increased. There was one exception to this point, transistor 14NRNO1 which was biased at +5.00 V, was observed to have a positive V_T shift after irradiation from 100 to 200 krad(Si). This positive shift was unexpected and it is uncertain as to why only this on transistor behaved in this manner.

One possible explanation is that this positive shift is due to a buildup of trapped negative charge after irradiating from 100 to 200 krad(Si). It is known that RNO devices may contain relatively large concentrations of electron traps, which could explain the buildup of trapped negative charge. However, the question arises as to why the concentration of trapped negative charge would suddenly increase by going from 100 to 200 krad(Si), and then saturate (or decrease) for doses above 200 krad(Si). It does not seem likely that there would be a sudden increase in trapped negative charge when going from 100 to 200 krad(Si). This positive shift may also be due to a sudden annealing of trapped positive charge from 100 to 200 krad(Si). Furthermore, this positive shift could be a combination of both of these processes, an anomaly associated with this one device, or possibly an error with the data point at 100 krad(Si).

Similar to transistor 14NRNO1, all of the NRNO2 transistors showed positive shifts in the threshold voltage. Figure 5-6 shows the I_D-V_G curves for transistor 2NRNO2, biased at +3.0 V. From Figure 5-6 it is observed that there is a positive shift from pre-rad cold to 100 krad(Si) as well as from 100 to 200 krad(Si). From 200 to 500

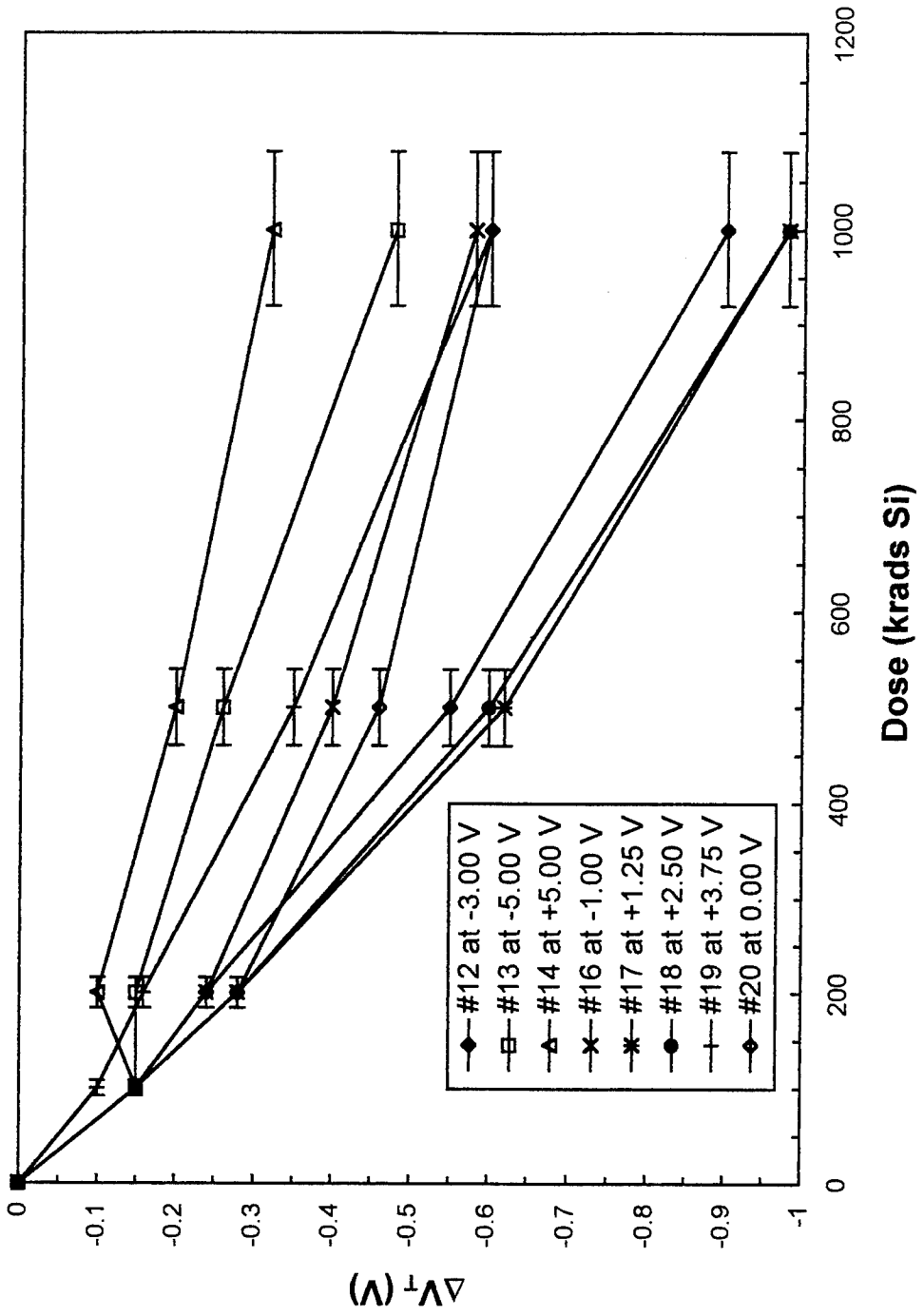

Figure 5-5. Threshold voltage shift versus total dose for the NRNO1 transistors. The legend lists the transistor number and its gate bias during irradiation.

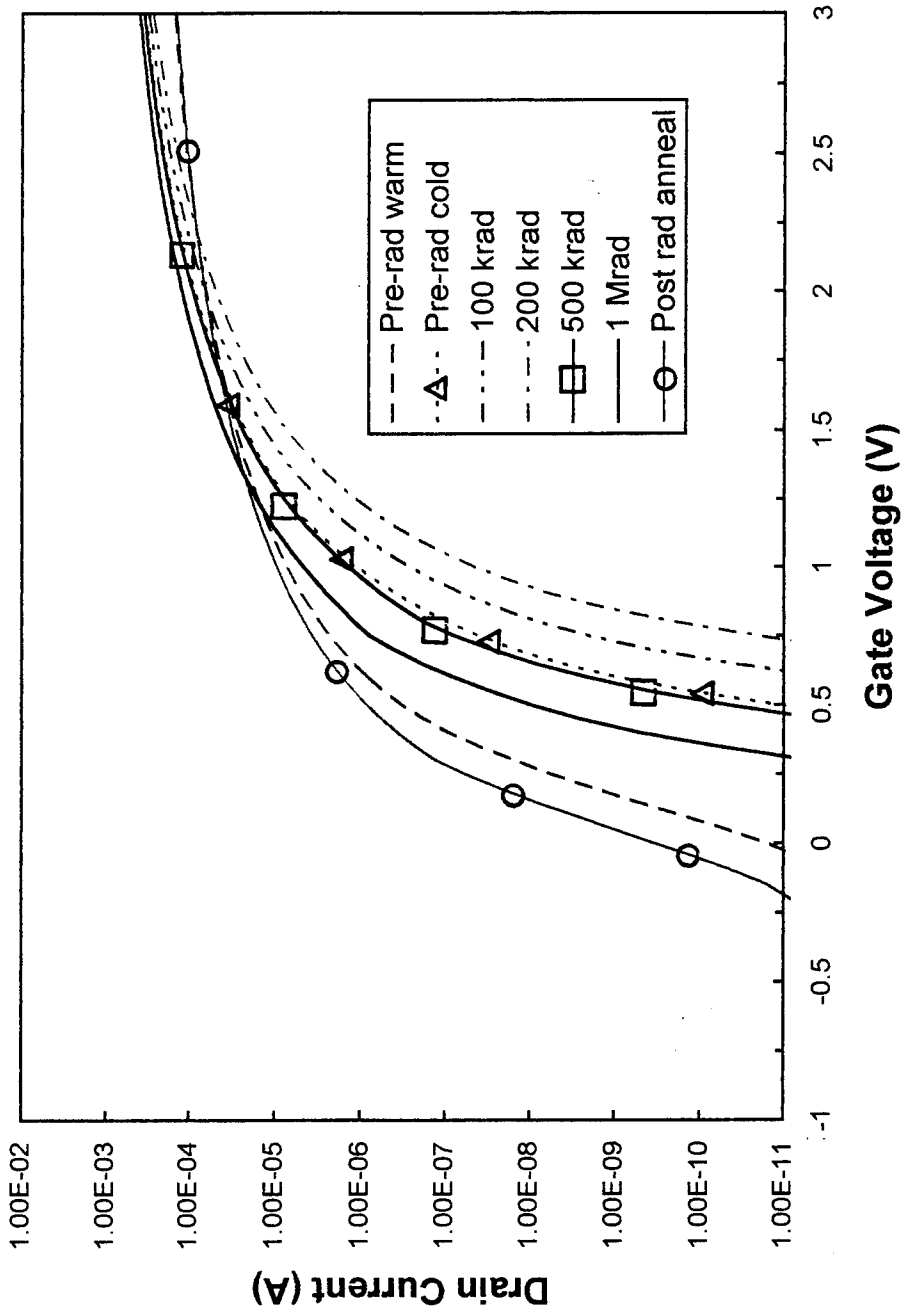

Figure 5-6. I_D-V_G characteristics of transistor 2NRNO2, V_D = 1.0 V, gate bias during irradiation was +3.00 V.

krad(Si) and from 500 krad(Si) to 1 Mrad(Si) the threshold voltage shifts are negative. Figure 5-7 shows the plot of ΔV_T versus total dose for the NRNO2 devices. The positive shifts for all of the NRNO2 transistors up to 200 krad(Si) are seen in this figure. After 200 krad(Si) all of the NRNO2 transistors exhibit negative shifts up to 1 Mrad(Si).

It is proposed that the negative trapped charge (electrons) is dominating the positive trapped charge (holes) in the oxide. First consider a thermal oxide device. When thermal oxides are irradiated the radiation-generated electrons are much more mobile and encounter far fewer traps than the holes do. Therefore, in thermal oxides there is a much greater concentration of trapped positive charge compared to the amount of trapped negative charge in the oxide. This large concentration of positive trapped charge is responsible for the observed negative shifts in V_T for the thermal oxides.

Now let us consider a RNO device. In RNO devices there can be large concentrations of electron traps, as discussed in Chapter 3. In addition to these electron traps, there can also be a reduction in the concentration of hole traps compared to a thermal oxide. It needs to be made clear that even though there can be large concentrations of electron traps and fewer hole traps in RNO devices compared to TO devices, there can still be significantly more hole traps than electron traps in the reoxidized devices. A further point that was mentioned in Chapter 3 is that at 77 K, hole transport in RNO devices can be accelerated in comparison to TO devices. Therefore, the holes in RNO devices may be swept out of the oxide relatively quickly. In thermal oxides there are two main reasons why radiation generated electrons usually do not play a

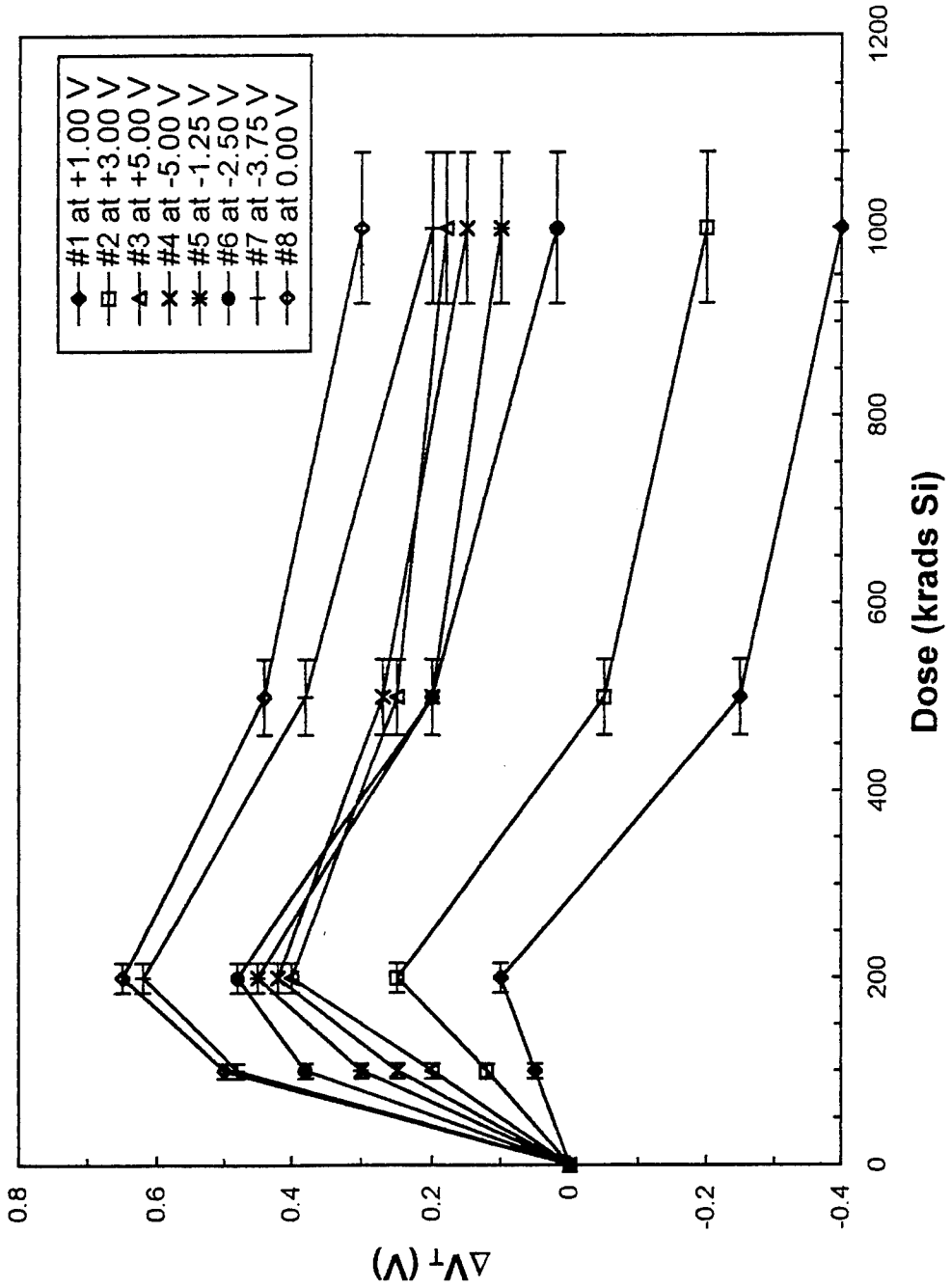

Figure 5-7. Threshold voltage shift versus total dose for the NRNO2 transistors. The legend lists the transistor number and its gate bias during irradiation.

significant role in the irradiation response of MOSFETs. First, the electrons are highly mobile in comparison to holes. This may not be the case at 77 K in RNO devices, where the holes may be significantly mobile. Second, the amount of electron trapping in thermal oxides is several orders of magnitude less than for hole trapping. This also may not be true in RNO devices, where there can be relatively large concentrations of electron traps. When RNO devices are irradiated, a large number of the radiation-generated electrons can become trapped in the oxide. Furthermore, the radiation-generated holes can still become trapped in the RNO devices, but at reduced concentrations compared to thermal devices. Thus, there are two competing processes, electron trapping and hole trapping. Which process will dominate depends on the density, distribution, and charge capture cross sections of the traps.

Based on the observed behavior of the NRNO2 devices it is proposed that there are more electron traps being filled compared to hole traps at dose levels up to 200 krad(Si). We suggest that this is due to a higher capture efficiency of the electron traps (greater charge capture cross section). Therefore, the electron traps will become filled more rapidly than the hole traps. However, it appears that these electron traps saturate around 200 krad(Si). After the electron traps have saturated, the hole traps can continue to become filled and eventually there can be a greater concentration of trapped holes compared to trapped electrons, depending on the concentrations of traps. This is why we see the threshold voltage start to shift in the negative direction above 200 krad(Si).

A further point that needs to be discussed is that in thermal oxides, holes trapped within 2 to 5 nm of the silicon-oxide interface are removed predominantly by a tunnel

annealing process. Electrons from the silicon tunnel to, and recombine with, the trapped holes near the interface (see section 3.6.2). In RNO devices it may be possible to have a faster rate for tunnel annealing compared to thermal oxides. Therefore, a relatively fast tunnel annealing rate may be contributing to the positive threshold voltage shifts that were observed in the RNO2 devices.

The lack of this positive threshold voltage shift in most of the RNO1 devices shows the importance of oxide processing on device response. Based on the data it seems likely that there are far fewer electron traps in the RNO1 devices compared to the RNO2 devices. This could be attributed to a lack of bridging nitrogen centers (electron traps) being produced for nitridation at 1050 ^{o}C versus nitridation at 1150 ^{o}C. In addition, there may be far greater concentrations of hole traps in the RNO1 devices compared to the RNO2 devices. An extremely important point to mention is that the results presented in this thesis are from only a single total dose test. The conclusions that have been discussed so far are based on the validity of this one test. Several more tests, similar to the one performed for the NRNO2 devices, need to be performed to prove the validity of these results.

5.1.4 P-Channel Transistors. The p-channel devices are discussed next. Figure 5-8 shows the I_D-V_G curves for transistor 8PTO, biased (gate bias) at 0.0 V during irradiation. It can be seen from Figure 5-8 that there is only negative threshold voltage shifts as the total dose increases. All of the PTO devices showed these negative shifts for

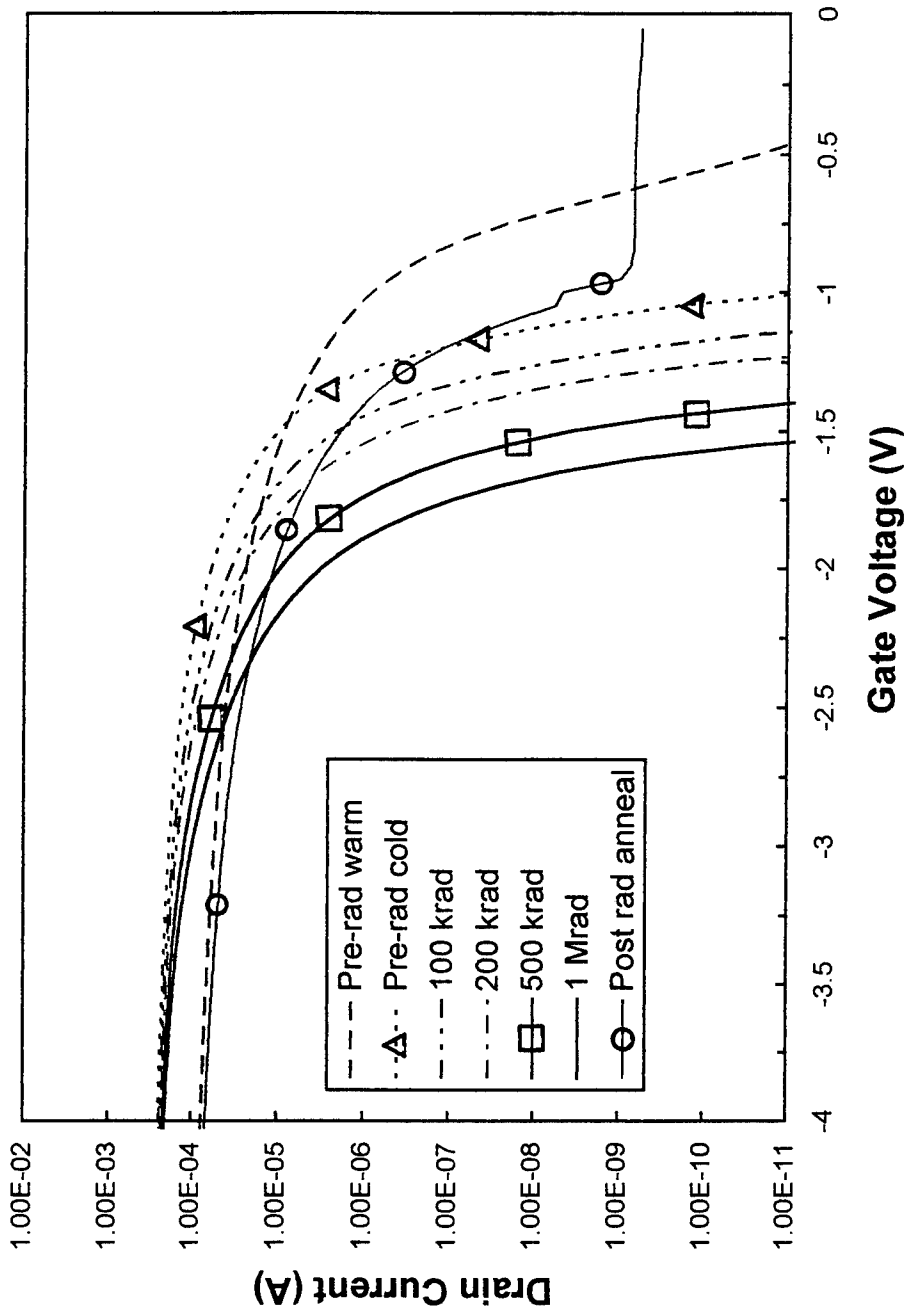

Figure 5-8. I_D-V_G characteristics of transistor 8PTO, V_D = 1.0 V, gate bias during irradiation was 0.00 V.

increasing dose. As with the n-channel transistors, that exhibited these characteristics, these negative shifts are due to the build up of positive trapped charge in the oxide. A plot of the threshold voltage shift versus total dose for the PTO devices is shown in Figure 5-9. The negative V_T shifts observed for every PTO device can be seen clearly in Figure 5-9. The PRNO1 devices were similar to the PTO devices, since all of the PRNO1 transistors experienced negative V_T shifts as the dose increased. Figure 5-10 shows the threshold voltage shift versus total dose for the PRNO1 transistors.

The PRNO2 devices also showed similar characteristics to the other p-channel devices, except for transistor 13PRNO2, biased at +5.0 V. All of the PRNO2 devices exhibited negative V_T shifts with increasing total dose except transistor 13PRNO2. Figure 5-11 shows the I_D-V_G characteristics for device 13PRNO2. From this figure it is observed that from pre-rad cold to 100 krad(Si) that there is the expected negative shift, but from 100 to 200 krad(Si) there is a positive shift in V_T. The threshold voltage shift versus dose is plotted in Figure 5-12 for the PRNO2 devices. The positive shift in 13PRNO2 can easily be seen in this figure. This positive shift between 100 and 200 krad(Si), which is similar to the behavior of transistor 14NRNO1, can be attributed to an increase in trapped negative charge, a decrease in trapped positive charge, a combination of both of these processes, an anomaly associated with this one PRNO2 device, or an error with the data point at 100 krad(Si).

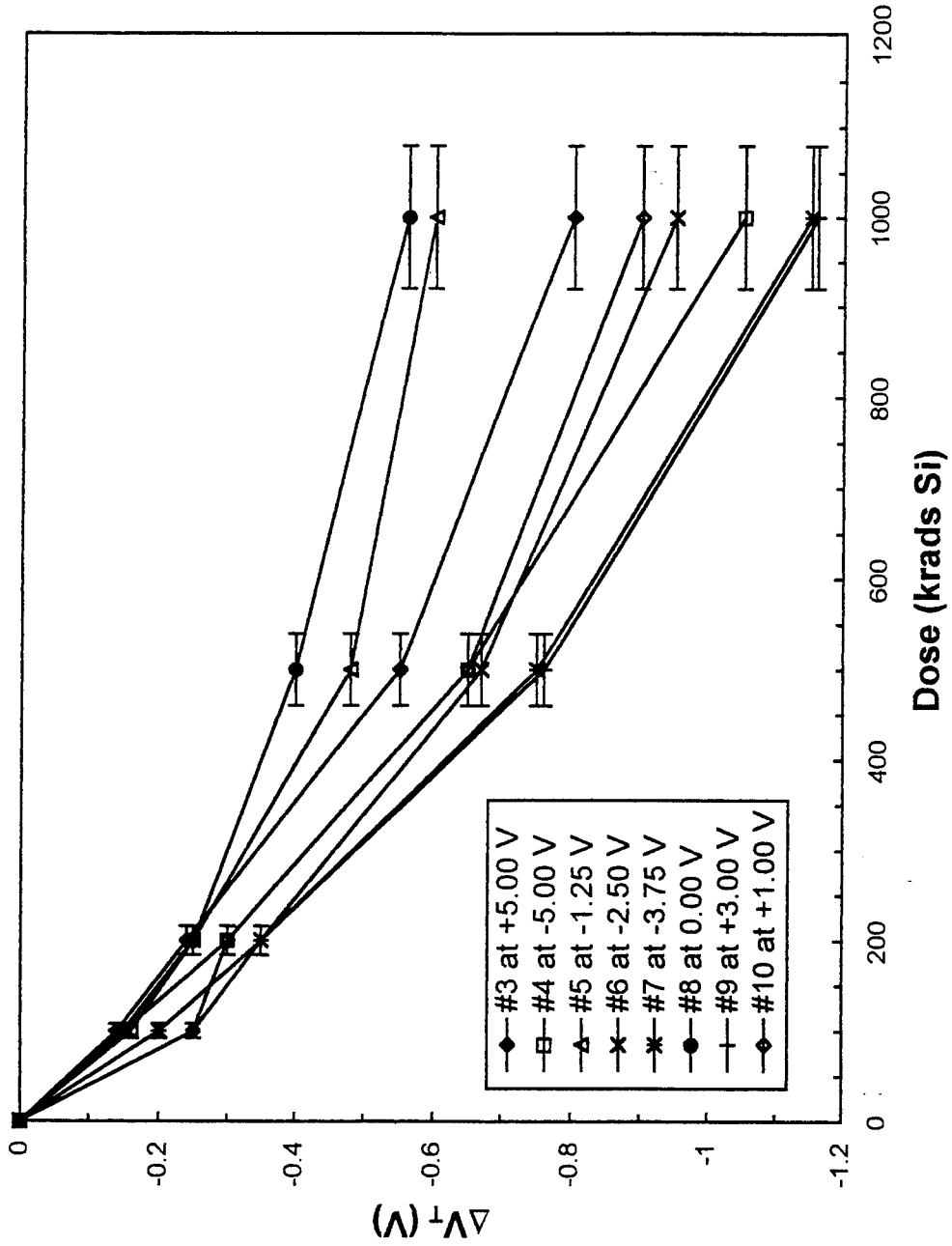

Figure 5-9. Threshold voltage shift versus total dose for the PTO transistors. The legend lists the transistor number and its gate bias during irradiation.

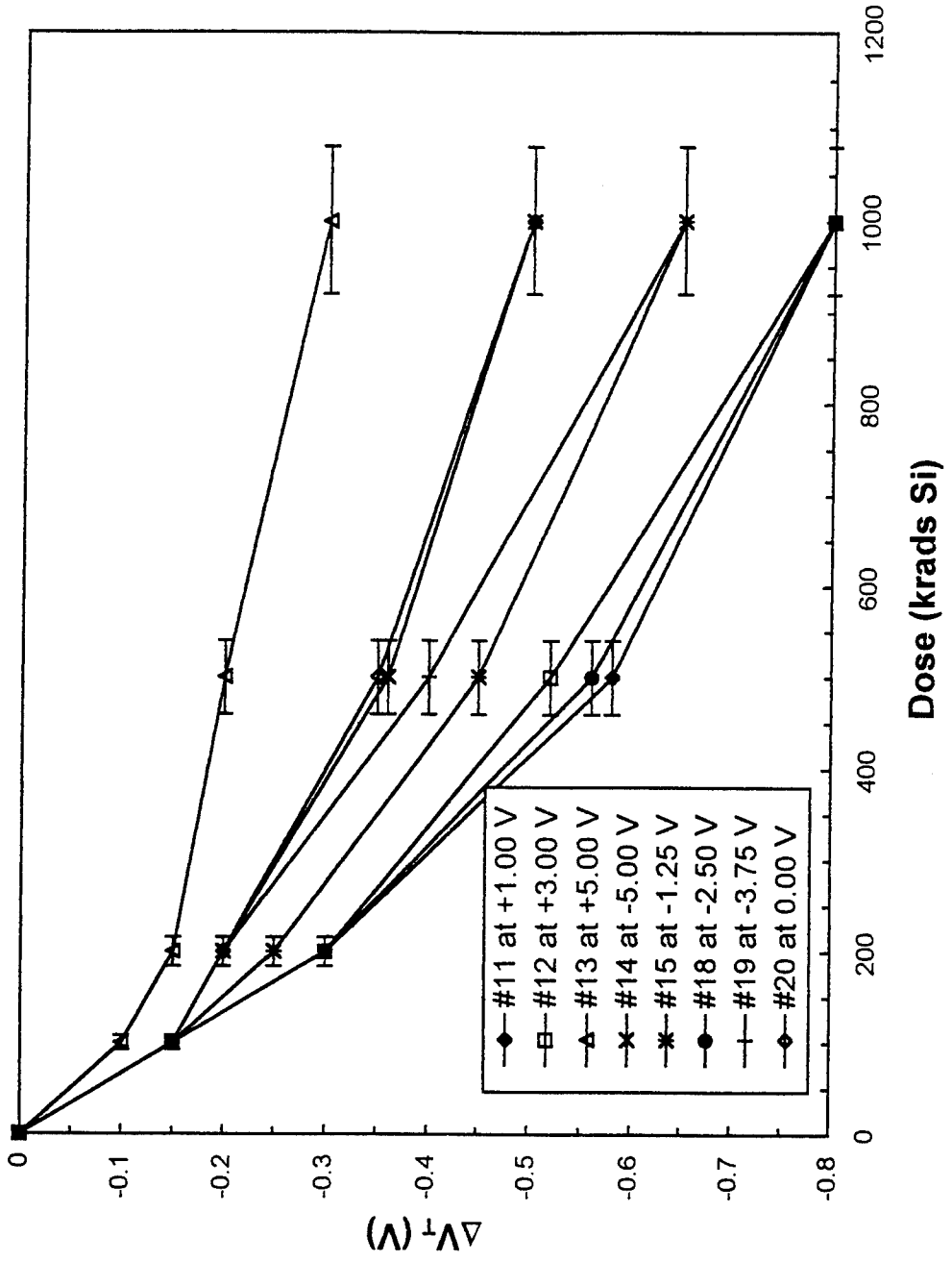

Figure 5-10. Threshold voltage shift versus total dose for the PRNO1 transistors. The legend lists the transistor number and its gate bias during irradiation.

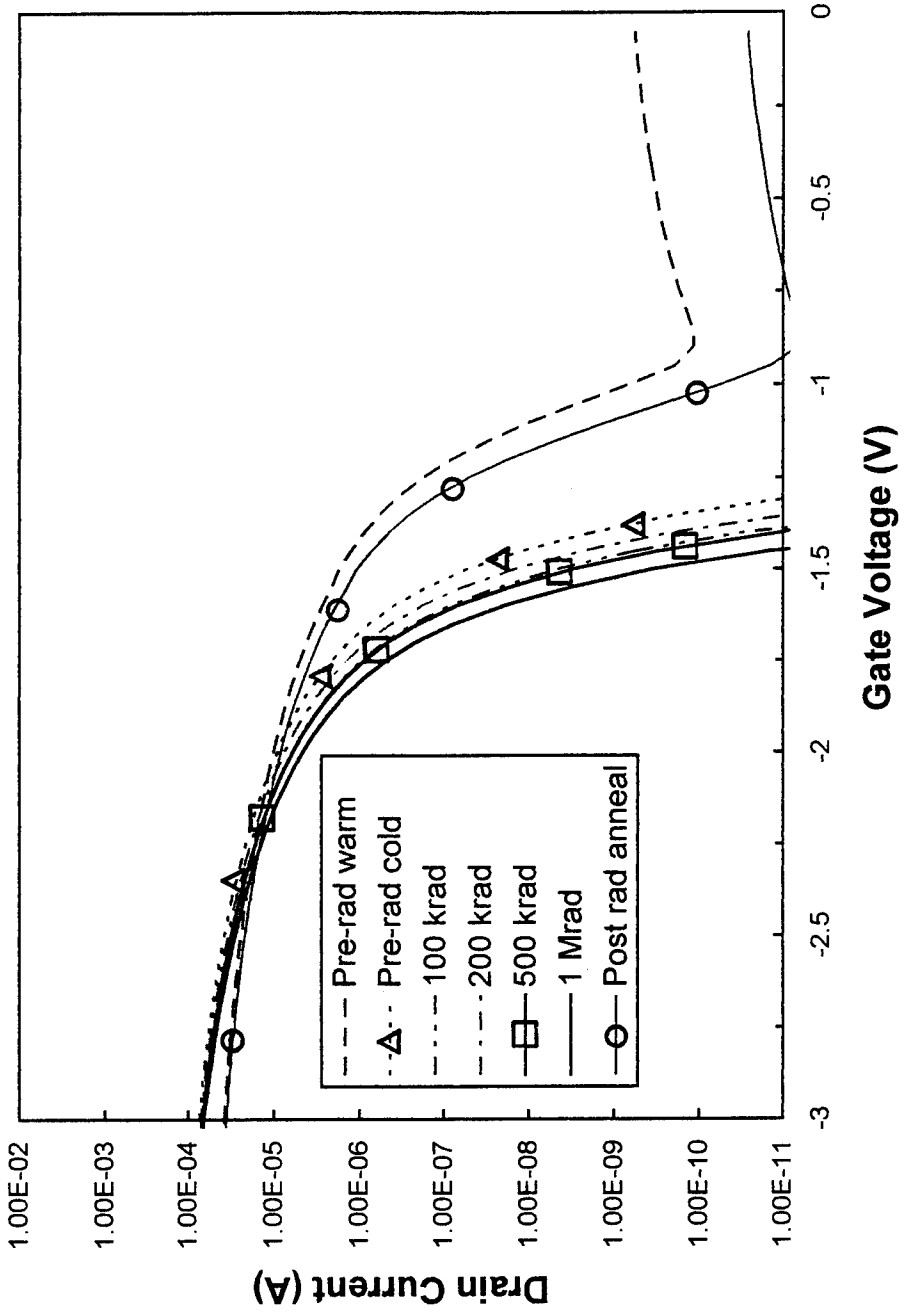

Figure 5-11. I_D-V_G characteristics of transistor 13PRNO2, V_D = 1.0 V, gate bias during irradiation was +5.00 V.

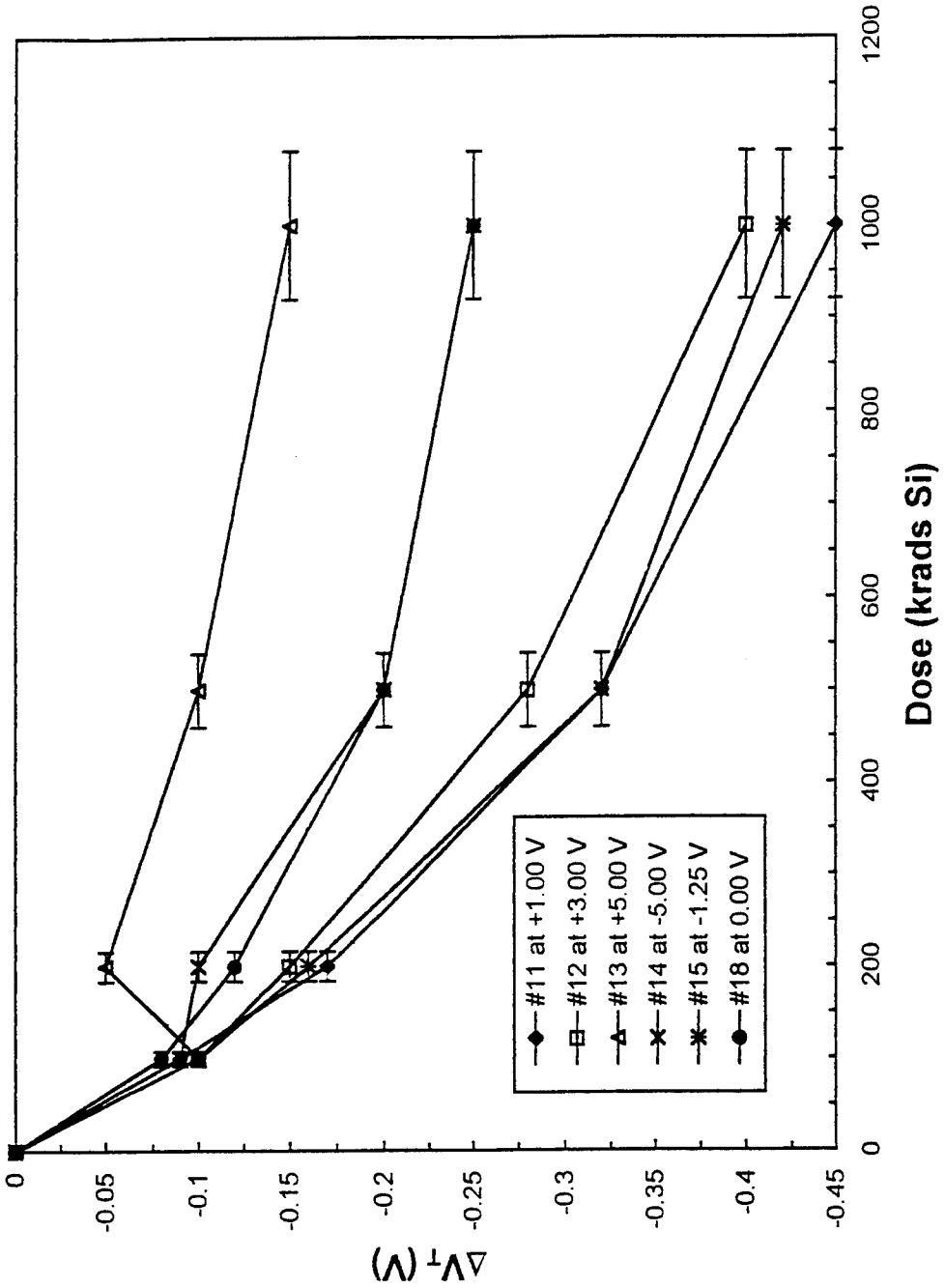

Figure 5-12. Threshold voltage shift versus total dose for the PRNO2 transistors. The legend lists the transistor number and its gate bias during irradiation.

5.2 Transconductance

The transconductance, gm, versus gate voltage for transistor 18PRNO2 with V_D = 0.1 V is plotted in Figure 5-13. All other transistors displayed similar transconductance behavior as 18PRNO2, except the PTO devices. It is observed from Figure 5-13 that the transconductance increases from the pre-rad warm condition to the pre-rad cold condition. As explained in Chapter 3 this increase in gm from room temperature to 77 K is due to an increase in the carrier mobility. Figure 5-13 also shows that there is virtually no change in the peak value of gm as the total dose increases. In fact there is very little change in the shape of the curves at the different dose levels. Very little change in transconductance is due to very little degradation of mobility, which is consistent with the observation that very few, if any, interface states buildup. However, the curves do shift in the negative gate voltage direction. These negative shifts of the gm curves correspond to the negative shifts in the I_D-V_G curves. There was very little change in gm as dose is increased for all of the transistors, except the PTO devices.

Figure 5-14 shows a plot of gm versus gate voltage for transistor 8PTO with V_D = 0.1 V. From this figure it is seen that the peak value of the transconductance decreases as the total dose increases. This decrease in the peak value for the PTO devices may be due to an increase in carrier scattering due to the trapped oxide charge (see section 3.4). These transistors typically had the largest negative V_T shifts which indicates large

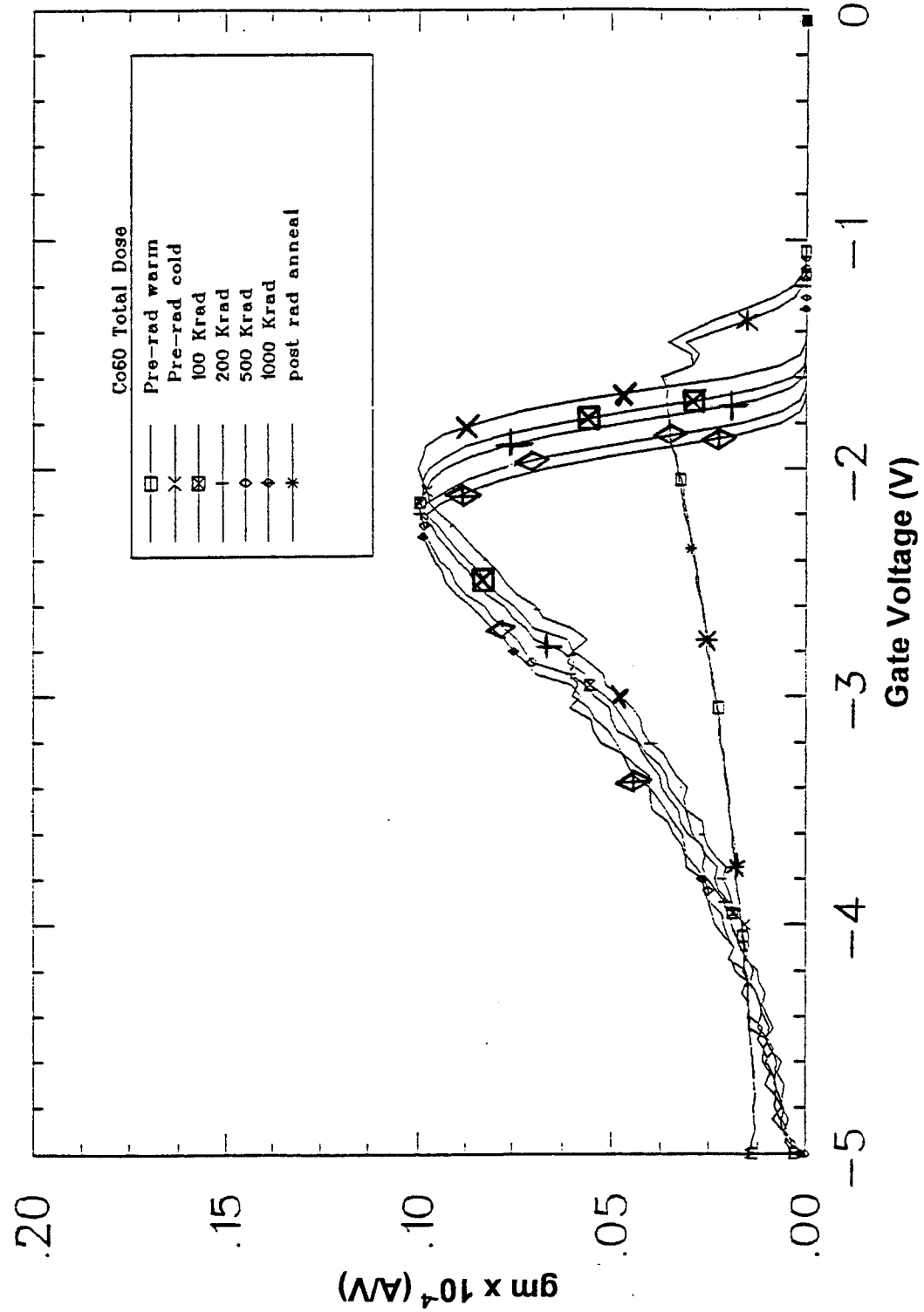

Figure 5-13. Transconductance versus gate voltage for transistor 18PRNO2, $V_D = 0.1$ V, gate bias during irradiation was 0.00 V.

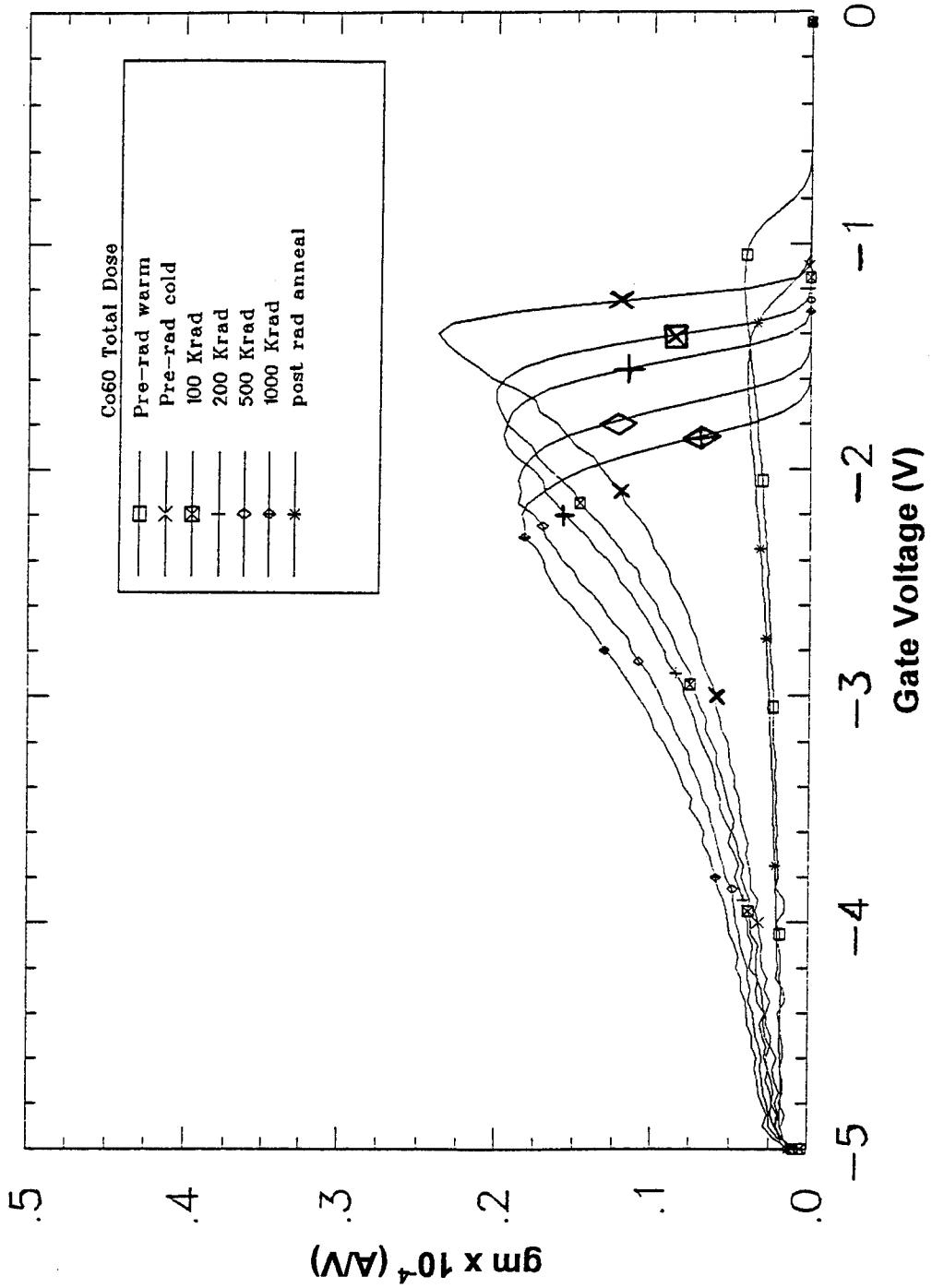

Figure 5-14. Transconductance versus gate voltage for transistor 8PTO, V_D = 0.1 V, gate bias during irradiation was 0.00 V.

concentrations of trapped positive charge. This increase in carrier scattering causes a reduction in the carrier mobility, and therefore a reduction in the transconductance. In the NTO devices the V_T shifts were significantly less compared to the PTO devices. This implies that there was far smaller concentrations of trapped charge in the NTO devices compared to PTO devices, and therefore far less change in the transconductance.

5.3 Gate Bias Effects

The effects that gate bias during irradiation has on device response is discussed in this section. Figure 5-15 shows the threshold voltage shift versus irradiation bias at the different dose levels for the NTO transistors. Displayed in Figure 5-15 is a cubic spline fit to the data. Every other transistor displayed similar bias dependencies as the NTO devices with the exception of the NRNO2 devices. Therefore, Figure 5-15 is a representative diagram for all of the devices, except the NRNO2 devices, which are discussed later in this chapter. It is seen from this figure that there is no bias dependence of ΔV_T at 100 krad(Si) and very little dependence at 200 krad(Si). However, as the total dose is increased above 200 krad(Si), there is a noticeable bias dependence of ΔV_T.

At a total dose of 1 Mrad(Si) there are two negative peaks in ΔV_T, one at +2.5 V and the other at -3.0 V (these correspond to electric fields of about +1.67 MV/cm and -2.00 MV/cm). At small values of the gate voltage (low electric field) some of the

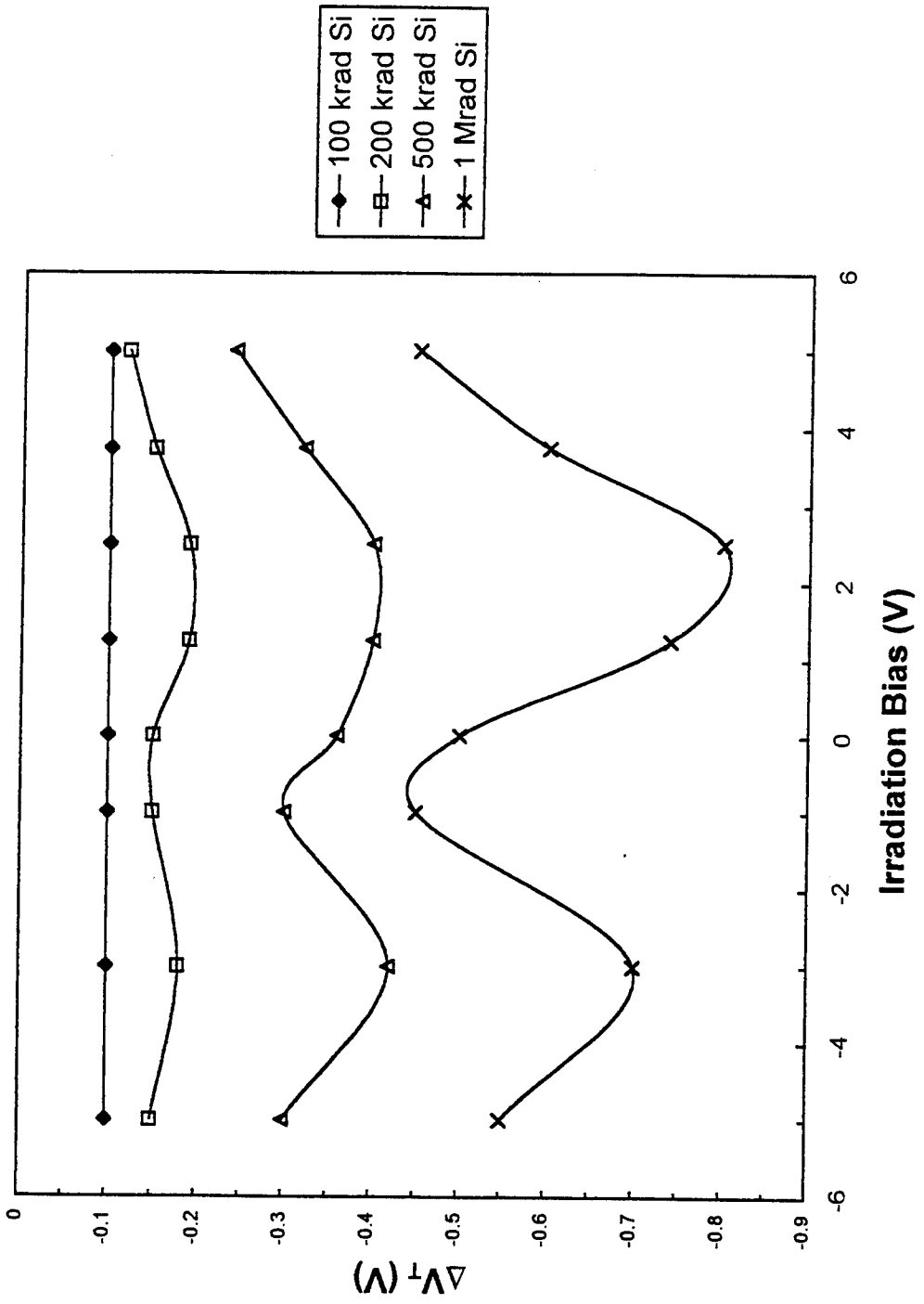

Figure 5-15. Threshold voltage shift versus bias during irradiation for the NTO transistors.

electrons and holes will recombine in the oxide. At 77 K, the electrons escaping recombination are swept out while the remaining holes are immobile. As the bias is increased, a larger fraction of the electrons escape recombination leaving an increasingly larger amount of trapped positive charge. Therefore, the V_T shift increases, in the negative direction (due to the trapped holes), with increasing applied voltage up to a point (about ± 2.00 MV/cm). At still higher gate voltages (greater than ± 2.00 MV/cm), the holes become mobile which results in less positive charge in the oxide, and thus a decrease in threshold voltage shift with increasing bias is observed. These results are in agreement with previously published results (13; 40; 41), see sections 2.1.1, 3.6.1, and 3.7.

Now consider the NRNO2 devices. Even at the low total dose levels the NRNO2 transistors showed a strong bias dependence. Figure 5-16 shows the threshold voltage shift versus irradiation bias for the NRNO2 transistors. Displayed in Figure 5-16 is a cubic spline fit to the data. From this figure it is clear that the NRNO2 devices are strongly dependent on the gate bias for all dose levels. All of the curves in Figure 5-16 are similar in shape, but there are shifts in the positive direction from 0 to 100 krad(Si) and from 100 to 200 krad(Si), and shifts in the negative direction as total dose is increased above 200 krad(Si). As discussed earlier in this chapter, this would imply that the negative trapped charge dominates up to 200 krad(Si) and then the trapped positive charge starts to counter this at doses above 200 krad(Si).

In the RNO devices for low applied gate bias there will be some recombination that takes place. It is proposed that at these low gate biases the trapping of electrons is

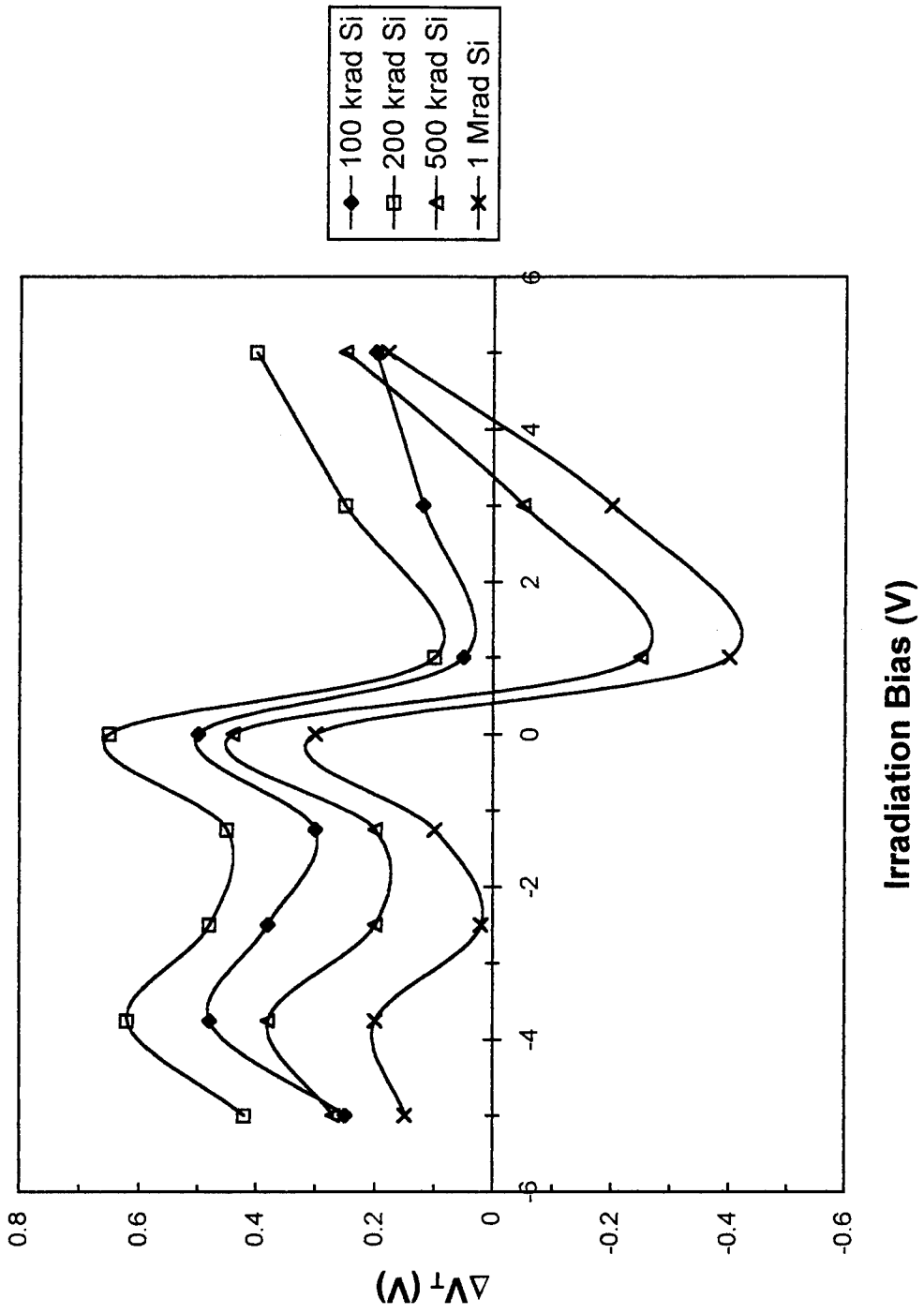

Figure 5-16. Threshold voltage shift versus bias during irradiation for the NRNO2 transistors.

much more efficient than the trapping of the holes up to 1 Mrad(Si). For no applied bias (0.0 V) we see the largest positive shifts in V_T, which reinforces this idea of electron trapping dominating at low biases. For 0.0 V biases, we can expect more electrons to be in the oxide, and for them to be around longer, compared to the other bias conditions, resulting in the largest V_T shifts. Therefore, in the RNO2 devices for low irradiation biases, we always observe positive threshold voltage shifts at all dose levels up to 1 Mrad(Si). Thus at low biases the positive threshold voltage shifts can be due to a relatively large concentration of trapped negative charge, a relatively small concentration of positive trapped charge, the location of the trapped charge within the oxide, or a combination of all of theses. In any case, at low gate biases the electron trapping dominates the hole trapping.

As the gate bias is increased there is less recombination taking place and the electrons are swept out of the oxide at a faster rate than the holes, which remain relatively less mobile. Therefore, as the bias increases more positive charge becomes trapped in comparison to the trapped negative charge. This results in a change in ΔV_T towards the negative direction. As you further increase the gate bias, the holes become much more mobile which results in a reduction in the trapped positive charge, and thus a change in the threshold voltage shift in the positive direction is observed. There appears to be still another change in the direction of ΔV_T as the gate bias is increased still further. At these large gate biases it is proposed that the electrons that are trapped become

detrapped due to the high electric field present in the oxide. These electrons are swept out of the oxide producing a change in the threshold voltage in the negative direction.

There is one last point to mention on the effects of bias on transistor response. Notice from Figure 5-16 that there is the tendency of the curves to shift further in the positive direction for negative biases. As discussed in chapter 3 the threshold voltage shift depends on where the charge is located within the oxide. The closer that the trapped charge is to the gate the less effect it has on ΔV_T. Therefore, for a negative gate bias the electrons will become trapped further from the gate than for a positive gate bias. Thus, if electron trapping is important, a negative gate bias will produce a more positive shift in ΔV_T compared to a positive gate bias. This does not mean that ΔV_T has to be positive for negative gate biases, but that it is more positive compared to positive applied biases.

5.4 Radiation Hardness

This section compares the magnitude of the threshold voltage shifts as functions of oxide processing. Figure 5-17 shows the threshold voltage shift versus total dose for the n-channel devices which were biased at +5.00 V during irradiation. Similar results were observed at the other gate bias conditions during irradiation. From Figure 5-17 it is

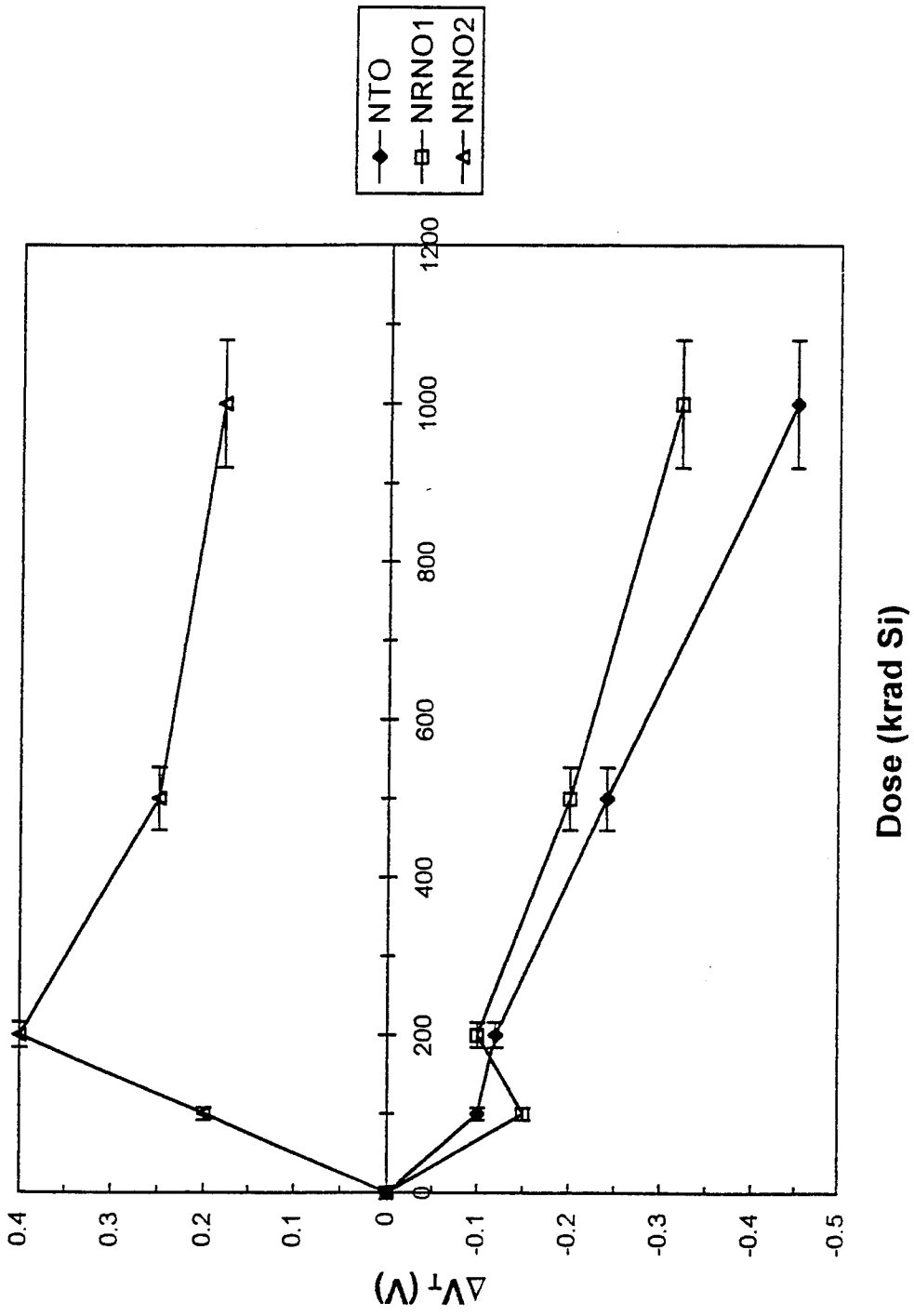

Figure 5-17. Threshold voltage shift versus total dose for n-channel devices which were biased at +5.00 V during irradiation.

observed that at low dose levels, below 200 krad(Si), the NTO device is as resistant to radiation degradation effects as the NRNO devices. However, at the largest doses the NRNO devices are much harder (greater resistance to radiation effects) than the NTO device. For example, at 1 Mrad(Si) the magnitudes of the threshold voltage shifts are 0.18, 0.32, and 0.45 V for the NRNO2, NRNO1, and NTO, respectively. The other n-channel devices, which were biased differently during irradiation, displayed similar results. Up to 1 Mrad(Si), none of the observed threshold voltage shifts would seem to be damaging given that a typical circuit can be designed to function with threshold voltage shifts up to 1.0 V (3).

The improved radiation hardness of the RNO devices is further illustrated by Figure 5-18. The threshold voltage shift versus total dose for the p-channel devices which were biased at -5.00 V during irradiation is shown in Figure 5-18. Similar results were also observed for the other p-channel devices, which were biased differently during irradiation. It is observed from Figure 5-18 that at every dose level the PRNO devices are more resistant (harder) to radiation degradation effects compared to the PTO device. In fact the hardest device is always the PRNO2 device. For example, at 1 Mrad(Si) the PRNO2 device displayed a threshold voltage shift of -0.25 V, compared to -0.50 V for the PRNO1 device and -1.05 V for the PTO device. The threshold voltage shift of -1.05 V at 1 Mrad(Si) for the PTO device could present a problem if the circuit was only designed to function with shifts up to ± 1.0 V. Therefore, the RNO devices would be better to use in circuits which are exposed to a total dose of 1 Mrad(Si). Based on the

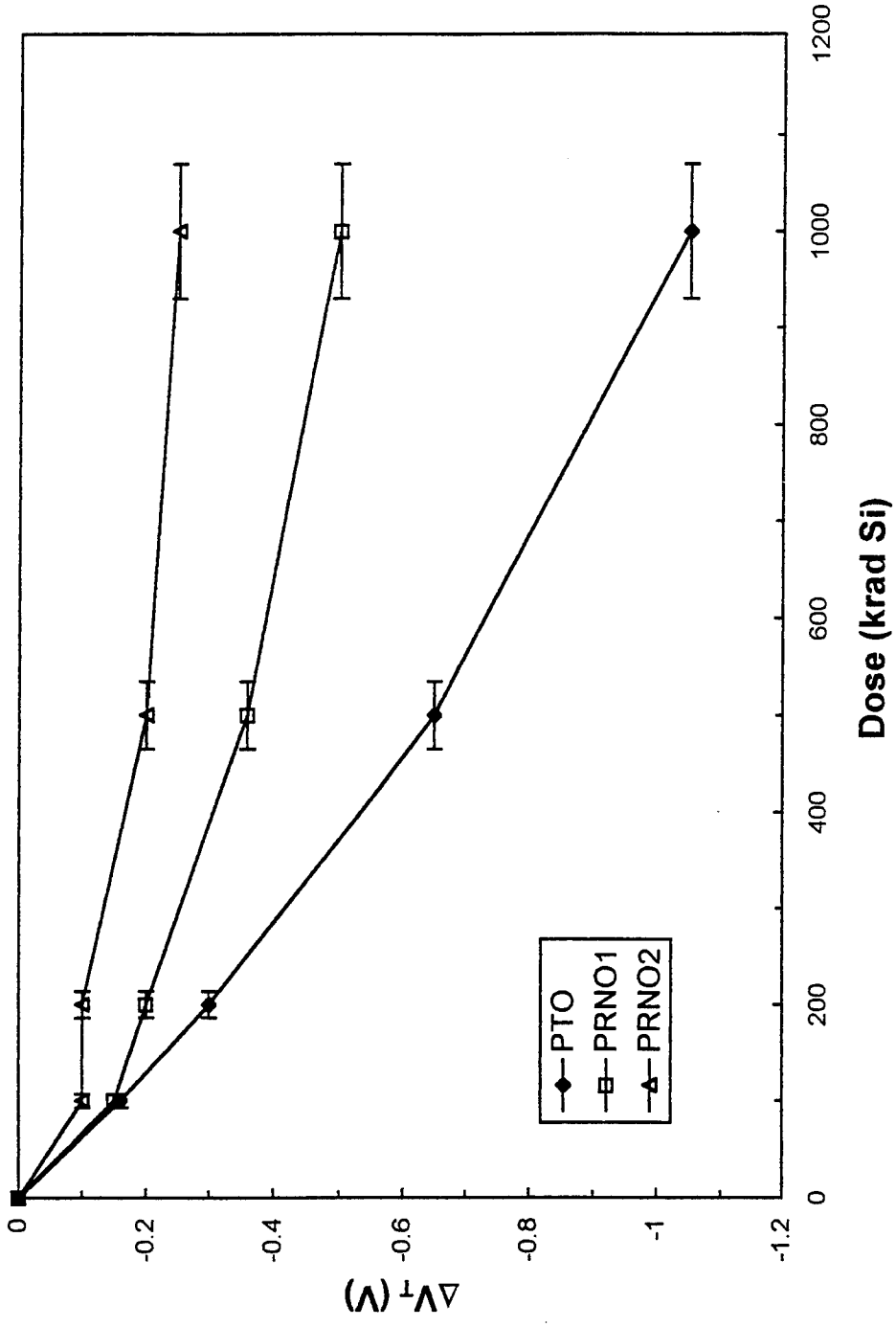

Figure 5-18. Threshold voltage shift versus total dose for p-channel devices which were biased at -5.00 V during irradiation.

results of this thesis it appears that the RNO devices are less susceptible (harder) to radiation degradation effects compared to thermal oxide devices.

VI. Summary and Recommendations

This thesis investigated total ionizing dose effects on MOSFET devices operated at 77 K. The MOSFETs, which were manufactured using the TRW process, consisted of both n-channel and p-channel variants. The gate oxide thickness of all the devices was 150 Å. A thermal oxide process and two different reoxidized nitrided oxide (RNO) processes were explored. The first set of RNO devices, RNO1, was processed by utilizing a rapid thermal nitridation (RTN) step for 60 seconds at a temperature of 1050 ^{o}C in a NH_3 ambient. The second set of RNO devices, RNO2, was processed using a RTN step for 60 seconds at a temperature of 1150 ^{o}C in a NH_3 ambient. Both sets of RNO devices went through a rapid thermal reoxidation step for 60 seconds at a temperature of 1050 ^{o}C in an oxygen ambient.

The total dose testing of the MOSFETs was performed at the Naval Weapons Support Center, Crane, Indiana. The transistors were immersed in liquid nitrogen (77 K) and irradiated using a Shepherd ^{60}Co test cell at a dose rate of 107.4 rads(Si)/sec. The dose rate was determined with CaF_2:Mn thermoluminescent dosimeters. Electrical measurements were made before irradiation at both room temperature and 77 K. The transistors were irradiated, at 77 K, up to a total dose of 1000 krad(Si), with measurements made at 100, 200, 500, and 1000 krad(Si). During irradiation each transistor was biased at a specific gate voltage between -5.0 V and +5.0 V. Drain

current-gate voltage (I_D-V_G) characteristics of the transistors were obtained at applied drain biases of 0.1 V and 1.0 V. The I_D-V_G data was used to determine the threshold voltage, V_T, transconductance, gm, and to check for the buildup of interface states.

It was observed that there was no significant change in the subthreshold slope, ΔS, indicating no significant buildup of interface states in any of the transistors after irradiation up to 1 Mrad(Si). The suppression of radiation-generated interface states at 77 K was expected based on the present understanding for the formation of interface states. The major mechanism for the formation of interface states is believed to include the transport and /or trapping of holes in the oxide, and the release and transport of hydrogen ions to the interface, where they react to form interface states. At 77 K both the holes and hydrogen ions will be relatively immobile, and are thus incapable of forming interface states. If no interface states are formed by irradiation, then any shift in the threshold voltage must be attributed to trapped charge, positive or negative, in the gate oxide.

All of the thermal oxide transistors, both n-channel and p-channel, displayed negative shifts in threshold voltage as total dose increased. The negative threshold voltage shifts are due to the trapping of positive charge (holes) in the oxide. As the radiation dose increases the amount of trapped positive charge increases, which results in larger negative shifts in threshold voltage.

The RNO1 devices exhibited behavior which was similar to the thermal oxides. Negative shifts in threshold voltage for increasing total dose was also observed in the

RNO1 devices. However, there was one exception to the observed negative threshold voltage shifts of the NRNO1 devices. Transistor 14NRNO1 displayed a positive shift in threshold voltage after being irradiated from 100 to 200 krad(Si). This positive shift was unexpected and it is uncertain as to why this one transistor behaved in this manner. The positive shift may be attributed to trapped negative charge, annealing of trapped positive charge, a combination of both of these processes, an anomaly associated with this particular device, or an error with the data at 100 krad(Si).

In the n-channel RNO2 devices it was concluded that electron trapping dominates over hole trapping up to 200 krad(Si). Positive threshold voltage shifts from 0 to 100 krad(Si) and from 100 to 200 krad(Si) were observed for all of the n-channel RNO2 devices. It is proposed that up to 200 krad(Si) there are more electron traps being filled compared to hole traps due to a higher capture efficiency of the electron traps. Therefore, electron traps become filled more rapidly than hole traps, resulting in positive shifts in threshold voltage. The electron traps appear to saturate around 200 krad(Si), producing a maximum positive shift in the threshold voltage. After the electron traps have saturated, the hole traps continue being filled, resulting in negative shifts in the threshold voltage for doses above 200 krad(Si). In addition, it may be possible to have a significantly large tunnel annealing rate for holes trapped near the silicon-oxide interface in the RNO devices. If trapped holes are annealing at a significantly fast rate, then this would contribute to the positive threshold voltage shift. The observed positive threshold voltage shifts in the NRNO2 devices may be due to a combination of the above mentioned processes, or possibly something happened to all of these devices during

testing. One possible explanation is that positive charge somehow built up in the substrate, resulting in the positive threshold voltage shifts. However, it is the author's belief that the NRNO2 substrates were properly connected to prevent this buildup of charge.

By looking at the data on applied gate bias during irradiation we can obtain support for the argument that electron trapping is dominating over hole trapping. For a negative gate bias, electrons will become trapped further from the gate than for a positive gate bias. This results in a greater positive shift in threshold voltage for the negative bias case compared to the positive bias case, which was verified by the experimental results.

The p-channel devices exhibited negative shifts in threshold voltage with increasing total dose due to positive trapped charge in the oxide. There was one exception to these observed negative shifts, transistor 13PRNO2 displayed a positive shift after irradiation from 100 to 200 krad(Si). As with the n-channel RNO1 device, which displayed similar characteristics, it is uncertain as to why this behavior was observed. Once again it is possible that there was an increase in trapped negative charge, and/or a decrease in trapped positive charge, or some type of anomaly for this transistor.

In addition to threshold voltage, the transconductance was determined from the I_D-V_G characteristics. There was very little change in the transconductance after irradiation up to 1 Mrad(Si) for all of the devices tested, except for the PTO devices. This lack of change in the transconductance can be attributed to the absence of change in carrier mobility, which is consistent with the observation that there is no radiation-generated interface state buildup. The change in transconductance for the PTO

devices can be attributed to an increase in carrier scattering due to large concentrations of trapped oxide charge. The increase in carrier scattering causes a reduction in carrier mobility, and therefore a reduction in transconductance.

It was the goal of this research project to enhance the understanding of the effects of total radiation dose on MOSFETs operating at 77 K. Based on the results of this thesis it was determined that the RNO devices are typically less susceptible to radiation degradation effects compared to thermal oxide devices. In addition, to the best of the author's knowledge, this report presents some of the first evidence that electron trapping may dominate over hole trapping in RNO transistors up to 200 krad(Si). It needs to be stressed that this was only one experiment and that several similar experiments need to be performed to prove the validity of these results. There still needs to be more research conducted in this area of study, since several questions remain unanswered. Questions concerning the exact process or processes responsible for the formation of interface states, the microscopic nature of both hole and electron traps in RNO, and the transport and capture of both holes and electrons in RNO as functions of temperature and applied bias need to be explored further.

There are several possible follow on projects which could be conducted at the Air Force Institute of Technology in the area of radiation effects on MOSFETs. A follow on experiment that attempts to repeat the results obtained on the NRNO2 devices would be extremely beneficial. Another project that would be beneficial would be to do total ionizing dose testing on nitrided oxide devices as well as thermal oxide and RNO devices. In addition, a greater range of nitridation and reoxidation times and

temperatures would provide more insight into the effects of oxide processing on total ionizing dose response. It would also be beneficial to take measurements at several more applied gate bias conditions and ionizing dose levels, including dose levels below 100 krad(Si). This way one can get a better look at the response of the RNO devices leading up to 200 krad(Si) to see if electron trapping is dominating in the entire low dose level regime. Furthermore, hot carrier effects on MOSFETs could also be explored. Hot carriers, like ionizing radiation, can also produce trapped oxide charge and interface state buildup. Therefore, a combined total dose/hot carrier effects study could be of significant value.

Bibliography

1. Gaensslen, Fritz H. "Very Small MOSFET's for Low-Temperature Operation," IEEE Transactions on Electron Devices, 24: 218-229 (March 1977).

2. Fox, Robert M. and Richard C. Jaeger. "MOSFET Behavior and Circuit Considerations for Analog Applications at 77 K," IEEE Transactions on Electron Devices, 34: 114-123 (January 1987).

3. Pickel, J. C. and others. "Infrared Focal Plane Array Hardening Concepts." Draft Report. Maxwell Laboratories, Inc., 1992.

4. Schwank, James R. "Basic Mechanisms of Radiation Effects in the Natural Space Environment." IEEE NSREC Short Course. 1994.

5. Bhat, N. and J. Vasi. "Interface-State Generation Under Radiation and High-Field Stressing in Reoxidized Nitrided Oxide MOS Capacitors," IEEE Transactions on Nuclear Science, 39: 2230-2235 (December 1992).

6. Dunn, Gregory J. and Peter W. Wyatt. "Reoxidized Nitrided Oxides for Radiation-Hardened MOS Devices," IEEE Transactions on Nuclear Science, 36: 2161-2168 (December 1989).

7. Terry, F. L. Jr. and others. "Radiation Effects in Nitrided Oxides," IEEE Electron Device Letters, 6: 191-193 (June 1983).

8. Malik, A. and others. "Electron Trapping During Irradiation in Reoxidized Nitrided Oxides," IEEE Transactions on Nuclear Science, 40: 1380-1387 (December 1993).

9. Boesch, Edwin H. Jr. and others. "Hole Transport and Charge Relaxation in Irradiated SiO_2 MOS Capacitors," IEEE Transactions on Nuclear Science, 22: 2163-2167 (December 1975).

10. Boesch, H. E., and others. "Temperature and Field-Dependent Charge Relaxation in SiO2 Gate Insulators," IEEE Transactions on Nuclear Science, 25: 1012-1016 (June 1978).

11. Boesch, H. E. and others. "Enhanced Flatband Voltage Recovery in Hardened Thin MOS Capacitors," IEEE Transactions on Nuclear Science, 25: 1239-1245 (December 1978).

12. McLean, F. B. and others. "Hole Transport and Recovery Characteristics of SiO_2 Gate Insulators," IEEE Transactions on Nuclear Science, 23: 1506-1511 (December 1976).

13. McLean, F. B. and Timothy R. Oldham. Basic Mechanisms of Radiation Effects in Electronic Materials and Devices. Harry Diamond Laboratories. HDL-TR-2129 (September 1987).

14. Ma, T. P. and Paul V. Dressendorfer. Ionizing Radiation Effects in MOS Devices and Circuits. New York: John Wiley and Sons, 1989.

15. Boesch, Edwin H. Jr. and G. J. Dunn. "Hole Transport in SiO_2 and Reoxidized Nitrided SiO_2 Gate Insulators at Low Temperature," IEEE Transactions on Nuclear Science, 38 : 1083-1088 (December 1991).

16. Conley, J. F. and P. M. Lenahan. "Molecular Hydrogen, E' Center Hole Traps, and Radiation Induced Interface Traps in MOS Devices," IEEE Transactions on Nuclear Science, 40 : 1335-1340 (December 1993).

17. Lenahan, P. M. and P. V. Dressendorfer. "Hole Traps and Trivalent Silicon Centers in Metal/Oxide/Silicon Devices," Journal of Applied Physics, 55: 3495-3499 (May 1984).

18. Lenahan, P. M. and P. V. Dressendorfer. "Microstructural Variation in Radiation Hard and Soft Oxides Observed Through Electron Spin Resonance," IEEE Transactions on Nuclear Science, 30 : 4602-4604 (December 1983).

19. Yount, J. T. and P. M. Lenahan. "Electron Spin Resonance Study of Radiation-Induced Point Defects in Nitrided and Reoxidized Nitrided Oxides," IEEE Transactions on Nuclear Science, 39: 2211-2219 (December 1992).

20. Lenahan, P. M. and P. V. Dressendorfer. "An Electron Spin Resonance Study of Radiation-Induced Electrically Active Paramagnetic Centers at the Si/SiO_2 Interface," Journal of Applied Physics, 54: 1457-1460 (May 1984).

21. Oldham, T. R. and others. "An overview of radiation-induced interface traps in MOS structures," Harry Diamond Laboratories : 986-999 (August 1989).

22. McLean, F. B. "A Framework For Understanding Radiation-Induced Interface States in SiO2 MOS Structures," IEEE Transactions on Nuclear Science, 27: 1651-1657 (December 1980).

23. Winokur, P. S. and others. "Two-Stage Process for Buildup of Radiation-Induced Interface States," Journal of Applied Physics, 50: 3492-3494 (May 1979).

24. Shaneyfelt, M. R. and others. "Interface-Trap Buildup Rates in Wet and Dry Oxides," IEEE Transactions on Nuclear Science, 39: 2244-2251 (December 1992).

25. Saks, N. S. and M. G. Ancona. "Generation of Interface States by Ionizing Radiation at 80 K Measured by Charge Pumping and Subthreshold Slope Techniques," IEEE Transactions on Nuclear Science, 34: 1348-1354 (December 1987).

26. Saks, N. S. and others. "Formation of Interface Traps in MOSFETs During Annealing Following Low Temperature Radiation," IEEE Transactions on Nuclear Science, 35: 1234-1240 (December 1988).

27. Neaman, Donald A. Semiconductor Physics and Devices. Illinois: Richard D. Irwin, 1992.

28. Clark, W. F. and others. "Low Temperature CMOS A Brief Review." IBM General Technology Division (July 1991).

29. Messenger, George C. and Milton S. Ash. The Effects of Radiation on Electronic Systems. New York : Van Nostrand Reinhold, 1992.

30. Sze, S. M. Physics of Semiconductor Devices. New York : John Wiley & Sons, 1981.

31. Saks, N. S. and J. M. Modolo. "Radiation Effects in N-Channel MNOS CCDs at Low Temperature," IEEE Transactions on Nuclear Science, 30: 4197-4204 (December 1983).

32. Saks, N. S. and others. "Radiation Effects in MOS Capacitors With Very Thin Oxides at 80 ^{o}K," IEEE Transactions on Nuclear Science, 6: 1249-1255 (December 1984).

33. Lamarsh, John R. Introduction to Nuclear Engineering. Menlo Park, California: Addison-Wesley, 1983.

34. McLean, F. B. and others. "Electron-Hole Generation, Transport, and Trapping in SiO2," in Ionizing Radiation Effects in MOS Devices and Circuits, edited by T. P. Ma and P. V. Dressendorfer, John Wiley & Sons, New York, 87-192, 1989.

35. Shaneyfelt, M. R. and others. "Field Dependence of Interface-Trap Buildup in Polysilicon and Metal Gate MOS Devices," IEEE Transactions on Nuclear Science, 37: 1632-1640 (December 1990).

36. Winokur, Peter S. "Radiation-Induced Interface Traps," in Ionizing Radiation Effects in MOS Devices and Circuits, edited by T. P. Ma and P. V. Dressendorfer, John Wiley & Sons, New York, 87-192, 1989.

37. Saks, N. S. and D. B. Brown. "Observation of H+ Motion During Interface Trap Formation," IEEE Transactions on Nuclear Science, 37: 1624-1631 (December 1990).

38. Saks, N. S. and others. "Effects of Switched gate Bias on Radiation-Induced Interface Trap Formation," IEEE Transactions on Nuclear Science, 38: 1130-1139 (December 1991).

39. Lai, S. K. "Two-carrier nature of interface-state generation in hole trapping and radiation damage," Appl. Phys. Lett., 39: 58-60 (April 1981).

40. Srour, J. R. and K. Y. Chiu. "MOS Hardening Approaches for Low-Temperature Applications," IEEE Transactions on Nuclear Science, 24: 2140-2145 (December 1977).

41. Pantelakis, Dimitris C. and others. "Freeze-Out Characterization of Radiation Hardened N+ Polysilicon Gate CMOS Transistors," Unpublished Report. Harris Semiconductor.

42. Dunn, Gregory J. and others. "Radiation-Induced Increase in the Inversion Layer Mobility of Reoxidized Nitrided Oxide MOSFET's," IEEE Transactions on Electron Devices, 39: 677-684 (March 1992).

43. Dunn, G. L. and others. "Radiation Effects in Low-Pressure Reoxidized Nitrided Oxide Gate Dielectrics," Appl. Phys. Lett. 52: 1713-1715 (May 1988).

44. Naiman, M. L. and others. "The Constitution of Nitrided Oxides and Reoxidized Nitrided Oxides on Silicon," Journal of Applied Physics, 58: 779-792 (July 1985).

45. Sundaresan, Ravishankar and others. "Rapid-Thermal Nitridation of SiO_2 for Radiation-Hardened MOS Gate Dielectrics," IEEE Transactions on Nuclear Science, 33: 1223-1227 (December 1986).

46. Shepherd Model 484 Irradiation Facility Fact Sheet.

47. Cole, Patrick. Unpublished Internal Notes. Naval Surface Warfare Center. October, 1991.

48. Schwank, J. R. and others. "Physical Mechanisms Contributing to Device Rebound," IEEE Transactions on Nuclear Science, 31: 1434-1438 (December 1984).

Vita

Captain Kevin J. Daul was born on 18 May 1967 in Rochester, New York. He graduated from Brockport High School in Brockport, New York in 1985 and attended Worcester Polytechnic Institute, graduating with a Bachelor of Science in Mechanical Engineering in May 1989. Upon graduation, he received a commission in the USAF and served his first tour of duty at Kirtland AFB, New Mexico. There he was responsible for research into satellite vulnerability and survivability until entering the School of Engineering, Air Force Institute of Technology, in May 1993.

1 Dogwood Drive
Hamlin, New York 14464

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	DEC 1994	Master's Thesis

4. TITLE AND SUBTITLE
TOTAL IONIZING DOSE EFFECTS IN MOSFET DEVICES AT 77 K

5. FUNDING NUMBERS

6. AUTHOR(S)
Kevin J. Daul, Captain, USAF

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Air Force Institute of Technology
2750 P Street
WPAFB OH 45433-6583

8. PERFORMING ORGANIZATION REPORT NUMBER
AFIT/GAP/ENP/94D-01

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
DNA/RAEE
6801 Telegraph Rd.
Alexandria, Virginia 22310

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

Total ionizing dose effects on thermal oxide and reoxidized nitrided oxide (RNO) MOSFET devices at 77 K were studied. The MOSFETs were immersed in liquid nitrogen and irradiated, using a Co-60 source, up to 1 Mrad(Si) at a dose rate of 107 rads(Si)/sec. Drain current-gate voltage characteristics were obtained and used to determine threshold voltage and transconductance. At 77 K the subthreshold slopes indicated no observed buildup of interface states in any of the transistors. Furthermore, all transistors experienced very little change in the transconductance. Typical negative shifts in threshold voltage as dose increased were observed in all of the thermal oxide devices. The threshold voltage shifts of the RNO devices were typically less than those for thermal oxide devices.

14. SUBJECT TERMS
MOSFET SEMICONDUCTORS, RADIATION EFFECTS, CRYOGENICS, IONIZING RADIATION, RADIATION DOSE

15. NUMBER OF PAGES
124

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	Unlimited

GENERAL INSTRUCTIONS FOR COMPLETING SF 298

The Report Documentation Page (RDP) is used in announcing and cataloging reports. It is important that this information be consistent with the rest of the report, particularly the cover and title page. Instructions for filling in each block of the form follow. It is important to ***stay within the lines*** to meet ***optical scanning requirements***.

Block 1. Agency Use Only *(Leave blank)*.

Block 2. Report Date. Full publication date including day, month, and year, if available (e.g. 1 Jan 88). Must cite at least the year.

Block 3. Type of Report and Dates Covered. State whether report is interim, final, etc. If applicable, enter inclusive report dates (e.g. 10 Jun 87 - 30 Jun 88).

Block 4. Title and Subtitle. A title is taken from the part of the report that provides the most meaningful and complete information. When a report is prepared in more than one volume, repeat the primary title, add volume number, and include subtitle for the specific volume. On classified documents enter the title classification in parentheses.

Block 5. Funding Numbers. To include contract and grant numbers; may include program element number(s), project number(s), task number(s), and work unit number(s). Use the following labels:

C	- Contract	**PR**	- Project
G	- Grant	**TA**	- Task
PE	- Program Element	**WU**	- Work Unit Accession No.

Block 6. Author(s). Name(s) of person(s) responsible for writing the report, performing the research, or credited with the content of the report. If editor or compiler, this should follow the name(s).

Block 7. Performing Organization Name(s) and Address(es). Self-explanatory.

Block 8. Performing Organization Report Number. Enter the unique alphanumeric report number(s) assigned by the organization performing the report.

Block 9. Sponsoring/Monitoring Agency Name(s) and Address(es). Self-explanatory.

Block 10. Sponsoring/Monitoring Agency Report Number. *(If known)*

Block 11. Supplementary Notes. Enter information not included elsewhere such as: Prepared in cooperation with...; Trans. of...; To be published in.... When a report is revised, include a statement whether the new report supersedes or supplements the older report.

Block 12a. Distribution/Availability Statement. Denotes public availability or limitations. Cite any availability to the public. Enter additional limitations or special markings in all capitals (e.g. NOFORN, REL, ITAR).

- **DOD** - See DoDD 5230.24, "Distribution Statements on Technical Documents."
- **DOE** - See authorities.
- **NASA** - See Handbook NHB 2200.2.
- **NTIS** - Leave blank.

Block 12b. Distribution Code.

- **DOD** - Leave blank.
- **DOE** - Enter DOE distribution categories from the Standard Distribution for Unclassified Scientific and Technical Reports.
- **NASA** - Leave blank.
- **NTIS** - Leave blank.

Block 13. Abstract. Include a brief *(Maximum 200 words)* factual summary of the most significant information contained in the report.

Block 14. Subject Terms. Keywords or phrases identifying major subjects in the report.

Block 15. Number of Pages. Enter the total number of pages.

Block 16. Price Code. Enter appropriate price code *(NTIS only)*.

Blocks 17. - 19. Security Classifications. Self-explanatory. Enter U.S. Security Classification in accordance with U.S. Security Regulations (i.e., UNCLASSIFIED). If form contains classified information, stamp classification on the top and bottom of the page.

Block 20. Limitation of Abstract. This block must be completed to assign a limitation to the abstract. Enter either UL (unlimited) or SAR (same as report). An entry in this block is necessary if the abstract is to be limited. If blank, the abstract is assumed to be unlimited.

★U.S.GPO:1989-0-273-271