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Atomic Layer Epitaxy of Group IV Materials: Surface Processes, Thin Films, Devices and Their Characterization

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13. ABSTRACT ***(Maximum 200 words)***

Residual surface contaminants were removed from vicinal 6H-SiC(0001) surfaces in UHV via high temperature annealing in SiH_4. Characterization via AES, EELS, LEED, XPS, and UPS was conducted. At T>850°C, the surface oxide was rapidly removed. Exposure to ≈400 Langmuir (10^{-6}Torr•liter/s) of SiH_4 resulted in complete surface oxide removal and a nearly stoichiometric (1×1) 6H-SiC surface suitable for ALE of SiC. Further exposure resulted in a (3×3) Si-rich reconstructed surface. Subsequent annealing in UHV resulted in a $(\sqrt{3}\times\sqrt{3})R30°$ Si deficient/graphitic reconstructed surface. The first set of wafers containing HBT device structures were fabricated on SiC films grown via ALE. No transistor activity was detected. Electrical characterization and SEM showed the most likely fault to be inaccurate etching of the SiC emitter. Nucleation and growth of oriented diamond particles on seeded, <0001> oriented single crystal Co substrates was achieved via multi-step, hot-filament CVD process involving seeding, annealing, nucleation and growth. Diamond particles oriented <111> were obtained. Micro-Raman showed a FWHM of 4.3 cm^{-1}. A very weak graphitic peak was observed on regions of the substrate not covered by the diamond particles. A nucleation model has been proposed. Initial results showed that CeO_2 film grows epitaxially on (111)Si substrates. The CeO_2 films had density of interfacial traps and fixed oxide charge values comparable to that of amorphous SiO_2/Si.

14. SUBJECT TERMS

ALE, SiC, silicon carbide, surface contaminants, SiH_4, AES, EELS, LEED, XPS, UPS, bipolar transistor, diamond, Co substrates, CVD, micro-Raman, CeO_2/Si MOS structure, RBS, amorphous α-SiO_2

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I. Introduction

Atomic layer epitaxy (ALE) is the sequential chemisorption of one or more elemental species or complexes within a time period or chemical environment in which only one monolayer of each species is chemisorbed on the surface of the growing film in each period of the sequence. The excess of a given reactant which is in the gas phase or only physisorbed is purged from the substrate surface region before this surface is exposed to a subsequent reactant. This latter reactant chemisorbs and undergoes reaction with the first reactant on the substrate surface resulting in the formation of a solid film. There are essentially two types of ALE which, for convenience, shall be called Type I and Type II.

In its early development in Finland, the Type I growth scenario frequently involved the deposition of more than one monolayer of the given species. However, at that time, ALE was considered possible only in those materials wherein the bond energies between like metal species and like nonmetal species were each less than that of the metal-nonmetal combination. Thus, even if multiple monolayers of a given element were produced, the material in excess of one monolayer could be sublimed by increasing the temperature and/or waiting for a sufficient period of time under vacuum. Under these chemical constraints, materials such as GaAs were initially thought to be improbable since the Ga-Ga bond strength exceeds that of the GaAs bond strength. However, the self-limiting layer-by-layer deposition of this material proved to be an early example of Type II ALE wherein the trimethylgallium (TMG) chemisorbed to the growing surface and effectively prevented additional adsorption of the incoming metalorganic molecules. The introduction of As, however caused an exchange with the chemisorbed TMG such that a gaseous side product was removed from the growing surface. Two alternating molecular species are also frequently used such that chemisorption of each species occurs sequentially and is accompanied by extraction, abstraction and exchange reactions to produce self-limiting layer-by-layer growth of an element, solid solution or a compound.

The Type II approach has been used primarily for growth of II–VI compounds [1–13]; however, recent studies have shown that it is also applicable for oxides [14–18], nitrides [19], III–V GaAs-based semiconductors [20–33] and silicon [34–36]. The advantages of ALE include monolayer thickness control, growth of abrupt interfaces, growth of uniform and graded solid solutions with controlled composition, reduction in macroscopic defects and uniform coverage over large areas. A commercial application which makes use of the last attribute is large area electroluminescent displays produced from II–VI materials. Two comprehensive reviews [37,6], one limited overview [38] and a book [39] devoted entirely to the subject of ALE have recently been published.

In this reporting period, investigations concerned with (1) removal of residual oxygen and other surface contaminants from 6H-SiC(0001) via high temperature annealing in SiH_4, (2) the fabrication and testing of heterojunction bipolar junction devices of SiC films grown via ALE,

(3) nucleation, growth and Raman characterization of oriented diamond particles on seeded <0001> Co substrates and (4) the study of the epitaxial growth of CeO_2 on Si substrates and of material growth and electrical performance of the films in MOS structures and correlation of these properties to the growth conditions and structural properties.

The following sections introduce each topic, detail the experimental approaches, report the results to date and provide a discussion and a conclusion for each material. Each major section is self-contained with its own figures, tables and references.

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II. Surface Cleaning and Oxide Removal from 6H-SiC Wafers and Epitaxial Layers

A. Introduction

In order to continue development and find applications for silicon carbide as a semiconducting material, the methods used to obtain clean stoichiometric SiC surfaces must also be continually refined. Clean stoichiometric SiC surfaces are needed for the epitaxial growth of SiC and III-V nitrides via growth techniques such as ALE, MBE, CBE, OMVPE, etc. Clean, stoichiometric SiC surfaces are also necessary for developing ohmic and rectifying metal contacts to SiC. Fortunately, silicon carbide is closely related to silicon (the most dominant semiconducting material in the world) and, therefore, advantage can be taken of the immense research that has been performed to develop clean silicon surfaces.

One of the increasingly popular wet chemical treatments for obtaining clean silicon surfaces consists of a combination of ultraviolet exposure and HF etching. UV/HF cleaning has been found to produce clean (oxygen and hydrocarbon contamination free) silicon surfaces which are hydrogen terminated and stable against further contamination.[1] Naturally, one would expect that UV/HF cleaning could also be used for cleaning SiC. However, it is found that this procedure is not quite as effective in removing oxygen from the (0001) 6H-SiC surface as it is for the Si (111) surface as shown in Fig. 1. The amount of oxygen left on the SiC surface after HF dipping is quite large in comparison to the amount of oxygen left on the silicon surface. This difference in unremoved oxygen from the two surfaces perhaps could be due to the differences in the step densities between the two surfaces. It is generally believed that oxygen at a step on silicon or a silicon terminated SiC surface is much more difficult to remove. Recent STM images of both on and off axis SiC surfaces indicate that the step density for both of these surfaces is quite high.[2] Therefore, one would expect to see more unetched oxygen on a SiC surface after HF dipping as compared to a silicon surface. However, until SiC wafer manufacturing can reduce the step density, one must find some other procedure for further removing oxygen from the SiC surface.

One common way to remove oxygen from a semiconducting surface is to simply physically remove it via sputtering. Ar^+ ion sputtering has been used by many to remove oxygen from silicon carbide surfaces, but high temperature annealing afterward is required to remove the surface disorder/damage produced by the sputtering.[3,4] Ideally, one would like to remove the oxygen without physically damaging the silicon carbide surface. Chemical routes, therefore, are of more interest and here again silicon carbide researchers have taken advantage of research done on silicon.

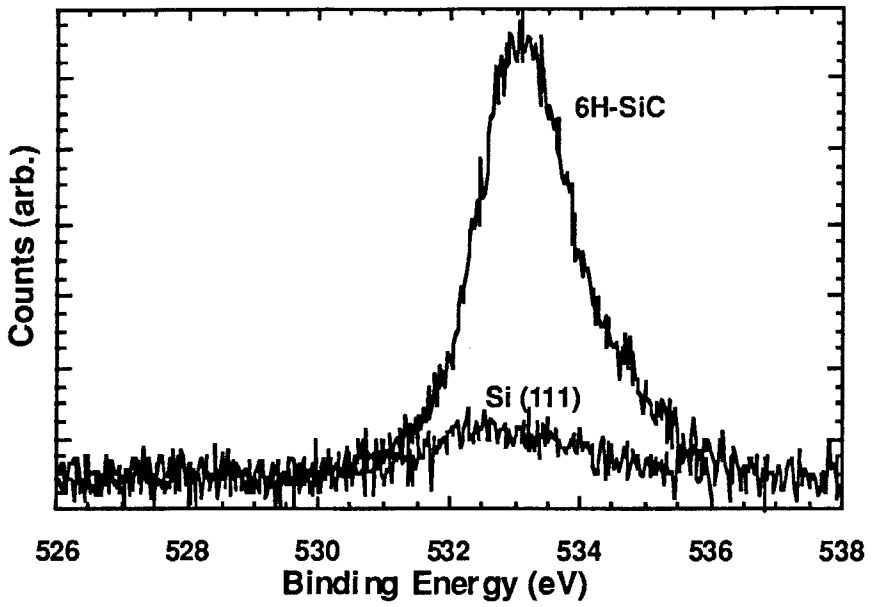


Figure 1. XPS spectrum of O 1s peak from Si (111) and (0001) Si face 6H-SiC surfaces after dipping a 10% HF solution for 10 min.

In the case of silicon, Wright and Kroemer showed that nonvolatile silicon dioxide (SiO_2) on silicon could be reduced to volatile silicon monoxide (SiO) by heating the silicon to 800°C and exposing it to a Ga flux. The Ga reduces the oxide via the following reactions:

$$SiO_2 + 4Ga = Si + 2Ga_2O,$$
$$SiO_2 + 2Ga = SiO + Ga_2O.[5]$$

The vapor pressures of both SiO and Ga_2O are sufficiently high at 800°C that they easily evaporate and are pumped away. The vapor pressure of gallium is also sufficiently high that any excess gallium adsorbed on the silicon surface is easily desorbed and evaporated away. This procedure was put to use by Kaplan *et al* for SiC and found to give similar results.[6] Unfortunately, the removal of silicon from a silicon carbide surface via SiO desorption leaves behind excess carbon which can result in graphite formation at the surface. Therefore, Kaplan replaced Ga with a flux of Si which also reduces SiO_2 to SiO but also simultaneously replenishes the SiC surface with silicon as the oxide is removed in the form of SiO.[7] Recently, Kern *et al.*, have found that by pre-exposing a 6H-SiC wafer to disilane (Si_2H_6) prior to epitaxial SiC growth via GS-MBE the amount of oxygen at the wafer epilayer interface can be reduced and eliminated as evidenced by SIMS analysis.[8]

The objective of this research is to conduct a detailed surface analysis of oxygen removal from 6H-SiC wafers/epilayers via high temperature annealing in a silane flux. A battery of surface analytical techniques was used to characterize the surfaces including: Auger electron

spectroscopy (AES), low energy electron diffraction (LEED), electron energy loss spectroscopy (EELS), ultra-violet photoelectron spectroscopy (UPS), and x-ray photoelectron spectroscopy (XPS).

B. Experimental Procedure

NCSU Integrated Surface Science Facility. All experiments were conducted in the NCSU Integrated Surface Science Facility which has been described in detail in previous reports. Briefly, this integrated surface science system consists of several independent UHV (ultra-high vacuum) systems connected to one another via a 36 ft. UHV sample transfer line independently pumped by two CTI cryopumps. To date, this integrated UHV system incorporates the following: a hydrogen plasma cleaning chamber, an ASTEX diamond deposition system, a chamber for *in-situ* Raman spectroscopy, an angle resolved-ultraviolet photoelectron spectroscopy (AR-UPS) system, a Si-Ge molecular beam epitaxy (MBE) system, an analysis station for performing Auger electron spectroscopy (AES) and low energy electron diffraction (LEED), an atomic layer epitaxy (ALE) system, and a x-ray photoelectron spectroscopy (XPS) system. The experiments discussed in this report employ the XPS, ALE, AES/LEED, and AR-UPS systems.

ALE System. The ALE system employed in this research has not been significantly modified since the last reporting period and a detailed description of the system can be found in the June 1994 Semiannual ALE report. However, one significant addition was made to the ALE system which was the installation of a silane (SiH_4) doser. The silane doser is of the same design as the hexachlorodisilane and ethylene/acetylene dosers used in previous experiments. Briefly, the ALE system has a base pressure of 3×10^{-10} Torr and is pumped by a 400 l/s turbo pump (Leybold), a 500 l/s ion pump (Varian), and a water cooled Ti sublimator (Varian). The ALE system incorporates two gas dosers for the carbon and silicon ALE precursors (ethylene and hexachlorodisilane), a Hiden Analytical RGA for residual gas analysis, and a sample heating stage capable of temperatures >1200°C.

XPS System. XPS experiments were performed in a stainless steel UHV chamber equipped with a VG XR3E2 x-ray source and VG CLAM II hemispherical electron energy analyzer. The base pressure in this system is 1×10^{-10} Torr and is pumped by a 220 l/s ion pump (Varian). All XPS spectrums reported here were taken using Al K alpha radiation (1486.6 eV). Calibration of the binding energy scale for all scans was achieved by periodically taking scans of the Au $4f^{7/2}$ and Cu $2p^{3/2}$ peaks from standards and correcting for the discrepancies in the measured and known values of these two peaks (83.98 eV and 932.67 eV, respectively). Curve fitting of the data was performed using the software package GRAMS 386. A combination Gaussian-Lorentzian curve shape with a linear background was found to best represent the data.

AES/LEED/EELS. The Auger electron spectrometer (Perkin Elmer 10-155 CMA) and the low energy electron diffraction optics (Perkin-Elmer) were mounted on a cross off the transfer line and pumped through the line. In AES analysis, a 3 keV, 1mA beam was used and the Auger spectrum was collected in the undifferentiated mode and then numerically differentiated. In EELS and LEED a 80 eV, 1mA beam was used.

Substrate and Wafer Cleaning. In these experiments, roughly 1cm×1cm fragments of n-type (N_d=1×$10^{18}$$cm^{-3}$), Si face 6H-SiC (0001) wafers obtained from Cree Research were used as substrates. These wafers came with a one micron epi layer (N_d = 5×10^{17}) grown by Cree. The back sides of these wafers were sputtered coated with platinum to increase the heating efficiency of the SiC as SiC is partially transparent to the infrared radiation from the sample heater. Later experiments used tungsten on the back sides of the wafers as platinum was found to react with the back of the wafer forming Pt-silicides which evaporated at the temperatures used in these experiments. Also in experiments where these wafers were annealed at high temperatures (>1000°C) for long periods of time (2hr), platinum was discovered at the surface. This is presumably due to diffusion of the platinum to the surface through the micro pipes in the SiC wafers.

Prior to insertion into vacuum, all wafers where given a standard 10 minute dip in a buffered 10% HF solution to remove the native oxide from the SiC surface. After HF dipping, the SiC crystals where mounted to a ring shaped molybdenum sample holder using tantalum wire. Once in vacuum, the SiC crystals were inserted into the ALE system where they were outgassed at 250°C, 450°C, and 700°C for 30 min. prior to any silane cleaning. All samples treated in this manner exhibited (1×1) LEED patterns.

Gases and Gas Dosing. The silane used in these experiments was semiconductor purity silane purchased from Matheson. Mass spectroscopic analysis of the as-received silane using the Hiden RGA revealed that the primary resolvable impurities were H_2O, CO_2, and Si_2H_6 in concentrations of 180 ppm, 31 ppm, and 170 ppm respectively. Impurities such as CO and O_2 were expected but difficult to resolve due to overlap with the silane cracking pattern. However, we estimate that the level of these impurities were at least below 600 ppm or better. No further purification was deemed necessary and the silane was used in this purity. Dosing of the silane was handled in a manner analogous to which the hexachlorodisilane and ethylene were handled in previous experiments as described in previous reports.

C. Results

Temperature Dependence of SiH_4 Cleaning. Figure 2 shows several AES scans taken from a 6H-SiC (0001) surface after exposure to SiH_4 at various temperatures. Spectrum (a) is from a sample exposed to 200£ (£ = Langmuir = 10^{-6} Torr/second) SiH_4 at 750°C and is also

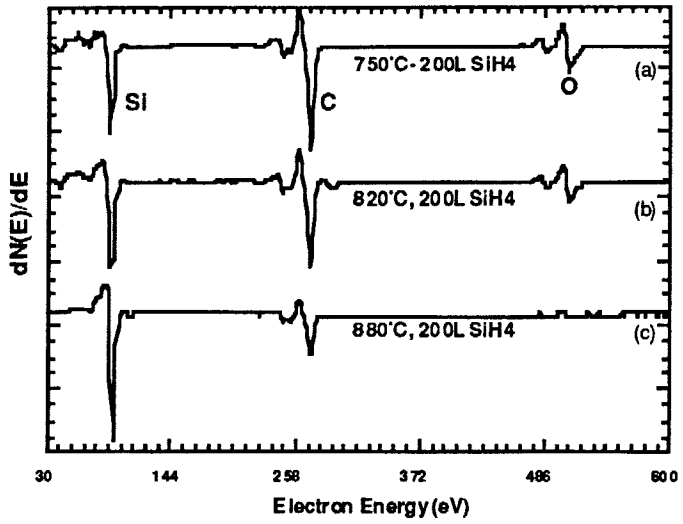
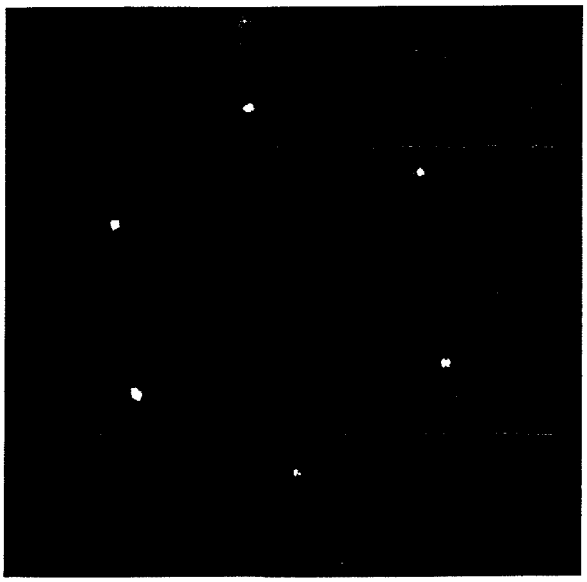


Figure 2. AES spectrum of 6H-SiC Si face (0001) surface after dipping in 10% HF-10 min., degassing at 700°C-30 min. and (a) 200£ SiH_4-750°C, (b) 200£ SiH_4-820°C, and (c) 200£ SiH_4-880°C

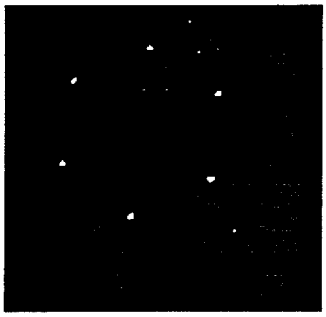
representative of the SiC wafer after HF dipping and outgassing. As can be seen, there still is quite a substantial amount of oxygen left on the surface after outgassing and silane exposure at 750°C. A second 200£ exposure of silane at 820°C (Fig. 2b) shows a significant reduction in oxygen but not complete removal. By increasing the temperature to 880°C (Fig 2c), a third 200£ SiH_4 exposure is sufficient to remove all surface oxide in a timely fashion. It is important here to point out that there is a 2:1 difference in sensitivity for Si to C in AES. Due to this difference, a stoichiometric SiC surface will appear to be Si rich when in fact it is not. The Si:C ratio in the AES spectrum in Figure 2c is 3:1 indicating that extra silicon has been deposited on the SiC surface. If the SiC is given too large a silane exposure at 900°C, excess silicon coverages can start to approach monolayer levels and a silicon bilayer can be formed on the SiC surface. The formation of such a silicon bilayer can lead to changes in the silicon carbide surface structure as witnessed in LEED.

SiC Surface Structures. Figure 3 shows the three LEED patterns witnessed in these experiments. Figure 3a. shows the (1×1) LEED pattern which is typically found for SiC wafers after HF dipping and after oxide removal via silane annealing. The quality of the (1×1) pattern obtained after HF dipping is usually sample dependent with diffuse spots and a substantial background. After SiH_4 cleaning, the (1×1) pattern becomes very sharp with sharp spots and no background. In cases where the SiC is exposed to too much silane, a silicon bilayer can be deposited on the silicon carbide. The formation of a silicon bilayer is easily observed by a change in the LEED pattern from (1×1) to (3×3). Figure 3b shows the (3×3) LEED pattern obtained and the following section will show XPS data which illustrates that a silicon bilayer has formed. The (3×3) pattern can be easily reconverted to the (1×1) pattern by simply annealing in vacuum at 1000°C for approximately 10 minutes.



(a)

(b)



(c)

Figure 3. LEED patterns from (0001) 6H-SiC surfaces cleaned via high temperature annealing in SiH_4. (a) (1×1), (b) (3×3), and (c) ($\sqrt{3}\times\sqrt{3}$) reconstructions.

A third SiC surface reconstruction, ($\sqrt{3}\times\sqrt{3}$)R30°, was obtained in these experiments and is shown in Fig. 3c. This reconstruction was obtained by annealing the oxide free (1×1) surface in vacuum at 1000°C for approximately 15 minutes. XPS and EELS (not shown) analysis

performed in these experiments indicates that the ($\sqrt{3}\times\sqrt{3}$)R30° reconstructed surface is silicon deficient in comparison to the other two surfaces and that this surface reconstruction signals the beginning of graphite formation. It has been found that the ($\sqrt{3}\times\sqrt{3}$)R30° surface can be reverted back to the (1×1) surface by simply re-exposing it to silane at 900°C.

XPS analysis of (1×1), (3×3), and ($\sqrt{3}\times\sqrt{3}$)R30° Surfaces. Figure 4 shows XPS spectrums of the Si 2p peak from the (1×1), (3×3), and ($\sqrt{3}\times\sqrt{3}$) reconstructed 6H-SiC surfaces. The lower binding energy tails on the Si 2p peak for these three surfaces in Fig. 3 clearly illustrates the differences in these surfaces. For the (3×3) surface, one can clearly see the formation of a second peak at ≈ 99.5 eV on the lower binding energy side of the SiC Si 2p peak (≈ 101.6 eV). The binding energy value of 99.5 eV corresponds to Si-Si bonding and indicates the formation of an extra monolayer of silicon on the silicon terminated SiC surface. Further data analysis (via peak integration) of the (3×3) Si 2p XPS spectrum indicates that a partial bilayer of silicon has formed on the SiC surface.

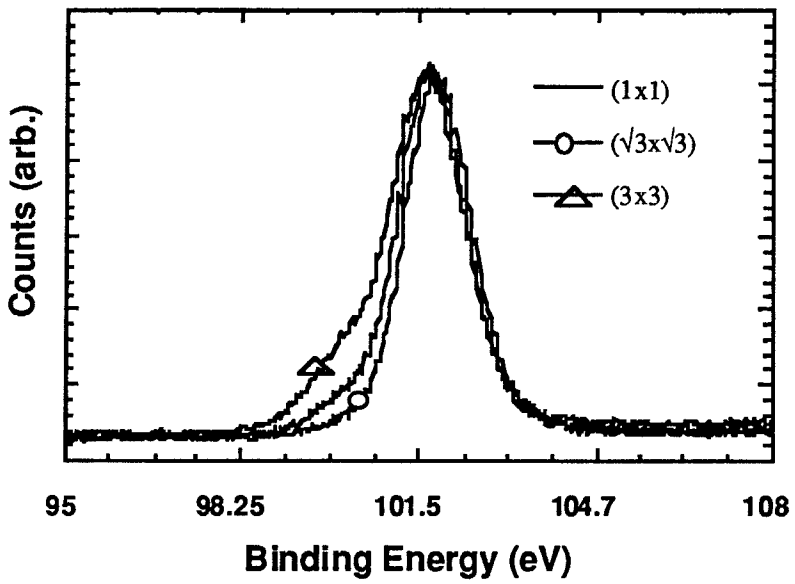


Figure 4. XPS spectrum of Si 2p peak from SiH_4 cleaned 6H-SiC (0001) surfaces with (1×1), ($\sqrt{3}\times\sqrt{3}$), and (3×3) reconstructions.

In the case of the (1×1) and ($\sqrt{3}\times\sqrt{3}$)R30° surfaces, XPS does not show as large a second Si 2p peak at 99.5 eV as the (3×3) surface. Comparing the low binding energy tail for the (1×1) surface to the tail for the ($\sqrt{3}\times\sqrt{3}$)R30° surface, one can see that the ($\sqrt{3}\times\sqrt{3}$)R30° surface is comparatively devoid of any excess silicon. XPS of the C 1s peak from the ($\sqrt{3}\times\sqrt{3}$)R30° surface shows a "graphitic" hump on the lower binding energy side of this peak. With EELS also indicating the presence of graphite on the ($\sqrt{3}\times\sqrt{3}$)R30°, it seems logical to

conclude that the ($\sqrt{3}\times\sqrt{3}$)R30° is a slightly silicon deficient surface and that the (1×1) surface represents the ideal stoichiometric surface. Although in reality the (1×1) surface can exhibit a range of stoichiometries.

D. Discussion

The existence of the three SiC surface reconstructions witnessed in these experiments can serve as a guide to indirectly measure the surface cleanliness of 6H and 4H (0001) SiC wafers and epitaxial layers. Most growth systems (MBE, CBE, CVD, ALE, OMVPE, etc.) do not have surface analytical techniques such as AES, XPS, EELS, LEED, and UPS available to characterize the cleanliness of their substrates prior to growth. However, in the case of MBE and CBE, RHEED (reflection high energy electron diffraction) is a common analytical tool found on such systems and it can be used to dynamically monitor oxide removal from SiC surfaces during a high temperature silane clean. One can simply expose a SiC surface to silane (or disilane) at around 900-1000°C and wait until RHEED shows a change from a (1×1) pattern to a (3×3) pattern. Subsequently, the silicon source can be shut off and growth started on either a clean oxide free (3×3) surface or (1×1) surface after a short anneal. This procedure is already in use by Kern and has been found to improve GS-MBE epitaxial growth of SiC.[8] In the case of non-UHV growth techniques such CVD, OMVPE, etc., techniques such as surface photo adsorption (SPA) and reflection difference spectroscopy (RDS) can probably be used with equal success. SPA and RDS have been shown to be extremely useful in monitoring layer by layer growth such as in ALE.

The XPS data for the (3×3) SiC reconstruction is an excellent agreement with the results of Kaplan who based on EELS data argued that the (3×3) surface is due to the formation of a bilayer of excess silicon on the SiC surface.[7] To the authors knowledge, the XPS data shown here is the first direct experimental evidence clearly indicating that the (3×3) SiC (0001) surface reconstruction is due to a silicon bilayer. However, the work by Kaplan indicates that the (1×1) surface is silicon deficient compared to the ($\sqrt{3}\times\sqrt{3}$)R30° surface and that the ($\sqrt{3}\times\sqrt{3}$)R30° surface reconstruction is due to the presence of a fractional monolayer of excess silicon. The XPS data shown here does not support this. The XPS shown here does not reveal any excess silicon on the ($\sqrt{3}\times\sqrt{3}$)R30° surface and shows the (1×1) surface to be more silicon rich. This suggests a possible need for a different explanation for the reconstruction.

UPS was also performed on the (1×1) and ($\sqrt{3}\times\sqrt{3}$)R30° surfaces during the course of these experiments. This data will be reported and discussed in a separate ONR report. However, it should be mentioned that the (1×1) surface appeared to exhibit a surface state in the UPS spectrum whereas the ($\sqrt{3}\times\sqrt{3}$)R30° surface did not.

Finally, two recent papers by researchers in Russia indicate the possibility of e^- beam cleaning SiC surfaces at lower temperatures than those used here.[10,11] These researchers

used a 640 eV electron beam with a flux of 5×10^{17} e^-/cm^2 and apparently achieved oxide-free surfaces. If true, e^- beam cleaning could become a viable alternative to the silane cleaning described here.

E. Conclusions

Dipping off-axis Si terminated (0001) 6H-SiC surfaces in 10% HF does not remove all of the surface oxide from the SiC surface. By exposing SiC surfaces to 200-400£ silane at 900°C, one can remove all of the surface oxide and generate a clean, stoichiometric, (1×1) SiC surface. SiH_4 exposures at 900°C greater than 500£ can generate a silicon rich surface with an extra bilayer of Si which is characterized by a (3x3) LEED pattern. Annealing a (3×3) (0001) 6H-SiC surface in vacuum at 1000°C can restore the (1×1) surface. Continued annealing at 1000°C can lead to a $(\sqrt{3}\times\sqrt{3})R30°$ surface which indicates the beginning of graphite formation. Exposure of a $(\sqrt{3}\times\sqrt{3})R30°$ surface to SiH_4 at 900°C can regenerate the (1×1) surface.

F. Future Research Plans and Goals

1. Investigate differences in the effectiveness of removing oxygen from both on and off axis 6H-SiC using a 10% HF dip.
2. Comparative study of the effectiveness of SiH_4 cleaning for on and off axis Si face (0001) 6H-SiC.
3. Comparative study of the effect of high temperature silane exposure to C face and Si face 6H-SiC, and Si (111).
4. Investigate potential of using a 640 eV electron beam (5×10^{17} e^-/cm^2s) to clean SiC surfaces.
5. Further investigation of SiC surface state and (3×3) reconstruction using UPS.

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III. Atomic Layer Epitaxy of Silicon Carbide Films and the Fabrication and Testing of Heterojunction Bipolar Transistor Structures

A. Introduction

Beta-SiC has tremendous potential in the construction of semiconductor devices. Conventional ratings for comparing the characteristics of semiconductor materials rank β-SiC far above Si in many applications. Johnson's figure of merit rates the maximum performance to be expected of a semiconductor material in discrete bipolar transistors[1], giving β-SiC a rating 33.9 times higher than Si, largely due to an E_B(β-SiC) that is 13.3 times higher than that of Si. Keyes' rating, which assesses a materials suitability for high density integrated circuit applications[2] rates β-SiC 5.82 times higher than Si due to the superior value of σ_T(β-SiC) that is 1.22 times that of copper at room temperature[3]. Although these ratings for β-SiC demonstrate that both discrete devices and integrated circuitry employing β-SiC components should attain levels of performance unachievable with device technologies based solely on Si, relatively few β-SiC containing devices have been produced[4,5].

A significant barrier to the widespread exploitation of the capabilities of β-SiC is the lack of an advanced β-SiC processing infrastructure. The most expeditious route to devices accessing the performance increases possible with β-SiC would be the development of a thin-film deposition technique to allow the integration of β-SiC into the existing Si device fabrication infrastructure. Currently, β-SiC films may be deposited on Si(100) wafers in a two-step process where the wafer surface is converted to β-SiC via exposure to a hydrocarbon gas prior to high temperature deposition by chemical vapor deposition[6]. This process is poorly suited for integration into the existing sub-micron Si process routes. However, as shown in the previous report (June, 1994), atomic layer epitaxy offers the ability to deposit monocrystalline β-SiC films on Si(100) substrates at low temperatures without the carbonizing pretreatment and may serve as a vehicle to facilitate the use of β-SiC in selected devices.

The objective of this research is to extend the state-of-the-art regarding SiC thin film deposition and application via the employment of ALE to deposit β-SiC films on select substrates. During this reporting period, work has continued toward the fabrication of trenched heterojunction bipolar transistors (HBTs) employing a wide bandgap β-SiC emitter. The first batch of transistors has been completely processed. The following sections describe the fabrication steps followed in this work and the results of characterization of the resultant devices via electrical measurements and scanning electron microscopy (SEM).

B. Experimental Procedure

ALE Reactor. The ALE reactor employed in this research has not been significantly modified since it was described in detail in a previous report (June, 1993). To prevent mixing

of process gases, flowing Ar "curtains" divide the reactor into 4 radial quadrants through which isolated fluxes of Si_2H_6, C_2H_4, NH_3 and triethylaluminum ($Al(C_2H_5)_3$) may flow. The quadrant containing NH_3 also contains a W filament that may be heated to produce atomic hydrogen or to crack NH_3 depending on gas flow conditions. During deposition, heated samples can be rotated alternately between quadrants and exposed to the species present to form films in a layer-by-layer process. Due to the construction of the reactor, SiC films can be deposited and doped n- and p-type with N and Al, respectively.

Fabrication of Trenched HBTs The six-level mask system designed to produce HBTs was described in detail in the previous report (June, 1994). Each die contained four transistors: a planar HBT, two HBTs in trench structures and one HBT with a corrugated or "waffle iron" structure. The geometry of the latter devices were engineered to exploit the high degree of conformality possible with layer-by-layer deposited SiC films. The procedures followed in producing the devices are explained in the two following sets of figures and tables. Figs.1 and 2 correspond to Tables I and II, respectively.

Due to the complexity of the HBT fabrication process and the number frequently repeated steps, several secondary steps have been omitted or simplified in this outline. A full review of current integrated circuit fabrication technology is beyond the scope of this document, and the reader is referred to several publications which survey this field[7-10].

Deposition. SiC films were deposited on the partially processed wafers as described in step 14 of Table I. Four samples: HBT1-HBT4 were processed under the conditions listed in Tables III and IV. Prior to etching of the SiC to define the emitters, the thickness of each film was determined via cross-sectional SEM observation.

Ni Contacts (N-Type SiC). Ni contacts were sputtered onto the films using a photolithography lift-off technique. The specifics of the lift-off technique were discussed in detail in the previous report (June, 1994). Sputtering conditions were power = 100 watts 13.56 MHz R.F. and 20 mTorr Ar ambient. Deposition rate was ≈ 2000 Å/Hr. Contacts were then annealed in a Heatpulse rapid thermal annealer (RTA) with an Ar ambient at 1000° C for 20 sec.

Al contacts (P-type Si). Al contacts were vacuum evaporated from pure Al shot (99.9999% pure). The deposited Al film was subsequently processed using conventional microelectronic fabrication techniques.

Electrical characterization. I-V and I_C vs. V_{EC} characterization was performed with a Hewlett Packard 4145A Semiconductor Parameter Analyzer. Ambient light was found to have a significant effect on measured factors, therefore, all data was collected under dark conditions. Typical contact points are indicated in Fig. 3. Emitter and base connections for testing were made with W probes while the collector contact was made with a large area silver paint electrode on the wafer backside after grinding.

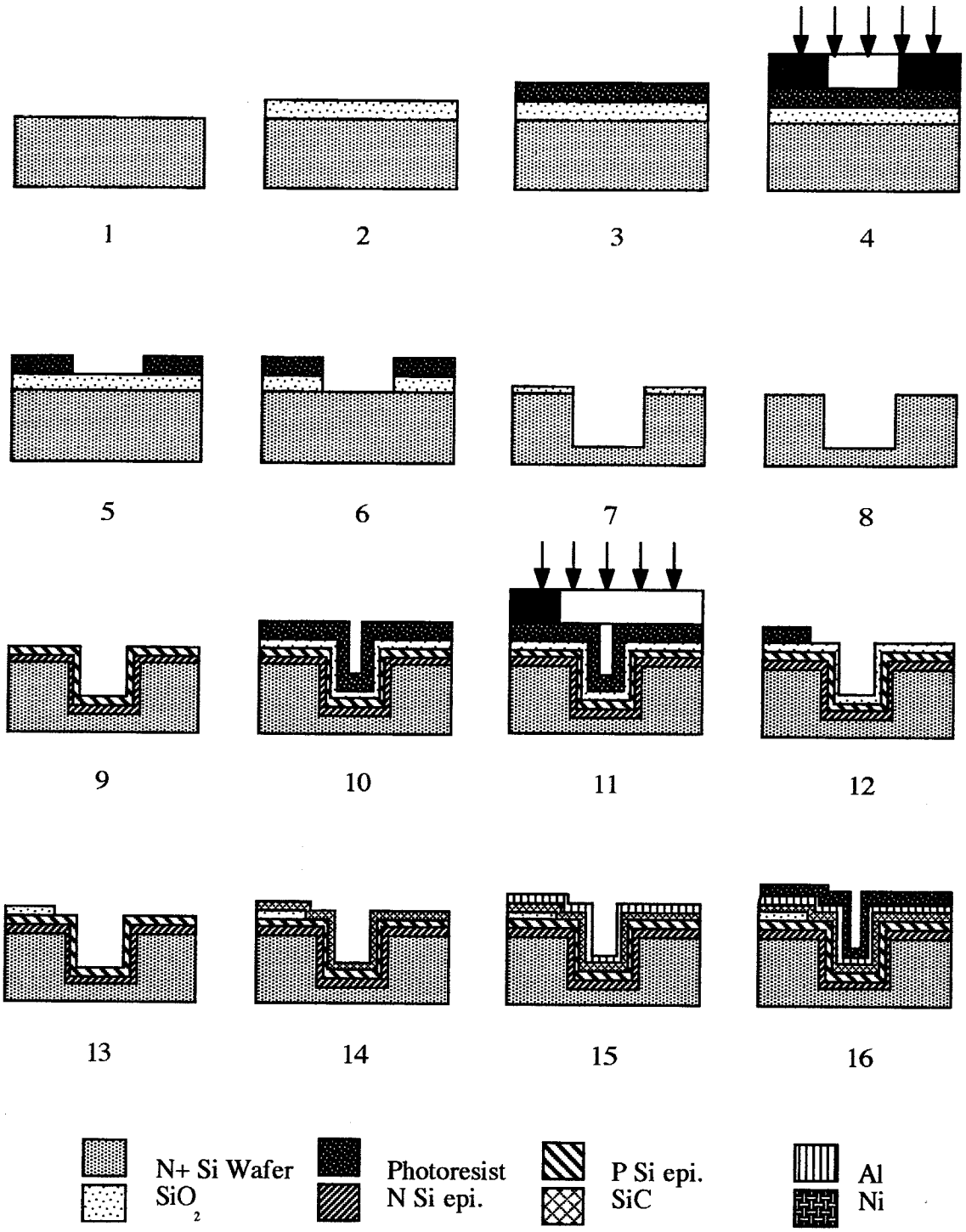


Figure 1. Part I of fabrication process for HBTs. Details explained in Table I.

Table I. Part I of Fabrication Process for HBTs. Refer to Fig. 1

Step	Procedure
1	RCA clean N^+ Si(100) wafers.
2	Grow thermal SiO_2 layer.
3	Spin on HMDS primer and JSR-1X700 positive photoresist (PR).
4	Expose PR for 20 s. using mask HBT-1 (Trench etch).
5	Develop PR in Microposit developer for 60 s. Bake for 5 min. at 120°C after developing.
6	Immerse wafers in 10% HF for 700 s. to remove exposed SiO_2.
7	RIE in 5:6 atmosphere of SF_6:O_2 at 30 mTorr for 40 min. to etch exposed Si.
8	Immerse wafers in 10% HF for 3 min. to remove remaining SiO_2.
9	N^- and P epitaxial Si deposited by APCVD using trichlorosilane ($SiCl_3H$) at 1200°C. N^- layer 1.0 μm thick, P layer 1.5 μm thick.
10	Deposit ≈1000 Å of low temperature SiO_2 at 410°C and 0.65 Torr using a 1:2 atmosphere of diethylsilane ($Si(C_2H_5)_2H_2$) and O_2 for 13 minutes. Apply HMDS primer and JSR-1X700 PR.
11	Expose PR for 20 s. using mask HBT-2 (Pad isolation).
12	Develop PR in Microposit developer for 60 s. Bake for 5 min. at 120°C after developing.
13	Immerse wafers in 10% HF for 700 s. to remove exposed SiO_2.
14	RCA clean wafers as in Table 7.2, except limit HF immersion to 8 s. Deposit SiC film.
15	Evaporate 3000 Å Al to serve as emitter etch pattern.
16	Apply HMDS primer and JSR-1X700 PR.

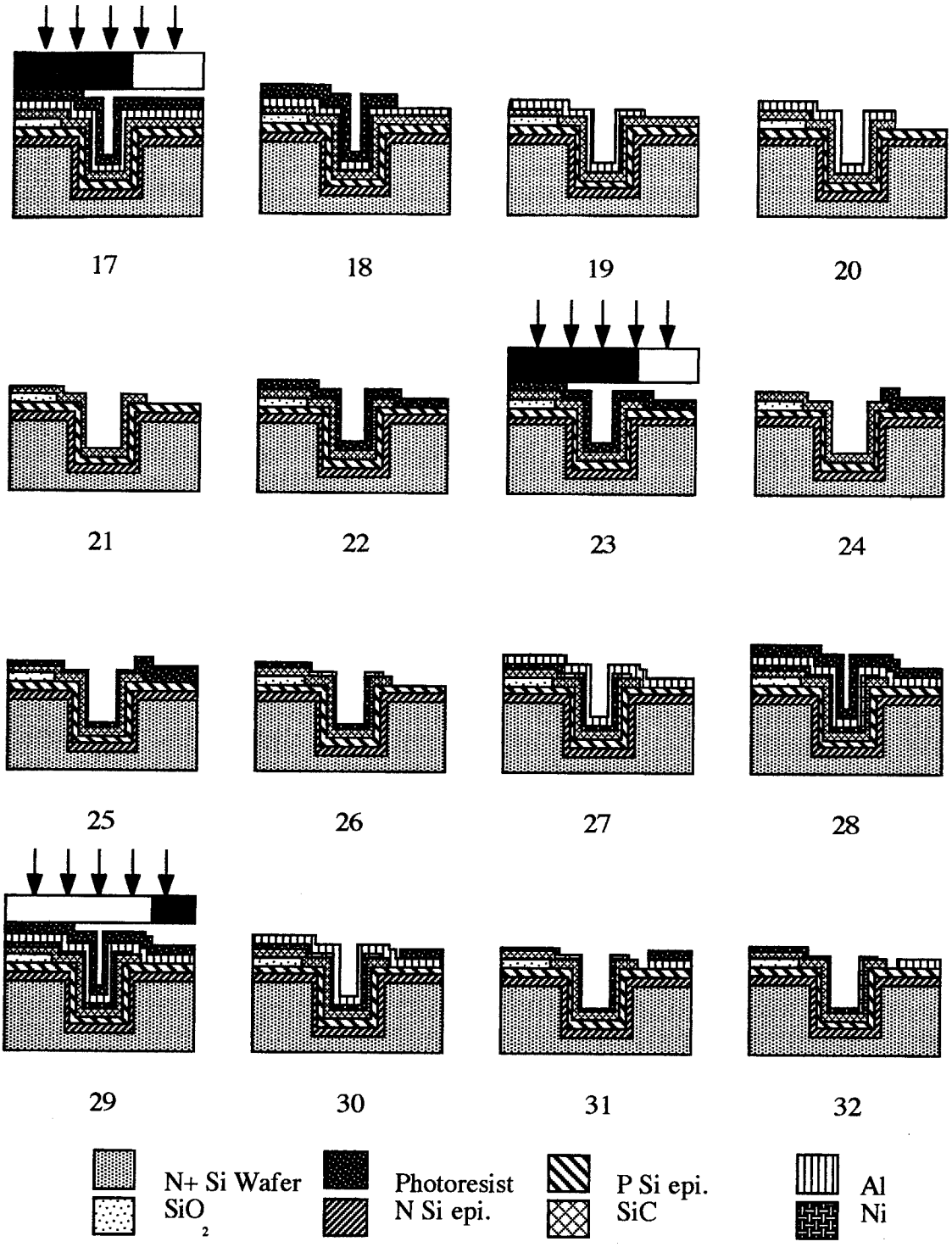


Figure 2. Part II of fabrication process for HBTs. Details explained in Table II.

Table II. Part 2 of Fabrication Process for HBTs. Refer to Fig. 2

Step	Procedure
17	Expose PR for 8 s. using mask HBT-3 (Emitter etch).
18	Develop PR in Microposit developer for 60 s. Bake for 30 min. at 120°C after developing.
19	Immerse wafers in Transetch® to remove exposed Al. Visible "flash" when all exposed Al is removed. Care required to prevent over-etching. Remove PR with Accustrip®.
20	RIE in NF_3 / CHF_3 to remove exposed SiC.
21	Immerse wafers in Transetch® to remove remaining Al.
22	Apply HMDS primer and Imidizol® treated JSR-1X700 PR.
23	Expose PR for 20 s. using mask HBT-4 (Emitter contact).
24	Bake wafers 30 min. @ 90°C, flood expose on aligner 60 s., develop in Microposit® developer 60 s.
25	Sputter ≈ 1000Å Ni onto wafers.
26	Dissolve remaining PR in Accustrip® to "lift-off" undesired Ni.
27	Evaporate ≈ 2000 Å Al onto wafers.
28	Apply HMDS primer and JSR-1X700 PR.
29	Expose PR for 8 s. using mask HBT-5 (Base contact).
30	Develop PR in Microposit developer for 60 s. Bake for 30 min. at 120°C after developing.
31	Immerse wafers in Transetch® to remove exposed Al. Visible "flash" when all exposed Al is removed. Care required to prevent over-etching.
32	Remove PR with Accustrip®. Mesa isolation process not depicted, repeat steps 3–5 with mask HBT-6 (Mesa isolation) and immerse in $H(NO_3)$:HF:H_2O 1:1:2 solution for 20 s. Remove PR with Accustrip®.

Table III. SiC Deposition Conditions for Depositing Emitters for HBTs

Process parameter	HBT 1	HBT 2	HBT 3
Sample temperature	870° C	870° C	850° C
Si_2H_6 flow/ H_2 carrier	step 1: 0.8 / 300 sccm step 2: 3 sccm	0.8 sccm/ 300 sccm	0.8 sccm/ 300 sccm
C_2H_4 flow/ H_2 carrier	step 1: 2 / 200 sccm step 2: 4 sccm	2 sccm/ 200 sccm	2 sccm/ 200 sccm
Ar curtain flow	step 1: 200 sccm step 2: 2 sccm	200 sccm	200 sccm
H_2 across filament	step 1: 100 sccm step 2: 2 sccm	100 sccm	100 sccm
Filament temperature	step 1: 1700°C step 2: unheated	1700° C	1700° C
Pressure	step 1: 1.5 Torr step 2: $\approx 10^{-3}$ Torr	1.5 torr	1.5 torr
Rotational Scheme	step1: rotate through Si_2H_6 and C_2H_4, wait under fil. 30 s. rpt 146 times. step 2: Si_2H_6 5 s., under H_2 30 s., C_2H_4 5 s., under H_2 5 s., rpt. 2085 times	rotate through Si_2H_6 and C_2H_4, wait under fil. 30 s. rpt 3750 times.	rotate through Si_2H_6 and C_2H_4, wait under fil. 30 s. rpt. 3412 times.
Film thickness	0.1 μm	0.714 μm	0.17 μm

Table IV. SiC deposition conditions for depositing emitters for HBTs

Process parameter	HBT 4	HBT 5	Etch standard
Sample temperature	850° C	890° C	850° C
Si_2H_6 flow/ H_2 carrier	1.5 / 300 sccm	1.5 sccm	1.5 / 300 sccm
C_2H_4 flow/ H_2 carrier	2.5 / 200 sccm	3 sccm	2.5 / 200 sccm
Ar curtain flow	200 sccm	0 sccm	200 sccm
H_2 across filament	100 sccm	0 sccm	100 sccm
Filament temperature	unheated	unheated	unheated
Pressure	1.5 Torr	$\approx 10^{-3}$ torr	1.5 Torr
Rotational scheme	Si_2H_6 for 1 s., H_2 for 10 s., C_2H_4 for 2 s. H_2 for 2 s., rpt. 9200 times.	Si_2H_6 for 5 s., H_2 for 30 s., C_2H_4 for 5 s. H_2 for 5 s., rpt. 4900 times.	Si_2H_6 for 2 s., H_2 for 5 s., C_2H_4 for 3 s. H_2 for 2 s., rpt. 11287 times.
Film thickness	3.2 μm	1.77 μm	4.8 μm

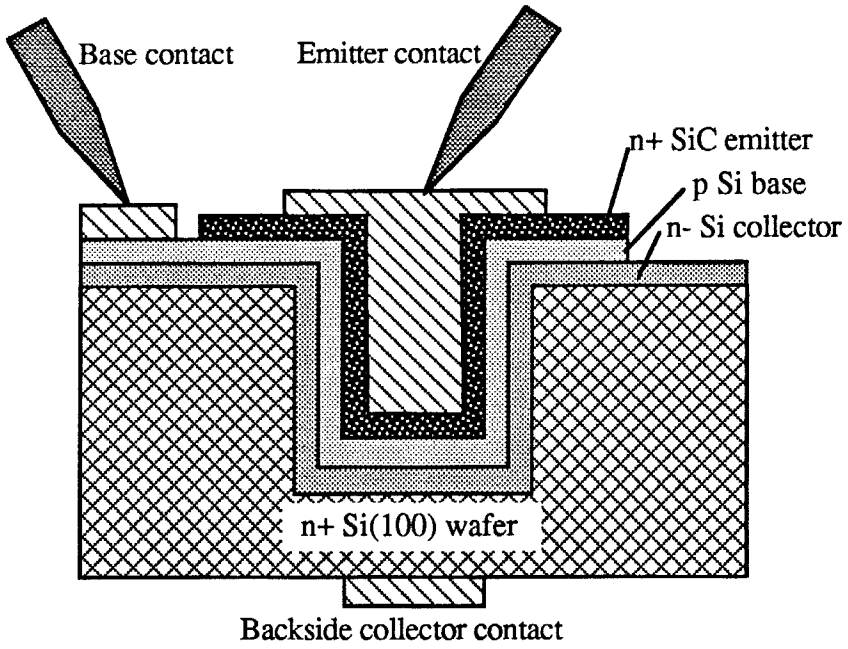


Figure 3. Testing contacts for electrical characterization of HBTs.

C. Results

The collector and base regions indicated in Fig. 3 were deposited by a commercial contractor. A spreading resistance profile of the deposited layers is presented in Fig. 4. Both the base region (p-type) and the collector region (lightly n-type) were much thicker than ordered. This is due to the complication of carrier migration during deposition. As these films were deposited at ≈1300°C, abrupt changes in carrier concentration are not possible due to the diffusion of donors and acceptors. As a consequence, thicker films are necessary to achieve a relatively constant dopant level.

Prior to analysis of the HBTs constructed in this period, a commercially available Si based NPN bipolar transistor (Archer® Cat. No. 276-1617) was examined as a reference. A typical plot of quasi-static performance is presented in Fig. 5. The gain of this transistor is indicated by the increases in the I_C (collector current) vs. V_{EC} (emitter-collector voltage) with steps in I_B (base current). As the curves are separated from each other by >10 μA, I_C increases quickly with increases in I_B. The ratio of I_C/I_B is the gain of the device.

Figure 6 shows a typical performance curve for most of the transistors produced in the first batch. These devices did not exhibit good transistor activity, but rather operated with a gain of 1. A variety of I_B step values and operating voltages were explored on all five wafers. Except for instances where the devices were physically damaged by testing at high voltages and currents, curves similar to the one pictured in Fig. 6 resulted.

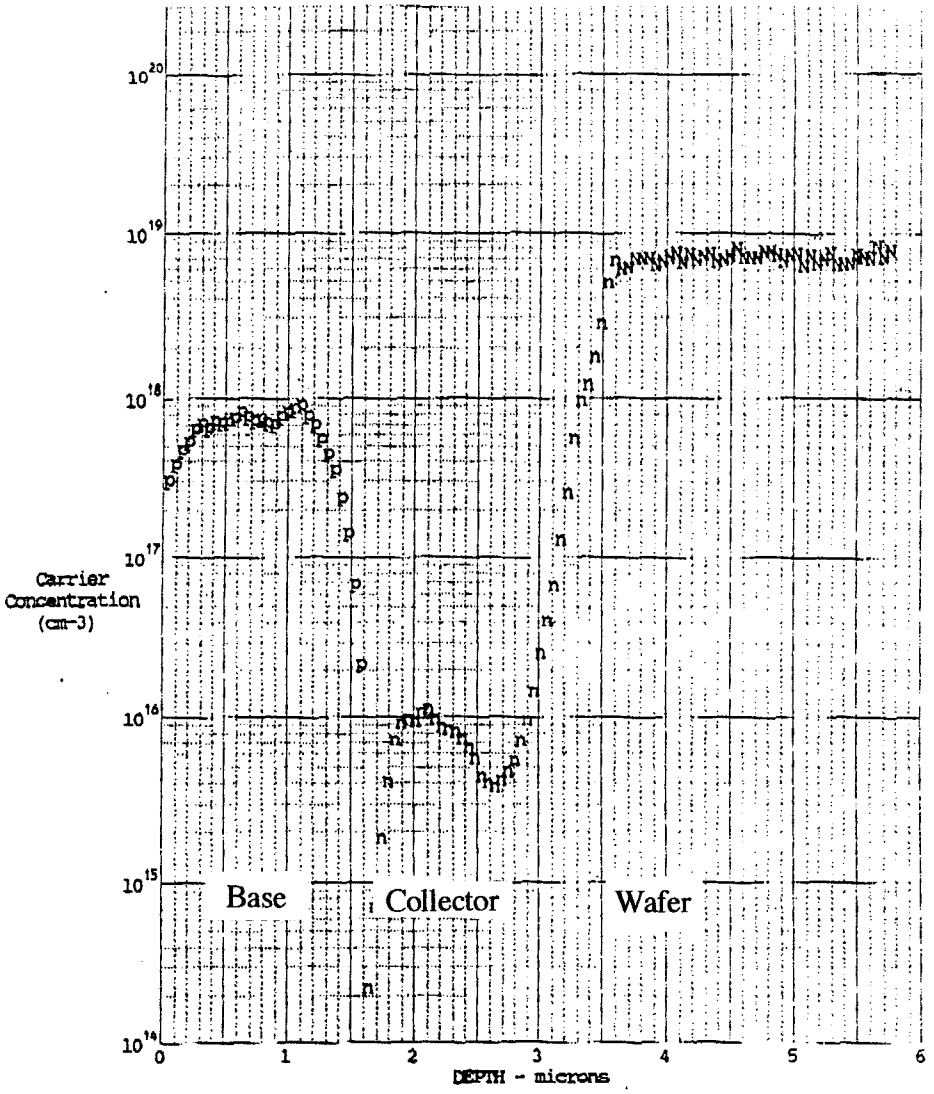


Figure 4. Spreading resistance profile of deposited layers.

I-V characterization of the emitter-base and the base-collector junctions was performed to determine the cause of the lack of performance. Anomalous readings were frequently collected on wafers HBT 2 through HBT 5 where there was no rectifying behavior at one or the other junction. In some instances, the base-collector junction appeared to behave ohmically while the emitter-base junction carried very little current in either bias condition. SEM analysis of these samples revealed that the SiC film was occasionally over-etched. This was particularly evident on wafer HBT 4 as shown in Figs. 7-9. These SEM images of that wafer concentrate on a planar transistor displayed at several magnification factors. In Fig. 7, the entire transistor is visible. As the magnification increases up to Fig. 9, the edge of the emitter becomes clearly visible. In Fig. 9, the Ni film for electrical contact is visible on the SiC. However there is marked over-etching of the Si, as indicated by the rough surface around the SiC and the "undercut" below the SiC.

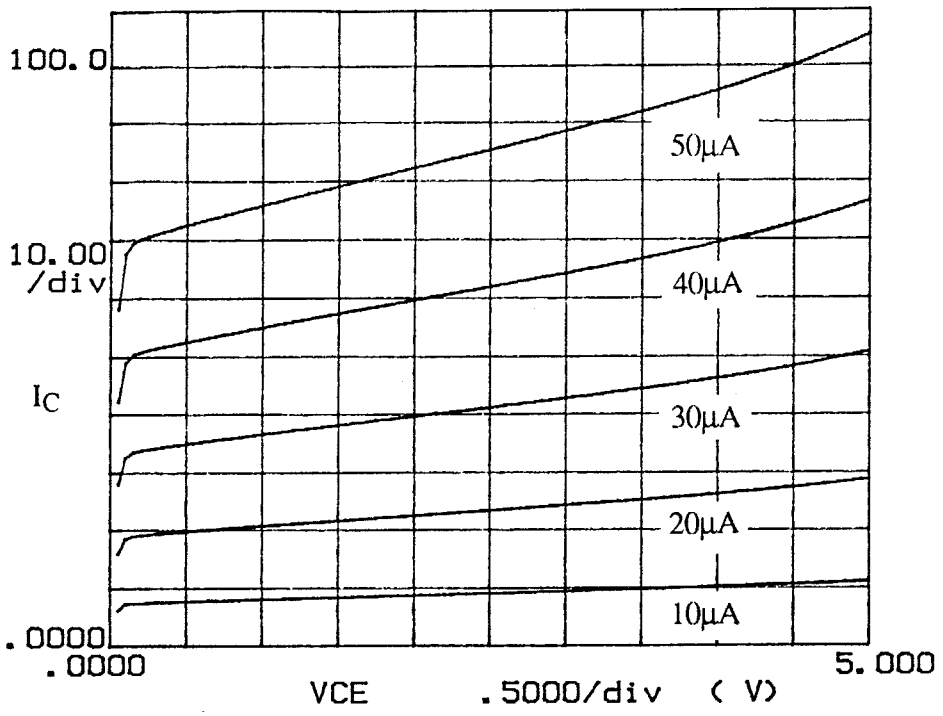


Figure 5. I_C vs. V_{EC} behavior of commercial Si NPN transistor at several I_B values.

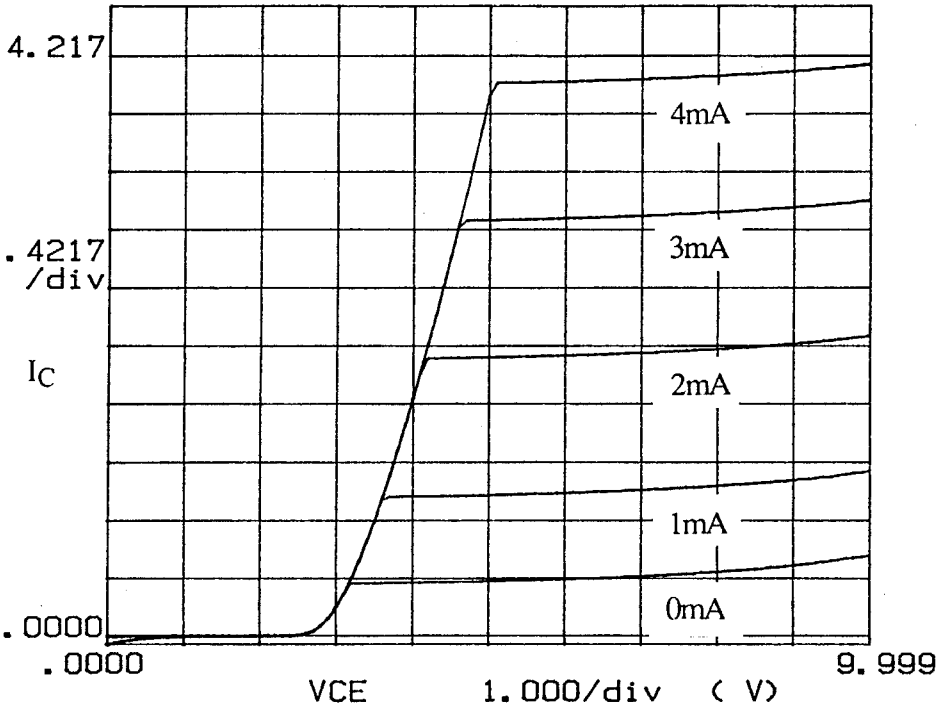
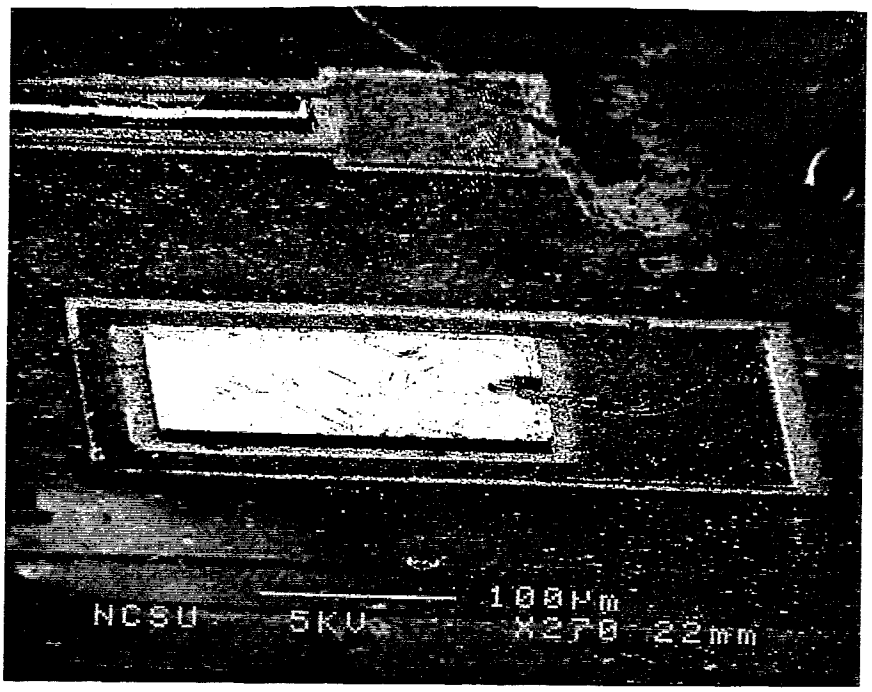


Figure 6. Typical I_C vs. V_{EC} behavior of constructed HBTs at several I_B values.



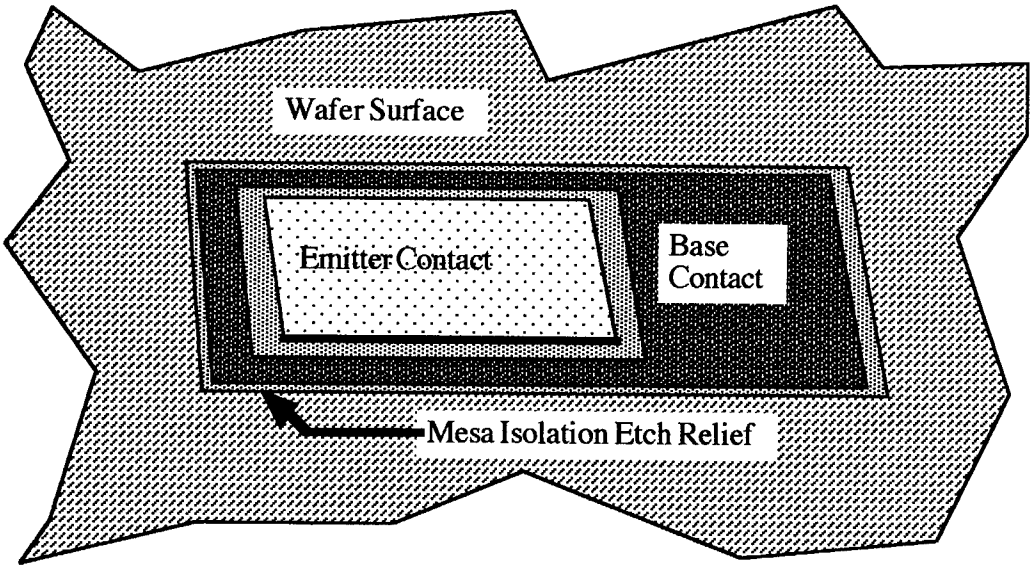


Figure 7. Low magnification view of planar transistor on wafer HBT 4.

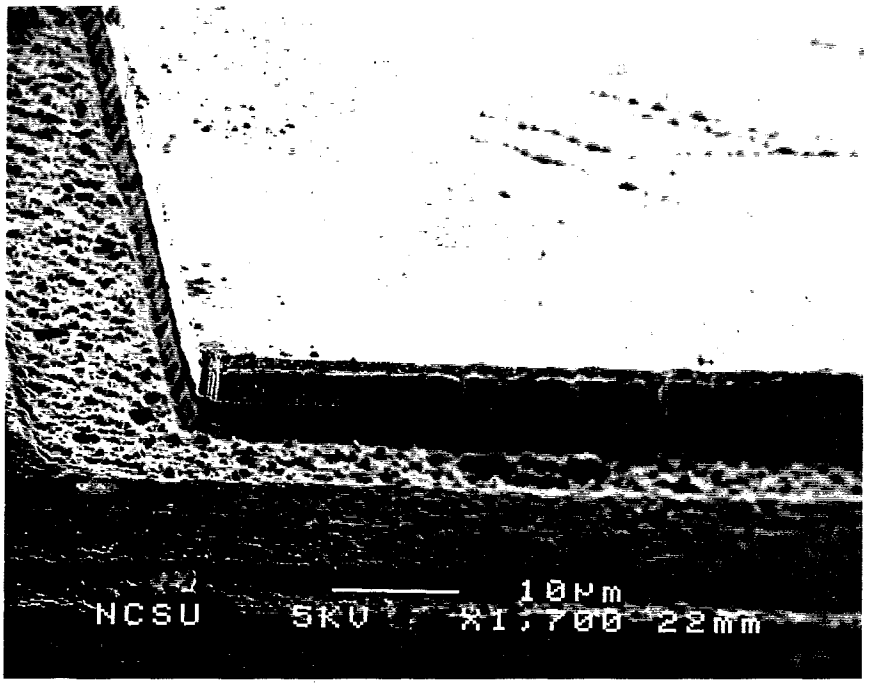
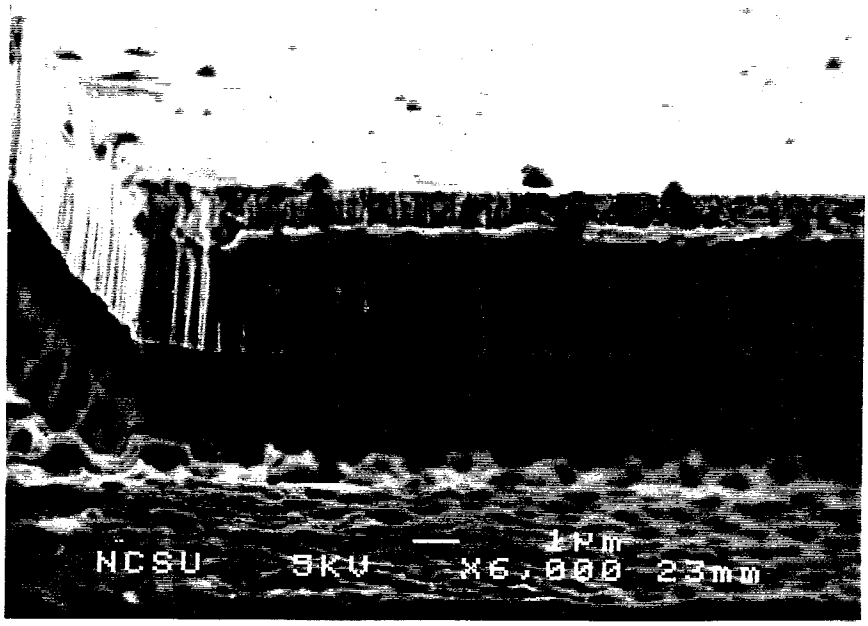


Figure 8. Medium magnification view of planar transistor on wafer HBT 4.



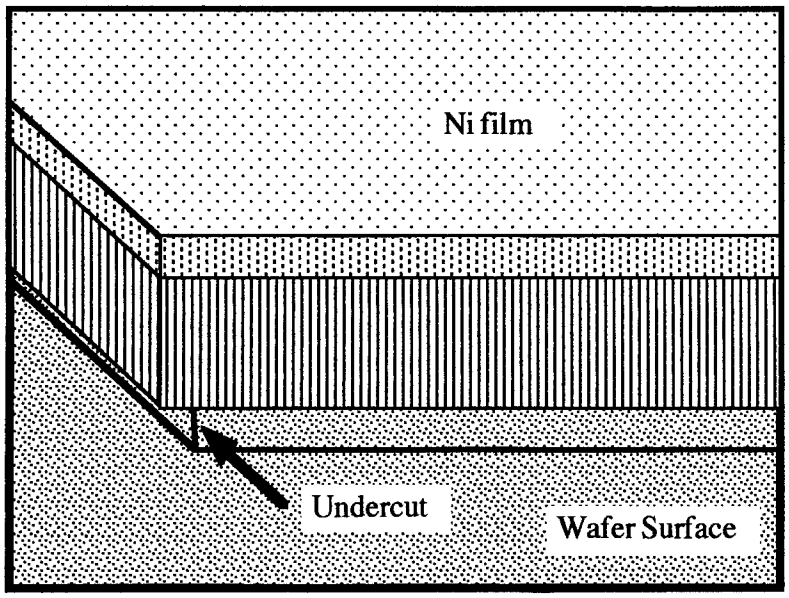


Figure 9. High magnification view of planar transistor on wafer HBT 4.

The amount of undercutting in this wafer exceeds the thickness of the deposited p-type base. As a result, when the base contact was formed on this wafer, it was actually contacting the n-type collector region or even the n-type substrate. This accounts for the observation of the ohmic behavior across the expected base-collector junction because there was no p-n junction, but rather simply two contacts to n-type regions. The low current passing between the emitter and base contacts is also explained because these contacts were not on opposite sides of a p-n junction, but were instead separated by a n-p-n bi-junction. In this configuration, one junction will always be reverse biased, resulting in only a relatively small reverse current.

Another difficulty arising from the etching was observed in which the SiC was not completely removed. Figure 10 is a SEM image of the surface of HBT 2. Circular regions of SiC are visible on this surface due to under etching. The I-V curve of Fig. 11 was collected between the base and collector contacts of this sample. Although rectifying behavior is observed, no appreciable current flows until a forward bias of $\approx$ 3.5 V is achieved. This may be due to the presence of n-type SiC between the Al base contact and the p-type base region.

D. Discussion

After processing the first batch of HBTs, no transistor activity has been observed in any of the devices. At this time, there appears to be two possible difficulties with completing

Figure 10. Surface of wafer HBT 2 with evidence of remaining SiC.

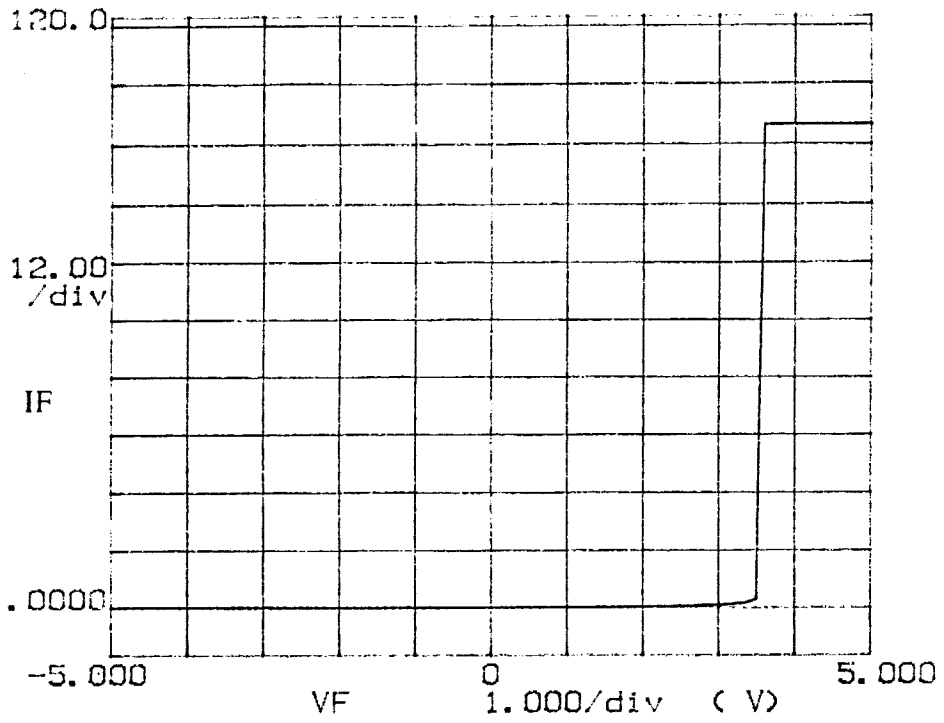


Figure 11. I-V characteristics between base and collector contacts on wafer HBT 2.

successful devices. First, the base region width had to be increased due to complications in the Si-epi process. The result of this may be that the electrons injected from the emitter may recombine in the base region before reaching the base-collector junction and contributing to I_C. The second difficulty in achieving successful devices has been clearly observed: the lack of sufficient precision in etching SiC. The SiC film was etched in a very aggressive NF_3 process by CREE Research Inc., Durham, NC. This process etched SiC fairly quickly. However, these conditions etch Si with extreme ferocity. Since Si is etched approximately 25 × as fast as SiC under these conditions, it becomes almost impossible to etch through ≈ 2 μm of SiC, but then stop within Si with an accuracy of ≈ 0.5–1 μm. At this time, the best approach appears to be the use of thinner SiC films which should proportionately reduce the required accuracy to completely remove all of the undesired parts of the SiC film without consuming the majority of the base region.

E. Conclusions

1. First batch of HBTs completely processed and examined.
2. No transistor activity observed in any of the produces devices.
3. Two possible difficulties in achieving successful devices: (a) base region too thick and (b) SiC etch process not sufficiently accurate.

F. Future Research Plans and Goals

1. Process a second batch of HBTs with thinner SiC emitter films.
2. Continue optimization of recipe for thick SiC films on Si(100) substrates.

G. Acknowledgments

The author would like to acknowledge John Palmour at Cree Research Inc., Durham, NC for his diligent efforts in performing the etching of the SiC films in this research.

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IV. Nucleation of Oriented Diamond Particles on Cobalt Substrates

I. Introduction

The heteroepitaxy of diamond films on non-diamond substrates by chemical vapor deposition (CVD) has been the subject of intensive research due to its potential impact on the electronic industry. The high surface energy of diamond (in the range of 5.3-9.2 J/m^2 for the principal low index planes) and the existence of interfacial misfit and strain energies between diamond films and non-diamond substrates due to lattice mismatch are believed to be the primary obstacles in forming oriented two-dimensional diamond nuclei. However, there is some promise in overcoming these obstacles, as evidenced by the heteroepitaxial nucleation and growth of diamond films on β-SiC and Si through use of a biasing technique [1-4]. Unfortunately, partial misorientation and three-dimensional growth continue to persist, thereby necessitating the investigation of alternative substrates.

Nickel, a catalyst-solvent in the HPHT process, is also a substrate of intensive research for heteroepitaxy of diamond films due to its close lattice parameter match with diamond [5]. However, its high solubility for carbon and its strong catalytic effect on hydrocarbon decomposition and subsequent graphite formation at low pressures have prevented CVD diamond nucleation on the Ni surface without the deposition of an intermediate graphite layer [6]. With a seeding and multi-step CVD process, these adverse effects have been overcome [7-10]. The graphite formation can be completely suppressed through presumably forming a surface Ni-C-H molten layer. Atomic hydrogen plays an important role in lowering the melting point of the substrate's surface and stabilizing the sp^3 C bonding. High density (111) and (100) oriented diamond nucleation was obtained on the respective single crystal Ni substrates without graphite codeposition.

Cobalt, adjacent to nickel in the periodic table, has an even better lattice match with diamond. The FCC lattice constant of cobalt and nickel are 3.554 and 3.517 Å [11], respectively, resulting in a lattice mismatch with diamond of 0.6 and 1.2 %. It also has other properties similar to those of Ni, such as unfilled d shell electrons (Ni with $3d^8$ and Co with $3d^7$), formation of a metal-C eutectic (melting point of Ni-C eutectic at 1326 °C and Co-C at 1318 °C), carbon and hydrogen solubility, etc., which make it another good catalyst-solvent for synthesizing diamond in the HPHT process [12]. Because of their similarities, it is certainly of interest to determine if cobalt can be used as a non-diamond substrate for heteroepitaxial nucleation and growth of diamond by the seeding and multi-step process used with nickel. Another impetus for this type of investigation is cobalt's use as a binder in tungsten carbide cutting tool inserts. In fact, poor adhesion to tungsten carbide substrates has been attributed to the cobalt binder [13,14]. Thus, studying diamond nucleation and growth on cobalt substrates

will help in understanding the basic mechanism of adhesion problems, which will aid in depositing diamond films directly on cobalt-bonded tungsten carbide.

B. Experimental Procedure

This article reports the investigations of oriented diamond nucleation and growth on single crystal cobalt substrates by a seeding and multi-step process, similar to that used in the nickel growth mentioned earlier [7-10]. Cobalt (0001) oriented single crystals were used as substrates. It is known that the lattice structure of cobalt changes from primitive hexagonal to face-centered cubic (fcc) above 417 °C [15]. Thus, at the diamond deposition temperature utilized, approximately 900 °C, it is believed that the orientation of the cobalt substrate is a <111> fcc structure which has been transformed from the <0001> room temperature hexagonal lattice. However, the (111) and (0001) surfaces have almost identical atom positions. Thus, in either case, it is expected that <111> oriented diamond particles would be nucleated if the process is successful.

The deposition experiments were carried out in a hot-filament chemical vapor deposition system. The cobalt substrates were polished down to 0.01 μm with Al_2O_3 powders and subsequently cleaned with trichloroethylene, acetone, and deionized water. Then, the surface of the substrate was seeded with either diamond powders, gaseous carbon species or graphite powders. For diamond seeding, the powders (1-2 μm) were prepared as a suspension in acetone. The cobalt substrates were immersed in the suspension, resulting in the formation of a layer of diamond powders on the cobalt surface upon removal from the suspension. The seeded cobalt substrates were then annealed at a temperature of 900 °C in a hydrogen atmosphere for 10 to 30 minutes to allow for deoxidation of the substrate surface and evaporation of water vapor and other adsorbates from the diamond seeds. The substrates were heated by radiative heating from the tungsten filaments. (All cited temperatures were actual surface temperatures that were calibrated by the melting points of Ge, Cu and their alloys, as well as thermocouples attached to the substrate surface.) After the annealing, the substrate temperature was raised to about 1100 °C while the tungsten filament was held at a temperature of approximately 2300 °C. At this high temperature, the diamond seeds started to dissolve rapidly into the cobalt lattice. The high temperature annealing time varied depending on the degree of seeding and the exact surface temperature. It is believed that the anneal must be held long enough to allow for sufficient reaction between the cobalt, diamond seeds and hydrogen to form a Co-C-H intermediate layer which suppresses graphite formation and promotes diamond nucleation. In practice, the duration of the anneal was effectively controlled by the visual appearance of the seeded substrates, which would change from dark gray in the initial annealing stage to reflective or shiny when the desirable Co-C-H surface layer was formed. After annealing, the substrate temperature was lowered to approximately 900 °C for diamond

nucleation and normal growth at a pressure of 30 Torr and a total gas flow rate of 600 sccm. The methane concentration in hydrogen was 0.3%, which is a preferred concentration for yielding <111> texturing [16, 17].

In a second type of pretreatment, the cobalt substrates were seeded *in situ* at 1100 °C in a hydrogen atmosphere with a methane concentration of 5.0 %. The purpose of such a treatment was to effectively saturate the cobalt surface with gaseous carbon species and form the desirable cobalt-carbon-hydrogen intermediate surface layer upon which oriented diamond could nucleate. It was found that at such a high temperature there was no observed carbon accumulation on the substrate surface because of the rapid dissolution of carbon into the cobalt lattice. The time duration for such a high temperature saturation process typically lasted from 15 to 30 minutes.

Finally, graphite powders were also used as a seeding source. The graphite powders were in the size range of 10-15 μm. They were prepared as suspensions in acetone. The Co substrates seeded with the graphite powders were then loaded into the CVD reactor and annealed in atomic hydrogen at 1100 °C. During the anneal, the visual appearance of the substrate turned from black to light gray. However, severe etching of graphite powders by atomic hydrogen occurred during the annealing which gasified the powders, and only allowed them to be partially dissolved into the cobalt lattice. For this reason, annealing of graphite-seeded cobalt substrates was also conducted in an argon atmosphere which allowed an improvement in nucleation density over that in the hydrogen atmosphere. After the annealing, the substrate temperature was decreased to about 900 °C to start the diamond nucleation and growth process.

C. Results and Discussion

The diamond nucleated and grown on the cobalt substrates was characterized by scanning electron microscopy (SEM) and Micro-Raman spectroscopy. Figure 1 shows the SEM micrographs of <111> oriented diamond particles formed on single crystal cobalt (0001) substrates seeded with diamond powders (a) and the high methane pretreatment (b). Micro-Raman was done by focusing the laser beam on the diamond surface. The spectrum in Fig. 2a shows that the oriented particle is high quality diamond with a FWHM of 4.3 cm^{-1} [18]. Micro-Raman also shows a very weak graphitic peak when focused on the substrate, as presented in Fig. 2b. It is speculated that some graphitic carbon was formed on the surface upon cooling the substrate to room temperature. Figure 3 displays an SEM micrograph of the growth resulting from the graphite powder seeding. Oriented diamond particles, similar to those observed with diamond seeding, were observed with the graphite seeding process as indicated by Raman spectroscopy. In addition, unusual faceted structures (as indicated by

arrows on the micrograph) were also observed which had a similar morphology to that of diamond.

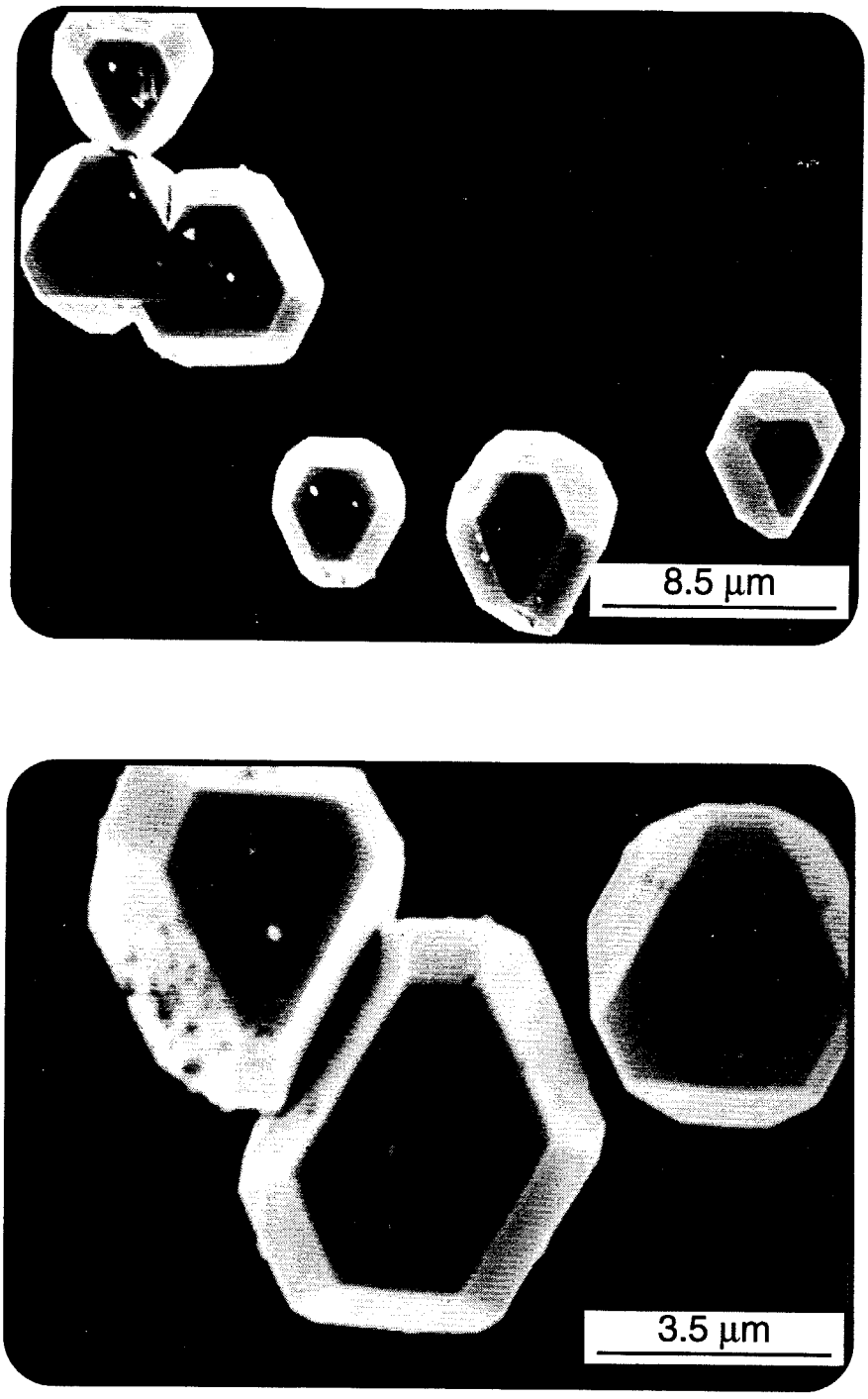
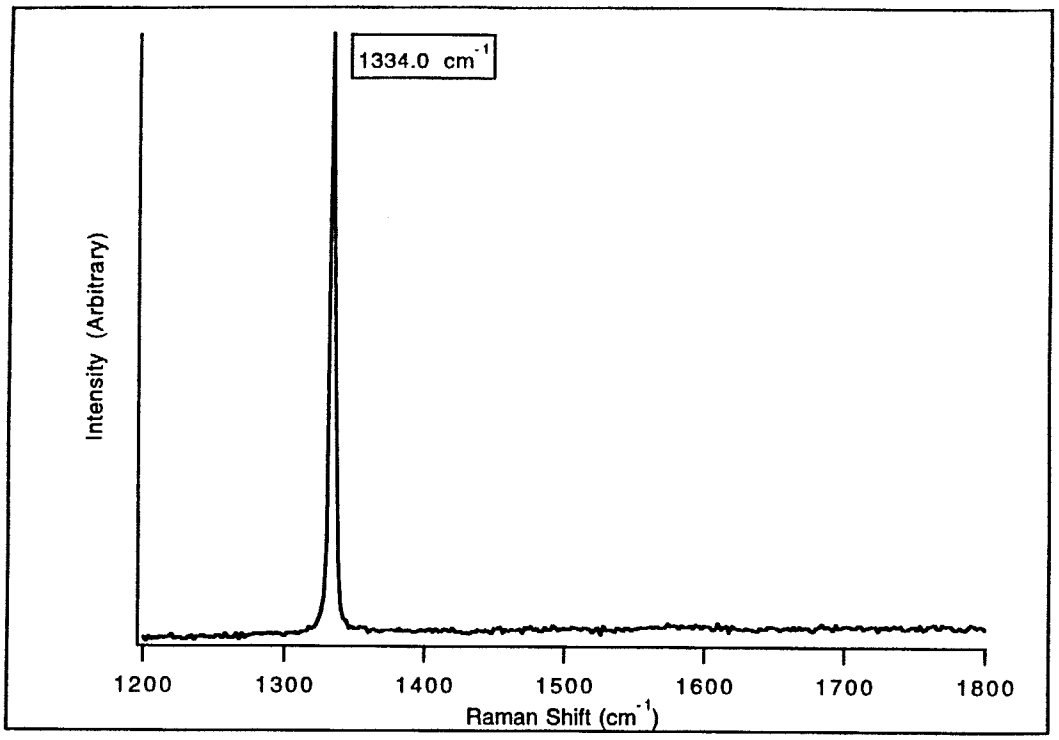
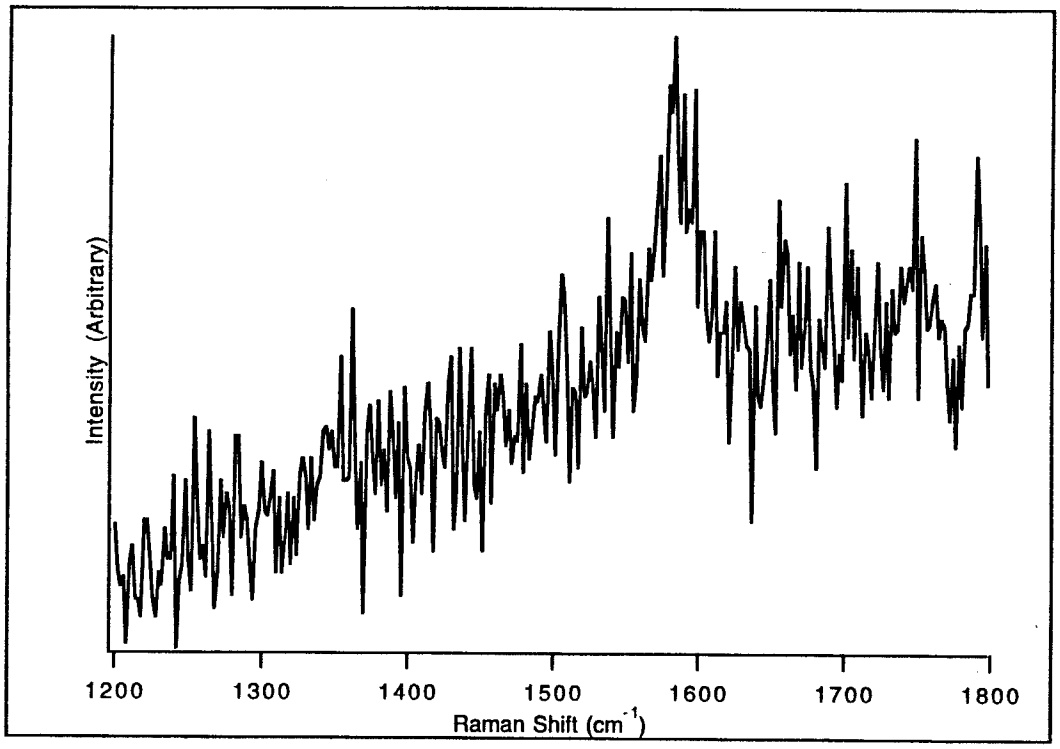


Figure 1. SEM micrographs of <111> oriented diamond particles formed on single crystal cobalt (0001) substrates (a) with diamond powders seeding (b) with high methane pretreatment.



a



b

Figure 2. Micro-Raman spectrum (a) on a diamond particle (b) on the substrate.

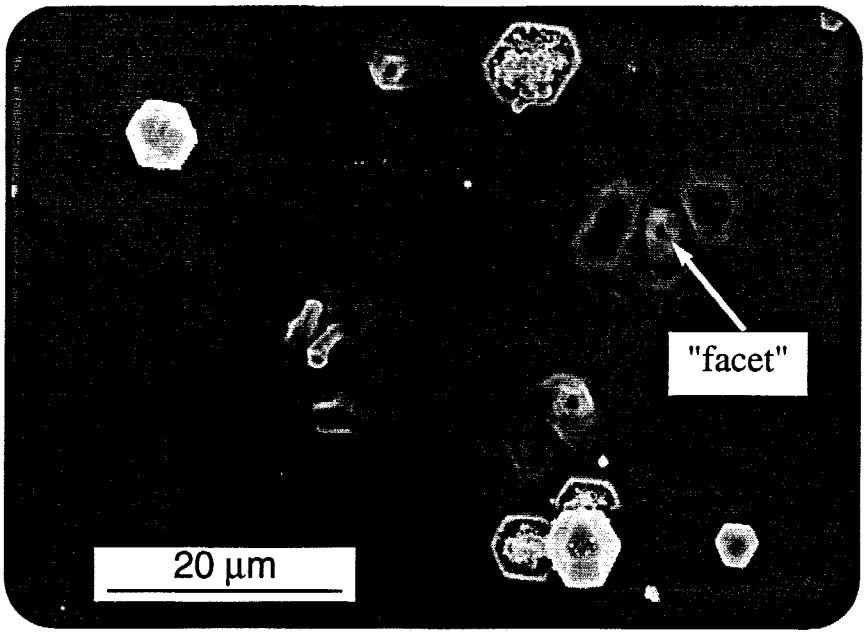


Figure 3. SEM micrographs of growth on cobalt(0001) substrate with graphite seeding pretreatment.

However, although most of these "facets" are aligned with each other, Micro-Raman shows neither a diamond nor a graphite peak.

Scanning Auger analysis was also performed on the "facets," diamond particles and substrate as shown in Fig. 4. Figure 4a is the scanning Auger depth profile analysis on a diamond particle which showed that the change in the carbon signal is quite small with sputtering time. Figure 4b is the depth profile analysis on the substrate beside the diamond particle, and showed that the carbon signal reduced quickly to zero at sputtering times approaching 3 minutes. Also, the cobalt signal increased very rapidly to a maximum over the same sputtering time. However, the depth profile analysis on the "facets," as represented in Fig. 4c, showed that the carbon signal decreased slowly while the cobalt signal increased slowly. After approximately 3 minutes sputtering, the intensity lines of carbon and cobalt become parallel to each other indicating the possible formation of an intermediate Co-C phase. Notably, the C/Co intensity ratio for 0 minutes sputtering on the diamond particle and on the facet were quite similar at 16 and 13 %, respectively, suggesting that the surface of this "facet" has the same carbon concentration as the diamond particles.

Finally, x-Ray Diffraction (XRD) analysis was also utilized to study the resultant diamond growth on cobalt. The primary interest in using XRD was to observe the phase transformation from hexagonal to fcc, which occurs at temperatures above 417 °C. However, there is very little change in the peak position in single crystal cobalt ($(0002)_{hex}$ at a 2θ of 44.76° and $(111)_{fcc}$ at a 2θ of 44.22°) and it was difficult to estimate from the XRD pattern of the substrate

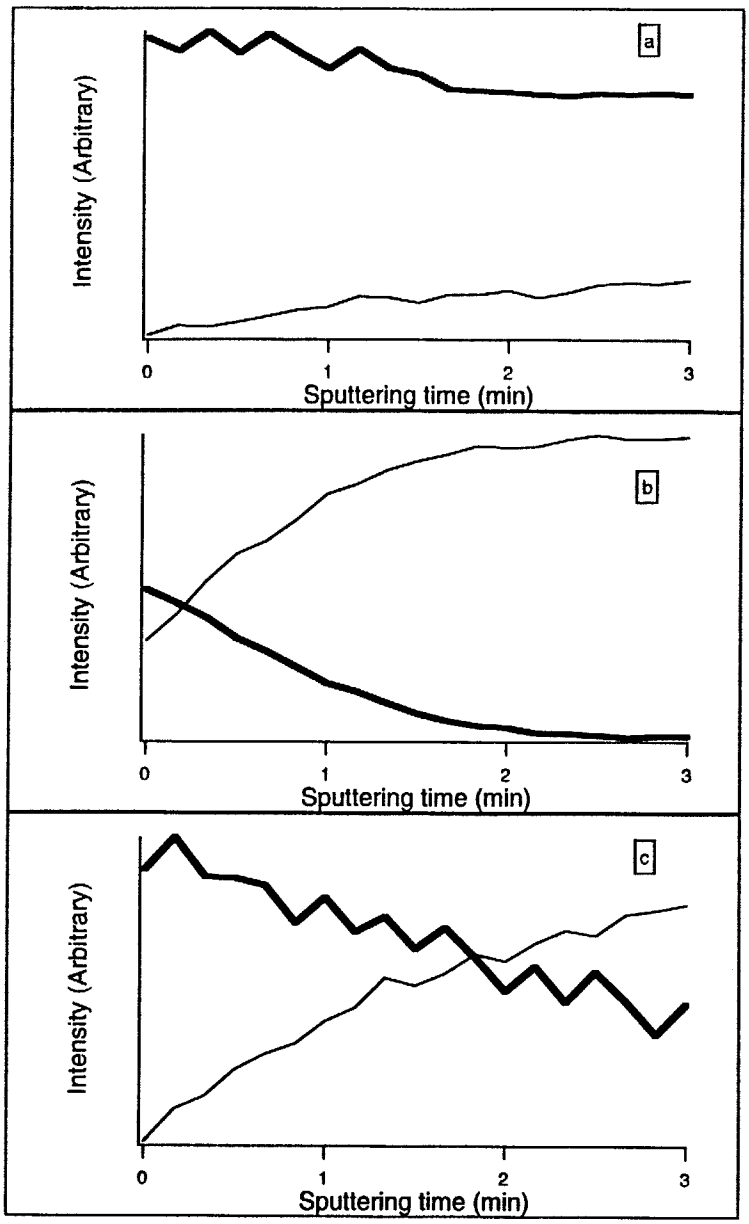


Figure 4. Scanning Auger depth profile analysis (a) on diamond particles, (b) on the substrate besides the diamond particle, (c) on the " facet."

that the transition had occurred. Thus, polycrystalline cobalt substrates, which had been treated in the same method described above, were used instead to study the transformation. It was found that the polished polycrystalline material contained both hexagonal and fcc components. After diamond growth, both components were still present with very little change in the intensities. As discussed above, the processing temperatures of approximately 900 °C utilized in these experiments should result in a phase transformation from the hexagonal to the cubic phase. Because of the lack of greatly increased fcc reflection intensities after diamond growth, it is believed that upon cooling of the substrate to room temperature, that the substrate transforms back to the hexagonal structure. However, it is possible that at the diamond/cobalt

interface, the cobalt remained in a fcc crystal structure. Further research will include grazing angle XRD to determine the crystal structure of the interfacial cobalt.

Utilizing premises based on eutectic alloy phase diagrams, phase diagrams made for the HPHT synthesis of diamond [19], and experimental evidence for cobalt and nickel, a model was proposed to understand the mechanism of oriented nucleation and growth of diamond on cobalt substrates by the multi-step process. As schematically shown in Fig. 5, a (0001) oriented single crystal cobalt substrate is first seeded with carbon powders which include diamond or graphite. Then the seeded substrate is heated to about 1100 °C in a hydrogen atmosphere to allow for sufficient reactions among cobalt, carbon, and atomic hydrogen to occur and the formation of molten, ternary, eutectic compounds on the surface consisting of cobalt, carbon, and hydrogen. These two steps can also be accomplished by simply saturating the cobalt surface with gaseous carbon species at 1100 °C. During the subsequent cooling to a substrate temperature of 900 - 950 °C to start the diamond nucleation, the molten eutectic compounds at the surface are believed to be supersaturated with carbon. The orientation of the diamond nuclei was then determined by the lattice potential of the subsurface, solid cobalt substrate, which has a very close lattice constant to that of diamond. Finally, diamond grows

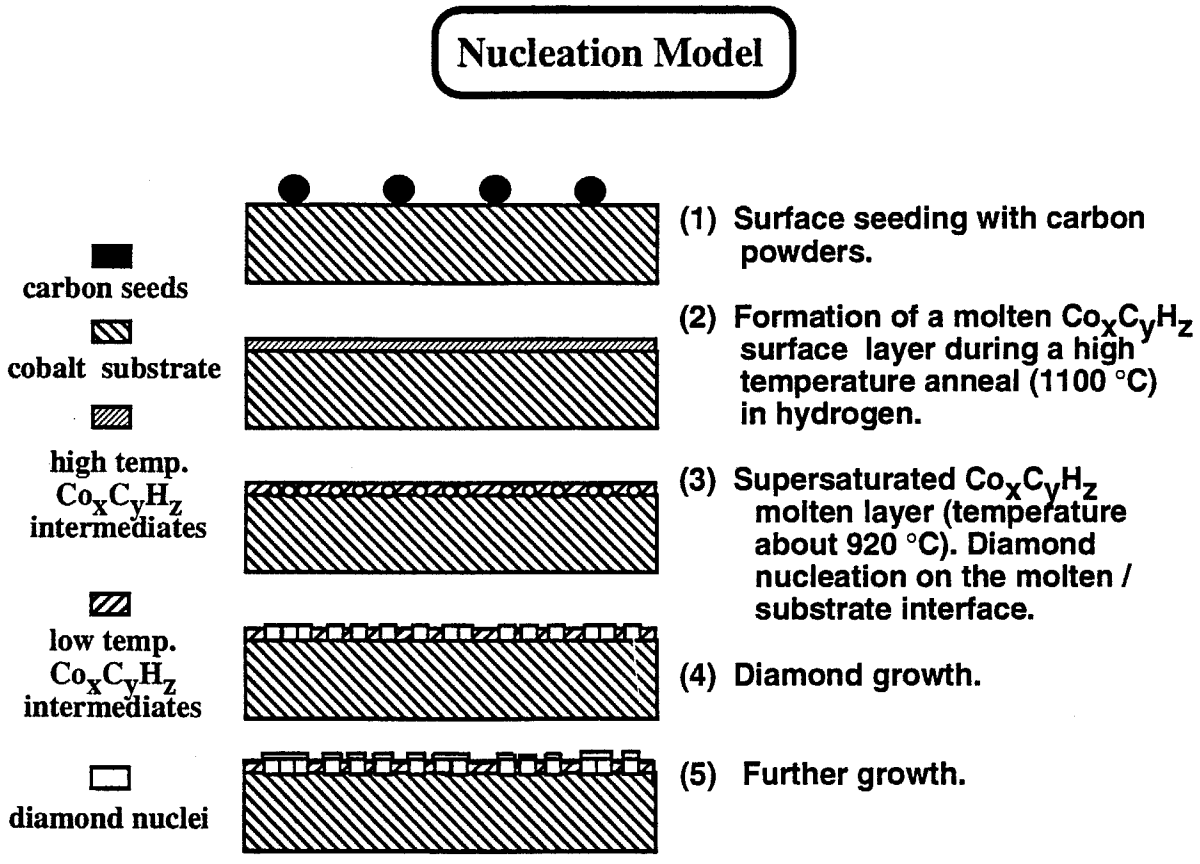


Figure 5. Schematic of a model for oriented diamond nucleation on single crystal cobalt substrate.

out from the nuclei and forms oriented diamond particles using normal CVD diamond growth conditions.

This model emphasizes the importance of forming a molten Co-C-H surface layer during the high temperature anneal in hydrogen and it is the authors' belief that step 2 of the nucleation model results from increasing the temperature of the sample above that of the liquidus temperature. In the area surrounding oriented diamond particles, flow patterns have been observed on the substrate, as shown on nickel, for example, in Fig. 6. The reason for such emphasis is that these flow patterns suggest a surface melting phenomenon as being necessary for orientation. The solubility of hydrogen in cobalt strongly depends, of course, on the activity of atomic hydrogen. Hydrogen solubilities increase dramatically when the substrate is in an atomic hydrogen environment, especially near the melting point [20]. It is known that when carbon and cobalt form a eutectic, the melting point temperature is lowered to 1318 °C. Cobalt and hydrogen also form a eutectic. Thus, it is likely that the melting point of the Co-C-H layer is much lower than that of pure bulk cobalt. This belief is supported through powder experiments, where a mixture of cobalt and carbon powder was heated in the HFCVD system in both hydrogen and argon environments. It was found that the powders melted at lower temperatures in the hydrogen environment, approximately 1150 °C, than in the argon environment, around 1400 °C. Figure 7 presents SEM micrographs for a 2.7 % carbon in cobalt powder mixture that were heated separately in hydrogen, a, and argon, b, to approximately 1150 °C. These micrographs show that, in hydrogen, the mixture has completely melted and developed a smooth surface. However, in argon, Fig. 7b, the sample has only sintered, a process that occurs above approximately 2/3 of the melting point. This molten surface layer is believed to have effectively suppressed graphite formation, as observed from Raman spectra.

The temperature drop of step 3 decreases the temperature below that of the liquidus temperature. But, it must be higher than that of the eutectic temperature from experimental evidence that has produced only graphite in the area of the phase diagram below the eutectic temperature. As the surface energy of graphite is much greater when it borders with a metal than with a gas [21], more energy is needed to form a graphite embryo in the molten surface layer. Its growth is thus inhibited [22]. At the same time, a sp^3 C cluster formed by the seeding and annealing process may be stabilized in the surface layer by atomic hydrogen, enhancing diamond nucleation. Also, in HPHT, it has been found that diamond is less soluble than graphite in the nickel catalyst in the region between the liquidus and the eutectic; thus, diamond is precipitated without graphite formation [19]. The position on the phase diagram where the experiments are conducted must be to the right of the eutectic point, i.e. hypereutectic, because carbon is the primary microconstituent and not cobalt. Further, from the temperatures needed to

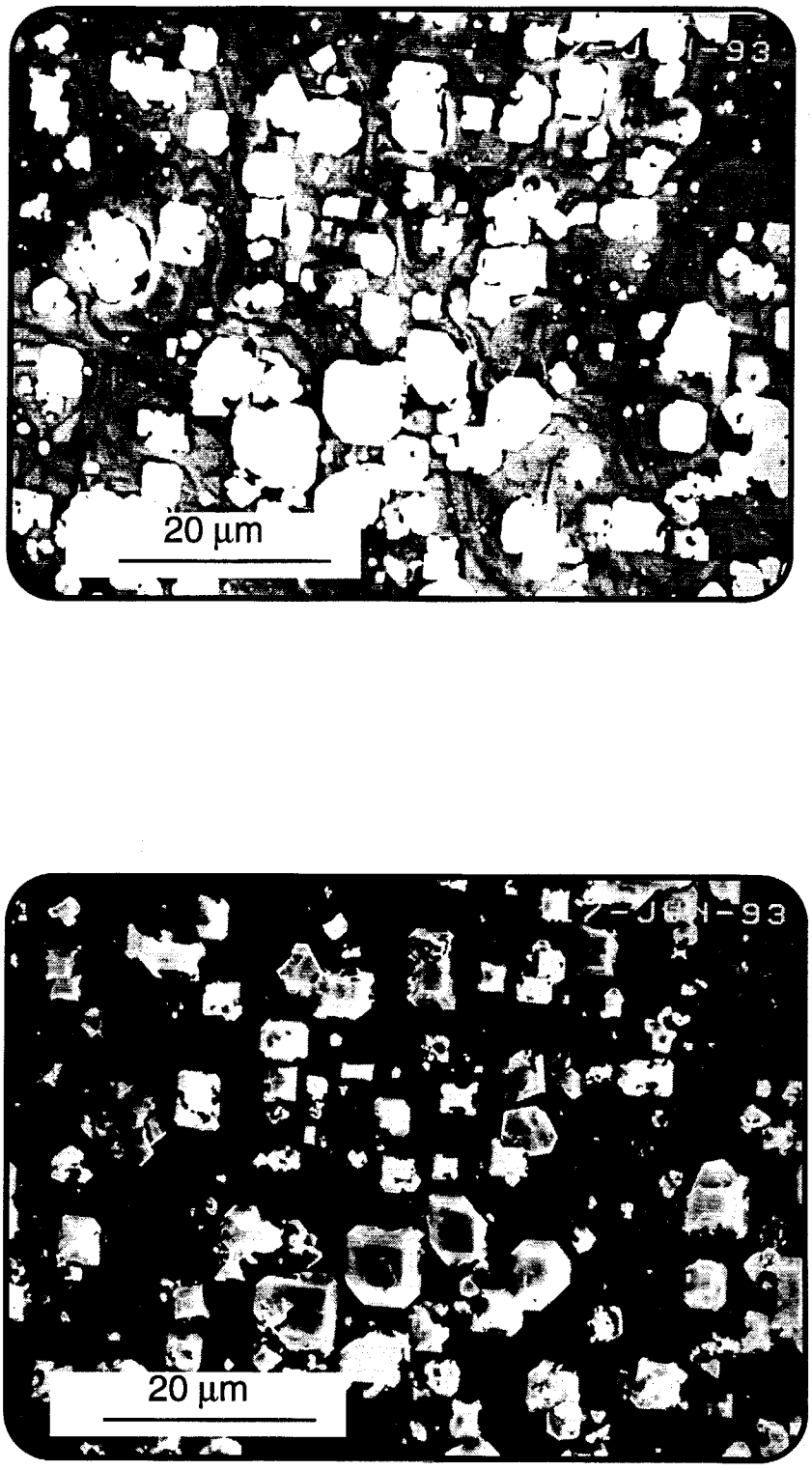
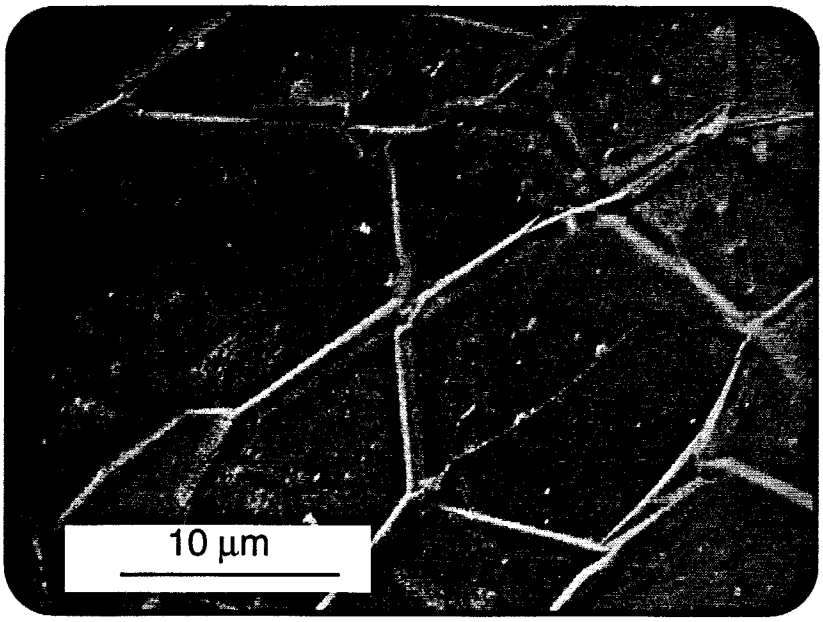


Figure 6. SEM micrographs of different areas on carbon seeded, (100) oriented Ni substrates showing evidence of surface melting and flow patterns. These two micrographs are highly contrasted with the oriented diamond nuclei appearing white in order to illustrate the surface morphologies of the underlying Ni surfaces.



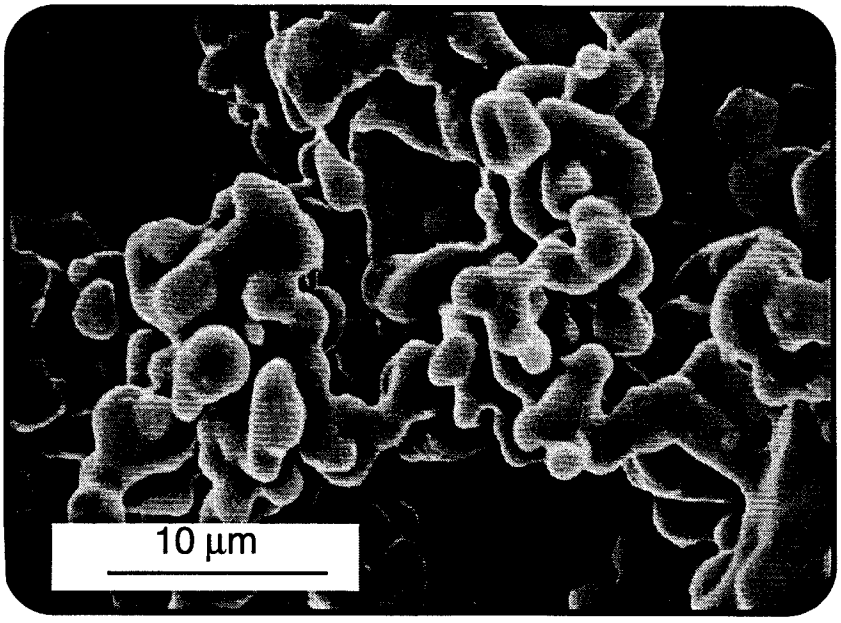


Figure 7. SEM micrographs of a 2.7 wt. % C in Co mixture heated to 1150°C in (a) hydrogen and (b) argon.

melt this alloy and reconciling that hydrogen has suppressed temperatures over those on the binary phase diagram, it is surmised that the solidification line is just right of the eutectic point,

approximately 2.3 and 2.7 wt.% carbon in nickel and cobalt, respectively. Because of the slope of the solvus, the liquidus temperature of nickel will be higher than cobalt for these two carbon percentages. Indeed, experimentally it has been verified that a lower temperature is needed to precipitate diamond when cobalt substrates are used.

Although the main properties of nickel and cobalt are nearly identical, there are still some differences between them which can be seen on their respective carbon binary phase diagrams (23) as schematically reproduced in Fig. 8. The eutectic temperature is lower in cobalt. Also, the slope of the hypereutectic liquidus for nickel is steeper than that for cobalt. Thus, a temperature decrease of 1°C results in a greater amount of carbon precipitation in cobalt than nickel due to the increased supersaturation. These dissimilarities are most probably the reason why there are differences in the parameters, such as the length and exact temperature of the high temperature anneal, for obtaining oriented diamond on nickel and cobalt.

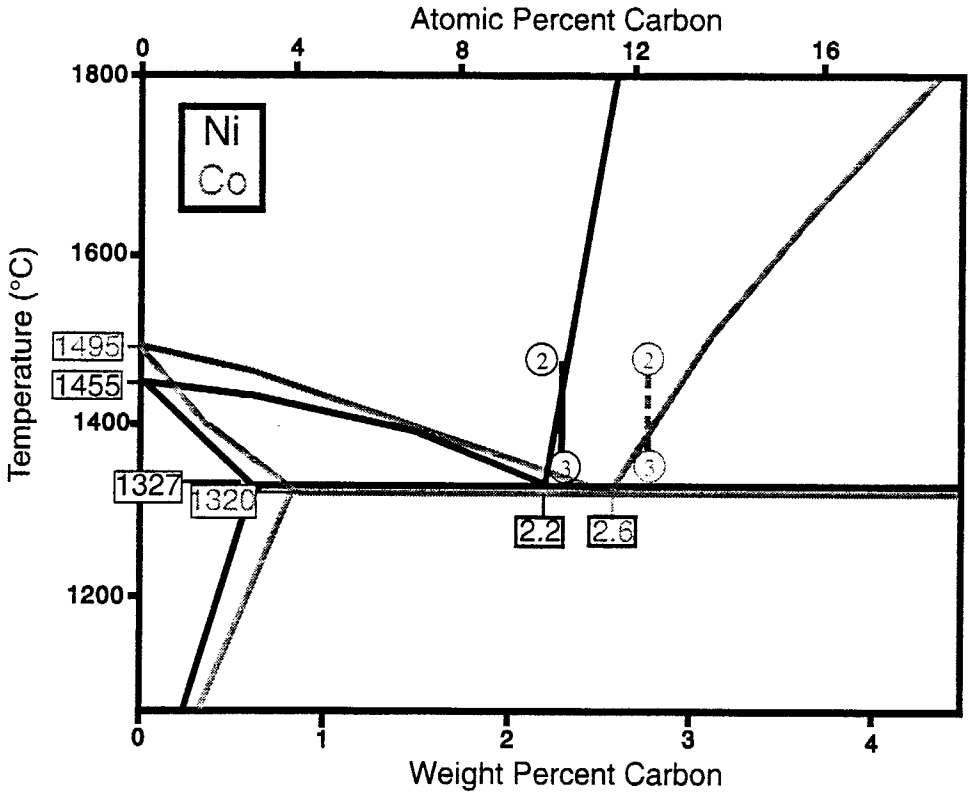


Figure 8. Schematic depiction combining the nickel-carbon and cobalt-carbon binary phase diagrams.

D. Conclusions

In conclusion, <111> oriented diamond particles were obtained on cobalt (0001) oriented single crystal substrates by a seeding and multi-step process. Diamond powders, graphite powders and gaseous carbon were used as seeding materials. Micro-Raman shows that the

oriented particles are high quality diamond, with a FWHM of 4.3 cm^{-1}. Scanning Auger depth profile analysis was done to analyze the differences of the qualitative change in the Co/C ratio among an oriented diamond particle, substrate, and an unusual "facet" structure. The results suggested the existence of Co-C intermediate phase formation and its relation to oriented diamond nucleation. A mechanistic model was proposed to understand the process, which emphasized the suppression of graphite codeposition and oriented diamond nucleation through forming the molten Co-C-H surface layer.

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E. Future Research Plans and Goals

Future work will include attempting to increase the nucleation density on these films. This will involve refining the current parameters, especially the high temperature step. Also, detailed grazing angle X-ray Diffraction experiments will be performed to determine if the cobalt has remained cubic near the surface. Other catalyst materials, such as iron, manganese, and platinum, will be studied to see if they too will provide substrates capable of producing oriented diamond with the multistep growth process.

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V. Epitaxial Cerium Oxide on Silicon Substrates

A. Introduction

Cerium dioxide (CeO_2) is of present interest due to its potential applications to Si on insulator structures, stable capacitor devices, and stable buffer layers between high-temperature superconducting materials and Si-substrates[1-4]. It can offer a new material system for SOI structure because:

(1) CeO_2 has a CaF_2-structure [i.e., cubic symmetry, a=0.541 nm].

(2) Cerium dioxide's lattice parameter matches significantly with Si, compared with other insulating materials such as sapphire (hexagonal), spinel, CaF_2 (cubic), and Zirconia (tetragonal). The lattice mismatch ($\Delta a/a$) of CeO_2 to Si is 0.35%. This small lattice mismatch in CeO_2 can solve the above mentioned problems in SOI technology. It has been proposed to be used as a buffer layer for high T_c superconductors.

(3) CeO_2 has a high dielectric constant (ε_r=26) compared to SiO_2 (ε_r=2.3). The higher value indicates that CeO_2 can have a potential for DRAM, where large storage capacitance are needed, without the need to reduce the oxide film thickness "d" ($C=\varepsilon A/d$).

(4) CeO_2 is a stable oxide and does not deteriorate due to environmental conditions.

Material growth and electrical performance of CeO_2 films in MOS structures[5-10] have been studied and these properties have been correlated to the growth conditions and structural properties. The electrical properties of the films were correlated to the structural properties observed by HRTEM and RBS analyses[7]. The following outlines the main findings in the deposition parameters, effect of annealing, and the electrical properties of CeO_2/Si MOS structure.

B. Experimental Procedure

Thin films of CeO_2 have been grown on Si substrates using a specially designed UHV laser ablation deposition system. The deposition system used an ArF excimer laser with both the target and the substrate are rotating during deposition. The UHV system is desirable for the *in-situ* surface diagnosis by reflection high-energy electron diffraction (RHEED). High resolution transmission electron microscopy (HRTEM), x-ray diffraction, and C-V characteristics of the grown films were employed as characterization techniques. The electrical properties of the films were correlated to the structural properties observed by HRTEM and RBS analyses. The MIS capacitor structures were fabricated by evaporating aluminum dots onto the CeO_2 surface and uniform Al onto the back of Si (111) wafer. Most of our current activities were directed to the growth on (111) Si substrates. The following outlines the main

findings in the deposition parameters, effect of annealing and the electrical properties of CeO_2/Si MOS structure.

C. Results and Discussion

CeO_2 Growth and Structural Characterization. Films of CeO_2 grown on (111) Si substrates were found to grow epitaxially at ~ 700°C with thickness uniformity of $\pm$ 20 ^{O}A along a 1 1/2 inch Si wafer. An atomically clean substrate was found to be critical for the epitaxial growth of CeO_2 on Si. Several cleaning schemes were utilized. Specifically, chemical RCA cleaning was only partially successful in obtaining a good growth surface as determined by observation of the RHEED pattern. Similarly, variations of uv-ozone cleaning left islands of SiO_2 on the substrate surface. However, when using a modified version of the RCA clean, a good 7×7 RHEED pattern was observed, indicating a clean surface. when the substrate surface is carefully cleaned a streaky RHEED pattern was observed for the epitaxial growth of (111)CeO_2/Si(111).

Figure 1 shows a microstructure of an as-grown film observed by HRTEM. It consists of a single crystal CeO_2 overlayer having B-type orientation to the Si (111) substrate, an amorphous CeO_x layer, an amorphous SiO_2 layer, and the Si(111) substrate. This unusual

Figure 1. A lattice image of an as deposited sample from <110> direction. Single crystalline CeO_2, amorphous CeO_x (dark contrast region) followed by SiO_2 (bright contrast region) were observed on the Si(111) substrate. CeO_2 has a B-type orientation to the Si substrate.

condition of having a single crystal layer of CeO_2 with the same orientation as the substrate atop two different amorphous layers was not expected but it can be beneficial. A tentative model to explain the deposition of this complex structure can be outlined as follows[5]: At first, few monolayers of CeO_2 grow epitaxially on the Si(111) substrate. As the growth proceeds, a reaction occurs at the interface between Si and CeO_2:

$$Si + 4CeO_2 \rightarrow SiO_2 + 2Ce_2O_3$$

which has a heat of formation ΔH = -46.6 Kcal[8]. Thus oxygen from CeO_2 reacts with Si to form SiO_2 creating an oxygen deficient CeO_x that is partially amorphized. Meanwhile, epitaxial CeO_2 remains near the surface to act as a template for further growth. The growth conditions are thought to be important parameters that control the reaction and the appearing microstructure in cerium oxide. This model is confirmed by our observation that a single crystal CeO_2, indicated by the RHEED pattern, exist at the surface for all growth stages. Also, by digital diffraction [or Fast Fourier Transform (FFT)] of the high resolution images, we have found residual single crystal of CeO_2 still exists in the CeO_x amorphous film.

Oxygen Annealing of CeO_2 Films. Rutherford Back Scattering (RBS) measurements showed that the as grown films are not of good crystalline quality as indicated in Fig. 2a {χ_{min} = 49%}. Also the electrical measurements indicated the poor electrical properties of these films. Thus, to makeup for this lost O_2 atoms used to form amorphous SiO_2 film, some samples were post annealed in dry O_2 at 900°C for varying lengths of time. Fig. 2b Shows that oxygen annealing improves the film crystalline quality as indicated by χ_{min} (26%). Figure 3 shows a lattice image of a sample observed after oxygen annealing. The α-CeO_x layer is recrystallized back into CeO_2, and the SiO_2 layer is made thicker, depending on the length of time a sample is oxidized. Annealing has also improved the electronic properties of the films as compared to the as grown films.

Electrical Characterization. Altering the structure of the film from CeO_2/ α-CeO_x/ SiO_2/ Si(111) to CeO_2/ (thicker) SiO_2/ Si(111) by annealing greatly enhanced the electrical properties of the films. This is readily seen in Fig. 4, which shows high-frequency (100kHz) capacitance-voltage curves measured on MOS capacitors constructed directly on both as-grown and annealed films. The as-grown film exhibits fairly high capacitance at accumulation as expected, due to the high dielectric constant of CeO_2 film. However, it has a low breakdown voltage and goes into deep-depletion as opposed to inversion. The hysteresis observed in the C-V curves in Fig. 4 was detected by sweeping the voltage from inversion to accumulation and back again. The large amount of hysteresis in the C-V curve of the as-grown film indicates a significant amount of trapped charge. The capacitance at accumulation for the annealed films is reduced due to the thicker SiO_2 layers, yet annealed films show marked improvement in all other

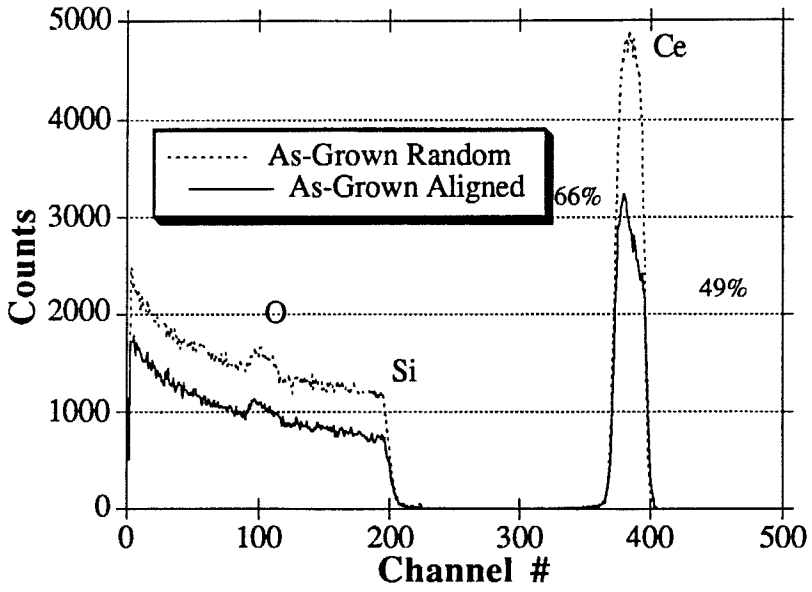

Figure 2a. Rutherford Back Scattering (RBS) measurements shows that the as grown films are not of good crystalline quality as indicated by χ_{min}.

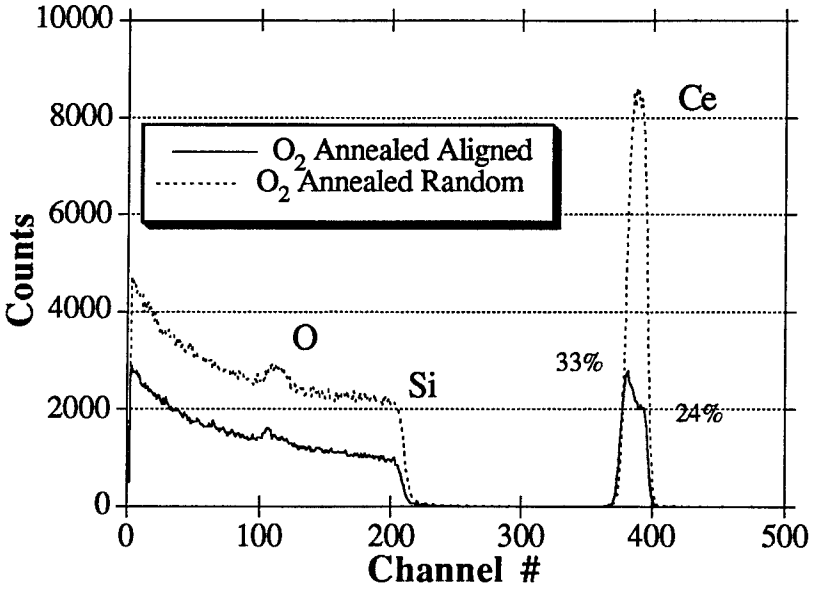

Figure 2b. Rutherford Back Scattering (RBS) measurements shows that the oxygen annealed films are of better crystalline quality as indicated by χ_{min}.

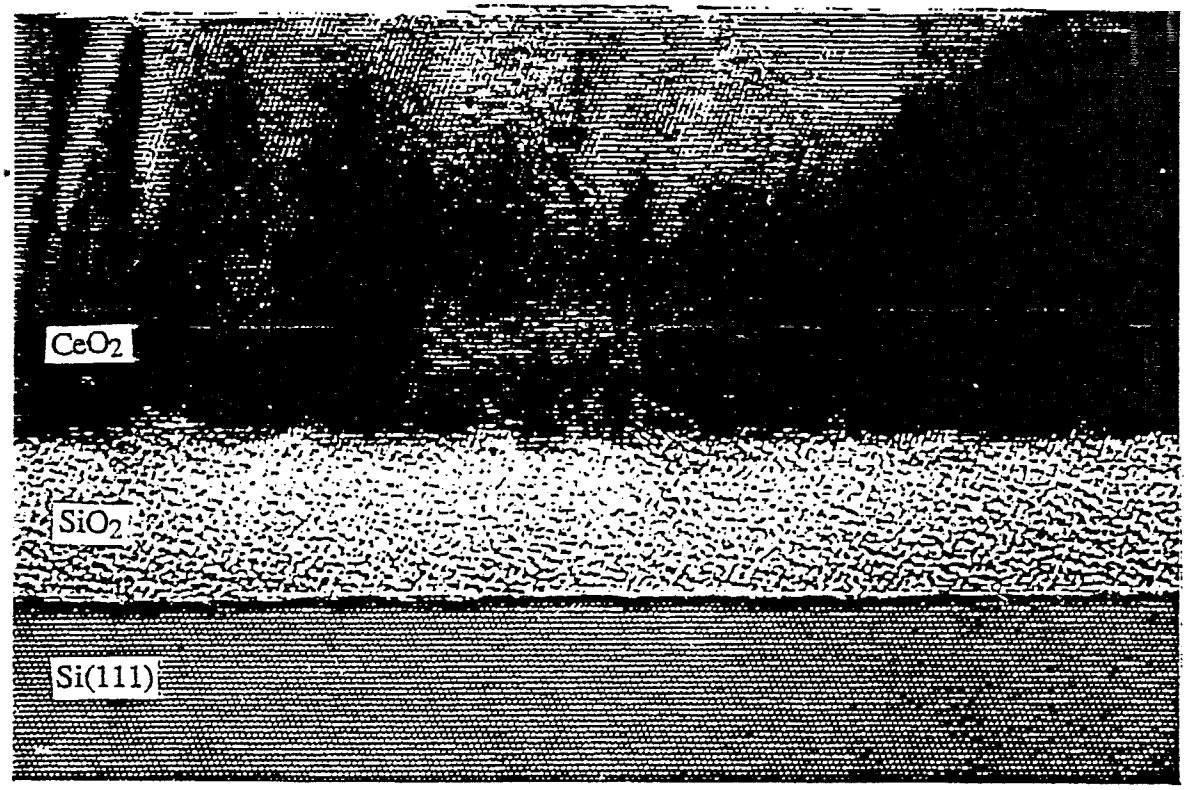

Figure 3. A lattice image of a sample after the post annealing in oxygen atmosphere. The dark amorphous region disappeared and the bright amorphous region increased in thickness, indicating the recrystallizaztion of CeO_2 and growth of α-SiO_2.

aspects of C-V behavior. For instance, inversion is achieved for the annealed films. These measured C-V curves were compared to theoretical C-V curves for analysis. Annealing lowers the fixed oxide charge, and reduces the oxide trapped charge by two orders of magnitude (from $\sim 10^{12}$ to $\sim 10^{10}$), indicating that the majority of Q_{ot} was contained in the α- CeO_x layer. The density of interface traps was also lowered by annealing to 6×10^{11}; a level acceptable for the Si(111) surface.

D. Conclusions

From the above studies of CeO_2/Si(111) one can expect that the cerium oxide is a potential material system for MOS application. However, further studies are needed to control the interfacial reaction between the cerium oxide and silicon. The oxidation schemes to control the amorphous silicon dioxide film thickness and the insulator quality requires further studies as well.

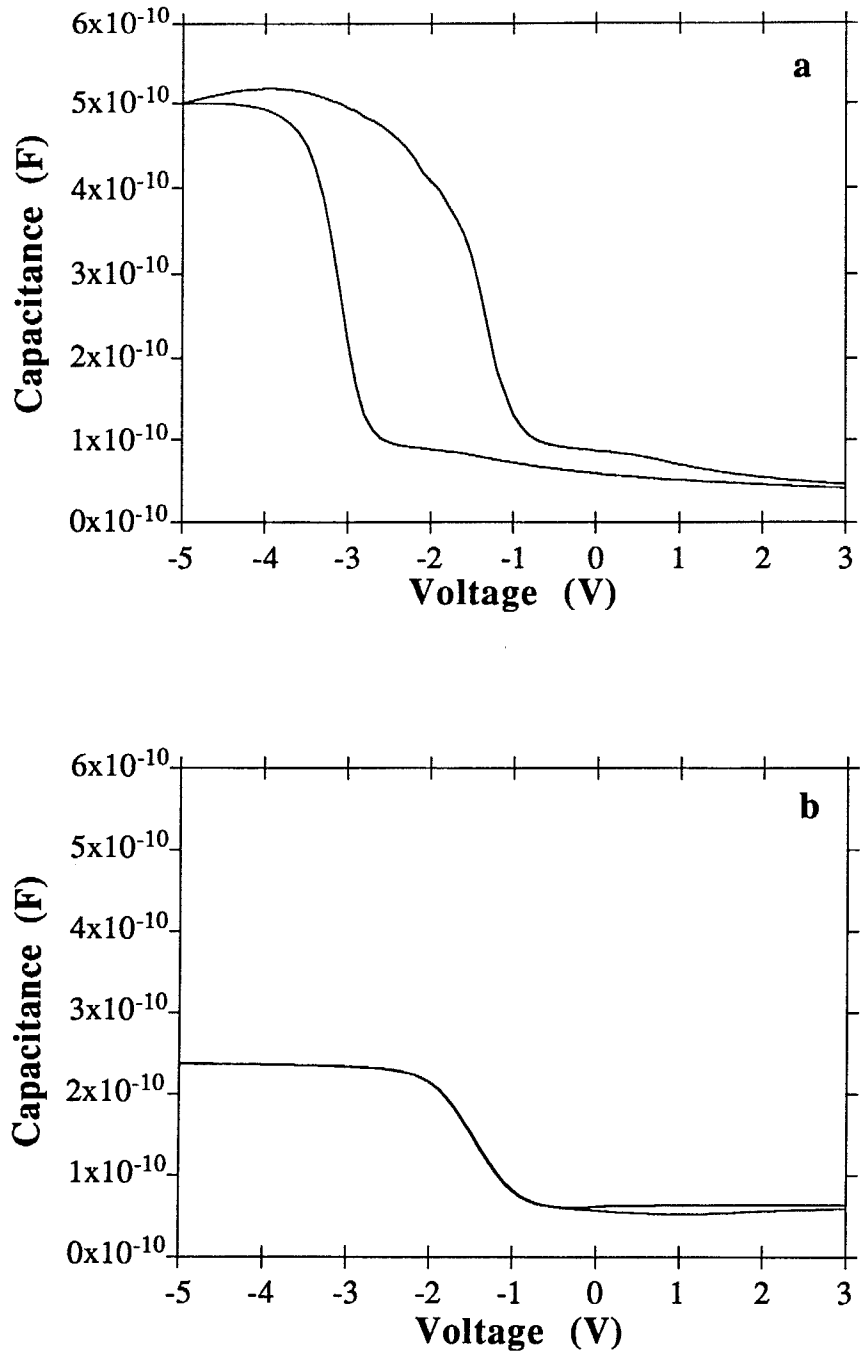

Figure 4. High frequency C-V curves for: a) as grown CeO_2/(111)Si, b) annealed in dry oxygen (900°C, 35 min.).

E. Future Plans

Our achievement in the growth of CeO_2 on Si has a unique feature which is the presence of an amorphous α-SiO_2 layer at the CeO_2/Si interface, while maintaining a single crystal CeO_2

film that is lattice matched to Si as shown in Fig. 1. The presence of the SiO_2 is desirable and results in fairly low interface charge density with the Si substrate while the top surface maintains single crystal CeO_2. The goal of the future work is to capitalize on this unique feature and add new dimensions to the SOI technology based on CeO_2/Si materials system. These goals can be outlined as follows:

i) Optimizing the CeO_2/Si MOS capacitance.

ii) Epitaxial growth of Si on the CeO_2/Si structure.

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