RL-TR-94-103
In-House Report
August 1994

GaAs OPTICAL CIRCUITS

M. A. Parker, J. S. Kimmet, 2Lt, USAF, S. I. Libby, Capt, USAF, (Rome Laboratory); P. D. Swanson, (National Research Council)

Rome Laboratory
Air Force Materiel Command
Griffiss Air Force Base, New York

This report has been reviewed by the Rome Laboratory Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RL-TR-94-103 has been reviewed and is approved for publication.

APPROVED:

JAMES W. CUSACK, Chief
Photonics & Optics Division
Surveillance & Photonics Directorate

FOR THE COMMANDER:

LUKE L. LUCAS, Colonel, USAF
Deputy Director
Surveillance & Photonics Directorate

If your address has changed or if you wish to be removed from the Rome Laboratory mailing list, or if the addressee is no longer employed by your organization, please notify RL (OCPB) Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	August 1994	In-House Oct 92 - Sep 93

4. TITLE AND SUBTITLE
GaAs OPTICAL CIRCUITS

5. FUNDING NUMBERS
PE - 62702F
PR - 4600
TA - P3
WU - 21

6. AUTHOR(S) M. A. Parker, J. S. Kimmet, Jr., USAF, S. L. Libby, Capt, USAF, (Rome Laboratory); P. D. Swanson, (National Research Council)

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Rome Laboratory (OCPB)
25 Electronic Pky
Griffiss AFB NY 13441-4515

8. PERFORMING ORGANIZATION REPORT NUMBER
RL-TR-94-103

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (OCPB)
25 Electronic Pky
Griffiss AFB NY 13441-4515

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Michael A. Parker/OCPB (315) 330-7671

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This report presents two new smart pixels for use in optical computing and communications. These devices are Configurable Optical Gates (COGs) that form the Diode Laser Logic (DLL) family and Spontaneous Emission Filtered Laser Amplifiers (SEFLA). DLL is a complete, new logic family comprised of Q-switched lasers and photodetectors. The lasers and detectors are monolithically integrated on multiple quantum well laser heterostructure with semi-insulating substrates. Preliminary results indicate an ON/OFF contrast ratio better than 500:1, gain in excess of 20 and variable I/O hysteresis characteristics. As a result, the devices can be cascaded to form more complex optical circuits. In addition to introducing the Diode Laser Logic family, a basic model is presented and the fabrication process is described in detail. The SEFLA combines an optical amplifier with a spontaneous emission filter in order to increase the signal-to-noise ratio by actively filtering out the spontaneous emission from the output signal. The filtering function is accomplished by integrating the amplifier with a semiconductor laser in such a way that the signal in the amplifier suppresses the gain in the laser. Unlike conventional optical amplifiers, these can, in principle, be cascaded without significantly decreasing the performance.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Configurable Optical Gates (COGs), Diode Laser Logic (DLL), Spontaneous Emission Filtered Laser Amplifiers (SEFLA)	48
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	U/L

ABSTRACT

This report presents two new smart pixels for use in optical computing and communications. These devices are Configurable Optical Gates (COGs) that form the Diode Laser Logic (DLL) family and Spontaneous Emission Filtered Laser Amplifiers (SEFLA). DLL is a complete, new logic family comprised of Q-switched lasers and photodetectors. The lasers and detectors are monolithically integrated on multiple quantum well laser heterostructure with semi-insulating substrates. Preliminary results indicate an ON/OFF contrast ratio better than 500:1, gain in excess of 20 and variable I/O hysteresis characteristics. As a result, the devices can be cascaded to form more complex optical circuits. In addition to introducing the Diode Laser Logic family, a basic model is presented and the fabrication process is described in detail.

The SEFLA combines an optical amplifier with a spontaneous emission filter in order to increase the signal-to-noise ratio by actively filtering out the spontaneous emission from the output signal. The filtering function is accomplished by integrating the amplifier with a semiconductor laser in such a way that the signal in the amplifier suppresses the gain in the laser. Unlike conventional optical amplifiers, these can, in principle, be cascaded without significantly decreasing the performance. The gain characteristics can be tailored during epitaxial growth for operation at a number of different wavelengths including 0.85 and 1.3 μm.

This report also discusses the fabrication techniques used to fabricate the COGs and SEFLAs. The material includes the multiquantum well heterostructure design, masking layers and specific clean room information. These devices are the subjects of patent disclosures through the JAG office at Rome Laboratory, Griffiss AFB NY, 13441.

ACKNOWLEDGEMENTS

The authors wish to acknowledge C. L. Tang and the members of his group at Cornell University, the staff at the National Nanofabrication Facility and the USAF Photonics Center, and other members of R. J. Michalak's group at Rome Laboratory.

The authors contributed equally to the work discussed in this report. The devices were designed and tested by M. A. Parker, P. D. Swanson and S. I. Libby. They were fabricated by P. D. Swanson, J. S. Kimmet and M. A. Parker.

TABLE OF CONTENTS

LIST OF FIGURES

I. INTRODUCTION

The subject of optical processing spans vast amounts of research and written word. Optical processing has the potential to offer many significant advantages over electronics however, to date, few of those advantages have been exploited. Photonics research is still in its infancy whereas silicon based electronics continues to increase in use in established commercial products and to improve in its operating and packaging characteristics. Many researchers argue that optical processing needs to fill niches for specific applications while developing the broader spectrum of potential advantages. In this way, optical processing might one day assume its own legitimate role in the vast world of information processing.

One of those niches or areas of near term payoff is the optical interconnect. The advantage here is to use fairly well established techniques to provide information highways between either macro-size systems such as computers or micro-size ones such as electronic integrated circuits. Components of the optical interconnect actually form a subset of the family of smart pixels. These smart pixels are generally viewed as micro-miniature devices capable of performing both logic and optical interconnect functions. The logic function might be as simple as one of the Boolean logic operations. With such devices, entire optical processors can be constructed.

The all optical processor would ideally transform two-dimensional sheets of analog or digital optical data (images) by sequentially passing the images through stacked planes consisting of optical logic gates and memory elements; each plane would perform a function on the images or store them in memory. Data and programs might be stored in three dimensional crystals or holograms. Each image would consist of a large number of pixels (or bits) arranged in a checker board pattern; these pixels would be light beams that together make up the entire image. The logic gates in such a processor would perform a function on several of the pixels by combining those light beams directly in the material of the gate in such a way that a third beam is produced; this third beam would carry the result of the logic function. The logic gate would not require any conventional electronics to perform the logic function and it would also serve as the interconnection with the next plane.

Besides operating in a multi-planar environment, a smart pixel might be required to operate on light confined to travel in one of the 2-D planes described above. In this case, two light beams in the plane would converge on the smart pixel through individual optical waveguides, a third beam would be produced at the smart pixel as a result of the logic function, and the resulting beam would be sent out through a third optical waveguide. Of course, this scenario can be expanded to include some light beams confined to the plane and some traveling between planes. From this discussion, it can be seen that the

smart pixel is the key device which links opto-electronic computers of today with the all-optical computers of tomorrow.

Another type of smart pixel consists of an optical amplifier with an integrated spontaneous emission filter. In general, optical laser amplifiers are used to increase the amount of signal from a device or system for which the signal is conveyed by stimulated emission (laser beam). These amplifiers are common in fiber communication networks and switching systems, for example. The output from an optical amplifier generally consists of the amplified stimulated emission and also the unwanted spontaneous emission. The spontaneous emission occurs as a result of the random recombination of carriers in the laser amplifier.

Figure 1.1 shows possible plots of light intensity from a typical laser amplifier as a function of wavelength. The plot with a high Signal to Noise Ratio (SNR) level shows a large amplified signal compared with the spontaneous emission. The plot with the low SNR shows that the spontaneous emission has broad bandwidth compared with the smaller amplified signal. It should be emphasized that the noise in this discussion corresponds to the integral -- over wavelength -- of the spontaneous emission (total spontaneous power). The basic problem with detecting an optical signal with a low SNR is that a photodetector produces photocurrent that is orders of magnitude larger for the integrated spontaneous emission than for the amplified stimulated emission.

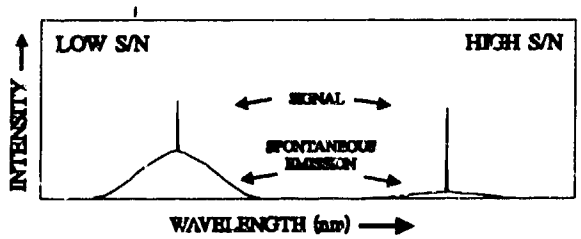

Figure 1.1: Typical spectra of the emission from an optical laser amplifier. The amplified signal is stimulated emission (1 or 2 angstroms wide) and the noise is spontaneous emission (approx. 300 angstroms wide).

Several techniques can be used to extract the optical signal from the noise. In the laboratory, the signal can be viewed on an optical spectrum analyzer with sufficient resolution. Lock-in amplifiers can also be used. Both of these are large, costly and slow. Another method uses holograms to redirect the laser light which results in spatial separation between the stimulated and spontaneous emission. However, the hologram introduces additional optical losses, it is large and mechanically unstable. In some applications, the optical signal must be electronically reconstructed to obtain the required amplification due to the large noise accrued by cascaded optical amplifiers. This reconstruction process consists of detecting the optical signal at a point of relatively large SNR, electronically amplifying and processing the detected signal, and then re-transmitting it through a laser.

The optical amplifier with an integrated spontaneous emission filter operates faster, cheaper and with much less complexity than the systems just described. It is small, has gain and is integrable with emitters, receivers, logic and analog signal processing circuits.

For functional systems, the same filtering can not be accomplished with any existing optical filters fitted to the output of an optical amplifier for two independent reasons: (1) these filters have band-pass characteristics insufficiently narrow to pass the laser signal while rejecting the spontaneous emission; (2) as the temperature of the optical amplifier shifts, the wavelength range of the spontaneous emission shifts outside the filtering range of a stand-alone bandpass filter.

The work presented in this technical report covers areas of research on smart pixels for digital and analog optical processing and communications. The focus is on optoelectronic devices that work as smart pixels without undue concern regarding speed and power during the initial phase of development. These devices rely on the interaction of light with charge to implement the desired functions. Unlike the all-optical device that combines several light beams in a small volume of material and produces a third light beam representing the result, these devices spatially separate the receive and transmit functions. Unlike the hybrid devices that have electronic logic gates to perform the logic, these devices perform logic by the unique combination of optical transmitters and receivers.

This report covers two devices first presented in patent disclosures. The second chapter covers the Configurable Optical Gates (COGs) that form the complete Diode-Laser Logic (DLL) family. The COGs consist of monolithically integrated, MultiQuantum Well (MQW), q-switched lasers with integrated photodetectors and current sources. The third chapter discusses Spontaneous Emission Filtered Laser Amplifiers (SEFLAs). The fourth chapter covers the fabrication sequence for both devices.

II. DIODE-LASER LOGIC USED FOR SMART PIXELS

Diode Laser Logic is a complete, new logic family comprised of Q-switched lasers and photodetectors. The lasers and detectors are monolithically integrated on multiple quantum well laser heterostructure with semi-insulating substrates. Preliminary results indicate an ON/OFF contrast ratio better than 500:1, gain in excess of 20 and variable I/O hysteresis characteristics. As a result, the devices can be cascaded to form more complex optical circuits. In addition to introducing the Diode Laser Logic family, a basic model is presented and the fabrication process is discussed.

A. THE DIODE LASER LOGIC FAMILY

The Diode Laser Logic (DLL) gates form a complete logic family for use as smart pixels and in optical signal processing applications.[1] The individual gates, Configurable Optical Gates (COGs), of the family can be interconnected to form more complex circuits such as fully integrated optical adders and crossbars; however, in many cases, the unique features of the family simplify the circuits to one or two COGs.

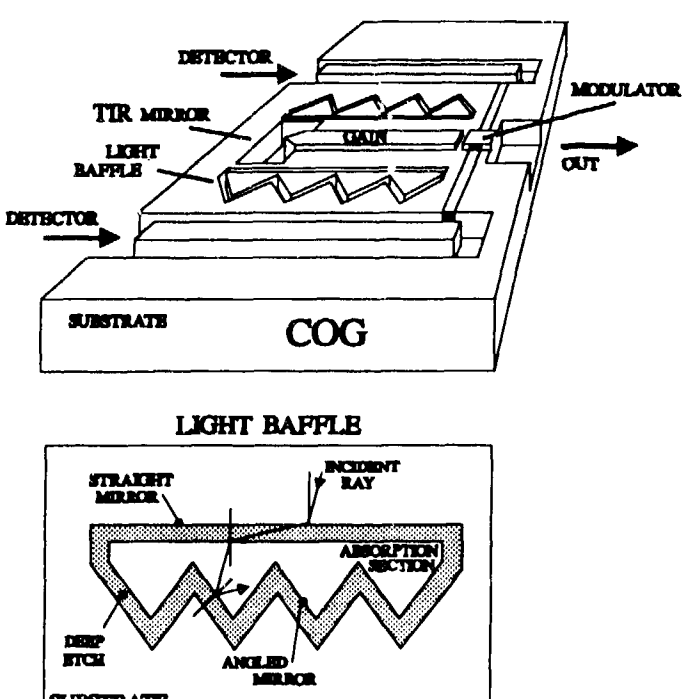

Figure 2.1: The top diagram shows a relief drawing of the NOR gate as an example. The anode of the modulator connects to the cathodes of the two photodetectors that are isolated from all other devices by a deep etch through the n-layer. The bottom diagram shows the light baffle that provides optical isolation between gain and photodetector sections.

Each COG consists of an integrated Multiple Quantum Well (MQW) Q-switched laser,[2,3] one or more integrated photodetectors[4,5] and, in some devices, an integrated current source. The Q-switched laser consists of a long gain section and a small modulator sandwiched between two etched mirrors. In general, the current source, which connects to the modulator, sets the state of the laser (ON or OFF). Photocurrent from the photodetector modifies the current and voltage at the modulator and, thereby, changes the state of the laser. Figure 2.1 shows a relief drawing for a typical COG with two optical inputs (photodetectors) but without the current source.

The laser consists of gain and modulator sections that are located between an etched Total Internal Reflection (TIR) mirror[6] on one end and an etched flat mirror on the other. The TIR mirror improves the efficiency of the laser by providing up to 100% reflectivity. In some devices, the TIR mirror is replaced by another flat mirror for a second output. The modulator and gain sections are separated by a shallowly etched region with an oxygen implant;[7] this region provides electrical isolation between the two sections without significantly altering the index of refraction. A large index difference would prevent the device from operating properly by introducing a partially reflecting surface there and possibly setting up sub-cavities.

Reverse bias on the modulator inhibits laser action by increasing the optical absorption within the quantum wells. Increasing the reverse bias on the modulator results in an increasing threshold current for the laser. The laser bias current, however, is fixed between the threshold currents set by a forward and reverse biased modulator. Thus, the bias voltage on the modulator determines the lasing state of the cavity.

INVERTER

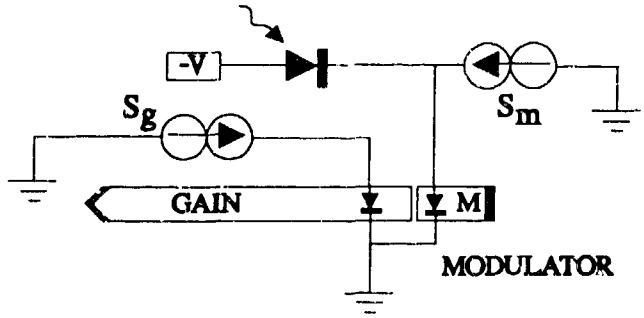

Figure 2.2: Schematic diagram of the inverter COG. For an optically unbiased detector, the current source S_m forward biases the modulator. The photodetector, with optical bias, sinks the current and reverse biases the modulator. The laser is ON and OFF respectively.

An optical inverter is shown in Figure 2.2. The cathode of the photodetector is electrically connected to the modulator. Under normal operating conditions, the anode of the photodetector and the n-layer are all grounded while the p-contact on the laser is positively biased. Without illumination on the photodetector, the modulator current source S_m forward biases the modulator and lowers the threshold current of the cavity; this causes the cavity to lase. The modulator current source is not actually needed in this circuit since emission from the gain section produces charge in the modulator

OR GATE

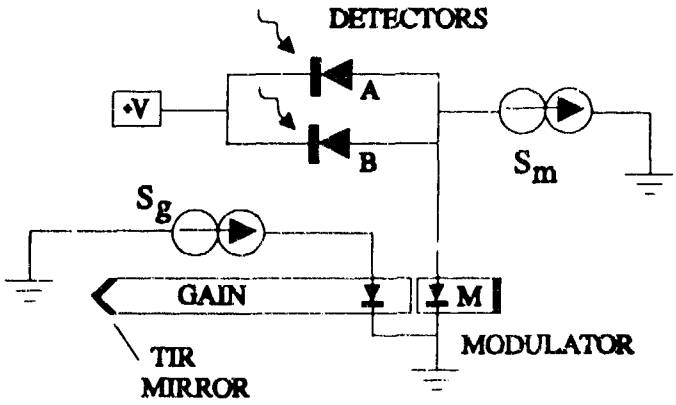

Figure 2.3: Without optical bias to the detectors, the current source S_m reverse biases the modulator. Optical bias applied to either detector produces sufficient photocurrent to satisfy the source and forward bias the modulator. The laser is OFF and ON respectively.

that can forward bias it. When the photodetector is illuminated, it sinks both the current from the current source and the photocurrent from the modulator. The modulator becomes reverse biased and the cavity quenches.

The COG version of the OR gate appears in Figure 2.3. When the photodetectors are not illuminated, the modulator current source reverse biases the modulator. The high threshold current prevents lasing. Illuminating either detector produces sufficient photocurrent to satisfy the current source and forward bias the modulator to allow the cavity to lase.

Two distinct versions of the AND gate are possible. The *series detector* configuration appears in Figure 2.4. The current source S_m reverse biases the modulator as before. A single illuminated photodetector forward biases itself and produces negligible photocurrent. Both detectors must be illuminated to satisfy the modulator current source and forward bias the modulator. The other AND gate configuration uses a dual modulator design that operates similarly to the OR gate previously discussed. One modulator is located at each end of the cavity. This second version has the disadvantage that the two modulators introduce higher cavity loss than the single modulator; thus, the lasing threshold currents are necessarily higher. However, when both ends of the cavity are to serve as outputs, the double modulator design has an advantage. The modulators absorb significant amounts of spontaneous emission when reverse biased. Thus, photodetectors coupled to each end of the cavity have higher on/off contrast ratios.

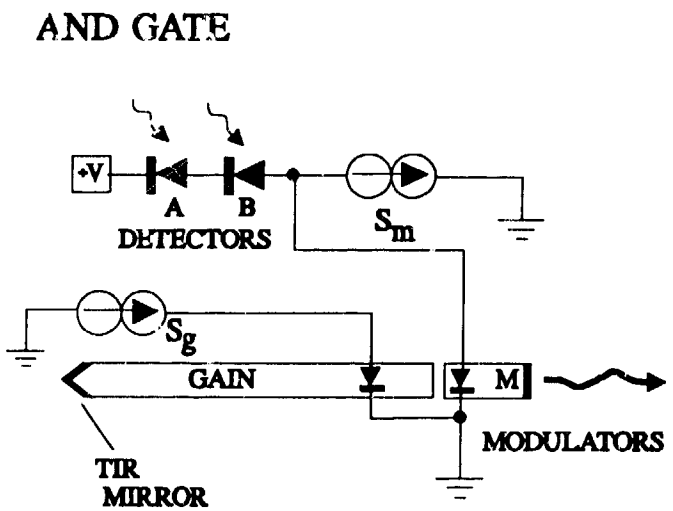

Figure 2.4: For the series-detector AND gate, both detectors must be illuminated for the laser to oscillate.

Only one version of the NAND gate (Figure 2.5) is possible with the fabrication techniques presently used. Any other design requires the cathode of the modulator to be electrically isolated from the cathode of the gain section. At present, deep etches through the active

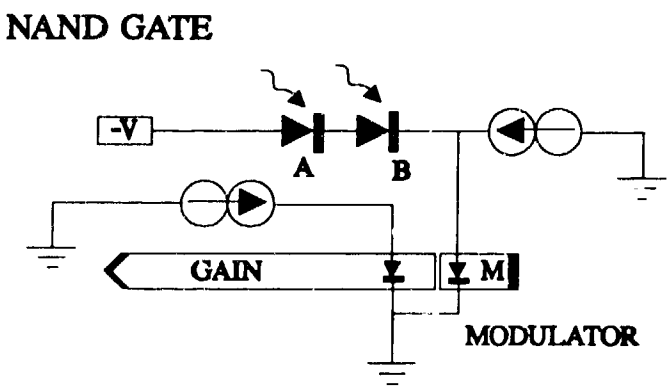

Figure 2.5: Both detectors must be illuminated for the gate to switch.

region are used to electrically isolate sections of the N-layer. Such an etch around the modulator introduces a mirror between the gain and modulator sections and, thereby, degrades the performance of the device.

NOR GATE

An optical NOR gate is shown in Figure 2.6. It operates similarly to the inverter except for the two photodetectors in parallel.

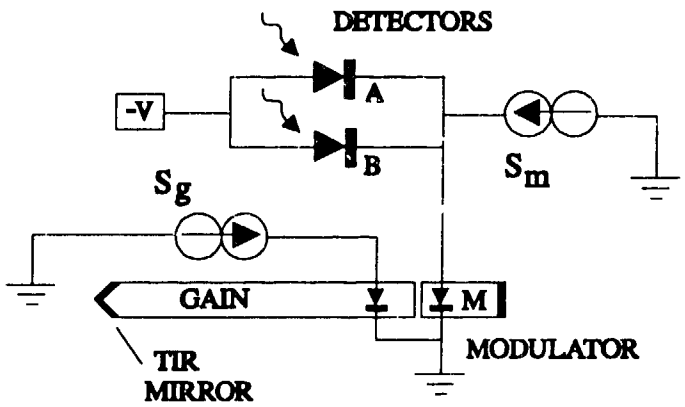

Figure 2.6: The optical NOR gate operates similarly to the INVERTER except for the two detectors in parallel.

A note is in order concerning the possible optical coupling between the laser and photodetectors. If necessary, a light baffle can be included with the device. The light baffle helps to optically isolate the detectors from the laser (refer to the close-up shown in Figure 2.1). The light baffle consists of two deep etch regions, two mirror surfaces and an absorption region with a metal electrode. The flat mirror totally reflects light with wave- vectors making more than a 17^{o} angle with respect to the normal; thus most of the stray light is reflected back. The light falling within the 17^{o} angle is refracted and enters the absorption region; the wave vector within this absorption region again falls within the 17^{o} of the normal to the flat surface. The absorption region reduces the intensity of light passing through it. The absorption is enhanced by applying reverse bias to the metal electrode on the top of the absorption section. The angled reflecting surfaces totally reflect the remaining light because the angle between the wave vector of this light and the normal to any of the reflectors is always larger than 17^{o}.

Elements of the DLL family can be combined to build larger circuits. With standard Boolean logic, on the order of 10 gates are required for a 2 X 2 CROSS BAR or an ADDER. Unique features of the COGs can be used to greatly simplify the designs. Any function that can be realized through Boolean logic can be implemented with the DLL family.

The integrated optical ADDER appears in Figure 2.7. The ADDER has two optical inputs and each has two photodetectors electrically isolated from one another on the P side. There are two output lasers. The one on the left (right) represents the *carry* (*sum*) bit. To illustrate how it operates, consider the following cases. CASE 1: Optical bias is not present on either set of detectors. In this case, the two modulators on the *carry* laser are reverse-biased. As a result, detector D5 is not illuminated and source S3 forward biases the top modulator on the *sum* laser. However the lower modulator is reverse-biased so the *sum*

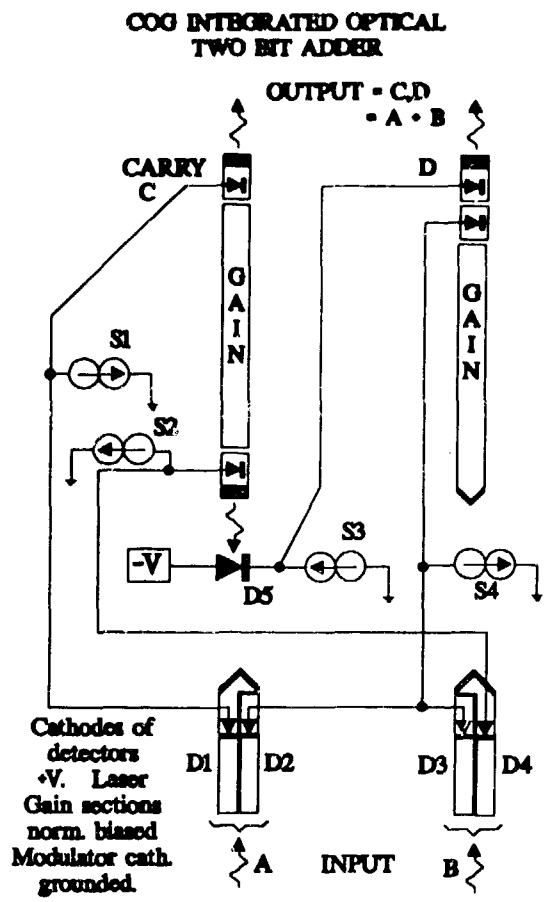

Figure 2.7: An integrated optical adder.

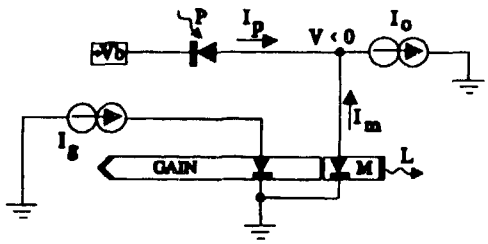

Figure 2.8: The basic circuit for the model of the COGs.

laser is off. CASE 2: Optical bias is applied to exactly one detector. The *carry* laser is quenched since only one modulator is forward-biased. Thus S3 forward biases the top modulator in the *sum* cavity. Light strikes either D2 or D3 so the lower modulator in the *sum* cavity is forward-biased. The *carry* laser is *off* and the *sum* laser is *on*. CASE 3: Optical bias is applied to both sets of detectors. Light incident on both sets of detectors causes both modulators on the *carry* laser to be forward-biased and the cavity lases. As a result, D5 reverse biases the top modulator on the *sum* cavity and the cavity does not lase.

B. MODEL

It is possible to provide a simple model for the operation of the COGs. The Q-switched laser consists of the gain and modulator sections. Due to a two-dimensional Franz-Keldysh effect, the optical absorption in the modulator increases with larger reverse-bias. The resulting photocarriers either recombine in the wells or tunnel through the barriers to be swept out.[8] The radiative recombination rate decreases with field in the well since the overlap of the electron and hole wavefunctions decreases. The tunneling rate increases exponentially with electric field because, at high fields, the barrier is triangular. Thus, the electric field in the modulator determines the ratio of recombination to sweep-out currents. For the modulators with a PIN structure, the application of bias voltage alters the existing built-in field and, thus, also, the ratio of currents. For a cavity to lase, its gain must balance out its losses. The loss in the cavity of the COG can be controlled with the voltage applied to the modulator because of the sweep-out process.

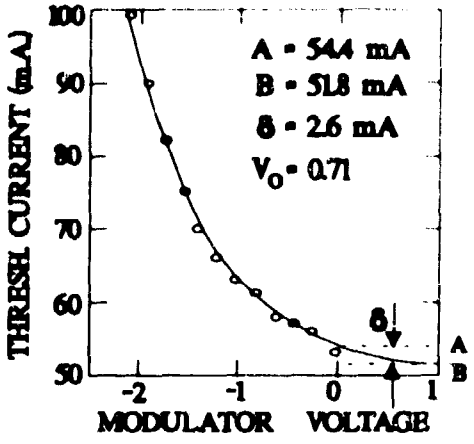

Figure 2.9: Typical threshold current data for a 20 μm X 20 μm modulator.

A simple model explains the operation of the COG shown in Figure 2.8. For a Q-switched laser near threshold, assume that the optical power through the modulator L is approximately related to the gain-section bias current I_g and the threshold current I_{th} by

$$L = L_o\left[\exp(I_g / I_{th}) - 1\right] \tag{2.1}$$

where L_O is a constant. Here, I_g is fixed and I_{th} is considered to be the variable since the switching is controlled by the modulator bias.

Referring to Figure 2.8, the photodetector and modulator are considered to be optically controlled current sources with some bias voltage dependence characterized by resistances R_p and R_m respectively. (Measured resistances might have some voltage dependence.) The currents I_m and I_p are both combinations of photocurrents and the reverse bias leakage current. It follows that

$$I_m = k_m L - \frac{V}{R_m}$$
$$I_p = k_p P - \frac{[V - V_b]}{R_p} \tag{2.2a,b}$$

where P is the optical power absorbed by the photodetector, k_m and k_p are constants. For large values of current from the I_0 source, the reverse bias voltage must be limited by additional circuitry to prevent break-down of the modulator and detector diodes.

Typical data for the threshold current vs. modulator bias voltage appears in Figure 2.9. The gain section is 20 μm X 200 μm and the modulator is 20 μm X 20 μm for the plot. The curve is best approximated by an exponential function:

$$I_{th} = \delta e^{\frac{-V}{Vo}} + b \tag{2.3}$$

where δ, V_O and b have the approximate values of 2.65 mA, 0.714 V and 51.85 mA respectively. These values change for smaller modulators and waveguides. The smaller devices yield the high gain quoted previously. The previous equations can be combined with $I_O = I_m + I_p$ to yield:

$$\exp(I_g / I_{th}) - \frac{V_o}{R_{//} k_m L_o} \ln \frac{\delta}{I_{th} - b} = 1 + \frac{I_o - k_p P}{k_m L_o} \tag{2.4}$$

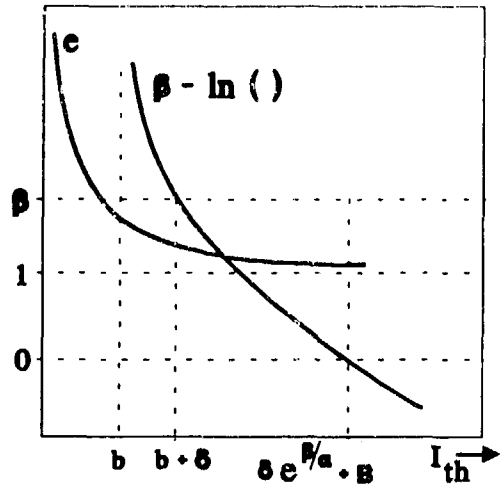

Figure 2.10: Both sides of equation 5 plotted on the same set of axes. The intersection is the threshold current.

where $R_{//}$ is the parallel combination of R_m and R_p and where V_b/R_p is negligible in comparison to I_o. This can be rewritten as

$$\exp(I_g / I_{th}) = \beta - \alpha \ln \frac{I_{th} - b}{\delta} \tag{2.5}$$

where

$$\beta = 1 + \frac{I_o - k_p P}{k_m L_o} \tag{2.6}$$

and

$$\alpha = \frac{V_o}{R_{//} k_m L_o} \tag{2.7}$$

Equation 2.5 can be interpreted as follows. β is the independent variable and I_{th} is the dependent one. The left-hand side represents the L-I characteristics. On the right-hand side, β represents the difference in the currents at the modulator. The logarithmic term is a result of the I_{th}-V characteristics for the Q-switched laser.

The left-hand and right-hand sides of equation 2.5 can be plotted on the same set of axes as shown in Figure 10. The effect on I_{th} of changing I_o or P is evident from the graph. Suppose, for example, that the power P incident on the detector increases. In this case, β will decrease and the LN curve shifts down and to the left. The intersection point moves to the left to indicate that the threshold current decreases. The other cases are similar.

There are two simplifying cases. The first occurs when the cavity is lasing (β near 1), i.e., for the approximate range of $b < I_{th} < b+\delta$:

$$I_{th} \cong b \tag{2.8}$$

The second case occurs for large β. Under this condition, the intersection point in Figure 10 is far to the right where $\exp(I_g/I_{th}) \cong 1$. This condition yields $I_{th} = \delta \exp(\beta/\alpha) + b$. Assuming $k_p P << I_o$ (i.e. the

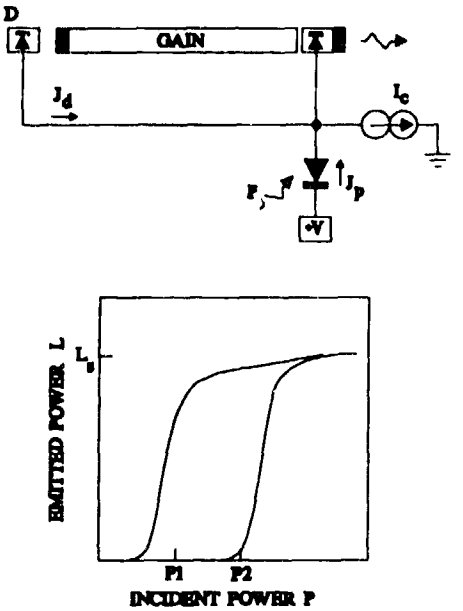

Figure 2.11: Positive feedback has been added in the top circuit to add control over the width of the hysteresis loop shown in the bottom part of the figure.

large β limit) and $k_m L_o << I_o$, β/α simplifies to $(I_o R_{//})/V_o$. Thus the threshold current for large β can be written as

$$I_{th} = \delta \exp(I_o R_{//} / V_o) + b \tag{2.9}$$

This equation is essentially the curve shown in Figure 2.9 where $I_o R_{//}$ is the voltage across the modulator. The laser is off in this case.

Hysteresis in the input-output characteristics can be adjusted by changing the geometry and bias of a photodetector D coupled to the output of a gate as shown in Figure 2.11. The photocurrent J_d is added to the input signal in a positive feedback arrangement. The length, bias and coupling of detector D can be adjusted. The branches of the resulting hysteresis curve for the circuit can be explained as follows.

As the input power increases along the lower branch up to point P2, the cavity produces spontaneous emission; the detector D produces photocurrent J_d that is small compared to the photocurrent $J_p = k_p P$ produced by input power P. The output power L remains small. At point P2, the photocurrent J_d is still small but J_p is sufficiently large to satisfy the current source. The cavity begins to lase.

$$J_p = I_c \text{ or } k_p P_2 = I_c \tag{2.10}$$

Thus,

$$P_2 = I_c / k_p \tag{2.11}$$

As the incident power P increases, the amount of gain available from the modulator will saturate. The output power L saturates at L_s for a given bias current to the gain section. Furthermore, L remains relatively constant along the top branch as the incident power is decreased to P1 since photocurrent J_d is also helping to satisfy I_c. As a note, the saturation intensity increases with bias current to the gain section. At power level P1, the lasing intensity decreases since the photocurrents are no longer large enough to satisfy the modulator current source (the reverse bias voltage across the modulator is limited by additional circuitry).

$$J_p + J_d \cong I_c \tag{2.12}$$

$$k_p P_1 + k_d L_s \cong I_c \tag{2.13}$$

where k_d accounts for the responsivity, coupling and the length of modulator D. Thus,

$$P_1 = \frac{I_c}{k_p} - \frac{k_d}{k_p} L_s \tag{2.14}$$

As the incident power continues to decrease past P1, the emitted power L also decreases. The width of the hysteresis loop is approximately the difference between P2 and P1.

$$Width \cong \frac{k_d}{k_p} L_s \tag{2.15}$$

The width of the hysteresis loop is controlled by changing the parameter k_d. This parameter increases with increased optical coupling between the laser and the detector and also with increased absorption within the detector due either to increased detector lengths or increased reverse bias. However, if this parameter becomes too large, then P1 becomes negative (i.e. Width > P2) which means that the laser can not be quenched by removing the illumination P from the photodetector.

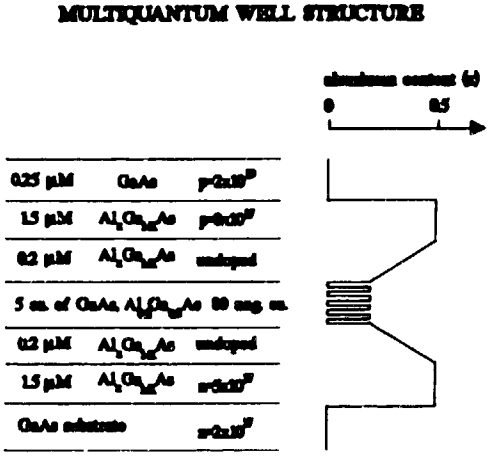

Figure 2.12: The heterostructure for the N-type substrates.

C. FABRICATION

The DLL family uses semi-insulating substrates; however, the preliminary devices described in the EXPERIMENTAL RESULTS section use N-type substrates. Similar processing is used on both types of substrates and the differences will be noted as the discussion progresses. Figure 2.12 shows the laser heterostructure, with five quantum wells, epitaxially grown on N-type substrates. Lasers fabricated on the heterostructure emit at 860 nm.

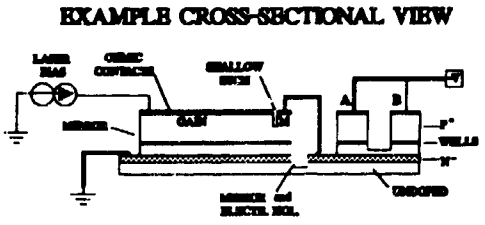

Figure 2.13: An example cross sectional view showing the various etches.

The wafers with the N-type substrate are processed as follows (See chapter IV for a complete discussion). The laser and photodetector waveguides are defined by photolithography with an image reversal process and the liftoff of a metallization layer. The metals, in the order evaporated onto the p-side of the wafer, are Ti, Pt, Au and Cr. The mirrors and waveguides are formed by etching the wafer in a Chemically Assisted Ion

Beam Etcher (CAIBE)[9] twice. The chrome in the metallization provides the etch mask and the edge of the Cr defines the mirror surface. For the first etch, a thick (3μm) layer of photoresist covers the wafer except in the regions of the deep etches. The photoresist is removed after the initial etch. The second etch, a shallow etch, forms the waveguides, the electrical isolation region between the modulator and gain sections and also continues the deep etch for the mirrors. The electrical isolation is accomplished with the ion implanting of oxygen[7] in the shallowly etched regions. Polyimide is spun on the wafer and vias are etched through the polyimide for electrical contacting. The polyimide acts as both an insulator for the electronics and a transparent dielectric for the optics. After the polyimide is fully cured, a final metallization is used for electrical connections. The wafer is thinned and an n-type Ohmic contact, consisting of Ni, Ge, Au, Ag and Au, is evaporated on the back surface. The devices are alloyed, cleaved and mounted in preparation for testing. For semi-insulating substrates, the above procedure is followed by a wet selective etch to expose the n-type GaAs, and the same photoresist mask is used to define the n-type contact by means of liftoff. Deep etches in the semi-insulating wafers extend into the substrate for electrical isolation between neighboring devices. An example cross-section of a semi-insulating device can be seen in Figure 2.13.

D. EXPERIMENTAL RESULTS

This section discusses the results from two prototype COGs with differing sizes for the gain and modulator sections. The larger laser cavity measures 20 x 200 μm with a 20 x 20 μm modulator while the smaller cavity measures 5 x 85 μm with a 5 x 5 μm modulator. An external current source and external silicon photodetector connect to the modulator. The device geometry is similar to that shown in Figure 2.1 except that (1) the light baffles are not required for the externally mounted photodetectors and (2) both mirrors are flat.

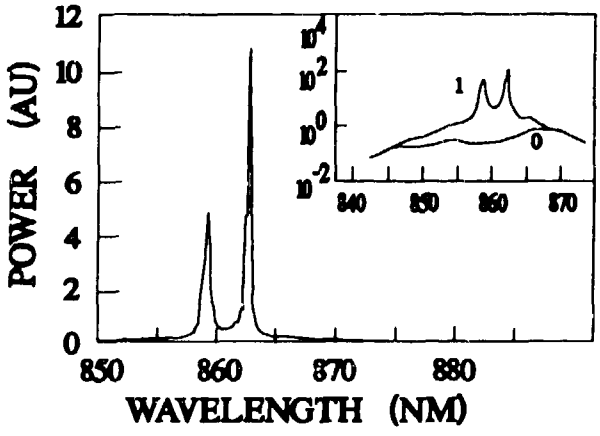

Figure 2.14: The emission spectrum for the larger COG in both the logic *0* and *1* states. The *0* state is coincident with the horizontal axis in the linear plot. The inset shows the semi-log plot of the two states. The *0* state corresponds to spontaneous emission which is 500 times smaller than the stimulated emission for the logic *1* state.

Several experiments were performed on the gates. (1) Optical logic was demonstrated. (2) Optical emission spectra were determined for the *0* and *1* logic states as proof of the switching. (3) The lasing threshold current of the laser as a function of modulator bias voltage was measured. (4) The responsivity of the integrated photodetectors was investigated. (5) The quality of the electrical isolation was ascertained. (6) The current vs. voltage (I-V)

characteristics of the modulator in forward and reverse bias were determined. (7) The gain of a gate was determined.

The optical logic was demonstrated by directing a HeNe laser beam onto the two photodetectors; the laser was switched *on* when either photodetector was illuminated. The modulator current source was set to 0.7 mA for the larger COG and 2 μA for the smaller one. The reverse bias on the modulator was limited to -4 V; this negative limit occurred when the current source could not supply the 0.7 mA due to the large reverse bias resistance of the diodes (modulator and photodetectors). The voltage to the gain section was pulsed to prevent thermal damage; the pulse width was 10 μs. When either photodetector was illuminated, the voltage on the modulator rose from -4 V to -0.1 V for the larger COG.

The emission spectra were obtained by directing the laser emission from the larger COG into a fiber and coupling the fiber to an Anritsu Spectrum Analyzer. The experimental conditions were the same as for the switching experiments. Figure 2.14 shows the emission spectra for both logic states. The spectrum for the *0* state (modulator reverse-biased at -4 volts) is essentially a straight line coincident with the horizontal axis. The inset to the figure shows the same data plotted in semilog format. The *0* state corresponds to spontaneous emission that is a factor of 500 smaller than the stimulated emission representing the *1* state (neg 0.1 V bias on the modulator). In addition, the modulator quite effectively absorbed most of the spontaneous emission that was incident on it (not shown).

The threshold current of the larger COG laser as a function of the modulator bias voltage was determined by applying a reverse bias voltage to the modulator, then noting the minimum current at which the COG laser would lase. The voltage applied to the gain section consisted of 60 Hz, full-wave rectified sinusoidal signals. Figure 2.9 shows the threshold current vs. modulator bias voltage. Note that a change of 2 Volts yields a factor of 2 change in the threshold current. As an example of modulator control, if the quiescent current of the laser is set to 60 mA, then modulator voltages larger than -0.75 V turn the laser *on* and voltages less than that turn the laser *off*.

The capacitance and response of the integrated photodetectors were investigated. The capacitance was verified to depend on the area of the electrode structure as 0.004 $pF/\mu m^2$ at a reverse bias of -5 V. The photocurrent was found to be essentially independent of the wavelength of incident laser light for wavelengths between 800 and 870 nm; beyond 870 nm, the response decreased. The photodetectors were found to be relatively linear in photocurrent vs. incident light intensity for a wide range of intensity.

The quality of the electrical isolation between the gain and modulator section was checked. As discussed previously, the electrical isolation between the two sections was formed by the new process of etching away the P^+ layer to within a few thousand angstroms of the active region and then implanting O_2 as a deep trap. Without the implant, the resistance was found to be 300 Ω to 1 KΩ. Figure 2.15 shows the I-V characteristics measured for this 2 μm wide region after the oxygen implant. The isolation resistance was thus determined to be about 1.7 MΩ.

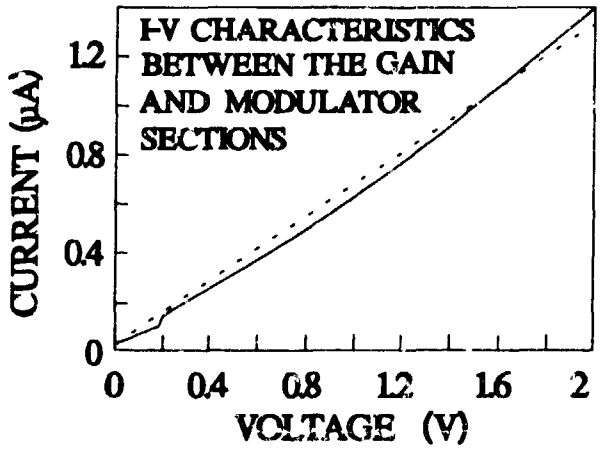

Figure 2.15: The I-V characteristics between the gain and modulator sections of the COG. The dotted line represents 1.7 MΩ for a 2 μm gap.

The reverse bias I-V characteristics of the modulator with the gain section floating were determined. For voltages in the range of $-5 < V < 0$, the resistance is larger than 3.5 MΩ. Thus, there are three sources for current flow to the modulator: leakage current between the gain and modulator sections; reverse bias leakage of the modulator; and the photocurrent produced in the modulator due to emission from the gain section.

The gain of the COG is defined as the ratio P_{out}/P_{in} where P_{out} is the intensity of the light emitted from the laser through the modulator, and P_{in} is the intensity of light absorbed in the photodetector that causes switching. For the COG, the gain is determined by the current from the current source. The photodetector must supply enough current to satisfy the current requirements of the source before the potential of the modulator can change. For unity quantum efficiency, the power of light absorbed must be

$$P_{in} = hcJ/e\lambda \tag{2.16}$$

where h, c, J, e, λ are Planck's constant, the speed of light in vacuum, the current through the current source, the electronic charge and the wavelength of light in vacuum, respectively.

The gain was determined for the smaller COG. The current source was set for 2 μA with a maximum reverse bias voltage of -4 V. The ON/OFF contrast ratio was better than 10:1. For these operating conditions, an input optical power of 4 μW switched the laser with an emitted optical power of 83 μW. These numbers correspond to a gain of 20.

E. SUMMARY

The DLL family is a new concept for optical computing and smart pixels. The features include: (1) an intra-cavity modulator that provides sensitive control of the laser output; (2) integrated detectors capable of being electrically contacted at both the anode and cathode; (3) integrated current sources; (4) substrates for complete isolation of individual components in the COG and for electrical connections between anodes and cathodes; (5) oxygen implanted shallow etches for electrical isolation between P^+ regions; (6) integrated light baffles employing Total Internal Reflection to prevent accidental optical coupling between the laser and detectors; (7) integrated photodetectors with wide optical bandwidth so that the transfer characteristics of the device are relatively independent of wavelength; (8) compatibility with silicon logic since only a lower voltage swing is required. For the first time, with the DLL family, integrated optical circuits can be fabricated. One key component is the intra-cavity modulator with the oxygen implanted shallow etches since it can control 10 to 20 fold more optical power at the COG output than is present at the input to the detectors as proved by the prototype device discussed above.

Since the modulator can be driven by a photodetector in reverse bias, a COG can be used as an optical amplifier. Linearity might be a problem for a small signal amplifier; however, for binary logic, the inverter COG can be used in a mode such that the laser is either *on* or *off*. The *on* state consists of maximum laser emission while the *off* state consists of spontaneous emission from the laser. However, the modulator absorbs most of the spontaneous emission and thus almost no light is emitted from the laser in the *off* state.

III. SPONTANEOUS EMISSION FILTERED LASER AMPLIFIER

The signal-to-noise ratio for optical laser amplifiers can be increased by orders of magnitude by actively filtering out the spontaneous emission from the output signal. The amplifier described here combines an optical amplifier with a spontaneous emission filter. The filtering function is accomplished by integrating the amplifier with a semiconductor laser in such a way that the signal in the amplifier suppresses the gain in the laser. Unlike conventional optical amplifiers,[10] these can in principle be cascaded without significantly decreasing the performance. The gain characteristics can be tailored during epitaxial growth for operation at a number of different wavelengths including 0.85 and 1.3 μm.

A. INTRODUCTION

One of several possible forms of the optical amplifier with a spontaneous emission filter appears in Figure 3.1. The minimum configuration of the device consists of two overlapping optical waveguides that are independently electrically pumped. One waveguide is the amplifier section. The other waveguide with its two mirrors forms a laser. The amplifier section provides normal signal amplification and quenches[11,12] off the laser. Each side of the amplifier makes a 2^{o} angle, as shown, for a couple of reasons: (1) the overlap with the laser section is increased, and so is the quenching efficiency; (2) the saturation characteristics of the amplifier are improved.[13] The absorber section reduces back reflections into the amplifier and reduces the necessity of Anti-Reflection (AR) coatings.

The device operates with the laser section biased above threshold, the amplifier section biased for optical gain and a laser signal applied to the input of the amplifier section. The relatively weak input signal, shown as the spectrum at the input in Figure 3.1, is amplified as it travels the length of the amplifier section. In addition to the amplified signal, the amplifier section adds spontaneous emission as shown by the spectrum at the junction between the amplifier and the laser sections. The stimulated emission from the amplifier quenches the laser and then enters the absorber region. The amplifier emission is absorbed in the absorber-section to prevent it from reflecting back into the amplifier; the back reflection would

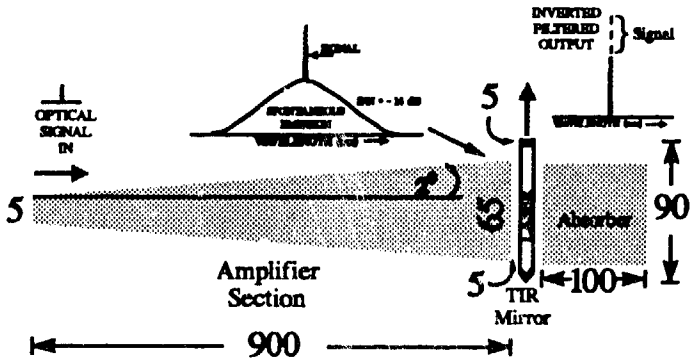

Figure 3.1: A prototype laser amplifier with a spontaneous emission filter. The spectra show the signals present at various points in the structure. The amplifier and laser sections are for signal amplification and filtered output, respectively. The sizes are in microns.

otherwise limit the useful gain of the amplifier. The absorber-section can be reverse-biased to further increase the absorption. The output from the laser decreases when the laser is quenched as shown by the dotted portion of the output spectrum in Figure 3.1. The section covering the experimental results further illustrates the quenching phenomenon.

It should be noted that this is an inverting amplifier. At quiescence, the filtered output produces a laser signal. However, with the input laser signal, the amplified signal quenches off the laser in proportion to the intensity of the stimulated component. Also note that the stimulated emission intensity from the laser is orders of magnitude larger than the spontaneous intensity because the carriers in the laser cavity preferentially recombine under the action of the impressed optical field to produce stimulated emission rather than recombining by the slower random process that produces spontaneous emission.

B. EXPERIMENTAL RESULTS

The quenching of one laser by another is the key to the operation of the spontaneous emission filter. To properly understand the quenching phenomenon, an experiment was performed using the proof-of-concept device shown in the inset to Figure 3.2. The device consisted of two GaAs-AlGaAs heterostructure lasers which emitted at 860 nm. The main laser was capable of being quenched off by the side quench laser. The quench laser was divided into two parts across the gain region of the main laser so that the quench and main laser cavities overlapped; the two halves of the quench laser were electrically connected in parallel.

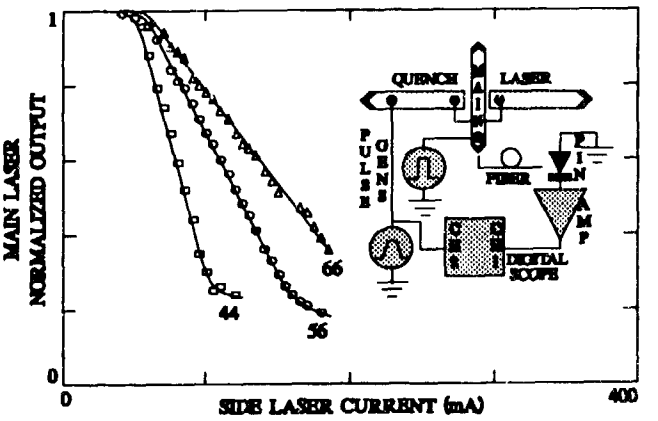

Figure 3.2: Normalized emitted optical power from the main laser of an optical inverter as a function of the current into the quench laser. The main laser had a 36 mA threshold current. The quench curves are parameterized by the current injected into the main laser: 44, 56 and 66 mA. The inset shows the inverter and the experimental setup.

The lasers employed near Total Internal Reflection (TIR)[14] mirrors to improve the laser threshold currents and decrease the power consumption of the device. The lasers had ridge waveguides and mirrors which were etched in a Chemically Assisted Ion Beam Etcher (CAIBE).

The laser quenching experiment[15] was performed as follows (refer to the inset to Figure 3.2). Both of the lasers were pulsed. A square voltage pulse was applied to the main lasers for 10 microseconds. During this time, a Gaussian pulse was synchronously applied to the quench laser for 10 microseconds. Light escaping from the tip of the main laser TIR mirror was coupled into a single mode fiber and routed

to a PIN photodiode circuit. Signals proportional to the emitted optical power and the current were plotted on a digital oscilloscope.

The graphs in Figure 3.2 show the optical power emitted from the main laser as a function of the current injected into the quench laser; the output power has been normalized to unity. The set of three curves was obtained from a proof-of-concept device with a main laser threshold current of 36 mA. The values of the current injected into the main laser parameterize the curves. The graph shows a linear decrease in the output intensity from the main laser as the side laser current increases. The linear portions of the curves occur for quench laser currents larger than about 40 mA, which corresponds to the threshold current for the quench laser. Note that the curves round-off at the bottom indicating a saturation of the quenching process. A maximum of approximately 80% of the optical power from the main laser can be quenched with the proof-of-concept geometry. Also note that the magnitude of the slope of the linear portion decreases for larger main laser currents. Thus, more side laser current is required for larger main laser currents in order to maintain a constant output power.

This plot can be re-interpreted in terms of the optical power emitted from the side laser as follows. The threshold current for the quench laser is near 40 mA. If the origin of the graph is translated to the right to that point then a change in quench laser output power is linearly related to the new variable I'=I-40mA (where I is the current into the quench laser). Changes in the output power from the quench laser (operated above threshold) then yield linear changes in the output power of the main laser (away from saturation). For a fixed change in the optical power from the quench section, the graph shows that larger currents injected into the main laser yield smaller changes in the output power of the main laser because the slopes of the quench curves in the linear regions approach zero.

The quench curves in Figure 3.2 consist of the Spontaneous Emission Region (SER), the Linear Region (LR) and the Saturation Region (SR). The SER corresponds to side laser currents smaller than about 40 mA; this region corresponds to the production of only spontaneous emission by the quench lasers. The optical power from the main laser can increase to values larger than 1 if the resistance between the main and quench lasers is sufficiently small or if the spontaneous emission from the quench laser aids the pumping of the main cavity. LR refers to the part of the graph where the optical power from the main laser linearly decreases. For this region, a photon from either the quench or main laser cavity can stimulate the emission of a photon from electron-hole recombination in such a way that the wave vector of this emission is parallel to either the quench or main laser cavity respectively. However, above threshold, the photon density in the quench laser is linearly proportional to the quench laser pump current. Thus the probability of interaction between the photons from the quench laser and electron-hole pairs in the common cavity increases linearly. As a result, the gain of the main laser linearly decreases to a fixed value. Main lasers operating at higher current densities require larger quench laser currents to

achieve the same amount of quench. SR refers to the region of the graph at which the emitted optical power saturates. The saturation level can be attributed to several effects. The volume of overlap between the main and quench laser cavities serves as a region of gain or loss for the main laser depending on the relative magnitudes of the two laser beams. For high quench laser powers, this common region decreases the gain of the main laser. If the volume of overlap between the main and quench laser cavities is small, the stimulated emission from the main laser cannot be totally suppressed. In this case, the main laser still lases at saturation. For large volumes of the common region, the bias current of the main laser cannot provide enough gain to compensate for the loss within the common region. In this case, the main laser only produces spontaneous emission at saturation.

C. DISCUSSION

In most actual analog and digital communications applications, optical fibers would be fitted to the input and output ports of the SEFLA. The quiescent laser intensity from the filtered output is set by the magnitude of current injected into the laser section. In some applications a Thermo-Electric (TE) Cooler could be added to keep the amplifier cool and to increase its mean time before failure.

It should also be noted that the amount of overlap between the quench section and the laser influences the gain at the filtered output as well as the observed saturation level at the filtered output; however, this overlap parameter is fixed during fabrication.

The most significant new feature of the amplifier is the spontaneous emission filter. For the first time, it is possible to amplify optical signals without introducing a high level of noise. Unlike previous optical amplifiers, these amplifiers can be cascaded without significantly increasing the noise level. It is now possible to amplify a signal in a low SNR environment with an optical amplifier, without complicated electronics. Optical signals can be reconstructed all-optically for either analog or digital communications. The amplifier with a spontaneous emission filter is faster, cheaper and much less complex than systems performing similar functions.

IV. THE FABRICATION OF GaAs OPTICAL CIRCUITS

This chapter discusses the design and fabrication of GaAs-based devices such as the COGs and the SEFLAs. In the first section, an overall view is given of the fabrication process and the CAD phase of the design. The remaining sections provide detailed fabrication data for the clean room phase.

A. THE CAD PHASE OF DESIGN

The fabrication process for the devices has four phases: (1) design and growth of the laser heterostructure; (2) design of the devices using Computer Aided Design (CAD) software; (3) fabrication of the wafer using clean room facilities; and (4) post-processing such as cleaving and mounting the devices. Obviously, the CAD design must take into account the other three phases of the fabrication process. The heterostructure design, for example, influences the number and type of masking steps drawn on the CAD. The equipment and processing steps in phase 3 determine the tolerance in the overlap of mask patterns as well as the number and type of such patterns. The cleaves and electrical contact points used in phase 4 must be drawn into the CAD diagram. Thus the CAD phase presumes knowledge of the entire fabrication process as well as the operational theory of the devices.

To fabricate the devices presented in this technical report, either four or five masking layers must be used depending on whether n-type or semi-insulating substrates are used, respectively. The masking levels can best be described with reference to an example. Suppose the example device is an etched ridge waveguide laser with etched mirrors and the heterostructure was grown on an n-type substrate. There are four masking levels: (1) p-contact; (2) deep etch; (3) via; and (4) top metal. The fabrication sequence appears in Figure 4.1. Subfigures C, E, G, and H show the CAD sequence while B, D, and F show the physical results after the corresponding fabrication. The first masking level defines the Ohmic contacts to the top p-type material and the waveguides. The CAD diagram appears as in Figure 4.1C. Photolithography and metallization steps produce the physical structure shown in Figure 3.1D. Next, the areas for deep etching are drawn on the CAD as shown in Figure 4.1E. The etch actually forms two separate regions during fabrication as depicted in Figure 4.1F. One region of the wafer is etched below the active layer so as to form the mirror surfaces at the ends of the waveguide. The other region is a shallow etch that defines the ridge for the waveguides. The shallow etch appears everywhere on the surface of the wafer except where the metal masks the surface. After the deep etches, oxygen is implanted for electrical isolation and a layer of polyimide is then applied across the entire top side. The polyimide improves the coupling between waveguides in the actual circuits and also provides electrical isolation for metal pads. Holes must be opened up in the polyimide above the waveguides for electrical connections as shown in Figure 4.1G for the vias. Finally, a top metallization mask defines the contact pads (Figure 4.1H). The metallization covers portions of the polyimide and makes contact with the exposed waveguides.

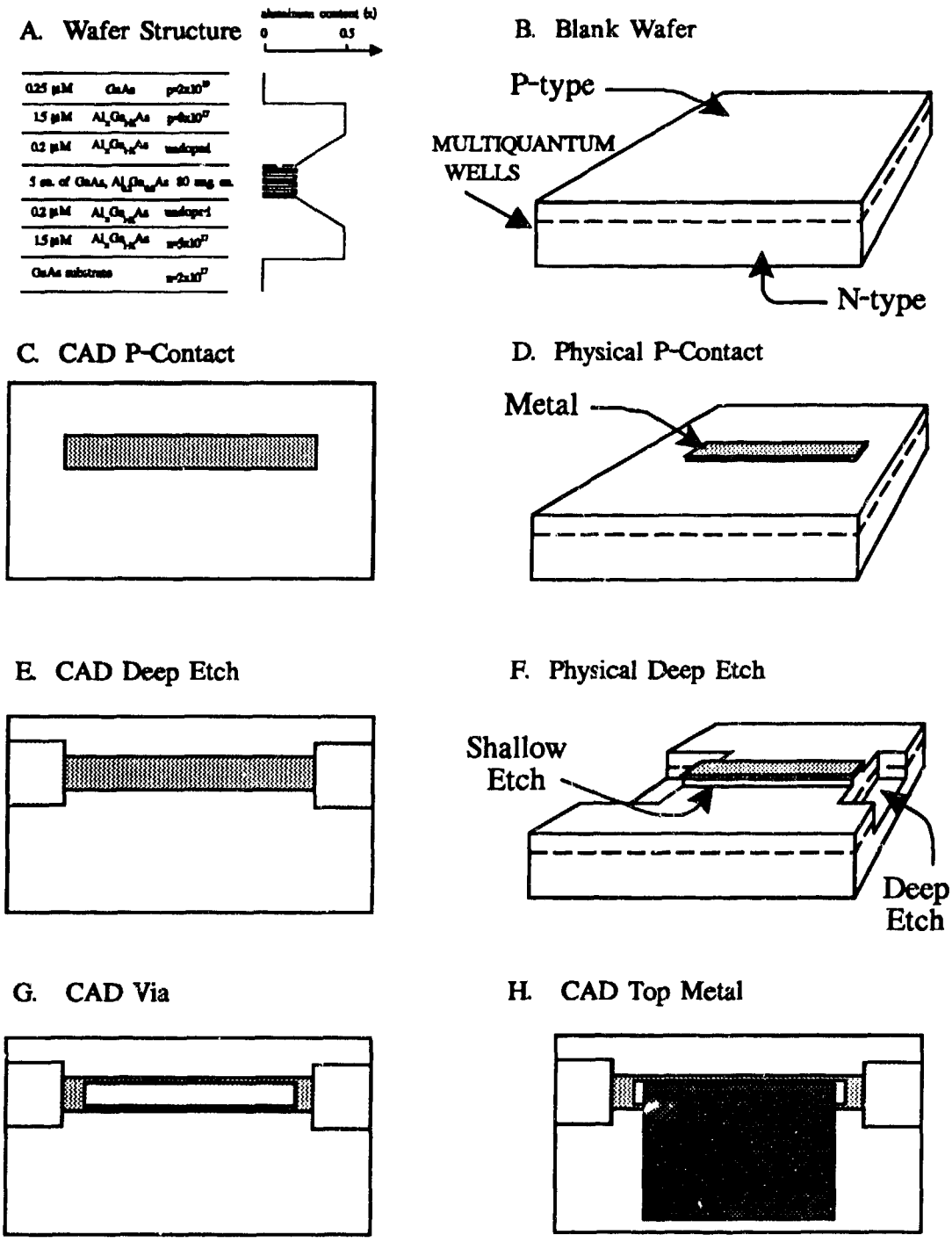

Figure 4.1: The processing sequence: subfigures C, E, G, H show the CAD design and subfigures B, D, F show the results of the processing. Subfigure A shows the wafer structure.

Electrical cross-overs can be made in the integrated circuit using the polyimide as the insulator between the two electrical traces. As a final note, the CAD design for semi-insulating substrates uses a fifth masking level for a wet etch to the n-type contact.

B. EVOLUTION OF THE FABRICATION PROCESS

The fabrication process has evolved over the past several years. Originally, the process began by coating the entire wafer surface with an insulating layer of SiO_2. Windows were then etched in this layer for p-contacts and mirror facets. After metallization, the Chemically-Assisted Ion Beam Etch (CAIBE) would be used to perform a vertical etch. The chrome etch rate in the CAIBE is much less than the etch rate of SiO_2, which is much less than that of GaAs. A single CAIBE etch could then produce a three-level topography.

This process was advantageous for simple geometries and devices, because the CAIBE etching could be performed in a single step. There were a few disadvantages to this method, however, as the device complexity increased. The first difficulty was alignment, since the processing sequence required tight tolerances in overlaying the metal waveguides on top of the SiO_2 windows. Secondly, the CAIBE etch rate widely varied, and it was difficult to predict the required etch duration to achieve the necessary depths. This lack of consistency was usually compensated by first etching a blank wafer as a calibration die. Thirdly, in the absence of a neutralizer filament, arcing became a problem on the wafer surface. It was conjectured that surface charge was building up on the sample as it was being bombarded with ions, since the SiO_2 was restricting charge dissipation through the wafer. This surface charge collected at windows in the SiO_2 (mirror facets), and arced to the GaAs substrate, destroying the wafer surface. These problems with the CAIBE etch were of great consequence, since the damage to the wafer occurred after the majority of the fabrication had already been completed. To bypass these processing problems, a new CAIBE sequence using different masking materials was developed.

The new processing sequence was actually devised as a method for fabricating devices on semi-insulating substrates, with contacts to both the p-doped and n-doped epilayers, but because of its success, it was implemented for use with n-substrate devices as well. It solves the alignment problem by putting down the chrome metal layer first. The deep-etch mask is then aligned to the metal, a step which does not require a time-consuming image-reversal, and does not require such tight tolerances. The CAIBE etch rate variation is corrected by replacing the single-step CAIBE procedure with a two-step process, whereby the first etch can be used to calibrate the required duration of the final etch. The arcing problem has been averted by switching from an insulating SiO_2 layer to a photoresist etch mask. Finally, the CAIBE etch

comes earlier in the overall fabrication process, so wafer damage in the CAIBE is less costly in terms of time and expense.

The overall clean-room process, then, for the *n-substrate* devices consists of initially cleaving and cleaning the wafer, applying metal ohmic-contacts for waveguides, masking the wafer for the deep etch, performing the dual etch in the CAIBE, improving electrical isolation by oxygen implantation, adding a polyimide insulating layer, opening vias in the polyimide, placing metal contact pads, thinning the wafer, applying the n-contact metallization to the back side, and finally alloying the metal contacts.

The process used for *semi-insulating* substrates differs only in that the n-contact metallization is performed following a wet etch between the oxygen implant and the polyimide, rather than towards the end. The contact pads for the n-contacts can be placed in the uppermost plane with the p-contact pads.

C. WAFER CLEAVING AND CLEANING

After scribing and cleaving the epitaxially-grown MQW wafer to a manageable size (typically 1-cm square), the sample is cleaned with a specific sequence of solvents: trichloroethane (TCE), acetone, methanol, de-ionized water, and finally isopropanol. The wafer is first sprayed with TCE, which removes grease from the wafer surface. Acetone is the next solvent used; it dissolves organic compounds, but leaves a residue behind as it dries. Methanol is therefore used to rinse off the acetone, but it also leaves a film behind. De-ionized water is used to drive off the methanol. The final rinse is with isopropanol, which dries in sheets, rather than droplets. The isopropanol is blown off the wafer surface with a nitrogen pressure gun, leaving a surface clean of dust and organic contaminants.

Photolithography and material deposition require baking the wafer above the vapor point of the solvents to remove any residual moisture. The wafer is placed in a convection oven at 100 - 150°C for at least 30 minutes.

D. APPLICATION OF OHMIC-CONTACT WAVEGUIDES

As shown in Figures 4.1C and D, the metal waveguides are the first fabrication level. Besides being the ohmic p-type contact for the laser diode devices, this metallization serves as an etch mask during the CAIBE etch, as well as an implant mask during the oxygen ion implantation. The processing sequence to apply the p-contacts begins with a shallow zinc diffusion to improve the ohmic contacts. This is followed by photolithographic pattern transfer, and an image reversal of the photoresist. The image reversal is required to produce an undercut in the photoresist for easy removal of the unwanted metal areas (see

Figure 4.2B). Next, the metals are applied by electron-beam evaporation, and finally a liftoff technique is used to remove the unwanted metal.

Zinc Diffusion

The GaAs surface can be more highly p-doped by diffusing zinc into the lattice. This creates better Ohmic contacts for the waveguides. This is the first process step, after initially cleaning the wafer, so the zinc diffusion is not masked. The entire wafer surface thus becomes more highly doped. This does not cause interference between devices, however, because the wafer surface between devices is later etched in the CAIBE to a depth surpassing the diffusion depth of the zinc. Also, the effect of the zinc diffusion on the back surface of the wafer is unimportant, since the back side is lapped down later in the fabrication process. The diffusion is performed by placing the wafer in a carbon susceptor with a solid zinc-arsenide source in a 650°C oven, with a hydrogen atmosphere, for 9 minutes, resulting in a diffusion depth of about 300 nm.

Photolithography and Image Reversal

The waveguide pattern is transferred to the wafer using photolithographic techniques. After applying an HMDS primer (20% hexamethyldisilazane), a 1.25-μm layer of photoresist (KTI-895i 16.5cs) is spun on at 4000 rpm for 30 seconds, and pre-baked at 90°C for 50 seconds on a hot-plate. The photoresist is exposed in a 10x magnification, i-line stepper for 0.3 seconds.

An image reversal process is performed on the exposed photoresist in preparation for liftoff of the first metallization. If the photoresist were to be developed immediately following exposure (the normal photolithography process), the sidewalls of the pattern would be vertical, as shown in Figure 4.2A. This profile is not acceptable for metal liftoff, as it allows the metal to cover the wafer in a continuous film. During liftoff, this tends to cause peeling of the metal from surfaces where adhesion is intended. The image reversal process causes an undercut slope in the photoresist sidewalls, as shown in Figure 4.2B, resulting in better metal liftoff. The image reversal is accomplished by performing an ammonia diffusion into the photoresist, followed by a 90-second ultraviolet flood exposure of the entire wafer surface. The ammonia diffusion causes a chemical reaction in the photoresist, hardening the areas which have been previously exposed, and leaving unaffected the unexposed areas. The flood exposure has no effect on the hardened resist, but exposes the remaining wafer area, which can be subsequently removed by developer.

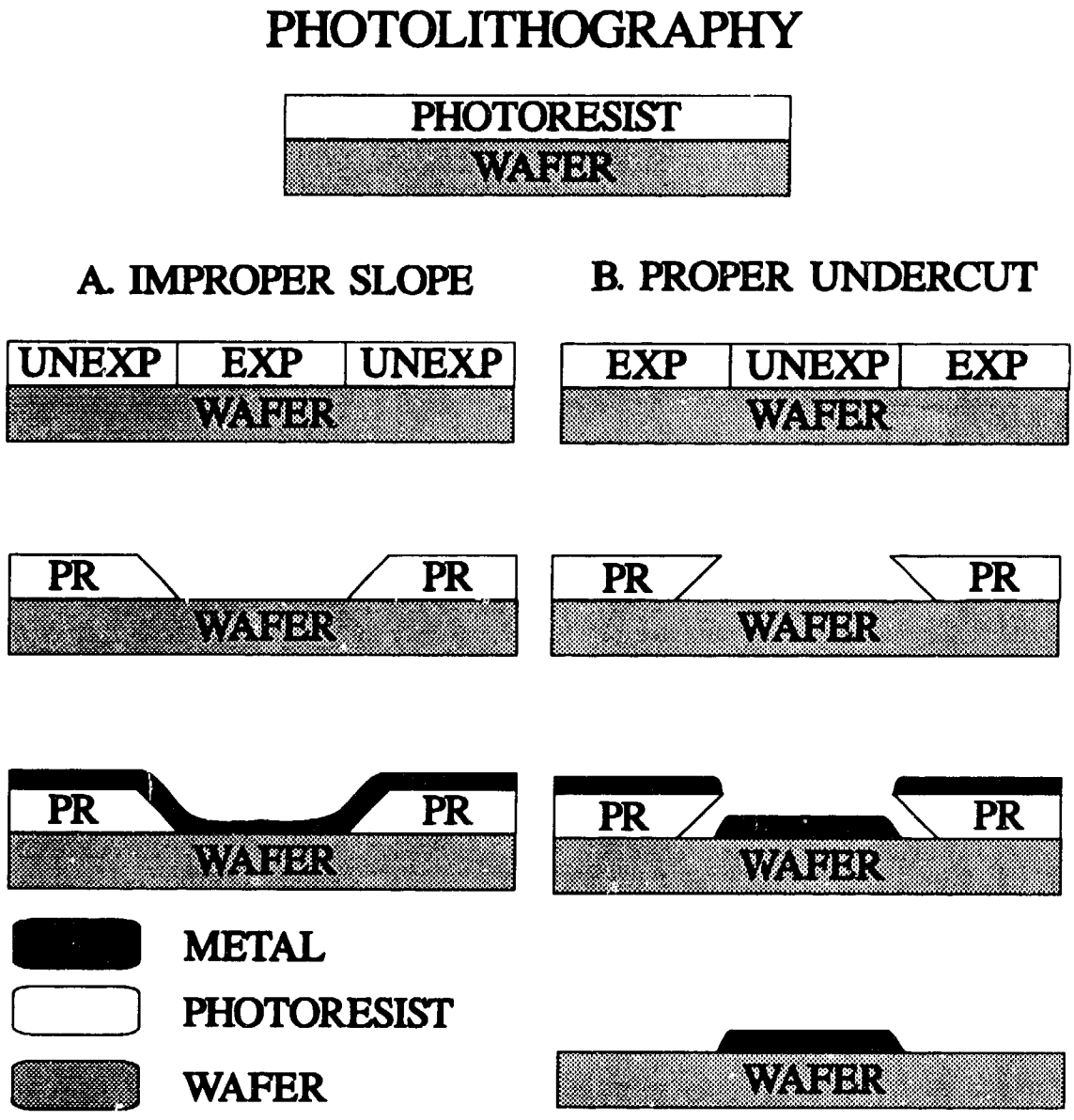

Figure 4.2: The Photolithography Process. The left side (part A) shows a view of the results for a normal photolithography process, while the right side shows the image-reversed photolithography process. The metal liftoff works more efficiently with the proper undercut than it does with the process depicted on the left side. [Exp = exposed, Unexp = unexposed]

The image reversal is followed by developing the photoresist in OCG 945 developer for 1.5 to 2 minutes. This opens the windows in the photoresist for waveguide metallization. To ensure that the photoresist is completely removed from the GaAs surface in each of the windows, a short, low-power plasma "descum" etch is performed in a Reactive Ion Etcher (RIE). The descum consists of an oxygen plasma (30 sccm O_2, 30 mT chamber pressure) at 0.15 W/cm^2 for 15 seconds, long enough to descum photoresist residue without risking damage to the pattern.

Metallization and Liftoff

To prepare the GaAs surface for metal adhesion, the wafer is dipped in a 10% solution of ammonia hydroxide for 10 seconds. This chemical removes surface oxides, after which the wafer is immediately loaded into the electron-beam evaporator. The p-contact metals are evaporated onto the wafer in a specific sequence to promote adhesion, and alloyed later in the fabrication process for optimal conductivity.

The p-contact metallization consists of 400Å titanium, 200Å platinum, 3000Å gold, 1500Å chromium, 500Å nickel, and another 1500Å chromium. The titanium is a buffer layer which adheres well to the GaAs surface. Platinum is used as a diffusion barrier for the gold during the alloy step. Gold is the primary metal for conduction and the main mask for the oxygen implant. Because gold is rapidly etched in the CAIBE, however, a chrome layer is added as the etch mask. Nickel is inserted midway into the chrome layer to reduce strain.

The metallization pattern is completed by performing a liftoff step. The photolithographic image reversal creates undercut sidewalls in the photoresist. This causes gaps between the metal on the GaAs surface and the metal overlaying the photoresist, facilitating the removal of the unwanted metal areas. The liftoff is performed by soaking the wafer in acetone, which dissolves the photoresist and carries with it any overlaying metal. It is often necessary to encourage the chemical process by agitating the surface in an ultrasonic bath. Shipley 1165 Stripper can also be used in place of acetone to accomplish the liftoff. After liftoff, the wafer is washed in the solvent sequence described above (see Section C) to remove any metal fragments clinging to the surface. Since the photoresist is hardened by the temperatures in the evaporator, an oxygen plasma descum in the RIE is necessary to completely remove the photoresist from the wafer surface. Usually, another low-power oxygen descum is used for 1 minute. A full-power (0.25 W/cm^2) oxygen plasma is not used because of the risk of chrome sputtering, which then masks further CAIBE etching. This damage appears as "grass" or "trees" grown on the etched GaAs surface, as shown in Figure 4.3.

E. TRANSFER OF THE DEEP-ETCH MASK

The second major processing step is to transfer the deep-etch mask to the wafer. As mentioned in Section B, we have switched from SiO_2 to photoresist for the mask material because of arcing problems in the CAIBE. However, it has been conjectured that in the CAIBE process, photoresist reacts with the chlorine gas, resulting in an organic by-product which partially masks the CAIBE etch.

The deep-etch mask transfer therefore begins with the application of a thin protective material over the entire wafer surface. This is followed by the photolithography process. For proper CAIBE etching of the mirror cavities, however, both the photoresist and the protective layer must be patterned with the deep etch windows. These windows are shown in Figure 4.1E.

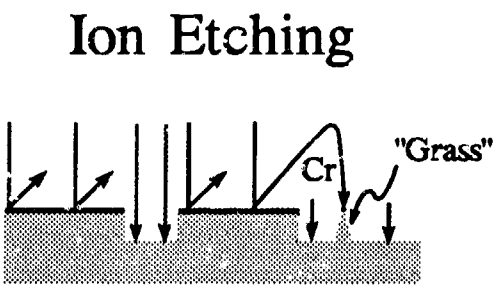

Figure 4.3: The Ion Etching Process. Chemically reactive ions etch unmasked portions of the surface. Collisions between ions and the Cr masking atoms cause sputtering and result in "grass."

Thin Protective Layer

Amorphous silicon is the material used for the protective layer. The thickness of the layer can be quite small, typically 500 - 1000Å. The material is applied in a plasma-enhanced chemical vapor deposition (PECVD) chamber prior to putting down photoresist for the deep-etch mask. In the PECVD, a silane gas plasma (SiH_4) is used (24 sccm SiH_4, 550 mT chamber pressure, 80 mW/cm^2 RF power) with a wafer temperature of 200°C, resulting in a deposition rate of about 160Å/minute.

Photolithography and Reactive Ion Etch

The deep-etch pattern is transferred to the wafer photolithographically. The process is similar to the photolithography step described above for the waveguide pattern, with a few exceptions. Since the photoresist itself is used as a mask in the CAIBE, it needs to be considerably thicker. A more viscous photoresist is used (KTI-895i 50cs), which when spun at 4000 rpm, results in a layer thickness of 2.5 μm. Also, since this pattern is not used for image reversal and liftoff, a different exposure and developing process is used. The pattern is exposed for 1.0 second, then immediately developed in OCG 945 for 60 seconds. The developing process opens windows in the photoresist where deep etches (mirror facets) are desired. Once again, to ensure that the photoresist windows are cleanly opened, a 15-second low-power oxygen plasma descum is performed in the RIE.

The same deep-etch windows also need to be opened in the protective layer underlying the photoresist before etching in the CAIBE. This is accomplished in the RIE chamber, using the photoresist layer as a

mask. An SF_6 plasma is used (20 sccm SF_6, 20 mT chamber pressure) at 0.15 W/cm^2, resulting in an etch rate of 1000Å/minute. Although the plasma is more selective towards the material used for the protective layer, photoresist is nonetheless slowly etched at the same time. This is another reason why the photoresist layer must be so thick.

F. CAIBE ETCHING

The CAIBE etch is one of the most important steps in the fabrication process. It is used to create a three-level topography for the laser devices. This topography is made up of the waveguides, shallow etches, and deep etches. The CAIBE achieves very-high-quality vertical etches in GaAs by directing an ion beam normal to the surface, and enhancing the etching by also directing reactive gases (namely chlorine) at the surface.

The shallow etch is the most critical because it delineates the optical mode. A secondary purpose of the shallow etch is electrical isolation between devices, but this is additionally aided by oxygen implantation later in the fabrication process. For optimal mode shaping, the shallow etch should be to within 100 nm of the quantum-well active region. This requires a shallow etch of 1.6 - 1.7 μm for the structure shown in Figure 4.1A.

The CAIBE deep etch provides mirror-quality vertical laser facets. To operate like a mirror, the etch must go deeper than the active region carrying the laser beam. Optimal results are obtained by taking this etch well into the n-doped epilayer. Typical deep etches are around 4.0 μm for *n-substrate* wafers. For *semi-insulating* wafers, the deep etch is taken down into the substrate to provide electrical isolation between the n-contact regions.

The etching process occurs in two steps. The first step, using the photoresist deep-etch mask, etches the mirror cavities to the difference (2.2 - 2.5 μm) between the shallow and deep etch depths. At this point, the wafer is taken out of the CAIBE chamber, and the photoresist mask and underlying protective layer are removed. At this point, the etch depth should be measured, since the CAIBE etch rate varies. The etch depth can be easily measured on an Alpha-Step Surface Profiler, giving an accurate method of calculating the etch duration for the more critical shallow etch. The entire wafer, delineated by the chrome mask, is then placed back into the CAIBE chamber and further etched for the shallow depth. In this way, the mirror cavities are ultimately taken to their final etch depth. With completion of both CAIBE etches, the wafer has features like those shown in Figure 4.1F.

CAIBE Etching Procedure

To prepare the GaAs surface for the CAIBE etch, the wafer is again dipped in a 10% solution of ammonia hydroxide for 10 seconds to remove surface oxides. The wafer is then mounted to an electrode with an electrically-conductive adhesive (tradename MUNG), and loaded into the CAIBE chamber for etching.

The CAIBE computer control is programmed to use an ion beam potential of 500 V, and an ion current density of about 0.1 mA/cm^2. This low current density is important, since the etch mask is photoresist, which can be damaged with too much energy. For the same reason, the substrate temperature is set no higher than 90°C. The computer is also programmed to provide a chlorine stream of 9 mL/minute, and an argon stream of 2 mL/min, which are directed at the wafer surface. These parameters have been shown to yield a GaAs etch rate of about 70 nm/minute.

Once the computer control is programmed, the CAIBE machine automatically governs the etch, controlling the ion beam, gas flows, and shutter.

Removal of Photoresist Mask and Protective Layer

As mentioned above, between the two CAIBE etches, the photoresist mask and protective layer must both be removed. The photoresist is removed by first washing in acetone, using the ultrasonic bath if required, then using an oxygen plasma. The RIE chamber can be used to remove the remaining protective layer, in the same manner that the deep-etch windows were initially opened in this layer. The resulting wafer has metal waveguides and partially-etched mirror cavities. After measuring the etch rate, the wafer is returned to the CAIBE for the second etch.

G. OXYGEN ION IMPLANTING

Devices on the wafer are isolated in two ways. The first isolation method is the shallow CAIBE etch described above, which physically delineates the device structures. Better electrical isolation, however, is achieved by implanting oxygen ions into the p-type semiconductor. With the shallow etch, the ions can be implanted down to the quantum-well region without destroying the metallization for the p-type Ohmic contacts. This has the effect of greatly increasing the resistivity of the semiconductor material between devices. Three implants are performed: a dosage of 10^{12} ions/cm^2 at 60 kV, a dosage of 10^{12} ions/cm^2 at 120 kV, and a dosage of 10^{13} ions/cm^2 at 180 kV. All three implants are at normal incidence.

H. APPLICATION OF N-CONTACT METAL (Semi-Insulating Substrate)

When fabricating devices on a *semi-insulating* substrate, it is necessary to make metal contacts to the n-doped epilayer. To accomplish this, vias must first be etched down to the n-doped layer before the metallization is performed. *N-substrate* wafers, on the other hand, do not require this procedure, since the entire back plane is n-doped and serves as a common ground plane. This section, therefore, applies only to fabrication on semi-insulating substrates.

Wet Selective Etch

The pattern for the n-contact vias is transferred to the wafer by photolithography. The same procedure is used as for the deep-etch windows, leaving holes in the photoresist where n-contact vias are desired. After an oxygen plasma descum to ensure clean windows, a wet chemical etch is performed which selectively etches AlGaAs faster than GaAs. The wet etch produces tapered sidewalls in the GaAs, facilitating metallization between the top surface and the n-doped layer, as shown in Figure 4.4. The faster etch rate for AlGaAs ensures that the etch will stop when it reaches the GaAs n-doped layer. A final advantage of the wet etch is that it creates an undercut in the GaAs beneath the photoresist which facilitates metallization liftoff.

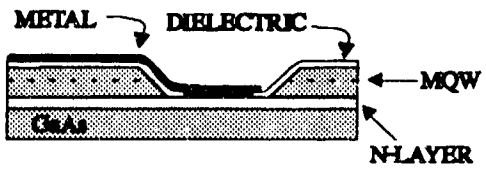

Figure 4.4: The wet selective etch creates tapered sidewalls for electrical contact between the top-metal and the n-layer.

The wet selective etch consists of 1 part methanol and 3 parts water, which are first mixed; then 1 part hydrogen peroxide and 1 part phosphoric acid are added to the mixture. The solution etches GaAs at 0.8 μm/minute, and AlGaAs at 4.0 μm/minute. The etch does not significantly affect the photoresist mask.

Metallization

The metallization procedure is nearly identical to the procedure outlined above for the p-contact metal, the only exception being the types of metals used. Immediately prior to metallization, an ammonia hydroxide dip is performed to remove surface oxides. The metallization sequence for n-type Ohmic contacts is 100Å nickel, 400Å germanium, 800Å gold, 500Å silver, and a final cap of 800Å gold. Germanium diffuses into the GaAs during a later alloying step as an n-type dopant for better Ohmic contacts. Nickel keeps the metal from forming "puddles" during the alloy. Gold and silver are the primary low-resistance metals for good conductivity. The unwanted metal is then removed with a liftoff procedure. The same photoresist n-contact mask which was used for the wet etch is used as the soluble liftoff layer.

I. POLYIMIDE INSULATING LAYER

A layer of polyimide is added to the wafer surface for two reasons. First, it acts as an insulator between the underlying structures and the contact pads which are to be placed on the uppermost layer. It also works as a planarizer, smoothing out the multi-level topography of the device structures for better metallization. The polyimide material must be chosen to have the same thermal expansion coefficient as GaAs to prevent strain during device processing and operation. We have used a 3-μm thickness of PIQ-L100 polyimide with good results.

The processing sequence for adding a polyimide layer begins with application of the coupling solution and the polyimide itself under specific conditions. The Via pattern, as shown in Figure 4.1G, is then transferred to the polyimide using the RIE.

Application and Curing of Polyimide Layer

The wafer is first washed in the standard solvent sequence described above (Section C), then baked at 150°C for 30 minutes to drive off moisture. A PIQ Coupler is then spun on while the speed is ramped from 1000 to 4000 rpm, for a total spin time of 90 seconds. The Coupler is cured at 350°C for 60 minutes in a hydrogen atmosphere. The PIQ-L100 polyimide is then spun on with a 2-minute spin sequence: 30 seconds at 2000 rpm, then 80 seconds more at 2000 rpm illuminated by an IR lamp, and finally 10 seconds at 5000 rpm under the IR lamp. The polyimide-coated wafer is baked at 90°C for 30 minutes, then at 200°C for 60 minutes in a convection oven.

Plasma Etch Windows (Vias) through Polyimide

The vias through which the contact pads meet the waveguides and n-contacts are patterned on the wafer using photolithography. KTI-895i 50cs photoresist is spun on at 2000 rpm for 30 seconds, yielding a photoresist thickness greater than 3 μm. Because of the thickness of the resist, the exposure time is increased to 2.0 seconds. A post-exposure bake at 90°C for 60 seconds on a hot-plate is performed to further harden the photoresist.

The polyimide vias are etched in the RIE with the following recipe: 30 sccm O_2, 2.0 sccm CF_4, chamber pressure of 30 mT, RF power 0.25 W/cm^2, for an etch duration of 6.5 - 7.5 minutes. This plasma also etches the photoresist mask at nearly the same rate, which is the reason such a thick layer is used. After stripping the photoresist mask in acetone, a low-power oxygen plasma descum is performed for 60 seconds to completely remove any photoresist residue. The polyimide is then subjected to a final curing cycle of 350°C for 60 minutes in a hydrogen atmosphere, followed by another low-power oxygen descum for 60 seconds.

J. APPLICATION OF TOP-METAL CONTACT PADS

With the insulating polyimide layer covering all underlying structures, contact pads can be placed on top of the polyimide without interfering with the devices below. The contact pads, shown in Figure 4.1H, only make contact to the underlying p-type or n-type metals where vias are etched through the polyimide. By strategically placing the vias, contact pads can be enlarged to cover the entire wafer area, facilitating electrical probing during test and evaluation. Additionally, if electrical crossovers are required in the device design, one leg can be routed up to the top-metal plane to bypass the other leg. The top-metal contact pads are added to the wafer with photolithography and the liftoff process.

Contact Pad Pattern

The contact pad metallization is added to the wafer using an image-reversal and liftoff procedure similar to the p-contact metallization process. The only difference is that a thicker photoresist is used because of the larger vertical profile over which the metal is being applied. KTI-895i 50cs is spun at 3000 rpm for 30 seconds, resulting in a thickness of about 2.8 μm.

Metallization, Liftoff

The top-metal contacts are applied with a metallization sequence of 500Å chromium, 3000Å silver, and 1000Å gold. The chrome is used to make the contacts stick to the polyimide surface. The thick silver layer is used primarily for economy, and the gold cap is applied to prevent oxidation and for later wire bonding. The unwanted metal between contact pads is then removed with the standard liftoff process of washing in acetone, followed by the solvent sequence and an oxygen plasma descum.

K. LAPPING THE WAFER TO FINAL THICKNESS

After the completion of all front-face patterning, the wafer is lapped down to an appropriate thickness. Thinning the wafer facilitates cleaving of the individual devices. On *n-substrate* wafers, thinning also lowers the series resistance of the devices by shortening the conduction distance through the semiconductor. Finally, lapping also improves heat dissipation, by bringing the devices closer to the heat sink. The final wafer thickness is determined by the feature size. Normally, wafers are lapped to a thickness of 10 mils (250 μm). If the cleaves are to be less than 500 μm apart, however, the wafer thickness is taken down to 4 mils (100 μm).

The wafer is mounted face-down on a chuck with white wax. The back side of the wafer is then manually circulated on a glass counter covered with a 3-μm alumina grit. The thickness of the wafer is gradually

reduced, with periodic measurements of progress. Upon completion, the wafer is removed from the chuck by melting the wax, and washed vigorously in acetone in an ultrasonic bath.

L. N-CONTACT METALLIZATION (N-Substrate)

As outlined in Section H above, the n-contacts for devices on *semi-insulating* substrates are metallized from the top. N-contacts for devices on *n-substrate* wafers, however, cover the entire back side of the wafer. Although this facilitates metallization of the n-contact, a disadvantage is that the n-contact cannot be patterned. The n-substrate is thus used only when a continuous ground plane can be used for all devices.

The n-contact metallization for n-substrate devices is accomplished following the lapping process. The metallization is essentially the same as for the semi-insulating substrate devices, except that there is no patterning or liftoff; the metallization is applied to the entire back side permanently. The sequence of metals used for the n-contact is the same as for the semi-insulating n-contacts: 100Å nickel, 400Å germanium, 800Å gold, 500Å silver, and a final cap of 800Å gold.

M. ALLOY METALS

At the completion of the final metallization procedure, an alloy step is performed to eliminate the Schottky barrier in the n-contact, making it Ohmic. The alloy is accomplished by placing the wafer in a 360°C oven for 60 seconds. This causes the germanium to diffuse into the GaAs at the n-contacts, and allows the metals to blend, decreasing any discontinuities. At this point, the samples are ready for final cleaving and mounting.

REFERENCES

1. M. A. Parker, P. D. Swanson, S. I. Libby, "Configurable Optical Gate For Use as a Smart Pixel," Patent Disclosure, Feb. 1993. Inquiries should be addressed to RL/JA, GAFB, NY 13441.
2. G. J. Lasher, "Analysis of a Proposed Bistable Injection Laser," Sol. State Electr., 7, 707 (1964).
3. C. Harder, K. Y. Lau, A. Yariv, "Bistability and Pulsations in Semiconductor Lasers with Inhomogeneous Current Injection," IEEE J. Quant. Electr. QE-18, 1351 (1982).
4. P. D. Swanson, "Characteristics of Semiconductor Optical Waveguides Fabricated by Impurity Induced Layer Disordering," Ph.D. thesis, University of Illinois, Urbana-Champaign, 1989.
5. C. M. Herzinger, P. D. Swanson, K. T. Tang, T. M. Cockerill, L. M. Miller, M. E. Givens, T. A. DeTemple, J. J. Coleman, J. P. Leburton, "Electroabsorption Properties of a single GaAs Quantum Well," Phys. Rev. B, 44, 13478 (1991).
6. W. Jung, Y. Kwon, "Nonlinear Quenching in a Monolithically Integrated Semiconductor Laser Logic Device," J. J. Appl. Phys. 28, L1242 (1989).
7. S. J. Pearton, M. P. Iannuzzi, C. L. Reynolds, L. Peticolas, "Formation of Thermally Stable High-Resistivity AlGaAs by Oxygen Implantation," Appl. Phys. Lett. 52, 395 (1988).
8. A. M. Fox, D. A. B. Miller, G. Livescu, J. E. Cunningham, W. Y. Jan, "Quantum Well Carrier Sweep Out: Relation to Electroabsorption and Exciton Saturation," IEEE J. Quant. Electr. 27, 2281 (1991).
9. W. J. Grande, J. E. Johnson, C. L. Tang "Characterization of Etch Rate and Anisotropy in the Temperature-Controlled Chemically Assisted Ion Beam Etching of GaAs," J. Vac. Sci. Technol. B8, 1075 (1990).
10. GTE Laboratories Inc., *Optical Amplifier Study*, Final Report for RL-DCLW contract number F30602-87-C-0107, March 1989. GTE Laboratories Inc., 40 Sylvan Rd., Waltham MA 02254.
11. G. J. Lasher, *Analysis of a Proposed Bistable Injection Laser*, Solid State Electronics 7, 707 (1964).
12. W. J. Grande, *A Study of Gallium Arsenide - Aluminum Gallium Arsenide Semiconductor Laser Devices for Monolithic Integrated Optical Circuits.* PhD. Dissertation, Cornell University (1989).
13. L. Eastman, private communication, Dept. Electrical Engineering, Phillips Hall, Cornell University 14853
14. W. Jung and Y. Kwon, Jap. J. Appl. Phys. 28, L1242 (1989).
15. M. A. Parker, S. I. Libby, P. D. Swanson, *An Optical NOR Gate Based on GaAs-AlGaAs Heterostructure Lasers.* June 1992 C3I Conference and Proceedings held at SUNY Tech. Univ. in Utica NY.

*U.S. GOVERNMENT PRINTING OFFICE

MISSION

OF

ROME LABORATORY

Mission. The mission of Rome Laboratory is to advance the science and technologies of command, control, communications and intelligence and to transition them into systems to meet customer needs. To achieve this, Rome Lab:

a. Conducts vigorous research, development and test programs in all applicable technologies;

b. Transitions technology to current and future systems to improve operational capability, readiness, and supportability;

c. Provides a full range of technical support to Air Force Materiel Command product centers and other Air Force organizations;

d. Promotes transfer of technology to the private sector;

e. Maintains leading edge technological expertise in the areas of surveillance, communications, command and control, intelligence, reliability science, electro-magnetic technology, photonics, signal processing, and computational science.

The thrust areas of technical competence include: Surveillance, Communications, Command and Control, Intelligence, Signal Processing, Computer Science and Technology, Electromagnetic Technology, Photonics and Reliability Sciences.