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STANDARD REQUIREMENTS FOR SOLDERED ELECTRICAL AND ELECTRONIC ASSEMBLIES

Approved by:

Director Manufacturing Technology Department (MT)

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FOREWORD

1. This technical report was developed as a draft Revision B of MIL-STD-2000. Standard Requirements For Soldered Electrical And Electronic Assemblies. It was developed as part of a triservice and industry development effort. As such, it should be suitable for procurement by all Departments and Agencies of the Department of Defense.

2. The Office of the Under Secretary of Defense (OUSD(PR)) determined that issuance of a Revision B to MIL-STD-2000 would not be in concert with the current OUSD goal of transitioning to commercial standards. As such, coordination of Revision B was discontinued.

3. After careful review of the available industry standards, the Navy Electronics Assembly Technology Working Group determined that the currently available industry standards can be used only with significant tailoring and supplementation. As such, a transition document was required to support immediate procurement needs associated with the elimination of ozone depleting solvents, implementation of alternative fluxes (i.e., water soluble and low residue fluxes (no-clean)), and the need to return to a single set of requirements for all Navy procurement.

4. This technical report was developed to act as a temporary means to support Navy procurement during the OUSD led effort to transition to industry standards.

5. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commanding Officer, Naval Air Warfare Center, Highway 547, Code MT14, Lakehurst, NJ 08733-5100.

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1. SCOPE

1.1 <u>Scope</u>. This standard establishes requirements for materials and procedures for making acceptable soldered connections in electrical and electronic assemblies. Soldered connections for components (with or without leads) and wires inserted in holes, surface mounted to lands, or attached to terminals shall be in accordance with this standard. In addition, component mounting requirements and acceptance criteria are provided to permit evaluation of complete assemblies.

1.2 <u>Applicability</u>. The requirements of Appendix D are applicable only when it is specifically invoked in the contract, a drawing, or the detail specification.

1.3 <u>Discrete device exclusion</u>. The manufacture of discrete devices, microcircuits, multichip microcircuits, and film microcircuits is outside the scope of this standard. Unless specifically required by contract, this document is not intended for application to the manufacture of transformers or similar magnetic devices (see 6.1).

1.4 Other applications.

1.4.1 <u>Nonelectrical soldered connections</u>. Soldered connections utilized to join surfaces in nonelectrical applications shall be in accordance with DOD-STD-1866.

1.4.2 <u>High frequency applications</u>. High frequency applications (i.e., radiowave and microwaves) may require part spacings, mounting systems, and assembly designs which vary from the requirements stated herein. When high frequency design requirements prevent compliance with the design and part mounting requirements contained herein, manufacturers may use alternative designs with prior approval of the government procuring activity.

1.4.3 <u>High voltage or high power applications</u>. High power applications such as high voltage power supplies may require part spacings, mounting systems, assembly designs, and soldering techniques which vary from the requirements stated herein. When high voltage or high power design requirements prevent compliance with the design and part mounting requirements contained herein, manufacturers may use alternative designs with prior approval of the government procuring activity.

1.4.4 <u>Fine gauge magnet wire applications</u>. The mounting and processing of fine gauge magnet wire which is 28 AWG or smaller shall be in accordance with either the requirements of this standard or a documented specialized technology procedure in accordance with 4.1.4.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 <u>Specifications, standards and handbooks</u>. The following specifications, standards and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of

Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATIONS

FEDERAL

- QQ-S-571 Solder, Electronic (96 to 485°C)
- MILITARY
 - MIL-F-14256 Flux, Soldering, Liquid, Paste Flux, Solder Paste and Solder-Paste Flux, (For Electronic/Electrical Use) General Specification For
 - MIL-C-28859 Connector Component Parts. Electrical Backplane, Printed Wiring, General Specification for
 - MIL-A-28870 Assemblies, Electrical Backplane, Printed Wiring; General Specification for
 - MIL-I-46058 Insulating Compound. Electrical (for Coating Printed Circuit Assemblies)
 - MIL-P-50884 Printed Wiring. Flexible and Rigid-Flex
 - MIL-P-55110 Printed Wiring Boards, General Specification for
 - MIL-S-83519 Shield Termination. Solder Style. Insulated. Heat-Shrinkable, Environment Resistant, General Specification for

STANDARDS

MILITARY

- MIL-STD-202 Test Methods for Electronic and Electrical Component Parts
- MIL-STD-275 Printed Wiring for Electronic Equipment
- MIL-STD-750 Test Methods for Semiconductor Devices
- MIL-STD-883 Test Methods and Procedures for Microelectronics
- MIL-STD-1686 Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts. Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (Metric)
- DOD-STD-1866 Soldering Process, General (Non-electrical) (Metric)
- MIL-STD-2118 Flexible and Rigid-Flex Printed Wiring for Electronic Equipment, Design Requirements for
- MIL-STD-2119 Design Requirements for Printed-Wiring Electrical Backplane Assemblies

MIL-STD-2166 Connections, Electrical, Compliant Pin

HANDBOOKS

MIL-HDBK-263 Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) Metric

MIL-HDBK-2000 Soldering of Electrical and Electronic Assemblies

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building #4, Section D, Philadelphia, PA 19111-5094.

2.2 <u>Nongovernment publications</u>. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN NATIONAL STANDARDS INSTITUTE

ANSI/J-STD-003 Solderability Test for Printed Wiring Board

(Application for copies should be addressed to the American National Standards Institute, 11 West 42nd Street, New York NY 10036.)

INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS (IPC)

- IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits
- IPC-D-275 Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies
- IPC-DW-425 Design and End Product Requirements for Discrete Wiring Boards
- IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards
- IPC-HM-860 Specification for Multi-layer Hybrid Circuits

(Application for copies should be addressed to the Institute for Interconnecting and Packaging Electronic Circuits, 7380 North Lincoln Avenue, Lincolnwood, IL 60646.)

2.3 <u>Order of precedence</u>. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document supersedes applicable laws and regulations.

3. TERMS AND DEFINITIONS

3.1 <u>Terms and definitions</u>. In addition to those listed below, the definitions applicable to this standard shall be in accordance with IFC-T-50.

3.1.1 <u>Capability</u>. A measurable property of a process which is in statistical control and produces output which falls within specification limits.

3.1.2 <u>Charred</u>. Burned or blackened. This is damage beyond simple discoloration.

3.1.3 <u>In-statistical-control</u>. The condition describing a process which exhibits stability and minimized variability, and remains predictable over time.

3.1.4 Low residue soldering process. An integrated process resulting in very low residue levels which, after the assembly and soldering processes, minimizes subsequent cleaning operations. This process typically includes preasembly cleaning and non-contaminating cleaning.

3.1.5 <u>MELF</u>. MELF denotes devices with <u>Metal EL</u>ectrode <u>Face</u> bonding as the termination attachment.

3.1.6 <u>Prior approval</u>. This refers to any of the approval processes which are permitted or defined in the contract. Prior approval may be granted in the form of technical direction letters, deviations, waivers, or any other document specified in the contract.

3.1.7 <u>Rework</u>. Rework is the repetition of prior operation the use of alternate operations to bring an item into conformance (see 4.3.8).

3.1.8 <u>Stacking (piqgybacking)</u>. A technique of mounting components in which the component leads or terminations are attached to the leads or terminations of another component.

3.1.9 <u>Statistical process control</u>. The use of statistical techniques to analyze a process or its outputs to take appropriate actions to achieve and maintain a state of statistical control and to improve the process capability.

3.1.10 Touch-up. Touch-up is rework (see 3.1.7 and 4.3.8).

4. GENERAL REQUIREMENTS

NOTE: Guidance on the manufacture of electrical and electronic assemblies may be found in MIL-HDBK-2000.

4.1 <u>Interrelation of applicable documents</u>.

4.1.1 <u>Conflict</u>. In the event of conflict between the requirements of this standard and the applicable assembly drawing(s), the applicable approved assembly drawing(s) shall govern. In the event of conflict between the requirements of this standard and an assembly drawing that has not been approved by the government. differences shall be referred to the designated government activity for approval. Upon such approval, the provisions shall be

officially documented (by notice of revision or equivalent) on the assembly drawing(s) which shall then govern.

4.1.2 <u>Existing designs</u>. The requirements of this standard shall not constitute the sole cause for redesign if the design has been approved. However, when existing designs undergo change which impacts hardware configuration, the design should be reviewed and changes made that allow for maximum practical compliance with the requirements of this standard.

4.1.3 <u>Requirements flowdown</u>. The applicable requirements of this standard shall be imposed by each contractor on all applicable subcontracts and purchase orders. The contractor shall not impose or allow any variation from this standard on subcontracts or purchase orders other than those which have been approved by the government for the applicable prime contract.

4.1.4 <u>Specialized technologies</u>. Mounting and soldering requirements for specialized technologies not specified herein shall be considered unique and shall be identified on the drawing and performed in accordance with documented processes which are subject to review.

4.1.5 <u>Assembly drawing additions</u>. This document requires that areas of risks, special part mounting requirements, and other configuration related information be added to the assembly drawing. It is recognized that for some programs, the cost of even minor drawing additions may be quite large. As such, unless otherwise specified in the contract, where contractors are required to make drawing additions by this document, they shall first provide the change information to the procuring activity, and unless directed otherwise, make the drawing additions in accordance with the contract requirements for drawing changes.

4.2 <u>Visual aids</u>. Line drawings and illustrations depicted herein are provided as aids for determining compliance with the written requirements of this standard. The written requirements take poincedence.

4.3. <u>Product integrity requirements</u>. Assemblies which contain defects shall be rejected and either reworked to conformance or processed in accordance with the contract requirements for non-conforming material. The contractor is responsible for identifying other areas of risk (critical parameters). Such items shall be documented on the assembly drawing (hardware characteristics) or process documentation, as applicable. In performing this risk identification, the contractor shall consider product operational environment and contractor manufacturing risks associated with assembly design and fabrication tecnniques.

4.3.1 <u>Workmanship</u>. Workmanship shall be of a level of quality adequate to assure that the processed products meet the performance requirements of the engineering drawings and the criteria specified herein. Rework of soldered assemblies shall be minimized since any heating cycle may induce damage that could affect product reliability.

4.3.2 <u>Process documentation</u>. The contractor shall prepare, maintain and conform to documented procedures for all processes, inspections and tests required in this standard.

4.3.3 <u>Implementation of corrective action</u>. The contractor shall establish and maintain a system which shall identify and properly disposition nonconforming material. This system shall ensure that cost-effective corrective action is taken to minimize the occurrence of defects.

4.3.4 <u>Defect occurrence rate definition</u>. The defect occurrence rate for a manufacturing operation is a percentage (%) rate calculated by dividing the number of defects resulting from the manufacturing process by the normalizing number for that assembly (i.e., part number, assembly number, etc.). This normalizing number is the total number of terminations plus the total number of parts. For plated-through holes, the top and bottom of the plated-though hole shall be considered one integral connection. References to defect rate thresholds within this document are to the defect rate for the entire, integrated manufacturing process. As part of the process control system, the contractor may calculate rates for individual manufacturing processes (steps) (e.g., initial machine soldering of most parts followed by hand soldering of subsequent heat sensitive parts) and the normalizing number should be calculated based upon only those parts affected by the manufacturing operation.

4.3.5 <u>Conformance verification</u>. The contractor shall be responsible for conformance to the product and process requirements specified in this standard. All process and product inspections and tests required by this standard shall be performed either directly or by subcontract. The contractor may use his own or any other facilities suitable for the performance of the

ispection requirements specified herein unless such other facilities are uisapproved by the Government. The Government reserves the right to perform an audit or survey to assure that the supplies and services conform to the prescribed requirements.

4.3.6 <u>Product inspection</u>. The contractor shall estallish and maintain a system which shall identify and properly disposition nonconforming material. The contractor may use a sample based inspection approach provided that the contractor demonstrates that the manufacturing process is achieving a defect occurrence rate (as defined in 4.3.4) of less than or equal to 2.700 parts per million (ppm). The contractor may use a one-hundred percent inspection approach at any time, but must use a one-hundred percent inspection approach when the defect occurrence rate is greater than 2.700 ppm. Automated inspection may be used with either the sample based or one-hundred percent inspection approaches (see 4.3.8.3).

4.3.7 <u>Inspection</u>. The acceptance criteria of this standard require evaluation of hardware characteristics for acceptance. Where a characteristic is not clearly rejectable, it shall be accepted. See 4.3.8 for inspection and 4.3.8.4 for magnification aids.

4.3.8 Inspection of soldered connections and assemblies. Assemblies shall be inspected to assure conformance with the end-item requirements of this document and the assembly drawings. Sampling or one-hundred percent inspection of all solder connections and assemblies shall be performed. During inspection, the contractor shall document the occurrence of all defects. Rework shall not be performed until the defects have been documented. This data shall be used to provide an indication of possible causes and to determine if corrective actions are required.

NOTE: Throughout this document, part mounting and solder fillet requirements contain dimensions in the form of actual numbers and percentages. Except for referee purposes. actual measurement of these dimensions is not required provided the contractor has implemented a system of periodic verification to ensure conformance. Where actual measurements are performed, nominal dimensions specified in the part drawing may be substituted for actual measurement of hidden (e.g., underside metallization) dimensions.

4.3.8.1 <u>Hidden connections</u>. Component side connections on densely populated printed wiring assemblies and hidden connections shall be inspected to the extent that the component side connections are visible provided that:

- a. it may be demonstrated to the government that the design does not prevent adequate solder flow to any connection element on the component side of the assembly:
- b. the visible portions of the connection (both component and solder side) fully conform to the requirements specified herein; and
- c. process controls are maintained in a manner assuring repeatability of assembly techniques.

4.3.8.1.1 <u>Connectors with hidden cavities</u>. When connectors contain hidden cavities (for stress relief and to facilitate solder flow) (see figure 1) which preclude visual inspection to the criteria contained herein, acceptability of hidden connections shall be based on verification that the connector design includes internal provision for stress relief and cavities which permit solder flow.

4.3.8.2 <u>Sample based inspection</u>. As an exception to 4.3.3, sample based inspection may be used when done as part of a process control system which is fully documented and subject to review. When sample based inspection is used, the process control system shall include the following elements as a minimum:

- a. Training, commensurate with their responsibilities, shall be provided to personnel assigned to the development, implementation, and utilization of process controls and statistical methods.
- b. Quantitative evidence shall be maintained that the process is in statistical control and is a capable process.
- c. Sampling techniques shall be statistically based and consistent with data collection requirements for maintaining process control.
- d. Criteria for switching between salpling and 100% inspection shall be defined. Sampling may not be used unless the defect rate is less than 2.700 parts per million. When processes become out of control, the contractor shall revert to 100% inspection for the lot which is represented by the sample hardware.

e. When defects in table IV are identified in the inspected sample, all hardware in that lot shall be 100% inspected for other occurrence of that defect or defects. The reinspection of the lot shall be documented.

4.3.8.3 <u>Automated inspection</u>. Automated inspection processes may be used in lieu of portions of the visual inspection requirement where:

- a. the automated inspection system is part of an overall inspection and process verification system which provides report data and feedback for process control correction (where corrections are required);
- b. the automated inspection system accurately verifies that the assembly meets the requirements of this document for the conditions the automated inspection system is designed to test for:
- c. the automated inspection system is used to inspect only for the defects which the system is capable of recognizing and is not used as a general waiver of the visual inspection requirement; and
- d. the manufacturer has characterized his assembly (both design and final product) and defined inspection criteria such that the automated inspection system is implemented using manufacturer defined inspection criteria which correspond to the requirements of this document.

4.3.8.4 <u>Magnification aids</u>. When visual inspection is used, it shall be performed using the magnification power specified herein. The tolerance for magnification aids is 15 percent of the selected magnification power (i.e., \pm 15% or a range of 30 percent centered at the selected magnification power). Magnification aids and lighting used for inspection shall be commensurate with the size of the item being processed. The magnification used to inspect solder connections shall be based on the minimum width of the lands or termination areas used for the device being inspected. The following magnification shall apply:

Land Width	<u>Inspection</u>	<u>Referee</u>
> 0.5 mm (0.020 inch)	4X-7X	10X
0.25 - 0.5 mm (0.010 - 0.020 inch)	10X	20X
< 0.25 mm (0.010 inch)	20X	30X

Referee conditions shall only be used to verify product rejected at the inspection magnification. For assemblies with mixed land widths, the greater magnification may be used for the entire assembly if the smaller land width is common to more than 50% of the connections inspected (see 6.3).

NUTE: For items 0.5 mm (0.020 inch) or larger, the inspection device shall be set at the lowest power in the 4X to 7X range which is within the device's capability (i.e., if a microscope's minimum inspection power is 5X, the assembly shall be inspected at 5X). Both Government and contractor inspectors shall use the same (minimum) power. 4.3.8.5 <u>Conformal coating inspection</u>. As an exception to 4.3.8.4, conformal coating may be inspected without magnification. When the conformal coating material contains an ultraviolet (UV) tracer, inspection for conformal coating coverage shall be performed under a UV light source. Magnification from 2X to 4X may be used for referee purposes.

4.3.9 <u>Inspection of reworked defects</u>. Reworked defects, including each resoldered or reheated connection, shall be reinspected and shall conform to the acceptance criteria.

4.4 <u>Disposition of nonconformances</u>.

4.4.1 <u>Defects</u>. Assemblies containing defects shall be reworked to conformance or processed in accordance with the contract requirements for honconforming material.

4.4.2 <u>Material and process nonconformances</u>. Hardware produced using either materials or processes which do not conform to the requirements of this standard shall be classified as nonconforming material and processed in accordance with the relevant contract requirements.

4.5 <u>Materials and equipment</u>. Materials used in the soldering processes stipulated in this standard shall be as specified herein. The materials and processes specified herein may be propartible in some combinations. The manufacturer is responsible for selecting those materials and processes that will produce acceptable products.

4.5.1 <u>Solder</u>. Solder composition Sn60, Sn62, or Sn63, solder form optional, conforming to QQ-S-571 shall be used. High temperature solder conforming to QQ-S-571 may be used when specified on the approved assembly drawing. The flux of cored solder shall be type R or RMA. Other flux cores may be used according to 4.5.3 and 4.5.4. Core conditions and flux percentages are optional.

4.5.2 <u>Flux</u>. Liquid rosin based fluxes conforming to types R or RMA of MIL-F-14256 shall be used for making soldered connections. When used, the flux contained within solder (wicking) braid shall be type R or RMA. Other fluxes may be used according to 4.5.3 and 4.5.4.

4.5.3 Use of alternative flux types.

4.5.3.1 <u>Use of alternative flux types for tinning</u>. Flux conforming to types RA, WSF-0 and WSF-1 of MIL-F-14256 may be used for tinning component leads of sealed devices, epoxy bodied parts, solid bus wire, and terminals provided that:

- a. The tinning process is performed in a closed area isolated from fabrication or production areas;
- b. The contractor maintains controls to prevent distribution or use of Type RA, WSF-0, or WSF-1 flux outside the prescribed tinning area and the flux is not stored in uncontrolled storage areas; and

c. Items processed are not returned to production or fabrication processes until the residues have been removed. The Government may review flux removal procedures, processes, and processing. If at any time flux residue is detectable after these processes are completed, the use of RA, WSF-0, or WSF-1 flux shall be suspended until acceptable corrective action is implemented.

4.5.4 <u>Qualification of nonrosin flux types</u> Nonrosin flux types may be used for soldering component leads of sealed devices, epoxy bodied parts, solid bus wire, and terminals when performed as part of an integrated fluxing, soldering, cleaning and cleanliness test system (or without cleaning in the case of LR flux) and either of the following conditions are met:

- a. Usage is approved by the procuring activity.
- b. Material is used to solder printed wiring assemblies and data demonstrating compliance with the testing requirements of Appendix A is available for review.

4.5.5 Low residue (LR) flux. Formulations of fluxes which minimize or eliminate the need for post-solder cleaning operations shall be low-solids (<5% solids) and shall be halide free. Whether low-solids (<5% solids) rosin or nonrosin, the fluxes shall be tested in accordance with Appendix A. Levels 1 and 2. When performing the Appendix A tests, the cleaning steps shall be either omitted or included such that the test process corresponds to the production process. The use of LR flux in a low residue soldering process may require the approval of the procuring activity (see 4.22.3).

4.5.5.1 Low residue flux compatibility. Low residue flux shall be selected so that the flux residue is cleanable and is compatible with flux which may be used during subsequent rework, repair, or other maintenance actions.

4.5.6 <u>Solder mask</u>. Polymer solder mask coatings shall conform to IPC-SM-840, Class III.

4.5.7 <u>Heat shrinkable soldering devices</u>. Heat shrinkable soldering devices shall be self-sealing and shall encapsulate the solder connection. The devices shall meet the requirements of MIL-S-83519. Terminations made with self-sealing, heat shrinkable solder devices shall be exempt from the cleaning requirements of this standard.

4.5.8 <u>Selection of equipment</u>. Soldering irons, soldering machines and systems, and associated process equipment (including fluxers, preheaters, solder pots, cleaning systems, and cleanliness test equipment) shall not compromise functional integrity by injecting electrical energy to the item(s) being processed.

4.5.8.1 <u>Soldering irons</u>. Soldering irons shall be temperature controlled and shall be capable of maintaining the measured idling tip temperature within $\pm 5.5^{\circ}$ C ($\pm 10^{\circ}$ F). Uncontrolled (constant output) soldering irons may be used when approved by the procuring activity. Resistance between the tip of the hot soldering iron and the workstation ground shall not exceed 5.0 chms. The potential difference between the workstation ground and the tip of the hot soldering iron shall not exceed 50 millivolts RMS when measured between 50 and 500 Hertz. Three-wire cords and tip grounding shall be used. The soldering iron shall be of such design as to provide zero voltage switching. Soldering guns of the transformer type shall not be used.

NOTE: The manufacturer shall evaluate the components being soldered to determine if more stringent electrical characteristics are needed for the soldering irons. tools, and equipment (e.g., when soldering electro-explosive devices).

4.5.8.2 <u>Storage containers</u>. Containers or bags which are utilized to store printed wiring boards, solderable components, or solderable wire shall be of a material that does not introduce gases or chemicals which are detrimental to the item or its solderability. In the case of tape and reel components, the tape and reel materials shall not detrimentally affect the solderability of the surfaces to be subsequently soldered. Bags, containers and tape and reel materials used for storage of electrostatic sensitive devices shall provide device protection in accordance with MIL-STD-1686.

NOTE: Containers, bags, tape and reel materials, or combinations may be verified under accelerated aging test conditions to determine whether item solderability is detrimentally affected. Silicones, sulphur compounds, polysulphides, etc., have been found to be detrimental to component solderability.

4.6 <u>Harness and cable assemblies</u>. Harnesses and cable assemblies shall conform to a specification approved by the procuring activity. The soldering and related processes and acceptance criteria shall be as stated herein. Low residue (type LR) fluxes which meet the requirements of MIL-F-14256 and 4.22.3 may be used. Where the physical configuration of the cable assembly and related hardware prohibits cleanliness testing in accordance with this document, the contractor may use controlled processes (procedures) which provide adequate cleanliness without performing the cleanliness testing. Periodic process (procedure) validation shall be performed, the results documented, and the data available for review. Wax-impregnated lacing tape shall be utilized only for harnesses which will not be subjected to cleaning solvents subsequent to lacing operations. Tape impregnated with bee's wax shall not be used.

4.7 <u>Printed wiring</u>. Rigid printed wiring shall be designed to either MIL-STD-275 or IPC-D-275 and built in accordance with MIL-P-55110 except as modified herein. Flexible and rigid-flex printed wiring shall be designed to MIL-STD-2118 and built in accordance with MIL-P-50884 except as modified herein. When used, blind and buried vias shall be incorporated in all test coupons. Multiwire boards, designed and built in accordance with IPC-DW-425, may be used when they pass the quality conformance inspection tests (Group A and B tests) of MIL-P-55110. The minimum electrical spacing on both printed wiring and multiwire boards shall be identified on the assembly drawing.

4.7.1 <u>Coefficient of Thermal Expansion (CTE) mismatch compensation</u>. The part mounting technique or the printed wiring design shall compensate for the CTE mismatch between the part and printed wiring to the extent necessary to assure the reliability of the design. Mounting techniques shall be limited to part leads, specialized mounting devices, and normal solder connections (see 4.7.2). Leadless components shall not be soldered into place utilizing

redundant interconnect wiring between the component castellation and the land. When bottom only terminations on leadless chip carriers are used, see 5.11.5.

4.7.2 <u>Solder connection contours</u>. Designs which utilize special solder connection contours as part of the CTE mismatch compensation system are prohibited.

4.7.3 <u>Conformal coating of all assemblies</u>. Unless otherwise specified on the approved assembly drawing, all assemblies shall be conformally coated. Conformal coating requirements for printed wiring assemblies. including the type of coating (i.e., the material), shall be specified on the approved assembly drawing. When used, conformal coating shall conform to MIL-I-46058.

4.7.4 <u>Conductor spacing for uncoated assemblies</u>. If the printed wiring assembly will not be conformally coated or encapsulated, the minimum spacing between conductive patterns of printed wiring boards shall be in accordance with tables I and II. Larger spacings should be used whenever possible. The use of uncoated printed wiring boards shall be documented on the approved assembly drawing.

4.7.5 <u>Interference spacing</u>. Components and parts shall be mounted with no portion overhanging the edge of the printed wiring assembly, terminal panel, or chassis member, except for connectors, edge clips or associated circuitry.

4.7.6 <u>Solder mask over nonmelting metals</u>. Conductor areas not covered by solder mask shall be nickel plated (ceramic boards), tin/lead plated and fused, or solder coated. Bonding/adhesion promoters may be required (used). Solder mask shall not be placed over metals which will become liquid or semiliquid during processing. Minor coverage of melting metals, which shall be less than 0.1 mm (0.004 in), is permissible provided it occurs where the solder mask meets a termination area.

4.7.7 <u>Solder mask coverage</u>. Solder mask shall be continue s in all areas designated to be covered. There shall be no chipping or fracturing of solder mask, nor shall there be separation of the solder mask from laminate or metallic foil. The solder mask shall not cover materials foreign to the laminate or foil. Adherence between solder mask and laminate and between solder mask and foil shall be complete for the total area. Temporary solder masking materials, if used, shall be removed.

4.7.8 <u>Plated-through holes without leads or wires inserted</u>. The holes may be left unfilled. When filled, the solder plug shall meet the requirements of 5.11.2 (see figure 2).

4.7.9 <u>Tenting of plated-through holes</u>. Permanent solder mask shall not tent empty plated-through holes (i.e., via holes) which are greater than 0.5 mm (0.020 inch) in diameter. When tenting plated-through holes, solder mask shall not be placed over melting metals beyond the limits of 4.7.6.

4.7.10 <u>Identification of via hole fill requirements</u>. All via holes (no lead or wire inserted in the plated-through hole) designated to be filled on the drawing shall be filled. Holes required to be left unfilled shall not be filled. If the drawing does not state whether the hole shall be filled or unfilled, then the design shall be considered insensitive to hole fill and hole fill requirements may be stated in the production process documentation

TABLE I.Conductor spacing (uncoated printed wiring boards)(sea_level to 10,000_feet).

Voltage between conductors <u>GC or AC peak (volts)</u>

0-150 151-300 301-500 Greater than 500

Minimum spacing

0.64 mm (0.025 inch) 1.3 mm (0.050 inch) 2.5 mm (0.10 inch) 0.005 mm (0.0002 inch) per volt

TABLE II.Conductor spacing (uncoated printed wiring boards)
(over 10,000 feet).

Voltage between conductors <u>DC or AC peak (volts)</u>

0-50 51-100 101-170 171-250 251-500 Greater than 500 Minimum spacing

0.64 mm (0.025 inch) 1.5 mm (0.060 inch) 3.2 mm (0.125 inch) 6.4 mm (0.250 inch) 12.7 mm (0.500 inch) 0.03 mm (0.001 inch) per volt

4.7.11 <u>Interfacial and interlayer connections</u>. Interfacial connections of circuitry on double sided printed wiring boards or assemblies shall be either plated-through holes or the clinched wire configuration of Appendix B (see 40.10.1.3). Interfacial and interlayer connections of circuitry of multilayer printed wiring boards or assemblies shall be of the plated-through hole configuration. Electrically nonfunctional, plated-through holes shall be identified as such on the assembly drawing and do not need to meet the electrical connection requirements.

4.7.12 Parts mounted in plated-through holes used for interconnection. Standoff terminals, eyelets, rivets, snug fit pins, or braided sleeves shall not be used to provide interfacial or innerlayer connection. Plated-through holes used for functional interfacial connections shall not be used for the mounting of devices which put the plated-through hole in compression. Terminals, eyelets, rivets, or snug fit pins shall not be installed in any plated-through hole utilized for interfacial or innerlayer connection.

4.7.13 Eyelets. Eyelets are unacceptable for electrical connections.

4.7.14 <u>Component selection and mounting</u>. Components shall be designed for and capable of withstanding the processing conditions to which they are exposed. The component mounting processes (steps) and the subsequent processes (e.g., soldering, cleaning, etc.) shall be designed and scheduled such that components are capable of withstanding temperatures incident to the processes to which they are subjected. When a design requires the mounting and soldering of components which are incapable of withstanding subsequent soldering and cleaning processes, these components shall be mounted and soldered to the assembly in an separate operation which minimizes stress to the part.

4.7.14.1 <u>Component selection</u>. Components shall be selected and mounted so that the final assembly will be capable of meeting the vibration, mechanical shock, humidity, and other environmental conditions for which the assembly is designed. Components shall be mounted such that the operating temperature of the component does not reduce component life below design limits. The component mounting technique shall ensure that the maximum allowable temperature of the board material is not exceeded under operating conditions.

4.7.14.2 <u>Component mounting</u>. Parts shall be mounted in accordance with Appendix B or the approved assembly drawing. If the contractor develops alternative part mounting requirements, they may be used in lieu of Appendix B provided they are approved by the procuring activity prior to use. When used, contractor-developed part mounting requirements shall be documented, available for review, and made part of the process documentation developed in accordance with 4.3.2.

NOTE: Changes in part mounting configuration must be evaluated to assure that pre-production or first article environmental tests remain valid.

4.7.14.3 <u>Component interconnection</u>. Leads and wires shall be mounted to through-holes, terminals, or lands (including offset lands). All terminations shall be soldered.

4.7.14.4 <u>Attachment points for interconnect wires</u>. Interconnect wiring connected directly to assemblies shall be installed in plated-through holes or on terminals. Bare tinned wire with added insulating sleeving shall not be used. Wires shall be installed on terminals if the wires are subject to removal for normal maintenance action.

4.7.14.5 <u>Sockets</u>. Components shall not be mounted in sockets. Additionally, components shall not be mounted in plug-in devices which rely upon contact pressure for part retention or electrical connection.

4.7.14.6 <u>Compliant pins (connectors)</u>. As an exception to 4.7.11 and 4.7.12, compliant pins in accordance with MIL-STD-2166 and connectors in accordance with MIL-C-28859 may be inserted in the plated-through holes of backplanes and mother boards designed to MIL-STD-2119 and fabricated to MIL-A-28870 and the requirements contained herein.

4.7.14.7 <u>Terminal selection</u>. Terminals shall be of the flat shoulder configuration (see figures 3 and B-13).

4.7.14.8 <u>Lead bends</u>. Lead bends shall not extend to the part body or weld. The minimum radius of lead bends shall be one lead thickness, one lead diameter, or one lead diameter prior to coining (see figure 4).

4.7.14.9 <u>Stacking (piggybacking)</u>. Unless a component or part is specifically designed to accept another part into its configuration, there shall be no stacking (piggybacking) of parts or components.

4.7.15 <u>Adhesive coverage limits</u>. If a component is secured to the printed wiring board utilizing an adhesive bonding resin, the area of resin coverage shall not flow onto or obscure any of the terminal areas. Part attachment processes shall control the quantity and type of bonding material such that the parts are removable without damage to the assembly. The adhesive used shall be compatible with both the printed wiring and the part.

4.8 <u>Electrostatic discharge</u>. Electrostatic discharge (ESD) control for the protection of electrical and electronic parts, components, assemblies and equipment shall be in accordance with MIL-STD-1686. ESD controls shall be maintained during receipt and test of parts, through the manufacture and inspection cycles, storage, and shipping. Guidance on ESD control is contained in MIL-HDBK-263.

NOTE: The manufacturer shall evaluate the components being soldered to determine if more stringent electrical characteristics are needed for the soldering irons, tools, and equipment (e.g., when soldering electro-explosive devices).

4.9 <u>Certification of personnel</u>.

4.9.1 <u>Certification</u>. Personnel performing tasks in accordance with this standard shall be trained and certified to the appropriate job functions and procedures of this standard. The training and testing program for certification shall be based on the requirements of this standard and shall reflect the actual work being performed. The contractor shall designate an individual responsible for employee certification.

4.9.2 <u>Certification record</u>. Each employee's certification shall be documented and the record shall include the date and location of training, the jobs or skills the error yee is certified to perform, the date of the most recent training or recertification, method and results of the contractor's evaluation of student's performance or graded test, and the signature of the contractor designated person responsible for training and certification (see 4.9.1).

4.9.3 <u>Training program</u>. The contractor's training program is subject to review by the government.

4.9.4 <u>Maintenance of certification</u>. The contractor shall perform periodic audits of the employee's performance to verify conformance with this standard. Certification shall be revoked when work produced by the employee does not meet the requirements of this standard.

4.10 <u>Tempered lead cutting</u>. Tempered leads (sometimes referred to as pins) shall not be cut with diagonal cutters or other tools which impart shock to connections internal to the component.

4.11 <u>Insulation stripping</u>. Chemical stripping agents shall be neutralized or removed prior to soldering.

4.12 Lead forming. Lead forming shall not damage the part-to-lead interface, the lead seal, lead material or part body beyond the damage limits allowed in the part specification (see figure 5). Leads shall be supported during forming to protect the lead-to-body seal. Leads shall be formed with dies or other appropriate tools such that they may be soldered into place by subsequent processes without application of external loads. When the leads of DIPs, flatpacks, and other multileaded devices become misaligned during processing or handling, they shall be straightened to ensure parallelism and alignment prior to mounting. Leads and wires shall be mechanically secured to their terminals before soldering. Such mechanical securing shall prevent motion between the parts of a connection during the soldering operation.

4.13 Hold down of surface mounted device leads. Except for lead compression during resistance reflow soldering, surface mounted device leads shall not be held down under stress (e.g., probes) during solder solidification. The resistance reflow systems should not deflect leads more than two times the lead thickness during reflow. Residual tensile stresses greater than 13.8 kPa (200 psi) shall not remain in the solder connection after cooling. Tool marks resulting from heating bar operation shall not be cause for rejection.

4.14 <u>Tinning of stranded wire</u>. Portions of stranded wire which will be soldered shall be tinned prior to mounting.

4.15 <u>Solderability</u>. The contractor's material control system shall establish a solderability testing schedule which ensures parts are solderable at the start of soldering operations. The contractor shall establish material control and storage procedures which ensure minimal part solderability degradation.

4.15.1 <u>Solderability testing of components and printed wiring boards</u>. Unless otherwise specified in the part specification, the solderability of parts shall meet the requirements of MIL-STD-750 Method 2026 for semiconductors, MIL-STD-883 Method 2003 for microelectronics. MIL-P-55110 for rigid printed wiring boards, MIL-P-50884 for flexible and rigid-flex printed wiring boards, and MIL-STD-202 Method 208 with only one hour of steam aging (insulation removed) for wire. Where the part specification does not require solderability testing, then solderability shall be tested to MIL-STD-202 Method 208.When tin and lead are plated as separate operations, the finish shall be fused (reflowed or hot solder dipped). Component leads which are simultaneously plated with tin-lead need not be subsequently fused provided the parts pass MIL-STD-202, Method 208, after eight (8) hours of steam aging. As an exception, magnet wire need not be solderability tested.

NOTE: ANSI/J-STD-003 may be used for solderability testing of printed wiring or multiwire boards.

NOTE: The use of Class I ozone depleting substances is not required when MIL-STD-202. Method 208 testing is performed. The testor may elect to use a non-ozone depleting substance which is permitted by the test method.

4.15.2 <u>Solderability testing of ceramic boards</u>. Metallic elements of ceramic printed wiring boards shall be tested as specified in IPC-HM-860 or an equivalent method. Testing may be performed on coupons in lieu of actual boards provided that the coupons were prepared at the same time, from the same lot of materials, and stored under the same conditions as the boards in question.

4.16 Solder pot and solder bath temperatures. The solder pots used for cleaning and tinning of areas to be soldered, drag soldering pots, and wave solder baths shall be temperature controlled. Solder pots or baths shall be set at a preselected temperature within the range of 245° to 275°C (475° to 525°F). The temperature shall be maintained within ± 5.5 °C (± 10 °F) of the preselected temperature.

4.17 <u>Single poirt soldering of surface mounted devices</u>. Single point soldering shall not be used on multicastellated components during initial soldering operations. Single point rework operations are permissible provided that adjacent solder connections are not simultaneously reflowed.

4.18 <u>Cooling</u>. Solder connections shall not be subjected to movement or stress at any time during the solidification of the solder. There shall be a smooth transition after completion of the soldering operation to prevent formation of disturbed solder connections. When machine soldered, the printed wiring assembly shall be retained on the conveyor until the solder has solidified. Prior to solidification of the solder, no liquid shall be used to cool a soldered connection. Heat sinks may be used to expedite cooling. Accelerated cooling may be used provided the cooling process is controlled and no thermal shock damage results.

4.19 <u>Lead cutting after soldering</u>. The cutting of component leads or wires after soldering shall be followed by the reflow of the solder connection.

4.20 <u>Cleanliness</u>. Work areas and tools shall be maintained in a clean and orderly condition. There shall be no visible foreign material including dirt, chips, grease, silicones, flux residue, solder splatter, solder balls, insulation residue and wire clippings at the workstation. Eating, smoking, or drinking at a workstation shall be prohibited. Containers of hand creams, ointments, perfumes, cosmetics, and other materials unessential to the fabrication operation, except hand creams approved and controlled for use in electronics areas, are prohibited at the workstation.

4.21 <u>Maintenance of solder purity</u>. Solder purity shall be maintained. Before soldering a printed wiring board, all dross appearing on the solder contact surface shall be removed. Dross blankets may be used provided the blankets do not contaminate the solder. If the amount of any individual contaminant or the total of contaminants listed exceeds the percentages specified in table III, the solder shall be replaced or altered to be brought within specifications. TABLE III. Contamination limits.

		Maximum Contaminat'on ^C ercent by Heigh	linat'on Limits by Height	9 1	Interval Between Testing B Hr Operating Day	reen Pay	Caldar Data (Parasteric Guidalines (17 Salder 15
Freconditioning Assy Soldering 2/ (lead/Hire Tinning) Assy Soldering 2/ (Pot. Wave. Etc.) A B C im 75 30 15 60 60 60 im 01 005 15 30 60 60 im 01 005 15 30 60 60 im 01 005 15 30 60 70 im 008 005 15 30 60 120 im 008 005 15 60 120 60 int 02 02 15 60 120 120 int 25 25 15 60 120 120 int 25 10 15 60 120 120	Contaminant <u>1</u> /				я Я		Contaminated) 4/
r 75 30 15 60 60 um 50 20 15 60 60 um 01 005 15 30 60 um 01 005 15 30 60 um 01 005 15 30 60 um 008 006 15 30 60 num 008 006 15 30 60 num 008 006 15 30 60 num 008 006 15 60 120 num 02 03 15 60 120 num 25 03 15 60 120 num 25 10 15 60 120		Preconditioning (Lead/Wire Tinning)	Assy Soldering 2/ (Pot. Wave. Etc.)	A	ß	J	-
Im 50 20 15 60 60 Im 01 005 15 30 60 Imm 01 005 15 30 60 Imm 008 006 15 30 60 Imm 008 006 15 30 60 Imm 008 006 15 30 60 Imm 003 005 15 60 120 Imm 25 25 15 60 120 Imm 25 10 15 60 120 Imm 25 10 15 60 120	Copper	75	.30	15	60	60	Sluggish solder flow. solder hard and brittle
m 01 005 15 30 60 m 008 005 15 30 60 m 008 006 15 30 60 m 008 006 15 30 60 m 008 006 15 30 60 m 02 .02 15 60 120 m 25 15 60 120 120 m .25 .10 15 60 120	Gold	50	.20	15	60	60	Solder grainy and brittle
008 005 153060Solder rough and grainy. frosty and porousnum 008 006 153060Solder sluggish. frosty and porousnum 008 006 153060Solder sluggish. frosty and porousnum 02 008 006 153060Solder sluggish. frosty and porousnum 02 008 006 15 00 Solder sluggish. frosty and porousnum 02 003 02 15 60 120 Front in compound FeSn2 is not solderable.num 02 03 15 60 120 Small blister-like spotsnum 25 25 15 60 120 Small blister-like spotsnum 25 10 15 60 120 00 25 10 15 60 120 001 $apearance - retards nature010501156012001apearance - retards nature$	Cadmium	01	.005	15	99	60	Porous and brittle solder joint. sluggish solder flow
008 006 15 30 60 02 02 02 02 120 03 03 03 15 60 120 03 03 03 15 60 120 1 25 25 15 60 120 1 75 10 15 60 120 025 01 15 60 120	21nc	.008	.005	15	e R	60	Solder rough and grainy. frosty and porous. High dendritic structure
02 02 15 60 120 03 03 03 15 60 120 03 03 03 15 60 120 7 75 .25 15 60 120 7 .75 .10 15 60 120 .025 .10 15 60 120	Aliminim	008	.006	15	8	60	Solder sluggish. frosty and porous
03 03 03 15 60 120 25 25 25 15 60 120 5/ 75 10 15 60 120 0 75 10 15 60 120 0 01 15 60 120	Iron	02	.02	15	60	120	iron tin compound FeSn2 is not solderable. Compound on surface presents resoldering problems.
25 25 15 60 120 \$1 75 .10 15 60 120 \$0 75 .10 15 60 120 \$25 01 15 60 120	Arsecto	.03	8	15	99	120	Small blister-like spots
5/ 75 .10 15 60 120 .025 .01 15 60 120	Rismuth	25	.25	15	93	120	Reduction in working temperature
. 025 01 15 60 120	Silver 5/	57.	.10	15	60	120	Oull appearance - retards natural solvent action
	Nicke)	.025	01	15	60	120	Blisters, formation of hard insoluble compounds

The tin content of the solder bath shall be within 1% of the limits of QQ-S-571 for the solder specified copper/gold contamination. The balance of the bath shall be lead and/or the items listed above.

The total of copper, gold, cadmium, zinc and aluminum contaminents shall not exceed .4% for assembly soldering.

An operating day constitutes any 8-hour period, or any portion thereof. during which the solder is liquified and used.

See 4.21.1 of this document. ちょ あ で ち

Kot applicable for Sn62 solder - limits to be 1.75 to 2.25 (both operations).

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NAWCADLKE-MISC-05-MT-0002

4.21.1 <u>Inspection for solder purity</u>. Solder in solder baths shall be chemically or spectrographically analyzed or renewed at the testing frequency levels shown in table III. column B. These intervals may be lengthened to the eight-hour operating days shown in column C. when the results of analyses confirm that such action will not adversely affect the purity of the solder bath. If contamination exceeds the limits of table III, intervals between analyses shall be shortened to those eight-hour operating days shown in column A or less until continued purity has been assured by analyses. Records containing the results of all analyses and solder bath usage shall be available for Government review.

4.21.2 <u>Machine soldering processes</u>. As part of the machine soldering process and its documentation (for all systems, including wave, vapor phase reflow, infrared reflow, etc.), manufacturers shall define a preheat schedule, dependent on the process selected, the flux, and the board and assembly design such that the assembly is properly preheated prior to soldering. The soldering process and its documentation shall provide consistent thermal profiles for each assembly type processed. The preheat and thermal profile requirements shall ensure proper flux activation, proper solder wetting, and shall ensure that thermal shock and excessive thermal stresses are avoided.

4.22 <u>Cleaning</u>. The contractor shall develop a documented cleaning process or processes. The maximum time between other processes (part mounting, soldering, rework, etc.) and cleaning shall be selected to assure that parts, subassemblies, and assemblies can be completely cleaned. The cleaning process shall have no deleterious effect on the parts, connections, and materials being cleaned. Items shall be cleaned in a manner that will prevent both thermal shock and moisture intrusion into components which are not totally sealed.

- NOTE: Class I ozone depleting substances (e.g., chlorofluorocarbon (CFC) based solvents) have been proven to be hazardous to the environment. Their continued use is not recommended and should be phased out. Use of solvent reclamation systems is encouraged.
- 4.22.1 <u>Ultrasonic cleaning</u>. Ultrasonic cleaning is permissible:
 - a. on bare boards or assemblies, provided only terminals or connectors without internal electronics are present, or
 - b. on electronic assemblies with electrical components, provided the contractor has documentation available for review showing that the use of ultrasonics does not damage the mechanical or electrical performance of the product or components being cleaned.

4.22.2 <u>Modification of cleaning processes</u>. When cleaning processes are changed during production, the contractor shall verify that the new cleaning system and the hardware processed meet the requirements of 4.5, 4.22, and 4.22.1. In addition, for rosin fluxes, the contractor shall verify the requirements of Appendix C are met. For nonrosin fluxes, the manufacturer shall verify the requirements of Appendix A are met.

4.22.3 Low residue soldering processes. As an exception to 4.22, postsoldering cleaning operations may be reduced or eliminated when a documented low residue soldering process is used. This documented process shall be approved by the procuring activity prior to use on missile, space, safety-offlight, man-critical, and mission critical systems. When a low residue soldering processes is used:

- a. materials, components, subassemblies, and assemblies shall be received, handled, stored, and otherwise processed in a manner which does not contribute to the contamination of the assembly;
- b. the final assembly shall be cleanliness tested in accordance with 4.23 and Appendix C; and
- c. the contractor shall have data available for review which shows that any residues left on the assembly do not adversely affect long term reliability, testability, or conformal coating adhesion. This shall be quantified data, from an appropriate test methodology, which may be derived from environmental stress screening tests, material compatability tests, accelerated life cycle testing, qualification tests, or equivalent tests.
- NOTE: If post-soldering cleaning steps are omitted, then prior to processing, all materials, components, subassemblies, and assemblies should be cleanliness tested and cleaned as necessary.

4.22.4 <u>Part markings and reference designations</u>. Parts markings and reference designations. when used, should remain legible after processing.

4.23 <u>Cleanliness testing</u>. For assemblies which are cleaned after soldering, periodic testing of ionic cleanliness of printed wiring boards and printed wiring assemblies after final cleaning (i.e., the cleaning prior to conformal coating, encapsulation, or incorporation into the next higher assembly) shall be conducted to ensure the adequacy of the cleaning When assemblies are not cleaned after soldering (e.g., low process(es). residue soldering), assemblies shall be periodically tested to verify cleanliness. As a minimum, a representative sample of each printed wiring board and printed wiring assembly (i.e., part number, etc) or the most complex assemblies processed through final cleaning shall be tested on a daily basis. If any assembly fails, the entire lot shall be recleaned and retested. The resistivity of solvent extract test, or the sodium chloride (NaCl) salt equivalent ionic contamination test, or an equivalent test, which is fully documented and available for review by the government. shall be used to test for ionic cleanliness. The resistivity of solvent extract test shall have a final value greater than 2 megohm-centimeters. The sodium chloride salt equivalent ionic contamination test shall have a final value less than 1.55 micrograms per square centimeter $(2.2 \times 10^{-8} \text{ lb}_{m}/\text{in}^2)$ of board surface area. There shall be no visible evidence of flux residue or other contamination. The resistivity of solvent extract test and the sodium chloride salt equivalent ionic contamination tests are defined in Appendix C. Alternative equipment, with the appropriate equivalence values, may be used to verify cleanliness.

NOTE: 2.2 x 10^{-8} lb_m/in² is equivalent to 10 micrograms/in².

4.23.1 <u>Qualification of cleaning and cleanliness testing processes for</u> <u>surface mounted assemblies</u>. Prior to use on production hardware which includes surface mounted components, the manufacturer shall test representative control assemblies and define acceptable ionic cleanliness testing equipment, processes and control parameters. The combined action of the equipment, process and controls shall consistently verify that the sodium chloride or equivalent ionic contamination test value for the production hardware is less than 1.55 micrograms per square centimeter (2.2 x 10⁻⁸ lb_m/in^2) of board surface area. The representative control assemblies used for establishing the test method shall be processed using the same materials, parts and designs that will be used in the production hardware.

NOTE: As a general rule, the combination of the ionic cleanliness testing equipment, processes and control parameters used for through-hole mounted devices and assemblies is not adequate for verification of the ionic cleanliness of surface mount assemblies.

5. DETAIL REQUIREMENTS

NOTE: Unless otherwise specified in the contract or detail specification, the requirements of this section are mandatory for all applications (contracts).

5.1 <u>Part damage</u>. Part bodies, lead seals, and lead material shall not be cracked, scored, chipped, broken, or otherwise damaged beyond the limits of the original part specification.

5.1.1 Charred (i.e., burned or blackened) components, wire insulation, or other insulating material are not acceptable.

5.1.2 Lead bends shall not extend into the lead seal. See figure 5.

5.1.3 The shank of terminals shall not be perforated, split, cracked, or otherwise discontinuous to the extent that oils, flux, inks, or other liquid substances utilized for processing the assembly are, or can be, entrapped within the mounting hole. Circumferential cracks or splits in the shank are not acceptable regardless of extent. There shall be no more than three radial splits or cracks. Regardless of the number, splits or cracks separated by less than 90 degrees or which extend beyond the rolled area of the terminal are unacceptable. Terminals and connector pins shall be approximately perpendicular to the surface upon which they are mounted. Terminals and connector pins shall not be bent or otherwise deformed.

5.2 <u>Printed wiring board damage</u>. Printed conductors, including lands, shall not be reduced in width or thickness by more than 20 percent. There shall be no tears or cracks in the conductors, including the lands.

5.2.1 Wrinkles in the conductor pattern shall not exceed the limits of MIL-P-55110 or MIL-P-50884, as applicable.
5.2.2 After soldering, the maximum allowed lifted land distance from the board surface to the outer, lower edge of the land shall be the thickness (height) of the terminal area or land. Normal undercut shall not be considered a lifted land.

5.2.3 The weave of glass laminates shall not be exposed on either surface beyond the limits of MIL-P-55110 or MIL-P-50884.

5.2.4 In addition to the requirements of 4.7.6, 4.7.7. and 4.7.9, solder masks shall meet the requirements of MIL-P-55110 or MIL-P-50884, as applicable, and IPC-SM-840, Class 3 and shall not contain cracks, wrinkles, peeling, or otherwise trap contaminants.

5.2.5 Printed wiring shall not be blistered or delaminated beyond the limits of MIL-P-55110 and MIL-P-50884.

5.2.6 When present, measled areas shall fit within a 6 mm by 6 mm (1/4 inch by 1/4 inch) square. The total measled area(s) on both sides of a board shall not exceed ten percent (10%) of the surface area of one side of the board. The printed wiring assembly shall include no measled area between two conductors at different potentials. on the same inner layer plane, which reduces the unmeasled distance between conductors to less than 50% of the minimum design electrical spacing. The barrels of adjacent plated-through holes shall be considered conductors on the same innerlayer plane. Measling which is visible between only surface level conductors shall not be cause for rejection (i.e., to be rejectable, the measling must be verified as occurring between sub-surface conductors on the same plane).

5.2.7 Charred (i.e., burned or blackened) printed wiring laminate, conductors, or other insulating material is not acceptable.

5.2.8 Warp or twist of the printed wiring board shall not exceed the limits of MIL-P-55110.

5.2.9 Pits, scratches, or inclusions in the base material shall not exceed the limits of MIL-P-55110 or MIL-P-50884, as applicable.

5.3 <u>Stress relief</u>. Parts shall not be mounted without stress relief.

NOTE: Solder in the stress relief bends does not constitute elimination of stress relief.

5.3.1 For leaded, through-hole or terminal mounted parts, stress relief shall be in the form of a lead or wire bend, visible without magnification, between the solder connection or terminal and the part body. As an alternative, the stress relief may be in the form of a slight, gradual bend in a lead, both leads, or a wire. See figure 6.

5.3.2 All parts weighing 7.1 grams (0.25 ounce) or more per lead shall be supported by clamps. spacers, or other means which ensure that the solder connections and leads are not relied upon for mechanical support.

5.3.3 Wicking under the insulation of wires shall not eliminate stress relief in an area which is required to be flexible.

5.4 <u>Wire and wire strand damage</u>. Wires or wire strands shall not be broken or severed. Nicks, cuts, scrapes, stretching, or other observable damage which exceeds 10 percent of the total cross-sectional area of the solid wire or stranded wire is not acceptable. Birdcaging (i.e., separation between wire strands) shall not exceed one strand diameter.

5.5 <u>Violation of the minimum electrical spacing</u>. Misregistration of components shall not reduce the spacing between conductors and adjacent printed wiring or other metallized elements to less than the minimum electrical spacing.

5.5.1 Leads, wires, or conductive part bodies shall not be mounted such that potential movement of the part, lead, or wire will cause conductors to violate the minimum electrical spacing. Excessive lead length, including excessive clinch length, which may violate the minimum electrical spacing (or cause shorting) is not acceptable.

5.5.2 Uninsulated metal cased components, uninsulated wires, and uninsulated component leads shall not be routed over exposed circuit paths (printed wiring conductors) such that shorting is possible.

5.5.3 Bridging and excess solder, including points, peaks, and icicles, which violates the minimum electrical spacing requirement or which contacts any nonmetallized portion of the component body is not acceptable (see figure 16). Sharp edges and solder peaks are permissible provided they do not present a potential abrasion point for adjacent parts or wires and the solder peaks do not reduce the electrical spacing below the applicable minimum. Solder peaks are not permissible in high power applications where there is the potential of corona discharge.

5.6 <u>Wire insulation</u>. Insulation on leads or wires shall not be embedded in the solder connection. The clearance between the solder of the connection and the separable or fixed insulation on a lead or wire shall not be such that it permits shorting. Insulation clearance for high voltage wires (wires carrying more than 6.000 volts) shall be not exceed 2 mm (1/16 inch). Insulation deformation or damage shall not exceed 20% of the insulation thickness.

5.7 <u>Contamination or foreign material</u>. There shall be no visible contamination or foreign material, including flux residue, greases, silicones, dirt, solder splatter, solder balls, solder slivers, insulation residue, wire clippings and lead clippings. Failure of a test assembly to pass cleanliness testing shall cause rejection of the entire lot represented by the sample. Small quantities of flux residues are permitted when they result from a low residue solder process. These residues shall not interfere with conformal coating adhesion nor contribute to operational contamination problems.

5.8 <u>Fractured, cracked, or disturbed solder connections</u>. There shall be no split, crack, fracture, or separation within the solder or between the solder and the connection elements (e.g., leads, wires, and board). There shall be no disturbed solder connections.

5.9 <u>Dewetting, non-wetting, and coid solder connections</u>. There shall be no solder dewetting or non-wetting in excess of 10 percent of the lead periphery. Cold solder, which may appear as a grayish connection combined with non-wetting, is not acceptable. The solder shall have a contact angle to the surfaces being joined which is not greater than 90 degrees.

5.10 <u>Voids, pits, and blowholes</u>. Voids, pits, and blowholes which occur in conjunction with the minimum permissible solder volume are not acceptable.

5.11 <u>Insufficient solder</u>. Solder shall wet the surfaces of all connection elements and form a fillet between elements. Solder fillets are not required to extend to the edge of the termination area. The absence of solder on connection elements which are supposed to be soldered is not acceptable.

5.11.1 <u>Insufficient solder: terminals</u>. Except for solder cup terminals, there shall be a solder fillet between the lead or wire and the terminal for the full length of the wrap. At least 75% of a solder cup shall be filled with solder. See figure 7.

5.11.2 <u>Insufficient solder</u>; <u>plated-through holes</u>. Plated-through holes, regardless of whether a lead or wire is inserted therein, shall have no more than 25% recession and evidence of good wetting. See figure 2.

5.11.3 <u>Insufficient solder; leaded surface mounted components</u>. The solder connection on leaded surface mounted parts shall include a fillet which extends across at least 75% of the lead width. The heel fillet shall extend above the midpoint of the lower bend of the lead. As a minimum, the solder shall extend along the lead for the length of the contact area or footprint. For J-leaded parts, the solder shall rise at least 1.5 times the diameter or thickness up the lead. For V-leaded parts, the solder shall rise at least 2 times the diameter or thickness of the lead thickness or to the midpoint of the bend radius, whichever is higher. Toe overhand is acceptable provided minimum design spacing is maintained and there is minimum lead coverage (lap) over the land. See figures 8, 9, 10, and 11.

5.11.4 <u>Insufficient solder</u>; <u>leadless chip carriers</u>. The solder connection on leadless chip carriers shall include a fillet which extends across at least 75% of the width of the castellation. It shall rise vertically at least 25% of the castellation height. The height from the substrate to the bottom of the leadless chip carrier shall be a minimum of 0.2 mm (0.008 inches). See figure 12.

5.11.5 <u>Insufficient solder; bottom-only leadless surface mounted</u> <u>components</u>. The solder connection on leadless surface mounted components which have only bottom terminations shall extend at least 75% across the width of the bottom metallization. They shall be at least 0.2 mm (0.008 inch) in height unless the printed wiring board compensates for thermal expansion stresses (i.e., CTE compensation is provided).

5.11.6 <u>Insufficient solder: chip devices</u>. As a minimum, 75% of the end metallization width (the end face. not including the side of end caps) shall be positioned over the land and shall have a solder fillet. At least 75% of the end metallization shall be over the termination area. A side fillet is not required. The solder fillet shall extend at least 25% or 1.0 mm (0.040 inch) up the end of the device, whichever is less. Solder may be present on the top of the end cap. The wetting angle of the solder to the part and to the land shall be less than 90 degrees except when the quantity of solder results in a rounded contour which extends over the edge of the land. See figures 13, 14, 15, 17, and 18).

5.12 <u>Gold removal</u>. Gold shall be removed from the to-be-soldered surfaces of parts plated with 0.00250 mm (100 microinches) or more of gold. For surface mounted parts, the gold shall be removed from all of the to-be-soldered areas of the part, regardless of the plating thickness.

5.13 <u>Wire and lead wrap on terminals</u>. Leads and wires shall be wrapped around terminals for a minimum of one-half turn and shall not overlap (see figure 19). On terminals with square or rectangular posts, the wire or lead shall be in contact with the flat surfaces of two non-adjacent sides. For AWG size 30 or smaller wire, the maximum number of turns should not exceed three. Continuous runs and small parts to which such mechanical securing would be impracticable (e.g., connector solder cups, slotted terminal posts and heat shrinkable solder devices) are exempt from this requirement.

NOTE: For continuous runs, wires need not be wrapped 180 degrees except on the end terminals.

5.14 <u>Conformal coating</u>. Conformal coating shall be cured. It shall not contain voids which expose conductors. It shall not contain foreign material. There shall be no mealing, peeling, or separation. There shall be no voids, bubbles, or clusters of bubbles which bridge conductors. When an epoxy coating is used, glass cased components shall be protected with buffer material.

5.15 <u>Drawing compliance</u>. The final assembly shall meet all drawing requirements. The absence of a part or the use of an incorrect part is not acceptable. Polarized parts shall be oriented in accordance with the drawing requirements.

5.16 <u>Connections made with heat shrinkable solder devices</u>. The solder shall reflow such that the shape of the connection elements can be discerned. The solder shall lose all appearance of ring shape and the contour of the solder preform shall not be visible. Inserts shall melt and flow along the wires. The outer sleeve may be darkened, but the connection area shall be visible.

Defect No.	Defect. Title	Reference Paragraph
1	Part damage	5.1 - 5.1.3
2	Printed wiring board damage	5.2 - 5.2.9
3	Stress relief	5.3 - 5.3.3
4	Wire and wire strand damage	5.4
5	Violation of the minimum electrical spacing	5.5 - 5.5.3
6	Wire insulation	5.6
7	Contamination or foreign material	5.7
8	Fractured, cracked, or disturbed solder connections	5.8
9	Dewetting, non-wetting, and cold solder connections	5.9
10	Voids, pits, and blowholes	5.10
11	Insufficient solder	5.11 - 5.11.6
12	Gold removal	5.12
13	Terminal mounting	5.13
14	Conformal coating	5.14
15	Drawing compliance	5.15
16	Connections made with heat shrinkable solder devices	5.16

TABLE IV. Defects.

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6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 <u>Manufacture of devices incorporating magnetic windings</u>. NAWCADLKE-MISC-05-MT-0002 is very limited in its applicability to the manufacturing processes associated with the mounting of internal electronic elements and the soldering of the internal connections of transformers, motors, and similar devices. Unless a user has a specific need for the controls provided by NAWCADLKE-MISC-05-MT-0002, it should not be imposed relative to the manufacture of the internal elements of these devices. However, the external interconnect points (i.e., terminals, pins, etc) shall meet the solderability requirements of this document and the device shall be adequately sealed to ensure it does not contaminate the final assembly (i.e., when active fluxes are used internally).

6.2 <u>Guidance on requirement flowdown</u>. Prime contractors are responsible for delivering fully compliant hardware to the government. The flowdown of NAWCADLKE-MISC-05-MT-0002 requirements is generally stopped when the contractor reaches the commercial off-the-shelf or standard military part level. Where a part is adequately defined by a basic part specification (e.g., MIL-T-27 for transformers), then the requirements of NAWCADLKE-MISC-05-MT-0002 shall be imposed on the manufacture of that part only when necessary to meet the end item requirements. When it is unclear where flowdown should stop, it is the responsibility of contractors to work with their cognizant government activities to determine which parts shall be considered commercial off-the-shelf or standard military parts.

6.3 <u>Guidance on inspection power selection and defect identification</u>. Acceptance and rejection shall be done at the inspection power specified herein. If the presence of a defect cannot be determined at the inspection power, the item shall be accepted. The inspector need not be able to accurately determine which defect is present at the inspection power. He need only recognize the presence of a defect. The referee power may be used only when there is a disagreement over whether a characteristic is acceptable. Higher powers may be used as part of the process control system for root cause analysis.

6.4 <u>Supersession note</u>. This standard is intended to replace all prior documents for electrical and electronic soldering. Where possible, this document should be used in lieu of prior documents on reprocurements. This will enable manufacturers to achieve a simpler manufacturing environment, eliminate the requirement for multiple production set-ups, and reduce errors induced by imposition of multiple sets of contracting requirements.

6.5 Subject term (key word) listing.

Connector Electronic components assembly Flux, soldering Printed circuit board Printed wiring, flexible Printed wiring board Solder Soldering iron

6.6 <u>Use of metric units</u>. While inch. pound, and Fahrenheit units continue to be used by United States industries for manufacturing electronic assemblies. a move toward metric units has been led by the introduction of surface mount components. In this document, measurements are provided in metric units followed by either the inch-pound equivalent or <u>an approximation of the inch-pound equivalent</u>. Some conversions were approximate to facilitate the continued processing of older design assemblies where direct conversion would yield unreasonable values. It is recommended that manufacturers transition to the metric system. In the event of conflict or referee measurement, the metric measurement shall take precedence.



ACCEPTABLE



NOT ACCEPTABLE







TOTAL DEPRESSION = 0 + 0≤25% OF d





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ACCEPTABLE (MINIMUM) D

FIGURE 2. <u>Plated-through hole interfacial and interlayer connections</u> (see 4.7.8 and 5.11.2).



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FIGURE 5. Device lead forming (see 4.12 and 5.1.2).

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DEVICES WITH BODIES EITHER SECURED OR UNSECURED TO THE MOUNTING SURFACE



ALTERNATE METHOD FOR DEVICES WITH BODIES UNSECURED TO THE MOUNTING SURFACE

FIGURE 6. Typical stress relief bends (see 5.3.1).



- I. SOLDER ALMOST FILLS CUP AND FOLLOWS THE CONTOUR OF THE CUP ENTRY.
- 2. WETTING BETWEEN LEAD OR WIRE AND CUP IS VISIBLE.
- 3. ANY SOLDER ON THE OUTSIDE SURFACE OF THE SOLDER CUP IN THE FORM OF A THIN FILM.

ACCEPTABLE



NOT ACCEPTABLE







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FIGURE 10. Leaded surface mounted part solder fillet (see 5.11.3).



FIGURE 11. J-leaded and V-leaded solder fillet (see 5.11.3).





ACCEPTABLE

NOT ACCEPTABLE





FIGURE 12. Leadless chip carrier solder fillet (see 5.11.4).



FIGURE 13. Chip side overhang (see 5.11.6).



FIGURE 14. Minimum lap of chip on terminal area (see 5.11.6).



FIGURE 15. Solder fillet - chip devices (see 5.11.6).



NOT ACCEPTABLE

FIGURE 16. Excessive solder - parts encased (see 5.11.6).



FIGURE 17. Mounting of MELFs (see 5.11.6).



FIGURE 18. MELF solder fillet (see 5.11.6).



FIGURE 19. Wire and lead wrap/continuous runs (see 5.13).

APPENDIX A

CONTROL OF FLUXES

10. SCOPE.

10.1 <u>Scope</u>. This appendix defines testing that is mandatory when a contractor elects to use nonresin or low residue (LR) fluxes. Testing must be performed prior to implementation on production hardware. It should be noted that this document identifies the minimum test requirements and additional tests or more harsh testing environments may be required for some applications.

10.2 <u>Intent</u>. The intent of this appendix is to set forth a standard screening test methodology which yields data on the use of nonrosin fluxes, in combination with the specific soldering and cleaning processes to be used for manufacturing product. Separate test options can be selected depending on the level of technology of the product: through-hole; surface mount; or mixed technology.

20. APPLICABLE DOCUMENTS.

20.1 Government documents.

20.1.1 <u>Specifications, standards and handbooks</u>. The following specifications, standards and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATIONS

MiL-F-14256 Flux, Soldering, Liquid, Paste Flux, Solder Paste and Solder-Paste Flux (For Electronic/Electrical Use) General Specification For

(Unless otherwise indicated. copies of federal and military specifications, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building #4. Section D, Philadelphia, PA 19111-5094).

20.2 <u>Nongovernment publications</u>. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS (IPC)

- IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits
- IPC-B-36 IPC Standard Test Assembly for CFC Replacement Testing

- IPC-TR-580 Cleaning and Cleanliness Test Program, Phase 1 Test Results
- IPC-TM-650 Test Methods Manual
- IPC-SF-818 General Requirements for Electronic Soldering Fluxes
- IPC-TR-1043 IPC Cleaning and Cleanliness Test Program, Phase 3, Water Soluble Fluxes Test Program, Part 1
- IPC-TR-1044 IPC Cleaning and Cleanliness Test Program, Phase 3, Water Soluble Fluxes Test Program, Part 2

(Application for copies should be addressed to the Institute for Interconnecting and Packaging Electronic Circuits, 7380 North Lincoln Avenue. Lincolnwood, IL 60646.)

30. TERMS AND DEFINITIONS.

30.1 <u>Terms and definitions</u>. In addition to those listed below, the definitions applicable to this standard shall be in accordance with IPC-T-50.

30.2 <u>Flux</u>. A chemically-active compound which, when heated, removes minor surface oxidation, minimizes oxidation of the basis metal, and promotes the formation of an intermetallic layer between solder and basis metal.

30.3 Low residue (LR) flux. Formulations of fluxes which minimize or eliminate the need for post-solder cleaning operations.

30.4 <u>Paste flux</u>. A flux formulated in the form of a paste to facilitate its application.

30.5 <u>Polyglycol</u>. Polyglycols are materials with polyether linkages, such as polyethylene glycol, or a material generally derived by the reaction of organic acids, amines, alcohols, phenols, or water with ethylene or propylene oxide or their derivatives. This family of materials includes, but is not limited to, polyethylene glycol, polypropylene glycol, and a wide range of polyglycol surfactants. This family of materials does not include glycols (e.g., ethylene glycol), polyols (e.g., glycerine), or mono-, di-, or triglycol ethers.

30.6 <u>Solder-paste flux</u>. Solder paste without the solder particles.

30.7 <u>Solder paste</u>. Finely divided particles of solder, with additives to promote wetting and to control viscosity, tackiness, slumping, drying rate, etc., that are suspended in a paste flux.

40. GENERAL REQUIREMENTS.

40.1 <u>Nonrosin based fluxes for component tinning</u>. Nonrosin based fluxes may be used for tinning component leads of sealed devices, epoxy bodied parts, solid bus wire, and terminals provided the following process information is available for review:

a. Chemical characterization of each flux to assure adequate incoming inspection control;

- b. A detailed control system for procurement, receiving, testing, storage, usage, and application;
- c. Detailed flux removal and cleaning processes, and process monitoring requirements; and
- d. Proof of cleanliness testing methods and results.

The system for controlling nonrosin flux usage shall meet the requirements of paragraphs 4.5.3 and 4.5.4 of this standard.

40.2 <u>Nonrosin based fluxes for soldering printed wiring assemblies</u>. Nonrosin based and LR fluxes may be used for soldering component leads of sealed devices, epoxy bodied parts, solid bus wire, and terminals to printed wiring assemblies, provided the following Level 1 and Level 2 testing information is available for review.

40.2.1 <u>Polyglycol based flux</u>. Fluxes containing polyglycols (type WSF-1) generally present a greater cleaning challenge and require a thorough understanding of how the polyglycols interact with materials being cleaned.

40.2.2 <u>Minimum testing requirement</u>. Level 1 tests (see 40.2.3) shall be performed for all nonrosin or LR fluxes which are not qualified to MIL-F-14256 and listed on its Qualified Products List. In addition, Level 2 tests shall be performed on all nonrosin or LR fluxes. The Level 2 test performed shall be representative of the type of attachment technology used on the assembly (surface mount, mixed technology, or plated-through hole). Since Level 2 tests are process and product specific, test data from one facility should not be used by another as the sole source for verification.

40.2.3 Level 1 tests. If a nonrosin or LR flux is not listed on the Qualified Products List for MIL-F-14256, then either the user or the flux manufacturer shall perform and meet all of the MIL-F-14256 qualification requirements, less submission of the qualification test report to the qualifying activity. The contractor (flux user) shall maintain a copy of the qualification data which shall be available for review. In addition, the contractor (user) shall have sufficient chemical characterization test data and verification inspection data to ensure that flux received and used corresponds to the flux tested in the qualification report.

40.2.4 Level 2 tests. Level 2 tests are used to evaluate the ability of cleaning processes (or lack thereof for type LR fluxes to be used in a low residue soldering process) to remove fluxes from an assembly which represents the type of product which will be cleaned during actual production. Surface Insulation Resistance (SIR), ionic cleanliness testing, and a visual inspection shall be performed. These tests are based on the IPC Cleaning and Cleanliness Test Protocol. Phase 3, Water Soluble Fluxes, Part II, IPC-B-36 Testing. Type LR fluxes shall be tested both after cleaning and without cleaning. The results of both tests shall be reported separately in the gualification report.

40.2.4.1 <u>Test assembly</u>. The IPC-B-36 test assembly, or equivalent, shall be used. The test boards shall be made of the same materials which will be used in the production hardware. A non-deliverable production assembly may be used as the test assembly. Equivalent assemblies shall be representative

of the most difficult cleaning conditions (e.g., smallest part spacings, etc.) found in production hardware. As a minimum, the alternate assemblies shall present the same cleaning challenges as the IPC-B-36 test assemblies and shall have test pattern spacing equal to or less than those on the IPC-B-36 assembly.

40.2.4.2 <u>Simulation of production conditions</u>. For surface mount and mixed technology assembly, the test assemblies shall be assembled Using the solder paste application, component mounting, reflow, and cleaning equipment and processes which will be used in actual production. For plated-through hole assemblies, the test assemblies shall be assembled using the methods specified herein (see 40.2.4.4). When required, minor variations in equipment and process flow may be used to compensate for the differences between the test assembly and actual production hardware. Where the test method specifies use of equipment which will not be used in actual production, the contractor may substitute actual production equipment.

40.2.4.3 <u>Mounting of chip carriers</u>. At least four 68-castellation leadless chip carriers shall be mounted on each test assembly. See 40.2.4.5.1.

40.2.4.4 <u>Plated-through hole assemblies</u>. The test assembly preparation techniques of 40.2.4.4 through 40.2.4.4.2.2 are appropriate for preparing the surface mount test vehicle to be subject to processes designed for plated-through hole assemblies. The IPC-B-36 test assembly shall be assembled, soldered, and cleaned before being subjected to the soldering and cleaning processes proposed for production.

40.2.4.4.1 <u>Reflow method</u>. This method may be used by facilities possessing mass reflow soldering equipment (i.e., infrared, condensation, vapor phase, hot gas, laser, etc., but not including soldering irons). After assembling and pre-test cleaning (see 40.2.4.4.1.1 and 40.2.4.4.1.2), the test assembles shall be subjected to the fluxing and soldering process which will be used in actual production.

40.2.4.4.1.1 <u>Assembly preparation and component mounting</u>. Solder paste shall be applied in a manner which assures consistent and repeatable solder volume and consistency (e.g., weight). The leadless chip carriers shall be placed on the tacky solder paste, the solder paste shall be adequately-dried (if drying is recommended by the paste manufacturer), and the assembly reflowed.

40.2.4.4.1.2 <u>Pre-test cleaning</u>. After completion of the assembly preparation, component mounting and reflow procedures, the assemblies shall be cleaned. After cleaning, cleanliness testing in ionic conductivity test equipment shall demonstrate a baseline conductivity of less than 0.155 micrograms per square centimeter (one microgram per square inch).

40.2.4.4.2 <u>Additive (machine or manual) soldering method</u>. This method may be used by facilities which do not possess mass reflow soldering equipment. After assembly preparation and pre-test cleaning, assemblies shall be processed using the proposed flux and soldering processes which are to be used in actual production.

NOTE: This method can also be used for hand soldering using flux-cored solder or liquid flux and solid wire solder. First. mount the leadless chip carriers on the four corners of the board using adhesive as described below. Next solder the leadless chip carriers to the board's lands using the proposed flux, solder, and soldering equipment.

40.2.4.4.2.1 <u>Assembly preparation and component mounting</u>. The IPC-B-36 test assembly shall be modified to allow for component mounting without the use of a solder paste.

- a. The test boards shall be fabricated without the dry film solder mask standoffs.
- b. An adhesive shall be applied to the area where the dry film solder mask would have been applied. The adhesive shall be applied in such a manner as to ensure a maximum stand-off height of 0.13 mm (0.005 inch) above the laminate surface. The adhesive dots should not overflow onto the copper test patterns. The adhesive chosen should not contribute to ionic contamination nor promote corrosion.
- c. The leadless chip carriers shall be mounted in the adhesive and then the adhesive shall be cured in accordance with the manufacturer's recommendations. After bonding, the leadless chip carriers shall be fluxed, but need not be soldered to the assembly.

40.2.4.4.2.2 <u>Pre-test cleaning</u>. After completion of the assembly preparation. component mounting and soldering procedures, the assemblies shall be cleaned. After cleaning, cleanliness testing in ionic conductivity test equipment shall demonstrate a baseline conductivity of less than 0.155 micrograms per square centimeter (one microgram per square inch).

40.2.4.5 <u>Detailed Level 2 test conditions</u>. Additional information may be found in IPC-TR-1043 and IPC-TR-1044, IPC Cleaning and Cleanliness Test Program, Phase 3, Water Soluble Fluxes Test Program.

40.2.4.5.1 <u>Sample size</u>. Twelve test assemblies are required. Six assemblies shall be assembled with four 68-castellation leadless chip carriers mounted on the four quadrants. Three of these will be used for cleanliness testing and three for SIR testing. Additionally, six control boards (three for cleanliness testing and three for SIR testing) shall not be processed beyond the initial pre-test preparation.

40.2.4.5.2 <u>Component mounting</u>. For each of the assemblies tested, four leadless chip carriers shall be mounted on the four quadrants of the test assemblies. The leadless chip carriers shall be non-functional (empty). Components shall not be mounted on the control assemblies.

40.2.4.5.3 <u>Assembly processing</u>. Except as provided herein, all test assemblies shall be fabricated in accordance with the pre-test preparation procedures outlined in IPC-TR-580. The finished test assemblies shall not be conformal coated.

40.2.4.5.4 <u>Ionic cleanliness testing</u>. After flux application, soldering and assembly cleaning, three of the test assemblies and three of the control assemblies shall be subjected to the ionic cleanliness tests of this standard. Prior to cleanliness testing, the components on the test assemblies shall be removed in a manner which does not contribute to nor remove contamination. The test assembly and its respective leadless chip carriers shall be tested at the same time. The test parameters, including the equipment manufacturer and model number, temperature of the test solution, test cell volume, starting resistivity, and test duration shall be recorded for each test.

40.2.4.5.4.1 <u>Minimum ionic cleanliness</u>. The tested assemblies shall pass the ionic cleanliness requirements of this standard (see 4.23).

40.2.4.5.5 <u>Surface Insulation Resistance (SIR) testing</u>. At least three of the test assemblies and at least three of the control assemblies shall be subjected to SIR testing. IPC-TR-1043. IPC-TR-1044, and IPC-TM-650. Method 2.6.3.3 may be consulted for guidance. The SIR test is a seven-day test (as measured starting at T_o), using a constant $85^{\circ}C \pm 2^{\circ}C$ ($185^{\circ}F \pm 4^{\circ}F$). 85% RH ($\pm 3\%$ RH) environment. The SIR test shall be conducted in accordance with (a) through (g), below.

- a. Resistance measurements shall be made at +100 (\pm 5) volts DC, with a 60-second electrification time. The nonmeasurement bias voltage, applied to all patterns wherever measurements are not being made, shall be -50 (\pm 2.5) volts DC.
- b. The chamber conditions shall be ramped up to the test conditions as follows (see figure A-1): The chamber shall be at 25°C (77°F) and 50% RH when the test boards are inserted. The test boards shall stabilize for two hours, then the initial resistivity (T_i) shall be measured and recorded. The temperature shall then be ramped from 25°C to 85°C (77°F to 185°F) over a 30-minute period. During this ramp-up period, the humidity may drop to 10 - 20% RH. The temperature shall be held at 85°C (185°F) for two hours. The humidity shall then be ramped to 85% RH over a 30-minute period.
- c. Once the conditions have stabilized for two hours, the -50 ± 2.5 VDC bias shall be applied and the 168-hour exposure shall begin (T_a). The temperature and humidity profile shall follow figure A-1.
- d. Surface resistance measurements shall be taken at 24 hours (T_1) . 96 hours (T_2) , and 168 hours (T_3) . The resistance at T_2 and T_3 shall be at least 100 megohms.
- NOTE: Although there are no established pass/fail criteria for the measurement taken at 24 hours (T_1) , the measurement is taken to ascertain how the flux is reacting during that phase of the test.
- e. At the end of the 168-hour exposure, the bias voltage shall be turned off for the remainder of the test. The conditions shall be ramped down to ambient conditions as follows: The humidity shall be ramped from 85% to approximately 50% RH over a 30-minute

period. The temperature shall then be ramped from $85^{\circ}C$ ($185^{\circ}F$) to approximately $25^{\circ}C$ ($77^{\circ}F$) over a 30-minute period. The humidity shall then be set to and stabilized at 50° RH.

- f. Two hours after the chamber has stabilized at approximately $25^{\circ}C$ (77°F) and 50% RH, the surface resistance shall be measured (T₄). Surface resistance shall be at least 500 megohms.
- g. After completion of the final measurements, the test assemblies shall be removed from the chamber and examined under a microscope at 7-10X, using a strong light source to backlight the test assembly.

40.2.4.5.5.1 <u>SIR test minimum cleanliness results</u>. The test assemblies shall not exhibit dendritic growth or evidence of other forms of electrochemical migration of residues (contamination) between adjacent conductors of the test patterns.

40.2.4.5.5.2 <u>Classification of visual defects</u>. Failures that are traceable to special cause process or material anomalies, not related to flux chemistry or cleaning, shall be documented and that pattern shall be excluded from the data set. No more than two test patterns may be excluded. Documentation describing the contamination, the results of the examination, and the rationale for excluding a test pattern shall be available for review. The documentation shall include a color photograph of the anomaly which shall be taken at a minimum magnification of 10X.



FIGURE A-1. Temperature and humidity profile for IPC-B-26 testing.

APPENDIX B

PART MOUNTING REQUIREMENTS

10. SCOPE.

10.1 <u>Scope</u>. This appendix defines mandatory part mounting requirements which may be omitted if the contractor has defined and included alternate, detailed part mounting requirements on the approved assembly drawing.

20. APPLICABLE DOCUMENTS. Not applicable.

30. TERMS AND DEFINITIONS. Not applicable.

40. GENERAL REQUIREMENTS.

40.1 Lead terminations. The length of the clinched portion of wires and component leads shall be no less than one-half the largest dimension (usually the diameter) of the terminal area or 0.8 mm (0.03 inch), whichever is greater, and no more than the diameter (or length) of the termination area (see figure B-1A). The lead length shall be determined prior to soldering. The clinch of leads on opposite ends or sides of a component shall be directed in opposite directions (see figure B-1B).

40.1.1 <u>Lead clinch restrictions</u>. Fully clinched leads are not applicable for leads of dual-inline packages (DIPs) or pins of other type modules. Fully clinched or partially clinched leads are not applicable for tempered pins or for leads over 1.3 mm (0.050 inch) in diameter.

40.1.2 <u>Partial clinch of dual-inline package leads</u>. Bends should be outward (away from the center of the part body). If manual clinching is used, only corner leads of DIPs may be partially clinched.

40.1.3 <u>Straight-through lead terminations</u>. Component leads terminated straight through shall be discernable and may extend a maximum of 1.5 mm (0.060 inch) above the termination area.

40.2 <u>Unsupported hole lead terminations</u>. When unsupported holes are used, leads shall be fully clinched.

40.3 <u>Parts and components mounted to printed wiring boards</u>. Axial and nonaxial-leaded components shall be mounted on only one side of a printed wiring assembly if the leads are dressed through holes. Surface mounted components may be mounted on either or both sides of a printed wiring assembly. On mixed technology assemblies with surface mounted components on both sides, through-hole components should be mounted on one side of the printed wiring board but may be mounted on both sides. As an exception, packaging and interconnect structures (P&IS) may contain a through-hole mounted connector on each side of the P&IS.

40.4 <u>Hole obstruction</u>. Parts and components shall be mounted such that they do not obstruct solder flow onto the topside termination areas of plated-through holes (see figure B-2).

40.5 <u>One lead per hole</u>. No more than one item, whether wire or component lead, shall be inserted in any one hole.

40.6 Attachment of parts.

40.6.1 <u>Lead attachment</u>. Component leads shall be either surface mounted in through holes. or mounted to terminals. Lead and wire terminations shall be soldered.

40.6.2 <u>Mechanical support</u>. All parts weighing 7.1 g (0.25 ounce) or more per lead shall be supported by clamps, spacers, or other means which ensure that the solder connections and leads are not relied upon for mechanical support. Potentiometers and other devices which may be adjusted mechanically shall be mounted in accordance with 40.10.2.5 through 40.10.2.5.3.

40.6.3 <u>Stress relief</u>. Axial or opposed lead devices with leads terminating at a connection point shall have a minimum lead-connection-to-body offset of at least 2 lead diameters or thicknesses, but not less than 0.75 mm (0.030 inch). Where the component body will not be secured to the mounting surface by bonding, coating, or other means, the lead(s) on only one of the opposing sides of the component need be so configured. Typical examples of stress relief are included in figure 6.

40.6.4 <u>Devices mounted over circuitry</u>. Parts mounted over protected surfaces, insulated parts over circuitry, or surfaces without exposed circuitry, may be mounted flush. Parts mounted over exposed circuitry shall have their leads formed to allow a minimum of 0.25 mm (0.010 inch) tetween the bottom of the component body and the exposed circuitry.

NOTE: Nonelectrical planes and vias used for heat dissipation are not considered circuitry.

40.6.5 <u>Maximum attachments to terminals</u>. There shall be no more than three attachments to any terminal other than turret or bifurcated terminals and there shall be no more than three attachments to any terminal section of turret and bifurcated terminals.

40.7 <u>Metal case component insulation</u>. Metal cased components shall be insulated from adjacent electrically conductive elements. Insulation material shall be compatible with the circuit and printed wiring board material.

40.8 <u>Moisture traps</u>. Parts and components shall be mounted such that the formation of moisture traps is precluded.

40.9 <u>Use of buffer material with conformally coated assemblies</u>. When type ER conformal coating is applied to glass bodied components, buffer material is required.

NOTE: Board designers are cautioned to consider that buffer material may be needed when allocating space and location for components to be mounted on printed wiring boards covered by this standard. 40.10 Detailed part mounting of through-hole mounted components.

40.10.1 Axial-leaded components.

40.10.1.1 <u>Jumper wires</u>. Jumper wires mounted and soldered in accordance with initial design requirements shall be treated as axial-leaded components and shall conform to the detail requirements herein stated for axial-leaded components.

40.10.1.2 <u>Axial-leaded parts</u>. Axial-leaded parts shall be mounted as specified on the approved assembly drawing and mounted approximately parallel so that the body is within 0.65 mm (0.025 inch) of the board surface.

40.10.1.3 <u>Clinched wire interfacial connections</u>. The wire connecting circuitry on opposite sides of the board or assembly which are not completed via a plated-through hole shall be uninsulated, solid, tinned, copper wire and shall be dressed through the unsupported (unplated) hole, clinched, and soldered to the terminal area on each side of the board or assembly. The clinched wire shall contact the terminal area on at least one side of the printed wiring board and shall approximate contact on the other side (normal springback to one half the wire diameter is acceptable). The clinched portions of the wire shall meet the requirements for clinched component leads. Unless both clinched portions are soldered and cooled simultaneously, the two connections shall be step-soldered (see figure B-3).

40.10.2 <u>Nonaxial-leaded components with leads extending from a single</u> <u>surface</u>. Nonaxial-leaded components shall be either side mounted or mounted with the surface from which the leads egress (the base) parallel to the surface of the printed board within the spacing tolerances specified herein.

40.10.2.1 <u>Minimum lead extension</u>. Leads shall extend straight from the base of the part and lead bends shall not extend to the part body or weld.

40.10.2.2 <u>Meniscus trimming</u>. Trimming of the lead coating meniscus is prohibited.

40.10.2.3 <u>Meniscus spacing</u>. There shall be a visible clearance between the coating meniscus on each lead and the solder connection (see figure B-4).

40.10.2.4 <u>Freestanding components</u>. When components are mounted freestanding, the spacing between the surface of the component and the surface of the board shall be a minimum of 0.75 mm (0.030 inch) and a maximum of 3.2 mm (0.125 inch) (see figure B-5). In no instance shall nonparallelism result in nonconformance within the minimum or maximum spacing limits.

40.10.2.5 <u>Supported components</u>. When components are supported, they shall be supported on:

a. Resilient feet or standoffs integral to the component body (see figure B-6A and B-6B) which shall be mounted in contact with the board, or

b. A separate standoff (see figure B-6C), or a specially configured nonresilient footed standoff (see figure B-6D) which shall be mounted in contact with the component and the board (see figure B-7).

40.10.2.5.1 <u>Footed standoffs</u>. Footed standoffs shall have a minimum foot height of 0.25 mm (0.010 inch).

40.10.2.5.2 <u>Standoff positioning</u>. No standoff shall be inverted.

40.10.2.5.3 <u>Nonresilient footed standoffs</u>. When a specially configured nonresilient footed standoff is utilized, that portion of the lead in the lead bend cavity (see figure B-8) shall be formed to coincide with an angular line extending from the lead insertion hole in the standoff device to the lead attachment hole in the printed wiring board and seated in accordance with 40.10.2.5.b.

40.10.2.6 <u>Side and end mounting</u>. When components are side or end mounted, the part body shall either be bonded to the printed wiring or be constrained in a manner which prevents movement during shock and vibration.

40.10.2.7 <u>In-line connectors</u>. In-line printed wiring board connectors may be mounted in full contact with the printed wiring board. Connectors mounted in full contact with the board shall be designed so that there are both stress relief provisions internal to the connector body and cavities (either visible or hidden) which preclude blocking of plated-through holes.

40.10.2.8 <u>Tall profile components</u>. Tall profile transformers and other devices with center of gravity in the upper half of the component body shall be mounted in accordance with 40.10.2.5 through 40.10.2.5.3 regardless of lead diameter or weight per lead ratios.

40.10.2.9 <u>Metal power packages</u>. Components of the metal power package configuration shall not be mounted freestanding. These components shall be mounted:

- a. in accordance with 40.10.2.5 through 40.10.2.5.3, or.
- b. if the leads are neither tempered nor greater than 1.3 mm (0.050 in) in diameter, and stress relief is provided, they may be side-mounted, through-board mounted, or mounted on nonresilient standoffs.

The leads of all components of the metal power package configuration shall be stress relieved in accordance with a stress relief method corresponding to the mounting technique.

40.10.2.10 <u>Mounting metal power packages to an assembly</u>. Metal power packages, standoffs, heat sink frames and resilient spacers on which metal power packages are mounted shall be of a configuration which does not block the plated-through holes, precludes excessive stresses (provides stress relief) and facilitates cleaning.

40.10.2.11 <u>Insulating metal power packages from underlying circuitry</u>. Lead holes shall not be plated-through if the component body is mounted in contact with the board or circuitry thereon.

40.10.3 <u>Nonaxial-leaded components with leads extending from more than</u> <u>a single surface</u>. Leads shall not be truncated.

40.10.3.1 <u>Dual-inline packages</u>.

40.10.3.1.1 <u>Base contact</u>. The base of the device shall be spaced from the surface of the printed wiring board a maximum of either 1.1 mm (0.043 inch) or the lead shoulder, whichever is greater. The base of the device may be in contact with the board surface. The spacing shall be selected such that the part is not mounted directly on conductive circuitry. When placed over conductive circuitry, the part shall be spaced off of the board such that contaminants may be cleaned from underneath.

40.10.3.1.2 Use of standoffs with dual-inline packages. When a separate resilient standoff is utilized in conjunction with a DIP, mounting shall be in accordance with 40.10.2.5 through 40.10.2.5.3. Standoffs shall be mounted in contact with the component and the printed wiring board.

40.10.3.1.3 <u>Dual-inline packages mounted to heat sinks</u>. DIPs mounted directly to heat sink frames shall have stress relief provisions included. Heat sink frames must comply with the hole obstruction requirements of 40.4.

NOTE: The inclusion of a pliable spacer material between the heat sink frame and the printed wiring board is an acceptable method for assuring stress relief provided the resilient added material is of sufficient thickness (0.5 mm (0.02 inch) typical) to compensate for forces imposed during temperature change.

40.10.4 <u>Terminal shank discontinuities</u>. The shank of the terminal shall not be perforated nor split, cracked, or otherwise discontinuous to the extent that oils, flux, inks, or other liquid substances utilized for processing the printed board are or can be entrapped within the mounting hole. Circumferential cracks or splits in the shank are not acceptable regardless of extent.

40.10.5 <u>Terminal flange discontinuities</u>. The terminal flange shall not be split, cracked, or otherwise discontinuous to the extent that flux, oils, inks, or other liquid substances utilized for processing the printed board can be entrapped within the mounting hole. After swaging, the flange shall be free cf circumferential splits or cracks, but may have a maximum of three radial splits or cracks provided that the splits or cracks are separated by at least 90 degrees and do not extend beyond the rolled area of the terminal (see figure B-9).

40.10.6 <u>Terminals used for mechanical mounting</u>. Terminals not connected to printed wiring or printed ground planes shall be of the rolled flange configuration. A printed foil pad may be utilized as a seating surface for a rolled flange provided that the pad is isolated and not connected to active printed wiring or ground plane.

NOTE: When a rolled flange is used in conjunction with an electrically inactive pad, solder is neither necessary nor particularly desirable.

40.10.7 <u>Terminals used for electrical mounting</u>. The flared flange terminals configuration (figure 3) shall be utilized only in conjunction with terminal areas (isolated or active) or ground planes; they shall not be flared to the base material of the printed board. Terminals shall be mounted in accordance with 40.10.7.1 through 40.10.7.3.

40.10.7.1 <u>Flange angles</u>. Flared flanges shall be formed to an included angle between 35 and 120 degrees and shall extend between 0.4 mm (0.015 inch) and 1.5 mm (0.060 inch) beyond the surface of the terminal area provided minimum electrical spacing requirements are maintained (see figure B-10) and the flare diameter does not exceed the diameter of the terminal land area.

40.10.7.2 <u>Hole support</u>. Terminals shall only be mounted in unsupported holes. If it is essential that a terminal be utilized for interfacial connection, a dual hole configuration incorporating a supported plated-through hole shall be combined with an unsupported hole interconnected by a terminal area on the solder side of the printed wiring board (see figure B-11). As an exception, the terminal may be mounted in a plated-through hole with a nonfunctional land on the component side (see figure B-12).

40.10.7.3 <u>Unacceptable configuration</u>. Terminals with a funnel shoulder on the component side shall not be used (see figure B-13).

40.10.8 <u>Mounting to terminals</u>. Whether terminals are mounted to printed boards, terminal boards or chassis members, components and wires shall be mounted in accordance with 40.10.8.1 through 40.10.8.6.

40.10.8.1 <u>Service loops</u>. Lead wires shall be dressed in the proper position with a slight loop or gradual bend as shown in figure B-14. The bend shall be sufficient to preclude tension on the connection when such is finished and to permit one field repair.

40.10.8.2 <u>Orientation of wire wrap</u>. Lead wires may be wrapped clockwise or counterclockwise but shall continue the curvature of the dress of the lead wires (see figure B-15) and shall not interfere with the wrapping of other wires on the terminal.

40.10.8.3 <u>Stress relief</u>. Unless mounted with the component body seated to a printed board, terminal board, or chassis with stress bends as shown in figure 6, components shall be mounted such that the body is displaced with respect to the terminal to which they are attached as shown in figure 6.

40.10.8.4 <u>Bifurcated terminals</u>. The order of preferred terminations of bifurcated terminals shall be as follows:

40.10.8.4.1 <u>Side route connection</u>. The wire or component lead shall be dressed through the slot and wrapped to either post of the terminal (see figure B-16A) and shall be in contact with the flat surfaces of two nonadjacent sides (see figure B-16B). The wire or lead shall also be in firm

contact with the base of the terminal or the previously installed wire (see figure B-16C). The number of attachments shall be limited to three per terminal post and shall be maintained such that:

a. Spacing betwee gires, and spacing between the wires and the terminal boarc panel is a minimum consistent with the thickness of the wire insulation.

b. The wraps are dressed in alternate directions (see figure B-16D).

40.10.8.4.2 <u>Bottom route connection</u>. The wire shall be wrapped on the terminal post and shall be in contact with the flat surfaces of two nonadjacent sides. The wire lead shall also be in firm contact with the base of the terminal or the previously installed wire. When more than one wire is to be attached, they shall be inserted at the same time but shall be wrapped separately around alternate posts.

40.10.8.5 <u>Hook terminals</u>. The maximum wire fill shall not exceed the end of the hooks There shall be no more than three conductors for each terminal.

40.10.8.6 <u>Pierced or perforated terminals</u>. For wiring to a single terminal, the wire shall pass through the eye and be wrapped around the terminal (see figure B-17). When a continuous run is used, the wire shall be attached to the end terminals (first and last) in the same manner that wires are attached to single terminals. The jumper wire shall contact at least two nonadjacent contact surfaces of each intermediate terminal (see figure 19).

40.11 <u>Surface mounted assembly requirements</u>.

40.11.1 <u>External connections to packaging and interconnect structures</u> (<u>P&IS</u>). Where P&IS are used to provide controlled thermal expansion, they [1] not be connected to external system elements (i.e., chassis or heat sinks) which will degrade the thermal expansion control below design limits.

40.11.2 <u>Body positioning</u>. The body of a surface mounted axial-leaded component shall be spaced from the surface of the printed wiring board a maximum of 0.6 mm (0.024 inch) (see figure B-18). Leads on opposite sides of surface mounted axial-leaded components shall be formed such that component cant (nonparallelism between the base surface of the mounted component and the surface of the printed wiring board) is minimal and in no instance shall body cant result in nonconformance with the maximum spacing limits.

40.11.3 <u>Vertical mounting</u>. If the vertical (V) dimension of reflow configuration chips is greater than the thickness (T) dimension, then reflow configuration chips should not be used in assemblies subject to high vibration or shock loads, especially in airborne or missile systems. Vertical mounting shall be utilized for:

- Low and tall-profile surface mount devices with reflow termination pads located on a single base surface;
- b. Nonaxial-leaded devices with leads egressing from two or more sides of the device(s); and

c. Nonaxial leaded devices with leads egressing from a single base surface.

40.11.4 Leaded parts.

40.11.4.1 <u>Perpendicular mounting</u>. Under no circumstance shall surface mounting for perpendicular axial leaded components be used.

40.11.4.2 <u>Flatpacks</u>. Leads on opposite sides of surface mounted flatpacks shall be formed such that the nonparallelism between the base surface of the component and the surface of the printed wiring board (i.e., component cant) is minimal. Component cant is permissible provided the final configuration meets the maximum spacing requirement.

40.11.4.3 Lead forming to prevent deflection. Leads shall be formed such that they will contact the termination area upon mounting without the need to impart stress on the lead to accomplish soldering.

40.11.4.4 <u>Parts not configured for surface mounting</u>. Flatpacks of the through-hole configuration, DIPs, transistors, metal power packages, and other nonaxial-leaded components shall not be surface mounted unless the leads are formed to meet the surface mounted device lead forming requirements.

40.11.4.5 <u>Miniature axial-leaded components</u>.

40.11.4.5.1 <u>Rectangular leads</u>. Components with axial leads of rectangular cross section shall be mounted in accordance with the requirements for ribbon leads of flatpacks.

40.11.4.5.2 <u>Coined leads</u>. Components with axial leads of round cross section may be coined or flattened for positive seating in surface mounting. If coining or flattening is used, the flathead thickness shall be $50 \pm 10\%$ of the original diameter (see figure B-18). Flattened areas of leads coined for surface mounting shall be excluded from the 10 percent deformation requirement.

40.11.5 <u>Dual-inline packages</u>. DIPs may be surface mounted provided the leads are formed into a configuration which meets the mounting requirements for surface mounted leaded parts (i.e., flatpacks). The leads of surface mounted DIPs shall be bent outward only. This lead forming operation shall be performed using die forming systems (hand forming is prohibited). The lead forming operation shall not cause lead seal cracks to exceed the limits imposed in the initial part specification. The use of butt mounted DIPs is prohibited.

40.11.6 <u>Other devices</u>. TO-can devices, tall-profile components (i.e., over 15 mm (0.60 inch)), transformers, and metal power package devices may be surface mounted provided the parts are bonded or otherwise permanently secured to the board in a manner which enables the part to withstand the end-item. shock, vibration, and environmental stresses.

40.11.7 <u>Break away tie bars</u>. As an exception to the lead cutting requirements of this document, components (e.g., connectors and flexible circuits) which incorporate break-away tie bars in their design may be installed or soldered in place prior to removal of the tie bar. Exposed basis metal resulting from tie bar removal is permissible.

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FIGURE B-1. Lead termination (clinched leads) (see 40.1).



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58



ACCEPTABLE

COMPONENT SEATED FLAT TO STANDOFF. FEET IN CONTACT WITH BOARD. A



NOT ACCEPTABLE

STANDOFF NOT IN CONTACT WITH BOARD.



NOT ACCEPTABLE

STANDOFF INVERTED. STANDOFF BLOCKS PLATED-THROUGH HOLE.

8



NOT ACCEPTABLE

STANDOFF TILTED. COMPONENT NOT SEATED FLAT TO STANDOFF. FEET DO NOT CONTACT BOARD. D



C

ACCEPTABLE

COMPONENT SEATED FLAT TO STANDOFF OF RESILIENT MATERIAL

BASE OF STANDOFF FLAT ON BOARD. E



NOT ACCEPTABLE

ALTHOUGH OF RESILIENT MATERIAL, STANDOFF CONCEALS CONNECTION ON COMPONENT SIDE OF BOARD.

F

FIGURE B-7. Mounting components using standoffs (see 40.10.2.5).



FIGURE B-8. Typical standoff devices (internal cavities) (see 40.10.2.5.3).



FIGURE B-9. Rolled flange terminals (see 40.10.5).



FIGURE B-10. Flare and extension of funnel flanges (see 40.10.7.1).







ACCEPTABLE

FIGURE B-12. Standoff terminal interfacial connection (see 40.10.7.2).

.



NOT ACCEPTABLE

FIGURE B-13. Funnel_shoulder_terminal_(see 40.10.7.3).



FIGURE B-14. Stress relief for lead wiring (see 40.10.8.1).



FIGURE B-15. Lead dress (see 40.10.8.2).



FIGURE B-16. Side route connections and wrap on bifurcated terminal (see 40.10.8.4.1)



FIGURE B-17. <u>Typical pierced or perforated terminal wire wrap</u> (see 40.10.8.6).



0.6mm (0.024 INCH) MAX ---



APPENDIX C

CLEANLINESS TEST METHODS

10. SCOPE.

10.1 <u>Scope</u>. This appendix defines standard cleanliness test methods for determining printed wiring assembly cleanliness. This appendix also delineates the requirements for evaluating a proposed change of the manufacturer's cleaning process and cleaning materials (e.g., solvents, cleaners, etc.).

20. APPLICABLE DOCUMENTS. Not applicable.

30. TERMS AND DEFINITIONS. Not applicable.

40. GENERAL REQUIREMENTS.

40.1 <u>Resistivity of solvent extract</u>. Solvent extract resistivity shall be measured as follows:

- a. Prepare a test solution of 75 +0/-2 percent by volume of reagent grade isopropyl alcohol, with the remainder being deionized water. Pass this solution through a mixed bed deionizer cartridge. After passing through the cartridge, the resistivity of the solution shall be greater than or equal to 6 ± 0.5 megohm-centimeters (conductivity shall be less than 0.166 micromhos/cm).
- b. Use a clean plastic bag, which can be sealed and which is free of ionic contamination. It is recommended that a heat sealable bag (e.g., Kapak® type or equivalent) which contributes no ionic contamination, be used. Another option uses a plastic "zipper locking" type bag, that has been rinsed with a portion of test solution. Measure 1.55 milliliters of fresh test solution for each square centimeter of assembly area (10 ml/sq.in.) into the clean plastic bag. The assembly area includes the areas of both sides of the board plus the components.
- c. Place the circuit board into the plastic bag with the test solution and seal the bag. The bag should be sufficiently large enough for the board, and the test solution shall be allowed to wash the surface of the board while in the bag. Shake the bag containing the circuit board and the test solution for approximately 10 minutes. Let the bag sit for 5 minutes with the assembly immersed in solution, then shake for an additional 5 minutes. Be careful not to let the corners of the board tear the bag while shaking.
- Remove the circuit assembly, and measure the ionic contamination of the test solution per 4.23. The final resistivity shall not be below 2 megohm-centimeters (conductivity is 0.5 micromhos/cm). A resistivity change from 6 to 2 megohm-centimeters indicates a contaminant level of 1.55 micrograms of ionic contaminant per square centimeter of board surface area.

40.2 <u>Sodium chloride salt equivalent ionic contamination test</u>. Sodium chloride salt equivalent ionic contamination shall be measured as follows:

- a. The sodium chloride salt equivalent ionic contamination test shall use a solution of 75 +0/-2 percent by volume of reagent grade isopropyl alcohol with the remainder being deionized water. The solution shall be verified for correct composition upon initial use, each shift, and according to manufacturer's recommendations. The time limit may be extended when the results of data provide a definite indication that such actions will not adversely affect the results of the test.
- b. The equipment must be validated using a known amount of sodium chloride standard on the same schedule as the percentage composition verification.
- c. The starting, or reference, purity of the solution shall be greater than 20 megohm-centimeters (conductivity shall be less than 0.05 micromhos/centimeter), before each sample is tested.
- d. The test length shall be in accordance with manufacturer's recommendations, but in no case shall be less than 10 minutes.
- e. The final conductivity is based on reference to the NaCl standard. However, the final ionic contamination shall be less than 1.55 micrograms per square centimeter of board surface area.

40.3 <u>Alternate methods</u>. Alternative equipment, with the appropriate equivalence values, may be used to verify cleanliness. The contractor shall develop equivalency factors for each individual system.

- NOTE: There are several commercially available ionic cleanliness testers that have shown to be equivalent to or more efficient than the resistivity of solvent extract method of 40.1. These alternative equipments may be either a static method, where the test solution is continually circulated in the test cell at a fixed volume and then measured, or a dynamic method, where the test solution is constantly being measured as the volume flows past the assembly. There are many variables of each system that will affect the final resistivity, i.e., heat, solution volume, or sprays.
- NOTE: Test procedures and calibration techniques for these methods are documented in Materials Research Report 3-78 "Review of Data Generated with Instruments Used to Detect and Measure Ionic Contaminants on Printed Wiring Assemblies." Application for copies of this report should be addressed to the Commanding Officer. Naval Air Warfare Center. Aircraft Division Indianapolis. Code DP3070N/MS-79, 6000 E. 21st Street. Indianapolis. IN 46219-2189.

50. DETAIL REQUIREMENTS.

NOTE: The following requirements are intended to be used when evaluating changes to a cleaning process and cleaning materials (i.e., solvents, cleaners, etc.). The following requirements are also intended for use when evaluating a new material to use as a replacement for chlorofluorocarbon-based cleaning solvents.

50.1 <u>Rosin flux cleaning; Phase II tested materials</u>. When evaluating a material which has been tested under the IPC/EPA/DOD Ad Hoc Solvents Working Group Phase II tests, the manufacturer shall prepare the following data:

- a. The intended cleaning process shall be documented in accordance with 4.3.2 and shall meet the requirements of 4.22.
- b. As required by 4.5, the manufacturer shall verify the intended cleaning material is compatible with the components, including the printed wiring board, solder masks, temporary maskants, and other process materials. The recommendations of the cleaning material manufacturer should be followed during this evaluation.
- c. Prior to use on production hardware, a test assembly should be cleaned and evaluated.
- d. Prior to use on production hardware, the manufacturer shall verify that the proposed cleaning system and material removes visually detectable contamination and that the assembly meets the ionic contamination requirements of 4.23 and 4.23.1.
- NOTE: Phase II approved materials have been tested by the Test Monitoring and Validation Committee of the IPC/EPA/DOD Ad Hoc Solvents Working Group and have been accepted by the DOD participants as providing cleaning characteristics equal to or better than chlorofluorocarbon-based solvents.

50.2 <u>Rosin flux cleaning; material not tested for Phase II</u>. When evaluating a material which has not been tested under the IPC/EPA/DOD Ad Hoc Solvents Working Group Phase II tests, the manufacturer shall prepare the following data:

- a. The material shall be tested in accordance with the requirements of the IPC/EPA/DOD Ad Hoc Solvents Working Group Phase II test program.
- b. The intended cleaning process shall be documented in accordance with 4.3.2 and shall meet the requirements of 4.22.
- c. As required by 4.5, the manufacturer shall verify the intended cleaning material is compatible with the components, including the printed wiring board, solder masks, temporary maskants, and other process materials. The recommendations of the cleaning material manufacturer should be followed during this evaluation.

- d. Prior to use on production hardware, a test assembly should be cleaned and evaluated.
- e. Prior to use on production hardware, the manufacturer shall verify that the proposed cleaning system and material removes visually detectable contamination and that the assembly meets the ionic contamination requirements of 4.23 and 4.23.1.

50.3 <u>Nonrosin flux cleaning systems</u>. When evaluating a cleaning material which will be used for cleaning of assemblies fluxed with nonrosin fluxes, the manufacturer shall prepare the following data:

- a. The proposed flux shall be evaluated in accordance with Appendix A.
- b. The intended cleaning process shall be documented in accordance with 4.3.2 and shall meet the requirements of 4.22.
- c. As required by 4.5, the manufacturer shall verify the intended cleaning material is compatible with the components, including the printed wiring board, solder masks, temporary maskants, and other process materials. The recommendations of the cleaning material manufacturer should be followed during this evaluation.
- d. Prior to use on production hardware, a test assembly should be cleaned and evaluated.
- e. Prior to use on production hardware, the menufacturer shall verify that the proposed cleaning system and material removes visually detectable contamination and that the assembly meets the ionic contamination requirements of 4.23 and 4.23.1.

APPENDIX D

CERTIFICATION OF PERSONNEL

10. SCOPE.

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10.1 <u>Scope</u>. This appendix defines detailed requirements for certification of personnel. These requirements are mandatory only when specifically required by contract. They are intended to supplement the requirements of 4.9 through 4.9.4.

20. APPLICABLE DOCUMENTS. Not applicable.

30. TERMS AND DEFINITIONS. Not applicable.

40. GENERAL REQUIREMENTS.

40.1 <u>Certification</u>.

40.1.1 <u>Certification of personnel</u>. Personnel performing soldering or inspection functions shall be certified in accordance with the following requirements prior to performing operations on deliverable articles. As a minimum, an individual shall be certified for those operations relating to MIL-STD-2000 which that individual will perform, and those operations shall be identified as part of the certification records.

40.1.2 <u>Visual acuity</u>. All personnel performing operations accordance with this standard shall meet vision requirements established by the contractors for the tasks assigned.

40.1.3 <u>Certification categories</u>. Certification certificates shall be issued in the following categories:

Instructor/Examiner Inspector Operator Operator/Inspector

Inspector. Operator and Operator/Inspector personnel shall be certified by the contractor. Operator/Inspectors shall be trained and certified as both operators and inspectors. The training program hall emphasize first pass yields, rework reduction, and defect documentation. Instructor/Examiner personnel shall be certification one of the following DOD Certification Centers:

- Naval Air Warfare Center Aircraft Division Indianapolis, IN (317) 226-5640
- b. Naval Air Warfare Center Weapons Drvision China Lake, CA (619) 446 5571

- c. U.S. Army Missile Command (MICOM) Redstone Arsenal, AL (205) 876-5902
- U.S. Army Armament Research Development & Engineering Center (ARDEC)
 Picatinny Arsenal, NJ (201) 724-4466

40.1.4 Authority.

40.1.4.1 <u>Instructor/Examiner</u>. Instructor/Examiner personnel are authorized to train, certify, recertify, and require recertification of Inspector, Operator, and Operator/Inspector personnel as defined herein. They are also authorized to monitor soldering processes and workmanship for compliance to this standard, and to perform inspections and solder operations.

40.1.4.2 <u>Inspector</u>. Inspector personnel are authorized to perform inspections for conformance to this standard.

40.1.4.3 <u>Operator</u>. Operator personnel are authorized to perform soldering and soldering related operations in conformance with this standard.

40.1.4.4 <u>Operator/Inspector</u>. Operator/Inspector personnel are authorized to perform inspections, soldering, and soldering related operations in conformance with this standard. Personnel certified to this category may inspect their own work as detailed in an approved quality assurance program.

40.1.5 <u>Limitation of authority</u>. The authority expressed herein shall be valid only at the same company, a division of the same company, or a subcontractor to the company which employs the certified individual on a full time basis.

40.1.6 <u>Prime contractor personne</u>]. All prime contractors shall have at least one Instructor/Examiner. When Appendix D is invoked, the person responsible for employee certification in accordance with 4.9.1 shall be a government certified Instructor/Examiner. It shall be the responsibility of the Instructor/Examiner to manage and control the certification of contractor personnel. The contractor shall designate a full-time employee of the contractor who is responsible for employee certification.

40.1.7 <u>saining programs</u>. The contractor shall establish and maintain an effective written training program to certify and recertify all personnel performing operations applicable to this standard. The training program is subject to review by the government and may be disapproved any time the requirements of this standard are not being met. Use of the Standardized Government and Industry Soldering Training Plan, TP-MT-0002, is authorized.

40.1.8 <u>Recertification</u>.

40.1.8.1 <u>Instructor/Examiners</u>. Recertification of Instructor/Examiner personnel shall be required at two-year intervals or when either the certificate holder changes employer or there is a reason to question proficiency.

40.1.8.2 <u>Inspectors, Operators, and Operator/Inspectors</u>. Recertification of Inspector, Operator, and Operator/Inspector personnel shall be required at two-year intervals or when either new techniques are to be employed which require new skills or the certificate holder changes employer.

40.1.8.3 <u>Recertification procedures</u>. Personnel requiring recertification shall be recertified by the same sources as those indicated for certification in 40.1.3. Recertification courses conducted by the contractor shall meet the requirements of 40.1.7, as conducted by an Instructor/Examiner in accordance with 40.1.4.1 and 40.1.5.

40.1.9 <u>Revocation of certified status</u>. Certifications shall be revoked when:

- a. The certificate holder fails to be recertified when required:
- b. The contractor training program fails to meet the requirements of this standard;
- c. Work produced by the employee does not meet the requirements of this standard: or
- d. The certificate holder leaves the employ of the certifying contractor.

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