Dist: A SEP 8 1994 8011

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	Aug 3, 1994	Final Report 1 April 93 - 30 Mar 94

4. TITLE AND SUBTITLE
Low temperature grown and highly non-stoichiometric GaAs and related materials

5. FUNDING NUMBERS
61102F
2305/CS

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Materials Research Society
9800 McKnight Road
Pittsburgh, PA 15237-6005

8. PERFORMING ORGANIZATION REPORT NUMBER
AFOSR-TR- 94 0574

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AFOSR/NE
110 Duncan Avenue Suite B115
Bolling AFB DC 20332-0001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
F49620-93-1-0236

11. SUPPLEMENTARY NOTES

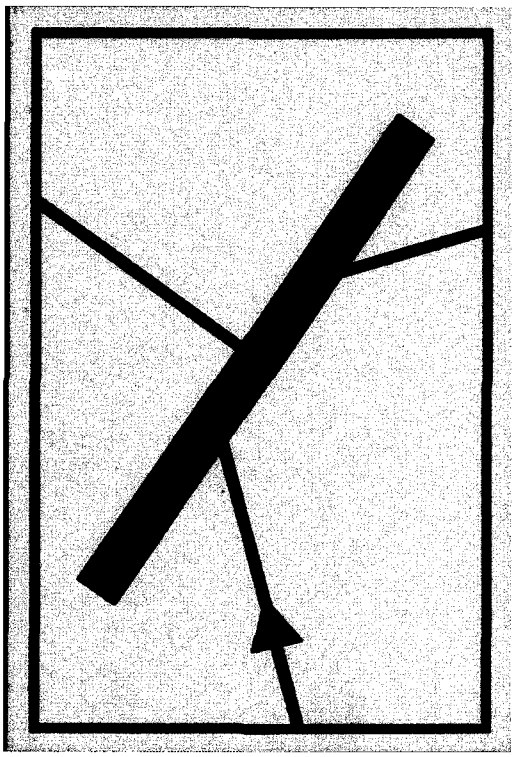
12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release distribution unlimited
A

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)
Selected proceedings of a two-day symposium on the subject topic held at the Spring Meeting of the Materials Research Society, April 12-16, 1993.

14. SUBJECT TERMS	15. NUMBER OF PAGES
LT GaAs, Alon-Stoichiometric GaAs	153
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED



JOURNAL OF ELECTRONIC MATERIALS

JEM is published monthly by TMS, 420 Commonwealth Drive, Warrendale, Pennsylvania 15086, and the Institute of Electrical and Electronics Engineers (IEEE), 345 East 47th Street, New York 10017-2394

Subscription rates for Volume 22, 1993 (12 issues):
- Individual subscription in the United States: $75 (outside of the United States: $93)
- Institutional subscriber in the United States: $185 (outside of the United States: $203)

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Second-class postage paid at Warrendale, Pennsylvania, and additional mailing offices. Postmaster: send address changes to TMS, 420 Commonwealth Drive, Warrendale, Pennsylvania 15086. USPS 047-350.

Copy Editor: Judy Parise, TMS • Graphic Artist: Sherry Walter, TMS • Printer and Binder: Edwards Brothers, Ann Arbor, MI 48103
Printed in the United States • 0361-5235/1993-93/TMS

Journal of Electronic Materials, Vol. 22, No. 12, 1993

Foreword

In 1988, it was discovered by Frank Smith, Bob Calawa, and coworkers that molecular beam epitaxial GaAs grown at the extremely low temperature of 200°C (normal growth temperatures: 580–600°C) was excellent material with very unusual properties, and solved a long-standing problem associated with GaAs integrated circuit technology. Since then, there has been a flurry of activity in this area, resulting in perhaps 300–400 papers being published up to date, not only on GaAs but on other III-V binaries and ternaries as well. To summarize the present state of the art, a two-day symposium, Low Temperature Grown and Highly Nonstoichiometric GaAs and Related Materials, was held at the Spring Meeting of the Materials Research Society (MRS), San Francisco, April 12–13, 1993. The symposium was organized by Gerald Witt, U.S. Air Force Office of Scientific Research; David Look, Wright State University; Michael Melloch, Purdue University; and Frank Smith, MIT/Lincoln Laboratory, and was sponsored by the U.S. Air Force Office of Scientific Research. Forty-one papers were presented in five sessions, as follows:

Session D2–1: **Growth Issues,** including growth of As and P-based compounds, annealing effects, and characterization by scanning tunneling microscopy (STM), real-time ellipsometry, and positron annihilation.

Session D2–2: **Processing and Characterization,** including point-defect and precipitate formations and their characterization by electrical, optical, magnetic resonance, and STM techniques.

Session D2–3: **Optical and Optoelectronic Properties,** including the materials GaAs, InGaAs, and InGaP, and their responses to light stimulation, explained by various models.

Session D2–4: **InP and Related Ternary Materials,** including the materials InP, InGaAs, InAlAs, and ordered InGaAs/InAlAs layers, characterized by optically detected magnetic resonance, electrical measurements, tunneling electron microscopy, and photoreflectance.

Session D2–5: **Applications of Nonstoichimetric Materials,** including power MESFET design, phase noise measurements, coherent microwave generation, excitonic electro-optic observations, and GaAs on Si device applications.

Included in this special issue of the *Journal of Electronic Materials* is a representative subset of this work, with each of the 31 papers herein receiving critical reviews. It is hoped that these papers will provide a good starting point for those entering the field as well as a synopsis of our current understanding for the more seasoned workers. We wish to thank T.C. Harman, editor of the *Journal of Electronic Materials*, and the editorial board for making this journal available to us as a forum for our symposium, and to our co-organizer, Gerald Witt, along with the MRS staff for their excellent help in keeping track of the papers, both before and after the MRS meeting.

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A Comparison of As and P-Based Semiconductors Grown at Low Temperatures by MBE and GSMBE

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Materials grown at low temperatures by molecular beam epitaxy techniques have exhibited high resistivity after annealing, and sub-picosecond carrier recombination times. Depending on growth parameters, the nonstoichiometric material can contain a high density of group V antisite defects and precipitates of group V and group III atoms. It is well known that a high density of As antisites and As precipitates formed in GaAs contribute to the high resistance. InP grown at low temperatures was also observed to contain precipitates consisting of both P and In. The latter material however does not exhibit the high resistivity of GaAs. This behavior may be due to the presence of indium or P antisite defects.

Key words: Antisite, gas-source MBE, LT GaAs, LT InP

INTRODUCTION

The discovery that GaAs metal-semiconductor field effect transistor (MESFET) buffer layers grown by molecular beam epitaxy (MBE) at temperatures around 200°C eliminated sidegating and backgating,[1] spurred considerable research in materials properties and new applications of the material. Low temperature layers have been used in MESFETs[2,3] to increase gate-to-drain breakdown voltage; heterojunction field effect transistors (HFETs)[4–6] to improve output characteristics and reduce noise; semiconductor lasers[7,8] to reduce threshold current density and improve current blocking; and in photoconductive switches[9–11] to obtain subpicosecond response. A recent review of device applications is given by Smith.[12]

This paper will concentrate on the structural and electrical properties of arsenic and phosphorus-based III-V semiconductors grown at low temperatures in attempts to provide information on the underlying mechanisms. To date GaAs, AlGaAs, InGaAs, InAlAs, InGaAlAs, InP, GaP, and InGaP have been grown at low temperatures by MBE. The resistivity in the various undoped material systems varies by approximately ten orders of magnitude ($10^{-2} < \rho < 10^{8}$ Ωcm) and is controlled by high densities of point defects and the presence of group V precipitates.

(Received April 12, 1993)

EXPERIMENTAL WORK ON LOW TEMPERATURE MBE III-V COMPOUNDS

GaAs

Low temperature GaAs (LT GaAs) is semi-insulating and exhibits resistivities on the order of 10^{6} Ωcm after annealing at approximately 600°C for 10 min. At growth temperatures of 150 to 300°C, approximately 0.5% to 2% excess arsenic (using either As_4 or As_2 as sources) is incorporated into the crystal. The crystal is thus nonstoichiometric in contrast to GaAs grown at "normal" (~580°C) growth temperatures. The epitaxial layer is thus strained since the lattice constant is increased above that of the GaAs substrate by $\Delta a/a \sim 10^{-3}$. Consequently, there is a critical thickness above which dislocations begin to form and render the epitaxial layer polycrystalline. An example of a film that is thicker than the critical thickness is shown in Fig. 1. Arsenic incorporation is very growth temperature and V/III ratio dependent and consequently so is the amount of strain. The latter statement implies a major reason that there are

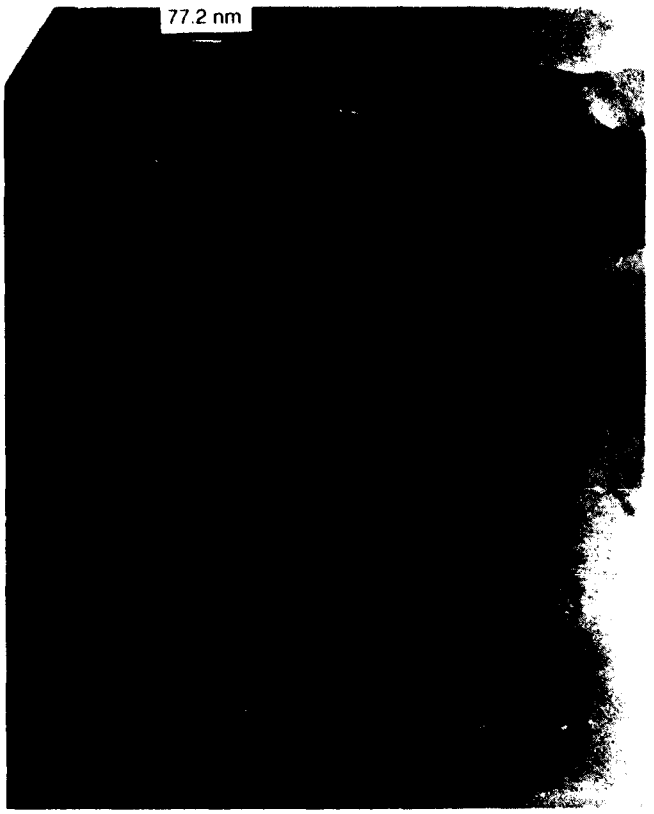


Fig. 1. Transmission electron microscopy cross section of a GaAs LT layer grown by gas-source MBE. This sample was grown at a high V/III ratio and is thicker than the critical thickness for dislocation formation. Because dislocation motion is very slow at the growth temperature, a polycrystalline layer is formed at the top which relieves the strain energy. Arsenic precipitates can be observed throughout the layer.

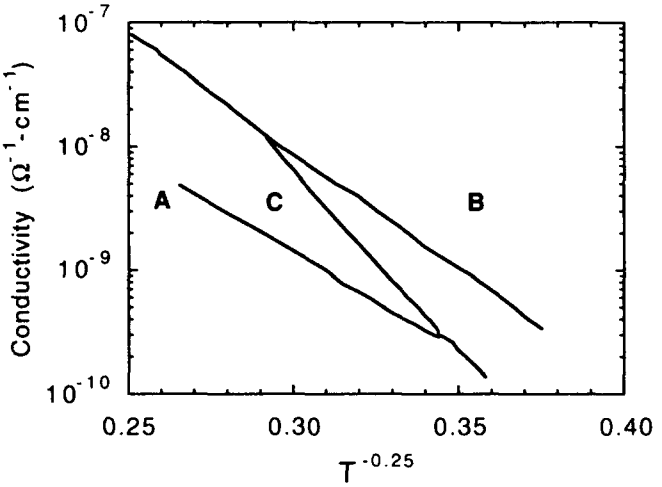


Fig. 2. Conductivity vs $T^{-0.25}$ for annealed LT GaAs grown under three different conditions. (A)–As4, V/III = 20, T_s = 24°C, (B)–As_2, V/III = 35, T_s = 245°C, and (C)–As_2, V/III = 52, T_s = 310°C. After Ref. 18.

considerable discrepancies in results from different groups. In MBE, the substrate temperature (T_s) is difficult to measure accurately at approximately 200°C because the primary thermometer is a thermocouple whose degree of thermal contact with the substrate varies significantly among different MBE reactors. Because of uncertainties in T_s, V/III ratios inferred by

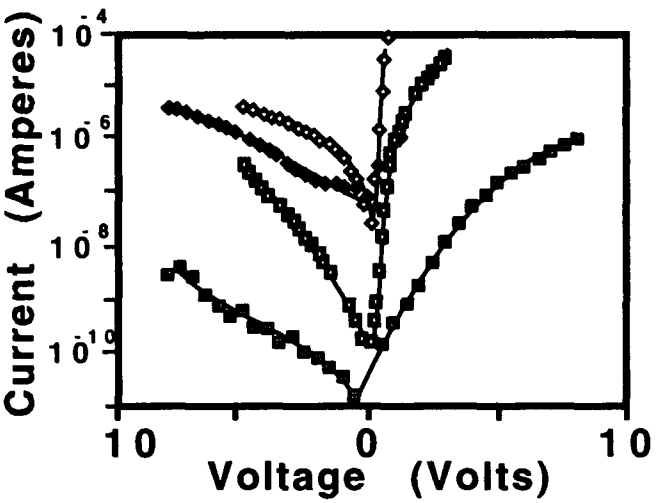


Fig. 3. I-V curves for 2000Å thick layers of undoped GaAs and AlGaAs. ¬ LGT AlGaAs, 20 min anneal, ◆ LGT GaAs, 20 min anneal, ● AlGaAs – T_{growth} = 636°C, ■ GaAs, T_{growth} = 635°C. Device area is 4.4×10^{-3} cm^2. Diodes consisting of LT and "normal" T material are shown. After Ref. 24.

beam equivalent pressure (BEP) ratios or group V induced oscillations also produce an ambiguity when comparing materials grown under apparently the same conditions.

As-grown LT GaAs has a resistivity on the order of 10^2 Ωcm because there is considerable interstitial arsenic (As_i) as well as traps associated with antisites (As_{Ga}), Ga vacancies (V_{Ga}), and complexes. Upon annealing, As diffuses toward regions of lower concentration (the free surface and the substrate) and also forms crystalline precipitates which range from 20 to 100Å.[13,14] Thus, after annealing, there are approximately mid-$10^{17}$$cm^{-3}$ As precipitates embedded in GaAs which has a point defect density on the order of 10^{18} cm^{-3}.[15,16] Arsenic precipitates can also be seen in Fig. 1. Their density is approximately constant throughout the layer.

Electrical and optical properties of LT GaAs grown under optimum conditions with dimeric and tetrameric As sources were found to be very similar.[17,18] When using As_2 (in GSMBE), growth of high resistivity LT GaAs was seen to occur in a narrower temperature and V/III ratio range than when As_4 was used.[19] The fact that larger quantities of arsenic are incorporated in GSMBE layers grown with As_2 can be attributed to the longer residence time of As_2 compared to As_4 during growth. As_2 associates to form As_4 before desorption which might explain the similarity of electrical and optical properties between MBE and GSMBE layers. Arsenic incorporation into the LTB layer is most efficient at 255°C. When the growth temperature is brought closer to 325°C, where As_2 is no longer believed to undergo an association reaction, this effect is less pronounced. Thus, at higher temperatures, As_2 desorption occurs with a much smaller time constant. The peak of this association reaction is at around 210°C and thus lower temperatures are less suitable for GSMBE growth.

Variable range hopping can be observed in a limited

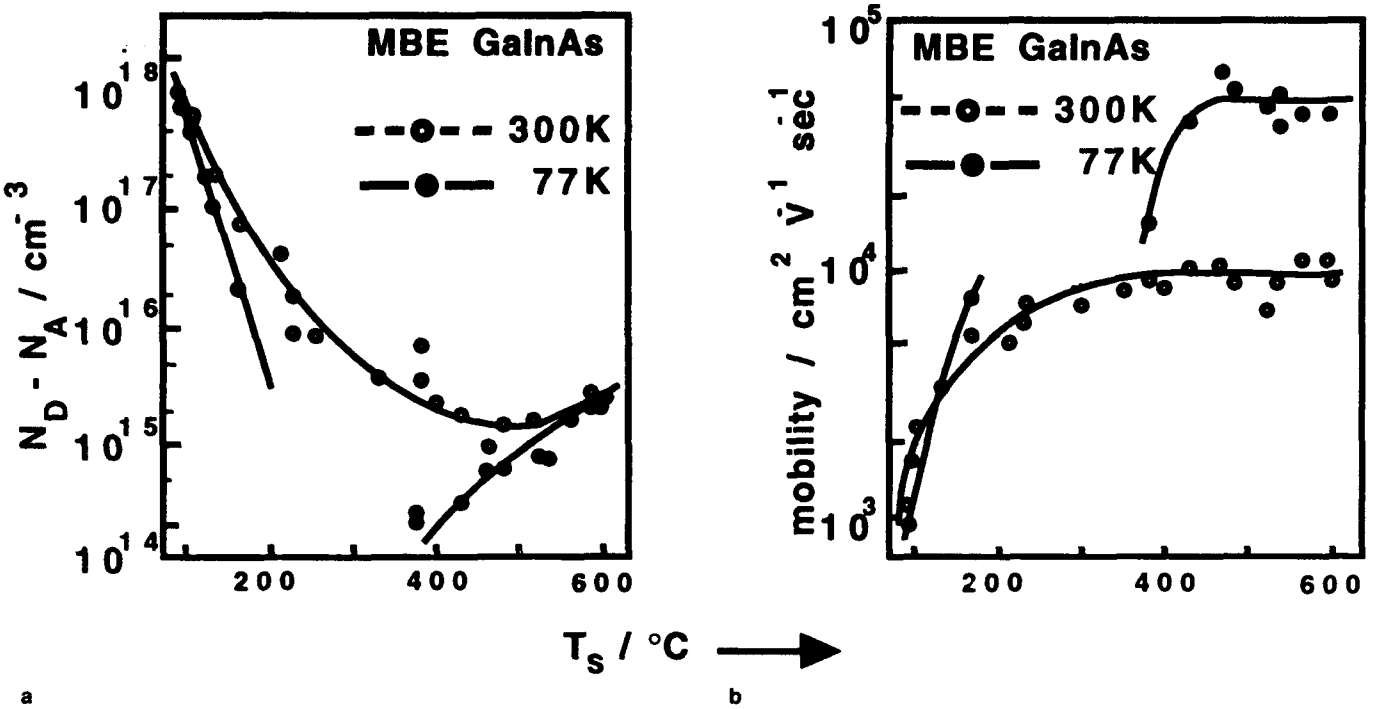


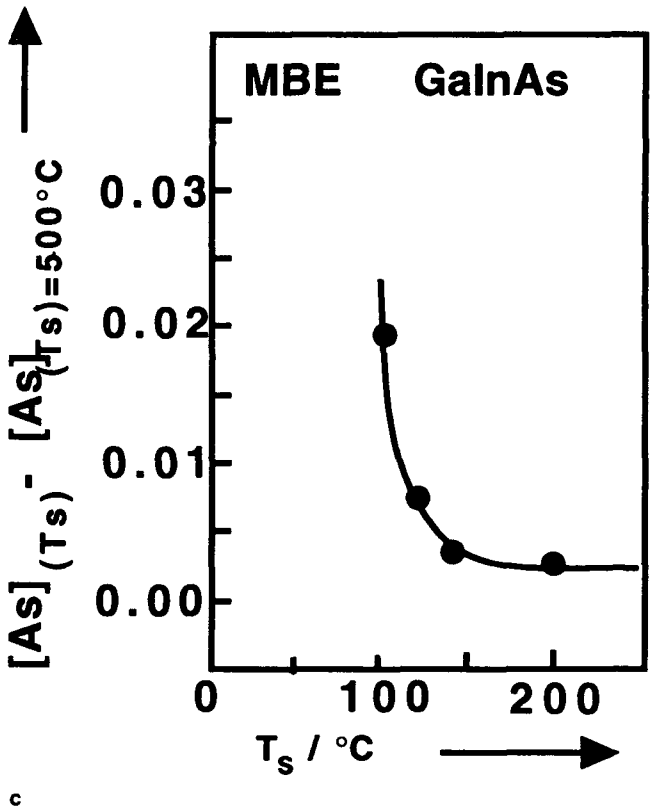
Fig. 4. Properties of LT InGaAs a) carrier concentration, b) mobility, and c) excess incorporated As dependence on substrate temperature. After Ref. 26.

temperature range by plotting the conductivity vs $T^{-0.25}$ on a logarithmic plot as shown in Fig. 2. The linear region which characterizes such a conduction mechanism is found below room temperature in LT GaAs.[18,20] Above room temperature, the sheet conductivity increases above that of the semi-insulating substrate. There are two main theories on the origin of such a high resistivity and the observation of hopping conductivity below room temperature. The first states that the well-characterized, high density of As_{Ga} and V_{Ga} related deep donors and acceptors is sufficient to compensate any carriers present in the material.[20,21] The second states that metallic As precipitates act as spherical Schottky barriers[22] whose overlapping space charge regions deplete the material of carriers and produce the observed high resistivities. It was calculated that semi-insulating behavior should occur in $n = 5 \times 10^{17}$ cm^{-3} doped material containing 30Å diameter precipitates for precipitate densities above 2×10^{16} cm^{-3}. This number varies as a function of precipitate size and shallow impurity concentration. At this time, there is evidence supporting both theories.

AlGaAs

Low temperature AlAs has been shown to be a barrier for As precipitates diffusing from LT GaAs.[4] It was proposed that[23] diffusion from the AlAs is not due to a gradient of As across the heterojunction interface but that Al increases the chemical potential of As causing it to diffuse away from the AlAs. In AlGaAs/GaAs superlattices precipitate accumulation and depletion zones were observed which were caused by diffusion of As from AlGaAs into GaAs. For samples grown at 250°C and annealed at 600°C, the same density and size of precipitates was found in both GaAs and AlGaAs layers but the AlGaAs had a 250Å region depleted of precipitates.

Low temperature AlGaAs grown at 250°C and annealed at 600° for 20 min exhibited very high resistiv-



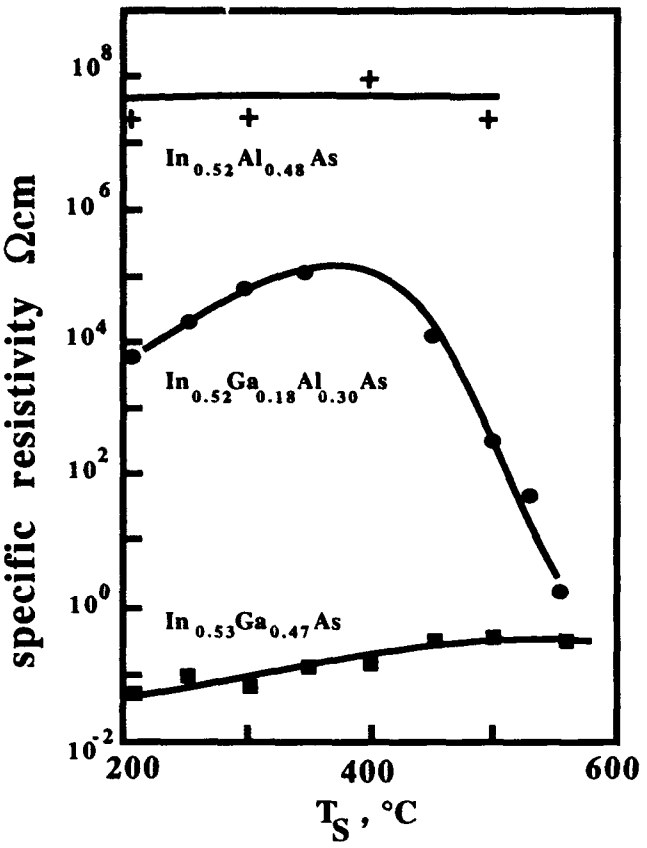


Fig. 5. Specific resistivity of MBE InGaAlAs vs T_s. + $In_{0.52}Al_{0.48}As$; • $In_{0.52}Ga_{0.18}Al_{0.30}As$; ■ $In_{0.53}Ga_{0.47}As$. After Ref. 31.

ity (~10^{11} Ωcm) when used in the 2000Å thick gate of an MIS structure.[24] The mobility was between 0.1 and 10 cm^2/Vs. A hole trap 0.14 eV from the valence band was detected but did not affect the gate I-V characteristics (Fig. 3). A strong pinning of the Fermi level at the LT AlGaAs surface was inferred from capacitance-voltage measurements.

AlGaAs doped with Si and Sn (to 3×10^{18} cm^{-3}) was grown at 350°C and annealed at 850°C for approximately 30 s.[25] Doping with Sn at these low temperatures was performed in efforts to reduce the Sn surface segregation to a few monolayers as compared to 1 μm at the conventional growth temperature of 620°C. After annealing, full activation of the dopant was attained for growth temperatures above 450°C. At 350°C, the activation decreased to one third of the value obtained under normal growth temperatures of 620°C indicating that there was a high level of compensating acceptors present.

InGaAs/InP

A study of electrical properties vs growth temperature (100°C < T_s < 600°C) of InGaAs lattice matched to InP was reported.[26] A BEP of V/III = 15 was used for temperatures below 500°C and higher above 500°C. Epitaxial layers were seen to be single crystalline down to T_s = 125°C where the As content of the layer increased to 0.5% off stoichiometry. At 100°C, the As incorporation produced InGaAs with 2% excess As and poor surface morphology, resulting most likely from the critical thickness being exceeded. Figure 4 shows the free carrier concentration and mobility vs growth temperature. For temperatures below 200°C, the electron concentration increases sharply to ~10^{18} cm^{-3} while the mobility drops from ~10^4 cm^2/Vs to 10^3 cm^2/Vs. This behavior was attributed to a 32 meV donor level which increases in concentration at low growth temperatures. The 77K mobility exhibits an anomalous behavior for growth temperatures around T_s = 300°C. The samples became highly resistive as the growth temperature was decreased and then became conductive again at low growth temperatures. A significant result is that the resistivity did not change after a 500°C anneal for one hour. This suggests that the resistivity is not dominated by As precipitates which are formed upon annealing. Künzel et al.[26] also suggest that the cause of the high conductivity may be a group III vacancy related defect. As will be seen later, there is some indication that the increased conductivity may be related to excess indium in the lattice.

Increased indium incorporation was observed at low growth temperatures in InGaAs/GaAs quantum wells.[27,28] Above 550°C, the indium composition was x = 0.3 while at 460°C, it increased to x = 0.45. Strong photoluminescence (PL) was observed from all of the wells throughout the aforementioned composition range. No electrical measurements were performed. A significant development was that the critical thickness for pseudomorphic growth was increased by a factor of seven for x<0.45.

InAlAs/InP

InAlAs lattice matched to InP was grown between 100°C < T_s < 250°C and produced material with resistivity 2×10^6 Ωcm < ρ < 2×10^7 Ωcm.[29] InAlAs grown at 500°C had ρ = 1×10^7 Ωcm which was equivalent to material grown at 250°C. This value of resistivity agreed with other measurements on InAlAs.[30] Breakdown voltages were on the order of 15V. All samples were annealed at 500°C for the duration of a 3000Å InGaAs cap layer growth. One sample (T_s = 100°C) was further annealed at 550°C for 1 h which exhibited a resistivity of ρ = 1×10^8 Ωcm. The PL decreases by a factor of 10^4 from T_s = 550 to 100°C. At T_s = 100°C, there was no measurable luminescence and x-ray showed that the sample was polycrystalline with excess As greater than 3.0%. Excess As of 1.4% was seen in the 100–150°C range, 0.4% in the 150–200°C range and 0.0% in the 200–250°C range. Variations in the As_4 overpressure had no significant effect on the resistivity.

An investigation of the structural properties of LT InAlAs was performed by Claverie et al.[31] Samples were grown at temperatures between 150 and 450°C with a V/III ratio of 20. They all exhibited high resistivity after an in situ anneal at 500°C for 10 min. Arsenic incorporation increased with decreasing temperature down to 200°C. At 150°C, a large density of pyramidal defects was formed and attributed to ex-

cess As. A reference sample was grown at 450°C and annealed at 500°C for 10 min. InAlAs grains (~50 nm in size) growing along the <100> and <011> directions were observed. Each grain was faulted in the {111} planes. At 200°C, an anomalously reduced As incorporation was seen and attributed to ordering of the ternary into small domains along the {111} planes. Various forms of As precipitates were also observed. The pyramidal defects observed are similar to those found in LT GaAs and due to excess As.

InGaAlAs/InP

Very little work has been done to date on quaternary growth by MBE at low temperatures. In one report, growth of InGaAlP was performed as a function of substrate temperature.[32] Figure 5 is a graph of resistivity vs T_s for InAlAs, InGaAlAs, and InGaAs. The maximum in resistivity (10^5 Ωcm) for InGaAlAs occurs for T_s = 400°C with a V/III BEP of approximately 15. InGaAs was seen to be conductive for all growth temperatures and InAlAs resistive for all growth temperatures as observed in the previous sections. For InGaAlAs, the gradual resistivity decrease below 400°C is reported to be a result of emission of free electrons from traps of high concentration. Above 400°C, the resistivity decreases rapidly as the trap density decreases for increasing T_s. The latter behavior is similar to that of InGaAs observed by Künzel et al.[30]

GaP/GaP

Work on the phosphides has only recently begun. The technological motivation for studying the phosphides is to obtain high resistivity and fast carrier recombination in these materials. The other reason is to see whether high resistivity can be obtained without As precipitates or As related deep centers such as As_{Ga} and As_i.

GaP was grown at 200°C using solid Ga and cracked PH_3[33] with a V/III ~40 as measured by quadrupole mass spectrometry. Below 160°C, the GaP was polycrystalline but at ~190°C the layers were single crystals. The dark resistivity was too high to be measured on a high impedance Hall effect system, but under intense illumination measured to be on the order of 10^6 Ωcm. High temp GaP had low resistivity while LT GaP was highly resistive as-grown and thus did not require annealing. The lack of P precipitates implies that the high resistivity is due solely to compensating centers in the GaP. No significant strain reduction is seen (by DCXRD) after annealing at 700°C for 1 h. This is different than in GaAs where the strain is reduced after annealing. A brief mention of preliminary GaAsP TEM results shows some "incoherent" As precipitates[33] which segregate to dislocation lines and microtwin boundaries.

InGaP/GaAs

Preliminary results on LT InGaP have been obtained by El-Masry and Bedair.[34] It is possible to grow

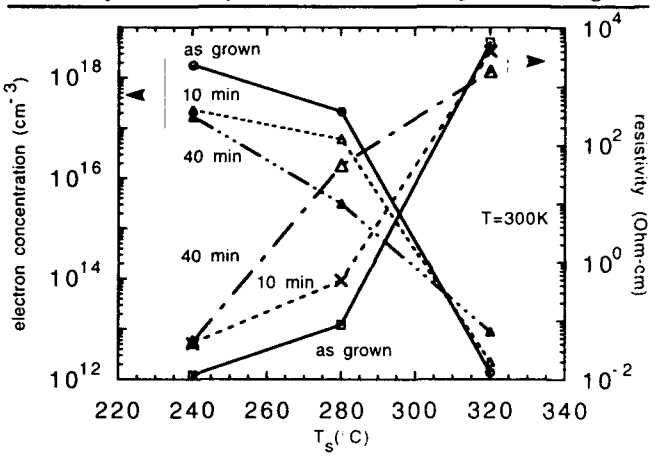


Fig. 6. Carrier concentration and resistivity of three LT InP samples grown at different substrate temperatures. Also shown are curves after 600°C anneals of 10 and 40 min. After Ref. 35.

Table I. Summary of Experimental Work on III-V As and P-Based Compounds Grown at Low Temperatures by MBE

Compound	ρ (Ωcm)	μ (cm²/Vs)	T_s (°C)	Anneal (°C)	Anneal Time	E_A (eV)	Ref.
AlGaAs	10^{11}	0.1–10	250	600	20 min	0.14 (hole)	24
GaP/GaP	$>10^{10}$ 10^6 (illum)	—	190	700	60 min	—	33
GaP/GaP	10^8	—	190	—	—	—	33
InGaP/GaAs	$>10^9$	—	200	600	60 min	0.8	34
InGaP/GaAs	10^6	120	200	—	—	0.48	34
GaAs	10^7	—	230	600	10 min	0.8	—
InAlAs/InP	2×10^7	—	250	500	—	—	29
InAlAs/InP	10^8	—	100	500	60 min	—	29
InGaAlAs	10^5	—	400	—	—	—	32
InGaAs/InP	~10^4	10^3	100	500	no effect	0.032	26
InGaAs/InP	~10^4	10^4	600	500	no effect	0.032	26
InP	10^4	—	320	600	10 min	0.61	35
InP	10^{-2}	—	240	600	10 min	—	35

InGaP/GaAs between 150 and 250°C. For T_s ~200°C, the material is n-type with $\rho \sim 9 \times 10^5 \Omega$cm and $\mu \sim 120$ cm²/Vs and has a donor activation of 0.48eV After annealing at 600°C for 1 h, ρ exceeds 10^9 Ωcm and has an activation energy of $E_A \approx 0.8$eV. Low temperature InGaP has slightly larger lattice constant than InGaP grown at normal temperatures (due to the excess P) which decreases upon annealing. Low indium composition regions were found (single crystal InGaP regions with graded composition) by TEM.

InP/InP

Low temperature InP was found to have a much lower resistivity than GaP and InGaP for growth temperatures between 240 and 320°C.[35] The electron concentration in the 0.3 μm thick samples decreases from low 10^{18} cm^{-3} at T_s = 240°C to 1×10^{12} cm^{-3} (depleted) at T_s = 320°C while the resistivity changes from 10^{-2} Ω-cm to almost 10^4 Ω-cm over the same temperature range (see Fig. 6). The electron mobility was seen to increase from 300 to 400 cm²/Vs over this growth temperature range.

In the series grown at T_s = 240°C with varying V/III ratio, the mobility was seen to increase as a function of decreasing V/III ratio from 200 to 675 cm²/Vs (compared with the SI InP substrate mobility of ~2900 cm²/Vs). There is a corresponding change in resistivity from 0.19 to 0.04 Ω-cm. Temperature dependent conductivity showed a thermal activation energy of 0.61 eV in the samples grown at 320°C. Limited hopping conduction occurred for this substrate temperature. In samples grown at lower temperatures, the conductivity was high and temperature regions of hopping conductivity disappeared.

Throughout the layer, a density of approximatelv 1 $\times 10^{10}$ precipitates per square centimeter ranging in size from 100 to 500Å was observed. Precipitate structures were observed and analyzed by electron probe energy dispersive x-ray nanospectroscopy. One type was and found to be crystalline and phosphorus-rich, similar to As precipitates found in LT GaAs. An excess P content of 3% was also observed in the epitaxial layer which produced an absolute lattice parameter variation of 0.09 nm ± 0.01 nm. Another report[38] showed that there was 7% excess phosphorus in the epitaxial layer which rendered it polycrystalline as the critical thickness was exceeded. This material had a resistivity of <0.1 Ωcm.

DISCUSSION

Table I summarizes the electrical data on the P and As-based III-V materials in order to illustrate the spread in properties observed to date on LT MBE grown materials. The materials are ordered from highest to lowest resistivity. Also shown are the carrier mobility, growth temperature, main compensating trap activation energy (E_A) and annealing process where available. Some resistivities were too high to be measured unless the sample was exposed to intense illumnination.

Some observations and general trends can be gleaned from the work done to date. Aluminum containing compounds tend to have higher resistivity than those with indium. The exact reason for this is not well known, but it has been suggested that indium may act a donor and reduce the resistivity. In InP, the donor may also be the antisite P_{In} which moves into the band gap from the conduction band. Another reason may be that introduction of indium reduces the material's band gap and thus increases the free carrier concentration at a particular temperature. Materials grown using dimeric and terameric arsenic have approximately the same conductivity behavior if grown in appropriate temperature and V/III ratio regimes. Based on GaAs growth kinetics, LT InP layers grown using P_2 and P_4 are expected to have similar properties. The effect of precipitates is still in question as InGaP is highly resistive without precipitates. However, a direct comparison of GaAs and InP is not straightforward because the conductivity depends on the band structure of the nonstoichiometric binaries which are different for the two. Hopping conduction behavior is not as pronounced in materials with low resistivity, even if the material has a high density of point defects and precipitates (e.g. InP).

While the sparse detailed knowledge of conduction mechanisms in LT III-Vs has not prevented their success in device applications, clearly there is still a considerable amount of research to be performed toward understanding the materials. The band structure, density, and nature of the point defects and their interactions must be understood to determine whether they compensate or provide carriers. Nonstoichiometric conditions further complicate knowledge of defects and band structure. The growth conditions (especially growth temperature) must be understood to a higher degree than they presently are so more accurate comparisons among different laboratories can be made. The presence of dislocated or polycrystalline layers needs to be identified before electrical and optical measurements can be effectively interpreted.

ACKNOWLEDGMENTS

The authors would like to thank S.M. Bedair for many helpful discussions and early dissemination of his work. We would also like to thank Z. Liliental-Weber for transmission electron microscopy of the gas-source molecular beam epitaxial GaAs layers. This work was supported by the U.S. Army Research Office and Air Force Office of Scientific Research.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

A Scanning Tunneling Microscopy Study of Low-Temperature Grown GaAs

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Scanning tunneling microscopy (STM) has been used to investigate the effect of low-temperature (LT) growth of GaAs by molecular beam epitaxy on the morphology of the resulting surface. We present STM images of a GaAs(001) surface that was grown at ~300°C and subsequently annealed at 600°C and show that there is a recovery of the (2 × 4) reconstruction. We also report images of a surface grown on top of a buried LT GaAs layer and show that the LT layer has little effect on the resulting surface morphology. In addition, scanning tunneling spectroscopy spectra are presented which demonstrate that the current-voltage characteristics of annealed and unannealed LT grown GaAs are significantly different.

Key words: Low-temperature grown GaAs, MBE, scanning tunneling microscopy

INTRODUCTION

GaAs samples grown by molecular beam epitaxy (MBE) at low (~300°C) temperatures and subsequently annealed at higher temperatures are of significant technological importance due to their high resistivity. This resistive property makes low-temperature GaAs potentially useful in devices as a way to eliminate common device problems such as backgating in GaAs metal-semiconductor field-effect transistors (MESFETs).[1]

There are two proposed mechanisms by which this material becomes semi-insulating (SI). Look et al.[2,3] have proposed that the material is semi-insulating similar to conventional SI GaAs, in which deep donors and acceptors pin the Fermi level midgap. The point defect model explains observed high conductivity in unannealed material, in which the high defect concentration leads to hopping conduction. Warren et al.[4] have proposed that the high resistivity of the annealed material arises from Schottky-barrier-controlled internal pinning on metallic arsenic precipitates that are formed during the anneal.[5] Recently, Vaterlaus et al.[6] were able to image As precipitates by using cross sectional scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS). They found a slight increase in the density of states within the band gap when tunneling on an As precipitate, suggesting that it is the precipitates that pin the Fermi level.

The detailed morphology of these surfaces, however, has not been as intensely studied. Good morphology is important if low temperature (LT) GaAs is to be used for device applications. We have known from our reflection high energy electron diffraction (RHEED) patterns that, after annealing at about 600°C, this material recovers the (2 × 4) RHEED pattern that is characteristic of GaAs (001) surfaces grown by molecular beam epitaxy at standard growth temperatures (~600°C). Melloch et al.[7] imaged low-

(Received April 12, 1993)

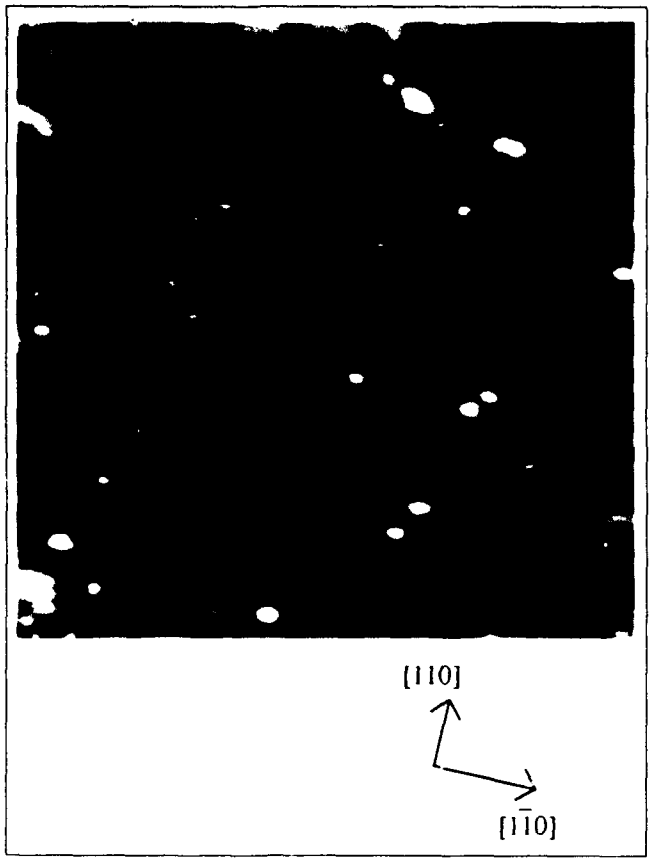

Fig. 1. A 50 × 50 nm² image is shown for an MBE-grown GaAs(001)-(2 × 4) surface resulting from growth at 300 C and subsequent anneal at 600 C. The tunneling current is 0.1 nA at a sample bias of −3 V.

temperature GaAs and AlGaAs layers in cross section using transmission electron microscopy. Their results show that the interfaces are of reasonable quality.

In this paper, we present the first STM images of the surface of LT GaAs (001). We have successfully imaged the reconstructed surface of GaAs grown at low temperatures and subsequently annealed under arsenic pressure. We show this surface to be of surprisingly good quality. We have also imaged surfaces that have been grown on top of a LT layer and show that the quality of these surfaces is not affected by the presence of the buried LT layer. In addition, some STS measurements are presented.

EXPERIMENTAL PROCEDURES

Measurements were performed in an ultrahigh vacuum (UHV) chamber with a base pressure of 5 × 10⁻¹⁰ Torr. The scanning tunneling microscopy head is equipped with Pt/Ir tips that are cleaned in situ by electron bombardment to give atomic resolution.[8] An ion-pumped interlock shuttle allows UHV transfer of samples from a Varian Gen II molecular beam epitaxy system to the STM chamber.[9] The transfer procedure is concluded in less than one hour and pressure during transport is maintained below 1 × 10⁻⁹ Torr. The GaAs substrates are indium bonded to small molybdenum sample holders to provide compatibility both to standard three-inch MBE sample holders and to the STM.

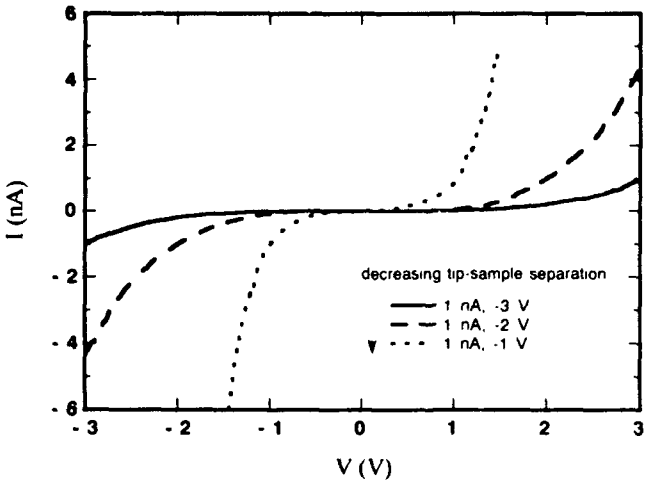

Fig. 2. Current vs sample voltage for LTU samples with various tip-sample separations determined by a set point current of 1 nA at sample voltages of −3 V (solid line), −2 V (dashed line), and −1 V (dotted line). See text for detail.

All growths began with thermal desorption of the native oxide at a substrate temperature of 630°C. For the samples referred to hereafter as low-temperature unannealed (LTU) and low-temperature annealed (LTA), an n-type GaAs layer of dopant concentration 1×10^{18} cm^{-3} was grown at a substrate temperature of 590°C, measured with an optical pyrometer, and a growth rate of 1 μm/h. Then, the growth was interrupted, the substrate temperature was ramped to ~300°C, and a 200Å thick layer of undoped GaAs was grown. During LT deposition, a (1 × 1) RHEED pattern was observed. After this growth, the LTA samples were annealed for 10 min at 600°C under an arsenic pressure of 8×10^{-6} Torr. After the anneal, the samples showed a (2×4) RHEED pattern. The surface was then quenched to room temperature by decreasing both the substrate temperature and the As background pressure, and the samples were transferred into the STM chamber.

For the samples referred to as low-temperature well (LTW) and conventional-temperature well (CTW), an n-type GaAs layer of dopant concentration 2×10^{18} cm^{-3} was grown at a substrate temperature of 590°C and a growth rate of 1 μm/h. Then, a 40Å thick layer of undoped AlAs was grown followed by the growth of 260Å of undoped GaAs. For the CTW samples, this growth took place at ~600°C, whereas for the LTW samples, this growth took place at ~300°C. Then a 25Å thick layer of AlAs was grown. At this point, the low-temperature well samples were annealed at 600°C for 10 min. Finally, a 25Å cap of undoped GaAs was grown, and the samples were transferred into the STM chamber for analysis. A test sample was grown, using the same sample mounting technique as used for the STM measurements, in order to calibrate the measured growth temperature. The presence of As precipitates (~1% by volume) under our growth conditions was confirmed by transmission electron microscopy.

RESULTS AND DISCUSSION

We were unable to obtain atom-resolved images of the LTU surfaces, and hence, the nature of the observed (1 × 1) RHEED pattern requires further investigation. An STM image obtained on a LTA sample is shown in the 50 × 50 nm² area of Fig. 1. Rows of (2 × 4) reconstruction, which extend ~8 nm, on the average, along the [1$\bar{1}$0] direction, can be seen. There are a large number of holes (through which the second layer is sometimes visible) in the rows as well as other defects such as kinks, indicating that the topographic order of these surfaces is not as good as the order of GaAs(001)-(2 × 4) surfaces grown at standard temperatures.[10,11] Still, these surfaces display a high degree of order.

Scanning tunneling spectroscopy was used to obtain current-voltage (I-V) spectra on the LTU samples. Scanning tunneling spectroscopy measurements are taken by opening the feedback loop, which controls the tip-sample distance, and measuring the tunneling current as a function of sample voltage.[8] By demanding a particular tunneling current at a given sample bias prior to opening the feedback loop, I-V spectra at various tip-sample separations can be obtained. Some representative I-V curves are shown in Fig. 2 for various tunneling set points. The smaller the sample bias at the set point, the smaller the tip-sample separation. A detailed examination of these I-V curves, to be presented elsewhere, reveals a large number of states in the band gap of this material. This result is consistent with the assertion by Look et al.[2] that the excess arsenic introduces mid-gap states in the low-temperature grown material. Additionally, it can be shown that the shape of the I-V curve does not change as a function of tip-sample separation, implying that no significant tip-induced band-bending occurs for this material.[8]

We were also able to obtain STS spectra on the LTA samples. Comparison of the spectroscopy of the LTA and the LTU (Fig. 3) shows a dramatic difference in the I-V characteristics of the two materials. The spectra typically obtained on GaAs(001)-(2 × 4) have been recovered for the LTA samples.[10] We do not expect As precipitates to be present in the LTA layers. Ibbetson et al.[12] found that, under similar anneal conditions, the diffusion length for excess As related defects is ~1500Å, much greater than the 200Å thickness of the layers. This leads us to believe that all of the As precipitates were annealed out of the LTA samples.

We have also examined the effect of buried LT layers on the resulting morphology (Fig. 4). We chose for our structure a low-temperature grown layer sandwiched between two AlAs barriers. After the second AlAs layer was deposited, the low-temperature layer was annealed at 600°C, and the samples were capped with 25Å of GaAs. AlAs barriers have been found to prevent the diffusion of the As precipitates during anneal, and hence, we expect this material to contain As precipitates.[13] We compared this surface with the surface of the CTW sample (not shown), which was an identical structure with the low-temperature and subsequently annealed GaAs layer replaced by simply a layer of GaAs grown at conventional temperatures. The two surfaces are identical, indicating that the buried LT layer did not affect the quality of the surface. No effect of the precipitates is

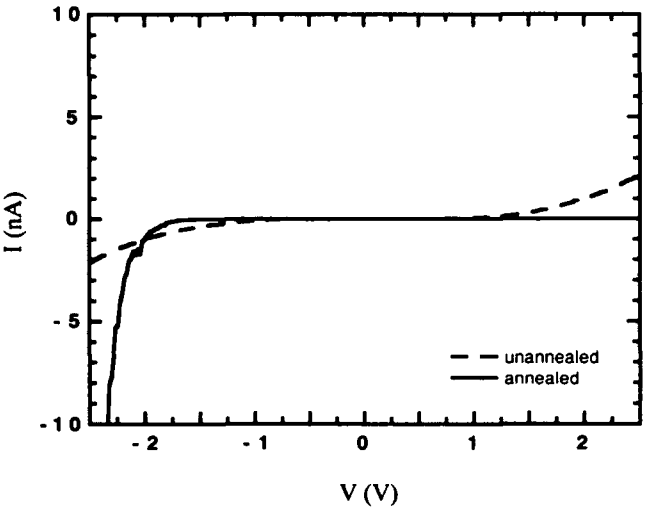

Fig. 3. A comparison of I-V curves taken on LTU and LTA samples at a set point of −2 V, 1 nA. See text for detail.

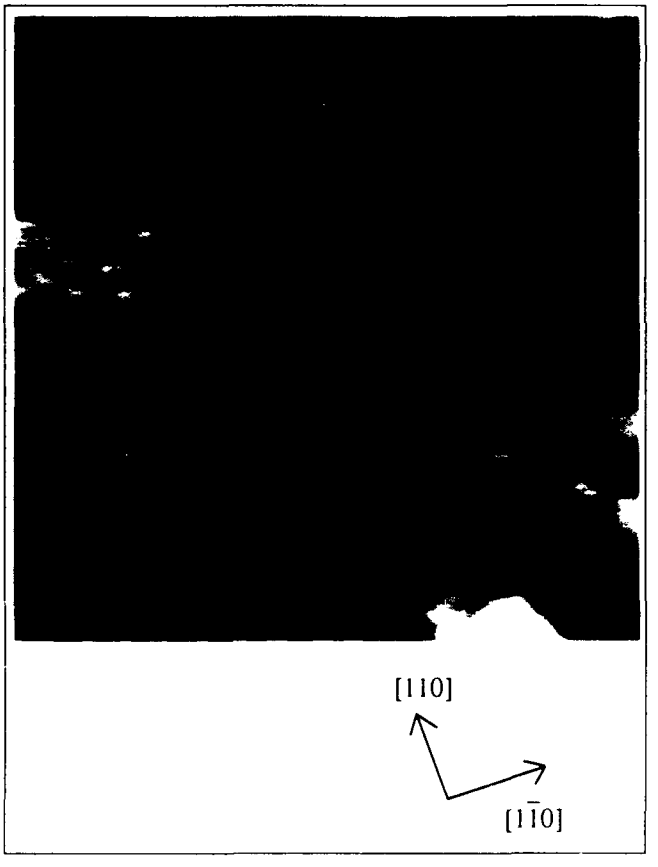

Fig. 4. A 69 × 69 nm² image is shown for a GaAs(001)-(2 × 4) surface grown with a buried low-temperature layer. A step and some surface adatoms are also visible. The tunneling current is 0.2 nA at a sample bias of −2.4 V.

observed in the STM images for the LTW surface. It is possible that the precipitates were not close enough to the surface to affect the surface electronic structure, but this question needs to be studied further. We have also studied I-V spectra of these samples, the results of which will be presented elsewhere.

CONCLUSIONS

In summary, we have shown that low-temperature grown and subsequently annealed GaAs(001) produces surfaces that are of good quality when imaged with STM. We have also shown that it is possible to grow high-quality materials on top of LT GaAs layers.

ACKNOWLEDGMENTS

We gratefully acknowledge financial support by the U.S. Air Force Office of Scientific Research, and by QUEST, a National Science Foundation Science and Technology Center for Quantized Electronic Structures (grant no. DMR 91-20007). One of us (WHW) acknowledges the support of a MICRO-SBRC grant and the W.M. Keck Foundation.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Observation of Low-T GaAs Growth Regimes By Real-Time Ellipsometry

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The molecular beam epitaxial growth of low temperature (LT) GaAs films has been studied by real-time ellipsometry. A modification in a GaAs(001) surface by cooling under a specific As_2 flux caused a change in the ellipsometry data. The thermocouple reading of this change was used as a signature to indicate the reproducible substrate temperature for the growth of LT-GaAs layers. The origin of this surface modification was studied by reflection high energy electron diffraction. The growth regimes of LT-GaAs layers were studied by real-time ellipsometry. The dielectric properties of the epitaxial layer and the critical thickness for epitaxial growth were extracted for various growth conditions. The microstructure beyond the critical point was found to be composed of amorphous as well as crystalline forms of GaAs.

Key words: Ellipsometry, LT-GaAs, MBE

INTRODUCTION

The growth of low temperature (LT) GaAs has been receiving considerable attention due to the high resistivities[1] and ultra-fast recombination rates[2] attainable in these films. Typical growth conditions for LT-GaAs layers are a growth rate of ~1 μ/h, an As/Ga beam equivalent pressure ratio of 3 and a growth temperature in the vicinity of 200°C. Under these conditions, as much as 1.5% excess As is incorporated into the layer, creating up to a 0.15% expansion of the lattice. The location and concentration of this excess As has been studied by several techniques[3,4] and has been found to be a combination of interstitial complexes and As antisite defects with a concentration in the range of $\sim 4 \times 10^{20}$ cm^{-3}. Upon annealing to ~600°C in an As overpressure, the excess As forms precipitates with sizes less than 10–20 nm[6] and the layer becomes highly resisitive.

(Received April 12, 1993)

It has been found that above a certain critical thickness, the crystallinity of the LT layers gives way to either amorphous[5] or polycrystalline[6] growth. In addition, it was found[5] that as the growth temperature exceeded ~210°C, an abrupt increase occurred in the critical thickness for epitaxial LT-GaAs.

The amount of excess As incorporated and the maximum epitaxial thickness for the LT layer depend on precise values for the As overpressure, the substrate temperature, and the growth rate. It has been reported[5,7] that film properties formed under supposedly identical conditions vary considerably. The dominant reason for this variation is the inaccuracy of the growth temperature. Variations of 10–20°C are typical and can cause the As concentration to deviate well over 20–30 percent. Recently, it has been demonstrated[8] that reproducible LT-GaAs layers may be formed by setting the growth temperature with a signature in the ellipsometric data. This signature is formed by cooling a GaAs wafer in an overpressure of As_2. In this study, the pressure-temperature rela-

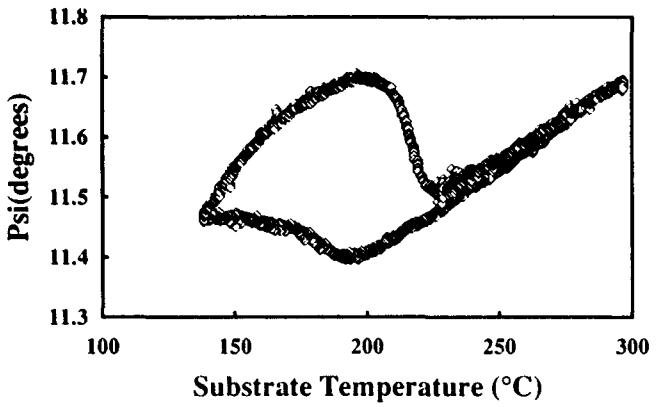

Fig. 1. Changes in ψ during the cooling of a GaAs(001) substrate in an overpressure of ~8 × 10^{-6} Torr. The minimum in the y response is labeled T_{sig}(As), i.e. the As transition temperature.

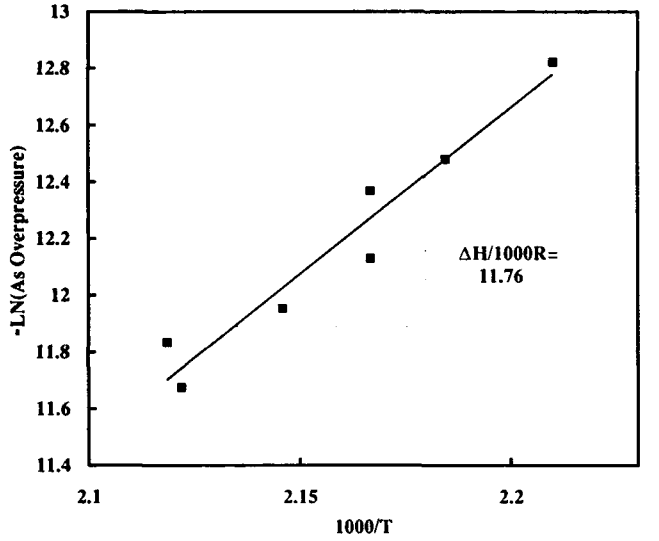

Fig. 2. Variation in the T_{sig}(As) for As overpressures in the range of 2–8 × 10^{-6} Torr.

tionship of the signature as well as the properties of LT-GaAs formed around this curve will be characterized.

EXPERIMENT

The LT-GaAs layers were deposited on both doped and semi-insulating liquid encapsulated Czochralski (001) GaAs substrates. The samples were grown in a VG V80H MkII molecular beam epitaxy (MBE) system with an As_2 overpressure of approximately 2–8 × 10^{-6} Torr as measured by the flux gauge and at a growth rate of 1.2 μ/h as measured from reflection high energy electron diffraction (RHEED) oscillation at normal growth temperatures, ~580°C. The base pressure of the system was ~5 × 10^{-11} Torr.

A single wavelength (6328Å) rotating analyzer ellipsometer was attached to two ports fitted with strain-free windows set at an angle of incidence of ~70°, near the Brewster's angle. The ellipsometer was calibrated using the residual method.[9] Intensity measurements were taken 72 times at five-degree intervals in each mechanical rotation of the analyzer. The measurements were averaged over ten rotations to increase the signal-to-noise ratio. The frequency of the rotating analyzer was ~4 Hz, resulting in a data rate of ~0.2 Hz for the average of ten rotations including computation and graphics. Ellipsometry data (ψ, Δ) were extracted from these intensity measurements every few seconds. Here (ψ,Δ) are defined by r_p/r_s = tanψ exp(iΔ), where r_p(r_s) is the complex amplitude reflectivity for light polarized parallel (perpendicular) to the plane of incidence.[10] The ellipsometer was used to follow changes which occurred during the preparation and growth of the LT-GaAs layers.

Structural characterization of the specimens was performed using a double-crystal x-ray diffractometer (DXRD) and a thin film diffractometer (TFD) equipped with a rotating specimen stage. Both instruments were attached to opposite sides of a water-cooled CuK_α source.

RESULTS AND DISCUSSION

The As Signature

When (001)GaAs is cooled in an environment of A a change in the ellipsometric data occurs at a te perature corresponding to the point at which condenses. Figure 1 shows the ellipsometric response for a sample in an As_2 overpressure of ~8 × 10^{-6} Torr cooled at a rate of ~2°C/min. The thermocouple reading which was acquired in real time has been approximately adjusted to an actual temperature reading by first using a two-color optical pyrometer to determine the temperature at a higher setting and then linearily extrapolating this value to the signature region. The psi value of the ellipsometric data is initially seen to decrease as the temperature is lowered, due to an increase in the band gap and associated decrease in the extinction coefficient, k. At a nominal value of 190°C in the cooling, psi started to increase and saturated at approximately 150°C. This minimum is designated the signature point, T_{sig}(As). Commensurate with the change in psi, the RHEED pattern was seen to change from a c(4x4) pattern to a hazy (1 × 1) structure. This result is in agreement with those reported by Bachrach et al.[11] and has been attributed to the adsorption of As onto GaAs, forming a disordered layer of As. Upon subsequent reheating, psi remains high for temperatures above the signature point. This hysteresis is believed to be a result of the kinetics of the adsorption-desorption phenomena and not due to the thermal lag of the substrate holder. This designation is based on the observation that upon heating, psi merges with the original cooling curve. The amount of separation was seen to increase monotonically with cooling rate.

Pressure-Temperature Relationship

The temperature position of the signature was studied for As_2 overpressures in the range of 2–8 × 10^{-6} Torr. Since this transition has been shown to be related to the condensation of a disordered As layer, it is reasonable to expect the boundary to follow the

Clausius-Clapeyron behavior. Figure 2 is a plot of the As overpressure used to form the signature against the As transition temperature represented in this form. A value of 11760 for $\Delta H/R$ is extracted from the slope. This value is approximately a factor of three lower than the heat of formation for As vapor and may result from the As structure pulling away from the underlying GaAs substrate. We believe this boundary separates the regions of high and low critical thickness for growth. Growth around this signature will be presented later.

Low Temperature GaAs Growths

Figure 3 shows the <ε1>, <ε2> trajectory of the LT-GaAs film growth. The squares indicate the experimental data, while the lines represent the simulated growth models. The initial stage of the film growth manifests the uniform layer by layer growth pattern, and corresponds to the epitaxial growth region of the LT-GaAs film. The solid line is the result of a simulation for layer by layer uniform growth. The dielectric constants of the LT-GaAs epitaxy layer obtained by the simulation were (ε1,ε2) equal to (15.09, 2.56). The LT film has higher optical absorption compared to the ordinary GaAs films. Double-crystal x-ray diffractometer analysis showed the film exhibited a single well-defined film peak with adjacent pendelosung fringes. These fringes would not be present if either interface of the LT-GaAs layer were rough. This mode of growth continues up to a thickness corresponding to point y. At this point, the trajectory deviates from the ideal spiral and progresses toward an end point different from the center of the spiral. This effect can only be explained with the nucleation of a second material which possesses different dielectric properties than that of the epitaxial LT-GaAs layer. Therefore, point y corresponds to the breakdown of crystallinity and the onset for the nucleation of previously reported pyramidal defects.[5,6] The broken line represents simulated growth beyond point "y" assuming that the film is composed of an epitaxial LT-GaAs and a second material. A post growth spectroscopic ellipsometry study indicated that the second material in the film was composed mainly of amorphous GaAs and voids. The dielectric constants of the physical mixture of two materials were determined by the Bruggman effective medium approximation.[12] A polycrystalline component could not be ruled out since the index of GaAs is isotropic, so that polycrystalline GaAs and single crystal GaAs possess the same dielectric properties. Thin film diffraction analysis showed the presence of a polycrystalline component for thick samples. In the simulation represented by the broken line, the volume of nucleating material is represented by a geometric model shown in Fig. 4.

In this model, nucleation occurs on a rectangular grid and the growth proceeds as "cones" centered on the grid. The shape of a cone is defined by its boundary which takes the form of $h/H = (r/a)^G$, where 2a represents the shortest spacing between two nuclei, and H is the height of the cones as they merge together. For the straight-line case, G is equal to 1. For the trajectory modeled in Fig. 3, G has a value of 0.9 and H has a value of 4100Å. Most of the LT-GaAs samples exhibit very similar growth patterns, al-

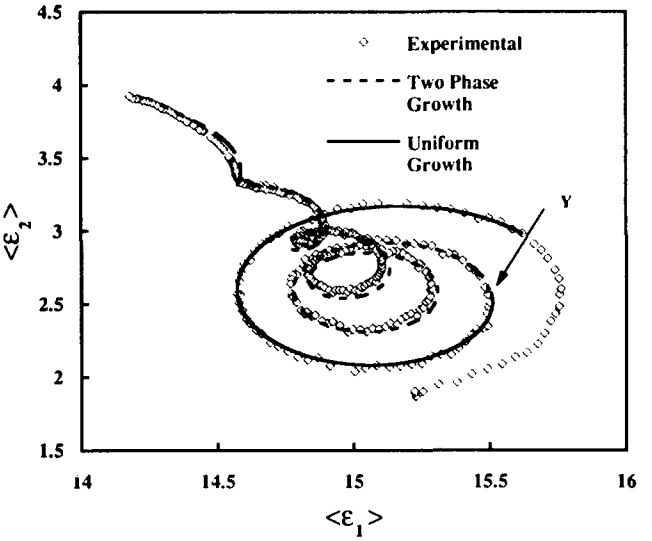

Fig. 3. Trajectory of <ε1> ,<ε2> for LT-GaAs film showing different regions of growth. The solid line represents homogeneous growth of a layer with (ε1, ε2) equal to (15.09, 2.56). The dashed line is a model for growth of a two-phase region consisting of LT-GaAs, amorphous GaAs, voids, and possibly other crystalline forms of GaAs.

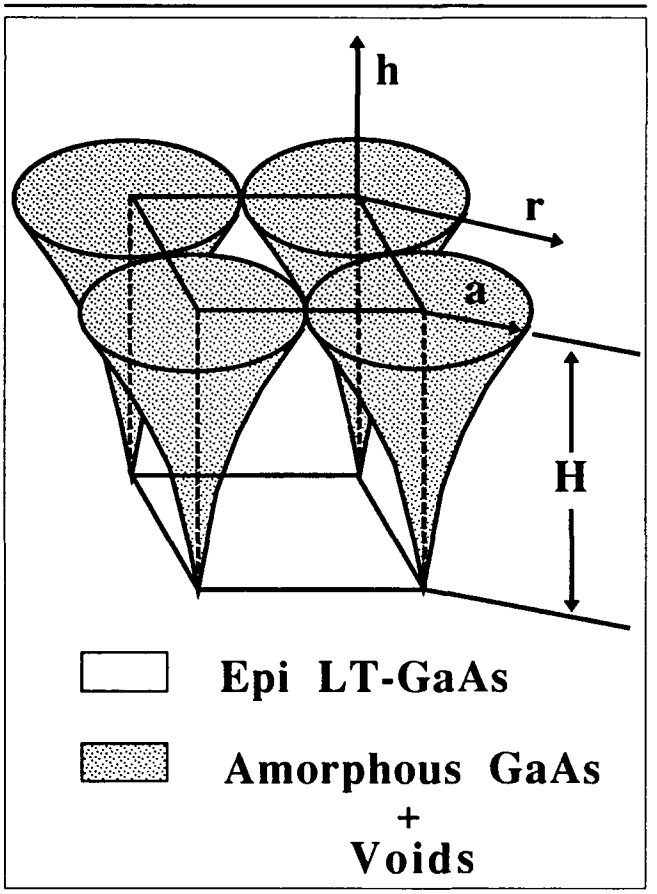

Fig. 4. The geometric model for growth in the two-phase region. The inverted cones represent a second phase which is nucleated and whose volume fraction increases as the film thickens.

Table I. Variation of LT-GaAs Film Properties with As Overpressure

As_2 Overpressure (Torr)	Refractive Index n	Extinction Coefficient, k	Critical Thick. (Å)
8×10^{-6}	3.955	0.276	2400
6×10^{-6}	3.961	0.271	4000
4×10^{-6}	3.977	0.293	>6300

though not every film can be simulated satisfactorily with this simple geometric model. The thickness at which the epitaxial structure breaks down can be extracted for all films by observing the point at which the data deviates from the homogeneous growth mode.

To study the effect of growth around the c(4 × 4) and 1 × 1 boundary, three LT-GaAs samples were formed at the same substrate temperature for different As overpressures. The growth temperature setting was determined by the thermocouple reading for T_{sig}(As) using an As overpressure of 8×10^{-6} Torr. The first sample was grown with the As overpressure held at the same value at which the signature was determined. The other two samples were grown with a much lower As pressure. Table I contains the index, extinction coefficient, the critical thicknesses extracted, and the As overpressure used during the growth. The sample grown close to the signature point was found to have a decreased critical thickness and an increased excess As concentration. As the pressure was lowered, the critical thickness increased quickly to 0.6 μ with a slight decrease in the excess As incorporated.

CONCLUSIONS

An ellipsometric signature caused by modification of the (001) GaAs surface was used to produce LT-GaAs films. This surface modification was shown by the RHEED observation to be in the c(4 × 4) to 1 × 1 transition region. Ellipsometric modeling of the growth trajectory for LT-GaAs was presented. Samples grown at the same T_{sig}(As) with different As overpressures were found to have different critical thicknesses. The lower As overpressure produced a LT-GaAs layer with an extended critical thickness relative to the sample grown at the signature overpressure.

ACKNOWLEDGMENTS

This work was supported by Materials and Manufacturing Technology Directorates of Wright Laboratories and by the Joint Services Electronics Program under Contract No. AFOSR F49620-92-C-0027.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Characterization of Crystalline Low Temperature GaAs Layers Annealed from an Amorphous Phase

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The results from an in-depth characterization of as-grown and annealed low-temperature GaAs layers deposited at less than 260°C are presented. The layers, amorphous as grown, became crystalline after annealing. The crystallization was documented by several characterization techniques including photoreflectance, Raman spectroscopy, photoluminescence, transmission electron microscopy, and double-crystal x-ray diffraction. The n-type conductivity of the annealed films was exploited for the construction of a diode structure.

Key words: Low-temperature-grown GaAs, MBE, TEM, XRD

INTRODUCTION

The growth by molecular beam epitaxy (MBE) of As-rich GaAs films at substrate temperatures (T_s) lower than conventionally used for the growth of GaAs has been reported in recent years.[1,2] The low temperature GaAs material (LT-GaAs) has been shown to have structural and electronic properties different from that of normal GaAs.

It was recently shown[3] that the electrical and physical characteristics of LT-GaAs films are dependent on T_s. Three temperature ranges were identified: a high temperature range, T_s>460°C; an intermediate range, 260<T_s<460°C; and a low range, T_s<260°C. The as-grown epilayers deposited in the low temperature range are amorphous, gold colored, and highly resistive.[3,4] After annealing, n-type self-doping with carrier concentration on the order of 2×10^{18} cm^{-3} occurs and the resistivity of the material decreases drastically.

The work presented in this paper is based on material grown within the low temperature range, T_s<260°C. It was shown, using several characterization techniques, that it is possible to obtain crystalline LT material by annealing the as-grown amorphous LT-GaAs.

(Received April 12, 1993)

EXPERIMENTAL

The LT-GaAs epilayers were grown by MBE on semi-insulating (100) GaAs substrates. The substrate preparation and growth procedure are described elsewhere.[3] No postgrowth annealing was performed in the MBE chamber. Subsequent annealings were performed by using a rapid thermal annealer (RTA).

The techniques used to investigate the formation of a crystalline epilayer were Raman spectroscopy, photoreflectance (PR), photoluminescence (PL), double crystal x-ray diffraction, and transmission electron microscopy (TEM). Photoreflectance and Raman spectroscopy were performed at room temperature, while the PL results were obtained at 1.6K. Raman spectroscopy was performed in the nominal backscattering geometry.

RESULTS AND DISCUSSION

Several samples were examined to study the effect of annealing on the LT-GaAs epilayers. A representative sample was sample #651, a 0.5 μm thick layer grown at 150°C. Two portions of #651 were annealed at 775°C for 6.5 and 10 min, respectively.

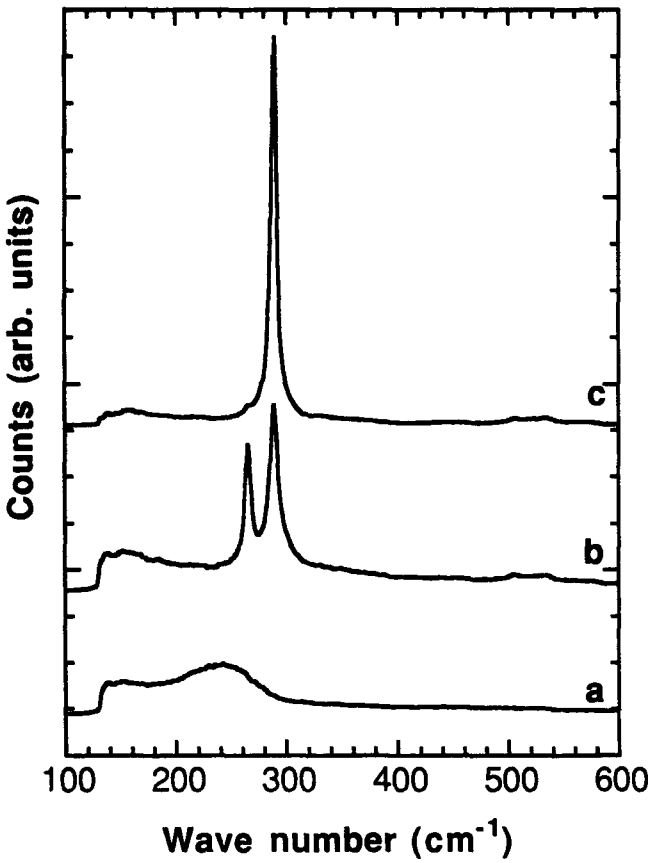

Fig. 1. The Raman spectra from: (a) an as-grown sample (#651) deposited at 150°C, (b) the same sample, annealed 6.5 min at 775°C, and (c) a conventionally grown n-type GaAs film.

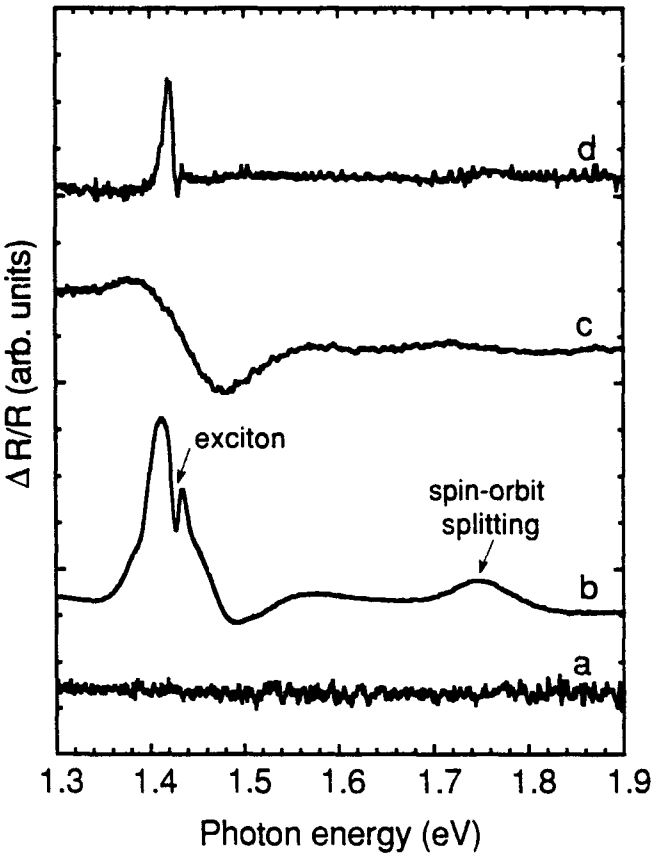

Fig. 2. The PR spectra from: (a) an as-grown sample (#651) deposited at 1 50°C, (b) the same sample, annealed for 6.5 min at 77°C, (c) a conventionally grown n-type GaAs film, and (d) the substrate of the sample in (b).

Figure 1 shows the Raman spectra for a series of samples, including #651 as-grown, (Fig. 1a), #651 annealed at 775°C for 6.5 min (Fig. 1b), and an MBE n-type GaAs film (Fig. 1c). The as-grown sample shows a broad feature in the vicinity of 250 cm^{-1}, characteristic of the vibrational spectrum of disordered GaAs. After annealing, two sharp lines due to LO and TO phonon modes appear. These lines indicate crystalline material, but in good quality (100) films, such as the reference film in Fig. 1c, selection rules prohibit the TO phonon mode. However, for other crystallographic orientations, such as (110), the TO mode is allowed. The presence of TO modes in films grown on (100) substrates indicates the existence of large misoriented crystallites or structural defects exposing non (100) planes. Because Raman scattering cannot distinguish between large crystallites and structural defects such as twin dislocations, it is necessary to perform TEM to obtain this information.

Cross-sectional TEM images of sample #651 annealed both 6.5 and 10 min showed As precipitates are concentrated near the interface between the GaAs substrate and the LT layer. The LT-GaAs film appears to be completely single crystal, except for twins near the surface. Since twins are formed at the boundary between crystal areas with different orientation, their presence may be responsible for the TO mode appearing in the Raman spectrum in Fig. 1b. These observations are in agreement with previous TEM work on LT-GaAs films, indicating that the recrystallization starts at the interface and progresses toward the surface.[4] Single-crystal and double-crystal x-ray diffractometry performed on a variety of samples also confirmed that the epilayers annealed at high temperatures were crystalline with a full width at half-maximum between 10 and 11 arc-s, comparable to good quality bulk GaAs.[4]

Figures 2a–2d, show the PR spectra obtained respectively from sample #651 as-grown, sample #651 annealed for 6.5 min, from a reference n-type conventional GaAs film with carrier concentration of 2×10^{18} cm^{-3}, and from the back of the annealed sample. No PR signal could be obtained from the as-grown film #651. Since modulation spectroscopy has been shown effective in probing amorphous semiconductors,[5] the lack of signal from the as-grown sample is probably not due to the amorphous nature of the film, but rather to a large number of traps in the film inhibiting the modulation of the surface field. The PR signal is proportional to the surface photovoltage;[6] a large number of traps will inhibit the modulation by eliminating the photoexcited electrons and holes that are required to induce the photovoltage. An alternative explanation for the lack of photovoltage would be the absence of built-in field due to heavy pinning of the Fermi level near midgap. Photoluminescence studies,

to be discussed later, indicate the existence of a large number of traps in the as-grown layer.

In Fig. 2b, the PR spectrum from the annealed sample #651, the high signal-to-noise ratio, and the presence of the spin-orbit splitting structure around 1.75 eV indicates that the crystalline quality of the epilayer is very good, and that the film is probably mostly single crystal. The crystalline quality of the epilayer is supported by the presence of an excitonic transition overlapping the E_0 structure at 1.42 eV, since excitons require the existence of crystallites having a radius greater than the excitonic Bohr radius. Furthermore, the width of the structure matches that from heavily doped GaAs, shown in Fig. 1c, in agreement with the observation of the n-type nature of the annealed LT-GaAs films. The decrease in resistivity with annealing as well with the increase in the signal amplitude also suggests a reduction in the number of traps and recombination centers.

In Fig. 2d, the PR spectrum from the back of the annealed sample #651, the band gap spectrum is dominated by the excitonic structure, in agreement with the semi-insulating nature of the substrate. The spin-orbit splitting is barely present. This spectrum confirms that the PR spectra in Figs. 1a and 1b cannot be attributed to the substrate.

Further support for the crystalline nature of the LT GaAs film after high temperature annealing is provided by PL. Representative PL spectra obtained at 1.6K from the as-grown LT-GaAs layer #651 and after a 10 min anneal treatment at 775°C are shown, respectively, in Figs. 3a and 3b. The increase in amplitude of the PL spectrum after annealing is by itself an indication of the reduction in the density of traps in the film. No sharp band edge related feature was found in the PL spectrum from the as-grown film. In contrast to this result, a fairly sharp band at 1.49 eV was observed from the sample after annealing at 775°C. This band is most likely due to donor-acceptor pair recombination based on comparisons with typical results obtained from GaAs layers grown by MBE in the conventional temperature regime (560–600°C). Thus, the observation of the band at 1.49 eV is consistent with the crystalline quality of the high temperature annealed sample. Three additional bands are found from this sample with peak energies at 0.97, 1.24, and 1.41 eV. The emission band at 1.24 eV has been reported recently by other workers for high-temperature annealed LT-GaAs samples and is thought to involve Ga vacancies.[7]

Crystallization of the LT-GaAs epilayer after annealing was also indicated by the improvement in the electrical properties of a diode structure, formed by growing an LT-GaAs film over a layer of conventionally grown p-type GaAs, with annealing. After annealing, the n-type carrier concentration in the LT overlayer effectively created an n/p junction. The as-grown structure was highly resistive and the current increased linearly with bias. After anneals at temperatures between 400 and 600°C, the diode developed rectifying characteristics; these characteristics

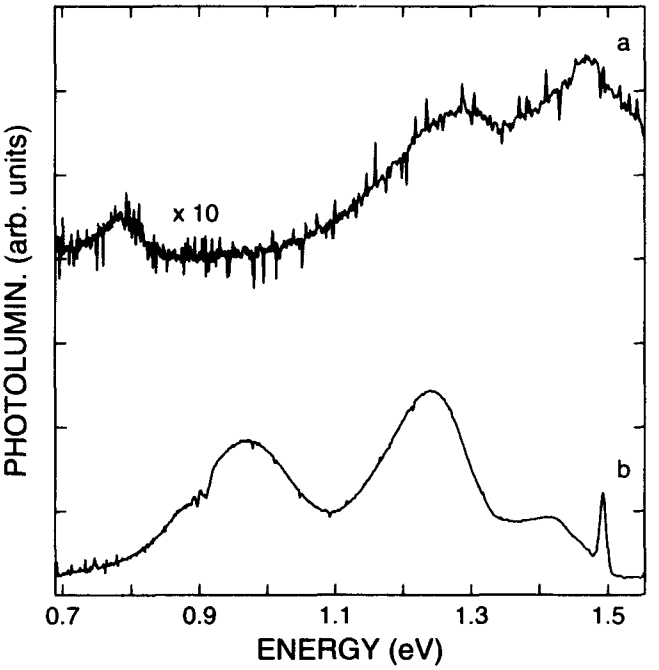

Fig. 3. Photoluminesence spectra obtained at 1.6K from the LT-GaAs sample #651 (a) as-grown, and (b) after a 10 min anneal at 775°C.

improved with higher anneal temperatures (T>600°C). From the evidence presented above, the improvement in the diode characteristics was attributed to the better crystalline quality of the LT layer after high temperature anneals.

CONCLUSIONS

In summary, the results from a set of characterization techniques indicate that the low-range LT GaAs films are amorphous as-grown and become crystalline with annealing. The crystallization progresses from the GaAs/LT-GaAs boundary toward the film surface, and As precipitates form at the interface. The n-type properties of the annealed films were used for the fabrication of a diode structure.

ACKNOWLEDGMENTS

The authors would like to thank Jeff Mittereder and Mark Goldenberg of SFA, Inc., for their invaluable technical assistance. Two of the authors (A.G. and C.S.K.) gratefully acknowledge the support of the U.S. Office of Naval Research.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Anomalies in Annealed LT-GaAs Samples

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The annealing behavior of low temperature (LT)-GaAs layers was investigated using transmission electron microscopy, x-ray rocking curves, and H^+ ion channeling. These data were compared to the Hall-effect and conductivity data obtained earlier on the same samples. An expansion of the lattice parameter above those observed for as-grown LT-GaAs layers was observed for the layers annealed at 300 and 350°C. No precipitation was observed in transmission electron micrographs for these annealing temperatures. Based on ion-channeling results, the As atoms (split interstitials) appear to be in the same position as found for the as-grown layers. A special arrangement of As split interstitials or out-annealing of gallium vacancies would be consistent with a decrease of the dominant acceptor in these layers and an increase in the lattice parameter. For annealing above 400°C, the lattice parameter decreased and in fact was found to achieve the substrate value at annealing temperatures of 500°C and above. The decrease in the lattice parameter above 400°C is related to the decrease of excess As antisite defects and As split interstitials in the formation of As precipitates.

Key words: Low-temperature-grown GaAs, MBE, precipitation, TEM

INTRODUCTION

Research in the last few years has shown that GaAs grown by molecular beam epitaxy (MBE) at low temperatures (about 200°C) has very interesting physical properties and can be used as a buffer layer and gate-insulator for field effect transistor (FET)-type devices, as well as an active layer, for fast photoconductive switches, since the lifetime of the minority carriers in these layers is very short (in the range of a few hundred fsec).[1,2] For layers 2 μm thick grown at 200°C or above, a high crystalline perfection can be obtained. At lower growth temperatures breaking of the perfect crystallinity is observed. It appears that at a given growth condition, only a specific "critical layer thickness" of crystalline material can be grown.[3] This layer thickness is linearly dependent on the excess of As in the layer. The excess As leads to an expansion of the unit cell in all three crystallographic directions. However, a much larger expansion is observed along the growth direction, leading to tetragonal distortion.[4] Due to the difference between the lattice parameter of the layer and that of the substrate, a strain buildup in the layer can explain the critical layer thickness at which the breaking of crystallinity is observed. A high density of As_{Ga} antisite defects (10^{20} cm^{-3}) detected in these low temperature (LT)-GaAs layers leads to hopping conduction.[5,6]

Annealing of LT-layers, either due to the growth at a higher temperature of a cap layer on the top of LT layer, or due to ex-situ annealing at about 600°C, leads to a decrease of the lattice parameter to a value close to that of the substrate. For such annealed layers, the formation of hexagonal arsenic precipitates is observed.[7-11]

Since annealing of these layers is necessary for most optoelectronic applications, it is important to understand the annealing dynamics. A previous study by Look et al.[12] of annealed LT-GaAs layers grown at 200°C on GaAs with AlAs interlayers showed strong anomalies in mobility and carrier concentration in the temperature range 350–450°C. It was shown that the dominant acceptor strongly decreases and then increases in the 350–450°C temperature range. Above

(Received April 12, 1993)

Table I. Splitting of the Rocking Curves ($\Delta\theta$) Between the Substrate and LT-GaAs Measured Along 004 Reflection and Equivalent Change of the Lattice Parameter of the Layer Compared to the Substrate (Δa) at Different Annealing Temperatures

	Sample A		Sample B	
T°C	$\Delta\theta$°	Δa(Å)	$\Delta\theta$°	Δa(Å)
As-grown	0.035	0.0053	0.03	0.0045
300	0.04	0.0061	—	—
350	0.0395	0.0060	0.025	0.0038
400	0.025	0.0038	0.025	0.0038
450	0.01	0.0015	0.01	0.0015
500	0	0	0.005	0.00076
550	0	0	0	0
600	0	0	0	0

450°C, donors, acceptors, and the antisite defects all decrease in concentration. In order to understand these phenomena and correlate them with previous observations, transmission electron microscopy, x-ray studies, and ion channeling using a 0.5 MeV H^+ beam were applied to the same samples.

EXPERIMENTAL

Two sets of LT-GaAs layers were grown by MBE at two different temperatures: 200°C (samples A) and 250°C (samples B). The growth temperatures are only approximate since the wafers were not In-bonded to the substrate holders. The layers were 2 μm thick and were separated from the substrate by a layer of 60 nm of AlAs. These layers were cut into pieces, and each piece was annealed for 10 min at a temperature in the range 300–600°C at 50°C increments. On parts of each sample, Hall-effect and conductivity data were obtained. These data were published earlier.[12] The remaining parts were used for the structural studies. X-ray rocking curves were obtained for each sample in order to obtain the lattice parameters of the layers.

For ion channeling measurements, 0.5 MeV H^+ ions were used. The ion beam was aligned along the <110> axis of the layer. Angular scans were obtained by tilting the sample parallel to a {110} plane across the <110> axis and measuring the GaK_α and AsK_α x-rays. The x-ray yields at each tilt angle were normalized to the values obtained when the ion beam was not aligned with any axis of the sample; i.e. in a random direction. The <110> axis was chosen since the Ga and As atoms form separate rows in this direction.[13]

A 002B Topcon microscope with 200 KeV accelerating voltage was used for the study of the structural quality of these samples. Plan-view and cross-section samples were prepared for each of annealed samples.

RESULTS AND DISCUSSION

X-ray rocking curves measured along the 004 Bragg reflection showed two separate peaks from the substrate and from the layer: $\Delta\Theta = 0.035°$ apart for sample A and 0.03° apart for sample B. This result

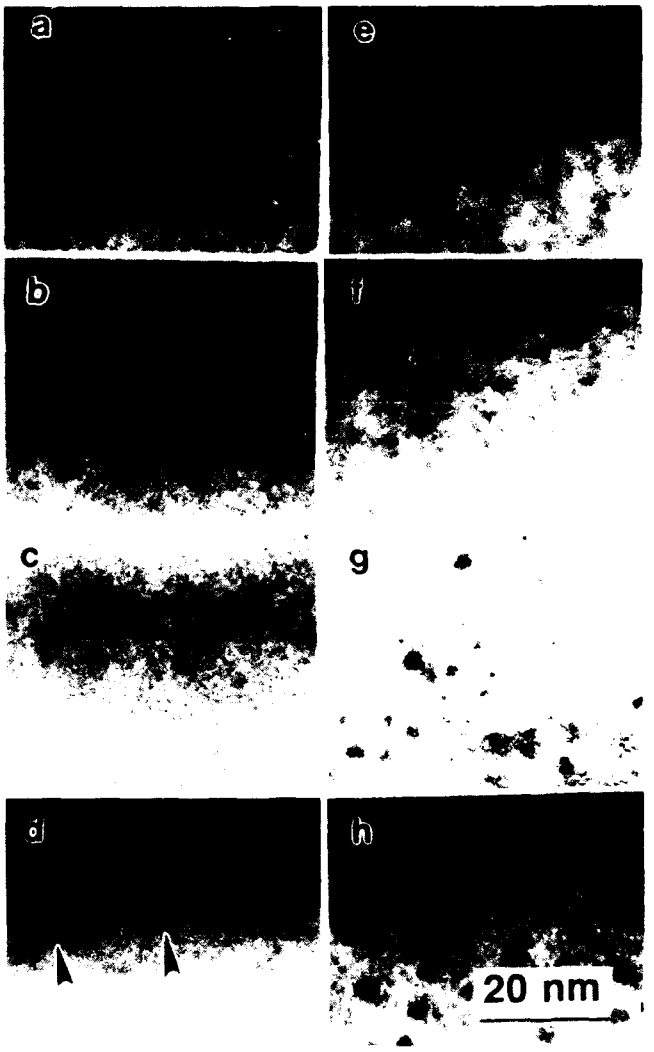

Fig. 1. Transmission electron micrographs from cross-section LT-GaAs layers annealed at different temperatures. For comparison, a micrograph of bulk GaAs sample is shown at (a). Some microclusters are observed already in bulk material. It was noticed that the number of microclusters did not increase at annealing temperatures of 300 C (b) and 350 C (c). A noticeable increase of microclusters was observed for annealing at 400 C (d). The size of microclusters increased with annealing temperature (e–h). All micrographs were taken in the two-beam condition (220) and the fractions of the micrographs shown indicate a layer thickness slightly above the second thickness contour; therefore, all microclusters appear with black contrast.

correlates with a change of the lattice parameter of 0.094% for sample A and 0.079% for sample B. Further increase in peak separation from 0.035° to 0.04° (see Table I) was observed for layer A annealed at 300–350°C. Two separate peaks were observed for annealing at 400–450°C, but the separation between these two peaks decreased below the original separation for the as-grown layers. Only at 500° and above did the peak separations between the layer and the substrate disappear, as was observed in our previous studies.[8] This disappearance was interpreted as a decrease of the lattice parameter to the substrate value. Very similar behavior was observed for the annealing of sample B. However, this sample was not annealed at 300°C. Therefore, the value of the lattice

parameter at this temperature is not known for this sample. For the annealing in the temperature range 350–400°, the peak separation remained the same (0.025°) and decreased only slightly below the value observed for as-grown samples (0.03°). A steady decrease in peak separation was observed in the temperature range 450–500°, with complete disappearance at 550 and 600°C.

Cross-section and plan-view tranmission electron microscopy (TEM) studies were performed on samples A and B for all annealing temperatures. For comparison, GaAs substrate samples were studied with the same diffraction conditions as those used for the LT-GaAs layers. All layers showed high crystalline quality. No precipitation was observed in samples A annealed at 300 and 350°C (Fig. 1). For annealing at 400°C, at which the lattice parameter began to decrease, some clustering did take place. These clusters appear in two-beam transmission electron microscopy micrographs as either white or black dots, depending on the thickness of the sample. The white dots appear on the side of the thickness contour closer to the perforation of the sample, and the black dots appear on the other side indicating that these defects are lighter than the surrounding matrix. The size of the microclusters in these samples does not exceed 1.0 nm. Annealing at 450°C leads to a large increase of the density of these microclusters, and some increase of their size (Fig. 1). At 500°C, where the lattice parameter of the layer decreases to the substrate value, the size of these microclusters further increases up to 2.5 nm. The density of these microclusters for anneals at 500°C was estimated as 2.3×10^{18} cm^{-3}. At 550°C, a slight increase of the size of microclusters (up to 3 nm) and decrease of their density down to 7.3×10^{17} cm^{-3} was observed. The majority of these clusters show a very specific contrast, with each second (200) plane enhanced, indicating an ordering within the cluster (Fig. 2). This can be interpreted by assuming that each second two adjacent planes are occupied by the same atoms; e.g. As atoms (an ordering of As_{Ga} antisite defects), such as: GaAs,AsAs,GaAs,AsAs,Ga....Such clusters cannot be metallic.

For the samples annealed at 600°C, moiré fringes were observed on all precipitates. Their size increased up to 5–8 nm in diam and the distance between the precipitates increased from 4 to 7 nm. Based on the diffraction patterns and high-resolution images, these microclusters were determined to be As precipitates. At early stages of their formation, no extra spots could be obtained in the diffraction pattern, suggesting that they were coherent with the surrounding matrix.

Annealing of samples B leads to the same conclusion. First, clustering of As is observed with annealing at 400°C. For the annealing at 550 and 600°C, extra spots consistent with hexagonal arsenic can be seen in the diffraction patterns.

Plan-view micrographs from both samples A and B show high crystalline perfection; and for annealing at 300–500°C, the surface was featureless. However, at 500°C, rectangular etching figures were observed similar to those observed in our earlier studies.[7] These figures were elongated in the [110] direction. For higher annealing temperatures, the size of the etching figures increased up to 40 nm in length and 10 nm in width.

Using H^+ ions, the critical half angle $\Psi_{1/2}$ of the Ga and As x-ray angular scans across the <110> channel parallel to a {110} plane can provide an indication of the lattice location of the excess As atoms in the layer. In particular, the ratio of the Ga and AsK_α x-ray $\Psi_{1/2}$, $x = \Psi_{1/2}(Ga)/\Psi_{1/2}(As)$, is influenced by the position of the excess As. The ratio of the back-scattered yield when the beam is exactly aligned in a channel, to the yield when the beam is incident on the target in a random direction, is designated as χ_{min} and is a measure of the crystalline quality of the sample. Table II summarizes the average of the GaK_α and AsK_α scans and χ_{min} for a bulk standard as well as for the as-grown and the annealed LT-GaAs layers. From Table II, one can notice that $x = 0.93$ for bulk GaAs while $x = 0.97$ for the as-grown LT-GaAs layer. This increase in x value is smaller for sample A than for another sample measured earlier ($x = 1.05$).[14] However, this is consistent with rocking curve measurements, since $\Delta\Theta$

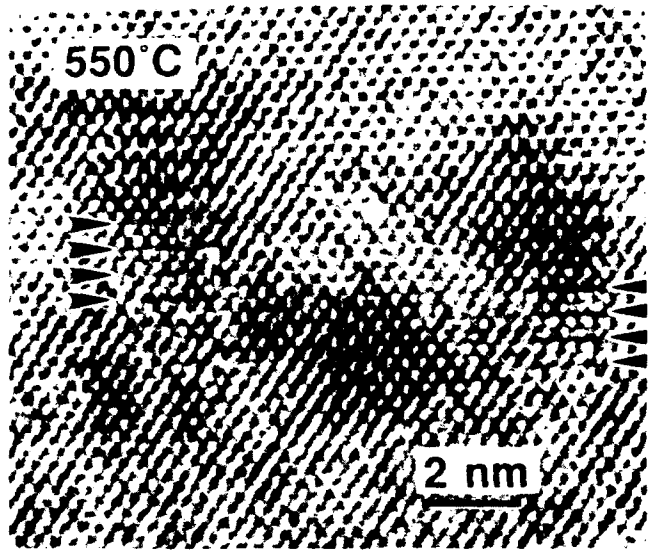

Fig. 2. Ordering (shown by arrows) of As_{Ga} antisite defects within the microclusters formed at 550°C.

Table II. An Average Critical Half Angle, $\Psi_{1/2}$, the Minimum Yield, χ_{min}, and Ratios $x = \Psi_{1/2}(Ga_{K\alpha})/\Psi_{1/2}(As_{K\alpha})$ Obtained for the GaK_α and AsK_β Scans of the Bulk GaAs Standard and the As-Grown and Annealed LT-GaAs Layers

Sple. A	$\Psi^\circ_{1/2}$ (±0.03°) Ga	$\Psi^\circ_{1/2}$ (±0.03°) As	$\Psi^\circ_{(Ga)}$ $\Psi^\circ_{(As)}$ (±0.02)	χ_{min} (±0.005) Ga	χ_{min} (±0.005) As
As-grown	0.75	0.77	0.97	0.24	0.22
350°C	0.80	0.82	0.98	0.23	0.20
450°C	0.79	0.83	0.95	0.24	0.22
Bulk	0.79	0.85	0.93	0.20	0.17

measured in this sample was 0.055 (more excess of As and larger differences in the lattices parameter of the substrate and the layer) instead of the 0.035 measured in sample A. This indicates that the channels in the LT-GaAs layers are obstructed by a high concentration of defects that dechannel the incident ion beam, but the concentration of these defects in sample A is smaller than in the sample measured earlier.[14] This excess of As can be in the form of As_{Ga} antisite defects or interstitial As defects. In the first case, this defect would not change the x value; therefore, the interstitial atom needs to be considered.

In GaAs, two isolated interstitial positions are possible, one with tetrahedral symmetry and the other with hexagonal symmetry. An interstitial atom in the tetrahedral site should show a symmetric double peak in the center of the <110> channels and no enhanced scattering from the other channels. In contrast, scattering from an interstitial atom in the hexagonal site should show a peak in the center of the <100> channels and no enhanced scattering from the other channels. Particle induced x-ray emission measurements in the channeling configuration did not show an As emission peak in the center of the <100> channel, nor did they show a symmetrical double peak structure in the center of the <110> channel. Therefore, this dechanneling is probably due to more complex defects involving interstitial As, such as a split interstitial that shares lattice sites with substitutional As.[15] It is interesting to observe that x = 0.98 for annealing of sample A at 350°C, similar to that observed for as-grown layers ((x = 0.97), estimated accuracy ±0.02). This indicates that the excess As atoms in the annealed sample remain in the same "split interstitial" position as for the as-grown layer. For layer A annealed at 450°C, one can observe the decrease in x value, suggesting that precipitation is taking place at this temperature, consistent with TEM observations. Since the changes in the x ratio are comparable to the measurement error, quantitative information on the interstitial As cannot be obtained. However, one can look at these results as a consistent trend in the annealing of the excess As atoms. Furthermore, the minimum yields of the Ga and As x-rays from this layer show that they are of high crystalline quality, again consistent with TEM observations.

Hall-effect and conductivity measurements compared with absorption measurements on the same sample A lead to the conclusion that the dominant acceptor (most possibly V_{Ga}) strongly decreases for annealing temperature 300–400°C.[12]

CONCLUSIONS

Four independent studies (TEM, x-ray rocking curves, H^+ ion channeling and transport measurements) are consistent with each other. Transmission electron microscopy studies show that the A and B LT-GaAs layers are of high crystalline quality, with an expansion of the lattice parameter of the order of 0.094%. Three types of point defects can contribute to an excess of As in the as-grown LT-GaAs layers: arsenic antisites (As_{Ga}), As-interstitials (As_i), and gallium vacancies (V_{Ga}).

The anomalies observed in the resistivity of these samples, as well as in the acceptor concentration, are probably related to the observed increase of the lattice parameter of the layers for annealing at 300 and 350°C. As indicated from ion-channeling results at these annealing temperatures, the As split interstitials need to be considered. According to the total-energy calculations,[16] As interstitals form a large negative-U system: $2As^0 \rightarrow As^+ + As^-$. In this reaction, As interstitial can be either in positively, neutral, or negatively charged state depending on their configuration in the unit cell. Different bond stretching (5–9%) is expected at each configuration.[16] In these low annealing temperatures, movement of interstitial atoms can be considered and bond stretching would explain the observed increase of the lattice parameter. One can speculate that the annealing of V_{Ga} out from the layer might increase the lattice parameter as well.

As can be observed from TEM results, the first As-rich clusters start to form at 400°C, but the size of these clusters is very small. The lattice parameter at this annealing temperature decreases compared to the one observed for as-grown layers. For annealing at 450°C, TEM results show an increase in the diameter of these clusters, leading to a further decrease of the lattice parameter of the layers. Specific ordering of As_{Ga} antisite defects can be observed at an early stage of clustering. Ion channeling results show a change in x, suggesting a decrease in the concentration of (As_i); e.g. "split interstitials." It can be speculated that a large number of vacancies can be created at this point. Three factors [a large number of vacancies, breaking of the bonds of "split interstitials," and migration of (As_{Ga}) to form As precipitates] would lead to the decrease of the lattice parameter of the layer. Annealing at 500°C and above leads to a further increase in the precipitate size, so that the number of (As_{Ga}) and (As_i) atoms must decrease as is confirmed by Hall measurements.

ACKNOWLEDGMENTS

This work was supported by AFOSR, Contract No. AFOSR-ISSA-90-0009, through the U.S. Department of Energy, under Contract No. DE-AC03-76SF00098. The use of facilities of the Materials Science Division and National Center for Electron Microscopy at Lawrence Berkeley Laboratory, supported by the Department of Energy under Contract No. DE-AC03-76F00098 is also appreciated. ZLW wants to thank Dr. J.B. Kortright for the use of the double-crystal diffractometer for the rocking curve measurements and W. Swider for excellent TEM sample preparation. DCL was supported under USAF Contract F33615-91-C-1465.

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Annealing of As_{Ga}-Related Defects in LT-GaAs: The Role of Gallium Vacancies

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We have studied the annealing properties of As_{Ga}-related defects in layers of GaAs grown at low substrate temperatures (300°C) by molecular beam epitaxy (low temperature[LT]-GaAs). The concentration of neutral As_{Ga}-related native defects, estimated by infrared absorption measurements, ranges from 2×10^{19} to 1×10^{20} cm^{-3}. Slow positron annihilation results indicate an excess concentration of Ga vacancies in LT layers over bulk grown crystals. A sharp annealing stage at 450°C marks a rapid decrease in the As_{Ga} defect concentration. We propose that the defect removal mechanism is the diffusion of As_{Ga} to arsenic precipitates, which is enhanced by the presence of excess V_{Ga}. The supersaturated concentration of V_{Ga} must also decrease. Hence, the diffusivity of the As_{Ga} defects is time dependent. Analysis of isothermal annealing kinetics gives an enthalpy of migration of 2.0 ± 0.3 eV for the photoquenchable As_{Ga} defects, 1.5 ± 0.3 eV for the V_{Ga}, and 1.1 ± 0.3 eV for the nonphotoquenchable defects. The difference in activation enthalpy represents difference energy between an As atom and Ga atom swapping sites with a V_{Ga}.

Key words: Defects, low-temperature-grown GaAs, MBE

INTRODUCTION

The incorporation of a high concentration of excess As is responsible for the unique properties of GaAs grown by molecular beam epitaxy (MBE) at low temperatures (LT) (200–300°C) (LT-GaAs). An excess of As atoms as high as 1.5% has been reported.[1] The excess As is incorporated mainly as As_{Ga}-related defects[2] in as-grown material and as As precipitates in annealed materials.[3] The As_{Ga}-related defects anneal away at temperatures less than about 500°C. This behavior is similar to the annealing characteristics of As_{Ga}-related defects in GaAs heavily damaged by plastic deformation[4] or neutron irradiation.[5] In stark contrast, As_{Ga}-related defects in undamaged GaAs are much more stable. EL2 defects in as-grown liquid encapsulated Czochralski (LEC) GaAs crystals anneal away only at temperatures greater than 1000°C.

(Received April 12, 1993)

The difference in the annealing behavior has led to suggestions that the As_{Ga}-related defects in heavily damaged GaAs are defect complexes rather than isolated As_{Ga} defects. We would argue that this does not have to be the case. To explain the lower thermal stabilty of As_{Ga}-related defects in LT and heavily damaged GaAs, we have previously proposed a model of diffusion limited precipitation which is enhanced by an excess concentraiton of V_{Ga}.[6] The mobile V_{Ga} facilitate the diffusion of As_{Ga} defects toward precipitates acting as As sinks. Since the V_{Ga} already exist in the material, only the energy of migration must be overcome and not the formation energy of a V_{Ga}.

This work will build on the model. Included is the fact that the excess concentration of V_{Ga} must also decrease, resulting in a time dependent diffusivity. The anlaysis of the As_{Ga}-related defect concentration vs isothermal annealing time yields intriguing information on the enthalpies and entropies of migration for As_{Ga} and V_{Ga}.

Samples were grown in a Varian Gen II MBE

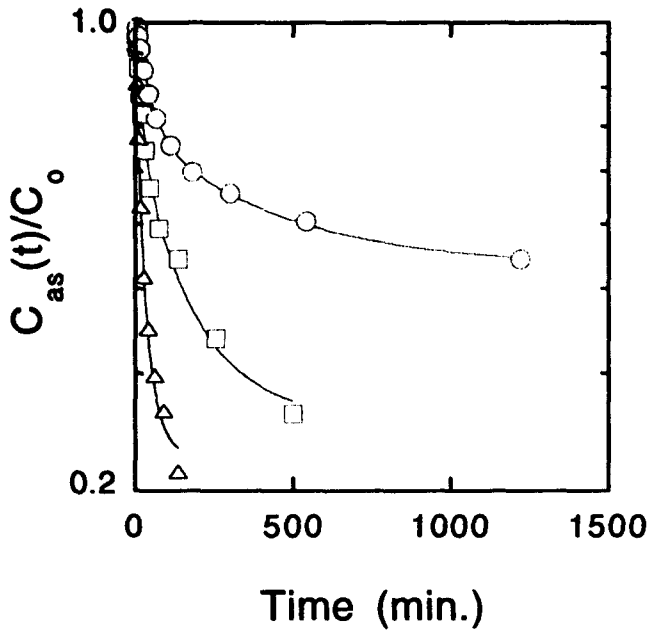

Fig. 1. Normalized concentration of As_{Ga}-related defects as a function of annealing time. Symbols are the experimental points. Annealing temperatures were: o 400°C, □ 440°C, Δ480°C. Solid lines are the Chi-squared nonlinear least-square fit of Eq. (6).

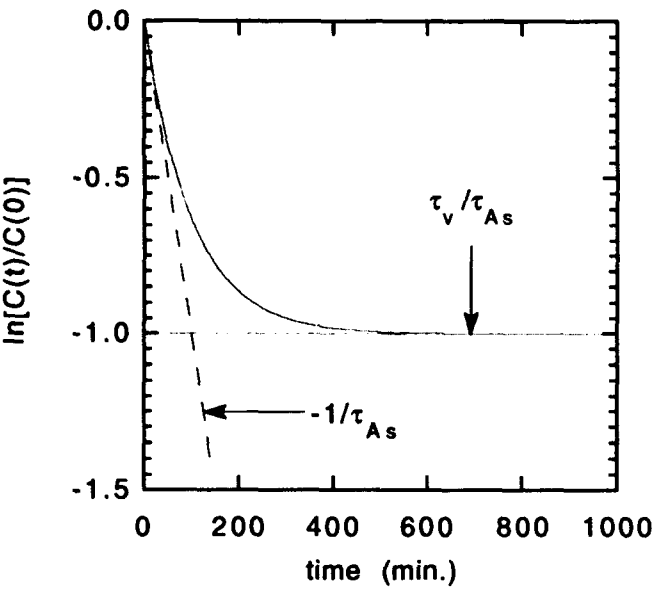

Fig. 2. Plot of Eq. (5) describing the average As_{Ga} concentration of a diffusion limited precipitation problem with an exponentially time dependent diffusivity. Limiting behavior is indicated by the dashed lines. $\tau_v = \tau_{As} = 100$ min.

system at a substrate temperature of 300°C. The As_4/Ga flux ratio was 2. The growth rate was 1 μm h^{-1}. The layer thickness was 3 μm.

The concentration of neutral As_{Ga}-related defects was measured by infrared (IR) absorption,[7] similar to EL2.[8] Defect concentrations were determined from the absorption at a wavelength of 1 μm (1.24 eV) relative to the background absorption at 1.7 μm (0.73 eV) using the calibration of Martin.[8]

The excess V_{Ga} concentration in the LT layers relative to the LEC substrate was determined from the S-parameter characteristic of the annihilation γ-ray spectrum.[9] Positron annihilation studies were performed at the Institute of Materials Science, Tsukuba, Japan, and the results have been discussed previously.[6] Although it is difficult to quantify the positron annihilation results, they provide us with very important information that excess V_{Ga} exist in LT-GaAs on the order of 10^{19} cm^{-3}.

In two series of isothermal annealing experiments, one set of samples was annealed in flowing N_2 at 420, 450, and 490°C and another set at 400, 440, and 480°C. Annealing was interrupted at specific time intervals to make room temperature IR absorption measurements. Before each absorption measurement, samples were rinsed in 30% hydroflouric acid.

The dependence of the IR absorption at 1 μm on the annealing time is shown in a semi-log plot in Fig. 1. Symbols represent measured values while the lines are fits of the model to the annealing transients. The 480°C annealing transient is nearly a straight line and tends to zero concentration with time. This implies a regular, first order, exponential annealing process. The transient at the lower annealing temperature of 400°C, however, does not exhibit first order kinetics. Instead, the concentration transient slows with time and saturates at a nonzero value. Further annealing up to 600°C does not change the As_{Ga}-related defect concentration more than 10%. Thus, the defect concentration has been stabilized and the annealing process is nonreversible.

In order to explain the annealing transients, consider first the case of diffusion limited precipitation with a constant diffusivity, D. The spherically symmetric diffusion equation is,

$$\frac{\partial C}{\partial t} = D\left(\frac{2}{r}\frac{\partial C}{\partial r} + \frac{\partial^2 C}{\partial r^2}\right) \tag{1}$$

If the precipitate volume is small compared to the total crystal volume, solutions for the average concentration of As_{Ga} defects are exponential,

$$C_{as}(t) = C_{as}^0 \exp\left[-\frac{t}{\tau_{as}}\right] \tag{2}$$

The annealing rate is $\tau_{as}^{-1} = 4\pi C_p r_o D$, where C_p and r_o are the precipitate concentration and radius, respectively.[6,10,11]

Now consider that the V_{Ga} concentration is not constant. Since the diffusivity is proportional to the V_{Ga} concentration, it will have the same time dependence. Assuming an exponential time dependence for the V_{Ga} concentration, the diffusivity becomes,

$$D(t) = D_o \exp\left[-\frac{t}{\tau_v}\right] \tag{3}$$

where τ_v is the time constant for the loss of V_{Ga} diffusing to vacancy sinks. These could be for example voids (vacancy precipitates), defect complexes or

interfaces which include the sample surface, the layer interface and the arsenic precipitate interface. Implicit in this assumption is that the spatial variation of the V_{Ga} concentration is not correlated to the As_{Ga} concentration. Thus, the diffusivity depends only on time and can be brought out of the gradient operator. Solutions to Eq. (1) for the average concentration of As_{Ga}-related defects take the form of an exponential

$$\overline{C}_{as}(t) = C^{o}_{as} \exp\left(-\frac{\tau_v}{\tau_{as}}\right)\exp\left[\frac{\tau_v}{\tau_{as}}\exp\left(-\frac{t}{\tau_v}\right)\right] \quad (4)$$

The logarithm of Eq. (4) becomes an exponential with an offset which can be compared to the semi-log plots of the data (see Figs. 1 and 2).

$$\ln\left[\frac{\overline{C}_{as}(t)}{C^{o}_{as}}\right] = \frac{\tau_v}{\tau_{as}}\left[\exp\left(-\frac{t}{\tau_v}\right) - 1\right] \quad (5)$$

The limits of Eq. (5) at short times and infinite time are informative. For $t << \tau_v$, the initial slope equals $-1/\tau_{as}$ (see Fig. 2) which is the same as Eq. (2), the solution for a constant diffusivity. In the other extreme, for $t >> \tau_v$, the limit of Eq. (5) is the constant τ_v/τ_{as} In the case of very long lived vacancies, $\tau_v >> \tau_{as}$, Eq. (5) again becomes the same as the solution for a constant, time independent diffusivity.

One additional correction must be made to Eq. (4) before all the annealing transients can be accurately described for all times. The fast initial transient of the less stable nonphotoquenchable (NPQ) defects must be accounted for. The initial fraction of NPQ defects is measured by low temperature IR absorption measurements. This fact can be used account for the effect of the NPQ defects. By including a fast exponential recovery of the NPQ defects in parallel with the PQ fraction, Eq. (4) is modified so that the average As_{Ga}-related defect concentration is

$$\overline{C}_{as}(t) = C^{o}_{as}\left\{\begin{array}{l}(1-f)\exp\left(-\dfrac{t}{\tau_{npq}}\right) + \\ (f)\exp\left(-\dfrac{\tau_v}{\tau_{as}}\right)\exp\left[\dfrac{\tau_v}{\tau_{as}}\exp\left(-\dfrac{t}{\tau_v}\right)\right]\end{array}\right\} \quad (6)$$

where f is the fraction of PQ defects, and τ_{npq} is the time constant for the annealing of the NPQ defects. This modification introduces one more free parameter, τ_{npq}. However, $\tau_{npq} << \tau_{as}$ or τ_v. Hence, it does not mix strongly and only slightly weakens the confidence in determining τ_{as} and τ_v accurately.

The lines in Fig. 1 are Chi-squared nonlinear least squares fits to the data using Eq. (6). One can see that Eq. (6) describes all the annealing curves exceedingly well for the entire annealing time. The values obtained for τ_{as}, τ_v, and τ_{npq} are plotted in an Arrhenius plot in Fig. 3. Over the range of annealing temperatures, τ_{as} and τ_v are comparable in magnitude indicating that the V_{Ga} and As_{Ga} anneal away at similar rates. The annealing activation enthalpies are determined from the slope of the Arrhenius plot. One sees immediately that the activation enthalpy for annealing of V_{Ga} is slightly less than for As_{Ga}. The averaged activation enthalpies for five samples measured are $\Delta H^{as}_m = 2.0 \pm 0.3$ eV, $\Delta H^{v}_m = 1.5 \pm 0.3$ eV, and $\Delta H^{npq} = 1.1 \pm 0.3$ eV. Our values for the activation enthalpies compare favorably with those found in other GaAs materials. Values of 1.2 and 1.6 eV were found for the annealing of defects in electron-irradiated GaAs.[12] In a study of V_{Ga} enhanced mixing of multilayers,[13] the V_{Ga} enthalpy of migration was determined to be 1.7 ± 0.3 eV.

The mechanism of an As_{Ga} hop is equivalent to a V_{Ga} hop in the opposite direction, in effect, swapping sites. V_{Ga} must be present for the As_{Ga} to move. The opposite is not true for V_{Ga} diffusion. In fact for most hops, the V_{Ga} is swapping sites with Ga atoms. Thus, we conclude that the difference in the enthalpy of migration is due to the difference in energy between an As atom and a Ga atom swapping sites with the vacancy. It is energetically more favorable for the Ga atom to swap places with the V_{Ga} rather than for the As atom. A slightly repulsive or attractive potential must exist between the As_{Ga} and V_{Ga} which hinders them from approaching or moving away from each other. It is our opinion that the latter case is true. As isolated defects, they have both opposite charge states and opposite strain fields, thereby attracting each other.

The interaction between the defects explains why annealing "soaks" at low temperature for long times stabilize the As_{Ga}-related defects. At low temperatures, the V_{Ga} can still diffuse through the crystal finding sinks, while the temperature is not sufficient to acti-

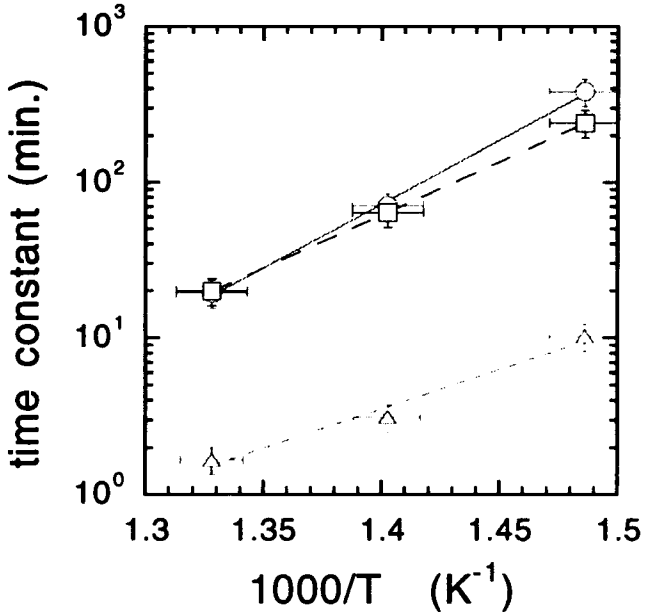

Fig. 3. Arrhenius plot of (o) τ_{as}, (□) τ_v, and (Δ) τ_{npq} determined from the Chi-squared nonlinear least-square fit of Eq. (6) to the isothermal annealing transients. Lines are exponential fits to the parameters giving activation enthalpies for the annealing process. Averaged values are summarized in the text.

vate the As_{Ga} diffusion. Once the V_{Ga} are eliminated, the As_{Ga}-related defects can no longer diffuse. Even when the temperature is elevated to 600°C after a low temperature soak, very little change in the As_{Ga}-related defect concentration is measured. Without the soak, the defect concentration would have been below the detection limit after annealing at 600 °C.

This "stabilization of As_{Ga}-related defects" could be very important for technological applications of LT materials. By tuning the annealing temperature and time, a desired concentration of defects could be stabilized for optimum device performance. Future high temperature processing would not affect the defect concentration.

CONCLUSION

In conclusion, we have investigated the annealing kinetics of As_{Ga}-related defects in LT-GaAs. The lower thermal stability of these defects in LT layers as compared to bulk grown crystals is explained by the enhanced diffusion of As_{Ga} to precipitates via the excess V_{Ga} present in the material. This model is general and could be applied to other damaged GaAs materials containing V_{Ga}. Considering that the supersaturated V_{Ga} concentration must also decrease, a detailed time dependent diffusion model accurately describes the isothermal annealing transients. The difference in activation enthalpy for V_{Ga} and As_{Ga} is interpreted as the energy difference between a Ga atom and an As atom swapping sites with a vacancy. This energy difference can be exploited to stabilize a large concentration of As_{Ga}-related defects against subsequent high temperature processing. This could be technologically important for device applications of LT-GaAs.

ACKNOWLEDGMENTS

Dr. Kam T. Chan is gratefully acknowledged for growing the layers and Professor Shoichiro Tanigawa for performing the positron annihilation measurements. This work was supported by the Director, Office of Energy Research, Office of Basic Energy Sciences, Materials Science Division of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Variable Energy Positron Beam Characterization of Defects in As-Grown and Annealed Low Temperature Grown GaAs

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Variable energy positron annihilation measurements on as-grown and annealed GaAs grown by molecular beam epitaxy at temperatures between 230 and 350°C have been performed. Samples were subjected to either isochronal anneals to temperatures in the range 300 to 600°C or rapid thermal anneals to 700, 800, and 900°C. A significant increase in the S-parameter was observed for all samples annealed to temperatures greater than 400°C. The positron annihilation characteristics of the defect produced upon annealing are consistent with divacancies or larger vacancy clusters. The concentration of as-grown and anneal generated defects is found to decrease with increasing growth temperature.

Key words: LT-GaAs, positron annihilation, vacancy

INTRODUCTION

The molecular beam epitaxy (MBE) growth of GaAs layers at low substrate temperatures (LT-GaAs) was first reported by Murotani et al. in 1978.[1] The as-grown LT-GaAs layers show good crystalline quality with the incorporation of 1 to 2% excess arsenic at growth temperatures as low as 200°C. However, the lattice is highly strained, as demonstrated with x-ray rocking curve measurements which reveal a lattice dilation of about 0.1%, and contains high densities of intrinsic point defects.[2] Upon annealing to 600°C, the LT-GaAs layer becomes highly resistive, exhibits a high breakdown voltage, and gives subpicosecond photoexcited carrier lifetimes.[2] Consequently, these layers are finding a wide variety of applications as insulating buffer layers as well as active layers in opto-electronic devices.

(Received April 12, 1993; revised July 14, 1993)
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Further, the high defect densities found in as-grown and annealed LT-GaAs has stimulated a large amount of scientific interest in these materials. However, the exact nature and concentration of these defects and their relation to the observed properties is still a matter of debate.

A variety of characterization techniques have been applied to as-grown LT-GaAs in order to identify and quantify the defect nature of the material. Electron paramagnetic resonance (EPR) has demonstrated concentrations of the arsenic antisite, in the paramagnetic (i.e., ionized, As^{+}_{Ga}) state, to be in the 10^{18} to 10^{19} cm^{-3} range which suggests the presence of similar concentrations of acceptors.[3,4] The neutral (As^{0}_{Ga}) has been identified by infrared (IR) absorption measurements to be in the 10^{19} to 10^{20} cm^{-3} range.[5] The remaining excess arsenic could be accounted for by the presence of gallium vacancies and/or arsenic interstitials. Ion channeling measurements suggest interstitials are located very close to an As lattice site, possible through the formation of split interstitial

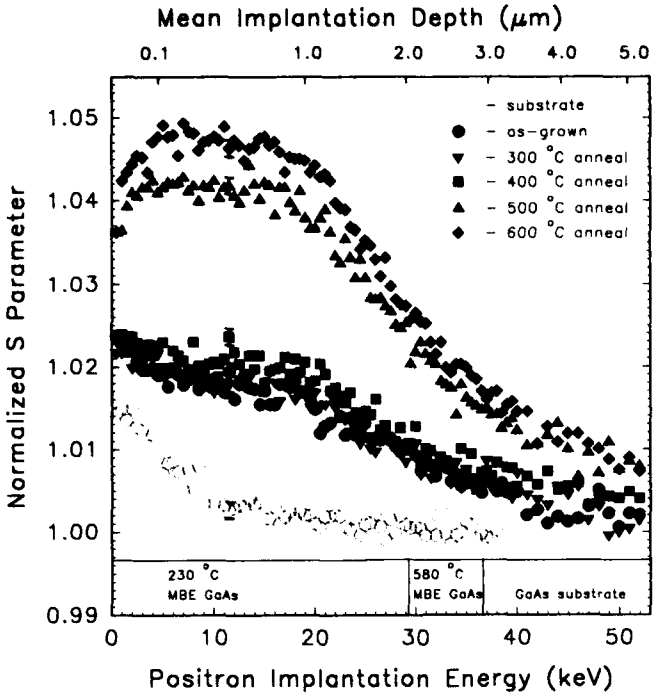

Fig. 1. Normalized S-parameter as a function of positron implantation energy for 15 min isochronal anneals of samples from wafer G975.

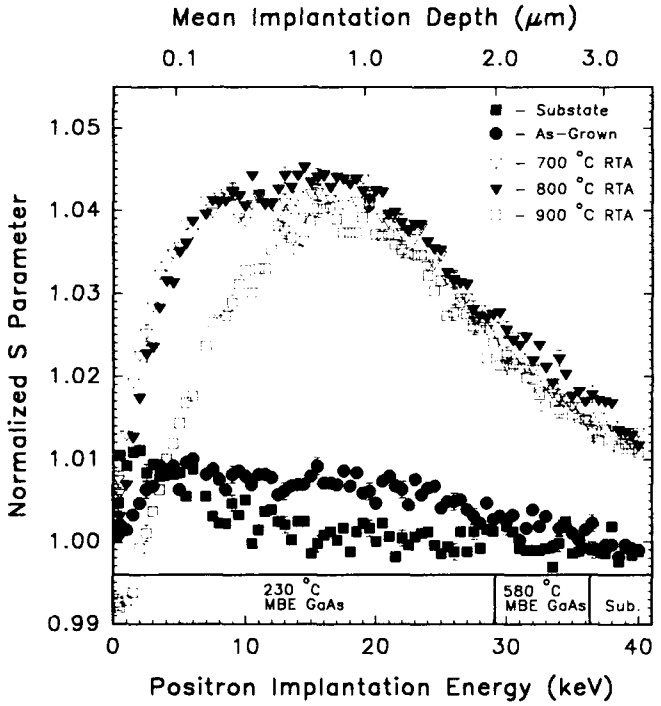

Fig. 2. Normalized S-parameter as a function of positron implantation energy for 60 s RTA anneals of samples from wafer G1034.

pairs.[6] Further, the as-grown material shows essentially no photoluminescence response.[7]

Both EPR and IR absorption demonstrate a reduction of the arsenic anti-site concentration with anneals greater than 400°C to a concentration in the 10^{17} to 10^{18} cm^{-3} range following a 600°C anneal. Annealing at 600°C also results in a relaxation of the lattice parameter to the bulk value accompanied by an increase in resistivity to ~10^6 Ωcm. Further, transmission electron microscopy (TEM) has demonstrated the formation of arsenic precipitates with an average diameter of approximately 5 nm and a concentration of $10^{17}cm^{-3}$ at the 600°C anneal temperature.[8] Increasing the anneal temperature has been shown to increase the diameter of the precipitates.[9]

In this paper, we report the results of variable energy positron annihilation studies of as-grown and annealed LT-GaAs. Positrons implanted into a condensed medium thermalize in a few picoseconds then diffuse until they annihilate with an electron. Annihilation can occur from either a free or a localized positron state, such as is produced by trapping into a bulk defect. The most probable annihilation event results in the production of two 511 keV γ-rays. The momentum of the electron-positron pair is nonzero and dominated by the electron contribution. This results in a deviation from colinearity for the two emitted γ-rays or, equivalently, in the Doppler broadening of the energy spectrum. The energy spectrum is commonly analyzed in terms of a lineshape parameter, the S-parameter defined as the ratio of the number of counts in a central region to the total. An increase in annihilations with low-momenta valence electrons would result in an increase in the S-parameter. Annihilation from trapping sites associated with open volume defects, due to the absence of ion cores, is manifested as an increase in the S-parameter from its value in "defect-free" bulk material, S_B.

EXPERIMENTAL PROCEDURES

All samples used in this study were prepared in a Varian GEN II MBE system at a growth rate of approximately 1 μm/h. A wafer holder was used and the growth temperature monitored with a thermocouple. The As_4 and Ga beam flux measurements were taken with an ionization gauge at the wafer position and a beam equivalent pressure (BEP) ratio calculated. Five wafers were grown to a thickness of 2 μm on a 580°C grown undoped GaAs buffer layer using either horizontal Bridgman (HB) or liquid-encapsulated Czochralski (LEC) (100) GaAs substrates. Hereafter, wafers denoted as G975 and G1034 were grown at 230°C with a BEP of 8.5. Wafers G1042, 1043, and G1044 were grown at 230, 280, and 350°C, respectively, using a BEP of 20.

Wafers G975, G1042, G1043, G1044 were sectioned and the pieces subjected to 15 min isochronal anneals at 300 to 600°C in flowing Ar with GaAs proximity wafers. Wafer G1034 was sectioned with three samples rapid thermal annealed (RTA) at 700, 800, and 900°C for 60 s, one sample was annealed at 600°C for 1 h in the MBE machine using an As overpressure and one was subjected to a 600°C proximity wafer anneal outlined above. Variable energy positron annihilation experiments were carried out using a slow beam described elsewhere.[10] The positron implantation energy was varied from 0.5 to 50 keV with 10^6 counts recorded at each implantation energy. The energy range used to define the S-parameter was 510.25 to

511.75 keV for the central region and 503.8 to 517.2 keV for the total.

RESULTS

The S-parameter vs positron implantation energy for the annealing stages performed on wafer G975 are shown in Fig. 1. The implantation depth scale shown on this and similar figures has been calculated from the parameters determined by Halec et al.[11] The S-parameter is normalized to the bulk S parameter, S_B, measured from the substrate material. The as-grown to 300°C annealed material show essentially the same increase in S-parameter above the bulk value, $S = 1.018\, S_B$. A very slight increase is observed for the 400°C annealed sample, however, a significant increase is seen for samples annealed to 500 and 600°C. A GaAs substrate (HB) was also subjected to 15 min isochronal anneals to 500 and 600°C with no increase in S observed. Measurements were also completed on lump arsenic metal. An S-parameter value of 1.018, normalized with respect to HB GaAs substrate material, was obtained for arsenic.

The results of the RTAs performed on wafer G1034 are shown in Fig. 2. The figure indicates that RTAs also produce a significant increase in S-parameter from the as-grown value. Figure 3 compares the effects of 600°C anneals performed with proximity wafer and MBE As overpressure methods along with the 700°C RTA on samples from wafer G1034. In all cases, a large increase in S with respect to as-grown was observed, however, a slightly lower value results from the proximity wafer method.

The results of the averaged S-parameter from the LT layer for as-grown and 600°C annealed samples are shown in Fig. 4. Data from wafers grown with a BEP = 20 at growth temperatures of 230 (G1042), 280 (G1043) and 350°C (G1044) along with a BEP = 8.5 and a growth temperature of 230°C (G1034) are given.

DISCUSSION

The observation of an increase in S-parameter within LT-GaAs layers upon annealing to 600°C has been reported previously.[12,13] Keeble et al. demonstrated that the dominant positron trap present after annealing above 500°C is physically distinct from the as-grown defects.[13] The S vs implantation energy data presented here for similar BEP 8.5 samples, as well as material grown at higher BEP, and annealed via different methods confirm the generation of new positron trapping defects in samples annealed to temperatures greater than 400°C. Further, the observation of the defect after 60 s RTA treatments suggests rapid formation. When the effects of positron diffusion are considered, the measurements presented here suggest a homogenous distribution of defects in the LT-GaAs layers. The apparent decrease in S for the 900°C RTA compared to the 800°C anneal may be due to changes within the GaAs surface.

The normalized S-parameters obtained for LT-GaAs layers annealed to 600°C are similar to those reported for positron trapping at vacancy clusters.[14] The concomitant increase in positron trapping with arsenic precipitate formation may lead to speculation on their effectiveness as positron traps. The S-parameter from highly defected lump arsenic metal would be expected to form an upper limit for such annihilations. However, the experimental value of 1.018 obtained is significantly lower than the approximately 1.04 value

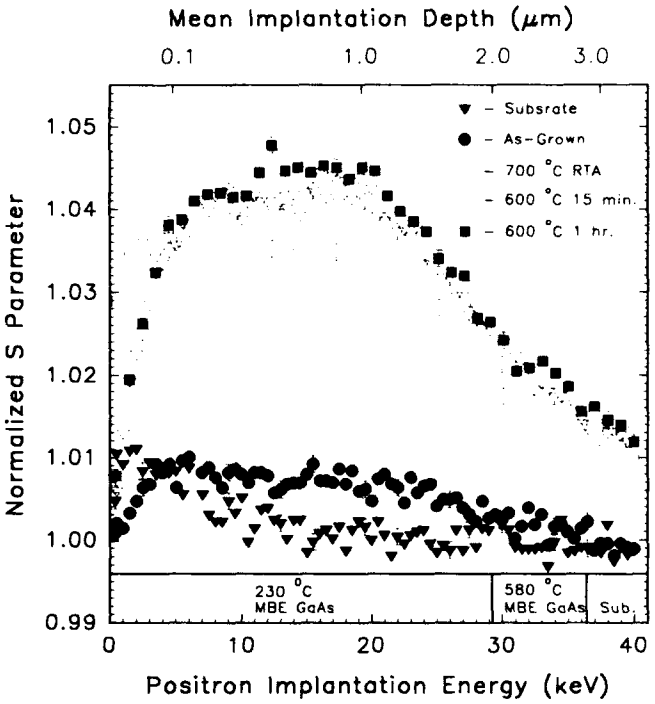

Fig. 3. Normalized S-parameter as a function of positron implantation energy for several anneal techniques on samples from wafer G1034.

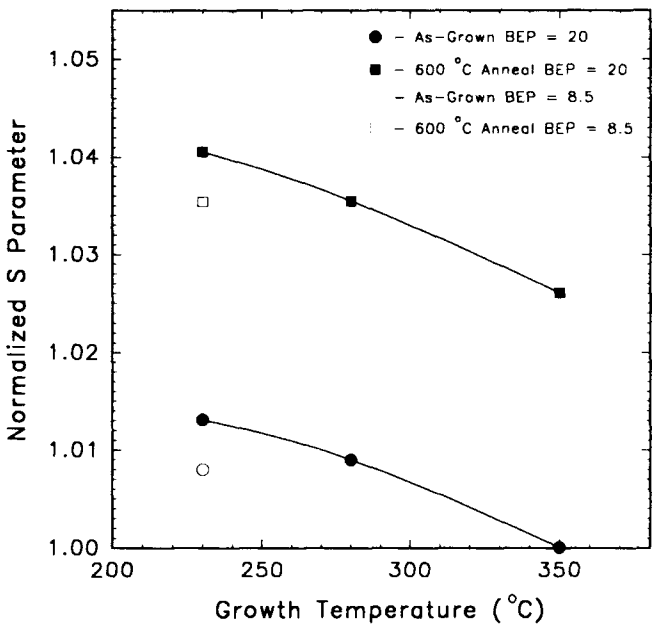

Fig. 4. Normalized S-parameter of the LT-GaAs layer as a function of growth temperature for as-grown and 600°C annealed samples. Samples from wafer G1034 are included to illustrate the effect of BEP. (Lines are drawn to guide the eye only.)

commonly observed in our samples with the anneal induced defects.

Figure 4 shows that increasing growth temperature decreases the defect content for both the as-grown and annealed LT-GaAs layers. The observed large increase in S-parameter for the 350°C (G1044) grown sample suggests that high concentrations of vacancies in the as-grown material are not required for the formation of the anneal induced defect.

CONCLUSIONS

As a result of a series of anneal experiments on MBE GaAs grown at temperatures from 230 to 350°C, it is concluded that a positron trapping defect has formed on annealing to 600°C. From variable temperature anneal experiments on 230°C grown samples, it is concluded that the onset of defect formation is in the region of 400°C.

From the magnitude of the observed increase in S-parameter with respect to the substrate, approximately 4%, and the experiments on defected lump arsenic metal, it is concluded that the positron trap formed upon annealing LT-GaAs to temperatures greater than 400°C is a vacancy duster type defect. These defects appear to be uniformly distributed throughout the layer.

ACKNOWLEDGMENTS

The authors would like to express their gratitude to B. Nielsen, Brookhaven National Laboratory for helpful discussions throughout the course of this investigation. Work at Brookhaven National Laboratory was supported by the U.S. Department of Energy Division of Materials Science, under contract No. DE-76CH00016. Work performed at U.S. Army Research Laboratory, Electronics and Power Sources Directorate.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Lateral and Vertical Isolation by Arsenic Implantation into MOCVD-Grown GaAs Layers

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We have demonstrated the formation of arsenic precipitates in GaAs using arsenic implantation and annealing. Electrical measurements show that very high resistivity (surface or buried) GaAs layers can be produced by this method. The arsenic-implanted materials are similar to GaAs:As buffer layers grown by low-temperature molecular beam epitaxy, which are used for eliminating backgating problems in GaAs circuits. Arsenic implantation is a nonepitaxial process which is compatible with current GaAs technology. Formation of insulating GaAs layers by this technique may improve the performance and packing density of GaAs integrated circuits, leading to advanced novel III-V compound-based technologies for high-speed and radiation-hard circuits.

Key words: Arsenic implantation, arsenic precipitates, GaAs insulating layers, high packing density

INTRODUCTION

The performance of GaAs-integrated circuits has been limited by backgate or sidegate effects which can lead to undesirable crosstalk between neighboring devices and impose limits on device packing density. Many performance improvements, including elimination of backgating, have resulted from incorporating a GaAs buffer layer grown at low temperature (LT) by molecular beam epitaxy (MBE).[1] Molecular beam epitaxially grown LT buffer layers exhibit high electrical resistivity and a breakdown strength about ten times that of semi-insulating (SI)-GaAs.[2-4] High resistivity has been attributed to the high density of arsenic precipitates which appear after annealing at 600°C for ten minutes.[5]

One dominant characteristic of GaAs buffer layers grown by LT-MBE is an excess of arsenic. We have used arsenic implantation and annealing to increase arsenic's concentration above the stoichiometric level and have demonstrated the formation of arsenic precipitates in GaAs by this method.[6] Electrical and material characterization of arsenic-implanted GaAs were similar to those from low-temperature MBE-grown and annealed GaAs:As buffer layers.

Our preliminary measurements indicate that very high resistivity surface or buried GaAs layers can be produced by arsenic implantation and annealing. Commercial processing for III-V compounds relies heavily upon SI-substrates and ion implantation to fabricate integrated circuits. Thus, arsenic implantation could be easily incorporated into processing to prevent crosstalk in GaAs circuits. In this paper, we report preliminary results of the breakdown voltage for test structures fabricated on n^+ GaAs grown epitaxially on SI substrates.

EXPERIMENTAL PROCEDURE

In most GaAs device applications, SI substrates are used for epitaxial growth of GaAs by MBE or metalorganic chemical vapor deposition (MOCVD); however, leakage at the interface of epilayers and SI

(Received April 12, 1993)

substrates is frequently observed.[7] Metalorganic chemical vapor deposition was used to grow n^+ epilayers with thicknesses ranging from 0.2 to 1.5 μm on two inch SI and n^+ GaAs substrates with 2° off(100) toward [110] orientations. We used a growth temperature of (typically) 650°C and doped the epilayer with silicon using SiH_4 gas.

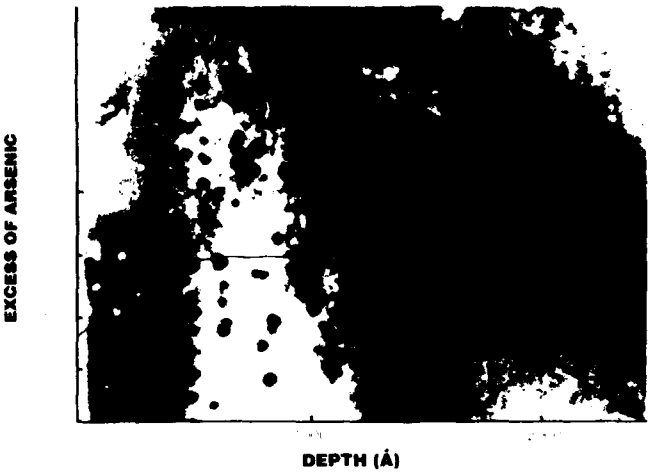

Fig. 1. Cross-section transmission electron microscopy shows formation arsenic precipitates in undoped GaAs sample implanted with 1×10^{16} As at 200 keV and annealed at 600°C for 30 min. Variation in shading of precipitates is due to over/under-focusing conditions produced by the finite thickness of film.

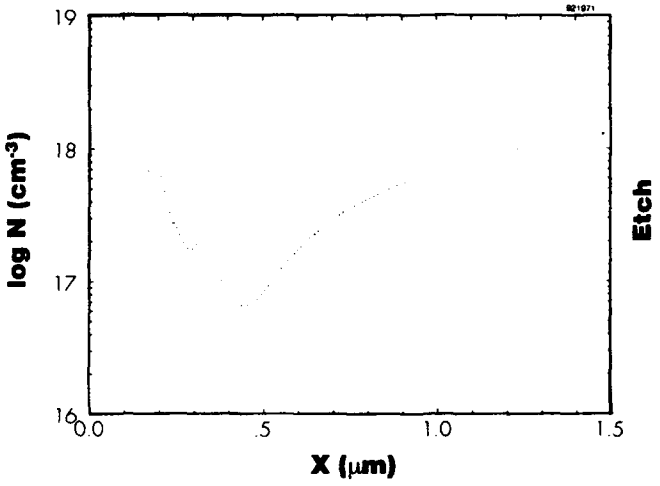

Fig. 2. Polaron profiling results of n^+ substrate of about 10^{18} As/cm³, implanted at 400 keV.

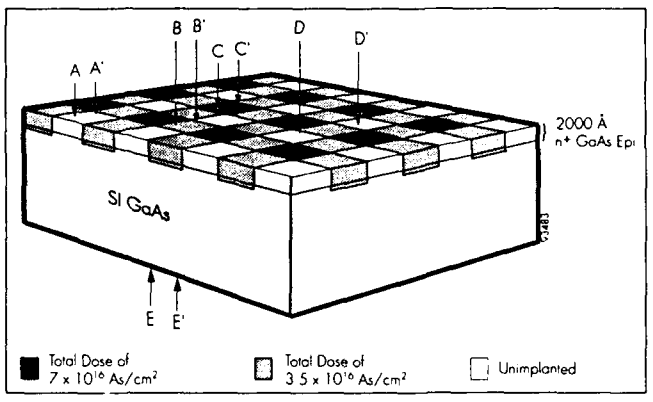

Fig. 3. Schematic of the test structure used to evaluate the electrical isolation quality of arsenic-implanted GaAs buffer layers.

Arsenic implantation was carried out at room temperature with energies of 180 to 400 keV. Implantation dose and energy were chosen to ensure that the resulting excess concentration in the layer, defined as $(N_{As} - N_{Ga})/(N_{Ga} + N_{As})$, reached a maximum of about 1–2%. These samples were annealed in an in-house MOCVD reactor at 600°C, using an AsH_3 ambient, for periods of 10 to 30 min.

EXPERIMENTAL RESULTS

A cross-sectional transmission electron microscopy (XTEM) micrograph, shown in Fig. 1, clearly reveals the formation of arsenic precipitates by arsenic implantation and annealing. The XTEM micrograph depicts a sample implanted with a dose of 1×10^{16} As/cm² at 200 keV and subsequently annealed at 600° for 30 min. Superimposed on this XTEM is a simulation of arsenic implantation generated by the Monte-Carlo code TRIM 91. Examination of Fig. 1 shows small arsenic precipitates (20–30Å) from the surface to a depth of about 2000Å. Results clearly demonstrate the formation of arsenic precipitates similar to those produced by LT-GaAs grown by MBE. High resolution XTEM results indicate that the density and size of arsenic precipitates can be controlled by varying implantation dose and annealing time.[8]

Capacitance-voltage (C-V) profiling was performed to detect changes in carrier concentration which occurred as a result of arsenic implantation and annealing. Polaron profiling of an n^+ substrate implanted at 400 keV (shown in Fig. 2) indicated a decreased carrier concentration which agreed reasonably well with the TRIM simulation. The implants that were incorporated into the n^+ material (on the order of 1×10^{18} As/cm³) had a depletion region that was very thin (~300Å). Since the size of the depletion spheres around the arsenic precipitates are a function of the host material (e.g., the more conductive the host material, the smaller the spheres), a very dense population would be required to deplete the material fully. We expect a more drastic depletion to occur if we implant arsenic into a less conductive GaAs substrate.

Figure 3 shows a schematic of the test structure used to study lateral and vertical isolation in GaAs wafers. An epitaxial n^+ GaAs layer about 2000Å thick was grown on a SI-GaAs substrate and implanted with arsenic using a shadow mask. The wafers were annealed for 30 min at 600°C in an arsine (AsH_3) ambient. This structure aimed to produce lateral isolation between the unimplanted n^+-regions.

The insulating behaviors of unimplanted and arsenic-implanted n^+ GaAs layers were measured and compared by contacting two metal probes at different regions of the samples and measuring the current-voltage (I-V) characteristics on a curve tracer. The ac bias was gradually increased to the point of catastrophic breakdown, whereby a large current could be measured between the two probes. The I-V characteristics were recorded before and after breakdown.

Figures 4 through 7 show I-V characteristics measured from each sample. Figure 4 shows the I-V characteristics measured between points A and A′ on an n^+ GaAs region without arsenic implantation. This I-V curve shows a turn-on voltage of about five volts with no apparent breakdown, as expected from the unimplanted semiconducting region. Figure 5 shows I-V characteristics measured between points B and B′ on an arsenic-implanted n^+ GaAs region. Current-voltage characteristics from this region indicate a highly resistive material with a breakdown voltage higher than 1000 V. The maximum applied voltage (1600 V) available from the curve tracer was not sufficient to cause a breakdown in the implanted film. Results clearly demonstrate the possibility of creating highly resistive buffer layers by arsenic implantation for lateral isolation between two adjacent GaAs device regions.

To test the vertical isolation in arsenic-implanted samples, we applied an ac voltage between 1) point E and point A on the unimplanted n^+ region (Fig. 6) and 2) point E and point C on the implanted region (Fig. 7). In Fig. 6, the value of breakdown voltage across the unimplanted test structure is estimated at about 100 V (V_{EA} = 100 V). In Fig. 7, the breakdown voltage across the test structure with an arsenic-implanted layer appears to be higher than 1000 V (V_{Ec} > 1000 V). By calculating the difference between these breakdown voltage values ($V_{Ec} - V_{EA}$), we estimate that a voltage of at least 900 V is required to cause a breakdown in the arsenic-implanted layer. Subsequently, the breakdown electric field strength of the layer was estimated to be about 4.5×10^7 V/cm. This relatively high breakdown field strength clearly indicates that the arsenic-implanted GaAs layer is highly resistive and has insulating properties comparable to those of high quality dielectrics.

SUMMARY AND CONCLUSION

We have demonstrated the formation of arsenic precipitates in GaAs by arsenic implantation and annealing. Our results are similar to those of low-temperature GaAs:As grown by MBE. High resolution XTEM data show the formation of arsenic precipitates 20–100Å in size. Experimental results indi-

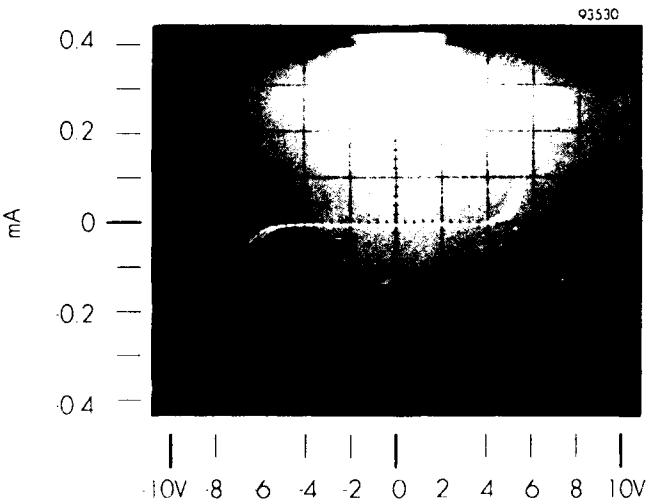

Fig. 4. Lateral breakdown between points A and A′ on an unimplanted n^+-type GaAs region.

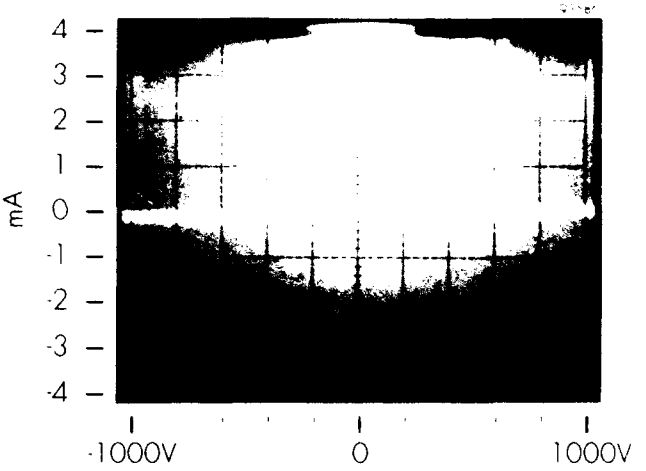

Fig. 5. Lateral breakdown between points B and B′ on an implanted n^+-type GaAs region.

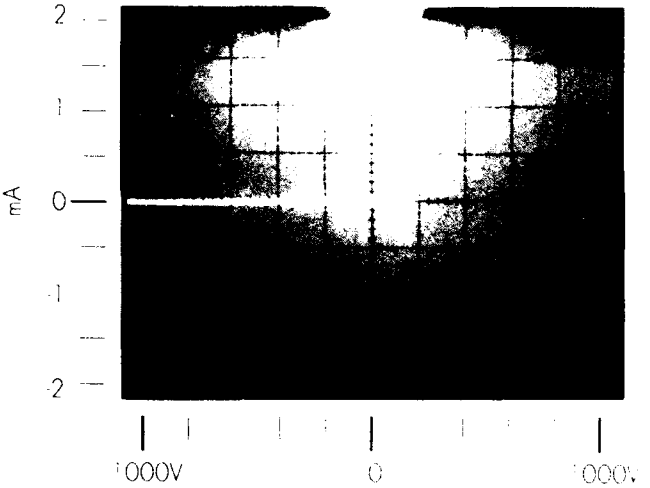

Fig. 6. Vertical breakdown between points A and E on the unimplanted n^+ layer and SI substrate, respectively.

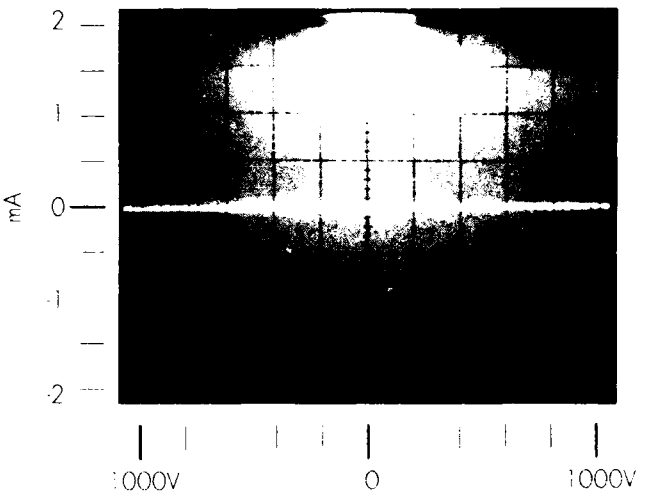

Fig. 7. Vertical breakdown between points C and E on the implanted region and the SI-GaAs layer, respectively.

cate that the density and size of arsenic precipitates can be controlled by varying implantation dose and annealing time, respectively. Electrical results clearly demonstrate that very high resistivity surface or buried GaAs layers can be produced by arsenic implantation and annealing. These regions can provide lateral and vertical isolation in GaAs device structures.

Our research grew out of the need to eliminate sidegating and backgating in GaAs devices requiring semi-insulating layers. However, we have also discovered that arsenic implantation and annealing can be used to improve the quality of individual devices and enable the advancement of new GaAs-based technologies. Through surface passivation, arsenic implantation can reduce gate-to-drain leakage in GaAs-based metal semiconductor field-effect transistors (MESFETs) and high electron mobility transistors. In addition, high resistivity thin surface layers produced by arsenic implantation may be used as gate insulators for GaAs-based metal-insulator (MIS)FETs. Such gate insulators may lead to the development of a novel GaAs-based complementary metal-insulator-semiconductor technology analogous to the advanced silicon-based complementary metal-oxide semiconductor technology. The insulators will offer added advantages of higher radiation hardness and operational speed. Arsenic implantation and annealing can also provide lateral isolation for vertical cavity laser diodes.

ACKNOWLEDGMENTS

We are grateful to Mr. Sam DiVita for his continued support and encouragement of this work. We would also like to acknowledge A. Cremins and S.E. Passmore for their assistance with the preparation of this manuscript. This work was supported in part by the U.S. Department of Defense, U.S. Army CECOM, under Contract No. DAAB07-92-C-B255.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Precipitation of Arsenic in Doped GaAs

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Precipitation processes in the p-type, n-type, and intrinsic GaAs layers grown by molecular beam epitaxy at a low temperature were studied by transmission electron microscopy. The average spacing, average diameter, and volume fraction of precipitates were measured as a function of the annealing time for the annealing temperature of 700°C. Volume fractions of precipitates are nearly constant in each layer over the period of annealing, implying that the precipitation process has reached the coarsening stage in the annealing times used in the study. The volume fraction of precipitates in the n-type layer is about a half of those in the p-type and intrinsic layers, suggesting that the incorporation rate of excess As into the n-type layer during the growth is lower than those into the p-type and intrinsic layers. Despite a large difference of amounts of excess As in as-grown n-type, p-type, and intrinsic layers, the average spacings and, hence, number densities of precipitates in three layers are nearly identical for each of the annealing conditions.

Key words: Arsenic, LT-GaAs, precipitation

GaAs epilayers grown by molecular beam epitaxy (MBE) at low substrate temperatures (200–250°C) were found to contain 1–2% excess arsenic.[1] Upon annealing at high temperatures, excess arsenic atoms form precipitates of the elemental arsenic phase.[2] The formation of arsenic precipitates during the annealing results in changes in material properties from those due to point defects (As interstitials and As antisites) to those due to the internal Schottky barriers associated with the arsenic precipitates.[3,4] A number of new electronic properties[5–7] as well as novel precipitation phenomena[8,9] have been observed from these GaAs layers containing As precipitates. As such observations, earlier studies found strong effects of impurity doping on precipitation processes of As in GaAs.[10–13] In the p-n junction with Be and Si as dopants, excess As atoms migrate toward the n-type region, forming higher density precipitates in the n-type region than in the p-type region.[11] A particularly interesting observation made in that study is a direct correlation of the precipitate distribution with the electron states, i.e., Fermi level positions, which suggests that the precipitation process in doped GaAs may have fundamental differences from the conventional ones observed in metal systems. In this paper, we present a quantitative study of the precipitation processes in doped and intrinsic GaAs layers grown by MBE at a low temperature. In order to investigate the precipitation process in each layer without effects of migrations of excess As atoms from neighboring layers, thick n-type, p-type, and intrinsic layers were grown with a thin AlGaAs layer at each boundary.

(Received April 12, 1993)

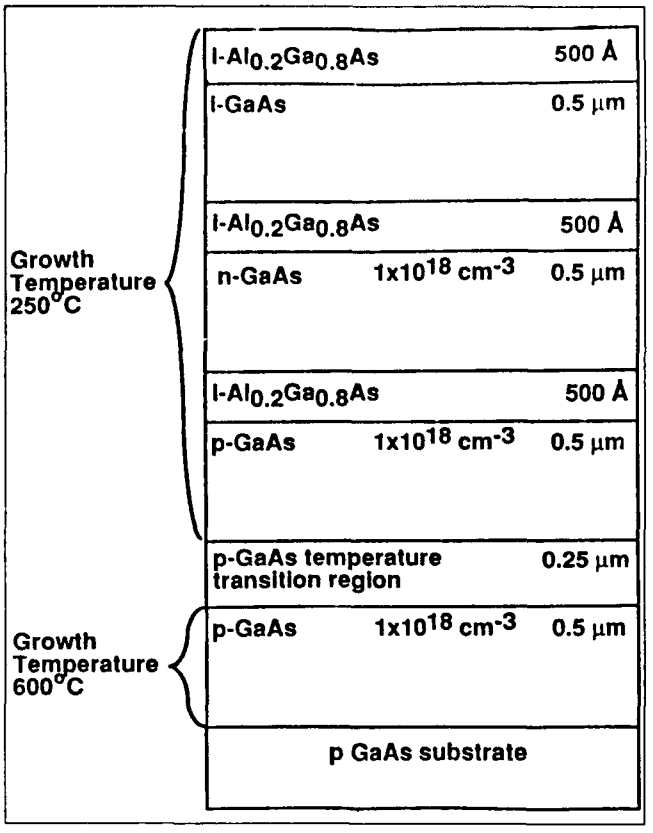

Fig. 1. Configuration of the p-n-i layer structure.

Fig. 2. (111) dark field image of the p-type region in the sample annealed at 700°C for 3 h.

The p-n-i layer structure used in this study was grown in a Varian GEN II MBE system. The configuration of the structure is shown in Fig. 1. The arsenic flux used was the dimer As_2, and Si and Be were used for the n-type and p-type dopants. All layers were grown at 250°C with a rate of 1 μm/h with a group V to group III beam-equivalent-pressure ratio of 20. The p-n-i layer structure was cut into a number of pieces and annealed at 700°C in an Ar gas flow for four different times, 5 min, 30 min, 3 h, and 10 h.

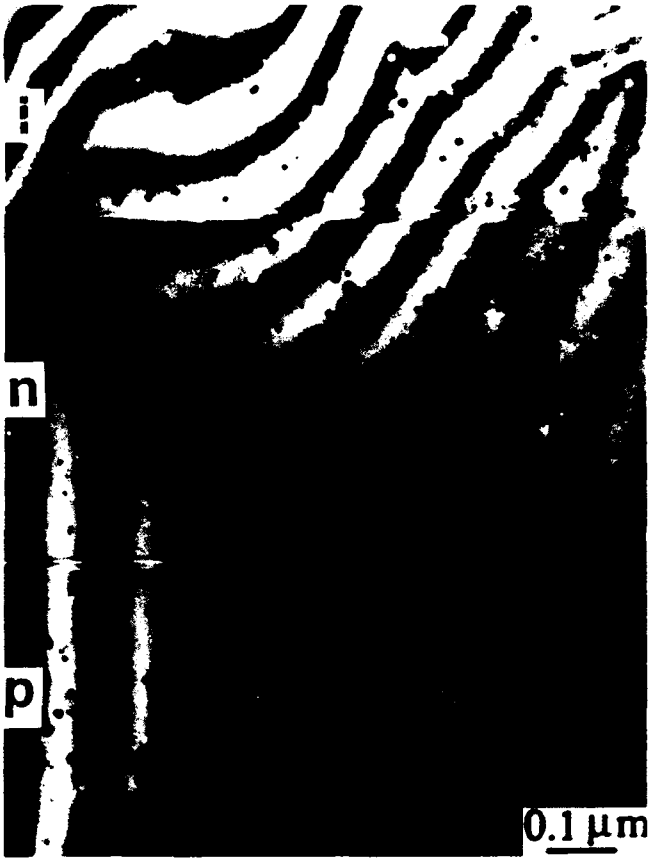

Fig. 3. (111) dark field image of the p-n-i layer structure annealed at 700°C for 10 h.

Transmission electron microscope (TEM) images of precipitates in annealed samples were obtained by observing cross-sectional specimens with a JEM 2000EX electron microscope. For the quantitative analysis of precipitate distributions, 111 and 220 dark field images were taken under the two-beam condition from each annealed sample.

The average diameter of precipitates was estimated by measuring sizes of nearly 200 precipitates in each region by using an Eyecon image analyzer. For this measurement, dark field images were taken at a magnification of 100, 000, and a diameter of each precipitate was determined by measuring two orthogonal directions and obtaining their average value. At this magnification, the majority of precipitates exhibit clear boundaries with the matrix in negatives of images. Figure 2 is an example of the image used for the measurement of precipitate diameters. The frequency distribution of precipitate diameters in each sample forms a single peak with the peak value being close to the average value. The standard deviations of measured diameters with respect to the average values, which correspond to broadening of peaks of frequency distributions, range from 11 to 23Å among samples. The average spacings of precipitates were determined by counting a number of precipitates in an area along an equal thickness contour of a dark field image. The volume of the area was estimated by using the extinction distance of the reflection used.

For each region, the average spacings of ten different areas were measured. The standard deviation of the average spacings obtained from ten areas ranges from 13 to 32Å. The number of precipitates in one measured area and the volume of the area are typically 15 and 2×10^9 Å^3, respectively. Volume fractions of precipitates were calculated by using the average diameters and the average spacings. Measured volume fractions may be significantly smaller than absolute values of volume fractions because of invisibility of a certain portion of precipitates in dark field images. In order to examine such a possibility, we have taken several dark field images using different reflections from the same area. By comparing those images, we found that almost all precipitates are visible in these dark field images although their contrasts vary from one image to another. Only a small portion of precipitates (a few percent) were found to be invisible when they were located at the centers of a dark thickness contours. The measured volume fractions of precipitates, therefore, are very close to the absolute values. We also would like to note that the imaging condition was kept identical in observations of all samples. The aforementioned problem, therefore, is not expected to affect the main findings of the present study.

Figure 3 is a 111 dark field image taken from the sample annealed at 700°C for 10 h. The image shows that sizes of precipitates in the n-type region are smaller than those in the p-type and intrinsic regions. Table I lists the average diameters of precipitates in three regions for four annealing times. It is seen from the table that the average diameter increases with increasing the annealing time in each region. For each annealing time, the average diameters of the p-type and intrinsic regions are close to each other, while that of the n-type region is significantly smaller than the others. Table II lists the average spacings of precipitates in three regions for four annealing times. In all regions, the average spacings increase with increasing the annealing time. The important point shown by this table is the nearly identical average spacings in three regions for each annealing time. The differences among the three regions are smaller than the standard deviations of measured values.

Table III lists volume fractions of precipitates. For each region, the volume fraction remains almost constant among different annealing times except for those of the p-type and intrinsic regions annealed at 5 min. The large deviation of these two values, 0.36 and 0.37%, from others is believed to be due to the difficulty in measuring precipitate diameters in the annealed samples where precipitates are still very small. The nearly constant volume fractions among four annealing times indicate that the precipitation process has already reached the coarsening stage in the 5 min annealing at this annealing temperature. This also implies that volume fractions of precipitates correspond to amounts of excess As in the as-grown layers because the nonstoichiometry of the matrix at the coarsening stage is considered to be close to the nonstoichiometry of the crystal under the equilibrium condition. Volume fractions listed in Table III, hence, suggest that the amount of excess As in the n-type region is about a half of those in the p-type and intrinsic regions. There may be the possibility that all three regions originally have nearly identical amounts of excess arsenic but a smaller portion of excess arsenic has changed into precipitates in the n-type region than in the other two regions, leaving a significant amount of excess arsenic in the matrix of the n-type region. This possibility, however, is very unlikely because it implies that the Si-doped GaAs can have a significant degree of nonstoichiometry toward the As-rich side under the equilibrium condition. The smaller incorporation of excess As into the n-type layer may be explained by considering that excess As atoms become deep donors in GaAs.[11] The incorporation of a deep donor into the n-type region requires a greater energy than into the p-type and intrinsic regions. Smaller sizes of precipitates in the n-type regions than those in the p-type and intrinsic regions may be attributed to the difference in the amount of excess As and, hence, the difference of degrees of supersaturations in as-grown layers.

There are two important findings in the present study which require further examinations. The first one is nearly identical average spacings or nearly identical number densities of precipitates in three

Table I. Average Diameters of Precipitates in Three Regions for Four Annealing Times

Anlg. Time	Region		
	N-Type GaAs	P-Type GaAs	Intrinsic GaAs
5 min	52Å	68Å	70Å
30 min	64Å	79Å	79Å
3 h	73Å	90Å	88Å
10 h	82Å	102Å	103Å

Table II. Average Spacings of Precipitates in Three Regions for Four Annealing Times

Anlg. Time	Region		
	N-Type GaAs	P-Type GaAs	Intrinsic GaAs
5 min	357Å	356Å	364Å
30 min	447Å	439Å	442Å
3 h	491Å	504Å	490Å
10 h	557Å	560Å	568Å

Table III. Volume Fractions of Precipitates in Three Regions for Four Annealing Times

Anlg. Time	Region		
	N-Type GaAs	P-Type GaAs	Intrinsic GaAs
5 min	0.16%	0.36%	0.37%
30 min	0.15%	0.31%	0.30%
3 h	0.17%	0.30%	0.31%
10 h	0.16%	0.32%	0.31%

regions at each stage of the annealing. The close matching of average spacings at all four annealing times suggests that the matching is not merely accidental but results from a novel mechanism underlying the precipitation process in doped GaAs. The other finding is the rate constants of coarsening which correspond to a slope of the linear relation of the cube of average radius with the annealing time.[14] The rate constant of the n-type region is smaller than those in the p-type and intrinsic regions. This result forms a distinct contrast to the case of As precipitation in thin p-n junctions.[11] In thin p-n junctions, precipitates grow more rapidly in the n-type region at the expense of precipitates in the p-type region through migration of excess As atoms across the junction. The analysis of these two results will be reported in a separate paper.

ACKNOWLEDGMENT

This work has been supported by the U.S. Air Force Office of Scientific Research Contract No. F49620-93-1-0031.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Electrical Characteristics of Low Temperature-$Al_{0.3}Ga_{0.7}As$

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In this work, we present electrical characterizations of n^+ GaAs/low temperature (LT)-$Al_{0.3}Ga_{0.7}As$/n^+ GaAs resistor structures in which the LT layers are grown at nominal substrate temperatures of 250 and 300°C. The resistivity and V_{tfl} parameters of these LT-$Al_{0.3}Ga_{0.7}As$ layers are compared with those of LT-GaAs and $Al_{0.3}Ga_{0.7}As$ grown at a normal growth temperature of 720°C. Low-temperature $Al_{0.3}Ga_{0.7}As$ layers exhibit resistivities as high as 10^{12} ohm-cm, nearly four orders of magnitude higher than that of LT-GaAs, and V_{tfl} values as high as 45 V, over twice that of LT-GaAs. We also find that the LT-$Al_{0.3}Ga_{0.7}As$ materials grown at 250 and 300°C appear to show opposite and contradictory trends with respect to resistivity and V_{tfl}. We propose that this result can be explained by residual hopping conduction in the 250°C material. Temperature dependent conductivity measurements confirm the presence of a hopping mechanism in LT-$Al_{0.3}Ga_{0.7}As$ grown at 250°C and yield activation energies of 0.77 and 0.95 eV for LT-GaAs and LT-$Al_{0.3}Ga_{0.7}As$, respectively.

Key words: Hopping conduction, low-temperature-grown AlGaAs, MBE

INTRODUCTION

The electrical properties of low temperature (LT)-GaAs have been extensively characterized. The high resistivity ρ and trap-filled limited voltage V_{tfl} exhibited by such layers have led to their use in a variety of device applications, most notably as a buffer layer to prevent backgating in GaAs metal-semiconductor field effect transistors[1] and as a gate insulator in GaAs metal-insulator semiconductor field-effect transistors (MISFETs).[2] Low temperature-AlGaAs layers have been shown to exhibit even higher resistivity than LT-GaAs,[3] and have also found some device applications, specifically in LT-GaAs/AlGaAs superlattices.[4] In general, however, the trap characteristics and corresponding electrical properties of these layers are yet to be fully characterized. Specifically, the trap-filled limited voltage V_{tfl} has not, to our knowledge, been examined for this material. This parameter has been shown to be a measure of the feasibility of a trap-filled layer as a MISFET gate insulator.[5]

In this work, we present electrical characterizations of n^+ GaAs/LT-$Al_{0.3}Ga_{0.7}As$/n^+ GaAs resistor structures in which the LT layers are grown at nominal substrate temperatures of 250 and 300°C. We compare the ρ and V_{tfl} of these layers with those of LT-GaAs and $Al_{0.3}Ga_{0.7}As$ grown at a normal growth temperature of 720°C. In addition, we have made temperature dependent conductivity measurements on LT-GaAs and AlGaAs resistor structures to determine the activation energies of their dominant trapping centers. Finally, we discuss implications of our results for the suitability of LT-AlGaAs layers in several device applications.

EXPERIMENT

The n-i-n test structures considered in this study have been fabricated using a Varian Modular Gen II

(Received April 12, 1993)

Table I. Sample Inventory

Sample	Layer x
543, 583	LT-$Al_{0.3}Ga_{0.7}As$;T_{sub} = 250°C
542, 558	LT-$Al_{0.3}Ga_{0.7}As$;T_{sub} = 300°C
585	Normal $Al_{0.3}Ga_{0.7}As$;T_{sub} = 720°C
677	LT-GaAs;T_{sub} = 250°C

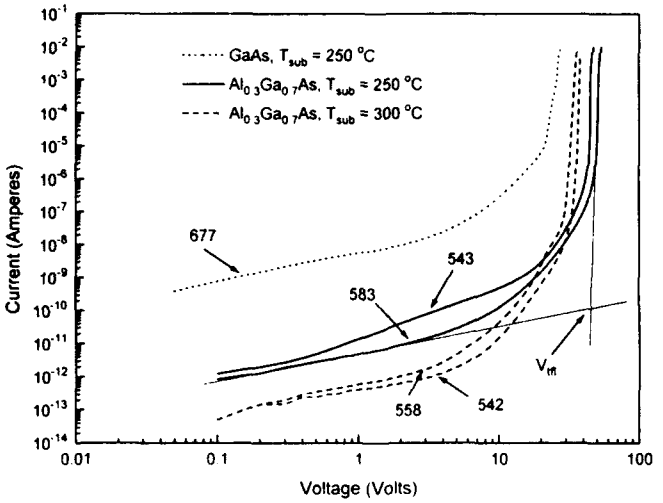

Fig. 1. Log-log current-voltage characteristics for LT-$Al_{0.3}Ga_{0.7}As$ and LT-GaAs samples.

Table II. Summary of Electrical Characteristics

Sample	ρ (V = 0.5V)	V_{tfl}
543	7.7×10^{10} Ω-cm	43.6 V
583	2.2×10^{11} Ω-cm	45.6 V
542	4.0×10^{12} Ω-cm	32.1 V
558	2.0×10^{12} Ω-cm	26.3 V
585	1.2×10^{10} Ω-cm	0.50 V
677	1.8×10^{8} Ω-cm	18.6 V

MBE chamber. Growth substrates were attached to molybdenum blocks using indium-free wire mounting. All samples were grown on n^+ GaAs substrates, and consist of 0.5 μm of normal epitaxial n^+ GaAs, followed by 1.0 μm of the material of interest (layer x), and capped with 0.5 μm of normal n^+ GaAs. The arsenic species used was As_4. An inventory of the samples grown and their corresponding x layers is given in Table I. Note that two $Al_{0.3}Ga_{0.7}As$ samples were grown at 250 and 300°C, respectively, to ensure reproducibility of results. The normal $Al_{0.3}Ga_{0.7}As$ layer grown at 720°C and the LT-GaAs layer were included for comparison. The purpose of the top n^+ GaAs layer in the sample structure is twofold: it provides a layer for ohmic contact; moreover, the growth of this layer at a nominal substrate temperature of 600°C *in-situ* anneals the LT material below it, a necessary step for the onset of high resistivity behavior in LT materials.[6] The test structure fabrication was completed by depositing square ohmic contacts (AuGe/Ni/Au) of side lengths varying from 50 to 300 μm on the top of the sample and a large ohmic contact over the entire bottom surface. After annealing the contacts, mesas were etched on the topside. This was done to force current flow through the resistive layer and reduce current spreading.

Room temperature current-voltage (I-V) measurements were then performed on these test structures using a probe station and an HP4145B semiconductor parameter analyzer. For high temperature measurements, a probe station equipped with a hotchuck was used.

RESULTS AND DISCUSSION

Room temperature current-voltage characteristics for all of the LT samples considered in this study are shown in Fig. 1. All of the I-V characteristics exhibit a shape consistent with that of a material containing deep traps. From these characteristics, we can extract the electrical parameters ρ and V_{tfl}. ρ is defined as the differential resistivity $\rho = A/L \times (dI/dV)^{-1}$ and is measured here in the initial linear region of the I-V curves, at V = 0.5 volts. V_{tfl}, the so-called trap-filled limited voltage, is defined in Fig. 1 as the intersection of the linear and "trap-filled" regions of the log-log I-V curve. The trap-filled regime is entered when all of the traps in the material are occupied, resulting in electron transport through the conduction band and a corresponding increase in current. Hence, V_{tfl} is a measure of the number of traps present in the material as defined in Lampert's model.[7]

The measured values of ρ and V_{tfl} for all six samples are summarized in Table II. From this table, several interesting comparisons can be made. First, it can be seen that the apparent resistivity of the LT-$Al_{0.3}Ga_{0.7}As$ samples grown at 250°C is on the order of 10^{11} Ω cm. This value, which is comparable to that reported previously,[3] is approximately three orders of magnitude higher than that of the LT-GaAs grown at the same temperature. This increase is partially attributable to the GaAs/AlGaAs heterojunction in these samples, as evidenced by the high resistance exhibited by the normal $Al_{0.3}Ga_{0.7}As$ sample. However, since the LT-$Al_{0.3}Ga_{0.7}As$ samples generally show a higher resistance than the sample grown at normal temperature, it is apparent that traps also contribute to this extremely high value.

From Table II, it can also be seen that the 250°C LT-$Al_{0.3}Ga_{0.7}As$ samples exhibit a much higher V_{tfl} than that of LT-GaAs: 45 V as compared to 19 V. Note also that the V_{tfl} value for the normal $Al_{0.3}Ga_{0.7}As$ sample is extremely small, less than 1 V. Hence, the extremely high V_{tfl} of LT-$Al_{0.3}Ga_{0.7}As$ cannot be attributed to the GaAs/AlGaAs heterojunction, but must be attributed to traps in the LT material.

We have also considered the variation of the electrical characteristics of LT-$Al_{0.3}Ga_{0.7}As$ as a function of substrate temperature during LT layer growth. From Table II, we see that samples grown at 300°C exhibit even higher apparent values of resistivity (~10^{12} Ω-cm) than those of the 250°C samples. The V_{tfl}, on the

other hand, is nearly 15 V lower in the 300°C samples than it is in those grown at 250°C.

Lampert's theory of deep traps predicts that an increase in trap density should result in an increase in V_{tfl}.[7] Simple trap statistics predict a similar increase in resistivity. In this study, the samples grown at 250°C exhibit higher V_{tfl} than those grown at 300°C, indicating that the lower temperature samples contain a higher density of deep traps. This result is consistent with the trends found in previous LT-GaAs growth studies.[8] Unfortunately, the 250°C samples also exhibit resistivity nearly an order of magnitude lower than the 300°C samples, a result which apparently contradicts the above conclusion.

To explain this contradiction, we may recall that LT-GaAs material is slightly conductive in its as-grown state, becoming highly resistive only after annealing. It has been suggested that this phenomenon is due to "hopping conduction" of electrons between spatially adjacent trap centers, which are abundant (~10^{20} cm^{-3}) in the as-grown LT-GaAs.[9] Upon annealing, the trap concentration drops by at least two orders of magnitude, and this conduction mechanism is no longer dominant. We speculate that a similar mechanism is responsible for the decreased resistivity in our LT-$Al_{0.3}Ga_{0.7}As$ samples grown at 250°C. This reasoning suggests that even after annealing there are indeed many more traps present in these samples than in those grown at 300°C, consistent with our V_{tfl} data as well as with the trend exhibited by LT-GaAs.

We have also made temperature dependent conductivity measurements on LT-GaAs (250°C) and $Al_{0.3}Ga_{0.7}As$ (250, 300°C) samples to determine the activation energies associated with the deep traps in each material. In addition, these measurements may verify the presence of a hopping conduction mechanism in the LT-$Al_{0.3}Ga_{0.7}As$ samples grown at 250°C. The resulting Arrhenius plot for the LT-GaAs sample is shown in Fig. 2. The calculated activation energy is E_A = 0.77 eV, approximately at midgap. This value is in close agreement with previously obtained values for LT-GaAs grown on SI substrates.[8]

The Arrhenius plots for LT-$Al_{0.3}Ga_{0.7}As$ samples grown at 250 and 300°C are shown in Fig. 3. The activation energy calculated from the 300°C sample plot is E_A = 0.95 eV. Again, this energy lies near the midgap of the material (Eg = 1.80 eV). At elevated temperatures, the 250°C sample plot also exhibits an activation energy of ~0.95 eV. Moreover, the conductivity of this sample is lower than that of the 300°C sample, a result consistent with the previously cited V_{tfl} data. At lower temperatures, however, the 250°C sample plot deviates from this activation energy and crosses the 300°C plot, so that at room temperature its conductivity is higher than that of the 300°C sample. This result does indeed confirm the suggestion of an additional hopping conduction mechanism in the 250°C sample, which dominates the room-temperature resistance of the 250°C sample. However, it should be noted that the hot chuck apparatus used in this experiment can introduce noise current

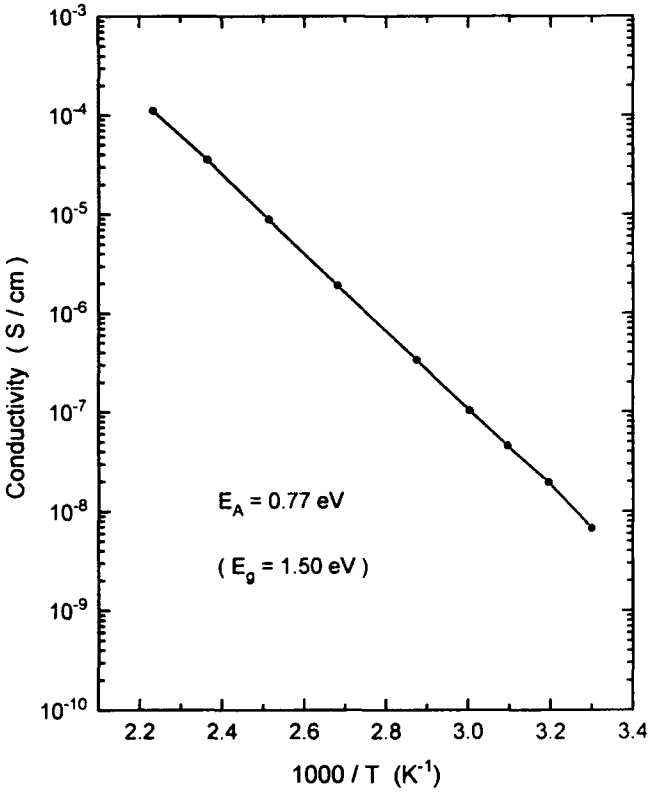

Fig. 2. Conductivity vs temperature, Sample 677 (LT-GaAs, T_{sub} = 250°C).

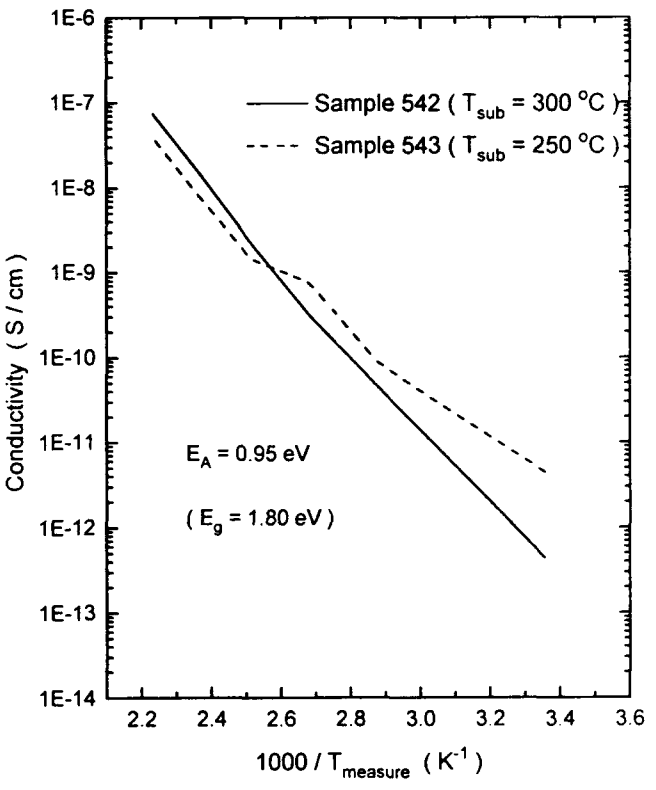

Fig. 3. Conductivity vs temperature, Sample 542 (LT-$Al_{0.3}Ga_{0.7}As$, T_{sub} = 300°C) and Sample 543 (LT-$Al_{0.3}Ga_{0.7}As$, T_{sub} = 250°C).

fluctuations with magnitudes on the order of 50 pA. These fluctuations (which are not present in the room temperature probe station) may affect the accuracy of measurements made at temperatures between 25 and 75°C; i.e., those which exhibit extremely low conductance at zero bias. We are, thus, currently repeating these measurements using a low noise apparatus.

SUMMARY AND CONCLUSIONS

We have measured the resistivity and trap filled limited voltage of annealed LT-$Al_{0.3}Ga_{0.7}As$ materials grown at 250 and 300°C. These samples exhibit resistivities as high as 10^{12} Ω-cm, nearly four orders of magnitude higher than that of LT-GaAs. Hence, LT-$Al_{0.3}Ga_{0.7}As$ should be a very effective electrical isolation layer for electronic and OEIC applications. Moreover, $Al_{0.3}Ga_{0.7}As$ grown at 250°C has a V_{tfl} of 45 V, over twice that of LT-GaAs. This extremely high value suggests that LT-$Al_{0.3}Ga_{0.7}As$ is a strong candidate for the gate insulator material in high power GaAs MISFET devices.

Low temperature-$Al_{0.3}Ga_{0.7}As$ materials grown at 250 and 300°C appear to show opposite and contradictory trends with respect to resistivity and V_{tfl}. We have proposed that this result can be explained by residual hopping conduction in the 250°C material. Temperature dependent conductivity measurements confirm the presence of a hopping mechanism in LT-$Al_{0.3}Ga_{0.7}As$ grown at 250°C and yield activation energies of 0.77 and 0.95 eV for LT-GaAs and LT-$Al_{0.3}Ga_{0.7}As$, respectively.

ACKNOWLEDGMENT

This work was supported by the U.S. Air Force Office of Scientific Research, contract number 91-0327.

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The Role of Microstructure in the Electrical Properties of GaAs Grown at Low Temperature

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We have examined the role of As precipitates on transport through undoped GaAs grown at low temperature by molecular beam epitaxy and annealed at high temperature. Temperature dependent I-V measurements exhibit two regimes. At temperatures less than ~200K, transport attributed to point defect-associated hopping conduction is observed even for samples annealed at 750°C. For temperatures greater than ~200K, the transport is quantitatively consistent with calculations of thermally assisted tunneling emission of electrons from metallic As precipitates acting as buried Schottky barriers.

Key words: High field, precipitates, transport, tunneling emission

INTRODUCTION

The material characteristics of low-temperature-grown (LTG)-GaAs have been studied by various groups due to its potential applications as a semi-insulating epitaxial layer.[1] The growth of GaAs at ~200°C by molecular beam epitaxy (MBE) is highly non-stoichiometric with ~1–2% excess arsenic being incorporated in solid solution during growth.[2] Following high temperature anneals (~600°C), the excess arsenic forms precipitates embedded in the GaAs matrix.[3] Among other interesting properties, the annealed material is found to be highly resistive. In one model, the high resistivity is qualitatively explained by viewing arsenic precipitates as buried Schottky barriers with overlapping depletion regions.[4] The metallic nature of the precipitates is supported by recent scanning tunneling microscopy results.[5] For such a model, the transport properties should quantitatively reflect the observed microstructural features. By combining the temperature dependence of I-V data with microstructure data obtained by transmission electron microscopy (TEM), we show that high field transport in annealed LTG-GaAs is consistent with thermally assisted tunneling of electrons from metallic As precipitates. A simple one-dimensional calculation is found to agree well with the experimental data.

(Received April 12, 1993)

DISCUSSION

To study transport at high fields, an n^+/LTG-i/n^+ structure was used, as shown in Fig. 1. The n^+ GaAs layers were degenerately doped with Si at a level of 2×10^{18} cm^{-3}. Following growth of the n^+ buffer at 600°C, a thin 5×(5Å AlAs/10Å GaAs) superlattice was grown to inhibit outdiffusion of the excess arsenic in the LTG layer during annealing.[6] Growth was then interrupted while the substrate temperature was ramped to 230°C, followed by growth of 5000Å of LTG-GaAs. The substrate temperature was then ramped

to 450°C and a top cladding superlattice and the n^+ cap were deposited. This growth architecture was employed to minimize spatial variations in the precipitate distribution. The sample was cleaved and annealed separately in a rapid thermal annealer for 30s at 600, 650, 700, and 750°C. A mesa structure diode was fabricated, with alloyed AuGe/Ni/Au contacts.

At room temperature, the observed transport properties of the LTG-GaAs layer are similar for all annealing temperatures (T_{anneal}). However, the temperature dependence measurements reveal more complex behavior, in which the transport is sensitive to the annealing temperature and the measurement temperature. For the sake of clarity, our results are summarized in schematic form in Fig. 2. We find evidence for two transport mechanisms. At low temperatures (<200K) the temperature dependence of the I-V data is attributed to defect-associated hopping conduction. This behavior has previously been shown to dominate the low-field transport in unannealed LTG-GaAs.[7] This result suggests that there is a significant residual concentration of point defects in the LTG-GaAs layer that has not precipitated out of solution even for annealing temperatures as high as 750°C. Indeed, for the sample annealed at 600°C, hopping conduction dominates the transport for nearly all measurement temperatures. Figure 3a shows the temperature dependence for samples annealed at different temperatures. As expected, we observe that the hopping conduction contribution to transport decreases as T_{anneal} increases, consistent with continued precipitation of As-related point defects.

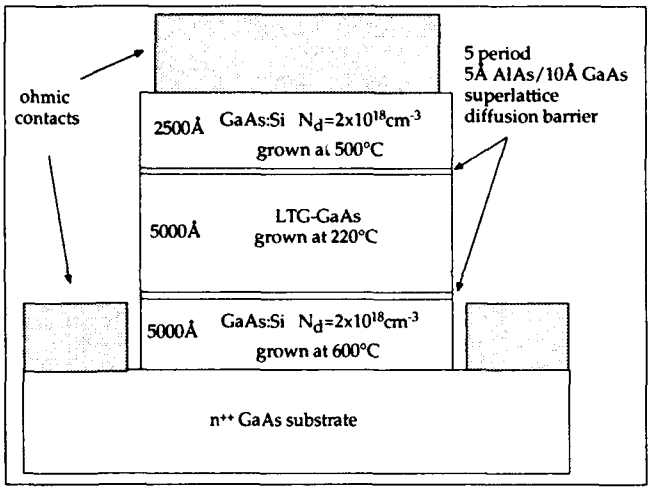

Fig. 1. Schematic of growth architecture used to study transport through LTG-GaAs annealed at different temperatures.

Except for the sample annealed at 600°C, transport at temperatures >200K is clearly dominated by a mechanism other than hopping conduction. In this regime, the transport exhibits a strong temperature dependence, with an activation energy of ~0.6 eV. In Fig. 3b, we show the I-V data at various T>200K for the sample annealed at 700°C. The current exhibits an approximately exponential dependence on the voltage, suggesting transport over a potential barrier. Since the contribution from point defects is decreased, we take the buried Schottky barrier model as a starting point in order to explain the high field transport properties for temperatures greater than ~200K.

Assuming that the precipitates are metallic, then we can model LTG-GaAs as a series of N equivalent metal/semiconductor/metal (MSM) junctions, where N is the total thickness of the LTG-GaAs layer multiplied by the average number of precipitates per unit length. Each junction is essentially a pair of back-to-back Schottky diodes, and we need only consider the transport through one MSM junction, since the electric field is the same across the LTG-GaAs layer. The average junction width can be measured directly by TEM. For the sample annealed at 700°C, TEM analysis yielded a precipitate density of 1.7×10^{16} cm^{-3}, and an average precipitate diameter of 107Å, from which

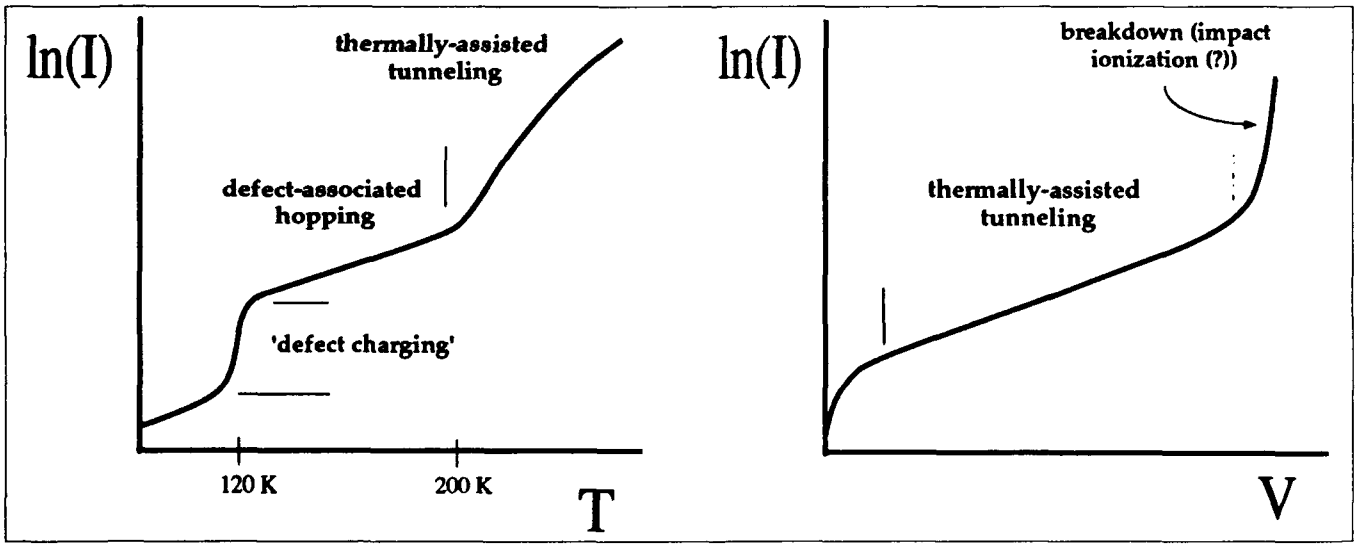

Fig. 2. Schematic summarizing data obtained from I-V measurements as a function of temperature. Behavior attributed to hopping conduction associated with point defects is observed in all samples at lower temperatures. The high temperature (>200K) behavior is consistent with tunneling emission from metallic As precipitates.

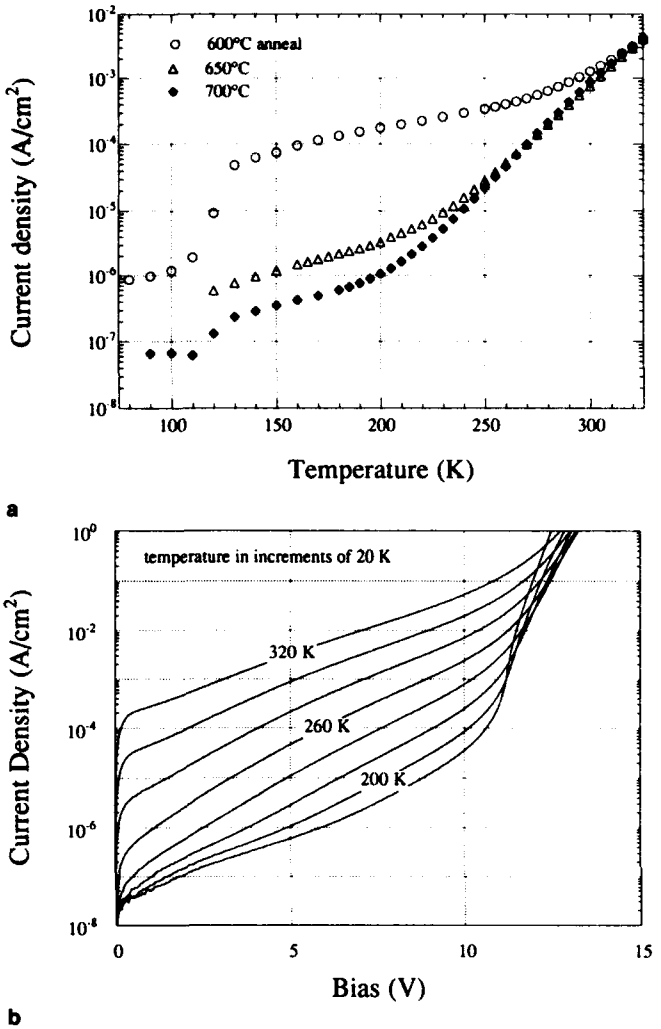

Fig. 3. (a) Current measured at 5 V bias as a function of temperature for samples annealed at 600, 650, and 700°C. As the annealing temperature increases, the contribution due to hopping conduction decreases. (b) Current-voltage measurements taken at various temperatures (200–320K) for the sample annealed at 700°C. For T > 200K, hopping conduction is negligible and the current is exponentially dependent on the applied bias.

an average junction width of 285Å was obtained. Since even a relatively high residual doping of 1×10^{18} cm^{-3} results in a maximum band-bending between Schottky barriers of only ~0.1 eV, it is reasonable to neglect free carrier conduction in the material between precipitates.

The equation for current flow due to thermionic emission over a reverse-biased Schottky barrier is given by the Richardson equation, modified to include image-force barrier lowering effects due to an applied electric field, ε. This gives a current equation with a $\varepsilon^{1/2}$ dependence. In our case, we also have to include a geometric factor, g, due to the finite size of the precipitates. An approximate value can be obtained from TEM results, by multiplying the mean precipitate cross-section area with the mean areal density. For this sample, a factor of 0.06 is obtained. A comparison between the calculated thermionic emission current density as a function of junction electric field, and the

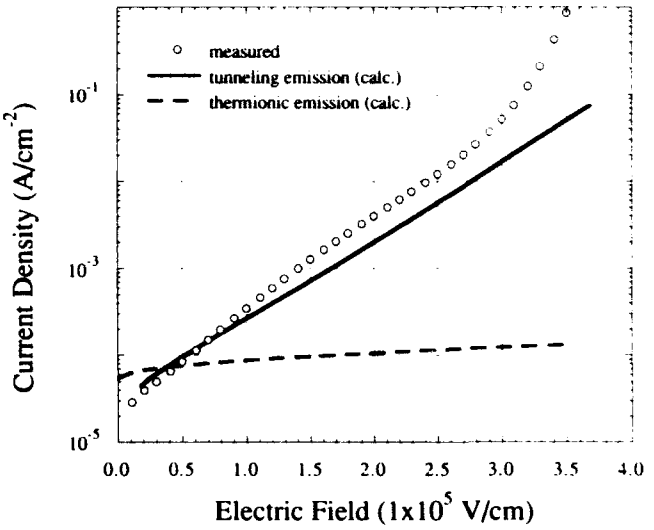

Fig. 4. Measured current-field dependence compared with calculations of thermionic emission, and tunneling emission current flow from metallic As precipitates. A Schottky barrier height of 0.6 eV was used in the calculations.

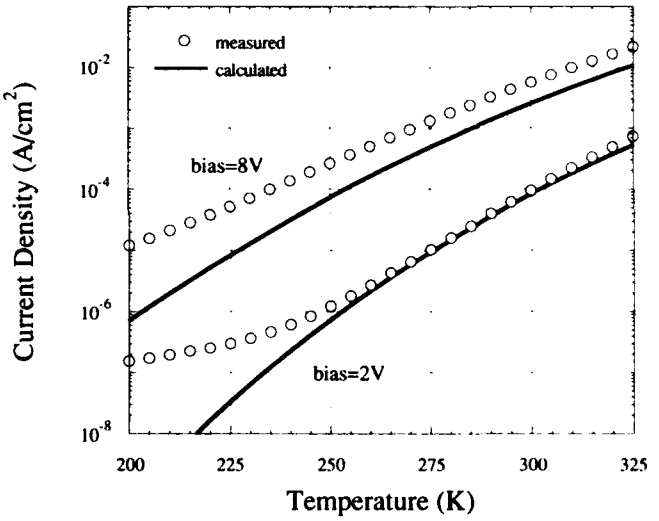

Fig. 5. Measured current-temperature dependence compared with calculations of tunneling emission current flow from metallic As precipitates.

measured data are shown in Fig. 4, using a barrier height of 0.60 eV. We find that the calculated current density gives the correct magnitude at low fields. However, thermionic emission theory does not correctly predict the field dependence.

Reconsidering the MSM band diagram and noting that the electric fields in the junction are large (~1×10^5 V/cm), we calculated the current through the reverse biased Schottky barrier taking into account both thermionic emission over the barrier and tunneling emission below the barrier tip. The expression for the total current density is given by[8]

$$J = \frac{qmkT}{2\pi h^3} \int_0^\infty \exp\left(-\frac{E}{kT}\right) P(E,\varepsilon)\,dE$$

where P(E, ε) is transmission probability for an electron with energy E. P(E, ε) explicitly contains the field

dependence since the potential energy profile of the barrier changes with the applied field. Since the Wentzel-Kramers-Brillouin method is not valid for electron energies near the top of the potential barrier, we employed a numerical method based on transmission matrices to calculate P(E, ε). This method discretizes the potential energy profile into a large number of potential steps. Complete details of the calculation will be discussed elsewhere.[9] Figure 4 shows the calculated and experimentally obtained current as a function of the junction field at 300K, for a barrier height of 0.6 eV. We find that there is good agreement between our model and the experimental data. The temperature dependence of the current, which arrives from the Fermi distribution of carriers in the precipitates, is shown in Fig. 5. Again, the calculated dependence is in good agreement with the experimental data.

CONCLUSION

In conclusion, we have studied the high field transport through undoped LTG-GaAs annealed at different temperatures above 600°C. Arsenic precipitates are present in all samples, but the transport temperature dependence suggests a significant background level of point defects have not precipitated out of solution. The background level, as qualitatively determined from the sample conductivity, decreases with increasing annealing temperature. By correlating microstructural features in samples annealed at temperatures greater than 650°C, the high temperature (>200K) transport is found to be quantitatively consistent with calculations of thermally assisted tunneling emission of electrons from metallic precipitates acting as buried Schottky barriers. The calculated electron transport through LTG-GaAs using a simple one dimensional model agrees well with both the observed field-dependence and the observed temperature-dependence.

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Electrical Properties of Molecular Beam Epitaxial GaAs Grown at 300–450°C

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We use the Hall effect and a new charge-transfer technique to study molecular beam epitaxial GaAs grown at the low substrate temperatures of 300–450°C. Layers grown from 350–450°C are semi-insulating (resistivity greater than 10^7 Ω-cm), as grown, because of an As_{Ga}-related donor (not EL2) at $E_C - 0.65$ eV. The donor concentrations are about 2×10^{18} cm^{-3} and 2×10^{17} cm^{-3} at growth temperatures of 300 and 400°C, respectively, and acceptor concentrations are about an order of magnitude lower. Relatively high mobilities (~5000 cm^2/V s) along with the high resistivities make this material potentially useful for certain device applications.

Key words: Defects, GaAs, low-temperature-grown, MBE

INTRODUCTION

Since the discovery[1] in 1988 of several startling new device improvements by the use of molecular-beam epitaxial (MBE) GaAs grown at the low substrate temperature (LT) of 200°C, much work has been initiated, and has naturally been concentrated in a similar temperature range, 180–275°C. However, it turns out that the first researchers to successfully employ LT MBE GaAs for device improvements used a substrate temperature of 400°C, and reported that the resistivity of this material was greater than 10^4 Ω-cm and was, therefore, useful for buffer layers.[2] Thus, it is worthwhile to carefully examine MBE GaAs grown at substrate temperatures of 300–450°C which should have both higher resistivities (as-grown) and higher mobilities than 200°C material, and which, therefore, may be more useful for certain applications. For example, we will show that 400°C GaAs has a resistivity $\rho \geq 10^7$ μ-cm (much higher than that surmised by Murotani et al.)[2] and a mobility $\mu > 5000$ cm^2/V s. Coupled with a reported[3] photoconductive (PC) lifetime τ of about 6 ps, this material should make a reasonably fast PC switch with very high responsivity. Lower growth temperatures lead to lower τ's but also lower μ's, as will be shown here.

(Received April 12, 1993)

Samples were grown in a modified Varian 360 MBE system which was essentially equivalent to a Varian Gen II system. The As_4/Ga beam-equivalent pressure was set at about 20, and substrate temperatures were measured with a thermocouple (tc) mounted in the narrow vacuum space between the heater plate and the substrate. At 400°C, the tc readings could be checked with an optical pyrometer, and the results typically agreed to within 10–15°C; however, at 300°C, no such check was possible. In all, we have grown layers at temperatures from 300–480°C, but will report extensively only on 300°C and 400°C layers in this paper. Interestingly enough, the resistivity of 400°C material, about 10^7 Ω-cm, is quite representative of all material grown from about 350–480°C, and even 300°C GaAs has a fairly high resistivity, about 10^5 Ω-cm.

RESISTIVITY, HALL EFFECT, AND CHARGE TRANSFER ANALYSIS

We have previously demonstrated that to get reliable Hall-effect measurements on LT GaAs layers it is absolutely necessary to remove the layers from their semi-insulating substrates.[4] (The technique for separating the layers has been described elsewhere.[4]) The reason is that the relevant additive quantity, $R_\square \sigma_\square^2$, where $R_\square$ and $\sigma_\square$ are respectively the sheet Hall coefficient and conductivity of a particular layer,

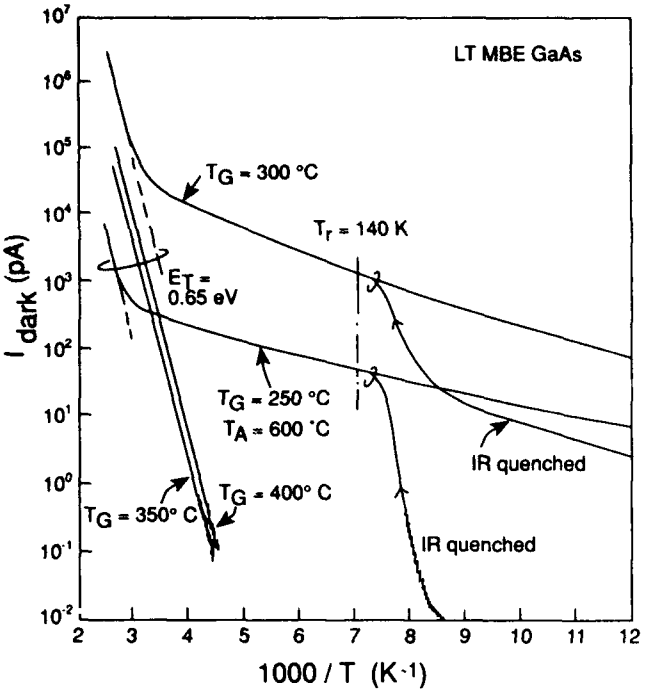

Fig. 1. The dark current (20 V bias) vs temperature (swept upward at 0.3K/s) for MBE GaAs samples grown at T_G = 300, 350, and 400°C, and not annealed, and also a sample grown at 250°C and annealed at T_A = 600°C. Typical sample dimensions are 6 mm × 6 mm × 5 μm. The quenching effects of IR light irradiation (hν ≤ 1.12 eV, ~10^{15} phot./cm² s, 5 min) at 80K are also shown for two of the samples. The quenched conduction recovers at T_r = 140K.

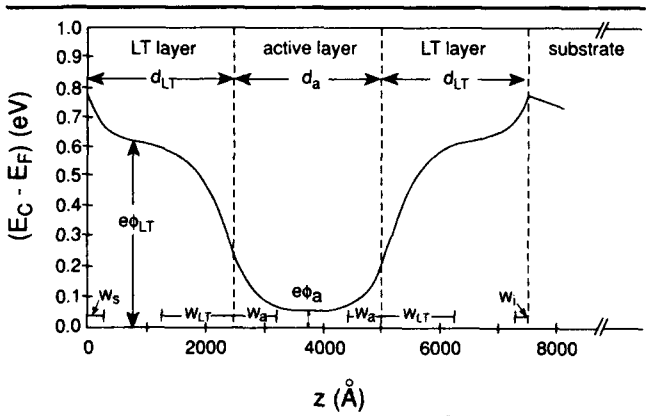

Fig. 2. A Poisson solution for a 2500/2500/2500Å LT/n/LT structure on a semi-insulating substrate with the following parameters: $N_{D,LT}$ = 2.0 × 10^{17} cm^{-3}; $N_{A,LT}$ = 3.0 × 10^{16} cm^{-3}; $(N_D-N_A)_a$ = 7.1 × 10^{16} cm^{-3}; $E_{D0,LT}$ = 0.648 eV; surface state acceptor density 1 × 10^{13} cm^{-2} at E_C – 0.7 eV; LT/substrate interface acceptor density and energy same as those at surface.

is much greater for the substrate than for any LT layer which is not heavily (and successfully) doped. For the charge-transfer analysis described later, substrate removal is not necessary because a doped, conductive 580°C layer is an integral part of the structure.

A very simple, convenient, and informative technique for studying and comparing LT GaAs layers is current (I) vs temperature (T) measurements performed at a fixed bias (usually 20 V) as temperature is swept (typically at a rate 0.3K/s) from 80–450K. The measurements shown in Fig. 1 well illustrate the general features of material grown at 250, 300, 350, and 400°C. First consider the samples grown at 350 and 400°C; clearly they exhibit the classical Arrhenius (lnI vs T^{-1}) behavior expected for a semiconductor material of conductivity σ controlled by a deep donor of concentration N_D compensated by an acceptor N_A. That is, $I \propto \sigma$ where

$$\sigma = e\mu(N_A,T)n(N_D,N_A,T) = e\mu CT^{3/2}(N_D/N_A-1)\exp(-E_{D0}/kT) \quad (1)$$

where $E_D = E_{D0} - \alpha T$ is the donor activation energy and C is a constant involving α and the degeneracy factor g. The dominant temperature-dependent term in Eq. (1) is the exponential so that $-E_{D0}/k$ is the slope of a lnI vs T^{-1} plot. The same value of E_{D0} (0.65 ± 0.01 eV) is found not only for the 350 and 400°C samples, but also for the 250 and 300°C samples at high enough measurement temperatures. These results are confirmed by Hall-effect measurements, which can separate μ and n. Thus, the dominant donor in LT MBE GaAs is not the expected EL2, which has E_{D0} = 0.75 ± 0.01 eV, but a related center which also has the As antisite defect As_{Ga} as a core, as is known from other studies.[5] The shallower lnI vs T^{-1} slopes in Fig. 1 are due to hopping conduction between the 0.65 eV donors, as will be discussed later but which has already been investigated extensively.[4,6]

If we know the donor temperature coefficient α and the degeneracy factor g, then the Hall measurement of μ vs T will give N_A [using Eq. (3) of Ref. 4], and n vs T will give N_D/N_A (and thus N_D). However, in this case we can only estimate α (≅ 3 × 10^{-4} eV/K) and g (≅ 2), resulting in uncertainties for N_D and N_A. For the layers grown at 200–300°C, the uncertainties are even greater, because the hopping conduction must also be included, as outlined in Refs. 4 and 6.

To circumvent some of these difficulties, we have devised a new method to measure N_D and N_A, which involves charge transfer from a conductive layer of known N_D–N_A to a resistive layer for which N_D and N_A are unknown, but the Fermi level E_F is known. Consider the LT/n/LT structure shown in Fig. 2. The active layer (n-type in this case) will transfer electrons from a region of width w_a to acceptors in the LT layers on either side. For simplicity of analysis, it is necessary to have flat-band regions in both the active layer and LT layers, which means that $d_a > 2w_a$, $d_{LT} > w_{LT} + w_s$, and $d_{LT} > w_{LT} + w_i$. Then a standard result, in the depletion approximation, is

$$w_a = \sqrt{\frac{2\epsilon(\phi_{LT} - \phi_a - kT/e)}{en_a(1+n_a/N_{A,LT})}} \quad (2)$$

where n_a is the volume electron concentration in the active layer. We want to determine $N_{A,LT}$ (henceforth called N_A) which means we need to know w_a, ϕ_{LT}, ϕ_a, and n_a. The key measurement is a Hall-effect determination of the sheet carrier concentration of the LT/n/LT structure, which will be always be dominated by

the n layer as long as $n_a \geq 10^{15}$ cm^{-3} and d_a and d_{LT} are reasonable values. Then

$$n_J = n_a(d_a - 2w_a) \quad (3)$$

By growing two structures, with different d_as, both n_a and w_a can be determined from Eq. (3). Then we can calculate the act.. -layer flat-band potential

$$\phi_a = \frac{kT}{e}\left(\ln\frac{N_C}{n_a} - \frac{n_a}{N_C\sqrt{8}}\right) \quad (4)$$

where N_C, the effective conduction-band density of states, is 4.16×10^{17} cm^{-3} at 296K. Finally, to determine ϕ_{LT}, it is necessary to grow a layer of a few-microns thickness, separate it from its substrate, and determine the carrier concentration n_{LT} from a Hall measurement. Then ϕ_{LT} can be found from Eq. (4) (with $n_a \rightarrow n_{LT}$). However, note from Table I that all of the LT layers we have measured, grown at temperatures from 200–450°C, have ϕ_{LT} values in the range 0.52 ± 0.05 eV. Thus, this value could probably be used for almost any LT layer without excessive error.

To determine N_A in 400°C GaAs, three samples were grown: two LT/n/LT structures of dimensions 5000/2500/5000Å and 5000/5000/5000Å, respectively, for charge-transfer (CT) analysis; and a single, 5 μm, 400°C GaAs layer on a 1000Å AlAs separation layer, for Hall effect analysis. The measurements and calculations are given in Table II, with the prime result $N_A = 3 \times 10^{16}$ cm^{-3}. Other CT results, using both LT/n/LT and LT/p/LT structures, are given in Table I. Note that to determine $N_{D,LT}$ by the CT method, it is necessary to use a p-type active layer. It also should be mentioned that a good choice for n_a is $n_a \cong N_A$ (or $p_a \cong N_D$, for a p-type active layer). That is, if $n_a << N_A$, then as seen in Eq. (2) w_a will not be a strong function of N_A, while if $n_a >> N_A$, then w_a will be very small and hard to measure accurately.

It should be mentioned here that the lower 400°C layers in these samples are effectively being annealed at 580°C during the time (15–30 min) that the active layer is being grown. Thus, for consistency, we performed a second 15 min. 580°C anneal after growth of the top 400°C layer in each sample with an active layer, and did the same for the 5 μm thick, semi-insulating sample. To see whether or not the annealing changed N_D and N_A, we performed the CT experiment in a slightly different way, by using only a 400°C unannealed cap (and not a 400°C buffer), and comparing n_J with that obtained from a sample without a cap. (This method requires the rather well-grounded assumption that the free GaAs surface has a Fermi level pinned at $E_C - 0.7$ eV.) In any case, the results for N_D and N_A were equal within error (a factor two), showing that a 580°C anneal does not affect the 400°C material appreciably. Thus, having established that the two CT methods gave basically equivalent results for the 400°C layers, we felt justified in using only the

Table I. Electrical Parameters of LT MBE GaAs

Growth Temp.	H or CT*	μ(300K) cm²/V s	n(300K) cm⁻³	E_F(300K) eV	N_D cm⁻³	N_A cm⁻³
200°C	H	250	2×10^9	0.50	8×10^{19}	1×10^{19}
300°C	H	1700	4×10^9	0.47	3×10^{18}	2×10^{17}
	CT	—	—	—	2×10^{18}	5×10^{16}
350°C	H	4700	1×10^8	0.57	3×10^{17}	1×10^{17}
400°C	H	5500	2×10^8	0.56	3×10^{17}	1×10^{17}
	CT	—	—	—	2×10^{17}	3×10^{16}
450°C	H	2600	4×10^8	0.54	—	—

*H = Hall-effect method; CT = charge-transfer method

Table II. Measured and Calculated Parameters for LT/n/LT Charge-Transfer Structures Involving 400°C GaAs

Parameter	Type	Sample G2-1647	G2-1648	G2-1651
d_{LT}	meas.	5000Å	5000Å	5 μm (single layer)
d_a	meas.	2500Å	5000Å	N/A
n_J	meas.	9.96×10^{11} cm^{-2}	2.77×10^{12} cm^{-2}	5.64×10^{4} cm^{-2}
n_{LT}	calc.	N/A	N/A	1.13×10^8
n_a	calc.	7.10×10^{16} cm^{-3}	—	
w_a	calc. [Eq. (3)]	548Å	—	—
ϕ_a	calc. [Eq. (4)]	0.0436 V	—	—
ϕ_{LT}	calc. [Eq. (4), using n_{LT}]	--	—	0.562 V
$N_{A,LT}$	calc. [Eq. (2)]	3.1×10^{16} cm^{-3}	—	—

latter variation on the 300°C samples listed in Table I, because at that growth temperature the annealing might be expected to have an appreciable effect. Interestingly enough, however, recent Hall-effect results have shown that N_D drops only about a factor two, and N_A only about 25% in material grown at 300°C and annealed at 600°C.

The Hall and CT results in Table I agree quite well for N_D, whereas the CT values for N_A are about a factor three below the Hall results. In principle, the CT result should be more accurate since no unknown parameters (such as g and α) are involved. Note that if α were taken as 2.3×10^{-4} instead of 3.3×10^{-4} eV/K in the Hall formulation, then the Hall and CT values of N_A would be much closer.

DISCUSSION

From Table I it is seen that N_D (the 0.65 eV As_{Ga}-related donor) decreases by more than two orders of magnitude as growth temperature T_G increases from 200–350°C, and N_D then remains relatively constant to at least 400°C. The acceptor concentration N_A, on the other hand, decreases about two orders of magnitude from T_G = 200–300°C, and then does not change more than a factor two from 300–400°C. At 450°C, we have not yet determined N_D and N_A, but it is clear from the data in Table I that $N_D > N_A$ and that E_F is still controlled by the deep donor. Thus, semi-insulating MBE GaAs can be grown over a wide range of growth temperatures, at least from 300–450°C, and even to 480°C by referring to some data not shown in Table I. The transition temperature, at which shallow impurity states begin to dominate the conduction, is not known yet but is probably close to 500°C. The identity of the acceptor defect is also unknown at this time, but is probably V_{Ga} related.

Finally, we wish to make some comments regarding the role of precipitates[7] vs point defects[4,6] in determining electrical properties. In Fig. 1, we display I_{dark} vs T for a sample grown at 250°C and annealed at 600°C, conditions which are known to produce large As precipitates. Note that the shape of this curve is nearly identical to that of a layer grown at 300°C and not annealed, which has no precipitates. Note also that the hopping conduction can be quenched by IR (1.12 eV) light irradiation in both cases.[8] Thus, there is no doubt that point defects, in particular the arsenic antisite center, control the electrical properties of both of these LT MBE GaAs layers, and that precipitates, therefore, have little or no effect.

CONCLUSION

In summary, we have used the Hall-effect and the new charge-transfer technique to elucidate the conduction mechanisms in MBE GaAs grown at substrate temperatures from 200–450°C. For $T_G \leq 300$°C, hopping conduction is dominant at room temperature, whereas for T_G = 350–450°C, only band conduction is important and the layers are semi-insulating without any anneal. Such material should be very useful for certain electronic and optical device applications.

ACKNOWLEDGMENTS

We wish to thank E.N. Taylor and J.E. Ehret for the GaAs crystal growth, R. Heil for manuscript preparation, and Z.-Q. Fang for helpful discussions. D.C.L. and G.D.R. were supported under U.S. Air Force Contract F33615-91-C-1765.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Hopping Conduction and Its Photoquenching in Molecular Beam Epitaxial GaAs Grown at Low Temperatures

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As the growth temperature of molecular beam epitaxial GaAs is increased from 250 to 400°C, the dominant conduction changes from hopping conduction to band conduction with a donor activation energy of 0.65 eV. A 300°C grown layer is especially interesting because each conduction mechanism is dominant in a particular temperature range, hopping below 300K and band conduction above. Below 140K, the hopping conduction is greatly diminished (quenched) by irradiation with either infrared ($h\nu \leq 1.12$ eV) or 1.46 eV light, but then recovers above 140K with exactly the same thermal kinetics as are found for the famous EL2. Thus, the 0.65 eV donor, which is responsible for both the hopping and band conduction, is very similar to EL2, but not identical because of the different activation energy (0.65 eV vs 0.75 eV for EL2).

Key words: Defects, hopping conduction, low-temperature-grown GaAs, photoquenching

INTRODUCTION

Molecular beam epitaxial (MBE) GaAs grown at low substrate temperatures (LT), 200–400°C, has been shown to be uniquely useful in several device applications.[1] Compared with the usual MBE GaAs growth at 580–600°C, the only major difference is a large concentration (10^{19}–10^{20} cm^{-3}) of As_{Ga} and V_{Ga} defects in the as-grown LT (200–250°C) materials[2] and a decrease of defect concentrations along with large As precipitates after annealing at 550–600°C.[3] Such high As_{Ga} concentrations lead to hopping conduction, because the average separation distance (~13Å) is close to the wave function dimension (~9Å from a hydrogenic calculation).[4] We have analyzed the hopping conduction and its photoquenching in LT MBE GaAs grown at 250°C and annealed at temperatures from 300 to 600°C.[5] Through a numerical analysis of the data, a thermal barrier of 0.26 eV for the thermal restoration of the quenched hopping conduction has been deduced, which is the same as the metastable-to-normal state activation energy for EL2.[6] In this paper, we present the results of similar studies on MBE GaAs layers grown at temperatures from 300 to 400°C, but without further annealing. The results confirm that

- the dominant defect in LT MBE GaAs is related to the As_{Ga}, but is not the famous EL2, and
- the hopping conduction is greatly reduced by increasing growth temperature due to a decrease of As_{Ga}.

(Received April 12, 1993)

EXPERIMENT AND RESULTS

The 5 μm thick LT MBE GaAs samples used in the study were grown at 300, 350, and 400°C in a modified Varian 360 system under normal As-stabilized conditions with As_4/Ga beam equivalent pressures of about 20. No post-growth anneal was performed on the samples. For unambiguous characterization, the LT MBE layers (6 x 6 mm in size) were separated from their substrates by a technique described elsewhere.[7] Indium contacts were put on the four corners of each layer with a soldering iron, without further annealing and either pair of the diagonal contacts was used in the measurements. The dark current (I_{dark}) and the thermally stimulated current (TSC) after the light excitation at 82K were measured under a 20 V bias as

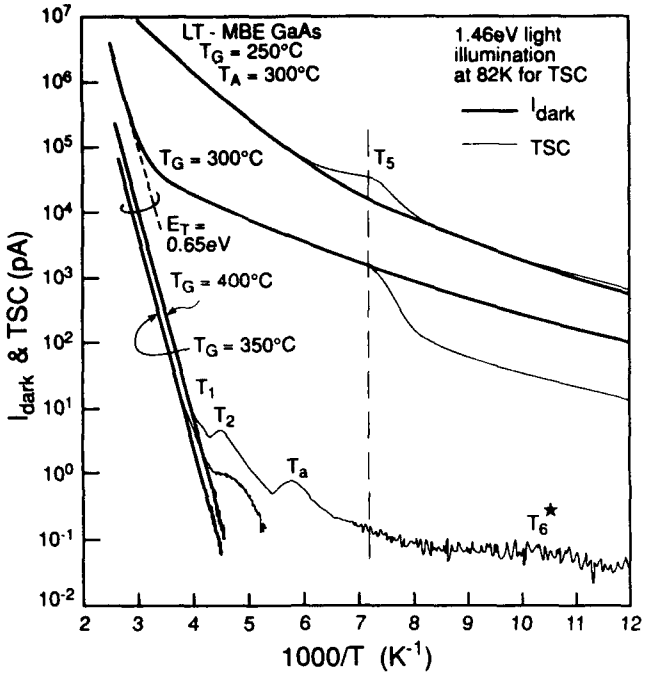

Fig. 1. A comparison of the dark and thermally stimulated currents for LT MBE GaAs grown at 250°C (with 300°C anneal), 300, 350, and 400°C.

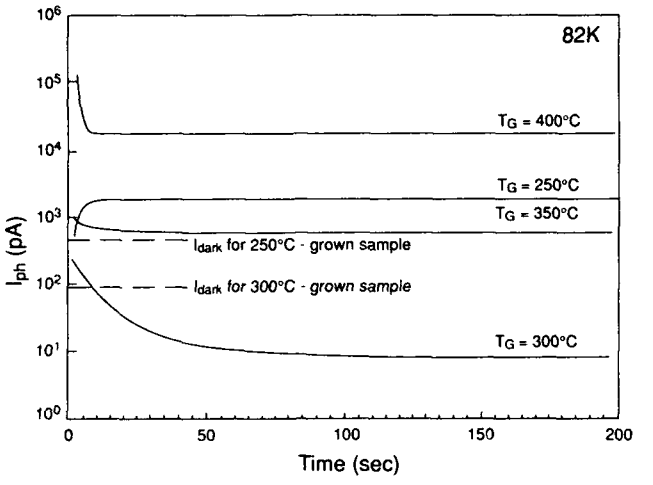

Fig. 2. Infrared photocurrent responses at 82K for the LT MBE GaAs samples, showing IR quenching of I_{ph}, except for the sample grown at 250°C.

the temperature was swept upward at a heating rate of 0.3K/s, while the photocurrent (I_{ph}) was measured at 82K to monitor its photoquenching. Both IR light ($h\nu \leq 1.12$ eV) and 1.46 eV light with different light intensities were used to produce the photoquenching phenomenon.

In Fig. 1, we show the dark currents and TS currents after 5 min excitation of the strongest available 1.46 eV light (2×10^{16} phot/ cm^{-2} s) for samples grown at 300, 350, and 400°C, and a sample grown at 250°C and annealed at 300°C, for comparison. The first thing to note in the figure is that the 250 and 300°C grown samples have strong conduction at low measurement temperatures. This conduction is due to hopping between the dense As_{Ga} centers and can be well described by the equation $\sigma_{VR} = C_{VR}\, e^{-(T_0/T)^{1/4}}$ for variable-range hopping.[6] For these two samples, T_0 was determined to be 90 and 64, respectively. In the 300°C grown sample, a significant band conduction can be clearly observed only above 300K. On the other hand, the 350 and 400°C grown samples show band conduction over the whole temperature range because the As_{Ga} centers are too far apart to sustain hopping. The second thing to note is the activation energy of the band conduction for the three samples, which is 0.65 ± 0.01 eV rather than the EL2 value of 0. 75 eV.[8] As for the TSC spectra, unlike the other samples, the 300°C grown sample shows no meaningful TSC peak but a reduction of the dark current at low temperatures and recovery of the current at 140K; these phenomena have been observed before on LT MBE samples grown at 250°C and annealed at temperatures from 350 to 600°C, and are due to the photoquenching of the As_{Ga} centers and their subsequent thermal recovery.[5] We do not discuss the possible nature of the observed TSC peaks in this paper.

The photocurrent responses resulting from IR light illumination with equal light intensities of 2 I_{ir} (see below) at 82K are shown in Fig. 2. In contrast to the 250°C grown sample, the other samples all show IR quenching of I_{ph}. However, for the 300°C grown sample, we see the IR photoquenching of the dark current as well. It seems that both illumination wavelengths can cause photoquenching of the dark current at 82K in LT MBE GaAs materials which show a moderate hopping conduction. However, detailed studies of the 300°C grown sample, using IR and 1.46 eV light with various relative light intensities do show differences both in the photoquenching process and in the final quenched I_{dark}, as pictured in Fig. 3 and Fig. 4. Figure 3 shows the photoquenching process of the I_{ph} as a function of the relative light intensity for (a) IR light, and (b) 1.46 eV light. Figure 4 shows the quenched I_{dark} and its thermal recovery for both types of light. The quenched dark current at 82K is identical for each light intensity shown in Figs. 3a and 3b as long as the illumination is stopped at the times shown in this figure (i.e., where the curves end). From these figures, we find that the light excitation at 82K, using either light, causes photoquenching not only in the net I_{ph} but also in the I_{dark}. For the IR light (see Fig. 3a), the asymptotic value of I_{ph} after complete photoquenching is proportional to the light intensity; also, the quenching time, t_q, which is needed to reach the final quenched I_{ph}, is inversely proportional to the light intensity. Therefore, the final quenching state, represented by the quenched I_{dark} can be reached by absorbing a fixed dosage of IR photons as explained above (see Fig. 4). However, for the 1.46 eV light (see Fig. 3b), we cannot find a final asymptotic quenched I_{ph} or such a dosage dependence for the quenching process. But the same quenching state still can be reached by absorbing different dosages of 1.46 eV photons (see Fig. 4). Although the quenched I_{dark}'s for both lights are different, they are recovered at nearly the same

temperature (140K). We also checked the photoquenching process this way on the samples grown at 250°C, but annealed at 350°C < T_A < 600°C, and found that the dosage dependence holds for all of them only in the IR excitation case, but not in the 1.4 eV light case.

DISCUSSION AND CONCLUSIONS

The prominent characteristics of the native defect in bulk semi-insulating (SI) GaAs, known as EL2 and having As_{Ga} as a core, is its IR photoquenching and thermal recovery, due to the reversible transition between the normal and metastable states of EL2.[6] Although the detailed atomic configurations of EL2 in both states have not been unambiguously established, the thermal barrier for the EL2 recovery has been determined to be E_b = 0.25–0.30 eV by measuring several different quantities which quench under the illumination, such as photocapacitance, IR absorption and photocurrent.[8] For LT MBE GaAs, which has hopping conduction at low temperatures, a new experimental quantity—the dark current—can be used to determine E_b. For the sample grown at 250°C and annealed at 550°C, a numerical analysis of the dark current recovery, based on the hopping conduction, gives an excellent fit to the data for a thermal recovery rate $r = 3 \times 10^8 \exp(-0.26\,eV/kT)$,[6] very close to the rate observed in a recent study of EL2 in bulk SI GaAs.[9] This proves that the conduction below 300K in this sample is due to hopping between As_{Ga}-related centers in their normal states. For the sample grown at 400°C, which shows only band conduction, the numerical fit to the photocurrent vs temperature data, after full IR quenching, results in a very similar thermal recovery rate, $r = 2.5 \times 10^8 \exp(-0.26\,eV/kT)$.[10] The nearly identical thermal recovery rate as that for EL2 and the same dosage dependence in the IR quenching of I_{ph}, as observed in bulk SI GaAs,[11,12] allows us to conclude that the dominant defect in LT MBE GaAs is related to As_{Ga}. However, based on the following experimental results, we have to argue that it is not the famous EL2. First, the thermal activation energy of the conduction at T >300K for the three samples grown at 300°C < T_G < 400°C is only 0.65 eV, much lower than the EL2 value of 0. 75 eV. Second, unlike EL2,[8] the As_{Ga} centers in LT MBE GaAs materials show a significant photoquenching of I_{ph} when 1.46 eV light is used. Finally, several other properties of As_{Ga} in a 400°C grown sample, including the electron-capture barrier energy, the hyper-fine constant and the magnetic circular dichroism spectrum have been found to differ from those same quantities in the EL2 of bulk SI GaAs.[10]

Now consider the effect of the growth temperature on the hopping conduction and the IR quenchability of the As_{Ga}-related center. The sample grown at 250°C shows a strong hopping conduction, which even hinders the band conduction from being observed, and little or no IR photoquenching of I_{ph}. On the other hand, while the samples grown at 350 and 400°C show only band conduction, the sample grown at 300°C shows both hopping conduction and band conduction. Thus, as the concentration of As_{Ga} centers decreases, both the hopping conduction decreases and photoquenchability increases. If the same center (the 0.65 eV center) is involved in all LT MBE GaAs materials, then the quenchability has to depend on the different environments that different growth conditions produce. For example, factors such as strain and recombination-center density could influence quenching.

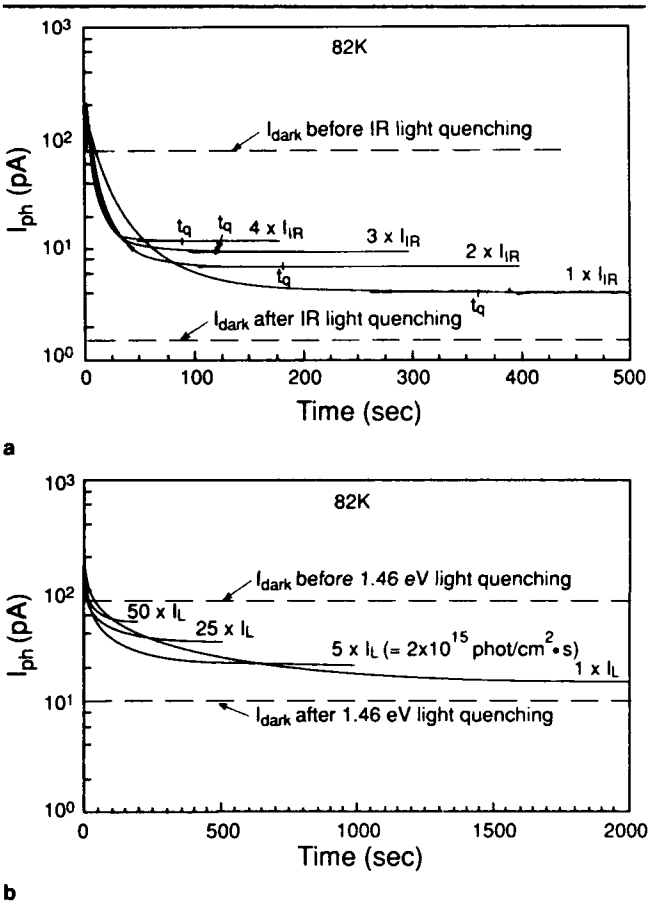

Fig. 3. Photoquenching of I_{ph} for 300°C grown sample by using (a) IR light (hν ≤ 1.12 eV) and (b) 1.46 eV light, with various light intensities.

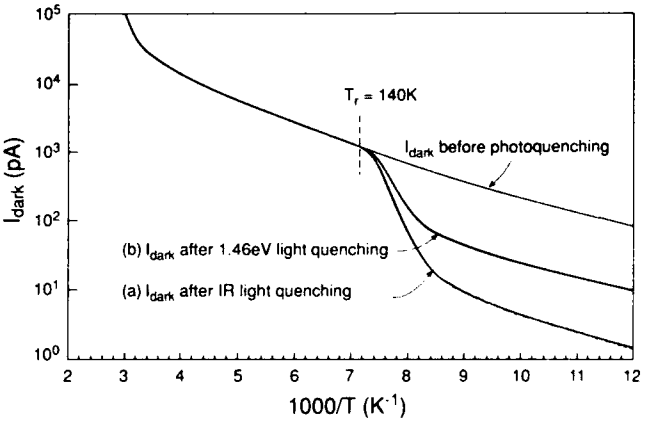

Fig. 4. Photoquenching of the dark current and its thermal recovery at 140K for 300°C grown sample after illumination of (a) IR light and (b) 1.46 eV light.

CONCLUSION

In conclusion, the photoquenching behavior of As_{Ga}-related centers in LT MBE GaAs materials was studied and compared to that of EL2 in bulk SI GaAs. For the 300°C grown sample, the conduction at T < 300K is controlled by carrier hopping in the defect band, depending on whether the defect is in its normal or metastable state; this behavior is similar to that found in a sample grown at 250°C and annealed at 350 < T_A < 600°C. For the 350 and 400°C grown samples, only the band conduction, with an activation energy of 0.65 eV, was observed. The dominant defect in the LT MBE materials is related to As_{Ga}, but is not the famous EL2. The differences between the As_{Ga} in LT MBE GaAs and that in bulk SI GaAs need further study.

ACKNOWLEDGMENT

We wish to thank E.N. Taylor and C.E. Stutz for the crystal growth, C.D. Robinson for the substrate removal, and N. Blair for the manuscript preparation. Z-QF was supported under Office of Naval Research contract N00014-90-J-11847 and DCL under U.S. Air Force contract F33615-91-C-1 765.

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Electrical Properties of Low-Temperature GaAs Grown by Molecular Beam Epitaxy and Migration Enhanced Epitaxy

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Measurements on low-temperature GaAs epitaxial layers (LT-GaAs) grown by molecular beam epitaxy and migration enhanced epitaxy showed that the excess arsenic incorporated during growth played a crucial role in determining their electrical properties. The electrical transport in LT-GaAs grown by a standard molecular beam epitaxy proceeded mainly via a hopping process, which showed a higher activation energy and onset temperature than those usually observed in lightly doped semiconductors. Using migration enhanced epitaxy to grow LT-GaAs, we were able to substantially reduce the density of As-rich defects and to achieve a good Hall mobility in Be-doped LT-GaAs. The study presented here indicates that, with controlled excess arsenic incorporation during growth, LT-GaAs can vary in a range of conduction properties and thus can be engineered for different device applications.

Key words: Low-temperature-grown GaAs, MBE, migration enhanced epitaxy

INTRODUCTION

The success of using molecular beam epitaxial (MBE)-grown low temperature (LT)-GaAs for electrical isolation in GaAs field effect transistors[1,2] has driven considerable research effort to study this material in recent years.[3–9] Much progress has been made in understanding the chemistry, atomic structure, and electrical properties of this material. The excess arsenic incorporated during epitaxial growth at reduced temperatures forms As-rich defects such as arsenic antisite defects (As_{Ga}),[4] arsenic interstitials (As_i),[6] and arsenic clusters.[7,8] These defects will inevitably affect the electrical properties of the LT-GaAs layers. It was reported that the Fermi level was pinned by defect states in this material[10,11] and the electrical transport proceeded via a hopping process through arsenic antisite defects.[9,12,13]

By controlling excess arsenic incorporation during low temperature growth, one may be able to change the defect density (and/or structures) and the electrical properties of the LT-GaAs layers. Migration enhanced epitaxy (MEE) is a technique to grow epitaxial layers at reduced substrate temperatures.[14] We have investigated extensively the electrical properties and device applications of LT-GaAs grown by MBE and MEE.[15–18] In this paper, we presented our results to show that, with controlled excess arsenic incorporation during growth, LT-GaAs can vary in a range of conduction properties and thus can be engineered for different device applications.

(Received April 12, 1993)

EXPERIMENTAL PROCEDURES

Growth of Epitaxial Layers

The samples used in this study were grown in a Varian Gen II MBE system by either conventional MBE or migration enhanced epitaxy. Liquid encapsulated Czochralski (LEC)-grown semi-insulating (SI) GaAs substrates were mounted on a Mo block using indium. The growth temperature for LT-GaAs was 280°C, as determined by a procedure discussed previously.[15] The same Mo block was used for all LT-GaAs growth to minimize the temperature reading errors which can be caused by variations in holder emmisivity. Both As_4 and As_2 species were used in this

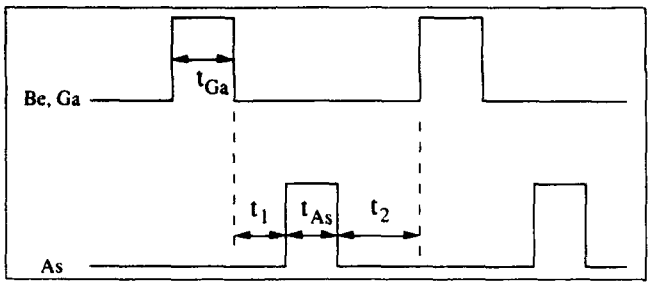

Fig. 1. Shutter operation sequence for migration enhanced epitaxy.

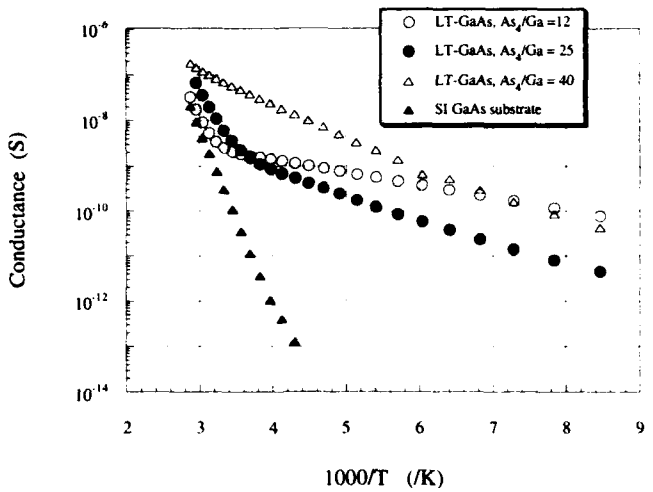

Fig. 2. Plot of conductance vs reciprocal temperature for LT-GaAs grown at different As-to-Ga beam equivalent pressure ratios.

Table I. Conduction Parameters Extrapolated from Temperature-Dependent Conductance Measurements of MBE-Grown LT-GaAs Samples

Growth Condition of LT-GaAs Samples	ε_3 (eV)	b ($K^{1/4}$)
$As_4/Ga = 40$	0.145	122.8
$As_4/Ga = 25$	0.118	103
$As_4/Ga = 12$	0.055	70
$As_4Ga = 25$ [Si]≈5×10^{16} cm^{-3}	0.095	116.9
$As_4/Ga = 25$ [Be]≈5×10^{16} cm^{-3}	0.059	30.1
$As_2/Ga = 12$ [Be]≈5×10^{16} cm^{-3}	0.061	18.9

experiment. The LT-GaAs layers were 2 μm thick.

The shutter operation sequence during MEE growth is shown in Fig. 1. The Ga deposition time (t_{Ga}) was 1.5 s, which corresponded to one monolayer of Ga deposition as determined by reflection high energy electron diffraction intensity oscillation measurements at 560°C. The As deposition can be varied by changing either the As deposition time (t_{As}) or the As flux. The t_1 and t_2 were growth interruption times between the Ga-deposition and As-deposition phases, which were 2 s in this experiment. The MEE-grown layers are 0.35 or 0.15 μm thick.

Electrical Characterization

The LT-GaAs samples grown by conventional MBE showed high resistance and were characterized by temperature-dependent conductance measurements. In-Sn alloy dots were used as ohmic contact and the corner-to-corner conductance was measured at a temperature range of 100~350K on square samples. A same size of sample cleaved from a 3" LEC-grown SI GaAs wafer was also measured for comparison. The MEE-grown LT-GaAs samples doped with Be showed high conductivity and were characterized by Hall effect measurements at temperature range of 10~300K. The ohmic contact on these samples were provided by In-Zn alloy dots.

EXPERIMENTAL RESULTS

MBE-Grown LT-GaAs Layers

Shown in Fig. 2 is the plot of conductance as a function of reciprocal temperature obtained from unintentionally doped LT-GaAs grown at three different As-to-Ga beam equivalent pressure (BEP) ratios, and an SI GaAs substrate sample. Similar to the previous work reported by other groups,[9,12,13] two different conduction mechanisms, band conduction, and hopping conduction were observed in different temperature ranges. For nearest-neighbor hopping, conductivity $\sigma = \sigma_3 \exp(-\varepsilon_3/kT)$, and for variable-range hopping, $\sigma = \sigma_o \exp(-b/T^{1/4})$. Notice that the sample grown at a high As-to-Ga BEP ratio of 40 showed only a hopping conduction at the temperatures even up to 350K. In addition, the activation energy for hopping conduction, ε_3, increases as the As-to-Ga BEP ratio increased (see Table I). The SI GaAs showed only band conduction with an activation energy of 0.75 eV.

Figure 3 shows the conductance as a function of temperature measured from Si or Be doped LT-GaAs samples. The dopant flux used during growth corresponded to a doping level of 5×10^{16} cm^{-3} in the GaAs layers grown at normal substrate temperatures. Both Si and Be doped LT-GaAs samples also showed hopping conduction behavior, but with a different activation energy ε_3. This implies that the hopping path in Be-doped LT-GaAs may be different from that in Si-doped LT-GaAs.

A Be-doped LT-GaAs sample (Be = 5×10^{16} cm^{-3}) grown using As_2 molecular species is also superimposed in the same figure. This sample appeared much more electrically resistive. The activation energy ε_3, however, remained unchanged as compared to the Be-doped LT-GaAs sample grown using As_4.

MEE-Grown LT-GaAs Doped with Be

In contrast to the MBE-grown LT-GaAs layers, MEE-grown LT-GaAs doped with Be showed a Hall mobility and carrier concentration comparable to that grown by MBE at normal substrate temperatures.[15,18] To make a direct comparison, we presented here only the plot of conductivity as a function of temperature obtained from the samples doped with

Be at 2×10^{17} cm^{-3}, as shown in Fig. 4. The results obtained from a controlled sample grown by MBE at 580°C are plotted in the same figure for comparison. It was observed that at temperatures above 25K, the control sample showed a slightly higher conductivity than that of MEE-grown samples. As the temperature dropped below 25K, however, the conductivity of MEE LT-GaAs samples exceeded that of the controlled sample, as a result of the onset of hopping conduction in MEE samples. As compared to MBE-grown LT-GaAs, the onset temperature for hopping conduction in MEE-grown LT-GaAs is substantially decreased. This is believed to be due to the controlled arsenic incorporation during MEE growth.

We extended this work to grow technologically important highly Be-doped LT-GaAs using the MEE technique. The room temperature Hall effect data, as shown in Fig. 5, indicated that MEE-grown LT-GaAs doped with Be in the range $1 \times 10^{19} \sim 1 \times 10^{20}$ cm^{-3} has the same Hall mobility as that of GaAs grown by MBE at 570°C. We used this material as the base layer for AlGaAs/GaAs heterojunction bipolar transistors (HBT) and those devices showed a useable dc common emitter current gain of 13.[18]

DISCUSSION

The experimental results clearly indicate that the electrical conduction behavior of LT-GaAs epitaxial layers can be dramatically changed using different MBE growth techniques. With controlled arsenic exposure during MEE growth, the defect density is substantially reduced and the onset temperature for hopping conduction drops to ~25K.

The hopping conduction was also observed in the conventional epitaxial GaAs[19] at temperatures below ~ 5K with an activation energy (ε_3) of 0.1~0.45 meV. Compared to this, the hopping conduction behavior observed in the LT-GaAs layers has two important features: the higher onset temperature and higher activation energy. The higher onset temperature can be attributed to the increase in hopping conductivity σ_3, which increases exponentially with the spacing between the hopping centers.[20] Hopping conduction at room temperature has also been observed in other highly disordered material systems such as high-dose neutron irradiated GaAs.[21]

The ε_3 obtained from LT-GaAs materials was significantly higher than that of conventional epitaxial GaAs layers. Moreover, this activation energy increased with the arsenic beam flux used for growth. This higher activation energy and its trend of change with arsenic flux cannot be simply explained in terms of the strong overlapping of the defect wave function caused by the high density of defects. Actually, we expect the overlap of donor wave function to reduce the activation energy, not increase it.[20] As the density of donors increases, eventually ε_3 disappears and as a result, metallic impurity conduction occurs, which would show no temperature dependence. In contrast, the ε_3 measured for LT-GaAs materials is high.

The high activation energy observed for hopping

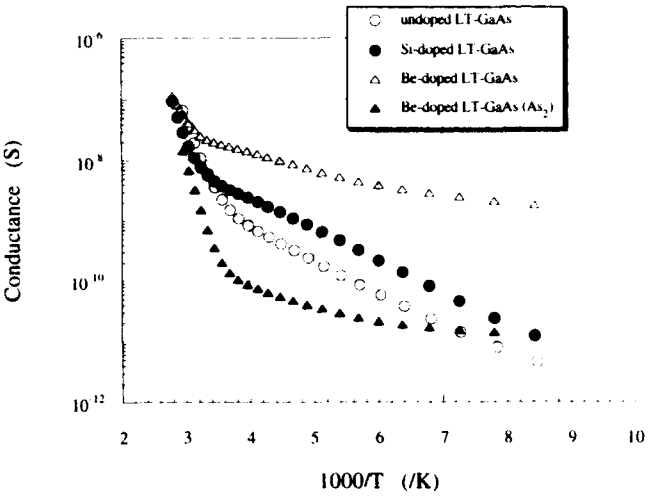

Fig. 3. Plot of conductance vs reciprocal temperature for doped MBE-grown LT-GaAs. The dopant flux used corresponded to a doping level of 5×10^{16} cm^{-3} in the GaAs layers grown at normal substrate temperatures.

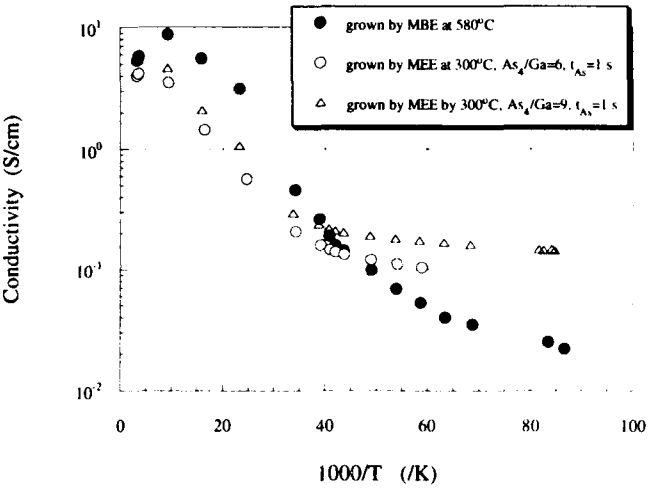

Fig. 4. Plot of conductivity vs reciprocal temperature for MEE-grown LT-GaAs doped with Be at 2×10^{17} cm^{-3}.

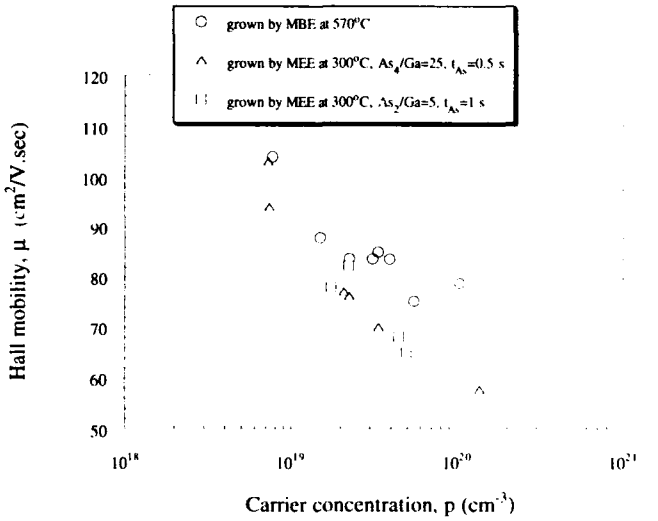

Fig. 5. Plot of room temperature Hall mobility of highly doped Be doped GaAs grown at different conditions.

conduction in LT-GaAs samples might be qualitatively explained in terms of the effect of strain and a spatial fluctuation in the electron potential. X-ray diffraction results indicated an expansion in the lattice constant of an LT-GaAs epitaxial layer, so this layer is presumably under biaxial compressive strain. It was previously reported[22] that for Sb-doped Ge under uniaxial compression, ε_3 increased from ~1.37 meV to ~2.42 meV. The effect of strain was more pronounced at a high density of donors (i.e., there is a strong overlapping), because the strain can cause changes in either the donor wave function or the overlap between wave functions of neighboring donors.

In addition, the defects in LT-GaAs are expected to be randomly distributed, particularly for Ga vacancies, because of the very low surface mobility of Ga adatoms during low-temperature MBE growth. This will lead to a random and localized spatial potential fluctuation in this material, which will enhance the energy barrier (ε_3) for hopping conduction. These two factors, strain and potential fluctuation, may need to be taken into account in any further attempt to quantitatively model the hopping process in LT-GaAs.

For doped LT-GaAs layers, the situation is more complicated. The presence of shallow dopants Si and Be affected ε_3. The changes in ε_3 might be associated with a possible change in defect structure and density due to the presence of the shallow dopants. The effect of shallow dopants has been observed in our study on Schottky barrier height modification using thin LT-GaAs cap layer[17] and others.[23] Further work needs to be done to reveal the role of shallow dopants in growth and resulting defect structures of LT-GaAs materials.

CONCLUSIONS

Our study indicates that the arsenic beam flux and the presence of shallow dopants affect the hopping conduction behavior in MBE-grown LT-GaAs. Using MEE growth technique, we can substantially reduce the onset temperature for hopping to 25K in Be-doped LT-GaAs material and achieve a good Hall mobility in highly Be-doped LT-GaAs. Thus, the electrical properties of LT-GaAs can be engineered for different device applications, such as Schottky barrier height modification,[17] and use in the base of AlGaAs/GaAs HBTs.[18]

ACKNOWLEDGMENTS

The authors wish to thank Dr. Noran Pan for providing temperature-dependent conductivity data for MEE-grown LT-MEE samples, Professor D.C. Look for very useful discussion. This work is supported in part by the U.S. Army Research Office

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Diode Structures from Amorphous Low-Temperature GaAs

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The effect of annealing on the electrical properties of a GaAs diode structure, which incorporated a nominally undoped low-temperature (LT) layer on top of conventionally grown p-type GaAs, is examined. Unannealed GaAs grown by molecular beam epitaxy at substrate temperatures below 250°C is amorphous and highly resistive. Annealing at high temperatures converts the undoped LT-GaAs from amorphous to single crystal material. The annealed material is n-type. The current-voltage characteristics of the LT on p-type GaAs structures showed greater asymmetry, with lower reverse leakage currents, as the anneal temperature was increased above 400°C. This reflects the improved crystal quality of the LT layer.

Key words: Annealing, low-temperature-grown GaAs, MBE

INTRODUCTION

Low-temperature GaAs (LT-GaAs) is of technological importance for both electronic[1-3] and optoelectronic[4-8] applications. The term LT-GaAs is generally used to refer to material grown by molecular beam epitaxy (MBE) at a substrate temperature, T_s, below 460°C.[9,10] We have previously shown that there are major physical and electrical differences between material grown at a T_s of less than 250°C and that grown between 260 and 460°C.[11] Most of the LT-GaAs studies in the literature deal with material grown above 250°C.[12-15]

This paper deals with MBE GaAs grown at 120°C. As grown, this material is amorphous and highly resistive. After a high-temperature anneal, the LT-GaAs is single crystal and becomes highly conductive with n-type conductivity. The ability to introduce n-type carriers through defect levels may be useful in cases where impurity doping is difficult. Though demonstrated in LT-GaAs, this capability may be applicable to other III-V materials, like AlSb, which are not easily made n-type with the use of conventional III-V n-type dopants.

We have grown LT-GaAs by MBE on a conventional, p-type, GaAs layer and used this structure to study the effect of annealing on the electrical properties of the LT-GaAs. The electrical measurements were correlated with a variety of material characterization techniques: transmission electron microscopy (TEM), double-crystal x-ray diffraction, photoreflectance (PR), and electron channeling.

EXPERIMENTAL

The LT/p-type GaAs layer structure was grown on a semi-insulating GaAs (100) substrate with an As_4-to-Ga beam equivalent pressure ratio of 18 and a growth rate of 1 μm/h. First, a 500 nm thick, 5×10^{18} cm^{-3} Be doped, GaAs layer was grown at 540°C. The growth was then interrupted while T_s was lowered to 120°C, under an As overpressure of 8×10^{-6} Torr. After the temperature stabilized, a 400 nm thick, nominally undoped, LT-GaAs layer was grown. Additional LT samples were also grown without the underlying p-type layer for use in the material characterization studies.

(Received April 12, 1993)

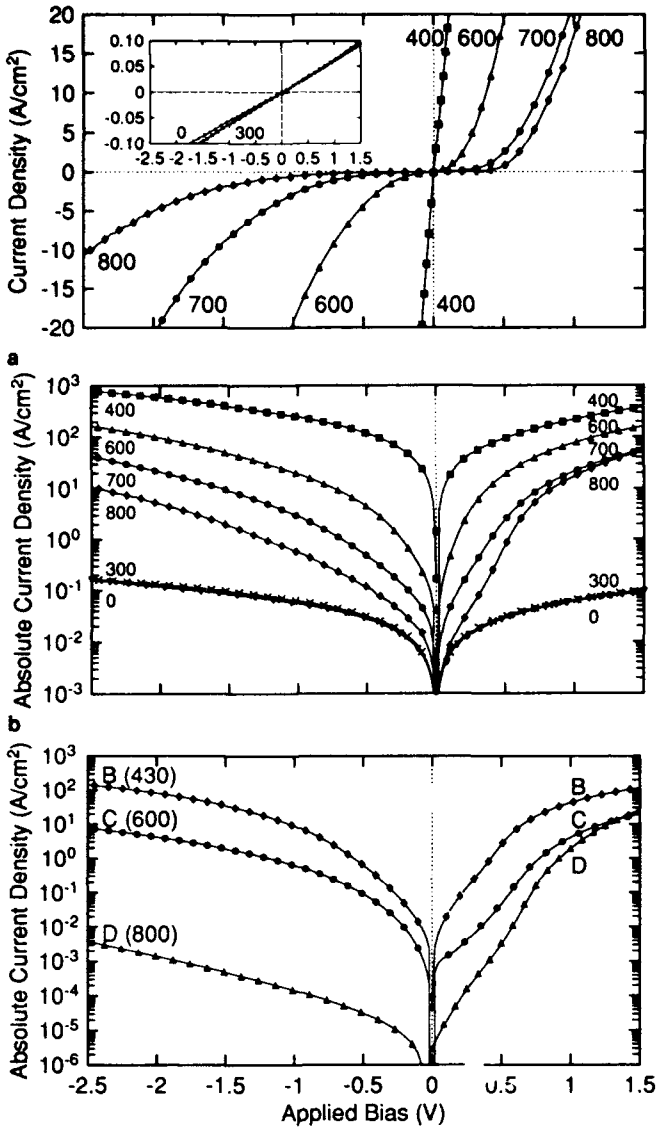

Fig. 1. (a) Typical electrical characteristics for the sample A devices after sequential anneals at T_A = 0 (as-grown), 300, 400, 600, 700, and 800°C. In the inset is a magnified view of the curves for T_A = 0 and 300°C. (b) The same curves in (a) displayed with the absolute current density on a logarithmic scale. (c) Typical electrical characteristics for samples B–D, annealed before device fabrication.

Samples were annealed before and after fabrication of diode mesa structures. Proximity anneals were performed in a rapid thermal anneal system. Sample A was annealed sequentially at temperatures of 300, 400, 600, 700, and 800°C after diode fabrication. Samples B, C, and D were annealed before diode fabrication at temperatures of 430, 600, and 800°C, respectively. For sample B, the ohmic contact alloy at 430°C effectively served as a LT-GaAs anneal. The anneal time, t_A, was limited to 60 s for the LT/p-GaAs samples to minimize Be out-diffusion at the higher anneal temperatures, T_A. As-grown and annealed samples were analyzed by secondary-ion mass spectroscopy (SIMS) to determine the extent of Be diffusion into the LT layer. The anneal times were varied

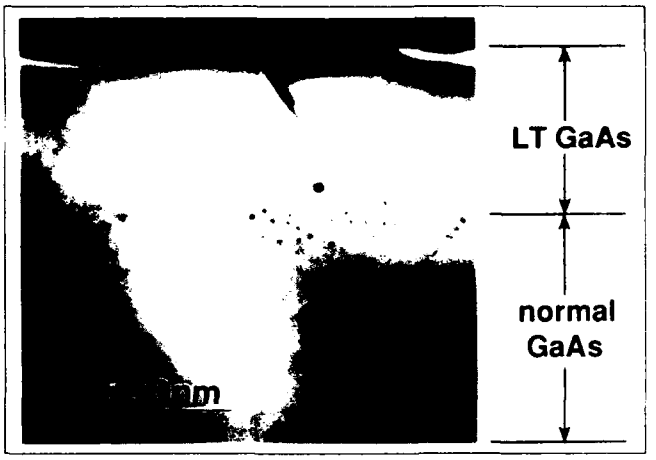

Fig. 2. Cross-sectional TEM picture of annealed (T_A = 775 C, t_A = 600 s) LT-GaAs. Arsenic precipitates (~10 nm in diam) are concentrated near the interface between the LT-GaAs and the normal GaAs layers.

for the LT-GaAs samples grown without the p-type layer. Anneal times of up to 600 s were investigated. The mesa structures were defined using conventional photolithography. Sample A devices employed unannealed Ti:Pt:Au contacts for both the LT and the p-type GaAs layers. On samples B–D, AuGe:Ni contacts to the top LT layer were deposited first and alloyed at 430°C. After mesa definition, Cr:Au contacts were defined onto the p-type GaAs layer and sintered at 300°C.

RESULTS AND DISCUSSION

Typical current-voltage characteristics for structures made from sample A (annealed after diode fabrication), following each high-temperature (300°C $\leq T_A \leq$ 800°C) anneal, are shown in Fig. 1. The large resistance associated with the linear characteristic for the unannealed devices (inset of Fig. 1a) was attributed to the high resistivity, ρ, of the as-grown LT-GaAs. A ρ of 3×10^5 Ω-cm was calculated, under the assumption that the layer accounted for virtually all of the device resistance. Double-crystal x-ray diffraction, TEM, and PR measurements all showed that the as-grown LT-GaAs was amorphous. An anneal at 300°C increased the device conductivity only slightly (inset of Fig. 1a). After a 400°C anneal, the characteristics remained linear; however, the conductivity increased dramatically (Fig. 1a). If the device resistance is again attributed to the LT layer, then a ρ ~ 1×10^2 Ω-cm is obtained. This ρ was still relatively large; although, it was more than three orders of magnitude lower than that calculated for the as-grown material. An increasing asymmetry in the characteristics was observed for T_A > 400°C (Figs. 1a and 1b). The reverse current increased by four orders of magnitude after annealing at 400°C, but decreased steadily with each increase in T_A. The electrical characteristics for structures made from samples B–D (annealed before diode fabrication), shown in Fig. 1c, exhibit similar behavior as seen in the sample A devices (Figs. 1a and 1b), evolving toward a rectifying characteristic with increasing T_A.

The increase in device conductivity after the 400°C anneal suggested an improvement in the LT layer crystal quality, possibly signaling a change from an amorphous to a polycrystalline phase. Our TEM study indicated a change from amorphous to polycrystalline material following isochronal (t_A = 600 s) 550°C anneals, while anneal temperatures above 775°C converted the LT layer from amorphous to single crystal material.[16] The double-crystal x-ray rocking curve full width at half-maximum for samples annealed above 775°C was 10 arc-s, which indicated crystal quality comparable to that of the substrate. Isothermal anneals were also performed at 600 and 775°C. The TEM analysis showed a complete and rapid change of the as-grown amorphous LT layer to polycrystalline material (~15 s at 600°C). This was followed by a gradual conversion of the polycrystalline layer to single crystal GaAs (~1 h at 600°C for complete conversion). Recrystallization progressed from the interface toward the surface with a faster rate of recrystallization at the higher T_A. This process differed from that observed in the annealing of ion-implant damaged GaAs where only an amorphous-to-crystalline transition occurs.[17]

The TEM analysis alsc revealed As precipitates concentrated within a 100 nm wide region near the interface between the LT and the conventionally grown GaAs (Fig. 2). Our observations of moiré imaging effects are consistent with those expected for As precipitated in GaAs. The precipitates formed with a typical diameter of 10 nm and a density of 10^{15} cm^{-2}. This resulted in an As precipitate volume fraction within the LT-GaAs of 0.02%, lower than the typical 1% volume fraction in annealed material grown above 200°C.[12] However, more As incorporation is expected at growth temperatures below 200°C because of the reduced As vapor pressure and improved sticking coefficient with the expected result of at least 1% excess As in the films. No As loss from the surface was observed after annealing, consistent with the use of a GaAs proximity cap during the anneals. Therefore, the small volume fraction of precipitates suggested that a large density of As-related defects remained after the high temperature anneals. These defects may activate as donors and contribute to the high n-type carrier concentrations (10^{18} cm^{-3}) found in the annealed LT-GaAs.

A dependence of LT-GaAs crystal quality on anneal times was also determined through PR measurements. The as-grown material displayed no PR signal, which indicated a highly defected layer. Annealing the sample at 775°C for 30 s produced a PR spectra showing a weak structure near the band gap energy of 1.42 eV (Fig. 3). A change in the PR signal was observed in samples annealed for longer times at 775°C. Following a 192 s anneal, a well-defined peak at 1.42 eV with a pronounced excitonic structure and a peak at 1.75 eV due to spin-orbit splitting were clearly visible in the PR spectra (Fig. 3), indicating that the material was single crystal. Electron channeling measurements provided a rough indication of the minimum anneal time necessary to convert the LT-GaAs from an amorphous to a single crystal structure. Higher anneal temperatures lead to progressively shorter anneal times for conversion with t_A of 150, 25, and 8 s required for T_A of 730, 800, and 900°C, respectively. These results suggested that the 60 s anneal at 800°C for the LT/p-GaAs structures was of sufficient duration to convert the as-grown amorphous LT layer into single crystal material.

The SIMS analysis identified diffusion of Be both toward the surface and into the substrate after annealing at 800°C for 60 s, with slightly greater movement into the LT layer (Fig. 4). The high n-type carrier concentration in the annealed material preserved the n/p structure despite the observed Be diffusion toward the surface. However, a graded doping region was formed, extending about 0.2 μm into the annealed LT material.

CONCLUSIONS

The effects of high-temperature anneals on the electrical and physical properties of LT-GaAs grown by MBE on conventional, p-type, GaAs have been investigated. Material characterization revealed that

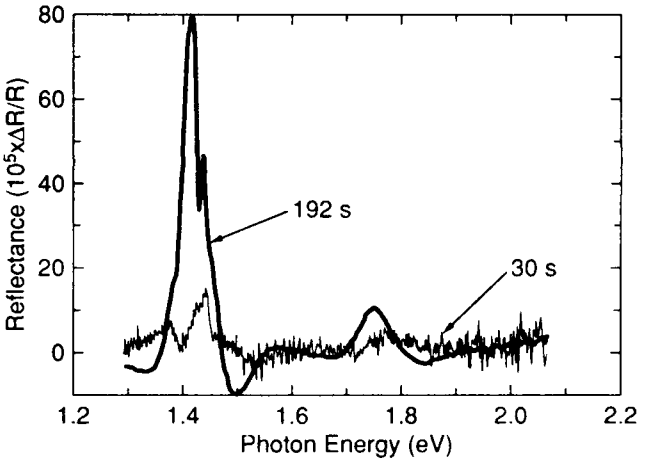

Fig. 3. Photoreflectance spectra for samples annealed at 775 C for 30 and 192 s.

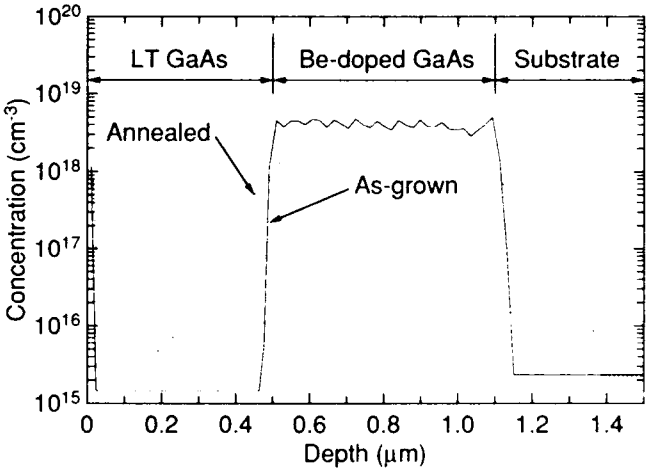

Fig. 4. Beryllium profile obtained from SIMS for as-grown and annealed (T_A = 800 C. t_A = 60 s) samples.

the LT-GaAs converted from amorphous to single crystal material after sufficient high-temperature anneals. The annealed LT material displayed a high net n-type carrier concentration, effectively creating a single crystal n/p GaAs structure. The electrical behavior of the LT/p-GaAs structures changed from a linear (highly resistive) to a nonlinear (rectifying) characteristic after moderate anneal temperatures (>400°C). The diode characteristics improved with higher anneal temperatures (>600°C), apparently benefiting from an improvement in the crystal quality of the LT layer.

ACKNOWLEDGMENTS

The authors wish to thank H.B. Dietrich and S.C. Binari of the Naval Research Laboratory for valuable discussion and support, and J. Mittereder of SFA, Inc. for technical assistance. This work was supported by the U.S. Office of Naval Research.

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Effects of Heat Treatment on the 0.8 eV Photoluminescence Emission in GaAs Grown by Molecular Beam Epitaxy at Low Temperatures

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We report 0.8 eV photoluminescence (PL) emission of GaAs grown at low temperatures between 325 and 400°C by molecular beam epitaxy. Effects of heat treatments of the 0.8 eV emission are compared with those of the 1.467 eV sharp bound exciton lines. This allows us to attribute the 0.8 eV emission to the As_i-V_{Ga} center. We discuss the assigning of the As_i–V_{Ga} center to the well-known EL6. The PL intensity variation of 0.68 eV EL2 and 0.8 eV As_i–V_{Ga} seen in substrate materials is explained in terms of dislocation—mediated As_i-V_{Ga} transformation to EL2 whereas the PL intensity variation of 0.8 eV As_i-V_{Ga} for molecular beam epitaxy layers can be attributed to the growth condition.

Key words: Defects, low-temperature-grown GaAs, MBE, photoluminescence

INTRODUCTION

Molecular beam epitaxy (MBE) GaAs is normally grown at substrate temperature T_G = 580–600°C. However, low temperature (LT) GaAs grown at T_G <500°C has recently attracted much attention because of the unique material properties and excellent device performances. The LT materials have been shown to be very nonstoichiometric[1] with up to 1 at. % excess As for the material grown at 200°C. The excess As is incorporated as ~10^{20} cm^{-3} As-antisite-related centers in as-grown materials[1] and primarily as As precipitates in annealed materials.[2] Assessment of LT materials must address the excess As and the associated intrinsic defects: the As antisite (As_{Ga}), gallium vacancy (V_{Ga}), arsenic interstitial (As_i), and associated pair defects. Deep-level emission originating from the defects can be expected to dominate the radiative mechanism of LT GaAs. Viturro et al.[3] observed a cathodoluminescence emission at ~1 eV from a 250°C grown material and assigned it to a transition involving EL2 and the valence band. Also, Ohbu et al.[4] observed a photoluminescence emission at 1.24 eV from a 300°C grown and 800°C annealed material which was assigned to a transition involving V_{Ga}.

We report here a PL emission band at ~0.8 eV which dominates the deep-center radiative mechanism for LT MBE GaAs grown at the temperatures between 325 and 400°C. Temperature-dependent measurements allow us to determine the thermal ionization level of the center responsible for the 0.8 eV emission. In particular, the heat treatment behavior of the 0.8 eV emission is compared with that of the sharp bound exciton lines[5] at ~1.467 eV. The comparison allows us to identify the center responsible for the 0.8 eV emission as an (As_i–V_{Ga}) C_{3V} type defect. The 0.8 eV emission is also compared with the one present in liquid encapsulated Czochralski (LEC) and vertical gradient freeze (VGF) substrate materials. We find that our assignment of the (As_i–V_{Ga}) for the 0.8 eV emission is consistent with all the experimental findings.

DISCUSSION

The MBE layers were grown in a Varian Gen-II system under As_4 using a non-indium bonded substrate holder. Growth temperatures were 325, 350,

(Received April 12, 1993)

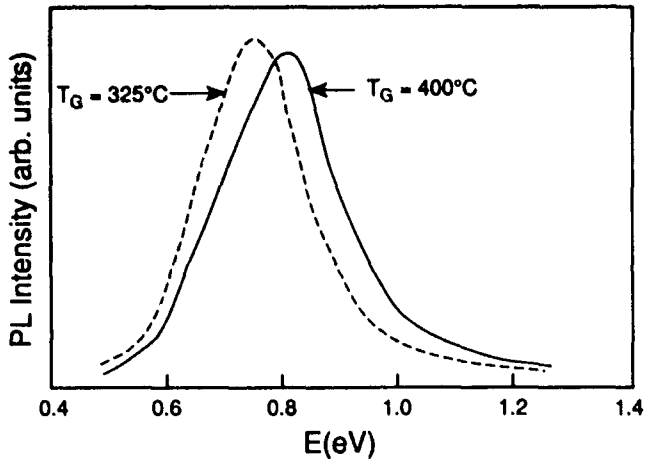

Fig. 1. Photoluminescence spectra from LT GaAs grown at (a) 325°C and (b) 400°C.

and 400°C and were determined by a noncontacting thermocouple. Details of the growth are explained elsewhere.[5] Photoluminescence measurements were measured using a variable-temperature Janis optical dewar. The 5145Å line of an Ar-ion laser was used as an excitation source with an intensity of $10^{-2} - 10^{1}$ W/cm^2. Photoluminescence spectra were obtained with Spex monochromators of focal length f = 0.5 and 1.29 m and were detected with a C31034 photomultiplier tube, a liquid-nitrogen cooled Ge and a liquid-nitrogen cooled InAs detector. Standard synchronous techniques were used with a lock-in amplifier. Heat treatments were performed at 200–700°C for 20 min in a furnace purged with flowing N_2. Another GaAs wafer was placed on top of the LT layer during heat treatments in order to inhibit As loss.

Figure 1 shows 2K PL spectra of 325 and 400°C grown layers. Photoluminescence emissions at 0.75 and 0.81 eV emerge, respectively, from 325 and 400°C grown layers. We designate two peaks near 0.8 eV as "the 0.8 eV emission" considering the proximity of the peak position. The 0.8 eV PL emission was first reported[6] in LEC semi-insulating GaAs substrates and has been the subject of a number of subsequent PL investigations.[7–11] The origin of the 0.8 eV emission has been suggested to be an association with "microdefects"[7] and the second level[8] of As_{Ga}. However, a consistent observation[7,8] with respect to the 0.8 eV emission is that it has an M-shaped intensity profile across the diameter of a semi-insulating wafer, in contrast to the W-shaped profiles for the C_{As}-related 1.49 eV emission and the 0.68 eV EL2 emission.[12] Recently, Shinohara[13] studied the 0.8 eV emission from MBE GaAs layers grown at 550–730°C and attributed the 0.8 eV emission to an As_{Ga}–V_{As} center.

We measured the temperature dependent PL spectrum of the 0.8 eV emission in the temperature range of 2–150K. The PL intensity and line shape do not change over the temperature range 2–50K. For temperature greater than 50K, the PL intensity of the 0.8 eV emission decreases and the overall spectrum shows the presence of two overlapping components, the original 0.8 eV emission and the emerging 0.68 eV

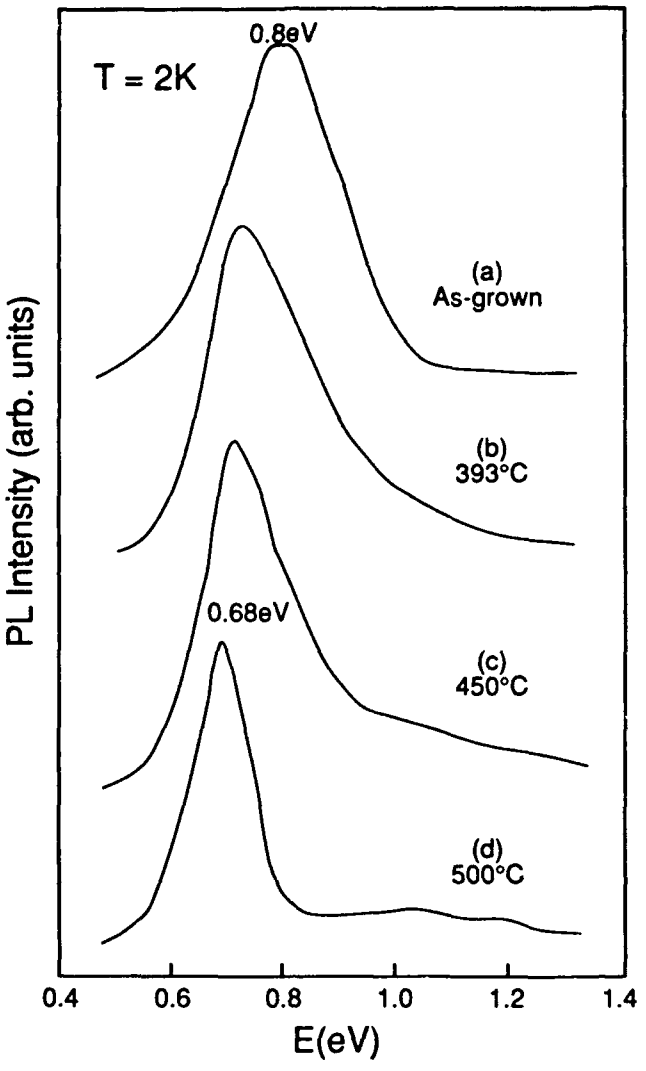

Fig. 2. 0.8 eV photoluminescence spectra from (a) as-grown, (b) 393°C annealed, (c) 450°C, and (d) 500°C annealed samples. All samples are from one wafer grown at 400°C.

emission. The known PL characteristics[12] of the 0.68 eV EL2 emission were used to extract the 0.8 eV emission. The obtained full width at half maximum of the 0.8 eV emission yields the values of the Huang and Rhys constant and the Franck-Condon shift, 8.9 and 0.344 eV, respectively. The thermal ionization energy E_{th} for the center responsible for the 0.8 eV emission can be obtained using the Franck-Condon shift and is determined to be E_{th} = 0.36 eV.

Figure 2 shows PL spectra obtained for the 0.8 eV emission from an as-grown sample grown at 400°C and from samples annealed at 393, 450, and 500°C measured over the energy range 0.5–1.2 eV. The PL intensity of the 0.8 eV emission decreases with increasing annealing temperature for temperatures of 300 to 450°C and the 0.68 eV emission appears with the decreasing intensity of the 0.8 eV emission. After heat treating at 500°C, the only radiative process is the 0.68 eV EL2 emission. With complete quenching of the 0.8 eV emission, the intensity of the 0.68 eV emission increases slightly. We attribute the increase

to dissociation of the center responsible for the 0.8 eV emission and to transformation into EL2. These heat-treatment effects of the 0.8 eV emission were compared with those[14] of the exciton bound to the C_{3v}-symmetric As_i-V_{Ga} center as reported[5] earlier, which is from the same sample used in Fig. 2. Figure 3 shows the sharp-line PL spectrum of an as-grown sample in the energy range 1.41–1.48 eV. The PL consists of no-phonon lines ("1," "1'," "2," and "3") at ~1.47 eV and associated phonon sidebands of both lattice and localized vibrational modes of the As_i–V_{Ga}. The gradual decrease of no-phonon line intensities with increasing annealing temperature (not shown) and the disappearance of all the sharp lines with 500°C annealing are consistent with the characteristics of annealing effects on the 0.8 eV center; i.e., the gradual peak shift to 0.68 eV emission with decreasing intensity of the 0.8 eV emission and the disappearance of the 0.8 eV emission with 500°C annealing. These experimental observations allow us to assign the center responsible for the 0.8 eV emission to the As_i-V_{Ga} center. The variation of PL excitation intensity with laser intensity in the range of 10^{-2} – 10^{1} W/cm^2 did not change the peak position and lineshape of the 0.8 eV emission. This indicates that the 0.8 eV emission is a transition from the As_i–V_{Ga} to the band edge.

Let us now consider the result of two previous works on EL6 and EL2 in neutron irradiated[15] and B-implanted[16] GaAs. The irradiation or implantation induced the formation of two donors, EL6 (E_C–0.35 eV) and EL2. An annealing study after the irradiation or implantation showed

- that there is an interaction between EL2 and EL6, and
- that at the annealing temperatures in the range 400–600°C, EL6 decreases by a pair-defect type dissociation whereas EL2 increases with increasing heat-treatment temperature.

These heat-treatment characteristics are almost the same as those of the 0.8 eV As_i–V_{Ga} and the 0.68 EL2 emission as discussed in connection with Fig. 2. Based on the almost identical value of the deduced thermal ionization energy of the As_i–V_{Ga} center and the measured energy of EL6, and the characteristics of EL6 and EL2 in the above experiments,[15,16] we tentatively attribute EL6 to the As_i–V_{Ga} center. If we assume that EL2 is the isolated[17] As_{Ga} we can describe the dissociation and transformation processes of the As_i-V_{Ga} as follows:

$$(As_i - V_{Ga}) \rightarrow As_i + V_{Ga}$$
$$(As_i - V_{Ga}) \rightarrow As_{Ga}$$

It is clear that these processes can explain the results of the above heat-treatment on the As_i-V_{Ga} center and EL2. Then, the 0.8 eV emission is the transition from EL6 to the valence band.

Figure 4 shows the intensity variation of the 0.8 eV emission along the <110> direction across a wafer for a LEC semi-insulating material and LT MBE crystals grown at 325 and 400°C. The LEC GaAs shows the usual[7,8] W shape for the 0.68 eV EL2 emission and M shape for the 0.8 eV As_i–V_{Ga} emission. The LT MBE layers show relatively flat profiles with slight decreases at the edge regions for the 400°C layer. We find that the substrate on which the 400°C layer was grown has only the 0.68 eV EL2 emission. Thus, the intensity profile of the LT layer unambiguously originates from the layer. The edge region of the 400°C layer exhibits transitions due to the Cu_{Ga} center at 1.35 eV and ~1.1 eV in addition to the 0.8 eV emission in contrast to only the presence of the 0.8 eV emission in the central region. We tentatively attribute the 1.1 eV emission to a V_{Ga}-related emission. The two transitions can be considered to originate from the non-uniformity of the crystal growth at the edge region. The PL intensities are influenced by the carrier concentration (n) and the trap concentration (N_T). The

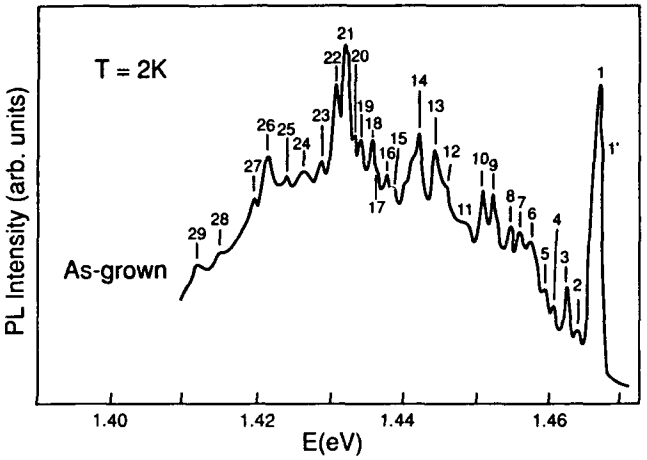

Fig. 3. Sharp-line emission spectrum from the as-grown sample used in Fig. 2a.

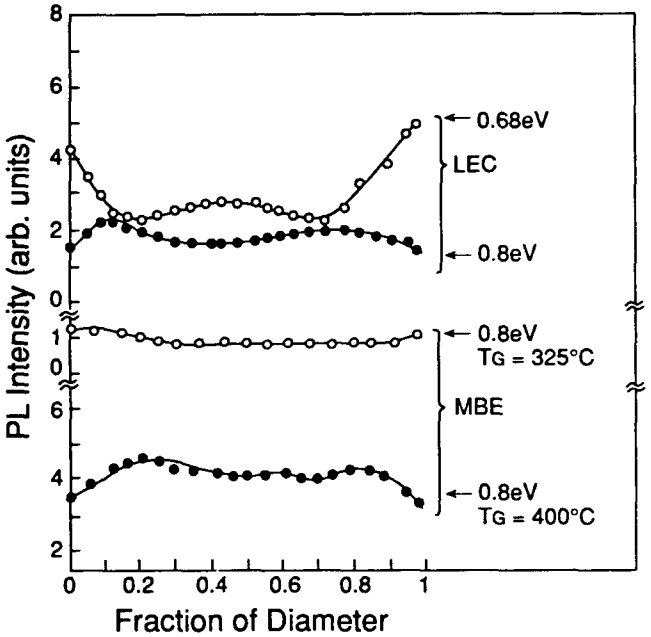

Fig. 4. (a) Relative PL intensity of the 0.68 eV EL2 and 0.8 eV As_i–V_{Ga} emissions along the <110> direction in wafers grown by LEC, and relative PL intensity of the 0.8 eV As_i–V_{Ga} emission along the <110> direction in wafers grown by (b) MBE at 325 C, and (c) MBE at 400 C. The diameters are 3 and 2", respectively, for LEC and MBE wafers.

carrier concentration is determined by the product of the carrier lifetime and carrier generation rate. The spatial distributions of carrier lifetime[18] and dislocation density[7] along the <110> direction across a LEC wafer show W shapes in contrast to the M shape[7,8] of the 0.8 eV emission. This indicates that the center responsible for the 0.8 eV emission increases in number causing the observed increase in PL intensity, that the concentration of As_i-V_{Ga} is larger in the region where dislocation density is lower, and that dislocations produce EL2 in the region where dislocation density is higher. The production of EL2 by dislocation climb is well proven[19,20] for LEC materials. An example of a bulk material with only the 0.8 eV emission is found in VGF materials[21] where the dislocation density is lower by about one order of magnitude compared to that in LEC GaAs. These experimental results are consistent with the observation that the lower dislocation densities in the VGF materials generate lower EL2 densities, consistent with our model.

CONCLUSION

In conclusion, the effects of heat treatments on the 0.8 eV emission and the ~1.467 eV exciton bound to the As_i–V_{Ga} center allow the center responsible for the 0.8 eV to be identified as an As_i–V_{Ga} center. The temperature dependent characteristics of the 0.8 eV emission show the strong electron phonon interaction of the As_i–V_{Ga} center. Thus, I would suggest "we propose assignment of the As_i–V_{Ga} center to EL6." Variation of PL intensity for the 0.68 eV EL2 emission and 0.80 eV As_i–V_{Ga} emission in LEC wafers are attributed to dislocation mediated dissociation of the As_i–V_{Ga} center and transformation to EL2. Spatial variations in these intensities for MBE layers are attributed to the nonuniformity of crystal growth condition.

ACKNOWLEDGMENTS

We gratefully acknowledge the technical assistance of W. Rice, J.E. Ehret, and E. Taylor. The work of P.W.Y. was performed at Wright Laboratory, Solid State Electronics Directorate (WL/EL), Wright-Patterson Air Force Base under Contract No. F33615-91-C-1765. This work was partially funded by the U.S. Air Force Office of Scientific Research.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Infrared Studies of Be-Doped GaAs Grown by Molecular Beam Epitaxy at Low Temperatures

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Samples of molecular beam epitaxial GaAs grown at low temperatures doped with Be defects are studied as a function of growth temperature (T_G) by measuring their localized vibrational modes at 77K using BOMEM Fourier transform infrared spectrometer. Localized vibrational modes of $^9Be_{Ga}$ in samples grown at T_G >350°C have been identified at 482 cm^{-1}. Secondary ion mass spectroscopy measurements show that the densities of Be defects remain approximately constant as T_G is lowered, however, additional structure in the $^9Be_{Ga}$ localized vibrational mode is observed. Calculations based on Green's function theory suggest that the additional structure in Be-doped LT GaAs can best be explained in terms of a complex center [$^9Be_{Ga}$-As_{Ga}] involving an intrinsic defect.

Key words: LT-GaAs, Fourier transform infrared spectrometer (FTIR), localized vibrational modes (LVM), Green's function

INTRODUCTION

Gallium arsenide grown at low temperatures (LT-GaAs) by molecular beam epitaxy (MBE) on GaAs substrates exhibit electrical and optical properties which are distinct from those observed when the layers are grown at the "usual" high temperature (HT) range; e.g., T ~600°C. It has been shown in recent years that an MBE grown LT-GaAs buffer layer deposited at 200°C exhibits an extremely high resistivity after a 600°C annealing treatment.[1,2] Metal semiconductor field effect transistors fabricated on the annealed LT-GaAs buffer layer showed an improved performance compared with devices grown directly on a semi-insulating GaAs substrate obtained from the liquid-encapsulated Czochralski (LEC) method.[3]

Despite numerous experimental studies performed in recent years, the nature of intrinsic defects responsible for the high resistivity of LT-GaAs is not yet well understood. It is clear, however, that the concentration of such defects in LT-GaAs is very high (~10^{18}–10^{20} cm^{-3}) compared to the concentration of intrinsic defects (10^{14} cm^{-3}) found in HT MBE GaAs layers. Among the various possible intrinsic defects in LT-GaAs (e.g., As_{Ga}, As_i, V_{Ga}, etc.), only an arsenic antisite (As_{Ga}) related-defects have been identified by electron paramagnetic resonance.[4] Recent Hall, and positron annihilation measurements have also suggested that the dominant acceptor in LT-GaAs is a Ga-vacancy (V_{Ga}).[5]

Infrared (IR) absorption local mode spectroscopy has proven to be a useful technique for the identification and characterization of both intrinsic and doped defects in semiconductors.[6] The impurity-induced IR absorption is caused by the breakdown of translational symmetry and the consequent relaxation of selection rules relating to the conservation of wave vectors. The absorption spectrum is expected to have features in common with one-phonon density of states of the host lattice. In addition, one expects relatively sharp absorption lines from specific defects if their natural modes of vibrations lie in the region where the density of phonon states is low.

In HT GaAs for example, a light impurity Be_{Ga} (with T_d symmetry) produces a triply-degenerate high

(Received April 12, 1993)

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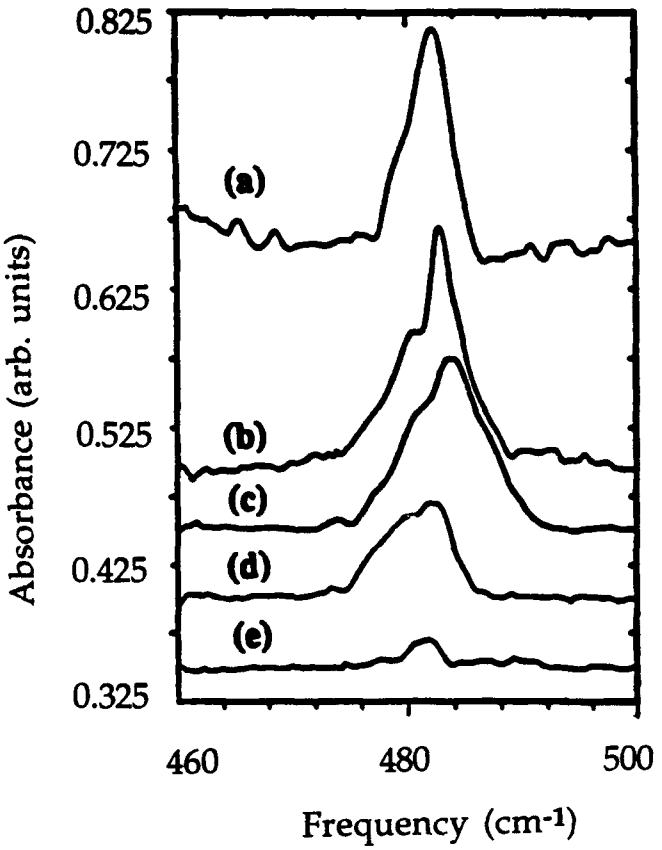

Fig. 1. The 77K localized vibrational mode absorption spectra of Be_{Ga} in LT-GaAs layers grown at (a) 325°C, (b) 300°C, (c) 275°C, (d) 250°C, and (e) 200°C.

frequency localized vibrational mode (LVM) far from the maximum phonon frequency of GaAs, which can be detected as a relatively sharp feature in the infrared absorption spectrum. An intrinsic defect As_{Ga}, on the other hand, resembles an impurity for which there is no significant mass change but the "impurity-host bonding" is modified. Due to the variation of "impurity-host bonding," it is feasible that As_{Ga} may give rise to an inband resonance mode similar to phosphorus impurity in a silicon lattice (P_{Si}).[6] If Be_{Ga}-As_{Ga} forms an acceptor-donor pair, as might be the case in Be-doped LT-GaAs, then the point group symmetry at the Be_{Ga} site will be reduced from $T_d \rightarrow C_s$. Such a reduction in the symmetry lifts the degeneracy of the Be_{Ga} LVM and thus modifies the absorption spectrum. This modification of IR spectrum can be used to monitor possible evolution of the formation of complex defect-centers involving impurities and intrinsic defect(s). Although the symmetry of such complex-centers can be determined, their identification relies strongly on supplementary data including realistic model calculations.[7]

In this letter, we present the results of IR absorption measurements for Be acceptors in LT-GaAs layers grown by MBE at temperatures (T_G) ranging from 200 to 325°C. The LT-GaAs layers were deposited on LEC-grown semi-insulating GaAs substrates under normal As-stabilized conditions. A growth rate of 0.8 μm/h, and a V/III flux ratio ~20 was used. Layer thicknesses varied between 2 to 4 μm. Absorption spectra were recorded by using BOMEM Fourier transform infrared (FTIR) spectrometer with a resolution of 0.25 cm^{-1} after cooling the sample at 77K.

EXPERIMENTAL

Measured LVMs near 482 cm^{-1} from five GaAs samples grown at different temperatures, all nominally doped with ~7×10^{19} cm^{-3} of Be are displayed in Fig. 1. In an earlier study of LEC GaAs doped with high concentration of Be, we observed a sharp and pronounced absorption of LVM near 482 cm^{-1}. To carry out IR measurements, the sample was irradiated with 2 MeV electrons to remove the free carrier absorption. A similar study of LVM induced by Be near 482 cm^{-1} in HT MBE GaAs has been reported by Wagner et al.[8] We, therefore, associate the observed LVM at 482 cm^{-1} as Be_{Ga}. The absorption data for LT GaAs:Be samples displayed in Fig. 1 reveal that for samples grown at increasingly lower T_G, the total integrated absorption of Be_{Ga} LVM is also decreased. Also at lower T_G, a low frequency shoulder near Be_{Ga} LVM starts to emerge. Our secondary ion mass spectroscopy (SIMS) results indicate that the concentration of Be impurities are approximately constant for all the samples. The additional structure in the LVM suggests that the symmetry at Be_{Ga} site is lowered. This lowering of symmetry may arise from the interaction of Be_{Ga} with either non-substitutional Be or intrinsic defects. The stress-strain in the GaAs layers is ruled out as being the cause of the Be_{Ga} LVM structure in Fig. 1. This assertion is based on our results from thermal annealing of the sample that gave spectrum (b) in Fig. 1 which indicates that there is no significant difference between the LVM before and after annealing the sample at 650°C for 30 min. Based on our Green's function calculations, it will be shown that intrinsic defects (e.g., V_{Ga}, As_{Ga}, etc.) in GaAs can produce low frequency inband modes and the structure in the Be_{Ga} LVM observed at low T_G arises from a pair [Be_{Ga}-As_{Ga}] defect of C_s symmetry.

THEORETICAL CALCULATIONS RESULTS AND DISCUSSIONS

Our theoretical description of LVMs due to defects in GaAs consists of two parts. In the first step, we used a bond-orbital model (BOM) to calculate lattice distortions caused by isolated defects (e.g., Be_{Ga}, As_{Ga}, etc.) in GaAs. In the second step, the frequencies of impurity vibrations are obtained by using a Green's function theory.[7] In setting up the dynamical matrix in the Green's function formalism, we evaluated all the involved Green's function (G^o) matrix elements numerically by incorporating phonons generated by an 11 parameter rigid-ion-model (RIM11) fitted to the inelastic neutron scattering data of GaAs.[9] The nearest-neighbor (nn) force constant changes caused by defects are properly included in the perturbation matrix (P) and the frequencies of LVMs are obtained by setting the determinant of the dynamical matrix [Re | I-G^oP | = 0] equal to zero.

For isolated defects (viz. Be_{Ga}, Si_{Ga}, As_{Ga}, etc.), it is convenient to express the Green's function and perturbation matrices of dimension (15 × 15) in the basis of symmetry coordinates. The 15-dimensional irreducible representation Γ of T_d symmetry expressed in terms of Cartesian coordinates can be reduced to $\Gamma_{T_d} = A_1 + E + F_1 + 3F_2$. The A_1 coordinate consists of a "breathing-type" motion in which the impurity atom remains stationary while the nn host atoms move radially. In the F_1 and E coordinates, the impurity remains at rest and the nn atoms move. It is worth mentioning that only in the triply degenerate F_2 mode the impurity vibrates. We, therefore, expect LVMs of this representation for light defects occupying either Ga or As site in GaAs. For heavier defects (e.g., As_{Ga}), on the other hand, we expect "inband modes" to occur for each type (A_1, E and F_2) of vibrations if force constant variations between impurity and its nn are included. It is worth mentioning that A_1, E, and F_2 type modes are Raman active while only F_2 type modes are infrared active.

The vector space formed by the displacements of the next nearest neighbor pair defect and its nearest neighbors transforms according to the irreducible representations Γ of C_s as $\Gamma_{C_s} = 19A_1 + 14A_2$. In this configuration, we expect A_1 and A_2 types of vibrational modes, all optically allowed. Since the degeneracies are lifted, six impurity vibrations are expected for a pair of light impurity atoms. For a Be_{Ga}-As_{Ga} (or Si_{Ga}-V_{Ga}) pair-defect, on the other hand, the effect of As-antisite (or Ga vacancy) is to lift the degeneracy of the impurity oscillator at Be_{Ga} (Si_{Ga}), and we expect three nondegenerate lines in the region of Be_{Ga} (Si_{Ga}) LVM.

In Table I, we report the results of our calculations of LVM frequencies in the F_2 representation for substitutional impurities in GaAs. In each case, the table lists the relative change in force constant [t, for defects occupying the Ga site (I_{Ga}) or u, for defects occupying the As site (I_{As})] between impurity and its nn, which reproduces the experimental frequency. Clearly, there exists no correlation with the signs of t or u and the size of the impurity-host atoms. However, it reflects a large variation in the values of t or u as we pass from isoelectronic (i) to charged [donor (d^+) or acceptor (a^-)] substituents of comparable masses. After analyzing nearly 80 cases of LVMs in 15 III-V (II-VI) semiconductors, we have established the following trends for closest mass a^-, i, and d^+ occupying III(II) and V(VI) in III-V(II-VI) compounds:

$$\Delta t\{a^-_{III(II)} - i_{III(II)}\} > 0 \text{ (softening)}$$
$$\Delta t\{d^+_{III(II)} - i_{III(II)}\} < 0 \text{ (stiffening)}$$
$$\Delta u\{a^-_{V(VI)} - i_{V(VI)}\} < 0 \text{ (stiffening)}$$
$$\Delta u\{d^+_{V(VI)} - i_{V(VI)}\} > 0 \text{ (softening)}$$

These trends in force constants are found independent of the long range Coulomb interactions, and we strongly argue that charged impurities in semiconductors affect only the short range forces via the redistribution of the electron charge density. In all cases, the explanation for changes in force constants follows from the relaxations for nn of impurities estimated from the BOM. That is, in semiconductors the nn atoms of defects relax inward for a consequent stiffening while softening in the force constant arises for outward relaxation. These intuitive arguments based on our lattice dynamical study are fully supported by recent ab initio calculations. Moreover, this understanding of bonding mechanism for defects in terms of force variations has helped us to identify intrinsic defects in LT GaAs and to establish their relationships to the IR absorption and/or Raman scattering experiments.

Table I. Summary of the Calculated and Experimental LVM and "Inband Modes" of V_{Ga}, As_{Ga}, Be_{Ga}, Si_{Ga}, and Be_{Ga}-As_{Ga} in GaAs

Impurity Ctr.	Sym.	Mode Frequency (cm⁻¹) Theoretical	Exper.	Δf/f (t or u)
V_{Ga}	T_d	40.4 A_1	47 F_2*	1.0
As_{Ga}	T_d	186.9 F_2		0.23
		198.4 A_1	200 F_2*	—
		220.1 F_2	223 A_1/F_2*	—
Be_{Ga}	T_d	482 F_2	482 F_2	0.63
Si_{Ga}	T_d	384 F_2	384 F_2	–0.03
Be_{Ga}–As_{Ga}	C_s	480.3 A_1	—	same as
		481.8 A_1	—	isolated
		482.3 A_2	—	case

*Ref. 10.

The solution of dynamical matrix {Re | I–G°P | = 0} with appropriate force perturbation for As_{Ga} provides no LVM in the F_2 irreducible representation. However, several "inband modes" of A_1 and F_2 representations are predicted. Green's function calculation for an ideal Ga-vacancy is also performed in which the V_{Ga} is modeled simply by removing interactions with the missing Ga-atom and leaving all other atoms at perfect lattice sites. The results of inband modes for As_{Ga} and V_{Ga} are reported in Table I and compared with the existing Raman scattering data of Berg et al.[10] The agreement in the frequencies with the data is a strong evidence of the reliability of our theoretical approach. Using an obvious extension of the above scheme, we present the results for Be_{Ga}–As_{Ga} pair defect. In the IR absorption measurements of LT MBE GaAs:Be, we could not resolve the Be_{Ga} LVM structure; however, the calculated Be vibrations are in good agreement with an overall observed spread of ~2 cm⁻¹ in the LVM structure. An alternative model to consider is [Be_{Ga}–As_i], where As_i occupies an interstitial site displaced from Be_{Ga} acceptor along a [100] crystallographic direction to give a center with C_{2v} symmetry. In this configuration, two of the vibrational modes of the complex would have displacement vectors that would lie in the plane defined by the Be atom and its two As nn on normal lattice site. Both of these modes would involve bond stretching and so they are expected to have higher frequencies. On the other hand, the third mode with displacements of the Be out of this plane involves primarily bond bending

and so a much lower frequency is expected. Based on our experience in the LVM studies in semiconductors, we suspect the spread in the three frequencies for Be_{Ga}–As_i center to be much higher than we have observed in the LT MBE GaAs:Be.

CONCLUSION

In conclusion, we have measured the IR absorption of LVM in LT MBE GaAs:Be as a function of growth temperature. The peak position energy of the Be_{Ga} LVM in HT MBE GaAs:Be is found near ~482 cm^{-1}. As T_G is decreased, the total integrated absorption of Be_{Ga} LVM in GaAs:Be is also decreased and a structure (shoulder) starts to emerge near ~482 cm^{-1} in samples grown at T_G <325°C. This additional structure is believed to be related to the reduction in symmetry at Be_{Ga} from $T_d \rightarrow C_s$ due to the formation of Be_{Ga}–As_{Ga} "acceptor-donor" pairs. Calculations based on the Green's function theory predict inband modes for As_{Ga} and V_{Ga} in GaAs. In LT MBE GaAs:Be, we believe that the decrease in the integrated absorption of Be_{Ga} near ~482 cm^{-1} is compensated by a possible gain in the absorption of As_{Ga} near ~220 cm^{-1} due to the formation of Be_{Ga}–As_{Ga} a pair defects.

ACKNOWLEDGMENTS

This work was supported in part by the U.S. Air Force Office of Scientific Research. Two of us (DNT and RK) were supported by the NRC Research Associateship program.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

High-Speed Photodetector Applications of GaAs and $In_xGa_{1-x}As$/GaAs Grown by Low-Temperature Molecular Beam Epitaxy

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GaAs grown by molecular beam epitaxy (MBE) at low substrate temperatures (~200°C) exhibits the desired properties of a high-speed photoconductor: high resistivity, high mobility, high dielectric-breakdown strength, and subpicosecond carrier lifetime. The unique material properties are related to the excess arsenic content in the MBE grown epilayers. Due to the combination of the above properties, dramatically improved performance has been observed in photoconductive detectors and correlators using submicron spaced electrodes. In addition to GaAs, low-temperature growth of $In_xGa_{1-x}As$ alloys also leads to the incorporation of excess arsenic in the layers, and therefore this material system exhibits many beneficial photoconductor properties as well. In particular, the lattice-mismatched growth of LT-$In_xGa_{1-x}As$ on GaAs appears to be the most suited for high-speed detector applications in the near-infrared wavelength range used in optical communications. The material issues and the photodetector characteristics required to optimize their performance are discussed.

Key words: LT-GaAs, LT-InGaAs, photodetector

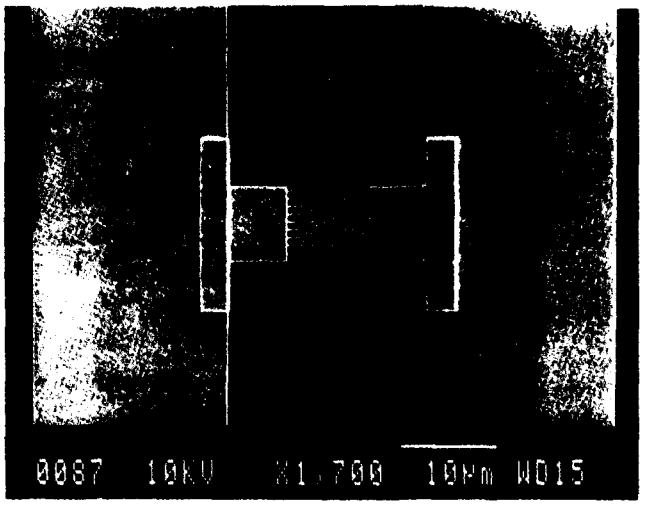
INTRODUCTION

Conventional growth of GaAs by molecular beam epitaxy (MBE) is done at temperatures of ~600°C. In recent years, it has been discovered that unique material properties are observed if the growth temperature is reduced to ~200°C, where the resulting low-temperature-grown (LT) epilayers contain excess arsenic (~1%) in the form of As-antisite defects and interstitials.[1] High-resolution transmission electron microscopy (TEM) and x-ray diffraction have shown that the crystallinity is preserved in these epilayers.[2]

The as-grown LT layers typically have quite low values of resistivity, although after a post-growth anneal at temperatures of ~600°C for times on the order of 10 min, these epilayers are found to be highly resistive. This has been related to the formation of As-precipitates resulting from the high-temperature anneal.[3] In early studies, the absence of photoluminescence from this material coupled with the observed high density of mid-gap defects indicated the dominance of nonradiative recombination processes, thus predicting short free-carrier lifetimes. Indeed, time-resolved optical absorption and reflection measurements have shown subpicosecond carrier lifetimes in numerous samples of this material.[4] Further measurements of the photoconductive switching behavior confirmed this ultrashort carrier lifetime, and also indicated the high sensitivity of this material for generating electrical impulses.[4,5] Therefore, LT-GaAs grown at ~200°C and subsequently annealed at higher temperatures possesses a combination of outstanding properties useful for applications in ultrafast photoconductive detectors: short carrier lifetime, high resistivity, high dielectric breakdown, and good responsivity.

In this paper, we demonstrate practical high-speed photoconductive detectors and related devices which have bandwidths of several hundred gigahertz and

(Received April 12, 1993)



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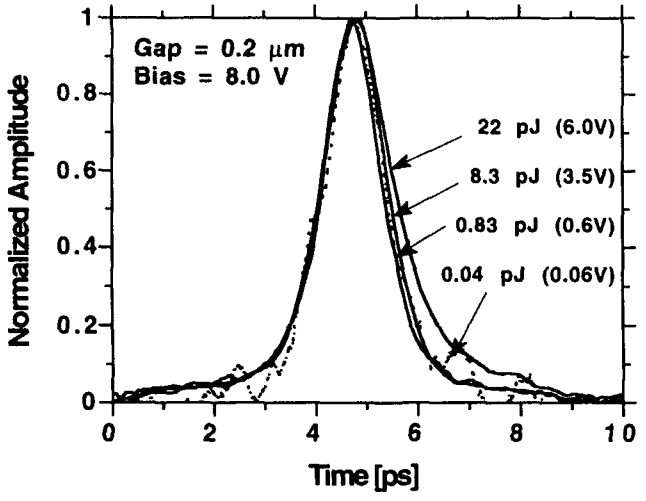

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Fig. 1. (a) Interdigitated-electrode detectors on LT-GaAs. E-beam lithography is used to define the 0.2 μm finger spacing and width. The detector is integrated with a coplanar strip line having 20 μm separation for high-speed response measurement. (b) Temporal response at different optical fluences for the detector in (a). For the lowest fluence of 0.04 pJ, the responsivity is 0.1 A/W and the FWHM is 1.2 ps.

are based on LT-GaAs.

Since the properties of LT-GaAs are related to the excess As incorporation due to the low-temperature growth, similar properties are also expected in other As-containing III-V compounds. In particular, the lower band-gap alloy, $In_xGa_{1-x}As$, is an important material to investigate due to its response in the longer wavelength region of 1.3 μm and 1.5 μm, where optical communications systems operate. In addition to applications of LT-GaAs, we discuss the properties of low-temperature MBE-grown $In_xGa_{1-x}As$ as they pertain to the application of the materials in detectors. The performance of several high-speed detectors fabricated using this material are also evaluated. With the field in its infancy, further studies of this unique material should lead to greatly improved high-speed detectors for use in optical fiber communication systems.

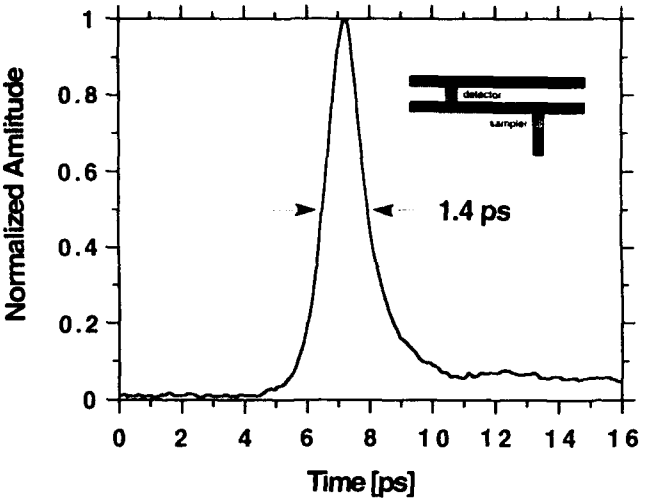

Fig. 2. Temporal response of the optical correlator showing an FWHM of 1.4 ps. (Data courtesy of Picotronix Inc.) Inset: Schematic of the optical correlator. Both the detector and the sampling gate have the interdigitated electrode structure shown in Fig. 1 (a).

ULTRAFAST PHOTODETECTOR APPLICATIONS OF LT-GaAs

For a high-speed photoconductive-detector application, it is necessary to match the lifetime of the carriers to the carrier transit time between the electrodes of the detector.[6] This ensures the highest speed of operation possible (determined by the ultrashort carrier lifetime) in a detector which is very efficient in collecting photogenerated carriers (e.g. like a metal-semiconductor-metal [MSM] photodiode) and thus has a high responsivity. For a carrier lifetime of ~1 ps, this condition is met for an electrode spacing of ~0.1 μm. To demonstrate such an ultrafast detector, an interdigitated photoconductive device with an active area of $7 \times 7\ \mu m^2$ was fabricated on annealed LT-GaAs grown at 200°C. The detector had finger widths and spacings of 0.2 μm defined using electron beam lithography.[6] This detector was embedded in a broadband coplanar-strip structure (Fig. 1a) for high-speed measurements using the electro-optic sampling technique. The response of the detector at various optical fluences is shown in Fig. 1b. For an optical energy of 0.04 pJ/pulse, the responsivity is 0.1 A/W, and the 3-dB bandwidth is 375 GHz (full width at half maximum [FWHM] = 1.2 ps for the measured electrical output pulse). The dark current at a 1-V bias is 100 pA. For the highest optical fluence of 22 pJ/pulse, the on-state resistance of the detector is ~30 Ω, and the response slows down only marginally to ~1.5 ps. This large dynamic range is a consequence of the short carrier lifetime, which eliminates any slow "tail" component in the response (which would be due to the transport of photogenerated holes), and also eliminates the space-charge screening of the electric field.[7,8]

The low on-state resistance also facilitates the use of this type of detector geometry as a sampling gate. Thus, it was possible to integrate two similar interdigitated structures, one serving as a detector and the other as a sampling gate triggered by a

reference laser pulse, in a compact space of several square millimeters.[9] The response of such an optical correlator is shown in Fig. 2, where a 1.4 ps FWHM resolution is obtained at a noise-equivalent power of ~500 pW.

Since the photoabsorbing material for the optoelectronic devices described above is GaAs (bandgap of 1.42 eV at room temperature), the high-speed detector applications in Figs. 1 and 2 are only sensitive to wavelengths of 870 nm or less. The main commercial applications, however, lie in the region of operation of fiber-optic systems; i.e., λ = 1.3 and 1.5 μm. Some success has been achieved in using a low-temperature MBE grown GaAs material for 1.3 μm photodetection, based on the absorption through internal photoemission by the As-precipitates.[10] Nevertheless, a much improved responsivity and speed of operation are certainly desirable.

LOW-TEMPERATURE MBE GROWTH OF $In_xGa_{1-x}As$

To extend the wavelength of operation of these detectors, it is, therefore, natural to investigate whether the desired material properties can be achieved in other LT MBE-grown materials. Low-temperature-grown $In_{0.52}Al_{0.48}As$ lattice matched to InP has shown similar properties of subpicosecond carrier lifetime and high resistivity when grown by MBE at about 150°C,[11] and since the above properties are related to the excess As incorporation due to the low growth temperature, it is also to be expected in other III-V compound semiconductors containing arsenic.

Lattice-Matched $In_xGa_{1-x}As$ on InP

Lattice-matched $In_xGa_{1-x}As$ on InP has a cutoff wavelength for photodetection of ~1.7 μm at room temperature, and it is easy to grow high quality $In_xGa_{1-x}As$ by MBE. A preliminary study using time-resolved reflectance measurements has indicated that the carrier lifetime decreases to ~2.5 ps by decreasing the MBE growth temperature down to 180°C.[4] Similar results have also been obtained by Tousley et al.[12] However, these epilayers have a very poor resistivity of ~0.1–1.0 Ω-cm, which does not improve with annealing, and hence this material cannot be used for photodetector applications. The electrical properties have been further investigated by Kunzel et al., who found similar highly conductive behavior which they attributed to the defect induced ionized deep centers.[13] The important finding is that it is possible to grow single crystalline epitaxial layers of 1–2 μm thickness, down to MBE growth temperatures of ~125°C.

Due to the low resistivity of the lattice-matched LT-$In_xGa_{1-x}As$, alternate approaches have been adopted to improve this quantity while still retaining the short carrier lifetime of the material. Molecular beam epitaxy growth of effective-lower-band gap materials using GaAs/AlAs superlattices grown at low temperatures has also resulted in highly conductive epilayers. Another approach might be the addition of a small mole fraction of Al in the alloy, which should improve the resistivity while altering the bandgap to only a small extent. The approach which has been followed in this investigation, with a good deal of success, is the low-temperature MBE growth of lattice-mismatched $In_xGa_{1-x}As$ on GaAs. Thus far, high-resistivity epilayers with short carrier lifetimes have been produced with mole fractions of InAs up to 35%.[4]

Low-Temperature MBE Grown $In_xGa_{1-x}As$ on GaAs

The ternary alloy $In_xGa_{1-x}As$ is suitable for applications from 1.0 to 1.7 μm in wavelength, depending on the mole fraction of In. Besides the resistivity benefit derived from lattice-mismatched growth, it is also very attractive to grow $In_xGa_{1-x}As$ on GaAs substrates, due to the lower expense of GaAs and the lower density of defects present in this material. Integration of longer-wavelength optoelectronic devices also becomes possible with the use of the more mature GaAs processing technology. The critical problem with such an approach is that the lattice mismatch makes the growth of high quality $In_xGa_{1-x}As$ on GaAs substrates difficult. It is only possible to grow a very thin (<200Å) layer of pseudomorphic $In_xGa_{1-x}As$ on GaAs. The growth of thicker layers results in the release of strain by the generation and propagation of misfit dislocations or by three-dimensional island growth.[14] Thus, the electronic properties of these lattice-mismatched epilayers is strongly influenced by the generated dislocations.[15] The main positive information regarding the mismatched growth is that by using multi-stage strain relief buffers, it is possible to grow device quality $In_xGa_{1-x}As$ layers on GaAs.[16]

Layers of 1.0 μm thick LT-$In_xGa_{1-x}As$ with 25% and 35% InAs mole fractions (having cutoff wavelength λ ~1.1 and 1.3 μm, respectively) were grown in a Varian Gen II MBE system on semi-insulating GaAs substrates. A wide range of growth temperatures from 120–550°C have been studied. A growth rate of 1.0 μm/h was used with a V/III beam equivalent pressure ratio of 15. Some of the layers were annealed at 600°C for 15 min in an As_4 ambient after the growth wa. completed. It is generally observed that the surfac morphology improves upon lowering the growth tem-

Fig. 3. Transmission electron microscopy photo of LT-$In_{0.25}Ga_{0.75}As$-on-GaAs grown at 200°C and subsequently annealed at 600°C for 15 min. Precipitates are clearly visible.

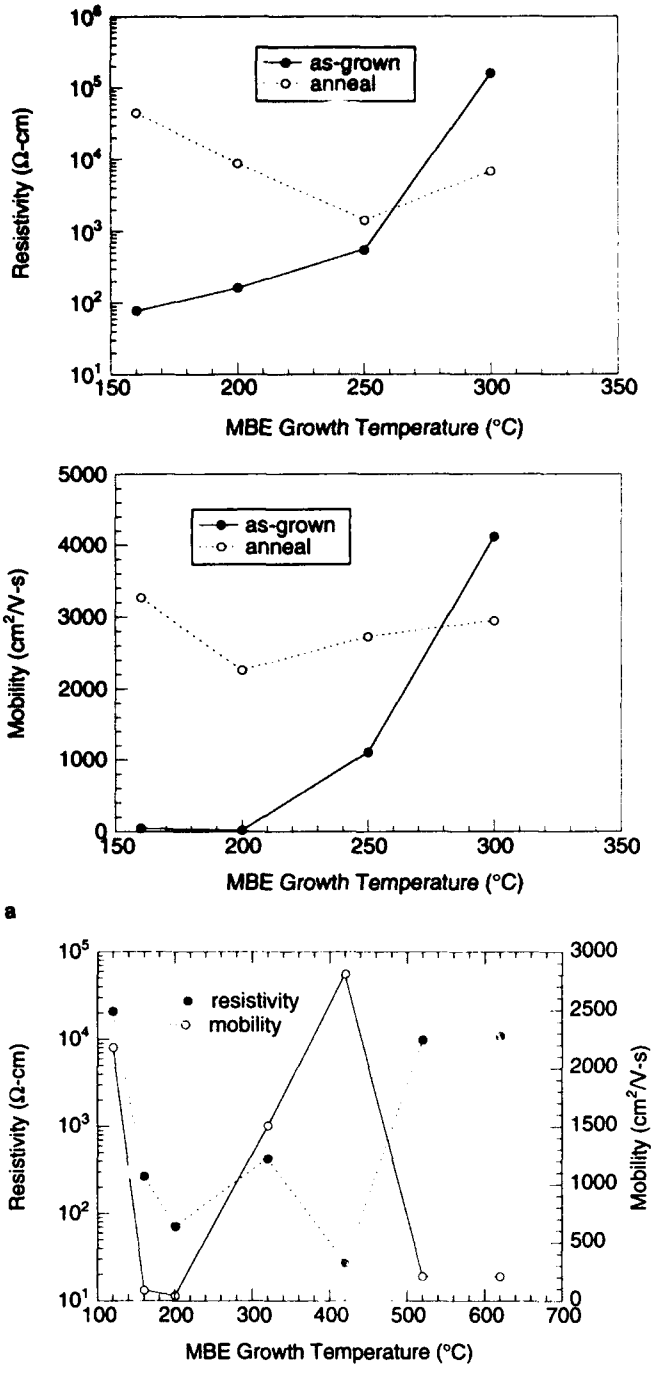

Fig. 4. Hall measurement of the resistivity and mobility of (a) 25% and (b) as-grown 35% mole fraction LT-$In_xGa_{1-x}As$ on GaAs.

perature; and, therefore, the layers grown at the lowest temperatures of ~120–200°C have excellent surface quality. Reflection high energy electron diffraction (RHEED) and x-ray diffraction show all the layers to be of very good crystalline quality except for the one grown at ~120°C, which appears to be polycrystalline.

Figure 3 shows a TEM micrograph of the LT-$In_{0.25}Ga_{0.75}As$ on GaAs epilayer grown at 200°C. Excess As is present in these epilayers. In the as-grown material, no precipitates have been observed; al-

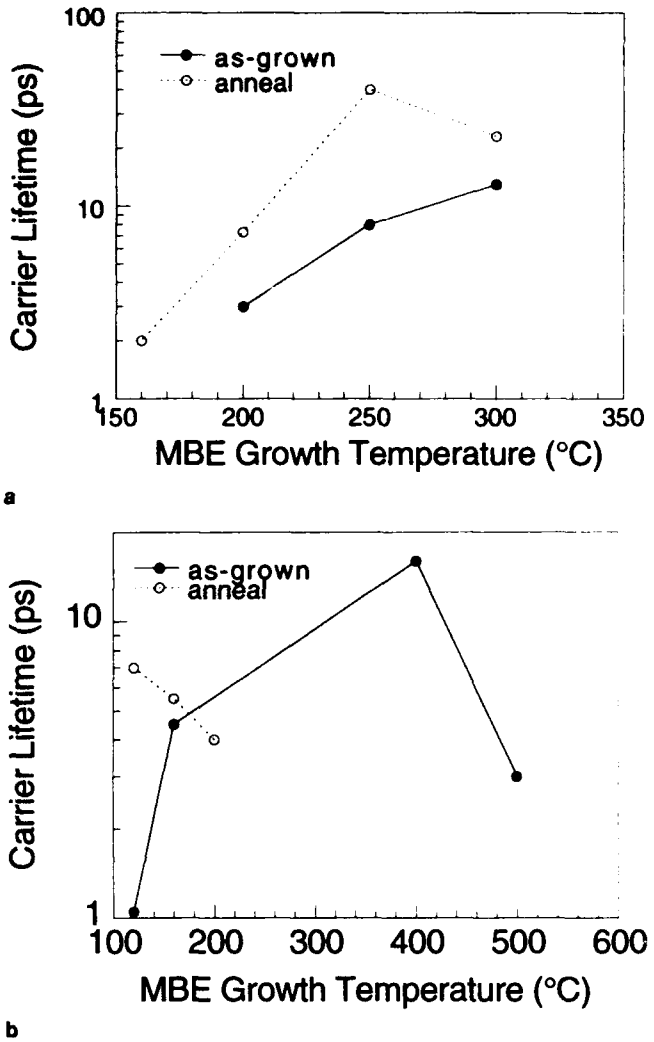

Fig. 5. Carrier lifetime vs the MBE growth temperature for (a) 25% and (b) 35% In-mole fraction LT-$In_xGa_{1-x}As$-on-GaAs.

though after annealing, they clearly become visible. Unlike LT-GaAs, however, the precipitate composition in LT-$In_xGa_{1-x}As$ does not appear to be 100% arsenic. Due to the high degree of lattice mismatch of ~2 and 3%, respectively, in the 25 and 35% mole fraction epilayers, a high density of dislocations which originate near the surface are also observed. The samples grown at higher temperatures are crystalline, though heavily dislocated. At the lowest range of growth temperature investigated, micro-twin formation is also observed. Further lowering the growth temperature results in an amorphous epilayer, as is observed for the LT-$In_{0.35}Ga_{0.65}As$ grown at 120°C.

To evaluate the electrical quality of the epilayers and to determine the feasibility of using this material in photodetector applications, room-temperature Hall parameters were measured (Fig. 4). Low temperature-$In_{0.25}Ga_{0.75}As$ on GaAs shows a well behaved dependence of the Hall parameters. Both the resistivity and the mobility decrease dramatically as the growth temperature is decreased to 160°C. However, after annealing, the resistivity and mobility improve

dramatically. Since at the lowest growth temperatures the carrier lifetime is expected to be its shortest, the annealed 160°C-grown LT-$In_{0.25}Ga_{0.75}As$-on-GaAs seems to be the most suitable layer for photodetector applications at this InAs mole fraction.

For the as-grown LT-$In_{0.35}Ga_{0.65}As$-on-GaAs material, there does not appear to be a uniform trend in the resistivity and the mobility, as seen from Fig. 4. Upon annealing, for the samples grown at the lower temperatures, the resistivity and mobility change only marginally, except for the sample grown at 120°C. Annealing decreases the resistivity to less than 100 Ω-cm for this sample. Nevertheless, the as-grown material at 120°C possesses both the properties of high resistivity and mobility desired for an ultrafast photoconductor. On the samples which exhibited an adequately high resistivity; i.e., so that photoconductive switching could be performed, coplanar strip electrodes separated by 15 μm were deposited using standard photolithographic techniques. A 10 μm long gap in one of the electrodes defined the photoconductor switch which was triggered by ~100 fs duration optical pulses from a mode-locked dye laser. The technique of electro-optic sampling was used to measure the photo-generated electrical pulses.[17] The carrier lifetime measured from the 1/e decay of the generated transient is plotted in Fig. 5 and also summarized in Table I.[18] The responsivity of this gap detector may also be found in Table I. The shortest carrier lifetimes, near a single picosecond, are observed for the material grown at the lowest temperatures for both the 25 and 35% InAs mole-fraction materials. For LT-$In_{0.35}Ga_{0.65}As$ grown on GaAs at 120°C, however, annealing significantly increased the carrier lifetime. This is believed to be due to the partial recrystallization of the near-amorphous, low-temperature epilayer, as observed from the TEM micrographs. For LT-$In_{0.35}Ga_{0.65}As$-on-GaAs, the material grown at a more conventional temperature near 500°C also demonstrated unusually short carrier-lifetime behavior. The reason for this is not understood at present and is under investigation. It should also be pointed out that similar ultrashort carrier lifetimes have also been obtained for low-temperature MBE growth of lattice mismatched GaAs and LT-$In_{0.6}Ga_{0.4}As$ on Si substrates.[19]

ULTRAFAST PHOTODETECTOR APPLICATIONS OF LT-$In_xGa_{1-x}As$/GaAs

To improve the responsivity of the simple, straight-gap detectors, it is necessary to reduce the electrode spacing as discussed in the section on ultrafast photodetector applications of LT-GaAs. Metal-semiconductor-metal detectors with interdigitated-electrode structures having 0.2, 0.5, 1.0 and 2.0 μm finger widths and separations were fabricated on the annealed 160°C MBE-grown LT-$In_{0.25}Ga_{0.75}As$ and the 120°C-as-grown LT-$In_{0.35}Ga_{0.65}As$ layers. The metal fingers were defined using electron-beam lithography, where the e-beam dosage was optimized to account for the somewhat rough surface of the LT-$In_{0.25}Ga_{0.75}As$ layers. After developing the photoresist, a brief etch in HCl was done and then a Ti/Au metallization was deposited to form the electrodes. Each MSM detector had the same total area of ~13 × 20 μm^2 and was fabricated in a shunt configuration in a coplanar strip having a characteristic impedance of 73 Ω. This geometry was employed to facilitate high-speed measurements using an external electro-optic sampling probe. The detectors, which did not have anti-reflection coatings, are shown in a scanning electron microscopy (SEM) photo in Fig. 6. A typical breakdown voltage for the 0.2 μm finger detectors is 4–5 V, or 200–250 kV/cm; and in the bigger detectors, the breakdown voltage scaled

Table I. Carrier Lifetime of LT-$In_xGa_{1-x}As$ on GaAs

Growth Temp. (°C)	Anneal	Lifetime (ps)	Responsivity (10^{-5} A/W)
x = 0.25			
300	no	13.0	4.9
250	no	8.0	3.0
200	no	3.0	0.6
160	no	unmeasurable	
300	yes	23.0	3.2
250	yes	40.0	3.0
200	yes	7.3	5.5
160	yes	2.0	0.4
x = 0.35			
500	no	3.0	4.2
400	no	16.0	8.5
200	no	unmeasurable	
160	no	4.5	0.2
120	no	<1.0	0.03
200	yes	4.0	3.0
160	yes	5.5	2.1
120	yes	7.0	3.1

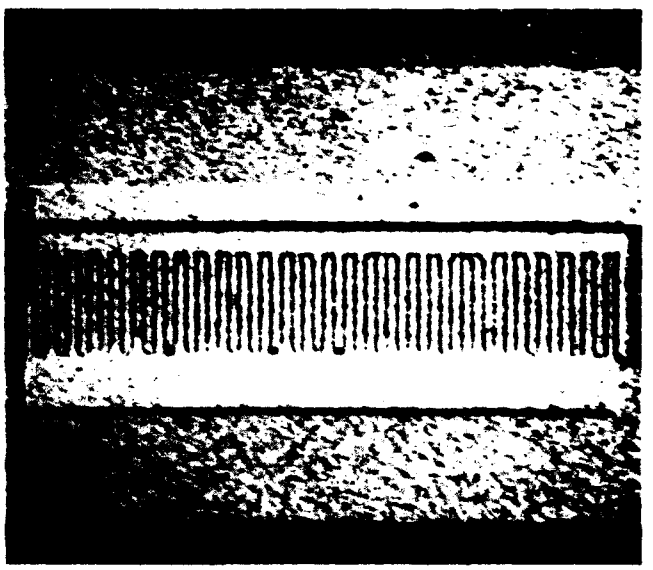

Fig. 6. Scanning electron microscopy photo of an LT-$In_xGa_{1-x}As$-on-GaAs interdigitated detector. E-beam lithography is used to define the patterns with 2.0, 1.0, 0.5, and 0.2 μm finger spacings and widths.

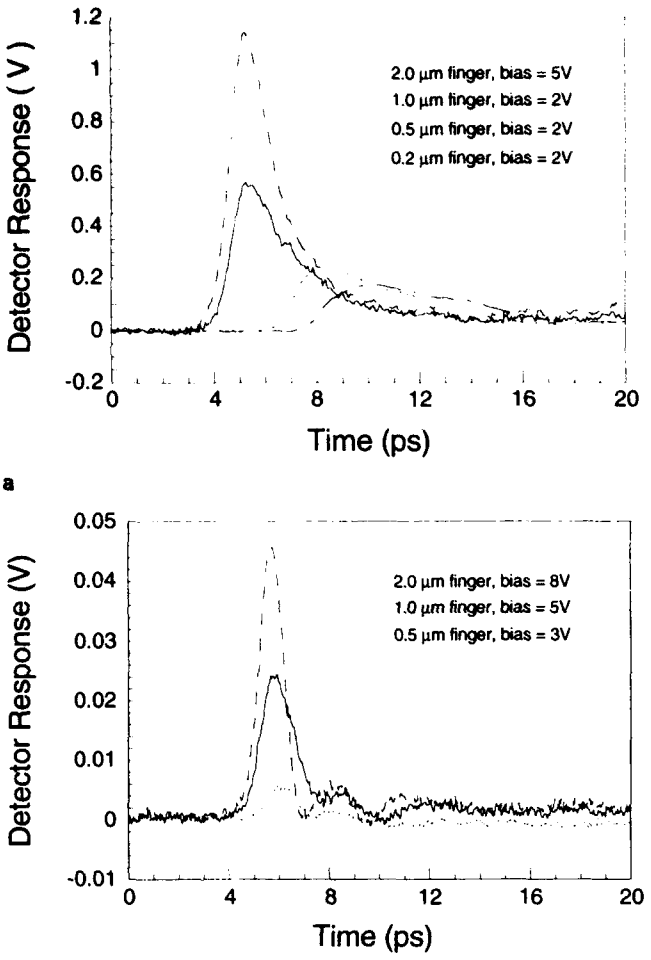

Fig. 7. Temporal response of the (a) 25% and (b) 35% mole fraction LT-$In_xGa_{1-x}As$-onGaAs detectors, as measured by external electro-optic sampling. The total detector area is 13 x 20 μm².

roughly with the gap between the fingers so that the 2 μm detectors had about a 40–50 V breakdown. A dark current of less than 1 nA was measured at a 2 V bias for discrete detectors with 1 μm fingers and spacings processed on a separate piece of the LT-$In_{0.25}Ga_{0.75}As$ material.

Figure 7 shows the detector response as measured by electro-optic sampling. The 0.2 μm detectors on the 35% mole fraction samples were not functional due to a short in the electrodes between the fingers. The 1.3 and 2.0 ps FWHM response of the 2 μm LT-$In_{0.35}Ga_{0.65}As$ and LT-$In_{0.25}Ga_{0.75}As$ detectors[20] are the fastest of any photodetectors reported using $In_xGa_{1-x}As$. The smaller finger and gap detectors were limited by the RC-time of the structure due to the increase of the capacitance with the increasing number of fingers, while it is also likely that the higher fields present in these structures lead to increased hole injection from the contacts and a subsequent increase in the detector response time. The 1 μm devices on the LT-$In_{0.25}Ga_{0.75}As$ and LT-$In_{0.35}Ga_{0.65}As$ layers had responsivities of 0.03 and 0.0003 A/W, respectively, measured at λ = 630 nm. The very poor responsivity of the latter is presumably an outcome of the amorphous nature of the epilayer. Further optimization of the material properties, backside illumination, and anti-reflection coating should further improve the responsivity. It is believed these detectors are useful up to wavelengths of 1.0 and 1.3 μm, respectively, although until stable ultrashort-pulse optical sources at these photon energies are readily available, the ultimate speed of the devices at the most desirable wavelengths will not be known.

CONCLUSIONS

From the above discussion, it becomes clear that low-temperature MBE growth offers a unique approach to optimizing the performance of high-speed photodetectors by enabling one to tailor the fundamental material properties. The excess As-incorporation due to the low-temperature growth of GaAs leads to high-resistivity behavior, high dielectric breakdown, suitable mobility, and ultrashort carrier lifetimes. It has also been found that these properties can be tailored in a variety of III-V materials containing arsenic. Simple photoconductive detectors with interdigitated electrodes fabricated on GaAs and $In_xGa_{1-x}As$/GaAs have attained bandwidths of several hundred gigahertz with moderate to good responsivities. Further understanding of the material properties of low-temperature MBE-grown materials and improvements in the detector design should lead to improved photodetector performance.

ACKNOWLEDGMENTS

This research is supported by AFOSR contract numbers F49620-91-C-0044 and AFOSR-90-0214 (University Research Initiative) and by the National Science Foundation through the Center for Ultrafast Optical Science under STC PHY 8920108.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Influence of Growth Temperatures on the Photoresponse of Low Temperature Grown GaAs:As p-i-n Diodes

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We report a study of the sub-bandgap photoresponse of p-i-n photodetectors with 1 μm low-temperature intrinsic layers, and its dependence on the growth temperature of the intrinsic layer. Diodes with intrinsic layers grown near 250°C exhibit the highest photoresponse. The photoresponse decreases gradually as the growth temperature is raised above 250°C. For growth temperatures at or below 200°C, a drastic drop in the photoresponse is observed, along with degradation of crystal quality in the material. The extracted internal Schottky barrier heights are found to be within the range 0.7–0.8 eV.

Key words: Low temperature grown GaAs, MBE, PiN detectors

INTRODUCTION

GaAs grown at low substrate temperatures (150–350°C) by molecular beam epitaxy (MBE) exhibits material properties different from regular MBE-grown GaAs.[1-7] Annealed low temperature (LT) GaAs:As has extremely high resitivities and has been successfully used as a buffer layer to reduce backgating in metal semiconductor field-effect transistor structures.[2,3,8] This material is also sensitive to 1.3 μm light[9] and has been used as the "active" layer in devices such as p-i-n diodes[9] and photoconductive detectors.[10-12]

The growth of GaAs at these low temperatures results in the incorporation of 1–2% excess arsenic in the epilayer.[3,6] The as-grown material is highly strained and has a high concentration of arsenic antisites and other defects.[4,5] After high temperature annealing, the strain is reduced and the excess arsenic agglomerates into precipitates.[4,6] The presence of a large number of defects and the observation of hopping conduction[13] have led to the theory of Fermi level pinning by deep donors.[14] Warren et al.[6] proposed an alternative theory, the buried Schottky model based on the observation of metallic arsenic precipitates in the GaAs layers. These arsenic precipitates in high enough concentration are expected to deplete the GaAs matrix of carriers.

The detection of sub-band gap light by LT-GaAs:As has been explained to be due to internal photoemission.[15] It would be interesting to study the dependence of the sub-band gap photoresponse on the growth temperature of the LT intrinsic layer, not only to establish the optimum growth temperature for maximum photoresponse, but also to gain additional insight into the operation of such devices. We report such a study here.

EXPERIMENT

The p-i-n structures were grown in an Intevac Gen II molecular beam epitaxy system. The schematic cross-sectional view of these structures is shown in Fig. 1. Dimeric arsenic from a valved cracker source[16,17] was used with a As/Ga beam equivalent pressure ratio of 15. The As overpressure used corresponds to an As/Ga flux incorporation ratio of 2.0 measured at 600°C for a 1 μm/h growth rate. The structures were grown under the same conditions. Growth interrupts were used to change the substrate temperature between the normal and LT layers. This differs from earlier work,[9,14] in which growth was continued during the time required for the temperature change, giving rise to temperature transition layers between the normal and LT layers. Growth interrupts were employed in this work in order to avoid differing

(Received April 12, 1993)

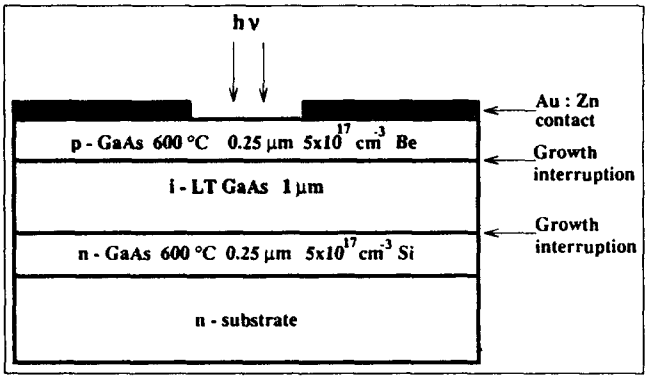

Fig. 1. Schematic diagram of p-i-n photodiode structures.

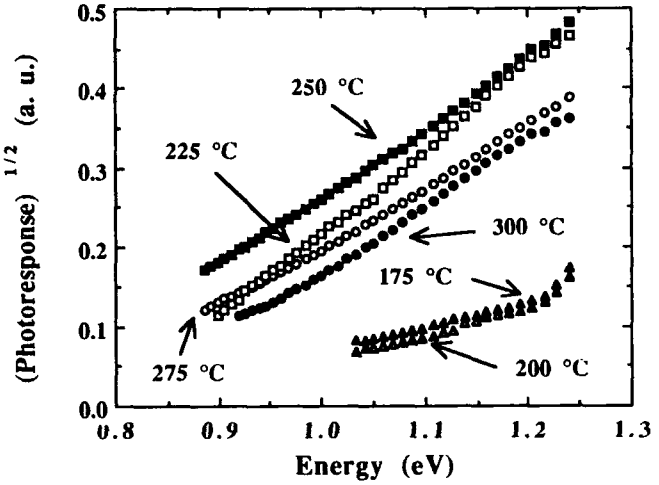

Fig. 2. Fowler plots for devices with LT layers grown at various temperatures.

transition-layer thicknesses that would result from different LT-layer temperatures and thus cooling times. During the cool-down interrupt, the As shutter was closed when the temperature dropped below 450°C to avoid the deposition of any excess arsenic. The As shutter is kept open during the entire warm-up interrupt, as any deposited arsenic was expected to evaporate as the temperature is raised. We note in passing that our results indicate that a temperature transition layer is not essential to the performance of the device. Following growth, each sample was annealed for 1 h at 600°C under an As flux. Following MBE growth, diode structures were fabricated using top Au:Zn ring contacts defined by evaporation and lift-off and annealed at 350°C for 30 s. Device isolation was achieved with a Br-methanol mesa etch. Photoresponse data were obtained for the range of wavelengths 1.0–1.4 μm using a monochromator and broadband source. Lock-in techniques were used to measure the photocurrent. The photoresponse data were normalized using a Ge photodiode calibrated at 5 nm intervals. A 980 μm filter was used to eliminate photons with energies greater than the band gap.

RESULTS AND DISCUSSION

The measured zero-bias photoresponse data are shown in Fig. 2. The most striking feature of the data is the poor photoresponse of devices with intrinsic layers grown at 200 and 175°C. This drastic drop in the photoresponse for growth temperatures at or below 200°C is clearly seen in Fig. 3. Arsenic precipitates have clearly been observed in samples grown at 200–300°C in other laboratories.[18] Despite possible variations in arsenic overpressure and growth temperature[19] from one laboratory to another, it is likely that our 175 and 200°C samples contain structural defects associated with low-temperature growth beyond the critical thickness. The 1 μm intrinsic layer used in our devices is thicker than the critical thickness for the formation of defects, estimated to be 0.8 μm at 200°C and smaller at 175°C.[20,21] The 200°C sample produced a spotty reflection high energy electron diffraction pattern immediately following the growth of the LT layer and had a somewhat hazy surface. The 175°C sample exhibited these features even more strongly. These observations are consistent with a dramatic decline in carrier collection efficiency due to degradation in crystalline quality.

Devices with LT layers grown at 225 and 250°C exhibit the highest photoresponse. The corresponding quantum efficiencies are close to those measured by McInturff et al.[9] on samples grown at 225°C, indicating the similarity of the devices made in the two laboratories. The difference between the photoresponse of the 225 and 250°C samples is within device-to-device variations on the same chip and cannot be unambiguously attributed to a temperature effect.

As the growth temperature is raised above 250°C, the photoresponse gradually falls. Since the concentration and size of the precipitates decrease as the growth temperature is raised,[18] a decrease in photoemission is expected.

Figure 2 indicates that regardless of the growth temperature, measured devices follow the Fowler relation[22]

$$\sqrt{PR} = h\nu - \phi_{bn} \quad (1)$$

where PR is the photoresponse per incident photon, hν is the incident photon energy, and ϕ_{bn} is the barrier height. The direct application of Fowler's theory to the present case is somewhat uncertain, since the Fowler relation was derived assuming a constant density of states in the metal. Furthermore, the geometry was that of a planar Schottky barrier. Removal of the first assumption is complicated by the fact that the density of states in a collection of small arsenic precipitates with varying sizes is probably different from that of bulk arsenic. The second assumption may be applicable to our devices if most of the photoresponse is due to carriers emitted toward the contact layers from precipitates near the contact-layer interfaces. In any case, our interest lies in the temperature dependence of the photoresponse rather than its origin. In our devices, the extracted barrier heights are generally between 0.7 and 0.8 eV. For a given MBE layer, the photoresponse data varies from device to device, with extracted barrier heights differ-

ing by some 0.05 eV. Within experimental uncertainties, our data provides no clear evidence of a growth-temperature-dependent barrier height. Nevertheless, the possibility of minor variations in the barrier height as a function of growth temperature cannot be discounted without extensive statistical analysis. We note in passing that the choice of the range of photon energies to be used in extracting the barrier height affects the results by about 0.03 eV. The barrier heights extracted by McInturff et al.[15] are based on photoresponse data up to a photon energy of 1.1 eV. We find that although using the data in this range results in excellent linear fits, extending the energy range to 1.25 eV results in linear fits of equal quality but a somewhat larger barrier height.

Any study of the dependence of the properties of LT-GaAs on growth conditions should address experimental difficulties in ascertaining the growth temperature. In this work, run-to-run calibration of the temperature was based on the oxide desorption temperature and thermally identical blocks were used for the different runs. Samples were indium mounted to minimize block-to-sample temperature variations. Earlier, the temperatures were checked against the melting points of aluminum, indium, and InSb. Whereas the absolute value of the growth temperatures may be somewhat uncertain, the samples do span a temperature range of some 125°C. Development of in-situ temperature measurement techniques should enhance our ability to pinpoint growth temperatures reliably.[19]

CONCLUSIONS

A series of p-i-n photodetectors with 1 μm low-temperature intrinsic layers were grown to establish the LT growth temperature for optimum sub-band gap photoresponse. Devices with intrinsic layers grown at 225–250°C were found to be most efficient. Lower temperatures resulted in drastically inferior detection, probably due to the formation of defects in the intrinsic layers. Photoresponse was found to decrease gradually as the growth temperature was increased beyond 250°C. No clear evidence of growth-temperature-dependent banier heights was found.

ACKNOWLEDGMENTS

We gratefully acknowledge conversations with M.R. Melloch and D.P. Neikirk. This work was supported by Joint Services Electronics Program under Contract #AFOSR F49620-92-C-0027, the Army Research Office under Contract #DAAL-03-91-G-0034, the Science and Technology Center program of the National Science Foundation, Grant #CHE 8920120, and the Texas Advanced Research Program.

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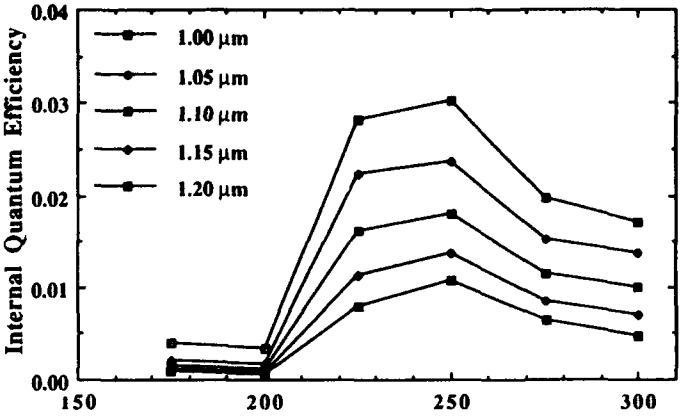

Fig. 3. The dependence of sub-band gap quantum efficiency on the growth temperature of the LT layer. The different plots indicate the wavelength at which the measurement was made.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Subpicosecond Carrier Response of Unannealed Low-Temperature-Grown GaAs vs Temperature

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The subpicosecond carrier lifetime of an unannealed molecular beam epitaxial layer of GaAs grown at ~210°C has been demonstrated between 10 and 290K through optoelectronic switching and all-optical pump-probe measurements. The low room-temperature resistivity of the as-grown layers, believed to arise from hopping conductivity through defect sites, has been observed to increase as the sample temperature was lowered, allowing ultrafast switching measurements to be performed using the low-temperature-as-grown GaAs as a photoconductive element. After illumination by 100 femtosecond optical pulses, photogenerated carriers in the sample have rapidly relaxed, returning the material to its high-resistivity state in less than 1 ps. This indicates that the precipitates present in post-annealed samples are not required for the fast relaxation of photoexcited carriers in low-temperature-grown GaAs. Ultrafast switching measurements on a post-annealed version of the GaAs film also resulted in the generation of similar, 0.6 ps full width at half maximum pulses.

Key words: LT-GaAs, opto-electronic, photoconductive switching

INTRODUCTION

Gallium arsenide grown by molecular beam epitaxy (MBE) at low substrate temperatures (LT-GaAs)[1] has become recognized for its unique and useful optoelectronic properties. As-grown samples prepared in the temperature range 180–250°C have been reported to contain an extreme number of As antisite-related defects[2] (between 10^{18} and 10^{20} cm^{-3}), and they exhibit relatively low resistivity and mobility. When annealed, arsenic precipitates form in the films, which have an enhanced dark resistivity and a high mobility,[3] and in addition are found to respond in an extremely short time (<1 ps) to ultrafast-optical-pulse illumination.[4,5] These properties have led to the application of annealed LT-GaAs in high-sensitivity (0.1 A/W), high bandwidth (375 GHz) photodetectors,[6] picosecond optical correlators,[7] and quasi-optical terahertz transmitters and receivers.[8]

(Received April 12, 1993)

It has been suggested that there is a significant connection between the presence of the precipitates in the annealed materials and their ultrafast carrier response.[9] Due to this belief, as well as to the existence of the outstanding properties of the annealed layers, optoelectronic studies involving the unannealed LT-GaAs have essentially been ignored. In order to increase the understanding of the mechanisms responsible for the short carrier lifetime in both annealed and as-grown LT-GaAs, and to further advance the potential for application of this material to optoelectronic applications, we demonstrate the first measurement of photoconductive switching and subpicosecond electrical pulse generation using as-grown LT-GaAs.

For further confirmation of the carrier response time of as-grown and annealed LT-GaAs, we have measured the temperature-dependent temporal response of their carrier behavior through femtosecond (fs) transient reflectivity. In all the time-resolved measurements, negligible changes in response were

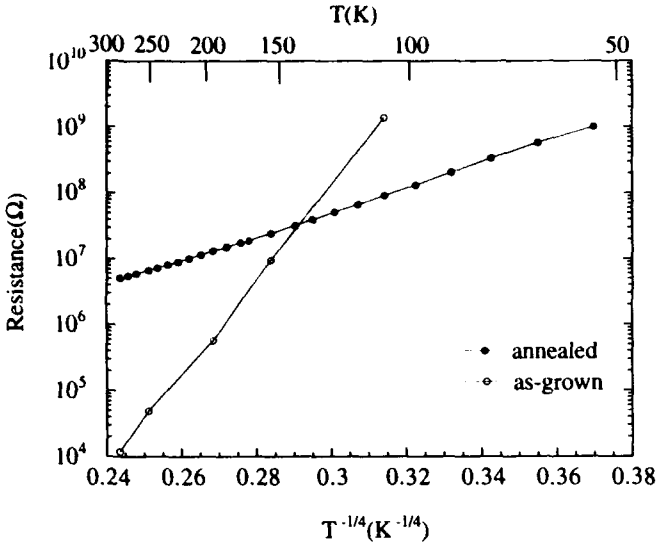

Fig. 1. Experimental temperature dependence of the resistance, which is primarily due to carriers hopping between defect centers in the as-grown LT-GaAs. Since $\rho \alpha \exp([T_o/T]^{1/4})$, $T_o^{1/4}$ was used as a parameter to fit the data. $T_o^{1/4}$ ~70 for the as-grown sample and $T_o^{1/4}$ ~20 for the annealed one.

found for both annealed and unannealed LT-GaAs between 300 and 10K.

MATERIAL PARAMETERS

The samples employed in this study were grown in a *Varian GEN II MBE system on semi-insulating* GaAs substrates mounted on a nonbonded block. A clean, oxide-free surface was established by growing a thin buffer layer on the substrate at 600°C before the substrate temperature was lowered to ~210°C for the growth of the LT-GaAs layer. A growth rate of 1 μm/h was used with a V/III beam equivalent pressure ratio of 15. The layers were grown to a thickness of 4.5 μm, after which the wafers were removed and cleaved so that one half could remain unannealed while the other half was post-annealed at 600°C for 15 min. From electron diffraction measurements, it appears that the samples are single crystals; i.e., there was no indication of polycrystalline nature. It was observed, however, that as the growth temperature was decreased, the layers did become polycrystalline, as found in another set of 4.5 μm samples grown at 170°C. From room temperature Hall effect measurements, the resistivity was in the range of 10^5 Ω-cm for the 210°C as-grown samples and 10^8 Ω-cm for the annealed ones. The dc mobility for the annealed material grown at 210°C was of the order 10^3 cm²/V-s, while it was two orders of magnitude lower for the unannealed layers.

Through our observations, we believe that an enhanced conductivity due to carrier hopping via defect sites is the origin of low resistivity values at room temperature or above for the unannealed material. This is because an increase in resistance proportional to $\exp([T_o/T]^{1/4})$[3,10] (Fig. 1) is measured as the sample temperature is decreased from 300 down to 50K. Curve fits to the data in Fig. 1 give values for $T_o^{1/4}$ of 70 for the as-grown and ~20 for the annealed layers. This indicates a substantially higher defect density in the as-grown material, due to the fact that T_o is dependent on the defect density in the sample.[11]

PHOTOCONDUCTIVE-SWITCHING EXPERIMENT

While there is evidence of ultrafast carrier lifetimes in as-grown LT-GaAs layers from previous transient reflectivity experiments,[12] those measurements probed the carrier response at an energy of 2 eV, or about 0.6 eV above the conduction band, where intervalley scattering may occur. Also in these experiments, the high-photon-energy optical probes may only be measuring part of the carrier lifetime, rather than the complete relaxation from the conducting state as determined in the photoconductive measurements. Unfortunately, photoconductive detector patterns on the unannealed material are practically useless in most cases at room temperature due to their low resistance and high leakage current. However, by decreasing the temperature to <160K, we defeated the hopping conductivity and obtained switch-gap resistance values above 10 MΩ, more than adequate to hold off substantial voltages for photoconductive switching.

Short electrical pulses were optically excited between two coplanar striplines fabricated on both the annealed and unannealed LT-GaAs photoconductive layers. A self-mode-locked Ti:sapphire oscillator provided the 70 fs excitation and sampling pulses used in this investigation. An external probe tip was employed in an electro-optic sampling system having 200 fs temporal resolution to measure the electrical transients output from the LT-GaAs switches and coupled to the coplanar transmission lines. In reality, the ultrafast electrical signals generated at the LT-GaAs switches suffered slight degradation before being measured due to the distortion mechanisms of attenuation and dispersion which arose from the short section of transmission line between the switch and the measurement point. These lines were 20 μm wide and also separated by 20 μm, and a dc bias of 20 V was applied between the lines, across the LT-GaAs region. The average optical power used in the switching experiments was 25 mW, and the wavelength of the laser source was 800 nm, corresponding to an energy of 1.55 eV. The laser pulses thus excited carriers ~0.13 eV above the minimum of the conduction-band edge, but not high enough so that scattering to the upper L valley occurred.

RESULTS

The response of the photoconductive gap on the unannealed LT-GaAs material was measured vs temperature between 160 and 10K. The dramatic characteristics of the switched waveforms are their very short rise time (~450 fs), full width at half maximum (FWHM) (~600 fs), and fall time (~450 fs). (The ringing at the end of the pulse can be attributed to dispersion, radiation, and measurement-probe effects,

and it is not related to the material response.) These values remained constant within experimental error over the entire temperature range. This is illustrated at temperatures of 100 and 150K in Fig. 2. The measurement limited fall times indicate the material has returned almost completely to a high-resistivity state in less than 1 ps, and that the carrier lifetime is less than 0.5 ps. The fact that this general response exists suggests that the precipitates normally present in the annealed material are not needed in order to observe an ultrafast carrier lifetime for LT-GaAs. That is, at least in the as-grown material, point defects associated with the excess arsenic, like As antisite defects (As_{Ga}), may be responsible for this behavior. However, since annealed samples typically contain structural precipitate defects formed from this excess As, it appears possible that some other as yet undefined defects associated with the excess As may dictate the short time response. Assuming some defects are actually responsible for the fast response, this further suggests that under the right growth conditions, there may be an optimum number of defect centers in annealed LT-GaAs to provide the combination of an ultrafast carrier response, a high resistivity, and a high mobility.[13]

In order to verify the expected fast response of the annealed LT-GaAs material, photoconductive response measurements were performed using the same detector pattern under the same experimental conditions as described above. The temperature range explored for the annealed material was larger, however, stretching from 10 up to 300K. The temporal behavior of the switched waveforms also remained constant with temperature for the annealed samples, and these characteristics were found to be virtually the same as those observed from the as-grown sample (Fig. 3). This indicates that if the mechanisms responsible for ultrafast response are different for the annealed vs the as-grown samples, namely precipitates for the former and other defects for the latter, then the time signatures for their photoconductive lifetimes are, interestingly, still essentially the same. The amplitudes of the switched signals from the as-grown photodetectors, however, were not as large as those from the annealed detectors, indicating that the mobility of the annealed LT-GaAs was still significantly superior to that of the as-grown material.

To provide additional evidence of the temperature-dependent behavior of carriers in LT-GaAs, we have employed the transient reflectivity technique referred to in the section on photoconductive-switching experiments,[12] pumping and probing at an 800 nm wavelength (1.55 eV) for sample temperatures between 10 and 300K. Figure 4 shows the normalized reflectivity of the annealed and unannealed samples at different temperatures. The long negative tails on the as-grown samples are not yet completely understood, although the above experimental data suggest that the hopping carriers may somehow play a role in their behavior. As in the photoconductive switching mea-

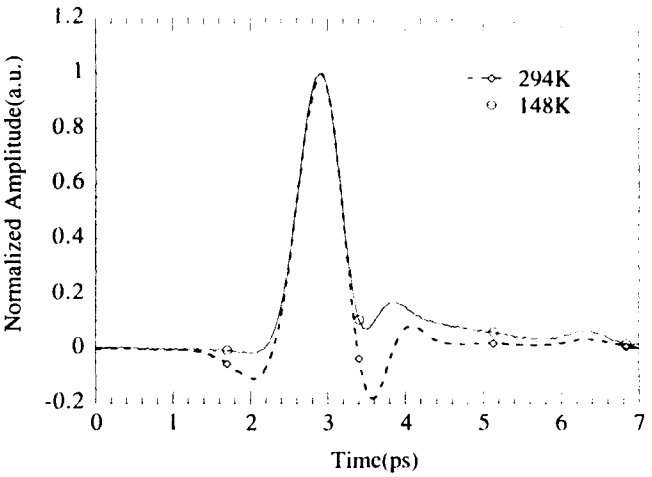

Fig. 3. Normalized photoconductive switch output for an annealed LT-GaAs sample at 294 and 148K. The characteristic times were virtually the same as those in Fig. 2, although the peak switched voltages were 5–10 times greater for the devices on the annealed material.

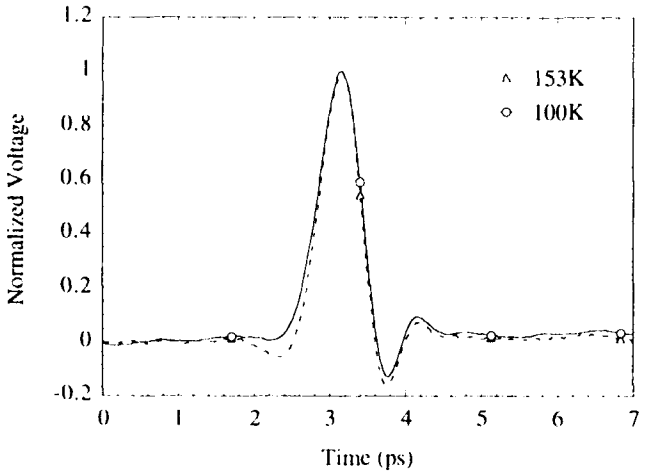

Fig. 2. Normalized photoconductive switch output for an unannealed LT-GaAs sample at 153 and 100K. The rise times are ~450 fs, with FWHM of ~600 fs. The peak voltage was ~1.8 V for each of these pulses.

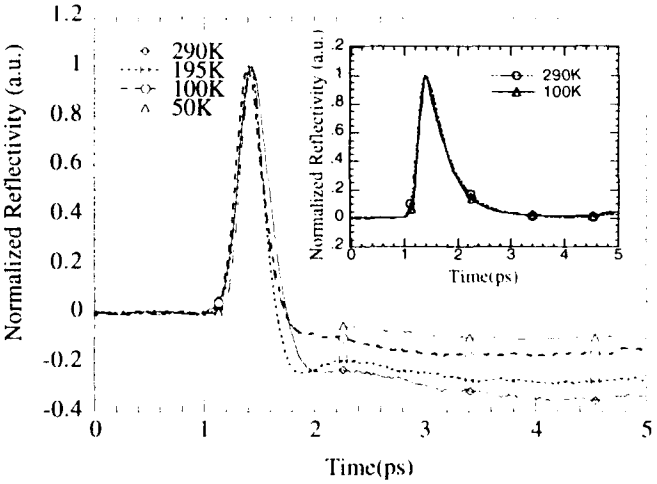

Fig. 4. Femtosecond transient reflectivity at 800 nm for the annealed (inset) and unannealed samples at several temperatures. The negative tails for the response of the as-grown sample did not appear to have any influence on the switching data in Fig. 2.

surements, one also observes that carrier lifetime appears to be independent of temperature, indicating that the fast carrier response must not be dependent on phonons, which one would expect to freeze out at low temperatures in LT-GaAs.

CONCLUSION

The first photoconductive switching measurements using an as-grown LT-GaAs layer have been demonstrated. Pulses were produced from the unannealed layers with nearly identical temporal characteristics—FWHM ≈0.6 ps and 1/e fall time of ~350 fs—as those generated using a layer from the same wafer after post-annealing. This provides evidence supporting contentions that the ultrafast carrier lifetime in LT-GaAs is mediated by some defects other than the structural arsenic-precipitate defect.

ACKNOWLEDGMENT

This research is supported by AFOSR contract numbers F49620-91-C-0044 and AFOSR-90-0214 (University Research Initiative) and by the National Science Foundation through the Center for Ultrafast Optical Science under STC PHY 8920108.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Structure and Carrier Lifetime in LT-GaAs

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The relationship between the structural quality of low-temperature GaAs layers and the photoexcited carrier lifetime has been studied. Transmission electron microscopy, x-ray rocking curves, time-resolved reflectance methods, and photoconductive-switch-response measurements were used for this study. For a variety of samples grown at temperatures in the vicinity of 200°C, subpicosecond carrier lifetimes were observed both in as-grown layers, as well as in the same layers after post-annealing and formation of As precipitates. These results suggest that the carrier lifetime, which was found to be shorter in the as-grown layers than in the annealed ones, might be related to the density of As_{Ga} antisite defects present in the layers. The annealed layers which contained structural defects before annealing appeared to exhibit the longest carrier lifetime due to gettering of As on these defects (and formation of relatively large As precipitates) and depletion of extra As (As_{Ga}) defects from the layer. It was found as well that the responsivity of detectors fabricated on these layers depended strongly on the structural quality of the layers, with the greatest response obtained not for the layers with the fewest defects, but for the layers with 10^7–$10^8/cm^2$ of pyramidal defects.

Key words: Carrier lifetime, low-temperature-grown GaAs, MBE, TEM

INTRODUCTION

The key to understanding the properties of GaAs layers grown by molecular beam epitaxy (MBE) at low temperatures (180–300°C) (LT-GaAs)[1-4] seems to be in the incorporation of high concentrations (up to 1.5%) of extra As, which leads to an increase in lattice parameter (up to 0.15%).[5,6] The crystal perfection of these layers is strongly related to parameters such as growth temperature, As/Ga flux ratio, and growth rate.[6] Layers grown at 200°C or above are monocrystalline, with no line or extended defects. However, breaking of crystallinity can be observed, especially for layers grown below 200°C.[5,6] At a specific critical layer thickness (related to the concentration of incorporated As), crystallinity breaks down, due to formation of polycrystalline grains or characteristic "pyramidal" defects with polycrystalline cores (mixture of GaAs and As grains) surrounded by dislocations, stacking faults, and microtwins.

Annealing of LT layers, either due to the growth at higher temperature of a cap layer on the top of the LT layer, or ex-situ annealing, leads to the formation of hexagonal arsenic precipitates.[5,7-10] These precipitates are semi-coherent with the matrix, and due to their formation, strain is relieved in the layer, and the lattice parameter decreases to the substrate value.

Such annealed layers exhibit semi-insulating behavior and thus may be employed as the active material for photodetector applications in which short lifetimes on the order of half a picosecond can be obtained.[4] After several years of study, however, it is still not clear if point defects (As antisite defects) or structural defects (precipitates, and line and plane defects) are responsible for the short reported lifetime. Some researchers tend to interpret short life-

(Received April 12, 1993)

time due to As precipitates present in the annealed layers.[11] Our previous studies indicated that short lifetimes can be obtained even for the as-grown layers, and that this lifetime was comparable to those obtained in annealed samples.[12] These results have been confirmed in another experiment which uses as-grown LT-GaAs layers as photoconductive elements.[13] There it was shown that at measurement temperatures lower then 160K, the material became highly resistive and displayed carrier lifetimes shorter than 1 ps, confirming that the presence of the precipitates is not necessary to obtain these interesting properties of the LT-GaAs layers. However, these studies did not provide structural information about these layers.

From our previous studies, it was evident that the responsivity of detectors fabricated on LT-GaAs layers was optimized for the layers not with the highest structural perfection, but for those where some low density of pyramidal defects was still present.[12] Since the best structural quality of the layers in this earlier investigation was obtained for an LT-layer with thickness less than 1 μm, it was believed that layer thickness might have influenced these measurements. To help explain these inconclusive results, new studies have now been performed on layers of the same thickness grown at different temperatures. Results on responsivity of detectors fabricated on these annealed LT-GaAs layers, and on the lifetime of two sets of annealed and as-grown materials, are presented and compared to those obtained earlier.

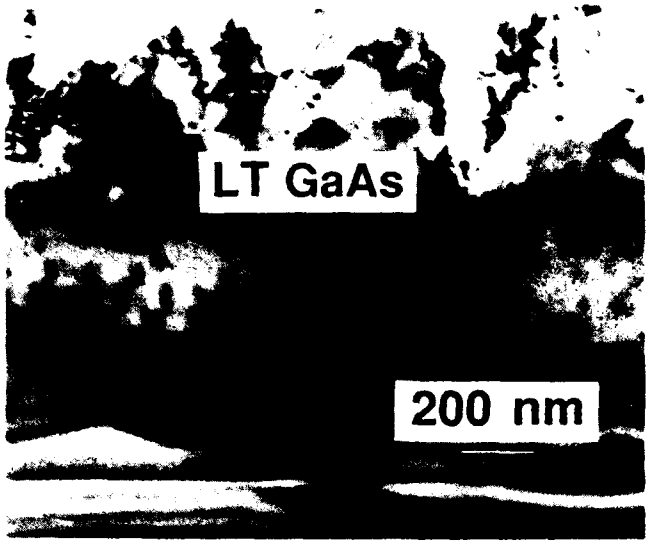

Fig. 1. Transmission electron micrograph showing the structure of sample I after annealing. Note the presence of pyramidal defects and formation of As precipitates.

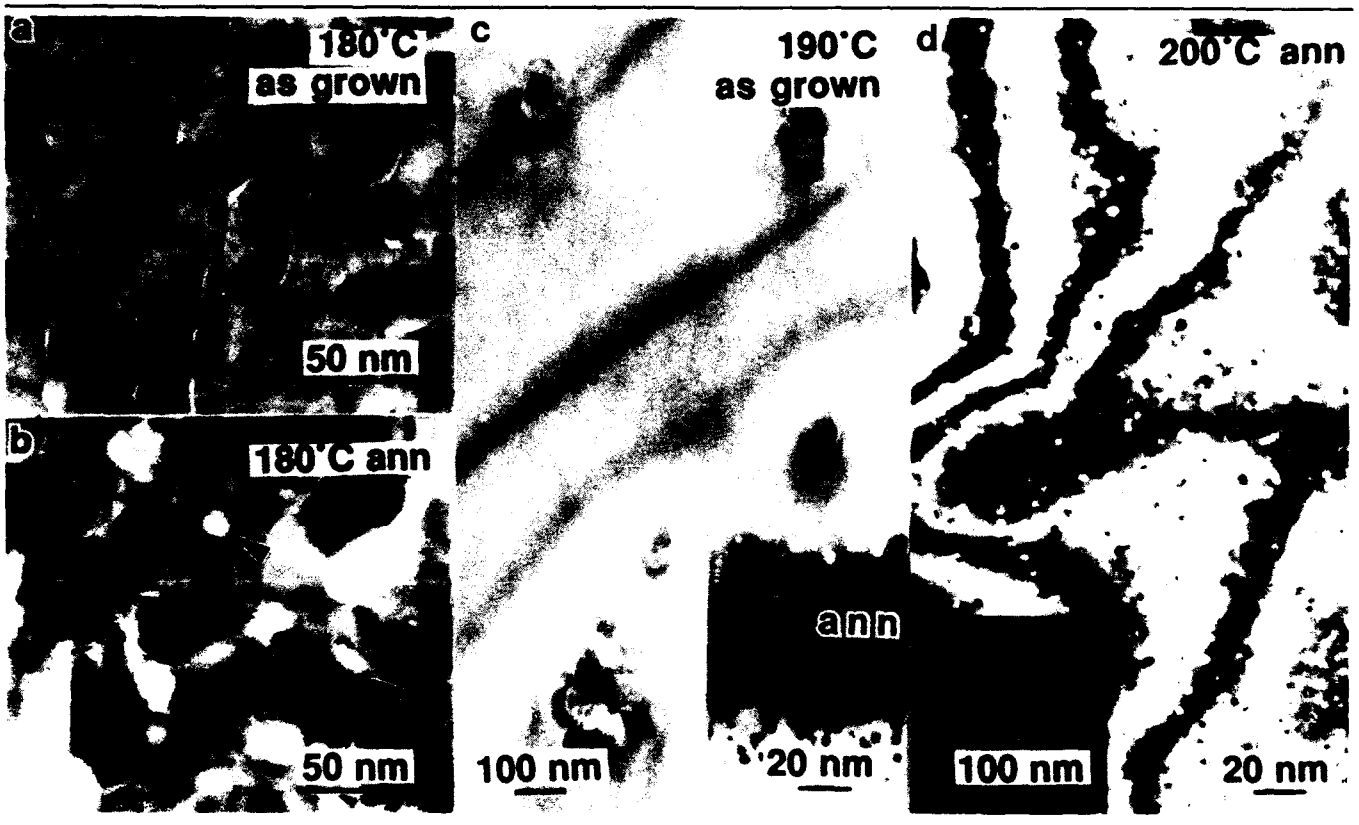

Fig. 2. (a) Transmission electron micrograph showing plan-view of as-grown sample I. Note that the top of the layer is polycrystalline and that grain boundaries show specific contrast. A close look by high-resolution TEM discovers rhombohedral As located in these areas. (b) Plan-view of the same sample annealed at 600°C for 10 min. Note voids (shown by arrows) present at grain boundaries suggesting As outdiffusion during annealing. (c) Distribution of pyramidal defects visible in plan-view micrograph of sample II. Large areas of this sample did not have these defects. An insert shows precipitates formed in this sample after annealing. (d) Plan-view of annealed sample III. Note lack of pyramidal defects and formation of precipitates after annealing. An insert shows formation of the rectangular figures on the sample surface after annealing.

EXPERIMENT

Two sets of samples have been studied: LT-GaAs layers, each 1.5 μm thick grown at different temperatures: 180°C (sample I), 190°C (sample II), and 200°C (sample III); and four different samples grown at 195°C with different thickness. Only the growth time was varied for the second set, resulting in different layer thicknesses: sample A, 3.3 μm; sample B, 1.75 μm; sample C, 1.6 μm; and sample D, 0.95 μm. Each sample was split into two pieces, with one part annealed in an MBE chamber in As overpressure at 600°C for 10 min. The structural quality of the layers was investigated using transmission electron microscopy (TEM) methods on plan-view and cross-section samples. Topcon 002B and JEOL 200CX transmission electron microscopes were used for these studies. In addition, x-ray rocking curves were taken to determine the lattice parameter of these layers and the concentration of excess As. The second part of each sample was used in the lifetime studies. Two kinds of measurements were made to determine lifetimes: time-resolved reflectance and photoconductive switching.

Annealed LT-GaAs samples are semi-insulating, and thus can be used as photoconductive switches. Therefore, coplanar strip transmission lines of Ti/Au were defined on these layers and a dc-biased gap in the lines was used as the detector. Electrical signals were generated by shorting the gap in the transmission line with 100 fs optical pulses from either a dye or Ti:sapphire laser. The generated electrical transients were measured using the external electro-optic sampling technique with a $LiTaO_3$ probe crystal. From the 1/e decay of the generated electrical pulse, the carrier lifetimes were determined.

RESULTS AND DISCUSSION

X-ray rocking curves showed different splitting between the substrate and the layers for all as-grown samples. This splitting in the sample I was $\Delta\theta$ = 0.065°, sample II, $\Delta\theta$ = 0.05° and sample III, $\Delta\theta$ = 0.045°. The samples A, B, C, and D had the same splitting, $\Delta\theta$ = 0.055 since they were grown at the same conditions. Transmission electron microscopy performed on cross-section sample I showed that pyramidal defects were already formed at the layer thickness of 0.85 μm and the remaining 0.65 μm top of the layer became polycrystalline (Fig. 1) with an average grain size of 60 nm (Fig. 2a). The presence of As was detected on grain boundaries. The sample II with the same 1.5 μm thickness had a very small density of pyramidal defects, covering only 0.3% of the layer surface (Fig. 2c). These defects were formed at ~1.4 μm from the interface, and their average density was estimated to be $10^7/cm^2$.

The sample III (1.5 μm thick) showed high crystalline perfection with no pyramidal defects found either in cross-section nor in plan-view samples (Fig. 2d). The four remaining samples A–D with variable layer thickness showed different structural quality. The sample A had pyramidal defects formed at a sample thickness about 1.35 μm from the interface, and the remaining 1.95 μm layer was polycrystalline. As in the sample I, As was present on grain boundaries. In sample B, 1.75 μm thick, pyramidal defects appeared at approximately the same layer thickness (~1.35 μm) as in sample A, suggesting that the growth conditions remained the same in sample B, as was intended. The pyramidal defect distribution was nonuniform in this sample, the defects being separated from each other in most of the sample, but coalescing in some areas. About 10% of the sample surface was covered by these defects yielding an average density estimated at $10^9/cm^2$. In sample C, 1.6 μm thick, large areas (hundreds of microns) were free of pyramidal defects, although in some areas single pyramidal defects separated from each other by more than 200 nm were found. The sample D, 0.95-μm thick, was practically defect-free.

After annealing, the arrangement of such structural defects as stacking faults, twins and dislocations remained the same as before annealing. However As precipitates were formed across the entire

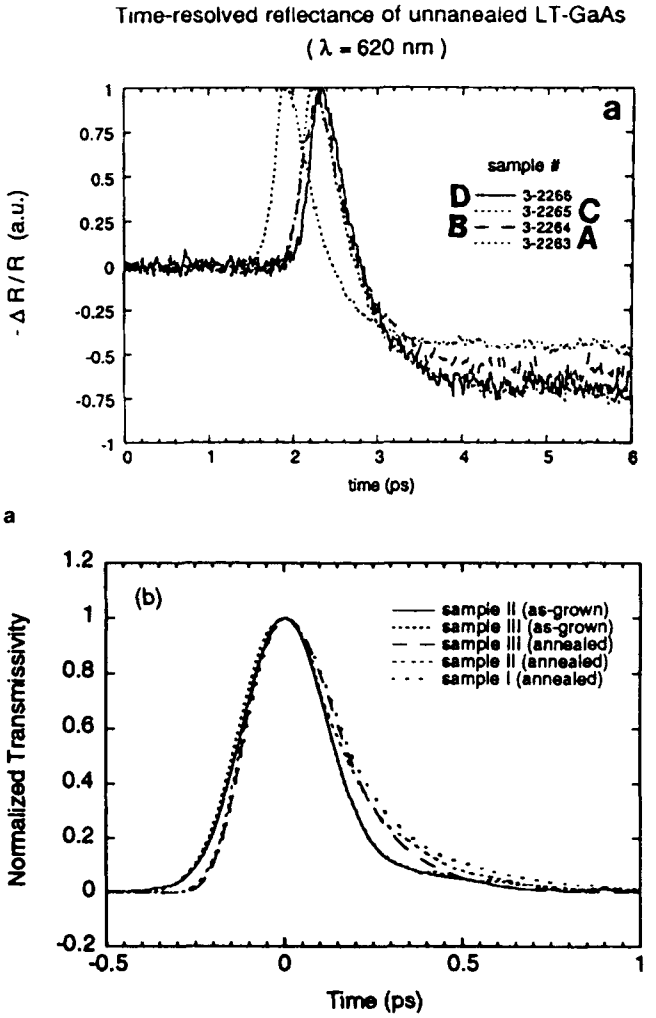

Fig. 3.(a) Optical transient reflectance for as-grown samples A–D. (b) Optical transient reflectance for as-grown and annealed samples I–III.

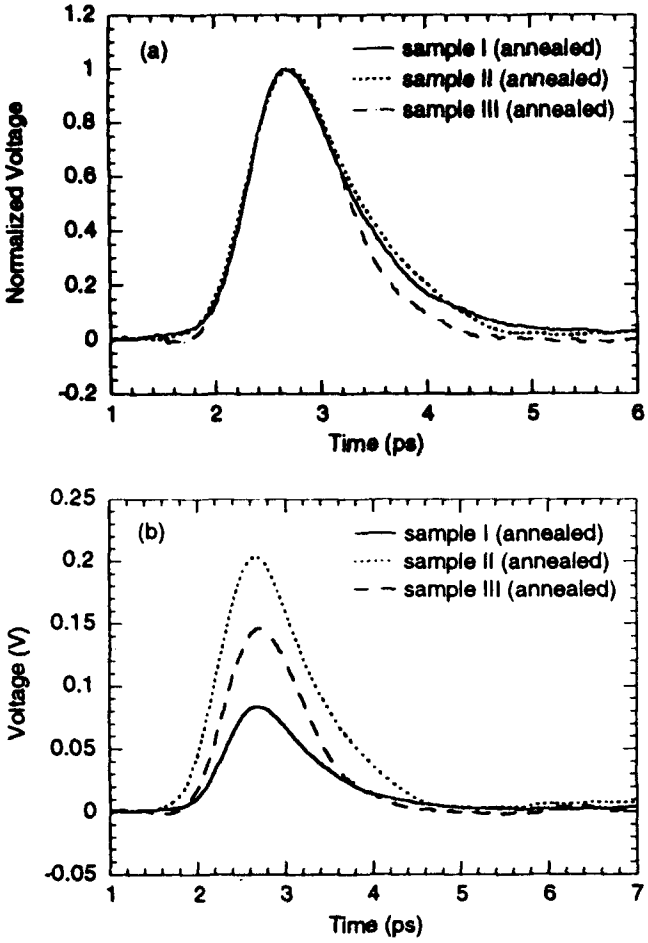

Fig. 4. (a) Normalized photoconductive response of samples I–III showing a 1/e time of 0.83 ps for sample I, 0.86 ps for sample II and 0.73 ps for sample III. (b) Photoconductive response for the samples I–III.

area of the samples (Fig. 1). In the monocrystalline samples, the size of the precipitates did not exceed 5–10 nm. In the samples with a polycrystalline surface, voids were formed at the grain boundaries (shown by arrows in Fig. 2b), indicating that As present at these places in as-grown samples partially disappeared from the subsurface area during annealing. In the monocrystalline part of the layer, hexagonal As precipitates were formed. They were larger in the vicinity of pyramidal defects (up to 30–40 nm), and their orientation relationship with the surrounding matrix was different compared to those precipitates formed in defect free areas, confirming our earlier observations.[10]

The carrier lifetime was determined for all the samples in this study using optical pump-probe techniques. As shown in (Fig. 3a), all as-grown samples with the same concentration of As and the same change of lattice parameter (samples A, B, C, and D) exhibit a similar, subpicosecond carrier lifetime (within experimental error). This was determined from transient reflectivity data as the 1/e decay time of the signal following the peak. The negative signals are not yet understood, although they may arise due to the fact that 2 eV photons were used in this instance to pump and probe carriers, substantially above the conduction band minimum. The same subpicosecond carrier lifetime was found in the annealed samples A–D from the transient reflectivity data. The pump-probe experiment was also performed on the three annealed and three as-grown layers having the different concentrations of As, samples I–III (Fig. 3b). An improved experimental scheme which used 1.5 eV photons (with full width at half maximum [FWHM] of 65 +/– 15 fs) to measure the transient transmissivity of the samples was utilized in this case. To measure transmissivity, the layers were all removed from their native substrates using etching techniques and an AlAs etch-stop layer which was incorporated just underneath the LT-GaAs, and grafted onto a quartz substrate.

The most interesting result that was found from the transmissivity data, and which confirmed the measurements on samples A–D, is that the relaxation time for each of these layers was subpicosecond in duration (for samples I–III, between 160–260 fs), and was shorter for the as-grown samples compared to the annealed ones. This seems to contradict previous suggestions indicating the precipitates are responsible for the fast carrier response.[11] It appears rather, that carrier lifetime could be related to the point defects associated with the excess As, such as arsenic antisite defects (As_{Ga}), which are present in these samples. The density of these defects decreases in annealed materials, and therefore the number of recombination centers also decreases so that the lifetime should be longer in annealed samples than in as-grown ones. This was indeed observed in all studied samples (I–III) and is clearly seen in the transmissivity data in Fig. 3b.

The shortest lifetime was measured for the unannealed sample I (not shown), followed by unannealed samples II and III, and then by the annealed samples III, II, and I, respectively. For the annealed samples our transmissivity data are consistent with the photoconductive response data shown in Fig. 4a, where the shortest lifetime was observed for annealed sample III (1/e = 0.73 ps), which did not have any structural defects, and the longest lifetime was observed for sample I (1/e = 0.86 ps), whose top 0.65 μm was polycrystalline.

That the shortest lifetime was measured on as-grown samples with structural defects was not surprising, since dislocations and stacking faults themselves can be the source of recombination centers, as demonstrated when the samples with structural defects such as GaAs on Si were used as photoconductive switches[14] with short carrier lifetimes. In our LT-GaAs samples, in addition to the structural defects a high density of point defects (As_{Ga}) was also present (with the highest density of As found for lower growth temperature). These As_{Ga} antisite defects can play an important role in the carrier recombination process. However, after initial studies, it was difficult to understand why, after annealing, the lifetime in the

samples containing structural defects was longer then in the samples which were defect free (sample III). The explanations are from the TEM data, which showed that annealing the LT-GaAs led to the formation of As precipitates, and that in the samples with structural defects much larger As precipitates are formed. Therefore, the layers with structural defects must be much more depleted of the point defects (in order to form larger precipitates) then the layers which are defect free (which form smaller precipitates and leave more As_{Ga} defects in the layer).

Since sample I had more defects than sample II, where only separated pyramidal defects were present, after annealing many more large precipitates were formed in sample I. Therefore, these layers were more depleted of As (As_{Ga}), and carrier lifetimes should have been longer in sample I, followed by sample II, and then III. This explanation is consistent with all our data (transmissivity and photoconductive-switching experiment). These data clearly show that point defects determine carrier lifetime much stronger than structural defects. The presence of the precipitates do not appear to make the lifetime shorter. However, it is possible that the opposite occurs, that more precipitates (or their larger dimension) decreases the density of point defects, such as As_{Ga} defects, thus limiting the number of recombination centers which can be involved in carrier recombination processes.

Another important feature to note is the dramatic enhancement of responsivity in the detector on sample II (Fig. 4b), which had large areas completely free of pyramidal defects, but also some areas with a defect density in the range of $10^7/cm^2$. This was also observed for sample C. It was expected that the high responsivity should be present in sample D, since this sample displayed much better structural quality than sample C. However, the responsivity in sample D decreased by four times compared to sample C. These results were confirmed on the samples with different As concentrations. The smallest responsivity was observed for the layers with a polycrystalline subsurface layer.

CONCLUSIONS

Systematic studies of the influence of the structural quality of LT-GaAs on carrier lifetime were performed. The lattice parameter (related to the excess As) was determined by x-ray rocking curves. Samples with the same concentration of As and different structural quality (samples A–D) were compared to ones with similar structural quality (structurally the sample A was comparable to sample I and sample D comparable to sample III) and different amounts of excess As. The structural quality of the these layers was studied by TEM in cross-section and plan-view samples.

Very short (subpicosecond) carrier lifetimes were found in all the LT-GaAs layers, with the annealed samples having longer carrier lifetimes than the as-grown ones. This observation is related to the decrease of density of As_{Ga} antisite defects in annealed layers compared to as-grown layers. The transmissivity and photoconductive switching data for the annealed samples indicate the shortest carrier lifetime occurs in the structurally perfect layers with small (5–10 nm) As precipitates. Gettering of As on structural defects (large 30–40 nm diameter) and strong depletion of As (As_{Ga}) in the layers is used to explain the longer carrier lifetimes in polycrystalline samples or in the samples with pyramidal defects.

The responsivity of detectors also seems to be closely related to the structural quality of the photoconductive layers. A low density of structural defects in the layers ensures higher response. The highest responsivity of detectors was found in the layers with some pyramidal defects separated from each other in the layers.

ACKNOWLEDGMENTS

This research was supported by AFOSR-ISSA-90-0009, through the U.S. Department of Energy, under Contract No. DE-AC03-76SF00098. The use of the Facility of the National Center for Electron Microscopy in Lawrence Berkeley Laboratory supported by U.S. Department of Energy under contract DE-AC03-76SF00098 is greatly appreciated. We would like to thank W. Swider for very careful and successful TEM sample preparation.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

$In_xGa_{1-x}As$ (x = 0.25–0.35) Grown at Low Temperature

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$In_xGa_{1-x}As$ (x = 0.25–0.35) grown at low temperature on GaAs by molecular beam epitaxy is characterized by Hall effect, transmission electron microscopy, and ultrafast optical testing. As with low temperature (LT) GaAs, the resistivity is generally higher after a brief anneal at 600°C. High-resolution transmission electron microscopy shows all the as-grown epilayers to be heavily dislocated due to the large lattice mismatch (2–3%). When the layers are annealed, in addition to the dislocations, precipitates are also generally observed. As with LT-GaAs, the lifetime shortens as growth temperature is reduced through the range 300–120°C; also, the lifetime in LT-$In_xGa_{1-x}As$ is generally shorter in as-grown samples relative to annealed samples. Metal-semiconductor-metal photodetectors fabricated on the material exhibit response times of 1–2 picoseconds, comparable to results reported on GaAs grown at low temperature, and the fastest ever reported in the wavelength range of 1.0–1.3 μm.

Key words: LT-InGaAs, MBE, MSM, photodetector

INTRODUCTION

Ultrafast optoelectronic applications require photoconductors with subpicosecond carrier lifetimes and high resistivity. Subpicosecond carrier lifetimes have previously been achieved by lowering growth temperatures to ≈200°C in molecular beam epitaxy (MBE)-grown GaAs epilayers.[1] The semi-insulating nature and high breakdown-voltage of these epilayers also enabled the fabrication of submicron interdigitated photodetectors with the unprecedented bandwidth of 375 GHz and a responsivity of ≈0.1A/W.[2] These properties have been attributed to excess As incorporation during low-temperature MBE growth.[3] In this article, we report our results of investigations in low-temperature MBE-grown $In_xGa_{1-x}As$ epilayers for applications to near-infrared wavelength detection.

Because lattice-matched $In_xGa_{1-x}As$ (x = 0.53) exhibits a very low resistivity of $\approx 10^{-2}$ Ω-cm, we chose to investigate the growth of $In_xGa_{1-x}As$ ($0.25 \leq x \geq 0.35$) on GaAs to produce higher resistivity epilayers. As with LT-GaAs, LT-InGaAs resistivity also increased after a brief anneal at 600°C. Transmission electron microscopy (TEM) showed that all the as-grown epilayers were heavily dislocated due to the large lattice mismatch (2–3%). When the layers were annealed, in addition to the dislocations, precipitates also formed. The precipitates were arsenic-rich, though whether these are pure arsenic clusters, as found in annealed LT-GaAs, has not yet been confirmed.

(Received April 12, 1993)

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Table I. Growth Data of $In_xGa_{1-x}As$ Wafers: X = 0.25

Wafer	Growth Temp. (°C)	Anneal	Resistivity Ω-cm	Mobility (cm^2/V-s)	Life-time (ps)	Responsivity (10^{-5} A/W)	Structure
1251	300	No	1.6×10^{5}	4120	12.5	3.1	Single crystalline, heavily dislocated
1252	300	Yes	6.8×10^{3}	2950	21.0	5.2	Like 1251, with precipitates
1623	250	No	5.5×10^{2}	1110	8.0	3.0	Single cyrstalline, heavily dislocated
1625	250	Yes	1.4×10^{3}	2730	40.0	3.0	Like 1623, with precipitates
1624	200	No	1.6×10^{2}	20	3.0	0.6	Single crystalline, heavily dislocated
1626	200	Yes	8.8×10^{3}	2260	7.3	5.5	Like 1624, with precipitates
1713	160	No	85	8.5	Unmeasur-able	—	High defect content, some twin grains
1714	160	Yes	4.5×10^{4}	4210	2.0	0.4	Like 1713, with precipitates

Table II. Growth Data of $In_xGa_{1-x}As$ Wafers: X = 0.35

Wafer	Growth Temp. (°C)	Anneal	Resistivity Ω-cm	Mobility (cm^2/V-s)	Life-time (ps)	Responsivity (10^{-5} A/W)	Structure
1747	200	No	71	44	Unmeasure-able	—	Epi, high defect content, many twin grains
1748	200	Yes	1320	303	4.0	3.0	Like 1747, with precipitates
1749	160	No	270	91	4.5	0.2	Amorphous with surface "cells" of crystallization
1750	160	Yes	260	894	5.5	2.1	Polycrystalline with near-substrate epi layer, reduced defect content
1751	120	No	1.8×10^{3}	1600	<1.0	0.03	Completely amorphous
1752	120	Yes	77	550	7.0	3.1	Epi w/twins, low defect content

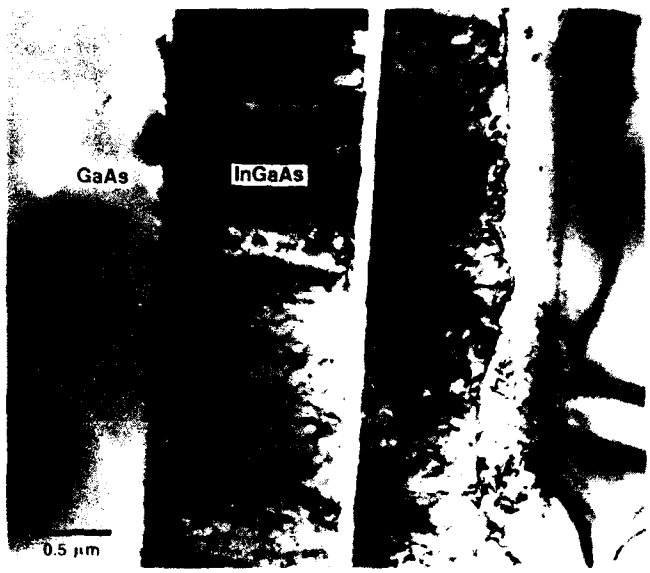

Fig. 1. Transmission electron microscopy cross section of 3-1626, grown at 200 C and annealed, is representative of x = 0.25 layers grown in the 200–300 C range and annealed. Precipitates and dislocations are prominent.

To ascertain the response of the InGaAs material for high-speed photoconductive detectors, we measured high-temporal-resolution optical switching. Like LT-GaAs, $In_xGa_{1-x}As$ lifetimes shorten as growth temperature is reduced through the range 300–120 C; also, LT-$In_xGa_{1-x}As$ lifetimes are generally shorter in as-grown samples than in annealed samples. We fabricated metal-semiconductor-metals (MSMs) by electron beam lithography with finger-widths and spacings of 2.0, 1.0, 0.5, and 0.2 μm. The MSMs were tested with the high-temporal-resolution optical switching measurement. Our results yielded the fastest detectors (1–2 ps full width at half maximum [FWHM]) ever reported in the 1.0–1.3 μm range.

MATERIALS GROWTH

We grew all of the InGaAs material layers in a Varian GEN II MBE system on 3 in GaAs substrates using indium-free substrate holders. The substrates were liquid encapsulated Czochralski (LEC) semi-insulating (100) +0.5 . The GaAs native oxide was desorbed in the MBE growth chamber at 600 C under an As_4 flux. Substrate temperatures were reduced to 120–300 C for the $In_xGa_{1-x}As$ growth. We used a growth rate of 1.0 μm/h with a V/III beam equivalent pressure ratio of 15. Films were grown to thicknesses of 1.0–1.2 μm. After layer growth, some layers were annealed in-situ by raising the substrate temperature to 600 C for 15 min. This approach of comparing separate as-grown and annealed wafers may not always be appropriate, especially for studies concerned with growth in a narrow temperature window where a small change in growth temperature might strongly alter the as-grown or annealed properties. However, careful analysis of the as-grown and annealed layer properties shows this not to be an issue

in this study. Tables I and II summarize the growth and characterization data. Similar to LT-GaAs, after an anneal precipitates are usually formed, coincident with a substantial increase in resistivity. The lowest temperature grown samples are an exception to this as described below.

TEM CHARACTERIZATION

We examined all the samples using a JEOL JEM-2010 transmission electron microscope. Operating voltage was 200 kV. X-ray spectra were obtained using a LINK eXL energy dispersive spectrometer system.

The micrographs and x-ray spectra from Sample 3-1626, grown at 200°C and annealed, show results that are representative of all the x = 0.25 samples grown at 200–300°C and then annealed. The boundaries of the layer are not very sharp; some roughness in the free surface and at the GaAs interface are visible. In addition to the high dislocation density, precipitates are also visible in the LT layer, even at magnifications of 40,000 (see Fig. 1).

Comparing x-ray spectra obtained from precipitates, the InGaAs matrix, and the GaAs substrate confirmed the As-rich nature of the precipitates. However, lattice fringes in the precipitates (see Fig. 2) are measured as 3.30Å which is not an obvious match with any of the pure As phases. This is in contrast to our earlier work on LT-GaAs, where we measured a 2.8Å spacing, comparing well with the most prominent d-spacing in rhombohedral arsenic (2.77Å).[1]

We can summarize the LT-InGaAs (x = 0.25) layers grown on GaAs substrates from 200–300°C by the following:

- The layers in all samples were epitaxial single crystals with high quality InGaAs interfaces.
- Precipitates were not observed for samples in the as-grown condition.
- The samples subjected to an anneal contained precipitates and these precipitates were not noticeably different for the samples and temperatures examined.
- The precipitates are As-rich, but no conclusive electron diffraction patterns could be obtained matching the precipitates to one of the pure As phases.
- The precipitates are coherent with their InGaAs matrix and their contrast in bright field TEM images is very sensitive to tilt/diffracting condition, which when combined with the observed shapes suggest a very thin disk precipitate.
- All LT layers contained a higher dislocation density than the adjacent GaAs substrate, but the available data cannot substantiate if more dislocations are present in the samples containing precipitates.

Some differences from the above results obtained at 200–300 C were observed as the growth temperature was lowered to 160 C. For example, Sample 3-1713, grown at 160 C, has planar defects along the <111> directions which appear to be very fine "micro"-twins (Fig. 3). The surface of the layer is somewhat rough, showing some topography due to the twins emerging at the surface. A few boundaries extend through the LT layer normal to the substrate and appear to separate very large twin-oriented grains or domains. Some of these latter boundaries may simply be low-angle grain boundaries.

The structure of Sample 3-1714, which was grown at 160°C and then annealed, is not very different from Sample 3-1713. The number of boundaries extending through the layer normal to the substrate is larger and these "macroscopic"-twin domains in the LT layer give characteristic twin diffraction patterns. The density of the micro-twins within a given domain appears reduced. As-rich precipitates are also in this sample, and some are substantially larger than those seen in the 200–300°C samples.

As we approached x = 0.35, the crystalline structure of our samples became more varied. Sample 3-1747

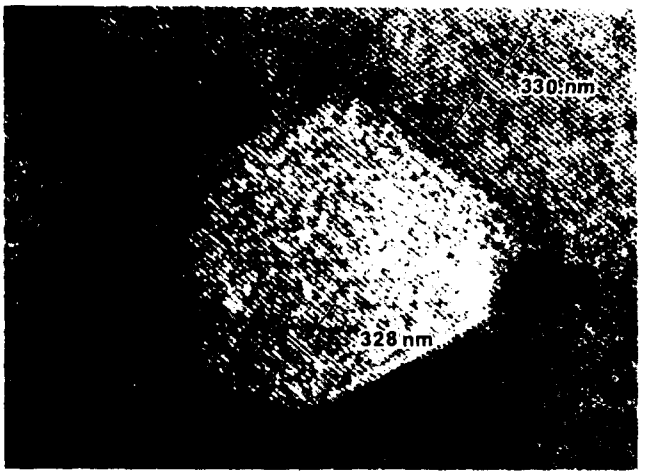

Fig. 2. High resolution imaging precipitate in 3-1626. Lattice fringe spacings of 3.3A do not conform to any known phases of pure arsenic.

Fig. 3. Transmission electron microscopy cross section of 3-1713, grown at 160 C, showing microtwin defects residing along <111> planes.

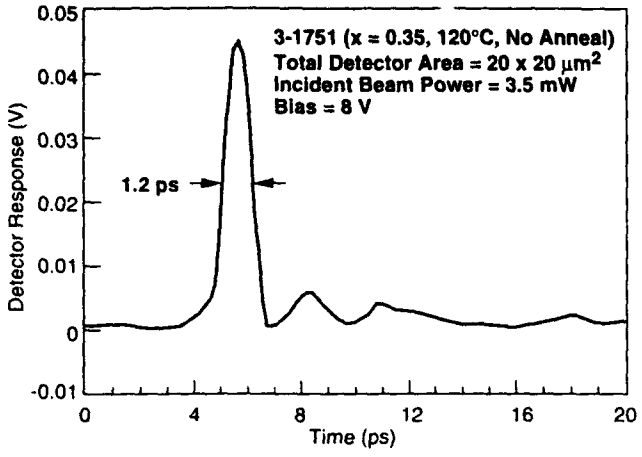

Fig. 4. Metal-semiconductor-metal detector results for 3-1751, x = 0.35 grown at 120°C

angle grain boundaries.

The structure of Sample 3-1714, which was grown at 160°C and then annealed, is not very different from Sample 3-1713. The number of boundaries extending through the layer normal to the substrate is larger and these "macroscopic"-twin domains in the LT layer give characteristic twin diffraction patterns. The density of the micro-twins within a given domain appears reduced. As-rich precipitates are also in this sample, and some are substantially larger than those seen in the 200–300°C samples.

As we approached x = 0.35, the crystalline structure of our samples became more varied. Sample 3-1747 (grown at 200°C) was predominantly epitaxial with many twin related grains or domains, very similar to what was seen in 3-1713 (grown at 160°C) and 3-1714 (grown at 160°C and annealed). The higher density of the macro-twin domains gives this sample a more columnar grain appearance.

Sample 3-1748, grown at 200°C and annealed, is very similar to 3-1747 and bears the same relationship to 3-1747 as 3-1714 does to 3-1713 (i.e., As-rich precipitates and a smaller concentration of micro-twin defects). We noted that there are large equiaxed grains near the surface of the LT layer, which could have resulted from a recrystallizing during the anneal.

Sample 3-1749 (grown at 160°C) has different regions of crystalline structure. The layer is mostly amorphous, and has a number of polycrystalline "cells" at the surface which appear to have crystallized into the amorphous material. The layer is thickest where there is the most polycrystalline surface material, which may indicate some significant difference in density between amorphous and crystalline material. The polycrystalline cells have a structure very much like that of Sample 3-1747 (grown at 200°C).

Sample 3-1750, grown at 160°C and annealed, has three regions demarcated: first, a near-substrate epi-region; second, a predominant, large, equiaxed grain center region; and third, a smaller, equiaxed grain surface region. We saw no evidence of precipitates in the polycrystalline regions. We could not ascertain if any precipitates are in the highly strained and defective epilayer, but none stands out clearly. X-ray information from the epilayer did not indicate any As-rich precipitates.

Sample 3-1751 (grown at 120°C) is the most uninteresting from a microstructural standpoint because it is completely amorphous. Such amorphousness is totally absent in Sample 3-1752 which was grown at 120°C and annealed. The anneal produced a crystalline layer without the high defect density found in previous samples as was indicated by their diffraction patterns. No images were observed that led us to believe there are precipitates in this sample. This may indicate that excess arsenic is not readily incorporated into films grown at the lowest temperatures.

We can summarize the TEM findings briefly by the following:

- For both single and polycrystalline samples, precipitates are always observed after anneals and never before.
- The grain structure and micro-twin density of the poly samples also changes significantly after anneals.
- Amorphous samples are crystallized by the anneals, and precipitates are not observed in either as-grown or post-annealed samples.

OPTICAL TESTING AND DEVICE RESULTS

Photoconductively Switched Coplanar Electrodes

Optical response testing involves coplanar electrodes that are photoconductively switched. A 15 μm gap switch (biased at 15V) is defined in a coplanar stripline with a characteristic impedance of 73Ω. External electro-optic sampling using a $LiTaO_3$ microprobe, and a CPM dye laser producing 100 fs optical pulses at 630 nm is used to measure the ultrafast switch response.[5] Tables I and II also show the carrier lifetimes and responsivities of the various epilayers, as obtained from the above measurement, and discussed elsewhere in detail.[6] Growth temperatures in the range of 120–160°C produced single picosecond carrier lifetimes. Annealing, in general, improves the responsivity while degrading the lifetime.

MSM Photodectors

To increase responsivity as a photoconductive detector, the electrode spacing can be reduced if the resistivity of the epilayer is high enough to sustain practical voltage levels.[2] Our MSM detectors were fabricated by hybrid lithography on wafers 3-1714 and 3-1751, the wafers with the shortest recombination times for x = 0.25 and x = 0.35. Detector fabrication and results are discussed in detail elsewhere.[7] Figure 4 shows the MSM detector responses for x = 0.35 material (Sample 3-1751, grown at 120°C) for 2 μm finger widths and spacings. The 1.2 ps of response at FWHM observed for the 3-1751 sample devices is

the fastest measured speed for a long-wavelength photodetector. The oscillations in the responses are due to reflections within the electro-optic probe.

The detectors on the 35% LT-InGaAs have very poor responsivity (0.0003 A/W), a hundred times worse than the x = 0.25 layer, consistent with the photoconductive switch data (Tables I and II), and presumably a result of the amorphous nature of the epilayer. The 25% LT-InGaAs devices, with responsivities of 0.03 A/W, are nearly comparable to MSMs made on LT-GaAs (0.1 A/W). The lower responsivity of the InGaAs may be related to lattice mismatch induced dislocations and the heavy twinning observed in the TEM. The temporal responses of the 1 and 2 μm detectors are also consistent with our photoconductive switch data presented in Tables I and II. However, the response slows down as the size of the electrodes is reduced, due to increased capacitance since total detector area remains the same as the number of fingers is increased.[6,7]

CONCLUSIONS

Given the current state of this technology, reasonable tradeoffs can be made between speed and responsivity. For example, as Table II indicates, Sample 3-1748 (grown at 200°C and annealed) exhibits one of the best combinations of a recombination time and responsivity. The recombination time of 4 ps, although certainly not record setting, is, however, slightly faster than the fastest InGaAs/InP PIN reported[8] and would provide a bandwidth over 100 GHz; also, its responsivity measured in the 15 μm gap configuration of 3×10^{-5} A/W is one of the highest in evaluated LT layers. Thus, it offers an excellent compromise between speed and responsivity, being roughly four times slower than the devices made on sample wafer 3-1751 (grown at 120°C), yet approximately 100 times more sensitive.

For the future, by reducing the total detector area, the RC limitations can be pushed down below the 1 μm level. With backside illumination, anti-reflection coatings and further materials optimization, the detector properties can be substantially improved. So, in summary, LT-$In_xGa_{1-x}As$ (x = 0.25–0.35) grown on GaAs has excellent promise as a photodetector in the 1.0–1.3 μm range. The device so produced is integratable with other GaAs devices, giving it a great advantage over InP-based PINs. As with LT GaAs, the resistivity is generally higher after a brief anneal at 600°C, coinciding with the formation of As-rich precipitates. Also, as with LT-GaAs, the lifetime shortens as the growth temperature is reduced; also, the lifetime in LT-$In_xGa_{1-x}As$ is generally shorter in asgrown samples than in annealed samples.

ACKNOWLEDGMENT

This research is supported by AFOSR contract numbers F49620-91-C-0044 and AFOSR-90-0214 (University Research Initiative) and by the National Science Foundation through the Center for Ultrafast Optical Science under STC PHY 89201 08.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Femtosecond Optical Response of Low Temperature Grown $In_{0.53}Ga_{0.47}As$

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A femtosecond, tunable color center laser was used to conduct degenerate pump-probe transmission spectroscopy of thin film low temperature grown molecular beam epitaxy $In_{0.53}Ga_{0.47}As$ samples. Low temperature molecular beam epitaxy $In_{0.53}Ga_{0.47}As$ exhibits a growth-temperature dependent femtosecond optical response when probed near the conduction band edge. Below T_g = 250°C, the optical response time of the material is subpicosecond in duration, and we observe induced absorption, which we suggest is due to the formation of a quasi–"three-level system."

Key words: Carrier lifetime, low-temperature-grown GaAs, molecular beam epitaxy

INTRODUCTION

Low Temperature III-V molecular beam epitaxy (LT-MBE) grown materials have generated significant interest recently, due to their ultrafast recombination time, their relatively high mobility (even after post growth anneal), and the high resistivity as a result of this anneal.[1] The optical response of LT-MBE GaAs and $In_{0.52}Al_{0.48}As$ has been examined and their usefulness as a photoconductive switch has been demonstrated.[2-5] The ternary III-V material $In_{0.53}Ga_{0.47}As$, lattice matched to InP, has been used extensively for optoelectronic devices operating at the direct band gap of 0.75 eV. Here, we report the results of an ultrafast characterization of the optical response of LT-MBE $In_{0.53}Ga_{0.47}As$ as a function of growth temperature and excitation intensity, near the conduction band edge. We have investigated the optical response of samples grown over a range of temperatures from 660°C down to 250°C, using a range of wavelengths and optical intensities.

(Received April 12, 1993)

EXPERIMENTAL CONDITIONS

Sample Preparation and Characterization

The LT-MBE $In_{0.53}Ga_{0.47}As$ samples were grown at the U.S. Army Research Laboratory and are listed in Table I. The samples were grown over a variety of temperatures, and the growth rate was 1 μm/h on (001) oriented semi-insulating InP substrates. The temperature of the MBE chamber was carefully ramped down to the desired growth temperature under As-rich conditions. The growth temperature, measured with a reactor thermocouple, is estimated to be 100°C higher than the actual growth temperature (due to offset). The beam equivalent pressure

Table I. LT-MBE $In_{0.53}Ga_{0.47}As$ Samples

Sample No.	Growth Temp. (°C)	Crystal-linity	Minority Carr. Density (/cm³)	μ (cm²/V.s)
G909	660	SC	4.0×10^{15}	5400
G906	550	SC	1.5×10^{16}	4000
G915	300	SC/PC	1.5×10^{17}	2350
G908	250(A)	R	2.7×10^{17}	150
G910	250	R/PC	2.0×10^{17}	1100

A = annealed in-situ for 10 min at 600°C under As overpressure; SC = single crystal, PC = polycrystalline, and R = relaxed.

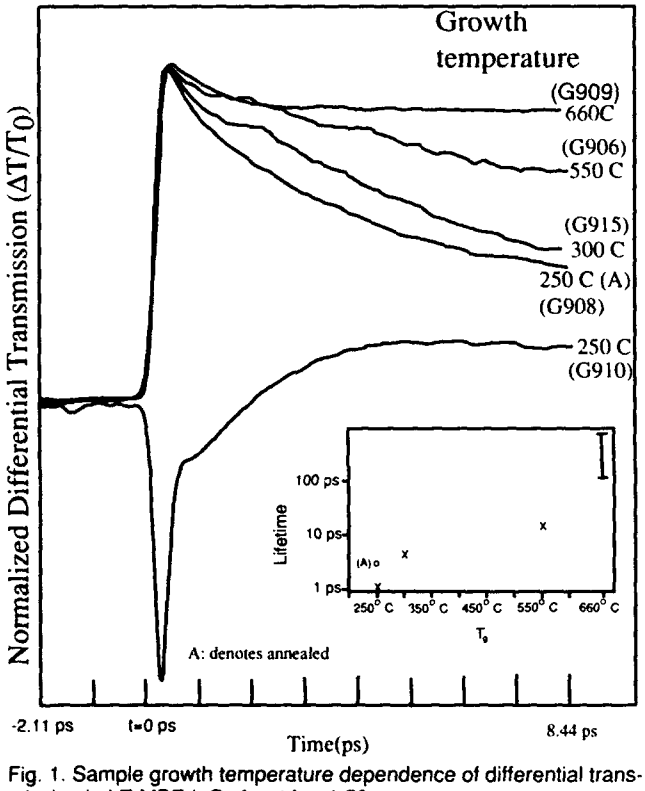

Fig. 1. Sample growth temperature dependence of differential transmission in LT-MBE InGaAs at $\lambda \approx 1.56$ μm.

ratio was approximately 35, and we used reflection high energy electron diffraction and double crystal x-ray diffraction to gain a qualitative measurement of the crystallinity. All samples were grown nominally lattice matched to InP. From previous studies, it is generally accepted that in LT-MBE GaAs and $In_{0.52}Al_{0.48}As$, excess As incorporation increases as the growth temperature is lowered, and below 200°C the material grows polycrystalline as the number of defects rapidly increases.[6,7] Hall measurements were taken in order to determine the majority carrier (electron) concentration, the resistivity, and the mobility. The LT-MBE layers were unintentionally doped; and, therefore, we assume that the donor concentration in these layers is due to the excess As. Some of the samples were annealed in-situ following growth, at a temperature of 600°C, under an As overpressure, for ten min. The large density of states near the band edge, due to traps/defects, changes the absorption curve. Absorption plots of normal growth temperature and LT-MBE (250°C) $In_{0.53}Ga_{0.47}As$ samples, taken using a Perkin-Elmer spectrophotometer, indicate the large number of near band edge states in the low temperature grown material.

Experimental Apparatus

Our experimental apparatus is the typical pump-probe femtosecond (fs) time resolved transmission and reflection spectroscopy setup. The pump-probe source is an APM NaCl:OH(-) color center laser, which delivers nominally 200 fs pulses, tunable from 1.47–1.65 μm, at a 76 MHz repetition rate, and with a useable output power of 100 mW. We were able to tune the laser (and hence our excitation energy) over a variety of wavelengths, although we concentrated our investigations near the bottom of the Γ valley, obtaining both transmitted and reflected signals, although qualitatively there was no difference in the temporal response.

EXPERIMENTAL RESULTS

We observe that in LT-MBE $In_{0.53}Ga_{0.47}As$, the recombination time drops as the growth temperature is reduced. Figure 1 is a composite plot of the differential transmission through samples G909, G906, G915, G908, and G910 where the decay times (recombination times) are respectively >100 ps, ~12 ps, 4.3 ps, 2.8 ps, and 520 fs. Sample G909 is the bulk control sample grown at normal MBE growth temperatures. Here we define the decay time as the 1/e point of the decay from the peak of the transmitted or absorbed signal. Note the linearity of the relationship between the sample growth temperature and the log of the decay time, shown in the Fig. 1 inset. This data was all taken at an excess energy of 50 meV above the conduction band edge. Qualitatively, there was no difference in decay time over the range of wavelengths used to excite the samples. The estimated excited carrier density is $3 \times 10^{17}/cm^3$ which corresponds to a change of absorption of $\sim 5 \times 10^2/cm$. The measured absorption of G910 was $7.8 \times 10^3/cm$ at 1.54 μm. We note that both G910 and G908 samples were grown at ~250°C, but only G908 has been in-situ annealed at high temperature. Sample G910 displays induced absorption, while sample G908 is bleached. Note that the bulk control sample, G909, displays behavior indicative of the bleaching of optically coupled Bloch states by the injection of an initially nonthermal electron-hole plasma. Because there is no scattering to satellite valleys, we observe the thermalization and cooling of the plasma near the conduction band edge, including carrier cooling by LO phonon emission and the effects of band gap renormalization.[8]

DISCUSSION

The minority carrier lifetime is inversely dependent on the product of the defect density, the capture cross section, and the thermal velocity.[3] Utilizing reasonable data from LT-MBE GaAs and $In_{0.52}Al_{0.48}As$ re-

sults, one would expect that the recombination time should drop below 1 ps as the number of defects exceeds 5×10^{17} cm^{-3}.[3] Due to the large number of traps, it has been established that the recombination time reduction is due to nonradiative processes.[9] We observe a reduction in recombination time as a function of growth temperature in LT-MBE InGaAs, consistent with that previously observed in LT-MBE GaAs and $In_{0.52}Al_{0.48}As$.[4] Sample G908 (T_g = 250°C) displays induced absorption and after annealing (Sample G910), the ultrafast component reverses sign to display transient bleaching. Induced absorption in 200°C grown unannealed $In_{0.52}Al_{0.48}As$ has been observed and when annealed the sample behavior also changes from induced absorption to induced bleaching.[4] The induced absorption has been previously explained as possibly due to the large density of near band edge states, created from the traps/defects, which results in larger free carrier absorption (FCA).[4] The signal change from induced absorption to transient bleaching was attributed to the net reduction of trapped states as a result of As precipitate formation by annealing. At the minority carrier densities (2.7×10^{17} cm^{-3}) and measured mobilities in sample G910, the FCA is less than 10 cm^{-1}, and is negligible compared to one photon absorption (~10^3 cm^{-1}). Additionally, surface field effects can be ignored because the absorption depth is significantly longer than our sample thickness, and we have conducted differential transmission spectroscopy, as opposed to previously conducted LT-MBE GaAs transient reflectivity measurements.[3,4]

It is well established that in GaAs[1] the As_{Ga} antisite defect is associated with the "deep" electronic level EL2. When LT-MBE GaAs is grown, the concentration of the antisite defect states dramatically rises to ~ 10^{19} /cm^3, and depending upon the location of the Fermi energy and the lattice temperature these states are significandy populated. The deep state defect EL2 has been recently observed in $In_xGa_{1-x}As$ grown on GaAs,[6] with x in the range .045 ~ x < 0.18. The energy level of these defects remains roughly at midgap, and scales appropriately as the In composition is increased. The defects are formed well away from the Ga substrate. Our analysis suggests that the LT-MBE material acts like a three-level system, as shown in Fig. 2. Low-temperature MBE $In_{0.53}Ga_{0.47}As$ forms defect states near the band edge which enhance the Urbach tail. Deep states with extended wavefunctions in k-space are created, and these are associated with antisite defects positioned roughly at midgap. These deep states are of the density of 10^{18}–10^{19} cm^{-3}, which is significantly *greater* than the conduction band density of states (DOS) at the Γ valley center. The Fermi energy at 300K is near the deep state location which suggests that most of the states are occupied. It is also well known that (in GaAs) these deep states act as traps/recombination centers. From Fig. 2, there are three likely optical transitions for 1.55 μm (0.75 eV) radiation. Transition 1 is the usual conduction-valence band transition. Transition 2 is the transition from the *occupied* deep state to the conduction band. Transition 2 is strong because these deep donor states are delocalized in k-space. Transition 3 is a transition from the heavy hole valence band to an unoccupied defect state. The deep states are heavily populated at room temperature, and therefore Transition 3 will most likely occur only when a significant number of these states are vacant.

The differential transmission signal will reflect the sum of all three of these transitions. In the bulk 660°C MBE material, only Transition 1 is observed, and the femtosecond optical response has been described previously as transient bleaching (see Fig. 1, T_g = 660°C). In LT-MBE materials, Transition 2 may be stronger because of the larger DOS, and sees a much larger absorption cross section than Transition 1. When the deep states have been depopulated (by a pump pulse exciting Transition 2), the absorption cross section for Transition 3 will also be much larger than that of Transition 1. Thus, immediately after the pump pulse illuminates the sample, the sum of the three transitions results in *induced absorption*. After a few ps, when trapping by the recombination centers and cooling of the total distribution to the lattice temperature has occurred, Transitions 2 and 3 are effectively shut off, and we observe band filling of the near band edge states. Using this simple three transition level model, one would expect that significant induced absorption should exist as low as ~0.375 eV, although we have not measured this as of yet. Additionally, since we propose that Transitions 2 and 3 account for the induced absorption, and these two transitions increase in strength with increasing deep defect density, induced absorption may be present in all of the samples. The induced absorption may be masked by induced transparency until the defect density is above 10^{17}/cm^3, and the sample starts to become polycrystalline.

CONCLUSIONS

In summary, we have investigated and modeled the femtosecond optical response of LT-MBE $In_{0.53}Ga_{0.47}As$ as a function of wavelength, excitation intensity, and thin film sample growth temperature. We have deter-

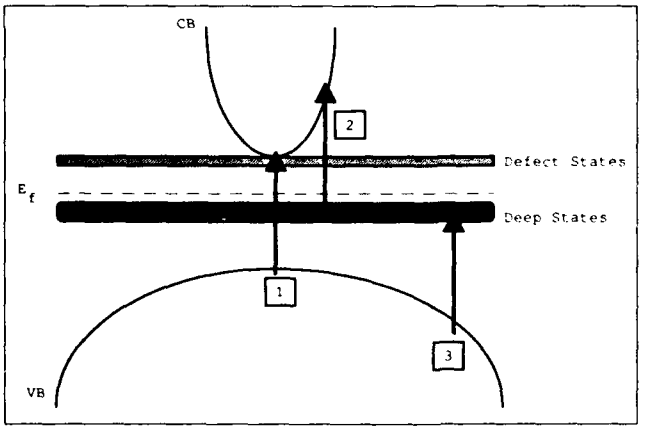

Fig. 2. Simplified band diagram of LT-MBE $In_{0.53}Ga_{0.47}As$.

mined there is a growth temperature dependent recombination time in this material, similiar to that in other LT-MBE III-V semiconductor materials. Below 250°C, the material displays induced absorption, as a result of the creation of a large density of near band edge defect states.

ACKNOWLEDGMENT

We acknowledge support from the Office of Naval Research Grant No. N00014-91-J-1488 and ARO Grant No. DAAL03-91-G-0173.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

High Resistivity LT-$In_{0.47}Ga_{0.53}P$ Grown by Gas Source Molecular Beam Epitaxy

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Low-temperature (LT) growth of $In_{0.47}Ga_{0.53}P$ was carried out in the temperature range from 200 to 260°C by gas source molecular beam epitaxy using solid Ga and In and precracked PH_3. The Hall measurements of the as-grown film showed a resistivity of ~10^6 Ω-cm at room temperature whereas the annealed film (at 600°C for 1 h) had at least three orders of magnitude higher resistivity. The Hall measurements, also, indicated activation energies of ~0.5 and 0.8 eV for the as-grown and annealed samples, respectively. Double-crystal x-ray diffraction showed that the LT-InGaP films had ~47% In composition. The angular separation, Δθ, between the GaAs substrate and the as-grown LT-InGaP film on (004) reflection was increased by 20 arc-s after annealing. In order to better understand the annealing effect, a LT-InGaP film was grown on an InGaP film grown at 480°C. While annealing did not have any effect on the HT-InGaP peak position, the LT-InGaP peak was shifted toward the HT-InGaP peak, indicating a decrease in the LT-InGaP lattice parameter. Cross-sectional transmission electron microscopy indicates the presence of phase separation in LT-InGaP films, manifested in the form of a "precipitate-like" microstructure. The analytical scanning transmission electron microscopy analysis of the LT-InGaP film revealed a group-V nonstoichiometric deviation of ~0.5 at.% P. To our knowledge, this is the first report about the growth and characterization of LT-InGaP films.

Key words: Double-crystal x-ray diffraction (DCXRD), gas source molecular beam epitaxy (GSMBE), high resistivity LT-InGaP

INTRODUCTION

GaAs epilayers grown at low temperatures (LT) of typically 200°C by molecular beam epitaxy (MBE) have recently been shown to be excellent buffer layers[1,2] for GaAs metal-semiconductor field-effect transistor (MESFET) devices and circuits. These new buffer layers are highly resistive and, therefore, provide excellent device isolation. As a result, they have been used to eliminate the backgating (or sidegating) effect which is one of the most significant parasitic problems associated with GaAs MESFETs. Since the success of LT-GaAs material, investigations have been extended not only to the LT growth of other As-based III-V compounds such as LT-AlGaAs[3] and LT-InAlAs,[4] but also to the LT growth of P-based materials such as LT-InP.[5] Recently, it has been shown that LT-GaP epilayers grown at ~200°C by gas source molecular beam epitaxy (GSMBE) also exhibit very high resistivity and thus a semi-insulating property.[6]

Two models have emerged for the explanation of the high resistivity of LT III-V materials, namely, deep levels/traps[7] and Schottky barriers.[8] In the Schottky-barrier model, the As precipitates formed after annealing were believed to virtually act as buried Schottky barriers with overlapping depletion regions in making the LT materials highly resistive. In LT-P-based epilayers, however, the mechanism for a LT epilayer to have a high resistivity cannot be explained that way. According to preliminary studies

(Received April 12, 1993)

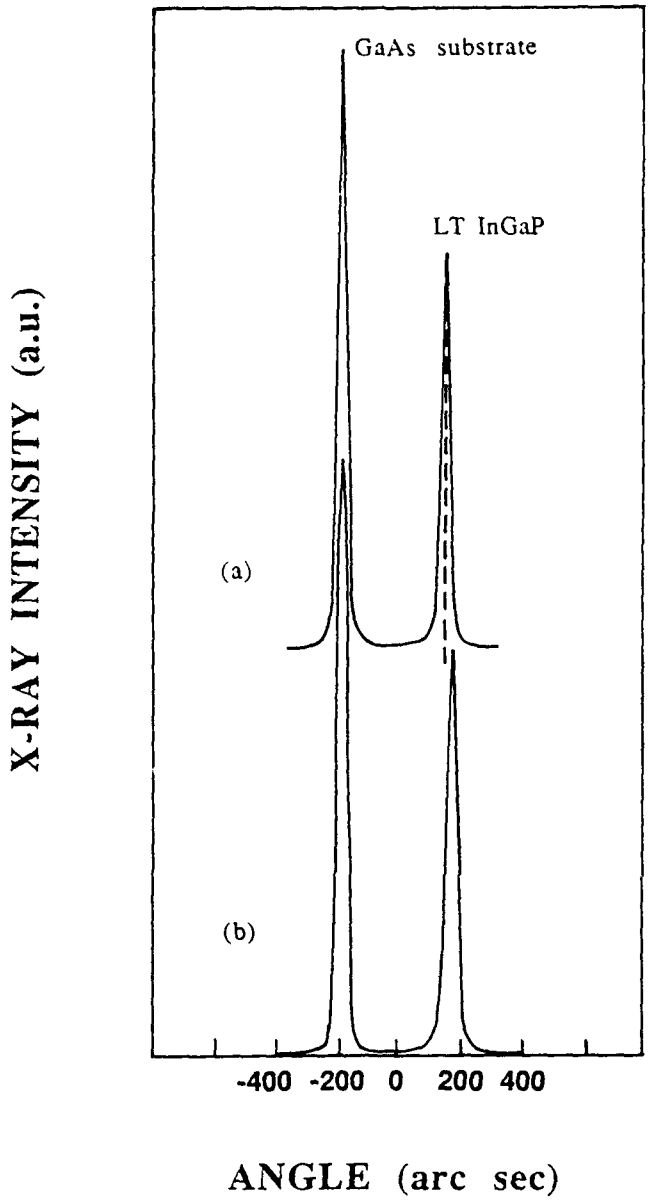

Fig. 1. Double-crystal x-ray diffraction from (400) reflection planes of the first structure described in the paper: (a) as-grown and, (b) annealed at 600°C for 1 h. The LT-InGaP peak was shifted to higher Bragg angle by 20 arc-s after annealing.

on LT-GaP,[6] annealing the LT-GaP layers at 650°C for 1 h did not result in any incoherent P-precipitates but some coherent precipitation instead. Resistivity measurements showed that as-grown LT-GaP films had high resistivity and that annealing increased it. These results implied that the high resistivity in LT-GaP was not a result of the precipitate formation and subsequent carrier-depletion near the metal-P semiconductor interfaces. The model for the explanation of high resistivity LT-GaP instead must be the excess-P-related deep levels/traps, which trap both electrons and holes. In both compensation models, group-V nonstoichiometry has been the common fundamental characteristic. Low-temperature GaAs was reported to have excess As on the order of 1 at.% as determined by Auger electron spectroscopy (AES)[7] or x-ray diffraction (XRD) analysis.[9] Recently, up to 2.2 at.% excess P from LT-GaP films grown at ~160°C by GSMBE has been revealed.[10]

Low-temperature InGaP can be extremely useful for some devices since it can be grown lattice matched to GaAs substrates and has a relatively high bandgap. However, to the best of our knowledge, little work has been done so far for this LT material. In this paper, we will report, for the first time, the growth and characterization of the LT-$In_{0.47}Ga_{0.53}P$ films.

EXPERIMENTAL CONDITIONS

All the epilayers presented in this work were grown in a Riber 32RD GSMBE system. Semi-insulating liquid encapsulated Czochralski GaAs(100) substrates were used. The substrate was degreased, etched and then mounted on a three inch molybdenum block with high purity indium solder. The substrate temperature was calibrated in advance using the oxide desorption temperature of GaAs (580°C). Before growth, the substrate was first heated to 630°C under a cracked AsH_3 flux for 10 min in order to desorb the oxide layer on the substrate surface. Elemental Ga and In sources and 100% PH_3 gas thermally decomposed at 900°C were used to grow the InGaP layers. The growth rate of all InGaP epilayers was 0.5 μm/h. The growth chamber pressure was stabilized at ~10^{-5} Torr during growth using a turbomolecular pump. The *in situ* reflection high-energy electron diffraction (RHEED) showed a streaky pattern, indicating crystalline growth of the LT-InGaP films. The samples used in this paper all had a mirror-like morphology. Double-crystal x-ray diffraction (DCXRD), cross-sectional transmission electron microscopy (XTEM), ultra-high resolution scanning transmission electron microscopy (STEM), and temperature-dependent Hall measurements were used to characterize the grown films.

RESULTS AND DISCUSSION

Double-crystal x-ray diffraction showed that the LT-InGaP films had ~47% In. For the sake of convenience, the ternary compound $In_{0.47}Ga_{0.53}P$ is hereafter simply written as InGaP unless otherwise stated. Two LT-structures were grown in this work for structural characterization of LT-InGaP films. The first structure had only a single LT-InGaP layer (200°C, 1.5 μm) grown on a GaAs buffer layer (550°C). Two Bragg peaks were observed for the DCXRD (400) reflection with the epilayer peak located at a higher Bragg angle than the substrate peak, as shown in Fig. 1a. This indicates that the LT-InGaP film is not lattice matched to the GaAs substrate and its In composition is lower than the InGaP-GaAs lattice-matched composition of ~49%. The narrow full width at half maximum (FWHM) of the epilayer peak (20 arc-s) indicates the high quality of the crystalline epilayer. Annealing this sample at 600°C for 1 h caused the angular separation between the epilayer and the substrate peaks to increase by 20 arc-s, as

seen in Fig. 1b. This observation indicates a slight reduction of the lattice parameter of the epilayer after annealing. As to the lattice relaxation as a result of annealing, this is similar to the LT-GaAs case. However, annealing LT-GaAs at 600°C for ~10 min results in a complete removal of the lattice mismatch while annealing LT-InGaP at the same temperature for 1 h results in only slight relaxation of the expanded lattice. This is manifested by a small peak shift of the annealed film to a higher Bragg angle. In order to compare the structural properties of the LT-InGaP and the InGaP epilayers grown at higher temperatures (~480°C, hereafter referred to as HT-InGaP), a second structure was grown, as shown in Fig. 2. During the growth of both HT and LT-InGaP epilayers, a fixed PH_3 flow rate of ~4 sccm was maintained. It should be noted that there was an interruption of the PH_3 flow into the growth chamber after the HT growth was ended and the substrate temperature was lowered to ~300°C. The In compositions of the LT and HT-InGaP epilayers were assumed to be identical by maintaining the same source temperatures during the layers' growth. Double-crystal x-ray diffraction analyses from (400) reflection planes were performed on both the as-grown and annealed samples. For the as-grown samples, three (400) Bragg peaks were observed: the substrate, LT-InGaP and HT-InGaP peaks, respectively, as shown in Fig. 3a. Upon annealing at 600°C for 1 h, the LT peak was found to be the only one shifted, as shown in Fig. 3b. The observation that the annealing did not have any effect on the HT peak position was as expected. The angular separation between the LT and HT-InGaP reflections was 70 arc-s before annealing and 50 arc-s after annealing. Therefore, the angular shift of the LT peak toward the HT peak after annealing was 20 arc-s, which was in good agreement with that of the first grown structure previously discussed. This relative shift, corresponding to the incomplete removal of the lattice-mismatch by 0.01%, might be caused by redistribution of the excess P atoms in the epilayer lattice due to the annealing. The nature of the redistribution is not yet known at this time. Considering the HT-InGaP as a "substrate," the LT-InGaP/HT-InGaP structure was found to have DCXRD characteristics similar to those of LT-GaP/GaP.[6] The fact that the LT peak was situated on the left side of the HT peak confirmed that the LT-InGaP had a slightly larger lattice parameter than that of the HT-InGaP (by 0.05% for the as-grown LT epilayer). This lattice expansion can be explained by the presence of the excess P atoms incorporated into the epilayer due to the nonstoichiometric growth. Both analytical scanning transmission electron microscopy (STEM) and DCXRD approaches revealed that the LT-InGaP had ~0.5 at.% more P atoms than the HT-InGaP. The details of this determination will be published elsewhere.[11]

LT InGaP	200°C	1 μm
HT InGaP	480°C	1 μm
GaAs buffer	550°C	1 μm
SI LEC GaAs (100) substrate		

Fig. 2. Schematic of the multilayer sample with the LT-InGaP film (T_s = 200 C) grown on top of the HT-InGaP film (T_s = 480 C).

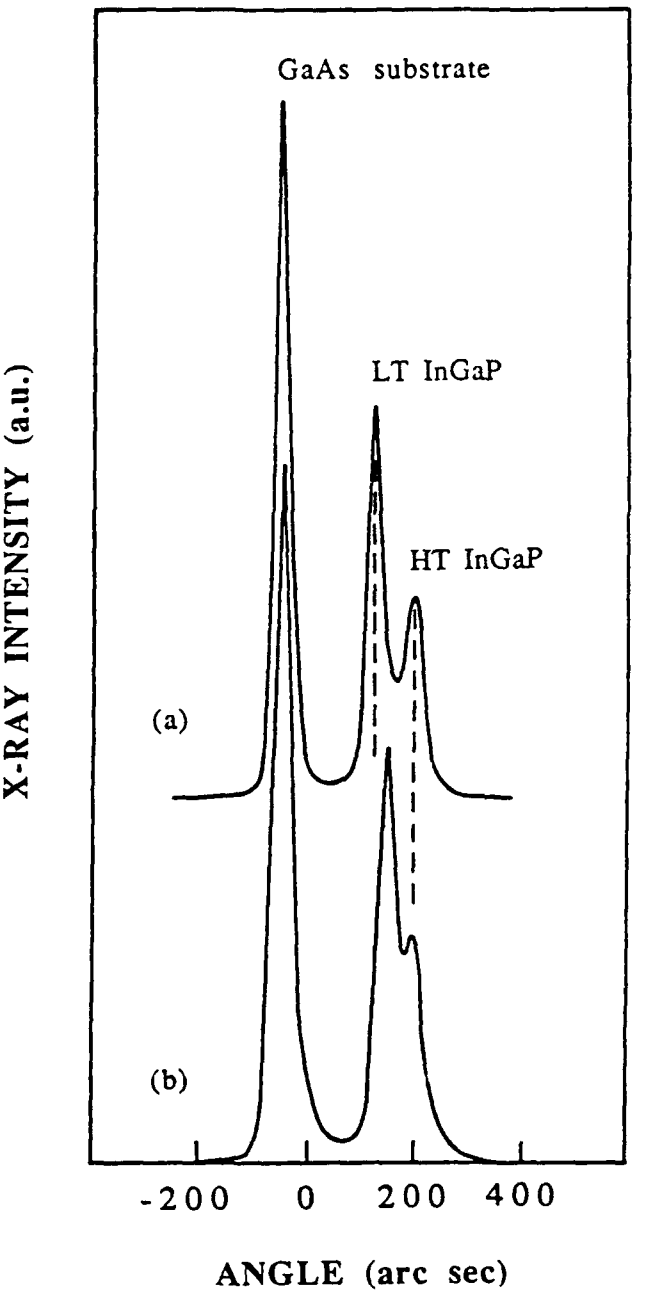

Fig. 3. Double-crystal x-ray diffraction from (400) reflection planes of the sample shown in Fig. 2: (a) as-grown, the angular separation between the LT-InGaP and the HT-InGaP reflections is 70 arc-s; (b) annealed at 600 C for 1 h, the angular separation between the LT-InGaP and the HT-InGaP reflections is 50 arc-s.

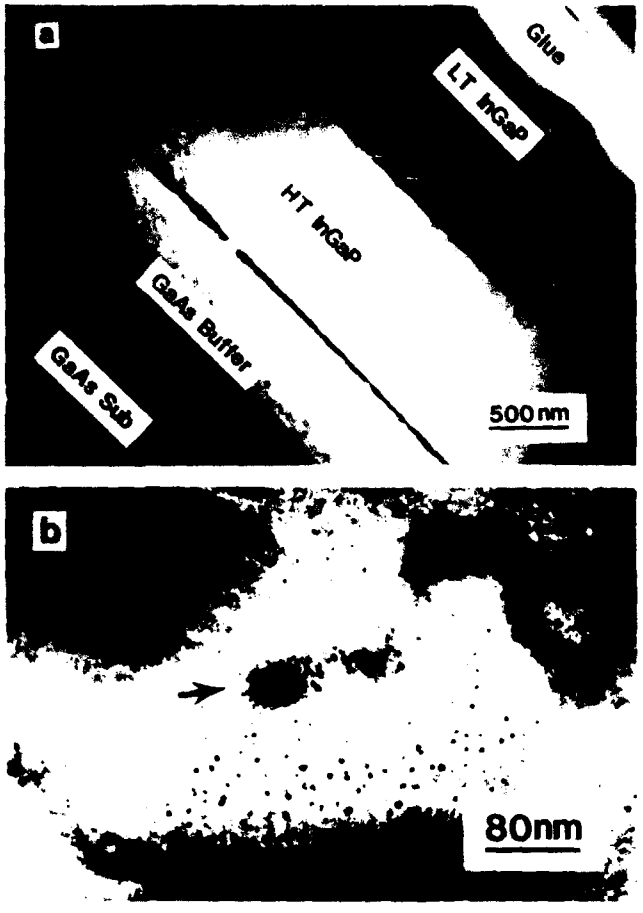

Fig. 4. Cross-sectional transmission electron micrographs obtained from the multilayer sample shown in Fig. 2 illustrate: (a) the layer structures and the phase separation, manifested in the form of a "precipitate-like" microstructure, in the as-grown LT-InGaP layer, and (b) the moiré fringe in one of the phase separated areas, as indicated by the arrow, after annealing the LT layer (600° C,1h).

An XTEM micrograph (Fig. 4a) from the second structure indicates the presence of phase separation in LT-InGaP epilayers. This is manifested in the form of a "precipitate-like" microstructure. The precipitate-like phase separation (~800Å in diameter for the layer grown at ~200°C) appears to decrease in volume as the growth temperature increases. Annealing, however, seems to have a slight influence on the phase separated microstructure. The phase separated areas were crystalline and strained as implied by the moiré fringes shown in Fig. 4b. Analytical STEM analyses indicated that the phase separated areas in the LT-InGaP layer had a slightly higher In composition than the LT matrix. The HT-InGaP showed a distinctive feature of slight decomposition. Both the phase separation in the LT-InGaP layer and the slight decomposition in the HT-InGaP layer might be explained by the spinodal decomposition usually observed in growth by liquid phase epitaxy (LPE) and metalorganic chemical vapor deposition (MOCVD). Spinodal decomposition causes the appearance of a two-phase microstructure with different In compositions at the growth temperature.

The resistivity of a LT material serves as a practical

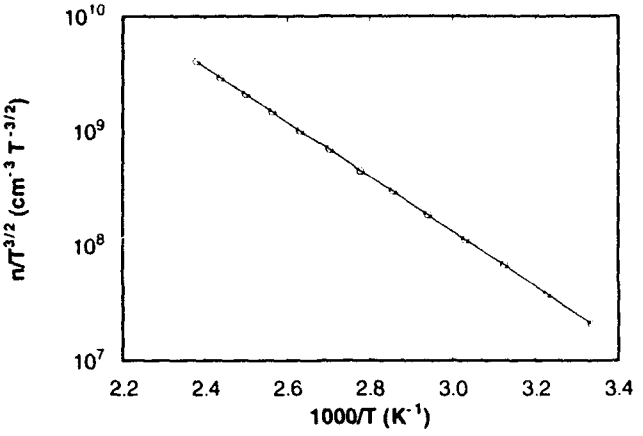

Fig. 5. Plot of $n/T^{3/2}$ vs 1000/T for the as-grown LT-InGaP film.

monitor for its device applications To measure the resistivity of LT-InGaP more accurately, a special structure was designed. A 2 μm thick LT-InGaP film was grown at ~200°C on a 500Å thick AlAs layer grown at 610°C. Epi-lift off technique was used to remove the LT-InGaP film by etching off the AlAs layer in hydroflouric acid. The temperature-dependent resistivity and Hall effect measurements on the as-grown LT-InGaP film revealed n-type conduction with a resistivity of 9×10^5 Ω-cm and mobility of 120 cm^2/V s at 296K. To determine the activation energy of the dominant donor,[12] we plotted $n/T^{3/2}$ vs T^{-1}, as shown in Fig. 5. The slope of this plot, which is just $-E_{D0}/k$, leads to E_{D0} = 0.48 eV, within error of what might be expected for the (0/+) transition of the P antisite in $In_{0.5}Ga_{0.5}P$. After annealing the LT film at 600°C for 1 h, the 296K resistivity increased to 10^9 Ω-cm but a Hall voltage could no longer be found. Nevertheless, a plot of lnρ vs T^{-1}, where ρ is the resistivity, produced an even larger activation energy, 0.8 eV. Thus, the material is stable against high conductivity conversion. It is necessary to point out that the LT-InGaP remains semi-insulating before and after annealing.

CONCLUSIONS

In conclusion, we have successfully grown $In_{0.47}Ga_{0.53}P$ at a low temperature of ~200°C for the first time. The LT-InGaP showed a lattice expansion of 0.05%, as determined by DCXRD relative to the HT-InGaP grown at 480°C with presumably the same In composition. The lattice expansion can be explained by the excess P atoms of ~0.5 at.% present in the LT layer with respect to the HT layer. The lattice parameter of the LT-InGaP did not return to that of the HT-InGaP after annealing at 600°C for 1 h. However, a slight reduction of the lattice expansion by 0.01% did occur after annealing, the possible explanation of which may be the redistribution of the excess P atoms. Cross-sectional transmission electron microscopy showed no formation of P-precipitates after annealing, but showed phase separation in the as-grown LT-InGaP epilayer, manifested in the form of a "precipitate-like" microstructure. This

precipitate-like phase separation can be explained by the tendency of the InGaP alloys to spinodally decompose at similar compositions that are close to the InGaP-GaAs lattice-match composition. The HT-InGaP layer indicated the occurrence of slight spinodal decomposition at the growth temperature. Further structural investigation of the phase separation is currently underway. The temperature-dependent Hall measurements performed on the LT-InGaP film after the substrate was removed showed that the as-grown LT film had a resistivity of ~10^6 Ω-cm at 296K whereas the annealed LT film exhibited at least three orders of magnitude higher resistivity. Activation energies of ~0.5 and 0.8 eV were also obtained from the Hall measurements for the as-grown and annealed LT films, respectively. As with LT-GaP,[6] annealing is not required for the LT-InGaP films to be semi-insulating.

ACKNOWLEDGMENT

This work was supported by URI funded through the U.S. Office of Naval Research. D.C. Look was supported by the U.S. Air Force Contract F33615-91-C-1765 and his work was carried out at the Solid State Electronics Directorate, Wright Laboratory, Wright-Patterson Air Force Base, OH.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Electronic Properties of Low-Temperature InP

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We have investigated InP layers grown by low-temperature (LT) gas source molecular beam epitaxy. Using high-pressure Hall effect measurements, we have found that the electronic transport in the LT epilayers is determined by the presence of the dominant deep donor level which is resonant with the conduction band (CB) located 120 meV above the CB minimum (E_{CB}). We find that its pressure derivative is 105 meV/GPa. This large pressure derivative reveals the highly localized character of the donor which via auto-ionization gives rise to the high free electron concentration n. From the deep level transient spectroscopy and Hall effect measurements, we find two other deep levels in the band gap at $E_{CB} - 0.23$ eV and $E_{CB} - 0.53$ eV. We assign the two levels at $E_{CB} + 0.12$ eV and $E_{CB} - 0.23$ eV to the first and second ionization stages of the phosphorus antisite defect.

Key words: LT InP, phosphorus antisite, pressure

INTRODUCTION

Thin films of III-V compounds grown under low-temperature (LT) conditions have recently been a subject of intense studies.[1,2] It has been found that lowering of the growth temperature leads to the high nonstochiometry of the LT epilayers.[2] In the case of LT InP, it was found that the LT epilayers were highly conductive.[3-7] Very recently, we have undertaken detailed studies of the electronic properties in the LT InP and some preliminary results have been published in Ref. 9. In the undoped epilayers grown in the temperature range from 130 to 500°C, the free-electron concentration (n) was very weakly temperature dependent. At low growth temperatures (T_g) below 350°C, metallic-like electrical transport indicated that the electrons formed a degenerate gas in the conduction band (CB). For samples grown at $T_g \leq 265$°C, n saturated at 4×10^{18} cm^{-3}. The dramatic increase of the n with decreasing T_g suggested a growth-temperature-dependent incorporation of native donor-like defects. The pressure-induced disappearance of free carrier absorption, indicated that there existed a deep donor level, resonant with the conduction band at p = 0, which with increasing pressure moved down with respect to the CB minimum and captured free electrons. The energy of the donor level was estimated to be 0.11 ± 0.02 eV above the bottom of the conduction band (E_{CB}). From the analysis of the electronic transport in LT InP epilayers grown at 310°C and doped with Be acceptors, it has been demonstrated that there exists another deep level in the band gap. The thermal ionization energy of this level was determined to be $E_{CB} - 220$ meV. Based on the results of the optically detected magnetic resonance (ODMR) and photoluminescence (PL) experiments, those two lev-

(Received April 12, 1993)

els (E_{CB} + 0.11 eV and E_{CB} − 0.22eV) have been tentatively assigned to the first ($P_{In}^{(0/+)}$) and second ($P_{In}^{(+/++)}$) ionization stages of the phosphorus antisite defect.[8,9]

In this paper, we report on our results obtained from Hall effect measurements performed under high hydrostatic pressure up to 1.5 GPa. Our studies give a direct experimental evidence for the presence of the deep level resonant with the CB. We analyse how the presence of the P_{In} defects influences electronic transport in LT InP. We determine the energetic position of the P_{In} (0/+) level and its pressure derivative. Moreover, using deep level transient spectroscopy (DLTS) experiments, we find the activation energies of the electron emission process for two electron traps with levels in the band gap to be 0.25 and 0.53 eV. Referring to the results of ODMR and PL measurements, we assign the activation energy of 0.25 eV to the $P_{In}^{(+/++)}$ level. We emphasize that due to the electronic structure of the dominant P_{In} defect, phosphorus-rich InP cannot be semi-insulating.

We studied InP samples grown by gas-source molecular beam epitaxy on semi-insulating and p^+ InP substrates. The growth technique has been described elsewhere.[6,7] The Hall effect experiments were done on two LT-InP 1 μm thick epilayers grown at 265°C (sample 1, doped with Be) and 310°C (sample 2, nominally undoped). A high-pressure low-temperature cell UNIPRESS GLC10, with helium as a pressure transmitting medium, enabled the measurement of conductivity, magnetoresistance, and Hall effect of the investigated samples (with indium contacts in a van der Pauw geometry) at T = 77K and T = 300K as a function of applied hydrostatic pressure up to 1.5 GPa and magnetic field up to 1.2 Tesla. Deep-level transient spectroscopy measurements were done using a deep-level spectrometer from SULA Technologies on the p^+n junctions fabricated by growth of an LT-InP epilayer (T_g = 310°C, n = 1 × 10^{17} cm^{-3}) on the p^+ InP substrate doped with 2 × 10^{18} cm^{-3} of shallow Be acceptors.

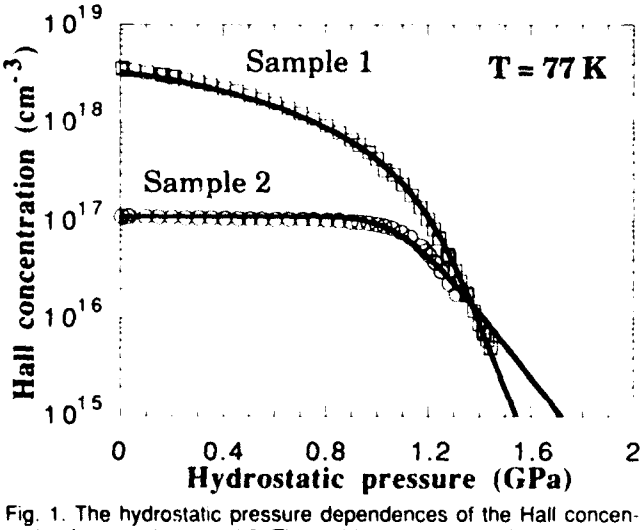

Fig. 1. The hydrostatic pressure dependences of the Hall concentration for samples 1 and 2. The solid lines were fitted to the experimental data in order to determine the $P_{In}^{(0/+)}$ level energy and its pressure shift; see text.

RESULTS AND DISCUSSION

First, we discuss how hydrostatic pressure influences the electrical transport in the LT InP. The isothermal (T = 77K) pressure dependences of the free electron concentration in the investigated LT InP epilayers are presented in Fig. 1. We would like to point out the following.

- For the sample 1 (T_g = 265°C), the free electron concentration at ambient pressure is n = 3.6 × 10^{18} cm^{-3} and then dramatically decreases with increasing pressure (p) by four orders of magnitude in the pressure range between 0 to 1.5 GPa. The pressure-induced rapid decrease of n can be clearly observed even at low and moderate pressures (p< 1 GPa).
- In the case of sample 2 (T_g = 310°C) n remains practically constant at 1.1 × 10^{17} cm^{-3} up to 1 GPa subsequently followed by a rapid freeze-out of electrons at higher pressures.

These results can only be explained assuming a presence of a deep donor level resonant with the CB at p = 0, which via an auto-ionization process provides free electrons to the CB. The applied pressure strongly influences the energetic position of the level (ε) with respect to the CB edge, and as a consequence, it modifies the thermal equilibrium between the level and the CB. With increasing pressure, the donor level moves down in energy with respect to the CB minimum and captures the free electrons, leading to the change of its charge state as well as a decrease of n. However, the situation is significantly different in the samples 1 and 2. In the case of sample 1, the Fermi energy E_F is very close to the energetic position of the deep level even at p = 0 and therefore due to the pinning of E_F at the donor level E_F simply follows its pressure-dependent ionization energy. On the other hand, in sample 2 grown at higher temperature, the concentration of the donor defects is substantially lower compared to that of sample 1. Thus, at p = 0, the donor level is completely ionized and the Fermi level is located well below this defect level. Therefore, the equilibrium population of the level remains unchanged up to 1 GPa. Further increase of pressure leads to the onset of Fermi-level pinning at this defect level when it enters the InP band gap.

In order to characterize this effect more quantitatively as well as determine the thermal ionization energy ε of the donor level and its pressure shift, we applied the following numerical analysis. We assumed that the donor level, $D^{(0/+)}$, was in thermal equilibrium with the CB and the degeneracy factor of the level was 1. Taking into account the charge neutrality equation: $n + N_A = N_{D^+}$ (where N_A stands for the acceptor concentration) and calculating the Fermi integral to get the free electron concentration, we were able to model n(p) dependences which could be then compared with the experimental data from Fig. 1. To get the best agreement, we fit two parameters,

$\varepsilon^{0/+}(p = 0)$ and $\delta\varepsilon^{0/+}/\delta p$, common for both samples, and additionally, N_A, for sample 1 only (which was doped with Be). The donor concentration N_D was taken equal to the $n(p = 0)$ values for both samples. The solid lines in Fig. 1, describing very well the experimental data for both samples, represent the result of the best fit obtained for: $\varepsilon^{0/+}(p = 0) = 120$ meV, $\delta\varepsilon^{0/+}/\delta p = 105$ meV/GPa, and $N_A = 5 \times 10^{17}$ cm^{-3}. The thermal ionization energy of 120 meV agrees perfectly with the Fermi level position ($E_F = E_{CB} + 120$ meV) derived from the upper saturation limit of the free electron concentration $n = 4 \times 10^{18}$ cm^{-3} found for all the LT epilayers grown at $T_g < 265$°C[9] and in other studies of phosphorus-rich LT InP.[4,6,7] A similar Fermi level pinning was observed in the surface layer of bulk InP annealed under P overpressure.[10] This finding implies that the higher the deviation from InP stochiometry, the higher the incorporation of the defects responsible for the increase of the electron concentration. Nevertheless, the Fermi energy cannot be higher than the energy position of the deep level at E_{CB} +0.12 eV which determines the saturation limit $n = 4 \times 10^{18}$ cm^{-3}. Another important finding is the large pressure derivative of the $D^{(0/+)}$, 105 meV/GPa, which can be compared with the pressure shift of the InP band gap energy of 84 meV/GPa.[11] This strong pressure dependence is characteristic for the states formed by deep defects (like transition metal ions)[12] reflecting pinning of their energy to the pressure-independent neutrality level. The large pressure derivative of the $D^{(0/+)}$ reveals that the wave function of the donor is indeed highly localized.

Although the E_{CB} + 0.12 eV defect level controls the electrical properties of LT InP, there is still an open question as to whether there are other levels associated with the same defect. From the Hall effect measurements, it has been shown recently that a defect level with thermal ionization energy of 0.22eV exists in this material.[9] To verify if this defect level can be detected using other experimental techiques, we have performed DLTS measurements on p$^+$n junctions. A typical DLTS spectrum demonstrating the presence of two electron traps in the LT-InP is shown in the insert to Fig. 2. From the Arrhenius plot (see Fig. 2), we determined the activation energies of the emission rate (E_e) to be 0.25 and 0.53 eV. No other levels shallower than 0.25 eV have been detected.

We would like to stress that most likely the thermal ionization energy E_T = 220 meV (Hall effect) and activation energy of the emission process E_e = 250 meV (DLTS) are due to the same defect. It has been shown from ODMR, PL, and excitation of ODMR signal measurements[8,9,13] that the second ionization stage of the isolated phosphorus antisite defect, $P_{In}^{(+/++)}$, is located in the upper half of the band gap at energy $E < E_{CB} - (0.3 \pm 0.1)$ eV. Therefore we assign the E_{CB} – 220 meV level to the $P_{In}^{(+/++)}$ level. Since no other energetically shallower deep levels have been found in the band gap either using Hall or DLTS measurements, the most natural identification of the deep level resonant with the conduction band at E_{CB} + 0.12 eV is that this is indeed the first ionization stage ($P_{In}^{(0/+)}$) of the phosphorus antisite double donor.

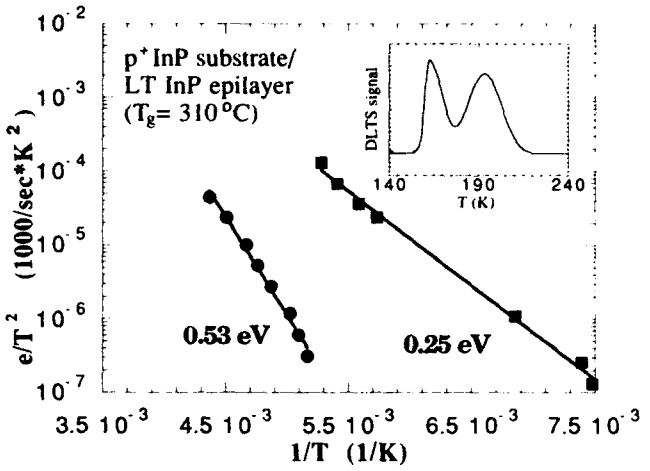

Fig. 2. The Arrhenius plots corresponding to the DLTS spectrum presented in insert. The activation energies of the emission process for the two electron traps were found to be 0.25 and 0.53 eV.

We would like to emphasize that the energetics of the P_{In} donor defect have some technologically important consequences. Clearly, due to the effect of autoionization of the $P_{In}^{(0/+)}$ level, as-grown nonstochiometric P-rich InP cannot be employed to produce semi-insulating material as it has been claimed up to now.[10,14,15]

CONCLUSION

In summary, by high-pressure Hall effect and DLTS measurements, we have demonstrated that the electronic transport of the P-rich LT InP epilayers are determined by the presence of the phosphorus antisite donor defects which are responsible for the conductive character of this material. We have studied the energetics of the P_{In} defect and its pressure dependence.

ACKNOWLEDGMENT

This work was supported by the U.S. Air Force Office of Scientific Research under grant AFOSR-88-0162 and by the Director, Office of Energy Research, Office of Basic Energy Research, Materials Science Division, of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

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Optically Detected Magnetic Resonance Studies of Low-Temperature InP

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We present experimental results from studies of low-temperature molecular beam epitaxially grown InP (LT InP), by optical detection of magnetic resonance (ODMR), where both the identification of defects and recombination processes can be studied simultaneously. The presence of the P_{In} antisites is unambiguously established, evident from the doublet hyperfine structure from the ^{31}P atom (with nuclear spin I = 1/2 and 100% natural abundance). The P_{In} antisites are shown to be involved in strong nonradiative recombination processes, which compete with radiative ones via other defects. In addition to the P_{In} antisites, another defect has been detected in ODMR experiments which is shown to be a low-symmetry defect, likely a complex related to Be. Photo-excitation of the ODMR signals allows determination of the energy level positions of these defects. The results indicate that the P_{In} antisite is the prevailing defect governing the electronic properties of the material.

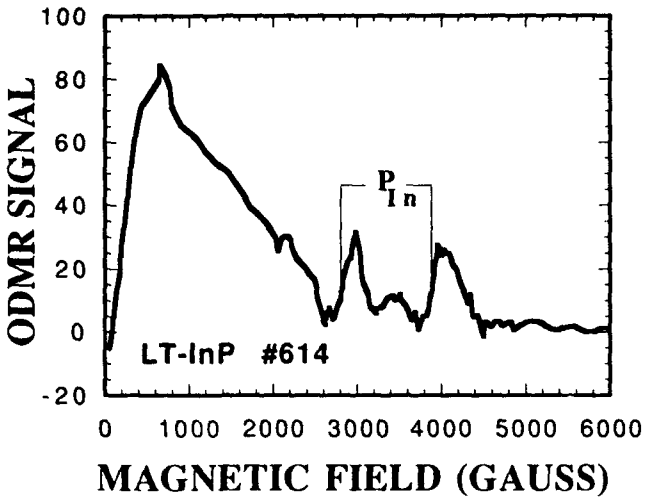
Key words: LT InP, optically detected magnetic resonance (ODMR), phosphorus antisite

INTRODUCTION

Off-stoichiometric growth of compound semiconductors has recently attracted increasing attention, due to the unique properties of these materials. GaAs and related ternary III-V compounds grown by molecular beam epitaxy (MBE) at low temperatures exhibit extremely high resistivity (semi-insulating), ultrashort carrier lifetime, and reasonably high mobility, which find potential applications; e.g., as buffer layers, as ultrafast photodetectors and switches.[1] In low-temperature (LT) GaAs, it is generally agreed that the excess As incorporated in the materials[2,3] is responsible for the above-mentioned unique properties, though the detailed mechanism of compensation and recombination is still in debate.[4,5]

Unexpectedly, LT InP epilayers have been shown to be intrinsically n-type conductive, unable to be compensated by doping with shallow acceptors.[6-8] The mechanism responsible for this is unknown, despite many speculations for the dominant presence of P_{In} antisites inspired by the results from LT GaAs. The conventional EPR technique, which has successfully detected as high as a few times of 10^{18} cm^{-3} of As_{Ga}^{+} antisites in as-grown LT GaAs,[3] was unable to detect any defects in LT InP,[9] however, due to the presence of a strong Fe-acceptor EPR signal from the InP:Fe substrate and lower defect concentrations in the 1 μm thick LT InP thin films. A combination of sensitive (as well as spectrally selective) optical spectroscopy and the microscopicly informative magnetic resonance techniques, such as the optically detected magnetic

(Received April 12, 1993)



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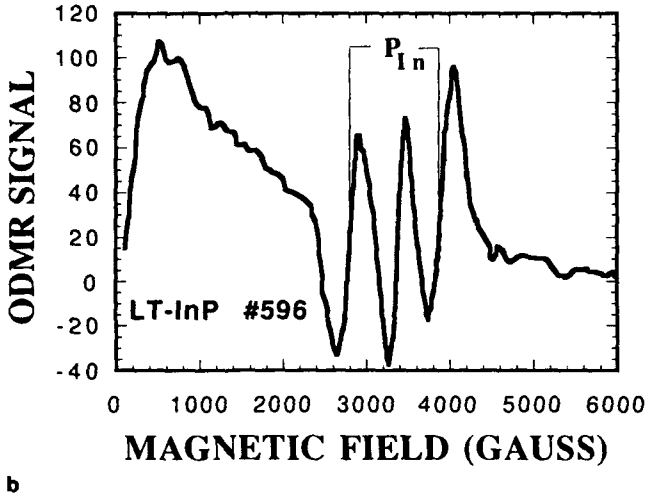

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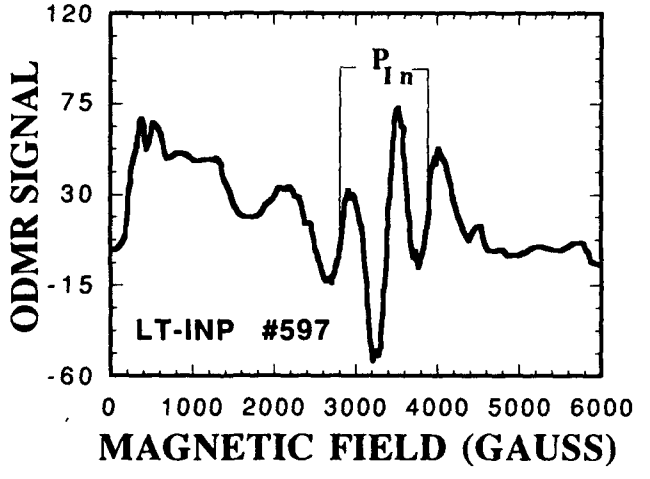

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Fig. 1. Optically detected magnetic resonance spectra from Be-doped LT InP grown at 300°C (#614) and at 310°C (#596 and #597), with increasing Be-doping level from sample #614 to #597.

resonance (ODMR) technique,[10] has been shown to be very sensitive (generally a few orders of magnitude higher compared to EPR). It is superior especially in studies of defects in semiconducting thin films and heterostructures.

In this work, we attempt to employ the ODMR technique to gain a better understanding of the physical properties of LT InP. The primary goal is to identify defects present in the material, in particular those governing the electronic properties. Carrier capture and recombination processes are studied, where the role of defects is examined. Photo-excitation by a tunable laser is employed to reveal the energy level positions of the electronic transitions via the defects.

EXPERIMENTAL

The samples used in this work were grown on (001) semi-insulating InP:Fe substrates by gas-source MBE at temperatures ranging from 130°C to 500°C. They were either undoped or Be-doped. Transmission electron microscopy (TEM) studies indicated a good single crystalline quality for LT InP thin films grown above 200°C. Detailed information on the sample growth and preparation can be found elsewhere.[6] Optically detected magnetic resonance experiments were performed with a modified Bruker 200D X-band ESR spectrometer, with a window on the microwave cavity wall for optical access. An Ar^+ laser (514.5 nm line) was used as the excitation source. In optical excitation experiments, a tunable Ti:Sapphire laser was used, with a rather low optical excitation level (<0.5 W/cm^2) to avoid a possible sample heating and saturation of recombination processes and to minimize the two-step excitation processes. The photoluminescence (PL) emissions from the samples were detected by a cooled Ge detector. The ODMR signal was detected by a lock-in technique, in phase with the modulated magnetic field or the modulated microwave field. An Instruments SA 1/4 m monochromator was employed in the PL experiments and the spectral dependence study of the ODMR signals.

RESULTS AND DISCUSSION

In Fig. 1a–1c, we show the ODMR spectra obtained from the samples grown at 310°C with varying Be-doping levels. They consist of three ODMR lines. Evidently, from the relative change in the intensity of these ODMR lines in samples of different Be-doping level, these three ODMR lines can be decomposed into two parts: a doublet (outer lines) and a singlet, arising from two different defect centers. These ODMR signals were only observed in samples grown at a temperature lower than 350°C and with Be-doping. They correspond to a decrease by up to 1–2% in the 0.8 eV PL band upon the ODMR transition.

In order to reveal the symmetry of the two defects detected in ODMR, we have carried out an angular dependence study of the ODMR signals by rotating the magnetic field with respect to the crystallographic orientation of the samples. The ODMR doublet is shown to be isotropic, reflecting a T_d symmetry for the corresponding defect. The middle ODMR line shows a slight anisotropy, on the other hand, indicating a low

symmetry for the defect (denoted as A below). The correlation between the ODMR intensity and the Be-doping level suggests that the A defect may be Be-related, possibly in the form of a complex.

The ODMR doublet is centered around g = 2, and is a fingerprint of the magnetic resonance from an unpaired electronic spin S = 1/2 of a defect with a nuclear spin I = 1/2 of 100% natural abundance. Based on the rather strong electron-nuclear interaction which gives rise to the large central hyperfine splitting observed in the ODMR experiments, reflecting an A_1 symmetry for the electronic wavefunction, the most plausible candidate for the defect is the P_{In} antisite in its singly positive charge state (P_{In}^+). In fact such a magnetic resonance signal has been observed earlier in bulk InP, both by EPR[11] and ODMR,[12,13] and was argued to be due to the P_{In} antisite. Analysis of the experimental data by a spin Hamiltonian

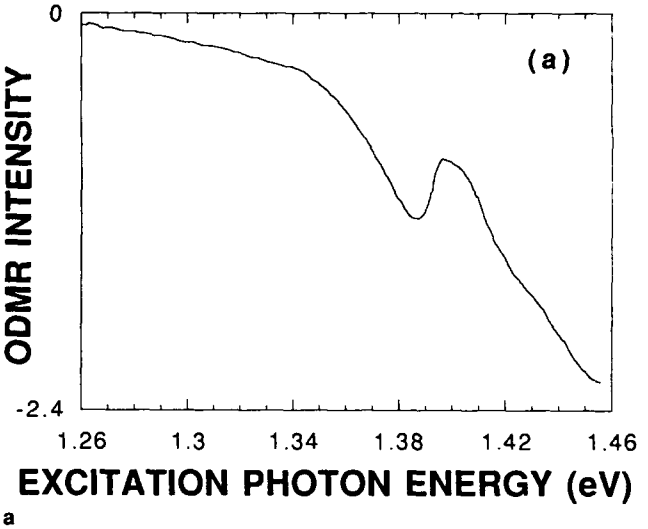
$$H = \mu_B S \bullet g \bullet B + S \bullet A \bullet I \qquad (1)$$

results in the best-fit parameters: g = 2.003 and A = 98×10^{-4} cm^{-1}. [The first term in Eq. (1) represents the electronic Zeeman interaction, and the second, the central hyperfine interaction, where μ_B is the Bohr magneton.] These spin Hamiltonian parameteers obtained are in a good agreement with those obtained previously for the isolated P_{In} antisite.[11-13]

It is important to note that the P_{In} antisite ODMR signal could only be observed in the samples grown at a temperature lower than 350°C, though a similar 0.8-eV PL band could be detected in those samples grown at or higher than 350°C. This observation shows that the 0.8-eV PL band is not directly related to the P_{In} antisite. Instead, a competing process is involved between the radiative recombination process detected in PL (i.e., the 0.8 eV PL band) and the nonradiative (or radiative beyond the spectral range of the Ge-detector) recombination process connected to the P_{In} antisite. A microwave induced transition enhances the recombination process via the P_{In} antisite, and thus decreases the 0.8 eV radiative recombination. Such a competing process is illustrated in Fig. 2, where the electrons from the P_{In} antisite and another deep level defect of unknown origin compete in recombining with holes bound at the common acceptor (A defect) of the donor-acceptor transitions.

The fact that the P_{In} antisite ODMR signal could be observed in the sample grown at 310°C but not in the sample grown at 350°C, though the 0.8 eV PL band was observed in similar intensity from both samples, strongly suggests an increasing concentration of the P_{In} antisite with decreasing growth temperature. The correlation between the ODMR signal and the free carrier concentration,[6-8] which increases by an order of magnitude from the sample grown at 350°C to the one grown at 310°C, indicates the P_{In} antisite to be the likely candidate responsible for the electrical properties of the material. This is further confirmed by the electronic structure of the P_{In} antisite as determined by photo-excitation spectra of the ODMR signals, which shows that the auto-ionization of the P_{In} antisite due to the (0/+) level at $E_c + 0.12$ eV[7,8] results in a high concentration of free electrons present in LT InP (to be discussed in more details below). In these experiments, the individual ODMR line and thus the corresponding defect were monitored while the optical excitation photon energy was varied by a tunable laser. The onset of the band-to-defect level transition measures the energy level position of the defect monitored.

In Fig. 2a, we show such an excitation spectrum obtained from the Be-doped sample grown at 310°C, by monitoring the ODMR signal shown in Fig. 1b. Similar spectra were obtained for the ODMR doublet and singlet. Besides the excitation of the InP across the band gap, there are two other resonant transitions which enhance the ODMR signals (corresponding to a further decrease in the intensity of the 0.8 eV PL band) related to the P_{In} antisite and the A defect. One of them is estimated to be at about 1.25 eV (the onset is not shown in the figure but was obtained by using another mirror set of the Ti:Sapphire laser), and the other at 1.34 eV. (The true onset for the 1.25 eV excitation could not be determined accurately due



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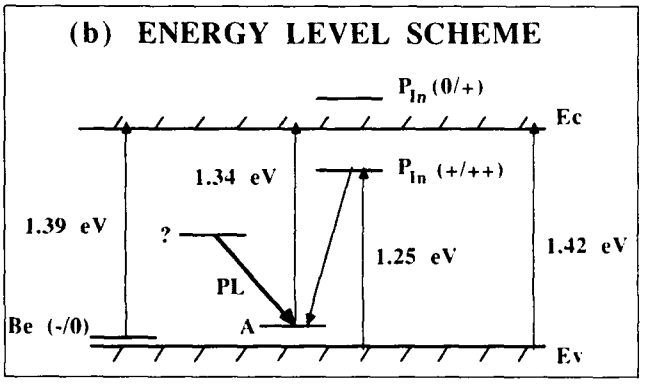

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Fig. 2. (a) Excitation spectrum of the P_{In} antisite ODMR signal from the Be-doped LT InP grown at 310°C, as shown in Fig. 1b. (b) Energy level scheme of the defects and related excitation and recombination processes.

to the very weak ODMR signal, and a more careful study is now in progress.) These two transitions correspond to the excitation between the bandedge and the defect level of the two defects involved in the ODMR, as shown in Fig. 2b. This is consistent with the energy level position $E_c - 0.23$ eV for the (+/++) transition level of the P_{In} antisite obtained from recent electrical measurements.[7,8] The decrease in the ODMR signal at 1.39 eV (see Fig. 2a) is suggested to be due to the transition from the Be-acceptor to the conduction band, which reduces the number of photons available for the excitation processes, which enhance the ODMR signal (e.g., 1.25 and 1.34 eV excitation processes). Such a competing process can be quite significant due to the fact that the concentration of the Be-acceptors is high and that a similar acceptor-to-conduction-band excitation process is involved for both 1.34 and 1.39 eV transitions.

CONCLUSION

It should be pointed out that there is no indication from the excitation spectra that the energy level (0/+) of the P_{In} antisite is within the band gap. This is consistent with the fact that we have not been successful in detecting such a deep donor level above the (+/++) level of the P_{In} antisite from electrical measurements. This level is thus expected to be resonant with the conduction band. In fact, it has been shown that there exists a deep donor level at $E_c + 0.12$ eV from Hall measurements and far-infrared free carrier absorption under hydrostatic pressure.[7,8] The autoionization (the first ionization stage) of the P_{In} antisite is, therefore, responsible for the n-type conductivity of the LT InP.

ACKNOWLEDGMENT

This work was supported by the U.S. Air Force Office of Scientific Research under grant AFOSR-88-0162 and by the Director, Office of Energy Research, Office of Basic Energy Research, Materials Science Division, of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Ordering in InGaAs/InAlAs Layers

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The structure of InGaAs/InAlAs layers lattice matched to an InP substrate, grown on either (100) or on (110) with a 4° tilt toward [11$\bar{1}$] at 500 and 300°C has been investigated by transmission electron microscopy. High perfection resulted for the layers grown on [001] oriented substrates whereas growth on the near [110] substrates resulted in compositional nonuniformities, macrosteps formation, and ordering of the group III elements. This difference in structural perfection between the two sets of samples was also reflected in differences in electrical properties.

Key words: LT InGaAs, LT InAlAs, ordering, transmission electron microscopy

INTRODUCTION

$Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ lattice-matched to InP are widely used for a variety of electronic devices. The electrical and optical properties of grown layers are strongly influenced by defects, compositional variations, and ordering. Electrical and optical properties in ternary semiconductor compound such as $GaAs_xSb_{1-x}$,[1,3] $Ga_xIn_{1-x}P$,[4,6] and $GaxIn_{1-x}As$[5,7] have been investigated during last decade. A two-dimensional electron gas (2DEG) mobility enhancement in the <110> directions was found in InGaAs channel layer due to ordering.[7] Ordering of CuAu-type (on {110} planes) and CuPt-type (on {111} planes) was observed in this system, and it was shown that neither short range nor long range order was influenced by elastic stress but rather was mainly determined by processes taking place on the growing surface.[1,7] Thus, the surface structure and surface growth steps definitely play an important role in the process of ordering.

(Received April 12, 1993)

In many of ternary and quaternary semiconductor alloys, a miscibility gap occurs giving rise to variations in layer composition.[9] The goal of this paper was to study the influence of different growth parameters of InGaAs/InAlAs layers on their structure and electrical properties.

EXPERIMENTAL

InGaAs/InAlAs layers lattice matched to InP have been grown at 500 and 300°C on (100) and on (110) tilted 4° toward [11$\bar{1}$]. Tilting toward [11$\bar{1}$] resulted in exposure of group III elements on the geometrically required surface steps. The growth conditions and the results of Hall measurements are shown in Table I. Three different beam equivalent pressure ratios V/III = 20, 50, and 80 have been used. Figure 1 shows the growth sequence of GaInAs/AlInAs modulation doped layers.

The film structure was investigated by cross-section transmission electron microscopy (TEM). To enhance the weak contrast from atomic ordering the multi-beam dark field imaging technique[10] was ap-

Table I. Results and Growth Conditions of Hall Measurements

Sample	A_1	A_2	B_1	B_2	C_1	C_2
Orientation	[100]	[100] + 4°	[100]	[100] + 4°	[100]	[110]
T_{sub}C	500	500	500	500	300	300
V/III Ratio	20	20	50	50	80	80
$\eta_s \times 10^{12}$ cm^{-2}, 300K	2.36	2.8	2.2	2.7	1.7	2.6
$\eta_s \times 10^{12}$ cm^{-2}, 77K	2.4	3.0	2.35	3.4	2.4	3.1
$\mu_s \times 10^3$ cm^2/Vs, 300K	10.5	6.7	10.6	8.2	6.6	7.8
$\mu_s \times 10^3$ cm^2/Vs, 77K	36.5	18.0	34.0	18.3	7.8	15.6

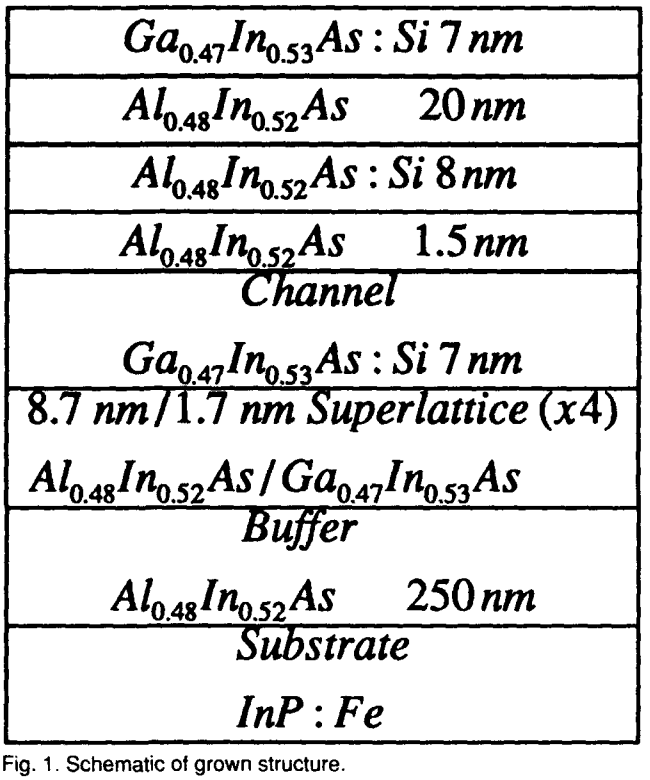

Fig. 1. Schematic of grown structure.

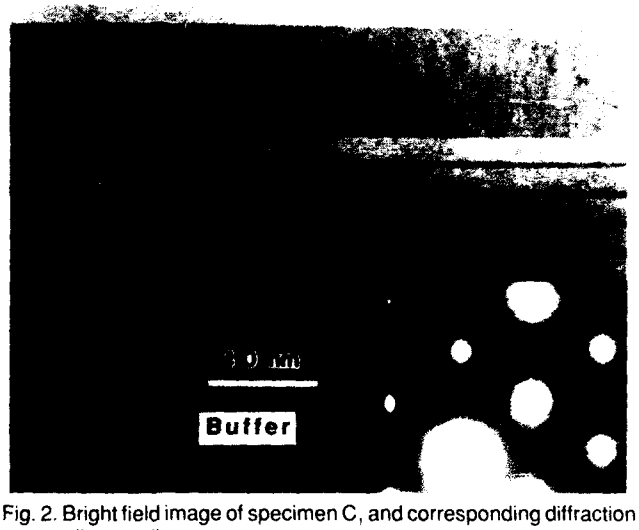

Fig. 2. Bright field image of specimen C_1 and corresponding diffraction pattern (inserted).

plied. The dark field images were formed by interference of seven diffracted beams with Miller indices: $(1\bar{1}1)$, $(1\bar{1}\bar{1})$, $(2\bar{2}0)$, $(\bar{2}22)$, $(\bar{2}2\bar{2})$, $(3\bar{3}1)$, and $(3\bar{3}\bar{1})$ while the $(2\bar{2}0)$ diffracted beam was adjusted along the optical axes.

RESULTS AND DISCUSSION

The TEM study of layers grown at 500°C on [100] surfaces (A_1 and B_1) show high crystal perfection. No substantial differences were observed with increasing V/III ratio. All interfaces between the layers shown on Fig. 1 are abrupt. The surfaces of these two samples were smooth. A low density of stacking faults was observed only in the layers grown at 300°C with V/III ratio of 80 (samples C_1). These defects can be a result of a slight mismatch between the InAlAs layer and the substrate.[11] Diffraction patterns obtained from the buffer layer in sample C_1 showed streaks along [100] (Fig. 2), indicating the presence of defects on (100) planes one or two atomic layers thick. However, multi-beam dark field high resolution TEM images do not show any contrast features. One can speculate that these defects were As-rich platelets; since in this case, the expected contrast between (Al-In) and As planes would be very weak.

For the layers grown on (110) at 300°C with V/III ratio of 80 (sample C_2) stacking faults and antiphase boundaries were found. The surface of the sample was smooth. Diffraction patterns obtained from the buffer layer showed as well streaks along [110] with clear maxima at $1/2g_{220}$, indicating group III elements ordering on (110) planes (CuAu type). This kind of ordering was found earlier in AlInAs.[8]

The layers grown at 500°C (samples A_2 and B_2) on [110] substrates tilted 4° toward $[11\bar{1}]$ were not as perfect as those grown on [100] substrates. In both cases, the surface of the sample was much more undulated. This thickness variation was observed only along $[1\bar{1}0]$ and not when viewed along [001] (Figs. 3 a,b). The amplitude was in the range of a few nanometers. The observed contrast was strongly anisotropic and showed compositional modulation. It was noticed that these inhomogeneities were mainly present in the InAlAs buffer layer and in InAlAs/InGaAs superlattices. It appeared that these inhomogeneities decreased strongly in the InGaAs channel layer and increased slightly again in the upper InAlAs layer. This suggests that the layer rich in Al was more susceptible to the compositional nonuniformities.

In the multi-beam dark field TEM images macro-steps about 2 nm high along [1 $\bar{1}$ 0] were observed at InGaAs/InAlAs superlattice interfaces (Fig. 4). They were not found in cross-section specimens oriented along [001]. The macro-steps at the InGaAs/InAlAs heterointerfaces on both sides of the superlattice packet were not situated above each other. This suggests step motion during the crystal growth. The trace of one such macro-step is shown by line AB in Fig. 4. Movement of such a step can even interrupt thin layers (Fig. 4). From detailed analysis of dark field images, one can conclude that the steps are mostly faceted by (1 $\bar{1}$ 1) planes. From the knowledge of the tilt direction, one can conclude that these (1 $\bar{1}$ 1) macro-step facets were terminated by In. Such macro-steps are potential sites for accumulation of impurities and point defects giving rise to inhomogeneities in the buffer layer and in the superlattices during their motion. Most probably, these inhomogeneities are related to the presence of Al, because they are not found in the Al-free channel layer. Multi-beam dark field images taken from the InAlAs buffer layer and the InAlAs/InGaAs superlattices show chains of bright spots along [001], which can either be InAs or AlAs monoatomic platelets (see A in Fig. 5). The presence of these platelets resulted in diffuse scattering along [110], clearly visible in the diffraction pattern (inserts in Fig. 3 and Fig. 5). Two diffuse intensity maxima between the 220 and 440 diffraction spots divided the 220 diffraction vector into three almost equal distances. This would suggest that on average each third (220) atomic plane was occupied by monoatomic platelets. However, one needs to note that the g_{220} was not equally divided into three parts but the distances between the matrix and diffuse spots were slightly larger than $1/3g_{220}$. In direct space, it corresponds to a smaller interplanar [110] distance between monoatomic platelets. Taking into account the atomic radii of the elements, $r_{Al}<r_{Ga}<r_{In}$, one can conclude that each third plane must be occupied by Al atoms. This ordering of platelets is stronger in sample B_2 grown at higher V/III ratio than in the sample A_2. It appears that substrate tilting plays an important role in ordering due to the lowering of the symmetry of the growth surface. By tilting to a specific direction, one type of surface steps will dominate lowering atomic symmetry of the grown layer. The type of ordering can be changed by substrate tilting as it was observed for the sample C_2 (Fig. 6) and B_2 (A_2).

From Hall measurements, it was observed that the mobility is much lower in samples A_2 and B_2 grown on [110] InP substrates tilted 4°-off compared to the samples grown under the same conditions on [001] oriented substrates. The sheet charge ηs is always higher for these samples (Table I). This fact is consistent with the observed structure of these specimens. The layers grown on [110] 4°-off oriented substrates are very inhomogenous with macro-steps at the interfaces, which are high enough to interrupt the 2DEG layer (Fig. 4) and reduce the 2DEG mobility.

The abrupt decrease of electron mobility μ_n in sample C_1 grown on the [001] oriented substrate at 300°C can be explained by formation of very small platelet de-

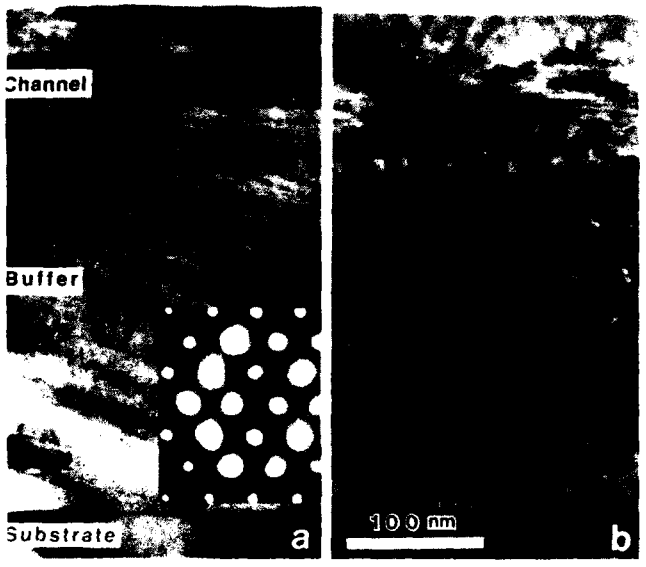

Fig. 3. Bright field image of specimen B_2 taken in [1 $\bar{1}$ 0] (a) and [001] (b) directions. Corresponding diffraction pattern is inserted.

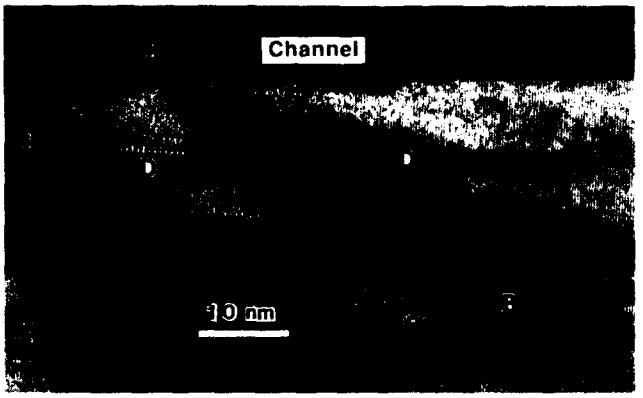

Fig. 4. Dark field multi-beam image of sample B_2.

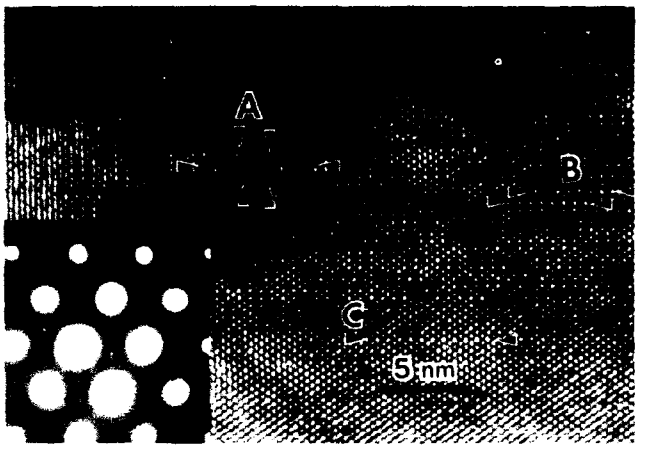

Fig. 5. Dark field multi-beam image of sample A_2 and corresponding diffraction pattern. (A) CuAu type ordered domain, (B) two AlAs platelets separated by two interplanar distances in [110] direction, and (C) single AlAs platelet.

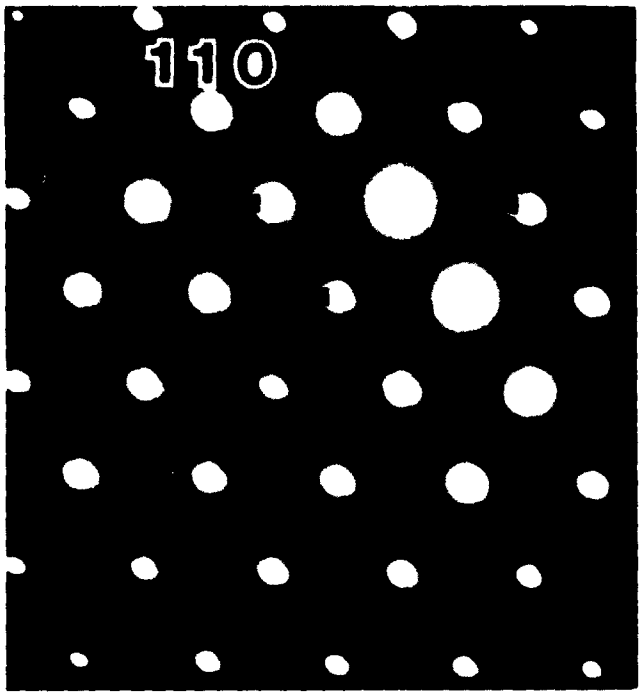

Fig. 6. Selected area diffraction pattern from sample C_2. Extra diffuse maxima correspond to CuAu-type ordering.

fects randomly distributed in the layer and the presence of stacking faults. The ordering along [110] observed in the sample C_2 leads to lower scattering and an increase of the carrier mobility.

CONCLUSIONS

Growth of InGaAs/InAlAs layers on [100] and [110] tilted substrates showed clear differences in the inhomogeneities formed in the layers and the formation of defects. No changes were observed for the samples grown on [100] surfaces at 500°C with an increase of the V/III ratio. In this case, all layers were homogeneous. However, for the layers grown at lower temperature (300°C with the V/III ratio of 80), the presence of monoatomic platelets was detected. Growth on [110] surfaces at this low temperature leads to ordering on (110). In both types of samples, stacking faults were observed, which most probably are formed due to a slight mismatch with the substrate.

For the samples grown at higher temperature, the ordering to form Al-rich platelets on each third atomic plane was observed. This was not found for samples grown on (100). Macro-steps terminated by (111) planes were found on all interfaces. The movement of these steps was most probably responsible for the inhomogeneities in these samples, which were mostly present in all layers containing Al. Incorporation of some impurities in these layers cannot be excluded. The observed compositional inhomogeneities and the macro-steps can explain the differences in electrical behavior of samples grown on (100) and (110) surfaces.

ACKNOWLEDGMENT

This work was supported by AFOSR-ISSA-90-0009, through the U.S. Department of Energy, under Contract No. DE-AC03-76SF00098. The use of the facility at the National Center for Electron Microscopy at the Lawrence Berkeley Laboratory is greatly appreciated.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

First Direct Observation of EL2-Like Defect Levels in Annealed LT-GaAs

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Nonstoichiometric arsenic-rich GaAs grown at low temperatures by molecular beam epitaxy (LT-GaAs) has been found to be semi-insulating after high-temperature annealing. The origin of this technologically important conversion is not yet fully understood. In order to study this effect, we performed photocurrent measurements on p-LT GaAs-n diodes in the spectral range between 0.75 and 1.5 eV at 8K. The photocurrent spectra revealed the following features which are unique to the EL2 level: photoquenching, characteristic photoionization transitions to conduction band minima and a presence of a broad band due to the effect of auto-ionization from the excited state. Moreover, modeling of the optical excitation process using realistic band structure demonstrates that these features cannot be explained by "internal photoemission" originating from As precipitates, as the "buried Schottky barrier model" predicts. This is the first direct experimental evidence for the existence of EL2-like defect levels and their importance for understanding the optical and electronic properties of annealed LT-GaAs.

Key words: Defect, EL2 defect, internal photoemission, low-temperature grown GaAs, photocurrent, photoquenching

INTRODUCTION

Low-temperature-grown GaAs (LT-GaAs) has recently attracted great interest due to its unique electrical properties.[1] In as-grown LT-GaAs excess As (up to 1.5 %)[2] has been found by optical absorption and electron paramagnetic resonance (EPR) to result in the formation of high concentrations of arsenic antisite (As_{Ga}) related defects (10^{20} cm^{-3}) which are responsible for hopping conductivity.[3] Upon annealing under arsenic overpressure, most of the excess As accumulates in a high density of precipitates.[4] Thereby the antisite concentration drops below the detection limits of optical absorption and EPR (detection limit approximately 10^{18} cm^{-3} in 1 μm thick films).[3] Concurrently, the material becomes semi-insulating.[1] The mechanism which is responsible for this technologically important property is still under debate. The following two models have been proposed: "defect mediated pinning"[3] and the "buried Schottky barrier model."[5] The "buried Schottky barrier model" proposes that the high resistivity can be understood in terms of the As precipitates, believed to be metallic, acting as internal Schottky barriers with overlapping depletion regions. On the other hand, the presence of deep defects (e.g., residual As antisites) could account for the semi-insulating behavior of the annealed LT-GaAs as in the case of bulk semi-insulating liquid encapsulated Czochralski (LEC) GaAs. However, an experimental technique which has adequate sensitivity to unambiguously detect deep defects in annealed LT-GaAs has not yet been applied.

This work presents the first direct evidence that after annealing, LT-GaAs layers still incorporate a

(Received April 12, 1993)
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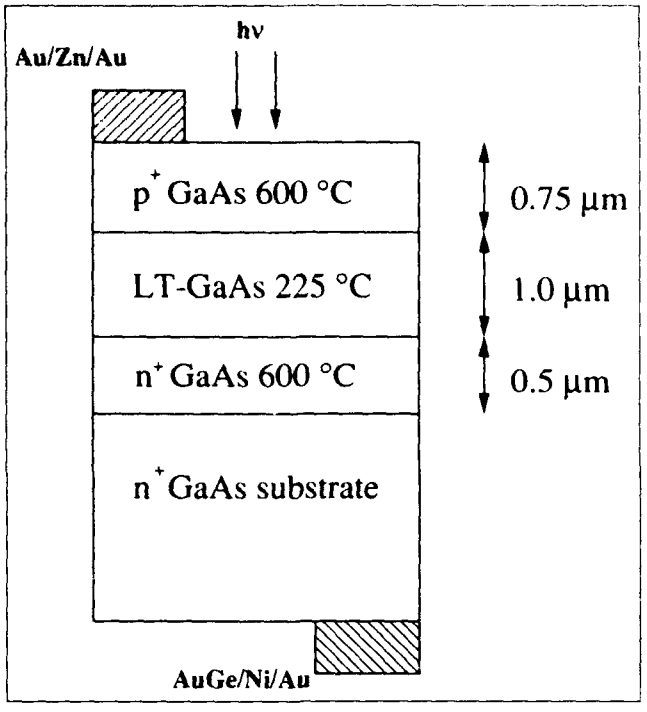

Fig. 1. Schematic of MBE grown p-LT GaAs-n photodiode. The substrate temperatures at which the MBE layers were grown are also shown.

significant concentration of the EL2-levels which are generally believed to be the first donor levels of the As_{Ga} antisite defect.[6] Based on photocurrent spectroscopy, which is known to feature very high sensitivity in the study of point defects and Schottky barriers, we demonstrate that the near-infrared optical sensitivity of the annealed LT-GaAs layers can be explained by photoexcitation of carriers from EL2-like defects.

EXPERIMENT

The photocurrent measurements were performed on p^+-LT GaAs-n^+ photodiodes which were grown by molecular-beam epitaxy (MBE) using a Varian Gen II system. Figure 1 shows a schematic diagram of our devices. The substrates used were n^+-type (2×10^{18} cm^{-3}) Si-doped (100) GaAs wafers. With such a high n-type doping, the formation of EL2 defects is essentially eliminated in bulk GaAs.[7] The absence of EL2 in the wafers used in this study was confirmed with optical absorption measurements. On the substrate, a 0.5 μm thick Si-doped n^+ buffer layer was grown at 600°C. Then, the As source was left open while the substrate temperature was reduced to 225°C. At this temperature, a 1.0 μm thick LT-GaAs epilayer was grown. Subsequently, the substrate temperature was raised to 600°C under As overpressure. The LT-layer was annealed during the overgrowth of a 0.75 μm thick Be-doped p^+ top layer. Au/Zn/Au and AuGe/Ni/Au contacts were evaporated on the top p^+ layer and the backside of the n^+ substrate, respectively. The metallizations were annealed at 350°C for 25 s to form ohmic contacts. Reference p^+-i-n^+ structures with 600°C grown intrinsic GaAs, instead of the LT-GaAs layer, were also fabricated. Analysis of the cross-sectional transmission electron microscopy revealed the existence of arsenic precipitates only in the annealed LT-GaAs layer. Rectifying behavior of both devices was confirmed by I-V measurements, showing that our samples were suitable for photocurrent measurements.

The photocurrent of a sample placed in a variable-temperature Janis cryostat was measured at zero-bias using standard lock-in techniques. Light emitted by a tungsten halogen lamp was dispersed with a 0.32 m Instruments S.A. grating monochromator used in the spectral range of $0.7\ eV < h\nu < 1.5\ eV$.

The experimental procedure was as follows. First, the p^+-LT-n^+ sample was cooled down to T = 8K in the dark and the photocurrent spectrum was measured using low intensity monochromatic light ("before illumination spectrum"). Next, this sample was illuminated with high intensity $h\nu = 1.2$ eV monochromatic light until the monitored photocurrent stabilized. After this, a second photocurrent spectrum was taken ("after illumination spectrum"). Then our sample was warmed up to 150K while the photocurrent was monitored. Next, the sample was cooled to T = 8K for a second time and a third spectrum ("restored spectrum") was recorded. Similar measurements were also performed on the reference p^+-i-n^+ structure. All recorded spectra were normalized by the photon flux determined in a separate measurement with a pyroelectric detector at the sample position.

RESULTS

The reference sample showed no significant photocurrent upon illumination with sub-band-gap light, whereas the p^+-LT GaAs-n^+ structure is extremely light sensitive. All three photocurrent spectra of the p^+-LT GaAs-n^+ sample show a smooth photoionization spectrum with three onset energies of 0.76, 1.08, and 1.3 eV (see "before" and "after illumination" spectra in Fig. 2a). Superimposed there is a broad band centered at about 1.18 eV with a full width at half maximum of 0.18 eV. The spectrum ("after illumination") taken after intense light illumination demonstrates that the photocurrent is partially quenched. However, the resulting overall shape is similar to the spectrum "before illumination." Between 0.9 and 1.05 eV, the quenching efficiency (i.e., the following ratio: |before-after|/before illumination spectrum) was 14%; the broad band centered at 1.18 eV could be quenched by 30%. Heating the sample above 130K fully restored the photocurrent spectrum ("restored spectrum") measured at T = 8K.

DISCUSSION

It is important to note that the onset energies in all three spectra fit quantitatively very well with the thresholds for the photoionization of the EL2 level from its midgap state to the Γ, X, and L conduction band minima.[8] Furthermore, the broad band is very characteristic to the EL2 defect observed in bulk semi-insulating GaAs.[9] This phenomenon is attrib-

uted to the $A_1 \rightarrow T_2$ intra-EL2 transition.[10] Subsequent multi-phonon relaxation back to the A_1 ground state or the transition to the metastable EL2* configuration does not contribute to the photocurrent, while the release of an electron to the conduction band via an auto-ionization process does.[6] This accounts for the difference in the absorption and photocurrent spectrum of EL2 in LEC-GaAs.[9] The probability of auto-ionization is dependent on the local environment of the EL2 defect. Local strain and electrical fields can be responsible for the relatively weak auto-ionization process observed in our samples in comparison to that in semi-insulating bulk GaAs.

The observed photoquenching effect and the recovery at 130K is a unique fingerprint of the EL2 level.[11] The photoquenching phenomenon of the EL2 defect is widely accepted to be due to the light-induced metastable transition of the As_{Ga} defect to its near interstitial position, resulting in the formation of an V_{Ga}-As_i pair.[6] In the case of bulk semi-insulating GaAs, the reverse transition at 120–130 K, the EL2 recovery, restores all the electrical and optical properties of the unquenched defect. As described above, we observe the recovery at this temperature.

The fact that the "after illumination" spectrum has the same overall shape suggests that the photocurrent again is due to EL2-like levels. Our observation that the signal is only partly quenchable can be attributed to the presence of the local strain in the region of the EL2-like point defects or by electric fields originating from the precipitates and the built-in voltage in the p^+-LT GaAs-n^+ junction.

Thus, our observations are evidence for EL2 defects being responsible for the optical sensitivity of annealed LT-GaAs.

In contradiction to our interpretation, based on a similar experiment, the optical sensitivity has previously been ascribed by D.T. McInturff et al.[12] to "internal photoemission" at buried Schottky contacts. They observed, as we do, a parabolic dependence of the photoresponse in the limited photon energy range of 0.8 to 1.1 eV at room temperature. To interpret their data, they used the analysis of Fowler[13] which predicts a parabolic dependence for the "internal photoemission" of carriers from the metal into the semiconductor at a two-dimensional Schottky barrier. This result is based on two assumptions. The first is that only those photoexcited carriers that have enough momentum perpendicular to the barrier can contribute to the photocurrent ("escape cone argument"). The second assumption is that the density of states at the Fermi energy is constant in the energy range of interest. This theory, however, cannot be directly applied to small three dimensional As clusters for the following reasons. First, the density of states of arsenic changes drastically at the Fermi energy,[14] as it is typical for semimetals. Second, the "escape cone argument" breaks down for small precipitates. These small clusters have a diameter of the order of the mean free path of a photoexcited electron. The presence of more than one surface within the mean free path length enhances the photoyield due to reflection at each interface.[15] In the limit of small three-dimensional clusters, all carriers excited with sufficient energy to overcome the barrier will contribute to the photocurrent and a photoyield proportional to $h\nu$-Φ_b would be expected.[13] Also, the semi-classical analysis is questionable since the De Broglie wavelength of a photoexcited electron is on the order of the observed As precipitate size.

MODELING

In order to determine the expected wavelength-dependence of the photocurrent from As clusters, we modeled the internal photoemission process in the limit of small particles. From local-density ab-initio calculations using the linear muffin-tin orbital method, the bulk As bandstructure was calculated. We assumed a constant oscillator strength because all direct transitions in the energy range under investigation are allowed due to the mixed s, p, d nature of all involved bands. All direct transitions in the three-dimensional Brillouin zone with sufficient energy in the final state to overcome the Schottky barrier height of 0.7eV[16] were integrated for the wavelengths in the range of interest. The calculated spectrum (see Fig. 2b) is smooth and shows, besides some

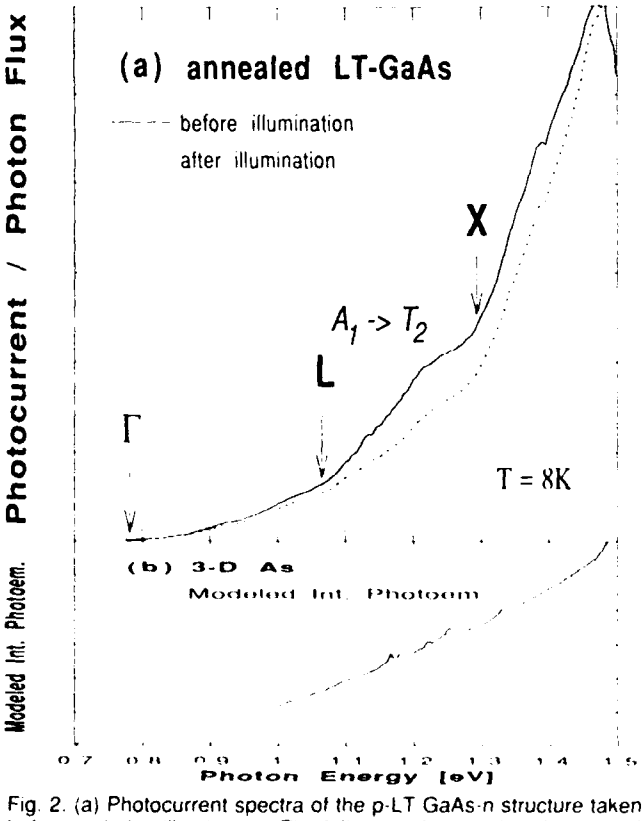

Fig. 2. (a) Photocurrent spectra of the p-LT GaAs-n structure taken before and after illumination. The following characteristic features of the EL2 defect are clearly visible: Transitions $A_1 \rightarrow \Gamma$, L, X, and T_2, and quenching. (b) Modeled internal photoemission spectrum of As precipitates in the limit of small clusters, using the band-structure as derived from the ab-initio density functional method. The spectrum is smooth, showing some small features between 1.15 to 1.35eV but no discontinuity in its slope.

small features between 1.15 to 1.35 eV, no discontinuity in its slope. Therefore, this result does not show any of the characteristic features of the experimentally determined photoresponse. However, one has to notice that the quantum confined nature of the small particles would cause the energy differences between occupied and unoccupied states near the Fermi level in the As bandstructure to be slightly larger then they are in bulk. This consideration alone is not expected to bring the calculated As spectral dependence in agreement with our experiment.

Therefore, these calculations further support our conclusion that the spectral dependence of the measured photoresponse is not dominated by internal photoemission at buried Schottky contacts.

CONCLUSION

In summary, photocurrent and photoquenching measurements were performed on annealed LT-GaAs. The spectral dependence of the photocurrent and its photoquenching behavior are direct evidence for the presence of EL2-like defects which are known to exist in bulk GaAs. In addition, model calculations that predict the expected photoresponse from As clusters reveal that our results cannot be explained by an "internal photoemission" process. Overall, we have directly shown, for the first time, that EL2 defects are present in annealed LT-GaAs, and that these levels have to be included when considering the optical and electronic properties of annealed LT-GaAs epilayers.

ACKNOWLEDGMENTS

We would like to thank W.E. Spicer for helpful discussions. This work was supported by the U.S. Air Force Office of Scientific Research under grant AFOSR-88-0162. M. van Schilfgaarde's work was supported by the Office of Naval Research under grant N00014-89-K-0132. The use of experimental facilities at the Lawrence Berkeley Laboratory supported by the U.S. Department of Energy is acknowledged.

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Temperature Investigation of the Gate-Drain Diode of Power GaAs MESFET with Low-Temperature-Grown (Al)GaAs Passivation

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We have investigated the breakdown-temperature characteristics of the gate-drain diode of a GaAs metal semiconductor field-effect transistor with low-temperature-grown (LTG) GaAs/AlGaAs passivation. An anomalous decrease in the breakdown voltage as a function of the temperature is observed. This behavior leads us to propose an explanation of how LTG passivation leads to a high breakdown voltage at room temperature; and this explanation in turn allows us to predict the power performance of the passivated devices.

Key words: Breakdown, LT-GaAs, MESFET, passivation

INTRODUCTION

The product of the maximum drain current and the gate-drain breakdown voltage is a good indication of the microwave power performance of a device. Whereas arbitrary value of drain current can be obtained by simply changing the channel epitaxial layer, a design that leads to a high gate-drain breakdown voltage is much more elusive. Recent works which incorporated the low-temperature-grown (LTG) GaAs as a surface passivant along with an overlapping gate structure have demonstrated dramatic improvement in the gate-drain breakdown voltage.[1,2] However, the mechanism through which the LTG passivating layer improves the breakdown voltage is not completely understood. In this work, we have fabricated and studied the temperature dependence of the gate-drain diode of a GaAs metal semiconductor field-effect transistor (MESFET) with LTG-(AlGaAs/GaAs) passivation and an overlapping gate structure. We have observed an anomalous decrease of the breakdown voltage at low temperature. By investigating this behavior, we can qualitatively explain how an LTG-passivant improves the gate-drain breakdown voltage.

(Received April 12, 1993)

DEVICE FABRICATION

The epitaxial structure was grown by molecular beam epitaxy (MBE) (Varian 360) on a (001) semi-insulating GaAs substrate. First, a smoothing buffer layer of 5000Å GaAs was grown at a substrate temperature of 600°C, followed by 1860Å of n-GaAs, and an arsenic-diffusion-barrier of 200Å of AlAs.[3] The substrate temperature was then lowered to 200°C, and 1000Å of LTG-GaAs was grown, followed by 1500Å of LTG-$Al_{0.3}Ga_{0.7}As$. The mobility and sheet charge concentration were determined from van der Pauw measurements on a separate structure, to be 3700 $cm^2/V\text{-}s$ and 3.8×10^{12} cm^{-2}, respectively.

The fabrication process of the device began with the definition of the mesa by wet chemical etching of the patterned sample. Next, the source-drain regions were defined and reactive-ion-etching (RIE) with Cl_2 was used to remove the insulating layers and expose the channel.

AuGe/Ni/Au ohmic contacts were defined by lift-off

and subsequent rapid-thermal-annealing at 375°C for 15 s resulting in a contact resistance of 0.3 Ω-mm. The foot of the gate was then defined and again RIE with Cl_2 was used to etch away the LTG layers down to the channel. Finally, the overlapping gate mask was aligned to the defined gate foot print and the gate was then formed by lift-off of Ti/Au metals. The schematic representation of the final cross-section profile of the device is shown in Fig. 1.

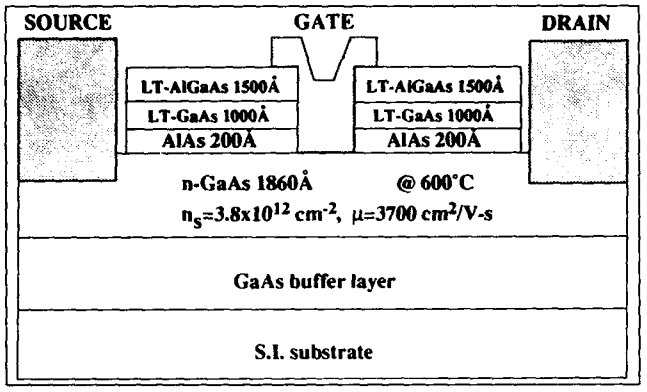

Fig. 1. Schematic representation of the cross section profile of a GaAs MESFET with LTG-($Al_{0.3}Ga_{0.7}As$/GaAs) passivation and overlapping gate structure.

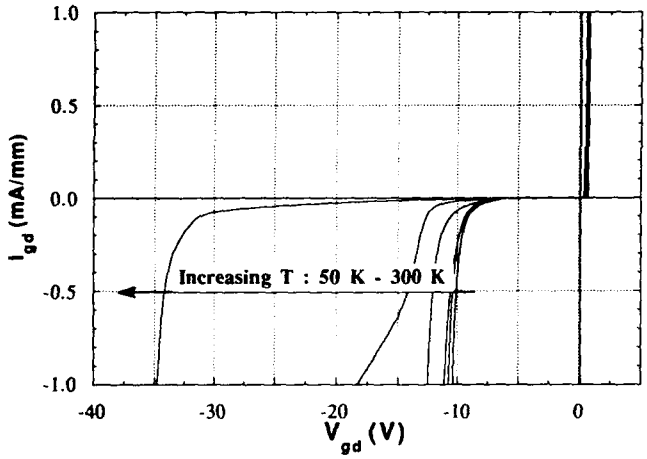

Fig. 2. Gate-drain diode characteristics at different temperature of a LTG-($Al_{0.3}Ga_{0.7}As$/GaAs) n-GaAs MESFET.

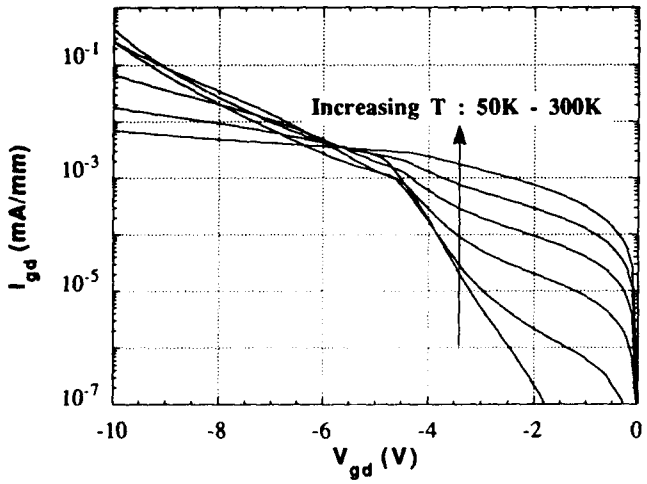

Fig. 3. Semi-log plot of the gate-drain diode characteristics.

RESULTS

The temperature characteristics of the gate-drain diode of a 1.2 μm gate-length GaAs MESFET with LTG-AlGaAs/GaAs passivation is shown in Fig. 2. At 300K, the diode shows a high breakdown voltage of 34 V. However, as the temperature is lowered, the breakdown voltage first decreased monotonically, then saturated to about 10 V at 7 K. A semi-log plot of the diode characteristic is shown in Fig. 3. In comparison, Fig. 4 shows the temperature-dependence behavior of a gate-drain diode in a conventional GaAs MESFET ($N_d = 3 \times 10^{17}$ cm^{-3}). In the conventional device, the observed dependence of the breakdown voltage with temperature is very small.

On-wafer continuous-wave power measurement of 1.2 μm × 300 μm devices are performed at 4 GHz. The output power and power-added-efficiency at a bias of V_{ds} = 13 V and V_{gs} = −1.5 V are shown in Fig. 5. The maximum power density obtained is 820 mW/mm at 26.4 % PAE.

DISCUSSION

The strong temperature dependence of the breakdown voltage observed in a MESFET with LTG-GaAs passivation can be explained by using existing breakdown models.[4,5] In the low gate voltage range, the current-voltage characteristics shown in Fig. 3 agree with the transport model of thermionically assisted tunneling between precipitates proposed by Ibbetson et al.[6] The electrons propagate from the gate metal onto the LTG-GaAs passivation layer by tunneling via the assistance of the local electric field and the temperature. However, since the electric field drops off rapidly away from the gate metal, the injected electrons are localized at those precipitates that are close to the gate metal. The resulting excess of the negative charges in the vicinity of the gate metal next

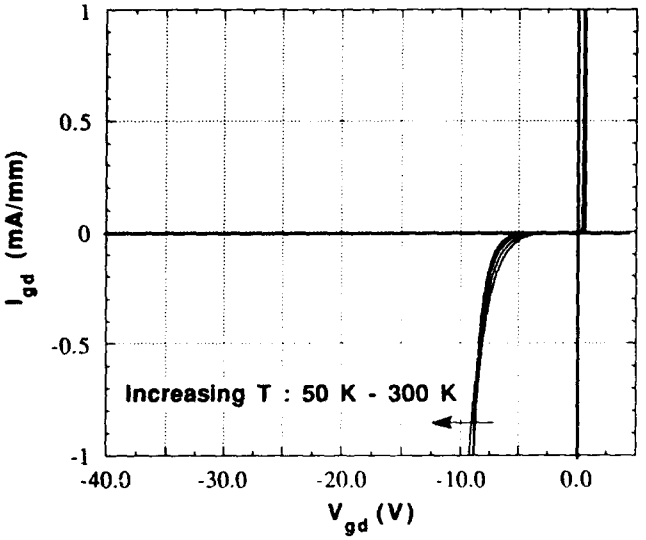

Fig.4. Gate-drain diode characteristics of a conventional GaAs MESFET.

to the drain would redistribute the associated electric field. Consequently, the peak electric field at the edge of the gate is alleviated. As the temperature is lowered, the number of electrons that can thermionically field emit into the precipitates is significantly reduced, thus the LTG-GaAs becomes less effective in reducing the field. At low temperature (77K), this field alleviation mechanism becomes relatively ineffective; thus, the breakdown voltage saturates at that of a conventional GaAs MESFET. Figure 6 shows schematically the electric field distribution with the field alleviation by the charged precipitates. The most conservative hypothesis we can draw is that, since the response of traps at low temperature is similar to their high frequency response, the rf breakdown may be close to the breakdown voltage at 77K. Even so, a large benefit results as explained below.

To obtain the maximum output power from MESFETs, the devices are usually biased at half of the breakdown voltage thereby allowing the rf signal to swing from zero to the rf breakdown voltage (BV_{rf}). However, the static electric field at the gate edge for LTG-passivated devices is low even at a gate-drain bias as high as BV_{rf} ($BV_{rf} << BV_{dc}$). We, therefore, expect that a full rf swing of $2 \times BV_{rf}$ can be accomodated in these devices, doubling (at the minimum) the rf power from passivated devices compared to conventional GaAs MESFETs. The power measurements on our device shown in Fig. 5 supports the above hypothesis.

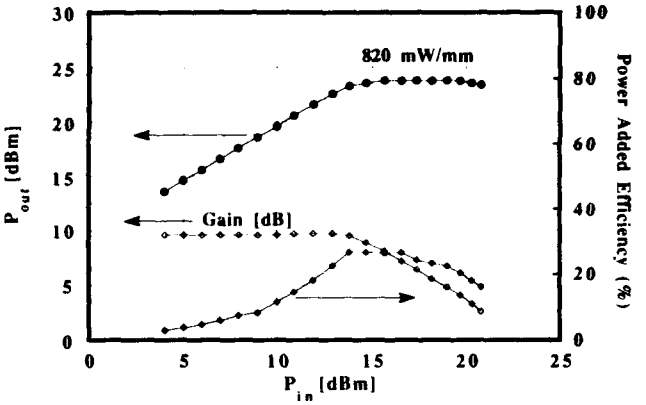

Fig. 5. Output power and power-added efficiency vs input power at 4 GHz for a 1.2 × 300 μm device.

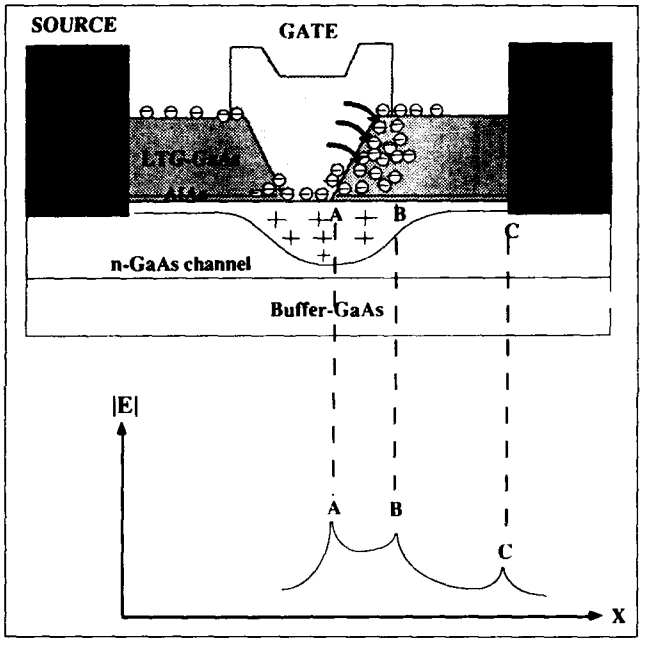

Fig. 6. Field redistribution by trapped charges at the gate metal edge at 300K.

CONCLUSION

By experimentally investigating the temperature dependence of the current-voltage characteristics of the gate-drain diode, we were able to explain the role that an LTG-($Al_{0.3}Ga_{0.7}As$/GaAs) layer plays in the alleviation of the electric field at the drain edge of the gate metal. This alleviation of electric field leads to a much higher breakdown voltage compared to that of the conventional MESFET. The device was able to deliver 820 mW/mm at 26.4 % PAE @ 4 GHz.

ACKNOWLEDGMENT

The authors would like to thank Wei-Nan Jiang for his assistance in the temperature measurement of the devices. This work is supported by the U.S. Air Force Office of Scientific Research (AFOSR-91-0111) and Hewlett Packard (MICRO); U.K. Mishra is supported by an NSF PYI Award (ECS-9144723).

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Low-Frequency Noise and Phase Noise in MESFETS with LTG-GaAs Passivation

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We report measurements of the low-frequency noise and phase noise of conventional unpassivated GaAs metal semiconductor field-effect transistors (MESFETs) and of MESFETs fabricated using an overlapping-gate structure and the low-temperature grown (LTG) GaAs as a passivation layer. The noise of the LTG-GaAs passivated MESFET was found to behave quite differently from that of a conventional MESFET and to be significantly reduced at low offset frequencies. These observations are explained in terms of the surface passivating effect of the LTG-GaAs. Low-frequency noise measurements seem to support the idea that the LTG-GaAs passivation reduces the number of active traps, in particular traps with large activation energies. These results indicate that LTG-GaAs passivation can substantially reduce the near-carrier phase noise of MESFET-based oscillators.

Key words: LT GaAs, noise, passivation

INTRODUCTION

Since the introduction of the low-temperature-grown (LTG) GaAs in 1988,[1] the interest in different applications of this material has been growing. Initially, it was used exclusively as a buffer layer between the substrate and the active layer in order to help reduce the effect of backgating. Later applications focused on increasing the gate-drain breakdown voltage[2] and on surface passivation.[3] Earlier noise measurements examined the influence of an LTG GaAs buffer on the low-frequency noise performance of metal semiconductor field-effect transistors (MESFETs)[4] and pseudomorphic heterojunction field-effect transistors.[5] In this paper, we focus on the effects of the LTG-GaAs on the low-frequency noise and phase noise of MESFETs when the material is used as a passivation layer on top of the conducting channel.

PHASE NOISE

An overlapping-gate MESFET with an LTG-GaAs passivation layer[3] (henceforth referred to as LTG-MESFET) and a conventional GaAs MESFET (henceforth referred to simply as MESFET) were used for the experiments. The 2000Å thick LTG GaAs passivation layer was grown in situ on top of the conducting channel by molecular beam epitaxy. No dielectric passivation layer was deposited to either the MESFET or the LTG-MESFET. The nominal gate length is 1 μm.

The phase noise of the devices was measured in the saturation regime using a 1 GHz carrier. The drain current was 60 mA and the drain-to-source voltage was 2.5 V. As illustrated in Fig. 1, the phase noise of the LTG-MESFET displays a flatter frequency dependence than the MESFET, which shows 1/f dependence, and is 15 dB lower at 1 Hz from the carrier and 10 dB higher at 100 kHz from the carrier. The lower near-carrier noise can be attributed to the passivation of surface states by addition of the LTG-GaAs layer. To test this assertion, we took low-frequency noise measurements on single devices when they were biased in saturation as well as the ohmic regime.

CHANNEL NOISE

The procedure for measuring low-frequency noise is standard and has been described elsewhere.[6] The

(Received April 12, 1993)

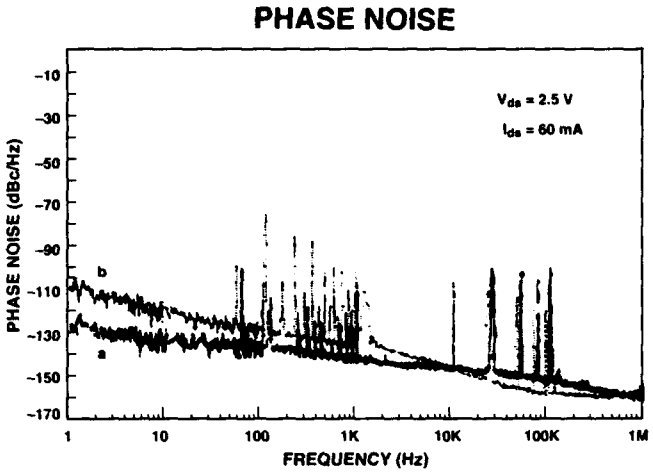

Fig. 1. Room-temperature phase noise measurements of devices biased in the saturation regime with I_{ds} = 60 mA: (a) LTG-MESFET, and (b) MESFET.

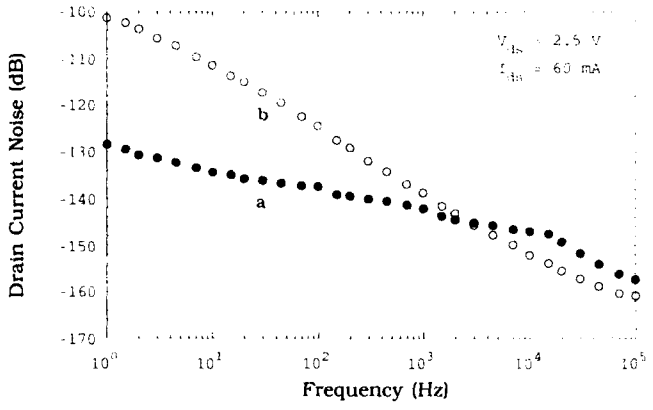

Fig. 2. Low-frequency noise of the same devices used in Fig. 1 for the phase noise measurement: (a) LTG-MESFET, and (b) MESFET.

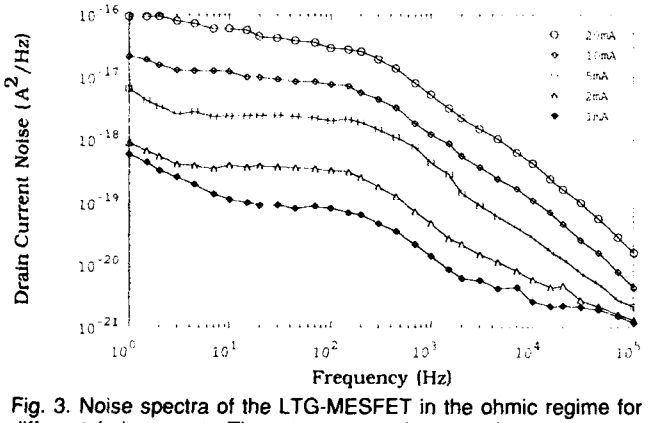

Fig. 3. Noise spectra of the LTG-MESFET in the ohmic regime for different drain currents. The gate-source voltage was kept constant at 0 V.

most noteworthy features of our technique are that it allows for amplifier noise and accounts for the nonflatness of the amplifier gain. In Fig. 2, we show the spectral intensity of the low-frequency drain-current fluctuations of the LTG-MESFET and MESFET in the saturation regime for a drain current of 60 mA and a drain-to-source voltage of 2.5 V. Two apparent differences between the devices are in the spectral shape and the magnitude of the noise. The MESFET exhibits a 1/f-shaped spectrum whereas the LTG-device has a weaker dependence on the frequency.

The low-frequency-noise measurements were consistent with the phase-noise results. At 1 Hz, the LTG-GaAs passivation reduced the phase noise and amplitude noise by 16 and 26 dB, respectively.

The low-frequency noise spectra for the LTG-MESFET biased in the ohmic regime are shown in Fig. 3. The gate bias was kept at 0 V while the drain current was varied from 0.5 to 10 mA. Further analysis identified two distinct spectral contributions: one (flat at small frequencies and rolling off at higher frequencies) that varies quadratically with the current (typical of a resistor) and may be associated with the conducting channel, and one (1/f-shaped and only observed at small frequencies and small currents) that varies linearly with current. The quadratic component has a frequency dependence that is weaker than 1/f and can in fact be modeled as a McWhorter-style[7] spectrum which is typical of a collection of trapping sites with a distribution proportional to the inverse of the trapping time constants:

$$S_i(f) = (A/f)\,[\arctan(f/f_1) - \arctan(f/f_2)],$$

where A is a constant proportional to the number of traps that are active, f the frequency, and $1/f_1$ and $1/f_2$ are the limits of the distritution of the trapping time constants. Such a spectrum is flat for frequencies smaller than f_1, rolls off as $1/f^2$ for frequencies larger than f_2, and behaves as 1/f for $f_1 < f < f_2$. The component that increases linearly with operating current can be modeled as having a 1/f dependence.

Similar measurements on the MESFETs in the ohmic regime reveal spectra that are almost perfectly 1/f-like and whose magnitude increases quadratically with increasing bias current. The fact that this component is not observed in the LTG-MESFETs leads us to believe that the 1/f noise is not fundamental in nature in the way described by Handel.[8] This component could not have been masked in the LTG-MESFETs because the observed noise is smaller than in the MESFETs. Hence, these 1/f shaped spectra could also be a manifestation of a McWhorter-style spectrum with a larger range of trapping time constants.

The difference between the MESFET and the LTG-MESFET is the addition of the LTG-GaAs passivation layer. It appears that the LTG-GaAs passivation layer modifies the distribution of the surface traps, resulting in a shift of the distribution of trapping time constants. One can view this as shifting the upper limit of the trapping time distribution to smaller values; i.e., deactivating the deeper traps that have long time constants. This interpretation is supported by Fig. 4, which compares the channel noise of the two MESFETs operating at 5 mA (ohmic regime) with two different gate voltages. The observed knee in the LTG-MESFET spectra is the upper limit of the trapping time constants. The 1/f part of the spectral intensity for the LTG-MESFET is slightly larger than

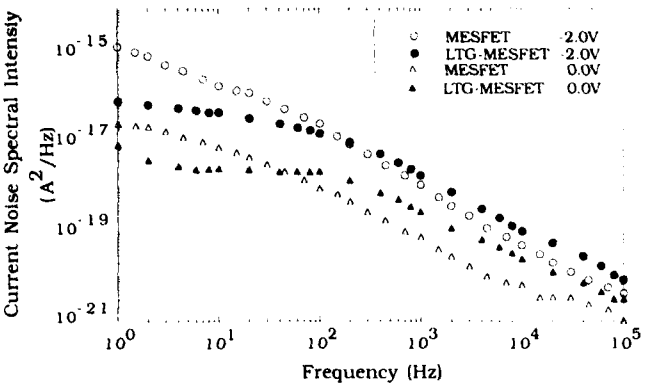

Fig. 4. Ohmic-regime noise spectra (I_{ds} = 5 mA) of the LTG-MESFET and MESFET for two different gate voltages.

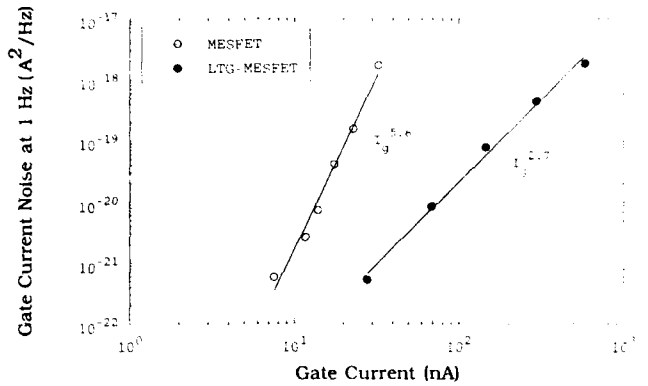

Fig. 5. Gate-current noise spectral intensity at 1 Hz as a function of the reverse gate current for both devices.

for the MESFET. (The spectra are measured in the ohmic regime at the same current so that comparison is warranted.) In addition, since the magnitude is a measure of the number of traps that are active, slightly more traps are active in the LTG-MESFET than in the MESFET. From these two observations, we conclude that for devices operating in the ohmic regime, the addition of the LTG passivating layer removes traps with larger activation energies and adds (only marginally) traps with smaller activation energies. Apparently, the modification of the surface changes the energy distribution of the traps. There have been examples where modification of the surface in MOSFETs reduced the trap density. In addition, experiments on buried channel MOSFETs and MESFETs showed improved noise performance.

GATE NOISE

To study the effect of gate current on noise, we measured the noise with the drain and source connected to ground and a reverse bias applied to the gate. Figure 5 shows the gate noise at 1 Hz as a function of the gate current with V_{ds} = 0 V. At a given gate current (10 nA < I_g < 1000 nA), the MESFET is much noisier and the current dependence of the noise is much stronger. For a given gate voltage, the LTG-MESFET has a larger gate current but a smaller noise coefficient, resulting in quieter operation than in the MESFET at an identical gate-voltage.

With this observation in mind, let us reexamine Fig. 4. We observe that the drain current noise of the MESFET increases more strongly as the gate voltage is changed from 0 to –2 V, at fixed drain current of 5 mA, than the noise of the LTG-MESFET. Changing the gate voltage from 0 to –2 V increases the gate current in both devices and increases the noise in the gate current of the MESFET more strongly (see Fig. 5). Since the gate current flows through the channel, the noise in the gate current does contribute to the drain current noise we measure, and could explain the larger increase of the MESFET drain current noise.

CONCLUSION

Including the LTG-GaAs layer as a passivating layer on top of the device seems to reduce the phase noise at low off-set frequencies. This is supported by measurements of the low-frequency noise. A noise reduction of 15 dB was observed when the MESFET and LTG-MESFET were biased in saturation with a drain current of 60 mA.

Further noise measurements taken when the devices were biased in the ohmic regime revealed that the passivation layer seems to deactivate the traps with larger activation energy and only marginally increase the density of the shallower traps.

The current dependence of the gate noise of the MESFET is much stronger than that of the LTG-MESFET and the noise level is larger for gate currents ranging from 10 to 1000 nA. As a result, for a given gate-to-source voltage, the MESFET is noisier than the LTG-MESFET. Further studies are underway to investigate a possible connection with the overlapping passivating layer.

ACKNOWLEDGMENT

The Lincoln Laboratory portion of this work was supported by the U.S. Air Force Office of Scientific Research.

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Journal of Electronic Materials, Vol. 22, No. 12, 1993

Application of Low Temperature GaAs to GaAs/Si

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Low Temperature grown GaAs (LT-GaAs) was incorporated as a buffer layer for GaAs on Si (GaAs/Si) and striking advantages of this structure were confirmed. The LT-GaAs layer showed high resistivity of 1.7×10^7 Ω-cm even on a highly defective GaAs/Si. GaAs/Si with the LT-GaAs buffer layers had smoother surfaces and showed much higher photoluminescence intensities than those without LT-GaAs. Schottky diodes fabricated on GaAs/Si with LT-GaAs showed a drastically reduced leakage current and an improved ideality factor. These results indicate that the LT-GaAs buffer layer is promising for future integrated circuits which utilize GaAs/Si substrates.

Key words: LT-GaAs, GaAs on Si

INTRODUCTION

The growth of GaAs on Si (GaAs/Si) has attracted much attention mainly because it offers large and mechanically strong GaAs substrates. These advantages make GaAs/Si suitable for substrates of low cost GaAs ICs. Another advantage lies in the high thermal conductivity of Si, which allows us to use higher power per chip. The GaAs/Si technique is also promising for monolithic integration of III-V devices with Si devices. The GaAs/Si technique, however, has several severe problems to be solved, which include poor crystal quality, poor surface morphology, and lack of a semi-insulating property. The severest problem is poor crystal quality caused by the differences in lattice constants and thermal expansion coefficients. A large number of studies have concentrated on this problem. These works include the two step growth technique, the use of a strained superlattice, and thermal annealing.[1-3] These techniques indeed improve crystal quality to some extent, but the numbers of residual threading dislocations are still on the order of 10^5–10^7/cm^2. These values are much higher than that of a bulk GaAs wafer. The rough surface of GaAs/Si is also a big problem especially for heterojunction devices which require atomically flat interfaces. Lack of the semi-insulating property causes difficulty in device isolation of field-effect transistors (FETs).

In industry, GaAs metal semiconductor field-effect transistors (MESFETs) are usually fabricated on liquid encapsulated Czochralski (LEC) wafers which are semi-insulating due to EL2. This semi-insulating property makes the fabrication process very simple and reduces parasitic capacitance greatly. However, in the case of GaAs/Si substrates, it is very difficult to introduce such deep levels at a proper amount. GaAs/Si often suffers from contamination of Si donors from the substrate.[4] Therefore, the use of some highly resistive buffer layer between active layer and sub-

(Received April 12, 1993)

strate is desirable for device isolation on GaAs/Si substrates.

Recently, F.W. Smith et al. showed that GaAs layers grown by molecular beam epitaxy (MBE) at substrate temperatures as low as 200–300°C (LT-GaAs) show high resistivity and eliminate the side-gate effect of MESFET devices significantly when this layer is incorporated between the transistor active region and the substrate.[5] Low-temperature GaAs layers are slightly conductive in the as-grown state and become highly resistive upon post-annealing at 600°C. Hence, the growth of the normal active GaAs layer on top of the LT layer causes it to become highly resistive. While as-grown LT-GaAs displays a dilated lattice constant ($\Delta a/a \cong 0.1\%$), LT-GaAs shows the normal lattice constant after the 600°C anneal.

We investigated the feasibility of the use of LT-GaAs as a buffer layer for GaAs/Si structures. The use of the LT buffer layer is supposed to help isolate devices on GaAs/Si substrates. The LT-GaAs buffer layer may also improve the crystal quality of the top layer because the LT layer is highly strained at least in the as-grown state. In this paper, we will show that the use of the LT buffer layer for GaAs/Si is advantageous in many aspects using characterization techniques such as photoluminescence, current voltage/capacitance voltage (I-V/C-V) measurements, and surface roughness measurements.

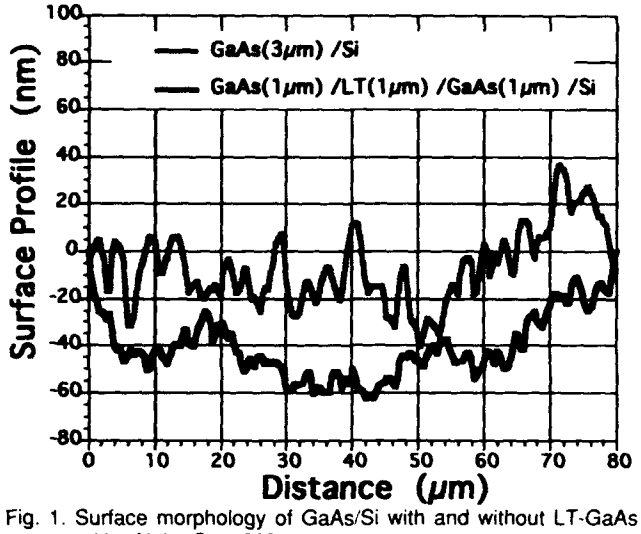

Fig. 1. Surface morphology of GaAs/Si with and without LT-GaAs measured by Alpha Step 200.

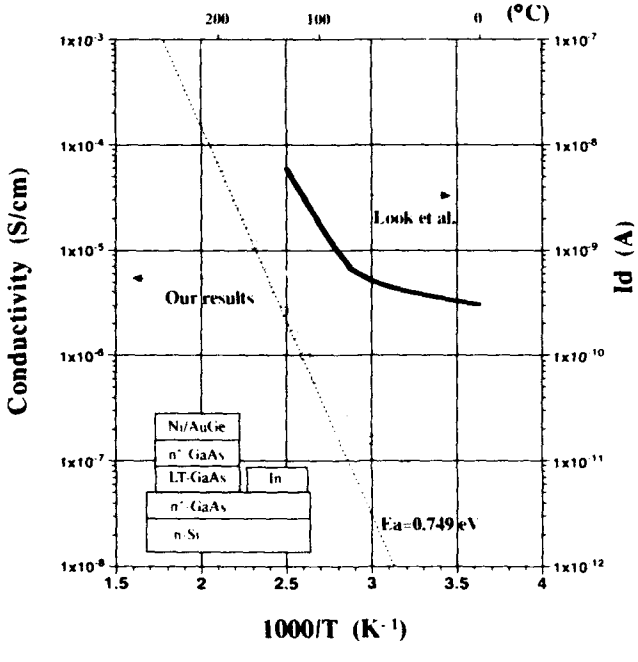

Fig. 2. Temperature dependence of conductivity of LT-GaAs on Si.

EXPERIMENTAL PROCEDURE

All the samples were grown using a RIBER 1000 MBE system. Silicon wafers with (100) four degrees off toward [011] orientation were used for all the experiments. Just before loading the substrate into the MBE chamber, the substrate was cleaned using a similar method to that reported by Ishizaka et al.[6] In the growth chamber, the samples were heated up to about 900°C by a direct radiation method for 10 min to remove the surface oxide. The substrate temperature for GaAs growth was chosen initially at 380°C and then increased up to the normal growth temperature (600°C). This is known as the two-step growth procedure. The LT-GaAs buffer layer was grown on this structure at a nominal temperature of 240°C. The thickness of this layer was varied from 0.5 to 2 μm. On top of LT-GaAs, the active GaAs layer was grown at 600°C. The growth rate for the normal GaAs and the total thickness were set at about 1 μm/h and 3 μm, respectively. For comparison, structures without LT-GaAs, but with the same total thickness of 3 μm were grown.

Some of the samples were processed into n-i-n mesa structures or Au Schottky diodes to check the electrical properties of the LT buffer layer and the top layer, respectively. The normal GaAs layers of such samples were doped by a Si effusion cell during growth. The other samples are used for photoluminescence and surface roughness measurements. Because LT-GaAs is extremely resistive, it is difficult to determine its resistivity without being affected by the current through the substrate. To overcome this problem, a mesa n-i-n structure was used.[7] In this structure, an LT-GaAs layer was sandwiched by two n⁺-GaAs layers and isolated by mesa-etching. Therefore, we can measure the resistivity accurately. A schematic representation of this sample structure is superimposed in Fig. 2. After evaporating Ni/AuGe through a mask, a rapid thermal anneal was performed at 350°C for 15 s to make contacts ohmic. Mesa etching was done using Ni/AuGe electrode as a mask. After mesa etching, In dots were placed on the bottom n⁺-GaAs layer and then the sample was annealed at 200°C for 10 min. To investigate the electrical properties of the top GaAs layers, Au Schottky diodes were fabricated. Since the LT-GaAs layer was incorporated under the active layer, both Schottky contacts and Ni/AuGe ohmic contacts were placed on the surface of the top GaAs layer.

RESULTS AND DISCUSSIONS

Figure 1 shows surface roughness of GaAs/Si with and without the LT-GaAs buffer layer measured by an Alpha Step 200 profilometer. One can see that the surface morphology is improved by the use of the LT-GaAs buffer layer. The surface becomes smoother with increasing thickness of the LT-GaAs buffer layer. However, a thick LT-GaAs buffer layer leads to a poor electrical property as will be described later. Therefore, there exists an optimum thickness for device applications. This improvement in surface morphology was also confirmed by Nomarsky interference micrographs. It can be attributed to the reduced surface migration of adsorbed atoms during the growth of the LT-GaAs layer.

To confirm the semi-insulating nature of the LT-GaAs layer on GaAs/Si, I-V curves were measured on n-i-n mesa structures. Figure 2 shows an Arrhenius plot of the zero-bias resistivity. The zero-bias resistivity at room temperature is 1.7×10^7 Ω-cm, which indicates that LT-GaAs has a semi-insulating nature even on a highly defective GaAs/Si. In Fig. 2, the temperature dependence of current through LT-GaAs by Look et al. is also shown; however, their sample structure is different from ours, and it is grown on a GaAs substrate.[8] Basically, our result has the same tendency as that of Look et al. up to 130°C except for the slope near room temperature. This slope is known to be sensitive to the anneal temperature.[8] In the temperature range from 140 to 200°C, we observed a typical band conduction with its activation energy of 0.749eV. This value is close to that for typical LEC wafers dominated by the EL2 midgap donor.

Photoluminescence (PL) was used to check the crystalline quality of the top GaAs layer on the LT-GaAs layer. Figure 3 shows PL spectra for samples with and without LT-GaAs measured at 8K under the same conditions. Broad peaks between 1–1.6 μm and large peaks between 0.8–0.85 μm can be assigned to emissions from deep levels and near-bandgap emissions, respectively. Comparing the two spectra, one can see that GaAs/Si with LT-GaAs has 25 times higher intensity than that without LT-GaAs, although both samples show the emissions from the deep levels. This result indicates that the use of LT-GaAs improves crystal quarity.

All the Au Schottky diodes fabricated on GaAs/Si showed straight $1/C^2$-V plots, which indicate that the Si doping is homogeneous. The typical doping concentration and the Schottky barrier height estimated by this measurement were 3.1×10^{16} cm^{-3} and 0.91 eV, respectively. Figure 4 shows I-V characteristics for Schottky diodes with and without LT-GaAs that were processed simultaneously. One can see that the use of an LT-GaAs drastically reduces the leakage current. This is a direct evidence for the improvement in electrical properties by the use of LTGaAs. The ideality factor for the diode is also improved by the use of LT-GaAs from 1.27 to 1.13. The

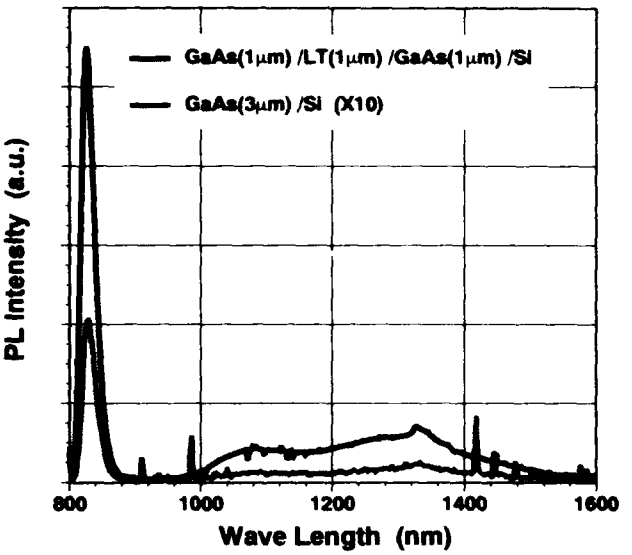

Fig. 3. Photoluminescence spectra of GaAs/Si with and without LT-GaAs.

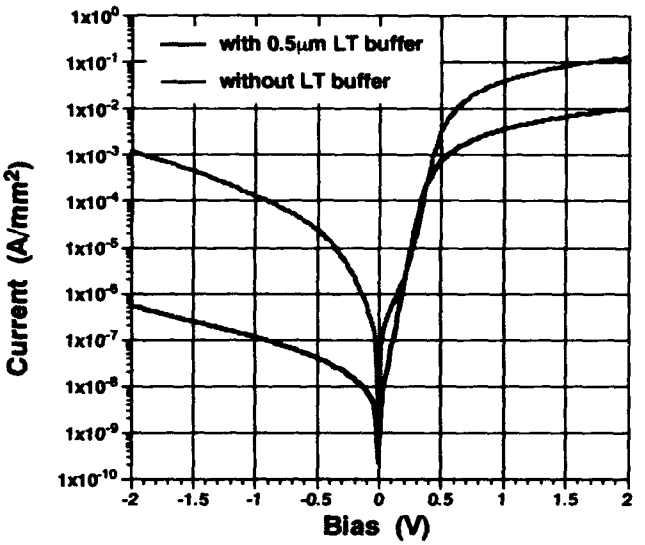

Fig. 4. Current-voltage characteristics of Schottky diodes with and without LT-GaAs.

lower series resistance in the foward bias region for the sample without LT-GaAs can be attributed to the current thorough the Si substrate. For further improvement in electrical properties, the combination of the LT-GaAs buffer layer with the other defect reduction techniques such as the strained superlattices are promising because their fabrication processes are basically compatible with each other. We also measured the temperature dependence of the leakage current of the diodes at –1V. The differential activation energy at room temperature for structures with and without LT-GaAs were 0.43 and 0.057eV, respectively. This result implies that the leakage current for the diode without LT-GaAs is dominated by a weakly temperature dependent transport through the defects. We also measured the LT-GaAs thickness dependence of the leakage current while keeping the

total thickness at 3 μm. The leakage current increased with increasing LT-GaAs thickness from 0.5 to 2 μm. This degradation in crystal quality is probably due to strain buildup in the LT-GaAs layer. This tendency is consistent with transmission electron microscopy observations by Liliental-Weber et al.[9]

CONCLUSIONS

Low temperature grown GaAs (LT-GaAs) was utilized as a buffer layer for GaAs on Si (GaAs/Si) to investigate the feasibility of device isolation with this layer. The LT-GaAs layer showed high resistivity of 1.7×10^7 Ω-cm even on highly defective GaAs/Si. We found two additional advantages of this buffer layer. They are improvements in electrical and optical properties of the top GaAs layer and in surface morphology. These results indicate that the use of the LT-GaAs buffer layer is promising for future integrated circuits on GaAs/Si substrates.

ACKNOWLEDGMENTS

This work was supported by the U.S. Air Force Office of Scientific Research, contract number 91-0321. The authors would like to thank Drs. K. Takasaki, T. Eshita, W. Chen, P. Dreszer, N. Newman, and Z. Liliental-Weber for helpful comments and discussions.

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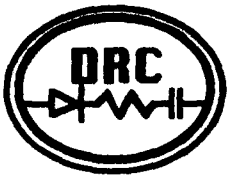

Announcement of the

52nd Annual
DEVICE RESEARCH CONFERENCE

UNIVERSITY OF COLORADO
BOULDER, CO
JUNE 20-22, 1994

Abstract Deadline: March 2, 1994

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The DRC brings together scientists, engineers, and students to discuss new and exciting breakthroughs and advances in the field of device research. The DRC is sponsored by the IEEE Electron Devices Society. The conference will be held at the University of Colorado from Monday, June 20 through Wednesday, June 22. The DRC and the Electronic Materials Conference (EMC) of the AIME will again coordinate activities. The EMC will be held at the same location on June 22-24. Device oriented papers should be submitted to the DRC and materials oriented papers to the EMC.

Papers are solicited on a wide variety of novel device structures including but not limited to the following:

- Silicon CMOS/BiCMOS
- Silicon Scaled and Ultrasmall Devices
- SOI and 3D Devices
- Thin Insulators & Hot Electron Effects
- Thin Film Transistors
- Device Modeling
- Vacuum Devices
- Sensors and Micromachined Devices
- Display Technology
- Silicon or Other Power Devices
- SiGe Devices
- III-V or II-VI FET or Bipolar Devices
- Quantum Effect Devices
- Integrated Optoelectronics
- Microwave Devices
- Optical Sources and Detectors
- Superconducting Devices
- Semiconductor/Superconductor Devices
- New Characterization Techniques
- Device Reliability
- Amorphous or Organic Devices
- Wide-Bandgap Devices

CALL FOR PAPERS: Authors are requested to send twenty-five (25) copies of a summary of their paper, together with the IEEE copyright transfer form, to Umesh K. Mishra, DRC Technical Program Chairman. A SUMMARY SENT BY FACSIMILE CAN NOT BE ACCEPTED.

The summary must consist of one page of text (600 words, abstracts that exceed the suggested length may be returned) and one page of figures (line drawings are preferred; photos with fine features or gray scale may not reproduce well). The summary must clearly reflect the content of the paper, and be in a form suitable for publication. The text page should include the authors' names, address, affiliation, telephone number, and appropriate literature references. The figures should be clearly labeled and captioned. Accepted summaries will be reproduced in the conference program exactly as submitted. Since the accepted abstracts will subsequently be published without figures in the IEEE Transactions on Electron Devices, the text should be understandable without figures and the figures should not be referenced. Previously published results will be automatically rejected.

The deadline for summaries is March 2, 1994. Late papers may be submitted up to the day before the conference, but the acceptance criteria will become more stringent as the conference approaches.

FURTHER INFORMATION: Registration forms and information on accommodations can be obtained from the Local Arrangements Chairman, Bart Van Zeghbroeck.

Early registration is encouraged with a reduced registration fee offered as an incentive. Students also will receive a reduced registration fee. Limited travel funds are available to students presenting papers. Further information on student assistance may be obtained by writing to Joe Campbell

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(Required by 39 U.S.C. 3685)

1A. Title of Publication	1B. PUBLICATION NO.	2. Date of Filing
Journal of Electronic Materials	0 3 6 1 5 2 3 5	September 30, 1993
3. Frequency of Issue	3A. No. of Issues Published Annually	3B. Annual Subscription Price
Monthly (1993)	12	$185.00

4. Complete Mailing Address of Known Office of Publication *(Street, City, County, State and ZIP+4 Code) (Not printers)*

420 Commonwealth Drive, Warrendale, PA 15086 (Allegheny County)

5. Complete Mailing Address of the Headquarters of General Business Offices of the Publisher *(Not printer)*

420 Commonwealth Drive, Warrendale, PA 15086

6. Full Names and Complete Mailing Address of Publisher, Editor, and Managing Editor ***(This item MUST NOT be blank)***

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Journal of Electronic Materials
Author Instructions

General Purpose

The *Journal of Electronic Materials (JEM)* is published by the Electronic Materials Committee of The Minerals, Metals & Materials Society (TMS) and the Electron Devices Society of the Institute of Electrical and Electronics Engineers. *Journal of Electronic Materials* regularly reports on the science and technology of electronic materials, while examining new applications for semiconductors, magnetic alloys, insulators, and optical and display materials. The journal welcomes articles on methods for preparing and evaluating the chemical, physical, and electronic properties of these materials. Specific areas of interest are electronic memory and logic structures, magnetic-optical recording media, superlattices, packaging detectors, emitters, metallization technology, superconductors, and low thermal-budget processing. The journal also selectively publishes invited and contributed review papers on topics of current interest to enable individuals in the field of electronics to keep abreast of activities in areas peripheral to their own. Further, *JEM* publishes papers from the annual conference sponsored by the TMS Electronic Materials Committee. It is the journal's editorial intent that the published papers be of interest to nonspecialists and specialists in the field of the particular contribution.

Review Process

Papers for *JEM* are reviewed by two qualified referees to determine suitability. The editor's decision to accept or reject a paper, based on referees' comments, is final. Send three copies of the manuscript key-stroked, double-spaced on 22 × 28 cm (8.5 × 11 in.) paper to the appropriate section or associate editor (see inside front cover). Alternatively, a paper/review/letter can be submitted directly to the editor (see inside front cover) as in the past, who will assign the manuscript to appropriate section or associate editor (obviously the latter procedure takes longer). Papers dealing with subjects not identified with any particular section or associate editor should be sent to Theodore C. Harman. Fax transmittal of one copy of a letter to G.B. Stringfellow followed simultaneously with two hard copies (one of which includes glossy prints or equivalent) via surface/air mail is recommended for shortened publication times. Authors will be notified when their manuscripts have been accepted for publication.

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JOURNAL OF ELECTRONIC MATERIALS

Volume 22, No. 12 **December 1993**

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