AD-A281 724

ATION PAGE

Form Approved
OMB No. 0704-0188

average 1 hour per response, including the time for reviewing instructions, searching existing data sources, ng the collection of information. Send comments regarding this burden estimate or any other aspect of this to Washington Headquarters Services, Directorate for information Operations and Reports, 1215 Jefferson f Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	Feb. 15, 1994	Final Report 4/1/90 - 3/31/93

4. TITLE AND SUBTITLE

Development of Nanostructure Fabrication Technology & New Electron-Quantum Wave Devices

5. FUNDING NUMBERS

DAAL03-90-G-0058

6. AUTHOR(S)

Professor Stephen Y. Chou

DTIC ELECTE JUL 13 1994 S F D

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of Minnesota
Department of Electrical Engineering
200 Union Street SE
Minneapolis, Minnesota 55455

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

U.S. Army Research Office
P. O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

ARO 27578.7-EL

11. SUPPLEMENTARY NOTES

The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

12a. DISTRIBUTION / AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

94-21120
2pp
94 7 12 064

13. ABSTRACT *(Maximum 200 words)*

Under the three-year grant, we have (a) investigated and developed various nanofabrication technologies including construction of an ultra-high resolution electron beam lithography system, sub-20 nm electron beam lithography techniques, etching of sub-40 nm silicon pillars and ridges; (b) fabricated various nanoscale transistors including a number of new device structures; (c) studied quantum effects and single electron effects; (d) designed, fabricated, and investigated ultra-fast metal-semiconductor-metal photodetectors with the record speeds on various of semiconductors, including low-temperature GaAs with 510 GHz bandwidth, bulk GaAs with 300 GHz, and bulk Si with 75 GHz.

DTIC QUALITY INSPECTED 1

14. SUBJECT TERMS	15. NUMBER OF PAGES
Nanofabrication, Electron Beam Lithography, Quantum Effect Devices, Single Electron Transistors, & High Speed Photodetectors.	18
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

DEVELOPMENT OF NANOSTRUCTURE FABRICATION TECHNOLOGY & NEW ELECTRON-QUANTUM WAVE DEVICES

FINAL REPORT

CONTRACT PEROIOD, APRIL 1, 1990 - MARCH 31, 1993

BY: PROFESSOR STEPHEN Y. CHOU

FEBRUARY 15, 1994

Accesion For
NTIS CRA
DTIC TAB
Unannounced
Justification
By
Distribution /
Availability Codes
Dist | Avail and / or Special
A-1

U.S. ARMY RESEARCH OFFICE

CONTRACT/GRANT # DAAL03-90-G-0058

PROPOSAL # 27578-EL

UNIVERSITY OF MINNESOTA
DEPARTMENT OF ELECTRICAL ENGINEERING
200 UNION STREET SE
MINNEAPOLIS, MN 55455

APPROVED FOR PUBLIC RELEASE;
DISTRIBUTION UNLIMITED.

TABLE OF CONTENTS

I. STATEMENTS OF INVESTIGATION

Under the three-year grant, we have (a) investigated and developed various nanofabrication technologies including construction of an ultra-high resolution electron beam lithography system, sub-20 nm electron beam lithography techniques, etching of sub-40 nm silicon pillars and ridges; (b) fabricated various nanoscale transistors including a number of new device structures; (c) studied quantum effects and single electron effects; (d) designed, fabricated, and investigated ultra-fast metal-semiconductor-metal photodetectors with the record speeds on various of semiconductors, including low-temperature GaAs with 510 GHz bandwidth, bulk GaAs with 300 GHz, and bulk Si with 75 GHz.

II. SUMMARY OF RESULTS

2.1 Construction of an Ultra-high Resolution Electron Lithography System

To establish a first-class nanofabrication research program, we must have an ultra-high resolution electron beam lithography (EBL) system. However, a commercial EBL system usually costs $2 - 3 million to purchase and $200 - 300 K per year to maintain, making it unaffordable to most universities. We built an ultra-high resolution electron beam lithography system for nanolithography by modifying a commercial high resolution scanning electron microscope, JEOL-840A, and adding pattern generator electronics that we designed and built. Special measures were taken in modification, electronics design, and noise reduction. These measures have made our system having a ultra-high resolution that can be equaled by only a few other U.S. universities. The EBL system was built for $180K--less than one-tenth the cost of a commercial system, and was financed by PI's Start-Up Grant from the University of Minnesota. The ARO grant supported part of the maintenance and operation cost of this EBL system. Using the EBL system and novel fabrication technologies, we have fabricated various nanostructures and nanodevices of sub-30-nm minimum feature sizes needed for our ARO supported research.

2.2 Development of 10 nm Electron Beam Lithography Technology

Stronger quantum effects, stronger Coulomb blockade effects, and higher operating temperatures for high functionality devices all require a smaller device size. In the past three years, we have been continuously improve our electron beam lithography technologies. We have examined various factors that can significantly impact the e-beam lithography resolution. Examples are resist types, resist thickness, developer contrast, proximity effects, e-beam accelerating voltage, etc. In the first year of the grant, we fabricated double 15 nm wide metal lines 10 nm apart on GaAs. Then we fabricated other sub-30 nm structures and transistors. Recently, we developed nanofabrication technologies that fabricated 10 nm linewidth metal gratings of 40 nm pitch and the

quantum devices' gates of 10 nm gap on GaAs. These nanofabrication technologies developed were the corner stones of our ARO supported nanodevices research.

2.3 Development of Sub-40 nm Reactive Ion Etching of Si

Using high resolution electron beam lithography and RIE with Cl_2 and $SiCl_4$ gases we have etched sub-40 nm Si pillars, trenches, and ridges with aspect ratios greater than 10. These are among the smallest features ever fabricated using these techniques. We believe that the size of these Si features etched with the recipe described here is limited by the size of the etching mask, rather than by the etching process itself. Furthermore, we found that the RIE etching is crystallographically dependent and that the nanoscale structures can be further reduced by wet HF etching. No photoluminescence has been detected from arrays of Si pillars with feature sizes of the order of 10 nm and passivated using HF acid.

2.4 Quantum Effects in Nanometer Transistors

A number of nanometer quantum effect devices were built. They include quantum effect devices (QEDs) with a constricted gate of a 20 nm gap, QEDs with double quantum boxes in the channel, QEDs with coupled quantum waveguides, and QEDs with a double bent channel. The nanoscale gates consist of 15 nm thick Ti and 35 nm thick Au on GaAs, and they were fabricated using our ultra-high resolution electron beam lithography and a lift-off process.

One-dimensional Waveguide Transistor

The first type of QEDs is the constricted gate QEDs that have a constriction much smaller than that of the previous devices. Therefore these QEDs showed the quantum effects at a much higher temperature. For example, distinct $2e^2/h$ staircase in the current-voltage characteristics were observed above 4.2 K (Fig. 2), instead of 0.3K. Each conductance stair corresponds to a new 1-dimensional subband contributing to the transport as the channel width is widened by the gate voltage.

Investigation of Leaky-Waveguide Transistor

The conductance oscillations in the I-V characteristics of a leaky waveguide transistor have been attributed to tunneling of one-dimensional (1D) electrons over a single barrier and the discreteness of the 1D density of states. We have fabricated leaky-waveguide transistors that have a structure similar to that made by Professor del Alamos group at MIT. But the uniqueness of our transistors is that it allows significant tunneling of 2D electrons over the single barrier in addition to that of 1D electrons. We have observed strong conductance oscillations in our devices, and we found that the oscillations are greatly enhanced with a DC source-and-drain bias. These observations cast doubts on the original explanation of the oscillation based on tunneling of 1D electrons and the

discreteness of the 1D density of states. Currently, we are investigating the origin of the oscillations by modeling, simulating, and examining different device structures.

2.5 Single Electron Transistors

We proposed a new type of nanometer single-electron field-effect transistor that has a single barrier inside a one dimensional channel. We fabricated the transistors in AlGaAs/GaAs heterostructure using high resolution electron beam lithography and observed periodic conductance oscillations due to the Coulomb blockade of a single electron.

The one dimensional channel was formed using a constricted gate scheme with a gap as narrow as 50 nm; the barrier is created using a metal bar of 50 nm width between the constricted gates. The metal gates were fabricated using e-beam lithography with a custom-built e-beam system followed by a lift-off process. Double layer resist with a 950K PMMA layer on top of a 100K PMMA layer was used.

At low temperatures, for a single electron transistor (SET) with a 50 nm gate gap, more than 10 conductance oscillations were observed, before the onset of the first $2e^2/h$ plateau, as the gate voltage was swept. Similar conductance oscillations were observed in SETs with a 100 nm gate gap. The oscillations were periodic, and the periods were 15 mV and 9 mV for devices with gate gaps of 50 nm and 100 nm, respectively. The oscillations persisted after thermal cycling and photon excitation. Analysis showed that the oscillation period in the gate voltage corresponds to the gate voltage needed to put a single electron into the 1-D channel and that the drain current reaches a peak when a Coulomb level aligns up with the Fermi level. The shape of the oscillation peak can be well fit by the derivative of the Fermi-Dirac distribution, indicating the peak width is caused by thermal broadening of a sharp energy level. Other aspects of the experiment were found to well agree with the single electron Coulomb blockade model. Furthermore, our investigation also shows that the smaller the gate gap, the larger the oscillation period, indicating that higher operation temperature can be achieved in smaller devices.

2.6 Ultra-high Speed MSM Photodetectors

Metal-semiconductor-metal (MSM) photodetectors are very attractive to optical fiber communication systems, future high-speed chip-to-chip connections, and high speed sampling. MSM photodetectors have several advantages over p-i-n photodiodes, such as higher speed, simple fabrication, and compatibility with large-scale FET IC fabrication technology. To increase MSMPD's speed, both the finger spacing and width should be reduced. The smaller the finger spacing, the shorter the carrier transit time, making the transit-time-limited MSM PD faster and the recombination-time-limited MSM PD more sensitive. The smaller the finger width, the less the

detector's capacitance and the higher the detector's external speed. Previously, the fastest transit-time-limited MSM photodetector was made on GaAs, and had a finger spacing of 0.5 μm, finger width of 0.75 μm, and a measured response time of 4.8 ps; the fastest recombination-time-limited high-sensitivity MSM photodetector was fabricated on low-temperature MBE grown (LT) GaAs, and had finger spacing and width of 0.2 μm, and response time of 1.2 ps.

Nanoscale finger spacing and width of MSM PDs were defined by PMMA resist coating, direct electron beam writing, metal evaporation, and a lift-off process. For finger spacing and width greater than 100 nm, double layer PMMA was used; for sub-100 nm spacing and width, single layer PMMA was used. The e-beam lithography system was operated at 35 kV.

Measurement using a 100 fs pulsed laser and an electro-optic sampling system showed that the full width at half maximum impulse response and the 3-dB bandwidth of the nanoscale MSM PDs are, respectively, 0.87 ps and 510 GHz for LT GaAs, 1.4 ps and 300 GHz for bulk GaAs, and 5.5 ps and 75 GHz for bulk Si. To our knowledge, they are the fastest high-sensitivity photodetectors for each material reported to date. Effects of carrier recombination time, carrier transit time, and RC constant on device speed have been studied. The capacitance and resistance of nanoscale MSM PDs were investigated. Monte Carlo simulation of device speed was studied and compared with experimental data. Based on these investigations, we proposed the scaling rules for designing high-speed MSM PDs.

III. PUBLICATION LIST

The work presented in the following 11 journal papers and 19 conference papers were partially supported by the ARO grant.

Journal Papers

[1] S.Y. Chou and P.B. Fischer, "Double 15nm-Wide Metal Gates Separated by 10 nm on GaAs," *J. Vac. Sci. and Tech.*, **B8**, pp 1919-1922, 1990.

[2] S. Y. Chou, Yue Liu, Paul B. Fischer, "Fabrication of Sub-50-nm Finger-Width and Spacing High-Speed Metal-Semiconductor-Metal Photodetectors Using High Resolution Electron Beam Lithography and MBE," *J. Vac. Sci. and Tech.*, **B9**, pp 2920-2924, 1991.

[3] S. Y. Chou, Yue Liu, and Paul B. Fischer, "Tera-Hertz GaAs Metal-Semiconductor-Metal Photodetectors with 25 nm finger Spacing and Finger Width," *Appl. Phys. Lett.*, **61**, 27, 1992.

[4] S.Y. Chou, Y. Liu, W. Khalil, P.B. Fischer, T.Y. Hsiang, and S. Alexander, "Ultrafast Nanoscale Metal-Semiconductor-Metal Photodetectors," *Appl. Phys. Lett.*, **61**, 819, 1992.

[5] S.Y. Chou and Y. Wang, "Single Electron Coulomb Blockade in a Nanometer Field-Effect Transistor with Single Barrier," *Appl. Phys. Lett.*, **61**, 1591, 1992.

[6] S.Y. Chou, and M.Y. Liu, "Nanoscale Tera-Hertz Metal-Semiconductor-Metal Photodetectors," IEEE, J. of Quantum Electronics, Vol. 28, pp 2358-2368, 1992.

[7] Y. Wang, and S.Y. Chou, "Engineering Sub-50 nm quantum Effect Devices and Single-electron Transistors Using E-Beam Lithography," *J. Vac. Sci. and Tech.*, **B10**(6), pp 2962-2965, 1992.

[8] M.Y. Liu, S.Y. Chou, T.Y. Hsiang, S. Alexander, and R. Sobolewski, "Nanoscale metal-semiconductor-metal photodetectors with subpicosecond response time fabricated using electron beam lithography," *J. Vac. Sci. and Tech.*, **B10**(6), pp 2932-2935, 1992.

[9] P.B. Fischer and S.Y. Chou, "Sub-50 nm High Aspect-ratio Silicon Pillars, Ridges, and Trenches Fabrication suing Ultrahigh E-Beam Lithography and Reactive Ion Etching" *Appl. Phys. Lett.*, **62**(12), 1414, 1993.

[10] P.B. Fischer and S.Y. Chou, "10 nm Electron Beam Lithography and sub-50 nm overlay using a modified scanning election microscope," *Appl. Phys. Lett.*, **62**(23), 2989, 1993.

[11] S. Alexandrou, C.C. Wang, T.Y. Hsiang, M.Y. Liu, and S. Y. Chou, "A 75-GHz Silicon GaAs Metal-Semiconductor-Metal Schottky Photodetectors," *Appl. Phys. Lett.*, **62**(20), 2507, 1993.

Conference Papers

[1] S.Y. Chou and P.B. Fischer, "Double 15nm-Wide Metal Gates Separated by 10nm on GaAs Fabricated Using Electron beam lithography, Single Layer Resist and Lift-Off," *The 34th International Symposium on Electron, Ion and Photon Beams*, San Antonio, Texas, May 29-June 1, 1990.

[2] Y. Liu, P.B. Fischer, and S.Y. Chou, "Picosecond Metal-Seminconductor-Metal Photodetectors with Sub-100-nm finger Spacing and Finger Width in GaAs," *Picosecond*

Electronics and Optoelectronics Topical Meeting, Salt Lake city, Utah, March 13-15, 1991, *OSA Proceedings on Picosecond Electronics & Optoelectronics,* Vol. 9, pp. 97-100, 1991.

[3] S. Y. Chou, Yue Liu, and Paul B. Fischer, "Fabrication of Sub-50-nm Finger-Width and Spacing High-Speed Metal-Semiconductor-Metal Photodetectors Fabricated Using High Resolution Electron Beam Lithography and MBE," *The 35th International Symposium on Electron, Ion and Photon Beams*, Seattle, Washington, May 29-June 1, 1991.

[4] S.Y. Chou, "Fabrication and Performance of nanoscale Quantum-Effect Devices and Tera-Hertz MSM Photodetectors," invited paper, *1991 Int'l. Semiconductor Device Research Symposium*, Dec. 4-6, 1991

[5] S. Y. Chou, Yue Liu, and Paul B. Fischer, "Tera-Hertz GaAs Metal-Semiconductor-Metal Photodetectors with Nanoscale Finger Spacing and Width," *1991 International Electron Device Meetings,* Washington, D.C., Dec. 8-11, 1991

[6] Yue Liu, Paul B. Fischer, and S. Y. Chou, "Fabrication of Sub-Picosecond Metal-Semiconductor-Metal Photodetectors with 25 nm Finger Spacing and Width Using High-Resolution Electron Beam Lithography," *1992 Conference on Lasers and Electro-Optics*, Anaheim, CA, May 10-15, 1992.

[7] S.Y. Chou, Y. Liu, T.Y. Hsiang, S. Alexandrou, and R. Sobolewski, "Picosecond metal-semiconductor-metal photodetector with nanometer finger structure on bulk Si, semi-insulating GaAs, and low-temperature GaAs," *1992 Conference on Lasers and Electro-Optics*, Anaheim, CA, May 10-15, 1992.

[8] T.Y. Hsiang, S. Alexandrou, C.C. Wang, R. Sobolewski, S.Y. Chou, and Y.Liu, "Subpicosecond Characterization of Nanometer-Scale Metal-Semiconductor-Metal Photodiodes, Conference on Lasers and Electro-Optics, Anaheim, CA, May 10-15, 1992.

[9] S.Y. Chou, "High Speed and High Functional Nanoscale Devices," *1992 Int'l. electron Device Martial Symp,* invited paper, Taipei, Taiwan, Nov. 1-4, 1992

[10] Y. Liu, W. Khalil, P.B. Fischer, S.Y. Chou, T.Y. Hsiang, S. Alexander, and R. Sobolewski. "Nanoscale Metal-Semiconductor-Metal Photodetectors with Sub-Picosecond Response Time Fabricated Using Electron Beam Lithography," The 36th Int'l Symp. on Electron, Ion and Photo Beams, Orlando, Florida, May 26-29, 1992.

[11] Y. Wang, and S.Y. Chou, "Engineering Sub-50 nm quantum Effect Devices and Single-electron Transistors Using E-Beam Lithography," The 36th Int'l Symp. on Electron, Ion and Photo Beams, Orlando, Florida, May 26-29, 1992.

[12] S.Y. Chou, and Y.Liu, T.Y. Hsiang, S. Alexandrou, C.C. Wang, R. Sobolewski, "Terahertz Metal-Semiconductor-Metal Photodiodes," third Int. Symp. on Space Terahertz Technology, Ann Arbor, MI, March 24-26, 1992.

[13] Y. Liu, W. Khalil, P.B. Fischer, S.Y. Chou, T.Y. Hsiang, S. Alexander, and R. Sobolewski. "Nanoscale Ultrafast Metal-Semiconductor-Metal Photodetectors," The 50 th Device Research Conference, Cambridge, Mass, June 22-24, 1992

[14] S.Y. Chou and Y.Wang. "A New Single Electron Transistor," The 50 th Device Research Conference, Cambridge, Mass, June 22-24, 1992

[15] P.B. Fischer and S.Y. Chou, "Sub-50 nm High Aspect-ratio Silicon Pillars, Ridges, and Trenches Fabrication suing Ultrahigh E-Beam Lithography and RIE," 1992 Int'l Conf. on solid State Devices and Materials, Tsukuba, Japan, August 26-28, 1992.

[16] S.Y. Chou and Y.Wang. "A New Single Electron Transistor," 1992 Int'l Conf. on solid State Devices and Materials, Tsukuba, Japan, August 26-28, 1992.

[17] S.Y. Chou, Y. Liu, W. Khalil, P.B. Fischer, T.Y. Hsiang, S. Alexander, and R. Sobolewski. "Nanoscale Sub-Picosecond Metal-Semiconductor-Metal Photodetectors," 1992 Int'l Conf. on solid State Devices and Materials, Tsukuba, Japan, August 26-28, 1992.

[18] P.B. Fischer and S.Y. Chou, "10 nm Electron Beam Lithography," Int. Conf. on Microcircuit Entering, Erlangen, Germany, Sept. 21-24, 1992

[19] P.B. Fischer and S.Y. Chou, "Sub- 40 nm RIE," Int. Conf. on Microcircuit Entering, Erlangen, Germany, Sept. 21-24, 1992

Double 15-nm-wide metal gates 10 nm apart and 70 nm thick on GaAs

Stephen Y. Chou and Paul B. Fischer
Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

(Received 29 May 1990; accepted 3 August 1990)

A method that can fabricate two narrow but thick metal lines separated by a small gap on a bulk semiconductor substrate is described. By opening a 40-nm-wide trench in a single layer of 70-nm-thick polymethylmethacrylate resist on GaAs using high resolution electron beam lithography, and by double shadow evaporations and a lift-off, two 15-nm-wide metal lines 10 nm apart and 70 nm thick were fabricated on a bulk GaAs substrate. The pitch size of the double metal lines is 25 nm. This is a factor of 2 smaller than the previous smallest pitch size on bulk semiconductors. It is found that the width and spacing of the two lines are uniform over tens of microns. It is also found that metals shadow evaporated on top of the resist can be removed successfully by a lift-off, even though they were connected to the metals in the resist trenches. These results suggest that using this method metal lines with even finer linewidth (< 15 nm) can be achieved on a bulk semiconductor substrate.

I. INTRODUCTION

Fabrication of lateral dual-gates electron quantum-interference transistors requires not only that width of gate-metal lines be narrow, but also that separation of the two gates be small and uniform since the separation determines width of a quantum well, and that thickness of the gate-metal lines be large since it determines gate resistance and therefore high frequency performances of the devices.[1,2] Previously, 8-nm-wide metal lines 10 nm apart and 10 nm thick have been fabricated on ultrathin carbon membrane using contamination resists, a high resolution electron beam system, and reactive ion etchings.[3] However, the finest metal lines with the smallest separation on a bulk GaAs substrate are 10 nm wide, 40 nm apart, and 15 nm thick.[4] In this paper, we describe a process which can fabricate double 15-nm-wide metal lines 10 nm apart and 70 nm thick on a bulk GaAs substrate. The method involves high resolution electron beam lithography, a single layer polymethylmethacrylate (PMMA) resist, double shadow evaporations, and a lift-off process.

Although the shadow-evaporation technique has been used to fabricate small metal structures on a bulk substrate for many years, it was limited to cases where metals were shadow-evaporated from a fixed angle toward one sidewall of a trench structure.[5-8] Furthermore, a lift-off process was not used in cases where metals were shadow-evaporated on a resist step which has a relatively straight sidewall, since it was believed that metal on the sidewall would be continuously connected to the metal on top of the resist and therefore the lift-off would fail. In the novel process described in this paper, metals were shadow evaporated twice from two nearly opposite angles toward both sidewalls of a resist trench. Moreover, a lift-off process is used to remove the metals on top of the resist, leaving two fine metal lines of a very small spacing on the substrate. Use of lift-off instead of reactive ion etching or ion milling can avoid ion bombardment of semiconductors and therefore preserves high electron mobility of semiconductor materials.

II. EXPERIMENT

Bulk GaAs substrates were spin coated with a single layer 950 000 molecular weight PMMA. While two thickness of PMMA were used, 37.5 and 70 nm, 70-nm-thick resist was used in most of the experiments. After spinning the resist, samples were baked at 160 °C for about 12 h. Line patterns were exposed into resists using a high resolution electron beam lithography system at a beam energy of 35 KeV and at various doses, and were developed in cellosove:methanol (3:1) developer at 22 °C for 7 s. Metals (Ti/Au) were then evaporated onto the resists profiles at angles varying from normal incident to 36° from the normal direction. For some samples metals were shadow evaporated only once from a fixed angle toward one sidewall of resist trench; for other samples metals were shadow evaporated twice from two nearly opposite angles toward both sidewalls of a resist trench. Thus two fine metal lines separated with a narrow gap are formed in the same resist trench. Finally, the metals on top of the resists were lifted off in acetone solvent. The processing sequence for fabricating double metal lines is illustrated schematically in Fig 1.

In the double shadow evaporations as depicted in Fig. 2, linewidth of a metal line on a GaAs substrate from the first shadow evaporation, LW_1, is given by $LW_1 = W - H \tan \theta_1$, where W is the width of the trench, H is the thickness of the resist, and θ_1 is the angle of incidence from the normal during the shadow evaporation. Width of upper-portion of the metal line is given by $t \sin \theta_1$, where t is the thickness of the metal if it is deposited from the normal. Linewidth from the second shadow evaporation is given by $LW_2 = W - t \sin \theta_1 - (H + t \cos \theta_1) \tan \theta_2$, where θ_2 is the angle in the second shadow evaporation. Clearly, in order to make linewidths of the two metal lines the same, the incident angle in the second evaporation should be slightly smaller than the first one. The thickness of metal lines fabricated in this way is approximately equal to the thickness of the resist. The important advantage of the double shadow-evaporations process is that the widths and the separation of

 0734-211X/90/061919-04$01.00 © 1990 American Vacuum Society

10 nm electron beam lithography and sub-50 nm overlay using a modified scanning electron microscope

P. B. Fischer and S. Y. Chou
University of Minnesota, Department of Electrical Engineering, Minneapolis, Minnesota 55455

(Received 26 October 1992; accepted for publication 17 March 1993)

Gratings of 10 nm wide metal lines 30 nm apart, and quantum transistor gates with 10 nm wide gaps over 300 nm long between two metal rectangles have been repeatedly achieved on thick GaAs substrates using a modified scanning electron microscope operated at 35 keV and liftoff of Ni/Au. Furthermore, multilevel electron beam lithography with a standard deviation (3σ) of an overlay accuracy (30 deviation) of 50 nm has been achieved using the same modified scanning electron microscope.

The desire to study the high-speed operation and quantization effects of semiconductor devices has motivated research on the fabrication of 10 nm lateral structures. For examples, lateral quantum effect devices require ultrasmall gate geometry,[1] and metal-semiconductor-metal photodetectors require extremely dense patterns of very fine interdigitated metal fingers for high performance.[2] In addition to high resolution, high overlay accuracy is another requirement in the lithography for many novel semiconductor devices. Modified scanning electron microscopes (SEMs) are an attractive tool for nanofabrication and nanodevice research due to their high resolution, high flexibility, and low cost. However, a modified SEM does not offer a direct means for high-accuracy multilevel overlay.

Previously, modified SEMs have been used to produce 10 nm wide isolated lines and gratings of 40 nm period with 12 nm linewidth on membranes,[3] as well as 10 nm wide isolated lines and gratings of 40 nm period with 10 nm linewidths on bulk GaAs substrates using a 250 keV beam exposure and chemically assisted ion beam etching with polymethyl methacrylate (PMMA) as an etch mask.[4] However, little work has been reported on ultrahigh overlay accuracy in multilevel e-beam lithography using a modified SEM.

This letter presents the study of lithographic resolution as well as overlay capability of a modified SEM operated at 35 kV. Using a liftoff technique with PMMA resists, 10 nm metal features, either isolated or periodic with periods as small as 40 nm, have been consistently achieved on bulk GaAs substrates. A liftoff process is used because it is more difficult and challenging to achieve nanostructures than etching with a PMMA etch mask. Moreover, sub-50 nm overlay accuracy has been accomplished.

In order to achieve ultrasmall structures in PMMA, the exposure of the resist by backscattered and laterally scattered electrons must be minimized. This can be accomplished by using thin resists and relatively small exposure areas. In our experiment, GaAs wafers were coated with a 45 nm thick layer of 950 K PMMA by spinning a 1.6% solution of 950 K PMMA (in chlorobenzene) at 6.0 krpm for 60 s. The samples were then baked for 12 h at 165 °C. Our e-beam lithography system consists of a modified JEOL-840A SEM with a tungsten filament gun and equipped with a magnetic beam blanking unit and electronic rotation system. The writing field can vary from 3×4 μm to 150×250 μm by selecting different magnifications of the microscope. A personal-computer controlled pattern generator is used to control the SEM. The pattern generator was designed and built in house, utilizes a commercial computer-aided design package for pattern specification, and offers a digital-to-analog converter resolution of up to 14 bits. Several measures have been taken to reduce noise from floor vibrations and electronics. High resolution exposures are performed using a field size of 34×26 μm^2, and DAC resolution of $2^{12}\times2^{12}$ pixels.

Exposures were performed with an accelerating voltage of 35 kV, and a beam diameter of about 4 nm. In order to achieve ultra-small features, a high contrast developer-resist system was used. Development was done at 23 °C using 2-ethoxyethanol:methanol (3:7) for 7 s, methanol for 10 s, and isopropanol for 30 s. The contrast of this development process for 950 K PMMA has been measured to be seven. After development, metals were deposited by e-beam evaporation. Liftoff was performed by alternately soaking in warm acetone and spraying with a pressurized acetone jet.

Both isolated and densely spaced patterns with 10 nm features have been obtained. Figure 1 shows a scanning electron micrograph of a 40 nm period grating with 10 nm linewidths on bulk GaAs. In this particular example only 3.5 nm of Ni and 4 nm of Au have been used, but liftoff is still possible with total metal thicknesses of 20 nm. The exposure dose for the grating was 0.9 nC/cm and must be carefully controlled. The exposure area is 2 $\mu m\times1.3$ μm and the liftoff was successful over the entire area. Gratings with a period smaller than 40 nm were patterned in PMMA, but did not liftoff properly.

Figure 2 shows a scanning electron micrograph of a Ni/Au (7 nm/8 nm) constricted gate for a quantum field-effect transistor with a gap of 10 nm and a gate length of 330 nm on bulk GaAs. The constricted gate was exposed with a dose of 480 $\mu C/cm^2$. This demonstrates that not only 10 nm lines but also 10 nm spaces can be achieved using a modified SEM operated at 35 kV with liftoff techniques.

To use the modified SEM to achieve high overlay accuracy, we selected a writing field size of 12×9.3 μm^2, corresponding to a SEM magnification of 10 K. The writ-

 0003-6951/93/232989-03$06.00 © 1993 American Institute of Physics

Sub-50 nm high aspect-ratio silicon pillars, ridges, and trenches fabricated using ultrahigh resolution electron beam lithography and reactive ion etching

P. B. Fischer and S. Y. Chou
University of Minnesota Department of Electrical Engineering, Minneapolis, Minnesota 55455

(Received 29 July 1992; accepted for publication 24 December 1992)

We present the fabrication of sub-50 nm Si pillars, ridges, and trenches with aspect ratios greater than 10 using ultrahigh resolution electron beam lithography and chlorine based reactive ion etching. These nanoscale Si features can be further reduced to 10 nm using an additional HF wet etch. No photoluminescence was observed from arrays of 10 nm Si structures passivated with HF.

The ability to etch nanoscale features in Si is of great interest for trench isolation[1] and trench capacitors[2] in very large scale integrated circuits and for novel quantum effect Si devices. Another attractive aspect for nanoscale Si structures is to study possible light emission which has been observed in porous Si.[3] Techniques such as wet chemical etching are not suitable for etching nanoscale, high aspect-ratio Si structures due to undercutting of the mask and sloped sidewalls. Chlorine based reactive ion etching (RIE), however, is well suited for etching nanoscale Si features with good control of undercutting and etch profiles.[4]

Previous letters have addressed various aspects of Cl-based RIE of Si such as: the role of chemistry in highly anisotropic Si trench etching,[1] elimination of mask undercutting,[4] mechanisms leading to RIE etch lag,[5] and the relationship between the RIE process and physical and electrical trench capacitor characteristics.[6] Light emission studies have been performed on Si nanostructures prepared using wet chemical dissolution[3,7] and sputter deposition[8] techniques. This letter focuses on the minimum achievable feature sizes in Si using Cl-based RIE. It also reports the preliminary results of a photoluminescence (PL) study of these Si nanostructures. We found that with an optimized composition of Cl_2 and $SiCl_4$, we can readily and repeatedly achieve sub-50 nm diam pillars 500 nm high at a pitch of 100 nm and gratings with a spacing of 30 nm and a linewidth of 50 nm which are 500 nm deep. Subsequent wet etching in HF was used to remove the Si skin damaged during the RIE process and to passivate the surface. No PL was observed in these structures.

The starting Si wafers, *p* type with a 10 Ω cm resistivity and a (100) orientation, were first cleaned using H_2SO_4:H_2O_2:H_2O (1:1:5) for 10 min at 120 °C, DI rinse for 5 min, and buffered HF:H_2O (1:9) for 30 s. Then, a layer of 950 K molecular weight poly-methyl-methacrylate (PMMA), 70 nm thick, was spun on the sample and baked at 165 °C for 12 h. Arrays of dots and lines were exposed in the PMMA using a modified JEOL-840A SEM, described elsewhere,[9] and developed in a mixture of 2-ethoxyethanol and methanol. Cr, 50 nm thick, was then deposited via electron beam evaporation at a rate of 0.1 nm/s. A lift-off process left arrays of Cr dots and lines on the Si wafers, which were used as the mask for RIE. Final surface cleaning, prior to RIE, consisted of an O_2 plasma etch and an HF dip.

RIE was performed using a Plasma-Therm parallel plate RIE system operated at 13.56 MHz. A variety of recipes consisting of Cl_2, $SiCl_4$, and He gases were tested. Chlorine was used because it has been shown to produce vertical sidewalls[4] due to the ion assisted etching mechanism,[10] but has the drawback of producing trenches in the bottom corners. $SiCl_4$ and He were added to control trench formation by simultaneous redeposition.[11] Prior to etching, the chamber was always cleaned for 10 min with an Ar plasma and then preconditioned for 10 min using the same etching recipe that was to be used. After inserting the sample, the chamber was pumped below 2×10^{-5} Torr.

All samples were etched with the same Cl_2 and $SiCl_4$ flow rates, 76.6 and 13.3 sccm respectively, a power density of 0.32 W/cm^2, and a pressure of 40 mTorr. These parameters were found to produce the sidewall profiles necessary for high aspect ratio nanoscale features without trenching at the bottom corners. The He flow rate was varied from 0 to 60 sccm to further optimize the etch parameters. After etching, the samples were analyzed using high-resolution scanning electron microscopy.

Previously, when etching with Cl_2 chemistries, the formation of roughened Si surfaces, "black Si," was reported.[4,12] The appearance of black Si has been attributed to the presence of SiO_2 micromasks. Maluf *et al.*,[13] also using mixtures of Cl_2, $SiCl_4$, and He, only observed black Si with high He flow rates. We found that proper cleaning of the sample and chamber resulted in relatively smooth surfaces with profile variations of 10–30 nm. Etched Si surfaces were typically light brown in color.

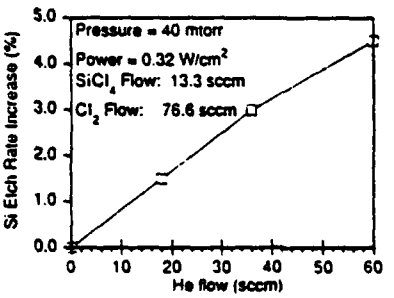

FIG. 1. Percent increase in Si etch rate vs He flow.

 0003-6951/93/121414-03$06.00 © 1993 American Institute of Physics

Engineering sub-50 nm quantum effect devices and single-electron transistors using electron-beam lithography

Yun Wang and Stephen Y. Chou
Electrical Engineering Department, University of Minnesota, Minneapolis, Minnesota 55455

(Received 2 July 1992; accepted 31 July 1992)

Fabrication and characteristics of various nanoscale quantum and single-electron devices are described. Using high-resolution electron beam lithography and double layer PMMA resist, we have successfully fabricated a 20 nm split-gate device, a novel 50 nm single barrier single-electron transistor, and a 75 nm triple barrier tunneling device. Effects of beam dose and the number of writing passes on the actual lithography pattern were investigated for various device gate geometries. Pronounced quantum and single-electron effects have been observed in these devices.

I. INTRODUCTION

New devices based on quantum or single-electron effects are opening up a fascinating new field of research thanks to advances in nanofabrication technology. In particular, devices using field-effect induced lateral confinement in combination with vertical confinement in semiconductor heterostructures have attracted much attention because they are very flexible in changing the confinement size and electron concentrations.[1,2] One of the requirements as well as the challenges in fabricating these field-induced nanodevices is to make the device size as small as possible since generally the smaller the size of the devices, the larger the quantum and single-electron effects will be. In this article, we report the fabrication of various nanoscale quantum effect and single-electron effect devices using a custom-built high-resolution electron beam lithography (EBL) system. These devices include a 20 nm split-gate field-effect transistor (FET), a 50 nm single barrier field-effect transistor (SBFET), and a 75 nm triple barrier field-effect transistor (TBFET). We show that the size of these devices can be well controlled by suitable choice of e-beam exposure dose. Pronounced quantum and single-electron effects have been observed in these devices.

Split-gate FETs have been widely used to study ballistic electron transport in a one-dimensional (1D) wire over the past several years.[3] The 1D wire is created at the AlGaAs/GaAs interface when the electrons beneath the negatively biased split gate are depleted. A SBFET has a structure similar to a split-gate FET except that an extra metal bar is placed inside the gap of the split gate. The metal bar that induces a potential barrier inside the 1D wire, together with the source-drain bias, can trap electrons in a triangular potential well. Due to coulomb repulsion, the trapped electrons will block the source-drain current.[4] A TBFET consists of three metal bars inside the gate gap. In such a device, both single electron charging effects and resonant tunneling exist.

II. FABRICATION

All of the devices were fabricated on an AlGaAs/GaAs heterostructure grown by molecular-beam epitaxy (MBE), which has a 500 nm thick undoped GaAs layer on top of a semi-insulating GaAs substrate, a 10 nm undoped $Al_{0.3}Ga_{0.7}As$ spacer layer, a 40 nm $Al_{0.3}Ga_{0.7}As$ layer with Si doping concentration of 1×10^{18} cm^{-3}, and 15 nm GaAs cap layer with Si doping concentration of 1.4×10^{18} cm^{-3}. The two-dimensional electron gas (2DEG) formed at the GaAs/AlGaAs interface has a Hall mobility of 12 m^2/V s and a carrier concentration of 8.9×10^{11} cm^{-2} at 77 K in the dark.

The fabrication process consists of four steps: mesa isolation using wet etch, formation of source and drain ohmic contacts, nanoscale gate fabrication, and final metallization for bonding pads. The critical part of the fabrication is the nanogate definition which is performed using EBL followed by a lift-off process.[5] A double layer resist scheme consisting of a 2% 950 K PMMA layer on top of a 3% 100 K PMMA layer was used. Each layer was spun at 7000 rpm for 1 min and baked at 168 °C for at least 10 h. The total PMMA thickness is about 110 nm measured using an ellipsometer. The main reason for using bilayer resist is to reduce the effect of electron backscattering and to produce a desirable undercut profile in the resist for easy lift-off. However, the undercut in bilayer resist may also have some adverse effects when the gap of a split gate becomes very narrow as will be discussed later.

The EBL system consists of a modified scanning electron microscope, JEOL-840A, and a custom pattern generator designed and built in-house.[5] The electron accelerating voltage used for EBL is 35 keV, and the beam diameter is about 3 nm. After e-beam exposure, the PMMA was developed in 3:7 cellosolve:methanol followed by a methanol rinse. The gate electrodes were formed by lift-off of e-beam evaporated Ti/Au (10 nm/20 nm).

A. Split-gate FET with 20 nm gate gap

The gate of the split-gate FET was defined using e-beam exposure of two long rectangles separated by a small gap in PMMA. After development, the width of a narrow PMMA line between two developed rectangles determines the gap width of the split gates. Due to the proximity effect and the finite resist contrast, the actual gate gap width, W_a, achieved after lift-off will be different from the nominal gate gap width W_n, defined by the e-beam pattern generator. In order to reliably obtain desired nanoscale gate gap

 0734-211X/92/062962-04$01.00 ©1992 American Vacuum Society

Single-electron Coulomb blockade in a nanometer field-effect transistor with a single barrier

Stephen Y. Chou and Yun Wang
Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

(Received 5 September 1991; accepted for publication 13 July 1992)

The first experimental study of a new nanometer field-effect transistor with a single barrier in its one-dimensional channel is presented. At low temperatures and as charge density in the channel was varied, nine reproducible periodic oscillations of conductance, in addition to $2e^2/h$ conductance plateaus, were observed before the onset of the first $2e^2/h$ conductance plateau. It was found experimentally that each conductance oscillation corresponds to the Coulomb blockade of a single electron in the one-dimensional channel. A model that describes the operation of the new single electron transistor is suggested.

As the size of semiconductor devices continues to shrink, their capacitance may decrease to a point where the effects of single electron charging significantly affect device operation. Such Coulomb effects are not only interesting in physics, but also open up new possibilities for new electronic devices. Previously, the effects of single electron charging have been studied in metal films consisting of small metal particles[1] and in small metal junctions.[2,3] In some of these structures, conductance oscillations, although weak, were observed and explained as a result of single electron charging. In semiconductor devices, single electron Coulomb blockade in a field-effect transistor (FET) that has a quantum well confined between two barriers was reported.[4] In all previous single electron charging experiments, two or more barriers were used to retain a single electron. Such a structure was believed to be critical to single electron charging.

Here, we present the first experimental study of a nanometer FET with a *single* barrier in its one-dimensional channel and suggest a model for its operation. We report observing, in addition to $2e^2/h$ conductance plateaus, nine reproducible periodic conductance oscillations before the onset of the first $2e^2/h$ plateau, and we show that these oscillations are due to the Coulomb blockade of a single electron.

The single-barrier nanometer FET has a structure similar to a constricted-gate FET (also called split-gate FET in some literature), except that a metal barrier is placed in the middle of the gate gap. Using a negative gate bias, the electrons underneath the gate will be depleted, creating two one-dimensional (1D) channels separated by a single potential barrier [Fig. 1]. The gate was fabricated using ultrahigh resolution electron beam lithography and a liftoff process.[5] The width of the metal barrier and the gap between the two constricted gates were as small as 50 nm (Fig. 2). The single-barrier FET (SBFET) has a heterostructure, grown by MBE, consisting of a 500 nm thick layer of undoped GaAs on top of a semi-insulating GaAs substrate, followed by a 10 nm undoped $Al_{0.3}Ga_{0.7}As$ spacer layer, a 40 nm $Al_{0.3}Ga_{0.7}As$ layer doped with a Si concentration of 1×10^{18} cm^{-3}, and a 15 nm GaAs cap layer with a Si doping concentration of 1.4×10^{18} cm^{-3}. The two-dimensional electron gas (2DEG) formed at the GaAs/AlGaAs interface had a Hall mobility of 120 000 cm^2/V s and a carrier concentration of 8.9×10^{11} cm^{-2} at 77 K in the dark. For comparison, constricted-gate FETs without any barriers were also fabricated on the same substrate.

The devices were cooled to 0.5 K using a sorption-pumped helium−3 refrigerator. Before cooling to 0.5 K, the devices were illuminated by a light-emitting diode (LED) at 10 K and were found to hold a constant 2DEG concentration at 0.5 K for hours. As the gate voltage was scanned, a SBFET with a 50 nm gate gap and a 50 nm wide metal bar showed nine repeatable periodic oscillation peaks in the drain current, in addition to $2e^2/h$ conductance plateaus, before the onset of the first $2e^2/h$ conductance plateau (Fig. 3). The oscillation period was 15 mV. Another SBFET with a 100 nm gate gap and a 50 nm wide metal bar showed five repeatable periodic oscillation peaks in the drain current with a periodicity of 9 mV before the onset of the first $2e^2/h$ conductance plateau (Fig. 4). Such periodic conductance oscillation peaks were absent when the conductance of these devices was greater than $2e^2/h$. They were also absent in the devices that were fabricated on the same substrate but had a straight constricted gate of the same size without any barrier.

Interestingly, the conductance oscillations in Fig. 4, measured with a direct *I-V* measurement using HP4145 semiconductor parameter analyzer, are much stronger than those in Fig. 3, which are measured with a lockin

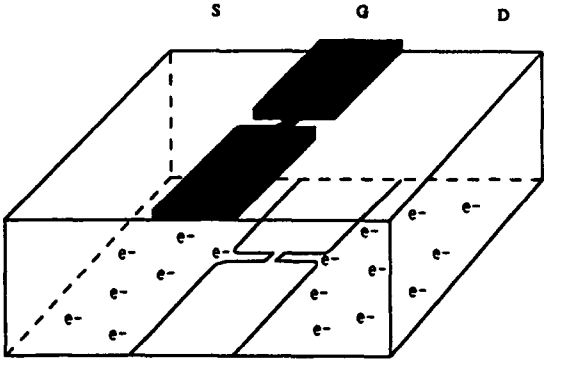

FIG. 1. Schematic of 2DEG in a nanometer FET with a 1D channel and a single barrier in the middle.

 0003-6951/92/381591-03$03.00 © 1992 American Institute of Physics

Fabrication of sub-50 nm finger spacing and width high-speed metal–semiconductor–metal photodetectors using high-resolution electron beam lithography and molecular beam epitaxy

Stephen Y. Chou, Yue Liu, and Paul B. Fischer
Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

(Received 30 May 1991; accepted 15 July 1991)

Using high-resolution electron beam lithography, we have fabricated metal–semiconductor–metal photodetectors with sub-50 nm finger spacing and finger width on GaAs grown by molecular beam epitaxy, which are, to our knowledge, the smallest ever reported. Direct-current measurements showed that they have low dark current and high sensitivity. Proper scaling of the detectors to reduce the finger resistance and detector capacitance and to increase detector speed was studied. The resistances of thin metal lines with various widths were measured and compared with the value calculated from resistivity for bulk metal. Monte Carlo simulation demonstrates that for the photodetectors with 30 nm finger spacing and width, the response time is below picosecond and the cut-off frequency is over 1 THz.

I. INTRODUCTION

Metal–semiconductor–metal (MSM) photodetectors are very attractive for optical-fiber communication systems and high-speed chip-to-chip connections.[1–4] MSM photodetectors have several advantages over *p-i-n* photodiodes,[5] such as higher sensitivity-bandwidth product, simple fabrication, and compatibility with large-scale field-effect transistor (FET) integrated circuit technology. The operation of a MSM photodetector can be classified into two groups: recombination time limited or transit time limited. In the first group, the semiconductor must be heavily damaged to shorten carrier recombination time for high-speed operation at the expense of low sensitivity and less compatibility with FET integrated circuits fabrication. In the latter group, small finger spacing is utilized to decrease carrier transit time and increase device speed. Therefore, the photodetector has very high sensitivity-bandwidth product (about two orders of magnitude higher than recombination limited detectors) and can be built on high-quality semiconductor crystals. For ultrahigh-speed applications, it is very desirable to make spacing and width of interdigitated metal fingers of a transit time-limited MSM photodetector small.[6–8] The smaller the spacing, the shorter the intrinsic response time of the MSM photodetector; the smaller the finger widths, the less the detector capacitance and the shorter the external response time.

Previously, MSM photodetectors with finger spacing and width greater than 0.5 μm have been reported.[2,7–10] The fastest GaAs MSM photodetector was fabricated by Van Zeghbroeck *et al.*[10]; it has a finger spacing of 0.5 μm and a finger width of 0.75 μm, a full width at half maximum (FWHM) of 4.8 ps, and an overall bandwidth of 105 GHz.

In this paper, we report on the fabrication of MSM photodetectors with finger spacing and finger width smaller than 50 nm, which are, to our knowledge, the smallest ever reported. The active GaAs layer is grown by molecular beam epitaxy, and the metal interdigitated electrodes are patterned by a high-resolution electron beam epitaxy. The dc measurements show that the devices have a low dark current (<40 nA at 0.5 V bias) and a high sensitivity (0.2 A/W). We also discuss the influence of finger resistance and device capacitance on high-speed operation.

II. FABRICATION

The MSM photodetector is shown schematically in Fig. 1. The devices were fabricated on a 0.4-μm-thick undoped GaAs layer grown, using molecular beam epitaxy (MBE), on a semi-insulating GaAs substrate with an AlGaAs/GaAs superlattice in between. The superlattice is for preventing carriers generated in the substrate from entering the undoped active layer. The undoped layer is kept thin for reducing carrier transit time and increasing device speed. This may degrade the device sensitivity, however, when the active layer thickness becomes less than the characteristic light absorption length. For some high sensitivity applications, an AlGaAs/GaAs quarter-wave-stack reflector can be fabricated between the active layer and the substrate. The reflector plus an antireflection coating of the metal surface can improve the detector sensitivity drastically.

The metal (Ti/Au) Schottky barrier contacts were fabricated on GaAs by using electron beam lithography and a

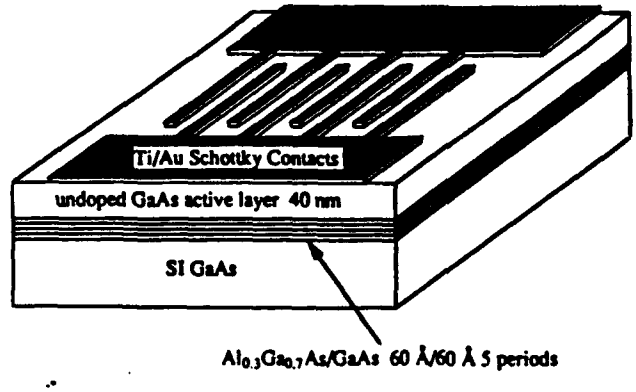

FIG. 1. Schematic view of a MSM photodetector. The pitch is equal to the addition of finger spacing and width.

 0734-211X/91/062920-05$01.00 © 1991 American Vacuum Society

Nanoscale metal–semiconductor–metal photodetectors with subpicosecond response time fabricated using electron beam lithography

M. Y. Liu and S. Y. Chou
Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

T. Y. Hsiang, S. Alexandrou, and R. Sobolewski
Department of Electrical Engineering, University of Rochester, Rochester, New York 14627

(Received 27 May 1992; accepted 24 July 1992)

Metal–semiconductor–metal photodetectors (MSM PDs) with finger spacing and width as small as 25 nm have been fabricated using high-resolution electron beam lithography. Measurements using an electro-optic sampling system show that the fastest detector has a full width at half-maximum response time of 0.87 ps and a 3 dB bandwidth of 510 GHz. Monte Carlo simulation of detector response time is studied and compared with experimental data. Finally, scaling rules for high-speed MSM PDs are proposed.

I. INTRODUCTION

Recently, much progress has been made in high-speed metal–semiconductor–metal photodetectors (MSM PDs), since they are very attractive for optical communication, future high-speed chip-to-chip connection, and high-speed sampling.[1–9] MSM PDs can be classified according to whether their speed is intrinsically limited by the carrier transit time between the fingers or the carrier recombination time. Certainly, the speed of the detectors will be limited by the R–C time constant if it is larger than the transit time or the recombination time. Usually, transit-time-limited detectors are fabricated on high-quality semiconductors and have a sensitivity several orders of magnitude higher than that of recombination-time-limited MSM PDs. However, in the past, the transit-time-limited MSM PDs generally were much slower than the recombination-time-limited MSM PDs, because it was difficult to fabricate small fingers.

As fabrication technology advances, the finger spacing of a MSM PD can be reduced to nanometer scale. The smaller the finger spacing, the shorter the intrinsic response time for the transit-time-limited MSM PDs, and the higher the sensitivity for the recombination-time-limited MSM PDs. Therefore, the difference in speed and sensitivity between the transit-time-limited and recombination-time-limited MSM PDs is getting smaller. Furthermore, the finger width is another important factor for high-speed MSM PDs. The narrower the finger width, the less the detector capacitance and the shorter the external response time.

Previously, the fastest transit-time-limited GaAs MSM PD reported has a finger width of 0.75 μm and finger spacing of 0.5 μm, an impulse response of 4.8 ps full width at half-maximum (FWHM), and a 3 dB bandwidth of 105 GHz.[4] The fastest recombination-time-limited MSM PD on low-temperature (LT) grown GaAs reported previously had a finger width and spacing of 0.2 μm, a FWHM of 1.2 ps, and a 3 dB bandwidth of 375 GHz.[6] The fastest MSM PD on crystalline silicon reported previously had a 4 μm single gap and a 3 dB bandwidth of 22 GHz.[7]

In this article, the fabrication of MSM PDs with finger spacing and width as small as 25 nm on bulk and LT GaAs, and crystalline Si is reported. Monte Carlo simulation of the impulse response of nanoscale MSM PDs and scaling rules for high-speed MSM PDs is presented. Finally, the subpicosecond characterization of the nanoscale MSM PDs is reported.

II. FABRICATION

Three different substrates were studied: bulk GaAs, LT GaAs, and crystalline silicon. The bulk GaAs substrate is semi-insulating (SI) GaAs with a carrier concentration of $\sim 1.5\times 10^7$ cm^{-3}, electron mobility of 6500 cm^2/V s, and resistivity of 5×10^7 Ω cm. The LT GaAs was 1 μm thick and grown at 210 °C and annealed at 600 °C for 1 h. The Si substrate was p-type with a doping concentration of 8×10^{14} cm^{-3}.

For high-speed measurements, the detectors were fabricated with coplanar striplines of Ti/Au (50 nm/200 nm thick) with a linewidth of 16 μm, a spacing of 9 μm, and a characteristic impedance of 75 Ω. The transmission lines and alignment marks for electron beam lithography (EBL) were defined using photolithography and lift-off. The nanoscale MSM PDs were fabricated using EBL and a lift-off technique. The fabrication steps consist of electron beam resist coating, direct electron beam writing, development, metal evaporation, and a lift-off process. First, polymethymethacrylate (PMMA) was spun on the substrate. For MSM PDs with finger pitch smaller than 200 nm, a single layer PMMA with thickness from 40 to 70 nm was used; for finger pitch greater than 200 nm, double layer PMMA was used, with a 70 nm thick layer of 100 K molecular weight PMMA on the bottom, and a 70 nm thick layer of 950 K molecular weight PMMA on the top. The double layer scheme is designed to achieve undercut in the resist for easier lift-off. Each layer of PMMA was baked at 160 °C for over 12 h after spinning. Interdigitated line patterns were exposed in the resist using a custom-built high-resolution EBL system converted from a JEOL-840 scanning electron microscope operated at 35 kV.[10] The exposed PMMA was developed in 2-Ethoxyethanol: methanol (3:7 by volume). After exposure and develop-

 0734-211X/92/062932-04$01.00 ©1992 American Vacuum Society

Tera-hertz GaAs metal-semiconductor-metal photodetectors with 25 nm finger spacing and finger width

S. Y. Chou, Y. Liu, and P. B. Fischer
Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

(Received 2 May 1991; accepted for publication 5 May 1992)

We have fabricated metal-semiconductor-metal (MSM) photodetectors with the smallest finger spacing and finger width of 25 nm on molecular beam epitaxy grown GaAs. Direct current measurement shows that they have low dark current and high sensitivity. Monte Carlo simulations demonstrate that for a MSM photodetector with 25 nm finger spacing and width, the full width at half maximum impulse response is as short as 0.25 ps and the 3 dB bandwidth is 0.4 THz. They also show that by eliminating holes, the bandwidth can be over 1.8 THz. Furthermore, the detector capacitance was calculated, indicating that by reducing the ratio of finger width to finger spacing the detector capacitance can be decreased.

Metal-semiconductor-metal (MSM) photodetectors are very attractive for optical fiber communication systems and high-speed chip-to-chip connections.[1] The operation of a MSM photodetector can be classified into two groups according to whether its intrinsic speed is limited by recombination time or transit time. In the first group, a large number of recombination centers have to be introduced into the semiconductor to shorten carrier recombination time for high-speed operation at the expense of low sensitivity and less compatibility with field effect transistor (FET) integrated circuits fabrication. In the latter group, small finger spacing is utilized to decrease the transit time and increase the device speed; therefore, the photodetector can be built on high-quality semiconductor crystals.[2,3] For ultrahigh-speed applications, it is very desirable to make both the spacing and the width of the interdigitated metal fingers of a transit-time-limited MSM photodetector small. The smaller the spacing, the shorter the intrinsic response time of the MSM photodetector, the smaller the finger width, the less the detector capacitance and the shorter the external response time. Furthermore, for the recombination-time-limited photodetectors, smaller finger spacing can increase the sensitivity.

Previously, the fastest transit-time-limited GaAs MSM photodetector, fabricated by Van Zeghbroeck *et al.*,[2] had a finger spacing of 0.5 μm and a finger width of 0.75 μm, a full width at half-maximum (FWHM) of 4.8 ps, and a bandwidth of 105 GHz. In this letter, we report fabrication of GaAs MSM photodetectors with finger spacing and finger width of 25 nm, which are, to our knowledge, the smallest ever reported. The dc characteristics show that the devices have a low dark current (<40 nA) and a high sensitivity (0.2 A/W). Monte Carlo simulations of the MSM photodetectors indicate a subpicosecond response time and a tera-hertz bandwidth.

The MSM photodetectors were fabricated on a 0.4 μm thick undoped GaAs layer grown, using molecular beam epitaxy (MBE), on a semi-insulating GaAs substrate with an AlGaAs/GaAs superlattice in between. The superlattice is for preventing carriers generated in the substrate from entering the undoped active layer. The metal (Ti/Au) Schottky barrier contacts were fabricated on GaAs by using electron beam lithography and a liftoff technique. For finger spacing and width greater than 100 nm, two layers of polymethylmethacrylate (PMMA) were spun on the GaAs layer for achieving a good undercut profile suitable for the liftoff. For finger spacing and width less than 100 nm, a single layer PMMA was used. Interdigitated line patterns were exposed in the resists using a high-resolution electron beam lithography system at a beam energy of 35 keV, and developed in cellosolve:methanol (3:7) developer.[4] Metals (Ti/Au) were then evaporated onto the samples and were lifted-off in acetone. Figure 1 shows scanning electron micrographs of MSM photodetectors with different finger structures, and the smallest finger spacing and width are 25 nm.

The dc characteristics of a GaAs MSM photodetector are shown in Fig. 2. The dark current of the photodetectors is typically 40 nA at 0.5 V bias for area of 14.5 μm$\times$15 μm. The sensitivity of the devices is about 0.2 A/W at the wavelength of 632.8 nm. The current-voltage characteristics do not show perfect saturation because of the surface recombination centers.

A Monte Carlo simulation program has been developed for calculating the carrier transit time. In the simulation, electric field is assumed to be one-dimensional and uniform in the semiconductor. The one-dimensional (1D) model is a good approximation since the electric field lines are mostly localized near the semiconductor interface.[5] Recently, femtosecond testing of nanoscale MSM photodetectors on bulk semiconductors showed that the carriers generated in the bulk of a semiconductor are insignificant to the FWHM of impulse response of the detectors, and that the 1D simulation is valid even when the finger spacing is much smaller than the thickness of absorption length.[6]

Figure 3 shows the Monte Carlo simulation of the intrinsic current of a MSM photodetector with 25 nm spacing and width, and the external current after introducing the capacitance of the detector and the load resistance. It indicates that for a 25-nm-finger-spacing MSM photodetector, the FWHM of intrinsic response is 0.16 ps, and the FWHM external response is 0.25 ps. By separating the electrons from holes, we found that the current peak is due to the electrons and the long tail is due to holes which

 0003-6951/92/290477-03$03.00 © 1992 American Institute of Physics

Nanoscale Tera-Hertz Metal-Semiconductor-Metal Photodetectors

Stephen Y. Chou, *Member, IEEE*, and Mark Y. Liu, *Student Member, IEEE*

Abstract—**Metal-semiconductor-metal photodetectors (MSM PD's) with finger spacing and width as small as 25 nm were fabricated on bulk and low-temperature (LT) grown GaAs and crystalline Si using ultrahigh resolution electron-beam lithography. High-speed electrooptic characterization with a 100 fs pulsed laser showed that the fastest MSM PD's had finger spacing and width, full width at half maximum response time, and 3 dB bandwidth, respectively, of 300 nm, 0.87 ps, and 0.51 THz for LT-GaAs; 100 nm, 1.5 ps, and 0.3 THz for bulk GaAs; and 100 nm, 10.7 ps, and 41 GHz for crystalline Si. To our knowledge, these detectors are the fastest nanoscale MSM PD's on each of these materials reported to date. Monte Carlo simulation was used to understand the impulse response of the MSM PD's and to explore the ultimate speed limitation of transit-time-limited MSM PD's on GaAs and Si. Factors that are important to detector capacitance were identified using a conformal mapping method. Based on the experimental data, Monte Carlo simulation, and calculation of detector capacitance, scaling rules for achieving high-speed MSM PD's are presented.**

I. Introduction

METAL-SEMICONDUCTOR-METAL photodetectors (MSM PD's) are very attractive for many optoelectronic applications, such as optical communication, future high-speed chip-to-chip connection, and high-speed sampling, because of their high sensitivity-bandwidth product and their compatibility with large-scale planar integrated circuit (IC) technology. A MSM PD consists of interdigitated metal fingers on a semiconductor, and it detects photons by collecting electric signals generated by photoexcited electrons and holes in the semiconductor that drift under the electrical field applied between the fingers (Fig. 1). MSM PD's can be classified according to whether their speed is intrinsically limited by the carrier transit time between the fingers or the carrier recombination time. Certainly, the speed of the detector will be limited by the *RC* time constant if it is longer than the transit time or the recombination time. Usually, transit-time-limited detectors are fabricated on high-quality semiconductors and have a sensitivity several orders of magnitude higher than that of recombination-time-limited MSM PD's. Furthermore, their fabrication technology is very compatible with field effect transistor (FET) fabrication. In the past, however, transit-time-limited MSM PD's generally were much slower than recombination-time-limited MSM PD's, because it used to be difficult to make the finger spacing small. In recombination-time-limited MSM PD's, shorter recombination time and therefore higher speed are achieved through introducing high-density recombination centers into the semiconductor. This drastically lowers sensitivity and makes fabrication less compatible with FET IC fabrication.

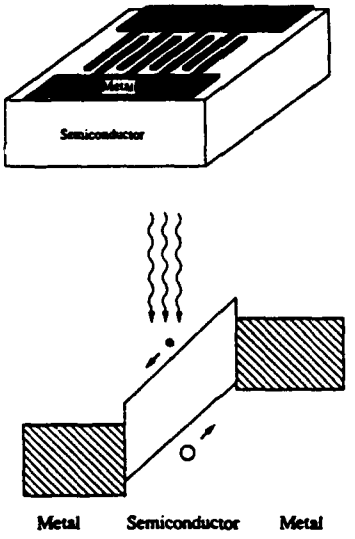

Fig. 1. Schematic view and band diagram of a MSM photodetector.

As fabrication technology advances, the finger spacing of a MSM PD can be reduced to nanometer scale. The smaller the finger spacing, the shorter the intrinsic response time for the transit-time-limited MSM PD's and the higher the sensitivity for the recombination-time-limited MSM PD's. Therefore, the difference in speed and sensitivity between the transit-time-limited and recombination-time-limited MSM PD's is getting smaller. As shown later, the finger width is another important factor for high-speed MSM PD's. The narrower the finger width, the less the detector capacitance per unit finger length and the shorter the external response time.

The study of MSM structures emerged in early 1970's [1], [2]. In 1975, recombination-time-limited MSM PD's on Cr doped GaAsCr substrates achieved an impulse response of 92 ps [3]. In the early 1980's, MSM PD's on amorphous silicon showed impulse response of a few pi-

Manuscript received February 18, 1992; revised June 16, 1992. This work was supported in part by the Packard Foundation through Packard Fellowship, by IBM through IBM Faculty Development Award, by the Army Research office under Contract DAAL03-90-0058, and the National Science Foundation by Grant ECS-9120527.

The authors are with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455.

IEEE Log Number 9202627.

0018-9197/92$03.00 © 1992 IEEE

Ultrafast nanoscale metal-semiconductor-metal photodetectors on bulk and low-temperature grown GaAs

S. Y. Chou, Y. Liu, and W. Khalil
Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

T. Y. Hsiang and S. Alexandrou
Department of Electrical Engineering, University of Rochester, Rochester, New York, 14627

(Received 28 February 1992; accepted for publication 16 June 1992)

Metal-semiconductor-metal photodetectors of finger spacing and width as small as 100 nm have been fabricated on bulk and low-temperature grown GaAs, and tested using a femtosecond pulse laser and high-speed electro-optic sampling. The fastest photodetectors have a measured full width at half maximum impulse response and a 3-dB bandwidth of 0.87 ps and 510 GHz, respectively, for low-temperature grown GaAs limited by carrier recombination time; and of 1.5 ps and 295 GHz for bulk GaAs, limited by the RC time constant. To our knowledge, they are the fastest detectors of their kinds reported to date.

Metal-semiconductor-metal photodetectors (MSMPDs) can be classified into two types, depending on whether their speed is intrinsically limited by the carrier transit time or the carrier recombination time. However, the RC time constant of MSMPDs can become the limiting factor to the speed of the detectors of either type if it is greater than the transit time or the recombination time. Both types of MSMPDs on GaAs have been investigated by several groups.[1-6] The fastest transit time limited GaAS MSMPD reported previously had a finger width of 0.75 μm and finger spacing of 0.5 μm, an impulse response of 4.8 ps full width at half maximum (FWHM), a 3-dB bandwidth of 105 GHz.[2] The fastest recombination time limited MSMPD on low-temperature grown GaAS (LT-GaAs) reported previously had a finger width and spacing of 0.2 μm, a FWHM of 1.2 ps and 3-dB bandwidth of 375 GHz.[6]

For ultra-high-speed applications, it is very desirable to minimize both finger spacing and width. The smaller the spacing, the shorter the intrinsic response time of the transit time limited MSMPDs and the higher the sensitivity of the recombination time limited MSMPDs; the smaller the finger width, the smaller the detector capacitance, leading to a smaller RC constant.[7]

In this letter, we report MSM photodetectors with nanoscale finger spacing and width, fabricated on bulk GaAs and LT-GaAs, that have faster FWHM impulse responses and higher 3-dB bandwidths than previously reported.

We fabricated nanoscale MSMPDs on two different substrates. One is semi-insulating GaAs, which has a resistivity of 5×10^7 Ω cm and electron mobility of 6500 cm^2/V s. The other substrate has a 1 μm thick layer of LT-GaAs grown on SI-GaAs. The LT-GaAs was grown at 210 °C with a growth rate of 0.5 μm/h and was annealed at 600 °C for 1 h. The metal fingers of the MSMPDs were defined using electron beam lithography and a liftoff process. Polymethylmetacrylate (PMMA) was spun on the substrates and baked, then interdigitated line patterns were exposed in the resist using a custom-built high-resolution electron beam lithography system converted from a JEOL-840 scanning electron microscope at a beam energy of 35 keV.[8] After resist development, Ti and Au of a total thickness of 50 nm were deposited on the wafer and lifted off in acetone. Although we have achieved 25 nm finger spacing and width,[7] the smallest detector finger spacing and width in these experiments is 100 nm. The detector area is 10×10 μm^2 (Fig. 1). For high speed measurements, coplanar striplines with a linewidth of 16 μm, a spacing of 9 μm, and a quasistatic characteristic impedance of 75 Ω were fabricated on the substrate.

The MSMPDs were characterized using a high-speed electro-optic sampling system consisting of a 100 fs colliding pulse mode-locked dye laser with a wavelength of 620 nm and a repetition rate of 100 MHz.[9] The response of the MSMPDs was measured using a $LiTaO_3$ tip probe placed 250 μm from the detectors.

MSMPDs on LT-GaAs with different finger spacings and widths—100, 200, and 300 nm—were tested. We found that the detector with 300 nm finger spacing and width had a FWHM of 0.87 ps (Fig. 2). The 3-dB bandwidth of the detector, calculated using 0.441/(FWHM), is 510 GHz.

The impulse response time of the MSM photodetectors on LT-GaAs becomes progressively worse as the finger spacing and width become smaller; the FWHM is, respec-

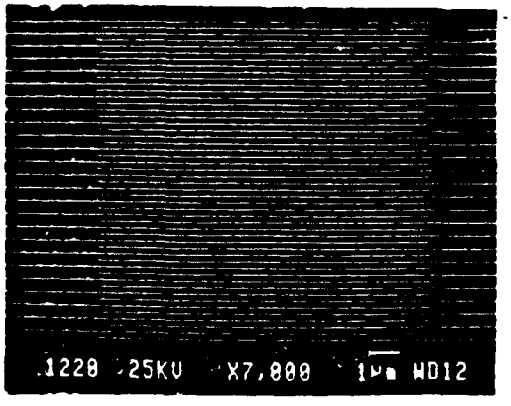

FIG. 1. Scanning electron micrograph of a MSMPD with finger spacing and width of 100 nm and an area of 10×10 μm^2.

 0003-6951/92/320819-03$03.00 © 1992 American Institute of Physics

A 75 GHz silicon metal-semiconductor-metal Schottky photodiode

Sotiris Alexandrou, Chia-Chi Wang, and Thomas Y. Hsiang
Laboratory for Laser Energetics and Department of Electrical Engineering, University of Rochester, 250 East River Road, Rochester, New York 14623-1299

M. Y. Liu and S. Y. Chou
Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

(Received 7 December 1992; accepted for publication 17 March 1993)

The ultrafast characteristics of crystalline-silicon metal-semiconductor-metal (MSM) photodiodes with 300 nm finger width and spacing were measured with a subpicosecond electro-optic sampling system. Electrical responses with full width at half maximum as short as 5.5 and 11 ps, at corresponding 3 dB bandwidths of 75 and 38 GHz, were generated by violet and red photons, respectively. The difference is attributed to the photon penetration depth which is much larger than the diode finger spacing at red, but smaller at violet. Light-intensity dependence was also examined at different wavelengths, indicating a linear relation and a higher sensitivity in the violet. These results not only demonstrated the fastest silicon photodetector reported to date, but also pinpointed the dominant speed-limiting factor of silicon MSM photodiodes. A configuration is suggested to improve the speed of these detectors at long wavelengths.

Metal-semiconductor-metal (MSM) photodiodes are a family of fast, high-sensitivity detectors. Their simple planar structures enable easy fabrication in a process compatible with planar circuit technology and are hence attractive for use in integrated optoelectronic-electronic systems. In the past, most attention was given to MSM diodes made on III-V substrates.[1-5] For example, we have reported on a range of MSM detectors made on low-temperature MBE-grown and semi-insulating GaAs with finger period as short as 100 nm.[1] These detectors had speed, measured by the full width at half maximum (FWHM) of the response transient, as fast as 0.87 ps. A comparison of our experimental results to Monte Carlo simulations demonstrated that the speed of these detectors was limited by their intrinsic *RC* time constant. Furthermore, since the underlying physical principle of ballistic transport is applicable to all semiconductors, it was inferred that comparable performance should also be achievable in silicon. Monte Carlo simulations predicted[6] a response speed as short as 6 ps FWHM for silicon MSM diodes with finger width and spacing of 300 nm.

Preliminary results on 1.2 μm and 300 nm silicon diodes,[7,8] measured with colliding pulse mode locked dye lasers (wavelength = 620 nm), however, indicated much slower response (14 and 11 ps, respectively) than the III-V compound detectors. In addition, these devices had a long "tail" response—a residual electron drift component past the main peak—as long as 1.4 ns for the 1.2 μm diodes.[7] The latter is a particularly undesirable feature for practical applications, since photoconductive current is cumulative—the device has to fully recover to its original, nonconductive state before the next optical pulse can be detected—thus limiting its use to less than 1 Gb/s. It was suggested[8] that a probable source of the slow response and the long tail is due to deep-carrier generation because of the long penetration depth of photons at wavelengths used in these experiments.

In this letter, we demonstrate that this is indeed the case. We report on the fastest photodetectors made with essentially undoped crystalline silicon, and show that by decreasing the wavelength of the excitation photons, hence reducing the light penetration depth, these diodes can have a speed close to the Monte Carlo predictions. Furthermore, at this photon wavelength, the slower drift-current component is completely eliminated. By pinpointing the speed-limiting factor of these devices, we are able to suggest a configuration for improving the temporal response of the diodes in a wide range of wavelengths.

Our MSM diodes were fabricated on unintentionally doped crystalline silicon ($p < 10^{15}$ cm^{-3} and carrier recombination time > 100 ns) using electron beam lithography. A 50-nm-thick Ti/Au metallization was chosen for the interdigitated fingers to ensure a Schottky barrier at the metal-semiconductor interface. Ten fingers with 300 nm width and separation formed a diode active area of 5×5 μm^2. The diodes were positioned in parallel to a 65 Ω coplanar transmission line, as shown in Fig. 1.

The response of the devices was tested using a subpicosecond electro-optic sampling system similar to that described in Refs. 9 and 10. Typical bias voltage across the diode was 3 V. A femtosecond Ti:Al_2O_3 laser provided tunable pulses in the red to near-infrared (700–1000 nm) range at a 76 MHz repetition rate and was used for both excitation and probing. A movable $LiTaO_3$ electro-optic crystal was positioned above the diode area (see Fig. 1) as the detector for the electrical transient. The excitation beam was focused down to the diode through the $LiTaO_3$ crystal, and the electrical signal was probed by the sampling beam guided through the electro-optic crystal in a total internal-reflection mode. This configuration allows the diode response to be measured directly with no propagation distortion.[10] At the fundamental wavelength range of the Ti:Al_2O_3 laser, the carrier penetration depth is > 5 μm, much larger than the finger spacing and, as a result, the photogenerated carriers are expected to penetrate deep into the substrate. To test the effect of the deep photoge-

 0003-6951/93/202507-03$06.00 © 1993 American Institute of Physics