AD-A280 380

I PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	4/30/94	Final 7/1/93-2/28/94

4. TITLE AND SUBTITLE
Submillimeter Quasioptical Josephson Junction Oscillator with Integrated Tuning Elements

5. FUNDING NUMBERS
F49620-93-C-0037
63218C
1602/01

6. AUTHOR(S)
Aleksandar Pance and Andrew Barfknecht

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Conductus, Inc.
969 West Maude Ave
Sunnyvale, CA 94086

8. PERFORMING ORGANIZATION REPORT NUMBER
AFOSR-TR- 94 0347
94003-SBIR-2-F

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Air Force Office of Scientific Research / NE
110 Duncan Ave Suite B115
Bolling AFB DC 20332-0001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
F49620-93-C-0037

11. SUPPLEMENTARY NOTES

DTIC
ELECTE
JUN 15 1994
S F D

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Unlimited — Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

The goal of this program was to demonstrate a Quasioptical Josephson Oscillator with Integrated Tuning Elements using standard Conductus niobium technology. This device is based on a novel approach that incorporates integrated tuning and impedance-matching structures at every Josephson junction/antenna pair. The device has been designed, fabricated and successfully tested. A new unit cell has been devised, incorporating a sub-array of 1 to 16 Josephson junctions. Microstrip transformers are used locally between each sub-array and its antenna. The oscillator with 110 Josephson junctions and bow-tie antennas was found to radiate close to its maximum available power at 115 GHz. The on-chip SIS radiation detector has detected 2.64 nW of power. The oscillator was tuned across 19 GHz, or 16% of fractional bandwidth, in reasonble agreement with the predicted value of 19%. This is the first demonstration of a distributed array Josephson oscillator, where each junction feeds its own antenna and phase-locks to the radiation of other junctions. It is also the first demonstration of using integrated microstrip tuning and impedance matching elements at every Josephson junction of an oscillator. Finally, this is the first distributed Josephson oscillator reported to date that appears to radiate close to its maximum available power.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Submillimeter, oscillators, Antenna arrays, Superconducting electronics, Quasioptical	26
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102

DTIC QUALITY INSPECTED 5

94 6 14 155

94-18491

Phase I Final Report

April 30, 1994.

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Contract #F49620-93-C0037

AFOSR-TR- 94 0347

Aleksandar Pance

Conductus, Inc.

(408) 524 9820

Report Summary

The goal of this program was to demonstrate a Quasioptical Josephson Oscillator with Integrated Tuning Elements using standard Conductus niobium technology. This device is based on a novel approach that incorporates integrated tuning and impedance-matching structures at every Josephson junction/antenna pair. The device has been designed, fabricated and successfully tested. A new unit cell has been devised, incorporating a sub-array of 1 to 15 Josephson junctions. Microstrip transformers are used locally between each sub-array and its antenna. The oscillator with 110 Josephson junctions and bow-tie antennas was found to radiate close to its maximum available power at 115 GHz. The on-chip SIS radiation detector has detected 2.64 nW of power. The oscillator was tuned across 19 GHz, or 16% of fractional bandwidth, in reasonble agreement with the predicted value of 19%. This is the first demonstration of a distributed array Josephson oscillator, where each junction feeds its own antenna and phase-locks to the radiation of other junctions. It is also the first demonstration of using integrated microstrip tuning and impedance matching elements at every Josephson junction of an oscillator. Finally, this is the first distributed Josephson oscillator reported to date that appears to radiate close to its maximum available rf power.

1. Background and Objectives

The goal of Phase I of this program was to demonstrate a Quasioptical Josephson Oscillator (QJO) based on a novel approach using Conductus' niobium technology. The concept of QJO has been introduced by Wengler [1] as a way of achieving μW power levels at submillimeter frequencies for airborne and satellite applications. Pance [2, 3] has proposed a new design that would eliminate three major problems associated with efficient implementation of the QJO:

1) tuning out the parasitic capacitances of Josephson junctions,
2) efficient power coupling to the radiation mode and
3) design robustness in the presence of scattering of the fabrication process parameters.

These tasks are accomplished by integrating every junction with a microstrip transformer that tunes out the parasitic capacitance and matches the junction impedance to the antenna impedance.

The technical objectives of Phase I were to:

1) determine the feasibility of implementing the QJO using Conductus' standard niobium technology with large-area junctions,
2) generate a number of designs to address the key design issues,
3) fabricate the QJO, and
4) perform initial proof-of-principle tests.

2. Status of Research Effort

2.1. Design feasibility

In the first phase of the program, the feasibility of the implementation of the proposed device in Conductus' Nb technology has been studied in detail. Of particular importance was the effort to use a reliable, commercially-available fabrication process [4] geared toward digital applications. In all previous implementations of Josephson oscillators [5-9], results have been achieved using very advanced processes, with small-area junctions and large critical current densities. Large-area junctions directly translate into large parasitic capacitances which severely influence the high-frequency operation of Josephson arrays. Further, design constraints imposed

by microstrip transformers needed to be determined. In particular, the feasibility study determined 1) the achievable range of microstrip impedances, 2) the minimum inductance values for Josephson junction capacitance tuning, 3) the maximum design frequency, 4) the maximum number of junctions in the array for a given chip size and 5) the maximum output power achievable with this design.

2.1.1. Microstrip impedances

The standard Conductus niobium fabrication process utilizes four Nb layers (trilayer and two wiring layers) of thicknesses 0.18 μ (base of the trilayer - S1), 0.36 μ (first wiring - S2) and 0.42 μ (second wiring - S3). The dielectric used as the insulator between the layers is SiO_2 with $\varepsilon_r = 5.1$ and with thickness of 0.35 μ (S2-S1) and 0.4 μ (S3-S2). Microstrip line (MS) can be made between any two layers. The standard process allows a minimum linewidth of 3 μ, and the advanced one a 2 μ linewidth. Table 1 lists the achievable range of microstrip impedances that can be used in integrated tuning structures. The impedances are calculated including the surface impedance of niobium. In designs, the MS line used for inductance tuning structures should not be wider than 10 μ because of a high-frequency cutoff and density considerations. These constraints translate in the usable range of microstrip impedances between 6.28 Ohm (10 μ wide, S2 on S1) and 26.43 Ohm (3 μ wide, S3 on S1).

2.1.2. Required tuning inductance and maximum operating frequency

Because of the large parasitic capacitance of our junctions (3 μ standard junction: 558 fF, 2 μ advanced junction: 248 fF, based on the measured value of 62 fF/μ2) the tuning inductance has to be very small for higher frequencies of operation. The minimum inductance is determined by the fabrication process design rules. Because of the definition of junctions through an anodization process, the standard requirement is that any structure must be at least 3 μ away from the junction (2 μ in the advanced process). Based on the 10 μ wide microstrip line S2 on S1, the minimum inductance is 0.174 pH (0.116 pH for a 2 μ long inductor in the advanced process). This determines the maximum operating frequency of 511 GHz in the standard process and 939 GHz in the advanced process (2 μ junction, 2 μ long inductor). It is also expected that a degradation in array operation will be observed above about 700 GHz, because of the onset of losses in niobium at that frequency.

2.1.3. Maximum number of junctions

The standard die size in the Conductus niobium process is 1 cm^2 with an active area usually about 8 mm X 8mm. In the Josephson array oscillator, the size of the unit cell will be of

the order of $\lambda_d/2$ at the operating frequency (λ_d - wavelength in the dielectric). For the maximum operating frequency of f_{max} = 939 GHz, the number of junctions (i.e. unit cells) is $N(f_{max}) = N_{max} \approx 22500$. For lower frequencies, the number of junctions is $N(f)=N_{max} (\frac{f}{f_{max}})^2$, so at 100 GHz it will be 225 and at 500 GHz, 5625 junctions can be integrated in the array.

2.1.4. Maximum power output

Assuming all junctions are locked in phase, the output power will be proportional to the number of junctions. In these designs, the junction impedance is matched to the antenna impedance through the impedance transformer. Assuming a low-loss transformer, the output power per junction P' is given by $P'=0.125\ I_c^2 R_j$, where I_c is the junction critical current and R_j is the junction impedance. If the junction is not externally shunted, it can be shown that its impedance will be of the order of the junction normal resistance R_n. For externally shunted junctions, the junction impedance will be the shunt resistance R_S [Ohm]$= 14.58 \frac{\sqrt{\beta_c}}{A\ [\mu]}$, where β_c is the McCumber parameter and A is the junction size. As an example, the maximum output power available from the array designed for 500 GHz with 5625 junctions would be 6.4 μW for $\beta_c = 1$ junctions, 9.5 μW for $\beta_c = 2.5$ and 37.25 μW for unshunted junctions.

2.2. Design issues

The goal of the design phase was to determine key design parameters and create a number of designs that would provide a maximum likelihood of success, while at the same time allowing one to exploit a variety of design issues experimentally. Considerable effort was directed toward a structured design approach, where a variety of design variations would be exploited by changes in the unit cell while keeping the array structure common to all designs. Extensive simulations were performed using the Touchstone [10] simulation program to determine the best array structure and the tuning circuit in terms of coupled power output and expected tuning bandwidth. Table 1 summarizes the Conductus fabrication parameters used for all the designs.

Critical current density [A/cm^2]	Parasitic capacitance [fF/μ^2]	Junction size[μ]	Junction critical current [μA]	Junction normal state resistance [Ohm]	Junction capacitance [fF]
2500	62	3 x 3	225	9.5	558

Table 1. Fabrication process parameters.

2.2.1. Design frequency

The operating frequency of the quasioptical array is determined by the resonant frequency of the locking Fabry-Perot type cavity formed inside the Si substrate. Our 20-mil double-polished Si substrate gives a set of resonant frequencies $f_n = (2\,n - 1)* 43.3$ [GHz], n = 0,1,2... We have chosen the base frequency of our designs to be f_2 = 129.9 GHz, and the harmonic frequency of f_5 = 389.7 GHz. Simulations have shown that at higher frequencies, the bandwidth becomes significantly reduced because of the large parasitic capacitance of the 9 μ^2 junctions employed in all designs.

2.2.2. Standard unit cell

In order to determine the most adequate tuning structure, a number of candidate circuits have been simulated in the designated frequency range. Candidate circuits included single inductor, single- and two-stage microstrip transformers [11], using both unshunted and shunted junctions. A new design involving a group of junctions shunted with a common resisto- proved to be the most promising approach for large bandwidth arrays, as long as the series inductance remained small. The unit cell circuit incorporates between 1 and 16 junctions shunted with a common resistor R and coupled to the antenna through a quarter wave transformer (Figure 1). A detail of the DC biasing circuit is also shown, with an optional series resistor Rs of the same order as R.

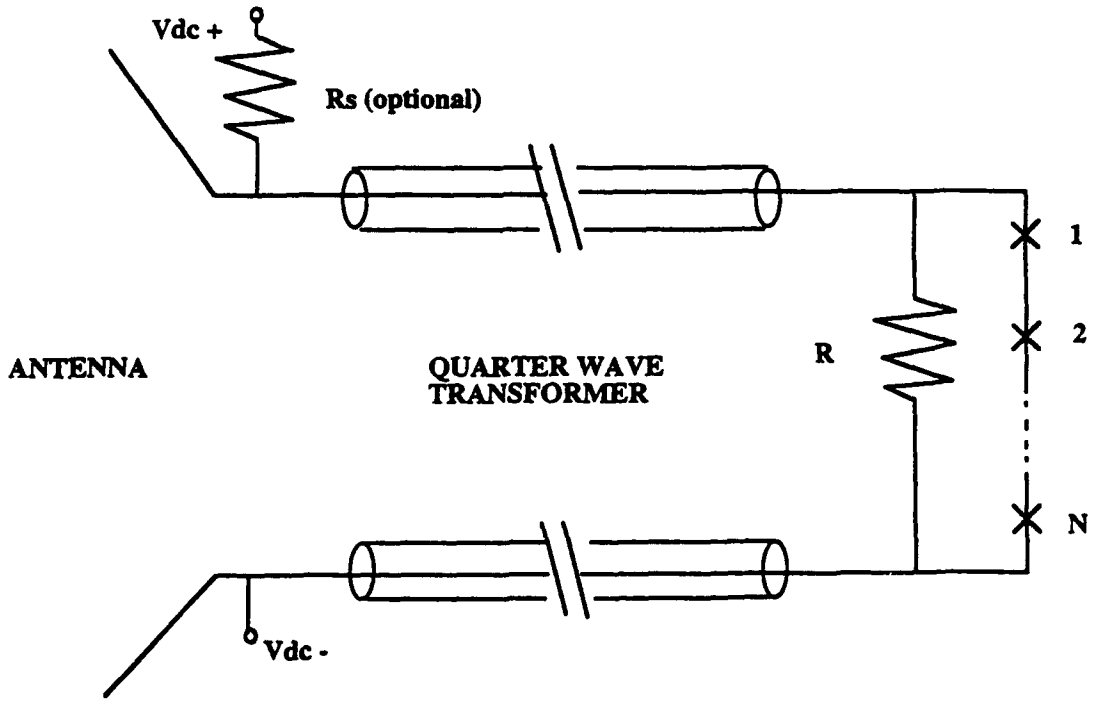

Figure 1. Quasioptical array standard unit cell.

A single-stage transformer was chosen in order to keep the array unit cell size as small as possible, since the two-stage transformers have not shown a bandwidth improvement significant enough to justify the increased size. This design is applicable as long as the series inductance between junctions is held as small as possible, up to about 0.5 pH maximum for the frequency range of interest. As long as this requirement is fulfilled, there does not appear to be any difference between the junctions being individually shunted by resistance R/N and the whole group of N junctions being shunted by the common resistance R.

Table 2 summarizes the design parameters for cases N=1, 4, and 8. Figure 2 shows results of the simulations for the case N=8. The bandwidth of 73 GHz is achieved in the fundamental band at the central frequency of 134 GHz, and 50 GHz at the harmonic band with the central frequency of 383GHz. The series inductance between each two junctions has been assumed at 0.5pH. Simulated fractional bandwidths for N=1, 4 and 8 are given in Table 3. The overall size of the unit cell is 600 x 600 μ, enough to fit a fundamental 130 GHz quarter-wave antenna in it.

number of junctions N per unit cell	Microstrip transformer impedance Z [Ohm]	Microstrip electrical length at 130 GHz [degrees]	Common shunt resistance R [Ohm]
1	5.2	91	0.4
4	10.5	90	1.6
8	15	90	3.2

Table 2. Unit cell parameters.

number of junctions N per unit cell	Fractional BW at base frequency (130 GHz)	Fractional BW at harmonic frequency (390 GHz)	Maximum power at 130 GHz [μW]
1	19 %	6 %	0.28
4	36 %	12 %	1.1
8	54 %	13 %	2.2

Table 3. Simulation results.

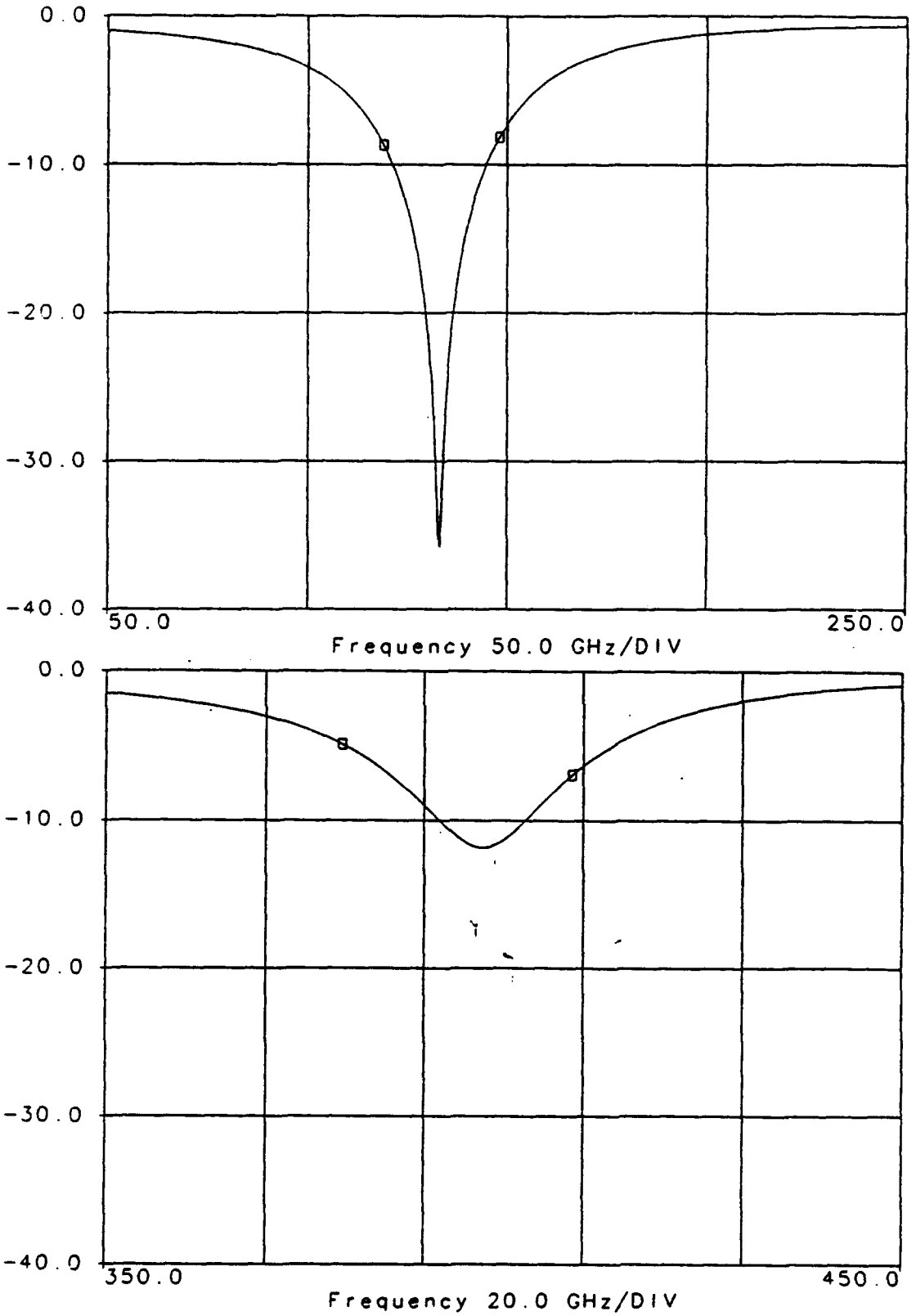

Figure 2. Touchstone simulations of the design with N=8 at fundamental (upper graph) and harmonic frequency (lower graph).

2.2.2. *Other unit cells*

Two chips with non-standard unit cells were also designed. The first one is the variation of the standard unit cell where, instead of a series array of N junctions a series-parallel array of N x M junctions is employed. In particular, bow-tie array with 16 junctions per unit cell (N=4, M=4) has been constructed. This would be the most natural way to increase the overall power of the array by increasing the number of junctions. The constraint is that the series inductance of junction-to-junction connections must be kept as small as possible.

A second non-standard unit cell is one of a quasi-compact array, where a unit cell slot antenna is periodically loaded with closely spaced microstrip transformers carrying shunted junctions at their ends. One such array has been designed with N=9 junctions per unit cell (see Figure 5 for a photograph).

2.2.3. *Array organization and layout*

Figure 3 shows the layout of the 1 cm chip. Arrays have been laid-out with unit cells organized in 11 rows and 10 columns, with each unit cell having N=1-16 junctions, so that the total number of junctions ranged from 110 to 1760 junctions per array. The dc biasing is organized such that the array can be biased top to bottom in the series-parallel fashion (i.e. rows biased in series, units in a row biased in parallel), but each row can also be biased separately, and finally the whole array can be biased in parallel. Further, designs were made with and without series biasing resistors. Also, provisions have been made for each row to be shunted with the parallel resistor by wire-bonding appropriate pads provided at the side of each row. The parallel resistor could possibly reduce the radiation linewidth of the array.

Arrays with two different antennas have been designed: bow-tie and slot. The bow-tie array is characterized by a large inductance between unit cells, whereas the slot array geometry presents much smaller inductance. This would allow a comparison of the phase-locking capability of the array between the two cases.

Arrays occupy an area of about 7 mm X 7 mm of 1 cm chips. Each array is accompanied by a single-junction detector integrated with a short bow-tie antenna, for the purpose of detecting the radiation coupled into the cavity. Also, each chip is provided with test structures for characterizing the junction parameters (Ic, Rn of single junctions), junction uniformity (series array of 100 junctions) and junction shunt resistance, as well as resonant frequencies of the tuning structures (single unit cells). Chips have a 32 pad layout for wire-bonding to the liquid - He probe.

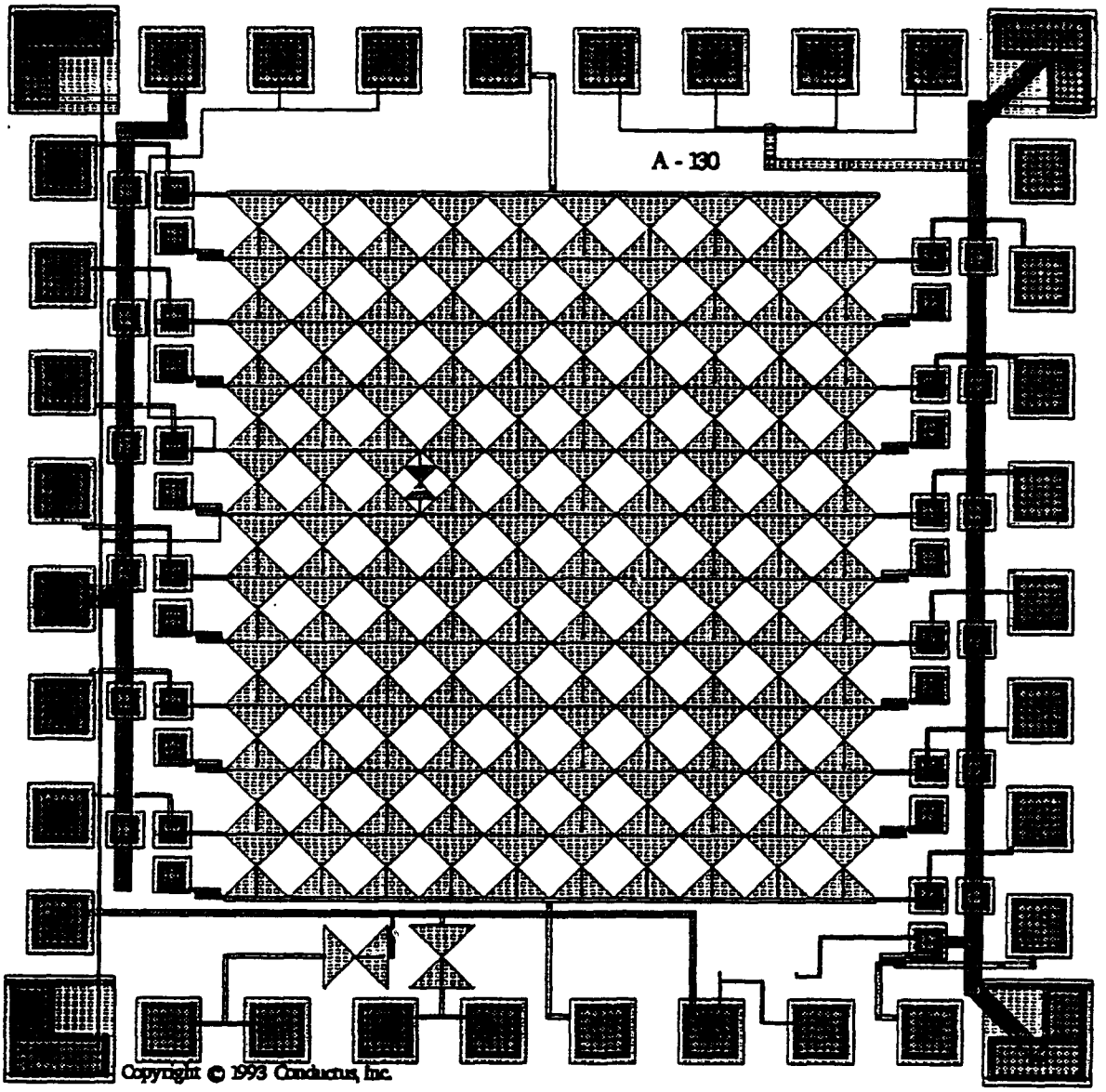

Figure 3. Layout of a 1 cm array chip.

2.3. Fabrication

A lot with four 4-inch wafers has been fabricated in Conductus standard 4-niobium-layer technology. The target critical current density was J_c = 2500 A/cm^2. The resistors came on target. The junctions turned out to be smaller than designed, around 4 μ^2 instead of 9 μ^2. Figure 4.a shows a typical I-V curve of a witness unshunted junction, with an I_c of about 90 μA. The uniformity of junctions, measured on a string of 100 junctions in series was typically within 6% (total spread). The I-V curve of a witness series array is shown in Figure 4.b. Two of the wafers had problems with over-etch and under-etch, respectively, of the resistive layer towards the periphery of the wafers. Overall, the fabrication was successful, yielding a number of chips with arrays, witness junctions and series arrays displaying correct I-V curves. Figure 5 presents a microphotograph of a detail of the quasi-compact array chip. Several rows of array strucutres are shown with a slot-line antenna densely loaded by microstrip lines with shunted junctions at their ends. The short bow-tie antenna near the edge of the array carries a detector junction at its apex.

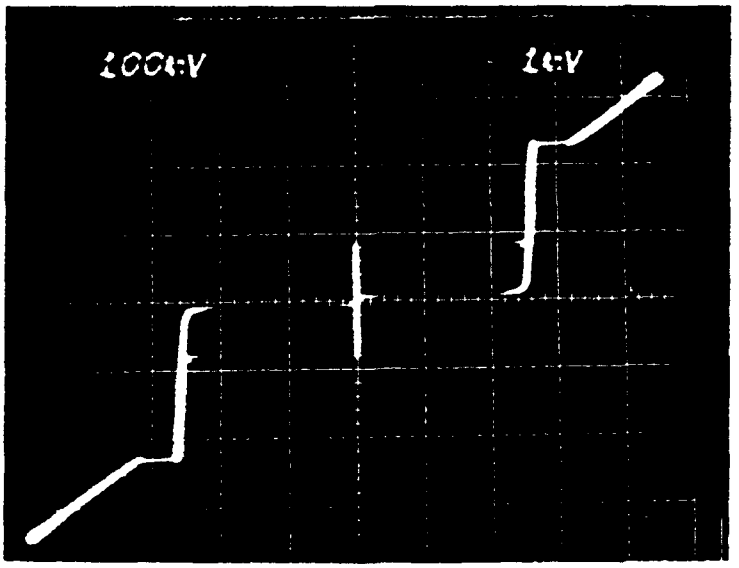

Figure 4.a. Typical I-V curve of an on-chip witness junction; scale: current -> 100 μA/div, voltage -> 1 mV/div.

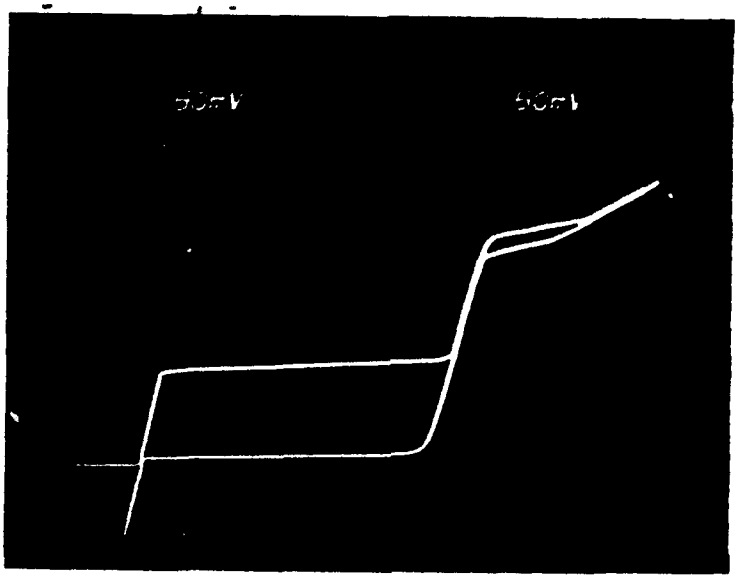

Figure 4.b. Typical I-V curve of an on-chip 100 junction series array; scale: current -> 50 μA/div, voltage -> 50 mV/div.

Figure 6 shows a detail of the fabricated standard unit cell on one of the bow-tie array chips. The junction is visible at the end of the quarter-wave microstrip line, together with the 0.4 Ohm shunting resistor. Also visible at the bottom of the picture is a 0.4 Ohm series biasing resistor for the junction in the row below (not shown in picture).

On some chips, problems with the interlayer contacts have been encountered, as demonstrated by large series resistance or open-circuits. This influenced detector junctions more than anything else, since their biasing lines went through S3-S2 contacts. Therefore, on a number of chips it was not possible to verify the oscillator operation even though arrays showed promising I-V curves since the detector junction appeared open-circuited.

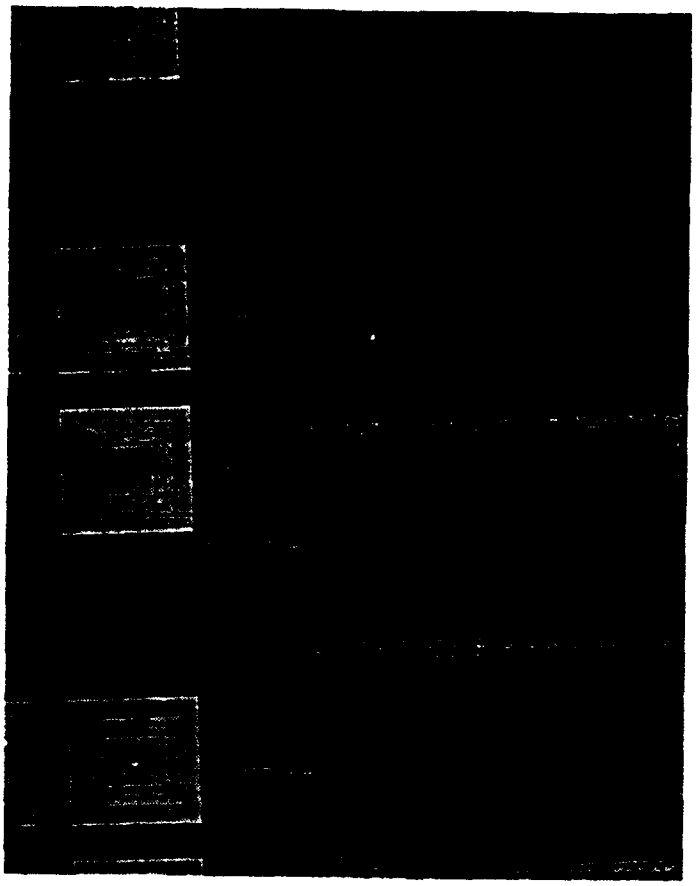

Figure 5. Detail of the fabricated quasi-compact array chip.

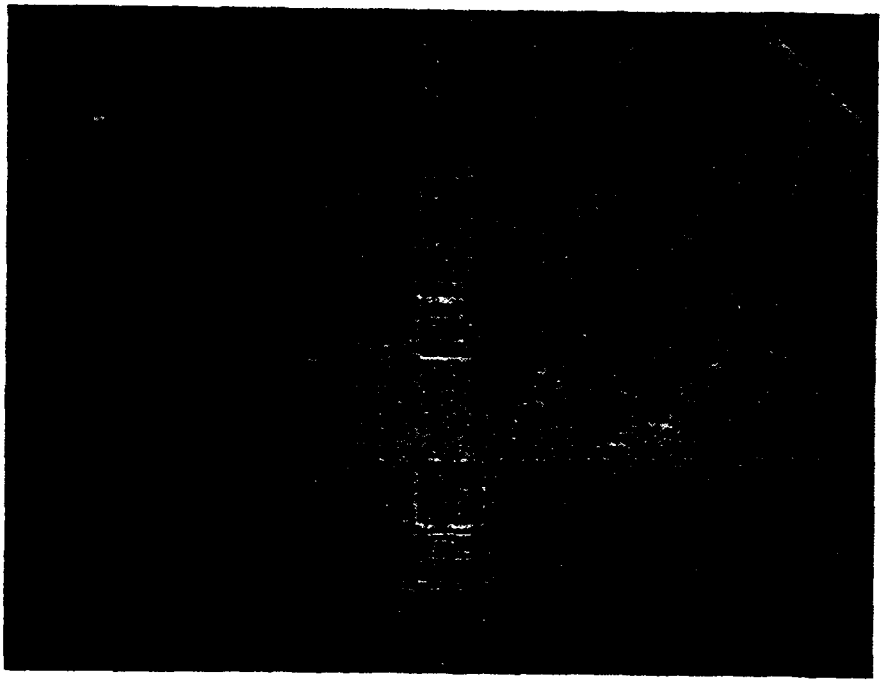

Figure 6. Detail of the standard unit cell on one of the bow-tie array chips.

2.4. Test results

All testing was performed in a custom liquid-He probe, with chip pads wire-bonded to the PC-board leads with outside connections. The probe has a two-layer μ-metal shield. However, none of the wiring leads are being filtered, and testing is done in a very noisy environment.

Testing included first measurements of the I-V curves of the diagnostic cells (on-chip single junctions and series array), single unit cells, detector junction and the whole array. Both single unit cells as well as whole arrays of different designs showed I-V curves with characteristic "humps", or steps, in the voltage range of 200-300 μV, indicating strong coupling between the junction and the microstrip-coupled antenna [12]. This dc voltage range, through the known voltage-frequency relation of 486.3 GHz/mV, corresponds to the Josephson oscillation frequency range of 97 - 146 GHz, encompassing the designed value of 130 GHz. Figure 7 shows a typical I-V curve of a single standard unit cell (N=1) with bow-tie antenna; the first step in the I-V curve is at 230 μV. The I-V curve of the corresponding array appeared very similar to this one, with scaled voltages and currents for the number of junctions biased in series and parallel. No steps were visible in I-V curves at voltages around 0.8mV, where interactions at the harmonic frequency of 390 GHz would be expected.

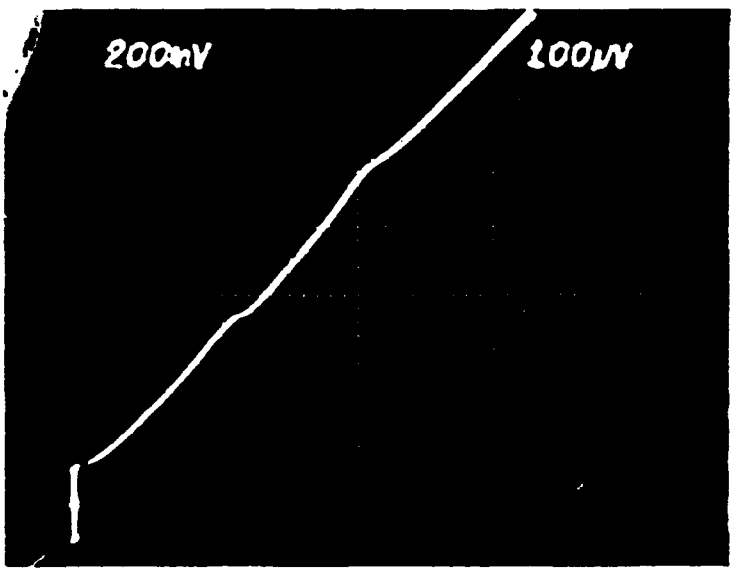

Figure 7. Typical I-V curve of the single unit cell (N=1), as well as of the array with scaled voltage/current, showing steps at frequencies of enhanced interaction between the junction and the microstrip/antenna circuit (scale: current -> 200 μA/div, voltage -> 100 μV/div).

However, a second step in the voltage range of 400-500 μV appears in most array I-V curves, indicating that some interaction exists between the junction and the microstrip transformer in the frequency range close to double the fundamental frequency. As will be shown later in the radiation tests, radiated power was detected only at the fundamental frequency of array operation, and no power was detected when the array was biased at the second step. Although the nature of the interaction at the second step is not intuitively apparent, the interaction does not appear constructive, and the array does not work in the oscillator mode.

2.4.1. Proof-of-principle test

The proof-of-principle test consists of detecting the radiation of the oscillator with the on-chip radiation detector. The detector is simply a shunted junction at the apex of a short bow-tie antenna, placed inside the array, but DC isolated from the array. Figure 8 shows a photomicrograph of a detector in a bow-tie array. When the array is operating in phase, it launches radiation mostly into the substrate because of the high dielectric constant of the silicon. This radiation hits the other side of the substrate and gets reflected back from its surface and/or the surface of the metal plate touching it. This radiation establishes a standing wave inside the substrate that serves as the self-injection-locking mechanism for the array, and a portion of it escapes as the free space plane wave radiation perpendicular to the chip surface. Some of the radiation is also coupled to the detector inside the array, and induces a Shapiro step in its I-V curve.

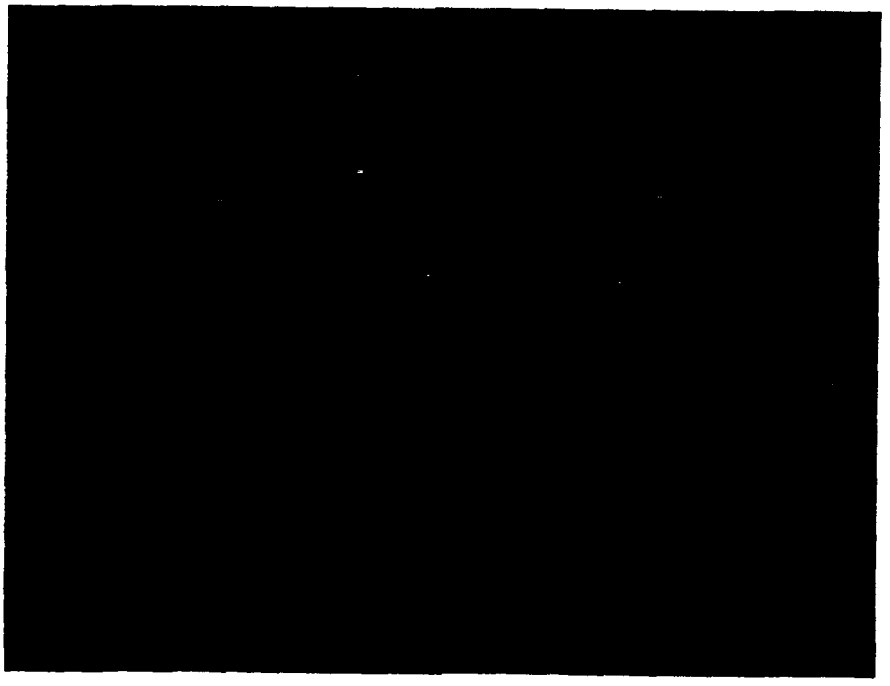

Figure 8. Microphotograph showing radiation detector inside array.

This test was performed on a number of chips, whenever both the array and the detector showed promising I-V curves. On two chips, both with standard unit cell with N=1, the radiation has been detected. Of those two chips, one had series bias resistors and the other one had purely superconducting bias. In both cases, the bias was series-parallel, i.e. rows of array were biased in series, while junctions in each row were biased in parallel.

2.4.2. Array #1 with series biasing resistors

Here we present results for the first array with standard unit cell N=1, a total of 110 junctions, bow-tie antennas and series biasing resistors. Figure 9 shows the I-V curve of the array (upper photo) and the detector (lower photo). The slope of 0.4 Ohm in the critical current portion of the array I-V curve is due to the series resistance in the DC bias path of each individual junction (see also Figure 6). The voltage is measured across 8 rows of the array, out of the total 11 rows. From the slope of the array, when the series resistance is de-embedded, the junction resistance is 0.475 Ohm. This photograph is a multiple exposure, with two large white spots on the array I-V curve representing the bias point BP#1 (origin,I=0, V=0, lower spot) and the bias point #2 (I=5.2 mA, V=3.6 mV, upper spot) at which the array has biased when radiation was detected. The lower photo is also a multiple exposure showing two traces of the resistive portion of the detector I-V curve: the lower one is with the array not biased (bias point #1), and the upper one is for the array bias at bias point BP#2. The two traces are mutually vertically shifted by one division for clarity (otherwise they would overlap); the origin of the I-V curve is 70 μA below the picture frame for the upper trace and 90 μA for the lower trace. There is a clearly visible Shapiro step in the upper trace at the voltage of about 240 μV, corresponding to the radiation frequency of around 116 GHz. From the array bias point #2, the DC voltage at each junction is calculated at 242 μV (5.2 mA is 520 μA per junction; 3.6 mV on 8 rows is 450 μV per row; minus voltage on the series resistance of 0.4 Ohm x 520 μA = 208 μV) or 117 GHz radiation, agreeing closely with the frequency of the detected radiation. It has also been observed that the Shapiro step would track the dc bias voltage of the array in the limited voltage range around the bias point #2. Therefore there is no doubt that the origin of detected radiation is indeed the array.

As evidence that the radiation comes as the result of the whole array of Josephson junctions locking in phase, and not as incoherent radiation from the junctions closest to the detector junction, the same experiment is performed when only a single row of the array in which the detector is inserted is biased, while the rest of the array is not. No radiation is detected in this case.

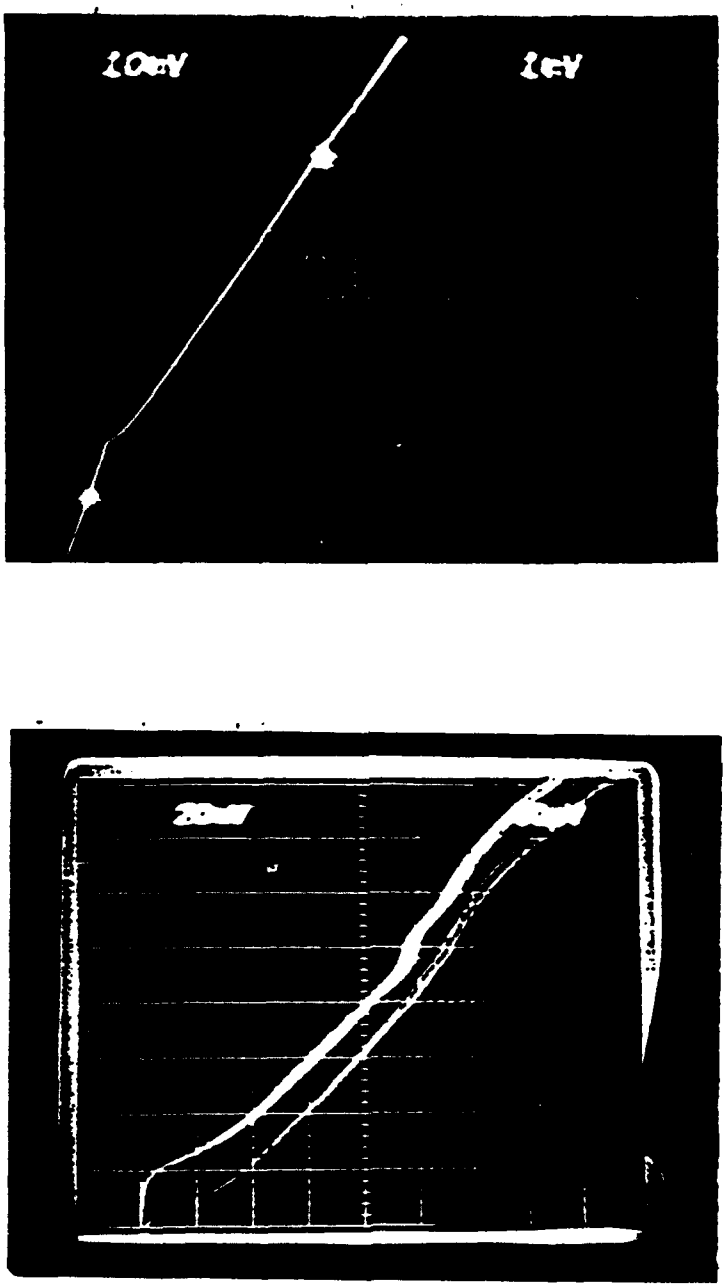

Figure 9. Measured I-V curves of the array #1, 8 rows-10 columns (upper photo, scale: current ->1 mA/div., voltage -> 1 mV/div.) and the detector (lower photo, scale: 20 μA/div., voltage ->50 μV/div.)

From the size of the Shapiro step (around 18 μA) we can estimate to the first order the detected RF power as $P = 0.5 \frac{V_a^2}{R}$, where Va is the amplitude of the RF voltage induced at the detector by the radiation and R is the impedance of the detector. Va is determined from the relation $\frac{DI}{I_c} = J_1(\frac{V_a}{V_{dc}})$, where DI is the size of the Shapiro step and V_{dc} is the dc bias voltage at the Shapiro step. The detected power is estimated at 2.64 nW. The maximum power this array is capable of producing is 44.5 nW, or 0.4 nW per junction. This is smaller than the designed maximum power (Table 3, N=1) because the junction critical current was 2.5 times smaller than designed. Nevertheless, the detected power is equivalent to the power that 6 junctions would produce radiating at their maximum level. From the position of the detector (Figure 8) it is obvious that it is only capable of detecting a fraction of the total array radiation, from its nearest neighbors, providing they are locked in phase through interaction with the cavity. We therefore find strong indication that the whole array is locked in phase and is radiating close to its maximum power.

2.4.3. Array #2 without series biasing resistors

Here we present results from the radiation test of the second array, which is the same as the array #1 except for the pure superconducting dc bias (no series resistances in the dc bias path). Figure 10 shows the results in a similar manner as for the array #1. The upper multiple exposure photo shows the array I-V curve (voltage measured across 8 rows) with bias point (I=5.4 mA, V=1.75 mV) designated by the large light dot, and lower photo shows the detector I-V curve with the array biased at that bias point. The detector I-V curve shows a Shapiro step at around 270 μV. however, there appears to be series resistance of around 0.3 Ohm in the detector I-V curve (apparently due to contact resistance) with current of 170 μA going through it, so the dc voltage across the junction is calculated at 219 μV, corresponding to the frequency of radiation of 106.5 GHz. This agrees well with the dc bias voltage of 218 μV of dc bias on each of the array junctions.

In the I-V curve of the array there is a set of barely visible steps immediately above the designated biasing point. Figure 11 (upper photo) shows a blow-up of this portion of the array I-V curve, where these steps are evident. When the array bias is slowly swept across this region, the Shapiro step in the detector I-V curve follows it. The lower photo of Fig. 11 is the same as the upper photo, aligned so that the middle vertical line of the oscilloscope screen is at a voltage of 2 mV. This photo shows the array bias range between the two white spots across which the above mentioned tracking occurs, 1.74 - 2.05 mV. On a single junction scale this voltage range corresponds to 217 - 256 μV, which is a radiation frequency range of 105.5 - 124.5 GHz.

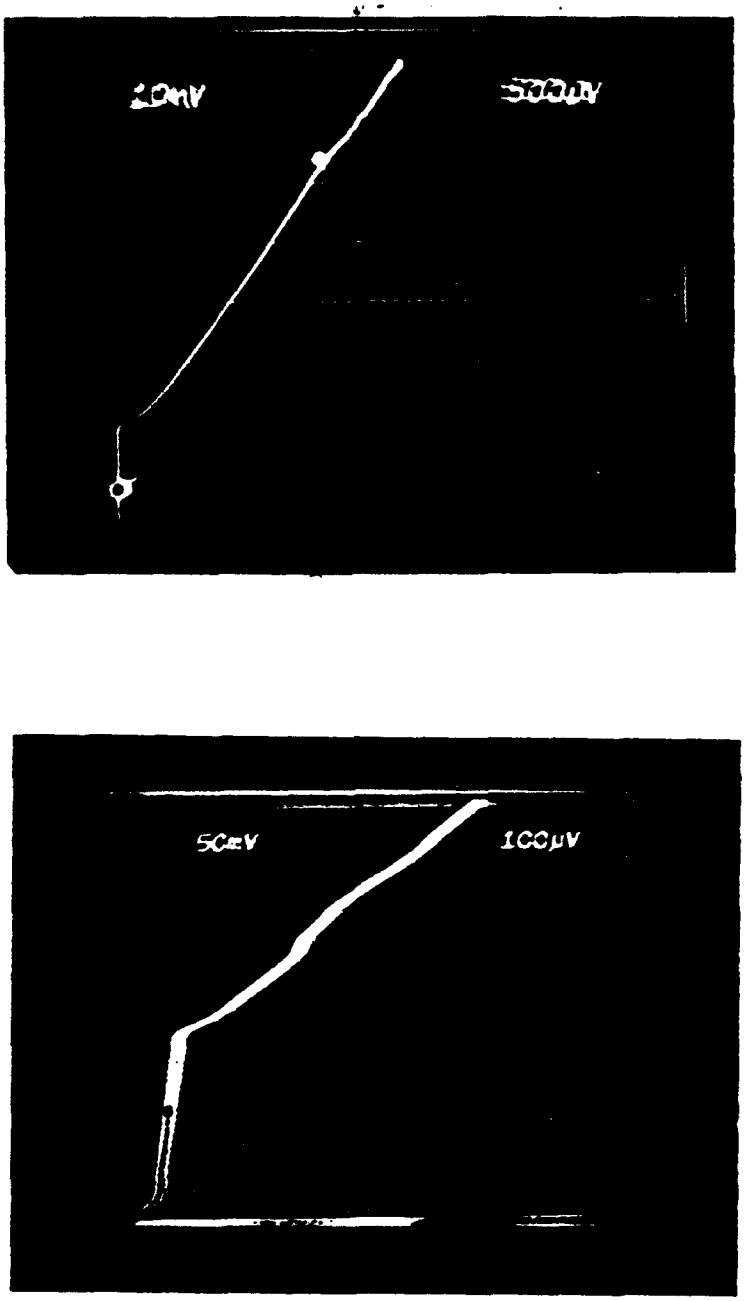

Figure 10. Measured I-V curves of the array #2, 8 rows-10 columns (upper photo, scale: current ->1 mA/div., voltage -> 0.5 mV/div.) and the detector (lower photo, scale: current ->50 μA/div., voltage ->100 μV/div.)

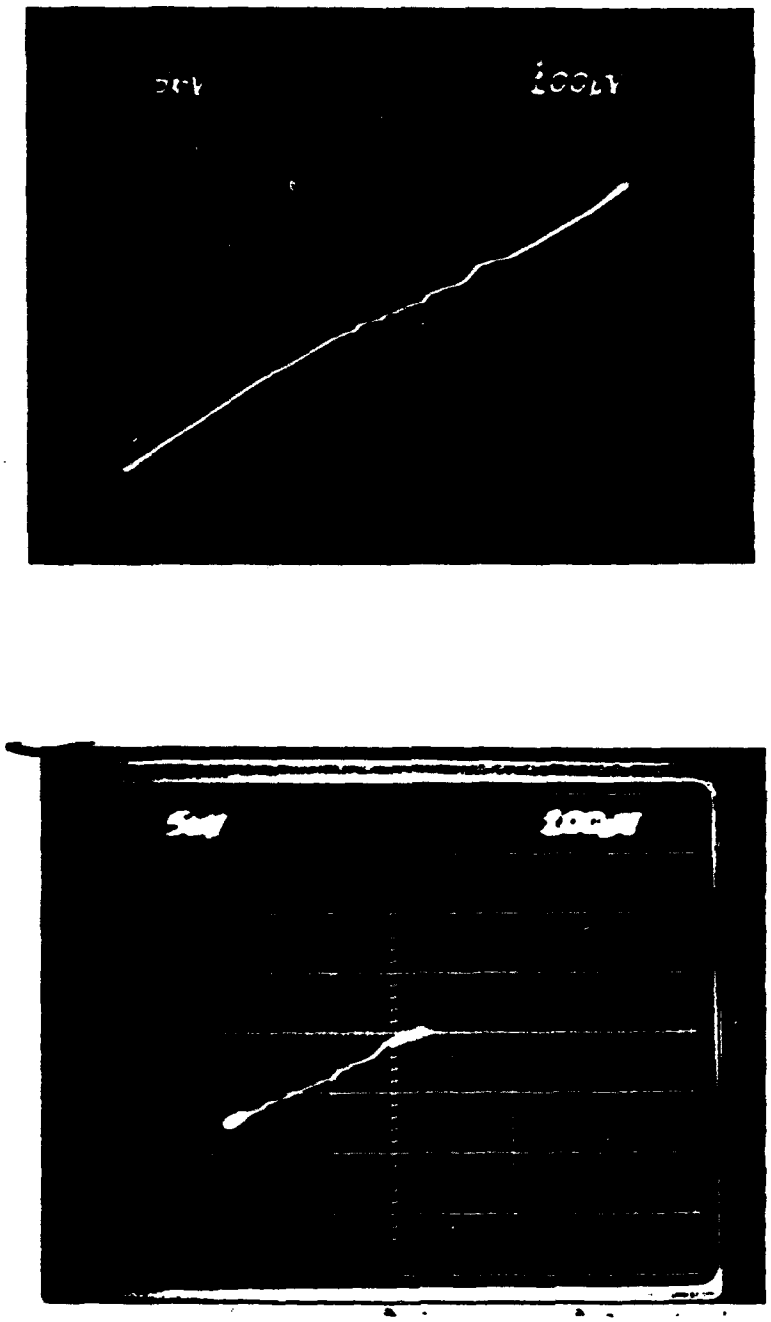

Figure 11. Enlarged portion of the array I-V curve showing little steps where array radiates (upper photo), and the array bias range across which the detector tracks array radiation (lower photo, aligned horizontally so that the middle vertical line is at 2 mV). Scale: current -> 500 μA/div., voltage ->100 μV/div.

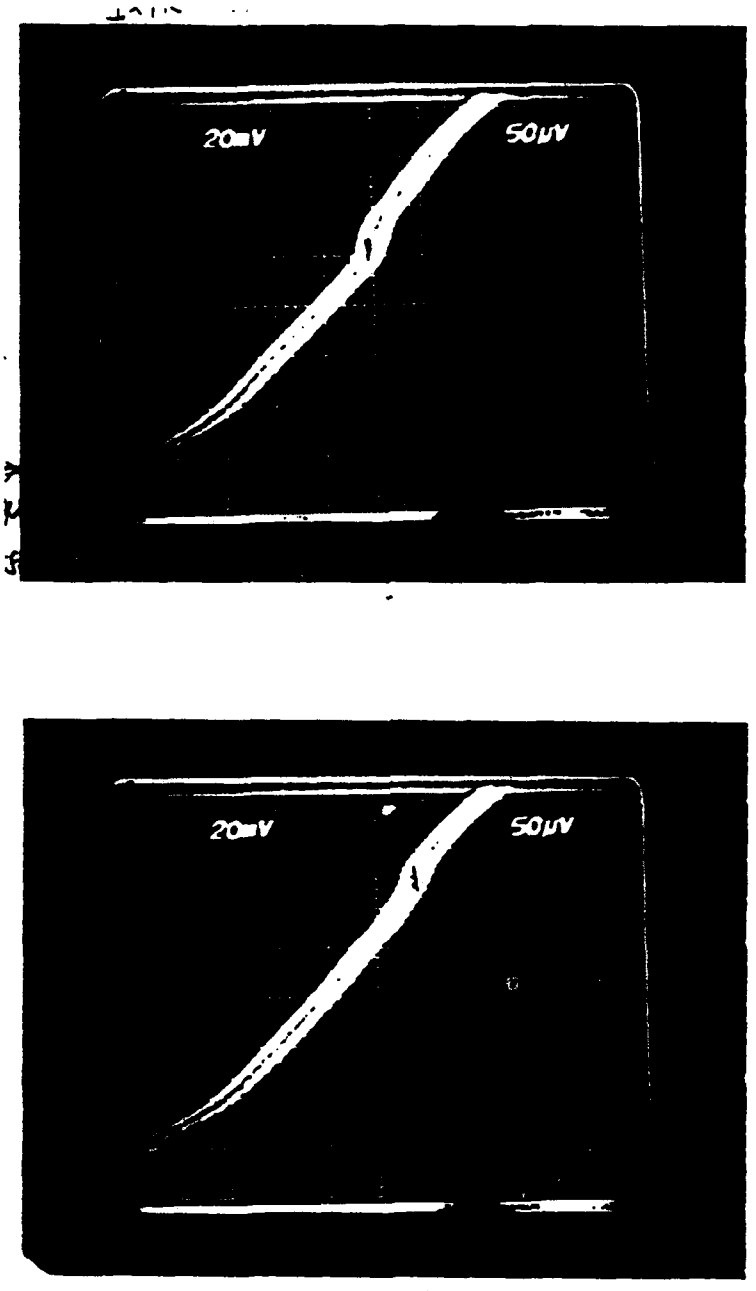

Figure 12. Measured resistive portion of the detector I-V curve showing Shapiro steps when array is biased at two extreme points of the tuning range: lower point, 105.5 GHz radiation (upper photo) and upper point, 124.5 GHz radiation (lower photo). Scale: current ->20 μA/div., voltage ->50 μV/div. The origin of the I-V curve is 60 μA below the lower edge of the photo.

Figure 12 shows the Shapiro steps in the detector I-V curve for the lower (upper photo) and upper (lower photo) extreme bias points of the tracking range. This tracking range is actually the tuning range of the array, indicating the bandwidth of 19 GHz, or 16% at the central frequency of 115 GHz. The predicted bandwidth for this array was 19% (Table 3). The appearance of the double trace in the I-V curves in Fig. 12 is due to a large amount of noise present during the measurement, as well as the excessive contact capacitance. The size of the Shapiro step is similar as in the case of array #1, so that this array also appears to radiate close to the maximum of its available power.

2.5. Discussion

From the testing performed under this program, several other observations can be made:

1) Series resistance - Series resistance in the dc biasing path does not appear to have a crucial impact on array phase-locking, but it doesn't hurt it, as seen from the two results presented above.

2) Harmonic radiation - No radiation has been detected in either demonstrations at harmonic frequency of 390 GHz. Since the predicted bandwidth for this type of array was only 6%, one possible reason is that stable bias could not have been achieved with the coarse biasing equipment that was used in the experiment. Also, the amount of radiated power at that frequency might have been below the observable amount in the noisy environment of the measurements.

3) Parallel biasing - All attempts to bias the whole array in the fully parallel fashion through wire-bonding of the pads provided for that purpose failed because the bonding wire was lifting off the pad metal on some of the pads in all cases. Therefore, no comparison could be made for the different biasing schemes.

4) Shunt resistor - The same limitations described in (2.5.3) were true for the attempts to shunt each row through the resistors provided at the sides, and test the array radiation in the presence of shunt resistance across the array.

5) Larger arrays - None of the arrays with larger numbers of junctions per unit cell (N>1) that we were able to test have shown signs of coherent radiation. We can speculate that some of the reasons might be due to local variations in junction uniformity, layout parasitics larger than anticipated, etc. Also, there were arrays with promising I-V curves whose detector junction appeared open. The same is true for a number of chips carrying

arrays identical to the two working arrays, that also did not radiate. Therefore, there is no reason to believe that arrays with standard unit cell and N>1 would not radiate, and we believe that it is only a matter of fabrication yield.

2.6. Conclusion

In this program we have designed, fabricated and performed successful proof-of-principle tests of the Quasiotical Josephson Oscillator with integrated tuning elements. To the best of our knowledge, this is the first demonstration of a distributed array Josephson oscillator, where each junction feeds its own antenna and phase-locks to the radiation of other junctions. Further, this is also the first demonstration of using integrated microstrip tuning and impedance matching elements at every Josephson junction of this oscillator. Finally, this is the first distributed Josephson oscillator reported to date that appears to radiate close to its maximum available rf power. We believe that this illustrates the distinctive advantages of the concept of using local impedance matching in the distributed oscillator structure.

2.6. References

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3. Publications

Two papers based on the work performed under this program are in preparation:

"Demonstration of the Quasioptical Josephson Oscillator with Integrated Microstrip Transformers," Aleksandar Pance, Andrew Barfknecht and Stephen R. Whiteley, to be published in Appl. Phys. Letters, 1994.

"LTS Josephson Array VCO with Integrated Capacitance Tuners," A. Pance, A. Barfknecht and S. R. Whiteley, to be published in IEEE Trans. Appl. Supercon., 1995.

4. Personnel

Aleksandar Pance

Current Position:

Member of the Technical Staff

Project Assignment:

Dr. Pance served as Principal Investigator for this project.

Education:

Ph.D., Electrical Engineering, University of Rochester

Experience:

Aleksandar Pance received the Diplom Engineer degree from the Electrical Engineering Department, University of Belgrade, Yugoslavia in 1987, and M.S. and Ph.D. degrees in electrical engineering from the University of Rochester in 1989 and 1992, respectively. He received the Link Foundation Energy Fellowship in 1991. His graduate work was focused on quasioptical submillimeter range oscillators. He joined Conductus, Inc. in 1992 where he is currently a Member of the Technical Staff. He is working on the development of ultra-high speed digital electronic circuits for digital signal processing applications based on LTS and HTS superconducting technologies.

Andrew Barfknecht

Current Position:

Process Engineering Manager

Project Assignment:

Dr. Barfknecht was responsible for low-temperature niobium fabrication of proposed devices.

Education:

Ph.D., Physical Chemistry, Stanford University

Experience:

Andrew Barfknecht heads up the niobium circuit foundry at Conductus and, in conjunction with the superconductivity group at Hewlett-Packard, has developed the circuit process now in place. He has introduced a number of innovations into superconductor circuit processing that come from his extensive semiconductor fabrication background. Prior to coming to Conductus, he was responsible at Lawrence Livermore National Laboratory for process development and production of advanced multi-chip memory modules for a solid-state recorder on a satellite. At Advanced Micro Devices, he was responsible for sustaining the thin film and etch activities of a state-of-the-art CMOS IC facility. Andy Barfknecht brings a wealth of integrated circuit fabrication experience to the niobium circuit foundry at Conductus.

5. Interactions

The paper entitled "LTS Josephson Array VCO with Integrated Capacitance Tuners" will be presented at the 1994 Applied Supperconductivity Conference in Boston, and subsequently published in the IEEE Transactions of Applied Superconductivity, March 1995.

6. New Discoveries and Inventions

To the best of our knowledge, this is the first demonstration of the distributed array Josephson oscillator, where each junction feeds its own antenna and phase-locks to the radiation of other junctions. Further, this is also the first demonstration of using integrated microstrip tuning and impedance matching elements at every Josephson junction of this oscillator. Finally, this is the first distributed Josephson oscillator reported to date that appears to radiate close to its maximum available RF power.

7. Directions for future work

The results of this program prove the feasibility of the Quasioptical Josephson oscillator as a highly efficient source for millimeter and submillimeter range. The design is easily scalable to higher power by integrating more junctions in an array, with higher critical current densities. Also, higher operational frequencies can be achieved by physically scaling the unit cell and by using junction with smaller area, larger critical current density. Large area junctions, and therefore large parasitic capacitance would inevitably limit the bandwidth at higher frequencies [2]. Also, series inductance in the standard unit cell might limit the arrays to N=1 case for the highest frequencies of operation. Quasi-compact arrays seem attractive because they combine large number of junctions, and therefore large potential output power with local impedance matching for increased bandwidth of operation. Design principles utilized in this program could be directly applied to even more attractive high-temperature superconductor (HTS) arrays, as the HTS fabrication process matures and approaches the complexity and uniformity of the LTS process. Finally, the demonstration of the Quasioptical Josephson Oscillator makes other quasioptical signal processing devices [13-16] based on Josephson array technology feasible.