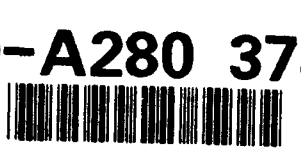

Quarterly Progress Report #1
(9/9/91 - 12/31/91)

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Principal Investigator: Gary Jones
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Phase One, Cathode Technology Development
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Field Emitter Array RF Amplifier Development Project
Phase 1, Cathode Technology Development

1.0 Executive Summary

- MCNC has theoretically determined the vertical column field emitter approach to be superior to its thin film and wedge emitter approaches for high frequency applications.

- Calculations indicate that the device transconductance/capacitance ratio per cell plays the most significant role in high frequency performance of FEA devices.

- Masks have been designed and fabricated for the pointed column device structures. Within the 1 cm^2 chip area, there are a variety of different size FE arrays. ranging from 1 emitter per cell to over 250,000 emitters per cell. The emitters are arranged in 2D arrays, which are the lowest parasitic capacitance configuration for a point cell array

- A 0.5 micron gate opening mask has been designed and is being fabricated which will provide ~1,000,000 tips in a 4x4 mm array and will provide ~0.25-0.30 micron gate-to-emitter tip spacing on top of the low capacitance columns.

- Low capacitance thin film emitter arrays are being processed for voltage spike protection devices since the small spacings in the thin film devices (potentially 10's of nanometers) will induce breakdown at lower voltages. This could be especially useful in providing safer insertion of point FEAs in high voltage tube systems. We also added points (saw blade design) to some of our thin film designs to allow them to operate at higher transconductances and thereby higher frequencies than straight edge designs.

- Deflection structures and lenses are under consideration for mask set updates.

- Silicon columns up to 10 microns have been successfully produced.

- Silicon column arrays have been coated with thick SiO_2 and planarized to form circular silicon islands in a sea of glass; processing of points on the columns is currently underway.

- Processing has begun on the new mask set, the first test runs are anticipated to be completed during the next quarter.

II. Milestone Status:

Milestones

	Completion Date Original	Actual
1. Theoretical RF analysis of Gated Emitters		
1.1 Down-Select RF FEA Designs	3/92	12/91
1.2 Identify Structure Parameter Targets	3/92	12/91
1.3 Modify Triangular Mesh Program for Gated Field Emitter Tips (Litton)	3/91	11/91
2. Field Emitter Development		
2.1 Design Mask Set/Device Layout	11/91	10/91
2.2 Fabricate Mask Set	12/91	11/91
2.3 Fabricate Basic Gated Point Emitters	12/91	12/91
2.4 Fabricate Column Emitter Structures	10/91	10/91
3. Vacuum Sealing/Testing System Design		
3.1 Design Vacuum Sealing/Test System	11/91	12/91
3.2 Order Vacuum Sealing/Test System	11/91	12/91
3.3 Expected Delivery of Testing System	3/92	4/92

Other milestones are not yet due and completion target dates appear unchanged.

III. Technical Progress:

1. Theoretical RF analysis of gated emitters

1.1 Capacitance for the gated columnar emitter appeared the best of all device types investigated. Figure 1 shows projected relationships between column height, gate dimensions and capacitance.

1.2 Transconductance of pointed column emitters has been identified as a primary development thrust. Cathode/gate resistance, interconnect design, and layout/dielectric capacitance were evaluated to be of minimal importance in the selected MCNC pointed column FEA device for practical designs. An evaluation of point structures by Dr. William Joines indicated that for a minimal overlap gate structure (approximated by a wire) and a column built on a plane, we obtain a best case cutoff frequency of 1.55 GHz per microsiemen. Early simulations of gate and column structures indicate that the current physical target structure should perform within 30% of this f_t per emitter (~1 GHz/Microsiemen) when other parasitic effects are included. This is being evaluated further and should be summarized in the next quarterly report.

2.0 Field Emitter Development

2.1 Masks have been designed and fabricated for the pointed column device structures. Within the 1 cm^2 chip area, there are a variety of different size FE arrays ranging from 1 emitter per cell to over 250,000 emitters per cell. The emitters are arranged in 2D arrays, which are the lowest parasitic capacitance configuration for a point cell array (a linear FEA configuration has more

parasitic capacitance due to requiring the same overlap area per cell and the addition of fringe capacitance). A 0.5 micron gate opening mask is being designed and fabricated which will provide ~1,000,000 tips in a 4x4 mm array and will provide ~0.25-0.30 micron gate-to-emitter tip spacing on top of the low capacitance columns. Some thin film designs were left on the mask set for arcing control devices to potentially protect large point emitter arrays in macro-vacuum tubes.

2.2 Development runs have been processed to better characterize different aspects of the process. Most test runs to date have been made using the old mask set and were used for experimentation with segments of the process. Some major fabrication accomplishments this quarter include:

- Silicon columns up to 10 microns have been successfully produced.
- Silicon column arrays have been coated with thick SiO_2 and planarized to form circular silicon islands in a sea of glass; processing of points on the columns is currently underway.
- Processing has begun on the new mask set, the first test runs are anticipated to be completed during the next quarter.

3.0 Vacuum Sealing/Testing System Design

3.1 An extensive design effort was directed at the vacuum wafer bonder/tester. Following discussion with two vendors, a final selection of a custom vacuum equipment company was made in mid-December. The company chosen was Litco, a small disadvantaged business. The system will have two chambers, one for testing and the other for bonding wafers together to form micro-vacuum cavities. The testing and bonding vacuum chambers will have the capability to evaporate thin films of barium, titanium, and other materials prior to testing or bonding without breaking vacuum. We have identified a simple swing source for large area evaporation of titanium and barium which will fit in our chamber. We have been given an April 1992 completion date by Litco. This will be important in evaluating low work function coatings. A diagram of the basic vacuum system is shown in Figure 2.

4.0 Other Developments

4.1 Duke University's work in modeling the RF characteristics of alternative diode structures has been most helpful as was discussed earlier in this report. This theoretical work will continue through the next quarter and is being dovetailed into the electric field and electron trajectory work at Litton.

4.2 UNC-Charlotte has been designing a vacuum test system for their part of this program. The Electrical Engineering Department at UNC-Charlotte will fund purchase of these parts. This system will be used to evaluate noise on emitter tips produced at MCNC. The system should be running by the end of the next quarter when there are plenty of new columnar emitter devices to evaluate.

4.3 North Carolina State University has been ordering parts to upgrade their electron trajectory system and assisting with modeling theoretical Field Emitter characteristics. Data from portions of this work were used by MCNC to generate some of the projected emission curves shown in Figure 3.

4.4 Litton has been updating their triangular mesh program to work with field emission devices. This work has been progressing rapidly and the program is now being tested with actual device structure parameters. An example of such

a recent plot is shown in Figure 4. This example shows no gate intercept for an experimental gated emitter design. Discussions have been held on how to best test and package FEA devices. Testing should begin at Litton during the next quarter.

IV. Fiscal Status

Fiscal Status will be sent from our contract accounting offices in January, 1992.

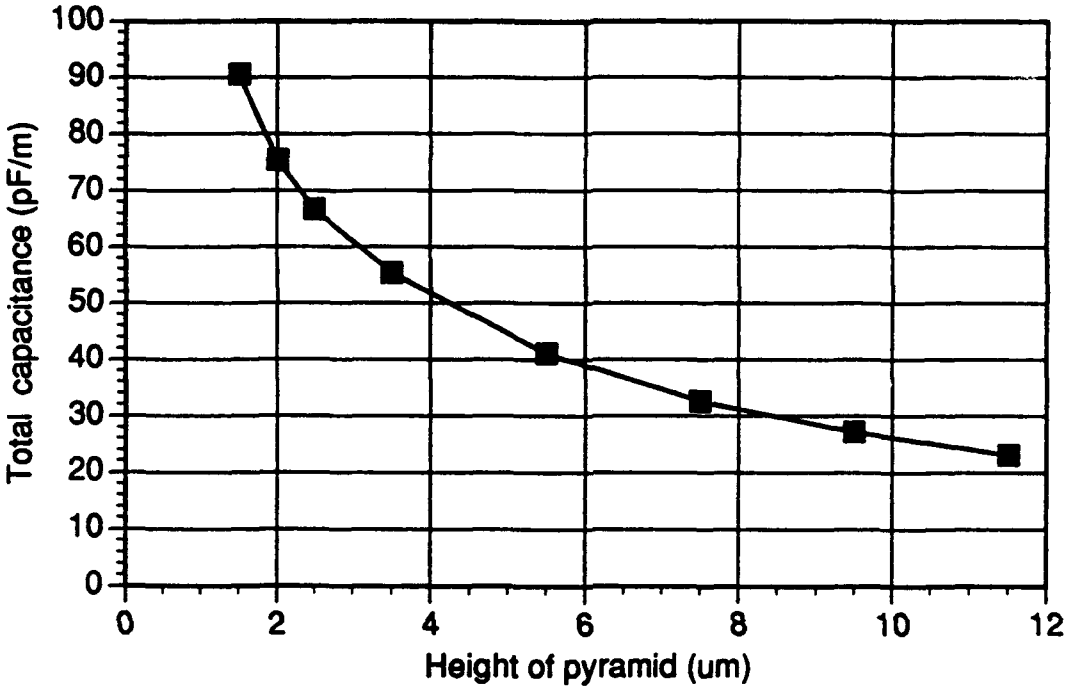
V. Problem Areas

The initial 1 GHz objective theoretically appears achievable with our current device design and emitter material selection, however, a potential problem is projected for the long term >10GHz Phase 2 objective unless the surface work function can be greatly reduced without degrading the tip dimensions, capacitance/tip, or other important device parameter. Several low work function materials have been ordered with the target of over 10 microseimens per tip as a long term objective. Alternative beam focusing and deflection based devices not requiring modulation of emission are also currently under early stage review for >>20 GHz applications.

VI. Visits and Technical Presentations

The only presentation made on this project outside the direct program participants during the contract time period has been the DARPA kickoff review. No visitors have come to review this project.

Figure 1
Relationship Between Column Heights and Capacitance



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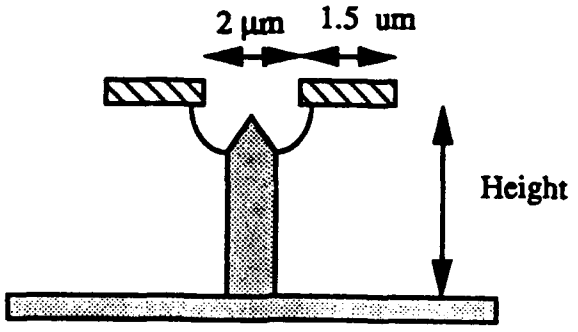


Figure 1 (continued)
Comparison of Capacitance Due To Different Gate Structures

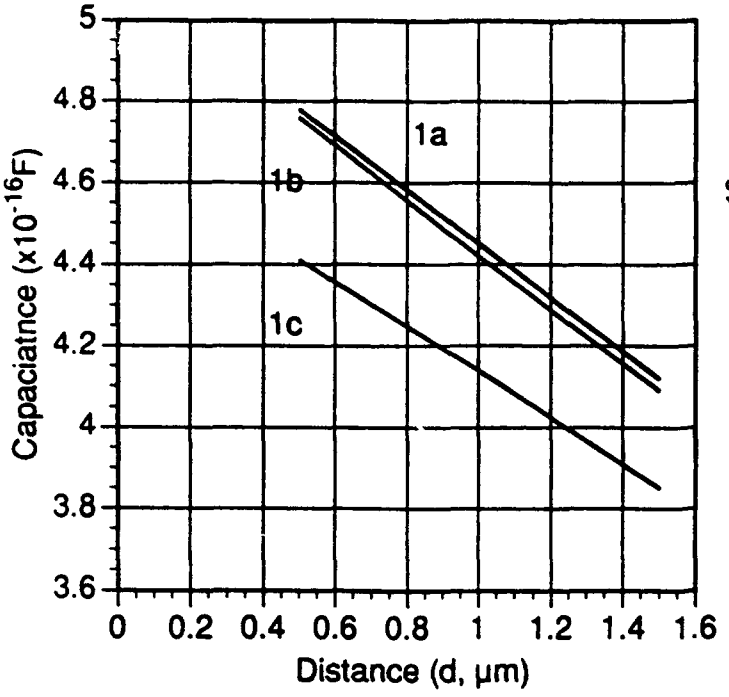


Fig. 1b

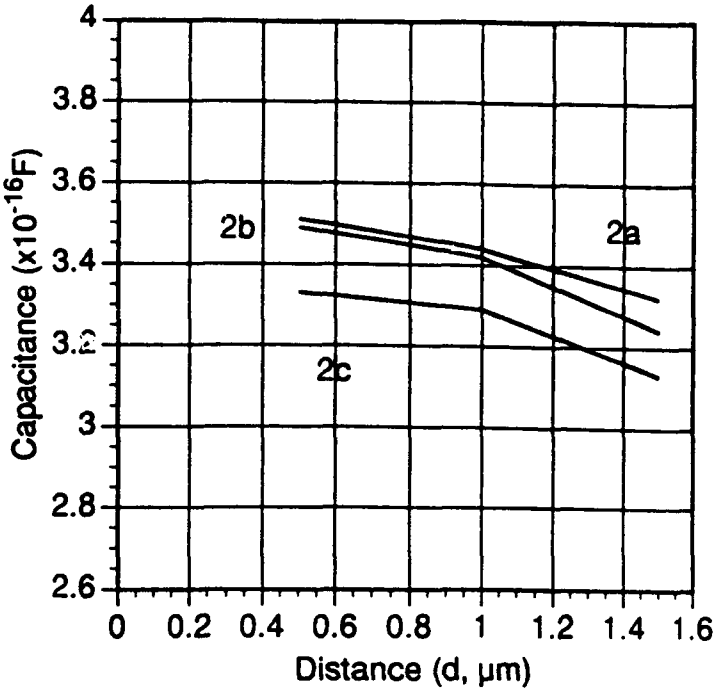


Fig. 1c

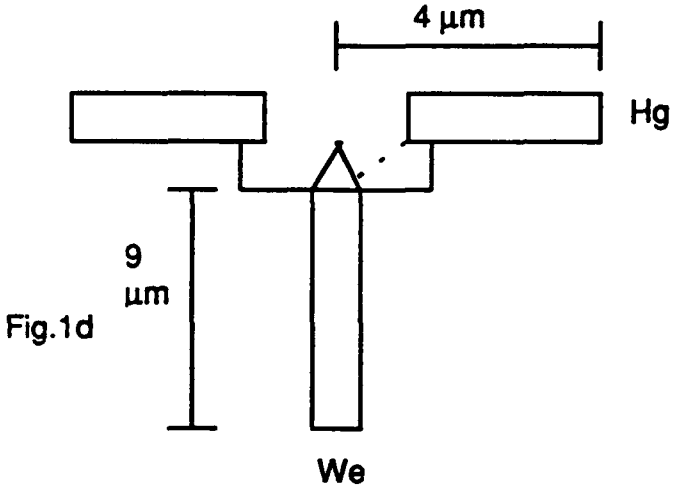


Fig.1d

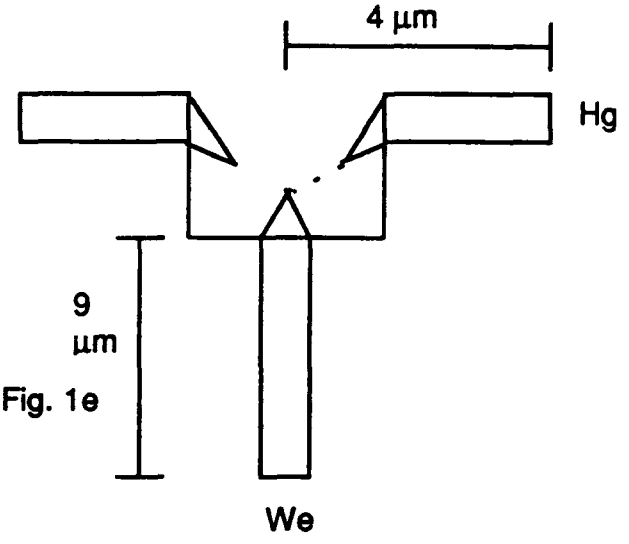


Fig. 1e

We=1.0 μm	Fig.	Hg (μm)
1a	Fig. 1d	0.5
1b	Fig.1d	0.1
1c	Fig. 1e	0.5

We=0.1 μm	Fig.	Hg (μm)
2a	Fig. 1d	0.5
2b	Fig.1d	0.1
2c	Fig. 1e	0.5

Figure 2

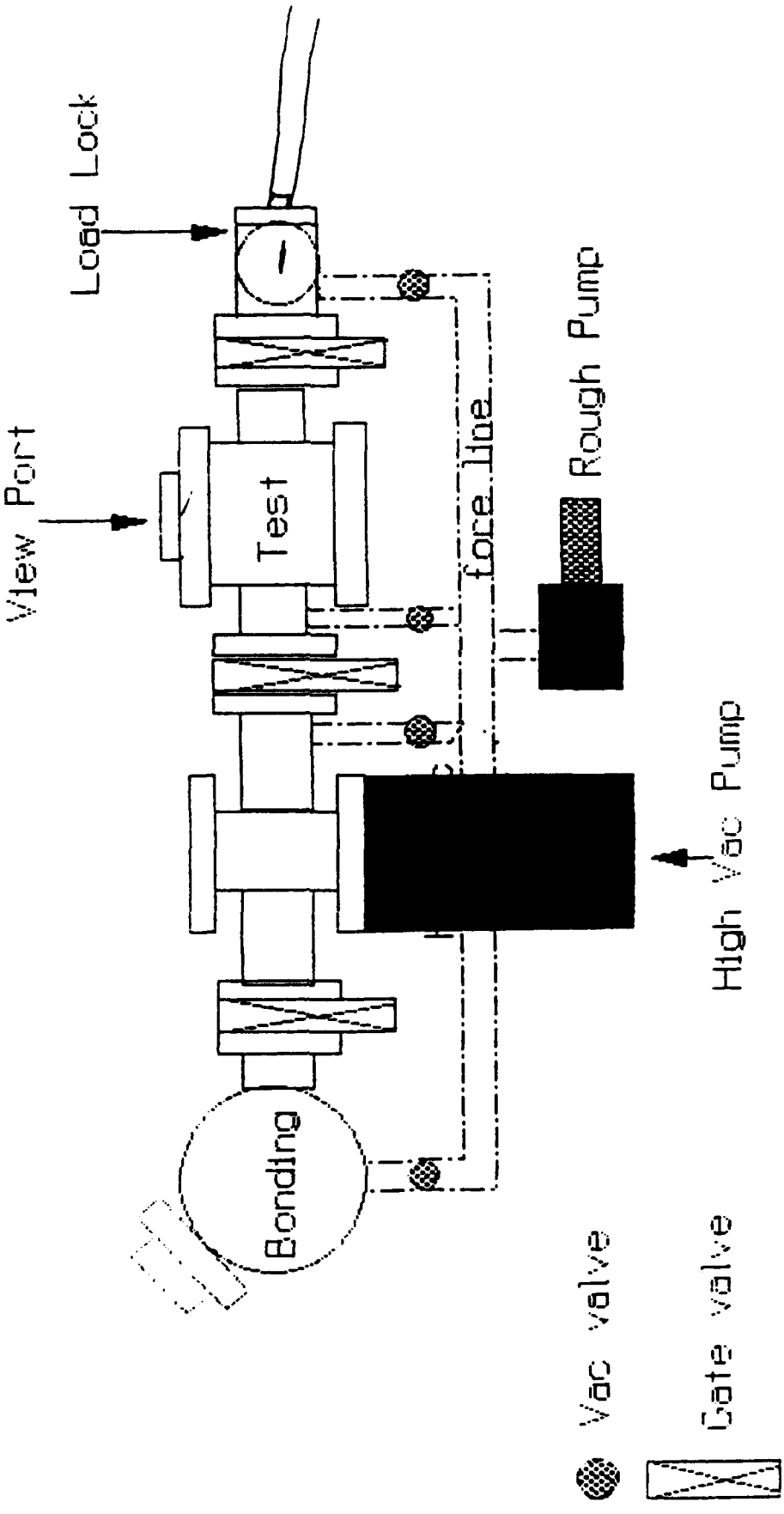
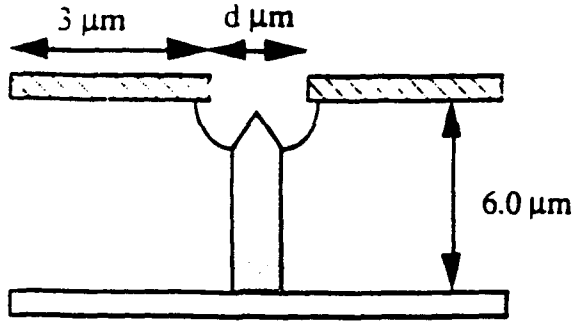
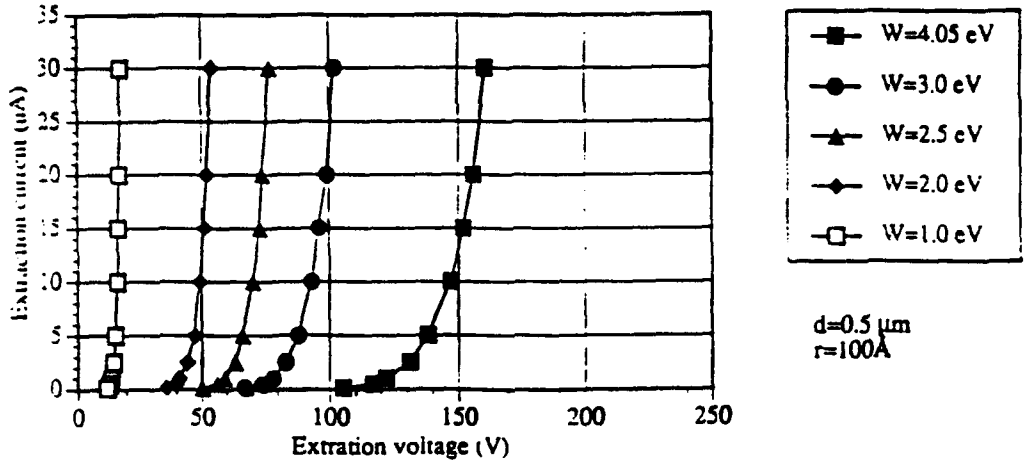
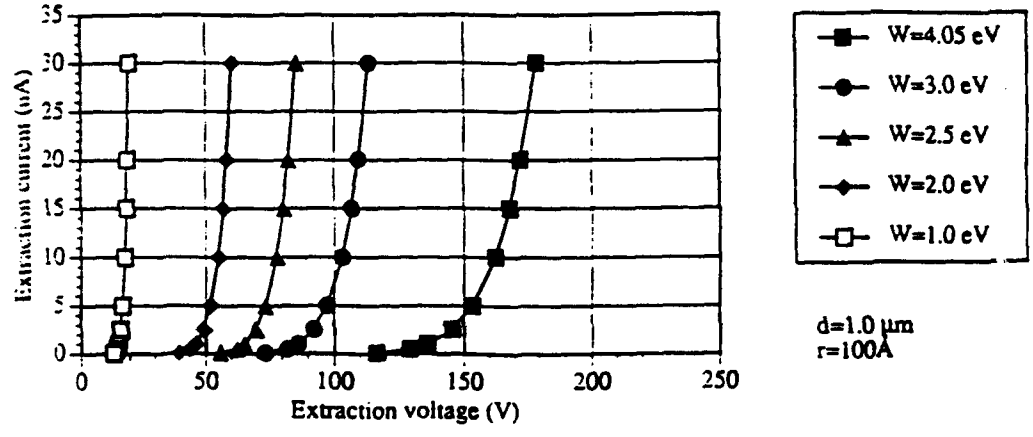

Load Lock
View Port
Test
Bonding
fore line
Rough Pump
High Vac Pump
Vac valve
Gate valve

Figure 3
Projected Emission Curves for Different Diameter Gate Openings







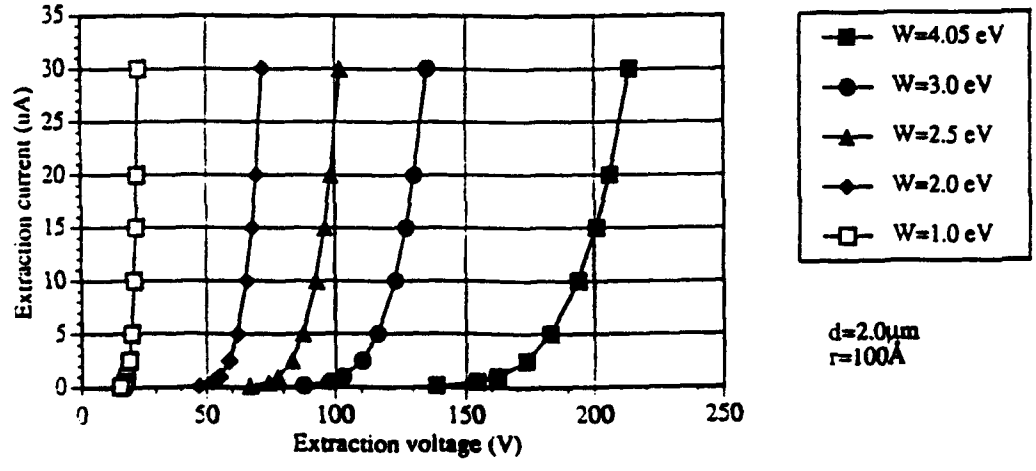
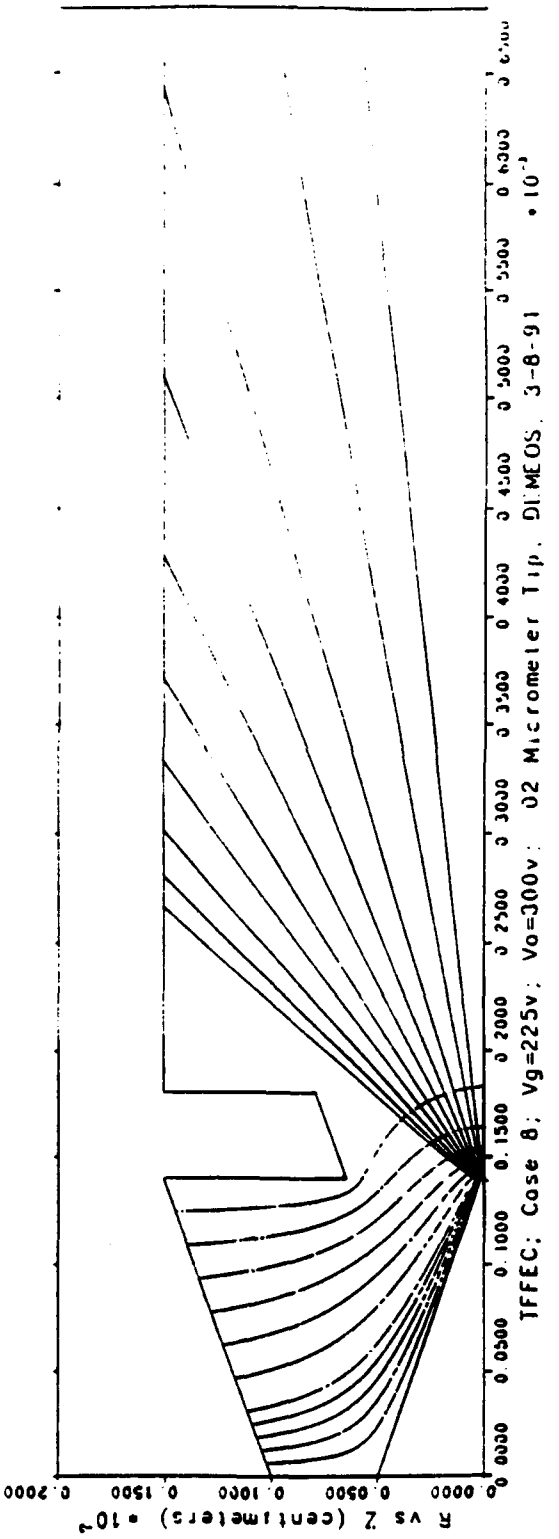


Figure 4


R vs Z (centimeters) • 10⁻²
0.0000
0.0500
0.1000
0.1500
0.2000
TFFEC; Case 8; Vg=225v; Vo=300v; 02 Micromeler Tip, DI MEOS, 3-8-91
• 10⁻²