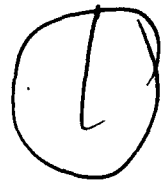

Quarterly Progress Report #6
1/1/93 - 3/31/93

Field Emitter Array RF Amplifier Development Project
Phase One, Cathode Technology Development
ARPA Contract #MDA 972-91-C-0028

Sponsored by:
Dr. Bertram Hui
ARPA / DSO

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Gary McGuire, Principal Investigator

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13. ABSTRACT (*Maximum 200 words*)

Sixth Quarterly R&D Status / Technical report for the Field Emitter Array RF Amplifier Development Project - Phase I, Cathode Technology Development. Effects of anode proximity on emission current capture is being examined in the electrical testing program. Two new processes for gate opening alignment are under development. Both eliminate the necessity of retaining the nitride caps on the field emitter tips through the entire processing sequence. Refinements in processing continue. Failure analysis of field emitter arrays from two lots was completed. Five mechanisms in two classes were identified as contributors to device failures: those mechanisms that destroyed working emitters, and those that prevented emitters from working.

In anticipation of continued ARPA funding for the field emitter project, revised budgetary and scheduling information was prepared. Design of the fabrication process and reticle set for the next generation of devices was begun.

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Quarterly Progress Report #6
(1/1/93 - 3/31/93)

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Effective Date of Contract: 9/09/91

Contract Expiration Date: 3/09/93

Contract Amount: Basic $1,178,466.00

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Title of Work: Field Emitter Array RF Amplifier Development Project
Phase One, Cathode Technology Development
ARPA Contract #MDA 972-91-C-0028

MCNC Field Emitter Array RF Amplifier Development Program

Phase One, Cathode Technology Development - ARPA Contract MDA 972-91-C-0028

Sixth Quarter - March 1993

Key Ideas

Develop microstructural field emission diodes and triodes with a cutoff frequency above 1 GHz, 5 A/cm^2 at < 200 V gate to emitter bias, and > 100 hour lifetime.

Reduce capacitance and increase transconductance of FEA devices to improve frequency response. Focus on development of tall emitter columns to minimize capacitance. Evaluate low work function materials for emitter surface coatings, reduce gate dimensions, and improve tip sharpening to increase transconductance.

Examine various test methods to permit characterization of more devices per test cycle. Evaluate test fixtures including controlled impedance RF test fixtures, vacuum tubes, and several methods of microencapsulation.

Develop a circuit model for our versions of the FEA device. Characterize the model for use in RF amplifier design and implementation. Establish model consistency across manufacturing methods and yield.

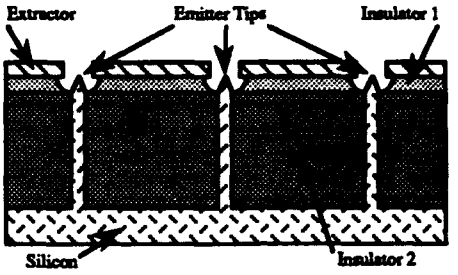
Major Accomplishments:

Electrical testing program continues at top speed. Effects of anode proximity on emission current capture at anode are under investigation.

Two new processes for gate opening alignment are under development. Both eliminate the necessity of retaining the nitride caps on the field emitter tips through the entire processing sequence. One requires alignment during an additional photolithography step, the other is self-aligning. Other refinements in processing continue.

Vacuum testing and microencapsulation bonding system installed at MCNC and fully operational. Bonding chamber modified to function as an additional test chamber to increase test throughput.

MCNC Silicon Field Emitter with Column



Major Milestones - This quarter and upcoming quarter:

Freeze the fabrication process flow to produce a standard process scalable to production levels. Systematically gather information for process control statistical analysis. Apply all acquired processing knowledge to future device runs to produce the best devices possible.

Fabricate devices capable of meeting frequency response requirement and providing current density of 5 A/cm^2 for > 100 hours. Improve yield on large arrays capable of meeting and exceeding total current requirements.

Revise budgetary and scheduling information in anticipation of continued ARPA funding for the field emitter amplifier project. Design process and new reticle set for the next generation of field emitter devices.

Field Emitter Array RF Amplifier Development Project
Phase 1, Cathode Technology Development

I. Executive Summary

Progress in research and development continues at all sites. MCNC's program continues at full speed with smooth transition of project personnel.

- Electrical testing of field emitter arrays fabricated at MCNC continues at all sites. Effects of anode proximity on emission current capture are being investigated.

- Two new processes for gate opening alignment are under development. Both eliminate the necessity of retaining the nitride caps on the field emitter tips through the entire processing sequence. One requires alignment during an additional photolithography step, the other is self-aligning.

- Refinements in processing continue. Better control of the anisotropic silicon etch for tip formation has been achieved. In-house chem-mechanical polishing is still under investigation as a method for wafer planarization. Other materials are being evaluated for use as the insulating layer between substrate and gate. Better methods for depositing evaporated oxides are being sought, and the oxides as deposited are being characterised

- Vacuum bonder and test system is operational. The bonding chamber has been outfitted for DC testing to improve test throughput, with electrical feedthroughs rated for 700 V at 10 A.

- Failure analysis of field emitter arrays from two lots was completed. Five mechanisms in two classes were identified as contributors to device failures: those mechanisms that destroyed working emitters, and those that prevented emitters from working.

- In anticipation of continued ARPA funding for the field emitter amplifier project, revised budgetary and scheduling information was prepared. Design of the process and reticle set for the next generation of devices was begun.

II. Milestone Status:

Task	Completion Date	
	Original	**Complete Expected**
Complete first diodes of each of the three device types: Horizontal, vertical, and trench. Deliver samples to NRL, NCSU, and Litton. (MCNC)	11/91	**11/91**
Prepare first pass device models and potential circuit models based on initial device IV data. (Duke, MCNC, and UNC-CH)	3/92	**11/92**
Down select RF FEA designs based on device performance predictions	3/92	**12/91**
Complete first generation of field emission IV curves for each of the device types fabricated along with initial electron trajectory data and electron time of flight data. (NCSU and MCNC)	3/92	**3/92 & Continuing**
Design and order vacuum sealing and test system (MCNC)	11/91	**12/91**
Modify Litton trajectory modeling programs for field emission. Initial macroscale high vacuum tube encapsulation of field emission cathodes. (Litton)	3/92	**11/91**
Complete second set of field emission diode device runs with column FEAs (MCNC)	3/92	**3/92**
Complete third series of gated column emitters with modifications for very low electric fields over gate emitter isolations to reduce gate leakage	-	**5/92**
Complete new mask set for half micron field emission devices. (MCNC)	5/92	**3/92**
Install vacuum sealing and test system (MCNC) MCNC set-up a temporary vacuum test system in a SEM (3/92)	3/92	**10/92**
Complete initial electron trajectory modeling and initial testing of macroscale tubes containing microstructural gated FEC diodes. (Litton)	7/92	**10/92**
Complete fabrication of first microencapsulated FEC transistors. (MCNC)	9/92	1/93 **POSTPONED**
Generate first pass transistor data from microencapsulated FE transistors. (MCNC, Duke, and Litton)	9/92	2/93 **POSTPONED**
Demonstrate microstructural FEA diode/open triode devices meeting device IV and g_m/C program requirements.	9/92	6/93
Determine priorities of future device development. Determine the primary amplifier design methodology from the three amplifier design approaches. (MCNC)	9/92	3/93
Complete design for first integrated FEC based RF amplifier and FEC tube RF amplifier based on device characterizations. (MCNC, Duke, and Litton)	3/93	3/93 **POSTPONED**
Complete second level models for FEC emission from surfaces treated in various manners. (UNC-CH)	3/93	3/93 **POSTPONED**
Complete testing of FEC electron trajectories, electron trajectory model verification. (NCSU, Litton)	3/93	3/93 **POSTPONED**
Determine packaging and cooling requirements for the prototype RF amplifier. (MCNC and Litton)	3/93	3/93 **POSTPONED**

III. Technical Progress:

1.0 Electrical testing and high-frequency performance measurements.

1.1 Electrical testing of both single and multiple tip arrays of gated column devices continues at MCNC and subprogram sites. A report on DC testing at NCSU is included as Attachment C.

1.2 Testing was performed in the ISI electron microscope vacuum chamber on a whole wafer from an earlier device lot with standard gated pyramid tips. These devices, which have a thick layer of LTO covering the gate metal, allow the anode to be placed within a few microns of the emitters without contacting the gate metal. The close proximity of the anode should eliminate space-charge effects. Some devices showed emission current collected at the anode. On the basis of these results, a more recent lot was brought to the point where the anisotropic etch and oxidation sharpening of the tips is complete.

2.0 Device processing.

2.1 A non-self-aligned method of processing the field emitter arrays past the point of column formation was proposed in response to a fabrication problem. Unlike previous runs, in this particular lot the columns and emitter tips had been formed by their respective etches and oxidation sharpened at an early stage in the processing, before the insulating layer of SiO2 had been deposited. The BOE etchbacks necessary for the insulator deposition tended to eat away the exposed thermal oxide directly underlying the nitride caps and thus strip them from the tips. With the caps gone at this stage of the standard process, there would be no means of creating self-aligned gate openings in the extractor metal.

The alternate method as proposed, referred to as "capless processing", is shown step-by-step in Figures 1 and 2. The first steps are the same as the self-aligned process; the silicon tips and columns are formed beneath nitride caps (Figure 1, Step 1). Then the nitride caps are stripped from the silicon field emitter tips immediately after the columns have been formed (Step 2). Once the caps have been removed from the tips, the insulator fill-in technique can proceed as usual to lay down the SiO_2 between the columns, without the necessity of maintaining cap integrity. After the insulator layer has been deposited and planarized at the desired thickness (at least as high as the columns), the locations of the tips should still be visible as bumps in the oxide (Step 3). The extractor metal is then deposited, followed by a layer of photoresist to form a gate mask (Steps 4 and 5).

The critical stage of the process is in forming this mask; in order to open up holes in the photoresist directly above the tips (using the same reticle level that had formed the original caps), accurate alignment to the still-visible bumps is required. Then the aligned mask is exposed (Figure 2, Step 6), and the exposed resist is developed away (Step 7). Once this has been done, the extractor metal covering the tips can be etched away to form the gates (Step 8); and the oxide surrounding the tips beneath the gate metal is removed to clear the emitter cavity (Step 9). Lastly, the photoresist is stripped away to reveal the complete gated column structure (Step 10). Two wafers were successfully fabricated using this technique, and electrical testing is underway.

The extractor metal chosen for use with this method is aluminum, due to the ease with which it can be isotropically etched. The chrome/tantalum/platinum metalization used in other field emitter devices can not be removed in such a direct manner using standard wet or dry etching techniques. Because of aluminum's low melting point, however, its use as an extractor metal imposes certain limitations on high temperature processing steps (such as oxide annealing or oxidation sharpening) and high temperature operation.

2.2 A new self-aligned process for structures that have no nitride caps is also under development. This technique uses deposited oxide remaining from the gate insulator backfill step to align the gate

opening during the metal deposition. This will guarantee a gated field emitter array with tips centered in the gate openings.

2.3 Some work was done to improve the uniformity of the anisotropic Si etch. Better control of the tip formation process should result.

2.4 Several different approaches were tested to achieve wafer planarization using Chem-Mechanical Polishing in-house. These approaches included varying the slurry concentration, lubricant, polish speed, and type of polishing pad. It was observed that a hard polishing pad (glass) with lapping oil as the lubricant is most effective.

2.5 Experimentation into the use of LTO (LPCVD) oxide as the gate insulator material continued. Limited success was achieved due to the BOE wet etch rate not allowing the oxide on the sides of the columns to be removed. Different anneal conditions were tested in an attempt to obtain better quality evaporated oxide and prevent cracking of oxide film due to thermal stress. The index of refraction of the backfill evaporated oxide was measured, and the BOE/RIE etch rates characterized.

3.0 Vacuum testing and microencapsulation bonding system.

3.1 The bonding chamber was modified so that electrical testing can take place in both system chambers simultaneously. This will improve test throughput.

3.2 Repairs on the bonding chamber heating circuit have proceeded to the point where new wiring had been successfully installed and the thermal shielding surrounding the heated wafer press reassembled into its original configuration. The system was pumped down and the new heating circuit tested to a maximum temperature of 553 °C in a simple up-and-down heating run. An examination of the wiring the next day revealed no damage due to melting of the insulation. A second test was performed, similar in nature, in which the temperature peaked at 792 °C. Once again, a post-test examination revealed no damage to the wiring. Many interior metal surfaces were discolored, however, indicating some sort of undesirable evaporation of the metal in the heating coil or the bonding chuck may be taking place. In the future, the temperature will be held to under 200 °C whenever possible.

4.0 Other Developments.

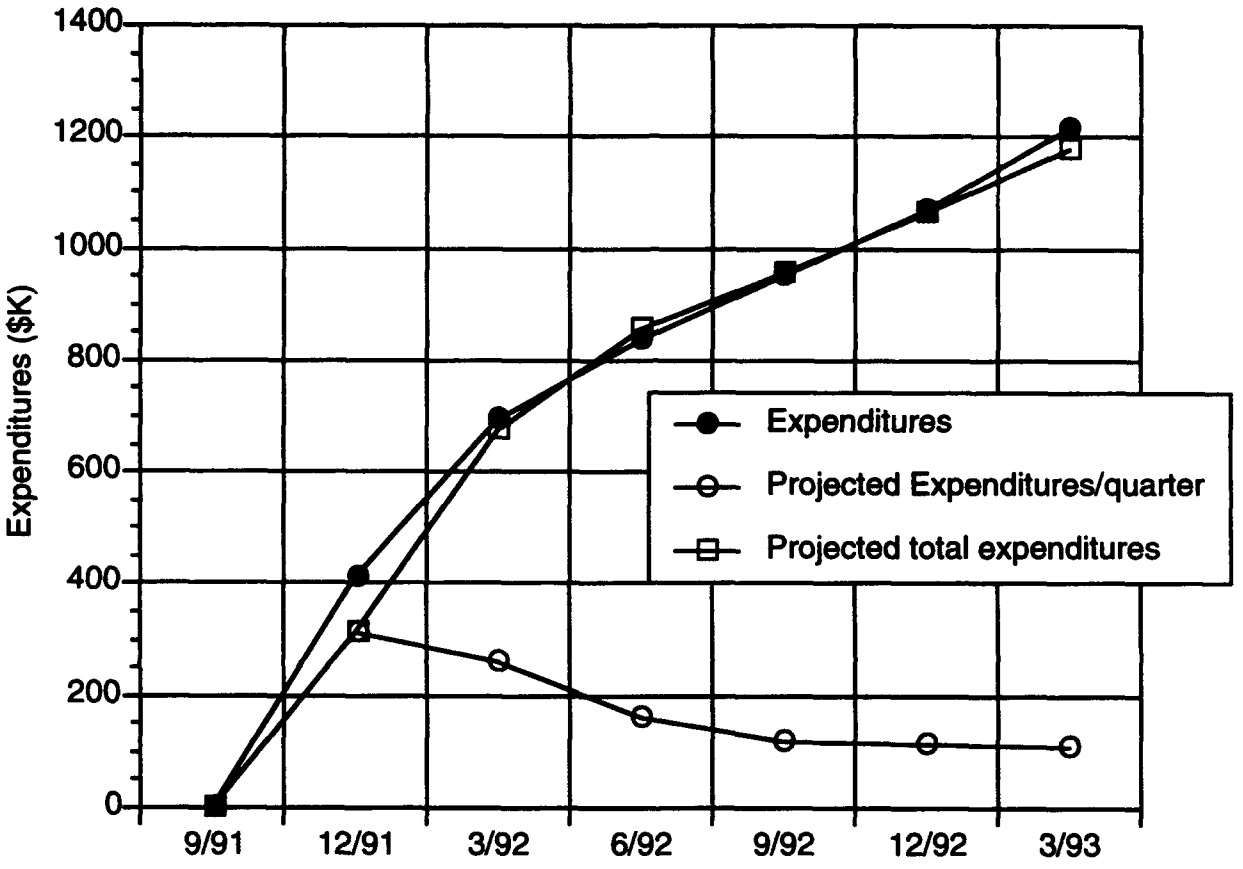
4.1 The first failure analysis of field emitter arrays from two lots was completed. Five mechanisms were identified as contributors to device failures, in two classes: those mechanisms that destroyed working emitters, and those that prevented emitters from working. Arc discharge between the anode and gate destroyed several devices. The gate metal on some devices melted in such a way as to increase the diameter of the gate hole opening. In these cases, the tips were not damaged, but the field intensity at the tips dropped below that required for electron emission.

In other devices, Frenkel-Poole leakage through the gate insulator layer prevented the application of sufficient gate voltage to produce the necessary fields at the tip. Some devices had tip radii too large to produce the necessary field magnification. Yet other devices appeared to have a residual oxide layer on the tips. All of these failure mechanisms are being studied, and solutions are being developed through process integration and control.

4.2 In anticipation of continued ARPA funding for the field emitter amplifier project, revised budgetary information was prepared. The project deliverables and schedules were revised accordingly.

Design of the new reticle set for the next generation of devices was begun. A group design review was carried out and the design finalized. The process design was started and a process review with MCNC personnel external to the program will be scheduled.

IV. Fiscal Status



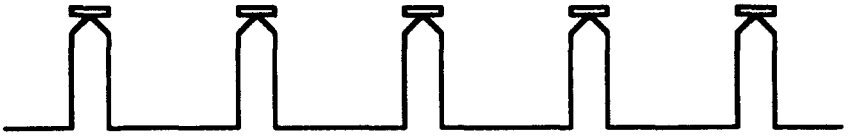
Expenditures this quarter (1/1/93 - 3/31/93)	$149,181.98
Total expenditures to date (9/09/91 - 3/31/93)	1,216,926.59
Contract Amount (Basic)	$1,178,466.00

V. Problem Areas

Perhaps the main problem facing the MCNC field emitter program at this time is fabrication yield and uniformity. Information gathered from all the processing done up to this point will be applied to future runs to produce the best possible devices meeting the ARPA performance criteria. Higher current density will be achieved by reducing the emitter tip pitch (tip-to-tip spacing), producing more uniform sharp tips, and using a hexagonal rather than rectangular grid for the emitter tips. Higher total current will be achieved by using larger arrays with improved yield.

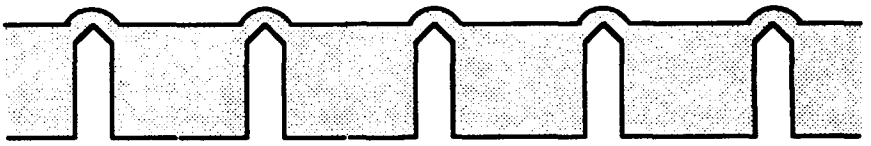
VI. Visits and Technical Presentations

Several closed meetings were held between MCNC staff and its subcontractors. One presentation on this project was made outside the direct program participants during the contract time period covered by this report. This presentation was the ARPA program review held at MCNC on 04 February, 1993. A process design review with MCNC personnel external to the program is planned, but a specific date has not been set. A presentation at the Vacuum Electronics Review in late June is also planned.

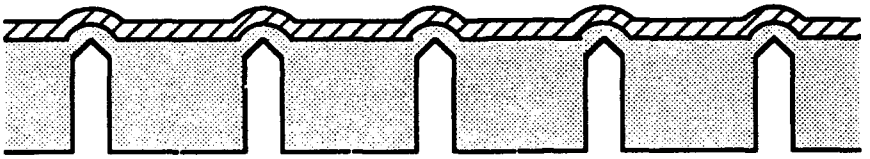


Step 1: Form silicon tips beneath nitride caps

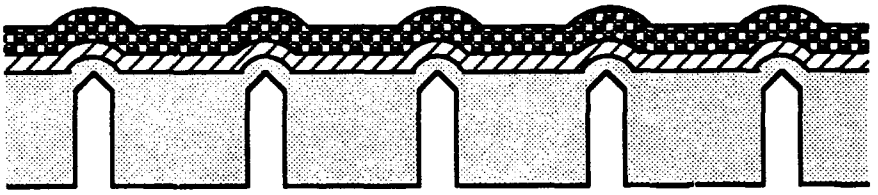
Step 2: Remove nitride caps



Step 3: Deposit oxide layer

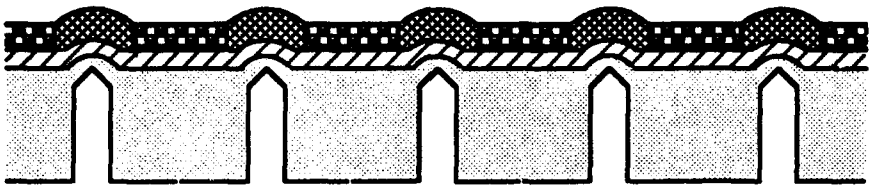


Step 4: Apply gate metal layer

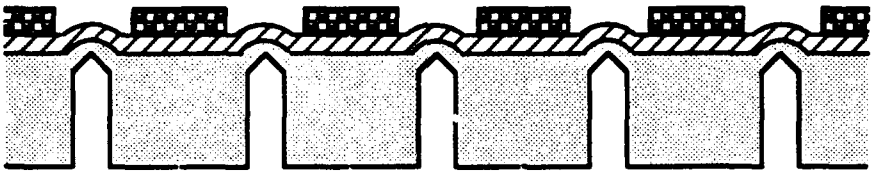


Step 5: Apply photoresist layer

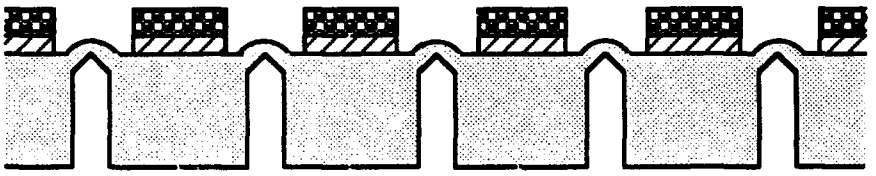
Figure 1: Capless processing, steps 1 through 5.



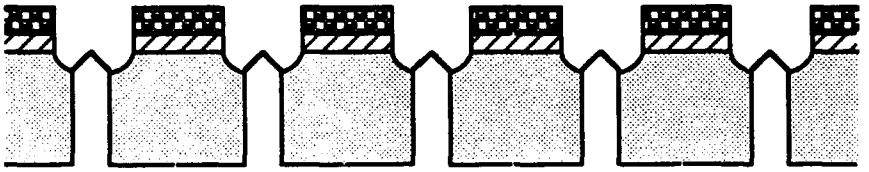
Step 6: Align mask and expose photoresist



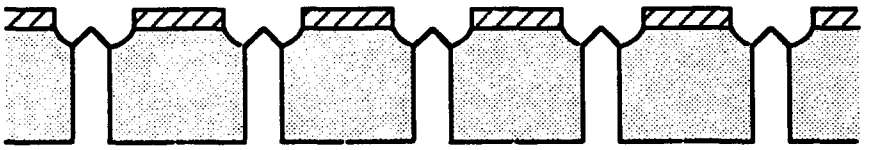
Step 7: Develop and strip photoresist



Step 8: Etch gate metal



Step 9: Clear emitter cavity



Step 10: Strip photoresist

Figure 2: Capless processing, steps 6 through 10.

LIST OF ATTACHMENTS

Attachment A: Duke subcontract progress report, 2 pages

Attachment B: Litton subcontract progress report, 16 pages.

Attachment C: NCSU subcontract progress report, 5 pages.

Attachment D: UNCC subcontract progress report, 1 page.

DUKE UNIVERSITY SUBCONTRACT SUMMARY FOR JANUARY THROUGH MARCH 1993

Joseph E. Mancusi and William T. Joines
Duke University, May 25, 1993

The research from the Duke University subcontract for the first quarter of 1993 includes building of RF test equipment, high-frequency device measurement, electromagnetic simulations of the device geometries, and determination of critical parameters for device processing. Our goals are to obtain the highest possible performance from the current device geometries developed at MCNC, identify design parameters for which it is important to control during the device manufacturing, and gain an understanding of how processing deviations affect the performance of large arrays. Work continues on developing measurement and testing procedures and refining the device model. In the analysis, numerical electromagnetic techniques are used to calculate the field enhancement factors and capacitances of particular device geometries. Several areas of research have been identified as crucial to achieving and exceeding the goals of the program.

In order to aggressively proceed with testing, additional high–frequency test fixtures have been built. Two additional test fixtures similar to those described in Quarterly Progress Report #5 have been constructed. This brings the total number of high--frequency test fixtures built at Duke to three. The additional test fixtures reduce the turnaround time in the measurement phase as new wafers can be installed in the test fixtures while testing is proceeding on another device in the vacuum chamber. In addition, a new set of bias tees has been constructed. All are currently in use for high-frequency testing of the field emitter arrays. The RF performance of each of these new test fixtures and the bias tees is found to be satisfactory for measurement at and around 1 GHz. Device testing results from the first quarter of 1993 are described elsewhere in this report.

Electromagnetic simulations of the devices have helped the process designers at MCNC identify areas of the production which are particularly important for device operation, especially for large arrays. Differences in some geometrical parameters, radius of curvature at the top of the emitter pyramid for instance, can cause large deviations in emitted current from tip to tip. A study is being developed to help quantify these effects for large arrays based on experimental data and simulations. It is expected that some of the results of the study will be reported in the next quarterly report. In terms of evaluating and predicting the performance of field emitter arrays, critical information includes the expected deviations from the nominal device geometry. Parameters which are especially important include the emitter tip radius of curvature, the alignment of the tip with the gate metallization, and the gate metallization aperture. The tip alignment includes centering of the tip in the aperture (horizontally) as well as alignment of the top of the emitter pyramid with the center of the gate metallization. Deviation of any geometrical parameter from its nominal value will affect the performance of a large array. Due to changes across the wafer, some arrays will undoubtedly have higher collected current levels for the same operating voltage.

In an array with devices whose performance varies, it is quite possible that some devices may emit no or few electrons while others have a very large electron current. While it may not be possible to have all of the emitters in an array produce the same amount of current, the evaluation of the effects of different parameters should identify which processing steps are particularly crucial for the performance of large emitter arrays. It is important to see if we can predict the number of devices that are on using the typical variations in the device geometries. Such use of a priori knowledge will significantly simplify the analysis. In addition, this understanding may explain the low emitting areas reported by some in the literature.

The ability to produce pedestals under the emitter pyramids has allowed MCNC to significantly lower capacitance while marginally enhancing the field enhancement factors of the geometry. Although there are significant design trade-offs associated with the additional processing steps, the addition of an emitter pedestal and the increase in the spacing between the gate and the substrate are important steps for improving the operating frequencies of MCNC's devices. Modeling efforts show a good probability for success of the column structures for achieving modulation at 1 GHz.

The basic model presented in previous quarterly reports is currently under evaluation. A careful study using experimental results along with the simulations should provide a comprehensive understanding of field emitter arrays. The addition of a significant amount of experimental data from future high-frequency testing on single devices and large arrays will be used to evaluate the model. Statistical analysis of the identified device parameters mentioned above may be included in the model. A better appreciation of critical device parameters should result from this study.

ATTACHMENT B

FIELD EMITTER ARRAY OF AMPLIFIER DEVELOPMENT PROJECT

SPONSORED BY
DARPA
CONTRACT # MDA 972-91-C-0028

PRIME CONTRACTOR	:	MICROELECTRONICS CENTER NORTH CAROLINA
SUB CONTRACTOR	:	LITTON ELECTRON DEVICES DIVISION
SUB-SUBCONTRACTOR	:	LITTON SOLID STATE DIVISION

PROGRESS REPORT
PERIOD : DECEMBER 1992 - FEBRUARY 1993

PREPARED FOR
W. DEVEREUX PALMER
MICROELECTRONICS CENTER NORTH CAROLINA

PREPARED BY
DIPTEN DEB
LITTON ELECTRON DEVICES DIVISION

OUTLINE

I INTRODUCTION

II CHIP MEASUREMENTS

III DC TESTING

IV RF TESTING

V PERSONNEL

1. INTRODUCTION

In early December of 1992, Litton Electron Devices Division (LEDD) received 5 chips from MCNC for DC & RF testing. These chips were sent to LEDD along with their maps and device layout. The location of the devices were marked on the chip map with various numbers which represented the number of emitters at those particular locations. A letter was sent along with the chips by the Program Manager Mr. C.T. Sune, in which it was stated that the chips with numbers may work and the devices that were not marked would not work. After careful study of all the chip maps, it was found that the chip #191604 had the maximum number of active devices. Six devices were selected and properly marked on the map for identification. This chip along with the map was handed over to Litton Solid State Division (LSSD) for thinning, cutting and mounting on suitable carriers and installing the anodes and external leads

During the prior tests, several questions were raised regarding cleanliness and handling of these chips. In order to avoid confusion the following instructions were given to LSSD.

(a) Thin down the wafers to suitable thickness as required. As these are field emission devices, all precautions shall be taken to avoid accumulation of any foreign materials in the emitter-gate structures.
(b) Scribe the wafer into individual chips.
(c) Pick six chips that have been identified on the map which have maximum number of emitters.
(d) Install the chips in the grounded grid configuration i.e the grid shall be properly grounded, the cathode will be the input and the anode will be the output
(e) Die attach to the gold plated Kovar carrier and attach ribbons to the input and output.
(f) Deliver the chips in boxes which do not have any silicone compound.

In order to perform accurate S-O-L calibration, LSSD was also requested to mount four calibration standards on similar carriers. These four carriers were for calibrating the (i) Short (ii) Open (iii) Load & (iv) Through conditions.

LSDD delivered all the six chips properly mounted and four calibration standards in the first week of February, 1993. As these chips were mounted in the grounded gate configuration, the old test set up could not be used. A new conflat flange having provision for testing nine devices at one time, was prepared with only two terminals for each device, one being for RF input and the other for RF output; the grid terminal was grounded in all cases. In order to perform this test three flanges are required. All these flanges were hydrogen fired at 400 °C for 15 minutes to get rid of all oil and other residues.

Five chips and four calibration standards were mounted along the circumference of the flange and they were properly numbered. The chip layout configuration is shown in Figure 1. A close up view of the chip mounting on the flanges is shown in Figure 2.

Particular attention was paid to minimize the mismatches along the transmission lines in question (between connector to the chip input and between chip output to the connector. The input and output terminals were laser welded to their respective windows and the entire assembly was prepared for pumping down. A Vac-Ion pump of 2-liter capacity was permanently attached to the assembly, to ensure that the pressure inside the assembly maintains a pressure below 10^{-8} Torr. The assembly was baked at 200 °C and simultaneously connected to an exhaust system for pumping down. After 24 hours of exhaust operation, when the pressure inside the assembly stabilized at 10^{-8} Torr, the assembly was pinched off and removed from the exhaust station. The Vac-Ion pump was energized and no increase of power supply current could be seen as in the previous experiment.This phenomenon indicated that there was no emission of gases and the chips have been cleaned and handled very carefully this time.

As it was intended to characterize the devices at RF frequency of 1 GHz, and as these chips need to be biased at high DC voltages, two Bias-Tee circuits (Model No ZFBT-4R2G from Mini-Circuits), one for the input and the other for the output were purchased.The Bias-Tee network isolates the RF measuring equipment from the DC supplies. These networks cover from 10 MHz to 4.2 GHz, but cannot handle the necessary high bias voltage. As the bias voltage in this case may exceed 400 volts, the DC blocking capacitors were replaced from 0.1 uF ceramic at 30 volts to 0.1 uf metallized milar at 600 volts. As the current in this case is extremely low, it was not necessary to change the inductor.

The S-Parameter characteristics of both the Bias-Tee networks were measured and plotted with the help of 8510B Network Analyzer. The instrument was first calibrated for S-O-L (short, open & load) - transmission, reflection and isolation condition using SMA connector (3.5mm). The S-Parameter characteristics of the two bias-tee networks are shown in Figure 3 & Figure 4.

II. CHIP MEASUREMENTS :-

The S-Parameters characteristics and corresponding Smith chart of Sample #1 and Sample #2 were also measured and plotted with the help of the network analyzer. This was done to find out the input, output and coupling capacitances of these devices. From these characteristics, the input impedance, output impedance and phase angle were noted. The S-Parameter plots and corresponding Smith Charts as obtained from the network analyzer are shown in figure 5 to figure 8. A very short program for Super-Star was written, and the phase angle values were inserted. The program was asked to optimize the circuit and determine the capacitance values. The short program is as shown in Table 1. The program calculated the capacitances and plotted the corresponding Smith Chart. The Smith-Chart as obtained from the Super-Star program is shown in Figure 9.

By comparing the charts obtained from HP 8510B and from the Super-Star program we find that the two plots are very similar as expected. After optimization the program

settled to specific capacitance values for C1, C2 & C3. The values obtained are C1 = 1.551871 pF, C2 = 0.400216 pF and C3 = 0.619718 pF. The above capacitance values indicate that the input capacitance (grid to cathode) is much higher than the output capacitance (anode to grid). This is quite expected as the grid is placed very close to the cathode whereas the anode is installed further away from the grid. These tests were performed without any DC bias applied.

III DC TESTING :-

The entire assembly was then connected for DC testing as shown in figure 10. The Bias-Tee networks were not used for these tests. A 1 MΩ carbon resistor was connected in series with the input and a 20 M Ωcarbon resistor was connected in series with the output circuit. A floating oscilloscope was connected across the 1 MΩ resistor. The Oscilloscope's vertical scale was set at 5 mV per division. If there happen to be emission of 1 nano amperes then the oscilloscope will indicate 1 milli volt. The ground connection was very carefully verified several times so that any sort of noise may not disturb the measurement. Grid cathode voltage was gradually increased to 100 volts and the scope was monitored. No indication of any emission could be seen. The grid cathode voltage was set at 100 volts. The anode voltage was then gradually increased while monitoring the oscilloscope. The voltage was raised to 400 volts and no indication of any emission could be observed. The pressure inside the assembly was maintained below 10^{-8} Torr as indicated by the current of the Vac-Ion pump supply. Similar tests were repeated to all the five chips and no emission could be seen in any of them.

As none of the devices showed any sign of life, the matter was discussed with Dev Palmer of MCNC. Mr Palmer mentioned that these devices were never tested before, so it was quite possible to arrive at the results as we obtained. The number of emitters as mentioned on the maps were counted while looking under a microscope.

IV RF TESTING

All necessary preparations were made to conduct RF testing. As the devices did not emit any electrons, this test could not be done.

V PERSONNEL

Jeff Panelli of Solid State Division under the guidence of Weiming Ou, performed all the thinning and mounting of the devices. The tests were conducted at LEDD. Helmut Bacher assisted in calibration of the bias tee networks and S-Parameter measurements. The tests were performed by Dipten Deb under supervision of John Siambis and guidence of R.S.Symons.

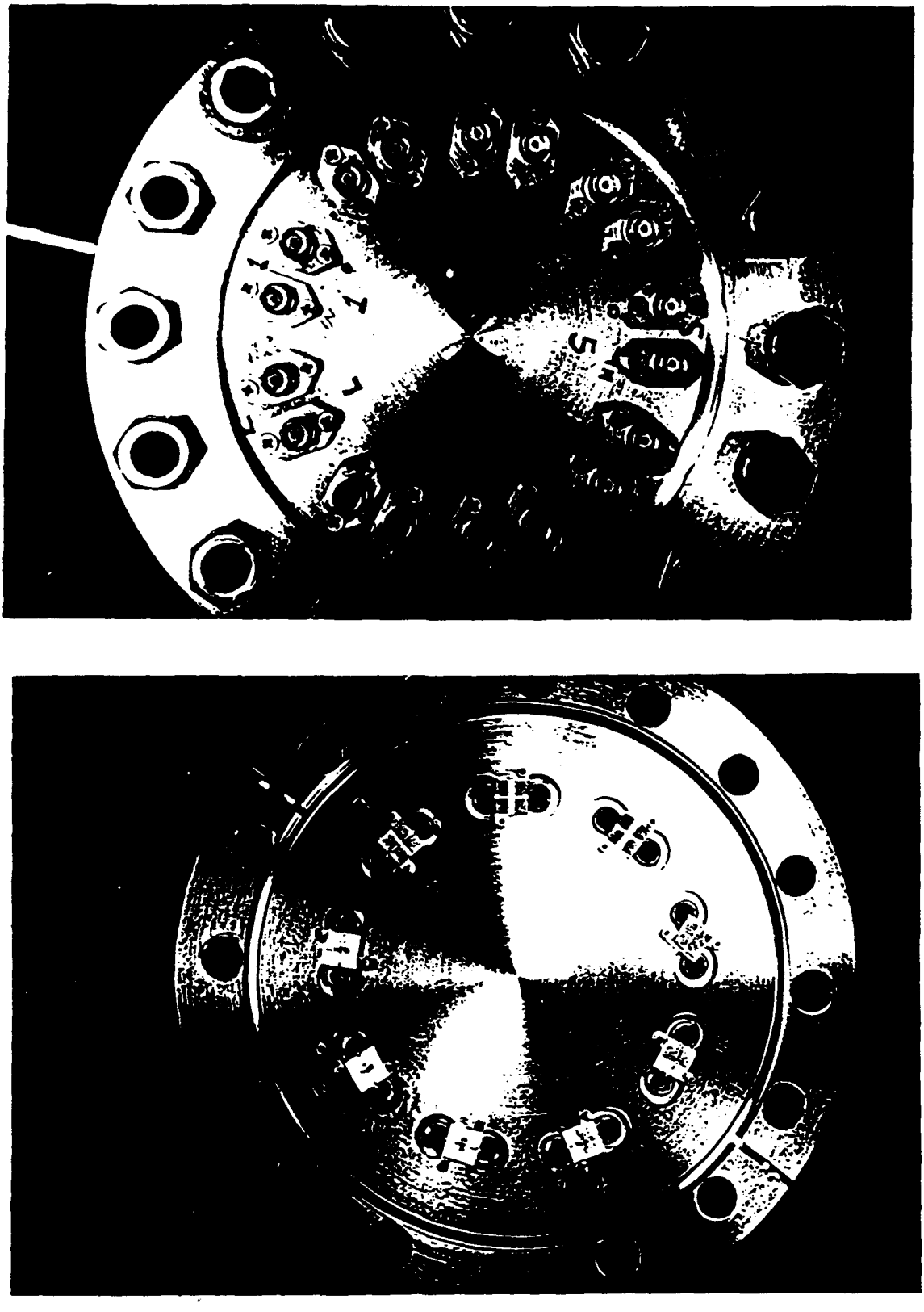


Figure 1

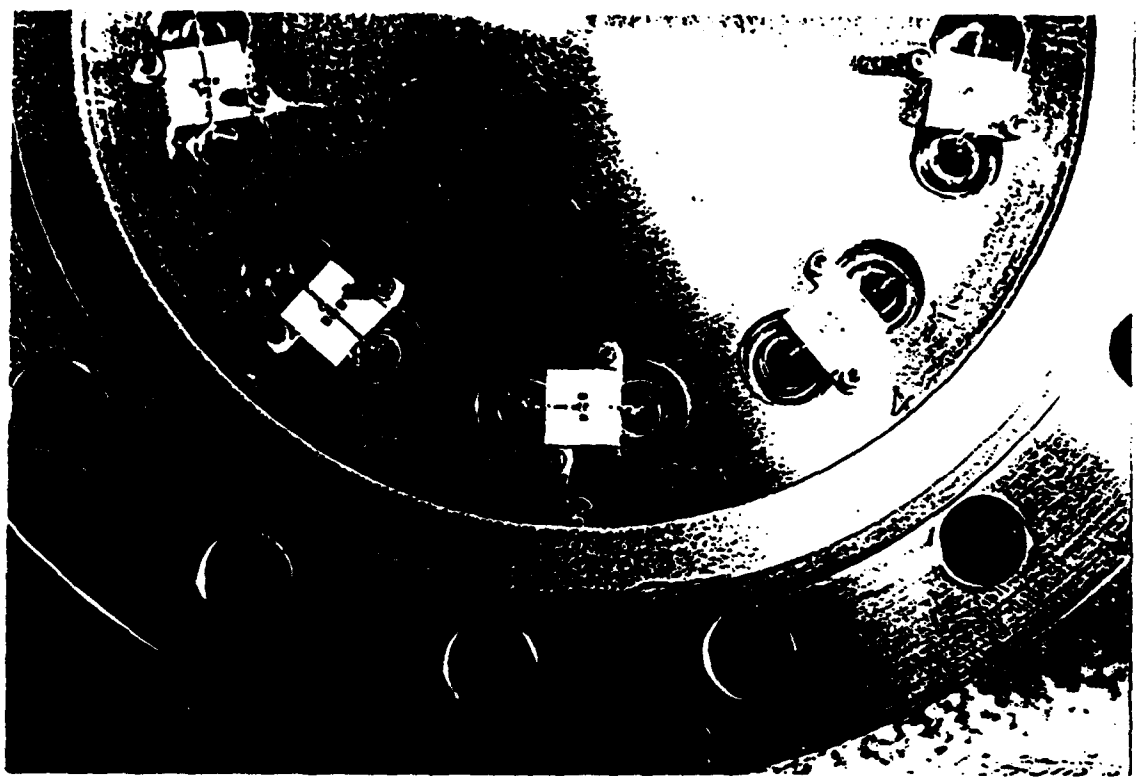
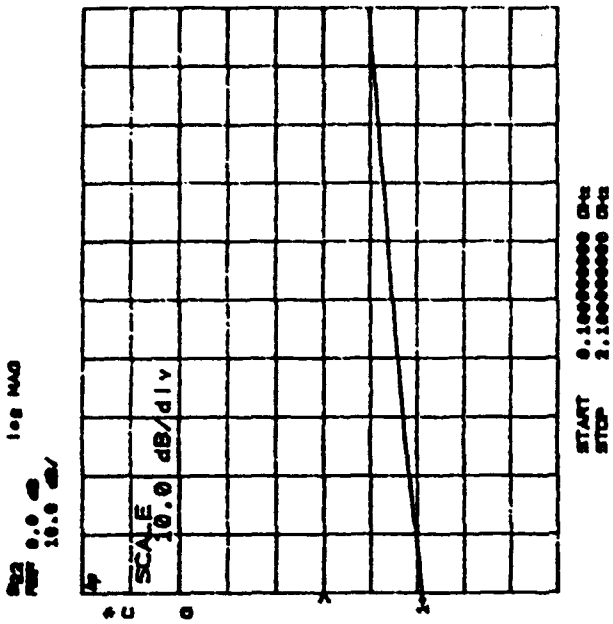
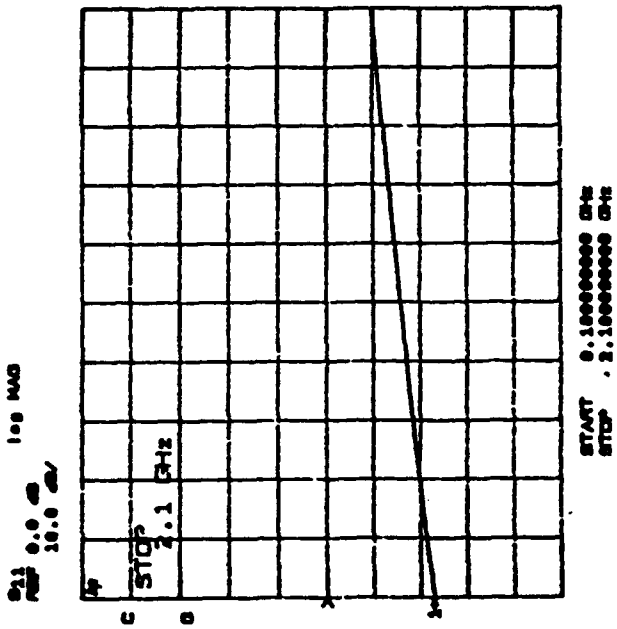
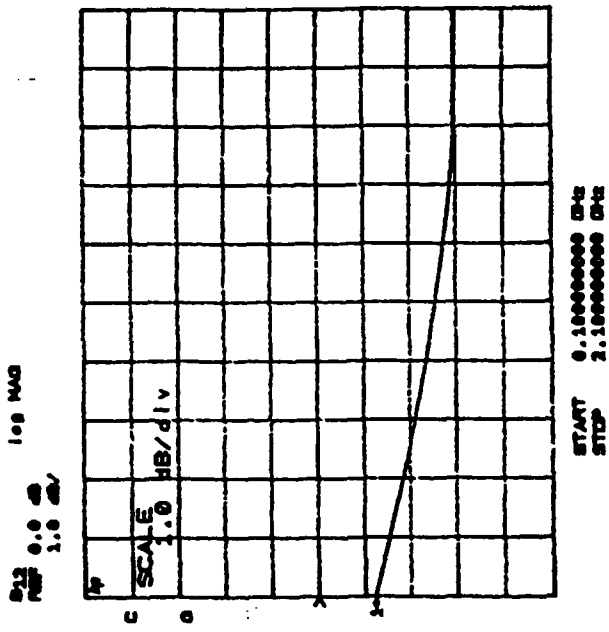


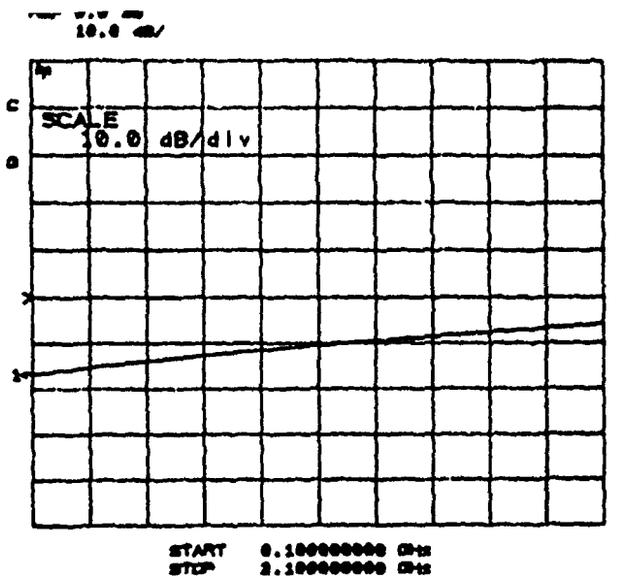
Figure 2

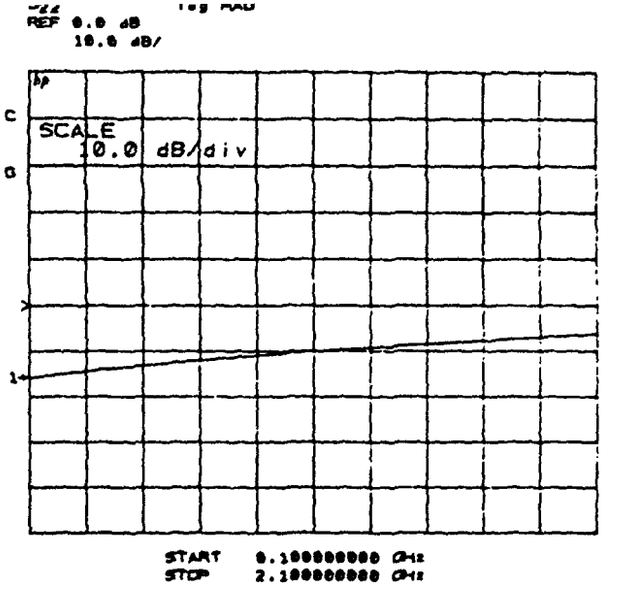


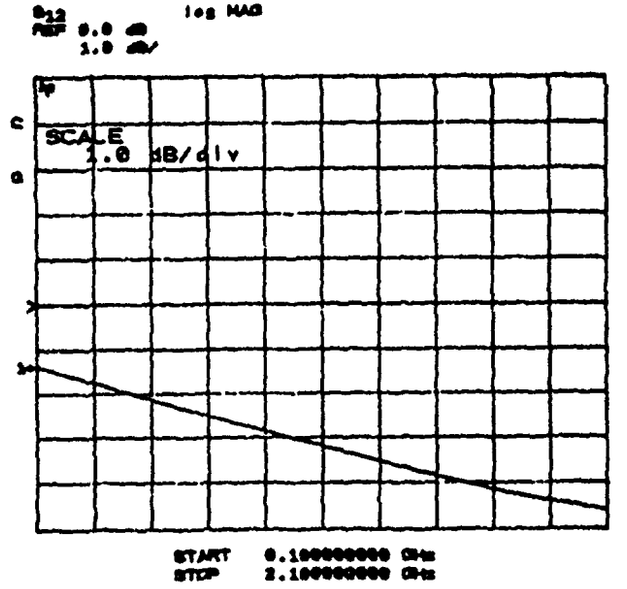




S-Parameter Characteristics of Bias-Tee Network 1







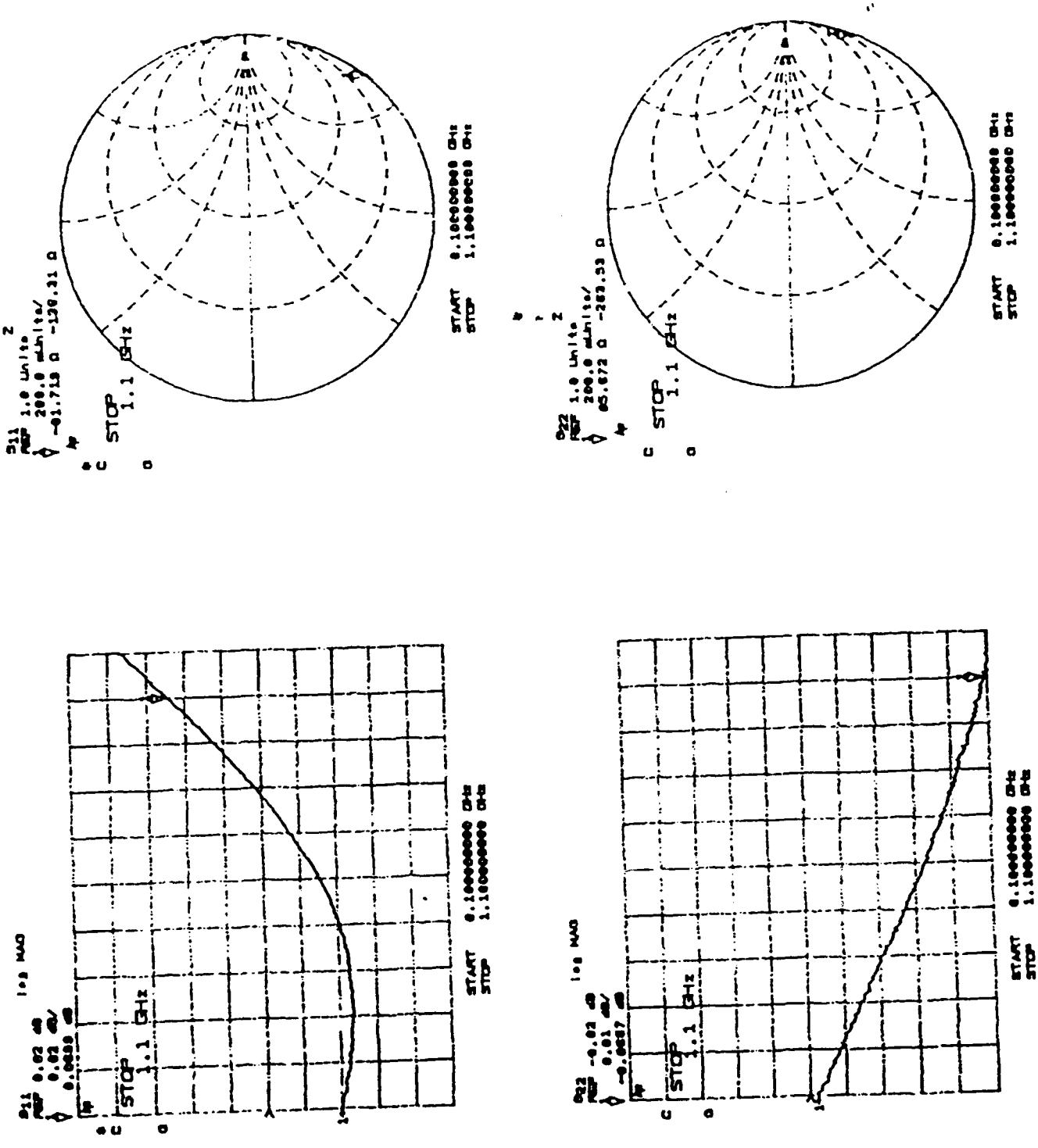
S11 = V1r/V1i + Input reflection Coefficient

S21 = V1t/V1i = Forward transmission coefficient

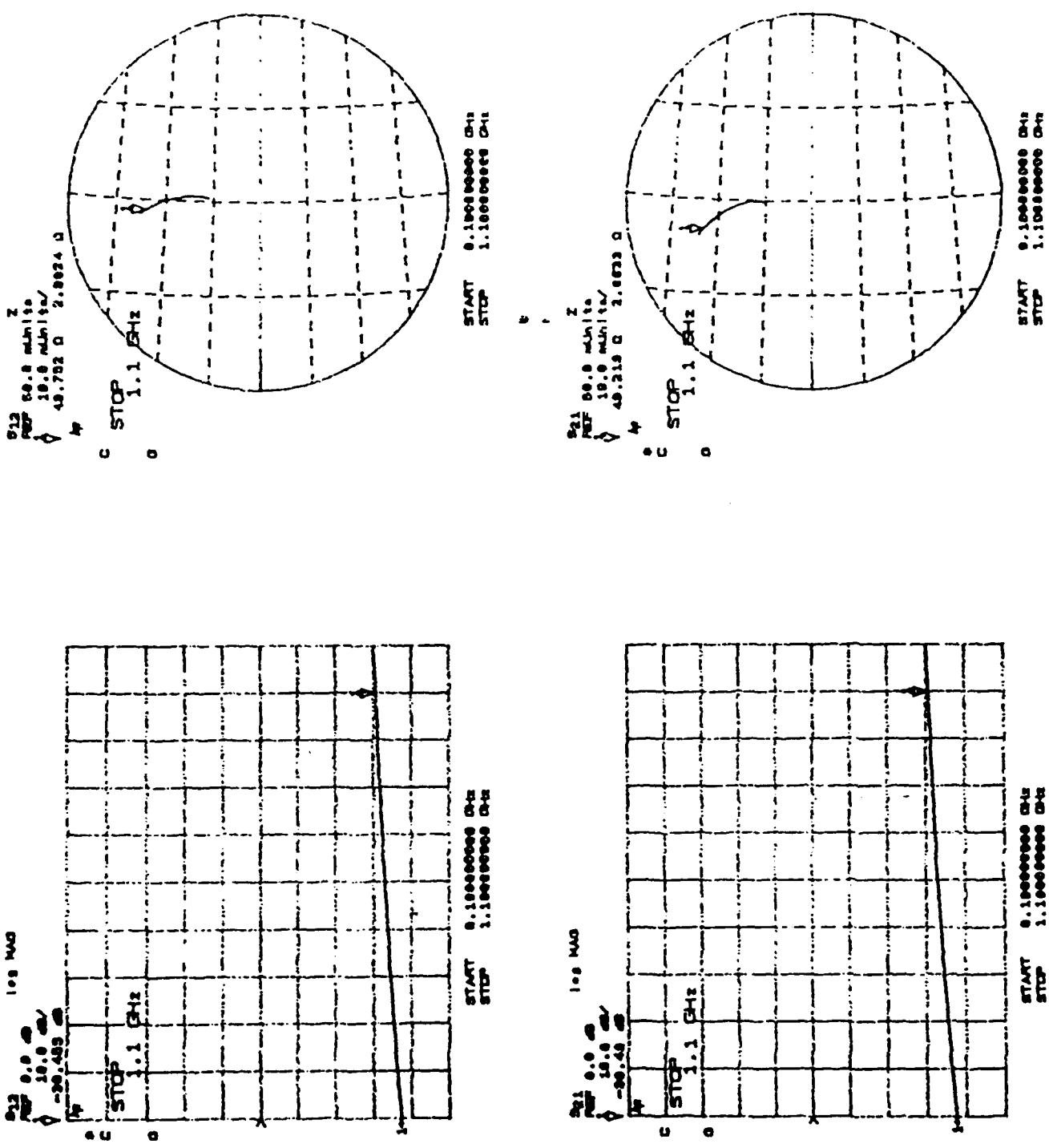
S22 = V2r/V2i = Output reflection coefficient

S12 = V2t/V2i = Reverse transmission coefficient

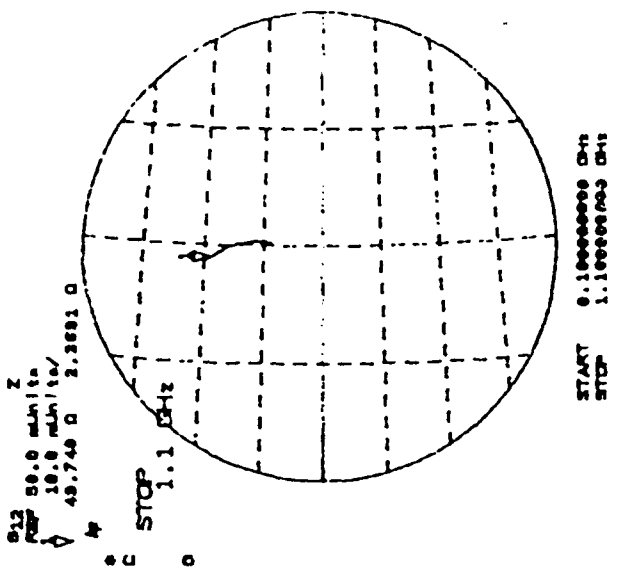
S-Parameter Characteristics of Bias-Tee Network 2

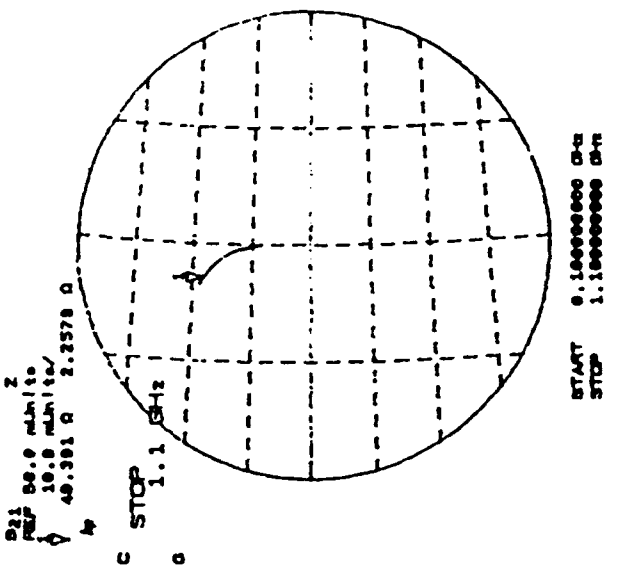


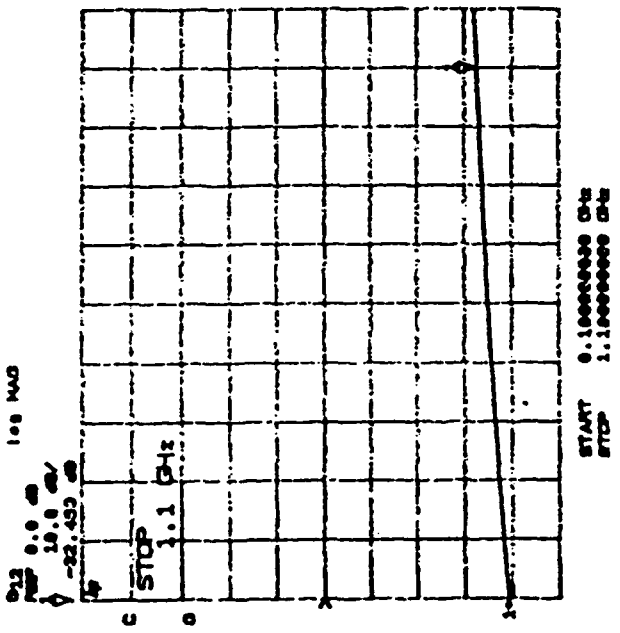
S-Parameter characteristics & Smith Chart of Chip 1

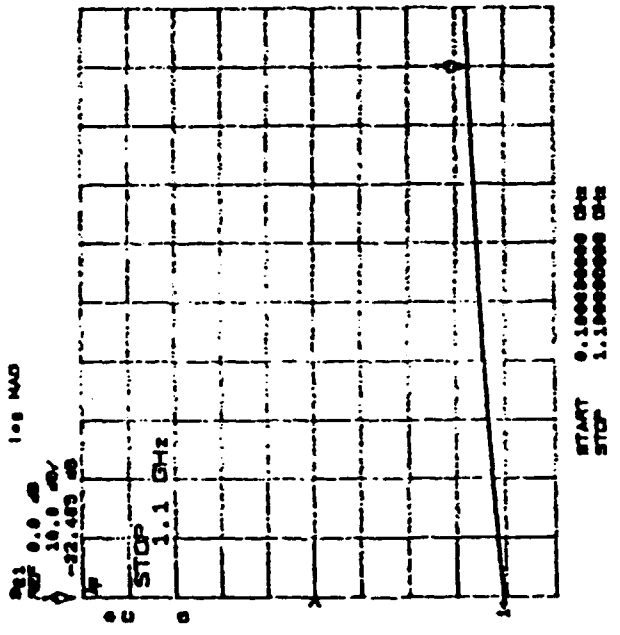


S-Parameter characteristics & Smith Chart of Chip 1

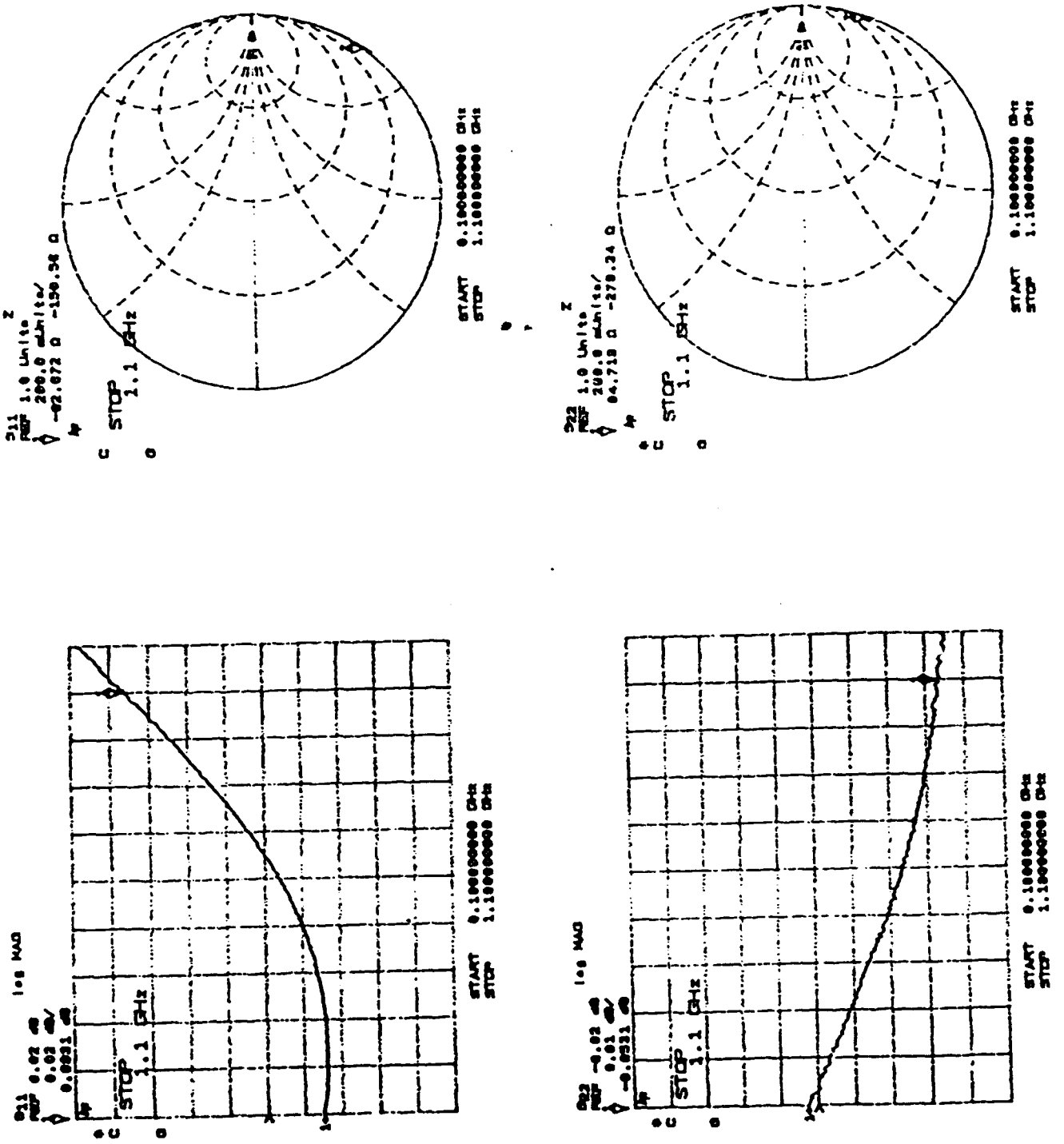








S-Parameter characteristics & Smith Chart of Chip 2



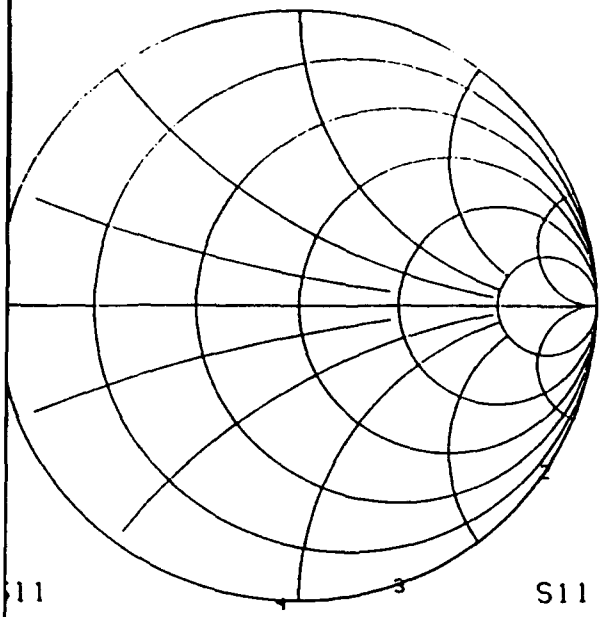
S-Parameter characteristics & Smith Chart of Chip 2

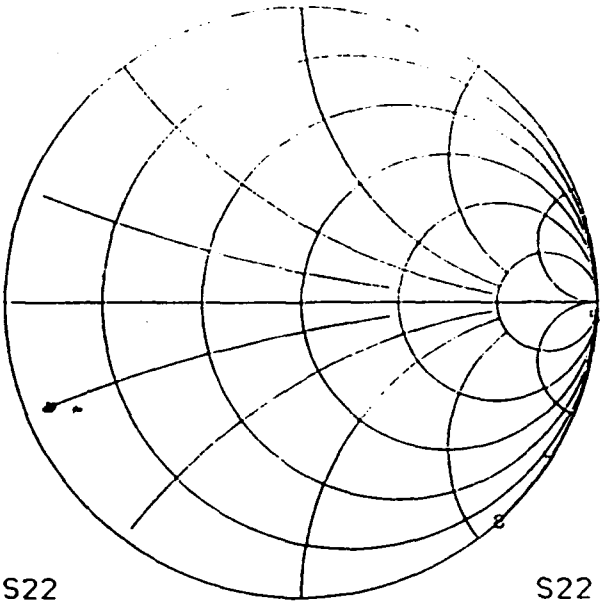
```
This file is : fed.ckt

Thu Mar 18 14:47:46 1993

circuit
cap 1 0 ?1.551871 NAME=C1
cap 1 2 ?0.0400216 NAME=C2
cap 2 0 ?0.619718 NAME=C3
DEF2P 1 2 FED
window GRAPH
FED (50)
smh s11
smh s11
smh s22
smh s22
freq
swd 100 2100 100
OPT
1999 2001 P11=-90
1999 2001 P22=-45
1999 2001 S21=-30
```

Table 1

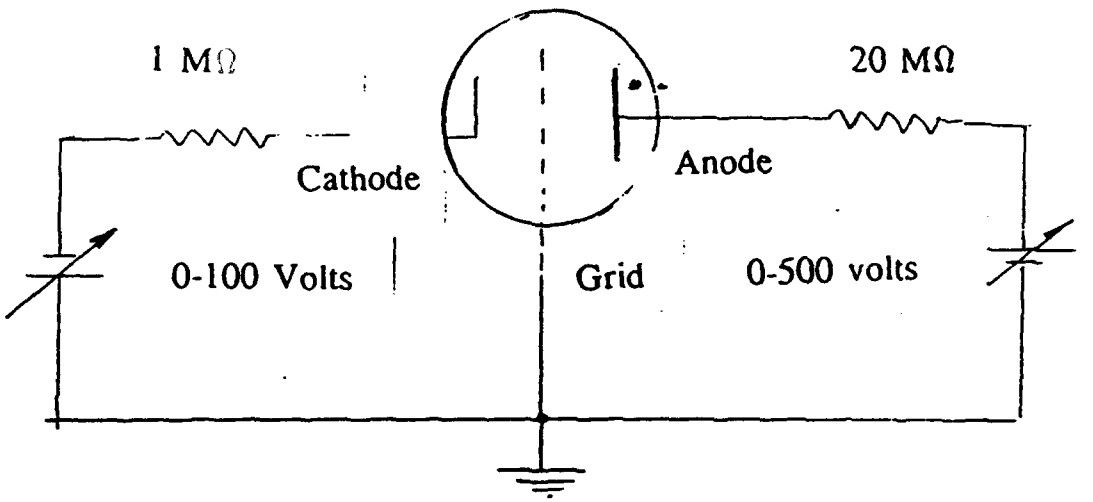




	S11			S22			
	600	1400	2100	100	600	1400	2100
e-05	-.000897	-.003339	-.004851	-2.8e-05	-.000895	-.003336	-.004849
e-05	-.000897	-.003339	-.004851	-2.8e-05	-.000895	-.003336	-.004849

Figure 9

D.U.T (Field Emission Device)



D.C TEST SET-UP

Figure 10

ATTACHMENT C

Quarterly Progress Report #6
(1/1/93 - 3/31/93)

John J. Hren and Jiang Liu
Department of Materials Science and Engineering,
North Carolina State University, Raleigh, NC 27695

I. Executive Summary

NCSU has been fully involved during this quarter in the effort to achieve the goal of high emission current and high frequency operation specified by the DARPA program. Researchers from Duke University and MCNC have gathered at NCSU a number of times to perform this joint testing. The column structural silicon field emitter devices, which were fabricated at MCNC, have shown significant improvements on the emission current as well as the reliability according to the prescreening test at NCSU. Several field emitter devices were also investigated by scanning electron microscope (SEM) before and after emission current-voltage (I-V) measurements.

II. Technical progress

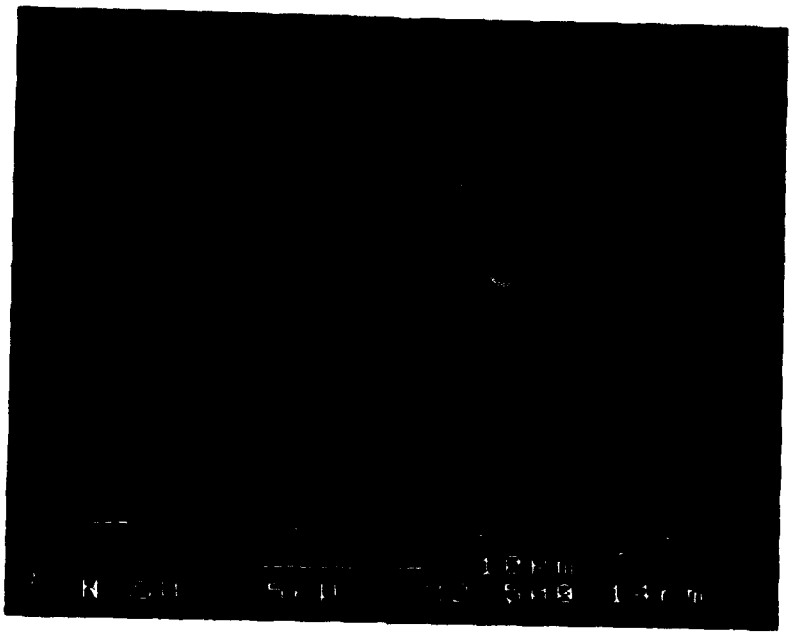
Experiments for the field emission I-V measurement and the high frequency modulation have been shifted from the imaging atom probe FIM/FEM system to the new multipurpose FIM/FEM analytical system whose vacuum chamber provides larger operating space and faster pumping speed (Fig. 1). High frequency compatible cables and feedthroughs have been installed into the system for the purpose of RF testing. The experiments were usually carried out at room temperature and a vacuum background of low 10^{-8} to 10^{-9} Torr. Prescreening of emitter devices by optical microscope and DC current-voltage measurement were performed before each high frequency modulation test.

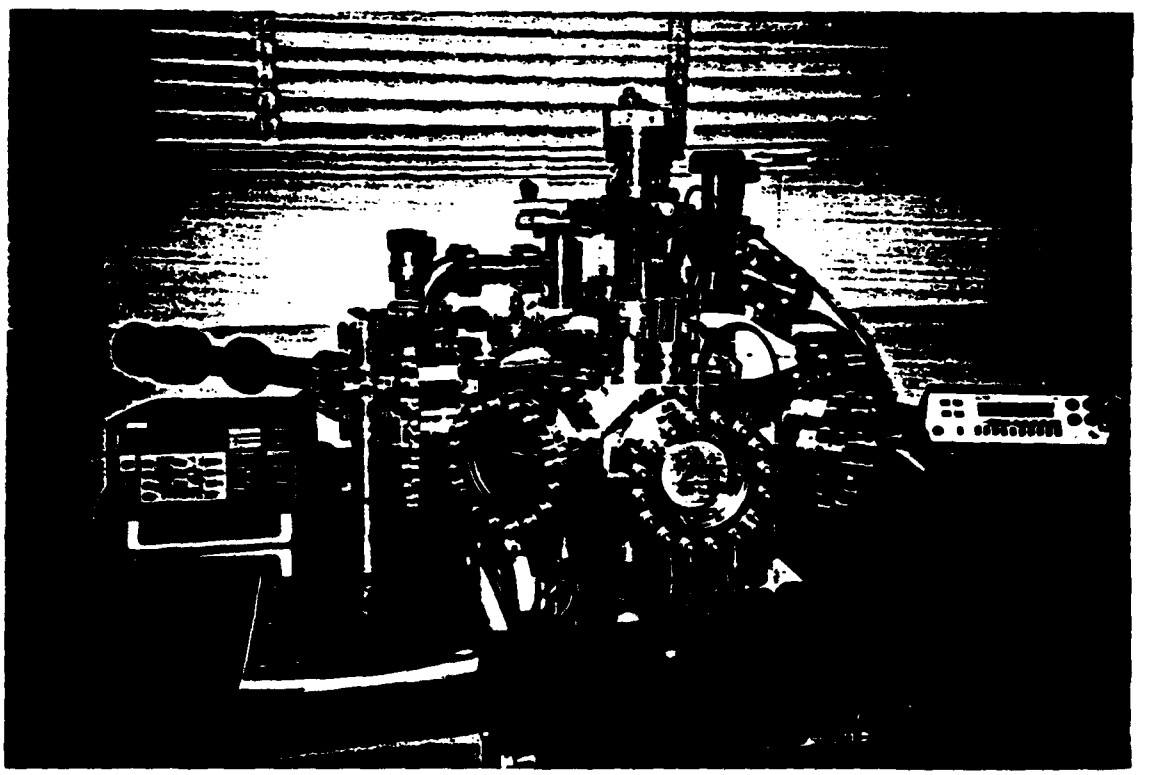
DC I-V characterizations have been carried out both on single and small emitter arrays. With a turn-on gate voltage around 80 volts, single emitter devices usually give an average emission current of 2 μA at gate bias below 200 volts. Stable and repeatable emission currents from 5x5 and 10x10 emitter arrays have also been measured. Fig. 2 shows a typical measured DC I-V curve from a 5x5 emitter array. High

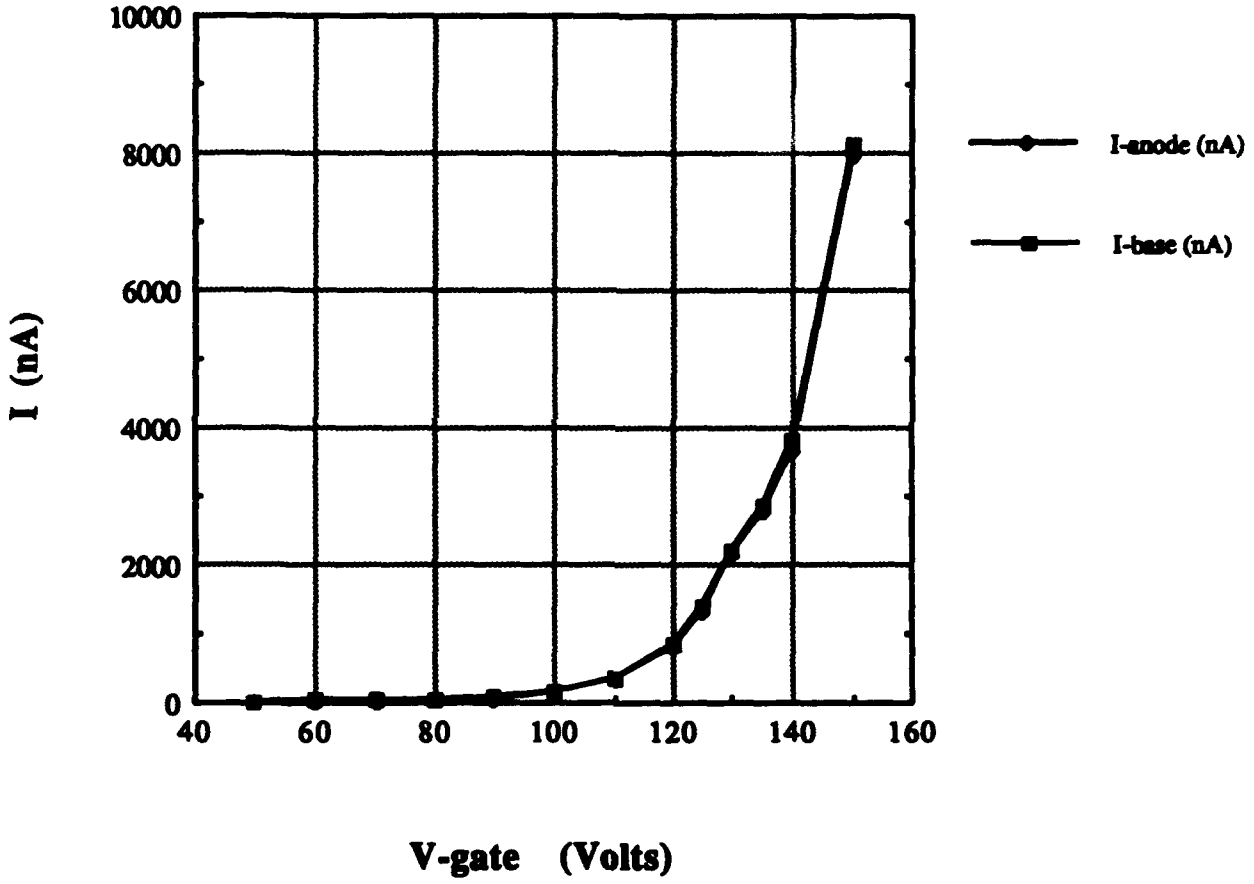
frequency modulation has been achieved on this and other similar devices. As the gate bias gradually increased, we were able to detect higher emission currents from 10x10 and larger arrays. However, unstable emission was usually observed especially during high current operation. This could be caused by the non-uniformity of the device which results in different operating field distribution throughout the entire emitter array.

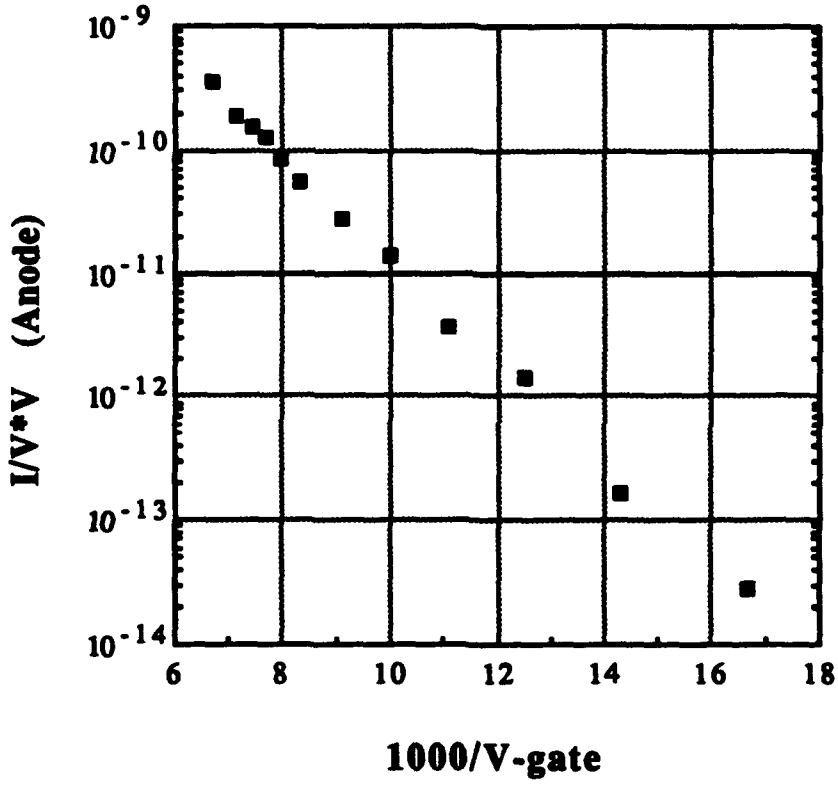
Under stable DC operating conditions, RF tests were carried out by injecting a high power RF signal into the emitter gate. A Tektronics oscilloscope with multi-GigaHertz signal processing capability was used to collect the modulation signal. At an anode operating current above 1 μA, a 1 GHz sine wave signal applied to the gate electrode was clearly detected from the anode. This modulation signal dropped to background noise level as the gate bias was withdrawn. This RF modulation test has been repeated a considerable number of times on several devices. Obviously, 1 GHz is not the limit of operation frequency for current devices. Since we were targeting the goal for the phase I, we have only focused on this frequency range.

ATTACHMENT C






10000
8000
6000
4000
2000
0
I (nA)
40
60
80
100
120
140
160
V-gate (Volts)
I-anode (nA)
I-base (nA)


10-9
10-10
10-11
10-12
10-13
10-14
I/V*V (Anode)
6
8
10
12
14
16
18
1000/V-gate

QUARTERLY PROGRESS REPORT NO.4

DARPA MCNC/ LITTON PROGRAM

R. F. GREENE, PhD, and K, DANESHVAR, PhD .
UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE, NC 28223

NOISE IN VACUUM MICROELECTRONIC MICROWAVE AMPLIFIERS

May 1, 1993

1. We have placed orders for electronic picoammeter and nanovoltmeter, etc for measurement of emission noise as a function of residual gas species, to determine the systematics of effects of residual gases of different species. Methods of work function lowering and passivation will be investigated.

2. A system of preferential deposition of very thin metallizations on the emission area of emitter cones, either metal or semiconductor, has been devised, in order to reduce field penetration and thereby raise field enhancement and transconductance. The method, was demonstrated by Greene and Zahavi NRL in 1987, involvesthe use of an elaytrolyte containing the ions of the metal to be deposited. Deposition occurs under laser illumination by means of electrons photoexcited into the electrolyte. Deposition thus does not occur on insulator surfaces, and has nanoscale resolution. A test sample, designed and FAXed to MCNC for fabrication, will be used to demonstrate that surface flashover or leakage does not occur.

3. The new theory of tunnelling which removes the untestable approximations of the classical WKB method of Fowler-Nordheim, has been worked out to the point where the more exact theory requires that the usual classical image term be replaced by a convergent and physically reasonable image term. An experimental method for measuring image potentials versus voltage, which has never before been attempted for field emitters, has been designed. It involves measurments of photoelectron threshholds using channel plates and fiber optics. This work has been accepted for presentation at the 1993 International Vacuum Microelectronics Conference

4. We have developed the first quantitative theory of flicker noise for field emission. The theory makes use of the fact that emission currents are strongly perturbed by adatoms, raising the current for outwardly positive dipoles (e.g. barium) and lowering the current for outwardly negative dipoles(e.g oxygen or sulfur.) When a current-decreasing adatom is adsorbed at an emission site, the decreased current lowers the ohmic loss inside the emitter lowering the temperature and shifting the adsorption-desorption kinetics toward increasedadatom coverage. When this feedback mechanism is imposed on the emission spectrum, a 1/f noise spectrum results, whose amplitude is dependent on the emission area. This may provide a method for estimating the actual emission area. This work will also be presented at the 1993 International Vacuum Microelectronics Conference