Quarterly Progress Report #4
7/1/92 - 9/30/92

Field Emitter Array RF Amplifier Development Project
Phase One, Cathode Technology Development
DARPA Contract #MDA 972-91-C-0028

Sponsored by:
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DARPA/DSO

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Fourth Quarterly R&D Status / Technical report for the Field Emitter Array RF Amplifier Development Project - Phase I, Cathode Technology Development. Progress in research and development continues at all sites. Efforts at standardization and improvement of processing techniques for columnar gated emitters are producing good results. MCNC's program continues at full speed with the smooth transisiton of project leadership.

RF testing has shown modulation of a 0.36 GHz carrier signal by a field emitter device fabricated at MCNC. An improved RF test system has been designed, constructed, and is in use. Testing of columnar devices proceeds on an aggressive schedule.

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Title of Work: Field Emitter Array RF Amplifier Development Project
Phase One, Cathode Technology Development
DARPA Contract #MDA 972-91-C-0028

MCNC Field Emitter Array RF Amplifier Development Program

Phase One, Cathode Technology Development – DARPA Contract #MDA 972-91-C-0028

Fourth Quarter – September 1992

Key Ideas

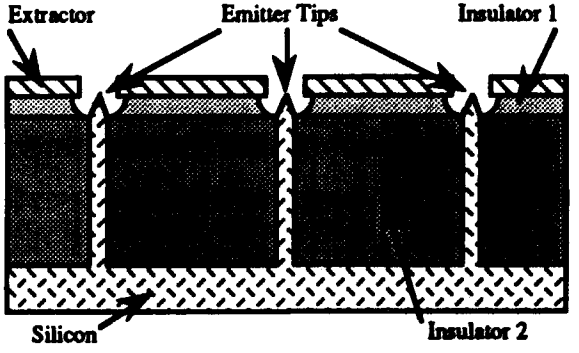
Develop microstructural field emission diodes and triodes with a cutoff frequency > 1 GHz, 5 A/cm^2 at < 200 V gate-to-emitter bias, and > 100 hour lifetime.

Reduce capacitance and increase transconductance of FEA devices to improve frequency response. Focus on development of tall emitter columns to minimize capacitance. Evaluate low work function materials for emitter surface coatings, reduce gate dimensions, and improve tip sharpening to increase transconductance.

Examine various test methods to permit characterization of more devices per test cycle. Evaluate test fixtures including controlled impedance RF test fixtures, vacuum tubes, and several methods of microencapsulation.

Develop a circuit model for our versions of the FEA device. Characterize the model for use in RF amplifier design and implementation. Establish model consistency across manufacturing methods and yield.

MCNC Silicon Field Emitter with Column



Major Accomplishments

RF testing has shown modulation of a 0.36 GHz carrier signal by a field emitter device fabricated at MCNC. Improved RF testing system designed, constructed, and in use. Testing of columnar devices proceeds on an aggressive schedule.

Major advances achieved in fabrication of columnar devices. Improved methods of oxide deposition allow oxide fill between columns of up to 12 μm, yielding finished columns up to 8.6 μm. Planarization by chemical-mechanical polishing ensures consistent emitter-to-gate spacing. Advances in photolithography permit gate aperture design targets of 0.6 and 1 μm.

Vacuum test and microencapsulation system delivered and qualified to meet vacuum specifications. Installation of test fixturing in progress.

Major Milestones – This quarter and upcoming quarter

Demonstrate amplitude modulation of a 1 GHz carrier signal with a field emission triode with gate-to-emitter bias < 200 V. Measure current density 5 A/cm^2 for > 100 hours.

Construct microencapsulated FEA and test. Produce microencapsulated devices with vacuum test and microencapsulation system. Fully outfit test chamber for DC characterization and RF testing. Automate data collection.

Deliver gated columnar structures to subprogram at Litton for further testing in amplifier modules. Deliver samples with diamond-like coatings to NRL for testing.

Field Emitter Array RF Amplifier Development Project
Phase 1, Cathode Technology Development

I. Executive Summary

Progress in research and development continues at all sites. Efforts at standardization and improvement of processing techniques for columnar gated emitters are producing good results. MCNC's program continues at full speed with the smooth transition of project leadership.

- Recent RF testing of a single field emitter tip in the new vacuum test system at North Carolina State University showed amplitude modulation of a 0.36 GHz carrier. Unmodulated carrier amplitude varied with varying gate DC bias, indicating amplification. The NCSU system is currently capable of measuring DC transfer characteristics and RF performance of field emitter devices. The electrical connections to the test chamber are being modified to allow operation at higher frequencies. A new test fixture has been designed that will allow testing of multiple devices with a single vacuum cycle. The fixture is designed with a self-contained anode, and maintains a constant impedance of 50 Ω from the test equipment connections to within a few millimeters of the device. Several of the test fixtures have been constructed by researchers at Duke and now carry mounted devices ready for testing.
- Improvement in the method of oxide deposition in the gate-emitter isolation structure of the columnar emitters has produced up to 12 μm of oxide between columns, resulting in finished emitter column heights of up to 8.6 μm. Chemical-mechanical polishing of the deposited oxide is used to planarize the structure, ensuring consistent emitter tip-to-gate electrode spacing. Two methods of nitride cap formation have been developed so that a wide range of polishing precision can be accommodated.
- Construction of columnar emitters with smaller and smaller gate dimensions requires extremely accurate photolithography as the feature size approaches the wavelength of the light used to expose the wafer. Experience with large numbers of prototype devices at MCNC have allowed gate opening design targets of 0.6 μm and 1 μm, with column heights of greater than 5 μm. These devices will be completed and tested in the next quarter.
- The microencapsulation and testing system designed and built for the DARPA field emitter program has been delivered to MCNC. It has been installed in the cleanroom facility and tested for vacuum integrity. Early results indicate that operating pressures in the 10^{-8} Torr range should be routinely accessible.
- A general device model has been developed at Duke University that will enable measured transfer characteristics of a field emitter array to be used to model its performance in a high-frequency circuit. A technique for inclusion of the emitter resistance in the device model is under development.
- The subprogram at The University of North Carolina - Charlotte is writing a paper on noise generation in field emitter arrays. A preliminary model for emission drift has been developed. If the drift model agrees with experimental results, it will affect the design of low interception extraction gate geometries.
- Litton Electron Devices Division has completed testing of the amplifier modules constructed with standard pyramid tip field emitter devices. Samples of column structures have been delivered, and the next generation of amplifier modules is under construction.

II. Milestone Status

Task	Completion Date	
	Original	Complete Expected
Complete first diodes of each of the three device types: Horizontal, vertical, and trench. Deliver samples to NRL, NCSU, and Litton. (MCNC)	11/91	11/91
Prepare first pass device models and potential circuit models based on initial device IV data. (Duke, MCNC, and UNC-CH)	3/92	11/92
Down select RF FEA designs based on device performance predictions	3/92	12/91
Complete first generation of field emission IV curves for each of the device types fabricated along with initial electron trajectory data and electron time of flight data. (NCSU and MCNC)	3/92	3/92 & Continuing
Design and order vacuum sealing and test system (MCNC)	11/91	12/91
Modify Litton trajectory modeling programs for field emission. Initial macroscale high vacuum tube encapsulation of field emission cathodes. (Litton)	3/92	11/91
Complete second set of field emission diode device runs with column FEAs (MCNC)	3/92	3/92
Complete third series of gated column emitters with modifications for very low electric fields over gate emitter isolations to reduce gate leakage	-	5/92
Complete new mask set for half micron field emission devices. (MCNC)	5/92	3/92
Install vacuum sealing and test system (MCNC) MCNC set-up a temporary vacuum test system in a SEM (3/92)	3/92	10/92
Complete initial electron trajectory modeling and initial testing of macroscale tubes containing microstructural gated FEC diodes. (Litton)	7/92	10/92
Complete fabrication of first microencapsulated FEC transistors. (MCNC)	9/92	1/93
Generate first pass transistor data from microencapsulated FE transistors. (MCNC, Duke, and Litton)	9/92	2/93
Demonstrate microstructural FEA diode/open triode devices meeting device IV and g_m/C program requirements.	9/92	12/92
Determine priorities of future device development. Determine the primary amplifier design methodology from the three amplifier design approaches. (MCNC)	9/92	12/92
Complete design for first integrated FEC based RF amplifier and FEC tube RF amplifier based on device characterizations. (MCNC, Duke, and Litton)	3/93	3/93
Complete second level models for FEC emission from surfaces treated in various manners. (UNC-CH)	3/93	3/93
Complete testing of FEC electron trajectories, electron trajectory model verification. (NCSU, Litton)	3/93	3/93
Determine packaging and cooling requirements for the prototype RF amplifier. (MCNC and Litton)	3/93	3/93

III. Technical Progress

1.0 Electrical testing and high-frequency performance measurements.

1.1 A copy of the Special Technical Report dated 17 November 1992 describing the experiment that showed modulation of a 0.36 GHz carrier signal is included as Attachment A.

1.2 An improved test fixture and method for demonstrating modulation of a 1 GHz carrier by a field emitter device in ultra-high vacuum at high frequencies is proposed. The overall plan is to test the devices under high vacuum on a fixture that will allow a substrate connection and three gate connections at once. A single anode will be integral to the test fixture, mounted directly above the device at the end of a microstrip line. This will provide controlled impedance (50 Ω) connections from the test equipment, through the vacuum chamber walls, and to within a few millimeters of the device. The measured RF performance then will be the performance of the device itself, unrestricted by the measurement equipment. A block diagram of the measurement setup is shown in Figure 1.

1.3 A new vacuum chamber is available for our constant use at NCSU in the laboratory of John Hren and Jiang Liu. For acceptable high-frequency performance, special feedthroughs must be purchased that are specified to the required constant impedance of 50 Ω. Such feedthroughs are available as a custom order item from Insulator Seal Incorporated. They provide dual SMA-type connectors on both atmosphere and high-vacuum sides on a 2.75" conflat flange. The connectors are rated to 700 V at a current of 1 A, and so will allow measurement of DC transfer characteristics as well as RF performance. The custom assemblies are less expensive than the equivalent number of feedthroughs from stock parts. The SMA connector is an industry standard for microwave packages and systems, and will be useful for future testing above 1 GHz.

In addition, the vacuum testing chamber at MCNC will be outfitted to perform initial DC device screening. Existing electrical feedthroughs and cabling can be used. An external heating jacket has been purchased to facilitate vacuum bakeout of the test chamber.

1.4 The proposed test fixture is shown in Figure 2. The fixture consists of a backplate, circuit board, die holder, anode, and associated hardware and connectors. The backplate is machined from aluminum, with clamps on each side to hold the connectors in place. The circuit board (1-oz copper on RT-Duroid dielectric) is also square, with 50 Ω microstrip lines from the center of each edge. A small square hole is cut in the center of the board for the die to protrude. The die holder is a small square of brass or copper. The anode is also a small square of brass or copper. The connectors are SMA flange mount, with the center connector terminating in a flat tongue that connects directly to the microstrip line on the circuit board. Several of these test fixtures have been constructed at Duke by Bill Joines and Joe Mancusi, and are currently in use for testing at NCSU.

The die is attached to the holder with lead-free (Sn-Ag) solder or a small dot of conductive epoxy. Then the die holder and printed circuit board are assembled to the aluminum backplate and fixed with screws. The stiffness of the printed circuit board holds the die in place and ensures good electrical contact. Then wirebond connections are made from the gate contacts of three selected devices to three of the microstrip lines. The anode is soldered to the fourth microstrip line and bent into place over the die. Lastly, the SMA connectors are clamped in place, and the center conductors are soldered to the microstrip lines.

Cables from the test fixture to the electrical feedthroughs are constructed from SMA connectors and RG-188/U 50 Ω coaxial cable. The cable has TFE dielectric and outer insulation for vacuum compatibility. The use of TFE in a vacuum chamber does, however, limit the chamber bakeout temperature to < 200 °C, with temperatures around 100 °C preferred. The RT-Duroid dielectric used in the test fixture printed circuit board has acceptable vacuum characteristics at temperatures up to 125 °C.

Outside the chamber, bias tee networks are attached to isolate the RF measurement equipment from the DC supplies used for gate and anode bias. The performance of the bias tees at 1 GHz is excellent as measured on a vector network analyzer. The bias networks are connected to the test equipment through coaxial cables with Type N connectors. *S*-parameters will be measured with a network analyzer and recorded. Modulation will be demonstrated with a function generator and oscilloscope. Photographs will be taken of the oscilloscope trace as an experimental record. The bias tees, external cables, and RF test equipment is provided by Dr. Joines from Duke.

1.5 The measurement cycle for each device will be about three days. A device is mounted on a test fixture and installed in the chamber. The chamber is pumped down and allowed to bake out for one to two days until the required vacuum level is reached. The devices are then tested for acceptable DC characteristics, and if a good device is located, it is tested for RF characteristics. While the chamber is pumping down, another device can be mounted. When testing is complete, the chamber is vented, the tested device is removed, and the test cycle begins again.

At best, measurements can be made three times per week-on Monday, Wednesday, and Friday. This hinges on the performance of the vacuum system and the availability of testable parts and substrates. At worst, we should still be able to test at least once per week. Personnel are available from MCNC and its subcontractors to continue testing through the holidays.

2.0 Device processing.

2.1 Devices with design targets including gate apertures of 0.6 and 1 μm and emitter column heights of > 5 μm will be completed and tested in the next quarter. These design targets are possible because of improvements in device processing techniques gathered through experience with large numbers of prototype devices at MCNC

2.2 Improvement in the method of oxide deposition in the gate-emitter isolation structure of the columnar emitters has produced up to 12 μm of oxide between columns, resulting in finished emitter column heights of up to 8.6 μm. Initial experiments with 5 μm columns successfully used low-temperature LPCVD oxide. On taller structures (6.5 - 7 μm), LTO deposits on the top and sides of the columns as well as on the wafer surface, eventually producing gaps or "keyholes" in the oxide layer. Figure 3 is an SEM photo showing an example. Repeated applications of evaporated oxide with some interim processing were used to fill the same structures with no keyholing, as shown in Figure 4. Once a contiguous oxide layer is formed, the surface must be planarized to ensure consistent emitter tip-to-gate electrode spacing. Chemical-mechanical polishing is the technique currently used, which leaves a smooth surface but has poor precision in the control of polishing depth. In-house mechanical polishing demonstrates high accuracy at the expense of extremely slow polishing rates.

2.3 Our method of tip fabrication requires that a nitride cap be present on the silicon emitter column before sharpening. Two methods of nitride cap formation have been developed so that a wide range of polishing precision can be accommodated. Precise polishing leaves the nitride cap formed during initial fabrication. Overpolishing removes the cap formed initially, leaving a bare silicon column surrounded by oxide. An example of an overpolished wafer is shown in Figure 5.

In one technique for restoring the nitride cap, the silicon column is etched back. A layer of nitride is deposited. The nitride on the surface of the wafer is etched away, leaving a small amount in the hole formed by the silicon etchback. This self-aligning method is simple and effective, but sacrifices column height and often leaves a hole or a very thin spot in the center of the new cap. In the second technique, a layer of nitride is formed over the polished wafer, coated with photoresist, and patterned. The exposed nitride is etched away, leaving a cap over the column. This method produces a thick cap, but the mask used to pattern the photoresist must be aligned to a buried layer. The resulting caps may not be centered on every column, but still can be used for sharpening. A cap produced by this method is shown in Figure 6.

2.4 Construction of columnar emitters with smaller and smaller gate dimensions requires extremely accurate photolithography as the feature size approaches the wavelength of the light used to pattern the wafer. There are two main challenges that we have confronted here at MCNC in the photolithography that is needed for field emitter devices: patterning very small dots that are uniform in size, and patterning the uneven topographies found in thin-film microencapsulated devices.

Wafers must be patterned so that the photoresist dots that form the mask for the etching of field emitter tips are uniform in size within the die, from die-to-die across the wafer, and from wafer-to-wafer across the lot. These are dots that are very small, from 0.5 μm to just under 2.0 μm. Field emitter arrays can consist of thousands of these dots spread over relatively large areas across the wafer.

In typical CMOS lithography, critical dimensions are usually associated with line widths but not with the diameter of circular dots. The patterning of contact holes, analogous to field emitter tip patterning, is usually not considered a critical dimensioning problem. But in patterning small dots that are approaching in size the wavelength of the light used to expose them, new issues emerge in controlling this process. One way of looking at the problem is to realize that the typical lens aberrations are now hitting you from all sides, rather than affecting only one dimension.

Our experience at MCNC in developing large numbers of prototype devices has also enabled us to learn how to deal with these new and challenging lithography issues. Still, some questions need to be answered.

1. How does one discover "best focus" in shooting a lot? We have had to develop better techniques to define best focus. These include reticles to determine focus from a "naked eye" examination, from techniques with our Hitachi S6000 SEM to examine the patterns themselves. Often best focus is a compromise among several different regions in the die. How does one make that compromise and on what basis?
2. What are the acceptable limits of nonuniformity? What causes nonuniformity within a wafer, and within a lot? We have taken extensive measurements and performed statistical analyses to determine whether variance is a function of intra die, inter die, intra wafer, wafer-to-wafer, etc.
3. What are the differences between using a light field reticle as opposed to a dark field reticle-that is, between a dark field reticle (in which either negative resist or an image reversal process isused) or a light field reticle, which uses a positive resist process? Our experience has led us to believe that there is an inherent advantage to dark field reticles.
4. How does exposure help or hinder uniformity?

The second major issue occurs in our thin film encapsulation prototypes. This involves the patterning of holes over highly contoured topography, which offers a major challenge to the focus control systems of our steppers. In these lots, uniformity in diameter is not as much an issue as is alignment with previous levels. This is a major challenge, because the alignment targets are often buried under films several microns thick.

We are developing valuable experience in the fabrication of field emitter devices. Some of our techniques involve simply doing the normal CMOS lithography, only better, whereas other techniques have required unique approaches to problems. One way we have measured our progress is that we are moving from the stage of "being stopped" by a problem to where we now at least know what we have to do. The successful method may be difficult, expensive, and time consuming, but nevertheless is a path leading to a solution.

3.0 Vacuum testing and microencapsulation bonding system.

3.1 The bonder/tester double-chamber vacuum system designed and built for the DARPA field emitter project was delivered to MCNC on 21 October 1992 after a period of engineering consultation lasting approximately six months. The system was designed in collaboration with LitCo Industries of Raleigh, NC, but was constructed by Shrader Scientific, Inc., of Hayward, CA. In the two months since the system's arrival, it has been installed inside MCNC's cleanroom facility and tested for vacuum integrity. Recent results indicate that operating pressures in the 10^{-8} Torr regime may be routinely accessible for device testing purposes.

4.0 Device modeling.

4.1 Much of the work of the researchers at Duke University has focused on device modeling. In particular, a general model is being developed that will enable measured transfer characteristics of a field emitter array to be used to model its performance in a circuit. Values for the small-signal device parameters can be estimated from DC transfer characteristics and used to develop a comprehensive model of the array in a particular type of circuit, such as an amplifier circuit. This analysis has already led to an increased awareness of the matching circuits needed for a matched field emitter array amplifier. Included are two reports on this research. One is a general field emitter model that develops an equivalent circuit from basic theory. Although the current field emission theory does not appear to be directly applicable to field emitter tips, the work provides a background for developing a model from measured characteristics. A report on this model is included as Attachment B. A second report covers the technique developed for inclusion of the emitter resistance in the device model, and is given as Attachment C.

4.2 A report by the subprogram at UNC-C on noise modeling in field emitter arrays is included as Attachment D.

5.0 Device testing.

5.1 Results of the amplifier module test by the subprogram at Litton Electron Devices Division is given as Attachment E.

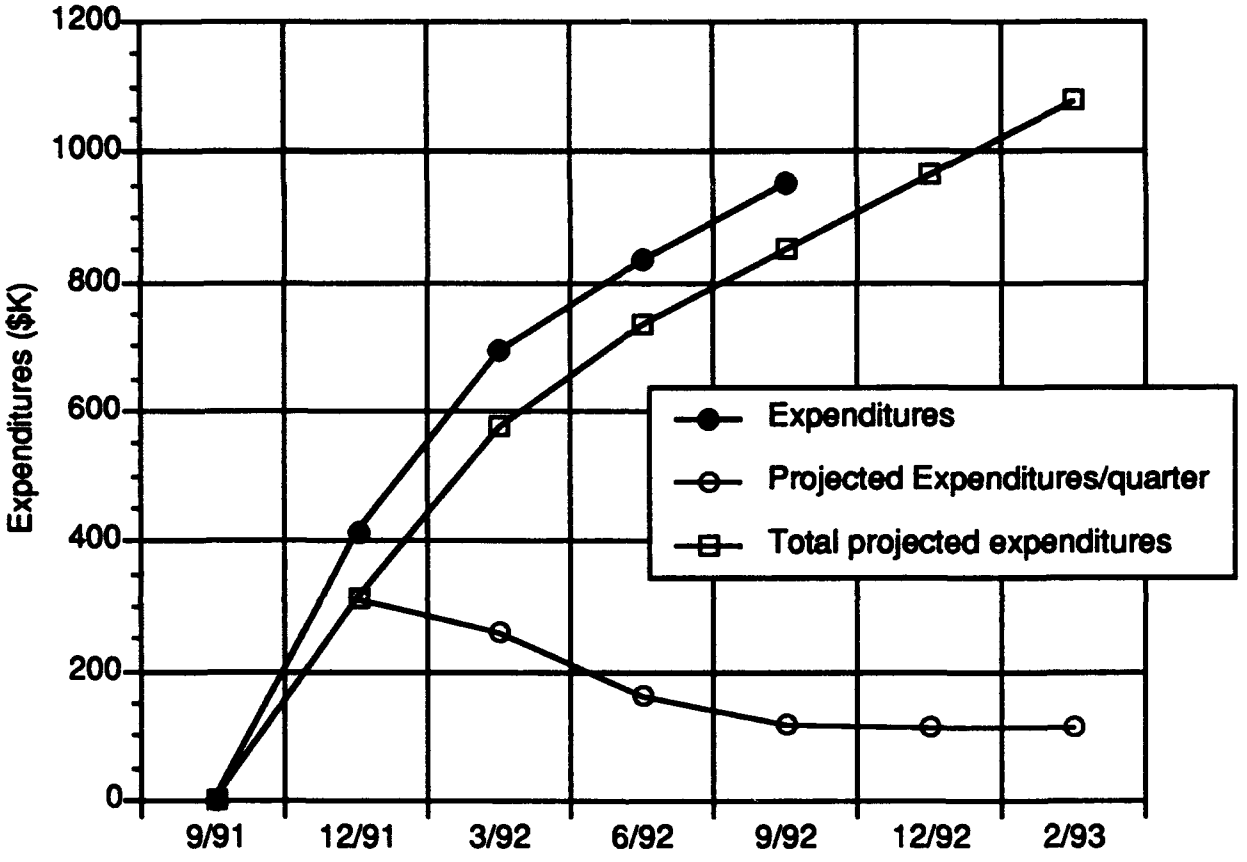
6.0 Other Developments.

6.1 In early summer of 1992, some work was conducted to fabricate field emitter tips out of TiW rather than silicon. Experiments were performed to determine which etching solutions proved most effective, and to see just how controllable these processes could be. The thick layers of TiW metal required to fashion these tips presented some problems of their own; the stresses they introduced into their silicon wafer substrates often warped them beyond the point of photolithographic processing.

Considerable effort was devoted toward reducing the stress in these wafers. The most effective means of stress reduction was simply to reduce the amount of TiW on the wafers by etching part of it away. Successive deposition of TiW layers with individual annealing steps was also discussed. A TiW sputtering target from Angstrom Sciences in Pittsburgh, PA, was ordered in late summer, and arrived 05 November 1992; this will enable MCNC to deposit its own TiW metal in the future rather than having it done by external contractors. Installation of this target is pending so that experiments can be conducted for the development of stress-free TiW films.

6.2 A design for macroencapsulation of field emitter devices in evacuated glass tubes was completed. An exploded view of the assembly is shown in Figure 7. Components for this assembly are being fabricated now. Assembly and testing of these devices will be completed in the next quarter.

IV. Fiscal Status



Expenditures this quarter (7/01/92 - 9/30/92)	$115,274.81
Total expenditures to date (9/09/91 - 9/30/92)	951,260.18
Projected expenditures:	
10/92 - 12/92	113,602.91
1/93 - 3/93	113,602.91
Contract Amount (Basic)	$1,178,466.00

V. Problem Areas

The greatest problem currently faced by this phase of the program is minimization of the time and effort involved in device testing, so that an aggressive testing schedule can be maintained. Testing an individual device may take up to five days when device selection, mounting, wire bonding, vacuum system pumpdown and bakeout, and DC and RF characterization are all considered. If this process is carried out on a device with less than optimal geometry, a great deal of time is lost, indicating the need for some method of prescreening for good devices.

Simple optical microscope screening is sufficient to screen out devices with obvious processing defects, but tip radius cannot be measured. SEM microscopy has the required resolution for tip inspection but can contaminate the tip through field-enhanced adsorption of residual vacuum pump oil and other compounds. The best approach seems to be selection of a group of devices with optical microscopy, inspection of a single device in that group with SEM, and pretest cleaning of the devices in the vacuum chamber.

VI. Visits and Technical Presentations

Numerous closed meetings were held between MCNC's staff and subcontractors. Chris Ball of MCNC travelled to the SRC Topical Research Conference on Chem-Mechanical Polishing for Planarization (14 & 15 September 1992, Troy, NY). A copy of his report is included as Attachment F.

Two presentations on this project have been made outside the program during the contract time period. Researchers from the program at MCNC and the subprograms at Duke University and Litton Electron Devices Division attended the DARPA Vacuum Microelectronics Initiative Review on 14 & 15 October 1992. Dr. Jiang Liu from the subprogram at NCSU presented a paper at the International Electron Devices Meeting (14-18 December 1992, San Francisco, CA) entitled "Field Emission Imaging Study of Silicon Field Emitters." A copy of this paper as it appears in the conference proceedings is given as Attachment G.

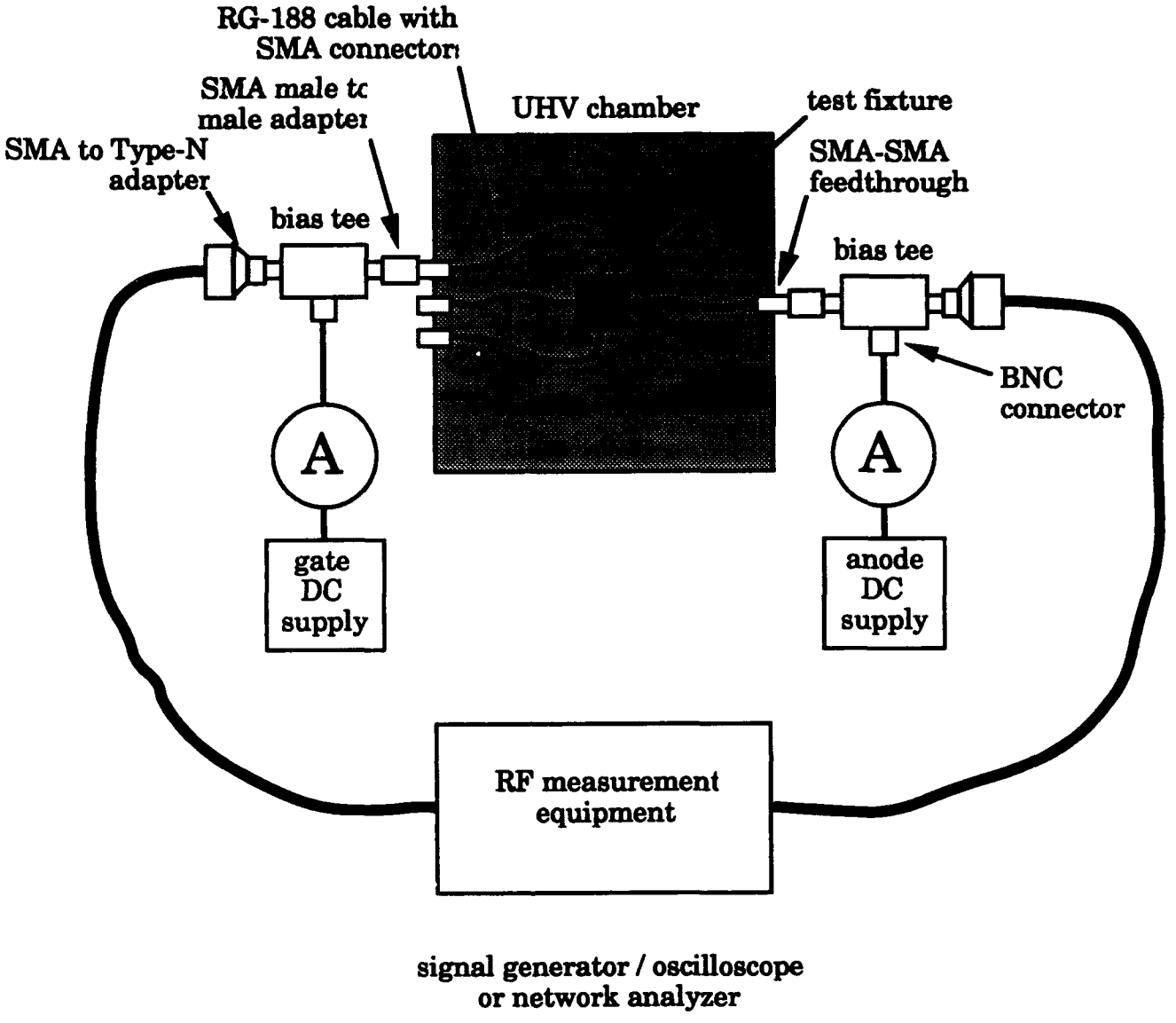
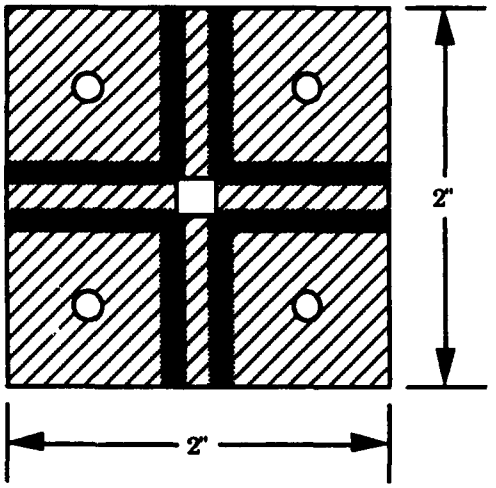
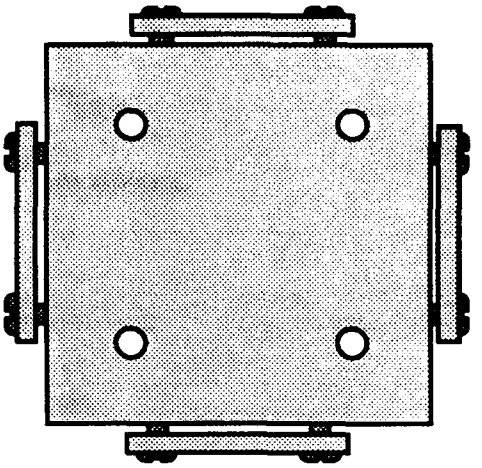


Figure 1: Block diagram of the MCNC/NCSU/Duke measurement setup.

Figure 2: Improved high-frequency test fixture. (overleaf)



printed circuit board
1 oz. copper on
1/16" rt-duroid dielectric

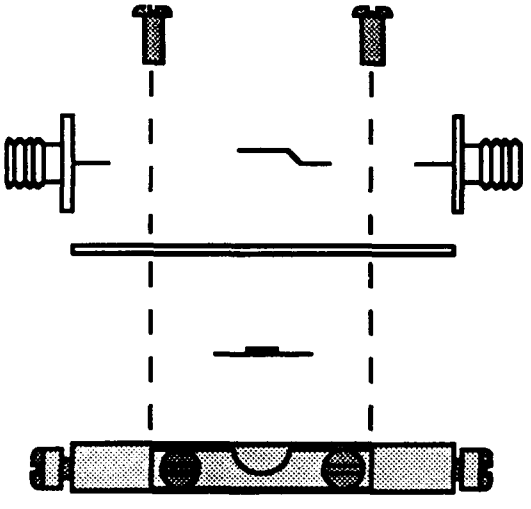


aluminum backing plate with
PCB mounting holes and
clamps for SMA connectors

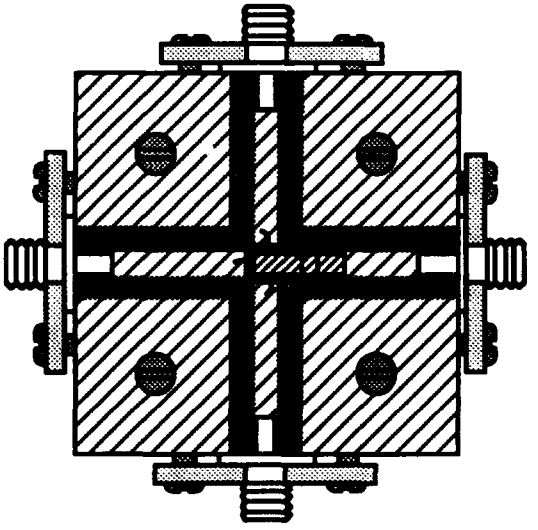
chip on brass
mounting plate

SMA connector

brass anode



test fixture assembly
side view



assembled test fixture
top view

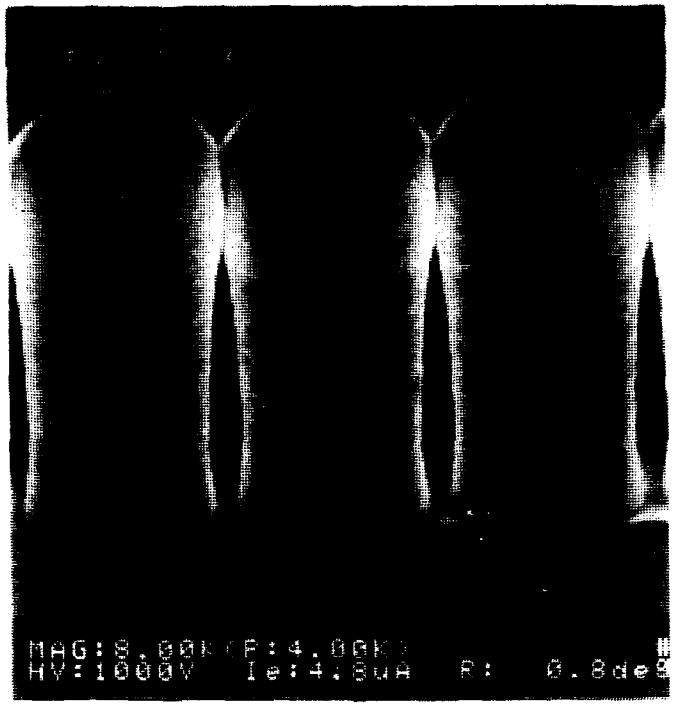


Figure 3: SEM photo of a tall column structure with keyholing in the oxide layer.

Figure 4: Same structure with the keyholing problem solved.

Figure 5: Surface of wafer after overpolishing.

Figure 6: Nitride cap formed postpolishing with photolithographic method.

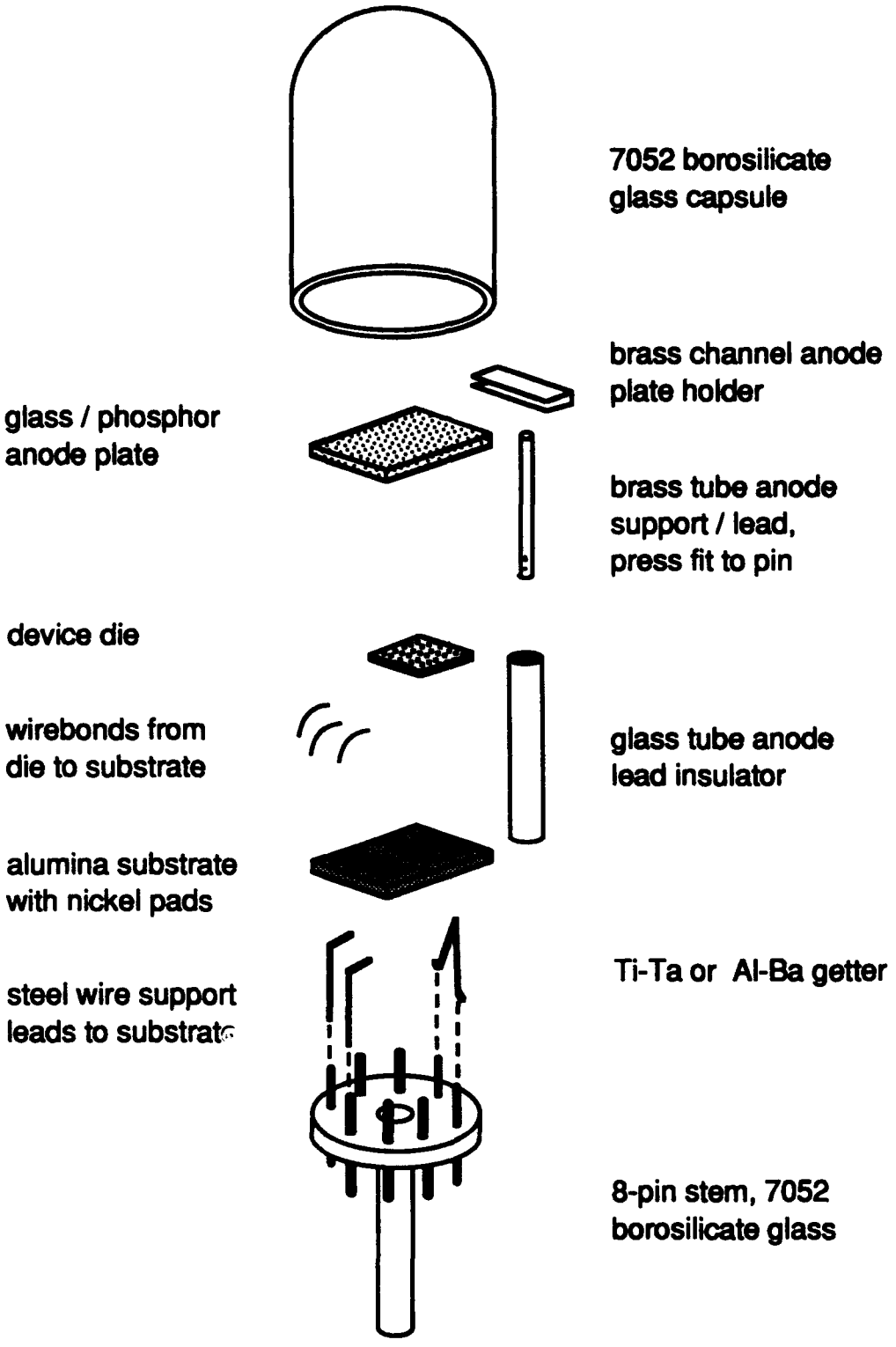


Figure 7: Exploded view of macroencapsulated field emitter array assembly.

Field Emitter Array RF Amplifier Development Project
Phase one, Cathode Technology Development
DARPA Contract #MDA 972-91-C-0028

Objective : RF modulation of gated column silicon field emitter with diamond coated

I. Introduction

The initial RF modulation testing of the gated column silicon field emitter with a diamond coated has been done. The set-up of the testing is as shown in Fig. 1. It should be noted that we didn't use 50 ohm coaxial cable inside the vacuum chamber for this testing since the configuration was initially used for DC testing, and we wanted to get earlier AC results at this time. It is well known the mismatch of the circuit will give a lot of loss during the RF measuring. This report completes modulation at 0.36 GHz, and even higher performance is expected after full blown AC testing.

II Testing results

DC testing:

Fig. 2a shows the DC characteristics of this device (5x5 array) on a linear scale while Fig. 2b shows the Fowler-Nordheim plot of the measured data. Fig. 3a and 3b show the SEM pictures of this devices for single and array field emitters respectively.

RF modulation:

Fig. 4a shows the carrier signal at 0.36 GHz. Fig. 4b shows the RF modulation of device biased at V_g=70V, V_a = 250V, I_a < 1 nA Fig. 4c shows the RF modulation of device biased at V_g=112V, V_a = 250V, I_a = 2.0 μA

III. Discussions

The DC characteristic, as shown in Fig. 2, of this device is comparable to what we reported from the standard silicon field emitter (2 μm opening at gate and 1 μm height, tip radius is about 100 Å). From Fig. 3, the gate opening is about 2.26 μm, the tip is 1 μm below the bottom of gate electrode, and the tip radius is more than 600 Å). The diamond-like film was coated on the silicon tips by remote plasma diamond-like film deposition techniques with a short sputtering etching before deposition and to a thickness of approximate 100 Å. The effect of diamond coating on the emission characteristic of the silicon field emitter is pronounced since much larger radius of the tip of this device than that of the standard device was observed from the devices shown in Fig. 3, while

this diamond coated device still has comparable electron emission characteristics.

From the results of Fig. 4, it is noted that even without a matching circuit inside the vacuum chamber, we still can get the RF modulation up to 0.36 GHz. No testing was done at frequency above 0.36 GHz. Compare the amplitute of the signal of Figs. 4b (device is barely turned on) and 4c (device is emitting about 2 μA electrons), it is found that this device responds with positive voltage gain at least up to 0.36 GHz without a matching circuit inside the vacuum chamber.

In order to eliminate any mismatch in the measurement, the configuration of RF testing (Fig. 5) has been proposed. The connections will be 50 ohm coaxial cables and be as close as possible to the device. The high voltage chip capacitor will be used at the input and the output to isolate the RF and DC signal. The input signal will be connected to the oscilloscope as a reference for comparison. The network analyzer will be used to measure S-parameters. The required parts have been ordered and we plan to do RF testing in a couple of weeks. The device is packaged on the ceramic DIP package now, but the microwave package will be used eventually.

IV. Conclusions

The devices were fabricated at MCNC, even without a matching circuit inside the vacuum chamber, performs the RF modulation up to 0.36 GHz, and even higher performance is expected after full AC testing with RF testing set-up.

Figure Captions

Fig. 1 Initial testing set-up for DC & RF testing.

Fig. 2a DC characteristics of this device (5x5 array) on a linear scale.

Fig. 2b The Fowler-Nordheim plot of the measured data.

Fig. 3 SEM pictures of this devices for single and array field emitters respectively.

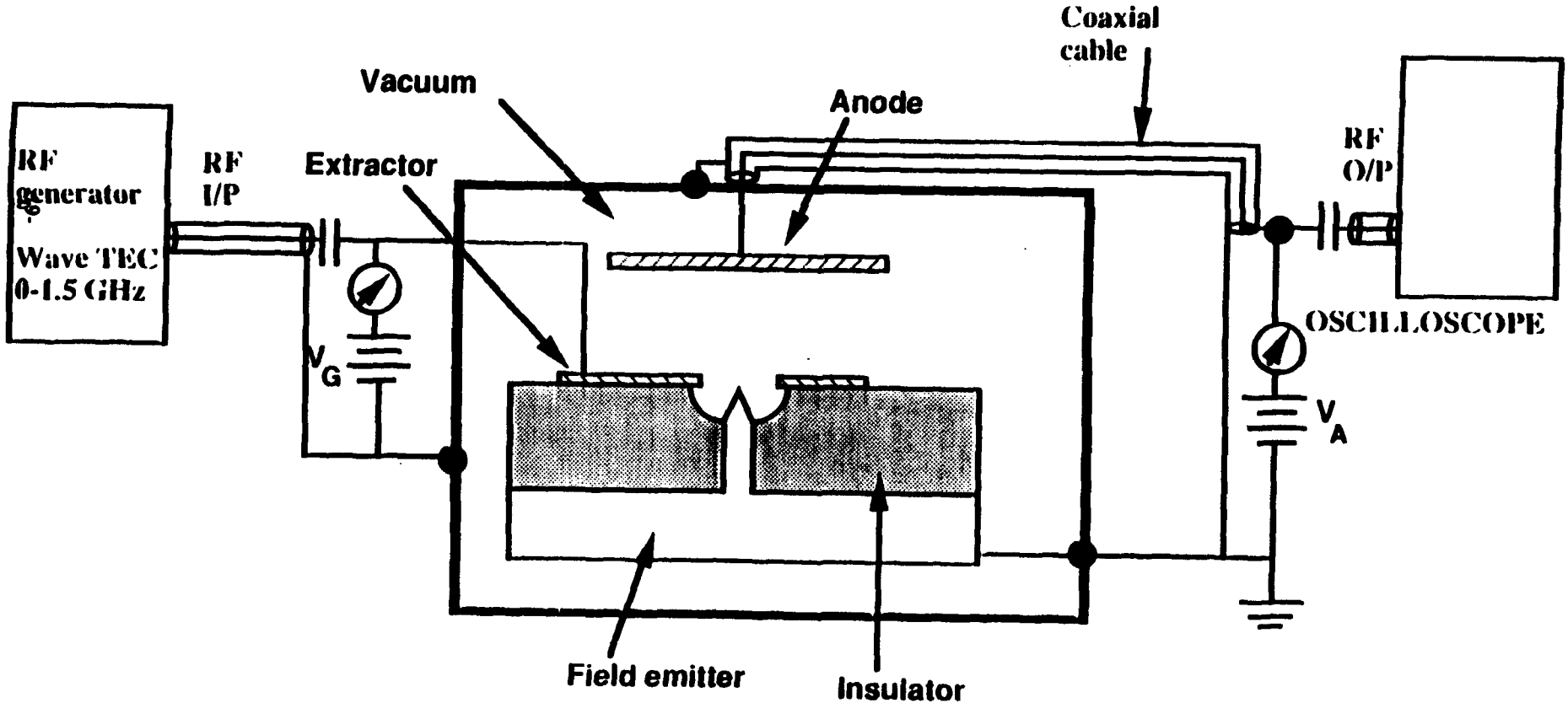
Fig. 4a The carrier signal at 0.36 GHz.

Fig. 4b The RF modulation of device biased at V_g=70V, V_a = 250V, I_a < 1 nA

Fig. 4c The RF modulation of device biased at V_g=112V, V_a = 250V, I_a = 2.0 μA

Fig. 5 Proposed RF testing set-up.

FIG. 1
Initial Configuration of RF Testing



ATTACHMENT A

Fig. 2a

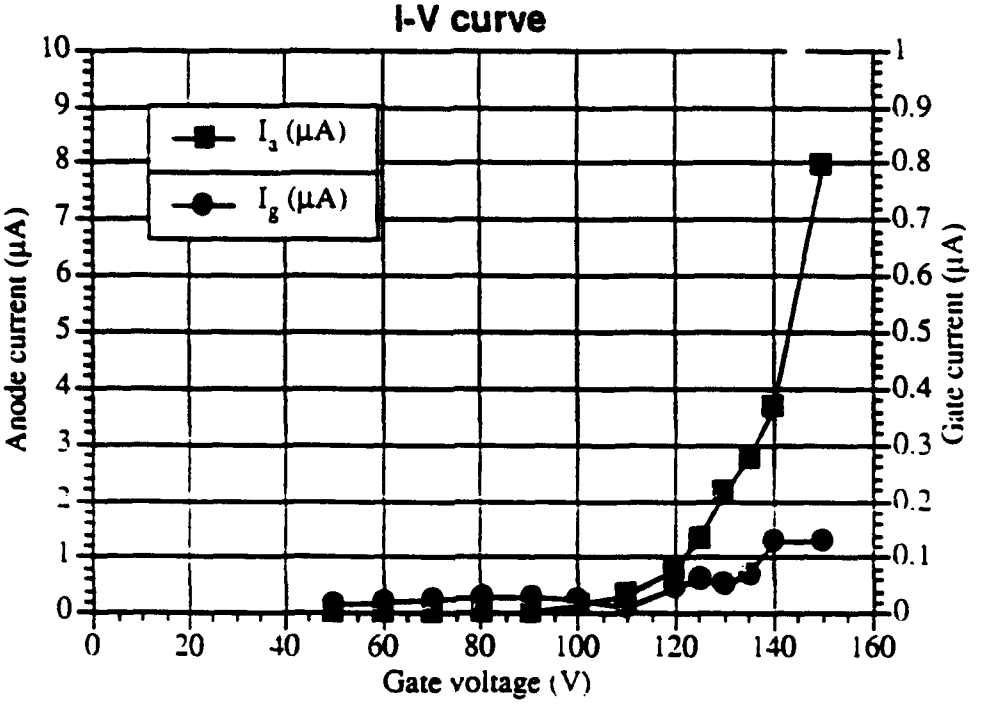

I-V curve
I_a (μA)
I_g (μA)
Anode current (μA)
Gate current (μA)
Gate voltage (V)
0
20
40
60
80
100
120
140
160
0
1
2
3
4
5
6
7
8
9
10
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

Fig. 2b

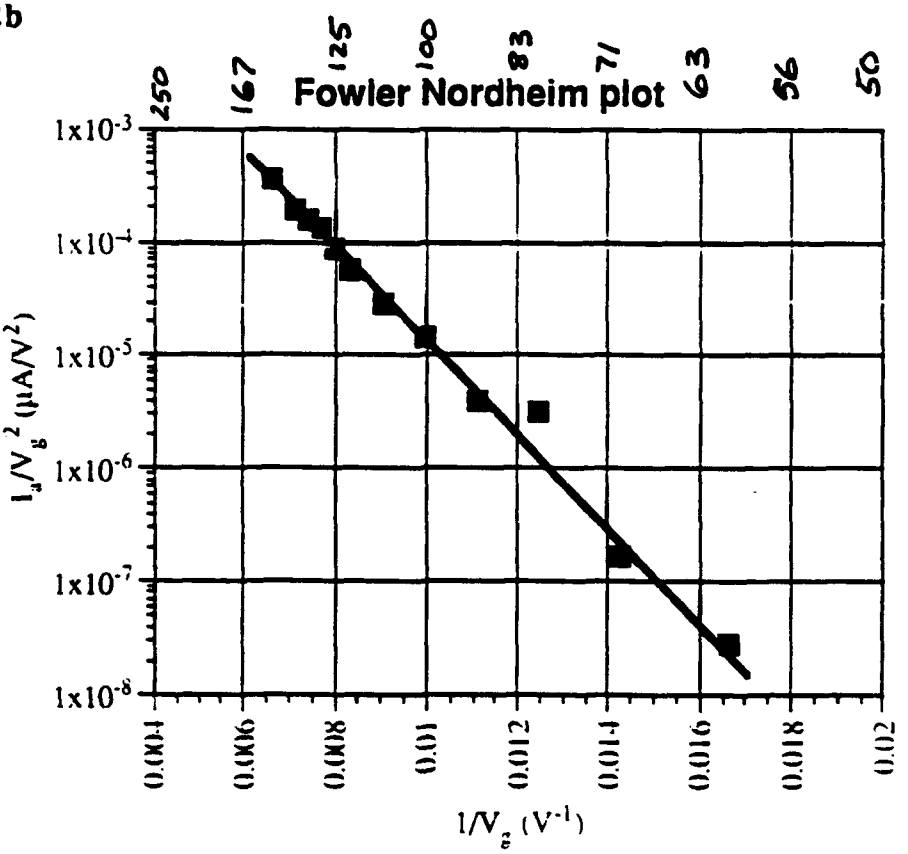

Fowler Nordheim plot
250
167
125
100
83
71
63
56
50
I_a/V_g^2 (μA/V²)
$1/V_g$ (V⁻¹)
1x10⁻³
1x10⁻⁴
1x10⁻⁵
1x10⁻⁶
1x10⁻⁷
1x10⁻⁸
0.004
0.006
0.008
0.01
0.012
0.014
0.016
0.018
0.02

Fig. 3a.

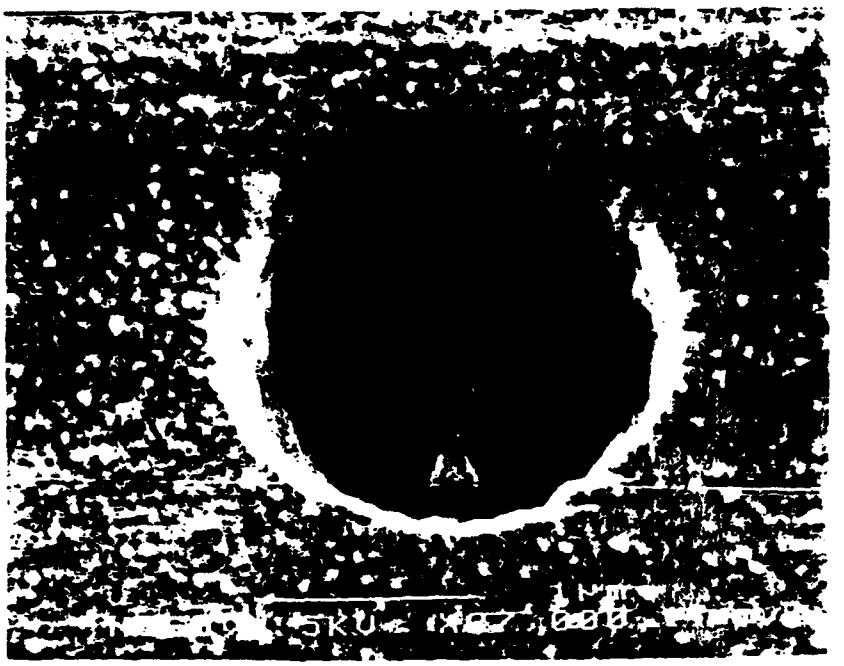


Fig. 3b.

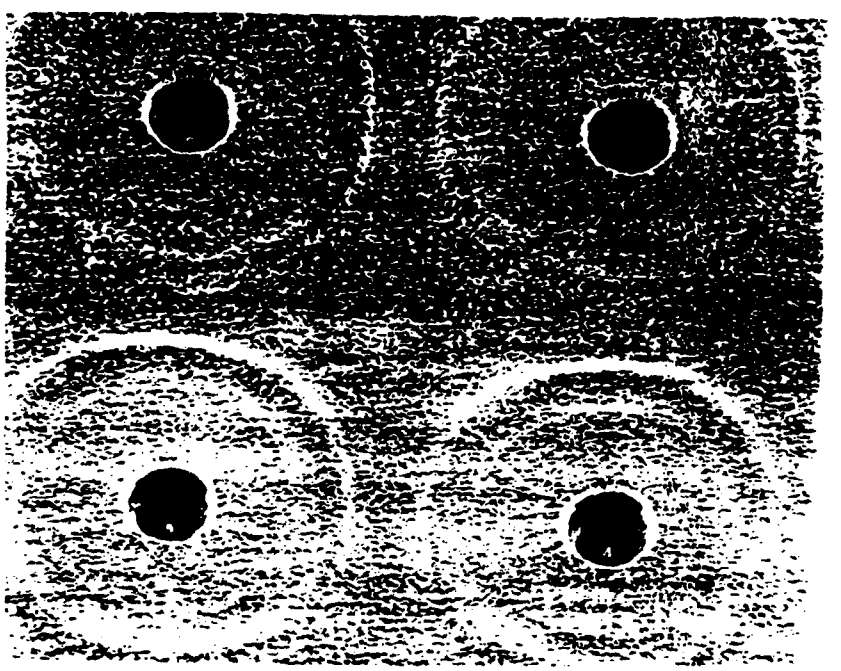


Fig. 4a.

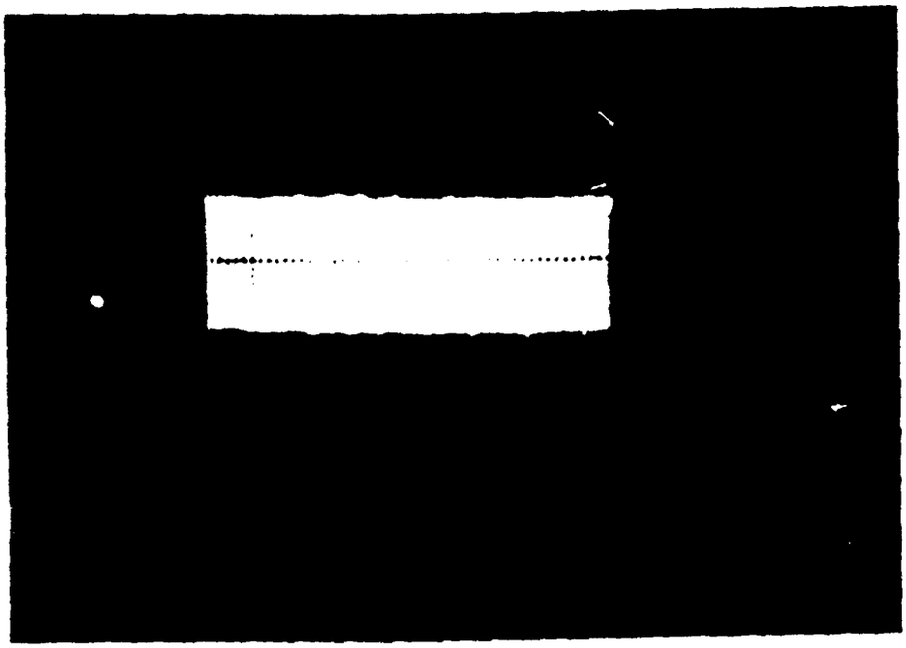


Fig. 4b.

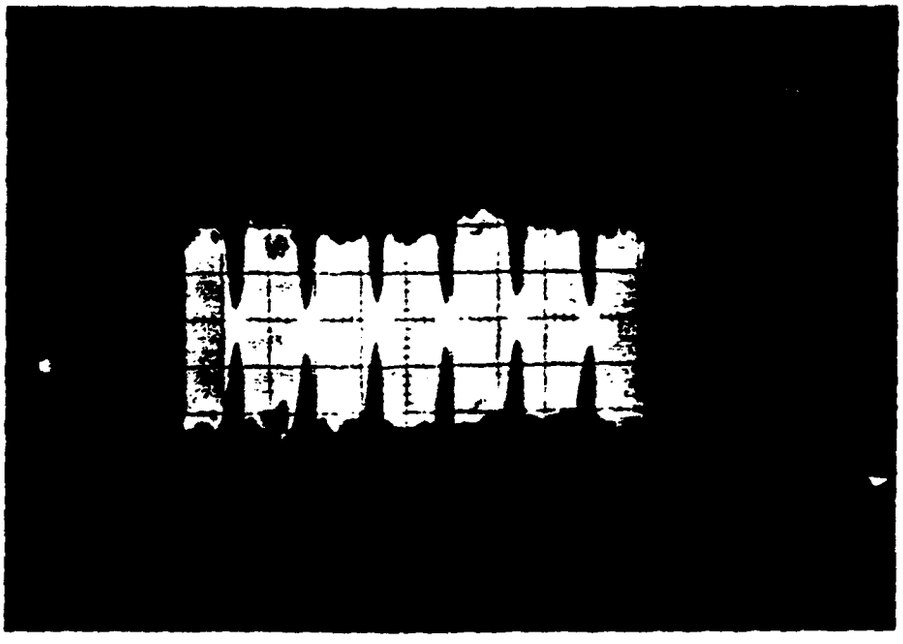


Fig. 4c.

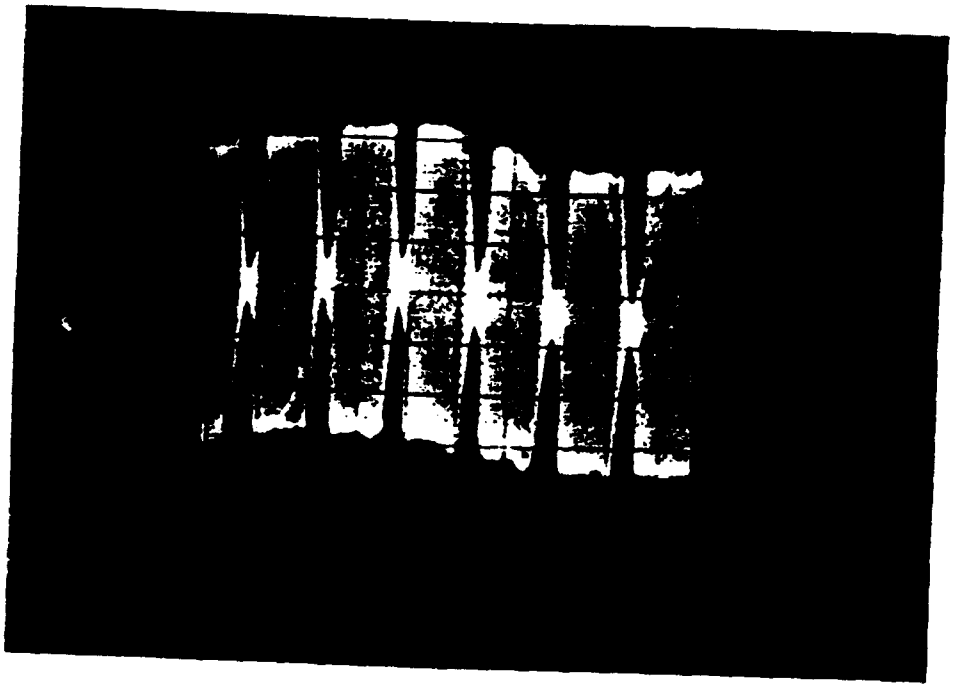
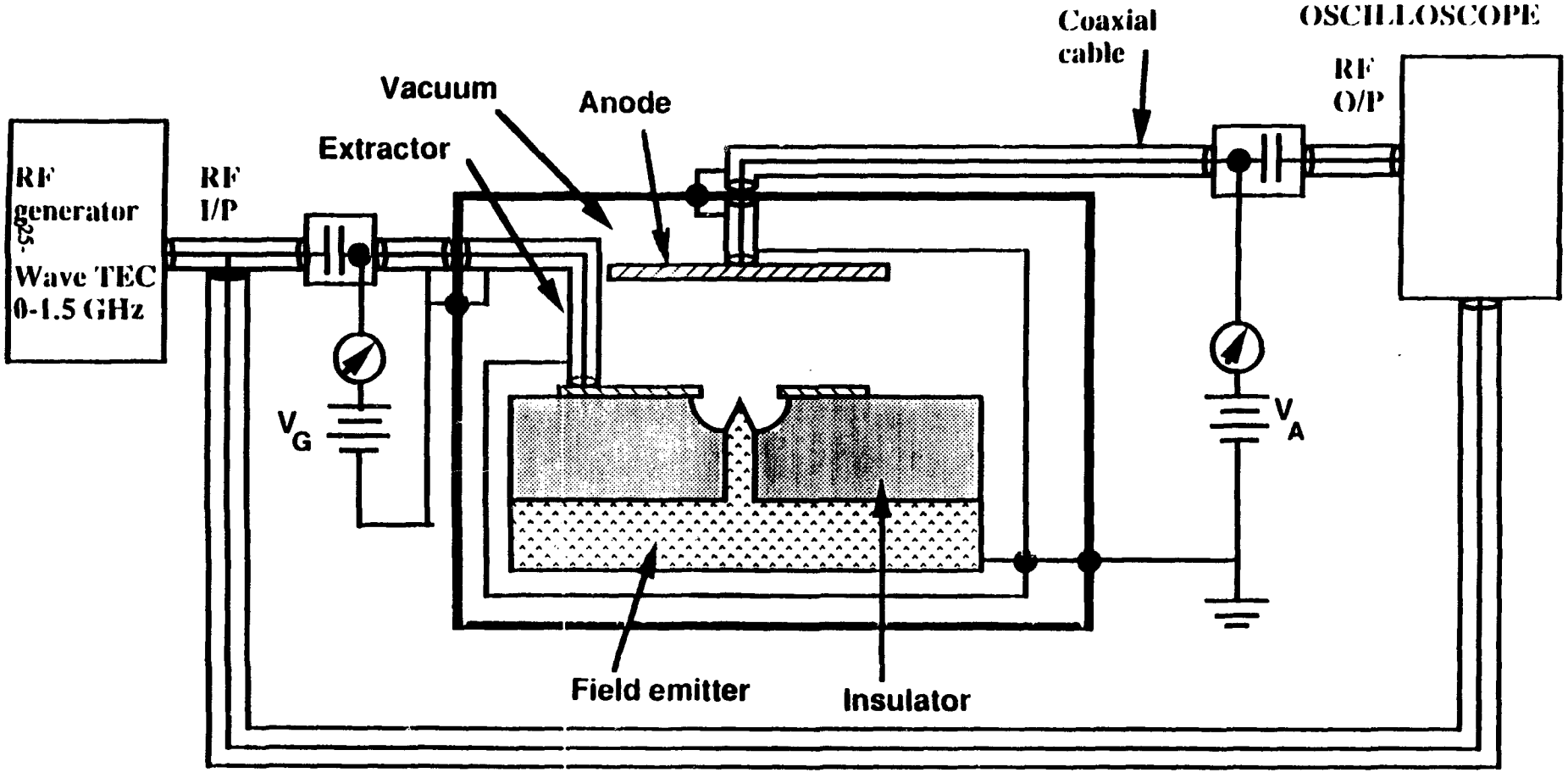


FIG. 5
Proposed Configuration of RF Testing



ATTACHMENT A

Field Emitter Amplifier Modeling

Joseph E. Mancusi and William T. Joines
Duke University, 9/18/92

1 Introduction

In this paper, the development of a field emitter model is described. It is our hope that this model will accomplish a number of goals including a better understanding of the limits on field emitter array performance, a measure of the reliability of standard modeling tools, an estimate of the actual device performance, a standard with which to compare actual device performance, an indication of areas in which device performance can be improved, and an analysis and comparison of possible device structures prior to fabrication.

The model begins with an electromagnetic analysis of the field emitter geometry to calculate the electric field on the tip of the emitter. At this time, the capacitance of the field emitter structure is calculated. The tip electric field versus gate and anode voltages are used with the Fowler-Nordheim equation to calculate standard DC current versus voltage curves. These are the same curves that would be measured for actual field emitter devices and for vacuum tubes and are analogous to the standard BJT curves of collector current versus gate and collector voltages. From these curves, a load line is drawn and an operating point chosen. The operating point and load line determine the bias circuit for the device when used as an amplifier, for example. In addition, the small-signal voltage gain and the operating range of the device about the operating point are chosen from the curves. The voltage gain and bias circuit also determine the small-signal transconductance of the device. A small-signal device model is developed from the parameters of the device, the capacitance, and estimates of other parameters such as series resistance and coupling capacitances. The s-parameters of such a device are characterized and the overall performance of the device is evaluated. For instance, the upper gain frequency can be obtained from the model when the device is operated as a matched amplifier. The s-parameters are important as they are often used with a program such as PUFF to model the amplifier's performance in a microwave circuit.

2 Electromagnetic modeling

The field emitter amplifier modeling begins with the geometry and materials of the actual field emitter device itself. It is important to accurately determine the capacitances and

electric fields of the device. Consider that one estimate of the upper frequency for voltage gain of a simple small-signal amplifier model is

$$f_T = \frac{g_m}{2\pi C} \tag{1}$$

where g_m is the device transconductance, $g_m = \partial I/\partial V$, and C is its capacitance. Obviously, this equation indicates the importance of a high transconductance and low capacitance for obtaining high frequency amplification. This definition, however, is misleading. It is usually possible to achieve *power* gain at frequencies much higher than indicated by the above equation by conjugately matching the amplifier's impedance at the input and output. Transconductance and capacitance are very important parameters, however, and critically effect device performance.

The electric fields evaluated using the Maxwell finite element electromagnetics software by Ansoft Corporation. Using the meshmaker program, the geometry for the field emitter is entered. Then the axially symmetric electrostatics program is used to calculate the electric fields, especially in the area of the tip where the electric field is the highest. At this time, the capacitance of the structure is also evaluated. This is done by assigning voltages to the objects of interest and computing the energy stored in the fields.

$$U = \frac{1}{2}\int_{vol}(E \cdot D)dv \tag{2}$$

The capacitance is then given by

$$C = \frac{2U}{\Delta V^2} \tag{3}$$

where ΔV is the potential difference between the two objects of interest. If the potential difference, ΔV, is one volt the expression for capacitance reduces to

$$C = \frac{2U}{\Delta V^2} = \int_{vol}(E \cdot D)dv \tag{4}$$

The capacitances of interest for the equivalent circuit model include the capacitance between the gate and the emitter (C_{ge}), the capacitance between the collector (or anode) and the emitter (C_{ce}), and the capacitance between the collector (anode) and gate (C_{gc}). Each of these capacitances is calculated by setting one of the conductors of interest to zero volts, setting the other conductor of interest to one volt, and putting no boundary condition on the other conductor, in effect letting its voltage float to assume its natural value under these circumstances.

3 DC transfer characteristics

The DC characteristics of the field emitter device are important when designing an amplifier using the field emitter as the active device. Figure 1 shows a possible bias

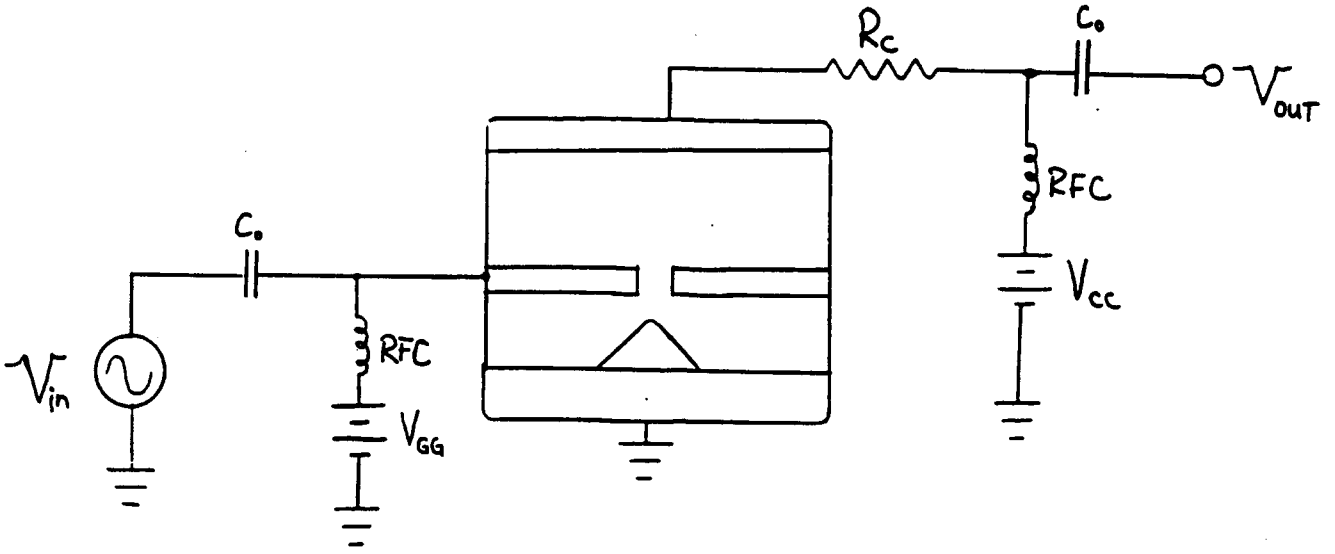


Figure 1: Field emitter in an amplifier circuit.

arrangement for the field emitter amplifier. The bias voltages, V_{GG} and V_{CC} as well as the bias resistor are determined from the DC transfer characteristics. The procedure for doing this is outlined in a previous report.

Once the electric field at the tip of the field emitter is known, the current density is calculated using the Fowler-Nordheim equation.

$$J = 1.40 \times 10^{-6} \frac{E^2}{\phi} \exp\left[-6.83 \times 10^{7} \frac{\nu \phi^{3/2}}{E}\right] \tag{5}$$

where

$$\nu = 0.95 - 1.217 \times 10^{-7} \frac{E}{\phi^2} \tag{6}$$

In the Fowler-Nordhiem equation, ϕ is the workfunction of the emitter tip material in electron volts (eV) and E is the electric field magnitude in volts per meter (V/m). The Fowler-Nordhiem equation is derived from a quantum mechanical expression that calculates the current density from a planar semiconductor or metal as a function of the electric field. The constants in the above equation result from evaluating the integral quantum mechanical expression for a particular material, in this case silicon. Although it is currently the standard tool for analyzing field emission from surfaces, it is unknown how well the Fowler-Nordhiem equation models the situation of a microvacuum device such as a field emitter. Calculated results have thus far shown poor agreement with experiment. It is not currently known whether these discrepancies result from the inapplicability of

the Fowler-Nordheim equation as it is expressed above to problems on the order of the small dimensions of a field emitter tip,or from the lack of an ideal tip surface (the tip is often contaminated). For these reasons, it is often preferable to use experimentally measured device characteristics if they are available.

Because the electric field is directly related to the applied voltage in dielectrics, the current density as a function of voltage is easily obtained from the Fowler-Nordhiem equation. In order to calculate the total current from an emitter tip, the current density must be multiplied by the area of the tip which emits electrons. The most obvious choice for the emitting area is a constant on the order of the area of a half-sphere with a radius similar to that of the radius of curvature of the tip. Unfortunately, the electric field is not constant over the whole tip area, which means that integration of the Fowler-Nordhiem equation over the tip should be performed to get an accurate theoretical value for the tip current. We have developed a tip integration scheme for calculating the current in successive spherical shells of the emitter tip over which the electric field is approximated by a constant. The field values are calculated using the axially symmetric electrostatics module of Maxwell Electromagnetics Solvers. This method shows that the current comes from a large part of the spherical tip and that the emitting area is about $2r^2$ as expected (r is the tip radius). Since the integration scheme is very time consuming, the usual method for calculating the tip current is to use the maximum electric field value in the Fowler-Nordhiem equation and multiply the resulting current density by an effective emitting area of about $2r^2$, a figure determined from the tip integration method.

The data for the current versus voltage curves are obtained from a FORTRAN program (on the AT) using the assumptions mentioned above, or are measured from an actual device. The appropriate curves are anode current versus anode voltage for different values of gate voltage as shown in Figure 2. These curves are used to obtain the operating characteristics of the device. The operating point, referred to as the Q-point, is the bias point of the device. Its specification includes the values of the gate-to-emitter voltage, the anode-to-emitter voltage, and the anode current when no RF signal is applied. In addition to the Q-point, the load line is also obtained from the operating curves of the device, shown in Figure 2. The load line indicates the range over which the amplifier can operate and its choice specifies the rest of the bias circuit. The choices of load line and Q-point determine the bias values for V_{ce}, V_{ge}, as well as the bias resistor R_C.

4 Small-signal equivalent circuit model

There are many possible choices for the small-signal equivalent circuit model. Many models are too simplified to accurately represent the device near the upper cutoff frequency. It is especially important to include internal and external capacitances and resistances that may affect device performance at high frequencies. The equivalent circuit device model in Figure 3 includes the input and output capacitances C_1 and C_2, the actual device capacitances transformed by the Miller theorem. This transformation

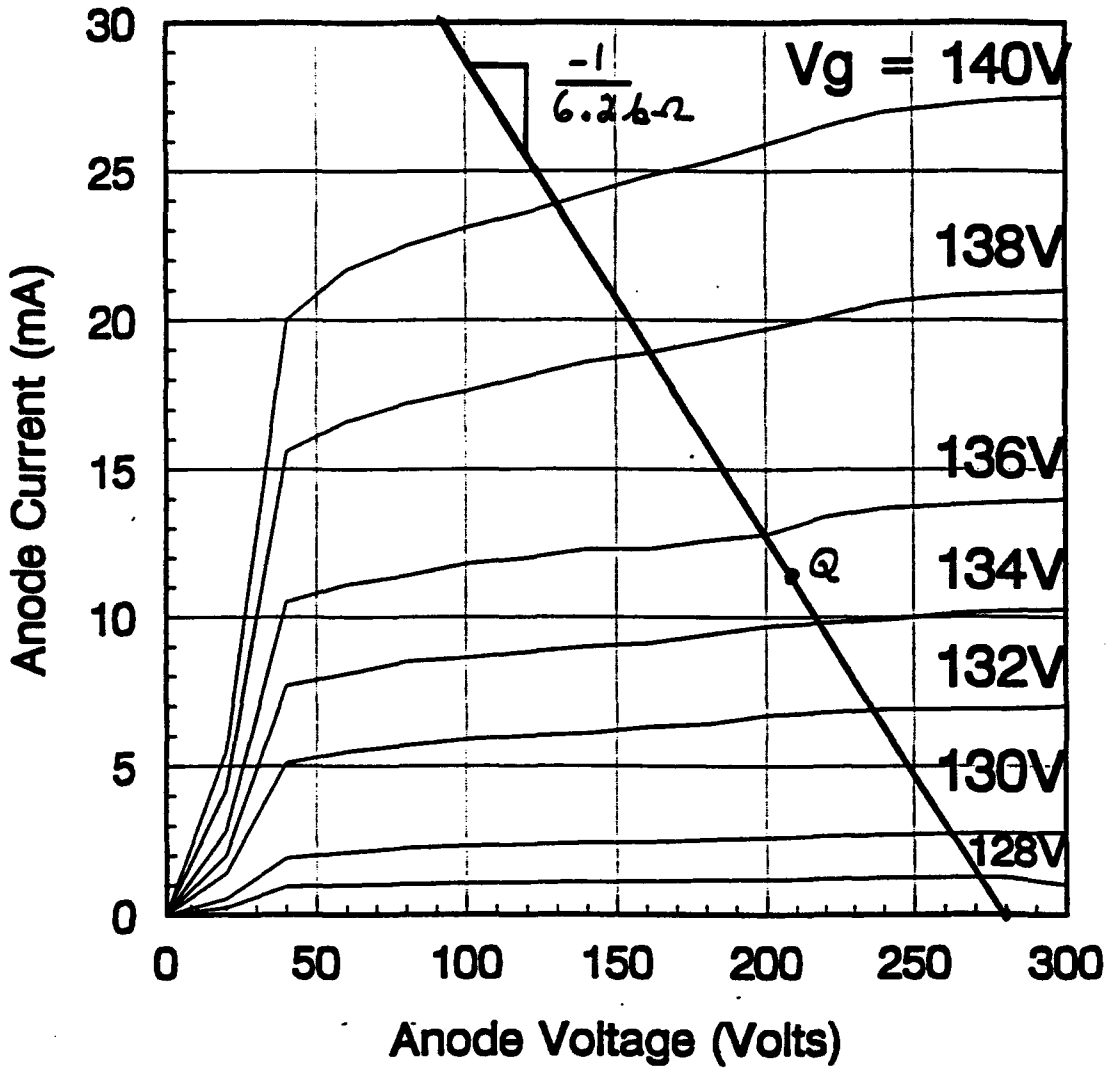


Figure 2: Typical DC output characteristics experimentally measured for an MCNC device.

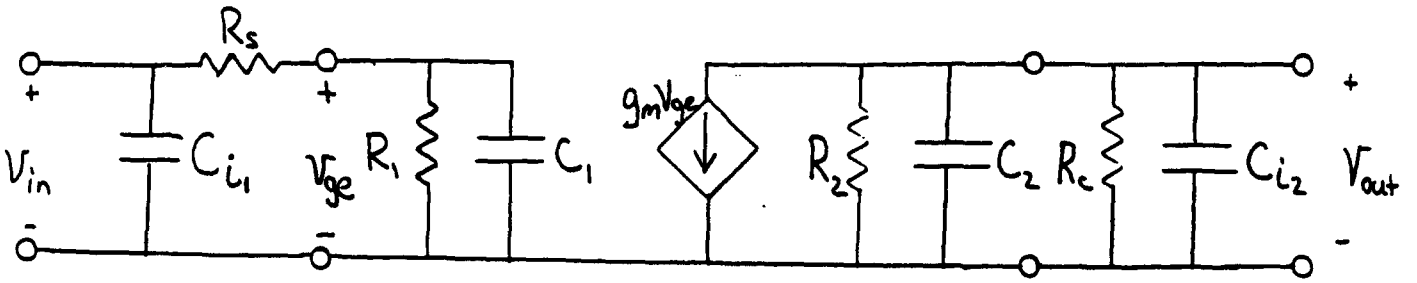


Figure 3: Small-signal equivalent circuit model for the field emitter amplifier.

is accurate below the cutoff frequency. The device model also includes the resistances of the SiO_2 layers R_1 and R_2, which are small, and a voltage-controlled current source indicating the active device. The transconductance, g_m, is a function of the operating point. In addition, the series lead resistance is included on the front end and the additional capacitance of the input and output circuits. These parameters are important at higher frequencies. As mentioned previously, the internal capacitances are derived from an electromagnetic analysis of the device using the Maxwell electromagnetic software by Ansoft Corporation. The output resistor, R_c, is the bias resistor. The input series resistance is estimated to be a few Ohms.

5 S-parameter representation

The s-parameters of the equivalent circuit are calculated using Mathematica on the NeXT computer. The s-parameters are voltage scattering ratios which are useful to characterize the device. Once the s-parameters are calculated, they can be used to determine the upper frequency for gain when the amplifier is matched at the input and output. Although the input and output matching circuits can only match the device at one frequency, an analysis of the matched circuit versus frequency provides useful information on how much gain can be expected at a given frequency. Ideally, the s-parameters would be measured in the laboratory at a frequency of interest. Then the matching circuits would be built, and the matched amplifier would be tested.

The s-parameter analysis is carried out by first finding the impedance matrix for sections of the equivalent circuit. Then, these impedance matrices are multiplied together in Mathematica. The resulting impedance matrix is converted to an s-parameter matrix. From this we can obtain s-parameters at different frequencies and use these to evaluate the gain of a matched amplifier made from the device.

6 Conclusion

We have presented a thorough device model of a small-signal amplifier using a field emitter as the active device. The model starts from first principles and includes electromagnetic modeling of the electric fields and device capacitances, a theoretical computation of the emitted current to provide the output characteristics, a choice of the Q-point and load line, an equivalent circuit model, and an analysis of the equivalent model using microwave techniques. It is hoped that this model will provide us with an increased understanding of the field emitter. Indeed, it has already provided information on possible matching schemes and circuit configurations. We expect that as more information is known about field emitter devices, our model will change to better reflect the new knowledge.

o Information about Maxwell 2D Field Simulator software available from Ansoft Corporation, Pittsburgh, PA, (412) 261-3200

Inclusion of the emitter resistance in the field emitter array model

Joseph E. Mancusi and William T. Joines
Duke University, 11/3/92

1 Introduction

Recent modeling efforts have not included the resistance of the emitter tip. The effects of emitter resistance may be significant, thus it is important to evaluate the effect of emitter resistance on the device model. Using z-parameters to represent the equivalent circuit, we have included the emitter resistance in the small-signal device equivalent circuit. In addition, the application of the Miller's theorem is explored by examining the equivalent circuit with and without the transformation.

2 Basic equivalent circuit

Ignoring the resistance of the emitter, we can denote the small-signal equivalent circuit amplifier as shown in Figure 1. We will denote this as the basic equivalent circuit. In this figure, R_1 and R_2 are due to the impedance of the SiO_2 layers, C_{ge}, C_{ce}, and C_{gc} are the device capacitances, and g_m is the small-signal transconductance. C_{ge} is capacitance between the gate and the emitter, C_{ce} between the collector and emitter, and C_{gc} between the gate and collector. These parameters are either experimentally measured, calculated, or estimated from the device materials and geometry. More information on these parameters is available in our other papers on modeling. Often Miller's theorem is used to transform the capacitance between the gate and the collector, C_{gc}, to the input and output sides, leaving no direct feedthrough. Although widely used at frequencies well below cutoff, we have found that the resulting model is not accurate for field emitter devices at the frequencies in which we are interested (around 1 GHz).

As can be seen from Figure 1, each element on the output side is in parallel with every other element on the output side. In addition, they are all parallel with the output sides of any other field emitter devices that are connected with them in an array. They are also in parallel with the load or bias resistors, and parallel inductances used for matching. The same statements are true for the input side. Thus, there is no problem understanding how to represent an array of field emitters. For a 10×10 array, each of the components add as if it were in parallel with 99 other components with the same value. Thus, the value of R_1 for the 100 device array, for instance, is $1/100^{th}$ of its value for a single device.

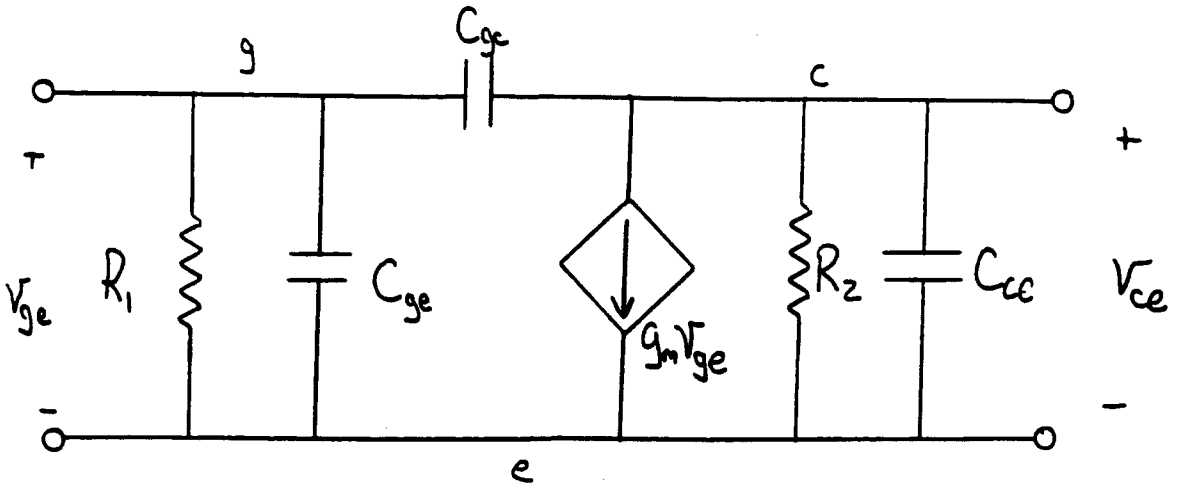


Figure 1: Basic AC equivalent circuit.

This model, however, ignores the emitter resistance. This resistance may be small. If so, its inclusion will not effect the performance of the emitter array substantially and it is justifiable to ignore it to dramatically simplify the equivalent circuit model. If appreciable, however, the emitter resistance changes the way we handle moving from the equivalent circuit model for one device to get the overall equivalent circuit for an array of devices.

3 Emitter resistance

The resistance of the emitter is not included in the basic equivalent circuit. Figure 2 shows the equivalent circuit upon inclusion of an emitter resistance. In the standard manner, we have replaced e by e' and given the physical connection to the emitter the symbol e. If we take e to be ground, then e' is no longer grounded. Therefore, v_{ge} and $v_{ge'}$ are now different. We apply v_{ge} but have no way of directly measuring $v_{ge'}$ which is the voltage that drives the output. Mathematically it is given by $v_{ge'} = v_{ge} - i_e R_e$, so it can be determined if we measure the emitter current and have an accurate value for R_e. If a device with the equivalent circuit of Figure 1 is connected in parallel with other devices, each component parameter simply adds in parallel. A device represented by the equivalent circuit of Figure 2 does not have any of its components in parallel with other devices in an array.

The tip of a field emitter device appears approximately as shown in Figure 3. The emitter is a silicon cone on top of a silicon column. Typical dimensions are shown in Figure 3. The conductivity of the doped silicon is about $\sigma = 10 S/cm$. To calculate the resistance, we can consider the emitter cone in two sections, the cylindrical base and the

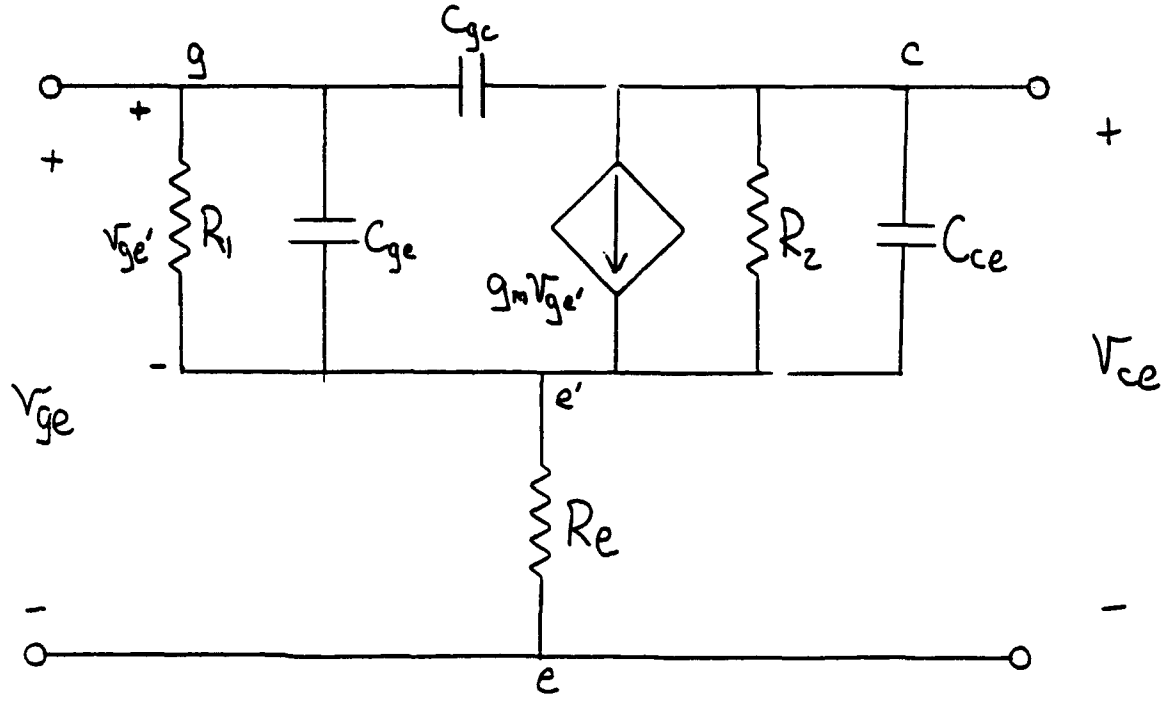


Figure 2: Equivalent circuit with emitter resistance included.

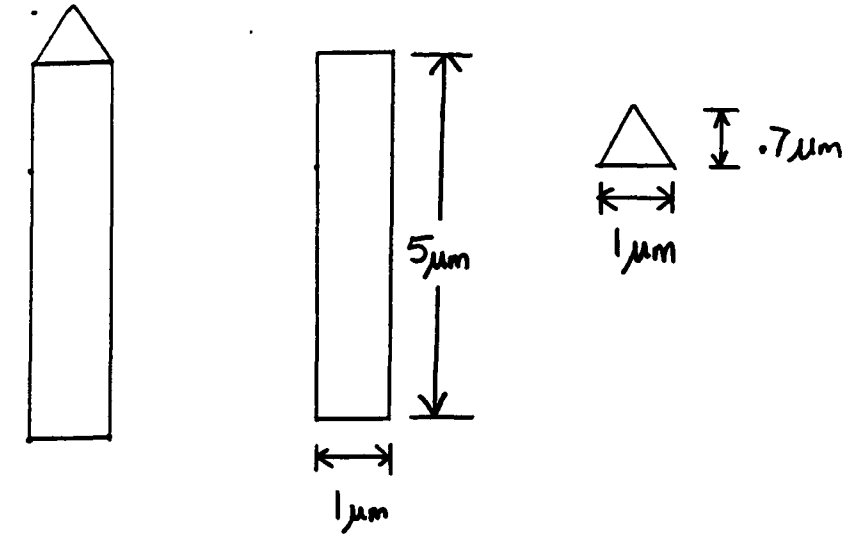


Figure 3: Geometry of the emitter cone for computing emitter resistance.

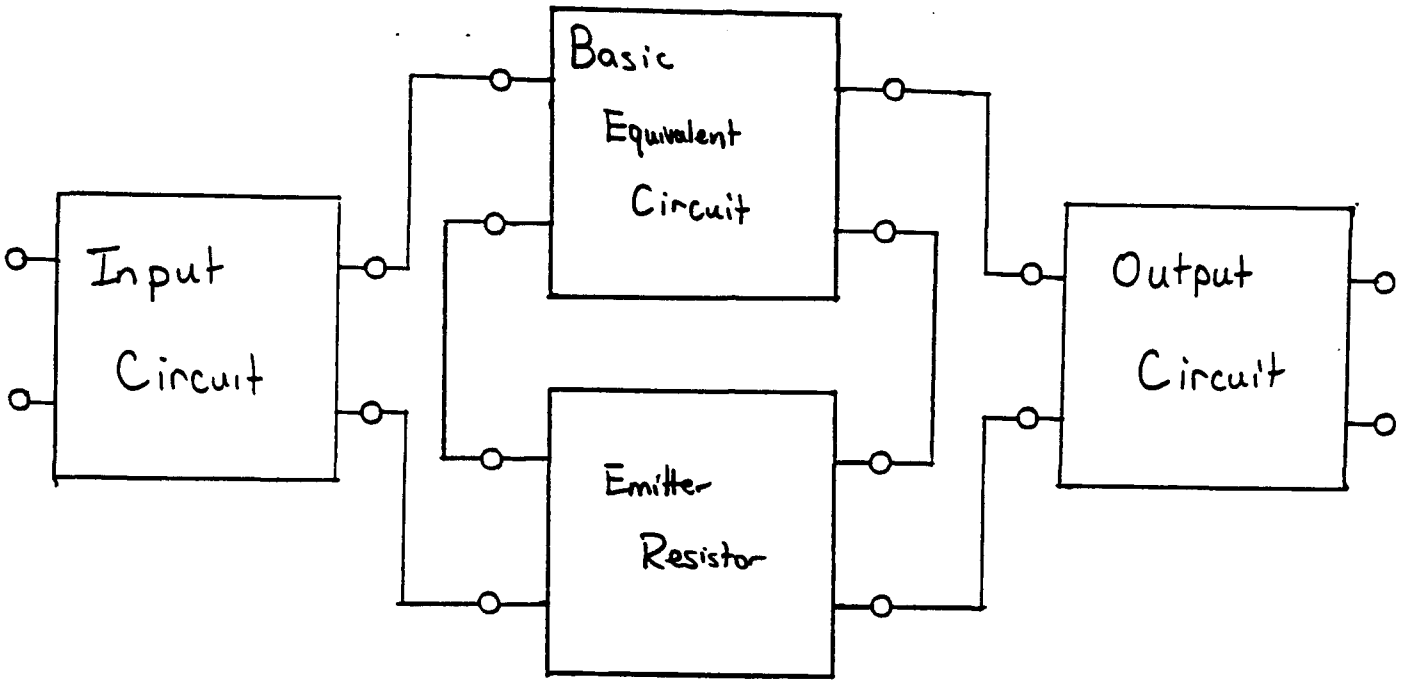


Figure 4: Overall network representation consists of combining smaller two-port networks which correspond to particular sections of the device.

conical tip. The base has a resistance of

$$R_{base} = \frac{1}{\sigma}\frac{h}{\pi r^2} = \frac{1}{10 S/cm}\frac{5\mu m}{\pi\,(.5\mu m)^2} = 6400\Omega \tag{1}$$

Similarly, taking the average cone width to be 1/2 of its base width, we have

$$R_{tip} = \frac{1}{\sigma}\frac{h}{\pi r^2} = \frac{1}{10 S/cm}\frac{0.7\mu m}{\pi\,(.25\mu m)^2} = 3600\Omega \tag{2}$$

Thus, the emitter resistance is the sum of these two resistances or $R_e \approx 10k\Omega$. Obviously, the estimation of the emitter resistance can change for different geometries. It is also dependent upon the conductivity of the emitter material. Current MCNC emitters use doped silicon emitters, but future emitters could be made from metal. In addition, emitters may be coated with substances such as Barium or diamond which may effect the resistance.

4 Network characterization

Characterization of a two-port network is accomplished by use of an equivalent representation of the network. These representations make use of the fact that it is enough to relate the current and voltage at the input to the current and voltage at the output. This can be specified with four parameters. The most commonly used parameters are the impedance parameters (z-parameters), the admittance parameters (y-parameters), the ABCD matrix, and the scattering parameters (s-parameters). Each of these has advantages and disadvantages for particular types of problems. Two-port network characterization has the advantage of breaking up the analysis of a network into sections and is flexible to changes.

The network of Figure 4 represents a field emitter array amplifier characterized by its equivalent two-port network parameters. The emitter resistance for a single device is represented by a two-port network in series with the basic equivalent circuit. The two together are represented by the center blocks of Figure 4. If the z-parameters of each of the above circuits are calculated, the two circuits in series are the sum of the individual z-parameters. Thus, for an array of identical field emitters in parallel, the z-parameters are the device z-parameters divided by the number of devices in the array. The resulting network is in cascade with input and output networks. Parameters for the overall device are obtained and represented by a matrix of frequency dependent complex numbers which represent the resistances and capacitances of the devices and the input and output circuits. From this matrix, the s-parameters of the amplifier are obtained.

The procedure outlined here is general enough to use on any linear two-port network and is easily implemented using software which performs symbolic matrix algebra, Mathematica, for example. The resulting ABCD matrix or s-parameters are functions of frequency. The model evaluates the field emitter arrays as amplifiers directly from their measured DC operating characteristics. Because the parameters are determined from experimentally measured characteristics, the model does not depend on knowledge of the exact microscopic tip structure. The measurement or calculation of the electric fields is not important since the Fowler-Nordheim equation is not used to calculate the transfer characteristics. The combination of experimental and estimated parameters makes this model very flexible. Due to the inclusion of the emitter resistance, it has the potential to be quite accurate for predicting the performance of a device when used as an amplifier.

ATTACHMENT D

DARPA SUBPROGRAM AT UNCC
FIELD EMITTER ARRAY RF AMPLIFIER DEVELOPMENT

NOISE IN FIELD EMITTER ARRAYS

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Prof K. DANESHVAR
MAYA DEEPAK (graduate student)

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OBJECTIVE:

DETERMINE CAUSES AND METHODS OF CONTROL OF NOISE IN FIELD EMITTER VACUUM MICROELECTRONIC POWER AMPLIFIERS

BACKGROUND:

- **NOISE AND DRIFT MECHANISMS NOT ESTABLISHED**
  1/f NOISE AND CURRENT DRIFT LIMIT AMPLIFIER STABILITY
- SPACE CHARGE CURRENT LIMITATION METHODS UNUSABLE
- NO SYSTEMATIC ATTACK ON FIELD EMITTER NOISE EXISTS
- 1-D MODELS OF ELECTRON TUNNELLING ARE INADEQUATE

ATTACHMENT D

NOISE IN FIELD EMITTER ARRAYS

APPROACH:

- QUANTITATIVELY MODEL NOISE AND DRIFT MECHANISMS IN INTEGRALLY GATED MCNC FIELD EMITTER ARRAYS
- EXPERIMENTALLY TEST NOISE MODELS IN REALISTIC VACUUM ENVIRONMENTS
- DETERMINE EFFECT OF EMITTER NOISE ON AMPLIFIER PERFORMANCE
- INVESTIGATE METHODS OF NOISE CONTROL IN FIELD EMITTER ARRAY DEVICES
- DEVELOP A QUANTITATIVE TUNNELLING THEORY

ATTACHMENT D

NOISE IN FIELD EMITTER ARRAYS

PROGRESS:

- LOW FREQUENCY NOISE MECHANISM FOUND:- INTERACTION BETWEEN ADSORPTION SITES ON TIPS $\approx 1/\omega$ SPECTRUM
  - COULOMB REPULSION ON SEMICONDUCTOR EMITTERS.
  - THERMAL INTERACTION ON METAL TIPS

- FULL 3-D ATOMIC TUNNELLING THEORY THRU ADATOMS USING BARDEEN'S TRANSFER HAMILTONIAN METHOD)

- PROVISIONAL MODEL OF EMISSION DRIFT:- E-BEAM DESORPTION OF GATE ADATOMS BY CURRENT INTERCEPTION

- UHV SYSTEM FOR INVESTIGATING FIELD EMITTER NOISE AND EMISSION DRIFT ASSEMBLED

ATTACHMENT D

NOISE IN FIELD EMITTER ARRAYS

PLANS:

- NUMERICAL EVALUATION OF LOW FREQUENCY EMITTER NOISE (SEMICONDUCTOR & METAL TIPS (2 PAPERS IN PROGRESS)
- EXPERIMENTAL TEST OF NOISE MODELS BY CONTROLLED EXPOSURE TO RESIDUAL GAS SPECIES:
- COMPLETION OF 3-D CALCULATION OF ADATOM-INDUCED FIELD EMISSION ON SEMICONDUCTOR & METAL TIPS
- CALCULATION OF AMPLIFIER NOISE FIGURES
- TEST CHANGE IN GATE STRUCTURE TO ELIMINATE DRIFT

NOISE IN FIELD EMITTER ARRAYS

SIGNIFICANCE OF 1/F NOISE

RMS CURRENT IS RELATED TO THE MEASURABLE SPECTRAL DENSITY BY

$$\langle I^2 \rangle = \int_0^{\omega_c} d\omega \; G_I(\omega)$$ where ω_c is the device cut-off

THEN IF $G_I(\omega) \sim A/(\omega + 1/\tau)$, BREAKDOWN OCCURS AT MTBF $\equiv \tau/A$

1/F NOISE MODEL

- 1/F NOISE MODELS REQUIRE A RANGE OF RELAXATION TIMES τ
- ADATOM ON EMISSION SITE PRODUCES CURRENT STEPS WITH ACCOMODATION TIMES τ
- RANGE OF τ VALUES IS PRODUCED BY ADATOM INTERACTION ON NEIGHBORING SITES WITHIN RANGE $\Delta L \sim \sqrt{}$(EMISSION AREA)
- INTERACTION IS THERMAL AND DEPENDS ON CURRENT
- PRODUCES 1/f NOISE FOR SMALL EMISSION AREAS

ATTACHMENT D

NOISE IN FIELD EMITTER ARRAYS

PRELIMINARY MODEL FOR EMISSION DRIFT

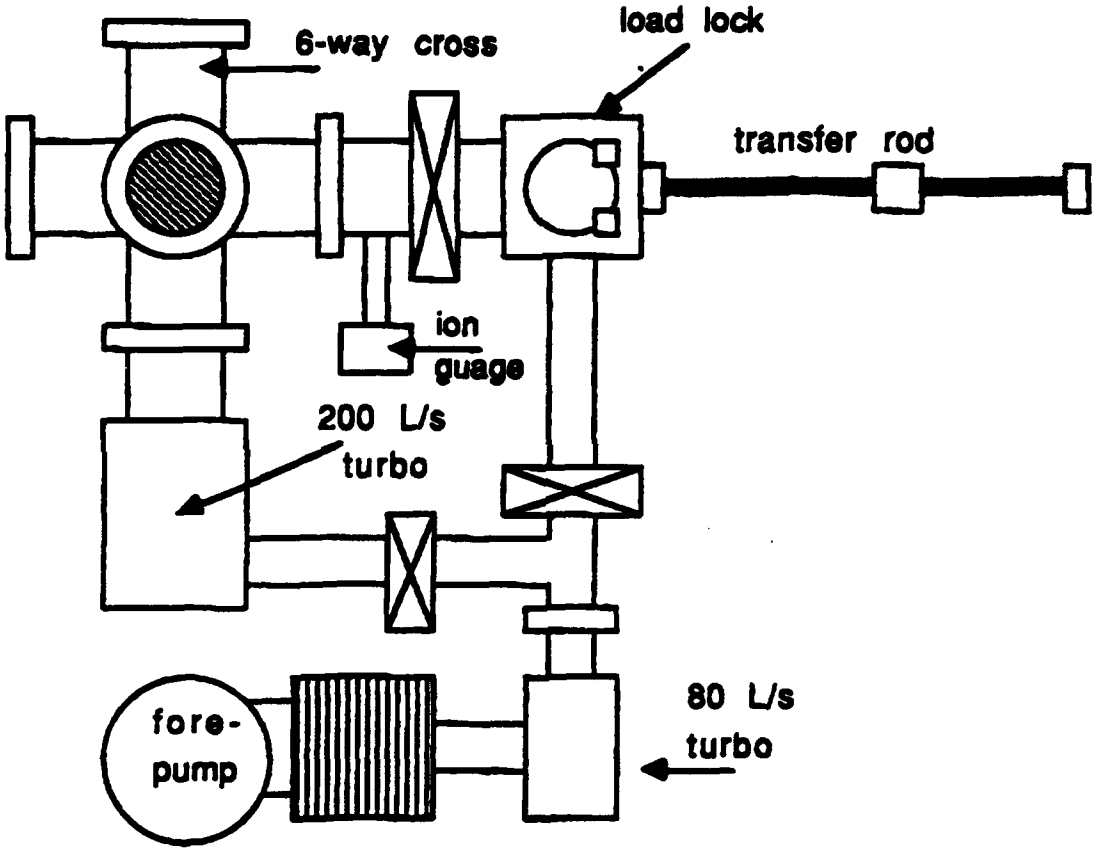
QUALITATIVE PICTURE: CHANGE IN GATE WORK FUNCTION PRODUCED BY e-BEAM DESORPTION OF ADATOMS ON EXTRACTION GATE UNDER LOW LEVEL CURRENT INTERCEPTION. CHANGE IN GATE WORK FUNCTION ACTS AS CHANGE IN EFFECTIVE GATE VOLTAGE.

SIGNIFICANCE:

IF DRIFT MODEL TESTS OUT IT WILL INFLUENCE DESIGN OF LOW INTERCEPTION EXTRACTION GATE

ATTACHMENT D

NOISE IN FIELD EMITTER ARRAYS



COMPLETED UNCC UHV SYSTEM:

NOTE: ELECTRONICS AND GAS HANDLING SYSTEMS NOT SHOWN

- DETERMINE EFFECT OF EMITTER NOISE ON AMPLIFIER PERFORMANCE
- INVESTIGATE METHODS OF NOISE CONTROL IN FIELD EMITTER ARRAY DEVICES
- DEVELOP A QUANTITATIVE TUNNELLING THEORY

2

3

ATTACHMENT E

October 8, 1992

REPORT ON THE TEST OF THE FIELD EMISSION DEVICES
(Vacuum Micro-Electronics)

Litton received six field emission chips from MCNC for test and evaluation. These chips were supplied to Litton without any lead connections to the cathode and the grid and the anode electrode was missing. As Litton Solid State has sufficient experience and adequate equipment to install the anode and attach necessary leads, the devices were handed over to them for these operations.

After attaching the leads and installing the anodes, the devices were returned to Litton Electron Devices for test and evaluation. All the six chips were installed around the circumference of a conflat flange, and the entire assembly was thoroughly cleaned with Acetone and then properly sealed for vacuum environment as shown in picture 1. A 2 liter Vac Ion pump was permanently attached to the assembly to ensure that the pressure inside remains below 10^{-6} Torr. The assembly was subjected to an exhaust system, where it was baked at 200°C and the pressure was brought down to 10^{-6} Torr. The unit was then pinched off.

The station pressure before pinch off = 4×10^{-6} Torr
Pressure after pinch off = 3×10^{-6} Torr.

The unit was then put on a pump supply. The pump drew 50 mA current at turn on and the 2 liter pump started to get very hot. High pressure air was blown on the pump to cool it down and then the pump started. After about 15 minutes the current went down to 125 uA. Finally the current stabilized to 2.7 uA. From the above phenomenon it seems that the chips were emitting some type of gases, and the pump was constantly eliminating these gases. In order to ensure that there was no leaks, the unit was leak tested several times. The pump was turned off for several hours and turned on again. The power supply current went up for a short time and then finally stabilized at 0.2 uA.

The test was then performed using the circuit as shown in figure 2. Sample #1, Sample #2 and Sample #3 did not respond at all to the applied voltages. Sample #4 and Sample #5, respond somewhat and the test results are attached. One of the connections to Sample #6 was broken during installation and thus it could not be tested.

From the data obtained from Sample #4 and Sample #5 it indicates that the applied field at the anode had no effect on the cathode current. Initially the 20 MΩ resistor was connected to the cathode lead, and current through this resistor varied only when the grid voltage was varied. The anode voltage was varied form 0 to 400 volts and the cathode current did not alter at all. In order to be sure that the field at the anode has no effect, the resistor was moved to the anode circuit and the experiment repeated. No current flow could be observer when the anode voltage was varied.

ATTACHMENT E

Figure 3 is the grid Voltage Vs cathode current characteristics of sample #5 at anode voltages of 300 volts, 350 volts, and 400 volts. The characteristics indicate that the anode voltage has no effect on them. Figure 4 is the characteristics of all the three together. Figure 5 is the grid voltage vs cathode current characteristics of sample #4 at zero voltage at the anode.

After the test the devices were taken down to Litton solid state for detecting any physical damage to the chips. Their findings are as follows:-

(1) Anode gates were burnt. Chip damaged. Anode being pushed up and burned.

(2) No physical damage. All ribbons connected.

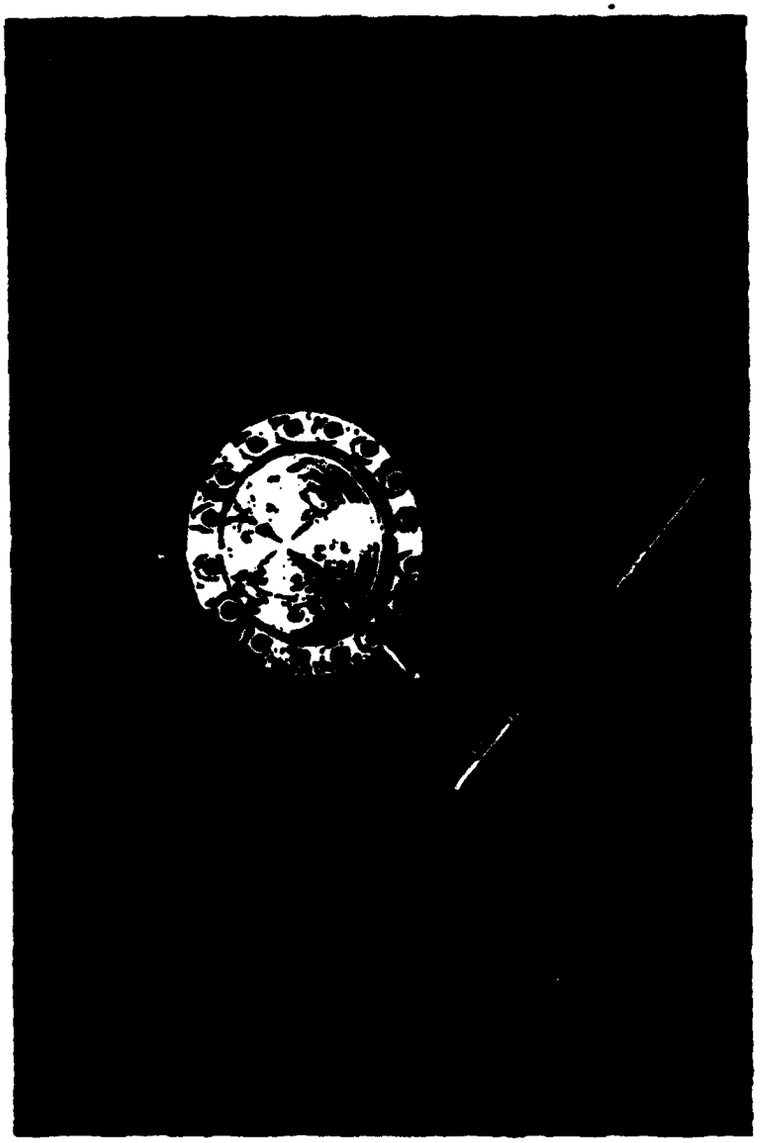
(3) No physical damage. All ribbons connected.

(4) No physical damage. All ribbons connected.

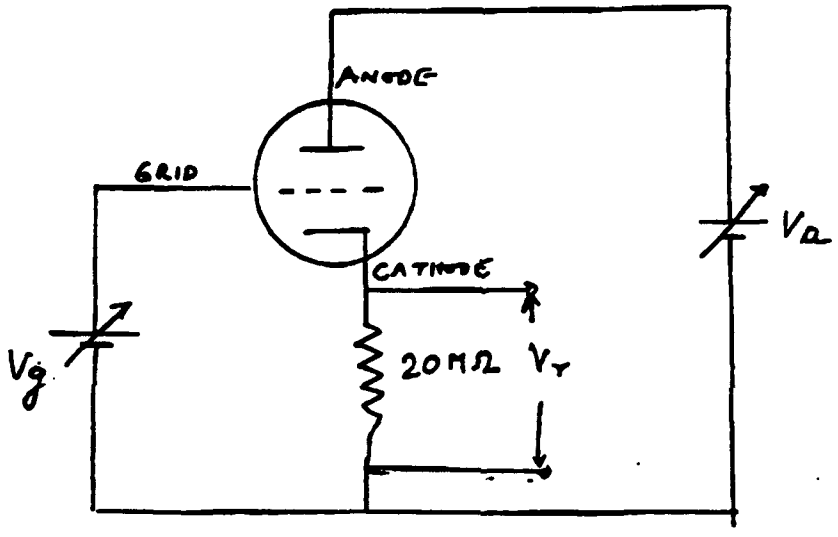
(5) No physical damage. All ribbons connected.

(6) Cathode wires burnt. Anode open. Chip damaged.

Figure 6 depicts the condition of sample #1 and sample #6. In both these cases the chips were damaged. Figure 7 indicates the location of the anode, which is about 90um away, and SCM photograph of the damaged chip #1.



Picture 1



Schematic of the experimental circuit

Figure 2

SAMPLE # 5

Vg	Vr	Ik	Va			
Volts	Volts	nA	Volts			
20	0.0123	0.615	300			
30	0.0336	1.68	300			
40	0.0739	3.695	300			
50	0.1402	7.01	300			
60	0.243	12.15	300			
70	0.3903	19.515	300			
80	0.5969	29.845	300			
90	0.8744	43.72	300			
100	1.2394	61.97	300			
20	0.0117	0.585	350			
30	0.033	1.65	350			
40	0.0727	3.635	350			
50	0.1395	6.975	350			
60	0.2437	12.185	350			
70	0.3854	19.27	350			
80	0.5948	29.74	350			
90	0.8775	43.875	350			
100	1.2324	61.62	350			
20	0.0124	0.62	400			
30	0.0345	1.725	400			
40	0.0763	3.815	400			
50	0.1445	7.225	400			
60	0.2486	12.43	400			
70	0.3984	19.92	400			
80	0.6076	30.38	400			
90	0.88905	44.4525	400			
100	1.2445	62.225	400			
Vg		Ik				

ATTACHMENT E

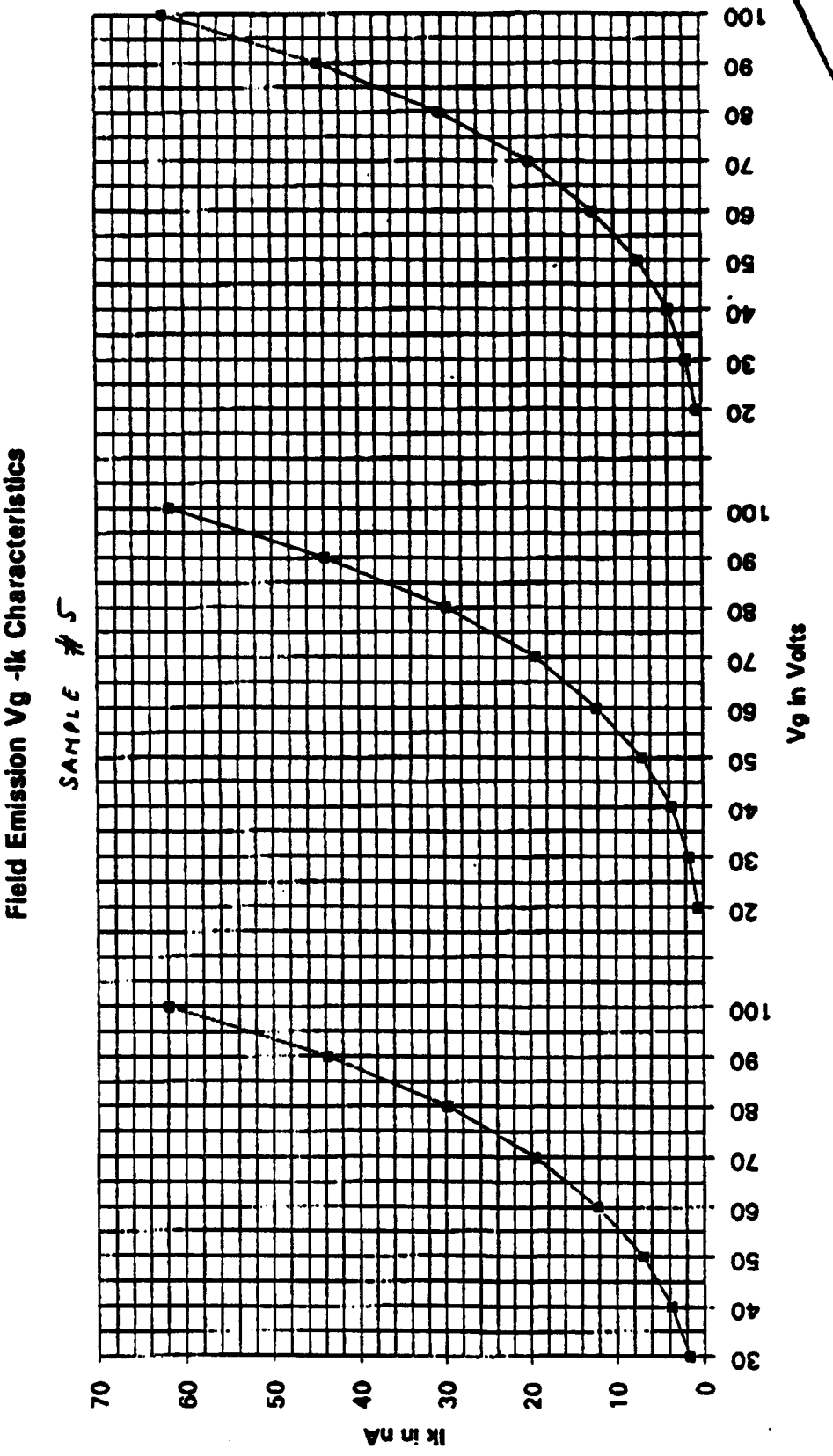


Figure 3

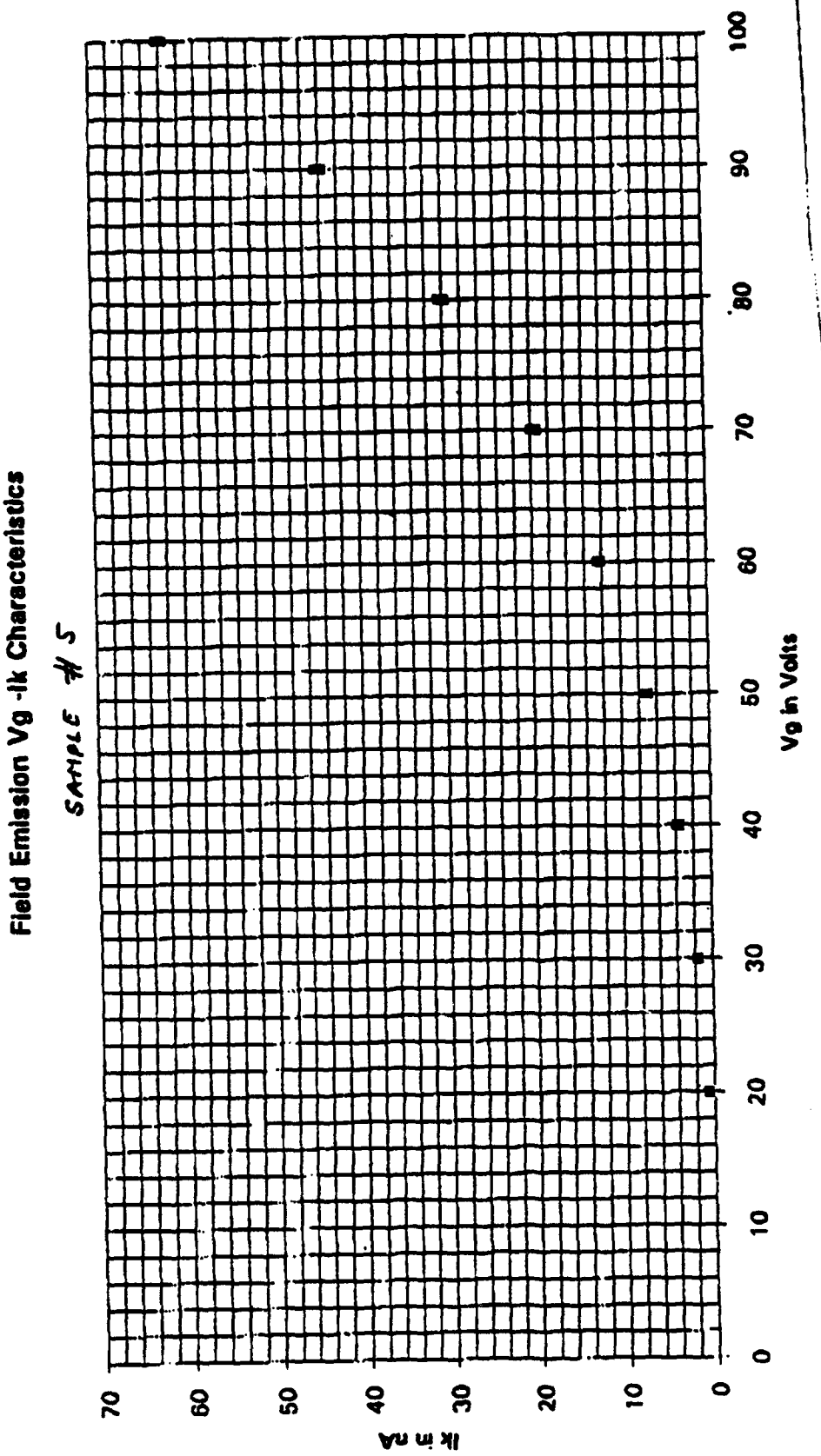

Field Emission Vg -Ik Characteristics
SAMPLE # 5
Vg in Volts
Ik in nA
0
10
20
30
40
50
60
70
80
90
100
70
60
50
40
30
20
10
0

Figure 4

SAMPLE # 4

Vg	Vr	Ik	Vi			
20	2.8	140	0			
30	5.92	296	0			
40	10.05	502.5	0			
50	15.02	751	0			
60	20.5	1025	0			
70	26.9	1345	0			
80	34	1700	0			
90	41.5	2075	0			
100	49.7	2485	0			

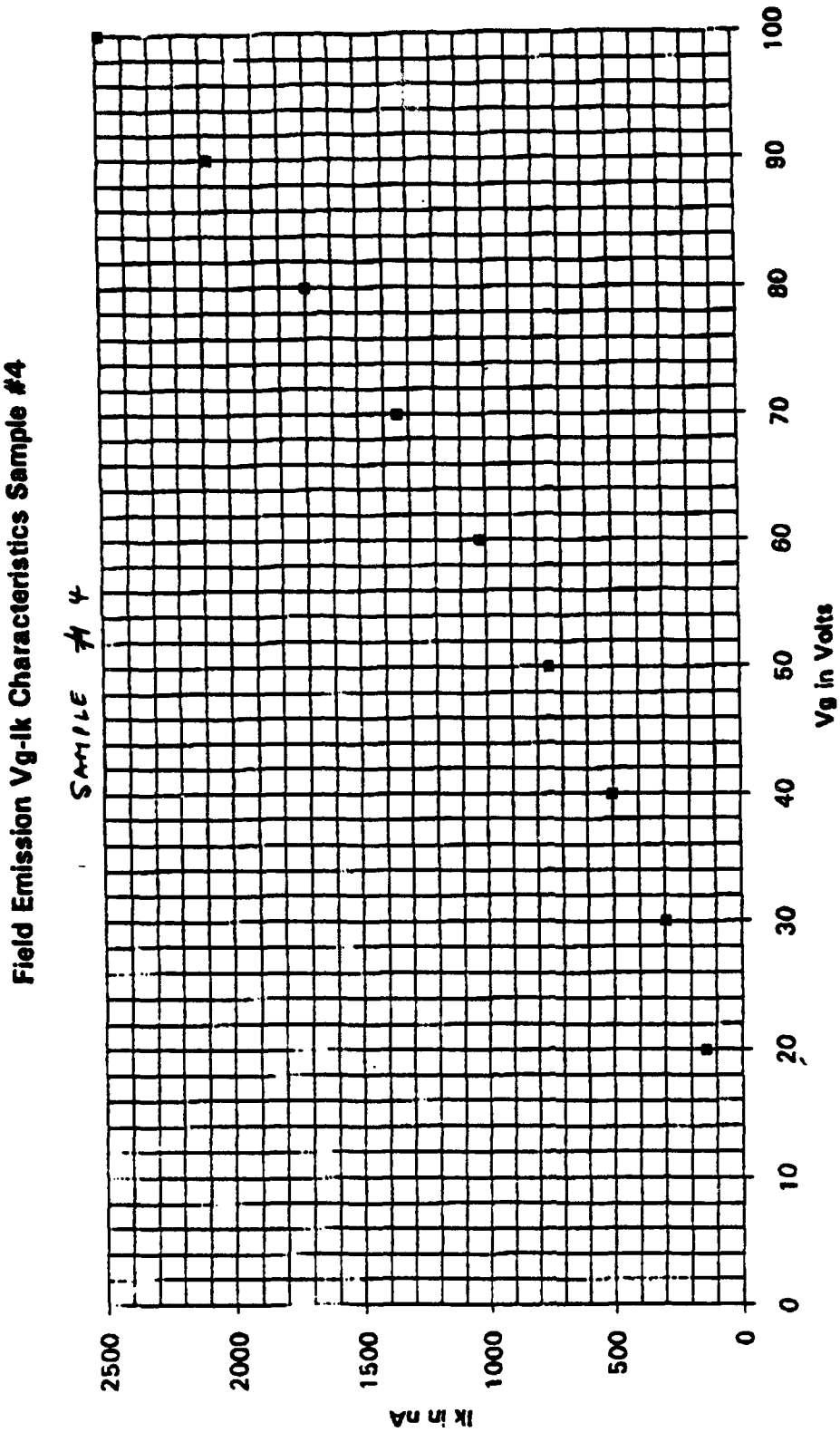
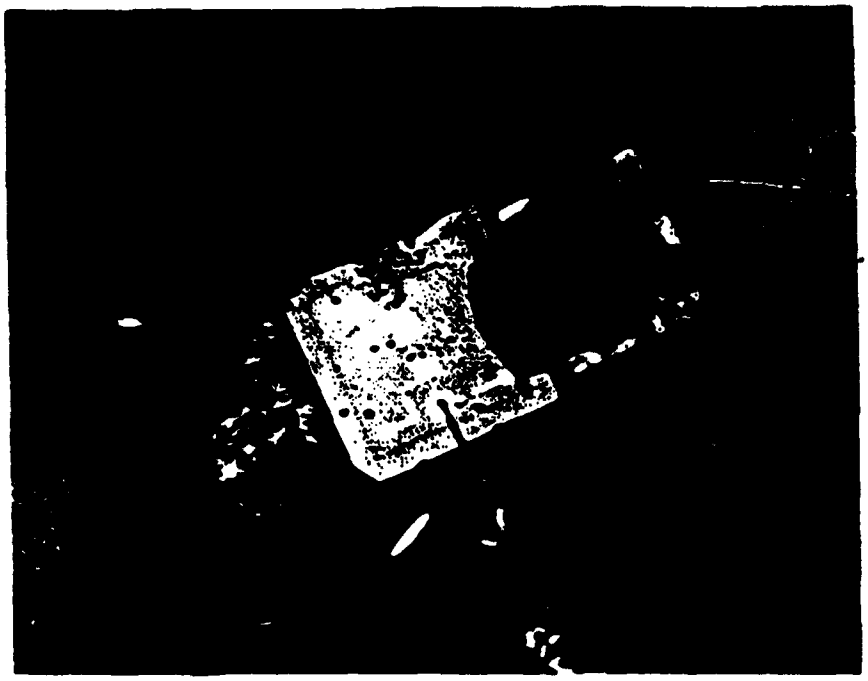
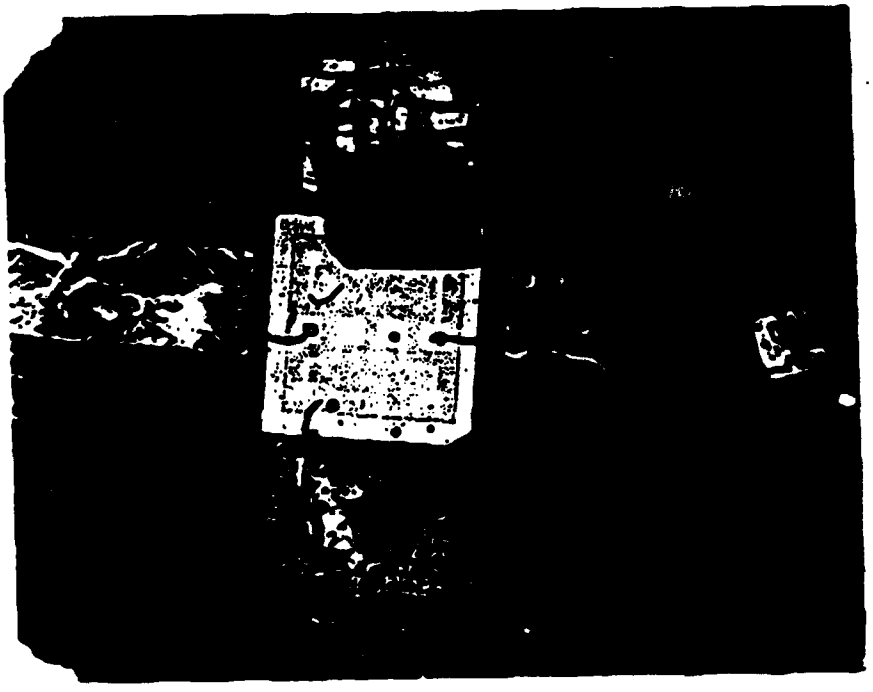

Field Emission Vg-Ik Characteristics Sample #4
SAMPLE #4
Ik in nA
2500
2000
1500
1000
500
0
Vg in Volts
100
90
80
70
60
50
40
30
20
10
0

Figure 5

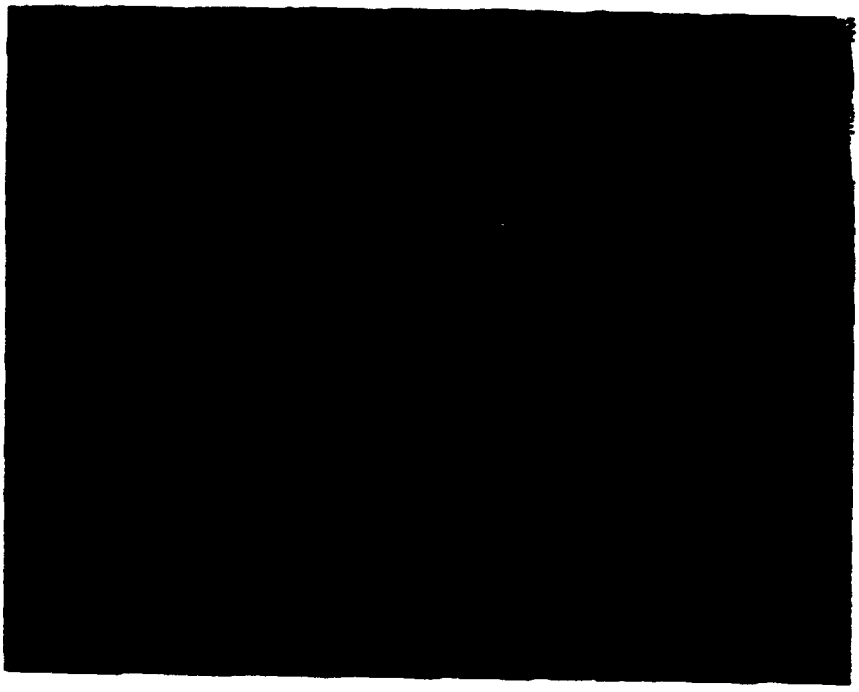


SAMPLE #1



SAMPLE #6

Figure 6



Picture of the damaged chip #1

Figure 7

MEMO

Field Emitter Devices/DFT

CHRISTIAN A. BALL

SRC TOPICAL RESEARCH CONFERENCE CHEM-MECHANICAL POLISHING FOR PLANARIZATION SEPTEMBER 14-15, 1992 RENSSELAER POLYTECHNIC INSTITUTE TROY, NY

TRIP REPORT

Chemical Mechanical Polishing (CMP) is fast becoming the new method of planarization for the semiconductor industry. In the past, the use of reactive ion etching for single and double level metallization planarization became common. As feature sizes become smaller (0.25um) and the complexity of the metal interconnects rise to triple, quad and more levels, it has become necessary to achieve much more planar surfaces. The use of chemical mechanical polishing has provided a method to achieve the planar surfaces needed for the future semiconductor devices.

The fabrication of the field emitter devices also requires planar surfaces at critical stages in the process sequence. The development of the gated column structure has led to the need for the planarization of the arrays. Attempts to planarize by RIE have not been successful. We must now look for alternative methods for creating planar surfaces. Chemical mechanical polishing (CMP) can provide the kind of planarization necessary for the development of the field emitter arrays.

Earlier this month the SRC held a conference at Rensselaer Polytechnic Institute in Troy, NY. There were approximately fifty representatives from most of the major semiconductor firms in the country. There were three major areas involving CMP that were discussed. They were: oxide planarization, CMP physics and the use of CMP on metals and polymers.

The first area of discussion, oxide CMP, was the most valuable to the field emitter devices. Unfortunately, most of the discussions involved the planarization of CMOS type devices, but

the basic technology is the same for the field emitter applications. The mechanisms of CMP of oxides, uniformity and polishing rate control, the physics of polishing, the characterization of polished oxides and the effects of water on SiO2 were the major topics discussed.

The second session covered the basic understanding of the CMP process. This included equipment related problems, slurry composition and polishing pad manufacturing. Modelling of the CMP process was presented and an analysis of the rotational kinetics during CMP was discussed. This area was dominated by the equipment and slurry-pad manufacturers.

The third session covered the polishing of metals and polymers. The Damascene Process was investigated. Polishing copper, aluminum and tungsten were also reviewed.

Most major semiconductor companies are now involved with chemical mechanical polishing (CMP). Some of the companies reported that they were currently using CMP in production with good results (IBM). The CMP process is in an infant state at this time. The issues of uniformity and repeatability are the greatest drawback to this new technology. Everyone is attempting to stabilize the process with limited results. There were four equipment manufacturers present but their basic knowledge of semiconductor processes is limited and their equipment requires a great deal of development to provide a stable, uniform and repeatable process.

The SRC workshop was a very good forum for information exchange. The development of the CMP process and equipment may become important to the semiconductor industry. The use of CMP in a controlled form is definitely needed in the development of the field emitter devices. I have contacted all of the vendors at the seminar and they all expressed interest in polishing some wafers for MCNC (at no cost). The conference notes are available for anyone interested in CMP.

Regards,

Chris Ball

FIELD EMISSION IMAGING STUDY OF SILICON FIELD EMITTERS

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ABSTRACT

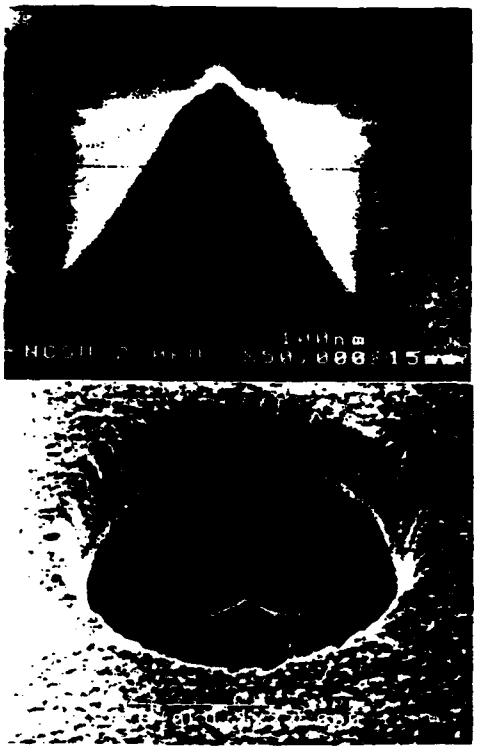
The behavior of electron emission from pyramid-shaped silicon field emitters has been studied by direct imaging of electron emission as well as by emission current-voltage measurement. Oxide covered silicon emitter surfaces have resulted in structureless emission patterns. The electron emitting angle is found to vary significantly with the extraction voltage or the emission current. Experimental measurement and analysis of emission images under moderate operating conditions showed that resulted final emitting angles are under 13° while initial electron emitting angles from the emitter could be as high as 18°.

INTRODUCTION

Recently, both metal and semiconductor field emitter arrays (FEAs) have been successfully fabricated and studied toward their ultimate applications such as: high-current-density electron source [1], flat-panel displays [2,3], and vacuum microelectronics [4]. With its small emitting angle and narrow energy spread, the electron beam emitted from a field emitter may also used as an ideal probe for scanning electron microscopy (SEM) [5], electron beam lithography [6], and electron holography [7]. To achieve most of these applications, it is important not only to have a low operating voltage at the desirable emission current density, but also to know the emitted electron beam optics. We present here our results on direct imaging of electron emission from silicon field emiters. The behavior of emitting electrons under lens-free configurations can be learned from emission images and the emission current-voltage characteristics. In addition to theoretical modelling and simulations [8], direct trajectory studies may also shed light on the design and miniaturization of electron optical system in practical devices.

FIELD EMITTER FABRICATION

The silicon field emitters used in the present studies were fabricated in doped n-type ($N_d = 10^{17}$ cm^{-3}) <100> silicon substrates by using orientation-dependent etching (ODE) techniques. A silicon oxide layer was first grown on the silicon wafer by thermal oxidation, and then patterned photolithographically and processed by reactive ion etching (RIE). A follow-up ODE results in square sided pyramidal field emitters which are bounded by <111> planes as shown in Fig. 1(a). The pyramids were further sharpened by linear dry oxidation at 850 °C in order to form the point like shape on the top. The platinum extraction gate with a 1.6 μm opening was formed over the dielectric layer of silicon oxide by self-aligned CVD process. After the final oxidation and cleaning processes, silicon emitters were formed at a radius of curvature less than 30 nm. Fig. 1(b) shows a SEM micrograph of a gated single silicon field emitter used in this study.



(a) (b)

Fig. 1. SEM micrographs of typical single silicon field emitter: (a) emitter pyramid; (b) metal gated emitter device.

EXPERIMENTAL PROCEDURES

Our experimental studies were carried out in an imaging atom-probe field ion microscope (FIM)/field emission microscope (FEM) system. A ~10^{-11} torr range background vacuum can be achieved in this system by turbomolecular and ion/sublimation pumping system. The silicon emitter was mounted on a specimen holder. Its position and orientation can be manipulated outside the UHV chamber. A Faraday cup is installed into the system to assist the electron emission study. A part of the experimental setup is shown schematically in Fig. 2. Several BERTAN power sources were used for the operating voltage of emitters and to bias the detectors. Operating current and voltage were recorded by Keithley 614 and 617 electrometers and a 196 digital multimeter. All these electrical devices and power sources are connected to the emitter by UHV electrical feedthroughs. Field emission images of the silicon emitter were displayed on the Chevron microchannel plates (MCP)-fiberoptic imaging assembly, and the emission current was directly collected in the biased Faraday cup. Meanwhile, electron currents were also measured from the gate and the substrate in correspondence to emission currents and images. Since the trajectories of emitted electrons are affected by the electric field between the extraction gate and the MCP anode, voltages across the anode and the emitter gate were also closely monitored during the electron emission imaging process. This information will be relevant to deducing the field distribution.

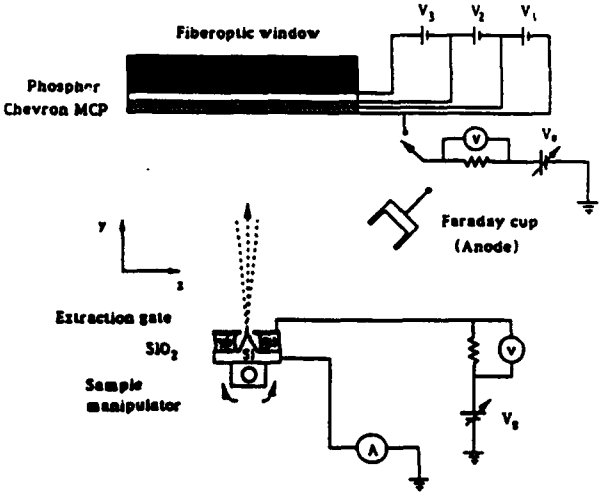


Fig. 2. Schematic of the experimental setup used in field emission imaging study.

ELECTRON EMISSION IMAGING AND CURRENT MEASUREMENT

Field electron emission data has been collected from single silicon emitters as well as from emitter arrays. For the purpose of studying electron trajectories, our measurements were focused on single emitters. During the emission imaging and current measurement, the vacuum was usually kept at 10^{-8} to 10^{-9} torr range without baking the vacuum chamber. The electric field needed for the emission is created by the positive voltage applied on the extraction gate with the silicon emitter base grounded. The emission current was detected at Faraday cup starting from the sub-picoamper range, and increased to around 1 to 2 μA at extraction voltages of about 150 volts. Fig. 3 shows the current-voltage characteristics of a typical single emitter. They followed the Fowler-Nordheim relation very well.

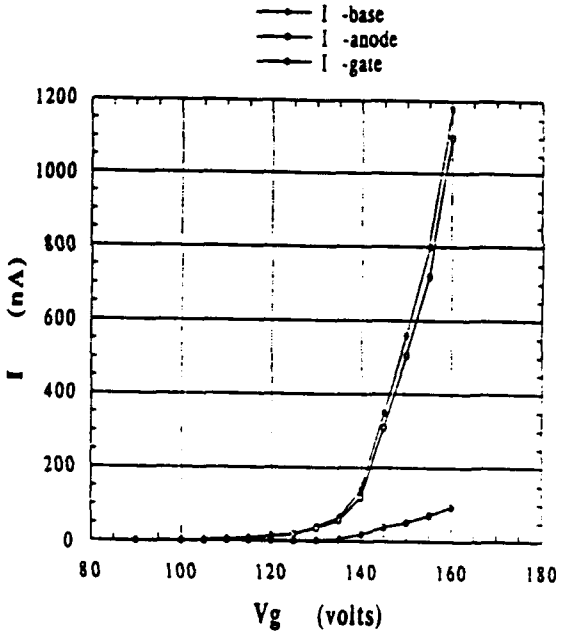
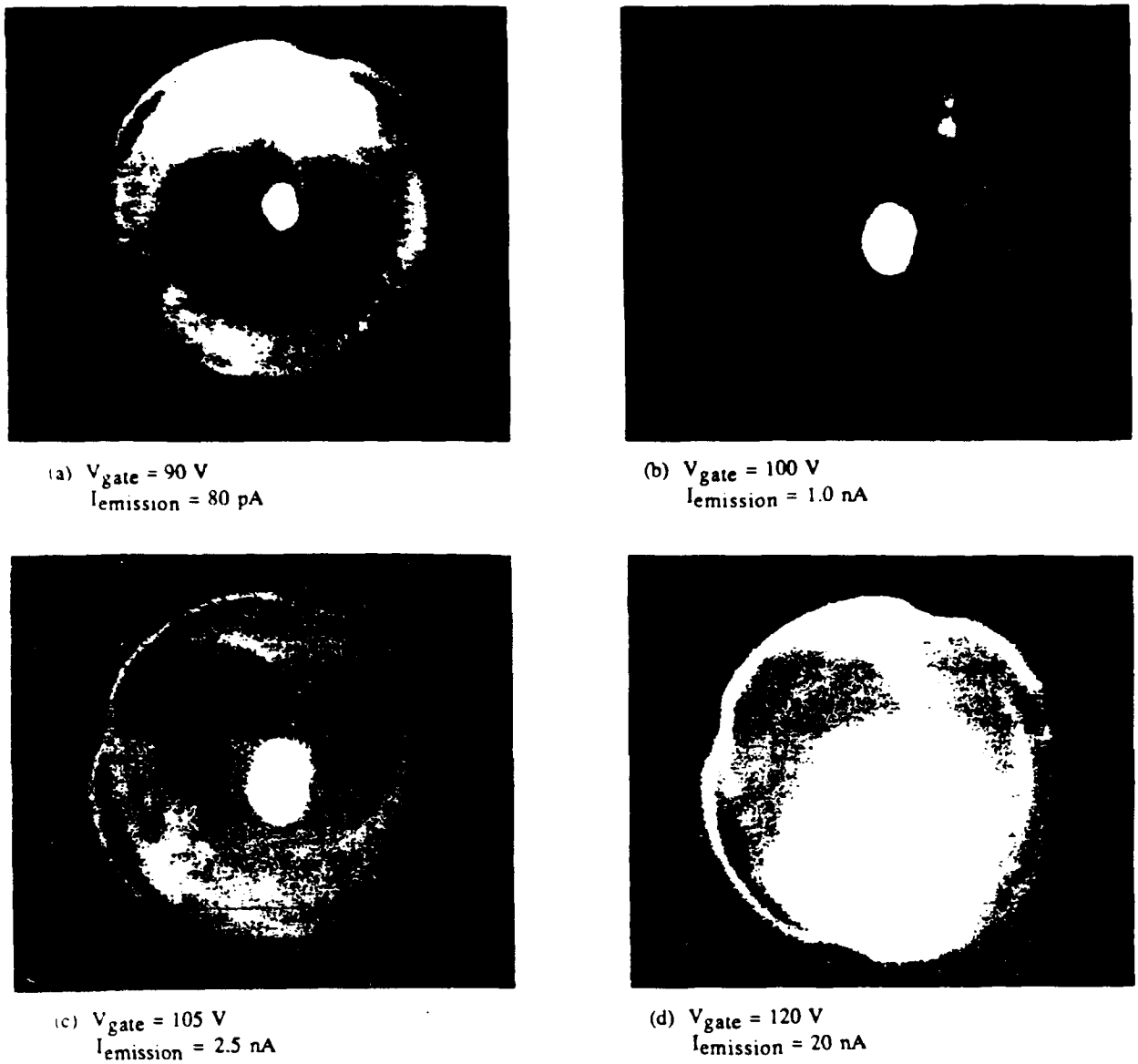


Fig. 3. The emission current-voltage characteristics of a silicon single emitter.

The electron emission image was first observed from the MCP-fiberoptic imaging assembly at an emission current of a few picoampers, where the electric field on the emitter surface is close to the silicon FE field (~3.5 V/nm). Emission images were continuously obtained thereafter as the emission current increased. The imaging distance was varied from 20 to 50 mm between the emitter and the imaging assembly. The size and intensity of emission images were found to change significantly with extraction voltage or emission



(a) V_{gate} = 90 V
$I_{emission}$ = 80 pA

(b) V_{gate} = 100 V
$I_{emission}$ = 1.0 nA

(c) V_{gate} = 105 V
$I_{emission}$ = 2.5 nA

(d) V_{gate} = 120 V
$I_{emission}$ = 20 nA

Fig. 4. Field emission images of the single silicon emitter. The MCP imaging assembly was biased at 400 volts.

current. The anode (MCP) bias was also found to influence the FE images below 400 volts. Fig. 4 shows four emission images under different extraction voltages at an imaging distance of 40 mm and anode bias of 400 volts. The uniform pattern of the images reveals that the Si emitter surface is covered with native oxide layer. This thin oxide layer and other contaminants can be removed from the Si surface by field evaporation in a H_2 environment. Since the trajectories of emitted electrons were affected by the electric field between the MCP anode and the extraction gate, the electron beam exhibited a resultant lateral drift which can be directly measured from the fiberoptic window. The corresponded emitting half angle, θ, can also be determined from this lateral drift of electrons and the imaging distance. In our experiment, θ was found to change from ~3° to 13° under moderate operating condition.

INTERACTION BETWEEN EMITTED ELECTRONS AND ELECTRIC FIELD

The experimental setup in our study does not involve any electrostatic lens. The emitted electron beam

will only be affected by the electric field which is created by the voltages on the emitter gate and the MCP anode. The equation of motion of electrons in this field can be expressed as:

$$\frac{d^2(\vec{x} + \vec{y})}{dt^2} = \frac{e}{m}\vec{E} \quad . \qquad (1)$$

where e and m are charge and mass of electrons. Eq. (1), however, does not have analytical solutions because of the form of $\vec{E}$. To estimate electron trajectories, we may consider that the electric filed is only uniformly distributed along the y direction, for which:

$$\vec{E} = \left(\frac{V_g - V_a}{d}\right)\frac{\vec{y}}{y} \quad . \qquad (2)$$

By considering the initial velocity of an electron when it leaves the horizontal plane of the extraction gate, and the initial emitting angle ϕ, we can deduce the relation between the imaging distance and the lateral drift δ of an electron at the MCP anode to be:

$$d = \frac{\cos\phi}{\sin\phi}\delta + \left(\frac{V_a - V_g}{d}\right)\frac{\delta^2}{4V_g\sin^2\phi} \quad . \qquad (3)$$

The initial emitting half angle of an electron which has the final drift δ can then be determined as:

$$\phi = \frac{1}{2}\sin^{-1}\left[\frac{2\alpha - \alpha^3\beta + \alpha(4+4\beta-\alpha^2\beta^2)^{1/2}}{2(1+\alpha^2)}\right] , \qquad (4)$$

where $\alpha = \delta/d$, $\beta = (V_a - V_g)/V_g$. Fig. 5 shows our measured final drift half angle θ and derived initial emitting half angle ϕ of the electrons. It can be seen that the emitting angle of electrons can be significantly reduced by the uniform electric field. The final drift half angle was found to be below 13° under the operating condition of emitting current up to 20 nA. The initial emitting half angle was determined to be as large as 18° when electron leave the emitter surface.

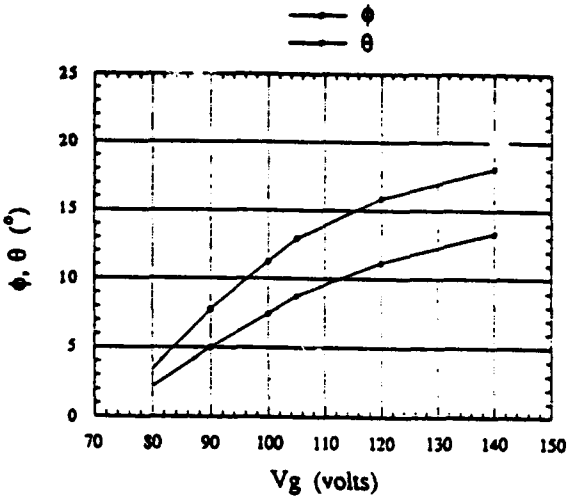


Fig. 5. The measured final drifting angle and the derived initial emitting angle of electrons emitted from a silicon emitter.

SUMMARY

Fowler-Nordheim type of field emission images of the pyramidal Si field emitter have been obtained and used to study the trajectories of emitted electrons. It was found that the final drifting angle of electrons can be significantly reduced by the electric field between the gate and display anode. In our experimental setup, however, the reduction effect of the electron emitting angle will be smaller than that of the uniform field because of the non-uniform distribution of the electric field between our anode and the emitter gate. In other words, our measurements have provided the extreme values. Both initial and final emitting angles in a real lens-free flat-panel display would tend to be smaller than our measured results.

ACKNOWLEDGMENTS

The project support from DARPA under contract no. MDA972-91-C-0028 is gratefully acknowledged.

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