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7a. NAME OF MONITORING ORGANIZATION: Office of Naval Research

6c. ADDRESS (City, State, and ZIP Code):
1400 NW Compton Drive, Suite 340
Beaverton, OR 97006

7b. ADDRESS (City, State, and ZIP Code):
Code 251A GBP
Ballston Tower One, 800 North Quincy Street
Arlington, VA 22217-5660

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Pattern Recognition
Image Processing

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Effort on Phase 1 tasks continued and good progress was made during this reporting period. The hardware design of the CNAPS/PC board was completed and five (5) prototype boards were fabricated. Preliminary debug of the boards has been successfully completed. Very good progress was made on the software port and debug of the CNAPS-C compiler and the source-level debugger. Progress was made, but not as much as planned, on the software port and debug of the OEMlib control software to the CNAPS/PC hardware and the DOS/Windows environment.

At the time of this report, the project has expenditures and commitments totaling 66% of the funds allocated for Phase 1 of the contract.

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22a. NAME OF RESPONSIBLE INDIVIDUAL: Wendell Henry

22b. TELEPHONE (Include Area Code): (503) 690-1236

22c. OFFICE SYMBOL

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R & D Status Report

May 23, 1994

ARPA Order No.:

A407

Contractor:

Adaptive Solutions, Inc.
1400 NW Compton Drive, Suite 340
Beaverton, OR 97006

Contract No.:

N00014-93-C-0234

Contract Amount:

$1,299,714.00

Effective Date of Contract:

November 8, 1993

Expiration Date of Contract:

June 7, 1996

Principal Investigator:

Wendell A. Henry

Telephone Number:

(503) 690-1236

Title of Project:

High Performance Hardware and Software for Pattern Recognition and Image Processing

Title of Work:

R&D Status Report

Reporting Period:

February 1, 1994 through April 30, 1994

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Project Summary:

Effort on Phase 1 tasks continued and good progress was made during this reporting period. The hardware design of the CNAPS/PC board was completed and five (5) prototype boards were fabricated. Preliminary debug of the boards has been successfully completed. Very good progress was made on the software port and debug of the CNAPS-C compiler and the source-level debugger. Progress was made, but not as much as planned, on the software port and debug of the OEMlib control software to the CNAPS/PC hardware and the DOS/Windows environment.

At the time of this report, the project has expenditures and commitments totaling 66% of the funds allocated for Phase 1 of the contract.

Description of Progress:

The previous Project R&D Status Report stated the following as the objectives for this reporting period:

During the next three months work will continue on Phase 1 of the contract and the following is expected to be achieved:

1. *Complete the design of the CNAPS/PC board*
2. *Complete fabrication and assembly of the first prototype of the CNAPS/PC board*
3. *The CNAPS/PC board will be undergoing debug and test*
4. *The preprocessor for the CNAPS-C compiler will have been completed and in test*
5. *The control software for the CNAPS/PC board will have been completed and in test*
6. *The CNAPS-C source-level debugger will still be in implementation.*

The following sections discuss the specific progress made in this reporting period in the hardware and software areas towards the stated objectives.

Hardware

Design:

Design of the CNAPS/PC board was completed. RTL-level modeling and simulation of the design was completed. Logic synthesis of the FPGA code was designed, simulated, and debugged.

Once the design was considered complete and error free, the netlist of the board design was generated and the design was prepared for component placement and route. The software tool PADS 2000, which runs on a 486 based PC was used to perform signal routing of the CNAPS/PC circuit board. Mechanical drawings for fabrication of the circuit board were also prepared. Once the signal routing had been completed the design was sent to a contractor for fabrication and assembly. Five prototype boards were built.

Testing:

Preliminary testing of the CNAPS/PC board has been completed. A complete set of hardware diagnostics were implemented. These were used to perform hardware functional testing. At this time the hardware is passing all tests and no modifications to the hardware design have been required. System-level testing which can be more extensive and exhaustive will begin when the control software becomes available (see next section).

Software

Design and Implementation:

Implementation of the preprocessor for the CNAPS-C compiler was completed and debugged. Documentation of the preprocessor is in progress. Implementation of the "separate compilation" facility of the compiler was completed and debugger.

Implementation of the CNAPS-C command-line debugger was completed and debugged. Implementation of the CNAPS-C graphical interface using the Galaxy graphical interface builder tool was completed and debugged. This version of the debugger will be used to port to the Windows NT environment.

Work on the implementation of the control software (OEMlib) required to interface the software with the CNAPS/PC board continued. The port of the software has been completed. Debug of the software is in progress. Debug of the control software has taken longer than planned. Porting of the software from the multi-tasking, 32-bit UNIX environment to the single-task, 16-bit segment/offset DOS/Windows environment has been more difficult than anticipated. Delays in the completion of the control software is impacting the completion of other tasks in this project. This portion of the project is approximately 4 weeks behind schedule.

Testing:

Unit-level testing of the CNAPS-C compiler preprocessor and the separate compilation facility have been completed. Unit-level testing of the OEMlib control software is underway. System-level testing will begin when the unit-level testing of the control software has been completed.

Issues and/or Concerns:

The project is making excellent progress except in the area of the port of the control software to the DOS/Windows environment. There is no concern over whether the port of the control software is technically feasible, the concern is simply that the port is taking longer than originally planned. The delay in the completion of the control software will not impact the funding required for the completion of the Phase 1 tasks; no incremental funding above the original agreed amount will be required for the successful completion of Phase 1 of the project.

Plans For Next Reporting Period:

During the next three months work will continue on Phase 1 of the contract and the following are expected to be achieved:

1. Complete the port of the OEMlib control software to DOS/Windows.
2. Complete the System-level testing of the CNAPS/PC board.
3. Complete the System-level testing of the CNAPS-C compiler preprocessor and separate compilation facility.
4. Beta testing of the CNAPS/PC board will be in progress.

Fiscal Status:

Amount currently provided on contract:	$1,299,714.00
Expenditures and commitments to date:	198,655.57
Funds required to complete work:	$1,101,058.50
Phase 1 funding:	$300,000.00
Expenditures and commitments to date:	198,655.57
Phase 1 funds remaining:	$101,344.43

At the time of this report, the project has expenditures and commitments totaling 66% of the funds allocated for Phase 1 of the contract.

Wendell A. Henry

Wendell A. Henry

5/23/94

Date