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CONSORTIA FOR KNOWN GOOD DIE (KGD) PHASE I

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13. ABSTRACT *(Maximum 200 words)*

This report describes the results of Phase I of the Infrastructure for KGD program at MCC. The objective of the work is to resolve the issues for supplying and procuring Known Good Die (KGD) in a way that fosters industry acceptance and confidence in Application Specific Electronic Modules (ASEMs for military systems) and MultiChip Modules (MCMs for commercial systems).

This report is divided into four sections. Section I describes the technical assessment of proposed industry approaches to KGD implementation.

Section II of the report contains an outline for the plan for industry and government cooperation for the demonstration, validation, and implementation of KGD methodologies identified in this Phase I study.

Section III of the report contains the industry-generated requirements for KGD implementation.

Section IV of the report contains the KGD specifications for TAB and flip chip ICs.

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Infrastructure for Known Good Die (KGD)
Phase I Report

This report describes the work done in Phase I of the Infrastructure for KGD program at MCC. The work is being funded through an ARPA contract (F33615-93-C-1213). The objective of the work is to resolve the issues for supplying and procuring Known Good Die (KGD) in a way that fosters industry acceptance and confidence in Application Specific Electronic Modules (ASEMs for military systems) and MultiChip Modules (MCMs for commercial systems).

The bulk of the Phase I work has been accomplished by a task group of industry volunteers from semiconductor manufacturers, ASEM foundries, MCM assemblers and users and equipment suppliers. The task group has met six times in the first half of 1993 to develop TAB and Flip Chip addenda to the *KGD Procurement Specification*[1], and to develop *The Technology Assessment Guidelines for Method, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product,*[2] which is being used in this program to evaluate technology being used or proposed to assure known good die. The six task group meetings have been attended by 81 different persons representing 37 different companies for a total attendance of 187 persons. In addition, a KGD supplier forum was held in Austin in May 1993, which was attended by 85 industry representatives. At the forum, 14 suppliers of bare die test, burn-in, pack and ship or inspection equipment made presentations about their KGD approach.

This report is divided into four sections which correspond to the four major tasks included in the contract statement of work. Section I describes the results of SOW paragraph 4.1.3, to identify and evaluate proposed industry approaches to KGD implementation. A survey form was sent to 26 companies that were identified by industry sources as developing test and/or burn-in technology for producing KGD. The survey was followed up with a phone call to each of the companies. The initial survey results indicated that 16 KGD technologies were being actively developed for test and burn-in of bare die or minimally packaged die. The companies plan to make the technology available to the industry through licensing, direct sales, or providing test and burn-in service.

Since the original survey, we have identified eight additional methods being developed for test and burn-in technology for KGD. Section I of the report details the technologies being developed by each of the companies and provides the results of the technical assessment, readiness review and costs.

Section II of the report contains an outline for the plan for industry and government cooperation for the demonstration, validation, and implementation of KGD methodologies identified in this Phase I study. This is paragraph 4.1.4 of the contact SOW.

Section III of the report describes the results of SOW paragraph 4.1.2, to compile and prioritize industry requirements for KGD implementation. The work completed for this task is contained in Revision 3.0 of *The Technology Assessment Guidelines for Method, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product.*[2] This document is contained in its entirety in Section III, including test methods with descriptions of how to test each requirement.

Section IV of the report contains the results of the SOW paragraph 4.1.1, to complete the KGD specifications to encompass die for TAB and flip chip bonding applications. This work is complete and the specifications have been submitted to JEDEC J-13 subcommittee on TAB as addenda to the original wirebond KGD procurement spec.[2]

[1] Standard for Known Good Die (KGD), submitted to JEDEC by MCC/Sematech task team in September, 1992.
[2] Referred to in this document as Technology Assessment Guidelines or TAG.

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1.0 Executive Summary

The bulk of the work done in phase I has been an assessment of the KGD Assurance Technologies that are being proposed in industry for single die test and burn-in, and that take advantage of the existing packaged part test and burn-in methods, equipment and strategies. The assessment was based on the *KGD Technology Assessment Guidelines (TAG)* developed by the task group composed of industry representatives. The TAG is contained in Section III of this report.

Table 1: Technical Assessment Overview

Company	Survey Rec'd	Desc Prov'd	Flow Desc.	TAG Scored
3M	✔			
Acsist Associates, Inc.	✔	✔	✔	✔
Aehr Test Systems	✔	✔	✔	✔
Amp, Inc.	✔			
California Contacts		✔	✔	✔
Chip Supply	✔	✔	✔	✔
Elm Technology Corp.	✔			
Elmo Semi Corp.	✔	✔	✔	✔
Fresh Quest Corporation	✔	✔	✔	✔
Hughes Aircraft Co. (TRB)	✔	✔	✔	✔
IBM (R3)	✔	✔	✔	✔
IBM (dendrites)	✔	✔	✔	✔
Micro SMT	✔	✔	✔	✔
Micron Semi (Softool)	✔	✔	✔	✔
Micron Semi (KGD^{plus})	✔	✔	✔	✔
MCC	✔	✔	✔	✔
MCNC	✔	✔	✔	✔
Modular Automation	✔			
nCHIP Inc.	✔			
Nitto Denko America	✔			
Northern Telecom		✔	✔	✔
Packard Hughes	✔	✔	✔	✔
Plastronics	✔	✔	✔	
Qualhi	✔	✔	✔	✔
TI/Micro Module Systems	✔	✔	✔	✔
Sandia Labs		✔	✔	✔
Stanford University	✔			
Tessera Associates	✔	✔	✔	✔
Tribotech	✔	✔	✔	✔
Yamaichi		✔	✔	✔

Table 2. Technical Assessment Summary

Company	Assessed TAG Score	Readiness	Contact Method
Acsist Assoc.	169	Conceptual	Temp contact
Aehr Test Sys.	173	Alpha Test	Temp contact
California Contacts	159	In development	Temp contact
Chip Supply	153	In production	Soft connect
Elmo Semi.	147	In production	Soft connect
Fresh Quest	165	Alpha Test	Temp contact
GE	150	Alpha Test	Soft connect
Hughes TRB	141	In development	Minimal Pkg
IBM (R3)	163	In production	Soft connect
IBM (dendrites)	165	In development	Temp contact
Micron Softool	144	In production	Soft connect
Micron KGD+	171	Alpha Test	Temp contact
MCC	163	In development	Temp contact
MCNC	162	In development	Soft connect
Northern Telecom	144	In development	Minimal Pkg
Packard Hughes	169	In development	Temp contact
Plastronics	153	Alpha Test	Temp contact
Qualhi	170	In development	Temp contact
Sandia	161	In development	Temp contact
TI/MMS	173	Alpha Test	Temp contact
Tribotech	171	In development	Temp contact
Yamaichi	173	In development	Temp contact

To begin the assessment, a survey of industry identified companies that were developing technology for test and burn-in of bare (or minimally packaged) die. Table 1 lists the companies that responded to the survey. The survey was sent to domestic suppliers only. A non-proprietary description of technologies was developed for the companies indicated, including a process flow — how to assemble and disassemble die for test and burn-in, and how each technology fared in a comparison with the *Technology Assessment Guidelines (TAG)*. The full descriptions of the various selected technologies assessed are contained in subsection 6.0 of this report.

Table 2 summarizes the technical assessment for three important parameters for the technologies under development. The Assessed TAG Score was derived from Revision 2.5 of the *KGD Technology Assessment Guide-*

lines developed by the task group. The TAG subcommittee of the task group assigned weights to each "rule" in the guidelines and the MCC technical staff judged whether the proposed technology could meet the guideline. If it was judged capable, the assigned weight was added to the score. The combined total is the Assessed TAG Score. Meeting all TAG rules, including test and burn-in parameters, accommodation of peripheral and array pads, bumped die as well as bare Al pads, earns a score of 175.

The readiness was determined through conversations, visits and, in some cases, nondisclosure agreements with suppliers. Only four technologies are in production today; the IBM R3 approach, which has been fully qualified through the "box" level by IBM, two temporary wirebond methods, Micron Softool and Elmo Semiconductor rerouted pad and wirebond approach, and Chip Supply SofTab, each of which has been qualified through some level of production.

Temporary contact probing is the dominant technology being pursued, and is the most capable of meeting the TAG rules. However, the problems associated with penetration of native oxides, probe to probe compliance and alignment have not been solved and there is not a consensus single best technology for making temporary probe contact to aluminum pads on bare die today.

Cost Modeling Results

A Monte Carlo simulation model was developed for examining the cost of KGD relative to packaged parts, focussing on highlighting the dominant cost drivers. Cost of KGD and packaged devices which go through test and burn-in are studied in the modeling effort by varying these key drivers and examining their sensitivities.

The model is capable of manipulating IC fab parameters (e.g., defect density, sort coverage, etc.), as well as packaging, test and burn-in costs. The phase I approach has focused on simulation modeling because the KGD technologies are not yet mature enough to proceed with a reliable cost of ownership type analysis.

Table 3. Generic Die Type

Case	Type	Size	I/O
1	ASIC	15 mm on each side	400 I/O
2	CPU	10 mm on each side	200 I/O
3	DSP	7.2 x 5.9 mm	74 I/O
4	DRAM	6.2 x 2.9 mm	38 I/O

The KGD cost model encompasses the entire KGD process, rather than isolated steps, using current industry accepted methods for test and burn-in. In developing the model, inputs were received from Sematech (wafer fab cost models, test inputs), Intel (burn-in cost model), Motorola (burn-in and test inputs), and IBM (process flow definition, cost model verification). Outputs are expressed as cost ratios of an equivalent conventionally packaged die.

Several generic device types that capture a wide range of key technology requirements were used to evaluate the cost impact of different KGD technologies in the modeling effort. (See Table 3). Plastic and ceramic packaging for these die types were assumed in forming a comparative cost analysis between bare and packaged KGD.

The above IC variations were combined in the model with other inputs relevant in the KGD process and key cost factors were identified. The key influence in this model is the package type to which KGD is being compared. The relative cost of KGD increases by up to a factor of 2 if it is compared to plastic rather than ceramic packaged parts. The key factors beyond package type, their cost impact and the necessary responses for achieving KGD economies are as follows:

- Number of carrier uses: High Cost Impact: Need carrier life of 100-1000 cycles with greater lifetime (up to the 1000 cycle limit) reducing cost. Cost impact of carrier lifetime decreases rapidly with higher number of cycles.
- Complexity of IC: High Cost Impact: Assembly cost for conventional packages is much more dependent on pin count than KGD.
- Recurring Cost of Carrier and Interconnect: Medium Cost Impact: Reduces material costs.
- Burn-in Hours: Medium Cost Impact: Shorter burn-in cycles mean more uses for a given interconnect thermal life.
- Time for Assembly/Disassembly: Medium Cost Impact: Shorter die load/unload times from carrier reduce labor costs and amortize cost of automation more rapidly.
- Equipment Costs: Low Cost Impact: Less expensive equipment reduces capitalization costs.

The emphasis of the cost study was to determine which factors had the greatest impact (and therefore demand the greatest future attention) when trying to achieve cost savings with KGD approaches. Further work is needed to validate the current model and develop the system specification for extensions to make this a useful tool for industrial users interested in evaluating specific cases. These specifications will be available to our phase II efforts and allow the model to be inserted into the MCC MSDA tool.

2.0 KGD Assurance Technology

Advances in reducing size and increasing functionality of electronics have been due primarily to the shrinking geometries and increasing parametrics of silicon. Recently, development efforts aimed at reducing size and increasing functionality have focused on the first level of the electronic package. The result has been the development of multichip modules (MCMs), a technology in which bare silicon chips are mounted on a single high density substrate that serves to "package" the chips, as well as interconnect them. A number of benefits accrue because of MCM packaging, namely, increased chip density, space savings, greater performance, and less weight. Therefore, MCMs are an attractive new technology for today's light weight, portable, high performance electronic equipment and devices.

In spite of these benefits, the MCM market has not shown the kind of explosive growth and expansion that was predicted[1]. A major inhibitor is the availability of fully tested and burned-in bare die, or "known good die."

Test and burn-in of bare (or minimally packaged) die is not a new requirement for IC makers; however, it has yet to be satisfactorily addressed. The IC industry currently does an excellent job of testing and burning-in traditionally packaged chips, although this can at times be a costly process. The resulting high quality, high reliability devices allow board-level products to be assembled with a high probability of success. Any board-level product failure will most likely not be due to component failure.

Table 4. Board Yield

Probability of KGD	Board Yield (10 ICs)	Board Yield (20 ICs)	Board Yield (40 ICs)
99.9%	99%	98%	96%
99%	90%	82%	67%
95%	60%	36%	13%
90%	35%	12%	1%
80%	11%	1%	0%
50%	0%	0%	0%

Table 4: Selected values of board (or module) yield when assembled with differing probability of KGD. As this chart show, board yield varies *exponentially* depending on die yield.

The following probability formula gives the expected yield of an assembled board:

$$Y_b = 100(P_c)^n$$

Y_b is the predicted board yield, P_c is the probability that an IC is good, and n is the number of ICs. Packaged ICs can approach 99.999% probability (considered to be known good) of performing correctly for some specified time in the final application. This probability index means that less than 10 parts out of one million will fail to perform their function correctly throughout a minimum guaranteed lifetime. The ability to fully test at-speed and over-temperature and to eliminate weak components with burn-in is not generally available or cost-effective for bare die. This significantly lowers the probability that a device will perform as specified over its expected lifetime. Table 4 shows the effect of lower KGD probability on the assembled MCM. Even with a 95% probability of KGD — which is typical of wafer probe results for very mature products — the resulting yield of the assembled board is unacceptable for

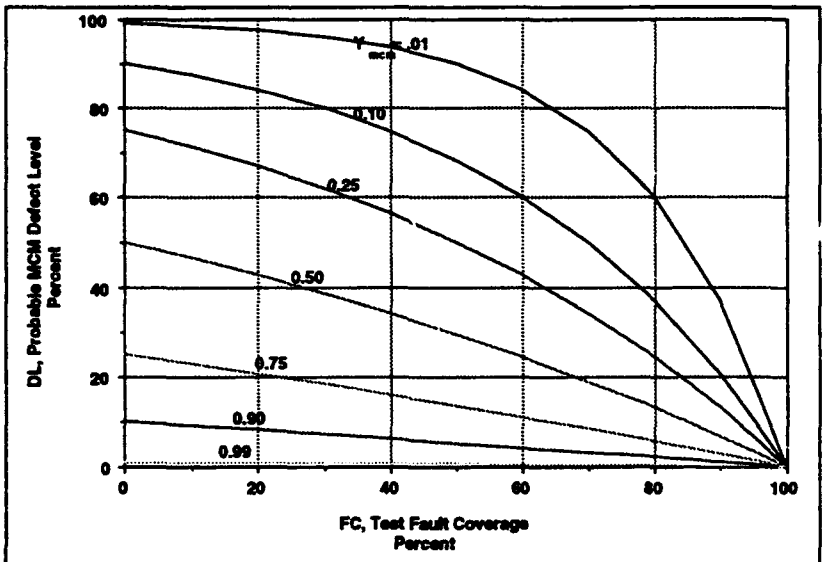

Figure 1: Probable MCM Defect Levels (probability of shipping defective module) vs. MCM Fault Coverage for Differing MCM Yields

Formula: $DL = 1\text{-}Y_{mcm}^{(1\text{-}FC)}$ x100

Low board yield at final test (a function of incoming die quality, manufacturing defects, etc.) is very difficult to "test out" of the product, requiring close to 100% fault coverage at the module level.

[1] MCM market projections for the year 2000 vary significantly — ranging from $2 billion to $20 billion — depending on the definition of the market, as well as the level of optimism concerning the industry's adoption and implementation of MCM technology.

systems with more than a few chips.

In addition, the test coverage required to identify the low yielding MCMs must be extremely high to avoid escapes. (See Figure 1.)

Thus, the lack of KGD is a crisis for today's MCM assemblers. Accelerating the widespread availability of MCMs in the short-term requires the development of KGD solutions that utilize existing processes and equipment — customizing them to meet the needs of KGD. Over the long-term, new KGD technologies and approaches that provide greater cost-effectiveness will be required. This report will focus on the near-term solutions which offer the most immediate access to KGD, which can be categorized as follows:

- Soft Connection Approaches
- Temporary Contact Approaches
- Minimal Package Approaches

Wafer Level Approaches are considered more long term and were not assessed in this project.

The most expedient KGD methods being proposed today take advantage of existing package-part test and burn-in infrastructure, tools, and supplies. In general, with these methods the die is mounted in a carrier that has the same form and function as a single chip package. Temporary electrical connection is made to the bond pads and the device is qualified through test and burn-in processes similar to the traditional packaged part. ATE test equipment, component handlers, burn-in boards, burn-in ovens, and loaders can be used. Once the die is qualified, electrical connections to the bond pads are released and the die is taken from the carrier. The result is a fully tested, qualified IC device with specifications comparable to those of an equivalent packaged part.

2.1 Soft Connection Approaches to KGD

Some KGD approaches consist of making a non-standard (or rerouted) connection (wirebond, C4, etc.) to a reusable standard package type; sending the assembly through test and burn-in, then breaking the connection, removing the die, inspecting and shipping. These approaches have been termed "soft" connections. Several technologies using soft connection are available for preparing KGD today, including temporary wire bonds and Reduced Radius Removal[3] (R3). These technologies rely most heavily on established processes and tools to condition die. In some cases, the soft connection technology is targeted toward a final assembly method exclusively, as R3 for solder-bumped die. Concerns with the cost effectiveness and final assembly limitations of some soft connection methods have resulted in heightened interest in temporary carriers with probe sets which are applicable to all die, regardless of final assembly methods.

Table 5. Soft Connection Methods

Company	Description
Chip Supply	SofTab Process: TAB tape frame is fabricated and lightly attached to gold bumped bond pads on the die. After burn-in and test using TAB equipment, the tape frame is removed. Also licensed is Micron Softool.
Elmo Semiconductor	Wafers are coated with a barrier material, bond pads are reformed for larger bond area. The die are packaged with thermoplastic die attach and wire bonded into a temporary reusable carrier. Following burn-in and test, the wire bonds are cut and the die are removed.
GE	Die are coated with a protective polymer and via holes are laser drilled to the bond pads. Temporary bond pads are formed on the overcoat and are used to wire bond die into a standard package. After burn-in and test, die are removed from the package and temporary bond pads are etched away.
IBM	Reduced Radius Removal (R3): Solder bumped die are reflow attached to reduced radius pads on a reusable ceramic substrate. Die are removed from carrier with a shearing process after burn-in and test.
Micron Softool	Temporary die attach and "soft" wire bonds are used to place the die into a standard package. After burn-in and test, the "soft" wire bonds are pulled away from the bond pads and the die is removed from package.
MCNC	Solder bumped die are attached to a reusable multilayer ceramic carrier using a sacrificial metallurgical connection. A special process is used to weaken the temporary bond and to allow removal of the die after burn-in & test.
nCHIP	Die-level technology for at-speed burn-in and test, employs a temporary package and temporary wire bonds. (This technology has been identified only recently and no assessment is available.)
Samsung	Conventional wirebond from chip to PC board is made in a multichip carrier. Gold wire is cut from bond pad with proprietary tool. (This technology has been identified only recently and no assessment is available.)

[3] The Reduced Radius Removal KGD technology was developed by IBM. See Section 6.0 for details.

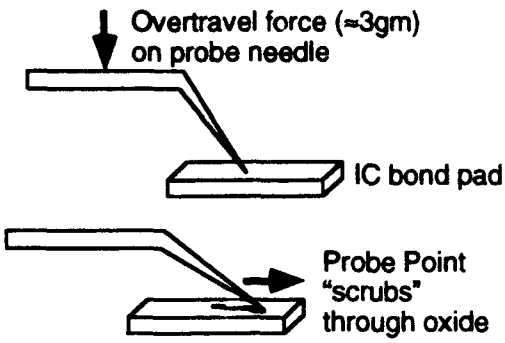

Figure 2. Overdriving the Probe

Figure 2: Overtravel force on probe needle causes horizontal motion that "scrubs" through native oxide on aluminum IC bond pad.

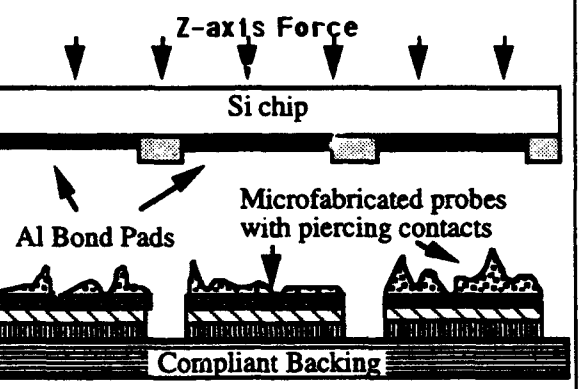

Figure 3. Piercing through the Oxide Layer

Figure 3: Microfabricated probe set makes reliable contact to the aluminum IC bond pad by piercing through the oxide layer on the surface of the pad.

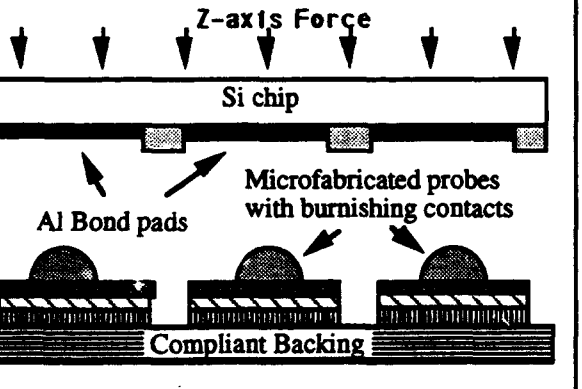

Figure 4. Deforming the Oxide Layer

Figure 4: Microfabricated probe set makes reliable contact to the aluminum IC bond pad by deforming the oxide layer on the surface of the pad.

2.2 Temporary Contact Approaches to KGD

Temporary contact approaches contain microprobe sets built into carriers that are made to mimic standard packages. The die is held in alignment to the probe set with force to insure reliable electrical contact to the IC bond pads. The main technical challenges with the probes/contacts are compliance to nonplanar pads on the die and penetration of the native aluminum oxide present on the IC pads without causing damage which could preclude the next assembly operation.

Pad Penetration — A temporary contact approach requires some form of "scrub" or penetration through the native oxide (typically on the order of 50 - 80 Angstroms) on the Al pad of the IC. Traditional needle and blade type probe cards achieve oxide penetration by forcing the tip of the probe to move laterally across the surface of the Al pad with a vertical force "overdriving" the probe. (See Figure 2.) This form of penetration, termed "scrub," may be used effectively for peripheral bond pads on an IC.

Many KGD approaches currently being developed require some form of z-axis penetration in which the microprobe is designed to be used with a piercing or burnishing vertical on-axis force. (See Figures 3 and 4.). This has been termed "z-axis scrub."

Compliance — Scrubbing actions on the bond pad require that some form of compliant member be available to equalize the force on each contact. For traditional epoxy ring needle probe cards, the spring constant of the needle provides compliance. For KGD carriers, especially those that rely on z-axis scrub to make reliable, low resistance contact, this problem is nontrivial. Since force is applied on-axis through the probe structure, the compliance must be built into the substrate on which the probe set is mounted — unless some form of compliant or deformable probe contact capable of z-axis scrub is available. This compliant substrate must be capable of providing two conflicting functions — the ability to transmit probe forces independently in the z-direction while maintaining x- and y-direction positional accuracy. In addition, the compliant members must be capable of maintaining these properties during burn-in temperature excursions which may reach 150°C. Many KGD carrier approaches use a form of membrane as the probe set substrate. Thin films, laminates, organic, and inorganic membranes have all been proposed as KGD carrier interconnect substrates. These membranes may be backed by an elastomer to provide the compliancy required for the probe set. Temporary contact KGD methods are summarized in Table 6.

Table 6. Temporary Contact Methods	
Company	**Description**
Acsist Assoc.	Contact to die is made with a micro particle interconnect.
Aehr Test Systems	Nitto Denko's ASMAT polyimide film provides electrical contact between the die and a uniquely designed carrier. Die are mechanically aligned.
California Contact	Electrical contact is made with traditional scrubbing action by microbeams, which are individually cantilevered. Die are placed directly into sockets on burn-in boards without the use of a carrier.
Fresh Quest	QC^2: A scrubbing probe technology on a thin film membrane is used to make contact between the die and the carrier. This technology is limited to peripheral bond pads.
IBM (dendrites)	Palladium dendritic structures are used to make contact to C4 solder bumped chips.
MCC	Reusable TAB tape with inner-leads bent upward and embedded in silicone elastomer provide normal force, compliance, and scrubbing under z-axis deflection. Usable with JEDEC standard TAB slide carriers and sockets for test and burn-in.
Micron Semi KDG^{plus}	A family of reusable, socketable, universal carriers is used to provide known good die. Specific information is limited.
Packard Hughes	Bumped flex carrier with "gold dot" microprobes is used with an elastomer backing, a spring clamp, and a support plate/heat spreader.
Plastronics	The carrier consists of a plastic base with a cavity for the die, a ceramic alignment plate with precision laser drilled holes for aligning wire probes to the die bond pads, and a contactor assembly which contains the probes. The compliant probes provide scrubbing contacts and the ability to accommodate non-planar surfaces.
Qualhi	Gold "bumps" are formed on thick film carriers by bonding gold ball bonds to the carrier; the wires are broken off and the remaining balls are coined (planarized). Die are placed in contact with the carriers using a flip chip bonder which provides enough scrubbing action to break through the oxide without forming an actual bond.
Sandia	Wafers are processed to reposition the normal peripheral bond pads of each die to an area array of much larger pads on top of the die to allow easy mechanical alignment to a pad array in a universal carrier. The die-to-carrier interface can be z-axis elastomers or diamond particle membranes.
TI/MMS	Pressure-contact carrier uses copper/polyimide interconnect and proprietary non-wiping contacts. Die self-aligns to carrier.
Tribotech	Either face-up or face-down versions of this carrier are available. A proprietary, non-scrubbing, fine point piercing method is used to contact the die and make contact to the thin film interconnect.
Yamaichi	Nitto Denko's ASMAT polyimide film material provides electrical contact between the die and a carrier.

2.3 Minimal package Approaches to KGD

These approaches take advantage of the fact that some minimal packaging approaches enhances the capability to do test and burn-in. Ruggedized packages, wider pitch, and gold contacts can help solve many of the problems with handling and contacting bare die. However, these approaches limit final assembly options.

Table 7. Minimal Package Methods

Company	Description
Chip Supply	Traditional TAB chip on tape is available.
Hughes Aircraft	Testable Ribbon Bonding (TRB): Die are ribbon bonded into low-cost carriers for burn-in and test. After test, the ribbons are cut leaving a TAB-like die which can be single-point bonded into its final application.
Micro SMT	Wafer level die packaging technology. Si posts are formed in wafer scribe lines.
Northern Telecom	Die are wire bonded into low-cost carriers for burn-in and test. After test, the wires are cut leaving a die with stub wires bonded to each pad, which can be single-point bonded into its final application.
Tessera	Flex circuitry is used to reroute center or peripheral die bond pads to an array of nickel/gold bumps. An elastomer layer provides compliance. The die array is temporarily attached to a PGA style carrier for burn-in and test and then removed. The die may then be flip chip array bonded into its final application.

2.4 Wafer-Level Burn-in

During the survey phase of the project, we identified suppliers working on wafer level KGD methods. We did not pursue these methods in this project.

Table 8. Wafer Level KGD Methods

Company	Description
Elm Technology	Micro machined silicon membrane with micro fabricated probe tips can be used for whole wafer probing.
Hughes Research	Extension of die-level membrane probe card can be used for whole wafer probing.
MMS	An extension of the die level carrier can be used as a whole wafer polyimide membrane probe card.
nCHIP	A probe card is formed from a silicon substrate with a multilevel interconnect. Compliant bump technology is used to mate the wafer under test to the substrate (under compression). Integral decoupling capacitance between the power planes and integral resistors for isolation of the chips are provided.

3.0 Infrastructure for KGD Program

In January of 1993, MCC launched the Infrastructure for KGD program under the auspices of an ARPA ASEM award, with Wright Laboratory acting as contract monitor. The objective of the program is to resolve the issues for supplying and procuring Known Good Die (KGD) in a way that fosters industry acceptance and confidence in Application Specific Electronic Modules for military systems. Work done on this program will extend into and help lay the foundation for acceptance of multichip modules (MCMs) for commercial systems as well. This report is the result of Phase I of the Consortia for KGD contract. Figure 5 is an outline of the tasks which were done during this Phase I program.

Prior to this Phase I work, an MCC/Sematech led task group had developed the *Standard for Procurement and Use of Known-Good Die* which was submitted to JEDEC in October of 1992 for adoption as a standard. See Figure 5. One of the tasks for the Phase One effort of the current work was to extend the proposed standard to include TAB and Flip-chip die.

Task Group Meetings

The program was officially begun with a meeting of the Bumped/TABed subcommittee of the KGD Task Group on 20 January 1993 at Sematech in Austin. The purpose of that meeting was to discuss modifications/ additions to the *Standard for Procurement and Use of Known-Good Die* required to facilitate Bumped/TABed Die sales. The participants in that meeting were IBM, Delco Electronics, Rockwell Intl., AT&T, and MCNC.

The subcommittee decided to draw upon the *Standard for Procurement and Use of Known-Good Die* to create a "core" document, followed by Wirebonded, Bumped and TABed Addenda.

The following day, January 21, the full KGD task group met at Sematech in Austin. Representatives of IC suppliers, MCM fabricators and assemblers, government and industry spokespersons met to begin a systematic attach on the KGD problem. These representatives agreed to form the task group which would guide the Phase I work.

The meeting on January 21, 1993 represented the first of six task group meetings; it began by identifying and quantifying a series of performance metrics which define known good die preparation processes.

The Task Group defined KGD Assurance Technologies as:

The processes, materials, equipment, information, etc., necessary to ensure performance, quality, and reliability of a bare or minimally packaged IC

a) meets the specifications of the Manufacturers Data Book for level of product required, OR

b) is as good as or better than an equivalent packaged device.

The Task Group then split into two subgroups to review the "strawman" document *Requirement Specification for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product.* This document is intended to be the tool which MCC will use for KGD technology assessment[1]. The Task Group was

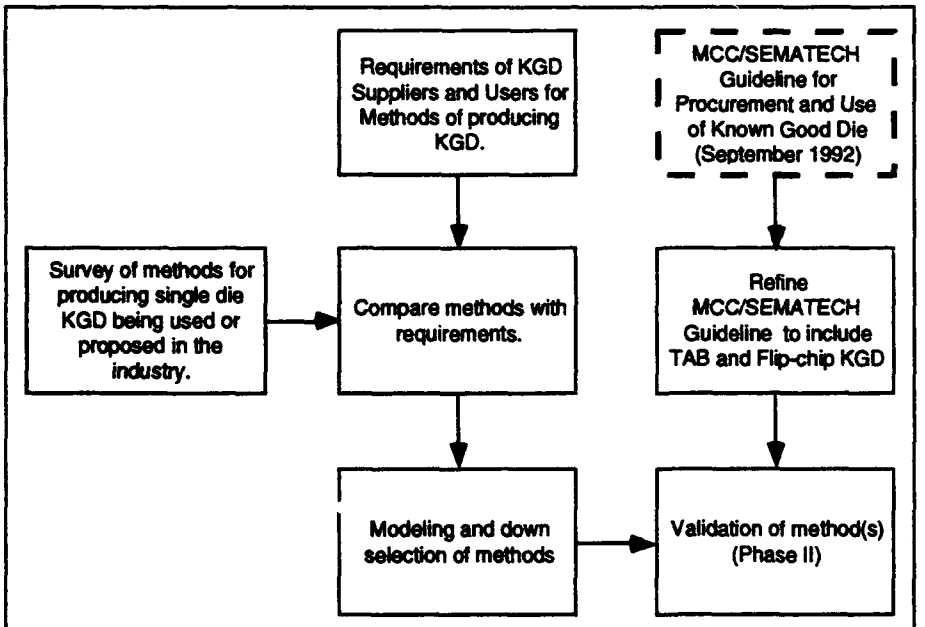

Figure 5. KGD Task Flow Chart

[1] This document was later renamed the *KGD Technology Assessment Guidelines for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product.* It is included in Section III of this report.

Table 9. KGD Meeting Summary				
KGD Meeting	**Group**	**Topic**	**Persons**	**Companies**
21-Jan-93	Task Group	Technology Assessment Guidelines	39	27
2-Mar-93	Task Group	TAB/Flip chip addenda	25	17
3-Mar-93	Task Group	Technology Assessment Guidelines	37	24
13-Apr-93	Task Group	Technology Assessment Guidelines	26	19
13-May-93	Industry	KGD Assurance Technologies	85	47
14-May-93	Task Group	Technology Assessment Guidelines, Phase II plans	33	20
29-Jul-93	Task Group	TAB/Flip-chip addenda, Technology Assessment Guidelines, Phase II plans	27	20
12-Oct-93	Industry	Review Technical Assessments, Phase II plans	51	33

split along the lines of die suppliers and die users. Each group worked on the document independently, and generated two separate documents based on the "strawman" original.

The second and third KGD Task Group meetings were held on March 2-3, 1993 at MCC in Austin, Texas .

The purpose of the meeting held at MCC on 2 March 1993 was to review the subcommittee recommendations for TAB and Flip-chip extensions to the MCC/Sematech *Guideline for Procurement and Use of Known-Good Die.* The meeting was attended by 20 persons representing 11 companies.

The task group approved a decision to develop three separate KGD specifications, one for TAB devices, and one for flip-chip devices in addition with the current wirebond document.

The meeting held at MCC on 3 March 1993 was to continue developing the *KGD Assurance Technology Requirements Guidelines* which had been initiated at the 21 January meeting (at Sematech) and further refined by subgroups during the month of February. The meeting was attended by 39 persons representing 21 companies.

The supplier and user versions of the documents were merged prior to the meeting and the task group spent most of the day going through the document line by line identifying areas of agreement. The resulting merged document was renamed *Technology Assessment Guideline for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product.*, version 1.5.

The KGD Task Group next met on 13 April, 1993 at the Radisson Hotel in Denver, Colorado, to continue the identification and quantification of a series of performance metrics which define known good die preparation processes. The goal of the meeting was to review the *Technology Assessment Guideline for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product* or simply *Technology Assessment Guidelines* and get to Revision 2.0. which could be called a discussion draft, and which is nearing consensus.

The main sections to be resolved at this meeting included the Die Preparation, Assembly and Disassembly section, the Test and Burn-in section and the Wafer Mount and Saw section.

A decision was made to include as Appendices, sections which ask the Technology Suppliers to provide information about their technologies. This was seen as an aid to MCC (and potential customers) in assessing the technology. These sections include the Die Preparation, Assembly and Disassembly section and the Wafer Mount and Saw section.

The Test and Burn-in section was extensively reviewed, and a decision was made to simplify the sections by reducing the categories to only two categories, low I/O (<100) and high I/O (>100) devices.

The Task Group agreed that the *Technology Assessment Guidelines* had indeed reached Revision 2.0 and could be used to begin the assessment phase of the project.

The task group also discussed the May KGD Technology Supplier Forum and asked that presenters at the forum to address the following questions:

1) What is your suggested manufacturing process flow to produce KGD?
2) What is the availability of your technology?
3) What is the cost per unit? (carrier/probe card cost)
4) How many reuses do you project for the carrier?
5) What is the lifetime and what is the time to refurbish?
6) What is the cleaning process?

The first industry-wide meeting of the program was held on 13 May, 1993 in Austin. Representatives from industry were invited to a KGD Technology Supplier Forum, where 14 companies made presentations about their bare die test, burn-in, shipping and inspection technologies.

The Forum objective was to promote a dialog between suppliers and users of the materials, components, and tools necessary for producing high quality, reliable, bare or minimally packaged integrated circuits (KGD). The forum agenda allowed the 14 KGD technology supplier attendees to make a presentation of 25 minutes and to participate in a panel discussion concerning the technology available for preparing, inspecting or shipping KGD. Each presenter was provided a copy of Revision 2.0 of *Technology Assessment Guideline for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product* prior to the meeting. This ensured that all presentations were focused on the technical issues involved with preparing KGD.

On 14 May, 1993, the KGD task group met at MCC to review the supplier forum, add shipping guidelines to the Technology *Assessment Guideline for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product* and review the plans for Phase II of the program. The requirements for shipping KGD were added and the *Technology Assessment Guidelines* were upgraded to revision 2.5.

On 29 July, 1993 MCC held the sixth task group meeting at the DFW Airport Marriott in Dallas, Texas. The purpose of the meeting was to review progress on all deliverables for phase I of the project.

TAB and Flip-Chip Addenda to the Procurement Specification

The *Standard for Procurement and Use of Known-Good Die* which was developed by the task group and submitted to JEDEC for standardization was edited by JEDEC 13 Task Group JC-13-92-04 as result of JEDEC Survey Ballot JC-13-92-191. The latest version of the *Standard for Flip-Chip Known Good Die* was edited to match language of JEDEC Ballot version. This Flip-Chip version, Working Version 1.0, 22 July, 1993, was reviewed and the updated version will serve as the addenda to the JEDEC standard. It was submitted to the JC-13 committee in August 1993.

The task group recommended turning over to the JC-13 subcommittee on TAB, the *Standard for Providing/ Using Known-Good Die, Addendum for Tape Automated Bonded Die*, Draft 2.0, 9 Apr 93. This was also done in August 1993.

Technology Assessment Guideline

Rev 2.5 of the *Technology Assessment Guidelines* as updated by the task group subcommittee after May 14 update was reviewed; this latest rev 2.9 was presented to the task group at the meeting.

A number of new assessment criteria were suggested by the task group, including shock and/or vibration and time at burn-in temperature. The task group also suggested that definitions of test methods and specifying the conditions for evaluating the technologies are needed. These latest updates, including test methods for all test rules, are included as revision 3.0 in Section III of this report.

Phase II Plan

The phase II plan includes a two-level strategy to evaluate the capability of selected KGD methods to meet the *KGD Technology Assessment Guideline* and to produce known good die. The details of the phase II plan are contained in Section II of this report.

A second industry meeting was held at MCC in Austin on October 12, 1993 to present the results of the KGD technical assessment. A preliminary draft of the phase I report was available for review and discussion. Some of the comments from that meeting have led to the improved detail of the readiness categorization.

4.0 Assessment/Scoring Methodology

Sub section 6.0 of this section of the report contains the descriptions of the 24 KGD approaches we assessed. The following paragraphs outline the methodology and content of the descriptions. The information contained in the assessments has been obtained from published papers and from interviews with individuals representing the supplier company. Each of these descriptions has been prepared by MCC personnel, and has been verified for correctness and nonproprietary content by individuals at each of the supplier's facilities.

General Information

Background information on the technology development and the vendor is given. A very brief description of the approach is provided, along with the type of contact mechanism employed, the alignment method used, and the provisions for thermal management. Finally, a brief synopsis of the vendor readiness to provide this technology is provided. This section is intended to provide a brief summary of the technology available for readers in a hurry, without interest in the details of the technology.

Technical Description

This section is a textual description of the KGD assurance technology, including the process methods required to use it. This description also contains a drawing or photograph intended to illustrate the technology described wherever possible. This description has been prepared by MCC personnel, and is intended to be nonproprietary.

Readiness Level

Most of the KGD technologies we assessed are in the development stage, and are changing. In order to accurately portray the state of readiness of each technology, we have provided information in five areas; a readiness category, the equipment status, process status, capacity issues, and qualification issues, are described in detail.

Readiness Category

We have established four categories for readiness, as follows:

Conceptual: These are ideas in the formative stages, with no prototypes or test data available.

In Development: These KGD methods are currently being developed by a supplier, and prototypes are being built and assembled at the supplier's site.

Alpha Test: These KGD methods have had prototypes developed and initial production units are currently being tested and evaluated for use in providing KGD at a user site.

In Production: These methods are being used to deliver KGD or KGD assurance technology devices to customers. The KGD technology must be fully developed and qualified for use to achieve this category.

Equipment status

MCC personnel have attempted to describe the equipment required for end user processing of KGD using the given technology. This usually involves assembly of die into carriers and subsequent disassembly. Where possible, we have also described the equipment required by the supplier to produce the KGD assurance technology devices. This section describes the availability of that equipment.

Process status

Some of the KGD technologies presented involve processing steps at the wafer level. Where appropriate, this section discusses the developmental stage of these processes. This section also addresses the die to carrier assembly/disassembly process status.

Capacity issues

The KGD production capability is discussed in this section. Limitations in production capacity are indicated here.

Qualification issues

This section discusses the work performed by the supplier to date to test and qualify the KGD technology for general production of KGD.

Alignment Method

The alignment method pertains mainly to probe set approaches. Mechanical alignment is a method of placing the die in the carrier by referencing the edges of the die, which implies they are always within some specified tolerance. The concern here is with the tolerance of typical IC manufacturers' sawing process[1]. Manual optical alignment refers to the use of an optical method of aligning the die bond pads with the carrier contacts involving an operator to make the necessary adjustments, typically by observing the movements through a microscope. Automatic optical alignment refers to the use of an optical method of aligning the die bond pads with the carrier contacts involving a computer based vision system and robotic actuators to position the die in reference to the carrier.

Contact Mechanism

There are several approaches to contacting the die bond pads presented by the KGD technology suppliers in this report, some of which are considered proprietary. Wherever permitted, we have indicated whether the contact is made with a scrubbing (x, y action) or a piercing or burnishing (z-only) action.

Key Features

This contains a list of the key features of the technology, compiled by MCC personnel from information provided by the suppliers. In many cases, features indicated by the supplier were considered to be TAG requirements, and are not listed here specifically.

Noncompliance with Technology Assessment Guidelines

This section contains a list of exceptions to the Technology Assessment Guidelines. The full TAG worksheet for each approach is included with each description.

Process Flow Description

MCC personnel used available supplier information to describe the likely process flow for each known good die technology. This is primarily the procedure for assembling and dissassembling the die in the KGD assurance technology devices.

Advantages

A list of advantages of the particular technology is given. Features which meet the TAG requirements are not listed as an advantage. If the majority of the suppliers are expected to have this advantage, it is also not listed. This list is compiled by MCC personnel.

Disadvantages

A list of disadvantages of the particular technology is given. Features which do not meet TAG requirements are discussed in Noncompliance with Technology Assessment Guidelines. This list is compiled by MCC personnel.

Concerns

This section contains the concerns raised by MCC personnel and others with regard to a particular technology. These items typically include missing pieces of important information, trade offs, and potential rather than actual problems with the technology.

Equipment Required

Each technology is dependent on some equipment for processing. In some cases, this is standard equipment, such as wire bonders and package handling equipment, and in other cases, custom designed equipment is required. MCC has attempted to provide as much information as is possible about the equipment required; however, details are often unknown or as yet undefined. An example table is given:

Item	Cost	Throughput
Assembler	$100K to $200K	20 die/hr

Equipment Description for Automated Process

A description of the process equipment required in order to have a fully automated assembly/disassembly of chip-to-carrier is given. Information from suppliers is limited; therefore, these are largely derived from engineering knowledge by MCC personnel.

[1] See Section II, Appendix B for a discussion of wafer saw requirements for mechanical alignment.

Table 10: Example of TAG Worksheet				
TAG Requirements	**Guideline**	**Meets TAG?**	**Weight**	**Score**
Interconnect Rules				
Planarity: Pad to pad height variation	up to 1.0μm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal				7

Cost

The following table illustrates the method of cost comparison, with the criteria used to rate costs as low ($), medium ($$) or high ($$$) for selected technologies.

Table 11: Cost Comparison Chart		
Factor	**Comment**	**Cost**
Wafer Processing	No additional processing Bumping required Rerouting required	$ $$ $$$
Materials cost per use	Parity w/plastic pkg possible Parity w/ceramic pkg possible Parity w/any pkg unlikely	$ $$ $$$
Assembly and Disassembly	Simple approach, low cycle time Higher cycle time than average Very high cycle time and/or potential for damage to carrier or die	$ $$ $$$

Cost information given by the supplier may also be listed.

Comments

This section contains general comments from MCC personnel pertaining to the technology and/or its application.

Supplier Business Information

The supplier company name, address, phone, primary business, number of employees, and 1992 sales or revenue are given if available.

Contact(s)

The name, address if different from above, and telephone/fax numbers are given for the individual(s) primarily responsible for the KGD technology within the supplier company.

4.1 Drawing or Photo

Where possible, a drawing and/or photo of the technology is included. These diagrams are often contained within the technical description or process flow sections, wherever appropriate.

4.2 Technology Assessment Guidelines Worksheet

The two-page TAG worksheet contains the "rules" from the KGD Technology Assessment Guidelines (Rev. 2.5) in the form of a spreadsheet. The TAG Requirements column gives the "rule;" the Guideline column lists the tolerance or limits; the third column indicates whether or not the technology meets the guideline; the weight column contains the weight or priority of that feature on a scale of 1 to 3; the last column gives the score. The score equals the value of the weight in cases where the TAG is met or zero in cases where it is not met.

Table 10 shows an example of the worksheet. This is for section 3.5, Die Interconnect Quality of the KGD Technology Assessment Guidelines. Each subsection is summed and added to make the final TAG score. The line items in this worksheet and the "weight" of each was defined by the KGD technology subcommittee, comprised of representatives from throughout the electronics industry. MCC personnel have assessed each technology by line item, to determine if the technology meets each requirement.

It should be noted that the technologies were assessed against Rev. 2.5 of the TAG, while the version given in Section III is Rev. 3.0. In order to complete the assessment during the time that revisions continued to be made to the TAG. It was necessary to fix the version at an earlier date.

5.0 Cost Analysis

5.1 Introduction

The cost analysis efforts presented in this report address general Known Good Die (KGD) cost issues rather than specific carrier+interconnect technology approaches. Based on industry interest, the focus is on temporary contact methodologies; however, the results are generally applicable to soft contact technologies as well. The analyses were performed using a Monte Carlo simulation in an MCC developed cost model. This method provides an effective means of handling a large number of variable, complex interactions and a high level of uncertainty with respect to specific values. The results are expressed as the cost ratio (KGD/Pkg) between bare die (KGD) and conventionally packaged die (Pkg).

5.2 Methodology

The cost model simultaneously follows a typical process flow for KGD and its equivalent packaged part. It is significant to note that the model encompasses the entire process from completed wafer fabrication to die ship, rather than focusing on assembly only (Table 12).

The cost analyses presented in this report make the following assumptions:

- Total number of die fabricated is 500,000.
- Equipment, methodologies, and times for test and burn-in are identical for conventional packaging and KGD.
- Wafer fabrication costs are identical for conventional packaging and KGD (since use of temporary contact methodologies are expected to require no additional wafer processing).
- Uniform, domestic labor rates are used, except for conventional package assembly.
- Conventional package assembly costs are derived from Messner [1].

The complexity of the model requires a case study approach (with key KGD independent variables fixed). The baseline case is a moderately sized die (0.42 cm^2) with a medium number of I/O (74). The product life is assumed to be 2 years and burn-in time is set at 24 hours. These two counteractive effects represent a rough compromise between typical commercial and military applications.

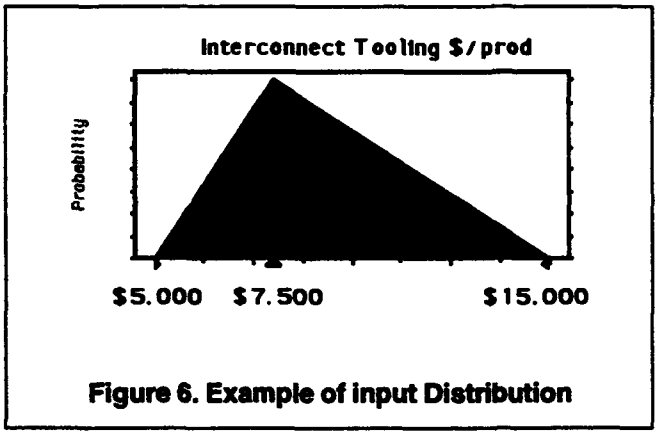

Figure 6. Example of input Distribution

A number of factors influence the cost of KGD relative to conventionally packaged parts. Most factors can be identified as either dependent or independent of the specific KGD technology used. The value for each factor is derived from one or more inputs, with the model containing over 100 inputs. Slightly less than half are fixed at one value; the others are defined by ranges and distributions. The variable inputs are primarily related to KGD dependent factors and are listed and explained in Appendix 1. An example input is given in Figure 6 above, where the range for interconnect tooling is set at $5000 to $15,000, with the most likely value being $8,000. This input

Step	Process Step	Applies to:	Key Inputs
1	Wafer fabrication and sort	KGD & Pkg	Die area, # of I/O, defectivity
2A	Assembly into a carrier	KGD	See Appendix 1
2B	Assembly into a conventional package	Pkg	# of I/O, Messner's formulas [1]
3	Burn-in	KGD & Pkg	Burn-in time, BIB costs, and operation parameters
4	Final test	KGD & Pkg	Cost per die
5	Disassembly	KGD	See Appendix 1

Table 12. Process Flow and Key Inputs for KGD and Pkg

is one of the many used to calculate the factor "cost of carrier+interconnect."

Each Monte Carlo simulation includes a total of 1000 runs. This captures the potential variability in the input ranges and accounts for the uncertainty in assigning specific values. Each of the 1000 runs uses randomly selected values from the defined input distributions. The output of a simulation is a population of possible results, which are analyzed and expressed as a mean and standard deviation. The graphs below depict a minimum of 10,000 runs, with the individual data points representing the mean of the population. When present, the error bars represent 1 sigma limits.

5.3 Results

Known Good Die costs are influenced by both KGD technology dependent and independent variables (Table 13). In addition, relative cost is affected by changes in the cost of either KGD or Pkg. One of the key influences on package cost and therefore, the KGD/Pkg ratio, is the package type to which it is being compared. The relative cost of KGD increases by up to a factor of 2 if it is compared to plastic rather than ceramic parts (Figure 7). Many die suppliers are targeting parity with plastic parts; however, in some cases parity with ceramic is adequate to justify investment in KGD.

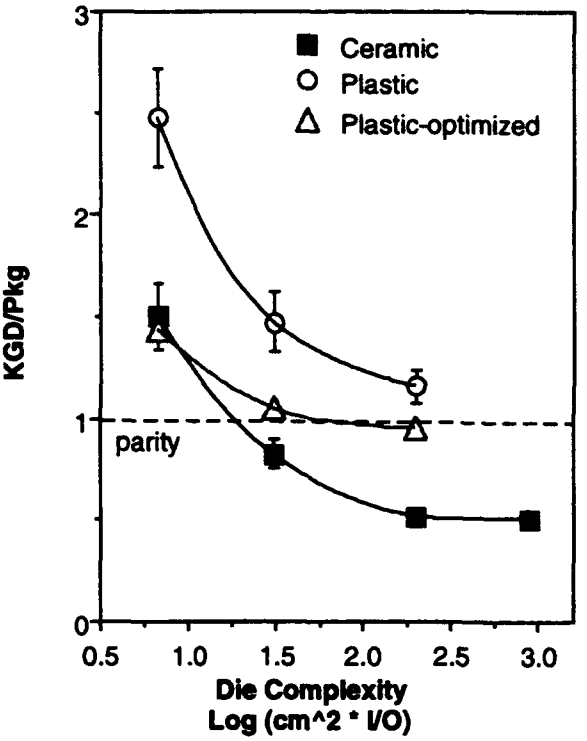

Figure 7. Die Complexity and Package Type vs KGD/Pkg

Die complexity has a significant effect on the relative cost of KGD, because of increased cost of conventional package costs. The model assumes a much greater penalty for high pin counts in conventional packaging

Technology Dependent or Independent Factor	Desired Trend	Comments	Full Range	Relative Effect, full range	Relative Effect if >100 uses
Die Complexity log (cm^2 per die * I/O per die)	More complex is better	Conventional package has higher per-pin costs than KGD.	0.8 to 3.0	High	Very high
Number of Uses per Carrier+Interconnect (C+I Life)	More uses is better	Number of C+I uses is the most critical factor when this number is small (<100)	5 - 280 uses	Very high	Medium
Product Life (Effective life-time of interconnect design)	Longer is better	Cost of C+I is amortized over a greater number of uses	0.5 to 2.5 yrs	Medium	High
Cost of Carrier+Interconnect (C+I)	Lower cost is better	Reduced material cost	$12 to $260	Medium	Medium
Burn-in Hours per Cycle	Less time is better	Number of uses per C+I is higher for a given thermal life	6 to 48 hrs	Medium	Medium
Cycle time per die (Assem+ Disassemb + Clean)	Lower time is better	Reduced demand on labor and equipment	17 to 170 sec	Low	Medium
Equip (Assembly+Disassembly Equipment Costs)	Lower cost is better	Reduced capitalization cost	$0.03 to $0.46 per die	Very low	Low

Table 13. Influence of Technology Factors on KGD/Pkg for a given packaging type

than for KGD temporary contact carriers. This is because in conventional packaging, costs increase significantly with pin count. The KGD carrier has a small penalty for pin count in order to account for increased complexity of the interconnect, but assembly costs change very little (if any) as the number of I/O is increased. An increase in die size with the same pin count has very little effect on the cost ratio. As die size increases, yield decreases for a given defect density [2] resulting in increased scrap rates of conventional packages. However, this benefit to the KGD/Pkg ratio is offset by the loss of an amortized use of the KGD carrier+interconnect (since it has been used to burn-in a die that cannot be sold).

Product life and burn-in time are both KGD technology independent factors which have a very significant effect on the cost of KGD. In some instances their effect can have a greater influence on the cost of KGD than the factors which are directly related to the selection of a specific KGD approach (Table 13). Both product life and burn-in time affect the maximum number of potential uses for a given carrier+interconnect, consequently increasing amortization effects (Figure 8). Over the ranges selected in this analysis, product life has a slightly more significant effect than burn-in time. An increase in product life increases the potential number of uses before the interconnect is made obsolete by design changes. A decrease in burn-in time will also increase the potential number of uses because it provides more uses for a given interconnect thermal life (i.e., it decreases thermal exposure per use).

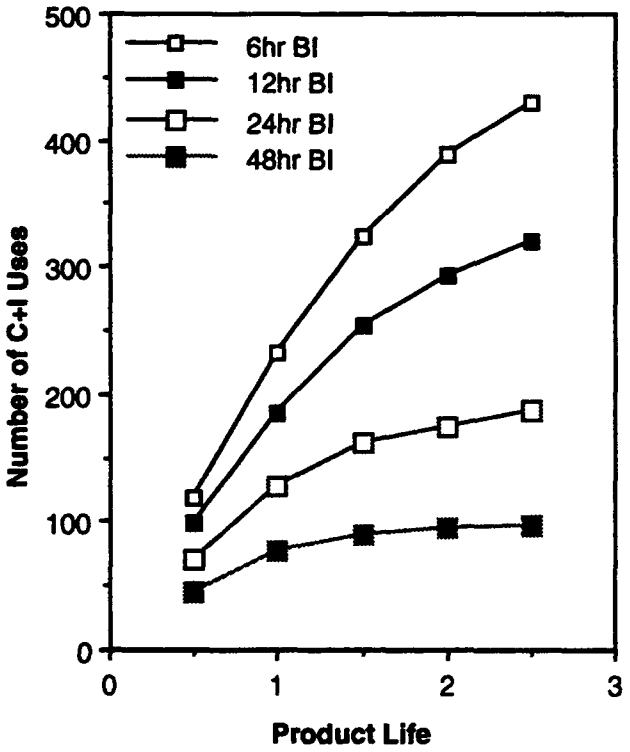

Figure 8. Product life and Burn-In Time vs Number of Carrier+Interconnect (C+I) Uses

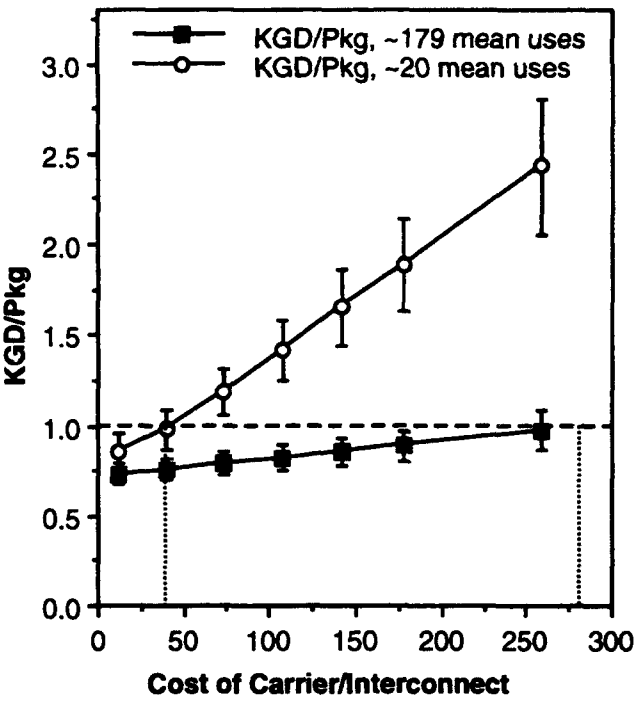

Figure 9. Cost of Carrier+Interconnect (C+I) and Number of Uses vs KGD/Pkg

The two most important KGD technology factors which affect cost are the cost of the carrier+interconnect (C+I) and the number of times that it can be used. If the number of uses is low (<100), it is by far the most important cost driver. Figure 9 illustrates the importance of determining both factors in selecting a cost effective KGD technology. The maximum possible number of uses for any carrier+interconnect is limited by product life and is unlikely to be more than 1000. The actual number of uses, however, is more likely to be determined by the thermal/mechanical life of the interconnect and/or probe tips. Based on analysis completed to date, it is believed that 100 uses is a desirable minimum number. Determination of carrier+interconnect life for specific KGD approaches will be critical for accurately determining costs of those particular technologies. Fortunately, thermal life and temperature cycling tests are relatively easy to perform in-house.

Cycle time for assembly and disassembly of the die into the carrier has a moderate to low effect on KGD costs. Longer cycle time adds to cost by decreasing throughput and potentially increasing the amount of labor required. The cost of equipment has a very low effect on KGD cost (a third less than cycle time). Cycle times and equipment costs will probably be fairly difficult to determine until the processes mature. Most of the suppliers do not yet have production lines in place, many have not yet identified key pieces of equipment or levels of automation, and some have not made a final decision on the exact process flow. Fortunately both cycle time and equipment costs have relatively low effects.

5.4 Conclusions

Cost effectiveness of KGD will ultimately depend on the point of reference. Parity with ceramic parts will be easier to achieve than with plastic. In addition, the nature of the product itself will have a larger impact on the relative cost than will most KGD technology dependent factors. Ideally the die have a high pin count, a low burn-in time, and a long product life. A die with a large number of I/O will be more cost effective than a less complex die because of the cost savings over conventional package costs. A design which is expected to have a relatively long product life will also provide greater economic benefits by increasing the potential number of uses per carrier+interconnect and the amortization of the carrier+interconnect design. A reduction in burn-in time will increase the number of uses per C+I (assuming a limited thermal life).

The two most critical KGD technology dependent factors are the cost of the carrier+interconnect and the number of uses per C+I. The number of uses is especially critical when the number of uses is low (<100). These two factors are probably best expressed in combination as a ratio of C+I cost to number of uses per C+I. Analysis to date indicates that the desired minimum number of uses is about 100. This is expected to be controlled by the thermal/mechanical life of the carrier+interconnect. The benefit of improving carrier+interconnect life diminishes rapidly after several 100 uses due to the use limits imposed by product life. For this reason, it is unlikely that any carrier+interconnect will be used more than 1000 times.

5.5 Appendix

See Appendix 1 at the end of Section I.

References:

[1] G. Messner, Price/Density Tradeoffs of Multichip Modules,: Proceedings of the International Symposium on Hybrid Microelectronics (ISHM), pp. 28-36, Seattle, WA, October 1988.

[2] B.T. Murphy, "Cost-Size Optima of Monolithic Integrated Circuits," Proc IEEE, vol. 52, pp. 1527 - 1545, (1964).

6.0 Technical Assessments of Selected Approaches

Soft Connection Approaches to KGD

Chip Supply

Elmo Semiconductor

General Electric

IBM

Micron Semiconductior

MCNC

CHIP SUPPLY, INC.
SofTAB/Softool

General Information

Chip Supply began supplying known good die by providing hard-bonded TAB components, and supplanted their capability by licensing the "Softool" technology from Micron Semiconductor (see Micron Softool). Chip Supply has since developed a known good die technology of their own, called "SofTAB." This new technology is based on using TAB leadframes and processing equipment, and performing a "soft" inner lead bond to gold bumped die, which is removable after test and burn-in. See Figure 10. Contact methodology is a soft bond with alignment performed by a TAB inner lead bonder. Thermal management is not provided, although the die backside is left accessible for contact in the TAB slide carrier. All three of these methods are in production now. The following will focus on SofTAB. A discussion of Softool is included under Micron.

Technical Description

Chip Supply's "second generation" approach to supplying known good die is based on a mature in-house TAB capability. Wafers are gold bumped in the same manner as for TAB. Thickness of the bumps can be varied to accommodate different final assemblies including HDI. The TAB tape frame is fabricated, and lightly attached to the gold bumped, peripheral bond pads of the die. After burn-in and test using TAB sockets, the tape frame is removed with a modified pull tester, and the die is visually inspected. Finished KGD are delivered in waffle packs. The finished die have gold plated bumped bond pads which are sealed to the glassivation for enhanced reliability. These bond pads readily accept gold wire bonds, and in bondability tests performed by customers, the gold to gold attach using both wedge and ball techniques has yielded 100 percent wire breaks.

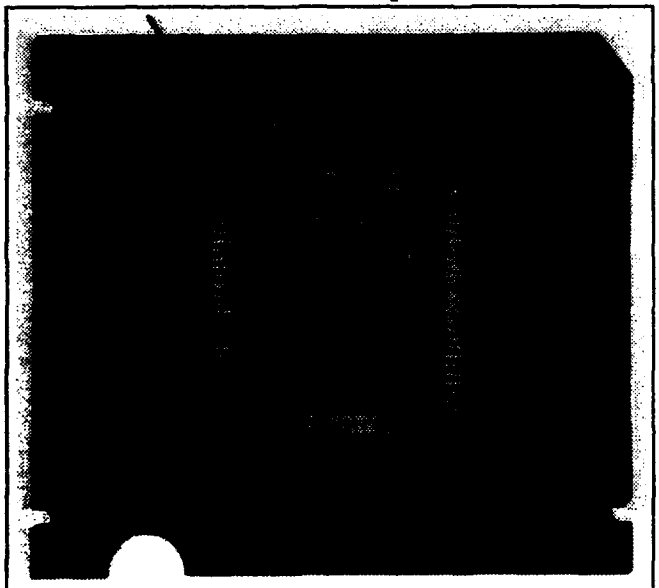

Figure 10. Soft Bonded TAB Carrier

Readiness Level

Readiness Category:

This technology is currently in production.

Equipment status:

All necessary equipment is currently in place and ready for use.

Process status:

The process for SofTAB is completely developed and has been independently verified.

Capacity issues

The SofTAB approach is capable of handling high I/O, fine pitch, and high volume requirements. Tooling is required for each new TAB tape design. Gang bonding and removal of tape is possible.

Qualification issues:

This method is currently in production and is being used to ship known good die. The quality of the bond pads on shipped die has been verified by customers. Since an actual bond is made, quality of burn-in and test is expected to be equivalent to traditional TAB.

Alignment Method

Alignment is done by visual set up of an inner lead bonder and is automatic thereafter.

Contact Mechanism

Contact to die is made with temporary TAB bonds.

Key Features

SofTAB is based on mature TAB technology.

Noncompliance with Technology Assessment Guidelines

The TAB based technology is limited to use with die which have peripheral, gold-bumped bond pads.

- TAB approach means that die with area array pads cannot be burned-in or tested
- Process not designed to convert from array to peripheral bond pads.
- SofTAB process not defined for use with Al pads.
- Additional wafer processing required (Au-bumping).
- Cannot accommodate incoming solder bumped die: SofTAB process not defined for use with solder bumps; Au-bump processing requires aluminum pads as initial surface.

It is assumed that the TAB tape will be single level and therefore unable to achieve 50 ohm controlled impedance.

SofTAB was not penalized for degradation to bond pads since the contacts are gold-to-gold. Lack of damage is supported by EDS analysis and pull-strength tests.

Process Flow Description

1.0 Begin with gold bumped die.
2.0 Soft ILB TAB tape leads to die bumps.
3.0 Test at room temperature.
4.0 Burn-in (160 hrs @ 125°C or 80 hrs @ 150°C).
5.0 Test at specified temperatures (-55°C to 125°C available).
6.0 Remove TAB contacts from die using modified pull test equipment.
7.0 Inspect.
8.0 Transfer die to shipping containers.

Advantages

- Uses existing TAB assembly.
- Demonstrated technology, currently in use.
- Wide assembly window; 10% process variation will retain good pull strength and still remove easily with shear because of flat interface.
- Uses existing TAB tape slide carriers.

Disadvantages

- Cooling required for high power dynamic burn-in may be a challenge.
- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- Selection of this technology means that wafers must be gold plated or bumped. Plating/bump process adds environmental protection to die in the form of gold sealed to glassivation. However, it may also introduce defects and limit final assembly options. If preferred final assembly requires gold pad then the cost of wafer bumping is value added.

Equipment Required

Item	Cost	Throughput
TAB inner lead bonder	$125K	1 bond/sec
Modified pull tester	Unknown	Unknown

Equipment Description for Automated Process

Wafer processing equipment is required for bumping the wafers. Normal TAB equipment is used to produce the SofTAB product. Chip Supply uses a Hughes TAB inner lead bonder to form TAB bonds on die pads, and a customized pull tester to remove bonds from the die.

Cost

SofTAB requires a nonrecurring engineering charge (NRE) of approximately $16,000 for tooling new products, plus an NRE charge for test software (dependent on complexity of test). There is no NRE charge for part types that Chip Supply has previously tooled.

Cost Factor	Comment	Cost
Wafer Processing	Au bumps	$$
Materials Cost/Use	Low materials cost (in volume); low number of uses	$$
Assembly, Disassembly	Cycle time higher than average	$$
MCC Cost Judgement		

Comments

SofTAB KGD technology provides the benefits of mature TAB technology using a process currently available. This approach meets the requirements of wire bonded applications, even though the aluminum bond pads have been physically changed. Using this approach means a customer is paying for TAB tested and burned-in die, but getting bare die with gold pads.

Supplier Business Information

- Chip Supply, Inc.
  7725 N. Orange Blossom Trail
  Orlando, FL 32810
  (407) 298-7100

- Primary Business: Electrical measurements, instruments
- Total Employees: 175
- 1992 Sales: $18M

Contact

Jim Rates
PHONE: (407) 296-5604
FAX: (407) 290-0164

Supplier:	CHIP SUPPLY	Method:	SofTAB	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	29
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	7
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	N	3	0
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	CHIP SUPPLY	Method:	SofTAB	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	21
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	21
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	22
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	153

ELMO SEMICONDUCTOR

General Information

Elmo Semiconductor uses their own process for overcoating die, forming enlarged bond pads, and placing temporary bonds on the die for burn-in and test. The die is placed into a temporary package using a thermoplastic die attach, and wire bonded into the package for burn-in and test. See figure 11. Afterward, the wire bonds are "clipped" off and the die is removed from the temporary package. The contact mechanism is a wire bond, and the alignment is performed by a wire bonder. Thermal management is provided by the temporary package, normally the package the part is usually provided in. Elmo is currently producing known good die using this methodology.

Technical Description

The Elmo approach is based on existing technology and capabilities. Wafers are coated with a dielectric material, either organic or inorganic, followed by a step to open up the original bond pads. New bond pads are then formed over the dielectric coat. These new pads are larger and may have a less aggressive pitch than the original die. The die is placed in a temporary, reusable carrier with thermoplastic die attach and then wire bonded. After burn-in and test, the wire bonds are cut and the die are removed on carriers. For assembly into the final application, new wire bonds are made adjacent to the KGD bond sites, which is facilitated by the larger bonding area.

Readiness Level

Readiness Category:

This technology is currently in production.

Equipment status:

The Elmo process is based on existing standard equipment for wafer processing and die attach/wire bonding operations. All of this equipment is in place and ready for use at Elmo.

Process status:

The wafer processes and the die attach/wire bonding operations involved are fully developed and qualified for use.

Capacity issues:

Elmo capacity for production is currently from 1000 to 2000 die per week (depending on the number of die per wafer), and all processes involved except the wire clip and die removal are fully automated. Capacity is limited by available personnel, not equipment. The capacity may be quickly expanded by adding personnel.

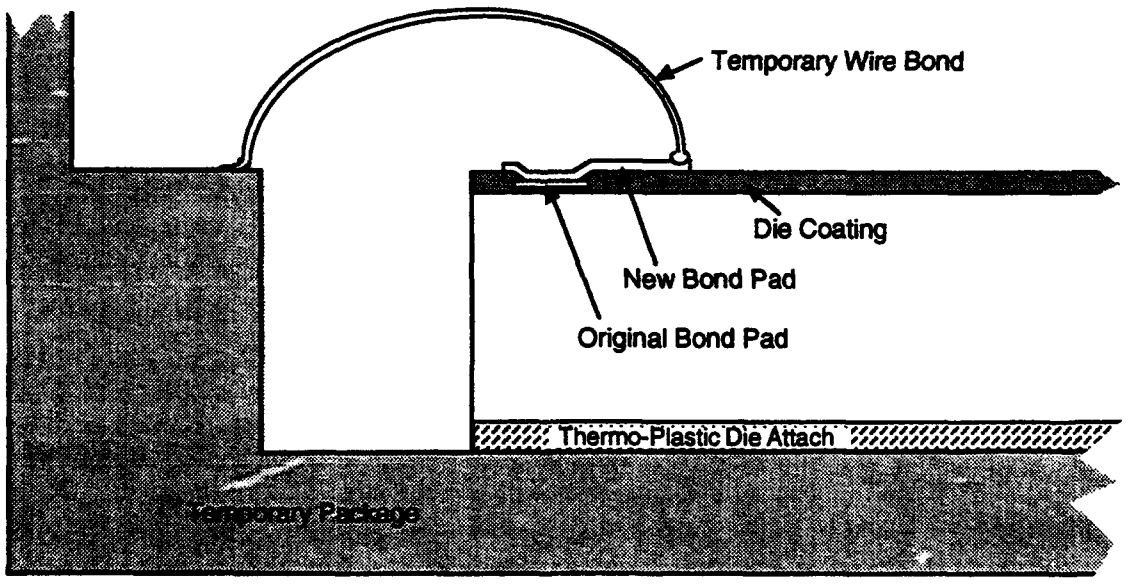

Figure 11. Die Installed in Temporary Package

Qualification issues:

The overcoat material(s) are commonly used passivation materials, and have been qualified for use at Elmo. The effects of the overcoat of bonding over active circuits are unknown at this time and need to be qualified.

Alignment Method

Alignment is manual optical and is performed on the wire bonder.

Contact Mechanism

Contact to die is made with temporary wire bonds on expanded die contact pads.

Key Features

Enlargement of die contact pads provides enough space for both temporary and final wire bonds.

Noncompliance with Technology Assessment Guidelines

The wire bond based technology, with required rerouting of original aluminum bond pads, is limited to use with die which have peripheral, aluminum bond pads.

- Wire bond approach means that die with area array pads cannot be burned-in or tested.
- Process not designed to convert from array to peripheral bond pads.
- Cannot accommodate incoming Au or solder bumped die; postpassivation processing, integral to technology, requires aluminum pads as initial surface.
- Additional wafer processing required (rerouting and enlargement of bond pads).

The dielectric overcoat was judged to be potentially incompatible with GaAs.

Clipped ball bond left after testing was judged to be a degradation in the quality of the final bond pad surface.

Wire bonding in combination with pad rerouting provides an uncontrolled impedance environment.

Optical inspection of the die is inhibited by the dielectric coat.

The Elmo process was not penalized for number of touchdowns, since enlarged pads will accommodate multiple bonds.

Process Flow Description

1.0 Begin with die which have added dielectric and rerouted pads, per Elmo's postpassivation process.

2.0 Inspect.

3.0 Mount die in carrier with thermoplastic

4.0 Wire bond.

5.0 Test.

6.0 Burn-in die.

7.0 Re-test.

8.0 Clip wire bonds.

9.0 Remove die from carrier.

10.0 Remove thermoplastic material from backside of die.

11.0 Transfer die to delivery packaging.

Advantages

- Uses existing wire bond assembly equipment.
- Enlarged bond pads allow for multiple bonding without violating pad damage ratios.
- Standard existing package may be used. No change in burn-in and test equipment, sockets or parameters is required.
- Demonstrated technology, currently in use.

Disadvantages

- Cost increases with pin count since both assembly and disassembly are done one pin at a time.
- Economic reuse of package is limited.
- See also Noncompliance with Technology Assessment Guidelines

Concerns

- "Clipped" bond balls may affect final assembly.
- Removal of die attach material may not be easy and/or may affect quality and ease of final assembly.
- Postpassivation wafer processing provides additional environmental protection for die and, if done

at a single location, may result in uniform metallization and therefore, uniform bonding parameters. However, wafer processing may also introduce defects. Overall, cost is high relative to value added.

- Potential for damage to die because bonding over active circuitry.
- Potential TCE mismatch between passivation and coating may result in metal movement.
- I/O limited.

Cost Factor	Comment	Cost
Wafer Processing	Reroute required	$$$
Materials Cost/Use	Low number of uses	$$$
Assembly, Disassembly	Assembly increases with I/O count; disassembly time high	$$$
MCC Cost Judgement		

Equipment Required		
Item	Cost	Throughput
Pick and place station	$150K-	2K - 7.2K/hr
	$300K	
Wire bonder	$120K	5 wires/sec
Die removal system	$100K	20 die/hr

Equipment Description for Automated Process

The application of a barrier coat and enlarged bond pads requires standard thin film and photolithographic equipment. The pick and place system would require a robot with four degrees of freedom and one end effector. In order to attach the die to the temporary package, a heated platen or end effector would be required to reflow the thermo-plastic material. The wire bonder required would be a gold or aluminum ball bonder that is either fully automatic (pattern recognition) or semiautomatic (manual fiducial entry). The method of wire removal is assumed to be manual. The die removal system would require a manual, semiautomatic, or fully automatic alignment system with at least four degrees of freedom. To remove the die from the temporary package, a heated platen or end effector would be required to reflow the thermoplastic material. Depending on the residual strength on the attach material after reflow, the end effector would use either vacuum or another thermoplastic material to remove the die from the temporary package.

Comments

This is one of the few currently available sources for KGD; however, it requires the customer to pay for the additional wafer processing and accept certain compromises and limitations. For wire bonded, face up applications it is a proven technology with an established track record and customer base. Rerouting of bond pads is possible; full array is not.

Supplier Business Information

- Elmo Semiconductor Corporation
  7590 N. Glen Oaks Blvd.
  Burbank, CA 91504
  (818) 768-7400

- Primary Business: Semiconductors, related devices
- Total Employees: 237
- 1992 Sales: $18.2M

Contact

Larry Duncan
PHONE: (818) 768-7400
FAX: (818) 767-7038

Supplier:	ELMO Semiconductor	Method:	no name	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	N	1	0
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	28
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	N	3	0
Interconnect Rules Subtotal			0	4
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	N	3	0
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	ELMO Semiconductor	Method:	no name	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	21
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	21
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	22
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	N	2	0
			0	
TOTAL SCORE			0	147

GENERAL ELECTRIC

High Density Interconnect

General Information

The High Density Interconnect (HDI) module technology developed at General Electric, requires known good die[1]. In response, an adaptation of the HDI process is being developed. This technology involves overcoating the die and forming temporary bond pads on the die overcoat layer, then temporarily placing the die into a package and wire bonding to it. After burn-in and test, the wire bonds are pulled and the die is removed from the package. The temporary bond pads are etched from the die, leaving a tested chip with an overcoat and openings to the bond pads. The contact method is wire bonds, and alignment is performed by a wire bonder. Thermal management is performed by the package. General Electric is in development of this technology, with plans to use it for an upcoming module design. Texas Instruments is also a current licensee of the HDI technology.

Technical Description

The KGD HDI process begins with the die placed nearly edge to edge on either a flat substrate or one milled to have a "well" for each chip. An overcoat polymer (proprietary formulation) is spray coated onto the bare chips, which provides protection from handling, probing, or processing induced damage (the coating is not hermetic). The GE HDI laser drilling process is then applied to "drill" via holes to the die bond pads through laser ablation of the polyimide. Metallization is applied using a sputtering process, and then patterned using standard HDI photolithography to form temporary bondpads on the overcoat polymer which are connected to the chip bond pads. The substrate is sectioned to separate the die, which are placed into standard chip packages (such as PGA or LCC) and wire bonded into place. The die are burned-in and tested with standard fixtures and processing equipment. Following burn-in and test, the wire bonds are removed from the temporary bond pads. The die are removed from the packages by dissolving the die attach material in a solvent soak. The temporary bond pads are removed with an etching step. The burned-in and tested die are then ready for use in the end application.

Readiness Level

Readiness Category:

The GE process is currently in alpha test with an outside user and under government contract.

Equipment Status:

All HDI processing equipment is in place at the GE corporate research and development center in Schenectady, New York.

Process Status:

All HDI processes are fully developed, although GE continues to refine this technology.

Capacity issues:

The capacity is unknown at this time.

Qualification issues:

This "temporary interconnect" approach, along with a "bare chip probe test" approach, is being demonstrated on a 16 chip module with three complex ASIC chips and 13 SRAM chips. The temporary interconnect test approach was used with the ASIC chips, and the final module fabrication is now underway.

Alignment Method

Alignment of the bonds to die is performed by a wire bonder.

Contact Mechanism

This KGD approach uses temporary, removable wire bonds on the temporary, deposited bond pads.

Key Features

Portions of HDI technology are used to produce KGD through the use of temporary wire bond pads.

[1] Bare Chip Test Techniques for Multichip Modules, R.A. Fillion, R.J. Wojnarowski, W. Daum. 1992 Proceedings of the International Electronics Packaging Society. pp. 554

Noncompliance with Technology Assessment Guidelines:

The wire bond based technology, with required rerouting of original aluminum bond pads, is limited to use with die which have peripheral, aluminum bond pads.

- Wire bond approach means that die with area array pads cannot be burned-in or tested.
- Process not designed to convert from array to peripheral bond pads.
- Cannot accomodate incoming Au or solder bumped die; postpassivation processing, integral to technology, requires aluminum pads.

The dielectric overcoat was judged to be potentially incompatible with GaAs.

Etching away of temporary bond pad was judged to potentially result in a degredation in the quality of the final bond pad surface. Qualification through chemical and physical testing of the surface could result in a reversal of this judgement.

Wire bonding in combination with pad rerouting provides an uncontrolled impedance environment.

Optical inspection of the die is inhibited by the dielectric coat.

The GE process was not penalized for additional wafer processing , since rerouting and enlargement of bond pads is done at the die level using HDI technology.

GE process was not penalized for number of touchdowns, since enlarged pads will accomodate multiple bonds.

Process Flow

1.0 Begin with bare, singulated die in wafer tape or in waffle packs.

2.0 Pick and place the die onto flat or milled substrate, using polymer die attach.

3.0 Apply overcoat polymer layer (spray coat).

4.0 Laser drill vias to the die bond pads.

5.0 Sputter metallization over surface.

6.0 Apply photoresist.

7.0 Use GE laser scan patterning system to align and expose, forming temporary bond pads over the overcoat polymer.

8.0 Etch away unwanted metallization.

9.0 Resist strip.

10.0 Saw the substrate to separate chips.

11.0 Pick and place the die with repatterned temporary bond pads into standard packages (such as PGA or LCC).

12.0 Wire bond to the temporary bond pads on the polymer overcoat.

13.0 Burn-in packaged ICs.

14.0 Test packaged ICs.

15.0 Remove wire bonds from temporary bond pads with bond pull equipment.

16.0 Dissolve die attach polymer in solvent soak, remove from package.

17.0 Etch off metallization over polymer on chip.

18.0 Place tested and burned-in chip, with polymer overcoat layer, into packaging for delivery.

Advantages

- Uses existing wire bond assembly equipment.
- Removal of temporary bond pads used for burn-in and test of die, elimates concern for their condition afterwards.
- Standard, existing package may be used. No change in burn-in and test equipment, sockets, or parameters is required.

Disadvantages

- Cost increases with pin count since both assembly and disassembly are done one pin at a time.
- Economic reuse of package is limited.
- See also Noncompliance with Technology Assessment Guidelines

Concerns

- Addition and removal of temporary die bond pads may adversely affect original die pads to which final assembly bonds are made.
- Removal of die attach material may not be easy and/ or may affect quality and ease of final assembly.
- Addition of coating provides additional environmental protection for die. Since coating is added to

singulated die, wafer fab is not affected. However, handling of singulated die may be cumbersome and potential for introducing handling damage and defects is high. In addition, laser process for opening bond pads may be difficult to establish and/or control.

Equipment Required

GE considers the equipment used and specifics about the HDI process to be proprietary; the KGD assurance equipment used after wafer processing consists of a wire bonder, bond pull equipment, a solvent bath, and etch equipment.

Cost

Cost Factor	Comment	Cost
Wafer Processing	Reroute required	**$$$**
Materials Cost/Use	Low number of uses	**$$$**
Assembly, Disassembly	Assembly increases with I/O count; disassembly time high	**$$$**
MCC Cost Judgement		

Comments

Texas Instruments has been granted a license to use the GE HDI technology, and GE is willing to license this technology to other vendors for use in providing KGD.

Supplier Business Information

- General Electric
  Corporate Research and Development Center
  P.O. Box 8
  Schenectady, NY 12301

- Primary Business: Electrical equipment
- Total Employees:
- 1992 Sales:

Contacts:

Ray Fillion
PHONE: (518) 387-6199
FAX: (518) 387-5442

Supplier:	GENERAL ELECTRIC	Method:	HDI	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	N	1	0
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	28
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	N	3	0
Interconnect Rules Subtotal			0	4
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	GENERAL ELECTRIC	Method:	HDI	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	21
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	21
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	22
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	N	2	0
			0	
TOTAL SCORE			0	150

IBM

Reduced Radius Removal (R3)

General Information

With over one million die delivered, the IBM R3 system is the most mature KGD technology available(Figure 12). IBM will perform this service under contract at the Burlington, VT facility, or the technology may be licensed from IBM for use by other vendors. In the Reduced Radius Removal (R3) system, C4 flip-chip ready die are solder-bonded to reusable temporary carriers for test and burn-in, and then removed from the carriers with a shearing process. The solder bumps are reflowed to provide C4 bumped, fully tested chips. The contact mechanism is a solder bond, and alignment is provided by an automated system (either mechanical or vision) in combination with the self-alignment characteristics of solder. Thermal management is performed through heat dissipating through the bonds to the carrier for most applications, and an optional heat spreader may be placed on the back side of the die for high power chips. This technology is in production.

Technical Description

In April 1990, IBM qualified their Reduced Radius Removal (R3) system for providing Known Good Die to both internal and external customers. This has since become a well established, mature process for providing known good die, although it is strictly for the Controlled Collapse Chip Connect (C4) flip-chip die attach process. To date, over 1,000,000 R3 KGD have been shipped to customers. IBM has developed a set of ceramic carriers with a variety of footprints to accommodate die from 6 mm x 6 mm to 18 mm x 18 mm, with up to 2700 total C4 bumps. These carriers are compatible with existing test and burn-in equipment.

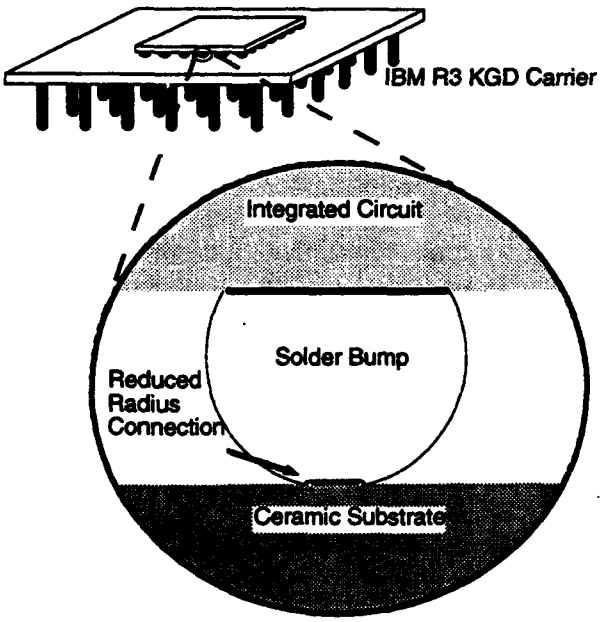

Figure 12. IBM R3 KGD Carrier

The R3 process requires that the incoming die have C4 solder bumps. The ceramic PGA carriers are patterned with an array of solder pads which have a reduced radius relative to the C4 bumps on the die. Initial alignment is done through an automated process, either mechanically or with a vision system. The solder provides characteristic self-alignment and a temporary attach. Final attachment is made using standard reflow and deflux processes. Lastly, a temporary metal cap is placed over the die to create a "packaged" IC with a PGA pinout configuration. After burn-in and test, the die is removed from the carriers using a shearing process. The reduced radius of the carrier pads makes this the weakest mechanical point of the bond and the shearing action breaks the solder cleanly at the connection point between die and carrier bumps. After disassembly the die are reflowed to reform the solder bumps. The burned-in and tested C4 die is ready for final assembly and the carrier is ready for reuse.

Although carriers are reusable, the number of uses is limited and is presumably less than the potential number of uses for most temporary contact KGD technologies. Another limitation to this technology is the number of C4 bumps which can be sheared using the current disassembly technique. However, this number is quite large (2700) and would be unlikely to affect most die. In addition, IBM is investigating alternate shearing strategies to accommodate a larger number of I/O.

Readiness Level

Readiness Category:

This technology is currently in production.

Equipment status:

All necessary equipment is in place and operating at IBM, Burlington.

Process status:

The process is completely developed for all IC types.

Capacity issues:

IBM is the only volume KGD supplier currently available. IBM is currently seeking to "grow" this service as a profit center, and has made the necessary investments to provide volume production.

Most IC fabrication facilities are not equipped to provide solder bump processing on their products. IBM is equipped and accustomed to performing this task. This implies that the die be provided in wafer format. Contact IBM for details.

Qualification issues:

IBM has completed extensive in-house qualification of the R3 process at die, module and system levels. One million die have been shipped since 1990. Qualification has been completed on die with up to 2700 total C4 bumps.

Alignment Method

The C4 bonding process is self-aligning after a rough mechanical placement.

Contact Mechanism

Contact to die is made by reflow of C4 bumps to solder ball bonds on the carrier.

Key Features

R3 is a proven and qualified process for C4 flip chip KGD.

Noncompliance with Technology Assessment Guidelines

The C4 based technology is limited to use with die which have solder bumped bond pads.

- R3 process not defined for use with Al or Au pads.
- Additional wafer processing required (solder-bumping).
- Cannot accommodate incoming Au bumped die: R3 process not defined for use with Au bumps; C4-bumping process requires aluminum pads as initial surface.
- C4 process requires a minimum of 100 C4 bumps per die; therefore, smallest die size is approximately 100 mils on a side; TAG calls for ability to accommodate 50 mil die.

IBM R3 process was not penalized for pad damage or number of touchdowns, since contact is solder-to-solder and both die and carrier bumps can be restored by reflow.

Process Flow Description

1.0 Begin with singulated, C4 bumped die.
2.0 Inspect.
3.0 Attach die to carrier by applying flux, aligning and placing die.
4.0 Reflow and deflux assembly.
5.0 Clamp protective lid over assembly.
6.0 Burn-in.
7.0 Test.
8.0 Unclamp and remove lid.
9.0 Remove die from carrier by shear.
10.0 Return carriers to inventory for reuse.
11.0 Reflow C4 bumps on die.
12.0 Inspect.
13.0 Load die into packaging for delivery to customer.

Advantages

- Uses existing C4 assembly equipment.
- Reflow of C4 die after burn-in and test ensures bumps are in good condition for final assembly.
- Mature technology, currently in use with over one million parts delivered.
- Burn-in and test parameters (speed, power dissipation, etc.) are the same as for a die in a single chip package.
- Easily accommodates high I/O (>200) die, for relatively low additional cost.
- Thermal management provided by bump contacts. Use of backside thermal grease for additional control is not a concern in final assembly assuming a flip chip application.

Disadvantages

- Number of uses per carrier is low.
- See also Noncompliance with Technology Assessment Guidelines

Concerns

- Selection of this technology means that wafers must be solder bumped, which limits final assembly options. Defects also may be introduced. If preferred final assembly requires solder bumps (e.g., C4) then cost of wafer bumping is value added.

Equipment Required

Item	Cost	Throughput
Pick and place system	$150-$300K	6-10 die/min
C4 solder reflow system	$100K	30-80 die/min
Flux removal system	$150K	10-30 die/min
Capping System	$10K	30-50 die/min
Cap removal	$20K	6-10 die/min
Mechanical shear removal system	$150K	6-10 die/min

Equipment Description for Automated Process

The pick and place system would require a robot with four degrees of freedom that is either fully automatic (pattern recognition), or semiautomatic (manual fiducial entry). The system uses either mechanical or a vision system for use in registering the die to the carrier within the needed tolerance. Vertical force sensing and control for die handling would be required. The C4 solder reflow and deflux stations would require a multiple stage belt oven that is computer controlled. The capping system would install the carrier lid prior to burn-in and functional test. The cap removal system would remove the carrier lid after burn-in and functional test operations. The mechanical shear removal system removes the die from the carrier. The removal system must be able to secure the die after removal to prevent the die from being damaged.

Cost

Detailed cost information was presented by IBM at the MCC KGD Technology Supplier Forum on 13 May 1993.

Cost Factor	Comment	Cost
Wafer Processing	Solder bumps	$$
Materials Cost/Use	Relatively low # of uses	$$
Assembly, Disassembly	Cycle times moderately high	$$
MCC Cost Judgement		

Comments

This is the only mature, volume oriented KGD process available now. IBM is best positioned to service the C4 KGD market.

Supplier Business Information

- International Business Machines Corporation
  Old Orchard Road
  Armonk, NY. 10504
  (914) 765-1900
- Primary Business: Electronics, Computers
- Total Employees: 300,000
- 1992 Sales: $64.6B

Contacts

Technical questions: Gary Hill
Dept. N39, Bldg. 962-2
1000 River Road
Essex Junction, VT 05452-4299
PHONE: (802) 769-3449
FAX: (802) 769-1249

Licensing: Mike Krueger
Dept. N80, Bldg. 962-1
IBM Corporation
1000 River Road
Essex Junction, VT 05452-4299
PHONE: (802) 769-3356

OEM Services: Don Swietek
Dept. 585, Zip 92E 1580
IBM Corporation
Route 52
Hopewell Junction, NY 12533
PHONE: (914) 892-5583

Supplier:	IBM	Method:	R^3	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	31
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	N	2	0
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	7
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	7
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	N	3	0
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	IBM	Method:	R^3	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	25
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	25
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	24
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	163

MICRON SEMICONDUCTOR, INC.

Softool

General Information

The Micron Softool process has been used for initial production of low pin count KGD by Micron, and this technology has been licensed to Chip Supply, Inc. for use in providing KGD to the general market. Die are placed into packages with a temporary die attach, and "soft" wire bonds are made to the die bond pads for test and burn-in. The wire bonds are then pulled off the die bond pads, and the die are removed from the packages and are ready to use as KGD. The contact mechanism is a "soft" wire bond, and alignment is performed by the wire bonder. Thermal management is performed by the package. This technology is currently in production.

Technical Description

A "soft" wire bond is used at the die bond pad. Control of the amount of force is critical. After burn-in and test, each wire is pulled individually. Time and care is required in order to prevent critical die pad damage.

Readiness Level

Readiness Category:

This technology is currently in production.

Equipment status

The Softool process uses existing standard wire bond and modified pull test equipment.

Process status

The process has been optimized for single sourced aluminum.

Capacity issues

Micron will supply their own chips as KGD using the Softool process, but is not prepared to accept die from other manufacturers; for this, contact Chip Supply. Softool is limited in bond pad pitch, total I/O count, and in throughput, especially as I/O counts increase.

Qualification issues

The Softool process is currently in use at Micron to supply SRAM and DRAM ICs to customers. Micron has licensed this process to Chip Supply to allow them to supply die to the commercial market.

Alignment Method

Alignment is performed by a wire bonder.

Contact Mechanism

Contact is made with temporary wire bonds.

Key Features

Technology uses standard packages with removable wire bonds.

Noncompliance with Technology Assessment Guidelines

The wire bond based technology is limited to use with die which have peripheral, aluminum bond pads.

- Wire bond approach means that die with area array pads cannot be burned-in or tested.
- Process not designed to convert from array to peripheral bond pads.
- Softool process not defined for use with Au or solder bumps.

The Softool process is limited to a single touchdown.

Removal of temporary bond was judged to likely result in a degredation in the quality of the final bond pad surface through physical damage.

Wire bonding is an uncontrolled impedance environment.

Process Flow

1.0 Begin with bare finished die on wafer tape or in waffle packs

2.0 Pick and place in standard package, using a temporary die attach.

3.0 Wire bond, using a soft adhesion wire bond.

4.0 Burn-in.

5.0 Test.

6.0 Remove wire bonds using modified bond pull equipment.

7.0 Remove die from package. Dissolve thermoplastic die attach with solvent bath, or by heating package to reflow.

8.0 Transfer die to delivery packaging.

Advantages

- Uses existing wire bond assembly equipment.
- Standard existing package may be used. No change in burn-in and test equipment, sockets or parameters is required.
- Demonstrated technology, currently in use.
- Low cost entry, suitable for prototyping and low volumes.

Disadvantages

- Cost increases with pin count since both assembly and disassembly are done one pin at a time.
- Economic reuse of package is limited.
- Removal of temporary wire bonds done one at a time is time consuming and potentially damaging to die bond pad.
- See also Noncompliance with Technology Assessment Guidelines

Concerns

- Soft bond assembly process may be difficult to optimize and control. Variations in Al from different die manufacturing make setting bond parameters difficult. Bond must be strong enough to survive handling, burn-in and test, yet weak enough to be cleanly and easily removed afterwards.
- Removal of die attach material may not be easy and/ or may affect quality and ease of final assembly.

Equipment Required

Item	Cost	Throughput
Pick & place system $300K	$150-	2K-7.2K
Wire bonder	$120K	5 wires/sec
Wire pull system	$100K	5-10 wires/min
Die removal system	$100K	20 die/hr

Equipment Description for Automated Process

The pick and place system would require a robot with four degrees of freedom that is either fully automatic (pattern recognition), or semiautomatic (manual fiducial entry). The system would require a vision system for use in registering the die and the thermoplastic preform to the carrier within the needed tolerance. Vertical force sensing and control for die handling would be required. In order to attach the die to the temporary package, a heated platen or end effector would be required to reflow the thermoplastic material. The wire bonder required would be a gold or aluminum ball bonder that is either fully automatic (pattern recognition) or semiautomatic (manual fiducial entry). To remove the die from the temporary package, a heated platen or end effector would be required to reflow the thermoplastic material. Depending on the residual strength on the attach material after reflow, the end effector would use either vacuum or another adhesive material to remove the die from the temporary package. The wire pull system would consist of a standard manual wire pull tester.

Cost

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use	Low number of uses	$$$
Assembly, Disassembly	Assembly increases w/I/O count; disassembly time high	$$$
MCC Cost Judgement		

Comments

This technology for KGD is currently available. This approach does not require the wafer processing and bond pad reforming that the Elmo approach requires, and does not leave a clipped ball bond at the pad site when the process is complete. It does still impose a number of significant restrictions, a relatively low throughput, and relatively high cost.

Supplier Business Information

- Micron Semiconductor, Inc.
  2805 E. Columbia Rd.
  Boise, ID 83706
  (208) 368-4000
- Primary Business: Semiconductors
- Total Employees: 4,200
- 1992 Sales: $323.5M

Contacts

Gene Cloud, Micron
PHONE: (208) 368-3951
FAX: (208) 368-4617

Jim Rates, Chip Supply
PHONE: (407) 296-5604
FAX: (407) 290-0164

Supplier:	Micron	Method:	Softool	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	29
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	N	3	0
Interconnect Rules Subtotal			0	4
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Micron	Method:	Softool	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
Low I/O Test Rules Subtotal			0	18
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
High I/O Test Rules Subtotal			0	18
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
Burn In Rules Subtotal			0	19
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	144

MCNC

Reusable Burn-In and Test Substrate (BATS)

General Description

A KGD technology for solder bumped chips has been developed by the Microelectronics Center of North Carolina (MCNC). This is a carrier-based approach utilizing a proprietary metallurgy and dejoin process (Figure 13). Die are attached to a carrier for test and burn-in, after which the dejoin process weakens the metallurgical connection between die and carrier, allowing for easy removal of the die. The contact is a sacrificial metal, and rough alignment is performed by a C4 flip chip bonder. The wettable sacrificial metal provides a final self-alignment. Thermal management is provided by the heat dissipating through the bond pads for normal applications, and an optional heat spreader may be placed on the backside of the die for high power applications. MCNC is currently developing this technology, and plans to make it available for licensing when development is complete.

Technical Description

The MCNC KGD method uses a temporary metallurgical connection between IC solder bumps and a reusable multilayer ceramic carrier. The temporary metallurgical connection is a solder-wetted sacrificial thin-film metallization over a nonwettable thick-film metallization pattern. The die is attached to the carrier using a standard flux and reflow operation. After burn-in and test, the IC is removed from the carrier with a special dejoin process which causes the sacrificial metal to dramatically reduce its connective strength. The IC then can be removed with very little force. After processing, the substrates are recycled by cleaning and redepositing the sacrificial thin-film metallization.

An adaptation of this method also allows for transfer of solder bumps from the carrier to the device. This permits use of die with aluminum bond pads. In this variation, a sacrificial thin film metal is deposited on the carrier over nonwettable metallization. Solder bumps are then deposited over the sacrificial metal. The die is

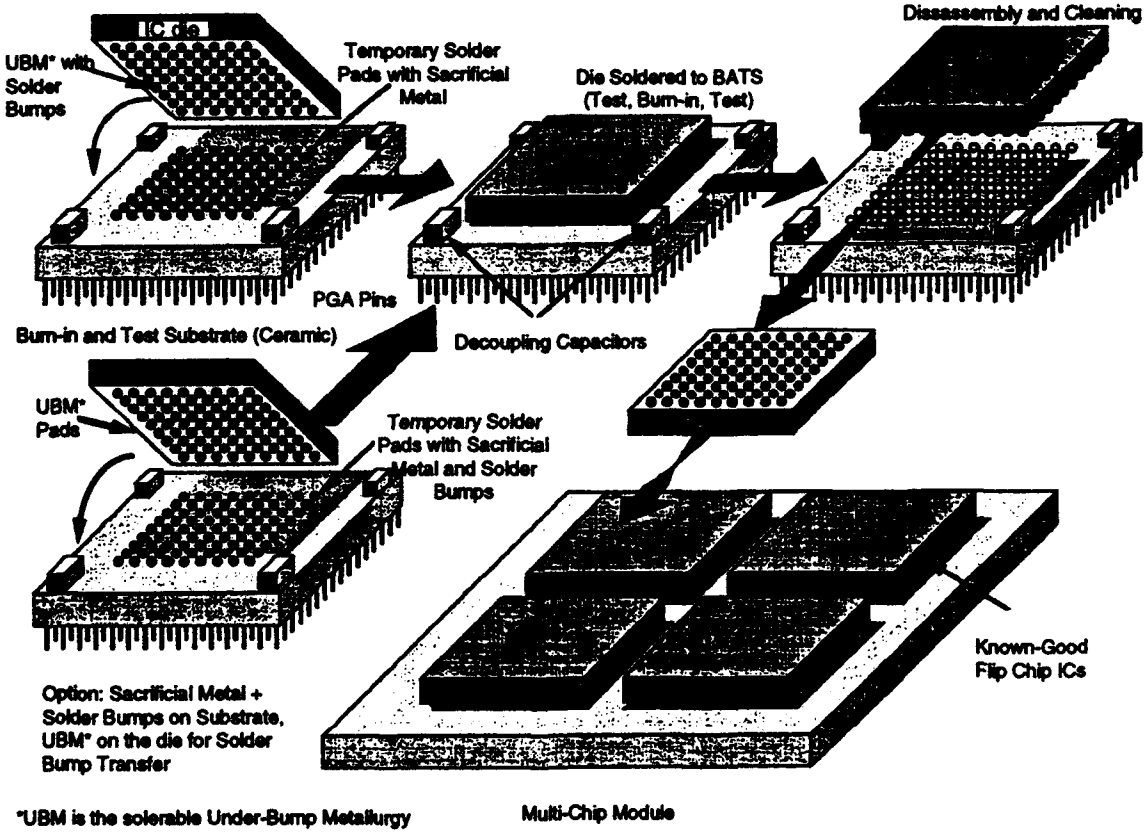

Figure 13. Reusable Burn-in And Test Substrate (BATS)

prepared by depositing a thin film barrier metal and a wettable nonsacrificial metal over the bond pads in wafer form. The die is bonded to the carrier in the normal fashion and processed through burn-in and final test. During the dejoin process, the solder bump de-wets from the carrier and stays with the die. The carrier can then be reused by replacing the sacrificial metal and the solder bumps.

Another adaptation currently beginning development allows for burn-in and test of wire bond and TAB ICs by relocating the solder bumps over the passivation using an aluminum redistribution metallization layer.

Readiness Level

Readiness Category:

This technology is currently in development.

Equipment Status:

All necessary equipment is in place at MCNC.

Process Status:

Working processes for depositing sacrificial metal on carriers and solder bump transfer have been developed, and are currently being refined for production use.

Capacity Issues:

MCNC is research and development facility with prototype capability only.

Qualification Issues:

In-house testing has been performed on between 300 to 400 devices.

Alignment Method

Self-alignment of the solder joints follows a rough automated vision-based alignment.

Contact Mechanism

The contact between die and carrier is made with a sacrificial metal that provides a metallurgical bond during test and burn-in.

Key Features

The BATS technology is characterized by a temporary metallurgical bond requiring low removal force. High I/O counts are possible. 1679 I/O has been demonstrated.

Noncompliance with Technology Assessment Guidelines

The BATS technology is limited to use with die which have solder bumped bond pads.

- BATS process not currently defined for use with Al or Au pads, although development efforts are underway.
- Additional wafer processing (solder-bumping) required (MCNC can bump wafers).
- Cannot accommodate incoming Au bumped die: BATS process not defined for use with Au bumps.

Use of sacrificial metal was judged to potentially result in a degradation in the quality of the final bond surface. Qualification through chemical and physical testing of the surface could result in a reversal of this judgement.

The BATS process was not penalized for number of touchdowns, since sacrificial metal does not affect ability to repeat the process.

Process Flow Description

1.0 Begin with bumped die on wafer tape (sawn) or in waffle pack type packaging.

2.0 Assembly

- 2.1 Pick, align, and place inverted die on ceramic substrate with flux.
- 2.2 Reflow the solder in a multizone belt furnace.
- 2.3 Remove flux residues in semiaqueous cleaner.

3.0 Test.

4.0 Burn-in.

5.0 Disassembly

- 5.1 Reflow the solder in a multizone belt furnace with flux.
- 5.2 Remove flux residues in a semiaqueous cleaner.
- 5.3 Pick the die off the carrier and place in package for delivery.
- 5.4 Recondition the substrate by redepositing the sacrificial metal.

Advantages

- Uses existing solder bump (flip chip) assembly equipment.
- Burn-in and test parameters (speed, power dissipation, etc.) are the same as for a die in a single chip package
- Easily accommodates high I/O (>200) die for relatively low additional cost.
- Thermal management provided by bump contacts. Use of thermal grease for additional control not a concern in final assembly assuming a flip chip application.

Disadvantages

- Solder bumping of die by transfer from carrier requires remetallization of carrier after each use.
- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- Selection of this technology means that wafers must be solder bumped which limits final assembly options. Defects may also be introduced. If preferred final assembly requires solder bumps, then cost of wafer bumping is value added.
- Addition of solder bumps by transfer from carrier still requires wafer-level processing in the form of barrier added. Process may be difficult to optimize.

Equipment Required

A flip chip aligner/bonder is used for die to carrier assembly. Thin film metallization plating equipment required to plate sacrificial metals on carrier.

Cost

MCNC current cost models indicate, at manufacturing volumes, the BATS processing cost including equipment amortization, substrate amortization, materials, and labor will range from $1.62 per die (< 100 I/O) to $5.40 per die (<2500 I/O). Test and burn-in charges not included.

Cost Factor	Comment	Cost
Wafer Processing	Solder bumps	$$
Materials Cost/Use	Relatively low # of uses	$$
Assembly, Disassembly	Cycle times moderately high	$$
MCC Cost Judgement		

Comments

The solder bump transfer capability is an innovative idea. By relegating the solder bump process to the carrier, device yield loss from this step can be avoided, and economies of scale can be achieved even for short run devices.

Supplier Business Information

- Microelectronics Center North Carolina
  Electronic Technologies Division
  3021 Cornwallis Road
  Research Triangle Park, NC 27709-2889

- Primary Business: Research and development
- Total Employees: 275
- 1992 Sales:

Contact

Glenn A. Rinne
(919) 248-1941

Supplier:	MCNC		Method:	Burn-in and Test Subs
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	31
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	N	3	0
Interconnect Rules Subtotal			0	4
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	N	3	0
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	MCNC	Method:	Burn-in and Test Subs	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	25
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	25
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	24
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	162

Temporary Contact Approaches to KGD

Acsist

Aehr Test Systems

Fresh Quest

IBM

MCC

Micron Semiconductior (KGD Plus)

Packard Hughes

Plastronics

Qualhi

Sandia National Lab

TI/MMS

TRIBOTECH

Yamaichi

ACSIST ASSOCIATES INC.

Particle Interconnect

General Information

ACSIST plans to apply their patented Particle Interconnect (PI) technology into a TAB slide type carrier in order to take advantage of the existing base of TAB processing equipment. The interconnect would be built with ACSIST laminate capabilities, and other parts of the carrier mechanism provided by partners. The contact mechanism would be based on the piercing action of the particle interconnect. Plans are to use meanical or optical alignment of the die to carrier interconnect. This product is currently conceptual, and ACSIST intends to enter into a partnership agreement with another company to develop the mechanical portions of the carrier.

Technical Description

ACSIST Associates has a patented contact methodology, Particle Interconnect (PI) for forming separable or permanent interconnections with minimal damage to the surface(s) being probed. PI forms a connection by utilizing a piercing action to penetrate any surface oxides. This interconnect technology has been successfully applied in a number of commercial test applications for packaged ICs, and is also currently being utilized for testing MCM-L substrates which are manufactured by ACSIST. In addition, this interconnect technology is being used by one external customer to test high I/O, flip chip ready, area array solder bumped integrated circuits.

ACSIST is currently developing a miniaturized version of Particle Interconnect on a laminate probe slide frame similar to TAB tape frames. These will be compatible with industry (JEDEC) standard TAB test carriers and sockets. The initial probes will have the capability of contacting peripheral bond pads on an 8 mil pitch and area array bond pads on a 20 mil pitch, with subsequent development (during 1994/95) to 3.8 mil pitch bond pads. These size limitations are a function of the interconnect rather than the particle technology. The membranes will have an integral compliance capability to accommodate the minor planarity variations of either the membrane probe or the device under test. In addition, PI technology may be incorporated directly on burn-in boards to increase the density of components on those boards. The condition of the die pads after use of this interconnect is unknown and may be dependent on metallurgy and configuration (e.g., thin Al pads vs. thick solder bumps). The number of uses per particle interconnect and required maintenance (cleans) are unknown. ACSIST will enter into strategic relationships to deliver an integrated solution for KGD.

Readiness Level

Readiness Category:

This technology is conceptual.

Equipment status:

Assembler/disassembler equipment is currently conceptual. Assembly/alignment and disassembly would have to be performed manually until this equipment is ready.

Process status:

Particle deposition and coating processes are still in development. ACSIST is currently working under a research grant to extend their membrane laminate interconnects to a 3.8 mil pitch capability, and also continuing development of the particle contact system. A generic carrier assembly process has been described, but ACSIST points out that each user may modify the process for insertion into their own process flow. Details of the "integral hold down mechanism" remain concealed, but indicate that it is a simple clamping action after alignment.

Capacity issues:

Production capacity for making laminate based membrane probes suitable for area array solder bumped ICs available now,

Qualification issues:

Some contact resistance work has been performed.

Alignment Method

Alignment methodologies will depend on the carrier, which has not yet been defined. Provisions for mechanical alignment (fiducials) can be fabricated on the membrane; this will require precision sawing of the die. In lieu of accurate sawing, optical alignment must be used.

Contact Mechanism

Extremely hard conductive particles (typically, plated diamond) pierce oxides without scrubbing, with comparatively small normal force applied. Particles may be as small as one micron, and several choices of metallurgy are available.

Key Features

Particles are used to make contact between the die and interconnect. Membrane probe sets (slides) will be designed to fit JEDEC TAB slide carriers and sockets for test and burn-in.

Non-Compliance with Technology Assessment Guidelines

The current choice of interconnect limits the technology to an 8 mil pitch and a 100 micron bond pad. Development plans call for an approach which will allow ACSIST to meet the TAG High I/O limits of 6 mil pitch and 75 micron pads.

Process Flow Description (conceptual)

1.0 Begin with die in waffle pack or sawn on wafer tape.

2.0 Place die in PI membrane slide.

3.0 Activate integral hold down mechanism.

4.0 Insert PI membrane slide into standard JEDEC TAB slide carrier; close lid.

5.0 Burn-in.

6.0 Test.

7.0 Deactivate integral hold down mechanism and remove die from PI membrane, placing die into delivery packaging.

8.0 Inspect.

9.0 Clean and return PI membrane and TAB slide carrier for reuse.

Advantages

- Piercing action may enhance contact reliability.
- Contact mechanism proven in packaged ICs.

Disadvantages

- Technology is be pitch limited nows.
- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- Nonuniform particle size and piercing action may cause pad damage, especially for nonplanar die with thin metallization.
- Size grading and sorting of particles may be costly.
- Frequency and method for cleaning contacts is unknown. Robustness to clean may depend on materials selection.
- Ultimate use and value of this contact technology is dependent upon carrier and interconnect selection.

Equipment Required

Item	Cost	Throughput
Assembler/disassembler	$50K (man.)	100/hr (man)
	$250K (auto)	1000/hr (auto)

The equipment for automated operation would require a high speed pick and place robot with six degrees of freedom and end effector control. Depending on the precision of the sawn devices, the system would require a vision system with pattern recognition for registering the die to the PI membrane slide to the required tolerance. Z-axis force control and sensitivity would be required particularly for delicate materials such as GaAs. If die can be presented to the pick and place unit in a face down orientation, it would eliminate the need for adding the equipment to invert the die. This may be accomplished by using reversible chip trays or waffle packs which would present the back side of the die to the manual or automatic pick and place equipment.

Cost

The following information was supplied by ACSIST. Tooling of PI membrane slides would range from $3K to $5K. Lead time for new designs would be four to six weeks, and lead time for repeat orders would be two weeks or less. The TAB slide frame carriers and sockets are currently commercially available from multiple suppliers.

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use	Size grading of particles required	$$
Assembly, Disassembly	Dependent on carrier approach	
MCC Cost Judgement		

Comments

This contact methodology may be best suited for bumped die, since there is less need to control particle size and penetration.

Supplier Business Information

- ACSIST Associates
  3965 Meadowbrook Road
  Minneapolis, MN 55426
  (612) 931-1300

- Primary Business: Printed circuit boards
- Total Employees: 130
- 1993 Sales: $14M

Contact

Carl Reynolds
PHONE: (612) 931-1334
FAX: (612) 938-3731

Supplier:	Acsist	Method:	Particle Interconnect	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Acsist	Method:	Particle	Interconnect
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	26
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	N	3	0
Min. pad dimension	75 µm	N	3	0
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	20
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	25
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	169

AEHR TEST SYSTEMS

Carrier/Socket

General Information

Aehr Test is developing a complete process for handling and performing burn-in and test of bare die in reusable carriers that are compatible with existing burn-in, test, and automated handling systems (Figure 14). The development includes a family of carriers which can handle die with up to 500 I/O. The carrier uses a derivative of the Nitto Denko ASMAT thin film interconnect. Contact to the die is made using the nonscrubbing, oxide piercing bumps which are an integral part of the interconnect. Alignment is strictly mechanical. The carrier lid is used as a heat spreader for thermal management. Aehr is currently in alpha test of this carrier with a partner company. Investments in equipment for carrier production and an automatic loading station are also currently being made. As a supplier of burn-in equipment and supplies, Aehr is particularly sensitive to issues of compatibility and automation.

Technical Description

The Aehr Test carrier uses Nitto Denko ASMAT thin film interconnect to provide electrical connection between the pads on the die and the contacts on the burn-in and test socket. The ASMAT material is a polyimide film which supports fine line pitch and through holes filled with metal, forming electrically conductive bumps on the film. Data from Nitto Denko indicates that the ASMAT die contact interface provides a low contact resistance (50 to 60 milliohms) at 30 to 70 grams of contact force per pin. Nitto has successfully used the ASMAT technology in probe cards for test applications. The carrier provides the mechanical support for the interconnect and the mechanical interface to the socket. A mechanism contained within the carrier mechanically aligns the die, interconnect, and socket interface. The hinged lid applies a controlled force to the die and allows it to mate properly to the substrate. Once installed in the carrier, the die is protected from the environment. Sufficient thermal mass is provided by the carrier to remove heat from the die. Work by Nitto Denko indicates that damage to aluminum bond pads due to contact with the ASMAT bumps is minimal. Thermal life of the interconnect is expected to be high.

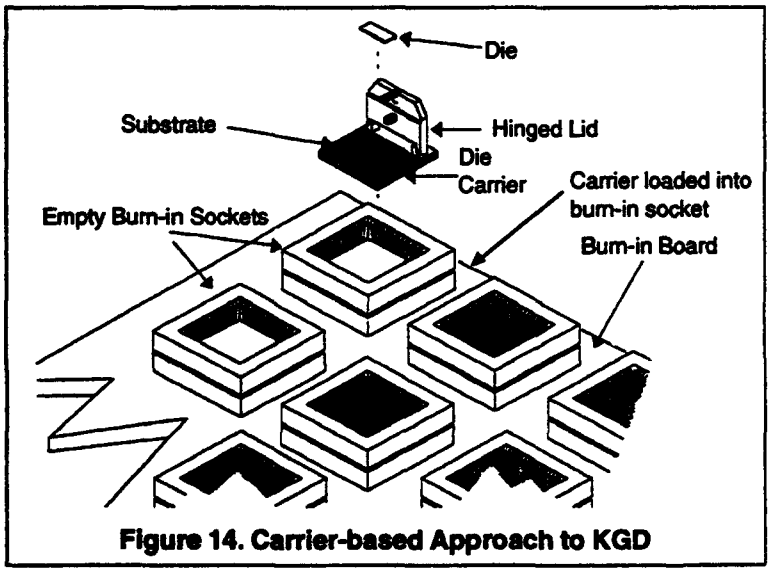

Figure 14. Carrier-based Approach to KGD

Readiness Level

Readiness Category:

The Aehr Test carrier is in alpha test, both in-house and at a beta site. Aehr is currently investing in the low-cost tooling required to produce carriers and sockets in quantity at low cost. The current generation of carriers is machined. Production sockets are available up to 116 pins.

Equipment status:

The die are currently loaded into carriers by hand. An automatic loading station is in the works and is expected to be ready by 3Q94. Carriers may be loaded into sockets on burn-in boards using Aehr Test's existing ALS-1000 automated loader/unloader.

Process status:

The Nitto Denko film has been characterized and is ready for use. The die loading/unloading process is currently performed by hand, automation will follow with the auto loading station.

Capacity issues:

Production capacity for sockets is essentially unlimited, but capacity for carrier assembly is currently 500 to 1000 per week. This capacity is limited by manual test and inspection throughput, which will be increased by automation. Lead

times for carriers and sockets is currently about 10 to 12 weeks ARO, which allows time for design verification.

Qualification issues:

Aehr is currently qualifying this carrier/socket for KGD production using test during burn-in to verify contact reliability. This qualification test data will be made available upon request when completed. An electrical performance evaluation is part of this qualification, as well as mechanical/contact resistance/alignment tests.

Alignment Method

Alignment is strictly mechanical, although later a version may offer provisions for optical alignment.

Contact Mechanism

Bumps in the Nitto Denko ASMAT film make contact similar to rivets by penetrating oxide without scrubbing motion.

Key Features

Simple carrier approach depends on ASMAT technology from Nitto Denko. Use of mechanical alignment offers potential for high throughput.

Noncompliance with Technology Assessment Guidelines

The current approach calls for mechanical alignment of the die which will require a high precision wafer saw process.

The Aehr Test technology was not penalized for die size, although there are some concerns as to how very small die might be handled and aligned. (TAG guidelines say that the technology will accommodate 50 mil die).

Process Flow Description

NOTE: This describes the process for assembling die into the prototype version of the carrier, and does not represent the process for the anticipated production version.

1.0 Begin with die on wafer tape (sawn) or in waffle pack type packaging

2.0 Assembly

- 2.1 Remove lid screw
- 2.2 Swing lid aside
- 2.3 Pick and place die face down in proper orientation
- 2.4 Rotate lid into place
- 2.5 Insert screw

3.0 Disassembly

- 3.1 Remove lid screw
- 3.2 Swing lid aside
- 3.3 Remove die with vacuum wand and place in delivery package
- 3.4 Rotate lid into place
- 3.5 Insert screw

Advantages

- Nonscrubbing contact may minimize pad damage, assuming excessive force is not required to overcome non-planarity.
- Contact materials and mechanism has been characterized by Nitto Denko at time and temperature.
- Quick mechanical align possible for precision sawn die.
- Company is very sensitive to compatibility and automation issues.
- Assembly provides air tight seal for protection during burn-in and test.

Disadvantages

- Currently no methodology for maintaining die placement during assembly if alignment must be made using vision (rather than mechanical) system.
- See also Noncompliance with Technology Assessment Guidelines

Concerns

- Nonscrubbing action may affect contact reliability.
- Frequency and method of cleaning contacts is unknown. If cleaning requires scrubbing,, it may significantly impact lifetime by weakening probe tip to interconnect interface.
- Die saw may not be precise enough to permit mechanical align.

Equipment Required

Item	Cost	Throughput
Die to carrier assembly station	$150K - $300K	2K/hr - 7.2K/hr
Carrier to socket assembly station	$100 - $150K	≈ 2000/hr

Equipment Description for Automated Process

Fully-automated system is in development.

Cost

Cost Factor	Comment	Cost
Wafer Processing	None required	$
Materials Cost/Use	High carrier reuse	$
Assembly, Disassembly	Mechanical align	$
MCC Cost Judgement		

Comments

Since Aehr is a supplier of burn-in equipment, it is expected that their solutions to KGD will be highly sensitive to compatibility with existing burn-in and test processes and strategies.

Supplier Business Information

- Aehr Test Systems, Inc.
  1667 Plymouth Street
  Mountain View, CA 94043
  (415) 691-9400

- Primary Business: Test and burn-in equipment
- Total Employees: 200 - 250
- 1992 Sales: $25M - $50M

Contacts

Lina Prokopchak
PHONE: (415) 691-9400
FAX: (415) 691-0980

Carl Buck
PHONE: (415) 691-9400

Supplier:	AEHR	Method:	no name	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	N	2	0
Wafer Mount & Saw Rules Subtotal			0	2
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	AEHR	Method:	no name	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	26
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	26
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(A.,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	25
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	173

CALIFORNIA CONTACTS

Microbeam

General Information

California Contacts is developing a KGD technology based on their microbeam probe technology (Figure 15). The configuration of the socket is for making contact to bare die, without the use of a carrier. Bare die are placed directly into the sockets, face down, where scrubbing style contact is made by the independently compliant probes in the socket. Rough alignment of the die is made mechanically by a machined chip guide and fine align is a manual optical operation. The die is held in place by a spring clip and pressure plate, which also serves as a heat sink. These microbeam sockets are directly mounted on the test and burn-in boards, where they remain, while bare die are inserted and removed. California Contacts is in development of this system, and they are currently under contract to produce a small quantity of sockets and burn-in boards. California Contacts relies heavily on subcontracting to supply components for their technology.

Technical Description

California Contacts plans to use their microbeam conductor and contact system to provide a controlled impedance interconnect environment in die sockets, which are mounted directly on a tester load board or burn-in board. The microbeam contact system provides controlled impedance to within mils of the IC bond pads, and allows for user selection of contact metallurgies. Electrical contact is made with traditional scrubbing action by the microbeams, which are individually cantilevered. This provides compliance for even contact force across all pads. A separate microbeam assembly is required for each side of the die. Only die with peripheral bond pads may be used. Initial alignment is made by mounting each of the four microbeam assemblies on the burn-in board and aligning each to the die. After one alignment, the microbeam assemblies do not need further alignment. The die are mounted into the die sockets face down using a mechanical/manual optical alignment system, and the die are held in place using an integrated spring clip/heat sink. Die may be placed into and removed from a test socket at the socket site, and an assembly station for loading die into multiple site burn-in boards is available.

The condition of bond pads after use is expected to be similar to those after conventional probe. This technology is expected to be pitch limited. The number of uses per microbeam assembly is expected to be moderate and may be limited by the number of cleans.

Readiness Level

Readiness Category:

This technology is in development. A customer has begun placing orders with California Contacts for bare die burn-in boards. Product qualification is anticipated based on prior experience with probe card products from California Contacts.

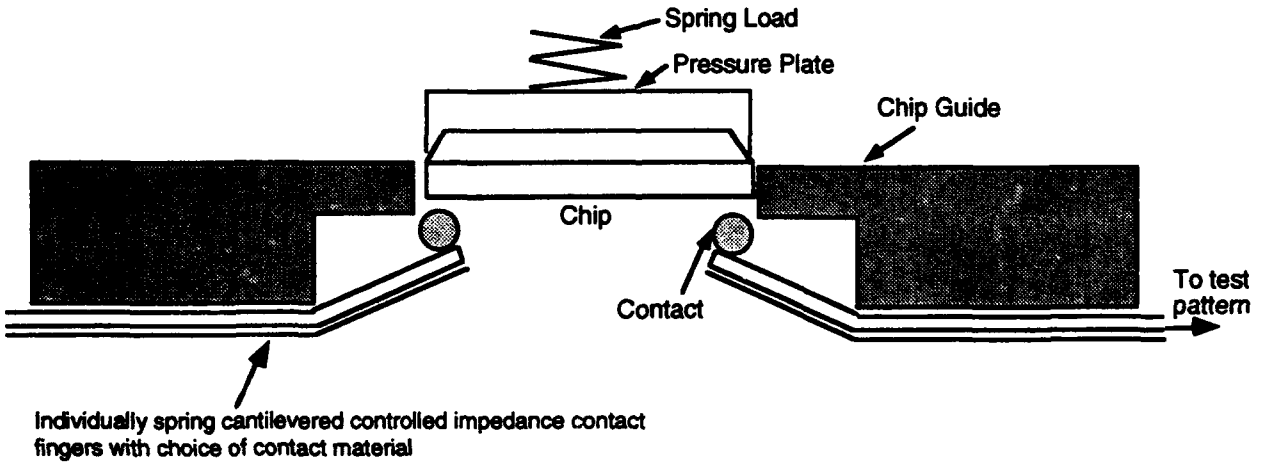

Figure 15. KGD Concept

Equipment status:

All equipment needed for fabrication of the components of this technology is in place at subcontractor facilities or at California Contacts. Assembly of the die into test sockets or burn-in boards may be performed manually, but the normal lead time for this product allows for design and production of a customer specific insertion and removal station. This design is specific to the particular burn-in boards used by each customer, due to the direct insertion of die into the sockets on burn-in boards.

Process status:

The assembly/disassembly is a direct insertion and removal. No other die processing is required. The process for fabrication of microbeam contacts has been in place for probe card production and is well established.

Capacity issues:

A 6 to 8 week lead time is required for microbeam, socket, and board design and fabrication. Following this period, California Contacts is capable of delivering 5 to 10 multiple site burn-in boards per week.

Qualification issues:

Although the microbeam probe contactors have been used for years and have demonstrated reliable probe life of over one million touchdowns, no specific qualification of the KGD carrier/socket has been performed. This will be performed in conjunction with an initial order (already pending).

Alignment Method

Rough mechanical placement is followed by manual optical align.

Contact Mechanism

Proprietary microbeam contactor mechanism uses individual cantilevered beams for compliance and scrubbing.

Key Features

Impedance controlled interconnect is provided in this carrier-free technology. Bare die are placed directly in burn-in board sockets.

Noncompliance with Technology Assessment Guidelines

The probe card based technology is limited to use with die which have peripheral bond pads with a pitch of 8 mils or greater. Development plans call for an approach which will allow California Contacts to meet the TAG High I/O limits of 6 mil pitch and 75 micron pads.

The current approach calls for mechanical alignment of the die which will require a high precision wafer saw process.

The California Contacts technology was not penalized for die size, although there are some concerns as to how very small die might be handled and aligned. (TAG guidelines say that the technology will accommodate 50 mil die).

Process Flow Description

1.0 Begin with bare die on wafer tape or in waffle packs

2.0 Assemble and align Microbeam contacts on load board and burn-in boards.

3.0 Load die and board into optical alignment station.

4.0 Align and place die into sockets on board.

5.0 Apply spring clip/heat sink to hold die in place.

6.0 Burn-in die.

7.0 Remove die from burn-in boards.

8.0 Load and align die in test load board

9.0 Test die in tester load board.

10.0 Remove Spring clip/heat sink.

11.0 Remove die from tester load board.

12.0 Place die in delivery packaging.

Advantages

- Scrubbing action may enhance contact reliability.
- Contact mechanism proven at ambient conditions in probe cards.
- Better than average compliance for reliable contact to non-planar die.
- Quick mechanical align possible for precision sawn die.
- User selectable metallurgy at probe tips.

Disadvantages

- Technology is pitch limited.
- Currently no methodology for maintaining die placement during assembly if alignment must be made using vision (rather than mechanical) system.
- See also Noncompliance with Technology Assessment Guidelines

Concerns

- Scrubbing action over temperature excursions may introduce unacceptable amounts of pad damage for final assembly application.
- Alignment directly to load board or burn-in board may be difficult.
- Probe tips may require more maintenance than average. Cleaning may shorten life of probes.

Equipment Required

Item	Cost	Throughput
Assembly station	Unknown	Unknown

Equipment Description for Automated Process

The pick and place system would require a robot with four degrees of freedom and two end effectors. The system would require a vision system with pattern recognition capabilities and two cameras for use in registering the die to the carrier within the needed tolerance. Vertical force sensing and control for die handling would be required. Chip inversion could be performed by using a reversible chip transport tray which could be flipped to present the back side of chip prior to component acquisition . If chip inversion is performed after component acquisition, the pick and place system must have two robot arms. One robot arm must acquire and rotate die, while the other arm must retrieve the die from the back side. A custom end effector will install and remove the carrier assembly.

Cost

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use	Probe tips require more maintenance than average	$$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Possibility for placement of "micro-fabbed" capacitors very near the pad contact points. Pad pitch down to 3.8 mils planned. Note die load directly onto burn-in boards or load boards.

Supplier Business Information

- California Contacts
  1118 Walsh Avenue
  Santa Clara, CA 95050
  (408) 986-0930

- Primary Business: Test fixtures for electronic components
- Total Employees: 3
- 1992 Sales: $250K — $500K

Contact

George Isaac
PHONE: (408) 986-0930
FAX: (408) 986-9841

Supplier:	California Contacts	Method:	Micro Beam sockets	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	31
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	N	2	0
Wafer Mount & Saw Rules Subtotal			0	2
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	California Contacts	Method:	Micro Beam sockets	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	24
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	N	3	0
Min. pad dimension	75 µm	N	3	0
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	18
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	23
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	159

FRESH QUEST CORPORATION

Quest Chip Carrier (QC^2) and Probe Card

General Information

Fresh Quest has proposed two approaches to the KGD problem; the first is a carrier approach called the Quest Chip Carrier (QC^2), the second is a probe card with controlled impedance and high operating temperature. This document describes the carrier approach.

The Quest Chip Carrier (QC^2) is a member of a family of products based on the "Photolithographic Pattern Plated Probe" (P4) technology developed by Fresh Quest Corporation. This is a temporary carrier approach, using a thin film membrane and the P4 contactor to make a scrubbing contact to the die (Figure 16). Alignment is currently using a manual optical system, with plans for a mechanical alignment system. Thermal management is provided by a chip support plate which serves as a heat spreader. Fresh Quest is now alpha testing the QC^2 carriers in cooperation with a chip supplier.

Technical Description

The Quest Chip Carrier (QC^2) uses a proprietary interconnect and die contact mechanism. The carrier may be used for burn-in and test of die with peripheral bond pads and pitches of 5 mil or greater. Pitch capabilities of 4 mil are targeted for 1994. The carrier itself consists of a die contact assembly, a carrier assembly, a chip support plate, and a spring clip which holds the assembly together and applies contact force. Alignment may be done with a machined alignment plate, which requires precision sawn die, or with a machine vision system. The die assembly is burned-in and tested using existing equipment. Disassembly simply involves removal of the spring clip. Damage to die bond pads is expected to be minor and probably the number of uses will be moderate to high.

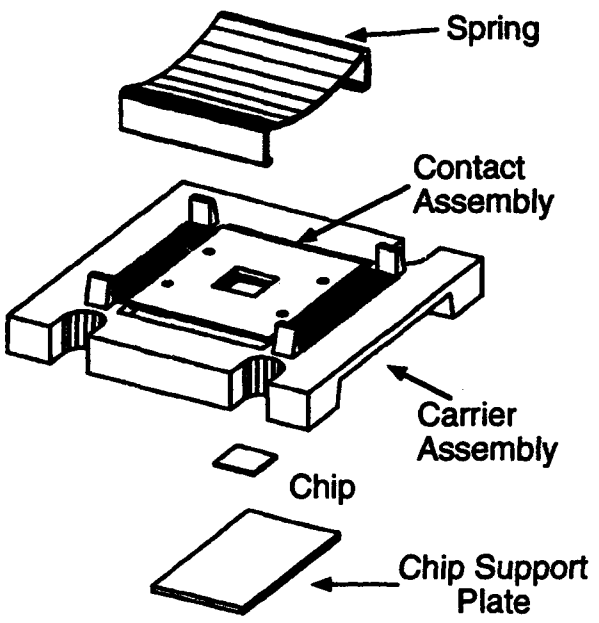

Figure 16. Exploded View of Carrier

Readiness Level

Readiness Category:

The Fresh Quest carrier is in alpha test. In addition to internal evaluation of this product by Fresh Quest, National Semiconductor and NEC are providing beta test evaluation of the die carrier technology. Sample parts in small quantities will be shipped to National and NEC in Q4 '93. Following the evaluation and characterization of these carriers, each plans to use these carriers to produce small quantities of known good die in pilot production.

Equipment status:

In cooperation with one pilot customer, Fresh Quest is evaluating a semi-automatic die load/unload workstation prototype which may be the basis for providing a turnkey automation solution for KGD production.

Process status:

Several versions of Fresh Quest probe cards have been produced for and tested by National Semiconductor, the primary beta test site for the probe card technology. Present development activities include technology refinement, testing, and characterization of the QC^2 die carrier. Specialized fixtures for building, loading, and testing carriers are being developed, in addition to probe cards.

Capacity issues:

Fresh Quest moved into a new 21,000 square foot facility in November 1993. This facility contains appropriate equipment and facilities for the design and produc-

tion of probe cards and die carriers. This facility will provide capacity for initial production and ongoing R&D activities.

Qualification issues:

Product testing and qualification is underway in conjunction with beta test sites.

Alignment Method

A machined alignment plate or machine vision system is used.

Contact Mechanism

Proprietary contact assembly, uses scrubbing to penetrate oxide.

Key Features

Proprietary die pad contact mechanism is used in combination with flex circuit.

NONCOMPLIANCE WITH TECHNOLOGY ASSESSMENT GUIDELINES

The current approach calls for mechanical alignment of the die which will require a high precision wafer saw process.

The Fresh Quest technology was not penalized for die size, although there are some concerns as to how very small die might be handled and aligned. (TAG guidelines say that the technology will accommodate 50 mil die).

PROCESS FLOW (MECHANICAL ALIGN)

1.0 Begin with sawn wafers on tape.
2.0 Vacuum pick up of chip.
3.0 Chip inversion.
4.0 Chip loaded into carrier using precision alignment plate.
5.0 Chip Support plate installation.
6.0 Burn-in.
7.0 Test.
8.0 Load carrier assembly into unload fixture.
9.0 Draw vacuum and remove spring clip.
10.0 Remove chip carrier sub assembly, leaving chip on support plate.
11.0 Visual inspection of chip.
12.0 Chip loaded into shipping container.

PROCESS FLOW (OPTICAL ALIGN)

1.0 Begin with sawn wafers on tape.
2.0 Vacuum pick up of chip.
3.0 Chip placed on chip support plate.
4.0 Chip aligned to carrier/contact sub assembly.
5.0 Spring clip aligned and assembled with chip carrier.
6.0 Burn-in.
7.0 Test.
8.0 Load carrier assembly into unload fixture
9.0 Draw vacuum and remove spring clip
10.0 Remove chip carrier sub assembly, leaving chip on support plate
11.0 Visual inspection of chip
12.0 Chip loaded into shipping container

ADVANTAGES

- Scrubbing action may enhance contact reliability.
- Better than average compliance for reliable contact to nonplanar die.
- Quick mechanical align possible for precision sawn die.

DISADVANTAGES

- Currently no methodology for maintaining die placement during assembly if alignment must be made using vision (rather than mechanical) system.
- See also NONCOMPLIANCE WITH TECHNOLOGY ASSESSMENT GUIDELINES

CONCERNS

- Scrubbing action over temperature excursions may introduce unacceptable amounts of pad damage for final assembly app
- Frequency and meth[illegible] cleaning contacts is unknown.
- Technology may be pitch limited.

Equipment Required

Item	Cost	Throughput
Assembler/ Disassembler	$170K	2K/hr
Pick & place system	$150K	2K/hr

Equipment Description for Automated Process

The fully automated die load and unload station is based on a robotic work cell initially designed for accurate placement of die in MCMs. A reversible chip transport tray is used to present the back side of die prior to component acquisition. Tandem upward-facing and downward-facing cameras coupled with pattern recognition capabilities are used to automatically align flipped die with the die carriers within necessary tolerances. Carrier assembly (clipping the die support plate against the back side of the die) is performed as a second operation within the same work cell. This work cell accommodates both die load and unload processes.

Cost

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use		$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Fresh Quest is working on both a mechanical alignment and a machine vision alignment system at the same time.

Supplier Business Information

- Fresh Quest Corporation
  531 E. Elliot Rd., Suite 120
  Chandler, AZ 85225-1118
  (602) 497-4200

- Primary Business: IC test fixtures
- Total Employees: 70 including Fresh Test
- 1992 Sales: Currently funded by Fresh Test

Contact

H. Dan Higgins
PHONE: (602) 497-4200
FAX: (602) 497-4220

Supplier:	Fresh Quest	Method:	QC/2	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	31
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	N	2	0
Wafer Mount & Saw Rules Subtotal			0	2
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Fresh Quest	Method:	QC^2	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	24
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	24
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	23
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	165

IBM
Dendrite Carrier

General Information

A second generation, carrier-based approach to C4 flip chip KGD is now being qualified by IBM. This approach uses ceramic carriers with palladium dendritic structures for making contact to the C4 solder bumps, in conjunction with a unique clamp top/heat sink subassembly to hold the die in place for test and burn-in. Contact is made by the piercing action of the dendrites into the solder balls, and alignment may be either mechanical or optical. Thermal management is integral to the clamp top subassembly. IBM is currently beginning the initial qualification stages with this product.

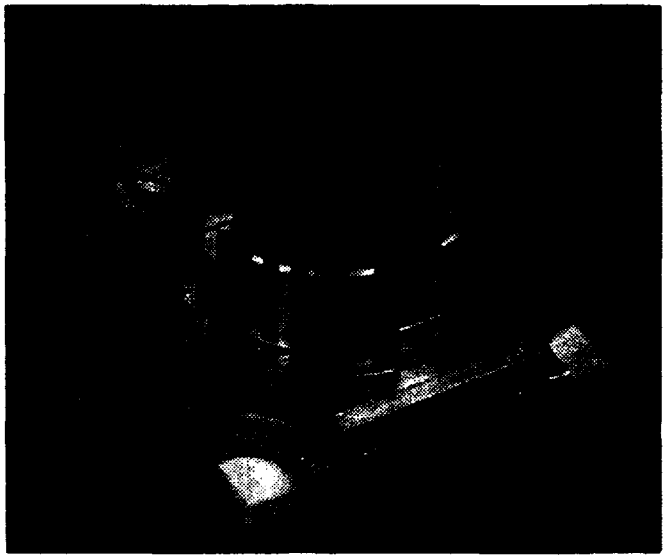

Figure 17. IBM Dendrite Carrier

Technical Description

The IBM dendrite carrier is a mechanical interconnection system using dendritic structures on the die carrier and a unique clamping methodology (Figure 17). The initial qualification will cover die up to 13mm x 13mm, with up to 2000 total C4 solder bumps. The carriers are ceramic pin grid array (PGA) carriers ranging from 24mm x 24mm to 50mm x 50mm and are compatible with existing test and burn-in equipment to address the compatibility requirements associated with those process steps.

The ceramic carriers are processed through a series of plating steps which result in the creation of a palladium dendritic structure on the contact pads of the carrier. The die are supplied with C4 solder bumps and are aligned and placed on the carrier so that the C4 solder bumps contact the dendritic "fingers" on the carrier. A slight pressure is applied to the back of the die to lightly embed the fingers into the solder bumps. The clamp top subassembly is then placed and locked into the base carrier assembly. The force required to place the C4 bumps into intimate electrical contact with the dendritic fingers is supplied by applying a given torque to the center screw in the clamp top subassembly which transfers a vertical force to the backside of the die. A gimbal design within the top subassembly insures that the clamp is planar with the backside of the die prior to the compression step. A spring in the gimbal design insures that the contact is maintained throughout the burn-in and test procedures. This assembly is then subjected to burn-in and test, and the carriers are then disassembled by reversing the torque of the screw in the clamp top, the clamp top removed, and the die is extracted from the carrier. The die is then reflowed to reshape the solder balls and then visually inspected. The number of uses per carrier is expected to be moderate with no rework and high with rework. The carrier requires only an IPA wash in-between uses.

Readiness Level

Readiness Category:

The IBM dendrite approach is in alpha test. This product has passed feasibility testing, and initial qualification testing is due to begin immediately.

Equipment Status:

Equipment for producing and plating the carriers is in place at IBM. A chip placement system for automated alignment and placement of the die into the carrier and subsequent clamp top placement and assembly is not yet available. This operation may currently be performed manually, with an optical microscope station for manual alignment, or using mechanical alignment methods.

Process Status:

The carrier dendrite plating process is proprietary to IBM, and is fully developed. The die to carrier assembly

process is also fully developed, although there is no automatic assembly equipment currently available.

Capacity Issues:

Production capability for dendrite plated ceramic carriers, for the purposes of KGD production, are virtually unlimited.

Qualification Issues:

IBM is currently in the initial stages of product qualification for this KGD method.

Alignment Method

Alignment of the die to carrier may use either a mechanical or optical system.

Contact Mechanism

Plated dendrites on the carrier contacts are mechanically held in contact with the C4 solder balls of the die, with the dendrites penetrating the surface of the solder.

Key Features

Proprietary dendrites provide good contact to C4, or other solder bumps, with much higher number of uses per carrier than with IBM R3.

Noncompliance with Technology Assessment Guidelines

The IBM dendrite technology is limited to use with die which have solder bumped bond pads.

- Dendrite process not defined for use with Al or Au pads.
- Additional wafer processing required (solder-bumping).
- Cannot accommodate incoming Au bumped die: Dendrite process not defined for use with Au bumps; C4-bumping process requires aluminum pads as initial surface.

Process Flow Description

1.0 Begin with singulated C4 bumped die.

Most IC fabrication facilities are not equipped to provide solder bump processing on their products. IBM is equipped and accustomed to performing this task. This implies that the die be provided to IBM in wafer format. Contact IBM for details.

2.0 Incoming visual sample inspection.

3.0 C4 die placement on burn-in carrier.

- 3.1 Mechanically or visually orient die on carrier.
- 3.2 Apply slight force to backside of die to seat C4 on dendritic fingers.

4.0 Assembly of clamp top.

- 4.1 Place clamp top subassembly in clamp base subassembly.
- 4.2 Lock top subassembly into base subassembly.
- 4.3 Apply required vertical force to backside of die by applying torque to top subassembly center screw.

5.0 Place carriers into burn-in board sockets, place in oven(s) and perform burn-in.

6.0 Remove carriers from burn-in board sockets, place into tester socket & test.

7.0 Remove clamp top subassembly.

- 7.1 Release vertical force on die by reversing torque of top subassembly center screw.
- 7.2 Unlock top subassembly from base subassembly.
- 7.3 Vertically lift top subassembly away from base subassembly.

8.0 Remove die from carrier using proprietary removal tool.

9.0 Die bond pad reflow.

10.0 Outgoing visual sample inspection.

11.0 Load die into package for delivery to customer.

Advantages

- Piercing action may enhance contact reliability.
- Die held in place by carrier contacts during align and clamp.
- Clamp top subassembly has an integral heatsink.
- Clean of dendrites between uses is accomplished with a simple wash.

Disadvantages

- See Noncompliance with Technology Assessment Guidelines.

Concerns

- Selection of this technology means that wafers must be solder bumped which limits final assembly options. Defects also may be introduced. If preferred final assembly requires solder bumps (e.g., C4), then the cost of wafer bumping is value added.

Equipment Required

Item	Cost	Throughput
Chip placement system		
Clamp assembly/ disassembly system		
C4 Solder reflow system		
Flux removal system (unless an H2 reflow is used)		

Equipment Description for Automated Process

The die placement system would use either a mechanical or a vision based system for alignment of the die to carrier within the needed tolerance. Vertical force sensing and control for die handling would be required. The carrier assembler would insert the clamp top subassembly into the base subassembly, lock the top subassembly into place, and apply the required torque to the top center screw. The disassembler would reverse the torque process, unlock the top subassembly, remove the top subassembly from the base subassembly, and the die removal tool would remove the die from the carrier, placing it into the reflow carrier. The die could be reflowed in nitrogen, necessitating a flux application system, or reflowed in hydrogen without flux.

Cost

Cost Factor	Comment	Cost
Wafer Processing	Solder bumps	$$
Materials Cost/Use		$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Supplier Business Information

- International Business Machines Corporation
  Old Orchard Road
  Armonk, NY 10504
  (914) 765-1900

- Primary Business: Electronics, Computers
- Total Employees: 300,000
- 1992 Sales: $64.6B

Contacts

Technical questions: Gary Hill
Dept. N39, Bldg. 962-2
1000 River Road
Essex Junction, VT 05452-4299
PHONE: (802) 769-3449
FAX: (802) 769-1249

Licensing: Mike Krueger
Dept. N80, Bldg. 962-1
IBM Corporation
1000 River Road
Essex Junction, VT 05452-4299
PHONE: (802) 769-3356

OEM Services: Don Swietek
Dept. 585, Zip 92E 1580
IBM Corporation
Route 52
Hopewell Junction, NY 12533
PHONE: (914) 892-5583

Supplier:	IBM	Method:	Dendrites	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	31
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	7
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	N	3	0
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	IBM	Method:	Dendrites	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	25
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	25
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	24
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	165

MICROELECTRONICS AND COMPUTER TECHNOLOGY CORPORATION

TAB Based KGD Carrier

General Information

The Microelectronics and Computer Technology Corporation (MCC) has developed a known good die technology. The technology was developed within a separate project, independent of the KGD project and is being transferred to participant companies. This approach is based on the use of TAB tape frames with additional plated metallurgy at the inner lead bond sites to form temporary carriers. An adaptation of a regular TAB slide frame carrier is used to hold the tape and die, with a clamshell fixture providing normal force through a clamping action (FIgure 18). The contact mechanism is a temporary scrubbing contact, and alignment is performed by a standard flip chip aligner/bonder. Thermal management is provided by the clamshell spring clip which acts as a heat spreader. This technology is currently being transferred to participant sites, and is considered to be under development.

Technical Description

MCC Flip Chip Technology Development Project required high speed test and dynamic burn-in of a single bare die. In response to this need, a technology was developed (independent of MCC Known Good Die projects) which allows for burn-in and test of die with peripheral bond pads.

The approach adapts a TAB tape frame to provide an "interposer" contacting mechanism which is usable with JEDEC standard TAB slide carriers and sockets. The adaptation involves plating the tape with metals which will not have undesirable interactions with the chip bond pads during burn-in and bending the inner leads upward. The bent leads are embedded in silicone elastomer, which holds the tape in the bottom half of a "clamshell" structure and provides a spring action, compliance, and scrubbing under z-axis deflection. The carrier includes a pedestal against which the die is pressed; this controls the amount of z-axis deflection. The top of the carrier is snapped into place, and the die assembly is handled as a chip on tape for test and burn-in.

No degradation in carrier materials was noted after five burn-in cycles (168 hrs/150°C); it is likely that the average number of uses per carrier be at least 10. Chips have been shown to be wire bondable even after burn-in in a noninert atmosphere. Wire pull strengths were identical to chips which had not been burned-in.

Readiness Level

Readiness Category:

This technology is currently in development.

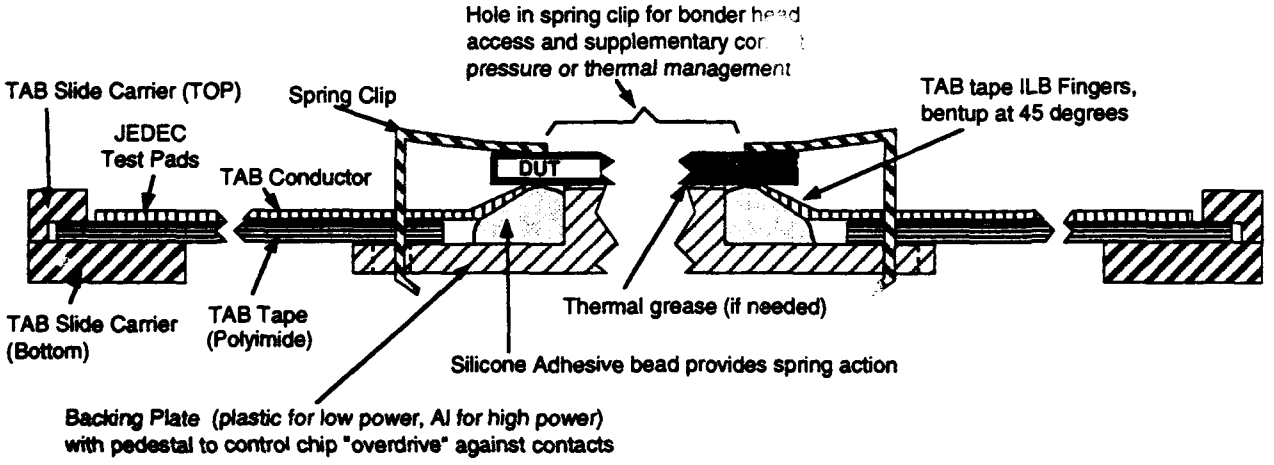

Figure 18. MCC Clamshell KGD Carrier

Equipment Status:

This KGD method requires a standard flip chip aligner/bonder and common TAB handling equipment. No automatic disassembler equipment exists.

Process Status:

No wafer processing is required, and the carrier assembly/disassembly is a manual operation. Fabrication of the carriers involves additional plating steps on standard TAB tape, depositing a silicon elastomer bead, and machining the clamshell structure. These processes have been developed and demonstrated.

Capacity Issues:

This technology is currently being developed at two sites, but no production capacity is in place yet. MCC is capable of prototype quantities only.

Qualification Issues:

This technology has been extensively investigated at MCC, using both a 216 lead device at 6 mil pitch, and one 328 lead device at 4 mil pitch. Contact resistances are approximately 20mΩ. These resistances do increase during burn-in, but remain below the 100 mΩ limit, and may easily be recovered by rescrubbing. Specific qualification plans will be the responsibility of vendor sites.

Alignment Method

Alignment is currently manual optical, but may be mechanical in the future.

Contact Mechanism

Metallic probe fingers provide scrubbing action.

Key Features

Adaptation of TAB tape uses JEDEC standard TAB slide carriers and sockets.

Noncompliance with Technology Assessment Guidelines

The TAB based technology is limited to use with die which have peripheral bond pads.

- TAB approach means that die with area array pads cannot be burned-in or tested
- Process not designed to convert from array to peripheral bond pads.

It is assumed that the TAB tape will be single level and therefore unable to achieve 50 ohm controlled impedance.

Process Flow Description

1.0 Begin with die on wafer tape (sawn) or in waffle pack type packaging.

Assembly

2.0 Place die, TAB tape test and burn-in carrier, and top of clamshell in flip chip aligner/bonder station.

3.0 Align die I/O to socket and press down against pedestal.

4.0 Press top of clamshell down onto bottom half.

Disassembly

5.0 "Declipping" tool opens clamshell and presents die for removal.

6.0 Use vacuum handler to remove the die and place in delivery packaging.

Advantages

- Scrubbing action may enhance contact reliability.
- Better than average compliance for reliable contact to non-planar die.
- Assembly clamping mechanism is integral to die alignment and placement so that die position is maintained during assembly.
- Access to back of die (75% exposed) may facilitate thermal management.
- Uses existing TAB tape slide carriers.
- No clean of contacts is required.

Disadvantages

- Relatively low number of uses per carrier/interconnect.
- Assembly/cycle time expected to be lower than average.
- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- Scrubbing action over temperature excursions may introduce unacceptable amounts of pad damage for final assembly application.

Equipment Required

Item	Cost	Throughput (cycles/hr)
Flip chip aligner/bonder	$250K(auto) $50K(manual)	750 (auto) 120 (manual)
Declipping fixture	$5K	> 1000/hr, limited by handler

Equipment Description for Automated Process

The flip chip aligner/bonder system would require a robot with four degrees of freedom and a custom end effector. The system would require a vision system with pattern recognition capabilities and for use in registering the die to the carrier within the needed tolerance. Vertical force sensing and control for die handling would be required. Chip inversion could be performed by using a reversible chip transport tray which could be flipped to present the back side of chip prior to component acquisition. If chip inversion is performed after component acquisition, the pick and place system must have two robot arms. One robot arm must acquire and rotate die, while the other arm must retrieve the die from the back side.

Cost

The costs were determined by the MCC Flip-chip project participants. Tape tooling is $7.5K - $9K and 8 to 10 week lead time. This cost includes the first 1000 tape sites. "Clamshell" tooling cost is approximately $5K, with 2 - 5 week lead times. After this the consumables cost is approximately $2 to $4 per chip (depending on I/O) at low volumes, decreasing towards $1 per chip at high volumes. Each TAB tape-based test and burn-in carrier is usable for four test/burn-in cycles.

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use	Low number of uses	$$$
Assembly, Disassembly	Assembly method and potential damage	$$$
MCC Cost Judgement		

Comments

MCC is inserting this technology into production, with one chip supplier (Harris Corporation) and one chip user (Hughes Aircraft Corporation) evaluating this technology for internal use.

Supplier Business Information

Commercial access to the MCC TAB tape-based KGD carrier is possible in two ways:

1. Through purchase of KGD from Harris Semiconductor, who is a licensee and user of the MCC KGD carrier technology.
2. Through a single-client service contract with MCC wherein MCC:

— designs and builds the carriers for the customer

— inserts the devices to be tested

— procures appropriate TAB test/burn-in sockets

— designs and procures test DUT boards and/or burn-in load boards or adapters

— subcontracts test and/or burn-in to a commercial test house

— removes the devices from the carriers

— delivers both "passed" and "failed" devices to the customer with test results data.

- Microelectronics and Computer Technology Corporation (MCC)
  3500 West Balcones Center Drive
  Austin, TX 78759-6509
  (512) 343-0978

- Primary Business: Electronics research
- Total Employees: 317
- 1992 Sales: $44M

Contact

Rick Nolan
PHONE: (512) 250-3016
FAX: (512) 250-2893

Supplier:	MCC		Method:	TAB Based Carrier
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	31
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	MCC	Method:	TAB Based Carrier	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	22
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	22
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	23
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	163

MICRON SEMICONDUCTOR, INC.

KGD^{plus} ™

General Information

Micron is currently testing their second generation KGD technology, known as KGD^{plus}, which will enable production of higher I/O devices with a higher throughput and lower cost per die than their Softool technology. Micron was unwilling to share specific details of their technology for this report. This document contains the information currently available. The KGD^{plus} system plans are for a temporary carrier, with custom contactor assemblies to make contact to die bond pads. The nature of the contact mechanism is unknown, as Micron is evaluating several technologies for this purpose. Alignment is a manual optical operation, with plans for automation. Thermal management will be a function of the carrier. Micron is in the alpha test stage with this technology, with plans for introduction of low pin count KGD products due in 1Q94.

Technical Description

KGD^{plus} is based on a family of reusable, socketable, universal carriers which address the requirements of low, medium, and high pin count devices. These carriers are adapted for each part type using a contactor assembly which is also reusable. Micron is planning to evaluate multiple contactor technologies for this purpose. Finally, Micron is partnering with equipment and parts suppliers to supply these components and the equipment required to handle them in an organized, product driven effort. Using this approach, bare die will be assembled into a universal carrier, contacted with a contactor assembly, burned-in and tested while in this assembly, and then removed for delivery to the customer.

The number of reuses per carrier will depend largely on the contact technology selected, as will the condition of the die bond pads after burn-in and test. However, as indicated at the May 1993 Supplier Forum, the amount of damage done to the pads is a key concern in selecting the connector (probe tip) technology.

Readiness Level

Readiness Category:

The KGD^{plus} carrier is in alpha test. A low pin count version is expected to be made available in the first quarter 1994. The high pin count version, fully automated version to be available at a later date.

Equipment status:

The KGD^{plus} is a carrier based approach using either manual assembly or automatic assembly/disassembly equipment. Manual assembly equipment is available now, and Micron is working with equipment vendors to develop the necessary automatic equipment for this process.

Process status:

The KGD^{plus} process is not yet available for either purchase of die or for licensing. The only details of the die-to-carrier assembly or disassembly that have been revealed outside of Micron is that the die into carrier assembly is currently performed manually.

Capacity issues:

As the technology is currently not in production, Micron is not prepared to reveal their potential capacity.

Qualification issues:

Not enough is known about the KGD^{plus} carrier and contact mechanism to make any assessment of quality issues.

Alignment Method

A vision system is used to align the die to the carrier.

Contact Mechanism

Several contactor technologies are still under evaluation.

Key Features

The key features of this technology are unknown.

Noncompliance with Technology Assessment Guidelines

Very little specific information is available regarding this technology. Based on inputs from Micron, the technology will be unable to achieve 50 ohm controlled impedance.

The Micron KGD+ technology was not penalized for die size, although there are some concerns as to how very small die might be handled and aligned.

Process Flow

1.0 Begin with bare wafer on film frame, presorted and sawn.

2.0 Assembly in carriers

- 2.1 Load into automated assembler
- 2.2 Load Universal Carriers
- 2.3 Select program/align/set up assembler.
- 2.4 Run production lot through assembler

3.0 Burn-in parts in universal carriers.

4.0 Final test

5.0 Disassemble

- 5.1 Load Carriers into assembler/disassembler
- 5.2 Set up/alignment/program selection
- 5.3 Run production lot for disassembly
- 5.4 Unload die to delivery package.
- 5.5 Unload carriers

6.0 Package die for delivery to customer (If not already packaged by disassembler).

Advantages

- Contact is believed to be nonscrubbing which may minimize pad damage, assuming excessive force is not required to overcome nonplanarity.
- Contact verified at assembly by built-in electronics.

Disadvantages

- Minimal information regarding this technology is available. Manufacturer claims indicate no potential disadvantages, but there is no supporting evidence.
- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- If contact is nonscrubbing, this may affect contact reliability.
- Mechanism for maintaining die placement during assembly is unknown.
- Frequency and method for cleaning contacts is unknown.

Equipment Required

Item	Cost	Throughput
Assembler/Disassembler	$100K to $500K	Unknown

Equipment Description for Automated Process

Assembler/disassembler installs die to and removes die from the universal carrier. Die will be picked from an expanded wafer ring. Carriers will be indexed from an elevator system. A robot with four degrees of freedom will be required to insert and remove the carrier lid. The pick and place system must have two robot arms. One robot arm must acquire and rotate die, while the other arm must retrieve the die from the back side. The system would require a vision system with pattern recognition capabilities and two cameras for use in registering the die to the carrier within the needed tolerance. Vertical force sensing and control for die handling would be required.

Cost

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use		$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Supplier Business Information

- Micron Semiconductor, Inc.
  2805 E Columbia Rd.
  Boise, ID 83706
  (208) 368-4000
- Primary Business: Semiconductors
- Total Employees: 4,200
- 1992 Sales: $320M

Contact

Jerry Johnson
PHONE: (208) 368-3958
FAX: (208) 368-3834

Supplier:	Micron Semiconductor	**Method:**	KGD+	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Micron Semiconductor	**Method:**	KGD+	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	24
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	24
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	25
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	171

PACKARD HUGHES, INC.
Membrane Probe Set

General Information

Packard Hughes has a fine pitch thin film contactor technology available which may be applied to the KGD market. The concept is a carrier with a Packard Hughes contactor membrane for making contact to the die together with an elastomer backing, and a spring clamp with a support plate/heat spreader mechanism (Figure 19). The contact made by the membrane is an oxide piercing temporary contact, and alignment is a manual optical operation. Thermal management is provided by a chip support plate/heat spreader. Packard Hughes could have a product line available within one year, given the right market situation. They are currently in development of this technology, capable of providing custom prototypes designed to meet specific contract requirements.

Technical Description

Packard Hughes is considering applying their "Gold Dot" membrane probe technology to the known good die problem. The probes can be configured as a traditional probe card or as contactors for individual die. The membrane probe contacts offer long lifetimes and high bandwidth impedance matching for signal fidelity. They are capable of accepting small pitch (4 mil) high pin-count devices, and Al, Au, and Sn/Pb metallization, in array or peripheral configuration, and bumped or unbumped format. This technology is still in need of some development and qualification for use in providing KGD, but the basic contacting technology meets the general requirements for getting signals to and from the die. Packard Hughes is also investigating scaling this technology to accommodate full wafer burn-in capability.

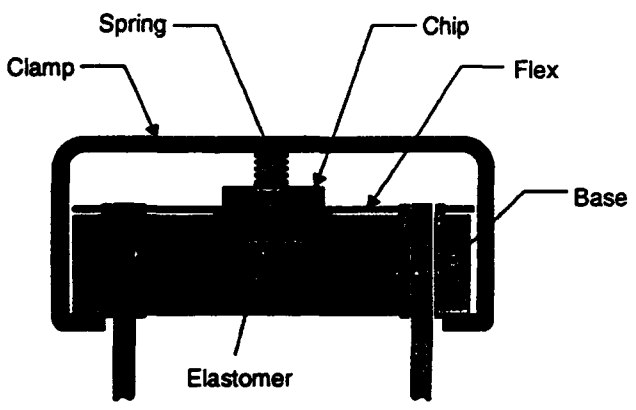

Figure 19. Single Chip Test Socket

The number of uses is expected to be high, assuming that a high temperature adhesive can be substituted for the current one. The shape and composition of the probe tips are conducive to very minimal pad damage.

Readiness Level

Readiness Category:

This technology is in development. Packard Hughes is prepared to provide custom designed KGD products, but does not have a KGD product line defined.

Equipment status:

The equipment required for automated carrier assembly and die insertion/removal is still in the developmental stage. These components would be manually assembled for prototype quantities.

Process status:

Packard Hughes is currently refining the materials and processes used to fabricate their membrane probe products, in order to increase the durability of this product at high temperatures. The burn-in carrier product does not exhibit thermal life problems, and the existing manufacturing process is capable of providing KGD burn-in carriers.

Capacity issues:

Packard Hughes has capital equipment and processes in place to produce medium volumes of custom designed KGD carriers, but these would be assembled manually.

Qualification issues:

In-house testing of the interconnect used in the KGD carriers has been performed at Packard Hughes, but no alpha site testing or qualification level testing has been performed to date.

Alignment Method

Alignment method is manual optical.

Contact Mechanism

Contact is made with proprietary gold dot contacts.

Key Features

Proprietary interconnection membrane uses gold dot contacts.

Noncompliance with Technology Assessment Guidelines

The adhesive currently used in forming the interface between the interconnect and probe tips will not survive burn-in temperatures. Development plans call for use of a higher temperature adhesive.

The Packard Hughes technology was not penalized for die size, although there are some concerns as to how very small die might be handled and aligned. (TAG guidelines say that the technology will accommodate 50 mil die).

Process (IC contactor)

1.0 Begin with diced wafer on tape.

2.0 Assembly

- 2.1 Load wafer tape and carriers into assembly station.
- 2.2 Acquire and invert die.
- 2.3 Retrieve inverted die, place and align face down on membrane.
- 2.4 While holding die in place, apply carrier lid and snap closed.

3.0 Test.

4.0 Burn-in.

5.0 Disassembly

- 5.1 Open carrier lid.
- 5.2 Remove die.
- 5.3 Return carrier and lid for reuse.

6.0 Place die in packaging for delivery to customer.

Advantages

- Nonscrubbing contact may minimize pad damage, as demonstrated on probe cards. This assumes excessive force is not required to overcome non-planarity.
- Contact mechanism proven at ambient conditions in probe card technology.

Disadvantages

- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- Nonscrubbing action may affect contact reliability, although fine point may offset this.
- Mechanism for maintaining die placement during assembly is not clear.
- Adhesive may be temperature sensitive.
- Frequency and method of cleaning contacts is unknown and must be compatible with adhesive. If scrubbing is required, its lifetime may be significantly impacted.

Equipment Required

Item	Cost	Throughput
Assembler/Disassembler	$100K to $500K	Unknown

Equipment Description for Automated Process

Assembler/disassembler installs die to and removes die from test socket. Die will be picked from an expanded wafer ring. The pick and place system must have two robot arms. One robot arm must acquire and rotate die, while the other arm must retrieve the die from the back side. The system would require a robot with four degrees of freedom and a vision system with pattern recognition capabilities for use in registering the die to the carrier within the needed tolerance. Vertical force sensing and control for die handling would be required. A custom end effector will be required to install and remove the test socket clamp.

Cost

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use		$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Packard Hughes has previously worked with MCC to demonstrate this carrier concept with their membrane technology.

Supplier Business Information

- Packard Hughes, Inc.
  17150 Von Karman
  Irvine, CA 92714
- Primary Business: Electrical interconnects and contactors
- Total Employees: 700 - 900
- 1992 Sales: $80M - $100M

Contact

William Crumly
PHONE: (714) 660-6914
FAX: (714) 660-5825

Supplier:	Packard Hughes	Method:	Membrane probe set	
TAG Requirements	*Specification*	*Meets TAG*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Packard Hughes	**Method:**	Membrane probe set	
TAG Requirements	*Specification*	*Meets TAG*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	26
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	26
Burn In Rules			0	
Die Temperature max	175°C	N	3	0
Ambient temperature max	150°C	N	3	0
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	19
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	169

PLASTRONICS, INC.
Wire-based Probing

General Information

Plastronics has been working with a test site to develop their wire probe KGD carriers for production use. This is a temporary carrier approach utilizing wire probes to make contact to the die bond pads for test and burn-in. The contact method uses compressed wire probes with a scrubbing action for penetrating oxides, and alignment is a manual optical process, with provisions for automation. Thermal management is provided by the carrier base, which serves as a heat spreader. Plastronics is currently in alpha test of this carrier concept, and all carriers are now machined. Production quantities would require tooling for molded components.

Technical Description

Plastronics, Inc. uses a wire based probing technology to provide contact to bare singulated die in a carrier based approach. The carrier consists of a plastic base with a cavity for the die, a ceramic alignment plate with precision laser drilled holes for aligning the wire probes to the die bond pads, and a contactor assembly which contains the probes. The compliant probes provide scrubbing contacts and the ability to accommodate non-planar surfaces. Plastronics has developed a cleaning process which may be employed to clean the probes, and claims that these carriers are good for approximately 2000 uses. Condition of the die bond pads after burn-in and test is expected to be similar to a wire probe. Laser drilling currently imposes a 10 mil pitch limitation which is reflected in this technology's inability to meet TAG requirements in this area for even low I/O die (8 mils).

Readiness Level

Readiness Category:

The Plastronics carrier is in alpha test.

Equipment status:

Loading and unloading of die is currently performed manually, under a microscope. Assembly rates are 2 to 3 die insertions/alignments per minute. No work has been done on providing automatic assembly equipment.

Process status:

The process for producing the machined version of this product is currently in place. Molded components would require tooling. The die/carrier assembly process is strictly manual at this time.

Capacity issues:

The machined version of the Plastronics carrier is viable for prototype quantities only. Producing large quantities of these carriers would require tooling molded carriers. The production ready version would replace screws with spring clips to hold the assembly together. Once the tooling was complete, quantities of carriers could be produced quickly and at a greatly reduced cost.

Qualification issues:

Plastronics and a beta test site are currently working to evaluate the carrier performance and further develop their KGD carrier product. Limited in-house testing has been performed, but no thorough evaluation of contact resistance over multiple insertions or many thermal cycles has been performed. A test plan is in place to perform this type of testing.

Alignment Method

Alignment is manual optical, with provision for automation.

Contact Mechanism

Wire probes provide scrubbing action.

Key Features

Wire probes are used with a ceramic alignment plate.

Noncompliance with Technology Assessment Guidelines

The probe based technology uses laser drilled holes which limits the pitch to 10 mils. It cannot meet the TAG guidelines for either low I/O or high I/O die (200 micron pitch/100 micron pad and 150 micron pad/75 micron pad, respectively).

The long thin probes provide an uncontrolled impedance environment.

The Plastronics technology was not penalized for die size, although there are some concerns as to how very small die might be handled and aligned. (TAG guidelines say that the technology will accommodate 50 mil die).

Process Flow Description

1.0 Begin with die on wafer tape (sawn) or in waffle pack type packaging.

2.0 Assembly

- 2.1 Place die into cavity of carrier
- 2.2 Place ceramic locator plate over die in carrier
- 2.3 Align die under the locator plate
- 2.4 Place contactor assembly over the locator plate, allowing probes to drop through holes in locator plate.
- 2.5 Clamp assembly

3.0 Disassembly

- 3.1 Remove clamp assembly
- 3.2 Remove contactor assembly
- 3.3 Remove locator plate
- 3.4 Remove die and place into packaging for delivery.

Advantages

- Piercing action may enhance contact reliability.
- Die held in place by carrier contacts during align and clamp.

Disadvantages

- Technology is pitch limited.
- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- Piercing action over temperature excursions may introduce unacceptable amounts of pad damage for final assembly application.
- Probe tips may require more maintenance than average. Cleaning may shorten life of probes.

Equipment Required

Item	Cost	Throughput
Assembly/disassembly station	Unknown	Unknown

Equipment Description for Automated Process

The pick and place system would require a robot with four degrees of freedom and a custom end effector. The system would require a vision system with pattern recognition capabilities for use in registering the die to the plastic carrier within the needed tolerance. Vertical force sensing and control for die handling would be required. The custom end effector will open and close the carrier lid.

Cost

Manufacturer provided information

- Tooling cost for each die design: $25,000.00
- Cost for each carrier: $1.00 to $1.50 per pin.

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use	Probe tips require more maintenance than average	$$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Plastronics is placing considerable importance in the scrubbing action of their probes; they believe a scrubbing contact is superior to a nonscrubbing contact. The minimum pad pitch of this approach limits the selection of die which may be used with this technology.

Supplier Business Information

- Plastronics, Inc.
  2601 Texas Drive
  Irving, TX 75062
  (214) 258-1906

- Primary Business: Plastic products
- Total Employees: 120
- 1992 Sales: $5M

Contacts

David or Wayne Pfaff
PHONE: (214) 258-1906
FAX: (214) 258-6771

Supplier:	Plastronics	Method:	Wire Probe set	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Plastronics	Method:	Wire Probe set	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	N	3	0
Min. pad dimension	100 µm	N	3	0
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	18
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	N	3	0
Min. pad dimension	75 µm	N	3	0
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	18
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	N	3	0
Min. pad dimension	100 µm	N	3	0
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	19
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	153

QUALHI CORPORATION

BTQI Carrier

General Information

Qualhi corporation is a spin-off from Consultar, Inc. which has been established specifically to provide KGD carriers based on the thick film technology developed at Consultar (Figure 20). These carriers are designated as Burn-in, Test, Quality, and Inspection (BTQI) carriers. These carriers utilize gold bumps deposited on thick film materials to make contact to the die bond pads, and scrubbing is provided by a flip chip aligner/bonder during assembly of the die into carrier. Alignment of the die to the thick film contactor assembly is performed by the flip chip aligner. Thermal management is provided by a ceramic or metal lid which serves as a heat spreader. Qualhi is currently in development of this carrier, with initial testing being performed in house and at a customer test site.

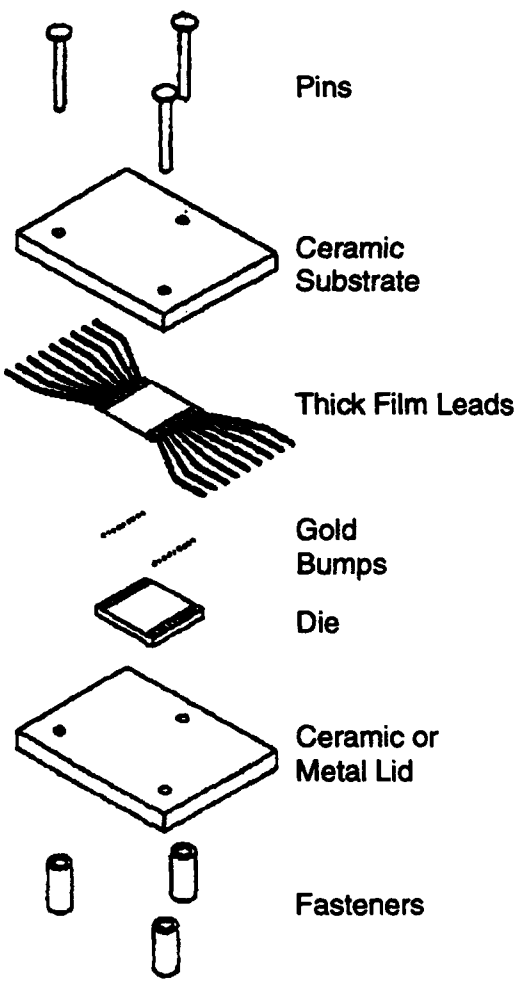

Figure 20. Exploded View of BTQI

Technical Description

The Qualhi carrier is composed of a low-cost thick film carrier with coined gold "bumps" forming die contact points. Gold ball bonds are attached to the thick film surface using standard wire bond equipment. The wires are then broken off and the remaining gold is coined to form planar die contacts. The die is placed and aligned in the carrier using a flip chip bonder, with very low force. The bonder provides sufficient scrubbing action to break through the oxide on the die pads, but low enough force to prevent bonding. The package is held together by Kovar pins, with heat shrink tubing "fasteners" applied while assembly is held in place under pressure. Work done to date indicates that the process leaves a 1 - 1.3 mil mark on the bond pad. Depth of the mark is unknown, but is targeted at 8000±4000Å. Potentially, the number of uses may be high. However, this may be adversely affected by the continual coining (and therefore, enlarging) of the carrier "bumps."

Readiness Level

Readiness Category:

This technology is in development. Testing is taking place both in-house and at a beta site.

Equipment status:

The BTQI carrier/die assembly is expected to be performed with a modified flip chip bonder used to place the die face down on the thick film carrier. At this time lid placement is performed manually, while the die is held in place with vacuum. A modification to the bonder will be required to provide automated lid placement. Semiconductor Equipment Corp. has quoted this modification at $20K, requiring 8 to 12 weeks for development and delivery.

Process status:

The die to carrier assembly process is expected to be performed by a modified flip chip bonder. This process will have to be optimized once the equipment is available. Lid placement is currently manual, but may be automated.

Capacity issues:

For the purposes of providing KGD carriers the capacity is unlimited (the thick film providers are capable of producing large quantities in quick turnaround times). The carriers may be designed and fabricated in a minimum of 3 weeks (with expedite charges) or in normal delivery times of 4 to 6 weeks.

Qualification issues:

Qualhi is currently performing testing in-house and working with a beta test site to complete qualification of the BTQI carriers. This qualification data will be made available upon request when completed.

Alignment Method

Alignment is manual optical, with provision for automation.

Contact Mechanism

Gold ball bonds on thick film interconnect provide scrubbing action with use of flip chip bonder.

Key Features

Thick film interconnect has scrubbing contacts.

Noncompliance with Technology Assessment Guidelines

The Qualhi technology uses a thick film interconnect and coined gold bumps, both of which impose certain geometric restrictions.

- No compliance built-in or provided by ceramic or gold bumps; unable to meet pad to pad variation guidelines.

It is believed that the lack of compliance is likely to cause significant pad damage on nonplanar die.

Process Flow Description

1.0 Begin with die on wafer tape (sawn) or in waffle pack type packaging.

2.0 Assembly

- 2.1 Acquire die.
- 2.2 Align and place inverted die onto base of carrier (thick film with ball bonds facing upward).
- 2.3 Use flip chip bonder to apply ultrasonic scrubbing, turn on vacuum to hold die.
- 2.4 Place ceramic or metal lid on top of die backside.
- 2.5 Assemble Kovar pins and lid clamps.

3.0 Disassembly

- 3.1 Remove fasteners by cutting tubing.
- 3.2 Remove lid.
- 3.3 Remove die and place into packaging for delivery.
- 3.4 Clean base and lid (if necessary) and return for reuse.

Advantages

- Scrubbing action may enhance contact reliability.

Disadvantages

- Technology is pitch limited, assuming thick film interconnect.
- Poor compliance will affect contact reliability to non-planar die.
- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- The amount of scrubbing required to overcome noncompliant nature of interconnect may introduce unacceptable amounts of pad damage for final assembly application.
- Number of uses without rework is likely to be low due to continued flattening and enlarging of gold carrier pads.
- Process to attach die is not yet qualified and may be difficult to optimize and control.

Equipment Required

Item	Cost	Throughput
Flip chip bonder	$200K to $300K	Unknown

Equipment Description for Automated Process

The pick and place system would require a robot with 4 degrees of freedom and a custom end effector. The system would require a vision system with pattern recognition capabilities for use in registering the die to the gold bumps within the needed tolerance. Three axis force sensing and control would be required for die handling and scrubbing . The custom end effector will open and close the carrier lid and assemble clamps. An automatic flip chip bonder has all of the required features except for the custom end effector.

Cost

Qualhi cost target for these carriers is $0.01 per lead per use.

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use	Low number of uses	$$$
Assembly, Disassembly	Potential damage	$$
MCC Cost Judgement		

Comments

The Qualhi approach to scrubbing proposes the use of a flip chip bonder to perform the scrubbing, as opposed to requiring mechanical probe action at the die site.

Supplier Business Information:

- Qualhi Corporation
  516 Country Plaza South
  Gilbert, AZ 85234
  (602) 892-6767

- Primary Business: KGD carriers
- Total Employees: 3
- 1992 Sales: $250K (Consultar)

Contact

Peter Normington
PHONE: (602) 892-6767
FAX: (602) 892-6767

Supplier:	QualHi	Method:	BTQI Carrier	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	N	2	0
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	N	3	0
Interconnect Rules Subtotal			0	4
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	QualHi	Method:	BTQI Carrier	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	26
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	26
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	25
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	170

SANDIA NATIONAL LABORATORIES

General Information

Sandia National Laboratories is developing a KGD technology based on rerouting bond pads to an area array configuration, and using Z-axis interconnect materials to provide connections to a temporary test carrier. Contact from the die area array bond pads to the carrier is provided by either a Z-axis conductive polymer, or by a particle interconnect membrane. Alignment is performed by a machined spacer component, and thermal management is provided by a lid which provides contact normal force and serves as a heat spreader. Sandia is currently in the development phase, and will seek to license a vendor for this technology at an appropriate time. As a major contributor in the Multi Chip Module development effort, Sandia National Laboratories has been working on an internal MCM project to specifically demonstrate known good die technology and module testing strategies. The MCM-D developed for this project contains four DSPs, two ASICs, and eight memory die to perform a two dimensional fast Fourier transform. All die used in this module will be repatterned and thoroughly tested and burned in before assembly. The ASICs contain boundary scan and BIST circuits to simplify module level testing and diagnosis. Data from this project, including KGD experience, will be shared with the MCM community.

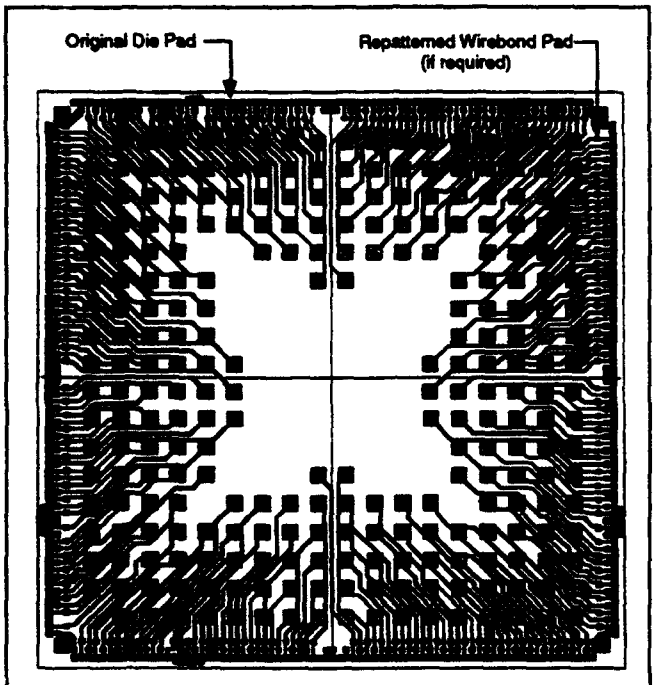

Figure 21. Repatterned LSI Logic LCA100106 Die

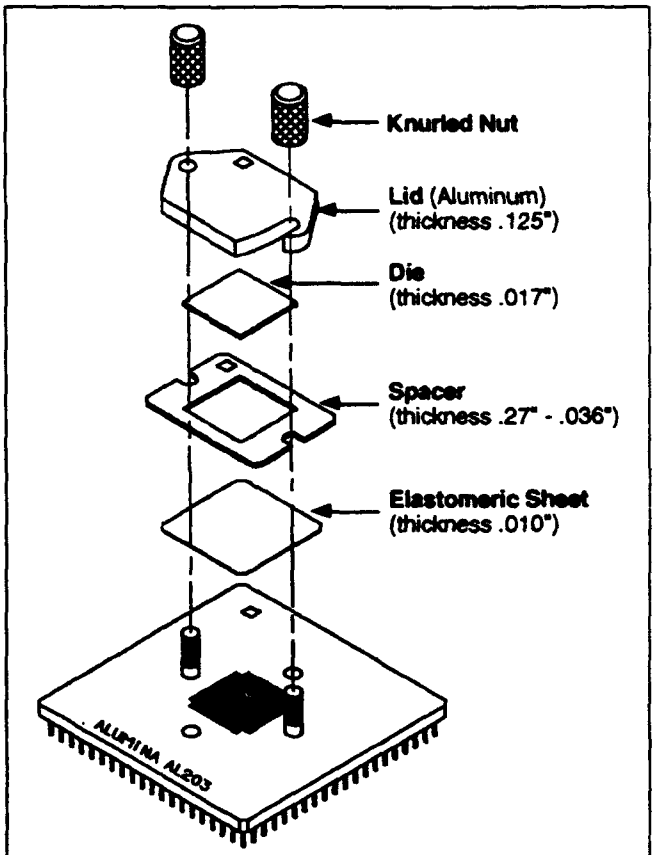

Figure 22. Universal Carrier for Repatterned Die

Technical Description

Sandia's strategy for providing KGD has three major elements: 1) die with repatterned pads, 2) universal die carriers, and 3) universal test and burn-in boards. Using two layers of polyimide/metal, wafers are processed, as shown in Figure 21, to reposition the normal peripheral bond pads of each die to an area array of much larger pads on top of the die. The array pads may be either gold or solder. The relatively large pitch of the repatterned pads allows easy mechanical alignment of the die to a corresponding pad array in a universal carrier as shown in Figure 22. The die-to-carrier interface has been successfully demonstrated with both diamond particle membranes and z-axis elastomers. The elastomer is embedded with vertical wires which allows connection between the

patterned carrier and die. Different die types and sizes are accommodated by changing only the plastic spacer. Since the carrier provides a common footprint for all die types, Sandia has designed compatible universal tester load boards and burn-in boards. The condition of the array pads after burn-in and the number of uses per interconnect (die-to-carrier interface) will depend on the materials selected. Final assembly may be flip chip, gold wire bond, or GE HDI interconnect.

Readiness Level

Readiness Category:

This technology is in development. Sandia will not enter the merchant KGD supplier market, but will seek to license the technology developed at SNL to a qualified vendor.

Equipment status:

Sandia is having the wafers repatterned at a third party MCM-D supplier, and the carrier assembly is currently a manual operation. Assembly automation would require development of an automated assembly station.

Process status:

Wafer repatterning uses standard thin film photolithography procedures, and the carrier assembly/disassembly is a simple operation.

Capacity issues:

Production capacity is dependent on resources available at licensee.

Qualification issues:

Five die types (memory, DSP, ASIC, FPGA, assembly test chip) have been repatterned with both gold and solder-bumped pad metallization. Carriers with 0.030" and 0.020" pad pitch have been tested over 4V to 6V and OC to 100C ranges and at test vector rates up to 100 MHz. Broader range characterization is underway. Burn-in boards have been procured, but no data yet.

Alignment Method

Die mechanically aligns to spacer cavity. Precise die sawing control is not required because large repatterned pads allow at least 0.004" misalignment.

Contact Mechanism

Contact to solder bumps is made either with a Z-axis elastomer sheet (from AT&T) or diamond-particle interposer (from Acsist). The membrane interposer is designed to allow at least 0.001" pad-to-pad vertical compliance. The penetrating interposer is required when testing any solder-bumped die which has a residual film of flux on the bumps. Alternatively, contact can be made to peripheral Au pads with traditional wire bond.

Key Features

Repatterned die provide an area array of pads compatible with universal, nonbonding PGA carriers. Die pad metallizations may be easily optimized for the die application; for example, solder for flip-chip attach, or gold for wire-bond or GE HDI interconnect.

Noncompliance With Technology Assessment Guidelines

The original aluminum bond pads are rerouted to solder-bumped array or Au-pad peripheral pads which limits incoming die to those with aluminum bond pads.

- Cannot accommodate incoming Au or solder bumped die; postpassivation processing, integral to technology, requires aluminum pads as initial surface.
- Additional wafer processing required (rerouting and enlargement of bond pads).

The dielectric overcoat was judged to be potentially incompatible with GaAs.

Pad rerouting uses uncontrolled impedance transmission lines. In the case where Au wire bonding is done, the ability to control impedance is further reduced.

Optical inspection of the die is inhibited by the dielectric coat.

Process Flow Description

1.0 Begin with singulated, repatterned die. Note this process requires two polyimide and two metal layers (four masks). Sandia has used third party, MCM-D suppliers for wafer processing.

2.0 Assembly

2.1 Verify that spacer corresponding to die type to be tested is positioned in carrier.

2.2 Use vacuum wand to place clean die in carrier

cavity. Use nonsymmetrical feature on die pad array to correctly orient die.

2.3 Rotate carrier lid in place and tighten knurled nuts snugly. The spacer prevents stressing the die due to over-tightening.

3.0 Treat die-in-carrier as a PGA-packaged part for electrical tests and burn-in.

4.0 Disassembly

4.1 Remove die from carrier by loosening nuts.

4.2 Swinging carrier lid aside,.

4.3 Lifting die out of cavity with vacuum wand. Place fully tested die (KGD) in waffle pack or other die transport medium.

5.0 Inspect carrier and clean or replace interposer if necessary. Gold die pads cause little change to the interposer (elastomer or particle membrane). Some residue from solder bumps, however, comes off on the interposers and must be cleaned off after tens of uses.

Advantages

- Enlargement and rerouting of the die bond pads permits mechanical align of die without precision saw of die.
- Reroute creates larger bond pads which facilitate alignment and minimize effects of pad damage.
- Piercing action may enhance contact reliability.
- Carrier lids, with or without fins, provide thermal management.

Disadvantages

- See also Noncompliance With Technology Assessment Guidelines

Concerns

- Frequency and method for cleaning contacts is unknown.
- Postpassivation wafer processing provides additional environmental protection and facilitates alignment. However, defects may be introduced and final assembly options may be limited. If preferred final assembly requires or is improved by presence of solder bumps or gold pads, then the cost of rerouting and bumping is value added.

Equipment Required

1. To repattern wafers, standard thin film photolithography and processing equipment are required, such as: spinner for polyimide and photoresist, contact mask align and exposure, oven for film cure, polyimide and metal etcher, metal sputter and plating, and wafer saw.
2. In order to automate loading and unloading the carriers, it would be necessary to fit the carrier with a snap-on lid and use a robotic system to pick and place the die.

Cost

Sandia provided the following analysis. Tooling and setup costs for die repatterning cost about $10K per wafer type. Wafer processing, including solder bumping, costs about $900 per wafer in small quantities and is estimated to drop to less than $400 per wafer in volume production. Carriers with ceramic substrates in small volume cost $500 (0.030" pad pitch) to $900 (0.020" pad pitch) each and are reusable thousands of times. Carriers with FR4 substrates in larger volumes are estimated to cost less than $200 each. Consumables (elastomer sheet or diamond particle interposer) are reusable tens of times and cost less than $1 per chip

Cost Factor	Comment	Cost
Wafer Processing	Reroute	$$$
Materials Cost/Use		$$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Sandia will make all data from the MCM project available, and will seek to license the KGD technology to a supplier.

SUPPLIER BUSINESS INFORMATION

- Sandia National Laboratories
  P.O. Box 5800
  Albuquerque, NM 87185-1073

- Primary Business: Research and development
- Total Employees:
- 1992 Sales: N/A

CONTACT

R. Keith Treece
Sandia National Labs
MCM Applications, Dept. 2277
Albuquerque, NM 87185-5800
PHONE: (505) 844-9684
FAX: (505) 844-8480

Supplier:	Sandia Laboratories	Method:	no name	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	N	1	0
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	30
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	7
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	N	3	0
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Sandia Laboratories	Method:	no name	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	24
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	24
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	25
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	N	2	0
			0	
TOTAL SCORE			0	161

TEXAS INSTRUMENTS and MICRO MODULE SYSTEMS

KGD Interconnect System

General Information

Texas Instruments (TI) and Micro Module Systems (MMS) have teamed to develop a KGD carrier which may be applied to all die types (Figure 23). MMS is providing the substrate (membrane and die pad contactor) while TI supplies the other carrier components, sockets, marketing, sales, and support services. This is a reusable temporary carrier approach, using a custom membrane with a proprietary contact mechanism to provide a piercing contact to the die bond pads. Alignment is a mechanical operation, relying on a "fence" built directly onto the membrane to locate the die. Thermal management is provided by the backside support plate, with optional heat sink attachment. TI is currently in alpha test of this KGD technology, using in house chips for testing. Carriers and sockets for low I/O components are expected to be ready by 1Q94.

Technical Description

The TI/MMS KGD interconnect system applies a copper polyimide substrate with a proprietary nonwiping bond pad contact mechanism to route electrical signals to and from the die. The die is aligned and then "sandwiched" between the substrate and a metal lid which also serves as a heat sink (additional sinking is optional). Inserts, backplates, frames and posts complete the assembly and compensate for non planarity of the die bond pads or bumps. This entire assembly then fits into standard test contactors and sockets used for test and burn-in. The preliminary test results presented so far indicate that the contact interface mechanism provides a low contact resistance (< 500 mΩ) with reasonable applied force, and is quite reliable over a large number of insertions (900). This technology offers good contact (<500 mΩ) over the entire temperature range as well. It accommodates a variety of metallurgies (including Al, Au, and Sn/Pb) in both flat and bumped configurations. The copper polyimide substrate provides a high bandwidth controlled impedance interconnect mechanism capable of very high wiring densities and either peripheral or array bond pad configurations. TI/MMS are well on the path to qualifying this technology for commercial use, with several test vehicles described in the literature and many tests already completed, and others awaiting completion.

Readiness Level

Readiness Category:

The TI/MMS carrier is in alpha test.

Equipment status:

The TI KGD carriers may be assembled using standard existing pick and place and package assembly equipment.

Process status:

The assembly process is compatible with existing equipment; no development is required.

Capacity issues:

A family of carriers and sockets has been developed, with a carrier/socket combination available for each die I/O

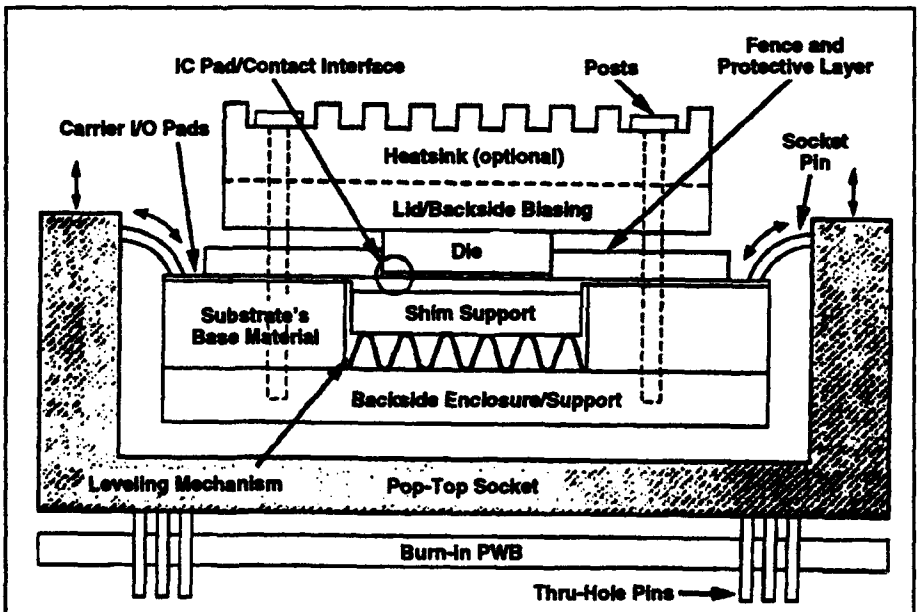

Figure 23. Cross Section of KGD Interconnect System

requirement. Carriers and sockets for 75% of the family are ready for production for I/O requirements up to 280 I/O. For higher I/O applications, the production capability will be available 12 weeks after receipt of an order.

Qualification issues:

TI will make carrier and socket qualification data available for each member of the "family." Since these carriers are intended for specific custom sockets, they are being evaluated together. The sockets have been redesigned, and limited quantities of these sockets are available at this time. Testing and verification is underway at alpha-site partners.

Alignment Method

Die alignment and/or holding features is used for mechanical die loading system. Manual optical alignment may also be used.

Contact Mechanism

Temporary contacts provide oxide piercing action.

Key Features

Copper polyimide interconnect membrane uses proprietary contact mechanism.

Noncompliance with Technology Assessment Guidelines

The current approach calls for mechanical alignment of the die which will require a high precision wafer saw process.

The TI/MMS technology was not penalized for die size, although there are some concerns as to how very small die might be handled and aligned. (TAG guidelines say that the technology will accommodate 50 mil die).

Process Flow

1.0 Begin with singulated die on tape.

1.1 Die extraction from wafer tape (removal and cleaning of the die)

2.0 Load die onto substrate.

The alignment step can be completed by either manual die placement (using vacuum wand) with mechanical guides (fence) or vision pick and placement. The fence structure is built on top of the interconnect layer which will hold the die aligned to the contact points using the die edges as its reference. This technique requires tighter wafer sawing control in semiconductor manufacturing. The fence simplifies the manual or automated pick and place operations which serve as both an alignment and environmental protection barrier.

3.0 Apply metal lid cover.

4.0 Place latch assembly onto substrate assembly to hold die in place.

5.0 Insert carrier assembly into cavity of test contactor or socket.

6.0 If required, functional test using either test contactor or socket.

7.0 Burn-in using standard socket.

8.0 Functional Test using either test contactor or socket.

9.0 Remove lid/latch assembly, place in stock for reuse.

10.0 Remove die from substrate assembly.

11.0 Clean substrate assembly, place in stock for reuse.

12.0 Visual inspection of die.

13.0 Place die in packaging for delivery.

Advantages

- Piercing action may enhance contact reliability.
- Quick mechanical align possible for precision sawn die.
- Die held in place by carrier contacts during align and clamp.
- Thermal management integral to technology.

Disadvantages

- See Noncompliance with Technology Assessment Guidelines.

Concerns

- Piercing action over temperature excursions may introduce unacceptable amounts of damage for final assembly application.
- May be complex assembly to automate.
- Full-speed test above 250Mhz may require custom

socket.

- Frequency and method for cleaning contacts is unknown.

Equipment Required

Item	Cost	Throughput
Assembler/Disassembler	$100K to $500K	>10K/month

Equipment Description for Automated Process

Assembler/disassembler installs die to and removes die from carrier. Die will be picked from an expanded wafer ring. The pick and place system must have two robot arms. One robot arm must acquire and rotate die, while the other arm must retrieve the die from the back side. The system would require a robot with four degrees of freedom and a vision system with pattern recognition capabilities and for use in registering the die to the substrate interconnect layer within the needed tolerance. Vertical force sensing and control for die handling would be required. Another end effector will be required to install and remove the carrier lid.

Cost

- Manufacturer cost projection is less than $1.00 per die

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use		$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Supplier Business Information

- Texas Instruments, Incorporated
  13500 N. Central Expressway
  Dallas, TX. 75243
  (214) 995-2011

- Primary Business: Semiconductors, related devices
- Total Employees: 60,577
- 1992 Sales: $7.4B

Contacts

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FAX: (508)699-5339

Supplier:	TI/MMS	Method:	KGD Interconnect	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	N	2	0
Wafer Mount & Saw Rules Subtotal			0	2
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	TI/MMS	Method:	KGD Interconnect	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	26
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	26
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	25
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	173

TRIBOTECH
Temporary LeadPak (T-L/P)

General Information

TRIBOTECH technology is based on a modified ceramic package, ideally the one in which the die is conventionally packaged. These packages are modified for use with the Temporary LeadPak (T-L/P) thin film and contactor to make contact between the die bond pads and a spring pin contactor to the package bond pads. The die may then be tested and burned-in, and removed as fully tested bare die. Contact to the die is a proprietary contact mechanism which is a nonscrubbing, fine point oxide piercing method. Alignment of the die in carrier to the T-L/P is a manual optical operation, with provisions for future automation. Thermal management is provided by a backside support plate, with built in heat sink for the face down version, and by a thermal transfer block in the face up version. This technology is currently in development, with some in house testing performed, but no product qualification work started.

Technical Description

TRIBOTECH modified ceramic package approach is designed to minimize retooling of test and burn-in boards, particularly in cases where this investment has already been made. The chip is interfaced using a proprietary custom contact mechanism integral to the Temporary LeadPak to bring the signals out and connect to the package bondpads, with the chip held between a heat sink and the T-L/P. Contact normal force is provided by an elastomer and support plate behind the T-L/P. The assembly is held in place by a spring clip, similar to a conventional lid seal station clip. An airtight seal is formed by an elastomer ring.. The entire process is set up to use standard ceramic packaging and handling equipment, without requiring major investment in new equipment. TRIBOTECH offers both a face up and a face down version of this technology. At a maximum force of 5 grams, SEMs of bond pads indicate negligible damage (<20μm mark).

Readiness Level

Readiness Category:

TRIBOTECH is performing in-house alpha testing.

Equipment status:

No special equipment is required for the TRIBOTECH carrier assembly. The die are aligned and placed in the carrier with a pick and place system, and the lid is placed using package "lidding" equipment.

Process status:

There is no die processing involved other than placement into the carriers. All of the equipment and processes for manufacturing the carriers is currently in place at TRIBOTECH.

Capacity issues:

After a small quantity build for qualification (100 pieces), the capability for producing carriers is greater than 1000 per week. Lead time for a new design is 12 to 16 weeks ARO. There is expected variation in cost for larger quantities.

Qualification issues:

In-house testing of carrier prototypes has been performed, but product qualification has not been started.

Alignment Method

Alignment is manual optical, with provisions for automation.

Contact Mechanism

Proprietary mechanism in T-L/P provides contact without scrub across TAG temperatures.

Key Features

Approach uses a standard (ceramic) package for each part with T-L/P interfacing the die and package bond pads. Integral heat sink provided.

Noncompliance with Technology Assessment Guidelines

The thin ribbon and pin contacts provide an uncontrolled impedance environment.

Process Flow Description

1.0 Begin with die in waffle packs, gel paks, or elastomeric dicing ring and membrane ready for die bond.

2.0 Load die, carriers, package T-L/P assembly, and spring clips into assembly station.

3.0 Manual die prealign or pattern recognition/precision station place and vacuum chuck release.

4.0 Orient and place die on carrier/package.

5.0 Use optical pattern recognition system to align T-L/P to die bond pads; bring T-L/P into contact with die and hold.

6.0 Engage spring clip while holding T-L/P firmly in place against mechanical stop.

7.0 Release tension on T-L/P, letting spring clip hold it in place.

8.0 Transport assembly to continuity check station.

9.0 Perform continuity check.

9.1 Disassemble failed assemblies for rework.

10.0 Load assembled carriers (Packages) into test and/or burn-in boards

11.0 Perform pretest, test or burn-in.

12.0 Remove packages from test or burn-in boards.

13.0 Perform additional electrical testing, as required.

14.0 Load parts into disassembly station.

15.0 Hold down T/LP firmly and remove spring clip.

16.0 Remove T-L/P with spring clip.

17.0 Remove die from carrier.

18.0 Die cleaning (optional, if thermal grease was used).

19.0 Mark and pack die for shipment.

20.0 Return carrier/package, T-L/P, and spring clip for reuse.

Advantages

- Piercing action may enhance contact reliability.
- Better than average compliance for reliable contact to nonplanar die.
- Thermal management integral to technology.
- Assembly clamping mechanism is integral to die alignment and placement so that die position is maintained during assembly and disassembly.
- Assembly provides air tight seal for protection during burn-in and test.

Disadvantages

- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- Piercing action over temperature excursions may introduce unacceptable amounts of pad damage for final assembly application.
- Probe tips may require more maintenance than average. Cleaning may shorten life of probes.
- Assembly cycle time and potential for damage to contact mechanism is uncertain. May be complex assembly to automate.

Equipment Required

Item	Cost	Throughput
Pick and Place System	$170-$350K	1-3.5K/hr

Equipment Required for Automated Process

For the face up application, the pick and place system would require a robot with four degrees of freedom and two end effectors. The system would require a vision system with pattern recognition capabilities for use in registering the die to the T-L/P within the needed tolerance. Vertical force sensing and control for die handling would be required. The lid would be sealed with a custom end effector.

Cost

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use	Probe tips require more maintenance than average	$$
Assembly, Disassembly	Cycle time and potential for damage	$$
MCC Cost Judgement		

COMMENTS

SUPPLIER BUSINESS INFORMATION

- TRIBOTECH

  Mailing address:
  P.O. Box 5030
  Wine Valley Unit
  Napa, CA 94581-0030

  Plant Address:
  100 Napa Junction Rd.
  American Canyon, CA 94588
  (707) 643-2148

- Primary Business: Machine tools and accessories
- Total Employees: 20
- 1992 Sales: $1.8M

CONTACT

Bud Cain
PHONE: (707) 643-2148
FAX: (707) 643-7942

Supplier:	Tribotech	Method:	Temporary Lead Pak	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Tribotech	**Method:**	Temporary Lead Pak	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	24
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10 W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	24
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	25
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	171

YAMAICHI ELECTRONICS, INC.

General Information

Yamaichi is developing a carrier and matching socket to address the KGD market. The carrier uses a derivative of the Nitto Denko ASMAT thin film interconnect. Contact to the die is made using the non-scrubbing, oxide piercing bumps which are an integral part of the interconnect. Signals are fanned out for socket contact by the thin film material. Alignment is a manual optical operation and thermal management occurs through an incorporated heat sink mechanism. This technology is in development, with in house testing underway. Plans call for delivery of prototypes to customer test sites by 4Q93.

Technical Description

Yamaichi Electronics has developed a carrier/socket based approach to providing known good die with future applications to wafer level test and burn-in. The carrier contains Nitto Denko ASMAT thin film interconnect to provide electrical connection between the pads on the die and the contacts on the burn-in and test socket. A mechanism within the carrier is used to align the die, interconnect, and the mechanical interface to the socket. The socket lid applies a controlled force to the die while mating it properly to the substrate. The system incorporates heat sink capability and is designed to be reusable and automatable with standard die pick and place equipment. Data from Nitto Denko indicates that the ASMAT die contact interface provides a low contact resistance (80 milliohms) at 30 grams of contact force per pin. Work by Nitto Denko indicates that damage to aluminum bond pads due to contact with the ASMAT bumps is minimal. Thermal life of the interconnect is expected to be high.

Readiness Level

Readiness Category:

This technology is in development. In-house testing and product refinement is underway, and plans for qualification at OEM beta test sites are in place. Plans call for delivery of prototypes to these sites by the end of 1993.

Equipment status:

A manual pick and place assembly workstation, with a throughput of 5 to 6 die per minute is available now, and an automatic workstation with an expected throughput of 10 to 12 die per minute is in development. Yamaichi is studying the cost effectiveness of automating this assembly vs. using manual assembly stations. If the decision to proceed with development of an

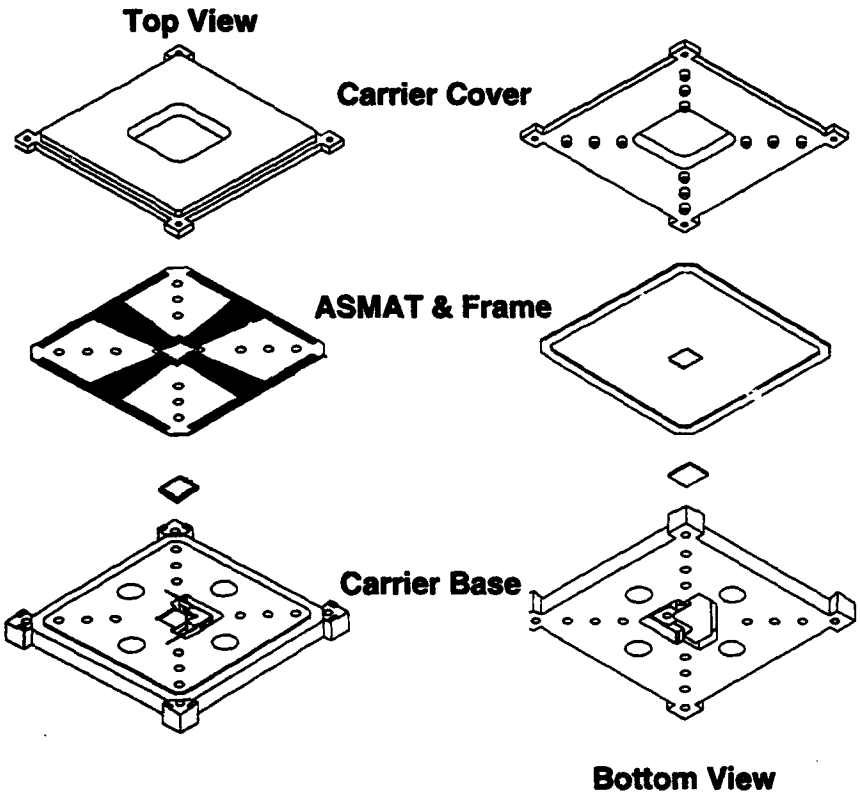


Figure 24. Exploded top and bottom views of Yamaichi chip carrier

automated station is made, it is expected to be ready in 3Q94.

Process status:

The Nitto Denko film has been characterized and is ready for use. The current assembly process for prototypes uses a single step snap carrier to place the die in alignment with the ASMAT film.

Capacity issues:

Yamaichi is not prepared for production at this time; the carrier is still in the prototype stage. The assembly process is being defined in such a way as to facilitate highly automated assembly. The intended throughput of a manual assembly station is 5 to 6 die per minute, with an automated station doubling that capacity.

Qualification issues:

In-house testing of contact resistance has been performed, but final qualification of this product has not yet begun.

Alignment Method

Die alignment and/or holding features will be used with a manual or automated optical loading system.

Contact Mechanism

Bumps in the Nitto Denko ASMAT film make contact similar to rivets (Au over Ni) by penetrating oxide without scrubbing motion.

Key Features

Simple carrier approach depends on ASMAT technology from Nitto Denko.

Noncompliance with Technology Assessment Guidelines

Die are handled and aligned with a chip holder which cannot accommodate very small die. (TAG guidelines say that the technology will accommodate 50 mil die).

Process Flow Description

NOTE: This process describes the assembly and use of a prototype carrier, and does not represent the process for the final, automatable production version.

1.0 Begin with die on wafer tape (sawn) or in waffle pack type packaging.

2.0 Assembly.

- 2.1 Open chip retainer spring on chip holder assembly.
- 2.2 Use pick and place equipment to place chip (face up) in chip holder assembly.
- 2.3 Release chip retainer spring, clamping die in place in chip holder.
- 2.4 Place ASMAT film over carrier base and chip holder (bumps down).
- 2.5 Insert chip cover through fiducials in ASMAT film, into holes in chip holder.
- 2.6 Align the ASMAT film chip carrier by optical alignment.
- 2.7 Place carrier cover on top of assembly while vacuum retention holds alignment.
- 2.8 Snap on carrier lid.

3.0 Use carrier assembly directly with sockets for test and burn-in.

4.0 Disassembly.

- 4.1 Remove carrier cover.
- 4.2 Remove film contactor.
- 4.3 Open chip retainer spring of chip holder subassembly.
- 4.4 Remove die and place in packaging for delivery.
- 4.5 Return all parts of carrier for re-use.

Advantages

- Non-scrubbing contact may minimize pad damage, assuming excessive force is not required to overcome non-planarity.
- Contact materials and mechanism has been characterized by Nitto Denko at time and temperature.

Disadvantages

- Assembly cycle time expected to be higher than average.
- See also Non-Compliance with Technology Assessment Guidelines

Concerns

- Non-scrubbing action may affect contact reliability.
- Frequency and method of cleaning contacts is unknown. If cleaning requires scrubbing,, it may significantly impact lifetime by weakening probe tip to interconnect interface.

Equipment Description for Automated Process

Fully automated system is awaiting decision on development.

Cost

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use		$
Assembly, Disassembly		$
MCC Cost Judgement		

Comments

Data has been presented which verifies low resistance contacts over a large number of thermal cycles.

Supplier Business Information

- Yamaichi
  1420 Koll Circle, Suite 3
  San Jose, CA
  (408) 452-0797
- Primary Business:
- Total Employees:
- 1992 Sales:

Contact

Bob Million
PHONE: (408) 452-0797
FAX: (408) 452-0799

Supplier:	Yamaichi	Method:	no name	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	Y	2	2
Bumped die	Accept	Y	2	2
Device Type Rules Subtotal			0	33
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	N	2	0
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	7
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	Y	2	2
Metallurgy Changes required	NO change in quality/reliability	Y	3	3
Interconnect Rules Subtotal			0	9
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Yamaichi	Method:	no name	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Low I/O Test Rules Subtotal			0	26
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	Y	2	2
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
High I/O Test Rules Subtotal			0	26
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	Y	2	2
Pad metallization accepted(Al,Au,Solder)	ALL	Y	1	1
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	Y	3	3
Burn In Rules Subtotal			0	25
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	173

Minimal Package Approaches to KGD

Hughes Aircraft

Micro SMT

Northern Telecom

Tessera

HUGHES AIRCRAFT COMPANY

Testable Ribbon Bonding (TRB)

General Information

The Hughes Testable Ribbon Bonding (TRB) technology is being developed to provide a quick turn, soft tooled alternative to traditional TAB (Figure 25). It involves using a ribbon bonder to bond leads from the die to a temporary carrier for test and burn-in, and then cutting the leads at the outer lead bond, leaving a die with ribbon bonds ready for placement and outer lead bonding. The contact mechanism is a ribbon bond, and alignment is performed by the ribbon bonder. Hughes is currently in development with this technology.

Technical Description

The Hughes Testable Ribbon Bonding (TRB™) system provides the benefits of Tape Automated Bonding (TAB) to a soft tooled environment without the disadvantages of TAB. The TRB system uses a patented lead forming tool to allow for bonding of a "ribbon" (a 1 x 3 mil gold wire) to the peripheral aluminum bond pads of a chip. The chip is bonded to a disposable carrier for test and burn-in using normal sockets and equipment, and then removed, with leads intact, for delivery. This technology provides low NRE costs, quick-turn around, and eliminates the need for expensive tooling.

Readiness Level

Readiness Category:

In development

Equipment status:

The only processing equipment that is required is a ribbon bonder system which has been fitted with a Hughes lead forming tool. The die are removed from the carrier using a laser cutting system with a pick and place machine to load the die into delivery packaging. Subsequent die handling must use automated pick and place equipment and TAB compatible outer lead bonding equipment. All of this equipment is currently commercially available.

Process status:

The only process required is the bonding and lead form, which is ready to be used.

Capacity issues:

The bonding and lead forming is a serial procedure, creating one lead at a time. The production capacity of this procedure is governed by the throughput of the ribbon bonder.

Qualification issues:

Hughes has been using prototype ICs to develop this technology for preparing KGD. The carrier qualification issues to be addressed are simply dealing with the ability to withstand high temperatures during the test and burn-in regime, since the contact mechanism is a bonded ribbon.

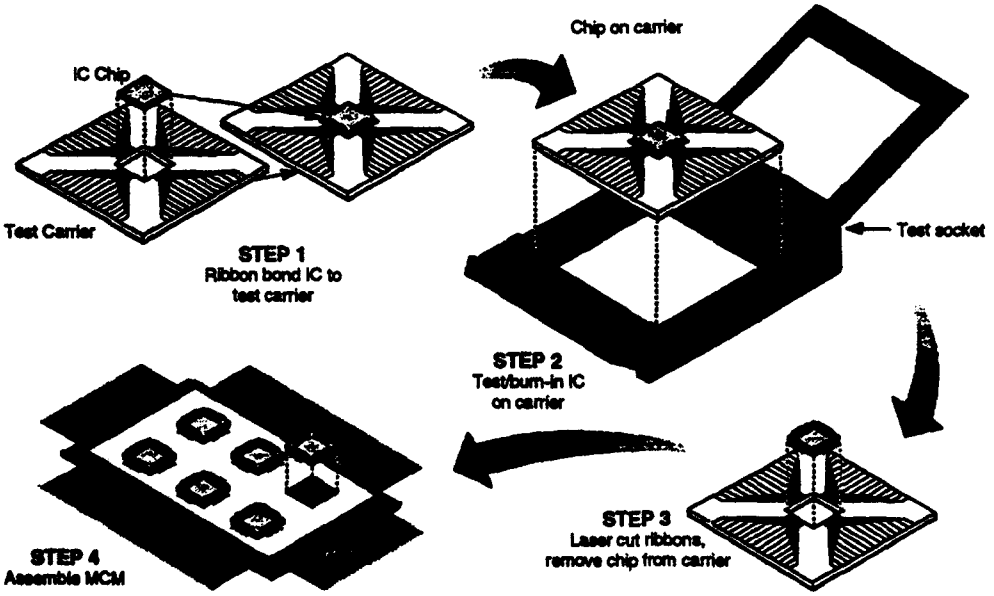


Figure 25. Testable Ribbon Bonding (TRB) Process Flow

Alignment Method

Alignment performed by ribbon bonding equipment

Contact Mechanism

TAB like ribbon bonds

Key Features

Patented lead forming tool used to create formed ribbon leads with low NRE costs and lead-time.

Noncompliance with Technology Assessment Guidelines

This is essentially a TAB based packaging technology which is limited to use with die which have peripheral, gold-bumped or Al bond pads.

- TAB approach means that die with area array pads cannot be burned-in or tested.
- Process not designed to convert from array to peripheral bond pads.
- Cannot accommodate incoming solder-bumped die; TRB process not defined for use with solder.

The TRB technology will require a pad larger than 3 mils (75 microns) due to the ribbon width.

It is assumed that the TAB-like environment will be unable to achieve 50 ohm controlled impedance.

Bonds are permanent and bond pads may not be used in future assemblies. This is counted as a significant change in the metal and limits the technology to a single touchdown.

Process Flow

1.0 Begin with bare singulated die, probe tested, on wafer tape carrier or in waffle packs.

2.0 Pick and place die onto carrier, applying vacuum to hold chip.

3.0 Use auto bonder with patented forming tool to bond and lead form gold ribbon in a single step.

4.0 Apply protective cover to carrier (optional).

5.0 Burn-in chips in carriers using conventional burn-in equipment.

6.0 Test chip in carrier using conventional test equipment and QFP handlers.

7.0 Cut ribbon leads just before OLB on carrier (use YAG laser or wire-bonder with chisel and ultrasonic).

8.0 Place leaded chips into vacuum release Gel-Paks™ for storage/shipment to customers.

9.0 Dispose of carriers (reclaim gold)

Advantages

- Permanent bond will enhance contact reliability.
- Quick turn-around, low NRE cost for small volume prototyping.
- Uses mature process technologies.
- Compatible with existing ribbon bond equipment.

Disadvantages

- Permanent bond will limit final assembly options.
- Technology is pitch limited.
- High volume will be relatively expensive due to cycle times.
- Leads are exposed and fragile after excise from carrier.
- See also Noncompliance with Technology Assessment Guidelines.

Concerns

- Minor bending will have significant impact on ease of subsequent assembly.

Equipment Required

Item	Cost	Throughput
Pick and place system	$150K	2K/hr
Ribbon bonder with lead form tool	$120K	1 wire/sec
YAG laser	$120K	≈1 inch/10 sec

Equipment Description for Automated Process

The pick and place system would require a robot with four degrees of freedom that is either fully automatic (pattern recognition), or semiautomatic (manual fiducial entry). The system would require a vision system for use in registering the die to the carrier within the needed tolerance. Vertical force sensing and control for die handling would be required. The ribbon bonder must have a heated platen and equipped with the Hughes patented lead form tool. In order to maintain correct positioning, a YAG laser is required to cut the gold ribbon from the carrier.

Cost

Cost Factor	Comment	Cost
Wafer Processing		$
Materials Cost/Use	Low number of uses	$$$
Assembly, Disassembly	Assembly increases w/I/O count; disassembly time high	$$
MCC Cost Judgement		

Comments

This technology is suitable for low volume prototype applications, due to its soft tooling approach to providing TAB like leads for either face up or face down bonding. It is less attractive for high volume applications due to the low throughput from the lead forming device. For applications planned to use TAB, this technology will allow for rapid prototypes of those systems and allows for initial production while the TAB tape is developed.

Supplier Business Information

- Hughes Aircraft Company
  7200 Hughes Terrace
  Los Angeles, CA 90045
  (310) 568-7200

- Primary Business: Aircraft, electronics
- Total Employees: 60,000
- 1992 Sales: $7.71B

Contacts

Chuck Bieber
PHONE: (512) 250-2881
FAX: (512) 250-2893

Randy Root
PHONE: (714) 759-2814
FAX: (714) 759-2868

Supplier:	Hughes	Method:	Testable Ribbon Bondin	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	29
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	N	3	0
Interconnect Rules Subtotal			0	4
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Hughes	Method:	Testable Ribbon Bondin	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
Low I/O Test Rules Subtotal			0	18
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	N	3	0
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
High I/O Test Rules Subtotal			0	15
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
Burn In Rules Subtotal			0	19
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	141

MICRO SMT/JOHNSTECH
SMT Die Package/Socket

General Information

A minimal packaging approach which encapsulates the die in micro-fabbed SMT packages and relies on fine pitch sockets from Johnstech International is proposed by Micro SMT to provide fully tested die in a small, thin, SMT style package. The Micro SMT process provides plated silicon pillars as surface mount style contacts, and the die are directly inserted into sockets from Johnstech for test and burn-in. These die may be shipped to customers for direct insertion in existing (fine pitch capable) surface mount assembly operations, and may also be re-screened in sockets at the customer site. The Johnstech socket uses a metallic contact pin with scrubbing action to make contact to the die package contacts with mechanical alignment (Figure 26). The backside of the die is used for the new contact points, and the front of the die is coated with epoxy; thermal management may be provided by an optional heat sink which is attached to a cap over the epoxy coat. Micro SMT is in development of this technology for VLSI components. It has previously been qualified for small, low pin count components. Initial packaging reliability testing of the package have been performed at a customer site. The issue of availability of suitable sockets appears to be resolved by sockets designed and fabricated by Johnstech International. That firm has indicated it's capability to fabricate both single and multiple site sockets which accommodate the Micro SMT package style.

Figure 26. Johnstech Short Contact Technology

Technical Description

Micro SMT performs additional wafer processing to create a die in a micro-fabbed package with peripheral SMT style leads fabricated directly onto the die (Figure 27). The die itself is completely encapsulated during the process. The method does not directly address the handling or test and burn-in issues which are normally a part of the KGD problem. The process instead ruggedizes the chips by packaging them in a micro fabricated SMT style format, so they can be handled effectively in a production environment. The process provides a hard contact surface that can be probed without significant damage and maintains tight planarity. Micro SMT has received assurances from equipment suppliers that standard SMT equipment for handling, test, and burn in can and will be scaled down to accommodate the new package type.

The acceptable wafer finishes would include Nitride or other material that acts as a good moisture barrier. The epoxy overcoat material applied to the wafer surface is the same used in TAB. A cap is then applied over the epoxy to further protect the die. No bond pads are required. Vias are required on a minimum pitch of 2 mil

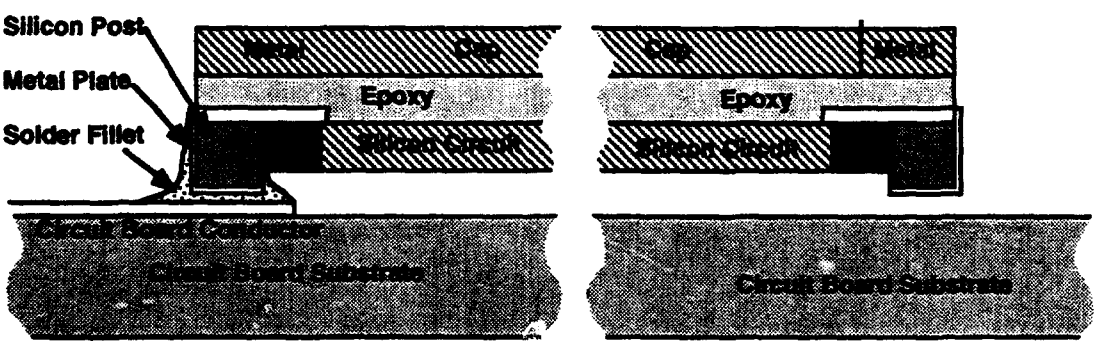


Figure 27. Micro SMT Package

and can be located anywhere on the die.

After the die are processed and separated, they are ready for insertion into the Johnstech sockets for test and burn-in and delivery as fully tested, packaged components. These components are then ready for direct insertion in a fine pitch surface mount board assembly process.

Readiness Level

Readiness Category:

In development; samples of both die and sockets have been delivered to customers.

Equipment Status:

Micro SMT is prepared to produce prototype quantities of Micro SMT packaged VLSI components, but is not yet capable of large production quantities. Equipment is currently in place for 3 inch diameter wafers, and plans are to expand the line capability to 4 inch by January 1994. Larger wafers must be sectioned for processing with existing equipment, which limits production volumes. Plans for volume production of larger wafers (4", 5", 6") call for that equipment to be in place in 1994.

Johnstech is prepared to produce prototype quantities of machined sockets, both for single site and multiple site configurations, but production quantities would require tooling of molded socket components.

Process Status:

The wafer processing steps have been completely developed. Once the die are "packaged" in the Micro SMT format, they may be handled in a manner identical to existing packaged parts, using the Johnstech sockets for test and burn-in. The parts would then be mounted on printed circuit boards using an advanced SMT process (current SMT placement equipment considers 12 mils as "fine pitch.")

Capacity Issues:

Equipment limitations restrict production of Micro SMT parts to 50 wafers per day, independent of how many die are on the wafer. If large wafers must be sectioned, each section must be treated as a wafer.

Qualification Issues:

The Micro SMT packaging format presents a host of issues for product qualification, including reliability without hermeticity. Limited evaluations have been performed at customer sites, but no definite qualification testing or burn-in yield comparisons have been performed to qualify this product for VLSI applications. The discrete applications have been qualified to Mil-Std-883 level B by several customers since 1990.

Sockets from Johnstech have been tested for continuity and contact resistance, and the materials have been selected for use in high temperature environments. Evaluations for specific designs of the MicroSMT VLSI sockets have not yet been performed.

Alignment Method

Reticle alignment in photolithography system for the Micro SMT fabrication process. Alignment of the Micro SMT packaged components in the Johnstech sockets is mechanical.

Contact Mechanism

Plated Metallization to die bond pads creates new, enlarged contact surfaces of "hard" metallization for contact in the sockets.

Key Features

The Micro SMT process creates a very small SMT package for any individual integrated circuit die. The Johnstech sockets provide reliable, high performance sockets for use with the micro packaged die.

Noncompliance with Technology Assessment Guidelines

This is essentially a packaging technology. Much of the Technology Assessment Guidelines does not apply.

Process Flow Description

1.0 Begin with Bare Finished Wafer

2.0 Micro SMT packaging process:

- 2.1 Remove oxide and epitaxial silicon from wafer scribe area.
- 2.2 Form metal connections in scribe line.
- 2.3 Scribe line etch to create Si pillars.
- 2.4 Epoxy coat top side of wafer.
- 2.5 Thinning.
- 2.6 Wafer Marking to identify die.

2.7 Isolated contact deposition

2.8 Deposit barrier and finishing metals

2.9 Wafer sort test

2.10 Wafer saw

2.11 Placement in temporary packaging or handling trays.

3.0 Remove parts from handling tray, place into burn-in sockets.

4.0 Place in oven(s) and perform burn-in.

5.0 Remove from burn-in board sockets, place into tester socket & test.

6.0 Placement in delivery carriers/tape load

Advantages

- Permanent bond will enhance contact reliability.
- Minimal package provides added protection against handling and environmental damage.

Disadvantages

- Permanent bond will limit final assembly options.
- Additional wafer processing will significantly increase wafer fabrication costs, and introduce defects.
- Wafer scribe streets are not available for test structures.
- Technology is pitch limited.

Concerns

- Minimal packaging does not fit intent of known good die.
- SMT processes may not be able to accommodate the most aggressive geometries on these packages.
- The Micro SMT process is quite different from standard processes; optimization and qualification are expected to be issues.
- Process may require wider than desired scribe streets which may limit the total number of die per wafer.

Equipment Description for Automated Process

The wafer processing for creating SMT style leads requires standard thin film and photolithographic equipment. To coat the top side of the wafer, an epoxy dispenser with a three axis positioner with a positive displacement pump would be desirable. The wafer saw station consists of a wafer mounter, wafer saw, and wafer cleaner.

Equipment Required

Item	Cost	Throughput
Barrier coat system	$700K	
Photo lithography station	$875K	
Etch system	$50K	
Furnace	$50K	
Metallization (sputter)	$1M	
Resist strip system	$50K	
Epoxy dispenser	$75K	
Wafer saw station	$50K	10 wafers/hr.

Comments

This approach to KGD seems best suited to extending existing surface mount assembly operations to their physical limitations. The very fine pitch requirement implies that the user of this technology employ "state of the art" SMT part alignment and placement equipment to obtain the benefits of this technology.

Supplier Business Information

- Micro SMT, Inc./M-Pulse
  576 Charcot Avenue
  San Jose, CA 95131
  (408) 432-1480
- Primary Business: Semiconductors
- Total Employees: 30
- 1992 Sales: $2.5M

Contact

Don Richmond
PHONE: (408) 432-1480
FAX: (408) 432-3440

Additional Supplier Business Information

- Johnstech Int'l.
  2800 Anthony Lane NE
  Minneapolis, MN 55418
  (612) 927-0485
- Primary Business: Short contact high-performance test sockets

Contact

David L. Senum
PHONE: (612) 927-0485
FAX: (612) 781-2584

NORTHERN TELECOM

Frame Automated Wire-bonding

General Information

Frame Automated Wire-bonding (FAW) is a KGD method which minimizes the resources required to achieve IC testability by maximizing utilization of existing resources. This technology was recently described in a presentation to the International Electronics Packaging Society[1]. The FAW approach is a carrier based approach which wire-bonds the die into a temporary carrier for test and burn-in (Figure 28), then—after the die has been shipped in the temporary carrier—cuts the wire-bonds (Figure 29), providing a fully tested die with wire-bonds already attached to the bond pads. The die may then be placed and outer lead bonded using the existing leads (Figure 30). The contact mechanism is a wire-bond, alignment is a function of the wire-bonder, and thermal management is performed by the carrier and the temporary die attach material. This technology is not currently in use, but is available for use, and little development effort would be required to bring it into production.

Technical Description

Simplicity of operations and use of common wire-bonding equipment, reusability, and use of existing test and burn-in resources are key points in the Northern Telecom Frame Automated Wire-bonding KGD method. Five key concepts together comprise the elements of this system:

- Reuseable, standardized family of temporary test carriers
- Use of existing automatic handling systems and standard test/burn-in sockets.
- The use of a wire-bonder as a multiaxis, pattern recognition assisted, programmable machine tool to consistently make and cut the short, low-profile wire-bonds which connect the IC to the test carrier.
- The use of a wirebonder to "skive off" the wire-bond stubs from the test carriers so that the carriers may be reused (Figure 31).
- The use of single point wirebonding to perform final IC attach to substrate in face up or face down configuration.

This KGD approach involves wire-bonding die into low-cost temporary test carriers (these carriers may be made in many configurations, but either FR4 or ceramic seem the most applicable) for test and burn-in, then cutting the wire leads, leaving a die with wires bonded to each pad. The die may then be placed onto a substrate in either a face up or face down configuration, and a single point wire-bonder is then used to bond the end of each wire to the substrate. The figures provided show the die being placed in recesses on both the carrier and the substrate, but this is not necessary for all applications. Die attach to the substrate is left as an open choice for the end

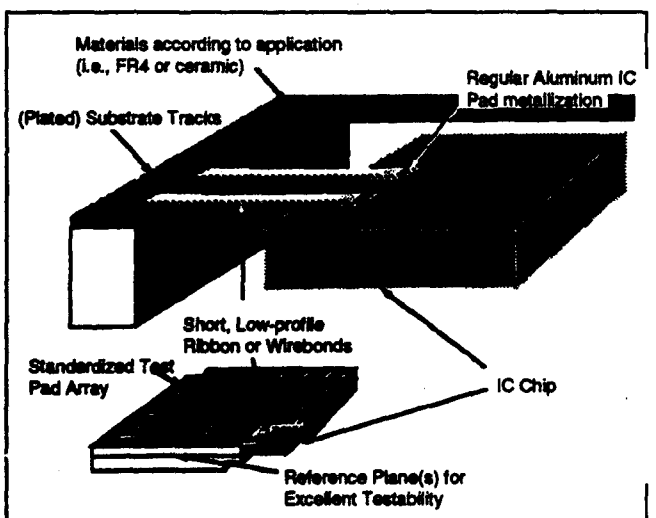
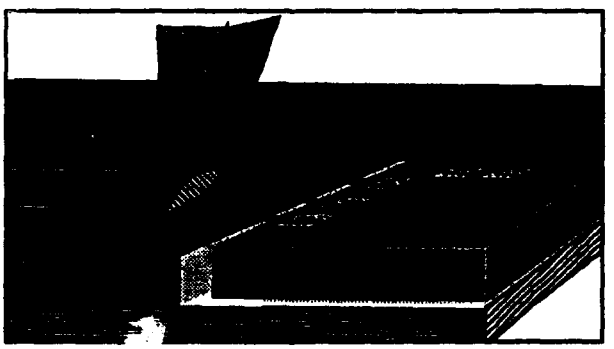


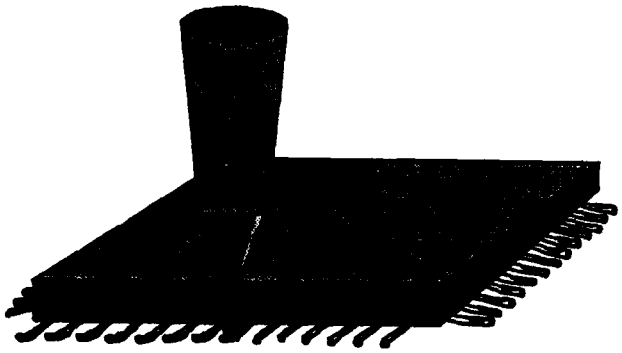
Figure 28. IC is wirebonded into carrier, which also serves as the shipping container.



Use auto wirebonder as programmable machine tool.
Z-axis cut and short leads obviate bent lead problems.
Gang tool to cut several/many leads simultaneously?

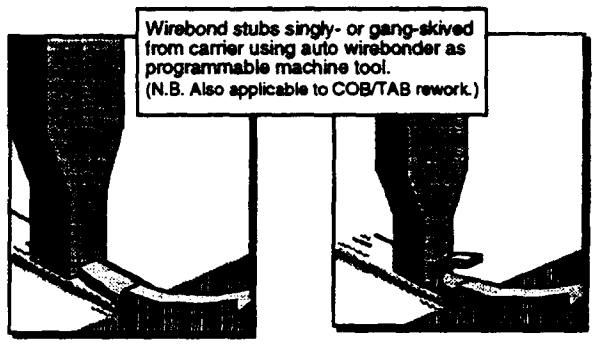
Figure 29. Chip is removed by cutting wires

[1] *"Frame Automated Wire-bonding: A TAB equivalent for multichip module assembly", John C. Walker, Proceedings of the IEPS 1992, pp. 389*



N.B. Fine-Pitch and Coplanarity not an Issue.

Figure 30. Single point bonding for final IC attach



Carriers Recycled for Multiple Use
(Augurs for Standard Carriers plus deposit to Promote Carrier Recycling)

Figure 31. Carriers may be recycled

user to select. A number of choices are available from using vacuum hold-down to reworkable polymers and thermo plastics. Thermal management is the key factor in this selection, and also is a driver in the design of the test carrier.

Readiness Level

Readiness Category:

Ready for production, but not currently in use.

Equipment Status:

All equipment required is common wirebonding and handling equipment.

Process Status:

Wire-bond processes are fully established and qualified at all major IC vendors; wire cutting is done with wire-bonder also, using a chisel point head and z-axis cutting motion.

Capacity issues:

Throughput is a function of wire-bonder activity; the bonder must be used to bond ICs into the test carriers, to cut the leads after test and burn-in, and to rebond the wires in the final application.

Qualification issues:

Although wire-bonding processes are routinely qualified at most IC vendors, this particular procedure for KGD has not been qualified. This method is not currently in use by Northern Telecom.

Alignment Method

The wire-bonder performs alignment with automatic optical system.

Contact Mechanism

Wire-bond

Key Features

Low cost of entry, exclusive use of wire-bonding equipment and processes, and low-cost temporary test carriers.

Noncompliance with Technology Assessment Guidelines

This is essentially a wire-bond based packaging technology which is limited to use with die which have peripheral, Au or Al bond pads.

- Wire bond approach means that die with area array pads cannot be burned-in or tested.
- Process not designed to convert from array to peripheral bond pads.
- Cannot accommodate incoming solder-bumped die; process not defined for use with solder.

Wire bonding is an uncontrolled impedance environment. However, it should be noted that wires used in this method are extremely short, minimizing the unshielded electrical path.

Bonds are permanent and bond pads may not be used in future assemblies. This is counted as a significant

change in the metal and limits the technology to a single touchdown.

Process Flow Description

1.0 Begin with die (sawn) on wafer tape or in waffle packs

2.0 Pick and place die into carrier recess (die attach?)

3.0 Optically reference die in carrier

4.0 Sequentially wire-bond each bond pad to carrier pad.

5.0 Apply protective cover or encapsulation to carrier (optional)

6.0 Follow normal test and burn-in procedures

7.0 Ship IC in temporary test carrier

8.0 Optically reference die in carrier (using wire-bonder)

9.0 Sequentially cut each wire-bond lead

10.0 Remove die from carrier, place into final assembly location, and use single point bond attach.

11.0 Either by using a second bonder or by replacing head in original, "skive off" the wire-bonds from the carrier bond pads to prepare the carrier for reuse. This step is accomplished by setting the bonder head flat against or close to the substrate surface and using a horizontal motion to shave the excess metal away from the surface.

12.0 Return carriers for reuse.

Advantages

- Permanent bond will enhance contact reliability.
- Quick turn-around, low NRE cost for small volume prototyping.
- Uses mature process technologies.
- Compatible with existing wire bond equipment.
- Face down bonding allows uniform ground plane placement

Disadvantages

- Permanent bond will limit final assembly options.
- High volume will be relatively expensive due to cycle times.
- Wires are exposed and fragile after excise from carrier

- See also Noncompliance to Technology Assessment Guidelines.

Concerns

- Minor bending will have significant impact on ease of subsequent assembly; wires will be difficult to keep in position as and after they are cut from carrier.

Equipment Required

- Pick and place system
- Automatic or semiautomatic wirebonder

Cost

Cost modeling performed by Northern Telecom indicates that frame wire-bonding offers at least cost parity with PLCC packaging with equivalent levels of test and burn-in.

Comments

This is one of the approaches which offers a method for IC vendors to enter the KGD marketplace without having to invest significant resources to do so. It leaves wire-bonds on the die, which dictates the nature of subsequent processing and module bond configurations.

Supplier Business Information

- Northern Telecom
  P.O. Box 3511 Station C
  Ottawa, Ontario
  Canada K1Y4H7

- Primary Business: Telecommunications
- Number of Employees:
- 1992 sales:

Contact

John C. Walker
Northern Telecom
Ottawa, Canada
PHONE: (613) 763-5201
FAX: (613) 763-5692

Supplier:	Northern Telecom	Method:	Frame Automated Wire	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Device Type Rules			0	
BiPolar	Accept	Y	2	2
CMOS	Accept	Y	3	3
BICMOS	Accept	Y	2	2
Si On Insulator	Accept	Y	1	1
GaAs	Accept	Y	1	1
Analog	Accept	Y	2	2
Digital	Accept	Y	2	2
Mixed	Accept	Y	2	2
Memories	Accept	Y	2	2
MPUs	Accept	Y	2	2
DSPs	Accept	Y	2	2
Logic	Accept	Y	2	2
Gate Arrays	Accept	Y	2	2
ASICs	Accept	Y	2	2
Peripheral bond pads	Accept	Y	2	2
Array pads	Accept	N	2	0
Bumped die	Accept	N	2	0
Device Type Rules Subtotal			0	29
Wafer/Die Size Rules			0	
Size	2.5K-500K mil2	Y	2	2
max. aspect ratio	3 to 1	Y	1	1
min. size tolerance	±0.5 mils or larger	Y	2	2
die thickness	10 - 30 mils	Y	2	2
min. thickness tolerance	±1.0 mils	Y	2	2
Wafer/Die Size Rules Subtotal			0	9
Interconnect Rules			0	
Planarity: Pad to pad height variation	up to 1.0µm variation	Y	2	2
IC Pad planarity	NO planarity degradation of die	Y	2	2
Metallurgy accepted	Al, Au, Solder	N	2	0
Metallurgy Changes required	NO change in quality/reliability	N	3	0
Interconnect Rules Subtotal			0	4
Device Design Rules			0	
Change or impact required	NO change	Y	3	3
			0	
Wafer Fabrication Rules			0	
Change or Impact Required	NO change	Y	3	3
			0	
Wafer / Die Probe Rules			0	
Does NOT Prohibit Use of wafer probe	Wafer probing OK	Y	3	3
New capital equipment required by fab	NO new equipment req'd	Y	2	2
Probe contact to passivation	NO probe contact	Y	3	3
Acceptable probe pad damage	per Mil spec 2010.6	Y	3	3
Wafer/Die Probe Rules Subtotal			0	11
Wafer Mount and Saw Rules			0	
Impact on current practices	NO change to practices	Y	2	2
Accuracy required for edge placement of di	Does NOT require +/- 0.5 mils	Y	2	2
Wafer Mount & Saw Rules Subtotal			0	4
Test & Burn In - General Rules			0	
BIST Capable	YES	Y	3	3
Basic function test	YES	Y	3	3
simulation/connection	YES	Y	3	3

Supplier:	Northern Telecom	Method:	Frame Automated Wire	
TAG Requirements	*Specification*	*Meets TAG?*	*Weight*	*Score*
Rc compatible w/ bandwidth	YES	Y	3	3
Backside electrical connection	YES	Y	3	3
Pin 1 Identifier provided	YES	Y	3	3
Contact passivaion wells up to 1.5 µm	YES	Y	3	3
Contact passivaion wells up to 8.0 µm	YES		2	0
Test & Burn In - General Rules Subtotal			0	21
Low I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	3W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
Low I/O Test Rules Subtotal			0	18
High I/O Test Rules			0	
Carrier Operation Temperature	0-125°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq	100 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	150µm	Y	3	3
Min. pad dimension	75 µm	Y	3	3
Char. Impedance	50Ω ±10%	N	2	0
Bandwidth	500 MHz	Y	2	2
Power handling capacity	10W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
High I/O Test Rules Subtotal			0	18
Burn In Rules			0	
Die Temperature max	175°C	Y	3	3
Ambient temperature max	150°C	Y	3	3
Contact Resistance	≤ 0.5 Ω	Y	3	3
Min. Clock Freq.	20 MHz	Y	2	2
Pad contact (Peripheral, array, both)	Both	N	2	0
Pad metallization accepted(Al,Au,Solder)	ALL	N	1	0
Min. pitch	200µm	Y	3	3
Min. pad dimension	100 µm	Y	3	3
Power handling capacity	3 W/cm2 - 10W/cm2	Y	2	2
Min. number of touchdowns / die	2	N	3	0
Burn In Rules Subtotal			0	19
Pack & Ship Rules			0	
per JEDEC KGD specification	YES	Y	3	3
			0	
Inspection			0	
Allow optical inspection of device	YES	Y	2	2
			0	
TOTAL SCORE			0	144

TESSERA ASSOCIATES
Compliant Chip

General Information

Tessera Associates is currently developing a KGD technology known as the Tessera Compliant Chip (TCC). This is a minimal packaging approach based on bonding a thin film rerouting layer to the chip bond pads, which provides area array contacts to the die bond pads, with a compliant elastomer "sandwiched" between the chip face and the thin film (Figures 32 & 33). These die may then be placed face down against a PGA style carrier and secured with a clamp/support plate, which also serves as a heat spreader. Contact to the die is a bond similar to a TAB inner lead bond, and contact to the carrier is a Nickel/Gold bump interfaced to a gold pad on the carrier. Alignment is mechanical, and thermal management is provided by the clamp/support plate. This technology is in development, with prototypes having been demonstrated. Product qualification is planned for 2Q94.

Technical Description

The TCC technology is a micro packaged die with a ball grid array interface to the next level interconnect. No after-fab wafer-processing is required. The TCC approach uses flex circuitry to route the electrical signal path from center or peripheral die bond pads to an array of nickel/gold bumps. The flex is attached to the die with an elastomer layer which also provides compliancy for the bump normal force in a carrier. Bond pad leads fabricated on the flex circuit are bonded to the die bond pads in a process similar to TAB inner lead bonding. The chip backside is completely available for thermal management, and the flex circuit interfaces the IC to substrate, with the elastomer providing a thermal insulator between.

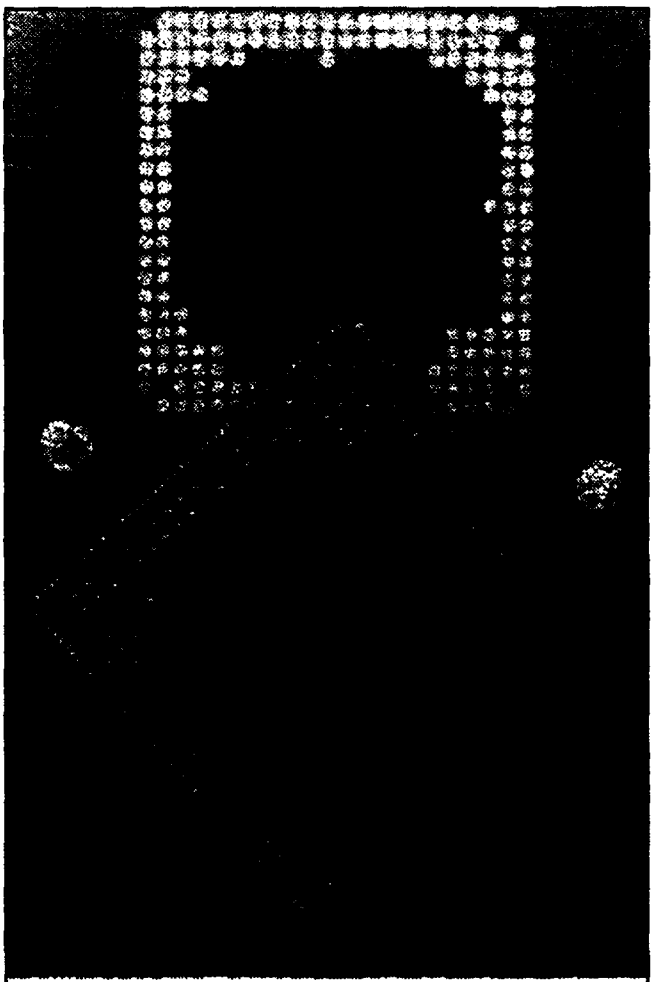


Figure 33. Tessera Compliant Chip

The leads of the flex circuit which are bonded to the die pads are allowed to bend, absorbing the expansion and contraction of the IC through thermal excursions, while the flex is interfaced to substrate through the nickel/gold bumps. The flex circuit is expected to absorb any expansion or contraction of the substrate. A PGA style carrier has been developed for test and burn-in of ICs with the nickel/gold bumps on flex interfacing to gold plated bond pads on the socket, and the elastomer providing the compliance and normal force.

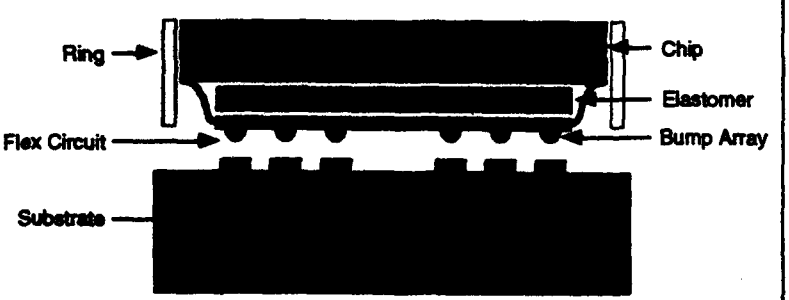


Figure 32. Generalized TCC Cross Section

Readiness Level

Readiness Category:

In development.

Equipment Status:

All equipment required for the TCC die micro packaging is now in place at Tessera, and certain pieces of this equipment are being optimized for production throughput increases.

Process Status:

The TCC uses flex circuit to route signals to ball grid array. Bonding processes similar to TAB inner lead bonding processes to create the micro packaged die. KGD carrier assembly/disassembly is currently a manual operation.

Capacity issues:

Tessera is currently producing about 50 parts per week at their facility, and plans to continue to use their own facilities (a 30,000 sq. ft. fab facility has been established which is now operational) for prototypes and early build requirements. Volume production of TCC micro packaged die would be licensed to a volume manufacturer.

Qualification issues:

Preliminary reliability testing has already been performed with good results (this information has been published by Tessera), and a full qualification plan is in place. The parts build for the qualification work is currently underway.

Alignment Method

The flex circuit reroutes the die bond pads to bump arrays on 0.5 mm to 1.25 mm pitches, which is easily aligned using mechanical placement mechanisms.

Contact Mechanism

Pressure contacts of nickel/gold TCC bumps on gold plated pads of PGA style carrier.

Noncompliance with Technology Assessment Guidelines

This is essentially a packaging technology. Much of the *Technology Assessment Guidelines* does not apply.

Process Flow Description

1.0 Begin with die sawn on wafer tape, or in waffle packs.

2.0 Fabricate the BGA flex tape.

3.0 Die is micro packaged in TCC format

- 3.1 Apply elastomer to tape
- 3.2 Bond tape to die
- 3.3 Encapsulate bonds
- 3.4 Attach ring if used

4.0 Place die into PGA carrier (alignment is by placement in spring-locked chip well or by pin alignment to ring)

5.0 Secure with clamp support plate.

6.0 Test as a PGA packaged component.

7.0 Burn-in as a PGA packaged component.

8.0 Remove TCC from carrier and place in packaging for delivery.

Advantages

- Permanent bond will enhance contact reliability.
- Minimal package provides added protection against handling and environmental damage.
- Interconnect leads are very short.
- Test contacts have relaxed pitch and increased compliancy and durability.

Disadvantages

- Permanent bond will limit final assembly options.

Concerns

Equipment Required

Once the die are micro packaged in the TCC format, the only equipment required is to support standard test and burn-in socket sites for PGA style packages. Assembly and disassembly of die into the PGA style carriers is a manual operation. Subsequent handling of the PGA carriers for loading into test sockets or burn-in boards may either be performed manually or with automated equipment.

Cost

Tessera is attempting to position the costing for TCC micro packaged die at parity with PQFP packaged die, given equivalent pin counts and equivalent levels of test and burn-in.

Comments

Supplier Business Information

- Tessera Associates
  3099 Orchard Drive
  San Jose, CA 95134
  PHONE: (408) 894 - 0700

- Primary Business: Compliant chip MCM technology
- Number of Employees: 18
- 1992 Sales: $3.5M financing

Contacts

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7.0 Conclusion

PHASE I TECHNOLOGY ASSESSMENT CONCLUSIONS

Section I of this report contains the assessments performed at MCC for the first phase of the Consortia for KGD contract. The phase I assessments focused on technologies which are being developed for single die test and burn-in, and which take advantage of the existing packaged part test and burn-in methods, equipment and strategies.

Soft Connection Methods

These methods of test and burn-in are the most mature, being the only methods being used today to actually product KGD. The R3 (reduced radius removal) KGD technology is the only technology which was identified as producing an appreciable volume of KGD into products. In general, the soft connection mehtods seem to be most suitable for low volume, cost tolerant applications. Some of the soft connection methods may require a particular final assembly method (such as C4 flip-chip for the IBM R3 technology).

Temporary Contact Methods

The temporary contact methods for KGD are the preferred (by TAG) KGD methods , and these technologies are attracting the most interest in the industry. They are, in general, less mature and most approaches have only recently begun to show promise. Contact to aluminum pads and the capability for contacting array pads seem to be critical requirements for the industry, again as spelled out by the TAG. These methods require no post processing to the wafer, which is also seen as critical for widespread applicability of the methods. The cost of these carriers is driven by the number of reuses possible, and die load/unload methods are not as cost sensitive as was originally believed.

Minimal Package Methods

For our phase I assessments, a number of technologies which were termed minimal package mehtods of producing Known Good Die were identified. Less attention was focused on these technologies because they are essentially packaging technologies which enhance the capability for doing test and burn-in. These technologies require the use of certain final assembly technologies.

PHASE I DELIVERABLES

The conclusion of phase I brings to closure a number of tasks which were undertaken by MCC and jointly by MCC and the task group of industry representatives.

This section (section I) of the report has been devoted the technical assessment of KGD technologies for test and burn-in of bare or minimally packaged die. The technical assessments were the culmination of much of the work in phase I.

The TAB and Flip Chip addenda to *Standard for Known Good Die* were developed by the industry task group and submitted to JEDEC for standardization. These documents are contained in section 4 of this report. These documents extend the original *Standard for Known Good Die* to encompass procurement standards for TAB and Flip Chip die.

The major task completed by the industry task group was development of the *Technology Assessment Guideline for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product* which is referred in this report as the *Technology Assessment Guidelines* or TAG. These guidelines were developed by the KGD task group as the industry consensus document to be used for the assessment of the various KGD technologies. We have added test methods to the guidelines which will enable 'hands-on' evaluations of various technologies to be done uniformly. We plan to use the TAG to guide the phase II evaluations and to make recommendations on updating the TAG after the evaluations are complete. The latest revision of the TAG is contained in section 3 of this report.

The cost model which was developed in phase I was used primarily to assess the cost of using KGD carriers vs costs of doing test and burn-in on packaged parts. The model is also capable of assessing the level of True Good Die at certain stages of assembly, test and burn-in which will enable a cost trade-off analysis for different test strategies in the phase II work.

Finally, we have worked with a subcommittee of the industry task group to define the evaluation and qualification testing to be done in phase II. We expect to continue to work with this group as a steering committee for phase II for the duration of the contract. The overview of the phase II work is contained in this report as section II.

TAG SCORE SUMMARY

Table 12 is a summary of each section of the TAG for each technology assessed. This summary is based on the weights recommended by the TAG subcommittee and used for the phase I assessments by MCC. To understand what different weighting schemes would do the relative scores, we have developed a series of Exel spreadsheets in which the assigned weights can easily be changed. Several examples are given in the tables that follow.

Table 14 Tag Score Summary (Task Group Weights)

Company	Device Type	Wafer/ Die size	Inter connect	Device Design	Wafer Fab	Probe	Mount & Saw	Test & Burn In- Genera	Low I/O Test	High I/O Test	Burn In	Pack & Ship	Inspect	Total
Perfect	33	9	9	3	3	11	4	21	26	26	25	3	2	175
Acsist	33	9	9	3	3	11	4	21	26	20	25	3	2	169
AEHR	33	9	9	3	3	11	2	21	26	26	25	3	2	173
California Contacts	31	9	9	3	3	11	2	21	24	18	23	3	2	159
Chip Supply	29	9	7	3	0	11	4	21	21	21	22	3	2	153
ELMO	28	9	4	3	0	11	4	21	21	21	22	3	0	147
Fresh Quest	31	9	9	3	3	11	2	21	24	24	23	3	2	165
GE HDI	28	9	4	3	3	11	4	21	21	21	22	3	0	150
Hughes TRB	29	9	4	3	3	11	4	21	18	15	19	3	2	141
IBM Dendrites	31	9	7	3	0	11	4	21	25	25	24	3	2	165
IBM R3	31	7	7	3	0	11	4	21	25	25	24	3	2	163
MCC	31	9	9	3	3	11	4	21	22	22	23	3	2	163
MCNC	31	9	4	3	0	11	4	21	25	25	24	3	2	162
Micron KGD+	33	9	9	3	3	11	4	21	24	24	25	3	2	171
Micron Softool	29	9	4	3	3	11	4	21	18	18	19	3	2	144
Northern Telecom	29	9	4	3	3	11	4	21	18	18	19	3	2	144
Packard Hughes	33	9	9	3	3	11	4	21	26	26	19	3	2	169
Plastronics	33	9	9	3	3	11	4	21	18	18	19	3	2	153
Qualhi	33	9	4	3	3	11	4	21	26	26	25	3	2	170
Sandia	30	9	7	3	0	11	4	21	24	24	25	3	0	161
TI/MMS	33	9	9	3	3	11	2	21	26	26	25	3	2	173
Tribotech	33	9	9	3	3	11	4	21	24	24	25	3	2	171
Yamaichi	33	7	9	3	3	11	4	21	26	26	25	3	2	173
Average	30.9	8.8	6.8	3.0	2.1	10.9	3.5	21.0	22.7	21.3	22.5	3.0	1.6	160.9
S.D.	2.0	0.6	2.3	0.0	1.4	0.6	1.1	0.0	3.2	3.9	2.5	0.0	0.8	10.5

Company	Device Type	Wafer/ Die size	Inter connect	Device Design	Wafer Fab	Probe	Mount & Saw	Test & Burn In- Genera	Low I/O Test	High I/O Test	Burn In	Pack & Ship	Inspect	Total
Perfect	9	9	7	3	3	11	4	6	9	0	14	3	2	80
Acsist	9	9	7	3	3	11	4	6	9	0	14	3	2	80
AEHR	9	9	7	3	3	11	2	6	9	0	14	3	2	78
California Contacts	9	9	7	3	3	11	2	6	9	0	14	3	2	78
Chip Supply	9	9	7	3	0	11	4	6	9	0	14	3	2	77
ELMO	9	9	4	3	0	11	4	6	9	0	14	3	0	72
Fresh Quest	9	9	7	3	3	11	2	6	9	0	14	3	2	78
GE HDI	9	9	4	3	3	11	4	6	9	0	14	3	0	75
Hughes TRB	9	9	4	3	3	11	4	6	6	0	11	3	2	71
IBM Dendrites	9	9	7	3	0	11	4	6	9	0	14	3	2	77
IBM R3	9	7	7	3	0	11	4	6	9	0	14	3	2	75
MCC	9	9	7	3	3	11	4	6	9	0	14	3	2	80
MCNC	9	9	4	3	0	11	4	6	9	0	14	3	2	74
Micron KGD+	9	9	7	3	3	11	4	6	9	0	14	3	2	80
Micron Softool	9	9	4	3	3	11	4	6	6	0	11	3	2	71
Northern Telecom	9	9	4	3	3	11	4	6	6	0	11	3	2	71
Packard Hughes	9	9	7	3	3	11	4	6	9	0	8	3	2	74
Plastronics	9	9	7	3	3	11	4	6	9	0	14	3	2	80
Qualhi	9	9	2	3	3	11	4	6	9	0	14	3	2	75
Sandia	9	9	7	3	0	11	4	6	9	0	14	3	0	75
TI/MMS	9	9	7	3	3	11	2	6	9	0	14	3	2	78
Tribotech	9	9	7	3	3	11	4	6	9	0	14	3	2	80
Yamaichi	9	7	7	3	3	11	4	6	9	0	14	3	2	78

Table15: The TAG weights were changed to reflect a specific application. The technologies are assessed to determine the capabilities for test and burn-in of a small low speed CMOS die, with a low number of peripheral I/O on relaxed pitch. The weights of the line items of the TAG which are not relevant to this die are simply set to zero.

Company	Device Type	Wafer/ Die size	Inter connect	Device Design	Wafer Fab	Probe	Mount & Saw	Test & Burn In- Genera	Low I/O Test	High I/O Test	Burn In	Pack & Ship	Inspect	Total
Perfect	*12*	*9*	*7*	*3*	*3*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*109*
Acsist	*12*	*9*	*7*	*3*	*3*	*11*	*4*	*12*	*0*	*17*	*22*	*3*	*2*	*105*
AEHR	*12*	*9*	*7*	*3*	*3*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*107*
California Contacts	*12*	*9*	*7*	*3*	*3*	*11*	*2*	*12*	*0*	*17*	*22*	*3*	*2*	*103*
Chip Supply	*12*	*9*	*7*	*3*	*0*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*106*
ELMO	*12*	*9*	*4*	*3*	*0*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*0*	*101*
Fresh Quest	*12*	*9*	*7*	*3*	*3*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*107*
GE HDI	*12*	*9*	*4*	*3*	*3*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*0*	*104*
Hughes TRB	*12*	*9*	*4*	*3*	*3*	*11*	*4*	*12*	*0*	*15*	*19*	*3*	*2*	*97*
IBM Dendrites	*12*	*9*	*7*	*3*	*0*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*106*
IBM R3	*12*	*7*	*7*	*3*	*0*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*104*
MCC	*12*	*9*	*7*	*3*	*3*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*109*
MCNC	*12*	*9*	*4*	*3*	*0*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*103*
Micron KGD+	*12*	*9*	*7*	*3*	*3*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*109*
Micron Softool	*12*	*9*	*4*	*3*	*3*	*11*	*4*	*12*	*0*	*18*	*19*	*3*	*2*	*100*
Northern Telecom	*12*	*9*	*4*	*3*	*3*	*11*	*4*	*12*	*0*	*18*	*19*	*3*	*2*	*100*
Packard Hughes	*12*	*9*	*7*	*3*	*3*	*11*	*4*	*12*	*0*	*21*	*16*	*3*	*2*	*103*
Plastronics	*12*	*9*	*7*	*3*	*3*	*11*	*4*	*12*	*0*	*15*	*16*	*3*	*2*	*97*
Qualhi	*12*	*9*	*2*	*3*	*3*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*104*
Sandia	*12*	*9*	*7*	*3*	*0*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*0*	*104*
TI/MMS	*12*	*9*	*7*	*3*	*3*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*109*
Tribotech	*12*	*9*	*7*	*3*	*3*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*109*
Yamaichi	*12*	*7*	*7*	*3*	*3*	*11*	*4*	*12*	*0*	*21*	*22*	*3*	*2*	*109*

Table 16: The TAG weights were changed to reflect a specific application. The technologies are assessed to determine the capabilities for test and burn-in of a large high speed, high power, ECL die, with a high number of peripheral I/O on aggressive pitch. The weights of the line items of the TAG which are not relevant to this die are simply set to zero.

Company	Device Type	Wafer/ Die size	Inter connect	Device Design	Wafer Fab	Probe	Mount & Saw	Test & Burn In- Genera	Low I/O Test	High I/O Test	Burn In	Pack & Ship	Inspect	Total
Perfect	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*23*	*22*	*3*	*2*	*100*
Acsist	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*17*	*22*	*3*	*2*	*94*
AEHR	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*23*	*22*	*3*	*2*	*100*
California Contacts	*8*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*17*	*22*	*3*	*2*	*91*
Chip Supply	*5*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*92*
ELMO	*5*	*8*	*0*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*0*	*87*
Fresh Quest	*8*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*95*
GE HDI	*5*	*8*	*0*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*0*	*87*
Hughes TRB	*5*	*8*	*0*	*3*	*0*	*11*	*2*	*12*	*0*	*15*	*19*	*3*	*2*	*80*
IBM Dendrites	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*23*	*22*	*3*	*2*	*100*
IBM R3	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*23*	*22*	*3*	*2*	*100*
MCC	*8*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*95*
MCNC	*11*	*8*	*0*	*3*	*0*	*11*	*2*	*12*	*0*	*23*	*22*	*3*	*2*	*97*
Micron KGD+	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*98*
Micron Softool	*5*	*8*	*0*	*3*	*0*	*11*	*2*	*12*	*0*	*18*	*19*	*3*	*2*	*83*
Northern Telecom	*5*	*8*	*0*	*3*	*0*	*11*	*2*	*12*	*0*	*18*	*19*	*3*	*2*	*83*
Packard Hughes	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*23*	*16*	*3*	*2*	*94*
Plastronics	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*15*	*16*	*3*	*2*	*86*
Qualhi	*11*	*8*	*0*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*95*
Sandia	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*0*	*96*
TI/MMS	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*23*	*22*	*3*	*2*	*100*
Tribotech	*11*	*8*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*21*	*22*	*3*	*2*	*98*
Yamaichi	*11*	*6*	*3*	*3*	*0*	*11*	*2*	*12*	*0*	*23*	*22*	*3*	*2*	*98*

Table 17: The TAG weights were changed to reflect a specific application. The technologies are assessed to determine the capabilities for test and burn-in of a large high speed, high power, BiCMOS die, with a large number of solder bumped array I/O. The weights of the line items of the TAG which are not relevant to this die are simply set to zero.

PHASE I OBSERVATIONS

KGD is still the major obstacle to a cost competitive MCM industry. During the course of phase I of the program, it has been clear that there is much interest in the KGD issue. Both as it pertains to the technology being developed and to the overriding issues of MCM test strategies, KGD market size and maturity, . Phase I of this program has focussed on the technology issues with test and burn-in at the die level. However, even with this narrow focus, a common understanding of the KGD issues, problems and opportunities developed among those who participated in the task group meetings. This is a valuable by-product of consortia programs such as this.

At this time there is not an industry-accepted technology solution to KGD problem. The industry preferred methods for assuring KGD (according to the TAG) are temporary contact approaches. However, the announced KGD carrier development schedules have slipped in the past year. Even given that the large IC supplier internal carrier development programs meet with success, this will not satisfy the MCM industry.

For the temporary contact approaches, the contact mechanism is still troublesome. Reliable, repeatable, low cost, low Ω contact to Aluminum bond pads over temperature remains a significant technical challenge.

Appendix 1. Cost Analysis Inputs

The cost model used to perform the analyses presented in Section 5.0 relies on the entry of over 100 inputs. Almost 60 of these inputs (listed below) are related directly to specific KGD technologies. For the general case we tried to capture a typical range based on our knowledge to date. Each Monte Carlo simulation randomly selects a data point from within the distribution defined below. The software we used allows for a number of different types of distributions. In general, we chose normal distributions defined by a mean and standard deviations when we assumed a single population and triangular distributions when we assumed multiple populations or had a single population that did not lend itself well to a normal distribution. Each Monte Carlo simulation included 1000 runs which corresponds to 1000 data points selected from within each distribution.

KGD Technology Dependent Inputs

A1.1 Materials- Interconnect/Carrier/Socket Assembly:

Multi-use material costs are divided up by interconnect, carrier, and socket costs. Although the interconnect, carriers, and sockets may not be sold specifically as a function of area and/or pin count, these elements are entered into the base model to allow for sensitivity to these potential cost drivers. They can be set at zero if appropriate, and the total cost be entered as cost per piece. The total cost is calculated by adding the inputs together. For example, using the most likely values listed below, the cost of the interconnect for a 1 cm die with 100 pins would be \$55 + \$2*1 + \$0.005*100 or \$57.50.

It is assumed that the carrier and socket will last through the product life with some level of replacement (fixed at 10% for the base model). The interconnect is expected to have a more limited life, as defined by factors such as hours of thermal life and number of temperature cycles to which the interconnect can be subjected and still make good physical and electrical contact . There is also a cost associated with replacing the interconnect in the carrier.

Tooling costs or NRE for the interconnect are divided over the total number of units produced. For the general case, NRE costs for carriers and sockets are included in the base price and are not entered separately. There may be instances where a temporary contact KGD technology includes the use of consumable materials. However, these are probably relatively unusual and for the general case this input was set at zero.

Interconnect:

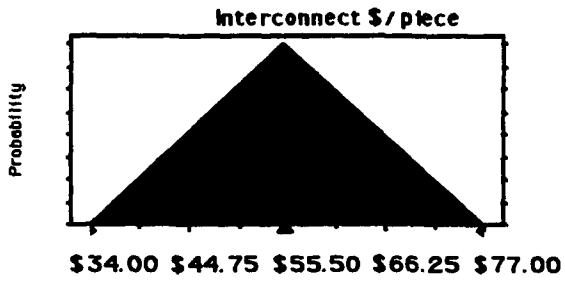
The base interconnect cost can be entered as a piece price or as a combination of piece, \$/cm, and/or \$/pin, depending on knowledge of the technology and specific pricing information. For our baseline, general case, we entered numbers that would produce a range of approximately \$35 to \$87 for a 1 cm 100 pin device, with a most likely cost of \$60 (excluding NRE costs). These number are derived from quotes that we have received to date for Phase 2, engineering knowledge, and inputs from an independent cost analyst. The quotes typically include carrier plus interconnect, so we are making educated guesses about the break-down of the costs.

Assumption: Interconnect $/piece **Cell:** C47

Triangular distribution with parameters:

Minimum	$34.00
Likeliest	$55.00
Maximum	$77.00

Selected range is from $34.00 to $77.00

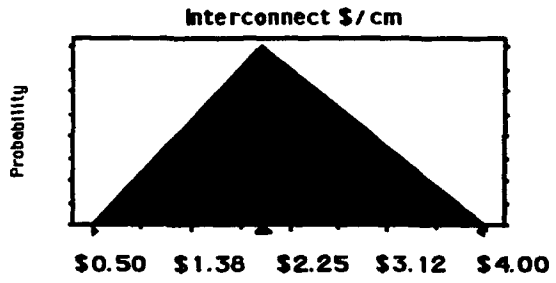


Assumption: Interconnect $/cm **Cell:** G47

Triangular distribution with parameters:

Minimum	$0.50
Likeliest	$2.00
Maximum	$4.00

Selected range is from $0.50 to $4.00

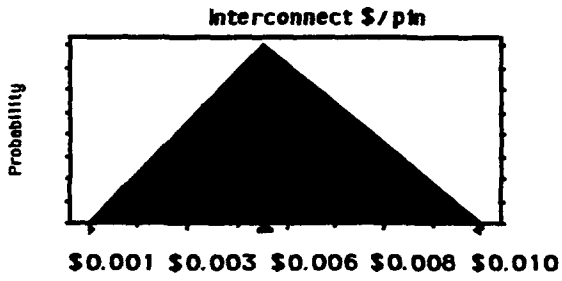


Assumption: Interconnect $/pin **Cell:** E47

Triangular distribution with parameters:

Minimum	$0.001
Likeliest	$0.005
Maximum	$0.010

Selected range is from $0.001 to $0.010



Interconnect Replacement Costs:

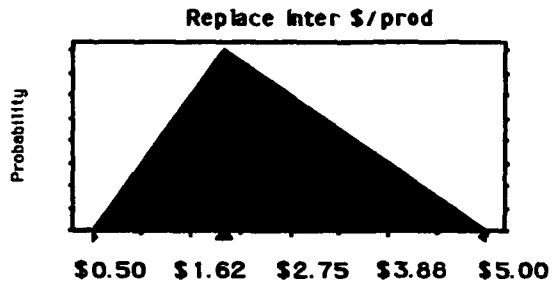
The cost to replace the interconnect is assumed to equal the cost of performing the original insertion. The cost is assumed to be largely labor costs and to take from 1 - 15 minutes at a rate of $20 per hour.

Assumption: Replace Inter $/prod **Cell:** C65

Triangular distribution with parameters:

Minimum	$0.50
Likeliest	$2.00
Maximum	$5.00

Selected range is from $0.50 to $5.00



Interconnect NRE Costs:

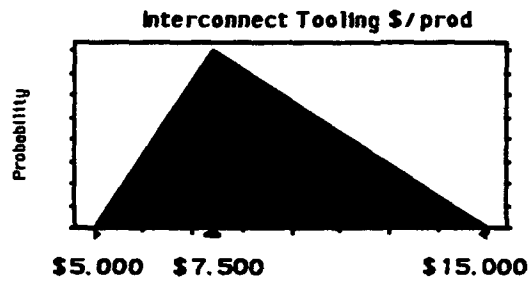
NRE costs are based on quotes that we have received to date for Phase 2, engineering knowledge, and inputs from an independent cost analyst.

Assumption: Interconnect Tooling $/prod **Cell:** E65

Triangular distribution with parameters:

Minimum	$5.000
Likeliest	$8.000
Maximum	$15.000

Selected range is from $5.000 to $15.000



Carrier:

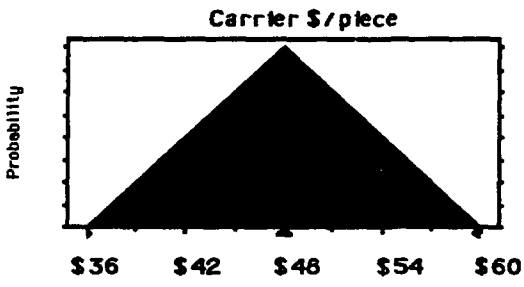
The carrier cost can be entered as a piece price or as a combination of piece and $/cm, depending on knowledge of the technology and specific pricing information. For the general case, we entered numbers that would produce a range of approximately $36 to $62 for a 1 cm 100 pin device, with a most likely cost of $49 (including NRE costs). These numbers are derived from quotes that we have received to date for Phase 2, engineering knowledge, and inputs from an independent cost analyst. The quotes typically include carrier plus interconnect, so we are making educated guesses about the cost break-down between carrier and interconnect.

Assumption: Carrier $/piece **Cell:** G34

Triangular distribution with parameters:

Minimum	$36
Likeliest	$48
Maximum	$60

Selected range is from $36 to $60

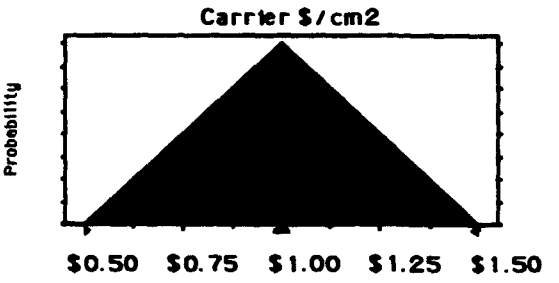


Assumption: Carrier $/cm2 **Cell:** C40

Triangular distribution with parameters:

Minimum	$0.50
Likeliest	$1.00
Maximum	$1.50

Selected range is from $0.50 to $1.50



Socket:

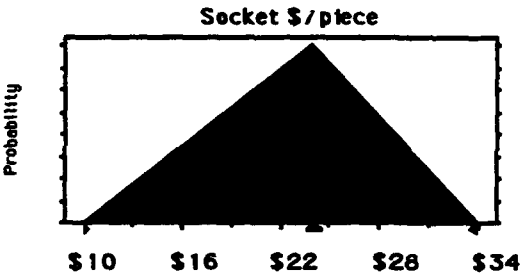
The socket may or may not be an off-the-shelf item. If not, its cost is calculated from the input assumptions described below. If it is an off-the-shelf item, the exact price can be entered instead. In some instances the socket and carrier are integral to each other. In this instance, the carrier cost is rolled into the socket cost and zeroed out in the carrier section. For the general case presented in Section 5.0, carrier and socket costs are treated separately.

Assumption: Socket $/piece **Cell:** G28

Triangular distribution with parameters:

Minimum	$10
Likeliest	$24
Maximum	$34

Selected range is from $10 to $34

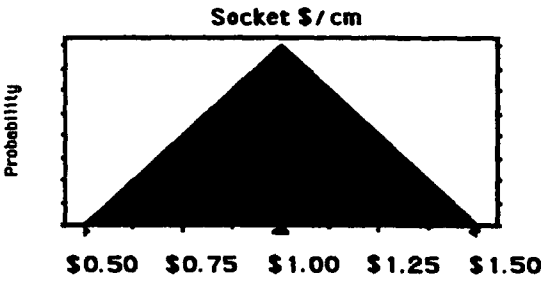


Assumption: Socket $/cm **Cell:** C34

Triangular distribution with parameters:

Minimum	$0.50
Likeliest	$1.00
Maximum	$1.50

Selected range is from $0.50 to $1.50

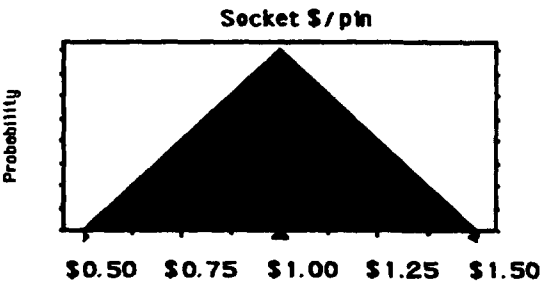


Assumption: Socket $/pin **Cell:** E34

Triangular distribution with parameters:

Minimum	$0.50
Likeliest	$1.00
Maximum	$1.50

Selected range is from $0.50 to $1.50



Interconnect Life

There are a number of factors which will ultimately affect the number of uses possible from a single carrier/interconnect assembly. These include nontechnology dependent factors such as product life and number of burn-in hours per cycles as well as the technology dependent factor listed below.

Number of Assemblies:

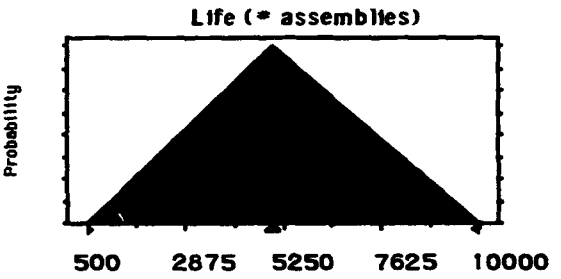
The number of assemblies is the number of times, independent of any temperature cycling, that a die can be placed in the carrier, put in contact with the interconnect, and removed. We assumed that the majority of the technologies will be able to easily handle 500 assemblies, independent of thermal or handling damage. 5,000 covers the "infinite uses" claim made by most suppliers while still falling within the realm of possibility for a two year product life. 10,000 is well above the limit likely to be imposed by nontechnology related factors such as product life and burn-in cycle time.

Assumption: Life (# assemblies) **Cell:** C53

Triangular distribution with parameters:

Minimum	500
Likeliest	5000
Maximum	10000

Selected range is from 500 to 10000



Thermal Life (hours):

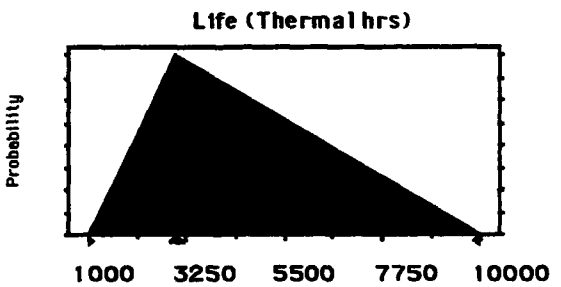
Thermal life is the number of hours at temperature that a carrier/interconnect assembly can withstand and still make good contact with a die. This measure is independent of any temperature cycling (i.e., only one temperature excursion). One thousand hours was chosen as a lower limit because it is believed to be consistent with life-times for Cu/PI interconnect. 3000 hours was selected as the most likely life-time for the interconnect. This is consistent with our knowledge of test results on Cu/PI based systems. The upper limit is set at 10,000 hours, since there is limited value in exceeding this number given typical product lives and turn-around times between burn-in uses.

Assumption: Life (Thermal hrs) **Cell:** E53

Triangular distribution with parameters:

Minimum	1000
Likeliest	3000
Maximum	10000

Selected range is from 1000 to 10000



Temperature Cycles:

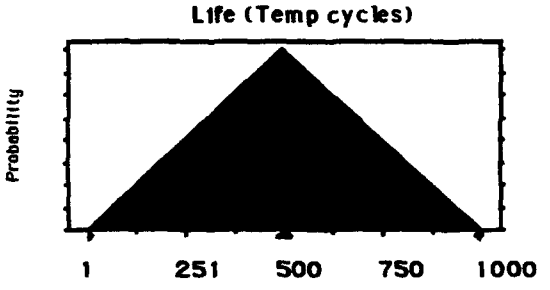
The number of temperature cycles is the number of times that a carrier/interconnect assembly can go from ambient to burn-in temperature and still make good contact with a die.

Assumption: Life (Temp cycles) **Cell:** G53

Triangular distribution with parameters:

Minimum	1
Likeliest	500
Maximum	1000

Selected range is from 1 to 1000



Interconnect Mechanical Failures Cycles:

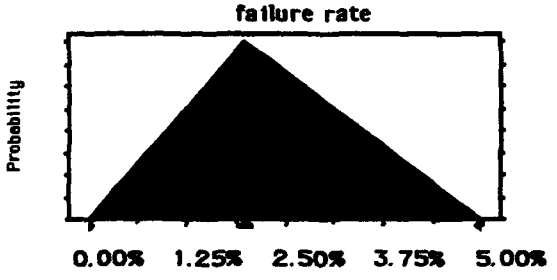
Mechanical failures is the percent of all interconnects which will have to be replaced due to handling damage.

Assumption: Interconnect mechanical failure rate **Cell:** G59

Triangular distribution with parameters:

Minimum	0.00%
Likeliest	2.00%
Maximum	5.00%

Selected range is from 0.00% to 5.00%



Cleans (Reclaim) of Probe Tips:

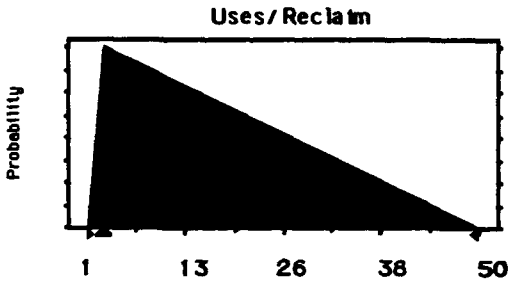
The number of times that probe tips can be cleaned without damaging either the interconnect or probe tips (Reclaim/Interconnect) multiplied by the number of times the interconnect/probe tips can be used between cleans (Uses/Reclaim) will have an effect on the total number of uses provided by a single interconnect. This particular factor was not used in the analyses presented in this report, but will be included in the future.

Assumption: Uses/Reclaim **Cell:** C59

Triangular distribution with parameters:

Minimum	1
Likeliest	3
Maximum	50

Selected range is from 1 to 50

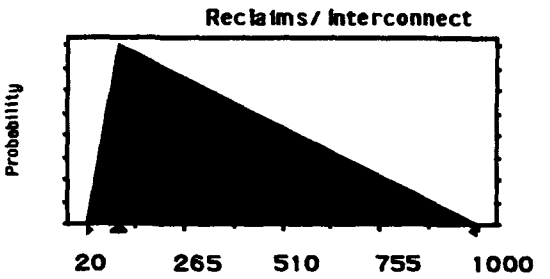


Assumption: Reclaims/Interconnect **Cell:** E59

Triangular distribution with parameters:

Minimum	20
Likeliest	100
Maximum	1000

Selected range is from 20 to 1000



A1.2 *Assembly:*

Assembly is modeled in two pieces. Pick and place is the the means by which the die is aligned to and placed into physical contact with the carrier. Lid/spring placement is the means by which a lid and/or some form of pressure is applied to ensure that the die is physically held within the carrier and reliable electrical contact between the die and carrier+interconnect is maintained. Note that the model for the general case assumes that the same carrier will be used for both burn-in and test. If this is not the case, this step will have to be included twice.

Pick and Place:

Pick and place is divided into three pieces for ease of modeling. There may be only a single piece of equipment, but it will have all three of the functions below. The cycle time for this step is taken as the maximum of the three pieces, carrier align, die align, and attach1 (i.e., placement of the die into the carrier). Labor times for automated systems are set equal to equipment cycle times, although the model permits this value to be set as a ratio to equipment time. For the general case we assumed no non-equipment related labor time for automatic systems, but the model will permit entry of this input if needed. For manual systems, all labor and cycle times are calculated from the entry "Align Manual Labor".

Carrier Align:

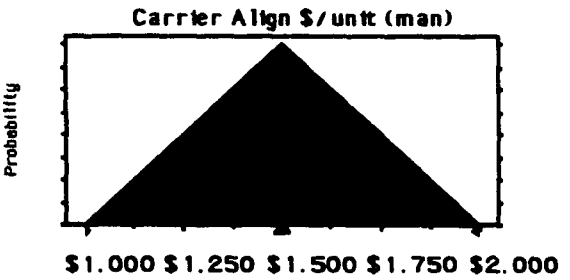
This step covers handling of incoming carriers and subsequent placement of the carriers at some reference point to which the die can be aligned. In the case of a manual operation, this may be a simple plate.

Assumption: Carrier Align $/unit (manual) **Cell:** C73

Triangular distribution with parameters:

Minimum	$1.000
Likeliest	$1.500
Maximum	$2.000

Selected range is from $1.000 to $2.000

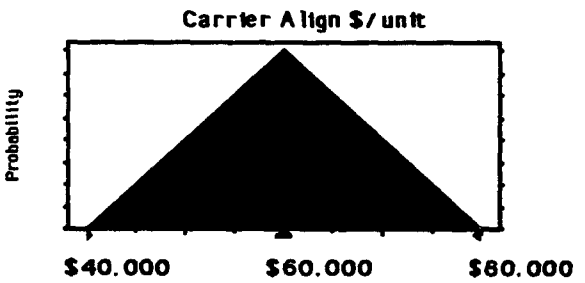


Assumption: Carrier Align $/unit (auto) **Cell:** C74

Triangular distribution with parameters:

Minimum	$40.000
Likeliest	$60.000
Maximum	$80.000

Selected range is from $40.000 to $80.000

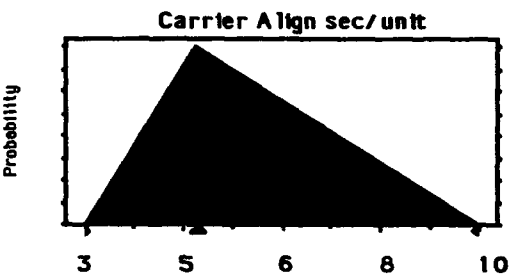


Assumption: Carrier Align sec/unit **Cell:** E73

Triangular distribution with parameters:

Minimum	3
Likeliest	5
Maximum	10

Selected range is from 3 to 10



Die Align:

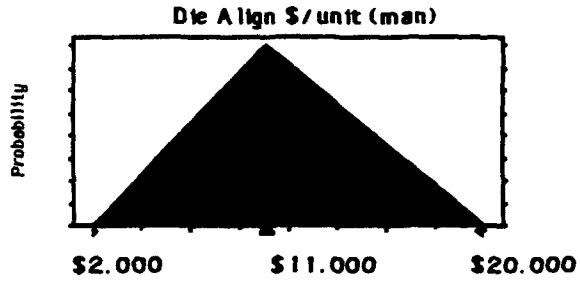
The die may be aligned manually with the aid of a microscope, mechanically using the edge of the silicon die as a reference, or visually using a computer aided vision system It is presumed that the mechanical method will be faster than a optical system, whether the latter is manual or automatic Alignment tooling is anything that is product specific needed in the alignment of the die. This cost is expected to be small, and highest for mechanical align.

Assumption: Die Align $/unit (manual) **Cell:** G73

Triangular distribution with parameters:

Minimum	$2.000
Likeliest	$10.000
Maximum	$20.000

Selected range is from $2.000 to $20.000

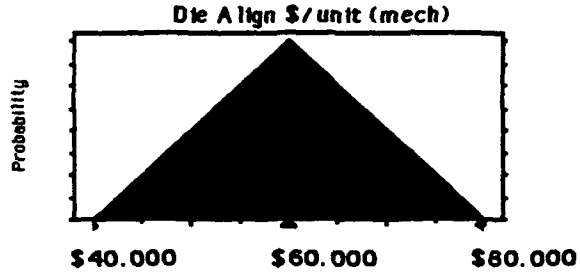


Assumption: Die Align $/unit (mechanical) **Cell:** G74

Triangular distribution with parameters:

Minimum	$40.000
Likeliest	$60.000
Maximum	$80.000

Selected range is from $40.000 to $80.000

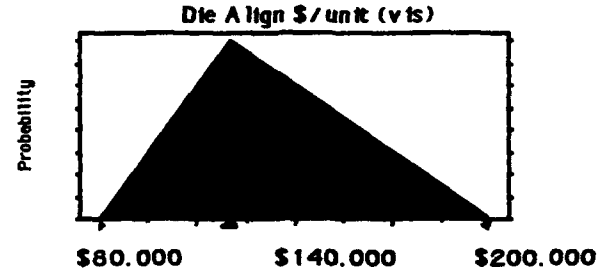


Assumption: Die Align $/unit (visual) **Cell:** G75

Triangular distribution with parameters:

Minimum	$80.000
Likeliest	$120.000
Maximum	$200.000

Selected range is from $80.000 to $200.000

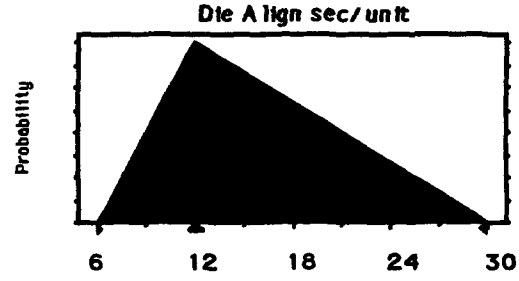


Assumption: Die Align sec/unit (visual, manual or auto) **Cell:** C81

Triangular distribution with parameters:

Minimum	6
Likeliest	12
Maximum	30

Selected range is from 6 to 30



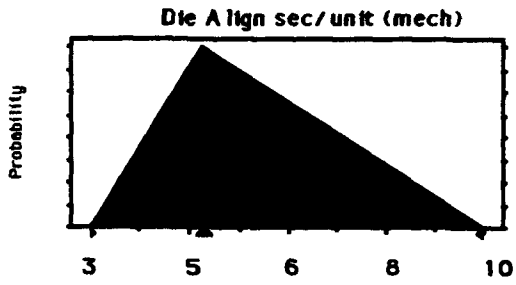
Assumption: Die Align sec/unit (mech)

Cell: C82

Triangular distribution with parameters:

Minimum	3
Likeliest	5
Maximum	10

Selected range is from 3 to 10



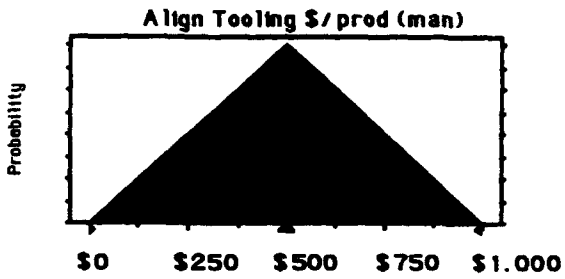
Assumption: Align Tooling $/prod (manual)

Cell: E81

Triangular distribution with parameters:

Minimum	$0
Likeliest	$500
Maximum	$1.000

Selected range is from $0 to $1.000



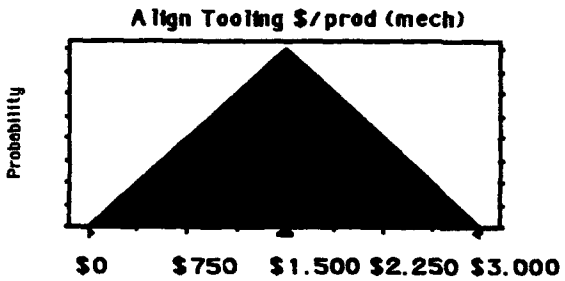
Assumption: Align Tooling $/prod (mechanical)

Cell: E82

Triangular distribution with parameters:

Minimum	$0
Likeliest	$1.500
Maximum	$3.000

Selected range is from $0 to $3.000



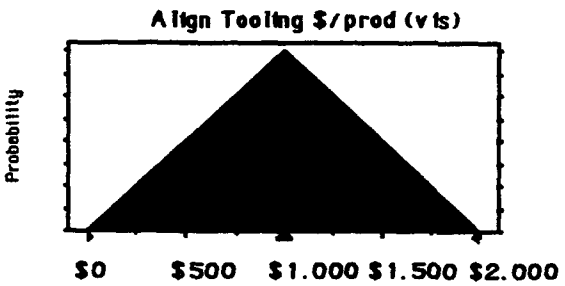
Assumption: Align Tooling $/prod (visual)

Cell: E83

Triangular distribution with parameters:

Minimum	$0
Likeliest	$1.000
Maximum	$2.000

Selected range is from $0 to $2.000

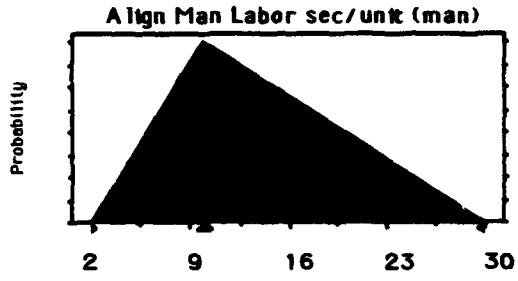


Assumption: Align Man Labor sec/unit (manual) **Cell:** G81

Triangular distribution with parameters:

Minimum	2
Likeliest	10
Maximum	30

Selected range is from 2 to 30



Placement of Die (Attach1)

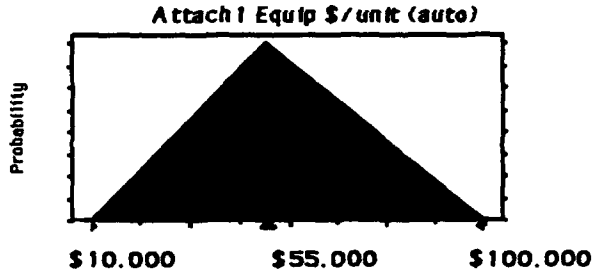
Attach1 puts the die in contact with the carrier+interconnect but does not provide a mechanism to secure the attachment of the die to the carrier. This step may be modeled as either an automatic or manual step. Labor times are set as equal to the equipment cycle times in the case of the former.

Assumption: Attach1 Equip $/unit (auto) **Cell:** C91

Triangular distribution with parameters:

Minimum	$10.000
Likeliest	$50.000
Maximum	$100.000

Selected range is from $10.000 to $100.000

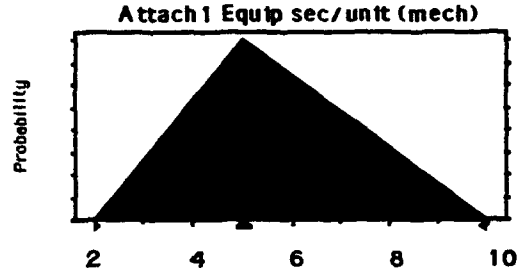


Assumption: Attach1 Equip sec/unit (auto) **Cell:** E90

Triangular distribution with parameters:

Minimum	2
Likeliest	5
Maximum	10

Selected range is from 2 to 10

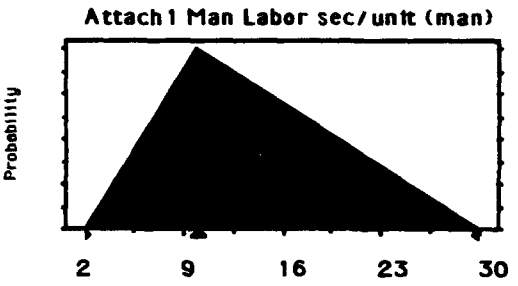


Assumption: Attach1 Man Labor sec/unit (manual) **Cell:** G89

Triangular distribution with parameters:

Minimum	2
Likeliest	10
Maximum	30

Selected range is from 2 to 30



Lid/spring placement:

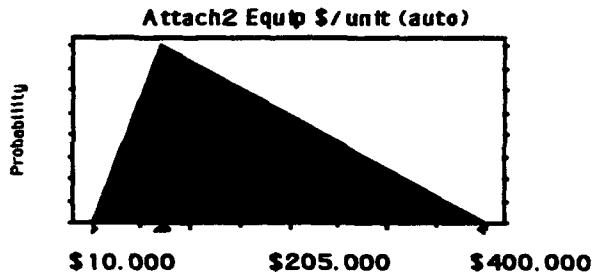
This step, termed Attach2, refers to placement of lids, caps, springs, screws, etc. which keep the die contained within the carrier and which apply force to the system to bring the die and interconnect into reliable electrical contact. This step may be modeled as either an automatic or manual step. Labor times are set as equal to the equipment cycle times in the case of the former.

Assumption: Attach2 Equip $/unit (auto) **Cell:** C98

Triangular distribution with parameters:

Minimum	$10.000
Likeliest	$80.000
Maximum	$400.000

Selected range is from $10.000 to $400.000

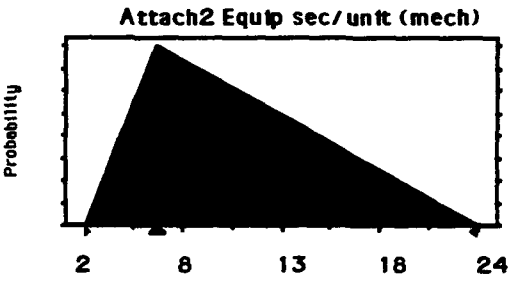


Assumption: Attach2 Equip sec/unit (auto) **Cell:** E98

Triangular distribution with parameters:

Minimum	2
Likeliest	6
Maximum	24

Selected range is from 2 to 24

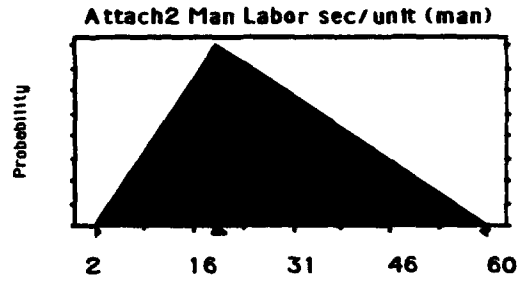


Assumption: Attach2 Man Labor sec/unit (manual) **Cell:** C105

Triangular distribution with parameters:

Minimum	2
Likeliest	20
Maximum	60

Selected range is from 2 to 60



A1.3 Disassembly:

Disassembly is the step which removes the lids, springs, etc., that hold the die in contact with the carrier+interconnect. Placement of the die into a waffle pack for shipping also occurs at this step. Note that the model for the general case assumes that the same carrier will be used for both burn-in and test. If this is not the case, this step will have to be included twice.

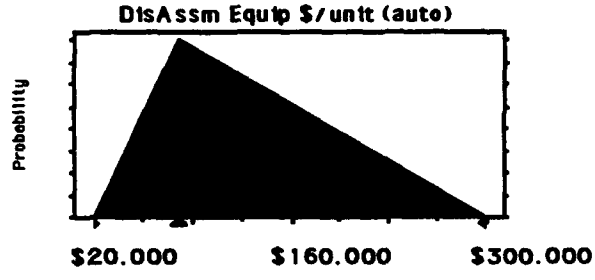
Disassembly may be modeled as either an automatic or manual step. Labor times are set as equal to the equipment cycle times in the case of the former.

Assumption: DisAssm Equip $/unit (auto) **Cell:** G106

Triangular distribution with parameters:

Minimum	$20.000
Likeliest	$80.000
Maximum	$300.000

Selected range is from $20.000 to $300.000

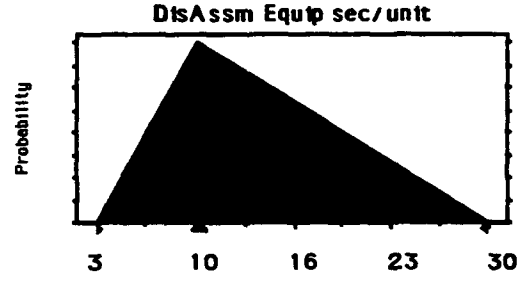


Assumption: DisAssm Equip sec/unit (auto) **Cell:** C114

Triangular distribution with parameters:

Minimum	3
Likeliest	10
Maximum	30

Selected range is from 3 to 30

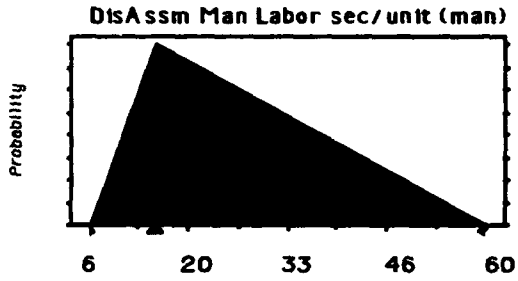


Assumption: DisAssm Man Labor sec/unit (man) **Cell:** G113

Triangular distribution with parameters:

Minimum	6
Likeliest	15
Maximum	60

Selected range is from 6 to 60



A1.4 Reclaim/Clean:

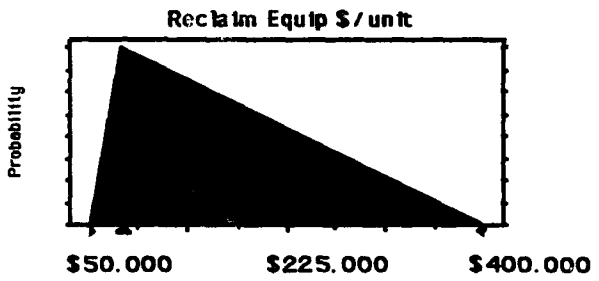
It is assumed that most probe tips will need to be cleaned or otherwise maintained/reclaimed. This may be done chemically and/or physically, depending on the materials and configuration. The equipment costs used for the general case are probably on the high side, but given that this is a largely undefined step, it was decided to err on the side of caution. It was also assumed that there might be a significant amount of manual labor involved. This step can be modeled more accurately once specific materials and configurations are better defined.

Assumption: Reclaim Equip $/unit **Cell:** E121

Triangular distribution with parameters:

Minimum	$50.000
Likeliest	$80.000
Maximum	$400.000

Selected range is from $50.000 to $400.000

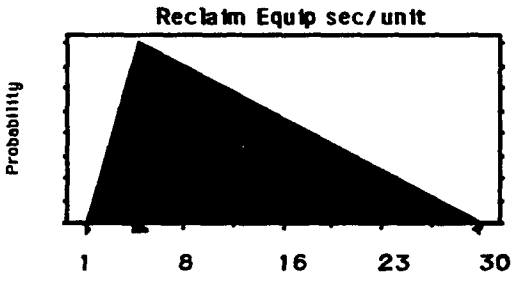


Assumption: Reclaim Equip sec/unit **Cell:** G121

Triangular distribution with parameters:

Minimum	1
Likeliest	5
Maximum	30

Selected range is from 1 to 30

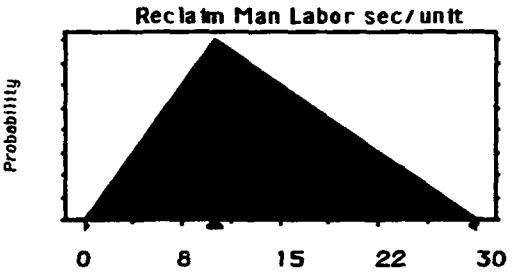


Assumption: Reclaim Man Labor sec/unit **Cell:** C127

Triangular distribution with parameters:

Minimum	0
Likeliest	10
Maximum	30

Selected range is from 0 to 30



A1.5 Failures:

The model is intended for use in larger modeling efforts where costs of entire systems are evaluated from wafer fab through module assembly and test. For this reason, it is desirable to have a measure of the outgoing defectivity of the bare die. The model calculates the level of defectivity and refers to it as True Good Die or TGD. This is a measure of escapes within the KGD population. For the current KGD modeling effort, assembly induced failures are added to the incoming defectivity levels at final test, but disassembly induced failures are always escapes since there is no test and sort mechanism after the die are removed from the carrier.

Assembly induced failures

Assembly induced failures are a measure of electrically identifiable failures which occur as a result of damage incurred during die to carrier assembly.

Disassembly induced failures

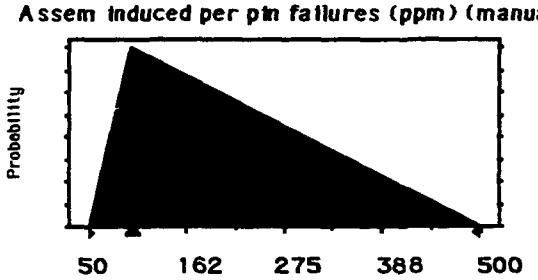
Disassembly induced failures are a measure of electrically identifiable failures which occur as a result of damage incurred during die to carrier disassembly.

Assumption: Assem Induced per pin failures (ppm) (manual) **Cell:** E105

Triangular distribution with parameters:

Minimum	50
Likeliest	100
Maximum	500

Selected range is from 50 to 500

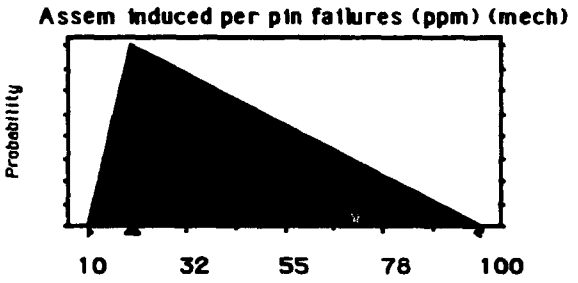


Assumption: Assem induced per pin failures (ppm) (mechanical) **Cell:** E106

Triangular distribution with parameters:

Minimum	10
Likeliest	20
Maximum	100

Selected range is from 10 to 100

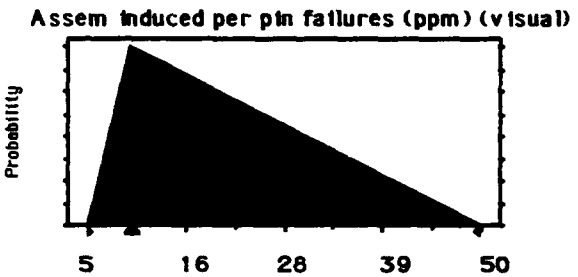


Assumption: Assem induced per pin failures (ppm) (visual) **Cell:** E107

Triangular distribution with parameters:

Minimum	5
Likeliest	10
Maximum	50

Selected range is from 5 to 50

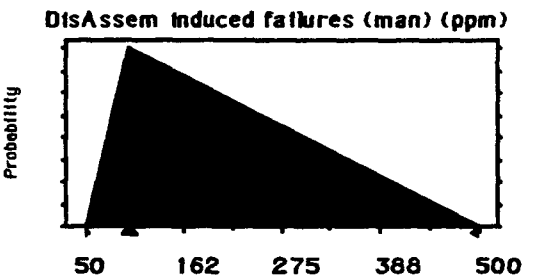


Assumption: DisAssem induced failures (man) (ppm) **Cell:** C121

Triangular distribution with parameters:

Minimum	50
Likeliest	100
Maximum	500

Selected range is from 50 to 500

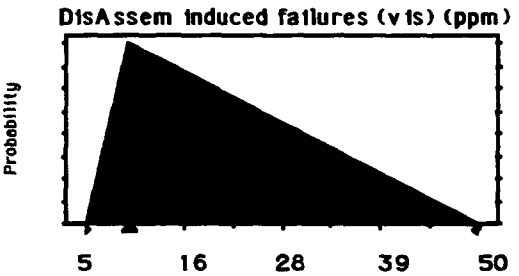


Assumption: DisAssem induced failures (auto) (ppm) **Cell:** C123

Triangular distribution with parameters:

Minimum	5
Likeliest	10
Maximum	50

Selected range is from 5 to 50



KGD Technology Independent Inputs

A1.6 Production Hours:

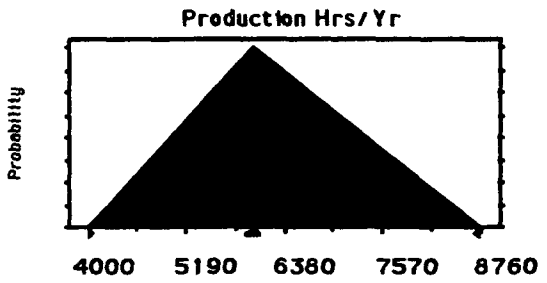
The minimum number of production hours is set at 4000 hours (two 8-hour shifts, 5 days per week, 50 weeks per year). The maximum set at 8760, 365 days a year, 24 hours a day.

Assumption: Production Hrs/Yr **Cell:** E20

Triangular distribution with parameters:

Minimum	4000
Likeliest	6000
Maximum	8760

Selected range is from 4000 to 8760



A1.7 Labor rates:

Wages for direct employees are determined from 3 different inputs, operator wages, burden rate, and nonproduction time.

Operator wages.

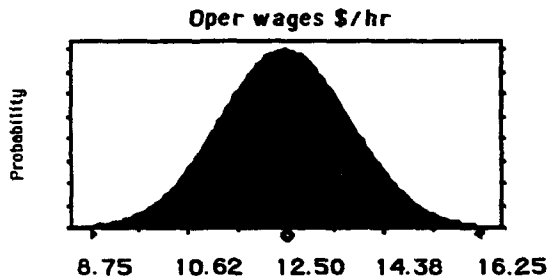
The mean base wage is set at $12.50/hour with a standard deviation of $1.25, resulting in an effective range of $8.75 to $16.25.

Assumption: Oper wages $/hr **Cell:** G20

Normal distribution with parameters:

Mean	12.50
Standard Dev.	1.25

Selected range is from - to



Burden rate.

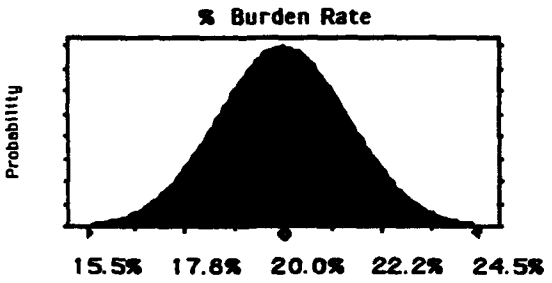
The mean burden rate is assumed to be 20% with a standard deviation of 1.5%, giving an effective range of 16-24%. This is the effective cost of benefits, etc.

Assumption: % Burden Rate **Cell: C24**

Normal distribution with parameters:

Mean	20.0%
Standard Dev.	1.5%

Selected range is from - to



Nonproduction time.

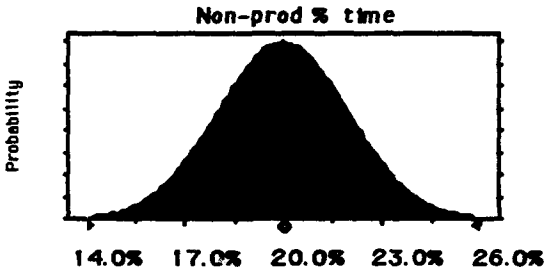
This is a measure of the time an operator spends not directly running production. The mean is set at 20% with a standard deviation of 2%, and an effective range of 14 to 26%.

Assumption: Non-prod % time **Cell: E24**

Normal distribution with parameters:

Mean	20.0%
Standard Dev.	2.0%

Selected range is from - to



A1.8 Yield:

Yield is calculated from three different assumptions.

Test Coverage at Wafer Sort.

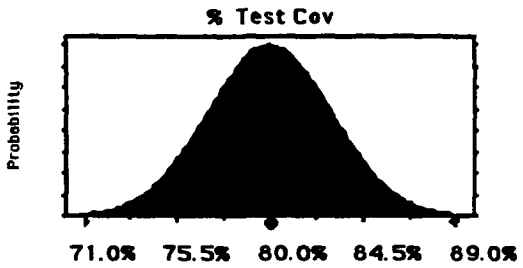
This is a measure of the test effectiveness or test coverage at wafer sort. The assumed mean is 80% and the standard deviation is set at 3%. The upper level of 90% is probably most appropriate for major suppliers like Motorola and Intel and for devices like DRAMs. The industry/device average is thought to be closer to 80%. For an explanation of this factor and its use see Williams and Brown [1].

Assumption: % Test Cov **Cell: C20**

Normal distribution with parameters:

Mean	80.0%
Standard Dev.	3.0%

Selected range is from - to



Test Coverage at Final Test.

This is a measure of the test effectiveness or test coverage at final test. Assumed is a fixed value of 99%. For an explanation of this factor and its use see Williams and Brown [1].

Defect Density in Wafer Fab

Defect density is a measure of the total defectivity of the wafer which may or may not be detected at test [2]. This value is fixed at 0.5 defects per cm2. Defect density is a measure of all defects which, given enough time and use, will eventually produce an electrical failure in the die. Some portion of these defects will escape burn-in and test and will result in field failures. Yield is calculated as a function of this number and test coverage.

Summary of Inputs

Factor	Likeliest or Mean	Range or Standard Deviation.
Interconnect		
Interconnect $/piece	$55.00	$34 - $77
Interconnect $/cm	$2.00	$0.50 - $4.00
Interconnect $/pin	$0.005	$0.001 - $0.010
Replace Inter $/prod	$2.00	$0.50 - $5.00
Interconnect Tooling $/prod	$8,000	$5,000 - $15,000
Carrier		
Carrier $/piece	$48	$36 - $60
Carrier $/cm2	$1.00	$0.50 - $1.50
Socket		
Socket $/piece	$24	$10 - $34
Socket $/cm	$1.00	$0.50 - $1.50
Socket $/pin	$1.00	$0.50 - $1.50
Interconnect Life		
Life (# assemblies)	5000	500 - 10,000
Life (Thermal hrs)	3000	1000 - 10,000
Life (Temp cycles)	500	1 - 1000
Uses/Reclaim	3	1 - 50
Reclaims/Interconnect	100	20 - 1000
Interconnect mechanical failure rate	2.00%	0.00% - 5.00%

Factor	Likeliest or Mean	Range or Standard Deviation.
Alignment		
Carrier Align $/unit (manual)	$1,500	$1,000 - $2,000
Carrier Align $/unit (auto)	$60,000	$40,000 - $80,000
Carrier Align sec/unit	5	3 - 10
Die Align $/unit (manual)	$10,000	$2,000 - $20,000
Die Align $/unit (mechanical)	$60,000	$40,000 - $80,000
Die Align $/unit (visual)	$120,000	$80,000 - $200,000
Die Align sec/unit (visual, manual or auto)	12	6 - 30
Die Align sec/unit (mechanical)	5	3 - 10
Align Tooling $/prod (manual)	$500	$0 - $1,000
Align Tooling $/prod (mechanical)	$1,500	$0 - $3,000
Align Tooling $/prod (visual)	$1,000	$0 - $2,000
Align Man Labor sec/unit (manual)	10	2 - 30
Attach1		
Attach1 Equip $/unit (auto)	$50,000	$10,000 - $100,000
Attach1 Equip sec/unit (auto)	5	2 - 10
Attach1 Man Labor sec/unit (manual)	10	2 - 30
Attach2		
Attach2 Equip $/unit (auto)	$80,000	$10,000 - $400,000
Attach2 Equip sec/unit (auto)	6	2 - 24
Attach2 Man Labor sec/unit (manual)	20	2 - 60
Disassembly		
DisAssm Equip $/unit (auto)	$80,000	$20,000 - $300,000
DisAssm Equip sec/unit (auto)	10	3 - 30
DisAssm Man Labor sec/unit (man)	15	6 - 60
Reclaim/Clean		
Reclaim Equip $/unit	$80,000	$50,000 - $400,000
Reclaim Equip sec/unit	5	1 - 30
Reclaim Man Labor sec/unit	10	0 - 30

Factor	Likeliest or Mean	Range or Standard Deviation.
Failures		
Assem induced per pin failures (ppm) (manual)	100	50 - 500
Assem induced per pin failures (ppm) (mechanical)	20	10 - 100
Assem induced per pin failures (ppm) (visual)	10	5 - 50
DisAssem induced failures (man) (ppm)	100	50 - 500
DisAssem induced failures (auto) (ppm)	10	5 - 50
KGD Technology Independent Inputs		
Production Hrs/Yr	6000	4000 - 8760
Oper wages $/hr	12.5	1.25
% Burden Rate	20.00%	1.50%
Non-prod % time	20.00%	2.00%
% Test Cov at Wafer Sort[1]	80.00%	3.00%
% Test Cov at Final Test [1]	99.00%	none

References

[1] T.W. Williams and N.C. Brown, "Defect Level as a Function of Fault Coverage", IEEE Transactions on Computers, vol. C-30, No. 12, December 1981, pp. 987-988, (1981).

[2] B.T. Murphy, "Cost-Size Optima of Monolithic Integrated Circuits", Proc IEEE, vol. 52, pp.1527 - 1545, (1964).

Section II

Phase II Validation Plan

PHASE II VALIDATION PLAN

Executive Summary

Our findings in Phase I reveal much activity and interest in the industry surrounding the KGD questions. The industry guidelines (TAG) developed in this project show a definite bias toward temporary contact methods as evinced by the top scoring technologies all being temporary contact methods. However, these technologies have not been proven, and we attribute the delay in product introductions to underestimating the difficulty of the problems with probing Al pads on silicon, and hence, a tendency to underfund development efforts; especially with lack of industry consensus behind any one method. The lack of a cost effective technology for assuring Known Good Die remains the stumbling block to widespread adoption of MCMs in industry.

The goal of the Phase II work is to develop industry confidence that one or more KGD solutions is in place and is effective at supplying KGD into real applications. The plan is composed of three stages.

- Evaluation
- Qualification
- Product Insertion

Under the Phase I effort, MCC has assessed the technology, determined readiness and identified cost drivers for KGD carriers. The price, availability, and applicability of die level KGD carrier technologies have been determined through the release of RFQ's for the Phase II validation. Three RFQs (carriers, test and burn-in services and die) and a Statement of Work were sent out to companies developing KGD solutions in the industry. As a major emphasis was put on the product insertion stage of the Phase II work, an addenda to the RFQ for die was issued spelling out the testing requirements and expected deliverables for the die supplier. Copies of the RFQs and SOW are included in this section of the Phase I report as an appendix.

A Phase II steering committee has directed MCC through the Phase II planning stages and has defined these test plans. This steering committee will transition into an advisory board once Phase II commences and will be responsible for decision points in the Phase II project. Figure 1 illustrates the overview of the KGD project, showing the relationship of Phase I to Phase II.

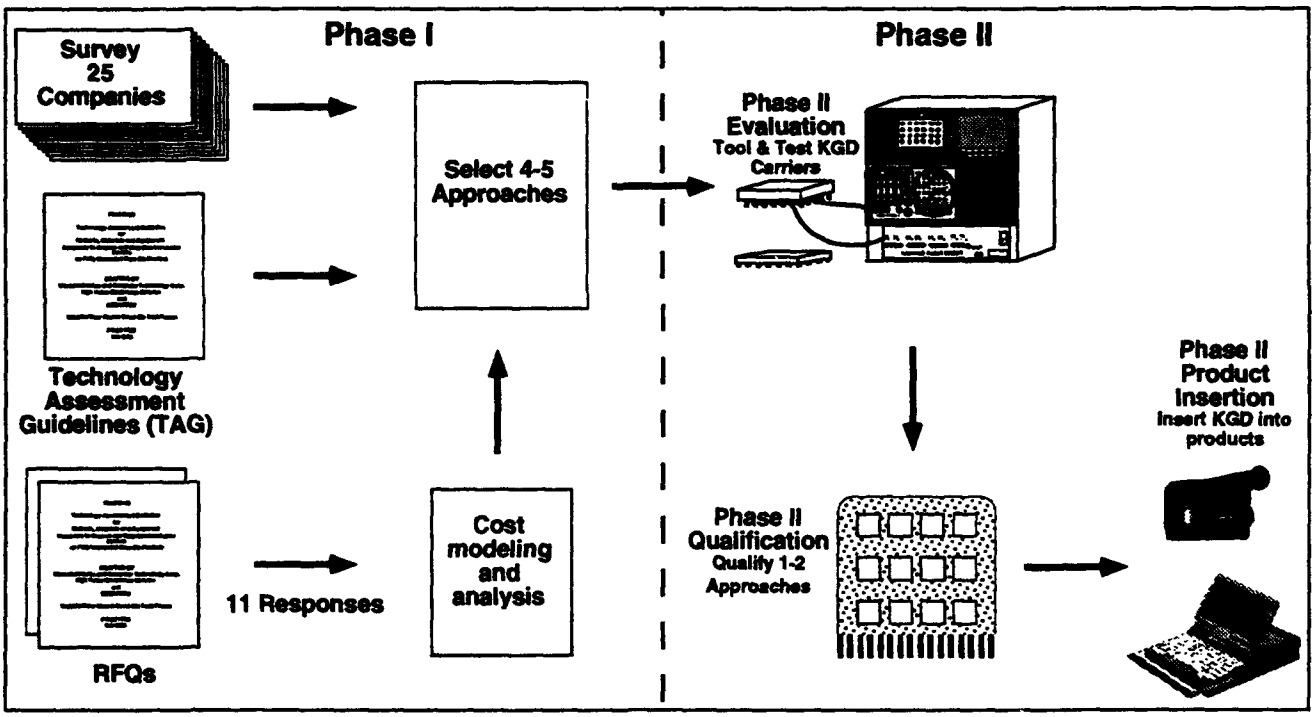


Figure 1: KGD Project Overview: This report summarizes the results of phase I, and outlines the plans for phase II.

1.0 Phase II Evaluation

Based on available funding for testing costs, we propose to evaluate four or five selected KGD approaches of the 24 assessed in Phase I (See Table 2, Subsection 1.0). The evaluation of the four or five selected approaches will be based on the industry generated *Technology Assessment Guidelines* (TAG) and the Phase II steering committee direction. The tests will be performed on KGD carriers in a laboratory setting using blanket aluminum or ink-dot die only. The following are tests that will be used to evaluate the carriers performance as specified in the TAG[1]. These tests will be performed at MCC's laboratories (or subcontracted to a qualified test company where appropriate).

1.1 Phase II Tests

Test Method 1. Planarity of Die/Interconnect

KGD carrier interconnect will be tested for its contact resistance to a dummy die with multiple Al layers to provide a range of pad heights.

Test Method 2. Die Damage or Contamination

Die will be stationed in KGD carrier or socket and removed per manufacturer's specifications. Die will be inspected for bond pad damage due to probe contact per MIL Standard 883D Method 2010.10. Die will be inspected for damage to layers underlying the bond pad metal due to probe contact per MIL Standard 883D Method 2010.10. Die will be tested for loss of adhesion to die attach material from damage or contamination of back side of die due to Carrier or socket contact per MIL Standard 883D Method 2019.5. Die will be inspected for intermetallic formation on bond pad due to probe contact with Auger Electron Spectroscopy per ASTM method E 827-88 prior to and after temperature and humidity (85/85) exposure for 168 hours.

Test Method 3. Temperature Cycling

KGD carrier will be temperature cycled per MIL Standard 883D Method 1010.7 except with a temperature ranges of 0 °C to 85 °C, 0°C to +125° C, and -55 °C to 150 °C.

Test Method 4. Contact Resistance

KGD carrier interconnect will be tested for its contact resistance per MIL Standard 883D Method 3017.3.3. Contact resistance must be less than or equal to 0.5 Ω. KGD carrier contact resistance will be measured prior to and during temperature cycling.

Test Method 5. Maximum Clock Frequency, Characteristic Impedance, and Bandwidth

KGD carrier interconnect will be tested for TDR rise time per MIL Standard 883D Method 3017. The characteristic impedance will be measured from the impedance waveform display on the TDR. The characteristic impedance must be within 10% of the designed impedance. Using the same test setup while replacing the TDR with a network analyzer, the KGD carrier interconnect will be tested for its bandwidth per MIL Standard 883D Method 4004.1.3.4. Bandwidth must be greater than or equal to 500 MHz. MIL Standard 883D Method 3018 will be used for measuring the level of cross coupling of signals and noise between pins, although no rules have been defined.

Test Method 6. Die Damage or Contamination After Two Touchdowns

Die will be stationed in KGD carrier or socket and removed twice per manufacturer's specifications. Die will be inspected for bond pad damage due to probe contact per MIL Standard 883D Method 2010.10. Die will be inspected for damage to layers underlying the bond pad metal due to probe contact per MIL Standard 883D Method 2010.10. Die will be tested for loss of adhesion to die attach material from damage or contamination of back side of die due to Carrier or socket contact per MIL Standard 883D Method 2019.5. Die bond

[1] These test methods were added to the TAG, making it revision 3.0, which is included as Section III of this report.

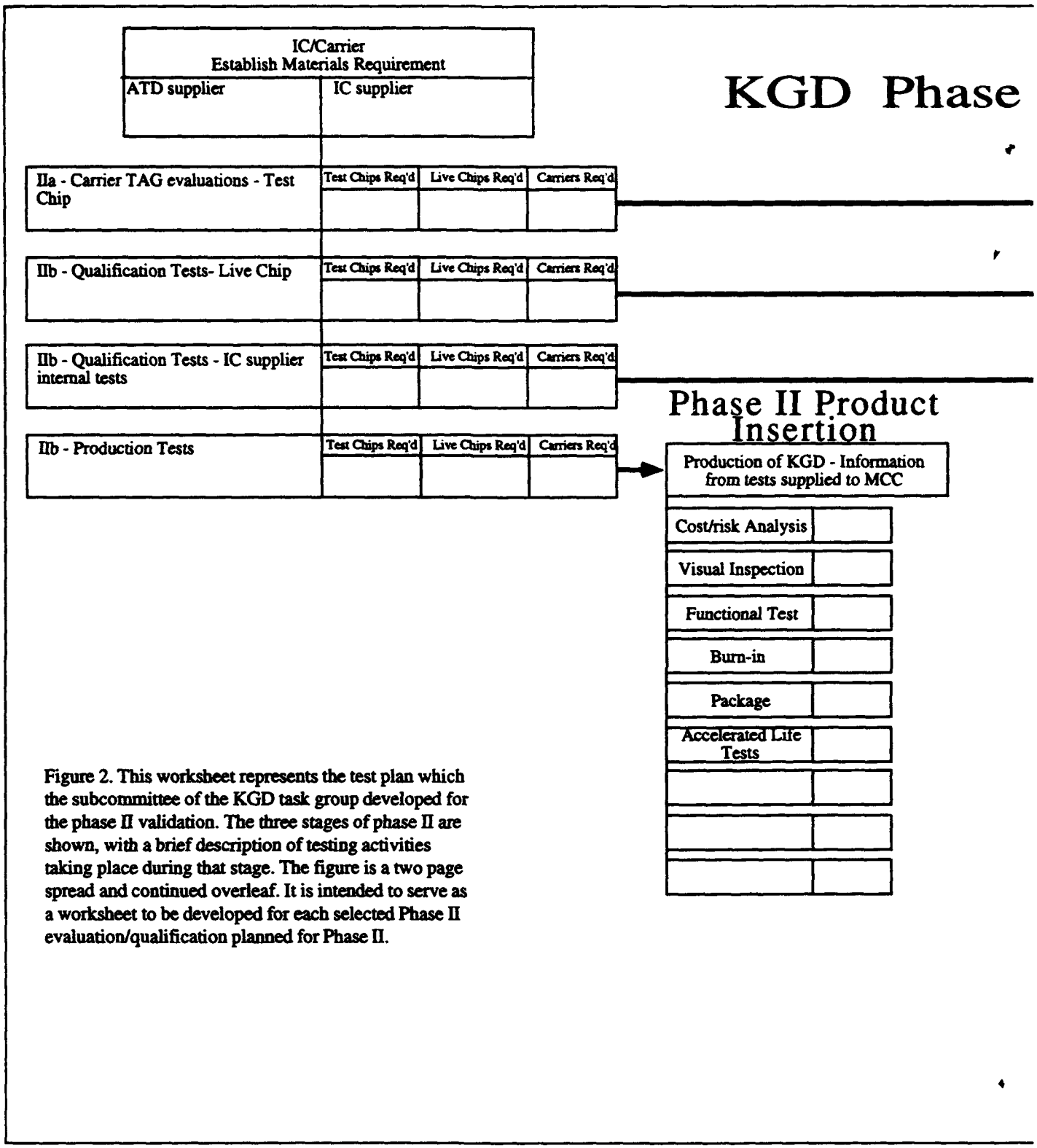


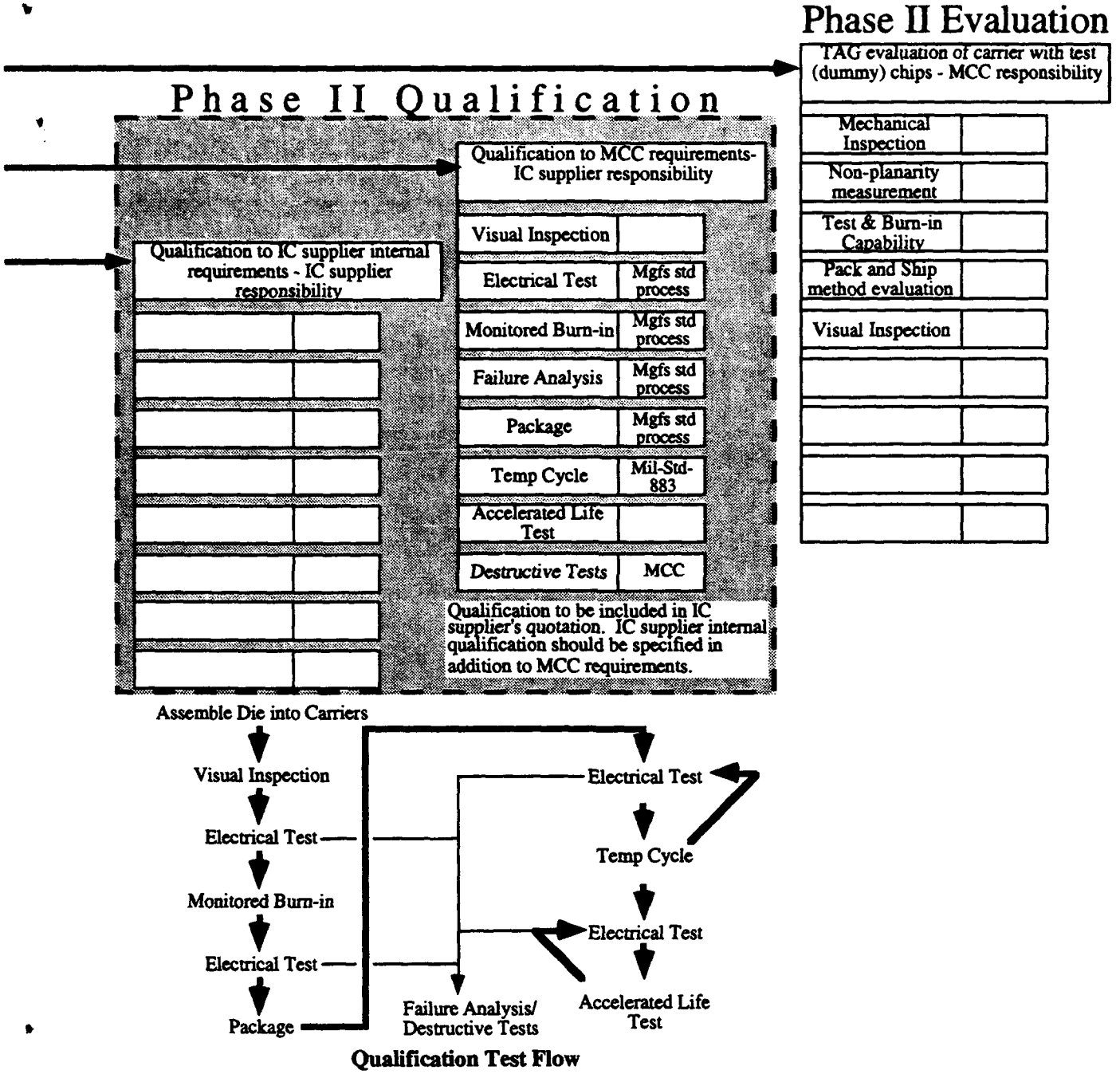
Figure 2. This worksheet represents the test plan which the subcommittee of the KGD task group developed for the phase II validation. The three stages of phase II are shown, with a brief description of testing activities taking place during that stage. The figure is a two page spread and continued overleaf. It is intended to serve as a worksheet to be developed for each selected Phase II evaluation/qualification planned for Phase II.

pads will be tested for compliance with bond strength requirements per MIL Standard 883D Method 2011.7 conditions C and F. Test 6 will be repeated after temperature cycling and burn-in.

Test Method 7. Burn-in Test

KGD carrier will undergo burn-in per MIL Standard 883D Method 1015.8 . Test method for contact resistance (test method 4) will be applied during burn in. Visual inspection per

II Test Plan



Qualification Test Flow

MIL Standard 883D Method 2009.8 will be performed after burn in.

Test Method 8. Thermal Resistance

KGD carrier will be tested for its thermal resistance per MCC specified thermal resistance test. The KGD carriers' thermal resistance will be tested using two test methods. One method would be to measure the junction-to-ambient thermal resistance in a forced or free convection environment. This method

could be similar to the SEMI specification G38, with the exception of using a thin film resistor sputtered on silicon rather than a thermal test chip. Another method would be to measure junction-to-ambient and junction-to-case thermal resistances in a system which uses a flat cooling surface to a cold plate for its primary heat transfer mechanism.

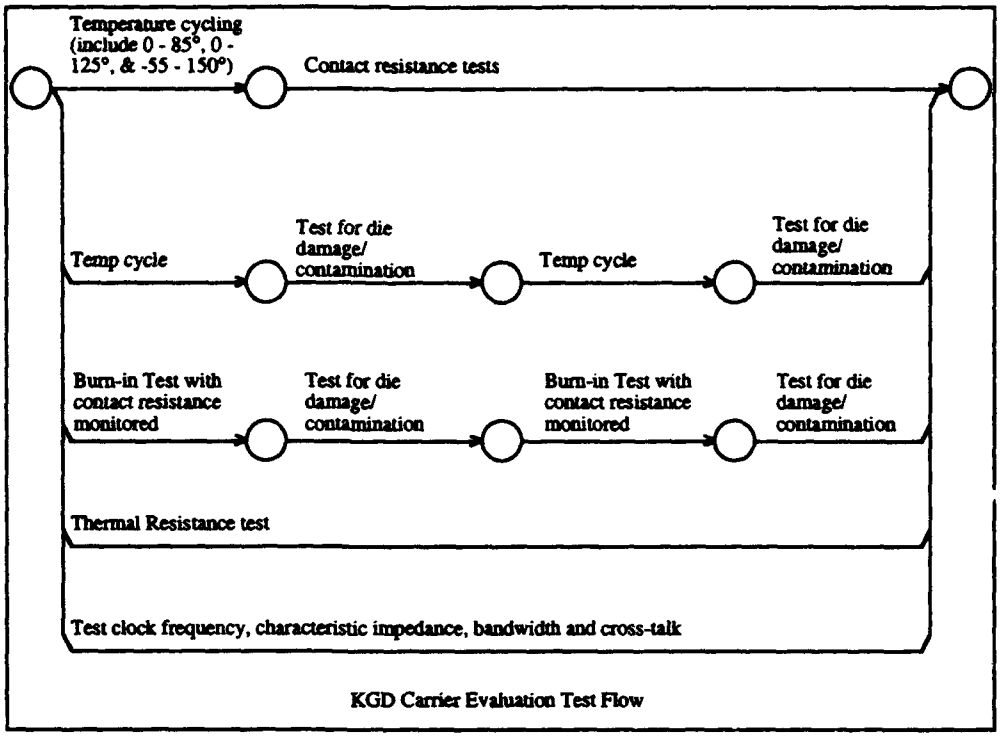


Figure 3: This figure shows the sequence in which the selected KGD carriers will be evaluated in accordance to the TAG test methods

Test Method 9. Contact Resistance During Burn In

KGD carrier interconnect will be tested for its contact resistance per MIL Standard 883D Method 3017.3.3 during the test method for burn-in (test method 7). Contact resistance must be less than or equal to 0.5 Ω.

Figure 3 shows the sequence of tests which will be done in conjunction with the Phase II evaluation of KGD carriers.

The above test methods were developed to characterize particular KGD approaches using the TAG guidelines. One additional test that has not been specified, but which we will recommend as part of the Phase II evaluation is to determine number of reuses. MCC will recommend to the Phase II subcommittee that a test (or series of tests) be identified to evaluate number of carrier assemblies (die load/unload), time at temperature and number of temperature cycles. This additional testing recommendation is the result of our cost modeling work which suggests that number of reuses of KGD carriers is a key cost driver.

The KGD program will tool suppliers to build these carriers for particular die specifications. Each carrier supplier will team with an IC supplier and tool for providing test and burn-in for a specific die. In other words, each carrier supplier will be tooled to accommodate a different die.

1.2 IC Supplier Tasks for Phase II Evaluation

The IC supplier will be responsible for performance of the following tasks for the Phase II evaluation.

Procure and supply the required numbers of dummy (ink dot) die for the KGD Technology demonstration for Phase II evaluation.

Contract with a selected KGD carrier Supplier

Design and fabricate the test sockets for the test and burn-in boards for the production device to be used in the demonstration.

Provide the KGD carrier supplier with all documentation necessary to fabricate the test and burn-in sockets and carriers.

Supply a number of example die for the Phase II evaluation.

Design and procure the test board for interfacing to carrier's socket.

Perform thermal analysis

Establish burn-in temperature to emulate existing production burn-in junction temperature levels.

2.0 Phase II Qualification

The Phase II advisory committee will recommend selection of one or two carriers for full qualification testing. The selection will be based primarily on the carrier's capability to meet the test and burn-in requirements of the specific die for which it has been tooled. This capability will be determined in Phase II evaluation using the test methods based on the TAG (as described above). Qualification testing will take place in the IC supplier's factory on a limited number of die (our test plan calls for 100 devices or less). The Phase II steering committee has developed a minimal qualification plan. Since the goal for the qualification is to develop the capability to supply KGD in a particular supplier's IC fab line, the expectation is that the IC supplier will have additional testing before the KGD technology is fully qualified to be used in production.

2.1 Phase II Qualification Tasks

The IC supplier will use the following test procedures as minimum recommended qualification requirements. Each IC supplier will add additional tests or more stringent procedures if required to facilitate full qualification in their fab line.

Modify the existing production device fixtures, loadboards, test programs, etc. to work with the carrier test socket.

Supply the required numbers of functional die for the qualification plan

Visually inspect each die after die is assembled into carriers

Functionally test each die in KGD carrier.

Burn-in each die using the KGD carriers.

The thermal environment should be maintained as close as possible to the production burn-in levels at the IC junctions. Monitor devices to assure continuous electrical contact. Test each die after burn-in using the KGD carrier.

Package devices to standard production requirements.

A subgroup control lot should be used only if similar accelerated life test data is not available from the production devices.

Accelerated Life Test Minimum Requirements

If the final package is a hybrid or multi-chip module, accelerated life test the package with a KGD device per Mil-H-38534 group C requirements.

If final package is a single chip device, then use Mil-H-38535 table V group C steady state life test, which requires 45 func-

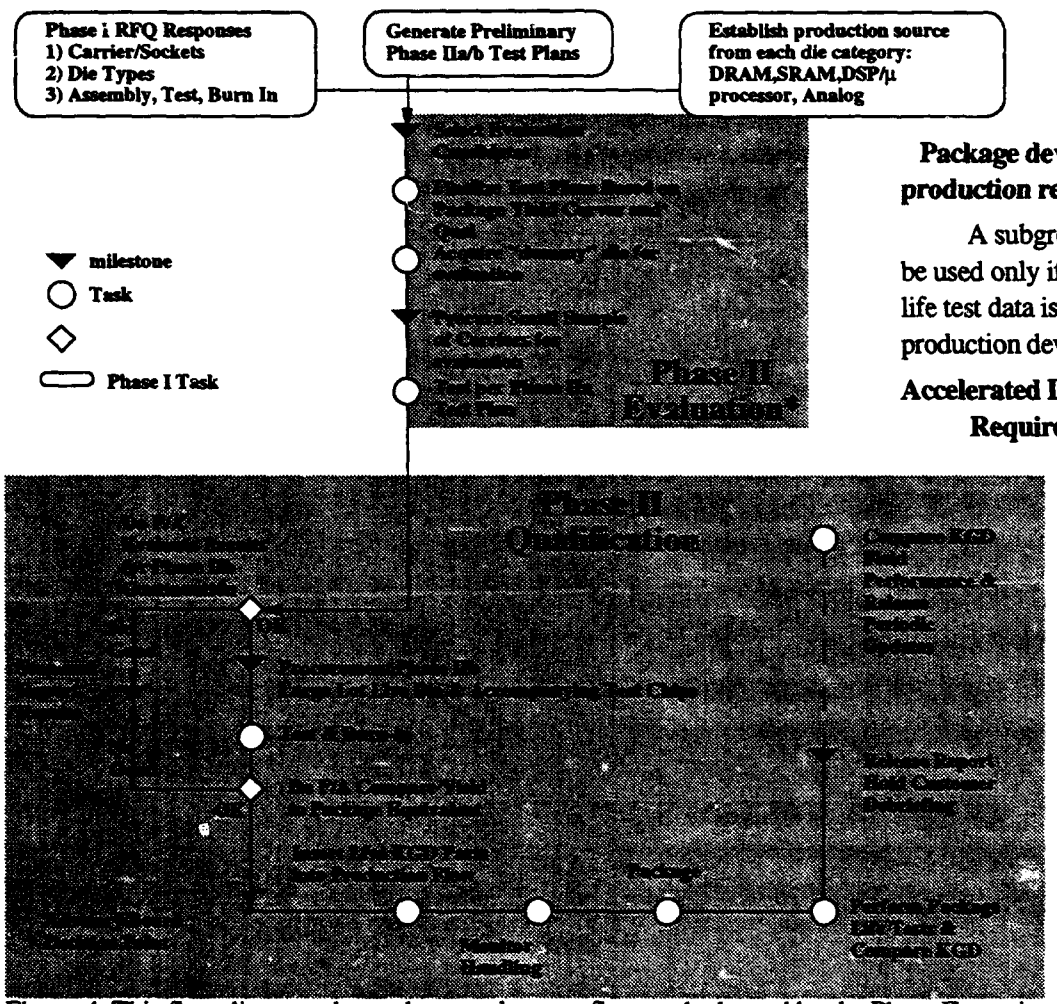


Figure 4. This flow diagram shows the complete test flow as devleoped by the Phase II steering committee.

tional parts.

Temperature Cycle

5 samples from above accelerated life tests will be subjected to temperature cycle per MIL-STD-883, Method 1010 Condition A(-55 to 85 C) at intervals of 100 cycles and electrically tested. Temperature cycling is to continue till failure or 1000 cycles, whichever occurs first.

Provide a final report documenting all testing and test results.

Once qualification is complete, the IC supplier will have the capacity to begin selling KGD based on the selected approach.

3.0 Phase II Product Insertion

The final stage of Phase II is a product insertion. At this stage, the IC supplier will have developed a qualified process for producing KGD and will be providing die into an application. We will acquire data on the KGD shipped into the product to determine the efficacy and cost effectiveness of the process.

3.1 Production Insertion Tasks

Provide KGD production insertion information.

This includes actual cost figures which can be used to compare test strategies.

Document all qualification additions or changes in writing to MCC.

The IC supplier will perform failure analysis on all failures as they occur and send documentation and failed parts to MCC.

3.2 Phase II RFQ Responses

The following companies have indicated they will quote either carriers, die or test and burn-in services for Phase II.

4.0 Conclusion

The quotations from the companies have been evaluated according to the criteria specified in the RFQs.

Criteria	Importance
Technical	40%
Schedule	30%
Cost	20%
Management	10%

The final selection of KGD technologies to be evaluated in Phase II will be made when the Phase II plans are approved by ARPA. The details of the Phase II testing, schedules and milestones will be developed with the KGD Task Group subcommittee when the exact KGD carriers, die and test and burn-in requirements are selected.

Company	Will Quote	Teamed With	Product	Die
Aehr Test Systems	Carrier, T & BI	Harris(die)	Fiber-optic Xmtr	136 lead, 6mm^2
Hughes (TRB)	Carrier, T & BI, die	NA		Various
Packard-Hughes	Carrier,	Harris (die, T & BI)	Radio Receiver	145 lead, DSP
IBM	Carrier, T & BI, die	NA	Various	Various
Fresh Quest	Carrier	Nat'l (die, T & BI)	Telecom	Memory
Micron	Carrier, T & BI, die	NA		Memory
Tribotech	Carrier	Phillips (die, T&BI)	Automotive	Microcontroller
TI/MMS	Carrier	Chip Supply (die, T & BI)		Memory
Johnstech	Carrier,	Micro SMT (die, T&BI)	Display	Display Driver
Qual High	Carrier	Nat'l (die, T & BI)	Telecom	Logic
California Contacts	Carrier	None		NA

Table 1. List of companies which have responded to the RFQs issued in Phase I. Most of the carrier suppliers are teamed with IC suppliers (or MCM assemblers).

Appendix II-A:

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MCC TECHNICAL REPORT
HVE-093-93

RFQ: Fabrication of Known Good Die Test and Burn-in Carriers

Request for Quotation - **Fabrication of Known Good Die Test and Burn-in Carriers**

Reference:

1) Technology Assessment Guideline for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product, Revision 2.5.
2) Statement of Work for the Procurement of Known Good Die, HVE-092-93.
3) Standard for Known Good Die, JEDEC modified Version 2.0, 18 May 1993, as submitted for ballot.
4) Standard for Flip Chip Known Good Die (FCKGD), working Version 1.0, 22 July 1993, based upon JEDEC Wire Bonded KGD ballot version.

Microelectronics and Computer Technology Corporation, Known Good Die (hereinafter referred to as "MCC, KGD") is hereby requesting a firm, fixed-priced Quotation for the below-mentioned products and services as specified in the work section of this RFQ. Please pay close attention to the Quotation parameters, direct omissions may cause your inputs to be non-acceptable.

Section I - Material Quotation

I. The Work

The Supplier shall furnish materials, supplies, services, special manufacturing aids, and facilities not furnished by the Buyer. The Supplier shall perform the work necessary to fabricate, assemble, test, and deliver the items specified below in accordance with the schedules, instructions, specifications and documents.

Any drawings referenced in this document and any other specifications and documents referenced herein, are hereby incorporated and made a part hereof, and shall be applicable to all work listed below. Deliverable items shall be provided in accordance with the attached Statement of Work.

The receiving party of this RFQ agrees to disclose such proprietary information necessary to sufficiently describe and document the Known Good Die Assurance Technology Devices (hereinafter referred to as "KGD ATD") and methods to be used by the Supplier. This information is to be clearly marked as confidential and proprietary in order that MCC, KGD may adequately protect this information. MCC, KGD agrees to protect this proprietary information according to prior agreement with the Supplier, and to reveal such proprietary information only to its employees with a need-to-know, and not to any third party.

****Accepting this RFQ Constitutes Agreement****

II. Deliverable Items/Descriptions

The Supplier is requested to submit a cost for each item of his preference listed below in accordance with the attached Technology Assessment Guidelines (reference 1). However, cost should include at a minimum one choice of items 1 through 4 and must include items 5 and 6. Each item should be priced separately with purchase order awards being on an item by item basis. Supplier should estimate the number of components (including yield loss) of each type required to yield the as specified quantities for each item. This yield loss estimate for each item should be included in the Quotation.

The same Technology Assessment Guidelines will be used to evaluate all KGD ATD methodologies. The dash number (xx) will be used to identify specific characteristics of an individual KGD integrated circuit category. To date the dash number refers to the following specific KGD die types:

Device Type	Test Vehicle Description
-01	DRAM memory
-02	SRAM memory
-03	ASIC, DSP, or µProcessor
-04	Mixed signal or analog integrated circuit

The device carrier (for carrier based methodologies) shall be as defined per the vendor specification. Devices shall be connected to the carrier using wire bond, tape automated bonding (TAB), and/or other technologies. Drawings of the device carriers and descriptions of their use and cost are to be provided by the Supplier.

Item	Quantity	Description	Buyer-Supplier Responsibilities
1)	100 500 1000	KGD ATDs for DRAM IC components, completely screened and tested to the quality assurance provisions of vendor specifications.	The Supplier should bid this item with the Buyer supplying the (bumped or unbumped) die, sort tested per reference 2. All other required components/parts are the Supplier responsibility. Primarily these are discrete IC carriers or temporary packages, and do not include any required additional components. Any deviations in additional components required are to be identified by the Supplier and included in the cost of this quotation.
2)	100 500 1000	Same KGD ATDs as item 1) above with the exception that carrier should be for SRAM IC components.	The Supplier should bid this item in the same way as item 1) above.
3)	100 500 1000	Same KGD ATDs as item 1) above with the exception that carrier should be for Microprocessor, Digital Signal Processor, or Application Specific Integrated Circuit class of components.	The Supplier should bid this item in the same way as item 1) above.
4)	100 500 1000	Same KGD ATDs as item 1) above with the exception of carrier should be for Analog or Mixed Signal class of integrated circuit components.	The Supplier should bid this item in the same way as item 1) above.
5)	100 500 1000	Continuity testing of carriers in items 1 through 4 above.	The cost quote should indicate the cost of electrically testing the carriers in each of the four categories above, in each of the requested pricing quantities.
6)	100 500 1000	Quality Conformance Inspection of carriers in items 1 through 4 above.	The cost quote should indicate the cost of inspecting the carriers in each of the four categories above, in each of the requested pricing quantities. If a sampling plan is used, the specifics of that plan should be outlined in the cost quotation.

III. Delivery Schedule

Component	Date
1) Response to RFQ	8/6/93
2) Expected purchase order (PO) release date is	10/1/93
3) Carrier Delivery	1Q94

The following Buyer furnished data and components will be made available with the purchase order.
1) Integrated circuit specifications, including power dissipation requirements.
2) Top layer layout of integrated circuit bond pads in GDSII or Gerber format.

IV. Submission of Quotations

The Quotation must be signed by an official authorized to contractually bind the offerer.

It is required that your Quotation be valid for a period of not less than 90 days from the submission date specified. Quotations may be modified or withdrawn by written or electronic communication notice received at any time prior to award. Quotations may be withdrawn in person by an officer or authorized representative, provided his identity is made known and he/she signs a receipt for the offer prior to award.

V. Order of Precedence

In the event of any inconsistency between the Request for Quotation and any specification or other provisions which are made a part of the Request for Quotation by reference or otherwise, the order of precedence shall be as follows:

1. Purchase Order.
2. Typed provisions in this Request for Quotation (RFQ).
3. Subcontractor Data Requirements List (SDRL), if applicable.
4. Other provisions of this RFQ when attached or incorporated by reference.

VI. Notice to Offerers

Offerers are cautioned to initially submit their most favorable Quotation, price, and other factors considered.

This RFQ does not commit MCC, KGD to award a contract. MCC, KGD reserves the right to reject any or all Quotations or to negotiate separately with any source considered qualified, and to waive informalities and minor irregularities in offers received. MCC, KGD shall not be liable to offerer for any costs incurred by offerer as a result of the submission of its Quotation in reply hereto.

VII. Late Quotations

MCC, KGD reserves the right to consider Quotations or modifications thereof received after the date indicated for such purpose, but before award is made, should such action be in the best interest of MCC, KGD. However, on time submittals will be given precedence.

Section II - Instructions for Quotation Preparation and Submission

I. Objectives

This section describes the requirements for preparing and submitting the requested Quotation. The instructions provided herein must be carefully followed inasmuch as substantial deviations,

qualifications, or omissions of essential data could result in your Quotation being considered non-responsive and, therefore, ineligible for subsequent contract award consideration.

II. Number of Copies

Submit the specified quantities of each Quotation as defined below to the address listed below.

1. 3 copies of the Management Quotation (Optional).
2. 3 copies of the Technical Quotation (Required).
3. 3 copies of the Cost Quotation (Required.)

Submit quotations to:
Brenda Ulbricht
12100 Technology Blvd.
Austin, TX 78746

-or-

FAX your Quotation to Larry Gilg at (512) 250-2893.

III. Management Quotation (Optional for this requirement)

The Management Quotation shall include the following information as a minimum:

1. Summary of your company capabilities and history, which should include a history of the business, business record and current business base.
2. Summary of your company manpower and identification of key personnel. A Program Manager may be required for the work specified herein.
3. A chart of the organization to be used in the performance of the effort. Identify key technical and management personnel assigned and indicate their function, responsibilities, and percent of time committed to this effort. Provide resumes for key personnel.

IV. Cost and Pricing Data (Subsequent Cost Quotation)

A. The Supplier shall segregate the cost as follows, if applicable and in accordance with each deliverable item per section I, paragraph II:

Cost Line Item	Recurring Cost	Non-Recurring Cost
KGD ATD Design/Layout	N/A	Required
KGD ATD Fabrication Cost	Required	Required
KGD ATD Open and Shorts Test	Required	Required
KGD ATD QCI inspection	Required	Required

V. Technical Quotation (Required)

The Technical Quotation shall provide a thorough understanding of the offeror's approach to satisfying the requirements of the Technology Assessment Guidelines (reference 1). This should include the Supplier capability to meet all of the requirements of the Technology Assessment Guidelines (TAG) and specif.. indications of failures to meet the TAG requirements. All information requested in the TAG should be fully described here.

Your Technical Quotation shall be organized according to the following format and shall include the following topics as a minimum:

1. Introduction

2. Requirements

3. Approach to satisfy technical requirements (include the identity of the person who has responsibility for the technical requirements being satisfied.
   A. Design definition including detailed definition of KGD ATD and assembly designs.
   B. Perform thermal analysis of the KGD ATDs; verify an adequate thermal path for the IC.
   C. Rationale for KGD approach, detailing advantages and disadvantages.
   D. Risk or areas of concern.
   E. Mechanical parameters (bonding and die attach requirements).
   F. Design reviews of KGD ATD in conjunction with MCC, KGD personnel.
   G. Technical documentation as defined in Technology Assessment Guidelines (reference 1).
   H. Compliance to this RFQ requires a response to each of the following items:
      1. Estimate the total quantity of each KGD ATD component type required to yield the specified KGD ATD quantities per section I, paragraph II deliverables.
      2. A preliminary parts list and physical layout of the KGD ATDs that will be required for each IC category (DRAM, SRAM, µP/DSP/ASIC, Analog). It is required that the Supplier acknowledge that layout deviations are required and a delivery date for these layouts in GDSII format must be identified to meet intent of this Quotation. The assembly constraint design rules should be supplied if different from the Technology Assessment Guidelines.
   I. Any Supplier using subcontract work for this effort must identify in their Quotation the tasks to be subcontracted and the subcontractor.
   J. Buyer requires that the Supplier provide a cost and schedule risk assessment of the processes and technologies proposed by the Supplier to meet the requirements of the Technology Assessment Guidelines. Alternatives to high risk items should be identified.

4. Testing Plan - Per Statement of Work
   A. Electrical Acceptance Testing (opens and shorts)
   B Quality Conformance Inspection (indicate full inspection or sampling plan and inspection criteria).

5. Table of Compliance
   Explain the methods and technical approach by which you propose to satisfy the technical requirements exhibited by the Technology Assessment Guidelines (reference 1). Describe specifically how you plan to accomplish the objectives and tasks. Provide sketches, drawings, flow diagrams, and charts as appropriate. Discuss alternative solutions explored, analyzed, and rejected, and the reasons for the rejections. Include a statement of any assumptions made by you as to the definition of the requirements.

   In addition to the Technology Assessment Guidelines, the KGD ATDs shall be evaluated for susceptibility to damage or loss of electrical contact due to mechanical shock encountered during normal handling .

Section III - Conclusion

I. Quotation Evaluation

Quotations submitted may be evaluated in strict accordance with the criteria listed below in order of importance:

Criteria	Importance
Technical	40%
Schedule	30%
Cost	20%
Management	10%

II. Technical Contact

Any questions of a technical nature may be directed to Mr. Chad Noddings, at (512) 250-2863.

III. Special Note

Offerer shall confirm receipt of this RFQ and advise MCC, KGD, in writing, no later than **close of business August 6, 1993** of his intent to submit a Quotation in accordance with these instructions. Please supply the requested information to fill in the TAG by **close of business August 16, 1993.**

It is requested that the Offerer formally respond to this Request for Quotation on or before the **close of business on September 1, 1993**. Please forward your final Quotation to the undersigned at the aforementioned address, as well as, any formal questions you may have in the proposing process. Thank you for your time and attention in this matter.

MCC TECHNICAL REPORT
HVE-094-93

RFQ: Integrated Circuits for Use in Known Good Die Process Evaluation

Request for Quotation - **Integrated Circuits for Use in Known Good Die Process Evaluation**

Reference:

1) Technology Assessment Guideline for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product, Revision 2.5.
2) Statement of Work for procurement of Known Good Die, HVE-092-93.
3) Standard for Known Good Die, JEDEC modified Version 2.0, 18 May 1993, as submitted for ballot.
4) Standard for Flip Chip Known Good Die (FCKGD), working Version 1.0, 22 July 1993, based upon JEDEC Wire Bonded KGD ballot version.

Microelectronics and Computer Technology Corporation, Known Good Die (hereinafter referred to as "MCC, KGD") is hereby requesting a firm, fixed-priced Quotation for the below mentioned products and services as specified in the work section of this RFQ. Please pay close attention to the Quotation parameters, direct omissions may cause your inputs to be non-acceptable.

Section I - Material Quotation

I. The Work

The Supplier shall furnish materials, supplies, services, special manufacturing aids, and facilities not furnished by the buyer. The Supplier shall perform the work necessary to fabricate, assemble, inspect, and deliver the items specified below in accordance with the schedules, instructions, specifications and referenced documents.

Any drawings referenced in this document and any other specifications and documents referenced herein, are hereby incorporated and made a part hereof, and shall be applicable to all work listed below. Deliverable items shall be provided in accordance with the attached Statement of Work.

The receiving party of this RFQ agrees to disclose such proprietary information necessary to sufficiently describe and document the Known Good Die Integrated Circuit methods to be used by the Supplier (references 3, 4). This information is to be clearly marked as confidential and proprietary in order that MCC, KGD may adequately protect this information. MCC, KGD agrees to protect this proprietary information according to prior agreement with the Supplier, and to reveal such proprietary information only to its employees with a need-to-know, and not to any third party.

****Accepting this RFQ Constitutes Agreement****

II. Deliverable Items/Descriptions

The Supplier is requested to submit a cost for each item of his preference listed below in accordance with the attached Technology Assessment Guidelines (reference 1). However, cost should include at a minimum one choice of items 1 through 4 and must include item 5. Each item should be priced separately with purchase order awards being on an item by item basis (for items 1 through 4, with item 5 awarded with each of items 1 through 4). Some KGD technologies require solder bumped die, others require aluminum bond pads. Please quote the die in each format, and indicate where die are not available in a particular format. Supplier should estimate the number of components (including yield loss) of each type required to yield the as specified quantities for each item. This yield loss estimate for each item should be included in the quotation.

The JEDEC Standard for Known Good Die will be used to evaluate all KGD methodologies (references 3, 4). The dash number (-xx) will be used to identify specific characteristics of an

individual KGD integrated circuit category. To date the dash number refers to the following specific KGD die types:

Device Type	Test Vehicle Description
-01	DRAM memory
-02	SRAM memory
-03	ASIC, DSP, or µProcessor
-04	Mixed signal or analog integrated circuit

The device carrier (for carrier based methodologies) shall be as defined per the carrier vendor specification. Devices shall be connected to the carrier using wire bond, tape automated bonding (TAB), and/or other technologies. Drawings of the device carriers and descriptions of their use and cost are to be provided by the Supplier.

Item	Quantity	Description	Buyer-Supplier Responsibilities
1)	100 500 1000	KGD DRAM IC components (-01)	The Supplier should bid this item with the Buyer supplying the (bumped or unbumped) die, sort tested per reference 2. All other required components/parts are the Supplier responsibility. Any additional processing steps (i.e., wafer bumping) required are to be identified by the Supplier and included in the cost of this quotation. This item should not include the costs associated with sort testing; those costs should be quoted separately under item (5). This item should include the costs associated with wafer saw and pick and place into a wafflepack die carrier for delivery to the Buyer.
2)	100 500 1000	KGD SRAM IC components (-02)	The Supplier should bid this item in the same way as item 1) above.
3)	100 500 1000	ASIC, DSP, or Micro-processor IC components (-03)	The Supplier should bid this item in the same way as item 1) above.
4)	100 500 1000	KGD Mixed Signal or Analog IC components (-04)	The Supplier should bid this item in the same way as item 1) above.
5)	100 500 1000	Wafer sort testing (including gross functional and parametric testing) of ICs in items 1 through 4 above.	The cost quote should indicate the cost of sort testing the ICs on wafers in each of the four categories above, in each of the requested pricing quantities. It is expected that the Supplier will coordinate with internal facilities for wafer saw and pick and place to transfer die failure information.

III. Delivery Schedule

Component	Date
1) Response to RFQ	8/16/93
2) Supply price quotation	9/1/93
2) Expected purchase order (PO) release date is	10/1/93
3) Known Good Die Delivery	1Q94

The following Supplier furnished data and components will be made available with the integrated circuits:

1) Integrated circuit specifications, including power dissipation requirements.
2) Top layer (bond pad) layout of integrated circuit bond pads in GDSII or Gerber format.
3) In the case that a third party is expected to perform test and burn-in of the integrated circuits, the IC Supplier is expected to cooperate with MCC and the third party test and burn-in Supplier, using non-disclosure agreements, to provide a test program in a usable format to the third party test and burn-in Supplier.

IV. Submission of Quotations

The Quotation must be signed by an official authorized to contractually bind the offerer.

It is required that your Quotation be valid for a period of not less than 90 days from the submission date specified. Quotations may be modified or withdrawn by written or electronic communication notice received at any time prior to award. Quotations may be withdrawn in person by an officer or authorized representative, provided his/her identity is made known and he/she signs a receipt for the offer prior to award.

V. Order of Precedence

In the event of any inconsistency between the Request for Quotation and any specification or other provisions which are made a part of the Request for Quotation by reference or otherwise, the order of precedence shall be as follows:

1. Purchase Order
2. Typed provisions in this Request for Quotation (RFQ).
3. Subcontractor Data Requirements List (SDRL), if applicable.
4. Other provisions of this RFQ when attached or incorporated by reference.

VI. Notice to Offerers

Offerers are cautioned to initially submit their most favorable quotation, price, and other factors considered.

This RFQ does not commit MCC, KGD to award a contract. MCC, KGD reserves the right to reject any or all Quotations or to negotiate separately with any source considered qualified, and to waive informalities and minor irregularities in offers received. MCC, KGD shall not be liable to offerer for any costs incurred by offerer as a result of the submission of its Quotation in reply hereto.

VII. Late Quotations

MCC, KGD reserves the right to consider Quotations or modifications thereof received after the date indicated for such purpose, but before award is made, should such action be in the best interest of MCC, KGD. However, on time submittals will be given precedence.

Section II - Instructions for Quotation Preparation and Submission

I. Objectives

This section describes the requirements for preparing and submitting the requested Quotation. The instructions provided herein must be carefully followed inasmuch as substantial deviations, qualifications, or omissions of essential data could result in your Quotation being considered non-responsive and, therefore, ineligible for subsequent contract award consideration.

II. Number of Copies

Submit the specified quantities of each Quotation as defined below to the address listed below.

1. 3 copies of the Management Quotation (Optional).
2. 3 copies of the Technical Quotation (Required).
3. 3 copies of the Cost Quotation (Required.)

Submit quotations to:
Brenda Ulbricht
12100 Technology Blvd.
Austin, TX 78746

-or-

FAX your Quotation to Larry Gilg at (512) 250-2893.

III. Management Quotation (Optional for this requirement)

The Management Quotation shall include the following information as a minimum:

1. Summary of your company capabilities and history, which should include a history of the business, business record and current business base.
2. Summary of your company manpower and identification of key personnel. A Program Manager may be required for the work specified herein.
3. A chart of the organization to be used in the performance of the effort. Identify key technical and management personnel assigned and indicate their function, responsibilities, and percent of time committed to this effort. Provide resumes for key personnel.

IV. Cost and Pricing Data (Subsequent Cost Quotation)

A. The Supplier shall segregate the cost as follows if applicable and in accordance with each deliverable item per section I, paragraph II :

Cost Line Item	Recurring Cost	Non-Recurring Cost
Integrated Circuit Fabrication	Required	N/A
Integrated Circuit Sort test	Required	N/A
Other costs	Required	Required

V. Technical Quotation (Required)

The Technical Quotation shall provide a thorough understanding of the offeror's integrated circuit components which are to be evaluated in accordance with the requirements of the JEDEC Standard for Known Good Die (references 3, 4). This should include the Supplier capability to meet all of the requirements of this standard and specific indications of failures to meet these requirements.

Your Technical Quotation shall be organized according to the following format and shall include the following topics as a minimum:

1. Introduction

2. Requirements

3. Approach to satisfy technical requirements (include the identity of the person who has responsibility for the technical requirements being satisfied.
   A. Integrated circuit definition including detailed data sheet with parametric and functional performance specifications.
   B. Mechanical parameters (bonding and die attach requirements).
   C. Risk or areas of concern.
   D. Technical documentation as defined in JEDEC Standard for Known Good Die (references 3, 4).
   E. Estimate the total quantity of each integrated circuit component type required to yield the specified KGD quantities per section I, paragraph II deliverables.

4. Testing Plan - Per Statement of Work
   A. Wafer sort testing, to be performed by the integrated circuit Supplier to screen out grossly defective die. This testing is to include both parametric and gross functional testing, per the vendor normal sort test specifications. Please include these specifications and any guardbands applied during sort testing with your quotation.
   B. Quality Conformance Inspection (indicate full inspection or sampling plan and inspection criteria). Inspections are to be performed on outgoing integrated circuit die.

5. Reinsertion Plan - Per Statement of Work
   Following the burn-in and testing of these dice in carriers for assurance as known good die, they are to be disassembled and returned to the IC manufacturer for reinsertion into the high reliability packaging which these parts are normally offered in. If possible, they are then to be included into products (preferably module or hybrid products, for which this project targets die qualification) and the lifetime reliability of these parts monitored throughout the manufacturer normal warranty period for any excessive failures. Please present a detailed plan for accomplishing this task.

Section III - Conclusion

I. Quotation Evaluation

Quotations submitted may be evaluated in strict accordance with the criteria listed below in order of importance:

Criteria	Importance
Technical	40%
Schedule	30%
Cost	20%
Management	10%

II. Technical Contact

Any questions of a technical nature may be directed to Mr. Chad Noddings, at (512) 250-2863.

III. Special Note

Offerer shall confirm receipt of this RFQ and advise MCC, KGD, in writing, no later than **close of business August 16, 1993** of his intent to submit a Quotation in accordance with these instructions.

It is requested that the Offerer formally respond to this Request for Quotation on or before the **close of business on September 1, 1993**. Please forward your final Quotation to Brenda Ulbricht at the aforementioned address, as well as any formal questions you may have in the proposing process. Thank you for your time and attention in this matter.

MCC TECHNICAL REPORT
HVE-095-93

RFQ: Assembly, Test, Burn-in, Disassembly, and Quality Conformance Inspection of Known Good Die

Request for Quotation - **Assembly, Test, Burn-in, Disassembly, and Quality Conformance Inspection of Known Good Die**

Reference:

1) Technology Assessment Guideline for Methods, Materials and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product, Revision 2.5/
2) Statement of Work for Procurement of Known Good Die, HVE-092-93.
3) Standard for Known Good Die, JEDEC modified Version 2.0, 18 May 1993, as submitted for ballot.
4) Standard for Flip Chip Known Good Die (FCKGD), working Version 1.0, 22 July 1993, based upon JEDEC Wire Bonded KGD ballot version.

Microelectronics and Computer Technology Corporation, Known Good Die (hereinafter referred to as "MCC, KGD") is hereby requesting a firm, fixed-priced Quotation for the below mentioned products and services as specified in the work section of this RFQ. Please pay close attention to the Quotation parameters, direct omissions may cause your inputs to be non-acceptable.

Section I - Material Quotation

I. The Work

The Supplier shall furnish materials, supplies, services, special manufacturing aids, and facilities not furnished by the Buyer. The Supplier shall perform the work necessary to fabricate, assemble, inspect, and deliver the items specified below in accordance with the schedules, instructions, specifications and referenced documents.

Any drawings referenced in this document and any other specifications and documents referenced herein, are hereby incorporated and made a part hereof, and shall be applicable to all work listed below. Deliverable items shall be provided in accordance with the attached Statement of Work.

The receiving party of this RFQ agrees to disclose such proprietary information necessary to sufficiently describe and document the Known Good Die Assurance Technology Devices (hereinafter referred to as "KGD ATD") and methods to be used by the Supplier. This information is to be clearly marked as confidential and proprietary in order that MCC, KGD may adequately protect this information. MCC, KGD agrees to protect this proprietary information according to prior agreement with the Supplier, and to reveal such proprietary information only to its employees with a need-to-know, and not to any third party.

****Accepting this RFQ Constitutes Agreement****

II. Deliverable Items/Descriptions

The Supplier is requested to submit a cost for each item of his preference listed below in accordance with the attached Technology Assessment Guidelines (reference 1). However, cost should include at a minimum one choice of items 1 through 4 and must include items 5, 6, and 7. Each item should be priced separately with purchase order awards being on an item by item basis. Supplier should estimate the number of components (including yield loss) of each type required to yield the as specified quantities for each item. This yield loss estimate for each item should be included in the Quotation.

The same Technology Assessment Guidelines will be used to evaluate all KGD methodologies. The dash number (-xx) will be used to identify specific characteristics of an individual KGD integrated circuit category. To date the dash number refers to the following specific KGD die types:

Device Type	Test Vehicle Description
-01	DRAM memory
-02	SRAM memory
-03	ASIC, DSP, or µProcessor
-04	Mixed signal or analog integrated circuit

The device carrier (for carrier based methodologies) shall be as defined per the vendor specification. Devices shall be connected to the carrier using wire bond, tape automated bonding (TAB), and/or other technologies. Drawings of the device carriers and descriptions of their use and cost are to be provided by the Supplier.

Item	Quantity	Description	Buyer-Supplier Responsibilities
1)	100 500 1000	KGD DRAM IC components (-01), completely screened and tested to the quality assurance provisions of vendor specifications.	The Supplier should bid this item with the Buyer supplying the (bumped or unbumped) die, sort tested per reference 2, and the required KGD ATD for those parts. All other required components/parts are the Supplier responsibility. Any additional components required are to be identified by the Supplier and included in the cost of this quotation. This item includes assembly of ICs into the KGD ATDs for test and burn-in, and disassembly afterward. It does not include costs associated with test and burn-in, which will be considered separately in items 5) and 6).
2)	100 500 1000	KGD SRAM IC components (-02), completely screened and tested to the quality assurance provisions of vendor specifications.	The Supplier should bid this item in the same way as item 1) above.
3)	100 500 1000	KGD ASIC, DSP, or Microprocessor IC components (-03), completely screened and tested to the quality assurance provisions of vendor specifications.	The Supplier should bid this item in the same way as item 1) above.
4)	100 500 1000	KGD Mixed Signal or Analog IC components (-04), completely screened and tested to the quality assurance provisions of vendor specifications.	The Supplier should bid this item in the same way as item 1) above.
5)	100 500 1000	Electrical functional and parametric testing of ICs in KGD ATDs in items 1 through 4 above.	The cost quote should indicate the cost of electrically testing the ICs mounted in KGD ATDs in each of the four categories above, in each of the requested pricing quantities. The Buyer will cooperate with the Supplier and IC Supplier to provide the required test program(s) in a suitable format.

Item	Quantity	Description	Buyer-Supplier Responsibilities
6)	100 500 1000	Dynamic monitored burn-in of ICs in KGD ATDs in items 1 through 4 above.	The cost quote should indicate the cost of performing an electrically active and monitored burn-in test of each of the assembled KGD ATDs in each of the four categories above, in each of the requested pricing quantities.
7)	100 500 1000	Outgoing Quality Conformance Inspection of integrated circuits in items 1 through 4 above.	The cost quote should indicate the cost of inspecting the die in each of the four categories above, in each of the requested pricing quantities. If a sampling plan is to be used, the specifics of that plan should be outlined in the cost quotation, along with inspection criteria.

III. Delivery Schedule

Component	Date
1) Response to RFQ	8/16/93
2) Supply quote	9/1/93
3) Expected purchase order (PO) release date is	10/1/93
4) Test and burn-in delivery begins	2Q94

The following Buyer furnished data and components will be made available with the purchase order:

1) Integrated circuit specifications, including power dissipation requirements.
2) Top layer layout of integrated circuit bond pads in GDSII or Gerber format.
3) Known Good Die Assurance Technology Devices (KGD ATD) ready for assembly.
4) Top level layout of KGD ATD in GDSII or Gerber format.

IV. Submission of Quotations

The Quotation must be signed by an official authorized to contractually bind the offerer.

It is required that your Quotation be valid for a period of not less than 90 days from the submission date specified. Quotations may be modified or withdrawn by written or electronic communication notice received at any time prior to award. Quotations may be withdrawn in person by an officer or authorized representative, provided his/her identity is made known and he/she signs a receipt for the offer prior to award.

V. Order of Precedence

In the event of any inconsistency between the Request for Quotation and any specification or other provisions which are made a part of the Request for Quotation by reference or otherwise, the order of precedence shall be as follows:

1. Purchase Order
2. Typed provisions in this Request for Quotation (RFQ).
3. Subcontractor Data Requirements List (SDRL), if applicable.
4. Other provisions of this RFQ when attached or incorporated by reference.

VI. Notice to Offerers

Offerers are cautioned to initially submit their most favorable quotation, price, and other factors considered.

This RFQ does not commit MCC, KGD to award a contract. MCC, KGD reserves the right to reject any or all Quotations or to negotiate separately with any source considered qualified, and to waive informalities and minor irregularities in offers received. MCC, KGD shall not be liable to offerer for any costs incurred by offerer as a result of the submission of its Quotation in reply hereto.

VII. Late Quotations

MCC, KGD reserves the right to consider Quotations or modifications thereof received after the date indicated for such purpose, but before award is made, should such action be in the best interest of MCC, KGD. However, on time submittals will be given precedence.

Section II - Instructions for Quotation Preparation and Submission

I. Objectives

This section describes the requirements for preparing and submitting the requested Quotation. The instructions provided herein must be carefully followed inasmuch as substantial deviations, qualifications, or omissions of essential data could result in your Quotation being considered non-responsive and, therefore, ineligible for subsequent contract award consideration.

II. Number of Copies

Submit the specified quantities of each Quotation as defined below to the address listed below.

1. 3 copies of the Management Quotation (Optional).
2. 3 copies of the Technical Quotation (Required).
3. 3 copies of the Cost Quotation (Required.)

Submit quotations to:
Brenda Ulbricht
12100 Technology Blvd.
Austin, TX 78746

-or-

FAX your Quotation to Larry Gilg at (512) 250-2893.

III. Management Quotation (Optional for this requirement)

The Management Quotation shall include the following information as a minimum:

1. Summary of your company capabilities and history, which should include a history of the business, business record and current business base.
2. Summary of your company manpower and identification of key personnel. A Program Manager may be required for the work specified herein.
3. A chart of the organization to be used in the performance of the effort. Identify key technical and management personnel assigned and indicate their function, responsibilities, and percent of time committed to this effort. Provide resumes for key personnel.

IV. Cost and Pricing Data (Subsequent Cost Quotation)

A. The Supplier shall segregate the cost as follows if applicable and in accordance with each deliverable item per section I paragraph II :

Cost Line Item	Recurring Cost	Nonrecurring Cost
KGD ATD Incoming QCI	Required	Required
Integrated Circuit Incoming QCI	Required	Required
IC Die Attach and Bonding	Required	Required
Other KGD ATD Assembly Steps	Required	Required
KGD ATD Disassembly	Required	Required
Integrated Circuit Outgoing QCI	Required	Required
Other Required Process Steps	Required	Required

V. Technical Quotation (Required)

The Technical Quotation shall provide a thorough understanding of the offeror's approach to satisfying the requirements of the Technology Assessment Guidelines (TAG) (reference 1). This should include the Supplier capability to meet all of the requirements of the TAG and specific indications of failures to meet the TAG requirements. All information requested in the TAG should be fully described here.

Your Technical Quotation shall be organized according to the following format and shall include the following topics as a minimum:

1. Introduction

2. Requirements

3. Approach to satisfy technical requirements (include the identity of the person who has responsibility for the technical requirements being satisfied.
   A. Rationale for KGD approach, detailing advantages and disadvantages.
   B. Risk or areas of concern.
   C. Mechanical parameters (bonding and die attach requirements).
   D. Design reviews of KGD test and burn-in methods in conjunction with MCC, KGD personnel.
   E. Technical documentation as defined in Technology Assessment Guidelines (reference 1), fill in as much information from the TAG as is relevant to test and burn-in.
   F. Any Supplier using subcontract work for this effort must identify in their Quotation the tasks to be subcontracted and the subcontractor.
   G. Buyer requires that the Supplier provide a cost and schedule risk assessment of the processes and technologies proposed by the Supplier to meet the requirements of the Technology Assessment Guidelines. Alternatives to high risk items should be identified.

4. Testing Plan - Per Statement of Work
   Quality Conformance Inspection (indicate full inspection or sampling plan and inspection criteria). Inspections are to be performed on incoming die and KGD ATD components, and on outgoing integrated circuit die.

5. Table of Compliance
   Explain the methods and technical approach by which you propose to satisfy the technical requirements exhibited by the Technology Assessment Guidelines (reference 1). Describe specifically, how you plan to accomplish the objectives and tasks. Provide sketches, drawings, flow diagrams, and charts as appropriate. Discuss alternative solutions explored,

analyzed, and rejected, and the reasons for the rejections. Include a statement of any assumptions made by you as to the definition of the requirements.

Section III - Conclusion

I. Quotation Evaluation

Quotations submitted may be evaluated in strict accordance with the criteria listed below in order of importance:

Criteria	Importance
Technical	40%
Schedule	30%
Cost	20%
Management	10%

II. Technical Contact

Any questions of a technical nature may be directed to Mr. Chad Noddings, at (512) 250-2863.

III. Special Note

Offerer shall confirm receipt of this RFQ and advise MCC, KGD, in writing, no later than **close of business August 16, 1993** of their intent to submit a Quotation in accordance with these instructions.

It is requested that the Offerer formally respond to this Request for Quotation on or before the **close of business on September 1, 1993**. Please forward your final Quotation to Brenda Ulbricht at the aforementioned address, as well as any formal questions you may have in the proposing process. Thank you for your time and attention in this matter.

MCC TECHNICAL REPORT
HVE-092-93

Statement of Work for the Procurement of Known Good Die

Reference

1) Technology Assessment Guideline for Methods, Materials, and Equipment Necessary to Prepare and Ship Semiconductor Devices as Fully Warranted Bare Die Product, Revision 2.5.
2) Request For Quotation for Known Good Die Assurance Technology Devices: HVE-093-93.
3) Request For Quotation for Assembly, Test, Burn-in, Disassembly, and Quality Conformance Inspection of Known Good Die: HVE-095-93.
4) Request For Quotation for Integrated Circuits for Use in Known Good Die Process Evaluation: HVE-094-93.
5) Standard for Known Good Die, JEDEC modified Version 2.0, 18 May 1993, as submitted for ballot.
6) Standard for Flip Chip Known Good Die (FCKGD), working Version 1.0, 22 July 1993, based upon JEDEC Wire Bonded KGD ballot version.

1.0 Scope

This Statement of Work describes the tasks associated with designing and fabricating Known Good Die Assurance Technology Devices (KGD ATD); screening up to four KGD ATD designs; and assembling, testing, disassembling, and performing quality conformance inspections on up to four categories of integrated circuits for MCC KGD Project per the KGD Technology Assessment Guidelines.

The vendors and processes to be used shall be selected from the responses to three separate Request For Quotation (RFQ) documents. These RFQ documents cover the following topics: 1) Known Good Die Assurance Technology Devices; 2) Assembly, Test, Burn-in, Disassembly, and Quality Conformance Inspection of Known Good Die; and 3) Integrated Circuits for Use in Known Good Die Process Evaluation. These categories may not fit the specific technologies or processes which may be applied by various vendors to solve the KGD supply issue; please respond to the RFQ which best fits your technology, or to all three. Suppliers of all phases of the KGD processing who wish to respond are expected to respond to all three as a single RFQ. Teaming between companies is encouraged in order to take advantage of optimized technologies, and to strengthen the capability for providing KGD to the marketplace.

2.0 Known Good Die Descriptions

2.1 Specification Designator

The same Technology Assessment Guidelines will be used to evaluate all KGD methodologies. The dash number (xx) will be used to identify specific characteristics of an individual KGD integrated circuit category. The dash number refers to the following specific KGD die types:

Device Type	Test Vehicle Description
-01	DRAM memory
-02	SRAM memory
-03	ASIC, DSP, or µProcessor
-04	Mixed signal or analog integrated circuit

The device carrier (for carrier based methodologies) shall be as defined per the vendor specification. Devices shall be connected to the carrier using wire bond, tape automated bonding (TAB), and/or other technologies. Drawings of the device carriers and descriptions of their use and cost are to be provided by the supplier.

3.0 Overview of Supplier/Buyer Tasks

It is anticipated that KGD ATD fabrication and screening, assembly, burn-in, high-speed functional test, disassembly, and quality conformance inspection (QCI) will be performed by the supplier(s). The buyer, in the instance where the supplier is not also the die provider, will be responsible for die procurement and the test vectors for each die type, which will be provided to the supplier. The expected overall flow for providing Known Good Die is shown in Figure 1. Each of the tasks identified in Figure 1 may be performed by independent suppliers, or the entire flow may be performed by a single supplier.

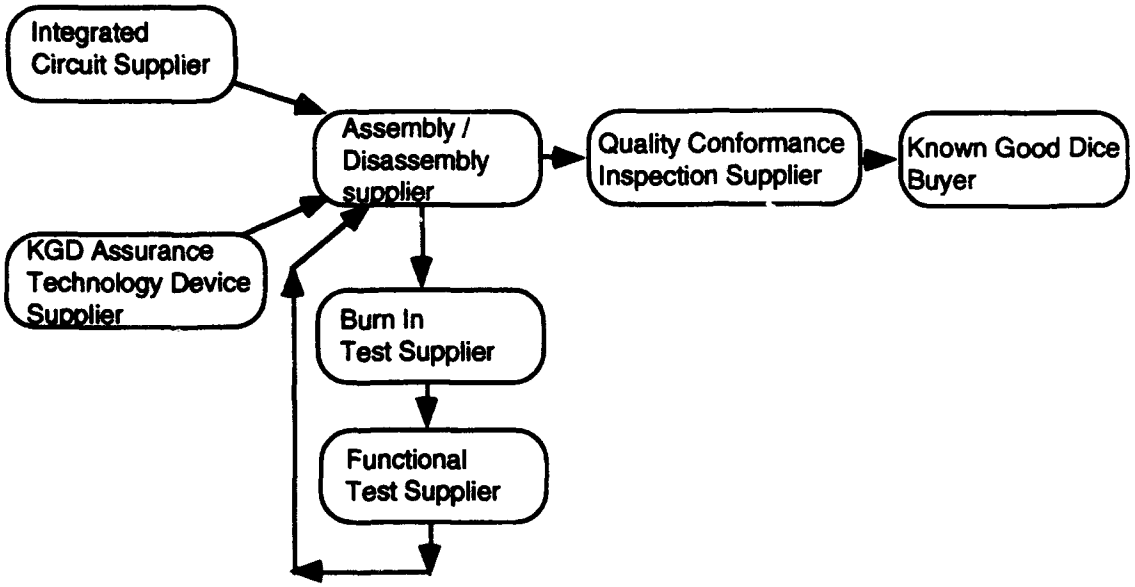


Figure 1. Expected overall process flow for providing known good die.

3.1 Supplier Tasks

3.1.1 Integrated Circuit Supplier

3.1.1.1 Provide sort-tested integrated circuit die that have been sawn and placed into waffle pack die carriers for delivery to KGD supplier.

3.1.1.2 Perform actions specified by reinsertion plan, to be agreed upon by supplier and MCC prior to assignment of purchase orders for die.

3.1.2 KGD ATD Supplier

3.1.2.1 Design/layout KGD ATDs as appropriate to TAB, wire bond, and/or all other types of bare die assembly.

3.1.2.2 Perform thermal analysis of the KGD ATDs.

3.1.2.3 Fabricate KGD ATDs with appropriate technologies as called out in supplier specifications.

3.1.2.4 Electrically test KGD ATDs for opens and shorts.

3.1.2.5 Perform Quality Conformance Inspections of KGD ATDs (optional).

3.1.3 Assembly and Disassembly Supplier

3.1.3.1 Perform assembly of die and KGD ATDs.

3.1.3.2 Following test and burn-in, disassemble the KGD ATDs and the dice, packaging the dice for delivery, and returning the KGD ATDs for re-use.

3.1.4 Burn-in Supplier

3.1.4.1 Perform burn-in of assembled KGD ATDs.

3.1.4.2 Failing components are to be separated from passing components, and each is to be identified with a serial number that matches an accompanying exception report which details the failure mode and time of failure.

3.1.5 Functional Test Supplier

3.1.5.1 Perform at-speed functional test and parametric test of KGD ATDs.

3.1.5.2 Failing components are to be separated from passing components, and each is to be identified with a serial number that matches an accompanying exception report which details the failure mode and time of failure.

3.1.6 Quality Conformance Inspection Supplier

Perform Quality Conformance inspection on the bare dice, after all above processing is complete.

3.2 Supplier Deliverable Items

3.2.1 Supplier will provide bonding level design information of KGD ATD for buyer in GDS II or GERBER format.

3.2.2 Supplier will provide documentation of the thermal analysis assumptions and resulting junction temperature predictions for each component.

3.2.3 Supplier will provide documentation on all supplier performed electrical tests.

3.2.4 Supplier will provide documentation on all Quality Conformance Inspections.

3.2.5 Supplier will provide the processed known good die, and the bad die, packaged separately and clearly marked.

3.3 Buyer Tasks

3.3.1 Supply integrated circuit components and bond pad layout data in accordance with the purchase order specification, if supplier is not the source of these components.

3.3.2 Supply test vectors for the dice to be tested, in a format to be specified in the purchase order specification, if the supplier is not the source of these components.

3.3.3 Supply integrated circuit data sheets for the dice to be tested, if the supplier is not the source of these components.

3.3.4 Perform on site handling damage control inspections. The supplier handling methods, ESD protection, and cleanliness will be inspected and reported on.

4.0 Detailed Supplier Tasks

4.1 Integrated Circuit Die Supplier

4.1.1 Provide sort tested integrated circuit die that have been sawn and placed into waffle pack die carriers for delivery to KGD supplier. Wafer sort testing is to be performed by the integrated circuit supplier to screen out grossly defective die. This testing is to include both parametric and gross functional testing, per the vendor normal sort test specifications. The complete specification for functional and parametric testing of the packaged parts, along with the burn-in specifications are required items. Please include these specifications and any guardbands applied during sort testing with your quotation.

4.1.2 Perform actions specified by reinsertion plan, to be agreed upon by supplier and MCC prior to assignment of purchase orders for die. Following the burn-in and testing of these dice in carriers for assurance as known good die, they are to be disassembled and returned to the IC manufacturer for reinsertion into the high reliability packaging in which these parts are normally offered. If possible, they are then to be included into products and the lifetime reliability of these parts monitored throughout the manufacturer normal warranty period for any excessive failures. Each integrated circuit supplier should be prepared to complete a detailed plan for accomplishing this task.

4.2 Assurance Technology Device Supplier

4.2.1 Design/layout KGD ATDs as appropriate to TAB, wire bond, and/or all other types of bare die assembly. The supplier is responsible for the complete design and implementation of specific Known Good Die Assurance Technology devices, whether those devices are in carrier or other form. The KGD ATD technology employed is proprietary to each supplier, and each supplier is responsible for adapting their specific KGD ATDs to the four categories of integrated circuit devices.

4.2.2 Perform Thermal Analysis. The supplier is responsible for performing a thermal analysis to verify that an adequate thermal path in the KGD ATD has been provided for each chip. Documentation of this analysis will be specified as part of the deliverables in the Request For Quotation.

4.2.3 Fabricate KGD ATDs with appropriate technologies as specified in the response to quotation, purchase order, and supplier specifications. The supplier will fabricate a quantity of KGD ATDs sufficient to complete the test and burn-in of the specified number of dice in accordance with the purchase order specification. The technology used for fabrication is at the discretion of the supplier.

4.2.4 Electrically test KGD ATDs for opens and shorts. Each of the KGD ATDs is to be electrically tested for opens and shorts to the vendor specification for contact resistance prior to its use for assembly with a bare die. Any defective KGD ATDs are not to be used for performance of KGD processing, and is to be considered as yield loss. Complete documentation of the testing, with exception reports identifying all failures, is to be delivered to the buyer.

4.2.5 Perform Quality Conformance Inspections of KGD ATDs (optional). QCI is to be performed on the KGD ATDs prior to their use in KGD processing, if this is a reasonable and prudent step for the KGD ATD methodology involved. If performed, complete documentation of the QCI is to be delivered, along with written documentation of the inspection criteria and the sampling plan used.

4.3 Assembly/Disassembly Supplier

4.3.1 Perform assembly of die and KGD ATDs. The supplier is responsible for assembly of bare die into the KGD ATD and all related processing (i.e., wire bonding).

4.3.2 Disassemble the KGD ATDs and the dice, packaging the dice for delivery. The supplier shall remove the dice from the KGD ATDs, performing any required processing steps, and place these die in an appropriate shipping container (i.e., wafflepack) for shipment to the buyer. Shipment to the buyer shall be the supplier's responsibility.

4.3.3 Perform Quality Conformance inspection on the bare dice. A final Quality Conformance Inspection on all of the bare dice is required prior to shipment to the buyer. Any damage to the dice, or any material or residue that is found on the die is to be identified; failures are to be separated from the known good die (in separate containers) and clearly marked as final QCI failures. Complete documentation of this QCI, with the inspection criteria, is to be delivered to the buyer with the dice.

4.4 Burn-in Supplier

4.4.1 Perform burn-in of assembled KGD ATDs. Each of the KGD ATD/die assemblies is to be subjected to a dynamic monitored burn-in that is commensurate with the requirements for verification of reliability of the die being processed. The burn-in requirements (time, temperature, signal connections, and monitoring) shall match the normal burn-in requirements for each part when that part is normally packaged and burned-in.

4.4.2 Separately package failing parts, clearly marked as failures. An exceptions report which details the type of failure and when it occurred should be included with the packaged failed parts.

4.5 Functional Test Supplier

4.5.1 Perform at-speed functional test of KGD ATDs. The supplier is responsible for performing an at-speed full functional test of each die while it is mounted in the KGD ATD. This test should be equivalent to the test that is normally performed on a packaged die. All test results, with a yield and exception report, will be delivered to buyer.

4.5.2 Separately package failing parts, clearly marked as failures. An exceptions report that details the type of failure and when it occurred should be included with the packaged failed parts.

5.0 Buyer Tasks

5.1 Supply Component Die and Layout Data

The buyer will be responsible for supplying sort test screened component die in the quantities as stated in the purchase order specification. The buyer will also be responsible for supplying all layout data required to connect to the devices.

5.2 Supply Test Vectors

In the event that the KGD supplier is not also the source of the integrated circuits to be processed, the buyer is responsible for obtaining the test vectors used for functional test of the integrated circuits. The required format of such vectors is a function of the type of test system used by the test supplier, and these details are to be settled by the buyer and supplier and included in the purchase order specification.

5.3 Supply Device Data Sheet Information

In the event that the KGD supplier is not also the source of the integrated circuits to be processed, the buyer will provide the device data sheet information which describes the power requirements, parametric pin information, and a detailed functional description.

Section III

Final Draft

Technology Assessment Guideline
for
Methods, Materials and Equipment
Necessary to Prepare and Ship Semiconductor Devices
as Fully Warranted Bare Die Product

DRAFTED BY

Microelectronics and Computer Technology Corp.

High Value Electronics Division

and

SEMATECH

Supplier/User Known Good Die Task Teams

15 December 1993

Rev 3.0

TABLE OF CONTENTS

Introduction and General Information

1.0 SCOPE:

This document describes the guidelines for processes, materials and equipment for manufacturing and delivering bare, or minimally packaged[1] semiconductor product with quality and reliability comparable to their functionally equivalent packaged components. For the purposes of this document, these methodologies will be called Known Good Die (KGD) Assurance Technologies. This document is limited to guidelines for these assurance technologies, and does not cover requirements for, nor performance of, the actual Known Good Die. KGD requirements and performance are addressed in the *Standard for Procurement and Use of Known Good Die.*[2]

This document provides guidance to organizations developing KGD assurance technologies, and evaluating and implementing those technologies. The body of the document contains the guidelines which were developed by the combined MCC/Sematech task team. Appendix A is included so that information needed to assess particular technologies for test and burn-in die carriers will be supplied by the technology supplier. Appendix B contains information on issues to be considered by the KGD technology supplier and user if mechanical die alignment is required.

The requirements for technologies can be divided into short term and long term groupings. Short term requirements are defined as those which can be implemented quickly and will have minimal impact on existing manufacturing methods, equipment and process flows. Minimum product cost and maximum manufacturing efficiency are of concern for all long term requirements. Short term requirements will be identified in this document with a **(-1)** paragraph suffix, long term with a **(-2)** suffix. The long term requirements are included in Appendix C.

Different applications and industry segments (Military, Industrial, Commercial, Consumer) can have different KGD assurance requirements. The requirements for assurance technologies developed here are intended to include the needs of all market segments. The ideal would be for each segment to use the same fundamental assurance technologies and truncating or reordering steps to suit the needs of their products. This approach will lead to the most manufacturable process for KGD suppliers, and ultimately the lowest cost for all users.

The requirements in each section are defined in terms of the following classifications:

Rules. These subsections contain a listing of baseline capability for assessing aspects of KGD technology being proposed for the short term.

Recommendations. These subsections indicate optional or desirable features for methods which should be considered when conforming to this guideline.

Test Methods These subsections contain a description of test methodology used for evaluating KGD technology against TAG rules. A complete description of each test method is included in Appendix D.

Appendix E contains the references which are noted in the document.

2.0 APPLICABLE DOCUMENTS

(A) *Standard for Procurement and Use of KGD*, Working Document, JEDEC Modified Version 2.0, 18 May 1993, As submitted for ballot

(B) MIL-STD-883 Microelectronics, Test Methods and Procedures

(C) Annual Book of American Society for Testing and Materials Standards

3.0 PHYSICAL CONFIGURATION

See Appendix C for (-2) future requirements (1996 timeframe).

3.1 Device types

3.1.1(-1) Rules

Shall accommodate all types of active devices including Analog, Digital and mixed; Bipolar, CMOS and mixed; Memories, Microprocessors, DSPs, Logic, programmable Gate Arrays, MMICs, OptoElectronics and ASICS; Silicon based, Silicon on Insulator and Gallium Arsenide.

3.1.2(-1) Recommendations

None

3.1.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

3.2 Incremental Cost targets

3.2.1(-1) Rules

Incremental KGD Assurance Technology Costs should not be significantly greater than those associated with packaging of otherwise conventionally prepared die.

3.2.2(-1) Recommendations

None

3.2.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

3.3 Wafer/Die sizes

3.3.1(-1) Rules

Shall accommodate devices from 2500 square mils [1.6 square mm] to 500,000 square mils [322 square mm], with a maximum aspect ratio of 3 to 1. Size tolerance on singulated die will be $\leq \pm 0.5$ mils [12 µm].

3.3.2(-1) Recommendations

Shall accommodate devices from 400 square mils [.25 square mm] to 640,000 square mils [413 square mm], with a maximum aspect ratio of 3 to 1. Size tolerance on singulated die will be $\leq \pm 0.5$ mils [12 µm].

3.3.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

3.4 Die thickness

3.4.1(-1) Rules

Shall accommodate devices with a thickness of 10 mils [250 µm] to 30 mils [750 µm] . Thickness tolerance is $\pm$ 1.0 mils [25 µm].

3.4.2(-1) Recommendations

Shall accommodate devices with a minimum thickness of 4 mils [100µm].

3.4.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

3.5 Die Interconnect Quality

3.5.1 PLANARITY[3] OF DIE/INTERCONNECT

3.5.1.1(-1) Rules

Adaptation

Shall maintain reliable contact of die with nonplanarity across the die of 2.0µm. (see Appendix A for bump information).

3.5.1.2(-1) Recommendations

None

3.5.1.3(-1) Test Methods

KGD carrier interconnect will be tested for its contact resistance to a dummy die with multiple Al layers to provide a range of pad heights per MIL Standard 883D Method 3017.3.3. Contact resistance must be less than or equal to 0.5 Ω. KGD carrier contact resistance will be measured prior to and during temperature cycling. Test Method 3.5.1.3 is described in Appendix D.

3.5.2 METALLURGY OF DIE/INTERCONNECT

3.5.2.1(-1) Rules

Adaptation

Shall maintain reliable contact for die/interconnect metallurgies including Al, Au, and solder.

Modification

Shall not change the metallurgy of, nor contaminate, the die/interconnect in a way which will degrade quality or reliability parameters of the device.

3.5.2.2(-1) Recommendations

None

3.5.2.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

3.5.3 DAMAGE TO DIE/INTERCONNECT/PASSIVATION

3.5.3.1(-1) Rules

Shall not cause damage to layers underlying the bond pad metal. Shall not preclude next level assembly. Probe shall not contact passivation (top or side)[4].

3.5.3.2(-1) Recommendations

None

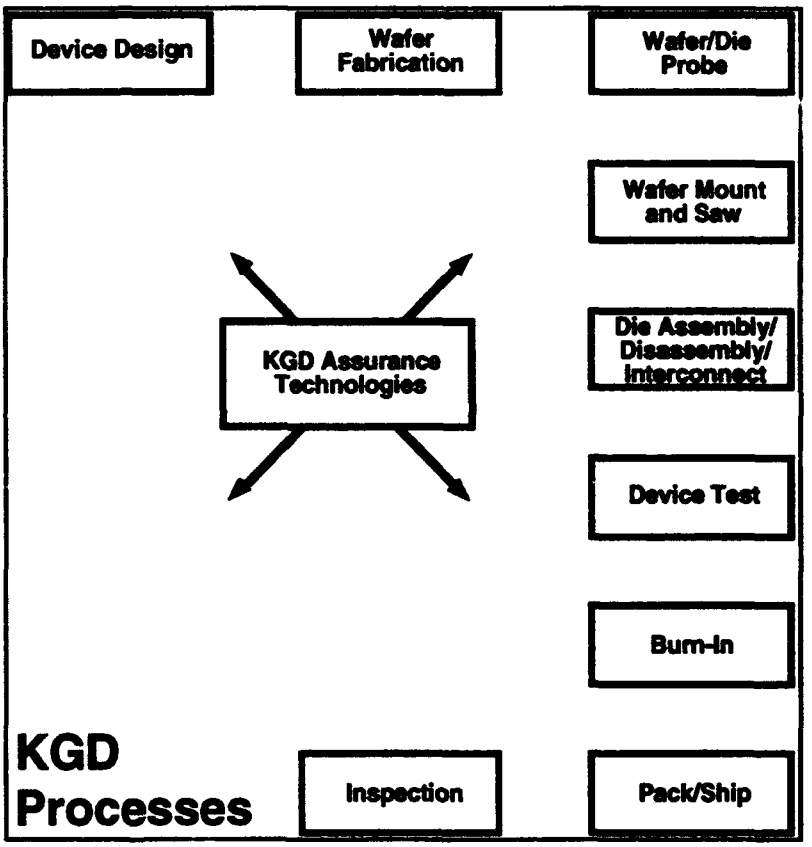
3.5.3.3(-1) Test Methods

Die will be stationed in KGD carrier or socket and removed per manufacturer specifications. Die will be inspected for bond pad damage due to probe contact per MIL Standard 883D Method 2010.10. Die will be inspected for damage to layers underlying the bond pad metal due to probe contact per MIL Standard 883D Method 2010.10. Die will be wirebonded and pull tested for bond pad damage or contamination due to probe contact per MIL Standard 883D Method 2011.7. Die will be tested for loss of adhesion to die attach material from damage or contamination of back side of die due to Carrier or socket contact per MIL Standard 883D Method 2019.5. Die will be inspected for intermetalic formation on bond pad due to probe contact with Auger Electron Spectroscopy per ASTM method E 827-88 prior to and after burn in at 150 °C for 168 hours. Test Methods 3.5.3.3 are described in Appendix D.

4.0 Die Process Steps

The process by which individual die undergo KGD Assurance Technology assessment will depend upon the nature and maturity of the circuit technology, circuit complexity, and demands of the die customer. It is not appropriate to designate a single die flow which applies to all assurance technologies. The following are identified as Assurance Technology Processes which may be ordered in any fashion suitable to the die vendors/customers involved.

Figure 1: KGD Assurance Technologies apply to the generic processes used for IC manufacture.



- Device Design
- Wafer Fabrication
- Wafer/Die Probe (Basic Functional Test)
- Wafer Mount and Saw
- Die Assembly/ Disassembly/ Interconnection
- Device Test (Full Function Test)
- Burn-In
- Pack/Ship
- Inspection

5.0 DETAILED PROCESS DESCRIPTION

5.1 Device Design

5.1.1 Rules(-1)

No change or impact required

5.1.2(-1) Recommendations

None

5.1.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

5.2 Wafer Fabrication

5.2.1 Rules(-1)

No change or impact required

5.2.2(-1) Recommendations

None

5.2.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

5.3 Wafer/Die Probe

5.3.1(-1) Rules

Nothing in the process should prevent the use of currently practiced wafer probe techniques.

5.3.2(-1) Recommendations

For some KGD products, wafer probe techniques will be able to support all electrical testing currently being performed on the packaged version of the product. For these products, wafer probe must perform the tests to the same levels and under the same conditions as the packaged product, or eliminate wafer probe by inclusion of test in subsequent processes.

5.3.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

5.4 Wafer Mount and Saw

5.4.1(-1) Rules

Nothing in this process should prevent the use of currently practiced wafer mount and saw techniques. See Appendix B for issues to consider if die edge is used for alignment.

5.4.2(-1) Recommendations

None

5.4.3(-1) Test Methods

Will be evaluated based on engineering judgment of design.

5.5 Die Assembly/Disassembly Interconnect

See Appendix A

5.6 Device Test & Burn-in

The device test and burn-in guidelines are divided into 2 sets of numbers, according to number of device I/O accommodated. Low I/O technologies are defined as those able to make electrical connection to fewer than 100 pads, and high I/O technologies are those able to make electrical connection to more than 100 pads.

General rules which apply to Assurance Technologies for electrical test are:

Shall be BIST[5] capable

Shall accommodate basic functional test

Shall accommodate simulation/connection of external devices

Contact resistance compatible with bandwidth

Shall accommodate die with backside electrical connection requirement

Shall have pin 1 identifier

Shall accommodate die pads in passivation wells ≤ 1.5μm in depth

5.6.1,3(-1) Rules & 5.6.2,4(-1) Recommendations for Low I/O Technologies

Test Attributes	5.6.1(-1) Test Rules	5.6.2(-1) Test Recommendations	5.6.3(-1) Burn-in Rules	5.6.4(-1) Burn-in Recommendations
Carrier Operating Temperature	0°C to +125° C	-55°C to +150°C	Die = 175°C Ambient = 150°C	Die = 175°C Ambient = 150°C
Time @ Max Temperature			12 Hours	168 Hours
Contact Resistance[6]	<.5Ω	<.25Ω	<.5Ω	<.25Ω
Min Clock Freq.	100 MHz	2GHz	20 MHz	50 MHz
Array/Periph pads?	Peripheral	Both	Peripheral	Both
Pad Metalization Accommodated	Al, Au, Solder	Al, Au, Solder	Al, Au, Solder	Al, Au, Solder
Pad pitch Accommodated	≥200μm	≥150μm	≥200μm	≥150μm
Passivation Opening	≥100μm	≥75μm	≥100μm	≥75μm

Char. Impedance Tolerance	±10%	±5%	±10%	±5%
Power dissipation	6W/cm^2	20W/cm^2	6W/cm^2	20W/cm^2
# of touch downs/die[7]	≥2	≥2	≥2	≥2

Table 1. Test and Burn-in attributes required for low I/O KGD Assurance Technologies

5.6.1.1(-1) Test Method for Temperature Cycling

KGD carrier will be temperature cycled per MIL Standard 883D Method 1010.7 except with a temperature range of 0 °C to 85 °C, 0°C to +125° C, and -55 °C to 150 °C. Test method 5.6.1.1 described in Appendix D.

5.6.1.2(-1) Test Method for Contact Resistance

KGD carrier interconnect will be tested for its contact resistance per MIL Standard 883D Method 3017.3.3. Contact resistance must be less than or equal to 0.5 Ω. KGD carrier contact resistance will be measured prior to and during temperature cycling and burn in. Test method 5.6.1.2 described in Appendix D.

5.6.1.3,4,5(-1) Test Method for Maximum Clock Frequency, Characteristic Impedance, and Bandwidth

KGD carrier interconnect will be tested for TDR rise time per MIL Standard 883D Method 3017. The characteristic impedance will be measured from the impedance waveform display on the TDR. The characteristic impedance must be within 10% of the designed impedance. Using the same test setup while replacing the TDR with a network analyzer, the KGD carrier interconnect will be tested for its bandwidth per MIL Standard 883D Method 4004.1.3.4. Bandwidth must be greater than or equal to 500 MHz. MIL Standard 883D Method 3018 will be used for measuring the level of cross coupling of signals and noise between pins, although no rules have been defined. Test method 5.6.1.3,4,5 described in Appendix D.

5.6.1.6(-1) Test Methods for Die Damage or Contamination After Two Touchdowns

Die will be stationed in KGD carrier or socket and removed twice per manufacturer's specifications. Die will be inspected for bond pad damage due to probe contact per MIL Standard 883D Method 2010.10. Die will be inspected for damage to layers underlying the bond pad metal due to probe contact per MIL Standard 883D Method 2010.10. Die will be

wirebonded and pull tested for bond pad damage or contamination due to probe contact per MIL Standard 883D Method 2011.7. Die will be tested for loss of adhesion to die attach material from damage or contamination of back side of die due to Carrier or socket contact per MIL Standard 883D Method 2019.5. Test 5.6.1.6 will be repeated after burn in. Test methods 5.6.1.6 described in Appendix D.

5.6.3.1(-1) Test Method for Burn-in Test

KGD carrier will undergo burn-in per MIL Standard 883D Method 1015.8 . Test method 5.6.1.2 for contact resistance will be applied during burn in. Visual inspection per MIL Standard 883D Method 2009.8 will be performed after burn in. Test method 5.6.3.1 described in Appendix D.

5.6.3.1(-1) Test Method for Thermal Resistance

KGD carrier will be tested for its thermal resistance per MCC specified thermal resistance test. The KGD carrier thermal resistance will be tested using two test methods. One method would be to measure the junction-to-ambient thermal resistance in a forced or free convection environment. This method could be similar to the SEMI specification G38, with the exception of using a thin film resistor sputtered on silicon rather than a thermal test chip. Another method would be to measure junction-to-ambient and junction-to-case thermal resistances in a system which uses a flat cooling surface to a cold plate for its primary heat transfer mechanism.

5.6.3.2(-1) Test Method for Contact Resistance During Burn In

KGD carrier interconnect will be tested for its contact resistance per MIL Standard 883D Method 3017.3.3 during test 5.6.3.1. Contact resistance must be less than or equal to 0.5 Ω. Test method 5.6.3.2 described in Appendix D.

Note: Test Methods for high I/O technologies identical to low I/O technologies.

5.6.5,7(-1) Rules & 5.6.6.8(-1) Recommendations for High I/O Technologies

Test Attributes	5.6.5(-1) Test Rules	5.6.6(-1) Test Recommendations	5.6.7(-1) Burn-in Rules	5.6.8(-1) Burn-in Recommendations
Carrier Operating Temperature	0°C to +125° C	-55°C to +150°C	Die = 175°C Ambient = 150°C	Die = 175°C Ambient = 150°C
Time @ Max Temperature			12 Hours	168 Hours
Contact Resistance[8]	≤.5Ω	≤.25Ω	≤.5Ω	≤.25Ω
Min Clock Freq.	100 MHz	500MHz	20 MHz	50 MHz
Array/Periph pads?	Both	Both	Both	Both
Pad Metalization Accommodated	Al, Au, Solder	Al, Au, Solder	Al, Au, Solder	Al, Au, Solder
Pad pitch Accommodated	≥125µm - Periph ≥200µm - Array	≥80µm	≥125µm - Periph ≥200µm - Array	≥80µm
Passivation Opening	≥75µm	≥50µm	≥ 5µm	≥50µm
Char. Impedance Tolerance	±10%	±5%	±10%	±5%
Power dissipation	10W/cm^2	50W/cm^2	10W/cm^2	50W/cm^2
# of touch downs/die[9]	≥2	≥2	≥2	≥2

Table 2. Test and Burn-in attributes required for high I/O KGD Assurance Technologies

Burn-in atmosphere or immersing liquid shall be such that device meets section 3.5 of this document (Die Interconnect Quality) without requiring new equipment.

5.7 Shock/Vibration

5.7.1(-1) Rules

To be determined.

5.7.2(-1) Recommendations

5.7.3(-1) Test Methods for Shock/Vibration

KGD carrier will be tested for damage after exposure to mechanical shock per MIL Standard 883D Method 2002.3. KGD carrier will be tested for damage after exposure to vibration per MIL Standard 883D Method 2007.3. .Test method 5.7.3 described in Appendix D.

5.8 Pack/Ship

5.8.1(-1) Rules

Shall accommodate shipment and transmission of information consistent with the requirements of the JEDEC KGD Specification[10]. Packing shall provide protection and compatibility with storage conditions listed in that specification.

5.8.2(-1) Recommendations

Shall accommodate individual die traceability (site on wafer) from shipping location back through fab.

5.9 Inspection

5.9.1 Rules(-1)

KGD Assurance Technology shall permit optical inspection including user incoming quality verification procedures on the entire device.

5.9.2(-1) Recommendations

None

Appendix A: KGD Assurance Technology Supplier Requested Information

It is intended that the information in Appendix A be provided by the supplier of a particular approach for test and burn-in die carriers. This information will be used for assessment of the technologies.

A.1 Die carrier information

Cost of Test/Burn-in Carrier[11]	
# of reuses[12]	
Capacitance - Trace to trace	
Resistance - Trace to trace	
Resistance of trace (Carrier to die pad)	
Bandwidth (—3db)	
CTE[13]	
Surface metal of Probe tip[14]	

Table A.1.1 Carrier attributes to be disclosed by KGD Assurance Technologies supplier.

A.2 Die interconnect/bump information

Bump Hardness Accommodated	
Bump Material Accommodated	
Bump Planarity Accommodated	

Table A.2.1 Attributes of bumped-die conformance requirements to be disclosed by KGD Assurance Technologies supplier.

A.3 Die Assembly-Disassembly and Interconnect

The following attributes of the die assembly, disassembly and interconnect aspects of a KGD assurance technology must be specified and accepted by die maker, assurance technology user and die customer. For each element, separate attributes are to be specified for bare, bumped and TABed die.

The methods by which die are to be physically and electrically connected to Assurance Technology equipment may vary according to the ultimate application. This guideline seeks to anticipate but not enumerate, all of the assembly-disassembly and interconnection attributes of possible Assurance Technologies. A checklist of applicable attributes is provided in this section through which each proposed Assurance Technology might be described. All applicable attributes must be specified by the Assurance Technology

manufacturer. Proposing manufacturers are encouraged to add descriptive parameters not listed herein so that their technology be fully understood. The completed list will serve as a basis for assessment of technology complexity, risk and application/development cost. For each element, applicable values must be provided for bare, bumped and TABed die related processes.

Die preparation includes those process steps required to provide compatibility between the die and the KGD carrier. These steps would not be required for a die which would be burned-in and tested at the finished package level.

A.3.1 Die Preparation

		Bare Die	Bumped Die	TABed Die
Purpose (i.e., pad cleaning, additional metal, etc)				
Form Factor				
Interconnect Applicability				
Availability for Licensing/Transfer to Second Source				
Pad Preparation				
Consumables				
Additional Processing				
	Process Flow Chart			
	Number of Steps (U/H, Cost)			
	Equipment List			
	Cost Sensitivity vs Complexity			
Process Constraints				
	Pad Shape, Pad Size, Quantity/Density			
	Wafer Size (Diameter, Thickness)			
	Die Size			
	Passivation Opening & Profile			
	Pad Footprint (i.e. array, peripheral, other)			
Special Features/Tooling Requirements (e.g. Adaptability to Wafer/Die Size)				

Incremental Capacity per Tool Set (i.e. Unit Capacity of Process Limiting Tool)				
Process Control				
Defect Definition Criteria				
	Limits			
	Yield Impacts			
	Ability to Automate			
Environmental Cost (Chemical Disposal, etc)				

Table A.3.1 Attributes of die preparation requirements to be disclosed by KGD Assurance Technologies supplier.

A.3.2 Die Assembly

		Bare Die	Bumped Die	TABed Die
Final Interconnect Applicability				
Process Qualification Status/Readiness				
	Method of Validation (i.e. Shipped Quality Level of Product, Manufacturing Verification or Feasibility, Level of Development and etc.)			
	Availability for Licensing/Transfer to Second Source			
Type of Bond (Mechanical, Metallurgical, Other)				
Method of Bonding (Thermal Reflow, Thermal Compression, Mechanical Clamp, Other)				
Consumables (One Time)				
	Solder			
	Lead Frame/Interface			
	Flux			
	Wire (Gold, Aluminum, etc)			
	Substrate/Carrier			

	Others (Process Dependent)			
Adaptability to Discrete Components (i.e. Decoupling Capacitors, Tuning Circuits, etc.)				
Footprint Constraints (i.e. Array, Peripheral, Depopulated Array, etc.)				
Reusable Fixtures (Clamps, Trays, Other)				
Carriers/Interfaces				
	Carrier Type (i.e., Ceramic, Organic, etc)			
	Carrier to BIB Interconnect (i.e. Pin Grid Array, Solderball etc)			
	Number of Reuses			
	Preparation for Reuse (if applicable)			
	Adaptability to Discrete Components (i.e., Decoupling Capacitors, Tuning Circuits, etc)			
	Footprint Constrains (i.e. Array, Peripheral, Depopulated Array, etc)			
Performance/ Physical Limitations				
	Die Size			
	Heat Sink Attachment			
	Maximum Temperature Range			
	Electrical Characteristics (i.e., Speed, Frequency, etc)			
	Pad/Pitch Limitations (Pad Size, Pad to Pad Distance, Pad Shape, Planarity Sensitivity)			
Process Control Inspectability				
	Orientation/Alignment			
	Type of Bond			
	Integrity of Assembly			
Process Description				

	Process Flow Chart			
	Automation			
	Tools (i.e., Existing, Unique, etc)			
	Force on Die			
	Protection from ESD, Contamination, Vibration, Shock			
	Carrier Shipability			
	Incremental Capacity of Tool Set			
	Reworkability			
	Method of Alignment, Die pads to Interconnect			
Traceability				
	Carrier Reuse (i.e. EOL)			
	Lot/Die Production Unit			
Cost				
	NRE			
	U/H and Consumables			
Environmental Cost (Chemical Disposal, etc)				

Table A.3.2 Attributes of die assembly requirements to be disclosed by KGD Assurance Technologies supplier.

A.3.3 Die Disassembly

		Bare Die	Bumped Die	TABed Die
Method of Detach				
	Shear			
	Reflow			
	Mechanical/Vacuum Removal			
	Other/None			
Process Qualification Status/Readiness (Availability for Licensing/Transfer to Second Source.)				
Consumables (One Time)				
	Adhesive Tapes			
	Other			
Fixtures/Carriers				
	Storage Capability			
	Special Protection (i.e., Environmental, Mechanical, etc)			

Process				
	Process Flow Chart			
	Automation			
	Tools (i.e. Unique, Existing, etc)			
	Force on Die			
	Rework of Die Pads			
	Robustness for Next Level of Assembly (i.e. SPQL, etc)			
Process Control				
	Inspection Limits			
	Die Protection (ESD Damage etc)			
	Defect Definition/Criteria			
	Verify Integrity of Next Level of Assembly			
Costs				
	NRE			
	U/H Plus Consumables			
Environmental Cost (Chemical Disposal, etc)				

Table A.3.3 Attributes of die disassembly requirements to be disclosed by KGD Assurance Technologies supplier.

Appendix B: Mechanical Alignment of Die Issues

Issues to be considered if mechanical die alignment is required; i.e., using the sides of a die for alignment to a probe set.

a. Saw Cut Placement Accuracy (i.e., Distance to Designated Die Feature)

b. Saw Alignment Accuracy: Placement of saw cut centerline +/- 0.15 mils [4 μm] of intended location at any point across wafers of up to 8 in. [200 mm] diameter.

c. Saw Cut Dimensions: Maximum Saw Cut widths maintained between 1.9 and 1.4 mils [48 and 35 μm] throughout blade life. (Dimension of New Blade 1.8 mils ± 0.1 mil [45 ± 2.5μm]).

d. Sawn Edge Camber: Total deviation (or bevel) of sawn edge from a straight vertical cut of not more that 2 mils [50 μm] through the thickness of a die, or 5% of wafer thickness, whichever is smaller.

e. Edge Cracks

f. Perpendicularity (Trapezoidal skew)

Total Saw Drift Control: It is recommended that wire saw system manufacturers work to control the total wafer to wafer drift of saw alignment to an average no more than +/- 0.15 mils [4 μm] from all causes. This goal might be attained through active process control based upon in-situ sensors. Midwafer optical recognition system based realignments may contribute to this goal if throughput is not dramatically effected. Alignment based on die row identification without special alignment marks is desirable.

Improved Saw Placement Accuracy: It is recommended that wire saw system manufactures move to field products with improved placement accuracy equipment. Placement of cut centerline to an accuracy of +/- 1 μm, even without improvements in blade thickness, is considered beneficial to saw operations for both packaged and die product.

Appendix C: Future Requirements (1996 Timeframe)

C.3.0 PHYSICAL CONFIGURATION (FUTURE)

C.3.1 Device types

C.3.1.1(-2) Rules

As 3.1.1(-1)

C.3.1.2(-2) Recommendations

None

C.3.2 Incremental Cost targets (Future)

C.3.2.1(-2) Rules

As 3.2.1(-1)

C.3.2.2(-2) Recommendations

Less than 1.0X the cost of the equivalent packaged part in volume

C.3.3 Wafer/Die sizes (Future)

C.3.3.1(-2) Rules

Shall accommodate devices from 400 square mils [0.25 square mm] to 3,100,000 square mils [2000 square mm] , with a maximum aspect ratio of 3 to 1. Size tolerance on singulated die will be $\leq \pm$ 1.0 mils [25μm].

C.3.3.2(-2) Recommendations

None

C.3.4 Die thickness (Future)

C.3.4.1(-2) Rules

Same as 3.4.1(–1)

C.3.4.2(-2) Recommendations

None

C.3.5 Die Interconnect Quality (Future)

C.3.5.1 PLANARITY OF DIE/INTERCONNECT

C.3.5.1.1(-2) Rules

Same as 3.5.1.1(-1)

C.3.5.1.2(-2) Recommendations

None

C.3.5.2 METALLURGY OF DIE/INTERCONNECT

C.3.5.2.1(-2) Rules

Same as 3.5.2.1(-1)

C.3.5.2.2(-2) Recommendations

None

C.3.5.3 DAMAGE TO DIE/INTERCONNECT/PASSIVATION

C.3.5.3.1(-2) Rules

Same as 3.5.3.1(-1)

C.3.5.3.2(-2) Recommendations

None

C.5.0 DETAILED PROCESS DESCRIPTION (FUTURE)

C.5.1 Device Design (Future)

C.5.1.1(-2) Rules

No changes that adversely impact the performance of the device.

C.5.1.2(-2) Recommendations

BIST, Boundary Scan, DFBI

C.5.2 Wafer Fabrication (Future)

C.5.2.1(-2) Rules

No change that adversely impacts reliability of the device

C.5.2.2(-2) Recommendations

Change allowed.

C.5.3 Wafer/Die Probe (Future)

C.5.3.1(-2) Rules

None

C.5.3.2(-2) Recommendations

Changes in wafer probe equipment and techniques permitted provided the resultant product will meet any and all wafer probe specifications currently in force.

Recommend whole wafer testing, or elimination of wafer probe by inclusion of test in subsequent processes.

C.5.4 Wafer Mount and Saw (Future)

C.5.4.1(-2) Rules

None

C.5.4.2(-2) Recommendations

None

C.5.5 Device Test & Burn-in (Future)

The device test and burn-in guidelines are divided into 2 sets of numbers, according to number of device I/O accommodated. Low I/O technologies are defined as being capable of making electrical connection to fewer than 100 pads, and high I/O technologies are those capable of making electrical connection to more than 100 pads.

General rules which apply to Assurance Technologies for electrical test are:

Shall be BIST[15] capable

Shall accommodate basic functional test

Shall accommodate simulation/connection of external devices

Contact resistance compatible with bandwidth

Shall accommodate die with backside electrical connection requirement

Shall have pin 1 identifier

Shall accommodate die pads in passivation wells ≤ 1.5μm in depth

C.5.5.1(-2) Rules & C.5.5.2(-2) Recommendations for Low I/O Technologies

Test Attributes	C.5.5.1(-2) Test Rules	C.5.5.2(-2) Test Recommendations	C.5.5.3(-2) Burn-in Rules	C.5.5.4(-2) Burn-in Recommendations
Carrier Operating Temperature	–40°C to +125° C	-55°C to +150°C	Die = 175°C Ambient = 150°C	Die = 175°C Ambient = 150°C
Time @ Temperature			24	168
Contact Resistance	≤.5Ω	≤.25Ω	≤.5Ω	≤.25Ω
Min Clock Freq.	200 MHz	2GHz	20 MHz	50 MHz
Array/Periph pads?	Both	Both	Both	Both
Pad Metalization accomodated	Al, Au, Solder	Al, Au, Solder	Al, Au, Solder	Al, Au. Solder
Pad pitch accomodated	≥100μm	≥100μm	≥100μm	≥100μm
Passivation Opening	≥50μm	≥50μm	≥50μm	≥50μm
Char. Impedance tolerance	±10%	±5%	±10%	±5%
Power dissipation	6W/cm^2	20W/cm^2	6W/cm^2	20W/cm^2

# of touch downs/die	≥2	≥2	≥2	≥2

Table C.1. Test and Burn-in attributes required for low I/O KGD Assurance Technologies (Future)

C.5.5.1(-2) Rules & C.5.5.2(-2) Recommendations for HIgh I/O Technologies

Test Attributes	C.5.5.5(-2) Test Rules	C.5.5.6(-2) Test Recommendations	C.5.5.7(-2) Burn-in Rules	C.5.5.8(-2) Burn-in Recommendations
Carrier Operating Temperature	–40°C to +125° C	-55°C to +150°C	Die - 175°C Ambient - 150°C	Die - 175°C Ambient - 150°C
Time @ Temperature			24	168
Contact Resistance	≤.5Ω	.≤25Ω		
Min Clock Freq.	100 MHz	500MHz	20 MHz	50 MHz
Array/Periph pads?	Both	Both	Both	Both
Pad Metalization accomodated	Al, Au, Solder	Al, Au, Solder	Al, Au, Solder	Al, Au, Solder
Pad pitch accomodated	70µm Periph, 150µm Array	70µm Periph, 150µm Array	70µm Periph, 150µm Array	70µm Periph, 150µm Array
Min Pad Size	50µm	50µm	50µm	50µm
Char. Impedance tolerance	±10%	±5%	±10%	±5%
Power dissipation	10W/cm^2	50W/cm^2	10W/cm^2	50W/cm^2
# of touch downs/die	≥2	≥2	≥2	≥2

Table C.2. Test and Burn-in attributes required for high I/O KGD Assurance Technologies (Future)

C.5.6 Shock/Vibration

C.5.6.1(-2) Rules

C.5.6.2(-2) Recommendations

C.5.7 Pack/Ship (Future)

C.5.7.1(-2) Rules

Same as 5.8.1(-1)

C.5.7.2(-2) Recommendations

Recommend coding of device history or tracking information on each die.

C.5.8 Inspection (Future)

C.5.8.1(-2) Rules

Same as 5.9.1(-1)

C.5.8.2(-2) Recommendations

None

Appendix D: Test Methods

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METHOD 1010.7

TEMPERATURE CYCLING

1. PURPOSE. This test is conducted to determine the resistance of a part to extremes of high and low temperatures, and to the effect of alternate exposures to these extremes.

1.1 Terms and definitions.

1.1.1 Load. The specimens under test and the fixtures holding those specimens during the test. Maximum load shall be determined by using the worst case load temperature with specific specimen loading. Monolithic loads used to simulate loading may not be appropriate when air circulation is reduced by load configuration. The maximum loading must meet the specified conditions.

1.1.2 Monitoring sensor. The temperature sensor that is located and calibrated so as to indicate the same temperature as at the worst case indicator specimen location. The worst case indicator specimen location is identified during the periodic characterization of the worst case load temperature.

1.1.3 Worst case load temperature. The temperature of specific specimens as indicated by thermocouples imbedded in their bodies. These indictor specimens shall be located at the center and at each corner of the load. The worst case load temperature is determined at periodic intervals.

1.1.4 Working zone. The volume in the chamber(s) in which the temperature of the load is controlled within the limits specified in table I.

1.1.5 Specimen. The device or individual piece being tested.

1.1.6 Transfer time. The elapsed time between specimen removal from one temperature extreme and introduction into the other.

1.1.7 Maximum load. The largest load for which the worst case load temperature meets the timing requirements (see 3.1).

1.1.8 Dwell time. The time from introduction of the load into the chamber until the load is transferred out of the chamber.

2. APPARATUS. The chamber(s) used shall be capable of providing and controlling the specified temperatures in the working zone(s) when the chamber is loaded with a maximum load. The thermal capacity and air circulation must enable the working zone and loads to meet the specified conditions and timing (see 3.1). Worst case load temperature shall be continually monitored during test by indicators or recorders reading the monitoring sensor(s). Direct heat conduction to specimens shall be minimized.

3. PROCEDURE. Specimens shall be placed in such a position with respect to the airstream that there is substantially no obstruction to the flow of air across and around the specimen. When special mounting is required, it shall be specified. The specimen shall then be subjected to the specified condition for the specified number of cycles performed continuously. This test shall be conducted for a minimum of 10 cycles using test condition C. One cycle consists of steps 1 and 2 or the applicable test condition and must be completed without interruption to be counted as a cycle. Completion of the total number of cycles specified for the test may be interrupted for the purpose of test chamber loading or unloading of device lots or as the result of power or equipment failure. However, if the number of interruptions for any reason exceeds 10 percent of the total number of cycles specified, the test must be restarted from the beginning.

3.1 Timing. The total transfer time from hot to cold or from cold to hot shall not exceed one minute. The load may be transferred when the worst case load temperature is within the limits specified in table I. However, the dwell time shall not be less than 10 minutes and the load shall reach the specified temperature within 15 minutes.

TABLE I. Temperature-cycling test conditions.

Step	Minutes	Test condition temperature (°C)					
		A	B	C	D	E	F
1 Cold	≥ 10	-55 +0 -10	-55 +0 -10	-65 +0 -10	-65 +0 -10	-65 +0 -10	-65 +0 -10
2 Hot	≥ 10	85 +10 -0	125 +15 -0	150 +15 -0	200 +15 -0	300 +15 -0	175 +15 -0

NOTE: Steps 1 and 2 may be interchanged. The load temperature may exceed the + or - zero (0) tolerance during the recovery time. Other tolerances shall not be exceeded.

3.2 Examination. After completion of the final cycle, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X. A visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X (except the magnification for examination shall be 1.5X minimum when this method is used for 100 percent screening). This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.3 Failure criteria. After subjection to the test, failure of one or more specified end-point measurements or examinations (see 4.d.), evidence of defects or damage to the case, leads, or seals or illegible markings shall be considered a failure. Damage to the marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Special mounting, if applicable (see 3).

b. Test condition letter, if other than test condition C (see 3).

c. Number of test cycles, if other than 10 cycles (see 3).

d. End-point measurements and examinations (see 3.1) e.g., end-point electrical measurements, seal test (method 1014), or other acceptance criteria).

METHOD 1015.9

BURN-IN TEST

1. PURPOSE. The burn-in test is performed for the purpose of screening or eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations which cause time and stress dependent failures. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions. Therefore, it is the intent of this screen to stress microcircuits at or above maximum rated operating conditions or to apply equivalent screening conditions which will reveal time and stress dependent failure modes with equal or greater sensitivity.

2. APPARATUS. Details for the required apparatus shall be as described in method 1005.

* 3. PROCEDURE. The microelectronic device shall be subjected to the specified burn-in screen test condition (see 3.1) for the time and temperature specified (see method 5004 for the appropriate device class) or, unless otherwise specified, for an equivalent time and temperature combination as determined from table I (see 3.1.1 and 3.1.2). QML manufacturers who are certified and qualified to MIL-I-38535 may modify the time or the temperature condition independently from the regression conditions contained in table I or the test condition/circuit specified in the military detail specification provided the modification is contained in the manufacturers Quality Management Plan and the "Q" certification identifier is marked on the devices. Any time-temperature combination which is contained in table I for the appropriate class may be used for the applicable test condition. The test conditions (duration and temperature) selected prior to test shall be recorded and shall govern for the entire test. Lead-, stud-, or case-mounted devices shall be mounted by the leads, stud, or case in their normal mounting configuration, and the point of connection shall be maintained at a temperature not less than the specified ambient temperature. Pre and post burn-in measurements shall be made as specified. Burn-in boards shall not employ load resistors which are common to more than one device, or to more than one output pin on the same device.

3.1 Test conditions. Basic test conditions are as shown below. Unless otherwise specified, test condition F shall not be applied to class S devices. Details of each of these conditions, except where noted, shall be as described in method 1005.

a. Test condition A: Steady-state, reverse bias.

b. Test condition B: Steady-state, forward bias.

c. Test condition C: Steady-state, power and reverse bias.

d. Test condition D: Parallel excitation.

e. Test condition E: Ring oscillator.

f. Test condition F: Temperature-accelerated test.

* 3.1.1 Test temperature. The ambient burn-in test temperature shall be 125°C minimum for conditions A through E (except for hybrids see table I). At the supplier's option, the test temperature for conditions A through E may be increased and the test time reduced in accordance with table I. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit employed should be so structured that maximum rated junction temperature for test or operation shall not exceed 200°C for class B or 175°C for class S (see 3.1.1.1). Devices with internal thermal shut-down circuitry shall be handled in accordance with 3.2.3 of method 1005. The specified test temperature is the minimum actual ambient temperature to which all devices in the working area of the chamber shall be exposed. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments, and the flow of air or other suitable gas or liquid chamber medium. Therefore, calibration shall be accomplished on the chamber in a fully loaded (boards need not be loaded with devices), unpowered configuration, and the indicator sensor located at, or adjusted to reflect the coldest point in the working area.

3.1.1.1 Test temperature for high power devices. Regardless of power level, devices shall be able to be burned in or life-tested at their maximum rated operating temperature. For devices whose maximum operating temperature is stated in terms of ambient temperature, T_A, table I applies. For devices whose maximum operating temperature is stated in terms of case temperature, T_C and where the ambient temperature would cause T_J to exceed +200°C (+175°C for class S), the ambient operating temperature may be reduced during burn-in and life test from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

3.1.1.2 Test temperature for hybrid devices. The ambient or case burn-in test temperature shall be as specified in table I, except case temperature burn-in shall be performed, as a minimum, at the maximum operating case temperature (T_C) specified for the device. Burn-in shall be 320 hours minimum for class K. The device should be burned in at the maximum specified operating temperature, voltage, and loading conditions as specified in the detail specification. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit should be so structured that the maximum rated junction temperature as specified in the detail specification, and the cure temperature of polymeric materials as specified in the baseline documentation shall not be exceeded. If no maximum junction temperature is specified, a maximum of 175°C is assumed. Accelerated burn-in (condition F) shall not be permitted. The specified test temperature shall be the minimum actual ambient or case temperature that must be maintained for all devices in the chamber. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments and the flow of air or other suitable gas or liquid chamber medium.

3.1.2 Temperature accelerated test details. In test condition F, microcircuits are subjected to bias(es) at a temperature (175°C to 250°C) which considerably exceeds the maximum rated junction temperature. At these elevated temperatures, it is generally found that microcircuits will not operate normally as specified in their applicable acquisition documents, and it is therefore necessary that special attention be given to the choice of bias circuits and conditions to assure that important circuit areas are adequately biased without subjecting other areas of the circuit to damaging overstress(es). To properly select the accelerated test conditions, it is recommended that an adequate sample of devices be exposed to the intended high temperature while measuring voltage(s) and current(s) at each device terminal to assure that the applied electrical stresses do not induce damaging overstress. Unless otherwise specified in the detail specifications, the minimum time-temperature combination shall be as delineated by table I. The minimum test time shall be 12 hours. The applied voltage at any or all terminals shall be equal to the recommended operating voltage(s) at 125°C. When excessive current flow or power dissipation would result from operation at the specified voltage(s), the applied voltage(s) at any or all terminals may be reduced to a minimum of 50 percent of the specified voltage(s) and the testing time shall be determined in accordance with the formula given in 3.5.6 of method 1005. Devices with internal thermal shut-down circuitry shall be handled in accordance with 3.5.6.1 of method 1005. Thermal runaway conditions must be avoided at all times.

3.2 Measurements. Pre burn-in measurements, when specified, or at the manufacturer's discretion when not specified, shall be conducted prior to applying burn-in test conditions. Post burn-in measurements shall be completed within 96 hours after removal of the devices from the specified burn-in test condition (i.e., either removal of temperature or bias) and shall consist of all 25°C dc parameter measurements) (subgroup A-1 of method 5005, or subgroups tested in lieu of A-1 as allowed in the most similar military detail specification) and all parameters for which delta limits have been specified as part of interim (post-burn-in) electrical measurements. Delta limit acceptance, when applicable, shall be based upon these measurements. If these measurements cannot be completed within 96 hours, for either the standard or accelerated burn-in, the devices shall be subjected to the same test condition (see 3.1) and temperature previously used for a minimum additional reburn-in time as specified in table I before post burn-in measurements are made.

3.2.1 Cooldown after standard burn-in. All devices shall be cooled to within 10°C of their power stable condition at room temperature prior to the removal of bias. The interruption of bias for up to 1 minute for the purpose of moving the devices to cooldown positions separate from the chamber within which burn-in testing was performed shall not be considered removal of bias, (bias at cooldown position shall be same as that used during burn-in). Alternatively, except for linear or MOS (CMOS, NMOS, PMOS, etc.) devices or unless otherwise specified, the bias may be removed during cooling provided the case temperature of devices under test is reduced to a maximum of 35°C within 30 minutes after the removal of the test conditions and provided the devices under test are removed from the heated chamber within 5 minutes following removal of bias. All 25°C dc measurements or alternate subgroups (see 3.2) shall be completed prior to any reheating of the device(s).

3.2.2 Cooldown after accelerated burn-in. All devices subjected to the accelerated testing of condition F shall be cooled to within 10°C of power stable at room temperature prior to the removal of bias. Interruption of bias for a period of up to 1 minute for the purpose of moving devices to cooldown positions separate from the chamber within which burn-in was conducted shall not be considered removal of bias, (bias at cooldown position shall be same as that used during burn-in). All specified 25°C dc electrical measurements shall be completed prior to any reheating of the devices.

3.2.3 Test setup monitoring. The test setup shall be monitored at the test temperature initially and at the conclusion of the test to establish that all devices are being stressed to the specified requirements. The following is the minimum acceptable monitoring procedure:

* a. Device sockets. Initially and at least each 6 months thereafter, (once every 6 months or just prior to use if not used during the 6 month period) each test board or tray shall be checked to verify continuity to connector points to assure that bias supplies and signal information will be applied to each socket. Board capacitance or resistance required to ensure stability of devices under test shall be checked during these initial and periodic verification tests to ensure they will perform their proper function (i.e., that they are not open or shorted). Except for this initial and periodic verification, each device or device socket does not have to be checked; however, random sampling techniques shall be applied prior to each time a board is used and shall be adequate to assure that there are correct and continuous electrical connections to the devices under test.

Connectors to test boards or trays. After the test boards are loaded with devices, inserted into the oven, and brought up to at least 125°C (or the specified test temperature, if less than 125°C) each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to assure electrical continuity and the correct application of specified electrical stresses for each connection or contact pair used in the applicable test configuration. This shall be performed by opening the oven for a maximum of 10 minutes.

c. At the conclusion of the test period, prior to removal of devices from temperature and test conditions, the voltage and signal condition verification of b above shall be repeated.

d. For class S devices, each test board or tray and each test socket shall be verified prior to test to assure that the specified test conditions are applied to each device. This may be accomplished by verifying the device functional response at each device output(s). An approved alternate procedure may be used.

Where failures or open contacts occur which result in removal of the required test stresses for any period of the required test duration (see 3.1), the test time shall be extended to assure actual exposure for the total minimum specified test duration. Any loss(es) or interruption(s) of bias in excess of 10 minutes total duration while the chamber is at temperature during the final 8 hours of burn-in shall require extension of the test duration for an uninterrupted 8 hours minimum, after the last bias interruption.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test duration if other than as defined for the applicable class in method 5004, or time-temperature combination shown in table I.

* b. Test condition letter.

c. Burn-in test temperature, and whether ambient, junction, or case (see 3), if other than as specified in 3.1.1.

d. Test mounting, if other than normal (see 3).

e. Pre and post burn-in measurements and drift limits, as applicable (see 3.2).

f. Authorization for use of condition F and special maximum test rating for condition F (see 3.1 and 3.1.2), when applicable.

g. Time within which post burn-in measurements must be completed if other than specified (see 3.2).

TABLE I. Burn-in time-temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.1)	Minimum reburn-in time (hours)
	Class S	Class B	Class K		
100	—	352	700	Hybrids only	24
105	—	300	600	"	24
110	—	260	520	"	24
115	—	220	440	"	24
120	—	190	380	"	24
125	240	160	320	A - E	24
130	208	138	—	"	21
135	180	120	—	"	18
140	160	105	—	"	16
145	140	92	—	"	14
150	120	80	—	"	12
175	—	48	—	F	12
200	—	28	—	"	12
225	—	16	—	"	12
250	—	12	—	"	12

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

METHOD 2002.3

MECHANICAL SHOCK

1. PURPOSE. The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shocks of this type may disturb operating characteristics or cause damage similar to that resulting from excessive vibration, particularly if the shock pulses are repetitive.

2. APPARATUS. The shock-testing apparatus shall be capable of providing shock pulses of 500 to 30,000 g (peak) as specified with a pulse duration between 0.1 and 1.0 millisecond, to the body of the device. The acceleration pulse shall be a half-sine waveform with an allowable distortion not greater than ±20 percent of the specified peak acceleration, and shall be measured by a transducer and optional electronic filter with a cut-off frequency of at least 5 times the fundamental frequency of the shock pulse. The pulse duration shall be measured between the points at 10 percent of the peak acceleration during rise time and at 10 percent of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be the greater of ±0.1 millisecond or ±30 percent of the specified duration.

3. PROCEDURE. The shock-testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and leveled before use. The device shall be rigidly mounted or restrained by its case with suitable protection for the leads. Means may be provided to prevent the shock from being repeated due to "bounce" in the apparatus. Unless otherwise specified, the device shall be subject to 5 shock pulses of the peak (g) level specified in the selected test condition and for the pulse duration specified in each of the orientations X_1, X_2, Y_2, Y_1, Z_1, and Z_2. For devices with internal elements mounted with the major plane perpendicular to the Y axis, the Y_1 orientation shall be defined as that one in which the element tends to be removed from its mount. Unless otherwise specified, test condition B shall apply.

Test condition	g level (peak)	Duration of pulse (ms)
A	500	1.0
B	1,500	0.5
C	3,000	0.3
D	5,000	0.3
E	10,000	0.2
F	20,000	0.2
G	30,000	0.12

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2. Failure criteria. After subjection to the test, failure of any specified measurements or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

* SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition, if other than test condition B (see 3).

b. Number and direction of shock pulses, if other than specified (see 3).

c. Electrical-load conditions, if applicable (see 3).

d. When required, measurement made after test (see 3 and 3.1).

e. When required, measurement during test.

METHOD 2007.2

VIBRATION, VARIABLE FREQUENCY

1. PURPOSE. The variable frequency vibration test is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range. This is a destructive test.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the required variable frequency vibration at the specified levels and the necessary optical and electrical equipment for post-test measurements.

3. PROCEDURE. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall be vibrated with simple harmonic motion having either a peak to peak amplitude of 0.06 inch (±10 percent) or a peak acceleration of the specified test condition A, B, or C (+20 percent, -0 percent g). Test conditions shall be amplitude controlled below the crossover frequency and g level controlled above. The vibration frequency shall be varied approximately logarithmically between 20 and 2,000 Hz. The entire frequency range of 20 to 2,000 Hz and return to 20 Hz shall be traversed in not less than 4 minutes. This cycle shall be performed 4 times in each of the orientations X, Y, and Z (total of 12 times), so that the motion shall be applied for a total period of not less than 48 minutes. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Test condition	Peak acceleration, g
A	20
B	50
C	70

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Measurements after test (see 3 and 3.1).

METHOD 2009.8

EXTERNAL VISUAL

1. PURPOSE. The purpose of this examination is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable acquisition document. This test would normally be employed at the outgoing inspection from the device manufacturer's facility or as an incoming user inspection. This test may also be utilized to inspect for damage due to handling and mounting of the devices.

2. APPARATUS. Apparatus used in this test shall be capable of demonstrating device conformance to the applicable requirements, which may include optical equipment capable of magnification of 1.5X minimum and a relatively large and accessible field of view such as an illuminated ring magnifier.

3. PROCEDURE. The device shall be examined under a magnification of 1.5X to 10X (as applicable) with a field of view sufficiently large to contain the entire device and allow inspection in accordance with the requirements of the applicable acquisition specification and the criteria listed in 3.2. Where adherence of foreign material is in question, devices may be subjected to a clean filtered air stream (suction or expulsion) of 68 feet per second maximum, and reinspected.

3.1 Inspection criteria. Criteria listed in 3.2a and b shall be inspected at 1.5 to 3X on a 100 percent basis. Criteria listed in 3.2c through h (as applicable) shall be inspected at 1.5X to 10X on a 100 percent basis, or on a sample basis using an LTPD of 2 with maximum accept number of 0. If one or more rejects occur in the sample, the lot shall be reinspected 100 percent using a magnification no less than that used for the original inspection for the failed criteria.

3.2 Failure criteria. Devices shall fail if they exhibit any of the following:

a. Marking (content, placement, legibility, etc.) not in accordance with the applicable specification.

b. Leads or terminals which are not intact or aligned in their normal location, free of sharp or unspecified lead bends, or free of twist outside the normal lead plane.

c. Device design, lead (terminal) identification, materials, construction, or workmanship are not in accordance with the applicable specification or drawing.

d. Metal or ceramic packages with hard glass to metal seals or glass feed through type seal; or ceramic packages with brazed leads or leads exiting through the sealing glass which exhibit any of the following:

(1) Broken packages or cracks in the packages. Surface scratches shall not be cause for failure except where they violate other criteria stated herein for marking, finish, etc.

(2) Any chip out dimension that exceeds 0.010 inch in any direction on the surface and has a depth which exceeds 25 percent of the thickness of the affected package element (e.g., cover, base, or wall).

(3) Any chip out of ceramic or sealing glass that penetrates the sealing glass deeper than the glass meniscus plane, or that exposes any lead frame material that is not intended to be exposed by design. See 2009-1.

(4) Visible evidence of corrosion, contamination, breakage, grossly bent or broken leads, cracked seals (except for glass meniscus), defective (peeling, flaking, or blistering) or damaged (scratches, mars, or indentations which expose underplate or base metal) finish. Discoloration of the finish shall not be cause for failure unless there is evidence of flaking, pitting, or corrosion.

(5) External lead metallization stripe forming a conductor to a brazed lead which exhibits voids greater than 25 percent of the conductor width.

(6) Leads with pits or depressions, or both which exceed 25 percent of the width (diameter for round leads) and are greater than 50 percent of the lead thickness in depth.

(7) Leads with burrs exceeding a height greater than 50 percent of the lead thickness.

(8) Lead misalignment to the braze pad to the extent that less than 75 percent of the lead braze section is brazed to the pad.

(9) Metallization (including solder lead finish) in which the isolation between leads or between lead and other package metallization is reduced to less than 50 percent of the lead separation, but in no case less than the case outline minimum.

(10) Braze material flow, or other foreign material (i.e., contamination or corrosion) which reduces the isolation between leads or between braze pads to less than 50 percent of lead separation (pad separation for brazed leads) but in no case less than the case outline minimum.

(11) Protrusions on the bottom (mounting) surface of the package which extend beyond the seating plane.

(12) Protrusions (excluding glass run out) on any other package surface which exceeds the lead thickness in height.

(13) Evidence of cracks, delamination, separation, or voiding on any multilayer ceramic package.

(14) Braze material which increases the lead dimensions to greater than 1.5 times the lead thickness above the design maximum between the seating plane and the ceramic body or which increases the lead dimensions to greater than the design maximum below the seating plane.

(15) Leads or terminals which are not free of foreign material such as paint or other adherent deposits.

e. Defects in the sealing glass on packages with hard glass seals, bead seals, or feed-through glass seals of individual leads which exhibit any of the following:

(1) Crazing of glass-seal surface (see figure 2009-2).

(2) Radial cracks that originate at the case body glass-to-metal and propagate inward toward the leads (see figure 2009-3).

(3) Radial or circumferential cracks which extend beyond, or are located in the region beyond the midpoints of distance from the lead to the case (see figure 2009-4 and 2009-5).

(4) Any single circumferential crack (or overlapping cracks) which do(es) not lie completely within a single quadrant (i.e., extends beyond 90° arc or rotation about the lead) (see figure 2009-5).

(5) Meniscus cracks, except those located within one-half the distance from between the lead to the case (metal-to-metal), (see figure 2009-6). The glass meniscus is defined as that area of glass which wicks up the lead or terminal. Hair-line cracks occurring in the glass meniscus are called meniscus cracks.

(6) Reentrant seals which exhibit nonuniform wicking (i.e., negative meniscus) at the lead or body interface, or both (see figure 2009-8.)

(7) Voids, or open or closed bubbles in the sealing glass (see figure 2009-7).

f. Ceramic packages without leads (e.g., leadless chip carriers) which exhibit any of the following:

(1) Visible evidence of corrosion, contamination, breakage, cracked seals or defective (peeling, flaking, or blistering) or damaged (scratches, mars, or indentations exposing underplate or base metal) finish or evidence of plating nonadhesion. (Discoloration of finish shall not be cause for failure unless there is evidence of flaking, pitting, or corrosion.)

(2) Ceramic chip-outs that dimensionally exceed 50 percent of the distance between terminals in any direction on the affected surface (edge or corner), and exceed a depth of 25 percent of the thickness of the affected package element (e.g., cover, lid, base or wall).

(3) Evidence of cracks, delamination, separation or voiding on any package element.

(4) Lid or cover protrusions that exceed 25 percent of the terminal width in height.

(5) Protrusions that exceed 25 percent of the terminal width in height beyond the surface plane of the solder pads.

(6) Metallization (not intended by design) between solder pads, between elements of thermal patterns and between seal ring or lid to metallized castellations which reduces the isolation to less than 50 percent of pad separation.

(7) Castellation to solder pad misalignment. The metal in the castellation, exclusive of the annular ring, shall be within the visually extended boundaries of the solder pad.

(8) Castellation configuration not in accordance with the following (see figure 2009-10). The castellation shall be roughly concave, confined by a 3-dimensional space traversing all castellated ceramic layers at the package edge. The surface of the castellation may be irregular. The "3-dimensional space" has these dimensions:

Minimum width > one-third package terminal pad width
Minimum depth > one-half castellation minimum width
Length = As designed (see figure 2009-10)
Maximum width ≤ package terminal pad width
Maximum depth ≤ one-half castellation maximum width

These dimensions attempt to assure with some reasonableness that the castellations are not viewed, in the extreme sense, as virtual flat surfaces on the package edge and are not virtual closed vias (holes).

* g. Evidence of any nonconformance with the detail drawing or applicable acquisition document, absence of any required feature, or evidence of damage, corrosion, or contamination which will interfere with the normal application of the device.

h. Dual-in-line packages exhibiting any visible scratch, mar, or indentation in the surface finish of the lead above the seating plane that exceeds more than one-half the width of the lead and severely damages the finish or exposes underplate or base metal.

* 4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Requirements for markings and the lead (terminal), or pin identification.

b. Detailed requirements for materials, design, construction, and workmanship.

c. Magnification if other than specified.

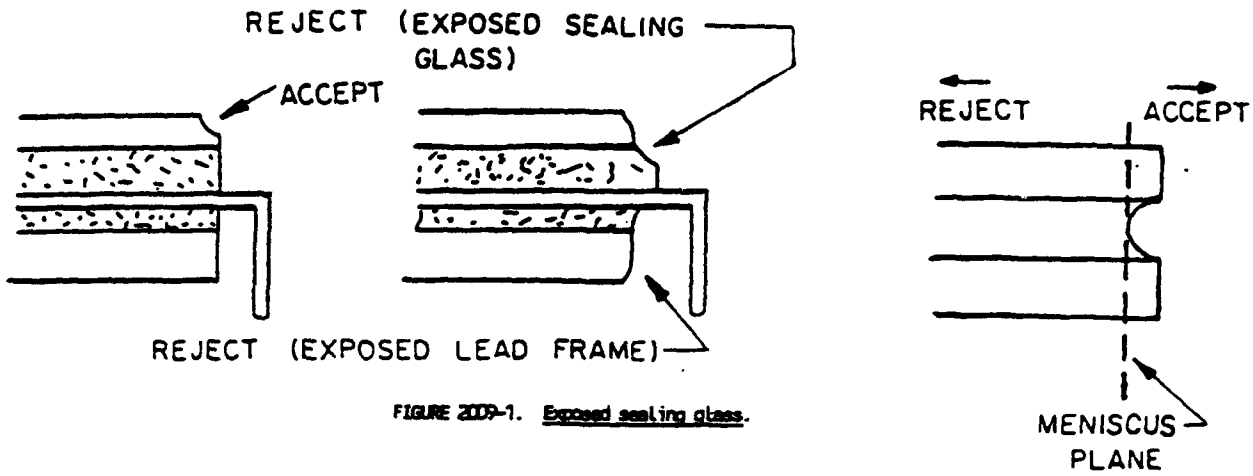

FIGURE 2009-1. Exposed sealing glass.

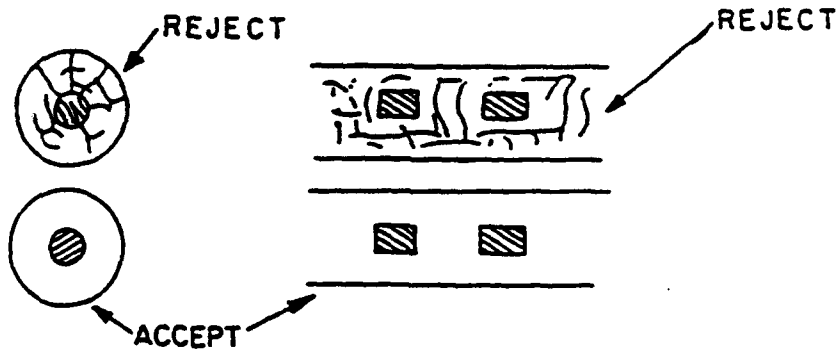

FIGURE 2009-2. Crazed glass surface.

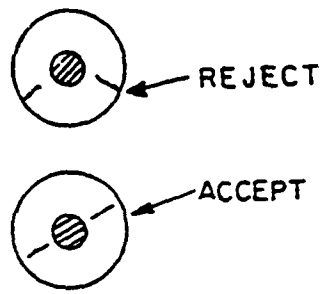

FIGURE 2009-3. Cracks propagating toward lead.

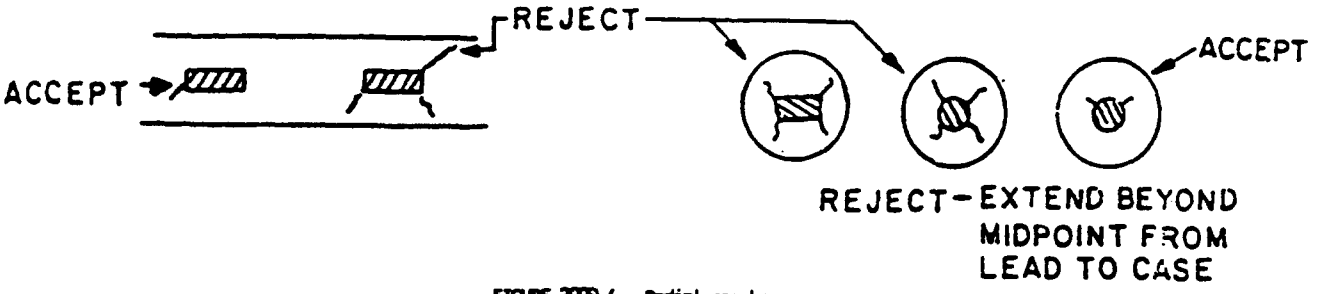

FIGURE 2009-4. Radial cracks.

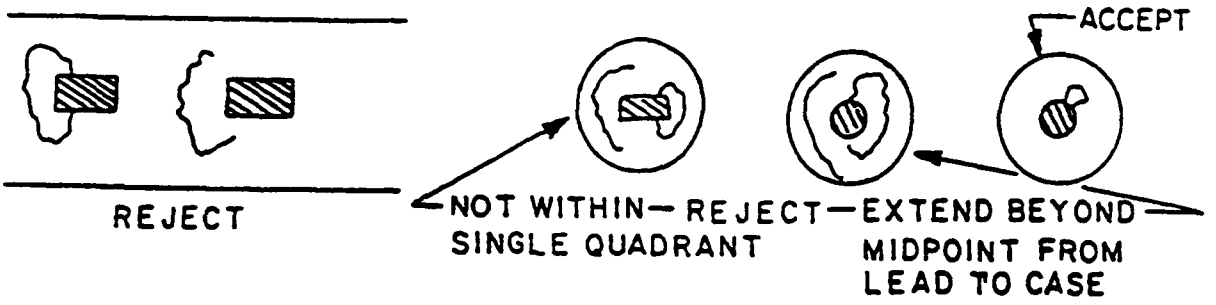

FIGURE 2009-5. Circumferential cracks.

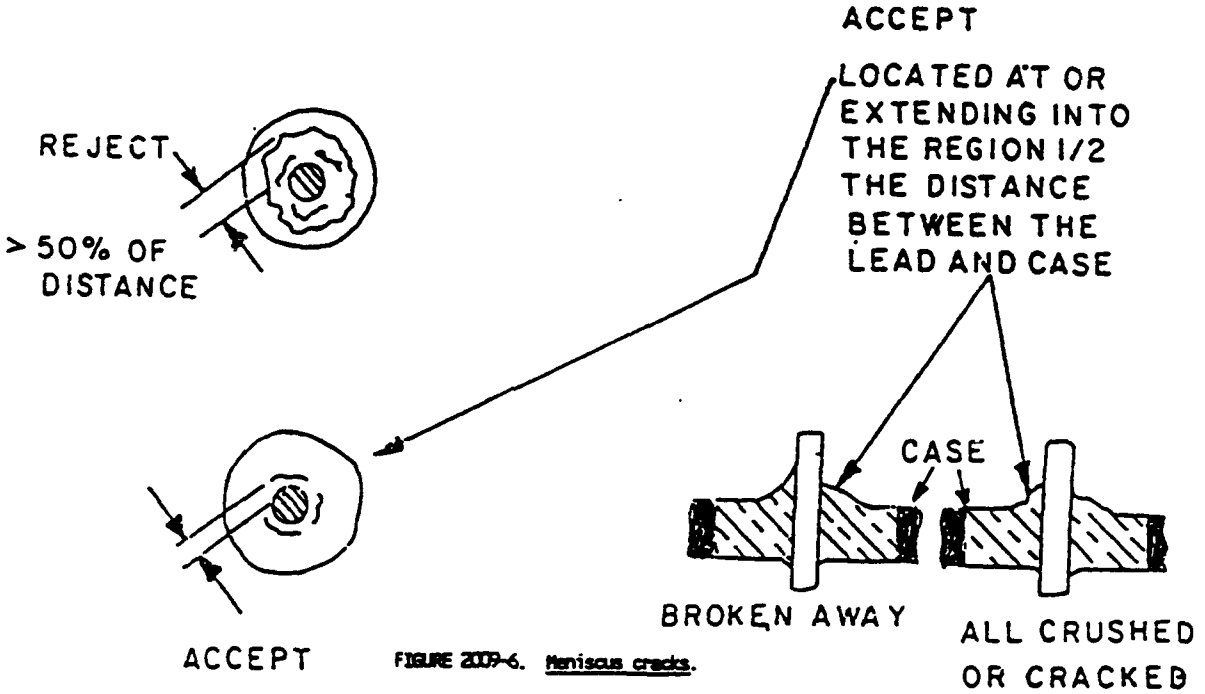

FIGURE 2009-6. Meniscus cracks.

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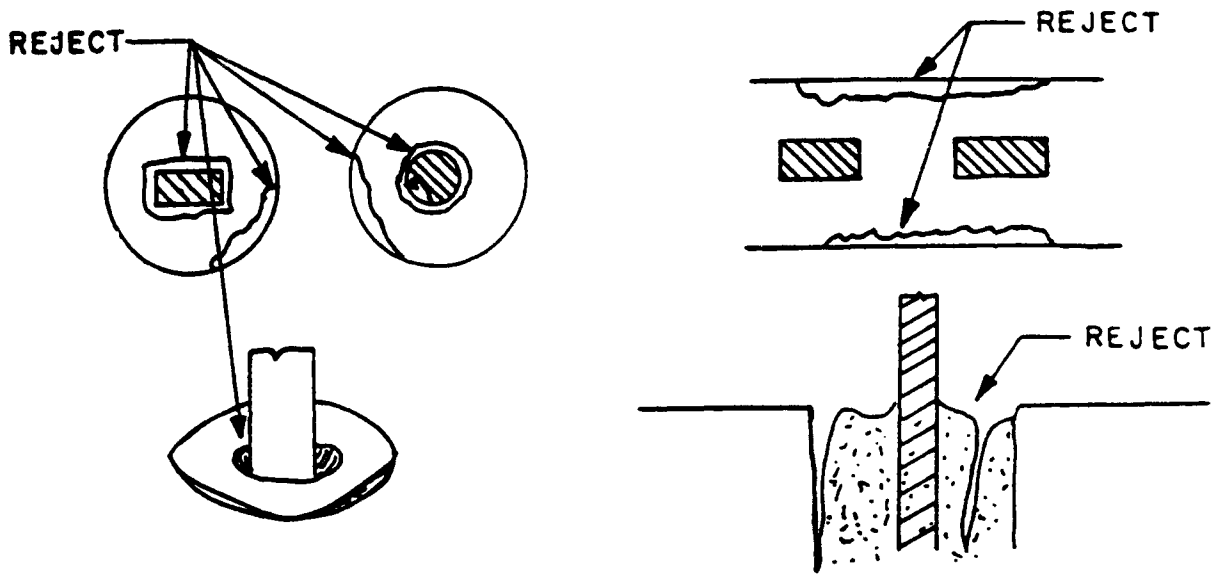


FIGURE 2009-7. Voids in sealing glass.

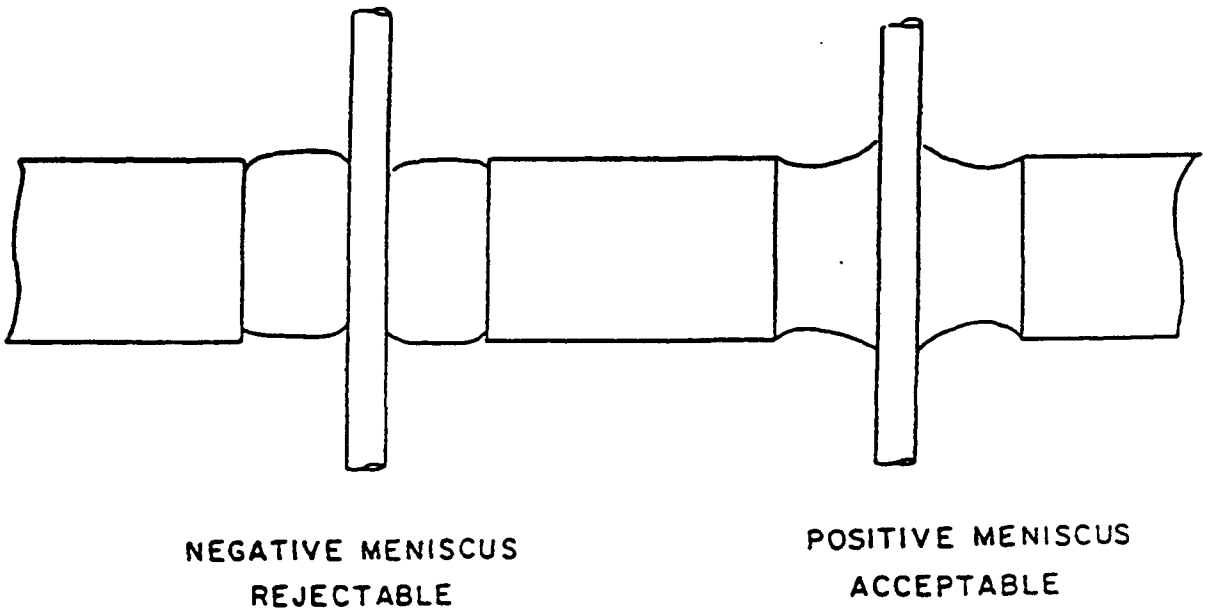


FIGURE 2009-8. Reentrant seals.

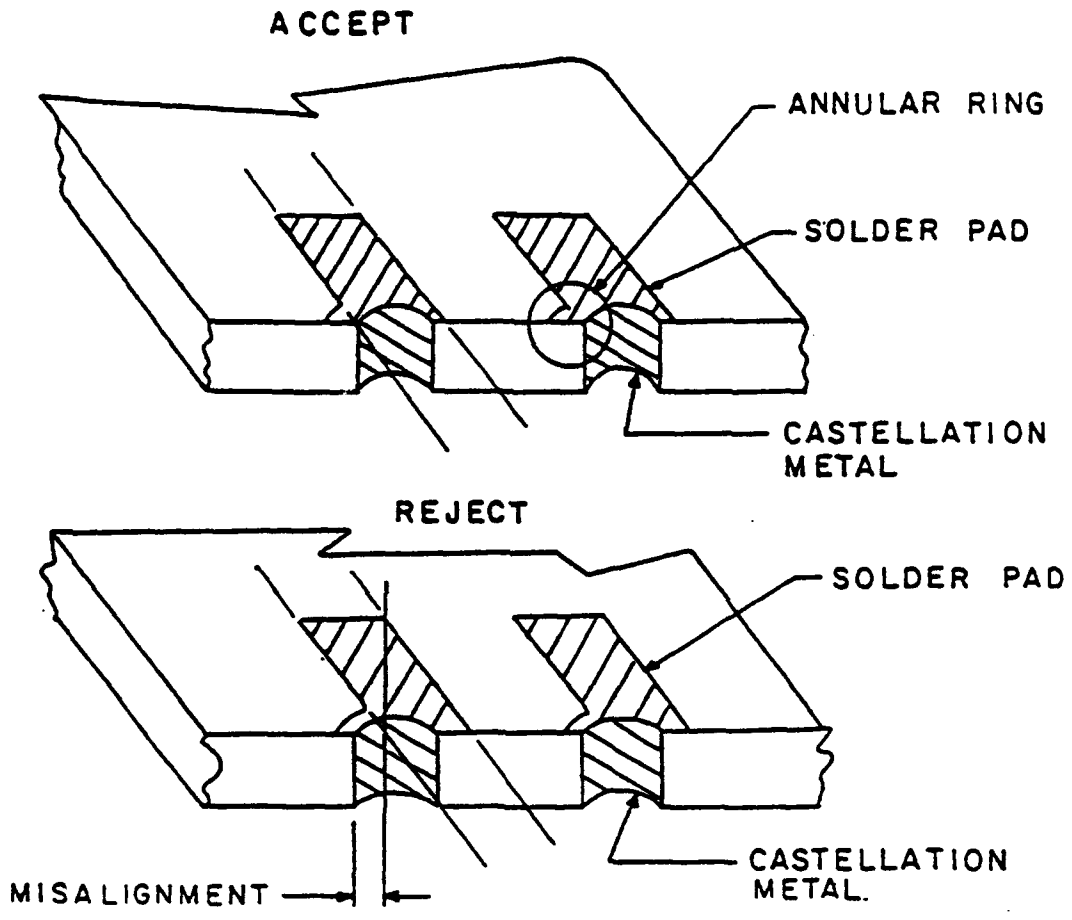
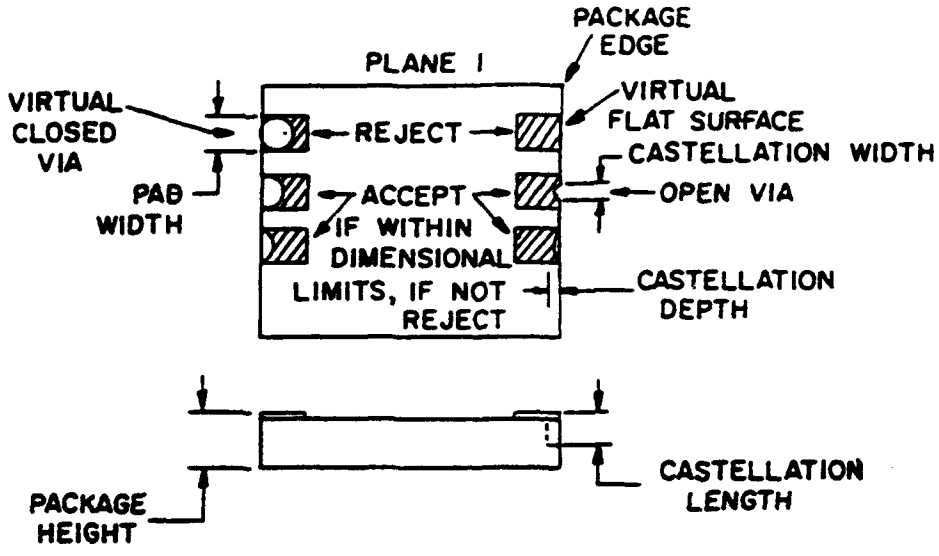
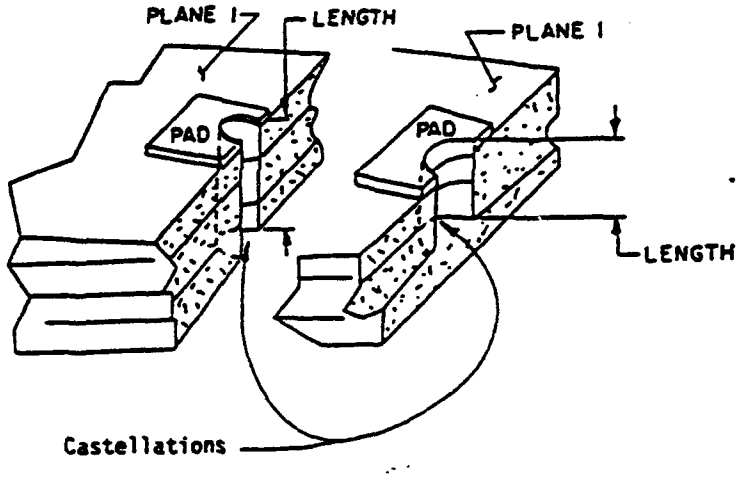


FIGURE 2009-9. Castellation to solder pad alignment.





Through two and three layers of ceramic.

Note: Ceramic layers shift, edges are rough after punching, plating buildup is not smooth, etc., all of these combine during package manufacture to make the castellation measurement difficult. Therefore, in the event of conflicts in determining castellation acceptance, direct contact measurement shall be made using the limits specified in MIL-STD-1835.

FIGURE 2009-10. Castellation requirements.

METHOD 2010.10

INTERNAL VISUAL (MONOLITHIC)

1. PURPOSE. The purpose of this test is to check the internal materials, construction, and workmanship of microcircuits for compliance with the requirements of the applicable acquisition document. This test will normally be used prior to capping or encapsulation on a 100 percent inspection basis to detect and eliminate devices with internal defects, that could lead to device failure in normal applications. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices. Furthermore, the criteria of this test method will be used during destructive physical analysis (DPA) following the procedures outlined in test method 5009, "Destructive Physical Analysis". Test condition A and B provide a rigorous and detailed procedure for internal visual inspection of high reliability microcircuits as specified in the screening requirements of test method 5004. For condition B product the alternate screening procedure documented in test method 5004 may be used by the manufacturer as an option to internal visual inspection as specified.

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification and any visual standards (gauges, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

2.1 GaAs device requirements. GaAs devices shall be inspected to all applicable criteria as listed herein. GaAs microwave devices shall also have additional specific criteria as listed and the applicable high power magnification for individual features of GaAs microwave devices shall be selected from the following table.

TABLE I. GaAs microwave device high magnification requirements.

Feature dimensions	Magnification range
> 5 microns	75-150X
1-5 microns	150-400X
< 1 micron	400-1000X

* 2.2 Silicon-on-Sapphire (SOS) device requirements. SOS devices shall be inspected to all applicable criteria specified herein, except where noted. The sapphire portions of the die shall be considered "nonconductive and nonoperational material".

3. PROCEDURE.

a. General. The device shall be examined within the specified magnification range to determine compliance with the requirements of the applicable acquisition document and the criteria of the specified test condition.

The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device process or technology, it has been indicat[illegible].

b. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer.

When inverted die mounting techniques are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to attachment of the die. Devices which fail any test criteria herein are defective devices and shall be rejected and removed at the time of observation.

Visual criteria may be inspected as follows:

(1) Prior to die attachment without re-examination after die attachment; 3.1.1.2, 3.1.1.5, 3.1.1.7, 3.1.2, 3.1.4 e and f, 3.1.5, 3.1.6 a-f, 3.2.6.

(2) Prior to bonding without re-examination after bonding; 3.2.3.

(3) For condition B only; the following criteria may be inspected prior to die attachment at high power, plus low power after die attachment, provided a high magnification sample to LTPD 5 is performed at precap inspection; 3.1.1.1, 3.1.1.3, 3.1.1.4, 3.1.1.6, 3.1.3, 3.1.4 a-d and g-o, 3.1.6 g and h, 3.1.7. If the sample fails the entire lot shall be reinspected at high magnification for the failed criteria.

* c. Inspection control. In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections in accordance with 3b, to insure that defects created during subsequent handling will be detected and rejected at final preseal inspection. During the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment. Devices examined to condition A shall be inspected and prepared for sealing in class 100 environment and devices examined to condition B criteria shall be inspected and prepared for sealing in a class 100,000 environment, (see 30.1.1.7 of appendix C of MIL-I-38535) except that the maximum allowable relative humidity in either environment shall not exceed 65 percent. Devices shall be in covered containers when transferred from one controlled environment to another.

* d. Magnification. "High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination perpendicular to the die surface. "Low magnification" inspection shall be performed with a metallurgical or stereomicroscope with the device under suitable illumination. Low magnification may be performed at an angle other than 90° to the die surface to facilitate the inspection. The inspection criteria of 3.2.1 may be examined at "high magnification" at the manufacturer's option.

* e. Reinspection. When inspection for product acceptance is conducted subsequent to the manufacturer's inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the acquisition document. When suspected defects or deficiencies are noted, additional inspection may be performed at magnifications needed to evaluate or resolve the suspect items. When sampling is used, 60.4 appendix A of MIL-I-38535 shall apply.

f. Definitions:

(1) Active circuit area. All areas enclosed by the perimeter of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.

(2) Coupling (air) bridge. A raised layer of metallization used for interconnection that is isolated from the surface of the element.

(3) Block resistor. A thin film resistor which for purposes of trimming is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.

(4) Channel. An area lying between the drain and the source of FET structures.

* (5) Controlled environment. Shall be class 1,000, (see 30.1.1.7 of appendix C of MIL-I-38535), except that the maximum allowable relative humidity shall not exceed 65 percent.

(6) Crazing. The presence of numerous minute cracks in the referenced material, (e.g., glassivation crazing).

(7) Detritus. Fragments of original or laser modified resistor material remaining in the kerf.

(8) Dielectric isolation. Electrical isolation of one or more elements of a monolithic semiconductor integrated circuit by surrounding the elements with an isolating barrier such as semiconductor oxide.

(9) Diffusion tub. A volume (or region) formed in a semiconductor material by a diffusion process (n- or p- type) and isolated from the surrounding semiconductor material by a n-p or p-n junction or by a dielectric material (dielectric isolation, coplanar process, SOS, SOI).

(10) Foreign material. Any material that is foreign to the microcircuit or package, or any nonforeign material that is displaced from its original or intended position within the microcircuit package.

NEW PAGE

(22) Narrowest resistor width. The narrowest portion of a given resistor prior to trimming.

(23) Operating metallization (conductors). Metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.

(24) Original width. The width dimension or distance that would have been present, in the absence of the observed abnormality (e.g., original metal width, original diffusion width, original beam width, etc.).

(25) Package post. A generic term used to describe the bonding location on the package.

(26) Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal or between metal levels on multilevel devices.

(27) Passivation step. An abrupt change of elevation (level) of the passivation such as a contact window, or operating metallization crossover.

(28) Peripheral metal. All metal that lies immediately adjacent to or over the scribe grid.

(29) Shooting metal. Metal (e.g., aluminum, gold) expulsion of various shapes and lengths from under the wire bond at the bonding pad.

(30) Substrate. The supporting structural material into or upon which or both the passivation, metallization and circuit elements are placed.

(31) Substrate via. A small hole formed through the wafer and metallized, causing electrical connection to be made from the frontside (the side on which the circuitry is formed) to the backside of the wafer.

(32) Thick film. That conductive/resistive/dielectric system that is a film having greater than 50,000Å thickness.

(33) Thin film. That conductive/resistive/dielectric system that is a film equal to or less than 50,000Å in thickness.

(34) Via metallization. That which connects the metallization of one level to another.

g. Interpretations. Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used for confirming that a reject condition does not exist, they shall be approved by the acquiring activity. For inspections performed on the range of 75X to 100X, the criteria of 0.1 mil of passivation, separation or metal can be satisfied by a line of separation or a line of metal visible.

h. Foreign material control. The manufacturer shall perform an audit on a weekly basis for (1) the presence of foreign material within incoming piece part lids and bases, and (2) the presence of foreign material on the die surface or within the package of assembled parts.

The audit of assembled parts may be satisfied during routine internal visual inspection. If the presence of foreign material is discovered, the manufacturer shall perform the necessary analysis on a sample of the foreign material on the suspect devices to determine the nature of the material. The manufacturer shall document the results of this investigation and corrective action to eliminate the foreign material and this information will be available to the Government QAR, and the acquiring activity or the qualifying activity, as applicable. A corrective action plan shall be obtained within a maximum of 10 working days of discovery.

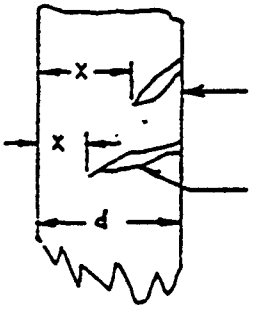
The audit of incoming piece part lids and bases shall be performed before parts are assembled, or may be satisfied during routine incoming quality inspection. If the presence of foreign material of a size 1 mil or greater is discovered, the manufacturer will analyze the foreign material to determine its nature and document the results of the analysis. If applicable, these results shall be distributed to the vendor supplying the parts, with the request that the vendor document corrective actions to minimize or eliminate such foreign material. This information will be available to the manufacturer, Government QAR, and the acquiring activity or qualifying activity, as applicable.

NOTE: The piece part audit requirements can be replaced by a piece part cleaning process, approved by the qualifying activity, that is always performed either prior to or during the assembly process and these piece parts are stored in a controlled environment until they are used.

The intent of these procedures is to require investigation and resolution of foreign material problems that do not have an effective screening or detection methodology but that could cause degradation and eventual failure of the device function. Repetitive findings without obvious improvements require escalation to Director of Manufacturing and Director of Quality Assurance to continue processing.

Condition A Class S	Condition B Class B
3.1 High power inspection. Internal visual examination as required in 3.1.1 through 3.1.3 shall be conducted on each microcircuit. In addition, the applicable criteria contained in 3.1.4 through 3.1.7 shall be used for the appropriate microcircuit area where glassivation, dielectric isolation or film resistors are used.	
* NOTE: Unless otherwise specified, for flip chip product the criteria of 3.1 shall apply only to top circuit side inspection. After die mounting, only criteria in 3.1.3i shall apply.	
The high magnification inspection shall be within the range of 100X to 200X.	The high magnification inspection shall be within the range of 75X to 150X.
* For high magnification inspection of GaAs microwave devices, see table I herein. Also, for < 1 micron features, the manufacturer may implement a sample inspection plan which shall be documented in the manufacturer's internal procedure and approved by the qualifying activity.	
3.1.1 Metallization defects. No device shall be acceptable that exhibits the following defects in the operating metallization.	
3.1.1.1 Metallization scratches:	
a. Scratch in the metallization excluding bonding pads and beam leads that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-4).	a. Scratch in the metallization, excluding bonding pads and beam leads, that exposes underlying passivation anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see figure 2010-5).

NOTE: For GaAs microwave devices, scratches in the gate stripe or gate insertion metallization.



For single layer metal products

Accept: Scratch where the remaining undisturbed metal width (X) is greater than d/2 (50 percent).

Reject: Scratch where the remaining undisturbed metal width (X) is less than d/2 (50 percent).

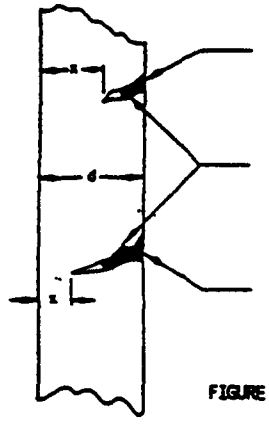
FIGURE 2010-4. Metallization scratch criteria for class S.

Condition A
Class S

b. For condition A, see 3.1.1.1a above.

Condition B
Class B

For single layer metal products



Accept: Scratch exposing underlying passivation where the remaining undisturbed metal width (X) is greater than d/2 (50 percent).

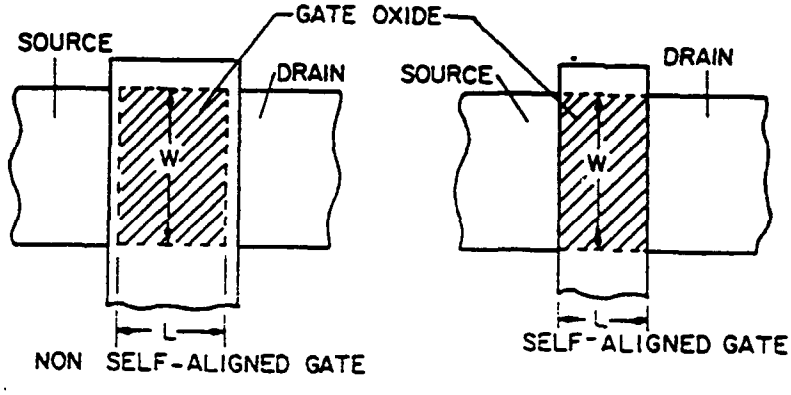
Underlaying passivation

NOTE:
d = Original metal width
X = Undisturbed metal width

Reject: Scratch exposing underlying passivation where the remaining undisturbed metal width (X) is less than d/2 (50 percent).

FIGURE 2010-5. Metallization scratch criteria for class B.

b. For condition B only. Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation, glassivation, or substrate on either side (for MOS devices, the path shall be the (L) dimension) (see figure 2010-6).



NOTE: When standard metallization scratch criterion is applied to the gate area, the dimensions (W) and (L) shall be considered as the original channel width and length respectively.

FIGURE 2010-6. MOS scratch criteria.

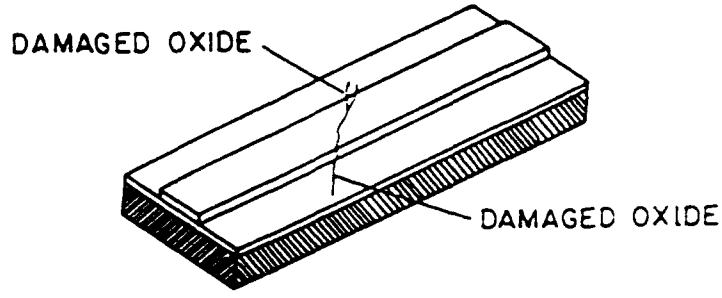
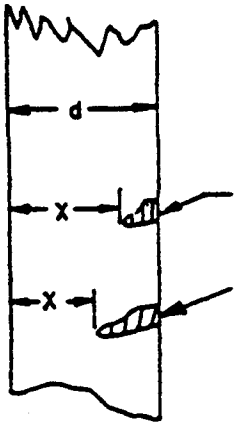
Condition A Class S	Condition B Class B
	
c. Scratch in multilayered metallization, excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 75 percent of the original metal width undisturbed (see figure 2010-7).	c. Scratch in multilayered metallization, excluding bond pads and beam leads that exposes the underlying metal anywhere along its length and leaves less than 25 percent of the original metal width undisturbed (see figure 2010-8).

FIGURE 2010-6. MOS scratch criteria - Continued.



For multilayered metal products only

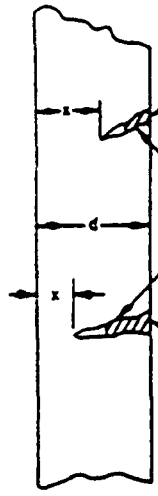
Accept: Scratch exposing underlying metal or passivation where the remaining undisturbed metal width (X) is greater than 3/4 d (75 percent).

Reject: Scratch exposing underlying metal or passivation where the remaining undisturbed metal width (X) is less than 3/4 d (75 percent).

FIGURE 2010-7. Scratch criteria for class S.

Condition A
Class S

Condition B
Class B



For multilayered metal products only

Accept: Scratch exposing underlying metal where the remaining undisturbed metal width (x) is greater than d/4 (25 percent).

Underlying Metal

NOTE:
d = Original metal width
x = Undisturbed metal width

Reject: Scratch exposing underlying metal where the remaining undisturbed metal width (x) is less than d/4 (25 percent).

FIGURE 2010-8 Scratch criteria for class B.

NOTE: For condition B only. Criteria 3.1.1.1a, b, and c can be excluded for peripheral power or ground metallization where parallel paths exist such that an open at the scratch would not cause an unintended isolation of the metallization path.

d. Scratch in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: For condition B only. Criteria 3.1.1.1a, b, c, and d can be excluded for the last 25 percent of the linear length of the contact cut and all metal beyond, on the termination end(s) of the metallization runs. In these cases there shall be at least 50 percent of the contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-9).

Condition A Class S	Condition B Class B

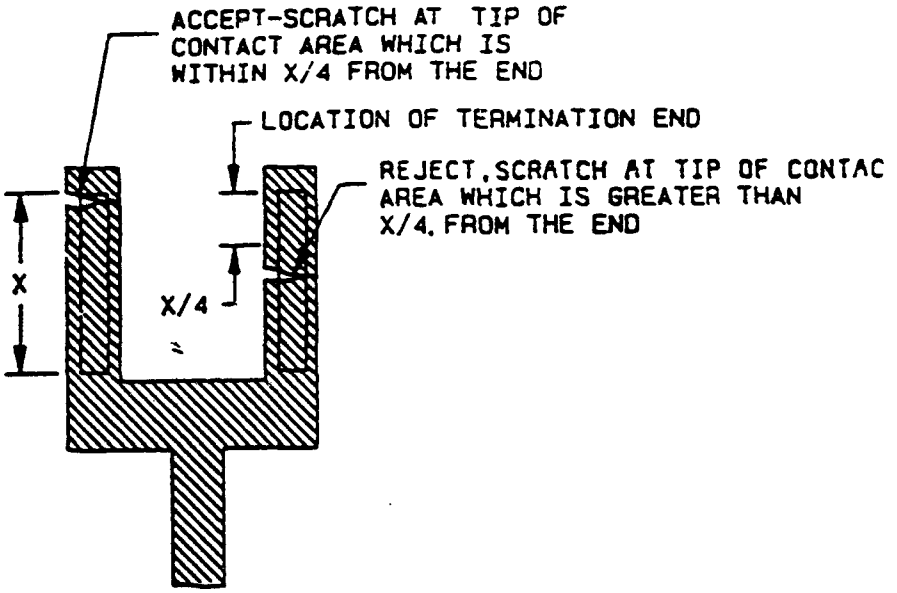


FIGURE 2010-9. Termination ends.

e. Scratch in the metallization, over the gate oxide (applicable to MOS structures only) (see figure 2010-10).	e. Scratch in the metallization, over the gate oxide, that exposes underlying passivation and leaves less than 50 percent of the length or width of the metallization between source and drain diffusion undisturbed (applicable to MOS structures only) (see figure 2010-11).

Condition A
Class S

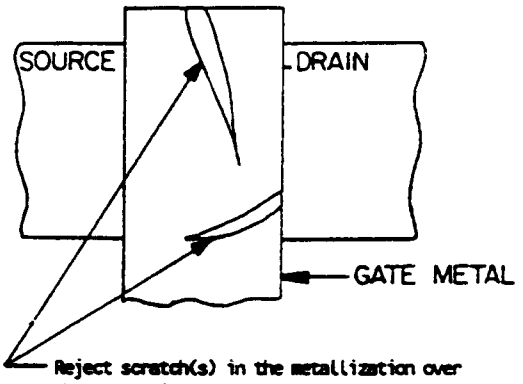


FIGURE 2010-10. MOS scratch criteria for class S.

Condition B
Class B

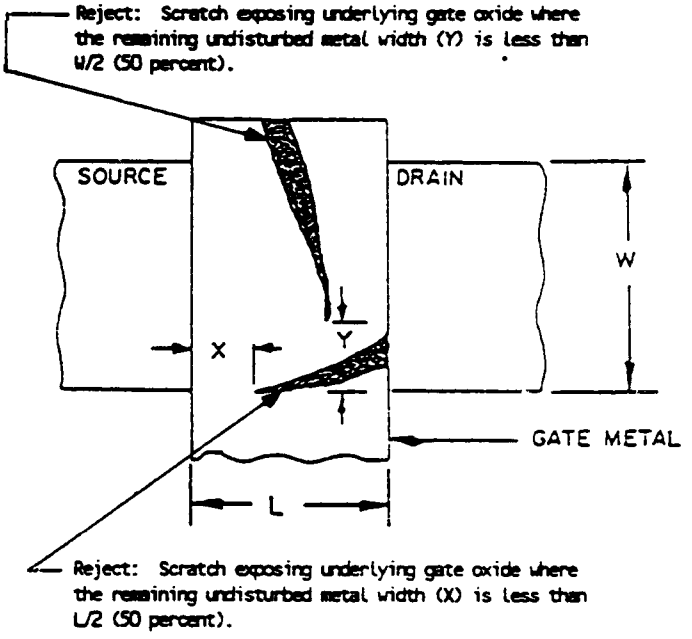


FIGURE 2010-11. MOS scratch criteria for class B.

Condition A Class S	Condition B Class B

f. Scratch in the metallization that exposes the dielectric material of a thin film capacitor or crossover. (Not applicable to air bridges.)

g. Scratch in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.

g. Scratch in the bonding pad or fillet area that exposes underlying passivation or substrate and reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.

h. Scratch(es) (probe mark(s), etc.) in the bonding pad area that exposes underlying passivation or substrate and leaves less than 75 percent of the unglassivated metallization area undisturbed.

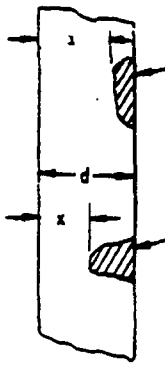
* i. For GaAs devices only, any tear in the air bridge metallization.

* j. For GaAs devices only, any lowering of the air bridge arch over active metallization due to mechanical damage (e.g., a scratch).

3.1.1.2 Metallization voids:

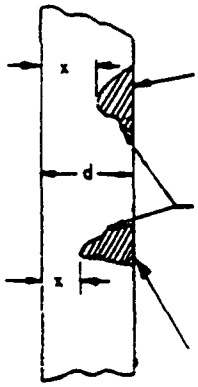
a. Void(s) in the metallization that leaves less than 75 percent of the original metal width undisturbed (see figure 2010-12).

a. Void(s) in the metallization that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-13).



Accept: Void exposing underlying metal or passivation where the remaining undisturbed metal width (X) is greater than 3/4 d (75 percent).

Reject: Void exposing underlying metal or passivation where the remaining undisturbed metal width (X) is less than 3/4 d (75 percent).



Accept: Void exposing underlying metal where the remaining undisturbed metal width (X) is greater than d/2 (50 percent).

Underlying Metal or Passivation

NOTE:
d = Original metal width
X = Undisturbed metal width

Reject: Void exposing underlying metal width the remaining undisturbed metal width (X) is less than d/2 (50 percent).

FIGURE 2010-12. Void criteria for class S.

FIGURE 2010-13. Void criteria for class B.

NOTE: For condition B only. Criteria can be excluded for peripheral power or ground metallization where parallel paths exist so that an open at the void(s) would not cause an unintended isolation of the metallization path.

Condition A Class S	Condition B Class B

b. Void(s) in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: For condition B only. Criteria of 3.1.1.2a and b can be excluded for the last 25 percent of the linear length of the contact cut and all metal beyond on the termination end(s) of metallization runs. In these cases there shall be at least 50 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-14).

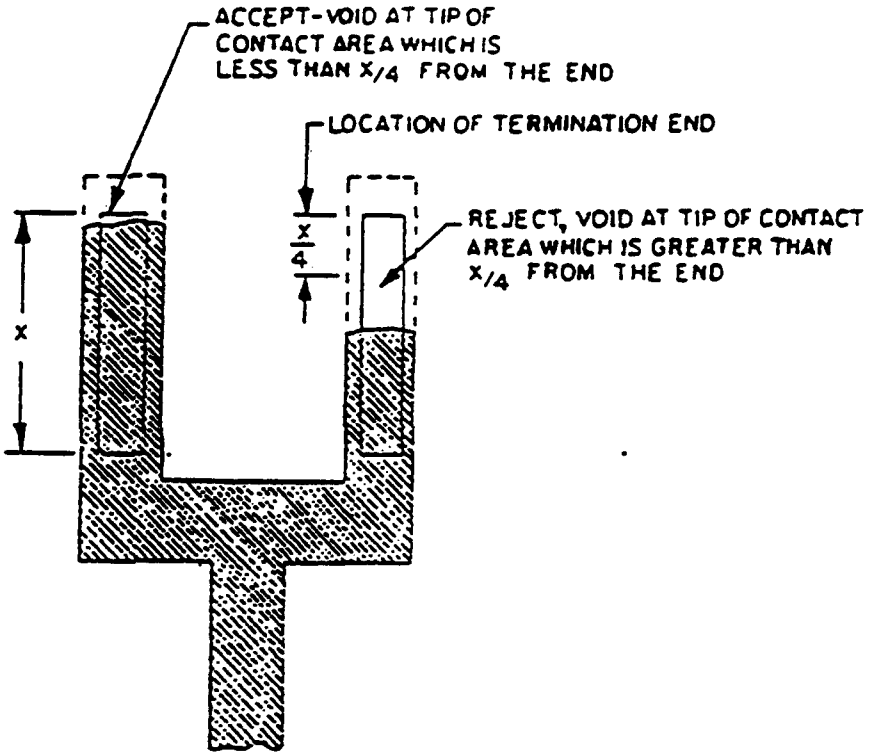


FIGURE 2010-14. Termination ends.

c. Void(s) in the metallization over the gate oxide that leaves less than 75 percent of the metallization length (L) or width (W) between source and drain diffusions undisturbed (applicable to MOS structures only) (see figure 2010-15).

Condition A Class S	Condition B Class B
d. Void(s) that leave less than 75 percent of the metallization area over the gate oxide undisturbed (applicable to MOS structures only).	d. Void(s) that leave less than 60 percent of the metallization area over the gate oxide undisturbed (applicable to MOS structures only).

e. Void(s) that leaves less than 75 percent of the metallization width coincident with the source or drain diffusion junction line undisturbed (applicable to MOS structures only) (see figure 2010-15).

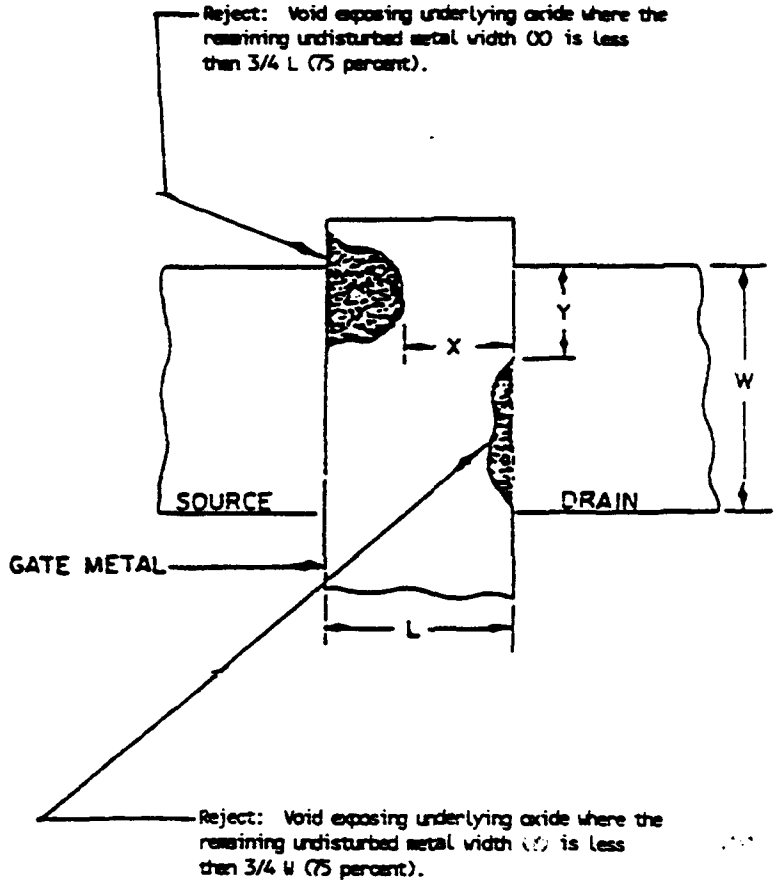


FIGURE 2010-15. MOS void criteria.

f. Void(s) in the bonding pad area that leaves less than 75 percent of its original unglassivated metallization area undisturbed (see figure 2010-16).

g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 75 percent of the narrowest entering metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately. (see figure 2010-16).	g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately (see figure 2010-16).

METHOD 2011.7

BOND STRENGTH (DESTRUCTIVE BOND PULL TEST)

1. PURPOSE. The purpose of this test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead or flip chip devices.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the test condition specified in the applicable acquisition document consistent with the particular device construction. All bond pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Unless otherwise specified, for conditions A, C, and D, the LTPD specified for the bond strength test shall determine the minimum sample size in terms of the minimum number of bond pulls to be accomplished rather than the number of complete devices in the sample, except that the required number of bond pulls shall be randomly selected from a minimum of 4 devices. Bond pulls in accordance with test conditions D, F, G, and H, while involving two or more bonds shall count as a single pull for bond strength and LTPD purposes. Unless otherwise specified, for conditions F, G, and H the LTPD specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices (all conditions), a minimum of 4 die or use all die if four are not available on a minimum of 2 completed devices shall be used. Where there is any adhesive, encapsulant or other material under, on or surrounding the die such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

When flip chip or beam-lead chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Test conditions:

3.1.1 Test condition A - Bond peel. This test is normally employed for bonds external to the device package. The lead or terminal and the device package shall be gripped or clamped in such a manner that a peeling stress is exerted with the specified angle between the lead or terminal and the board or substrate. Unless otherwise specified, an angle of 90 degrees shall be used. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.2 Test condition C - Wire pull (single bond). This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. The wire connecting the die or substrate shall be cut so as to provide two ends accessible for pull test. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull test at the opposite termination. The wire shall be gripped in a suitable device and simple pulling action applied to the wire or to the device (with the wire clamped) in such a manner that the force is applied approximately normal to the surface of the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.3 Test condition D - Wire pull (double bond). This procedure is identical to that of test condition C, except that the pull is applied by inserting a hook under the lead wire (attached to die, substrate or header or both ends) with the device clamped and the pulling force applied approximately in the center of the wire in a direction approximately normal to the die or substrate surface or approximately normal to a straight line between the bonds. When a failure occurs, the force causing the failure and the failure category shall be recorded. The minimum bond strength shall be taken from table I. Figure 2011-1 may be used for wire diameters not specified in table I. For wire diameter or equivalent cross section >0.005 inch, where a hook will not fit under the wire, a suitable clasp can be used in lieu of a hook.

3.1.4 Test condition F - Bond shear (flip chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted. A suitable tool or wedge shall be brought in contact with the die (or carrier) at a point just above the primary substrate and a force applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate, to cause bond failure by shear. When a failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.5 Test condition G - Push-off test (beam lead). This test is normally employed for process control and is used on a sample of semiconductor die bonded to a specially prepared substrate. Therefore, it cannot be used for random sampling of production or inspection lots. A metallized substrate containing a hole shall be employed. The hole appropriately centered, shall be sufficiently large to provide clearance for a push tool, but not large enough to interfere with the bonding areas. The push tool shall be sufficiently large to minimize device cracking during testing, but not large enough to contact the beam leads in the anchor bond area. Proceed with push-off tests as follows: The substrate shall be rigidly held and the push tool inserted through the hole. The contact of the push tool to the silicon device shall be made without appreciable impact (less than 0.01 inch/minute (0.254 mm/minute) and forced against the underside of the bonded device at a constant rate. When failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.6 Test condition H - Pull-off test (beam lead). This test is normally employed on a sample basis on beam lead devices which have been bonded down on a ceramic or other suitable substrate. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or Kovar wire) to make connection with a hard setting adhesive material (for instance, heat sensitive polyvinyl acetate resin glue) on the back (top side) of the beam lead die. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The device shall be pulled within 5 degrees of the normal to at least the calculated force (see 3.2), or until the die is at 2.54 mm (0.10 inch) above the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any bond pull which results in separation under an applied stress less than that indicated in table I as the required minimum bond strength for the indicated test condition, composition, and construction shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the category of separation or failure shall be recorded.

a. For internal wire bonds:

(a-1) Wire break at neckdown point (reduction of cross section due to bonding process).

(a-2) Wire break at point other than neckdown.

(a-3) Failure in bond (interface between wire and metallization) at die.

(a-4) Failure in bond (interface between wire and metallization) at substrate, package post, or other than die.

(a-5) Lifted metallization from die.

(a-6) Lifted metallization from substrate or package post.

(a-7) Fracture of die.

(a-8) Fracture of substrate.

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b. For external bonds connecting device to wiring board or substrate:

(b-1) Lead or terminal break at deformation point (weld affected region).

(b-2) Lead or terminal break at point not affected by bonding process.

(b-3) Failure in bond interface (in solder or at point of weld interface between lead or terminal and the board or substrate conductor to which the bond was made).

(b-4) Conductor lifted from board or substrate.

(b-5) Fracture within board or substrate.

c. For flip-chip configurations:

(c-1) Failure in the bond material or pedestal, if applicable.

(c-2) Fracture of die (or carrier) or substrate (removal of portion of die or substrate immediately under the bond).

(c-3) Lifted metallization (separation of metallization or bonding pedestal from die (or carrier) or substrate.

d. For beam lead devices:

(d-1) Silicon broken.

(d-2) Beam lifting on silicon.

(d-3) Beam broken at bond.

(d-4) Beam broken at edge of silicon.

(d-5) Beam broken between bond and edge of silicon.

(d-6) Bond lifted.

(d-7) Lifted metallization (separation of metallization) from die, separation of bonding pad.

(d-8) Lifted metallization.

NOTE: RF/microwave hybrids that require extremely flat loops which may cause erroneous wire pull data may use the following formula to determine the proper wire pull value.

$V_1 = V_2 \sin \Theta$

Where: V_1 = New value to pull test.
V_2 = Table I value for size wire tested.
Θ = Greatest calculated wire loop angle (figure 2011-2).

Also, RF/microwave hybrids that contain wires that cannot be accessed with a pull hook must be duplicated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production hybrids are bonded using the same setup, operator, and schedule. The test coupon wires are to be pull tested in lieu of the tuning or inaccessible wires on the production hybrid. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (figure 2011-3).

TABLE I. Minimum bond strength.

Test condition	Wire composition and diameter 1/	Construction 2/	Minimum bond strength (grams force)	
			Pre seal	Post seal and any other processing and screening when applicable
A	—	—	Given in applicable document	Given in applicable document
C or D	AL 0.0007 in AU 0.0007 in	Wire	1.5 2.0	1.0 1.5
C or D	AL 0.0010 in AU 0.0010 in	Wire	2.5 3.0	1.5 2.5
C or D	AL 0.00125 in AU 0.00125 in	Wire	Same bond strength limits as the 0.0013 in wire	
C or D	AL 0.0013 in AU 0.0013 in	Wire	3.0 4.0	2.0 3.0
C or D	AL 0.0015 in AU 0.0015 in	Wire	4.0 5.0	2.5 4.0
C or D	AL 0.0030 in AU 0.0030 in	Wire	12.0 15.0	8.0 12.0
F	Any	Flip-chip	5 grams-force x number of bonds (bumps)	
G or H	Any	Beam lead	30 grams force in accordance with linear millimeter of nominal undeformed (before bonding) beam width. 3/	

1/ For wire diameters not specified, use the curve of figure 2011-1 to determine the bond pull limit.
2/ For ribbon wire, use the equivalent round wire diameter which gives the same cross-sectional area as the ribbon wire being tested.
3/ For condition G or H, the bond strength shall be determined by dividing the breaking force by the total of the nominal beam widths before bonding.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition letter (see 3).

b. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.

c. LTPD or number and selection of bond pulls to be tested on each device, and number of devices, if other than 4.

d. For test condition A, angle of bond peel if other than 90°, and bond strength limit (see 3.2).

e. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).

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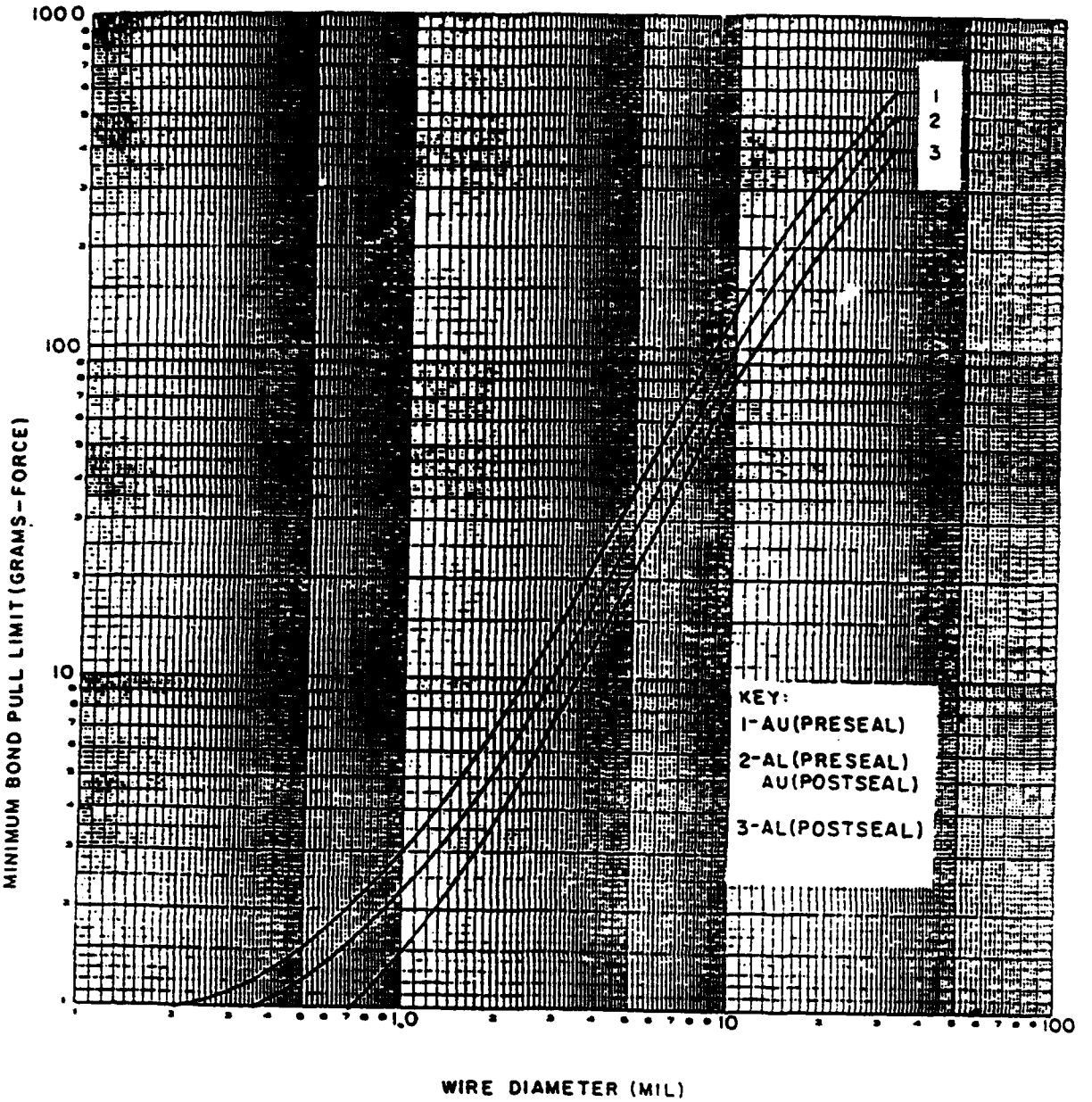


NOTE: The minimum bond strength should be taken from table I. Figure 2011-1 may be used for wire diameters not specified in table I.

FIGURE 2011-1. Minimum bond pull limits.

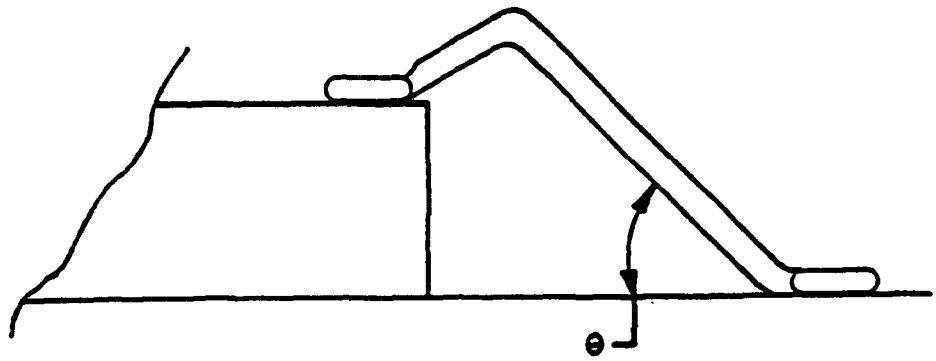


FIGURE 2011-2. Wire loop angle.

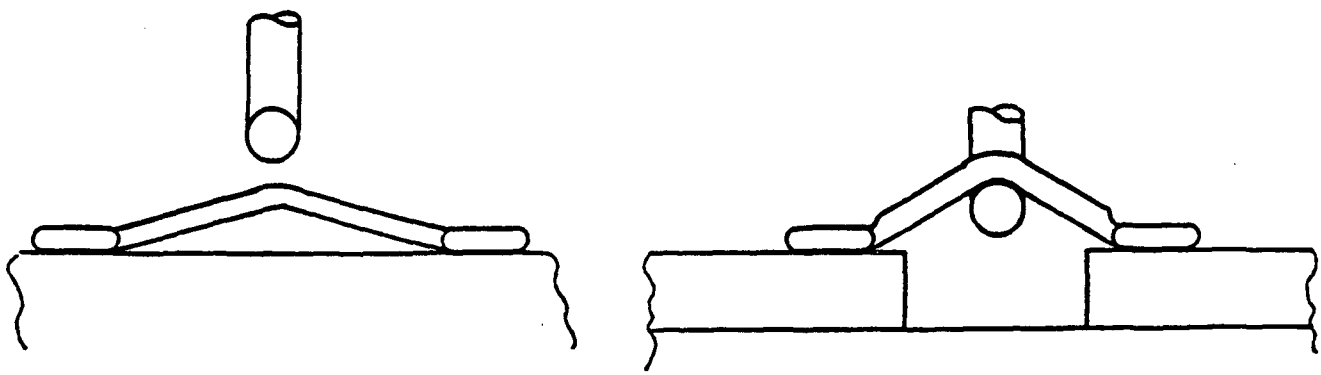


FIGURE 2011-3. Flat loop wire pull testing.

METHOD 2016

PHYSICAL DIMENSIONS

* 1. PURPOSE. The purpose of this examination is to verify that the external physical dimensions of the device are in accordance with the applicable acquisition document.

* 2. APPARATUS. Equipment used in this examination shall include micrometers, calipers, gauges, contour projectors, or other measuring equipment capable of determining the actual device dimensions specified in the applicable acquisition document.

3. PROCEDURE. Unless otherwise specified, the physical dimensions on the case outline drawing shall be measured.

3.1 Failure criteria. Any device which exhibits a dimension or dimensions outside the specified tolerances or limits shall constitute a failure.

* 4. SUMMARY. The following detail shall be specified in the applicable acquisition document:

External dimensions which are capable of physically describing the device (see 3). Dimensions to be considered shall include case outline dimensions; special lead shapes (e.g., required bend positions, angles of bend), where applicable; dimensions of any projecting or indented features used for coding of lead arrangement, automatic handling and similar purpose; and any other information which affects the installed size or orientation of the device in normal applications.

METHOD 2019.5

DIE SHEAR STRENGTH

1. PURPOSE. The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates. This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.

2. APPARATUS. The test equipment shall consist of a load-applying instrument with an accuracy of ±5 percent of full scale or 50 grams, whichever is the greater tolerance. A circular dynamometer with a lever arm or a linear motion force- applying instrument may be used to apply the force required for testing. The test equipment shall have the following capabilities:

a. A die contact tool which applies a uniform distribution of the force to an edge of the die (see figure 2019-1).

b. Provisions to assure that the die contact tool is perpendicular to the die mounting plane of the header or substrate.

c. A rotational capability, relative to the header/substrate holding fixture and the die contact tool, to facilitate line contact on the edge of the die; i.e., the tool applying the force to the die shall contact the die edge from end-to-end (see figure 2019-2).

d. A binocular microscope with magnification capabilities of 10X minimum and lighting which facilitates visual observation of the die and die contact tool interface during testing.

3. PROCEDURE. The test shall be conducted, as defined herein, or to the test conditions specified in the applicable specific acquisition document consistent with the particular part construction. All die strength tests shall be counted and the specific sampling, acceptance, and added sample provisions shall be observed, as applicable.

3.1 Shear strength. A force sufficient to shear the die from its mounting or equal to twice the minimum specified shear strength (figure 2019-4), whichever occurs first, shall be applied to the die using the apparatus of 2 above.

a. When a linear motion force-applying instrument is used, the direction of the applied force shall be parallel with the plane of the header or substrate and perpendicular to the die being tested.

b. When a circular dynamometer with a lever arm is employed to apply the force required for testing, it shall be pivoted about the lever arm axis and the motion shall be parallel with the plane of the header or substrate and perpendicular to the edge of the die being tested. The contact tooling attached to the lever arm shall be at a proper distance to assure an accurate value of applied force.

c. The die contact tool shall load against an edge of the die which most closely approximates a 90° angle with the base of the header or substrate to which it is bonded (see figure 2019-3).

d. After initial contact with the die edge and during the application of force, the relative position of the contact tool shall not move vertically such that contact is made with the header/substrate or die attach media. If the tool rides over the die, a new die may be substituted or the die may be repositioned, provided that the requirements of 3.1.c are met.

3.2 Failure criteria. A device which fails any of the following criteria shall constitute a failure.

a. Fails die strength requirements (1.0X) of figure 2019-4.

b. Separation with less than 1.25 times the minimum strength (1.0X) specified in figure 2019-4 and evidence of less than 50 percent adhesion of the die attach medium.

c. Separation with less than 2.0 times the minimum strength (1.0X) specified in figure 2019-4 and evidence of less than 10 percent of adhesion of the die attach medium.

* NOTE: For eutectic die attach, residual silicon attached in discrete areas of the die attach medium shall be considered as evidence of such adhesion. For metal glass die attach, die attach material on the die and on the package base shall be considered as evidence of acceptable adhesion.

3.2.1 Separation categories. When specified, the force required to achieve separation and the category of the separation shall be recorded.

a. Shearing of die with residual silicon remaining.

b. Separation of die from die attach medium.

c. Separation of die and die attach medium from package.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Minimum die attach strength if other than shown on figure 2019-4.

b. Number of devices to be tested and the acceptance criteria.

c. Requirement for data recording, when applicable (see 3.2.1).

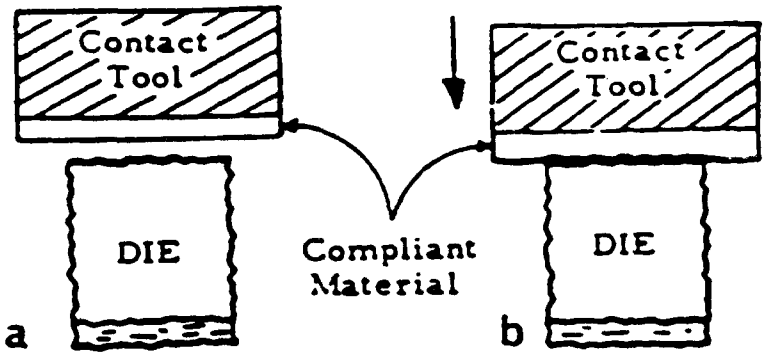


FIGURE 2019-1. Compliant interface on contact tool distributes load to the irregular edge of the die.

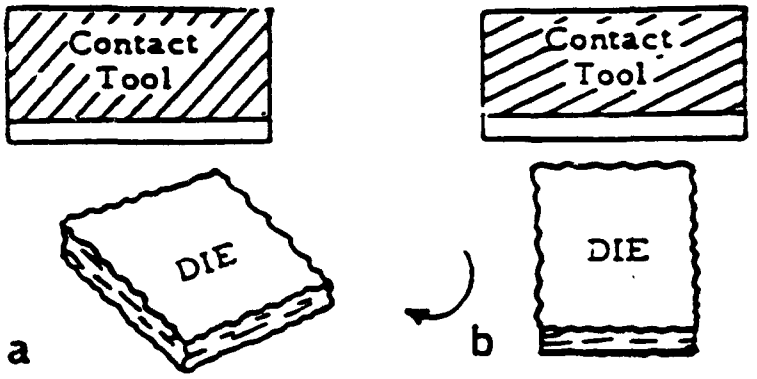


FIGURE 2019-2. Rotate the die contact tool or the device for parallel alignment.

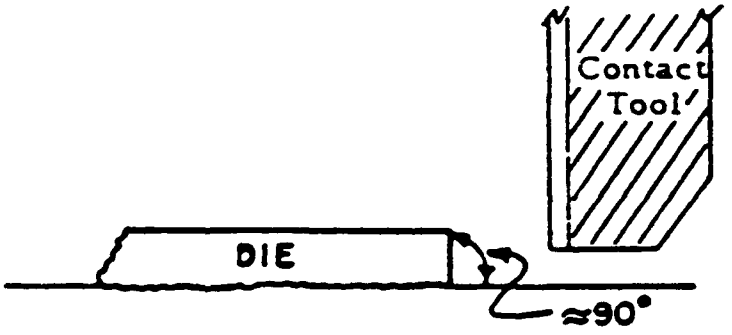
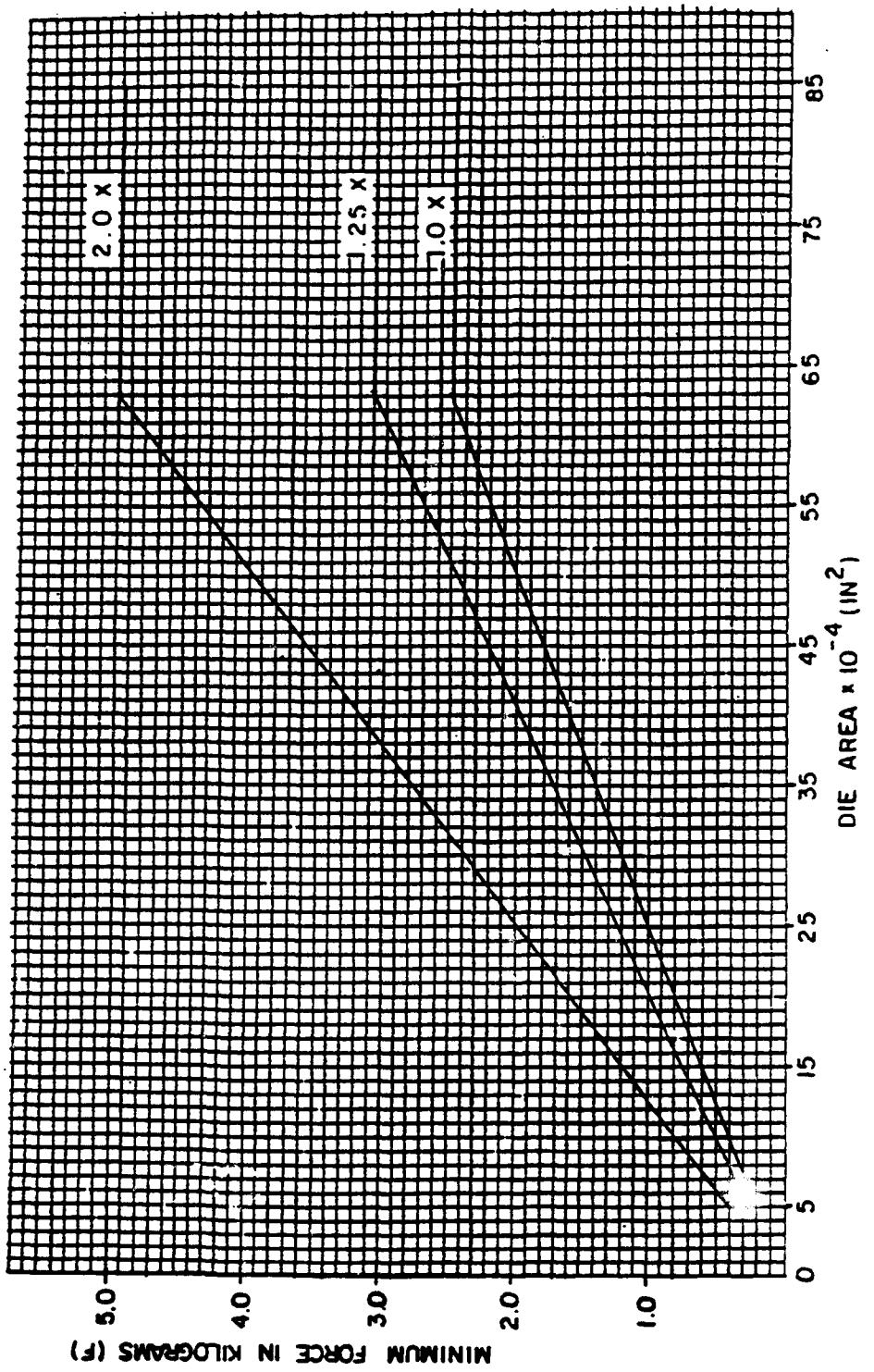


FIGURE 2019-3. The contact tool shall load against that edge of the die which forms an angle ≈ 90° with the header/substrate.



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NOTES:

1. All die area larger than 64 x 10^{-4} $(IN)^2$ shall withstand a minimum force of 2.5 kg or a multiple thereof (see 3.2).
2. All die area smaller than 5 x 10^{-4} $(IN)^2$ shall withstand a minimum force (1.0X) of 0.04 $kg/10^{-4}$ $(IN)^2$ or a minimum force (2X) of 0.08 $kg/10^{-4}$ $(IN)^2$.

FIGURE 2019-4. Die shear strength

METHOD 3004.1

TRANSITION TIME MEASUREMENTS

1. PURPOSE. This method establishes the means for measuring the output transition times of digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

1.1 Definitions. The following definitions shall apply for the purpose of this method.

1.1.1 Rise time (t_{TLH}). The transition time of the output from 10 percent to 90 percent or voltage levels of output voltage with the specified output changing from the defined LOW level to the defined HIGH level.

1.1.2 Fall time (t_{THL}). The transition time of the output from 90 percent to 10 percent or voltage levels of output voltage with the specified output changing from the defined HIGH level to the defined LOW level.

2 APPARATUS. Equipment capable of measuring the elapsed time between specified percentage points (normally 10 percent to 90 percent on the positive transition and 90 percent to 10 percent on the negative transition) or voltage levels. The test chamber shall be capable of maintaining the device under test at any specified temperature.

* 3. PROCEDURE. The device shall be stabilized at the specified test temperature.
The device under test shall be loaded as specified in the applicable acquisition document. The load shall meet the requirements specified in method 3002 of this document. The driving signal shall be applied as specified in method 3001 or the applicable acquisition document.

* 3.1 Measurement of t_{TLH} and t_{THL}. Unless otherwise stated, the rise transition time (t_{TLH}) shall be measured between the 10 percent and 90 percent points on the positive transition of the output pulse and the fall transition time (t_{THL}) shall be measured between the 90 percent and 10 percent points on the negative transition of the output pulse. The device under test shall be conditioned according to the applicable acquisition document with nominal bias voltages applied. Figure 3004-1 shows typical transition time measurement.

* 4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. t_{TLH} limits.

b. t_{THL} limits.

c. Transition time measurement points if other than 10 percent or 90 percent.

d. Parameters of the driving signal.

e. Conditioning voltages (static or dynamic).

f. Load condition.

g. Power supply voltages.

h. Test temperature.

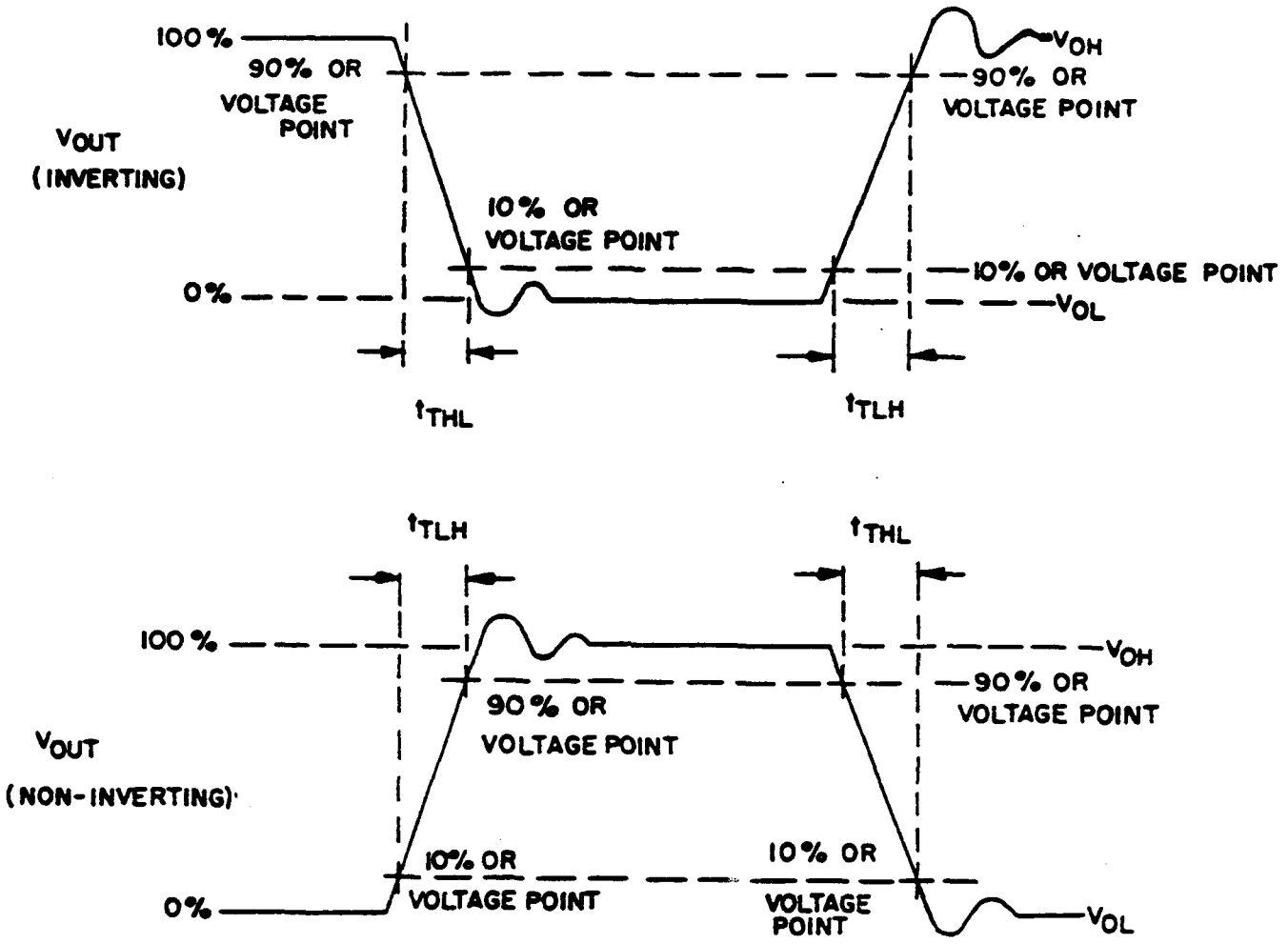

FIGURE 3004-1. Transition time measurements.

METHOD 3017

MICROELECTRONICS PACKAGE DIGITAL SIGNAL TRANSMISSION

1. PURPOSE. This method establishes the means of evaluating the characteristic impedance, capacitance, and delay time of signal lines in packages used for high frequency digital integrated circuits. It is intended to assure a match between circuit performance and interconnecting wiring to minimize signal degradation.

1.1 Definitions.

1.1.1 Characteristic impedance. The impedance that a section of transmission line exhibits due to its ratio of resistance and inductance to capacitance.

1.1.2 Delay time. The time delay experienced when a pulse generated by a driver with a particular drive impedance is propagated through a section of transmission line.

1.2 Symbols.

R: Resistance
L: Inductance
C: Capacitance
t_{pd}: Propagation delay time

2. APPARATUS. The approaches for transmission performance measurements shall include a suitable time domain reflectometer (TDR) (see 2.1) and dc resistance measuring equipment (see 2.2).

2.1 Time domain reflectometer. The TDR used for this test shall have a system rise time for the displayed reflection that is not less than 5 times and preferably 10 times the rise time (method 3004) for the candidate integrated circuits to be packaged. Interconnecting cables and fixtures shall be designed such that this ratio is not degraded due to reflections and ringing in the test setup.

2.2 DC resistance. DC resistance measuring equipment and probe fixtures shall be capable of measuring the resistance of the package leads and the chip-to- package interconnect media with an accuracy of no greater than ±10 percent of the actual value including errors due to the mechanical probing interface contact resistance.

3. PROCEDURE. The test equipment configuration shall be as shown on figure 3017-1 using a time domain reflectometer as specified (see 2). The characteristic impedance (Z_o), propagation time (t_{pd}), resistance and load capacitance (C_L) shall be measured for all representative configurations as determined by a review of the package drawings, and the intended applications (see 3.2 through 3.3).

3.1 General considerations.

3.1.1 TDR measurements. Accurate measurement of transmission performance of a package pin using a TDR requires careful design and implementation of adapter fixtures to avoid reflections due to transmission line discontinuities in the cables and junctions between the TDR and the package being tested. The accuracy of the measurement will be enhanced if the coaxial cable used to interface to the package is of a characteristic impedance as close as possible to the package pin impedance. The interface to the package should be a soldered connection and mechanical design of the actual coax-to-package interface should minimize the length of the uncontrolled impedance section. Stripline interfaces are the best method for surface mount package styles.

3.1.2 Test configurations. Obtaining a good high frequency ground is also important. Connection of the package ground plane (if the package design has one) to the test set-up ground plane should be accomplished with a pin configuration similar to actual usage in the intended package applications.

Pin selection for testing may vary according to package complexity. For packages with very symmetrical pin configurations only a few pins need be tested but configurations must include pins adjacent and nonadjacent to the ground pins. Packages with complex wiring and interconnection media should be tested 100 percent.

3.2 Test procedure for package transmission characteristics. Using a section of coaxial cable of known, calibrated characteristic impedance (Z_{Ref}) as a reference measure the minimum (Z_{min}) maximum (Z_{max}) and average (Z_o) values of reflection coefficient (ρ) for the section of line on the TDR display that has been carefully determined to be the package pin (locate using zero-length short circuits).

Calculate characteristic impedance (Z_o) for each of the cases from the formula:

$$Z_o = Z_{Ref} \times \frac{(1+\rho)}{(1-\rho)}$$

3.2.2 Delay time measurement. From the TDR display of 3.2.1 measure the time difference in picoseconds from the point identified as the start of the exterior package pin (t_1) to the chip interface point (t_2) ($\Delta t = t_1 - t_2$)

From the package design drawings, determine the physical length of the package run (L)

$$\text{Time delay } t_{pd} = \frac{\Delta t}{L}$$

3.2.3 Load capacitance calculation.

$$\text{Load capacitance } C_L = \frac{t_{pd}}{Z_o}$$

3.2.4 Load inductance calculation.

$$\text{Load inductance (series)} = \frac{(t_{pd})^2}{C_L}$$

3.3. Series resistance measurement.

Using the test setups of figure 3017-2, separately measure the dc resistance of the chip-to-package interface media (R_H) and the package lead (R_L).

4. SUMMARY. The following details, when applicable, shall be specified in the applicable acquisition document:

a. Z_{max}.

b. Z_{min}.

c. Z_o (max).

d. Z_o (min).

e. t_{pd} (max).

f. t_{pd} (min).

g. C_L (max).

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h. C_L (min).

i. L_L (max).

j. L_L (min).

k. R_H (max).

l. R_H (min).

m. R_L (max).

n. R_L (min).

o. Package pins to be tested.

p. Package ground configuration.

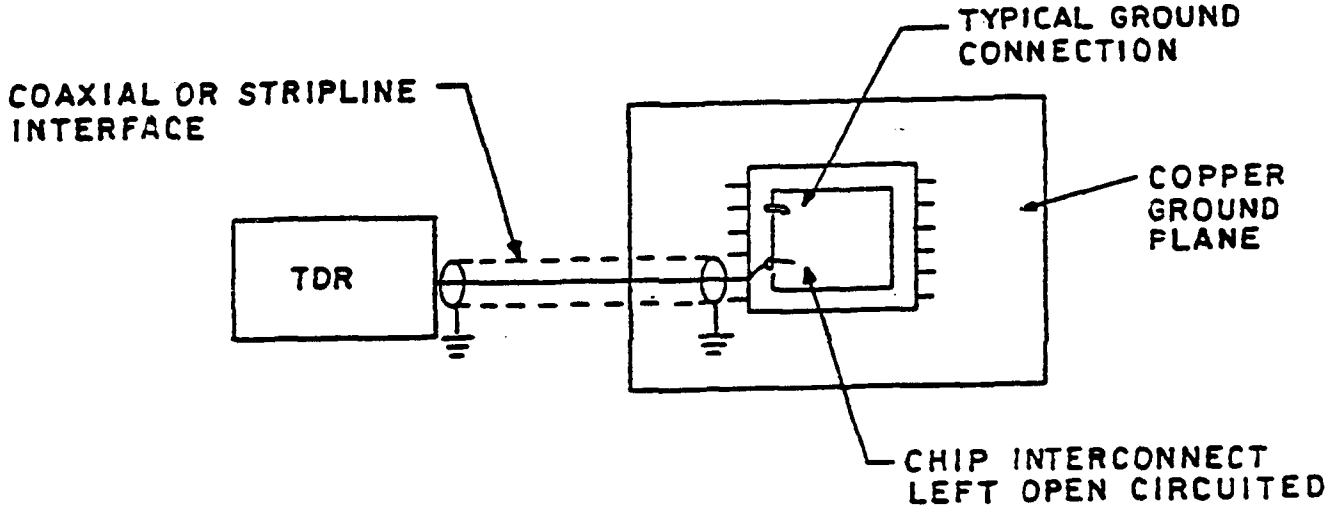


FIGURE 3017-1. Time domain reflectometer test setup.

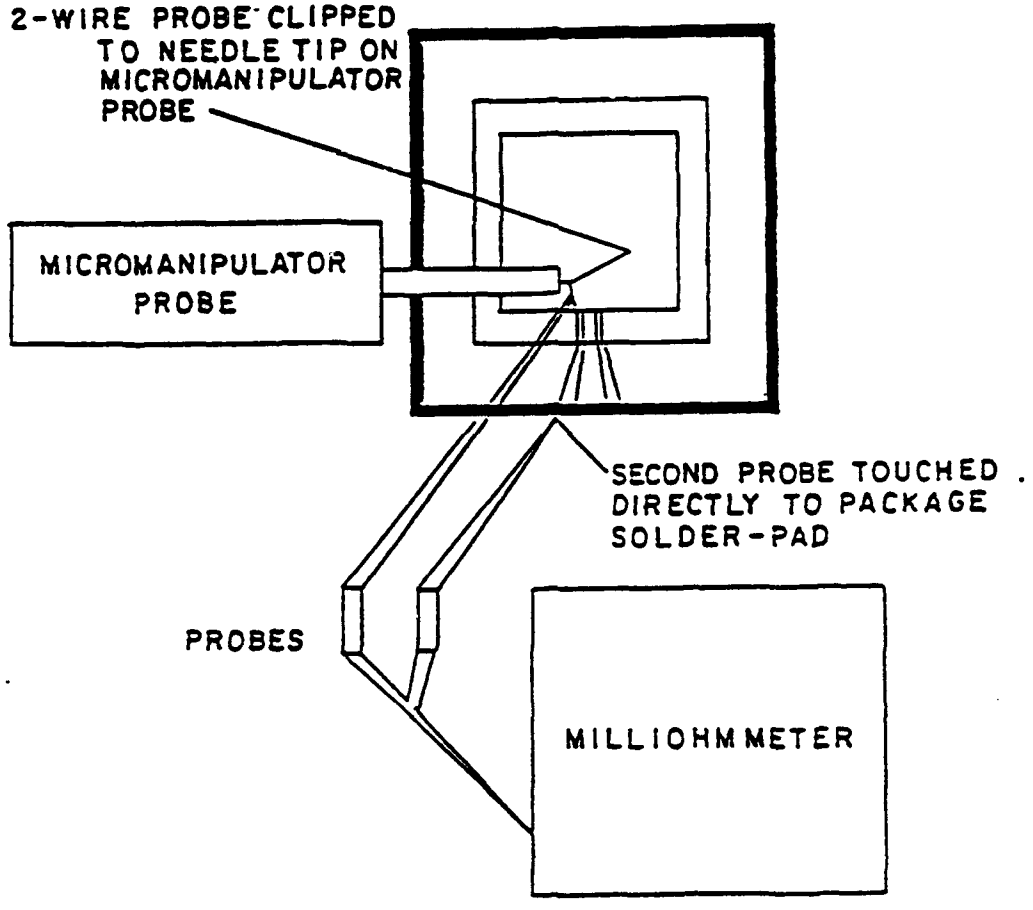


FIGURE 3017-2. Test setup for dc resistance using a milliohmmeter.

METHOD 3018

CROSSTALK MEASUREMENTS FOR DIGITAL MICROELECTRONICS DEVICE PACKAGE

1. PURPOSE. This method establishes the means of measuring the level of cross-coupling of wideband digital signals and noise between pins in a digital microcircuit package. The method may be used to gather data that are useful in the prediction of the package's contribution to the noise margin of a digital device. The technique is compatible with multiple logic families provided that the drive and load impedance are known.

1.1 Definitions.

1.1.1 Crosstalk. Signal and noise waveforms coupled between isolated transmission lines, in this case, package conductors.

1.1.2 Coupling capacitance. The effective capacitance coupling between a pair of conductors in a package as measured by the time constant of the charge pulse applied on one line and measured on the other.

1.1.3 Noise pulse voltage. The voltage of a crosstalk measured at the minimum noise pulse width as measured on a receiver input line.

1.1.4 Peak noise voltage. The peak value of the noise pulse measured on a receiver input line.

1.2 Symbols. The following symbols shall apply for the purpose of this test method and shall be used in accordance with the definitions provided (see 1.2.1 and 1.2.2).

1.2.1 Logic levels.

V_{OL}(max): The maximum output low level specified in a logic system.

V_{OH}(min): The minimum output high level specified in a logic system.

V_{IL}(max): The maximum allowed input low voltage level in a logic system.

V_{IH}(min): The minimum allowed input high level in a logic system.

1.2.2 Noise pulse width.

t_{PL}: The low level noise pulse width, measured at the V_{IL} (max) level (see method 3013).

t_{PH}: The high level noise pulse width, measured at the V_{IH} (min) level (see method 3012).

1.2.3 Transition times (see method 3004).

t_{TLH}: Rise time. The transition time of the output from the 10 percent to the 90 percent of the high voltage levels with the output changing from low to high.

t_{THL}: Fall time. The transition times from the 90 percent to the 10 percent of the high voltage level with the output changing from high to low.

1.2.4 Crosstalk parameters.

C_c: Coupling capacitance (see 1.1.2).

V_N: Noise pulse voltage (see 1.1.3).

V_{NPK}: Peak noise voltage (see 1.1.4).

2. APPARATUS. The apparatus used for crosstalk measurements shall include a suitable source generator (see 2.1), wideband oscilloscope (see 2.2), low capacitance probe (see 2.3) and load resistors (see 2.4).

2.1 Source generator. The source generator for this test shall be capable of duplicating (within 5 percent) the transition times, V_{OH} and V_{OL} levels of the logic system(s) being considered for application using the package style under evaluation. The source generator shall have a nominal characteristic source impedance of 50 ohms.

2.2 Wideband oscilloscope. The oscilloscope used to measure the crosstalk pulse shall have a display risetime that is less than 20 percent of the risetime of the logic systems being considered for application in the package style under evaluation. A sampling-type oscilloscope is recommended.

2.3 Low capacitance probe. The interface between the oscilloscope and the unit under test shall be a high impedance low capacitance probe. The probe impedance shall be 10 kΩ, minimum and the capacitance shall be 5 pf, maximum, unless otherwise specified in the acquisition document.

2.4 Load resistor. The load resistors specified for this test shall be low inductance, low capacitance, chip style resistors with a tolerance of ±5 percent. Load resistor values(s) shall be specified by the acquisition document to match the load impedance levels of the application logic family for a single receiver load.

* 3. PROCEDURE. The test equipment configuration shall be as shown on figure 3018-1 using a source generator, oscilloscope, probe and loads as specified (see 2). Measurements shall be made of coupling capacitance, (see 3.2) and if required by the acquisition document, of noise pulse voltage, peak noise pulse voltage, and noise pulse width (see 3.3).

3.1 General considerations.

3.1.1 Package test configuration. It is important to ground the package using the same pins as would be used in the microcircuit application. If the package has an internal ground plane or ground section, this should be connected via package pin(s) to the exterior test set-up ground plane. The package should be connected to the test set-up with coaxial cable or stripline. Unshielded conductor medium should not be used between the signal source and package. Coaxial shields must be grounded at both ends of the cable. Package sockets should not be used unless these are to be part of the microcircuit application configuration. Package leads must be formed and trimmed as specified in the application. Package-to-chip interconnecting media shall be installed in the package and used to connect to the load resistors.

* 3.1.2 Pin selection. For simple packages with symmetrical, parallel pin conductors, only a sample of pin combinations need be tested. Unless otherwise specified by the acquisition document, all combinations adjacent to the ground pin(s) and as combination opposite the ground pin(s) shall be tested, as a minimum. Complex packages with nonparallel conductors or multilayer wiring shall be tested for all adjacent-pair combinations, unless otherwise specified.

* 3.2 Coupling capacitance measurements. Connect the test equipment as shown on figure 3018-1. Use a 50 ohm chip resistor load in the driven pin channel, unless otherwise specified. For the pick-up channel, use the load resistor value(s) as specified by the acquisition document. (Load resistor values should be set such that the parallel combination of load resistance and probe impedance matches as closely as practical the specified load impedance of a single receiver in the logic system to be used in the microcircuit application.) Check the residual cross-coupling of the measuring set-up by touching the probe to the pick-up channel load before the pick-up pin is connected to the resistor. Measure and record the peak pulse voltage observed. This peak pulse reading must be less than 50 percent of the reading observed with the pin connected to the resistor for a reading to be valid. Adjust the test set-up cable orientation and configuration to minimize this residual cross-coupling.

Connect the pick-up pins to the load resistor and adjust the pulse width so that the time required to charge the coupling capacitance to 0 V can be observed. Measure the time at the 63 percent voltage point on the waveform (T) and calculate coupling capacitance (C_c) as follows:

$$Determine\ R_{Total} = \frac{R_{Probe} \times R_{Load}}{R_{Probe} + R_{Load}}$$

$$C_{Total} = \frac{T}{R_{Total}}$$

$$C_c = C_{Total} - C_{Probe}$$

Values of C_c can be used as a relative measure for comparison of potential crosstalk among several packages to a standard package. The coupling capacitance (C_c) can also be used to predict levels of crosstalk for various logic systems or circuit configurations by performing a pulse response analysis using a circuit simulator.

* 3.3 Noise pulse measurements. Using the same test setup as in 3.2, measure the crosstalk noise pulse voltage at the minimum noise pulse width specified for the logic system or as specified by the acquiring agency.

Measure the peak noise voltage value of the coupled crosstalk.

4. SUMMARY. The following details, when applicable, shall be specified in the acquisition document:

a. C_c.

b. V_{OL} (max).

c. V_{OH} (min).

d. V_{IL} (max).

e. V_{IH} (min).

f. t_{PL}.

g. t_{PH}.

h. t_{tLH}.

i. t_{tHL}.

j. V_N.

k. V_{NPK}.

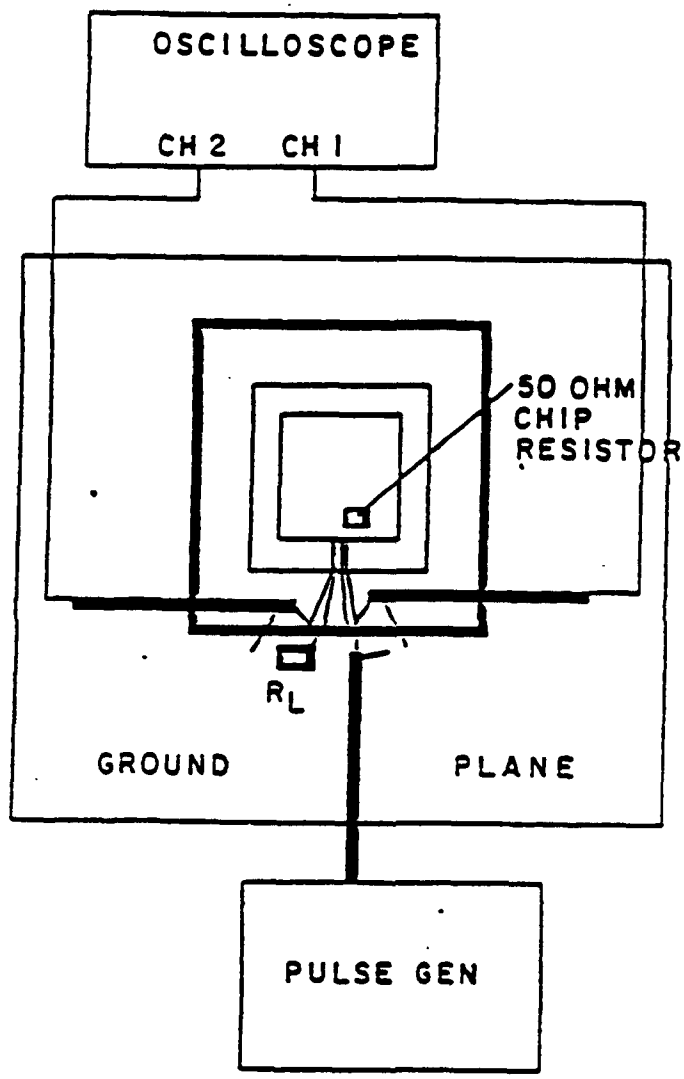


FIGURE 3018-1. Test setup for coupling capacitance measurement.

METHOD 4004.1

OPEN LOOP PERFORMANCE

1. PURPOSE. The purpose of this test procedure is to measure gain, bandwidth, distortion, dynamic range, and input impedance. Gain, dynamic range, and distortion are combined into a large signal test where the distortion measurement will indicate either lack of dynamic range or inherent distortion.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Maximum output voltage swing (V_{OP}). The maximum output voltage swing is the maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent dc output voltage is set at a specified reference level. The swing levels are denoted by $+V_{OP}$ and $-V_{OP}$.

1.1.2 Single ended input impedance (Z_{IN}). The single ended input impedance is the ratio of the change in input voltage to the change in input current seen between either input and ground with the other input terminal ac grounded. In case of single input amplifiers, it is the impedance between that terminal and ground. It is measured at the quiescent output dc level.

1.1.3 Differential input impedance (Z_{DI}). The differential input impedance is the ratio of the change in input voltage to the change in input current seen between the two ungrounded input terminals of the amplifier at the quiescent output dc level.

1.1.4 Voltage gain (A_{VS}). The voltage gain (open loop) is the ratio of the output voltage swing to the single ended or differential input voltage, required to drive the output to either swing limit.

1.1.5 Bandwidth, open loop (BW_{OL}). The open loop bandwidth is the range of frequencies within which the open-loop voltage gain of the amplifier is not more than 3 dB below the value of the midband open loop gain.

1.1.6 Distortion. The total ratio of the RMS sum of all harmonics to the total RMS voltage at the output for a pure sine wave input.

1.1.7 Unity gain bandwidth (GBW): The unity gain bandwidth is the frequency at which the output voltage is equal to the input voltage.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. A differential input is shown, but if a single ended inverting amplifier is under test, the components shown at the positive input terminal shall not be used. If a noninverting amplifier is under test, it shall be necessary to either use fixed bias instead of the dc feedback or to use an inverting gain of one amplifier in the feedback path. For differential output devices, the measurements described in 3.1, 3.2, 3.3, and 3.4 below, as applicable, shall be repeated for the other output using the same test figure except that the measuring equipment shall be connected to the other output.

3.1 Open loop gain using the null loop. The test figure is shown on figure 4004-3. The load resistor R_L is grounded. Set V_C to -10 V and measure E_{O1}. Set V_C to +10 V and measure E_{O2}.

$$A_{VS} = \frac{R_2}{R_1} \quad \frac{20}{E_{O2} - E_{O1}}$$

3.2 Distortion. Under the conditions of 3.1, read the distortion on the distortion meter or the voltage at the output of the rejection filter if that is used.

3.3 Maximum output voltage swing. The test figure is shown on figure 4004-3. Set V_C equal to zero. Switches S_1 - S_4 are closed. For $+V_{OP}$ apply a V_1 equal to the positive supply voltage $+V_{OP} = V_2$. For $-V_{OP}$ apply a V_1 equal to the negative supply voltage $-V_{OP} = V_2$.

3.4 Bandwidth. Establish the amplitude of V_2 within the linear region of the device under test at a frequency specified for the measurement of A_D. Increase the frequency, while maintaining the amplifier of V_1 constant, until V_2 reduces to 0.707 of the original value (3 dB down). This frequency shall be measured as the bandwidth for the device under test. The test figure is shown on figure 4004-1.

3.5 Input impedance. This will be specified as a minimum value and shall be measured by observing that the output voltage V_2 does not drop more than 6 dB (2:1 in voltage) when the switch S is opened. This test shall be performed at the specified frequency with a specific amplitude of V_2 within the linear region. R_2 shall be given as the value of the minimum input impedance. The test figure is shown on figure 4004-1.

3.6 Unity gain bandwidth. Increase the frequency of e_I (starting at 100 kHz) until $e_O = e_I$. The frequency at which this occurs is GBW. The test figure is shown on figure 4004-4. Set the input voltage V_1 to the required device voltage.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, C, $\pm V_{CC}$ for the nulling amplifier, R_3 and R_L.

a. V_{OP}, at specified temperature(s).

b. Z_{IN} (minimum), at specified temperature(s) and frequency.

c. Z_{DI}, where applicable, at specified temperature(s) and frequency.

d. A_{VS}, where applicable, at specified temperature(s) and frequency.

e. A_V, at specified temperature(s) and frequency.

f. BW_{OI}, at specified temperature(s).

g. Distortion (X), at specified temperature(s).

h. V_{OI}, when applicable, at specified temperature(s).

i. GBW, at specified temperatures.

j. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

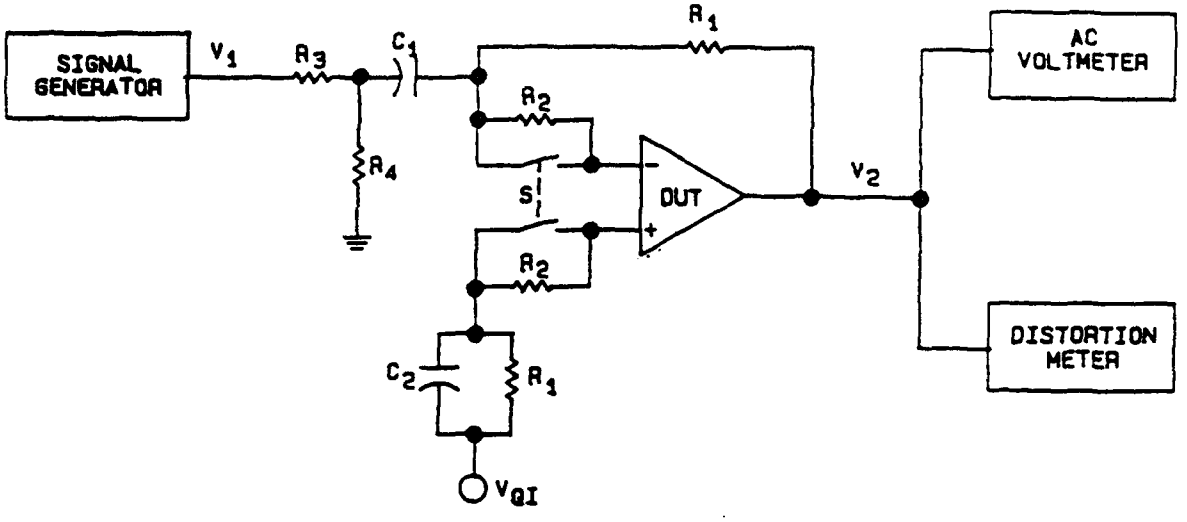


FIGURE 4004-1. Test figure for bandwidth and input impedance.

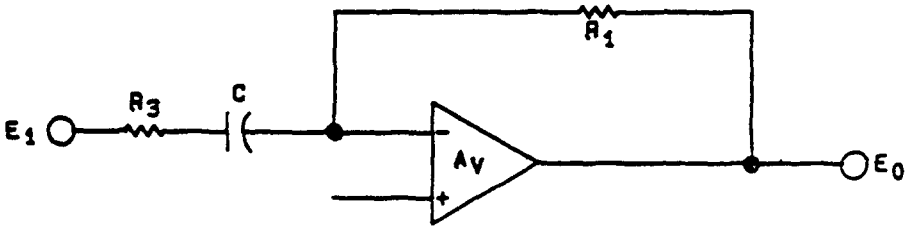


FIGURE 4004-2. Transfer function circuit.

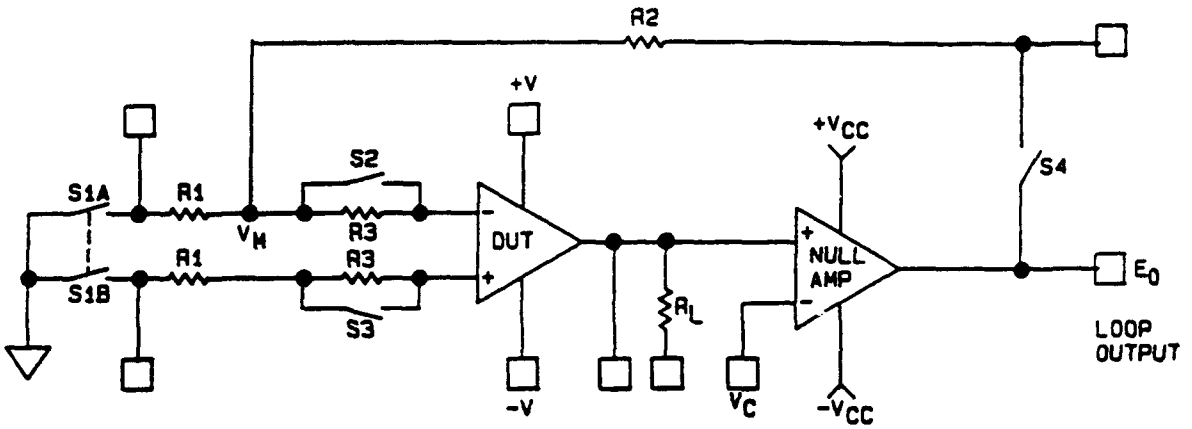


FIGURE 4004-3. Test setup for open loop gain, distortion and maximum output voltage swing.

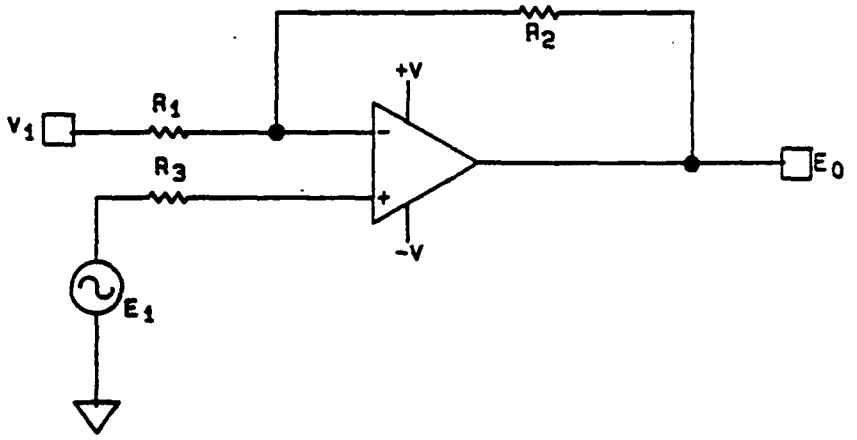


FIGURE 4004-4. Test setup for unity gain bandwidth.

SEMI G42-88

SPECIFICATION
THERMAL TEST BOARD STANDARDIZATION FOR MEASURING JUNCTION-TO-AMBIENT THERMAL RESISTANCE OF SEMICONDUCTOR PACKAGES

1. Preface

This document provides the requirements for a standard thermal resistance test board to be used in junction-to-ambient thermal resistance measurement of a semiconductor package under still and forced air condition as a referee method.

2. Applicable Documents

Information regarding the methods for measuring junction-to-ambient thermal resistance, the proper design and use of thermal test chips, and material specifications for printed circuit boards can be found in the applicable documents listed below.

2.1 *SEMI Specifications*

SEMI G32	Guideline, Unencapsulated Thermal Test Chip
SEMI G38	Still- and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of IC Packages

2.2 *Military Specifications*[1]

MIL-P-13949	Material Specification for NEMA Grade G-10 Printed Circuit Board Material
MIL-STD-883C	Method 1012.1, Thermal Characteristics

3. Selected Definitions

junction temperature, T_J - in degrees Celsius. Is used to denote the temperature of the semiconductor junction in the microcircuit in which the major part of the heat is generated. Usually the measured junction temperature is only indicative of the temperature in the immediate vicinity of the element used to sense the temperature.

junction-to-ambient thermal resistance, $R_{\theta JA}$ - in degrees Celsius/watt is the temperature difference between the junction and the ambient, divided by the power dissipation P_H.

power dissipation, P_H - in watts. Is the heating power applied to the device causing a junction-to-reference point temperature difference.

temperature sensitive parameter, TSP - Is the temperature dependent electrical characteristic of the junction under test which can be calibrated with respect to temperature and subsequently used to detect the junction temperature of interest.

4. Ordering Information

The material required for making the thermal test board can be ordered through any electronic supply store.

5. Requirements

General requirements regarding the materials used for test board, the specified physical dimensions of the test board and other necessary conditions are described in the following paragraphs:

5.1 *Material Requirements*

5.1.1 The test board material should be NEMA Grade G-10 or equivalent.

5.1.2 The conductor traces on the board must be copper and the total amount of copper should not exceed 20% of the surface area of the board.

5.1.3 The vias should be plated through.

5.1.4 External wire connections from the package leads to edge connector leads must be made with 24 gauge copper wire.

5.2 *Thermal Test Board Layout and Physical Dimensions* - Two separate boards are designed for the purpose of thermal measurements of different types of semiconductor packages.

5.2.1 Board One (shown in Figure 1), is for Dual-In-Line Packages or sockets

a. Dimensions:
Length: 4.50 inches $\pm$ 0.01
Width: 3.00 inches $\pm$ 0.01
Thickness: 0.060 - 0.065 inches $\pm$ 0.005

b. The vias shall be located on 0.10 inch centers $\pm$ 0.003 non-accumulative.

1 Military Standards, Naval Publications and Form Center, 5801 Tabor Avenue, Philadelphia, PA 19120

c. The diameter of the vias shall be 0.045 inches ± 0.003.

d. The location of the vias on the board shall be as shown in Figure 1.

5.2.2 Board Two (shown in Figure 2) is designed for chip carrier packages.

a. Dimensions:
Length: 4.50 inches ± 0.01
Width: 3.00 inches ± 0.01
Thickness: 0.060 - 0.065 inches ± 0.005

b. The copper traces shall be laid out on the PC board as shown in Figure 2. The traces are drawn on 0.050 inch centers ± 0.005 non-accumulative.

c. The vias at the end of the copper traces shall be located on the 0.10 inch centers ± 0.003 inch non-accumulative.

5.2.3 Equivalent boards for other packages should follow similar guidelines as described in 5.2.1 and 5.2.2.

5.3 *Mounting Guidelines* - Board One is designed to accommodate Dual-in-Line Packages and socket-mounted Chip Carriers, whereas Board Two is designed for surface mounting Chip Carriers and Flat Packs.

5.3.1 Example of package mounting on the boards is shown in Figure 3. Packages should be mounted such that the center line of the test board is coincidental with the center line of the package.

5.3.2 The longer edge of the package should be closest to the long edge of the board.

5.3.3 Packages must be mounted such that the standoff height above the board is as per JEDEC guidelines. In the case of a new package without such information available, a minimum of 5 mil air gap between the bottom surface of the package and the thermal test board is acceptable.

5.4 *Mounting the Test Board for Still-Air $R_{\theta JA}$ Measurement*

5.4.1 The test board should be mounted on a clamp as shown in Figure 4 through a suitable edge connector clamp.

5.4.2 The test board and the edge connector clamp are placed in a one cubic foot enclosure as shown in Figure 4. The edge connector clamp height must be adjusted to ensure positioning of the package in the center of the chamber.

5.4.3 The electrical wire connections from the package are routed out of the one cubic foot enclosure either through an edge connector or through small diameter holes in the box.

5.5 *Mounting the Test Board for Forced-Air $R_{\theta JA}$ Measurement* - Forced air $R_{\theta JA}$ measurements are performed in a wind tunnel whose diameter is 8.00 inches. Details of the wind tunnel are given in SEMI G38.

5.5.1 The test board should be mounted inside the wind tunnel on an edge connector clamp as shown in Figure 5.

5.5.2 The test board is placed in the wind tunnel such that the longer edge of the package is in a vertical position. (See Figure 5.)

5.5.3 The longer edge of the package should face the direction of air flow.

5.5.4 The longer side of the package must meet the air front first, as shown in Figure 5.

5.5.5 Air may be forced through the wind tunnel by either blowing from one end or by suction. (Suction being preferred.)

5.5.6 The test board and the edge connector clamp are placed in the wind tunnel as shown in Figure 5. The edge connector clamp height must be adjusted to ensure positioning of the package in the center of the wind tunnel.

5.6 *Thermal Resistance Measurement Methods* - Methods for measuring $R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) of IC packages using thermal test chips have been described in SEMI G32 and SEMI G38, respectively. These methods or equivalent methods such as the use of switching techniques, as described in MIL-STD-883C, Method 1021.1, should be used for making thermal resistance measurements of IC packages using thermal test chips or IC devices.

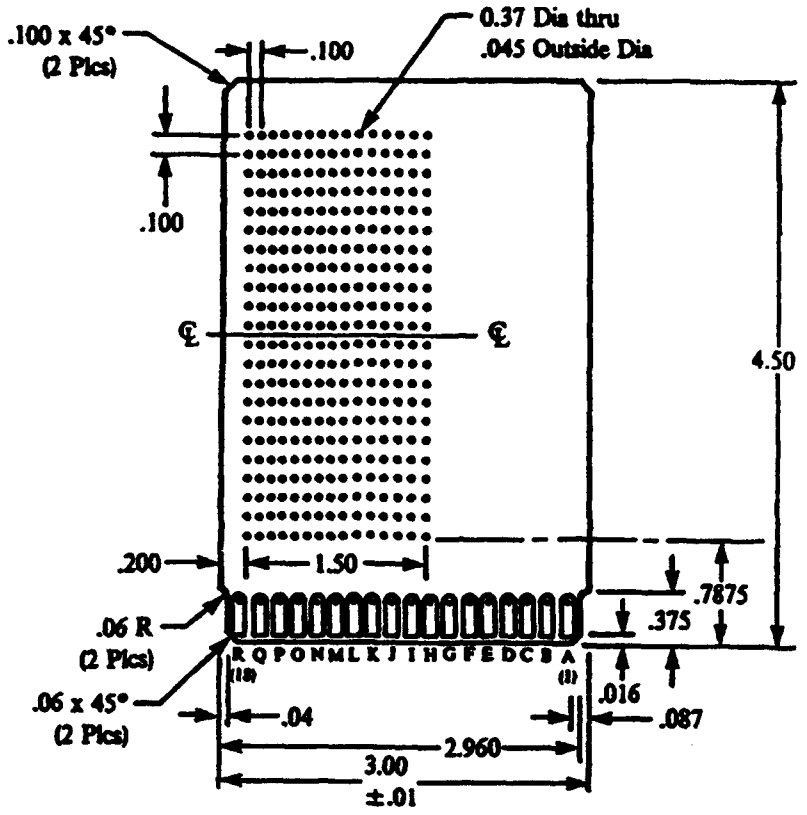
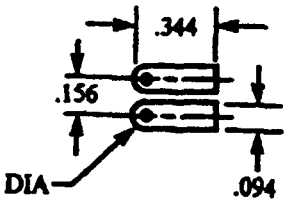


Figure 1
Thermal Test Board Dual In-Line Packages

Notes:

1. Material: Epoxy Glass, .062 Thk, FR-4 (Green), Copper Clad, 1 Oz. 1/1.
2. Gold-Plated Fingers, .00003 Min Thk, 18 on Each Side.
3. Fabricate Per IPC-D-320, Class III.
4. Tolerance: ±.003 (Unless Noted)
5. Fingers on Component Side of board (Shown) are Designated A Thru R.
6. All Holes Plated Thru.
7. Mates With Dale Connector, Part Number EB 7D-A18GFX Or Equivalent.

Singers on the Solder Side Are Designated as 1 Thru 18
(With 18 at Right When Viewing Face of Board).



FINGER DETAIL

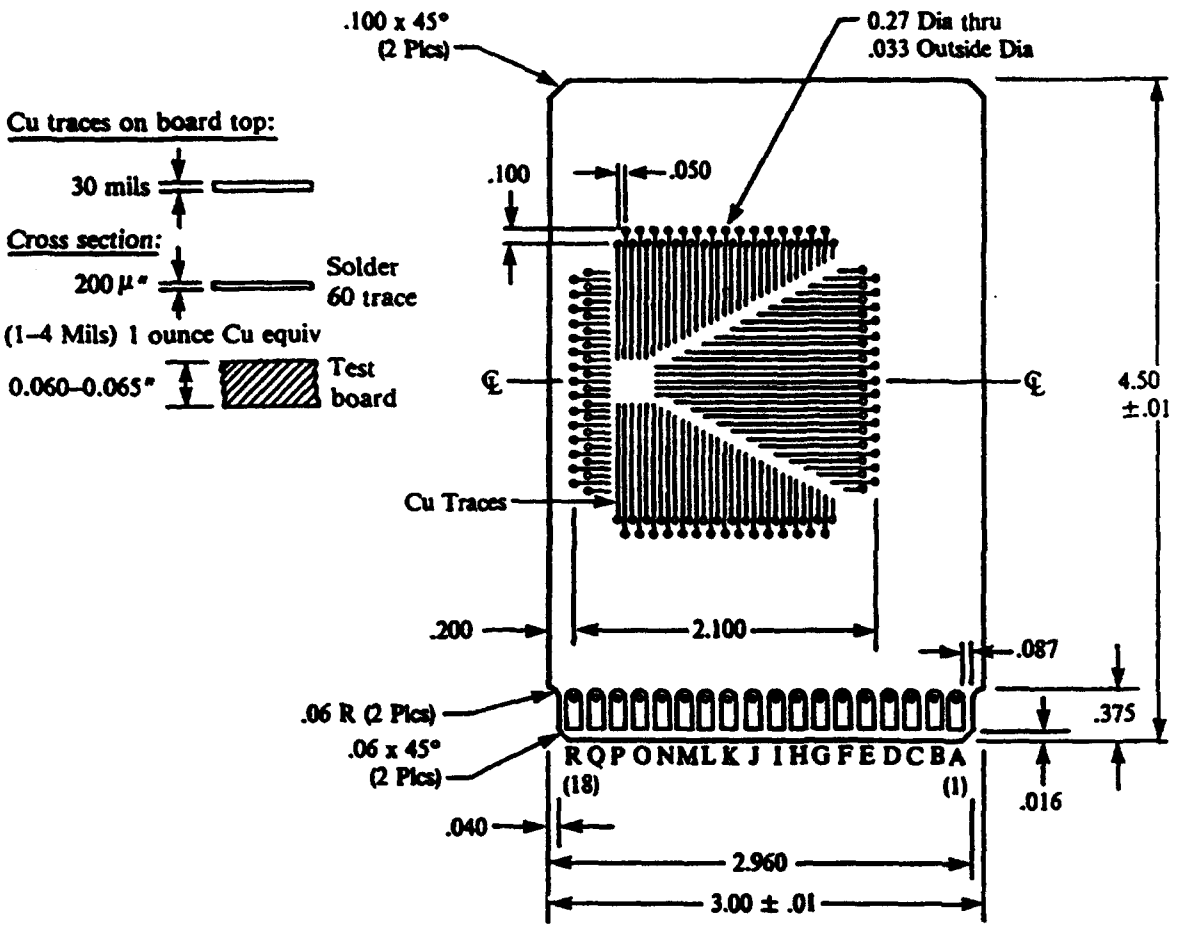
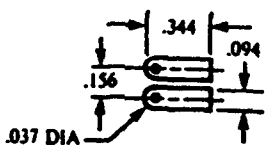


Figure 2
Thermal Test Board Surface Mounting PCC Packages

Notes:

1. Material: Epoxy Glass, .062 Thk. FR-4 (Green), Copper Clad, 1 Oz. 1/1.
2. Gold-Plated Fingers, .00003 Min Thk. 18 on Each Side.
3. Fabricate Per IPC-D-320, Class III.
4. Tolerance: ±.003 (Unless Noted)
5. Fingers on Component Side of Board (Shown) are Designated as A Thru R.

   Fingers on the Solder Side are Designated as 1 Thru 18 (With 18 at Right When Viewing Face of Board).



FINGER DETAIL

6. All Holes Plated Thru.
7. Mates With Dale Connector, Part Number EB 7D-A18GFX or Equivalent.

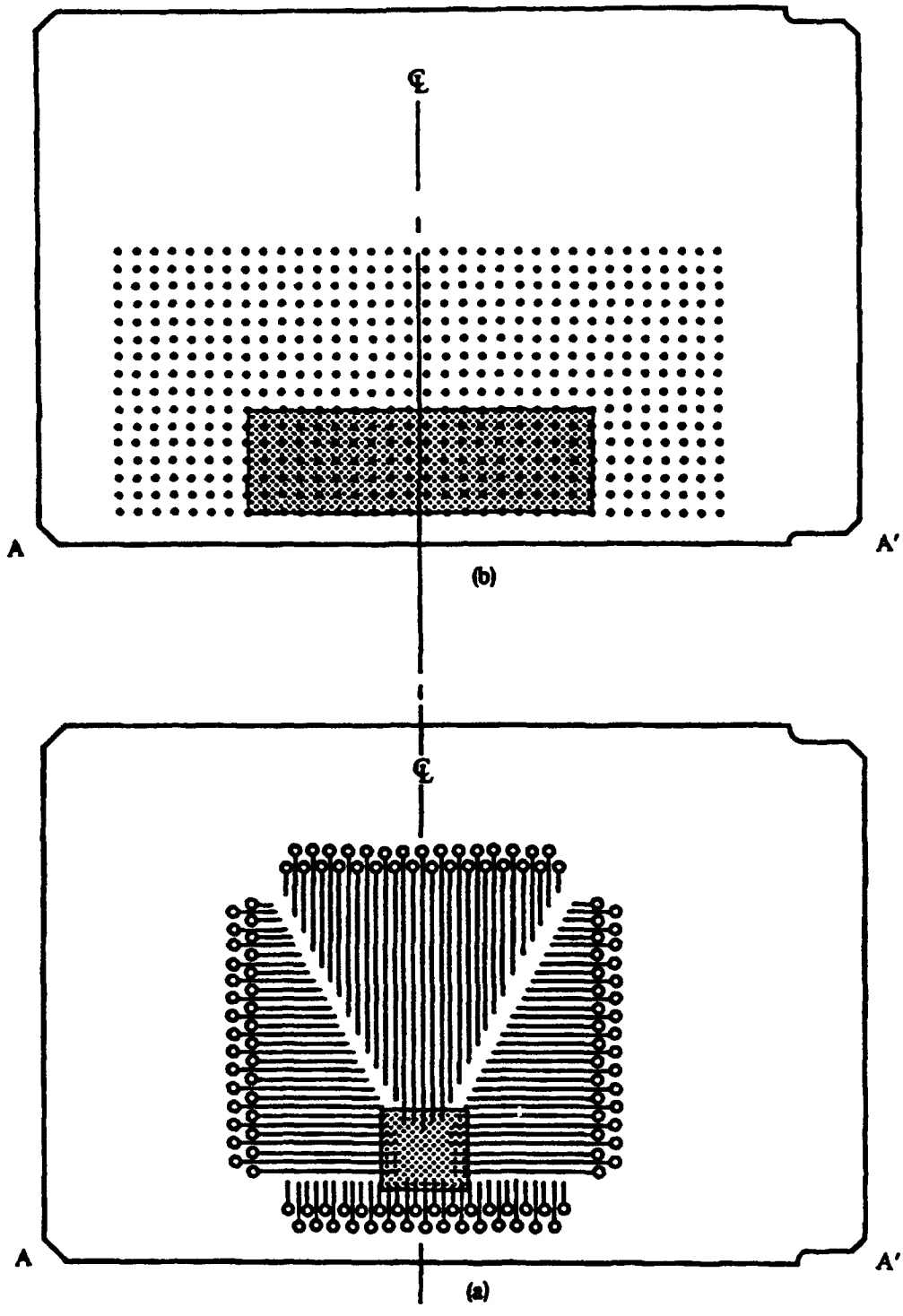


Figure 3
Location of Package While Mounting on Test Boards

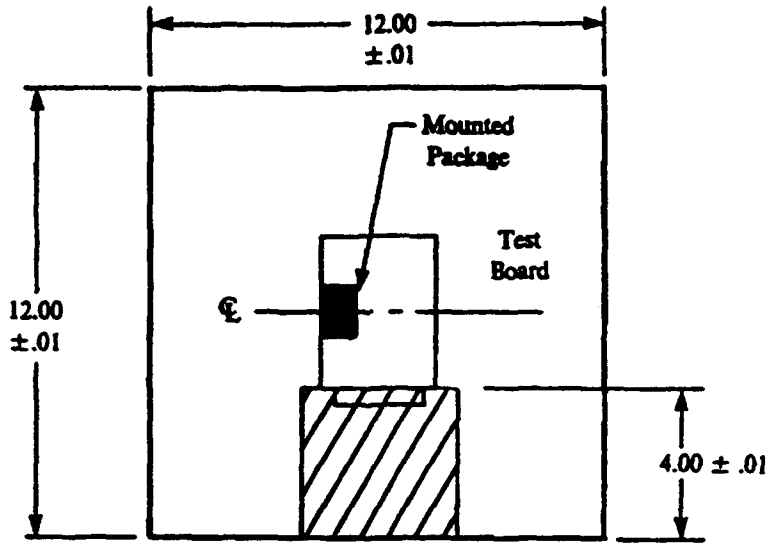


Figure 4
Test Board Positioning Inside Measuring Chamber

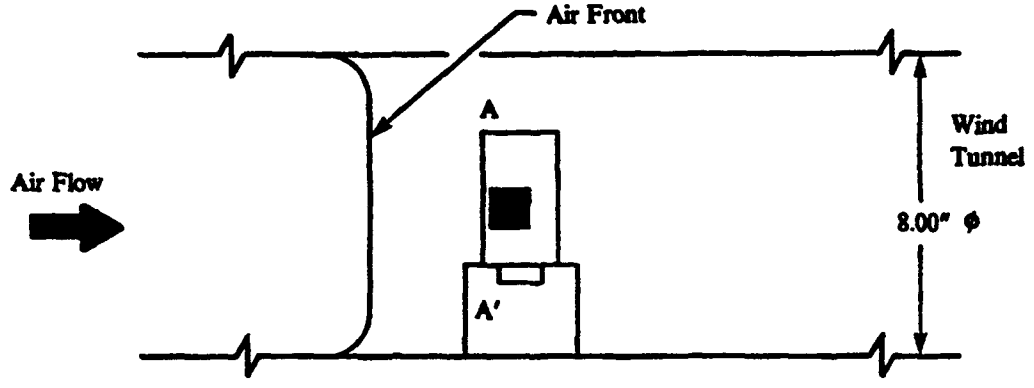


Figure 5
Test Board Orientation Inside Wind Tunnel

Appendix E: Endnotes

[1] Minimally packaged die have had some post processing done, e.g., bumped

[2] Working Document, JEDEC Modified Version 2.0, 18 May 1993, As submitted for Ballot.

[3] The bottom surface of the die is the plane of reference for planarity measurements.

[4] Refer to Mil-Std-883, Method 2010, level B for allowable pad damage

[5] Built In Self Test

[6] The resistance of an electrical connection from the carrier to the die, measured at the point of contact.

[7] Refer to Mil-Std-883, Method 2010, level B for allowable pad damage

[8] The resistance of an electrical connection from the carrier to the die, measured at the point of contact.

[9] Refer to Mil-Std-883, Method 2010, level B for allowable pad damage

[10] Working Document, JEDEC Modified Version 2.0, 18 May 1993, As submitted for Ballot.

[11] The estimated selling price/quantity of carriers, if applicable.

[12] How many times can the carrier be reused and still remain within its specifications. Further information on carrier maintenance cost and schedule to be furnished if applicable.

[13] Coefficient of Thermal Expansion of probe substrate material.

[14] Metal in contact with die pad/bump

[15] Built In Self Test

Section IV - Specifications

STANDARD FOR KNOWN GOOD DIE (KGD)

EIA Designation: _____

Preface

This standard was created to facilitate the procurement and use of high reliability semiconductor microcircuits or discrete devices provided in bare die form, commonly known as "Known-Good Die" (KGD).

This document provides requirements and guidance to KGD suppliers in regard to the high levels of as-delivered performance, quality and long term reliability expected of this type. It also reflects the special needs of KGD product customers in terms of design and application data. This document is applicable to KGD products used in both commercial and military applications.

This standard also reflects an understanding on the part of KGD users that quality and reliability cannot always be assured in the same fashion as for conventionally packaged microcircuits. KGD customers take on a significant responsibility for the proper application and long term environmental protection of this type of product. The extent to which KGD suppliers shall warrant die product is highly dependent upon customer capability and adherence to strict quality controls. Cooperation between suppliers and users is essential.

1. Scope

1.1 This standard provides guidelines and requirements for known-good semiconductor die (KGD) used in other than conventionally packaged microcircuit or discrete formats. The die described herein are intended to be high quality, reliable bare dice in die form only, for use in a variety of user-defined applications (e.g., multichip modules, hybrid circuits, memory cards, etc.) While this standard allows negotiation between supplier and user to establish specific requirements for performance, quality and reliability, it is important to recognize, in the case of military and aerospace applications, the minimum requirements described in relevant military specifications.

1.2 This standard is limited to KGD consisting of a single microcircuit or discrete device connected using conventional wire bonding or High Density Interconnect. KGD are intended to be equivalent to or better than their corresponding packaged parts in terms of electrical and reliability performance (unless specifically noted by the supplier). Per requirements mutually agreed upon by KGD supplier and user, the KGD supplier shall implement and demonstrate testing and screening required to assure this performance. This standard deals only with KGD supplied in individual die form, for which the user accepts responsibility for providing and assuring final environmental protection (e.g., hermetic sealing).

2. Reference Documents

2.1 Military and Federal Standards[1]

FED-STD-209	Clean Room and Workstation Requirements, Controlled Environments
MIL-STD-883	Microelectronics, Test Methods and Procedures
MIL-S-19500	General Specification for Semiconductor Devices
MIL-M-38510	General Specification for Microcircuits
MIL-H-38534	General Specification for Hybrid Microcircuits
MIL-I-38535	General Specification for Integrated Circuits Manufacturing

2.2 Institute of Electrical and Electronic Engineers Standards[2]

IEEE 1029.1	Waveform and Vector Exchange Specification
IEEE 1076-1987	VHSIC Hardware Description Language
IEEE/ANSI 1149.1-1990	Standard Test Access Port and Boundary-Scan Architecture

2.3 Electronics Industry Association - Joint Electron Device Engineering Council Standards[3]
JC 19C General Standard for Statistical Process Controls

2.4 American National Standards Institute Documents[4]
ANSI Y14.5 Dimensional Standards

2.5 International Standards[4]
ISO 9000 Series Quality Management Standard

2.6 Other Reference Documents
Relevant KGD Supplier Data Book/Sheet or Specification

2.7 Order of Precedence (microcircuits): In the case of conflict between/among applicable specifications, the following order of precedence shall apply for microcircuits:
2.7.1 Purchase order of other contractual documents
2.7.2 Detailed Specifications
2.7.3 Other mutually agreed documents
2.7.4 This Standard

2.8 Order of Precedence (discrete devices): In the case of conflict between/among applicable specifications, the following order of precedence shall apply for discrete devices:
2.8.1 JANC die manufactured and tested per MIL-S-19550, Appendix H
2.8.2 Die manufactured and tested by best commercial practices
2.8.3 die manufactured and tested per MIL-STD-883, Test Method 5008
2.8.4 This Standard

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[1] Available from: Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120.

[2] Available from: Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331.

[3] Available from: Electronics Industry Assn, 2001 Eye Street NW, Washington, D.C. 20006.

[4] Available from: American National Standards Institute, 1430 Broadway, New York, NY 10018.

3. Requirements

3.1 Overview: In addition to the information provided for the equivalent standard packaged die, KGD suppliers shall provide data as required in sections 3.2 to 3.9. For military and aerospace applications, requirements per the appropriate military specifications and requirements per section 3 shall be adhered to.

3.2 General Data: The following general data shall be provided for each KGD product type.

3.2.1 Part Numbering: Each KGD supplier shall establish a specific part numbering system which differentiates its KGD products from each other and from conventionally packaged equivalents.

3.2.2 Sample Die: Four types of sample die may be required by KGD users. Availability of these sample types and the quantities to be provided shall be negotiated as part of appropriate contractual agreements. These types include:

3.2.2.1 Conventionally packaged equivalents for system prototyping.

3.2.2.2 Mechanical samples of identical physical layout, orientation and pad metallurgy to the final KGD and clearly identified as "reject".

3.2.2.3 Prototype (proof of design) samples that are electrically functional and from a product representative of the KGD to be sold to a particular customer.

3.2.2.4 Acceptance samples which are representative of the updated version of a KGD type which is about to be released with design or manufacturing changes. These samples are intended to afford existing customers of this KGD type an opportunity to evaluate the impact of these changes upon their specific application.

3.3 Design Data: Design data specifically required for the application of KGD shall be provided. Mechanical data shall be provided in a format mutually agreed upon by KGD Supplier and user. The data to be provided are:

3.3.1 Individual KGD dimensions (x,y, thickness, pad shape, pad-to-pad centerline/location) with tolerances and units of measure referenced to die center line or other feature. (ANSI Std Y14.5 is the preferred format.)

3.3.2 Minimum die horizontal geometries (feature sizes).

3.3.3 Bond pad map (including available bonding area/passivation opening size), pin-out list, including electrical potential and pin number one identification with appropriate test designator.

3.3.4 Identification of any connections which must be jumpered or skipped (e.g., test pads).

3.3.5 Type and thickness of backside surface material and surface finish (e.g., polished or lapped).

3.3.6 Maximum and minimum allowable die junction operating temperature.

3.3.7 Known physical process limitations (e.g., temperature sensitivity, pressure sensitivity, uv light sensitivity, etc.).

3.3.8 Other conditions that affect die function, such as critical thermal environments, or additional materials (e.g., die attach materials) or components normally connected to or used within the packaged part (e.g., trimming capacitors).

3.3.9 Final die passivation (top protective layer) material and minimum thickness.

3.3.10 Pad metal composition and minimum and maximum pad metal thickness.

3.3.11 Electrical potential of die bottom surface (e.g., floating, V_{cc} ground), maximum bias voltage or current.

3.3.12 In high power applications, minimum current carrying requirement for the user's substrate.

3.4 Die Electrical Test Data: KGD suppliers shall provide, if applicable, and as negotiated in contractual agreements, the following specialized electrical test data for each KGI Nondisclosure agreements may be required prior to release of some of these data.

- 3.4.1 Designed-in testability features (e.g., redundancy, control fuses, error correction, ad hoc, structured, boundary scan, built-in self test, etc.) with a full description and explanation of each.
- 3.4.2 Device BSDL (Boundary-Scan Description Language) model in cases where IEEE 1149.1 boundary-scan is implemented (ref IEEE/ANSI 1149.1-1990).
- 3.4.3 Any other product specific information relevant to electrical testing.
- 3.4.4 Exceptions to supplier packaged die data book.

3.5 Quality Assurance Provisions: Under the terms of appropriate contractual agreements, KGD suppliers shall be prepared to demonstrate, with data or other certification, one or more of the quality provisions described below. Nondisclosure agreements may be required prior to release of some date. Visual or mechanical requirements shall be in accordance with MIL-STD-883, Test Method 2010, or MIL-H-38534, with particular emphasis on bond pad damage. Die acceptance testing shall be guided by best commercial practice or based upon elemental evaluation per MIL-STD-883, Method 5008.

- 3.5.1 MIL-I-38535 QML certification or equivalent
- 3.5.2 Compliance with MIL-STD-883
- 3.5.3 Compliance with ISO 9000
- 3.5.4 National Electronic Component Quality (NECQ) Audit
- 3.5.5 Compliance with JEDEC JC 19C
- 3.5.6 KGD supplier specific internal quality control methods
- 3.5.7 Outgoing die product DPM (Defects Per Million) due to all causes. (e.g., electrical reference to data sheet, visual and mechanical)
- 3.5.8 100% electrically tested to supplier and user agreed upon specifications.

3.6 Reliability Provisions: Under the terms of appropriate contractual agreements, suppliers shall demonstrate adherence to the agreed upon reliability levels with data, test and screens or other appropriate methods. One or more of the following reliability provisions shall be utilized. Nondisclosure agreements may be required prior to release of some data.

- 3.6.1 "Infant mortality" data or PDA (percent defective allowed) for burned-in die
- 3.6.2 Supplier life test data based on comparable packaged parts expressed as Failures In Time (FIT) rates
- 3.6.3 Projected long-term failure rates
- 3.6.4 Historical fabrication process yield data
- 3.6.5 Other company proprietary approaches (e.g., statistical process controls, in line/end of line monitors, tests and screens, etc.)
- 3.6.6 100% stress testing (e.g., burn-in; baking; temperature cycling) as agreed by supplier-user specification.

3.7 Change Notification: KGD suppliers shall provide notification of changes as specified below. For die defined as compliant to MIL-STD-883, MIL-S-19500, MIL-M-38510, MIL-H-38534, MIL-I-38535, or any other appropriate military documents, change notification shall be in accordance with the requirements defined therein.

- 3.7.1 Immediate Notification: Degradations in die quality or reliability or unanticipated changes in quality assurance provisions for as-delivered product.

3.7.2 Minimum 3 Months Advanced Notice:
- 3.7.2.1 Changes to die size, thickness, and size/location of contact pads, glassivation, bond pad opening or metallization.
- 3.7.2.2 Changes to the die electrical data
- 3.7.2.3 Changes to mechanical handling requirements
- 3.7.2.4 Changes to requirements for transportation protection, shipping and storage
- 3.7.2.5 Anticipated changes in die reliability, quality or quality assurance provisions

3.7.3 Minimum 6 Months Advanced Notice: Discontinuation of die type

3.8 Packing and Shipping: KGD suppliers shall pack and ship KGD product as follows:

3.8.1 Die shall be packed and shipped in a method suitable to ensure protection from mechanical damage, electrostatic discharge, and contamination while allowing recover of die. Special packing and shipping considerations may be included in contractual agreements.

3.8.2 The KGD supplier shall provide a method for coding and maintaining traceability for each die to its wafer lot, and shall maintain traceability data for a minimum period of 5 years, or as required by the procurement document. The KGD user accepts responsibility for maintaining die traceability to the suppliers wafer lot.

3.8.3 As a minimum, each shipment of KGD shall include the following information:
- 3.8.3.1 Generic die type and revision number
- 3.8.3.2 Name of the supplier
- 3.8.3.3 Supplier wafer lot number
- 3.8.3.4 Any other coding necessary to link KGD to proper corresponding documentation.
- 3.8.3.5 Guaranteed speed grade of the KGD (when specified)
- 3.8.3.6 Quantity of KGD in the shipment
- 3.8.3.7 Product specific information (e.g., ESD, sensitivity to light, atmosphere required upon opening, etc.)
- 3.8.3.8 Shipping date
- 3.8.3.9 Wafer number (when required per the contractual agreement)

3.9 Storage Requirements: The following conditions are recommended for the proper storage of KGD. The KGD supplier shall identify any deviations to these conditions and the reason for deviation from the following storage conditions:

3.9.1 Materials: ESD Protective

3.9.2 Storage in Cabinets:
- 3.9.2.1 Atmosphere: Inert gas (nitrogen) or dry air
- 3.9.2.2 Temperature range: 65 to 75°F
- 3.9.2.3 Humidity range: <30%
- 3.9.2.4 Particle count: Class 1000 per FED-STD-209

3.9.3 Sealed in a vacuum or container (not cabinets): Inert atmosphere

4. Additional Information

The KGD supplier may provide, as negotiated, the following data, if available, for information purposes. No warranty is required as to suitability or applicability of these data in the user application. Nondisclosure agreements may be required prior to release of some information.

4.1 Suggested die attach material and properties
4.2 Suggested bond wire size and down bonds (pad number and electrical potential)
4.3 Suggested bonding method (e.g., thermocompression, thermosonic, ultrasonic, etc.)
4.4 Descriptions of any other unique materials or exposed surfaces that may require special protection during assembly
4.5 Suggested limitations on handling methods, or die attach pressures
4.6 Suggested wire bonding sequence, quantity of bond wires on power and ground pins, and stitch-bond (connection) requirements between ground pins
4.7 Suggested lid sealing material and sealing procedure
4.8 Packaged component ESD sensitivity
4.9 Environmental conditions necessary to ensure long term die reliability (e.g., special sealing atmosphere)
4.10 Die power dissipation data or models as a function of frequency, junction temperature, loading and location on die surface.
4.11 Electrical test fault coverage and grader used, as well as test patterns in WAVES (Waveform and Vector Exchange Specification, IEEE 1029.1) format or equivalent
4.12 Die driver and I/O buffer models and data in Berkeley SPICE or equivalent
4.13 Die structural or behavioral models and data in VHSIC Hardware Descriptive Language (Ref IEEE 1076-1987) or equivalent
4.14 Identification of parameters actually tested versus guaranteed by other means (e.g., characterization, correlation, inference)
4.15 Maximum recommended allowable peak die assembly process temperature/times
4.16 T_j to $T_{\text{Die Backside}}$ Relationship
4.17 Dimensional data (for features of top metals and glassification mask layers) in GDS Stream II Format[5]
4.18 Backside surface roughness
4.19 Environmental conditions and storage duration prior to shipment
4.20 Saw kerf shape
4.21 Unusual die material properties (e.g., SiC backside coatings)
4.22 Moisture resistance data (for nonhermetic applications) based upon accelerated stress studies (e.g., 85% RH-85°C, Highly Accelerated Stress Testing, Autoclave, etc.) of existing nonhermetic packaged product.
4.23 Alpha Particle Die Coat. Recommended die coat material, thickness, and application process as required.

[5] GDS Stream II is a Trademark of Valid Logic Systems, Inc.

STANDARD FOR FLIP CHIP KNOWN-GOOD DIE (FC-KGD)

Addendum to Standard For Known Good Die
BUMPED DIE[1]

Preface

This standard was created to facilitate the procurement and use of high reliability semiconductor microcircuits or discrete devices provided in flip attachment die format, commonly known as "Flip Chip Known Good Die" (FC-KGD).

This document provides requirements and guidance to suppliers in regard to the high levels of as-delivered performance, quality and long term reliability expected of flip chip known good die. It also reflects the special needs of FC-KGD product customers in terms of design and application data. This document is applicable to FC-KGD products used in both commercial and military applications.

This standard also reflects an understanding on the part of FC-KGD users that quality and reliability cannot always be guaranteed or assured in the same fashion as for conventionally packaged microcircuits. FC-KGD customers take on a significant responsibility for the proper application and long term environmental protection of this type of product. The extent to which FC-KGD suppliers shall warrant die product is highly dependent upon customer capability and adherence to strict quality controls. Cooperation between suppliers and users is essential.

1. Scope

1.1 This standard provides guidelines and requirements for known-good semiconductor die (FC-KGD) used in other than conventionally packaged microcircuit formats. The die described herein are intended to be high quality, reliable bare dice prepared for flip chip attachment, for use in a variety of user-defined applications (e.g., multichip modules, hybrid circuits, memory cards, etc.) While this standard allows negotiation between supplier and user to establish specific requirements for performance, quality and reliability, it is important to recognize, in the case of military and aerospace applications, the minimum requirements described in relevant military specifications.

1.2 This standard is limited to FC-KGD consisting of a single microcircuit , electrically connected using "bumped" contact technology. The data described and conditions of sale outlined below are intended to cover all varieties of bumping technologies, regardless of metallurgy or physical configuration. Per requirements mutually agreed upon by FC-KGD supplier and user, the FC-KGD supplier shall implement and demonstrate testing and screening required to assure this performance.

1.3 Unlike wirebonded KGD, FC-KGD may not have widely distributed packaged equivalent parts. As such, supplier and user must work closely to ensure die quality assurance methodologies will meet both parties expectations and needs. This standard deals only with FC-KGD supplied in individual die form, for which the user accepts

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[1] A decision was made at the 2 March KGD Task Force Meeting to create a separate stand-alone standard for Bumped KGD corresponding to the JEDEC Wirebonded KGD Standard being balloted 4/93. As this document is as yet unavailable to SEMATECH, this document only highlights changes which will be made to the Wirebonded Standard in order to create the final Bumped KGD stand-alone standard. Major changes to the original Bumped Die Addendum discussed at the 2 March meeting are in boldface.

responsibility for providing and assuring final environmental protection (e.g., hermetic sealing).

2. Reference Documents

2.1 Military and Federal Standards[1]

FED-STD-209	Clean Room and Workstation Requirements, Controlled Environments
MIL-STD-883	Microelectronics, Test Methods and Procedures
MIL-S-19500	General Specification for Semiconductor Devices
MIL-M-38510	General Specification for Microcircuits
MIL-H-38534	General Specification for Hybrid Microcircuits
MIL-I-38535	General Specification for Integrated Circuits Manufacturing

2.2 Institute of Electrical and Electronic Engineers Standards[2]

IEEE 1029.1	Waveform and Vector Exchange Specification
IEEE 1076-1987	VHSIC Hardware Description Language
IEEE/ANSI 1149.1-1990	Standard Test Access Port and Boundary-Scan Architecture

2.3 Electronics Industry Association - Joint Electron Device Engineering Council Standards[3]
JC 19C General Standard for Statistical Process Controls

2.4 American National Standards Institute Documents[4]
ANSI Y14.5 Dimensional Standards

2.5 International Standards[4]
ISO 9000 Series Quality Management Standard

2.6 Other Reference Documents
Relevant FC-KGD Supplier Data Book/Sheet or Specification

2.7 Order of Precedence (microcircuits): In the case of conflict between/among applicable specifications, the following order of precedence shall apply for microcircuits:
2.7.1 Purchase order of other contractual documents
2.7.2 Detailed Specifications
2.7.3 Other mutually agreed documents
2.7.4 This Standard

2.8 Order of Precedence (discrete devices): In the case of conflict between/among applicable specifications, the following order of precedence shall apply for discrete devices:
2.8.1 JAN C die manufactured and tested per MIL-S-19550, Appendix H

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1 Available from: Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120.

2 Available from: Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331.

3 Available from: Electronics Industry Assn, 2001 Eye Street NW, Washington, D.C. 20006.

4 Available from: American National Standards Institute, 1430 Broadway, New York, NY 10018.

2.8.2 Die manufactured and tested by best commercial practices
2.8.3 Die manufactured and tested per MIL-STD-883, Test Method 5008
2.8.4 This Standard

3. Requirements

3.1 Overview: In addition the information provided for the equivalent standard packaged die, FC-KGD suppliers shall provide data as required in sections 3.2 to 3.9. For military and aerospace applications, requirements per the appropriate military specifications and requirements per section 3 shall be adhered to.

3.2 General Data: The following general data shall be provided for each FC-KGD product type.

3.2.1 Part Numbering: Each FC-KGD supplier shall establish a specific part numbering system which differentiates its FC-KGD products from each other, from other bare die product and from conventionally packaged equivalents.

3.2.2 Sample Die: Four types of sample die may be required by FC-KGD users. Availability of these sample types and the quantities to be provided shall be negotiated as part of appropriate contractual agreements. These types include:
3.2.2.1 Conventionally packaged equivalents for system prototyping. Packaged equivalents of FC-KGD may not be available in all cases. Suppliers and users may negotiate a mutually agreeable approach for providing prototyping samples for FC-KGD applications.
3.2.2.2 Mechanical samples of identical physical layout, orientation and pad metallurgy to the final FC-KGD and clearly identified as "reject."
3.2.2.3 Prototype (proof of design) samples that are electrically functional and from a product representative of the FC-KGD to be sold to a particular customer.
3.2.2.4 Acceptance samples which are representative of the updated version of a FC-KGD type which is about to be released with design or manufacturing changes. These samples are intended to afford existing customers of this FC-KGD type an opportunity to evaluate the impact of these changes upon their specific application.

3.3 Design Data: Design data specifically required for the application of KGD shall be provided. Mechanical data shall be provided in a format mutually agreed upon by KGD Supplier and user. The data to be provided are:

3.3.1 Individual FC-KGD dimensions (x,y, thickness, bump dimensions, bump-to-bump centerline/location) with tolerances and units of measure referenced to die center line or other feature. (ANSI Std Y14.5 is the preferred format.)
3.3.2 Minimum die horizontal geometries (feature sizes).
3.3.3 Bump map identifying bump function (i.e., electrical contact, mechanical stabilization, heat conduction, etc.) and electrical pinout list, including electrical potential and pin number one identification with appropriate test designator.
3.3.4 Identification of any connections which must be jumpered or skipped (e.g., test pads).
3.3.5 Type and thickness of backside surface material and surface finish (e.g., polished or lapped).
3.3.6 Maximum and minimum allowable die junction operating temperature.

3.3.7 Known physical process limitations (e.g., temperature sensitivity, pressure sensitivity, uv light sensitivity, etc.).
3.3.8 Other conditions that affect die function, such as critical thermal environments, or additional materials or components normally connected to or used within the packaged part .
3.3.9 Final die passivation (top protective layer) material and minimum thickness.
3.3.10 Bump metal composition, bump volume, and bump height with dimensions and tolerances and uniformity
3.3.11 Electrical potential of die bottom surface (e.g., floating, V_{cc} ground), maximum bias voltage or current.
3.3.12 In high power applications, minimum current carrying requirement for the user substrate.
3.3.13 Guaranteed die edge smoothness and smoothness tolerance. Specify die edge perpendicularity, parallelism and taper.
3.3.14 Minimum distance from the most peripheral bump to edge of a diced FC-KGD.
3.3.15 Physical requirements for mating substrate pads (e.g., heat flow capability, or pull strength).
3.3.16 Identification of polyimide dielectrics or other materials sensitive to plasma cleaning or bonding conditions and thus affect the attachment process.
3.3.17 Identification of the presence of any postdie manufacturing coatings intended to protect die in shipment, along with the processes/chemicals required to assure good connections..

3.4 Die Electrical Test Data: FC-KGD suppliers shall provide, if applicable, and as negotiated in contractual agreements, the following specialized electrical test data for each KGD. Nondisclosure agreements may be required prior to release of some of these data.

3.4.1 Designed-in testability features (e.g., redundancy, control fuses, error correction, ad hoc, structured, boundary scan, built-in self test, etc.) with a full description and explanation of each.
3.4.2 Device BSDL (Boundary-Scan Description Language) model in cases where IEEE 1149.1 boundary-scan is implemented (ref. IEEE/ANSI 1149.1-1990).
3.4.3 Any other product specific information relevant to electrical testing.
3.4.4 Exceptions to supplier packaged die or KGD data book.

3.5 Quality Assurance Provisions: Under the terms of appropriate contractual agreements, FC-KGD suppliers shall be prepared to demonstrate, with data or other certification, one or more of the quality provisions described below. Nondisclosure agreements may be required prior to release of some date. Visual or mechanical requirements shall be in accordance with best commercial practice.

3.5.1 MIL-I-38535 QML certification or equivalent
3.5.2 Compliance with MIL-STD-883
3.5.3 Compliance with ISO 9000
3.5.4 National Electronic Component Quality (NECQ) Audit
3.5.5 Compliance with JEDEC JC 19C
3.5.6 FC-KGD supplier specific internal quality control methods, including those specific to die bumps.
3.5.7 Outgoing die product DPM (Defects Per Million) due to all causes. (e.g., electrical reference to data sheet, visual, mechanical, missing/low volume bumps). Definitions of bump rejection criteria (i.e., reject vs. cosmetic defect) shall be provided.
3.5.8 100% electrically tested to supplier and user agreed upon specifications.

3.6 Reliability Provisions: Under the terms of appropriate contractual agreements, suppliers shall demonstrate adherence to the agreed upon reliability levels with data, test and screens or other appropriate methods. One or more of the following reliability provisions shall be utilized. Nondisclosure agreements may be required prior to release of some data.

- 3.6.1 "Infant mortality" data or PDA (percent defective allowed) for burned-in die
- 3.6.2 Supplier life test data based on comparable packaged parts expressed as Failures In Time (FIT) rates
- 3.6.3 Projected long-term failure rates
- 3.6.4 Historical fabrication process yield data
- 3.6.5 Other company proprietary approaches (e.g., statistical process controls, in line/end of line monitors, tests and screens, bump reliability testing/failure modeling, etc.)
- 3.6.6 100% stress testing (e.g. burn-in; baking; temperature cycling) as agreed by supplier-user specification.

3.7 Change Notification: FC-KGD suppliers shall provide notification of changes as specified below. For die defined as compliant to MIL-STD-883, MIL-S-19500, MIL-H-38534, MIL-I-38535, or any other appropriate military documents, change notification shall be in accordance with the requirements defined therein.

- 3.7.1 Immediate Notification: Degradation in die quality or reliability or unanticipated changes in quality assurance provisions for as-delivered product.
- 3.7.2 Minimum 3 Months Advanced Notice:
  - 3.7.2.1 Changes to die size, thickness, glassivation, bond pad opening or metallization.
  - 3.7.2.2 Changes to the die electrical data
  - 3.7.2.3 Changes to mechanical handling requirements
  - 3.7.2.4 Changes to requirements for transportation protection, shipping and storage
  - 3.7.2.5 Anticipated changes in die reliability, quality or quality assurance provisions
  - 3.7.2.6 Changes to contact bump location, composition, hardness(as required), height, and uniformity (as required).
- 3.7.3 Minimum 6 Months Advanced Notice: Discontinuation of die type

3.8 Packing and Shipping: FC-KGD suppliers shall pack and ship FC-KGD product as follows:

- 3.8.1 Die shall be packed and shipped in a method suitable to ensure protection from mechanical damage (including mechanical and chemical integrity of bumps), electrostatic discharge, and contamination while allowing recovery of die. This requirements extends to shipment of bumped die in special individual carriers, and to the protection of carrier electrical contacts. Special packing and shipping considerations may be included in contractual agreements.
- 3.8.2 The FC-KGD supplier shall provide a method for coding and maintaining traceability for each die to its wafer lot, and shall maintain traceability data for a minimum period of 5 years, or as required by the procurement document. The FC-KGD user accepts responsibility for maintaining die traceability to the wafer lot.

3.8.3 As a minimum, each shipment of FC-KGD shall include the following information:

3.8.3.1 Generic die type and revision number
3.8.3.2 Name of the supplier
3.8.3.3 Supplier wafer lot number
3.8.3.4 Any other coding necessary to link FC-KGD to proper corresponding documentation.
3.8.3.5 Guaranteed speed grade of the FC-KGD (when specified)
3.8.3.6 Quantity of FC-KGD in the shipment
3.8.3.7 Product specific information (e.g., ESD, sensitivity to light, atmosphere required upon opening, etc.)
3.8.3.8 Shipping date
3.8.3.9 Wafer number (when required per the contractual agreement)
3.8.3.10 Die coatings applied for protection in shipment

3.9 Storage Requirements: The following conditions are recommended for the proper storage of FC-KGD. The FC-KGD supplier shall identify any deviations to these conditions and the reason for deviation from the following storage conditions:

3.9.1 Materials: ESD Protective
3.9.2 Storage in Cabinets:
3.9.2.1 Atmosphere: Inert gas (nitrogen) or dry air
3.9.2.2 Temperature range: 65 to 75°F
3.9.2.3 Humidity range: <30%
3.9.2.4 Particle count: Class 1000 per FED-STD-209
3.9.3 Sealed in a vacuum or inert atmosphere

4. Additional Information

The FC-KGD supplier may provide, as negotiated, the following data, if available, for information purposes. No warranty is required as to suitability or applicability of these data in the user application. Nondisclosure agreements may be required prior to release of some information.

4.1 Suggested die attach material and properties
4.2 Suggested substrate pad size, thickness, and composition with dimensions and tolerances
4.3 Recommended bumped die attach process including heating process (e.g. hot bar, furnace, infrared, laser) and compatible chemical/materials.
4.4 Descriptions of any other unique materials or exposed surfaces that may require special protection during assembly
4.5 Suggested limitations on handling methods, or die attach pressures
4.6 Suggested lid sealing material and sealing procedure
4.7 Packaged component ESD sensitivity
4.8 Environmental conditions necessary to ensure long term die reliability (e.g., special sealing atmosphere)
4.9 Die power dissipation data or models as a function of frequency, junction temperature, loading and location on die surface.
4.10 Electrical test fault coverage and grader used, as well as test patterns in WAVES (Waveform and Vector Exchange Specification, IEEE 1029.1) format or equivalent
4.11 Die driver and I/O buffer models and data in Berkeley SPICE or equivalent
4.12 Die structural or behavioral models and data in VHSIC Hardware Descriptive Language (Ref. IEEE 1076-1987) or equivalent
4.13 Identification of parameters actually tested versus guaranteed by other means (e.g., characterization, correlation, inference)

4.14 Maximum recommended allowable peak die assembly process temperature/times
4.15 T_j to $T_{Die\ Backside}$ Relationship
4.16 Dimensional data (for features of top metals and glassivation mask layers) in GDS Stream II Format[5]
4.17 Backside surface roughness
4.18 Environmental conditions and storage duration prior to shipment
4.19 Saw kerf shape
4.20 Unusual die material properties (e.g., SiC backside coatings)
4.21 Moisture resistance data (for nonhermetic applications) based upon accelerated stress studies (e.g., 85% RH-85°C, Highly Accelerated Stress Testing, Autoclave, etc.) of existing nonhermetic packaged product.
4.22 Recommended alpha particle die coat material, thickness, and application process as required.
4.23 Recommended bumped die removal/rework process including compatible chemicals/materials.
4.24 Recommended re-use criteria/process (e.g., bump reflow) for reworked die prior to subsequent reattach.
4.25 Recommended materials, conditions and preparation for substrate bumps mating to die bumps.

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[5] GDS Stream II is a Trademark of Valid Logic Systems, Inc.

- DRAFT 2.0, 9 Apr 93 -

STANDARD FOR PROVIDING/USING KNOWN-GOOD DIE

Addendum For TAPE AUTOMATED BONDED DIE[1]

0. Preface

0.1 This addendum supplements the JEDEC Standard for Providing/Using Known Good Die (Wirebonded) through the identification of special considerations relevant to Tape Automated Bonded Known-Good Die. While these die will be physically and electrically connected differently than "bare" die, they are otherwise the same high reliability semiconductor microcircuits as described the wirebonded standard.

0.2 This addendum identifies only the additions or modifications to elements of the wirebonded standard which are effected by TABed die. Unless specifically stated, the requirements and conditions of the basic wirebonded die standard remain in force.

1. Scope

1.1 This standard covers KGD delivered in Tape Automated Bonding interconnect format. Bare die which are purchased for processing into TAB interconnection format arc not covered under this specification. This standard identifies all data requirements and conditions of sale which might apply to any variety of TABed KGD, regardless of size or contact technology.

2. Reference Documents:

2.3 Electronics Industry Association - Joint Electron Device Engineering Council Sta: lards[2]

JC11.4-UO-018 Tape Automated Bonding (TAB) Packaging Family Outline

2.6 Other Reference Documents

Supplier Bumped Die Data Sheets/Books

3. Requirements

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[1] A decision w#s made at the 2 March KGD Task Force Meeting to create a separate stand-alone standard for TABed KGD corresponding to the JEDEC Wirebonded KGD Standard being balloted 4/93. As this document is as yet unavailable to SEMATECH, this document only highlights the changes which will be made to the Wirebonded Standard in order to create the final TABed KGD stand-alone standard. Major changes to the original TABed die Addendum discussed at the 2 March meeting are in boldface.

[2] Available from: Electronics Industry Assn, 2001 Eye Street NW, Washington, D.C. 20006.

3.2 General Data:

3.2.2 Sample Die:

3.2.2.1 TAB interconnected die may not be available in packaged form in all cases. Suppliers and users may negotiate a mutually agreeable approach to providing sample die for prototyping a TABed die application.

3.3 Design Data: In some cases, non-disclosure and/or licensing agreements may be required prior to release of relevant mechanical design data as described in this section.

3.3.3 TAB frame map showing tab frame dimensions and identifying electrical potential, pin identification or test designator. Reference to corresponding standard TAB outline shall be provided if appropriate. (Ref JC11.4-UO-018, TAB Packaging Family Outline)

3.3.15 In order to facilitate use of optical pattern recognition equipment, TAB part map with alignment or registration marks identified.

3.3.17 In order to facilitate tab leadframe attach, identification of polyimide dielectrics or other materials sensitive to plasma etch cleaning or bonding pressures.

3.3.18 In order to facilitate proper TAB usage, identification of the presence of any post manufacturing surface coatings intended to protect TAB leads in shipment shall be identified, along with the process/chemicals for removal of these coatings.

3.5 Quality Assurance Provisions:

3.5.6 KGD supplier specific internal quality controls on TAB components including specialized process controls or inspection systems. These controls may include post-manufacturing die coatings and/or packing containers intended to preserve die quality.

3.5.7 For TABed die, defects contributing to DPM calculations include failures due to improper mechanical contacts between die and TAB frame (e.g. missing/broken TAB leads, or improper leadframe contacts). Definitions of criteria identifying a reject vs. cosmetic defect shall be provided.

3.6 Reliability Provisions:

3.6.5 For TABed die, Company proprietary reliability provisions must include those relevant to TAB interconnection and may include TAB lead reliability testing or TAB interconnection failure modeling.

3.7 Change Notification:

3.7.2 Minimum Three Months Advanced Notice:

3.7.2.1 Changes of TAB outline or location/configuration of TAB leads.

3.8 Packing and Shipping:

3.8.1 Packing and shipping methodologies shall also ensure mechanical and chemical protection of TAB leads, thus assuring proper TAB bonding. This protection includes consideration of tape reels or other containers in which TABed die may be shipped.

4. Additional Information

The KGD supplier may provide, as negotiated, the following data, if available, for information purposes. No warranty is required as to suitability or applicability of these data in the user's application. Non-disclosure agreements may be required prior to release of some information.

4.3 Recommended TAB excise method and attach process including bonding parameters (e.g. thermosonic bonding, laser, etc.) compatible chemicals/materials.

4.18 Recommended TAB removal/rework sequence process including compatible chemicals/materials. Recommended re-use criteria/process for TAB contact reprocessing prior to subsequent reattach.

4.19 Recommend materials, conditions and preparation for substrate bumps to which TABed die are to be attached.