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SUB-MILLIMETERWAVE SEMICONDUCTOR SIGNAL SOURCES

Hughes Research Laboratories

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Research on Indium Phosphide Pseudomorphic High Electron Mobility Transistors (InP PHEMTs) resulted in 155 GHz and 215 GHz monolithic integrated circuit oscillators. These circuits represent the highest frequencies achieved to date for a fundamental signal source using a three terminal device. Advances in epitaxial growth of the pseudomorphic semiconductor structures and the achievement of low-resistance, 50-nm-long self-aligned gates resulted in the highest short circuit current gain cutoff frequency (ft) transistors ever reported. The planar quasi-optical slot oscillators verify the high frequency capabilities of the InP PHEMT. Hughes Research Laboratories performed the research on materials, device design and processing, and device characterization and modeling. The University of Michigan designed the oscillator circuits, including the integrated planar antennas, and measured the oscillator performance.

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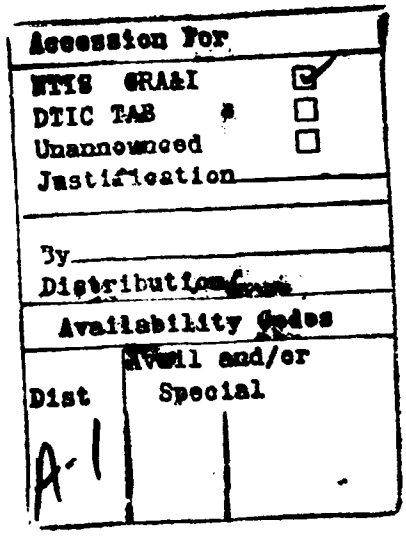

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Section 1
INTRODUCTION AND PROGRAM SUMMARY

Hughes Research Laboratories (HRL) is pleased to submit this final report to summarize the activities on the Sub-millimeterwave Signal Sources Program. The purpose of the program was to perform research on three-terminal room-temperature integrated oscillator circuits operating at frequencies at or above 500 GHz. This program has resulted in the fabrication and testing of world-record oscillator circuits that perform at more than twice previously reported frequencies and brought together the unique talents of the Hughes Research Laboratories' Microwave Devices and Circuits Laboratory, and the University of Michigan Radiation Laboratory and Center for Space Terahertz Technology, and the guidance of the Air Force Rome Laboratory.

The program efforts resulted in oscillators operating at frequencies of 155 and 213 GHz. These results are believed to be by far the highest frequency three-terminal oscillators reported to date.

The program proceeded through two iterations of the design, fabrication, and testing phases. The first iteration, while unsuccessful in producing working circuits, resulted in the highest short circuit current gain cutoff frequency (f_T) transistors ever reported. In addition, information learned in the first iteration made it possible to produce working oscillators on the second iteration.

Hughes Research Laboratories acted as the device design and modeling member of the team, as well as the circuit fabrication facility. The University of Michigan designed the oscillator circuits, including the integrated planar antennas. The University also measured the oscillator performance.

InP-based High Electron Mobility Transistor (HEMT) technology was used to fabricate the active devices that were at the heart of the oscillators. The HEMT gates were fabricated with sub-tenth-micrometer electron-beam techniques to achieve gate lengths on the order of 50 nm. Planar antennas were integrated into the fabrication process resulting in a compact and efficient Monolithic Integrated Millimeterwave Circuit (MMIC).

Section 2
MATERIALS RESEARCH

The epitaxial layers used in this work were grown sequentially in a Riber 2300 molecular-beam epitaxy (MBE) system, typically at a substrate temperature of 500°C, a growth rate of 600 nm/h, and a V/III beam equivalent pressure ratio of 40. Further details of these standard growth conditions can be found in Ref. [1]. Figure 1 is a diagram of the layer structure of the MBE material.

The growth of the delta-doped structures deviates from the standard conditions in several ways. The first is a reduction of the substrate temperature during and after the growth of the delta-doped layer, in order to minimize the surface segregation of silicon atoms in AlInAs. By controlling the growth temperature in this fashion, we are able to improve the abruptness of the silicon profile and achieve an increase of approximately 20 to 30% in electron transfer efficiency [2]. In this work, the growth was interrupted twice, approximately 1 minute each, to accommodate the temperature changes. The first interruption occurred just before the deposition of the delta-doped layer, during which the substrate temperature was reduced to 320°C. The second interruption took place immediately after the growth of this delta-doped layer and the first 1.7 nm of the undoped AlInAs Schottky layer, during which the substrate temperature was reset to 500°C.

The second modification is the use of a wider spacer thickness. In order to maintain a reasonably high mobility, we increased the spacer thickness of the delta-doped structures from 2 to 6 nm. Their room-temperature mobility rapidly increases from approximately 7800 to 10,050 cm^2/Vs as a result of a baseline uniformly doped structure with 2.0-nm spacer thickness.

Finally, the last, but most important, is a lower substrate temperature during the growth of the pseudomorphic channel. We grew this layer at a substrate temperature of 440°C, as opposed to the standard 500°C, to prevent the formation of three-dimensional nucleations and misfit dislocations. The high quality of our pseudomorphic structures is clearly evident in their high mobilities, both at 300°C and 77°K. Each wafer's mobility and sheet charge is shown in Table 1.

Three types of AlInAs/GaInAs HEMT structures were investigated during the course of this work. The first structure is a baseline design which consists of a relative-thick lattice-matched GaInAs channel (40 nm) and a uniformly doped donor layer (8 nm), 6×10^{18} cm^{-3}.[3,4] This design typically yields a 2DEG sheet density of 3.0×10^{12} cm^{-2} and a mobility of 10,500 $cm^2/V\cdot s$ at room temperature. The second structure employs a much narrower channel (20 nm) and a delta-doped donor layer (~5×10^{12} cm^{-2}), but exhibits a similar 2DEG sheet density and mobility (2.9×10^{12} cm^{-2}), 10,050 $cm^2/V\cdot s$). The third structure incorporates a thin pseudomorphic GaInAs layer (7.5 nm, 80% In) in the uppermost of its 20-nm-thick channel. This structure exhibits an approximately 20% increase increase in 2DEG sheet density, from 2.9 to 3.6×10^{12} cm^{-2}, and 26% increase in mobility, from 10.050 to 12,800 cm2/V•s at 300°K.

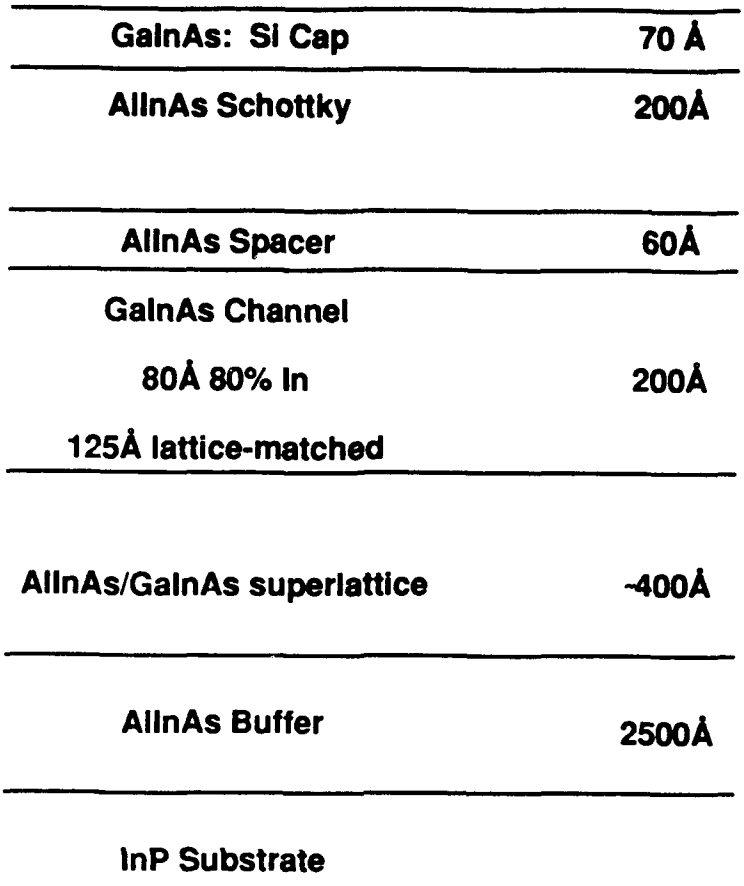


Figure 1. Diagram of layer structure of MBE material.

Table 1. Mobility and Sheet Charge Data on Oscillator Circuit Wafers.

Wafer	Sheet Charge (cm^{-2})	Mobility ($cm^2/V\text{-}s$)
3532	2.7×10^{12}	12,400
3533	3.0×10^{12}	11,600
3534	2.5×10^{12}	12,300
3535	2.6×10^{12}	11,950

Section 3
DEVICE DESIGN AND FABRICATION

We employed a self-aligned-gate (SAG) process first proposed by Mishra *et al.* [5], which consists of five levels: (1) alignment marks, (2) device isolation, (3) T-shaped gate definition, recess, and metallization (Ti/Pt/Au), (4) ohmic definition, metallization (AuGe/Ni/Au) with the T-shaped gate serving as a shadow mask, and alloying, and finally, (5) overlay. We defined the sub-0.1-μm gates in a bi-layer of PMMA/P(MMA-MAA) electron-beam resist using a Philips EBPG-4 electron-beam lithography system operating at 50-kV acceleration voltage. Figure 2 shows the cross section of a 50-nm T-shaped gate after the deposition of the self-aligned ohmic metal. The addition of the ohmic metal reduces the resistance of the gate from approximately 1500 to 1000 Ω/mm, which is the lowest resistance ever reported for a 50-nm-long gate [6].

Typical peak extrinsic transconductance for the final wafer lot was approximately 1400 mS/mm, with associated extrinsic short-circuit current-gain cutoff frequency f_T equal to approximately 330 GHz.

9125-11-051R1

Figure 2. Photograph of cross-section of 50-nm T-shaped gate.

Focused Ion Beam FIB (FIB) technology was also used to fabricate transistor gates at the beginning of this program. A gate fabrication technique was developed based on FIB exposure and reactive ion etching of a polymethylmethacrylate (PMMA)/Ge/PMMA multilevel resist structure. The FIB exposed the thin PMMA imaging layer that is transferred directly to the germanium layer using reactive ion etching (RIE). The underlying resist was etched first in oxygen at high pressure, providing an undercut, bowl-shaped profile, followed by an extremely low pressure, anisotrophic oxygen process, which etched a narrow stem down to the base of the resist, resulting in a chalice-shaped profile. Removing the germanium layer allowed the profile to be used to lift of the Ti/Pt/Au gate. The process was compatible with our self-aligned gate HEMT process and provided an alternative technique for gate fabrication below 75 nm.[7] The technology proved to be too immature, however, for use in this program. As a result we decided to employ our more fully developed electron-beam process.

Section 4
CIRCUIT PROCESSING

The processing of the circuits begins with ohmic contacts other than the device ohmics. The areas are defined by lifting off AuGe-Ni-Au metallurgy. Second is the isolation implant, used to define the active area of the transistors, achieved using boron ions. Implantation allows for a completely planar process (as opposed to a mesa isolation technique).

Next is the self-aligned-gate (SAG) process, which was described in the previous section. The process has two steps: the first defines the gate itself, and the second, which uses a broader beam, defines the gate feed. This process is followed by the device ohmic step, wherein the gate itself acts as a mask for the ohmic metal, also described in the previous section.

Next is what we refer to as the perimeter etch. In early iterations of the program, the transmission lines were fabricated directly on the highly doped cap layer of the material system. We believed there was a potential problem of excessive loss in the transmission lines due to conduction in the cap layer, causing leakage between the signal and ground of the coplanar transmission lines. For this reason, we added a step to the process to etch down to the InP substrate everywhere except in the device itself, to provide a very high resistance dielectric for transmission line fabrication.

A separate step is used to define the capacitor bottom plates, which results in a smoother metal surface to nearly eliminate the phenomenon of pinholes in the dielectric caused by too rough a lower capacitor surface. The following step is the metal overlay, also referred to as first-level metal, which defines the device electrodes and the transmission lines and ground planes. Next, the capacitor dielectric layer is formed. The dielectric material is 0.22 μm of silicon monoxide (SiO). The post fabrication step then defines the size of the capacitors. Finally, the span step is used to fabricate the airbridges from the capacitors, as well as the plated metal on the transmission lines and ground plane.

Section 5
DEVICE MODELING

The circuit designs in this program depended heavily on knowledge of the device performance and characteristics at the oscillators' intended frequency of operation. Since the oscillators were designed to operate at extremely high frequencies (150 GHz and above), which are higher than currently available vector measurement capabilities, an accurate model of the device was necessary. We used a method of obtaining this model that had been very successful in past programs.

The device intended for use in all of the oscillator circuits was a 10-μm-wide Self-Aligned-Gate (SAG) High Electron Mobility Transistor (HEMT). In order to obtain a model for such a device, however, we needed a larger gate width transistor so that the measurement would not be dominated by parasitics. For this reason, we used a 50-μm-gate-width HEMT.

The modeling process is based on an equivalent circuit extraction from the S-parameters of the device [8]. A full equivalent circuit model of the HEMT with parasitics is shown in Figure 3. The parasitics are modeled as a shell of Y-parasitics (capacitances) and a shell of Z-parasitics (resistances and inductances). The de-embedding procedure is as follows: The S-parameters of an "open" device (i.e., pads with no active transistor) are measured over frequency; then a "shorted" device (i.e., pads shorted together) is also similarly measured; these parameters are used to directly determine the parasitic element values. The intrinsic HEMT model is then determined as follows: The device S-parameters are measured and converted, using the well known transformation, to Y-parameters; then the parasitic Y-parameters are subtracted; the "stripped" Y-parameters are then converted to Z-parameters; next the parasitic Z-parameters are subtracted; and, finally, the "stripped" Z-parameters are converted to Y-parameters, which can now be considered the *intrinsic* Y-parameters. The element values of the intrinsic model are then calculated from the intrinsic Y-parameters using the following equations:

$$Y_{gs}=Y_{11}+Y_{12}$$

$$Y_{gd}=-Y_{12}$$

$$Y_{ds}=Y_{22}+Y_{12}$$

$$Y_{gm}=Y_{21}-Y_{12}$$

The intrinsic element values follow here:

$$C_{gs}=\frac{-1}{\mathrm{Im}[1 / Y_{gs}]\omega}$$

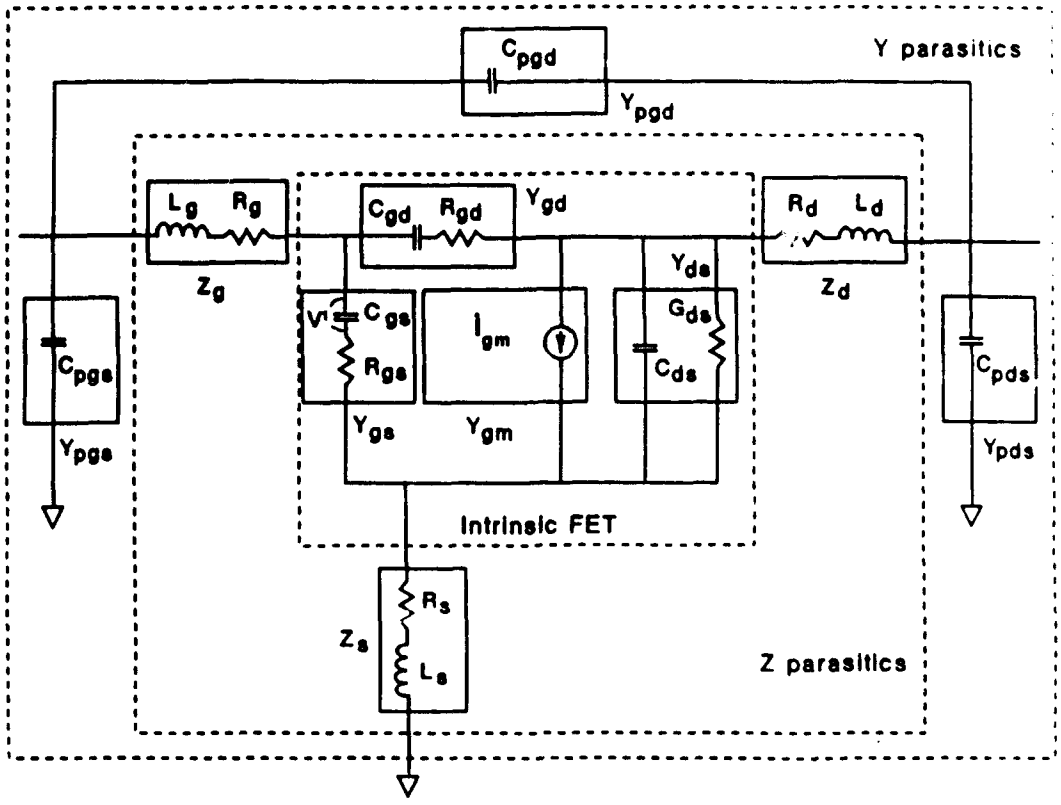


Figure 3. Equivalent circuit model of HEMT (with parasitics).

$R_{gs}=Re[1/Y_{gs}]$

$$C_{gd}=\frac{-1}{Im[1/Y_{gd}]\omega}$$

$R_{gd}=Re[1/Y_{gd}]$

$C_{ds}=Im[Y_{ds}]/\omega$

$G_{ds}=Re[Y_{ds}]$

$g_m=g_{mo}e^{-j\omega\tau}$

$g_{mo}=mag[Y_{gm}(1+j\omega\tau)]$

$\tau=ang[Y_{gm}(1+j\omega\tau)]/\omega$

Once the equivalent circuit of the 50 μm HEMT was determined using the method described above, it could be easily scaled to a 10 μm equivalent. The resulting equivalent circuit model was used to design the oscillator circuits. The process yielded the following intrinsic equivalent circuit model:

C_{gs}=6.6 fF

C_{gd}=1.0 fF

C_{ds}=0.4 fF

R_{gs}=5 Ω

R_{gd}=1200 Ω

G_{ds}=1.52 mS

g_m=16 mS

τ=0.5 ps

Because the HEMT had to be connected to the rest of the circuit by way of contacting electrodes we had to estimate new parasitic values for the device in the circuit. Since there was no way to measure and/or simulate these values directly, we determined high and low estimates of each parasitic so that designs could be done for each extreme. The following high and low values were used in the designs:

Cgsp(low)=2 fF	Cgsp(high)=4 fF
Cgdp(low)=1 fF	Cgdp(high)=2 fF
Cdsp(low)=1.5 fF	Cdsp(high)=3 fF
Lg(low)=5 pH	Lg(high)=10 pH
Ld(low)=10 pH	Ld(high)=20 pH
Ls(low)=6 pH	Ls(high)=12 pH

When measuring the DC I-V curves of the test devices, we noticed a discrepancy between the DC and RF values of the transconductance g_m. While the extracted RF transconductance was found to be 16 mS, the DC measurements showed it to be closer to 10 mS. For this reason, an additional variable was added to the matrix of device models, and designs were done using both values of transconductance.

Section 6
CIRCUIT DESIGN

Designs were completed for planar oscillators at several frequencies, using multiple configurations of parasitic and device parameters. The designs were done using a procedure that utilizes matching to the reflection coefficient of the output of the oscillator, rather than the real and imaginary impedances.

The design procedure places transmission lines at the gate and source terminals of the device model and uses the Touchstone/Libra optimizer to calculate the lengths of the lines necessary to give the largest reflection coefficient (much greater than one) at the drain terminal. Then a slot antenna is designed so that it can be matched to the unstable device with a length of line. The result of the matching is that the phase of the reflection coefficient is opposite in sign to that of the device, and the magnitude of the reflection coefficient is significantly larger than the inverse of that of the device. This will allow any noise signals in the system to build up into oscillations according to the reflection amplifier perspective.[9,10,11]

The designs were carried out using the given device model assuming all combinations of high transconductance (16 mS) and low transconductance (10 mS), and high and low values for the extrinsic parasitics. The low values were taken to be Lg=5 pH, Ld=10 pH, Ls=6 pH, Cpgs=2 fF, Cpgd=1 fF, and Cpds=1.5 fF. The high values were taken to be Lg=10 pH, Ld=20 pH, Ls=12 pH, Cpgs=4 fF, Cpgd=2 fF, and Cpds=3 fF. All the coplanar waveguide (CPW) lines have a center conductor width of 10 μm and gap widths of 5 μm, which give a characteristic impedance of 50 Ω and an effective dielectric constant of 6.7 on indium phosphide. The designs were conducted assuming a total loss in this line of 0.67 dB/mm at 60 GHz, scaled with the square root of frequency. We determined the loss by extrapolating information from two papers appearing in the 1992 IEEE MTT-S Digest (M. Zhang et al. and W. H. Haydl et al.). Designs were completed at frequencies of 150, 200, 300, 400, 450, 500, and 550 GHz.

In the first design iteration, we applied the bias voltages through airbridges at the end of the source and drain lines to bypass capacitors. This technique can lead to problems arising from the effects of these completely uncharacterized discontinuities located in critical areas of the circuit (right at the feed of the slot antenna or at an assumed RF short). Therefore, in the final designs, we used small slits in the ground plane to DC-isolate the source, drain, and gate of the transistor. The slits were fabricated with capacitive overlays to provide for good RF continuity.

Figure 4 is a simple diagram of a circuit template. The common-gate HEMT is in the middle of the diagram. The length of line extending to the left from the source terminal and the lengths of line extending from the gate terminal are adjusted for each design to achieve the highest positive magnitude of reflection coefficient at the drain terminal. The length of line connected to the drain is chosen such that when coupled with the planar antenna (far right), the

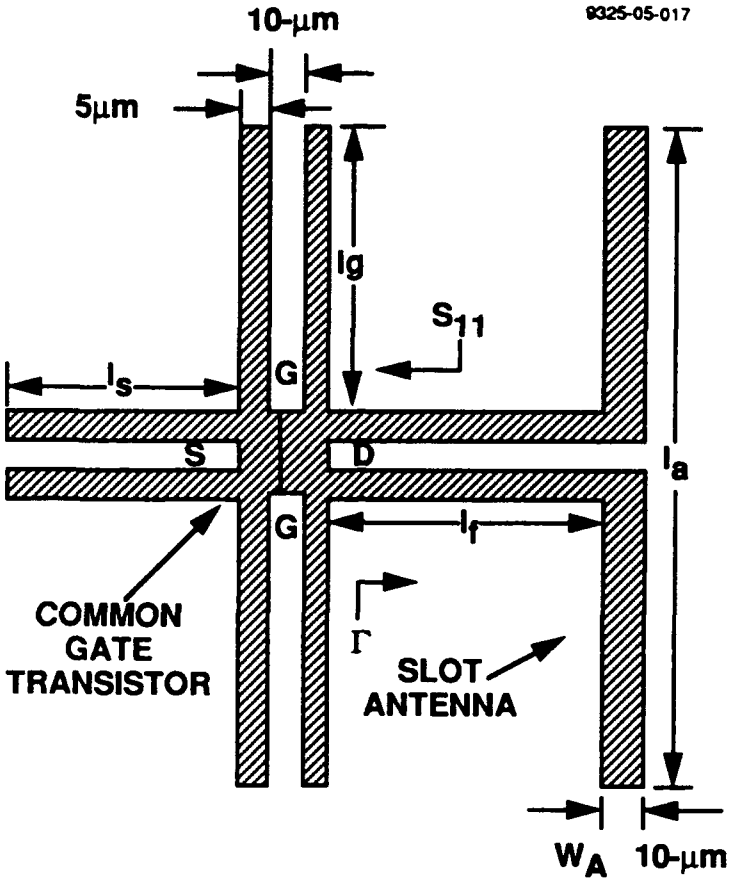


Figure 4. Simple diagram of circuit template.

reflection coefficient seen at the drain has the negative of the angle of the reflection coefficient looking into the drain terminal.

Table 2 is a complete matrix of designs. Not all the designs were physically possible to layout, however, so we used a subset of the designs. Figure 5 is a photograph of an example circuit. The final mask reticle is shown in Figure 6. Sixteen designs were used in the layout and were named according to the following convention: fffP_xx, where fff is the frequency in gigahertz, P is either H or L, for high and low parasitic values. respectively, and xx is 10 or 16, for 10 or 16 mS transconductance. The designs that make up the reticle are: (1) 150L10, (2) 150L16, (3) 150H10, (4) 150H16, (5) 200L10, (6) 200L16, (7) 200H16, (8) 300L16, (9) 400H16, (10) 450L16, (11) 450H16, (12) 500L16, (13) 500H16, (14) 500H16A (a second variation of 500 H16), (15) 550L16, and (16) 550L16A (a second variation of 550L16A).

Table 2. Oscillator Circuit Design Matrix

F (GHz)	Lp,Cp*	g_m (mS)	l_s (μm)	l_s (μm)	l_f (μm)	l_a** (μm)	l/S_{11} (mag,ang)	Γ (mag,ang)
150	Low	10	221	177	187.5	390	0.002, -176	0.500, -176
150	Low	16	205.5	183	183.5	390	0.007.-172.6	0.501, 172.6
150	High	10	239	164.5	230.5	360	0.188, 164.4	0.595, 164
150	High	16	291	155.5	112.5	390	0.010, -106	0.514, -106
200	Low	10	176	126	169	270	0.131, 171	0.606, 171
200	Low	16	223	118	132	300	0.010, 168	0.495, 168
200	High	10	180	113.5	5	0	0.497, 174	0.999, 174
200	High	16	194	109	195.5	300	0.010, 112.5	0.486, 112.5
300	Low	10	65	0	78.5	0	0.856, 33.5	0.973, 33.5
300	Low	16	111.5	76.5	93.5	200	0.022, -172	0.517, -172
300	High	10	30	0	50	0	0.677, 86.4	0.983, 86.4
300	High	16	52	0	2	110	0.433, 82.7	1.940, 82.3
400	Low	10	31	138	51	0	0.754, 53.4	0.980, 53.3
400	Low	16	41	0	8.5	90	0.400, 54	0.919, 54
400	High	10	0	123	14.5	0	0.612, 144	0.994, 144
400	High	16	9	119.5	89	160	0.098, 133.3	0.477, 133
450	Low	10	15.5	0	39	0	0.719, 72	0.984,71
450	Low	16	25	0	1	70	0.180, 81	0.949, 81
450	Low	16	29	120	132	70	0.192, 75	0.894, 75
450	High	10	121	104	0	0	0.786, -177.3	1.000, -180
450	High	16	127	99.5	71.5	130	0.157, 17[illegible]	0.594, 173
500	Low	10	12	104	31	0	0.720, 83	0.986, 83
500	Low	16	14	111	64.5	160	0.040, 103	0.249, 103
500	Low	16	11	0	79	130	0.074, 111	0.493, 110.5
500	High	16	107	86.5	71	70	0.323, -147	0.897, -146.5
550	Low	10	6	91.5	23.5	0	0.770, 100	0.989, 100
550	Low	16	1.5	0	89.5	60	0.283, 132	0.895, 132
550	Low	16	20.5	74.5	46	120	0.004, -162	0.500, -162
550	High	16	92.5	76.5	87.5	0	0.557, -118.5	0.960, -118.6

* Lp,Cp are the extrinsic parasitic inductors and capacitors in the device model where Low parasitics correspond to the following values: L_g = 5pH, L_d = 10pH, L_s = 6pH, C_{pgs} = 2fF, Cp_{gd} = 1fF, C_{pds} = 1.5fF, and High parasitics correspond to the following values: L_g = 10pH, L_d = 20pH, L_s = 12pH, C_{pgs} = 4fF, C_{pgd} = 2fF, C_{pds} = 3fF.

** A zero length in this column indicates that a short circuit should be used in place of an antenna. It is then the total length from the device drain to the short, and no attempt should be made to account for the antenna width (W_A).

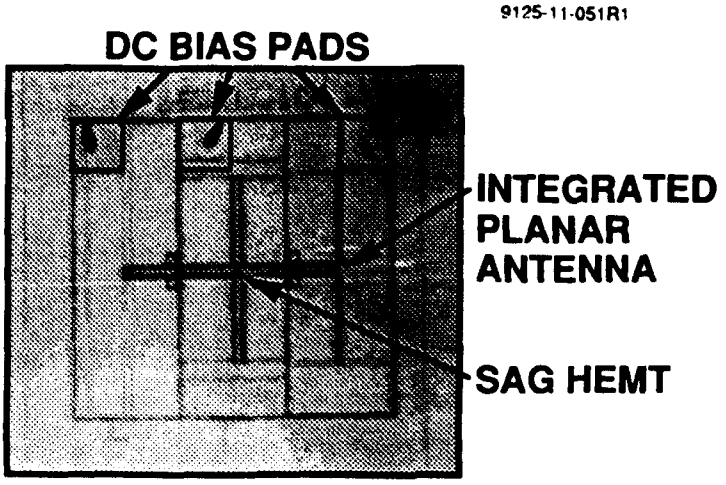


Figure 5. Photograph of oscillator circuit.

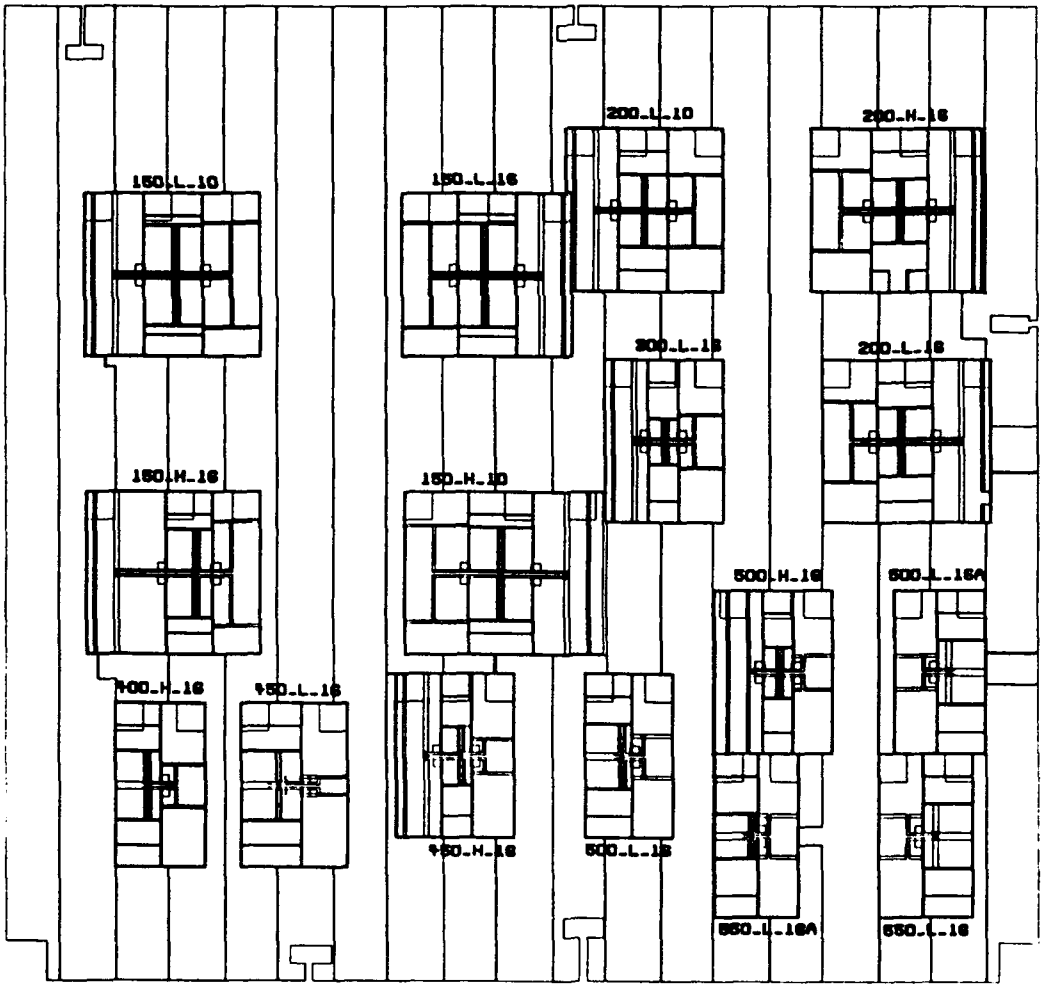


Figure 6. Final mask reticle.

Section 7
OSCILLATOR MEASUREMENTS

The oscillators were measured using two types of techniques for determining the frequency of operation and a third to determine, to first order, the output power of the oscillators. The former two methods include a direct quasi-optical interferometer technique and a coherent heterodyne detection technique that uses harmonic mixing to detect the oscillations at a lower IF frequency.

The block diagram in Figure 7 illustrates the quasi-optical measurement setup. The oscillator is biased through the use of DC needle probes and DC power supplies. A silicon substrate lens is mounted opposite the side of the wafer containing the circuits. The oscillation signal is reflected by a mirror through a chopper into an interferometer. The presence of an oscillation is detected by a liquid-helium-cooled InSb bolometer, which can detect signals well below the microwatt level. The bolometer output is amplified through a low-noise preamplifier before it is displayed on an oscilloscope. The spacing between the interferometer planes is varied to determine the distance between peaks in the signal, which denotes the wavelength of the oscillation and, hence, the frequency.

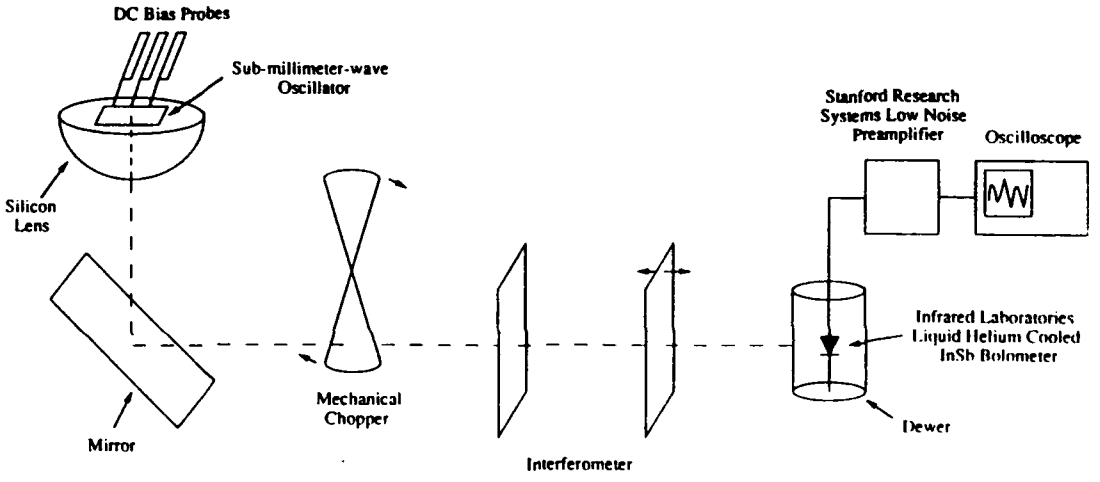


Figure 7. Quasi-optical interferometer measurement setup.

A second system used to determine the frequency of oscillation is the coherent heterodyne detection technique, illustrated in the block diagram in Figure 8. In this setup, the 11th or 12th harmonic of the LO signal is used to mix down the RF signal of the working oscillators. Once again, the oscillator is biased through DC needle probes on the metalized side, and there is a silicon substrate lens on the opposite side. In this case, however, the signal is fed into a

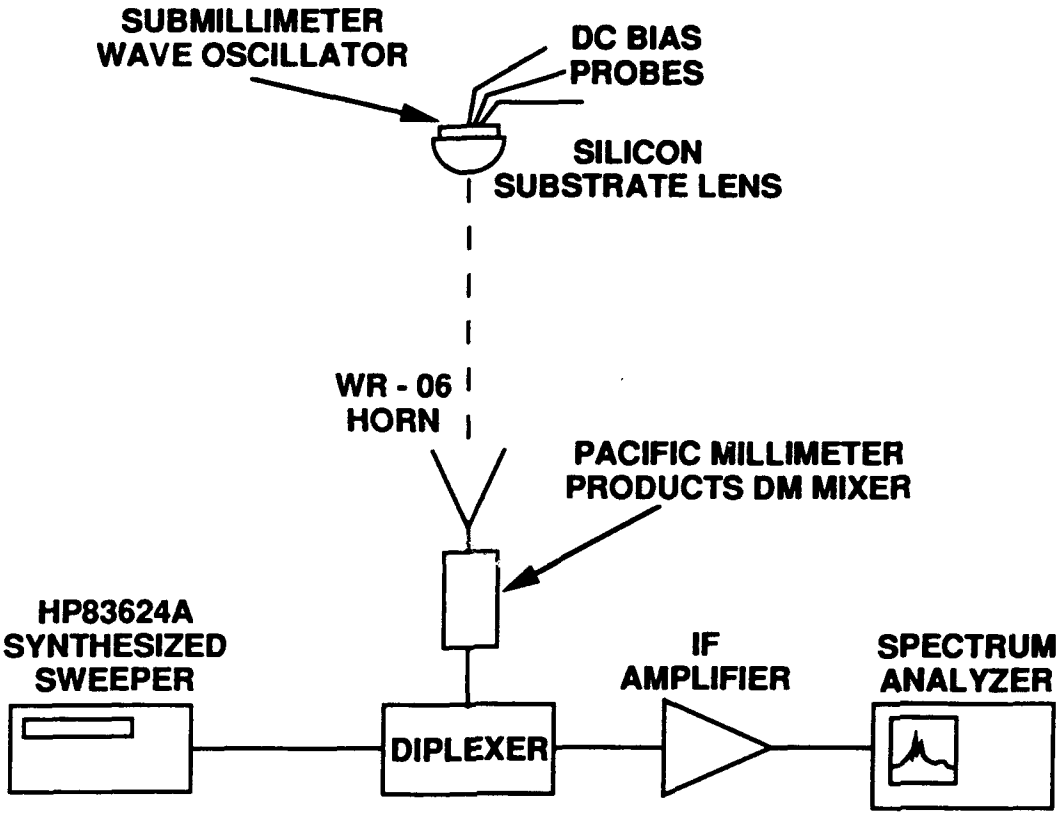


Figure 8. Coherent heterodyne detection measurement setup (11th and 12th harmonics).

waveguide horn rather than an interferometer. The signal is, in turn, fed into a mixer and then into a diplexer that is also fed by a synthesized sweeper. The resulting harmonic, the IF signal, is fed through an amplifier and into a spectrum analyzer. This technique enables one to see the spectrum of the oscillation.

Figure 9 shows the setup that uses the 3rd or 4th harmonic of the LO signal to mix down the RF signal of the oscillators. In this more complicated heterodyne setup, harmonics closer to the fundamental can be analyzed. As before, the oscillators are biased through the use of DC needle probes, and a silicon substrate lens is placed on the surface of the wafer opposite the circuits. The oscillation signal is reflected at a 90° angle towards a second optical lens. The signal passes through the lens and through a 45° wire grid beam splitter. The signal is, at that point, mixed with a three-times-multiplied signal from a synthesized signal source to produce an intermediate

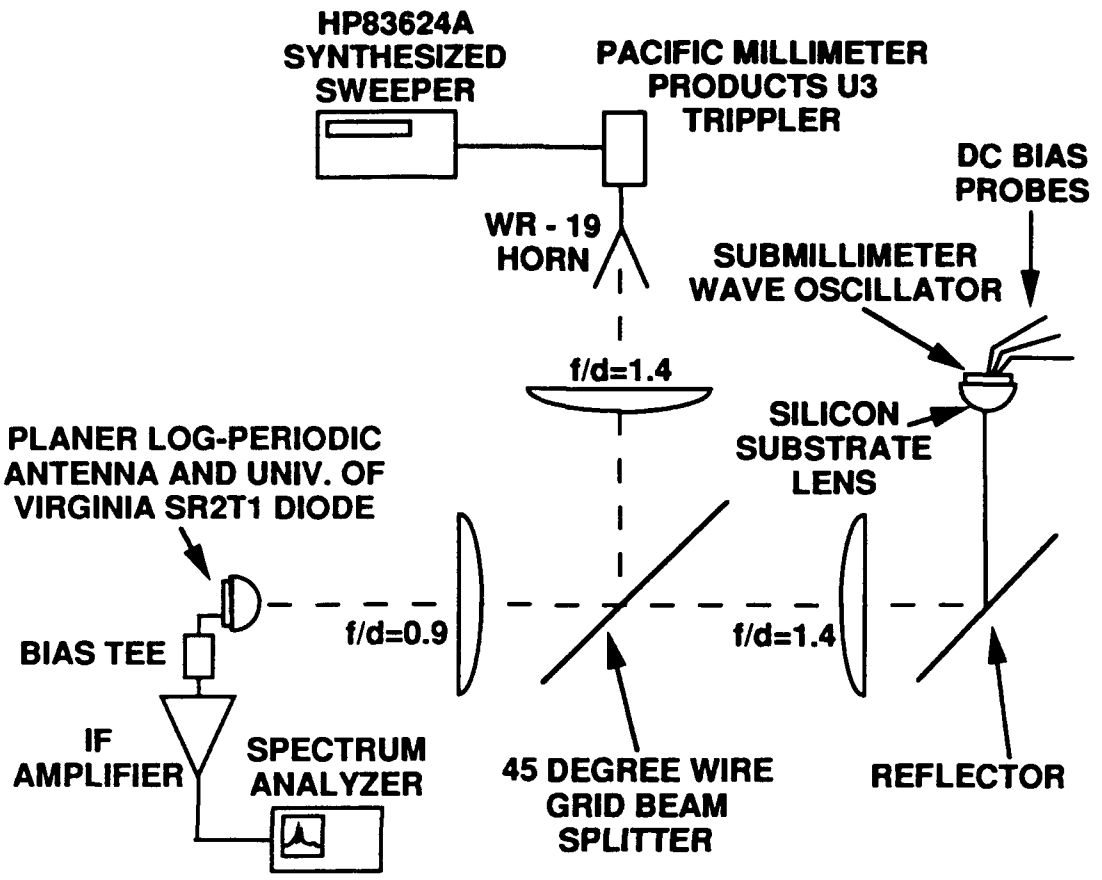
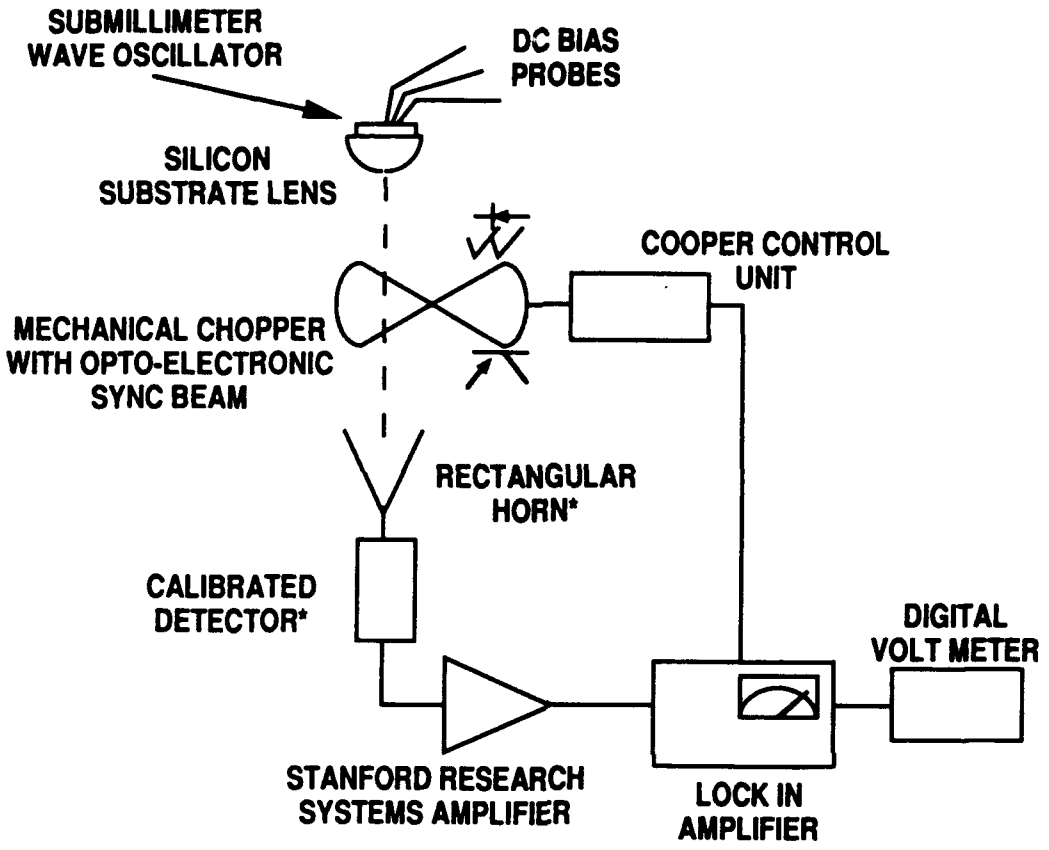


Figure 9. Coherent heterodyne detection measurement setup (3rd and 4th harmonics).

frequency (IF) at the third or fourth harmonic (depending on the frequency of oscillation). This IF then passes through another lens and is incident upon a planar log-periodic antenna that feeds a diode detector that is DC biased by means of a bias tee. The detector output is fed into an IF amplifier and then to a spectrum analyzer.

A method to determine the oscillators' output power, to first order, is also employed. The test setup is shown in Figure 10. The oscillators are mounted and biased as in the previous measurement setups. The signal passes through a mechanical chopper with an opto-electronic synchronization beam that is controlled by a chopper control unit and a lock-in amplifier. The signal is incident on a calibrated detector that feeds a pre-amplifier. The pre-amp in turn feeds the lock-in amplifier, whose output is read by a digital voltmeter. The detectors are calibrated against Millitech diode multipliers with known power output.



* AT 155GHz HORN IS WR-06 AND DETECTOR IS MILLITECH DXP-08
AT 210GHz HORN IS WR-03 AND DETECTOR IS MILLITECH DXW-03

Figure 10. Output power measurement setup.

Section 8
RESULTS

Our efforts on this program resulted in two world-record room-temperature three-terminal oscillator circuits. We found that circuits designed for operation at 150 GHz oscillated at approximately 155 GHz, and that circuits designed for 500 GHz oscillations operated at 213 GHz. To be sure there was no chance for error in the interpretation of the results because of an error due to the measurement technique, we measured each oscillator type using the three independent measurement setups described in the previous section. We found that the quasi-optical interferometer and both heterodyne techniques were each in agreement as to the actual fundamental frequencies of oscillation.

We used the interferometer technique to screen the wafers as to which circuits did and didn't oscillate. Table 3 shows the results of the complete scan of two wafers. The column marked "Design" indicates the type of design measured. The naming convention is described in the section of the report entitled, "Circuit Design." The second column, "Field," describes the circuit's position on the wafer. The column marked "Frequency" contains the frequency of oscillation, as determined by the interferometer technique. Finally, the last column notes the bias condition under which the circuit oscillated.

Once the working circuits were found by the above method, an independent method was used to verify the results given by the interferometer technique. Table 4 summarizes the results of this independent measurement by coherent heterodyne detection The two circuit types are shown in the first column of the table. The second column holds the synthesized source local oscillator (LO) frequency, which is used to mix with the oscillator (RF) signal. The harmonic number, in the third column, indicates which harmonic of the LO is being used to mix with the RF signal. For instance, the 12th harmonic of the LO signal is being used in the measurement in Row 1 of the table. The 12th harmonic is equal to 153.96 GHz, which when mixed with the RF oscillation frequency of 155.387 GHz, produces an IF signal at 1.427 GHz. The lower half of the table shows the fourth harmonic technique used to measure the 213 GHz oscillation.

Spectra of two representative measurements are shown in Figures 11 and 12. In the first, the 11th harmonic of a 14 GHz LO is used to mix with the RF oscillation at 155.373 GHz, producing an IF at 1.373 GHz, which can be seen in the spectrum analyzer display in the figure. The second figure shows that the 4th harmonic of a 52.916 GHz LO is being mixed with an RF oscillation at 213.07 GHz to produce a 1.41 GHz IF signal. The spectrum analyzer output of this measurement is shown in the figure.

Table 3. Interferometer Measurement Technique Results.

Design	Field	Frequency* (GHz)	Bias during oscillation Vg	Vd	Id(mA)
First Wafer					
150H10	4945	153.8	-0.0	0.89	4.3
	4946	152.8	-0.0	0.94	6.5
	4948	152.7	-0.3	1.00	8.7
	5045	153.4	-0.0	1.00	5.3
	5046	153.5	-0.0	1.00	5.4
	5146	154.8	-0.0	0.83	5.0
	5147	153.7	-0.0	1.00	7.1
	5148	155.0	-0.2	0.93	6.9
500H16	4947	219.6	-0.1	0.90	7.6
	5147	212.8	-0.3	1.17	5.4
	5146	osc begins	but dies out		
Second Wafer					
150H10	4946	152.4	-0.0	0.89	5.2
	5045	152.0	-0.2	1.00	6.0
	5046	152.0	-0.0	0.92	7.5
	5047	153.2	-0.0	1.00	4.5
	5145	155.9	-0.0	1.00	9.3
	5146	152.4	-0.0	0.87	5.6
	5246	153.0	-0.0	1.00	3.7
500H16	4946	210.1	-0.2	1.00	2.4
	5044	209.2	-0.4	1.10	7.8
	5046	211.6	-0.0	1.0	7.4
	5047	215.5	-0.03	1.10	3.0
	5143	210.0	-0.3	1.06	6.9
	5144	212.6	-0.3	1.07	9.9
	5145	212.2	-0.1	1.10	7.8
	5146	213.4	-0.1	1.10	4.9
	5245	203.0	-0.2	1.10	7.3
	5246	208.6	-0.0	1.10	4.4

Table 4. Coherent Heterodyne Detection Measurement Technique Results.

Oscillator	F_{LO} (GHz)	Harmonic Number	F_{IF} (GHz)	RF Sideband	F_{RF} (GHz)
150H10	12.830	12	1.427	Upper	155.387
(5047)	13.068	12	1.427	Lower	155.389
	14.000	11	1.386	Upper	155.386
	14.252	11	1.386	Lower	155.386
	14.036	11	0.995	Upper	155.391
	14.217	11	0.995	Lower	155.392
500H16	52.928	4	1.4117	Upper	213.124
(5048)	53.631	4	1.4117	Lower	213.112
	52.9766	4	1.2067	Upper	213.113
	53.5887	4	1.2233	Lower	213.131

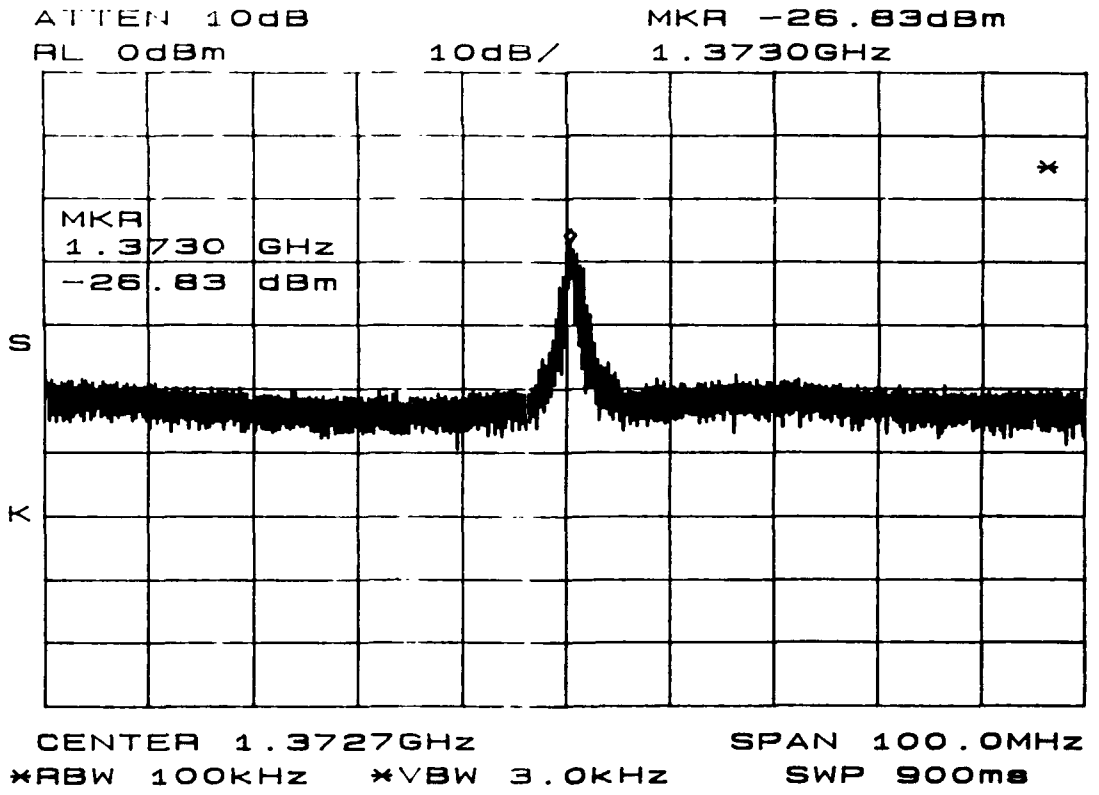


Figure 11. IF spectrum of 213 GHz oscillator.

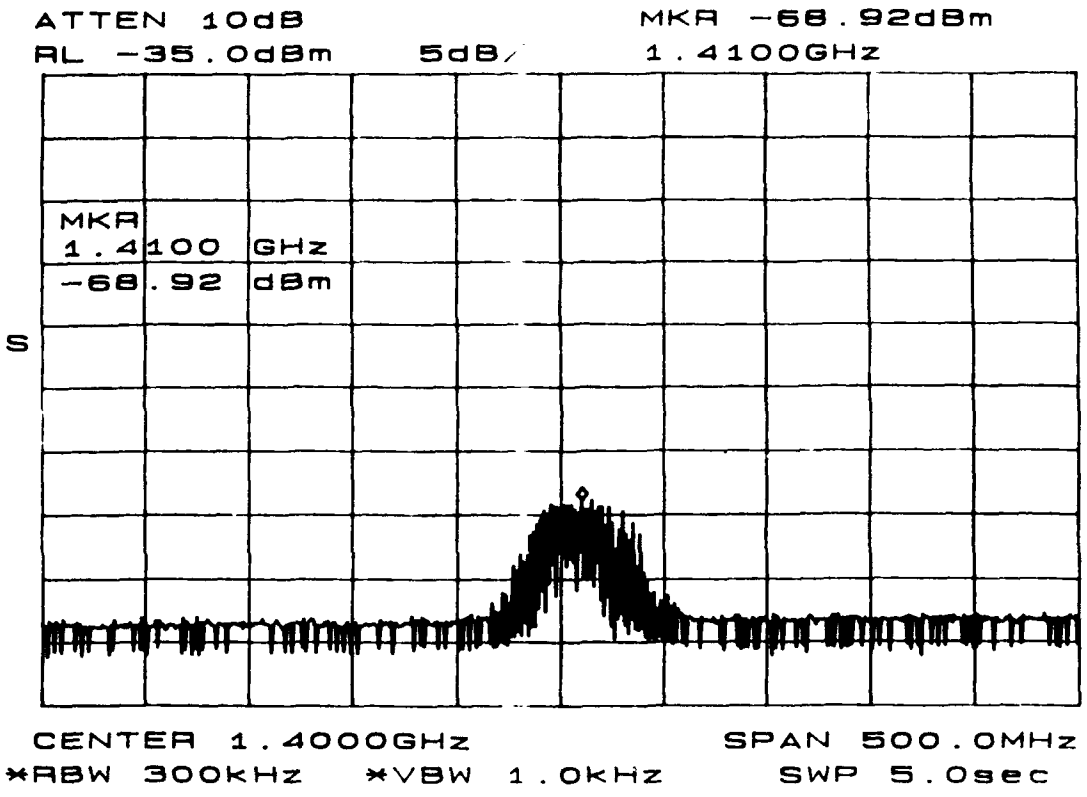


Figure 12. IF spectrum of 213 GHz oscillator.

Finally, a method was incorporated, as described in the previous section, to determine the output power of the oscillators. Since the measurement technique is not precisely accurate, we are reporting only that the powers are *not less than* the given values. The actual output powers may be as much as 3 dB (twice as much) higher than the results reported here. The output power of the 155 GHz oscillator is a minimum of 10 μW. The output power of the 213 GHz oscillator is a minimum of 1 μW. Additional work in this area must be done to more precisely determine the output power of the oscillators.

Section 9
CONCLUSIONS

This program has resulted in world record achievements in the areas of high frequency devices, integrated circuits, and integrated antenna design. We have demonstrated integrated three-terminal oscillator circuits that operate at what are believed to be more than twice previously published frequencies. The program brought together the disciplines of material design, device physics, sub-micrometer fabrication, transistor modeling, submillimeter-wave circuit design, planar antenna design, and quasi-optical circuit and measurement techniques in a real and intimate way. We were able to show that InP-based HEMT technology can be used at much higher frequencies than presently. For instance, since the HEMT is capable of oscillation at 213 GHz, it can also be used to amplify signals at that frequency. Additional time spent on the modeling of these transistors could lead to better circuit designs that will enable this same technology to yield oscillators at 300 GHz and above. Improvements in the technology will result in eventual frequencies of oscillation above 500 GHz.

This program also demonstrated how a mutually beneficial team consisting of government, industry, and higher education can work together to achieve world-record results in high technology. Certainly the program could not have succeeded were it not for the integral parts played by the Air Force, Hughes Aircraft Company, and the University of Michigan. We at Hughes Research Laboratories look forward to future successful programs with the talented members of this team.

Finally, we believe that this is only the beginning of exploration of the use of this technology at submillimeter-wave frequencies. Certainly there is a large variety of work to be done to further understand the mechanisms and possibilities that were uncovered by this program. We look forward to the positive consideration of this technology for future work in this area.

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APPENDIX
PUBLISHED PAPERS

The following papers, describing work funded by this contract, were published. The paper, "50-nm Self-Aligned Gate Pseudomorphic AlInAs/GaInAs High Electron Mobility Transistors," by L. Nguyen, et al. was selected for the IEEE Electron Devices Society's 1992 Rappaport Award as the best paper in an EDS publication during 1992. The award letter is attached.

1. S.E. Rosenbaum, L.M. Jelloian, A.S. Brown, M.A. Thompson, M. Matloubian, L.E. Larson, R.F. Lohr, Brian K. Kormanyos, G.M. Rebeiz, and L.P.B. Katehi, "A 213 GHz AlInAs/GaInAs/InP HEMT MMIC Oscillator," IEDM Conference Proceedings, Dec. 1993.

2. L.E. Larson, "The Effect of Intrinsic Parasitic Elements and Measurement Accuracy on the f_T, f_{MAX} and Equivalent Circuit Elements of Millimeter-Wave Field-Effect Transistors."

3. B.K. Kormanyos, W. Harokoupos, Jr., L.P.B. Katechi, and G.M. Rebeiz, CPW-FED Slot-Oscillators for Power Combining Applications."

4. B.K. Kormanyos and G.M. Rebeiz, "Active CPW-FED Slot Antennas for Power Combining Applications," Third International Symposium on Space Terahertz Technology.

5. B.K. Kormanyos, W. Harokopus Jr., L.P.B. Katehi, and G.M. Rebeiz, CPW-FED Active Slot-Antennas, IEEE Trans. on Microwave Theory and Techniques, 1992.

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Michael S Adler
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April 23, 1993

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Dear Dr. Nguyen:

I am delighted to inform you that your paper, "50-nm Self-Aligned Gate Pseudomorphic AlInAs/GaInAs High Electron Mobility Transistors," which you co-authored with April S. Brown, Mark A. Thompson, and Linda M. Jelloian, has been selected for the Electron Devices Society's 1992 Rappaport Award as the best paper in an EDS publication during 1992. Since well over 500 articles are published each year in EDS publications, there is very strong competition for the Award and your publication has been selected over many outstanding papers. My congratulations on the excellence of your article.

The Award will be presented at the International Electron Devices Meeting, to be held in Washington, DC, at the opening session of the meeting, starting at 9:00 AM on Monday, December 6. The Award consists of $1,000 divided among the four co-authors, and a certificate for each author. I strongly urge you to attend the ceremony to receive the Award in person.

Please contact William F. Van Der Vort, Electron Devices Society Executive Officer, at 908-562-3926 for more details on the presentation of the Award and to let him know if you will be able to attend.

Again, my congratulations for having your paper selected for the 1992 Rappaport Award.

Sincerely,

Michael S. Adler

MSA/akh

CC: W. Dexter Johnston, Jr., EDS Vice President
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