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Electronic Design Automation, Inc.

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Final Technical Report



# An MCM Concurrent Engineering Software Tool Market Study

Reference ARPA Contract #MDA972-92-C-0022



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# **An MCM Concurrent Engineering Software Tool Market Study**

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## **Section 1 — Executive Summary**

### **Market Study Overview**

This Market Study has been developed for the Advanced Research Projects Agency (ARPA) under the DICE program contract number MDA972-92-C-0022.

This Market Study is focused on the concurrent engineering software technology developed under the DICE program that uses the Rensselaer Object Storage Environment (ROSE). Referred to as "CHOICE", this technology has been developed by the Microelectronics Computer and Technology Corporation (MCC) in cooperation with Harris Electronic Design Automation, Inc. (Harris EDA), the Harris Government Aerospace Systems Division of Harris Corporation (Harris GASD), and STEP Tools, Incorporated (STEP Tools).

### **Objective**

The objective of this Market Study, based on a survey of end-user requirements, is to determine how CHOICE could be further developed and then distributed to the commercial market.

To reach our stated objective, an assessment of the current CHOICE technology, how this technology could be positioned in the commercial Electronic Design Automation (EDA) market place, and a proposed product-market launch plan are included.

## Market Study Summary

The conclusions reached in this Market Study are based on a combination of inputs:

- A review and analysis by senior software developers of the CHOICE technology.
- Interviews with ARPA contractors who are developing complementary technology for concurrent engineering environments.
- End-user reactions to demonstrations of CHOICE.
- A commissioned case study report submitted by Harris GASD, describing their implementation of concurrent engineering methods for MCM design.
- A telemarketing survey of systems electronic companies who represent potential end-users.
- An analysis of the EDA software, MCM technology, and concurrent engineering markets.
- The technology and business experience of the Market Study Program Team.

These inputs are discussed in detail throughout this Market Study. They have been compiled, reviewed, and debated with the following criteria in mind:

- Determine areas where CHOICE could be enhanced and modified to provide functions that address the concerns that were indicated by the end-users.
- Propose a product positioning of CHOICE in the EDA market.
- Forecast the potential market for CHOICE and the estimated cost of introducing CHOICE to the commercial market.
- Propose a product launch plan.

## Summary of Conclusions

The data collected in this Market Study identifies a significant end-user demand for concurrent engineering environments for MCM software tools. The commercially available systems do not satisfy the end-users needs as indicated by the large satisfaction gaps for MCM design data categories in our telemarketing survey.

Access to chip data, bi-directional translation of data, neutral data storage, and data transfer standards were identified as the top four areas that are not being addressed in a satisfactory manner. Respondents to our telemarketing survey offered these comments:

*"(EDA) Vendors prefer using their own internal formats instead of establishing standards."*

*"Using existing standards for other product domains that don't meet MCM needs."*

*"Advent of STEP standards will require the delivery of STEP for MCM products."*

Regarding their MCM design environments:

*"Hasn't gone all too smooth."*

*"Not much there. Foundries just beginning to build kits."*

Regarding STEP/PDES:

*"Has the right information content, but not useful until vendors support it."*

Several technology areas must be enhanced to condition CHOICE, or a product derivative of CHOICE, to become a commercially acceptable product. The continued support of ARPA remains a critical aspect of any business plan. ARPA support and its endorsement of CHOICE will ensure that the technology is further developed, provide credibility for the technology, and will stimulate end-user involvement in the testing and evaluation of the technology.

The market opportunity is growing rapidly as systems electronic companies adopt MCM technology into their next generation products. The data collected for this Market Study strongly support a forecast for a doubling of MCM technology-related expenditures in 1994.

End-users of MCM design environments and tools have invested -- and continue to invest -- in the development of costly manual processes (in terms of time, money, and human resources) to compensate for the missing functions that are, or could potentially be provided by the CHOICE concurrent engineering environment.

CHOICE could further be developed to create a commercial-quality concurrent engineering environment that MCM design companies could employ in conjunction with existing MCM design tools and environments. Specifically, the areas suitable for further development include:

1. Further develop the CHOICE technology to commercial quality levels by adding test vehicles representing multiple MCM process technologies, version control functions, and security features.
2. Develop product models and EXPRESS representations for MCM technology selection, Design Kits, and manufacturing optimization.
3. Enhance CHOICE with the addition of the Design Integrity Management software that validates EDA data collected from multiple applications.
4. Enhance CHOICE by adding support of the EXPRESS models for standard data interchange formats including the Electronic Design Interchange Format (EDIF), the Logic Modeling Corporation (LMC) Die Information Exchange (DIE) Format, and the CAx Interface Alliance data definition for MCM Foundries.

5. Create a graphical, open applications programming environment that allows end-users the opportunity to customize the integration of the DICE environment with currently existing and future tool selections.
6. Enhance the concurrent engineering environment to include design-for-test, automatic test program generation, automatic test validation software and support for MCM diagnostic testing.
7. Integrate an MCM Design Optimization software that adds multi-level system floorplanning and partitioning within the CHOICE environment.
8. Integrate a parts-and-materials management application into CHOICE.
9. Enhance CHOICE to allow for the concurrent operation of electronic design simulation tools, thereby allowing for mixed signal and chip and MCM level simulation of complex circuits.
10. Integrate CAE applications, including multiple digital and/or analog simulation tools, to promote multi-level and mixed signal system simulation.

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## Section 2 — Market Study Background

This Market Study focuses on the need for a concurrent design environment for MCM software tools. We identify the features that could be supported based on our interpretation of the requirements and opinions of a select group of systems electronics specialists employed by some of the leading electronics systems companies in the United States.

The information collected during the course of this program includes both concurrent engineering environment issues as well as the functionality of individual MCM design tools. Our focus is on the concurrent engineering environment issues; therefore, we do not discuss development of individual MCM design tools in our conclusions. We ask the reader to not make an inference from this emphasis the importance of design tools versus design environments -- rather, the reader should assume that end-users have needs in both areas.

The data presented in this market study was derived from a variety of industry sources, including end-users of concurrent engineering technology, suppliers of database technology, MCM manufacturers, and industry consultants. Prospective customers involved in either the design or the manufacture of MCMs were identified by Harris EDA, MCC, and Harris GASD. This select list was contacted through telemarketing services and personal interviews. The information gathered from surveys and interviews was combined with available published information from trade journals, consultant's presentations, vendor literature, industry reports, and other market studies.

Subsequently, the conclusions reached by this focused Market Study were then carefully reviewed, discussed and debated by the Market Study Program Team, resulting in the generation of this document.

### Program Team

The Program Team included representatives from several companies. *Tony Mazzullo*, Vice President of Business Development at Harris EDA has acted as the overall Program Manager and Team Leader.



**The Program Team is comprised of the following individuals:**

**Harris EDA**

*Dr. Tom Benfey, Marketing Communications Manager*  
*Tony Casciano, Manager, Software Engineering*  
*Jacqueline Flanagan, Manager, Corporate Relations*  
*Chuck Gannon, Senior Software Engineer*  
*Dennis George, CAD Product Manager*  
*Kimberly Hayton, Marketing Specialist*  
*Robert Ingold, Product Marketing Specialist*  
*Vess Johnson, Director CAD Development*  
*Tony Mazzullo, Vice President of Business Development*  
*Kathryn M. Wise, Supervisor, Technical Publications*

**Harris Corporation Engineering Productivity Group**

*Bruce Kraemer, Manager Engineering Productivity*

**Harris Corporation GASD**

*Don Hege, Lead Engineer*  
*Tom Young, Associate Principal Engineer*  
*Lou Paradiso, Sr. Principal Engineer*

**Harris Corporation Marketing Services**

*Terry Beard, Senior Manager, Marketing Support*  
*Glenn Pertersen, Senior Manager, Marketing Support Admin*

**Microelectronics and Computer Technology Corporation (MCC)**

*Hector Moreno, Program Manager*  
*Shaune Stark, Member of Technical Staff*

**STEP Tools, Inc.**

*Dr. Martin Hardwick, President*

**The following individuals also provided significant contributions to the development of this Market Study.**

*Bill Bicknell, General Electric Corporate R & D*  
*Ray Fillion, General Electric Corporate R & D*  
*Charles Incavellia, General Electric Corporate R & D*  
*Tim Ryan, IBM Microelectronics*  
*Mark Eskew, Texas Instruments*  
*Tom Laliberty, Raytheon Company*  
*Linda Lapoint, Raytheon Company*

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## Section 3 — Description of Technology

In recent years users of computer-aided design systems want their application programs (tools) capable of exchanging information as seamless as possible. The reasons are obvious: less of their time, less of their effort, and more economical use of their software/hardware investment. In parallel, the Federal government launched the DICE - DARPA (now ARPA) Initiative on Concurrent Engineering - program five years ago to support the development of tools and methodologies that improve productivity in design and manufacture through the concurrent activities in those areas.

Multi-Chip Module (MCM) design could benefit a great deal from enabling concurrent technology for many reasons:

- 1) MCMs represent the cutting edge of system technology at this time; therefore, design and manufacturing processes are relatively new and can be changed easier than processes in place for older technologies.
- 2) The complexity of the design tasks is so great that several inter-disciplinary teams are necessarily involved.
- 3) As a result, many distinct computer-aided tools must be used to complete the design of one MCM.
- 4) In the most part, the tools do not work together well since they have been developed by different software sources, and lack a common software environment.

Because of the tools have not worked together well, people have had to adopt a serial MCM design methodology. With this process, each set of experts accepts the design from the previous team, and tries to make the MCM comply with the product specifications necessary for its particular area. Because the information flow is uni-directional, a problem in the design results in it being "sent back" to a prior stage in order to be fixed. This back-trackings usually negates most of the work done at intermediate stages. Worse still, the work that one group does to achieve its own goals often collides and interferes with the needs of a different group. For example, in order to achieve full testability with a given test approach, additional circuitry may be needed. However, additional circuitry may contradict the needs for speed and performance, or the requirements for size and weight important to other design teams.

With the concurrent design engineering approach, information flows between users of distinct design tools in a multi-directional way. Any changes and solutions that a group offers can be quickly evaluated by others and problems can be identified early and solved quickly. Thus the serial design approach is transformed into a parallel one, and the design process becomes centered on the data (information) itself, and not controlled by the available tools.

With this important point in mind, a research group at the Rensselaer Polytechnic Institute (RPI), offered a proposal to DICE to develop an engineering data management system, called ROSE (Rensselaer Object Storage Environment). The proposal has been funded through several phases of DICE, and ROSE

continues to evolve to this date. ROSE is now commercially supported by STEP Tools, Inc.

Along with the problems of serial information flow, engineering design methods must solve engineering data management problems that are much more complicated than the typical data management problems found in business. In business, the data is usually well defined in advance of its creation. For example, banks deal with depositors and borrowers. A depositor's or borrower's business information is accessed through a name, address, social security number, and account number. The business data records contain balances, payments, loans, dates, and interest. All customers, regardless of the amount of money they possess, require the same number of records for data storage and management. This data can be handled with relational database technology, normally fixed-length records organized for presentation in tabular form.

By contrast, engineering design produces data in seemingly random form and size. The layout of an electrical connection path, for example, can have any number of corners or bends in its physical implementation. An actual picture of the electrical connection is a much more useful representation of the data. Thus, engineering data is more efficiently and faithfully represented by software objects, which are encapsulations of data and software like the graphics software that makes the drawing of the path appear on the screen, rather than as sets of fixed length records.

ROSE serves as a vast software library of object manipulation and storage which can be used by the engineering applications. This object-oriented software can be reused in a straightforward manner, eliminating duplication efforts and debugging problems. For example, the graphics display software that an object uses may have been written in advance for a more generic type of object. In the same manner, data management software for a particular piece of data can be inherited from software written previously.

ROSE also helps to expedite the flow of information between customers and suppliers, designers and users of design information, while complying with international standards. The ISO and PDES/STEP organizations as well as the work of the EDIF committees and CFI demonstrate the great interest in sharing data. ROSE is compliant with the STEP norms as the structured objects it operates on are defined through the ISO/PDES/STEP EXPRESS language for information modeling.

### **CHOICE Technology Overview**

In 1989, MCC proposed to DICE to validate the ROSE technology through the creation of a concurrent MCM design environment. Implementation of the design environment required two phases:

1. Define an EXPRESS information model for MCM physical design data and validate it through ROSE and the bidirectional linking of several commercially available CAD tools.

In addition, the validation included the concurrent design of a commercial MCM.

This first phase was funded and resulted in the CHOICE technology which is the subject of this market study.

2. Expand the concurrent design environment to include and validate other design aspects such as logical, electrical, mechanical, thermal modeling and simulation as well as design-for-test.

This second phase, although approved in principle, has not yet received funding.

### **Description of the CHOICE Technology**

There are two basic types of entities needed to represent MCM physical design data:

- Geometric information entities.
- Connectivity information entities.

Our method first examined what data types were required by a system which is predominantly used for layout since we expected these types were common among all the systems to be integrated. Then we determined which types were necessary to complete the picture for systems with connectivity intelligence. Each of these identified types was defined as an abstract entity. We expressed the information content through the interrelationship among all the entities. We codified this interrelationship, known as the schema, with the EXPRESS language and included the following geometric entities:

- Cells
- Mosaics (Arrays)
- Cell Instances
- Geometric Primitives
  - Paths
  - Rectangles
  - Polygons
  - Lines
  - Points

The connectivity entities were:

- Element-pin pairs (elPin)
- Nets

## EXPRESS Model Implementation

Figure 3.1 shows four physical design CAD systems and two ROSE implementations for two different information models: the CHOICE SYSTEM introduced in the previous section and one that implements the Initial Graphics Exchange Standard (IGES). IGES is a very general, three-dimensional standard that represents graphical information and was quite cumbersome for our purposes. However, we found it necessary to work with IGES because systems such as Allegro 6.1 (PCB-oriented tools) often accept IGES representation of graphical data as input, without providing many other acceptable means to reliably input data from external sources, and do not provide a procedural language to read or write to its internal data. (Allegro 6.1 is also capable of writing out its layout design data in IGES form.)

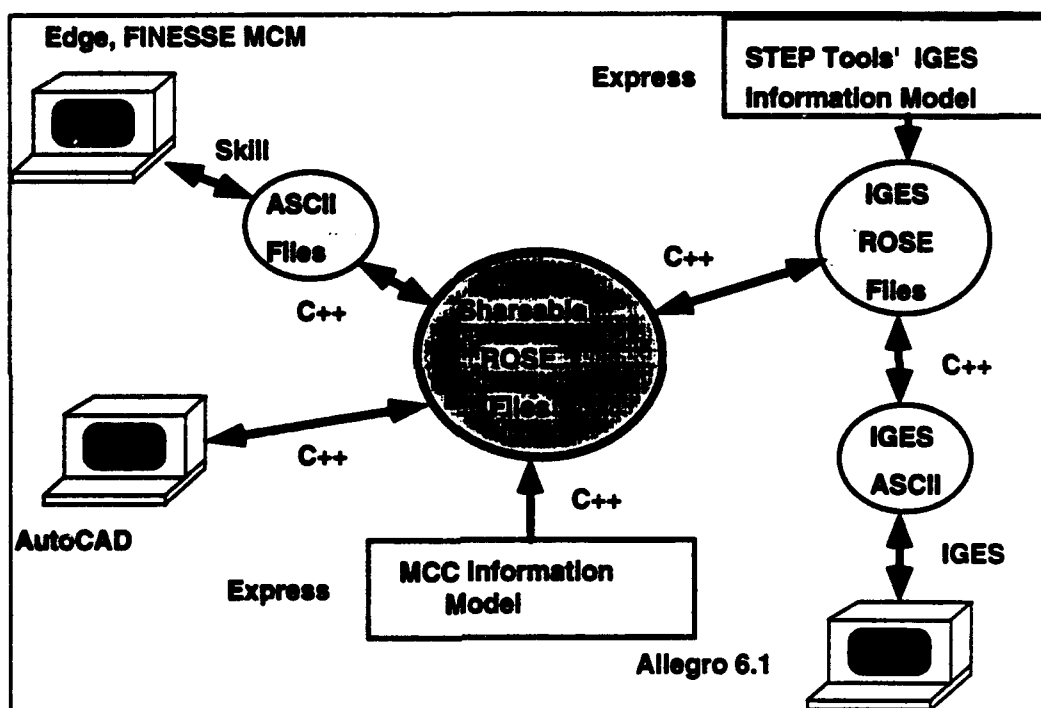


Figure 3.1. Architecture of the CHOICE system.

AutoCAD implements a more direct link between the MCC information model and its own internal format by using a direct C procedural access to its database; this provides a direct link for data exchange. AutoCAD reads from and writes to ROSE data directly, without an intermediate format, simply by loading the C language interface that MCC has written using AutoCAD's "AutoCAD Development System" (ADS) tool.

The two information models, MCC's and IGES, were written in the EXPRESS language. Software tools from STEP Tools, Inc. were then used to compile those models into C++ classes. ROSE also provides methods to create the class instances, to relate them according to the schema and to

manage them. In addition, we mapped the ROSE objects created under one model to objects created under the other through C++ ROSE code, thereby integrating Allegro into CHOICE.

The link between Edge/Opus and ROSE is achieved through an intermediate text form. Data goes in and out of Edge/Opus via software written in Cadence's SKILL language, which allows read/write access to Edge/Opus' internal data structures. The link to ROSE was completed through a parser written in C++, which reads the intermediate form and creates the (C++) objects that implement the EXPRESS layout information model. In the opposite direction, C++ software navigates through the ROSE objects and creates the intermediate form description, which is then read by the Cadence SKILL code.

The FINESSE MCM system was linked to the ROSE database through an intermediate text file form called a *dfile*, a standard textual database description form that FINESSE MCM supports and can be read back to recreate the FINESSE MCM database through that tool's command stream. Our original intention was to integrate FINESSE MCM in a direct fashion, without an intermediate text form, since Harris EDA owns the source code for FINESSE MCM. However, Harris EDA determined that such a route would take more time and resources than those allowed by our project. The link through the *dfile* was developed very much like the Cadence Edge/Opus link.

#### Operation of the Concurrent Engineering Layout System

Figure 3.2 illustrates the operation of the system.

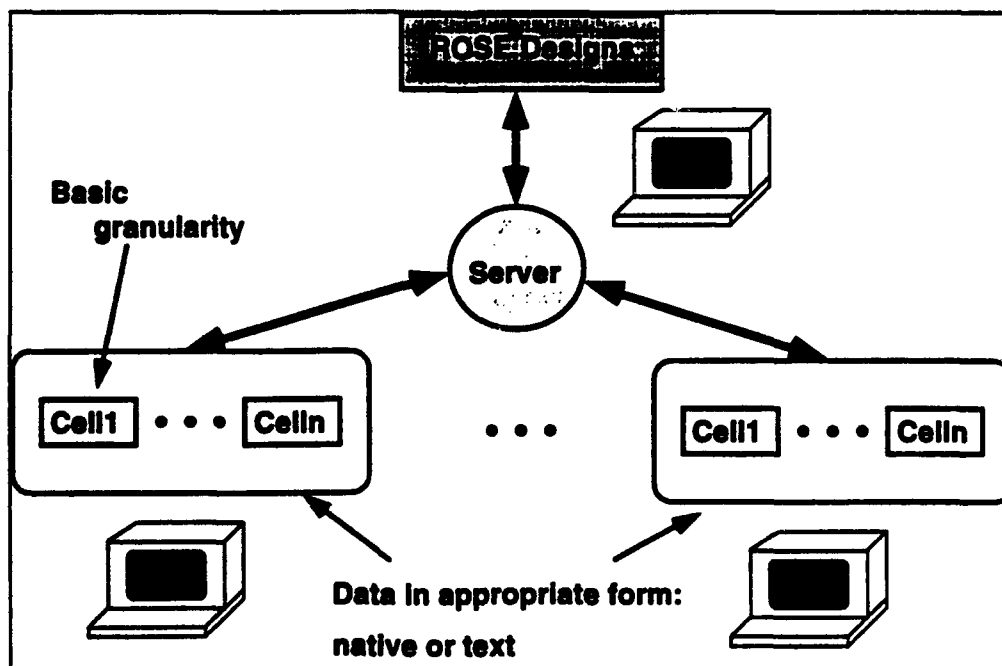


Figure 3.2. CHOICE system operation.

The basic object that is managed by ROSE is the cell, and any transaction between a user and the system involves at least the transfer of a complete Cell entity. That implies that layout designers must organize and structure data, limiting the size of individual cells so transfer of data relatively simple. Good data structuring, always a good practice regardless of concurrent engineering requirements, is essential with ROSE since all users of the system must be informed of every change. ROSE in and of itself does not require cells as basic exchange entities. However, from a practical point of view, defining the exchange granularity at a lower level, could produce a prohibitively large amount of network traffic due to the vast number of minute changes that the design team may make. This would trigger corresponding ROSE database searches for the objects being modified, added or deleted. Since the natural unit of work in layout is the cell, it is equally natural to use it as the transaction unit. The ROSE data then is updated only when the designer finishes a sizable amount of work. This approach also eliminates the need for database searches for individual objects, as the whole cell gets updated every time. However, the cells should remain small so updates are completed more quickly.

Every cell entity is stored as an individual ROSE design on one dedicated workstation with efficient disk access. The user invokes a custom server to update the other workstations in the network

When a designer receives an update, the system automatically backs up the designer's current working design. This enables the team to assess the update and either accept or reject the change. The team works together to determine whether the update is immediately acceptable, whether it should be modified, or whether the current working design needs to be modified to support the update. The automatic back-ups enable the team to return the design to previous stages, if that is the consensus.

### **Saving and Updating Information**

After completing work on a cell, the designer saves it to the local CAD system database and also invokes the ROSE server to receive the data and create the ROSE description of the cell. Because the server uses a different workstation, the designer experiences a minimal downtime when saving the cell to the ROSE environment. Since the cell updates are not occurring frequently, the network traffic is minimized. Once the cell has been stored as a ROSE design, the ROSE server translates it to all the other formats necessary to update the other CAD systems.

### **Special Considerations**

Internal database of certain CAD systems use a minimum of hierarchy. Essentially, these systems, which have evolved from Printed-Circuit Board layout applications to the MCM domain keep "packages," "pad stacks," and "boards" as basic entities. A board describes the MCM itself and contains packages and interconnect. The packages are built out of pad stacks and other geometric and electrical information. These systems,

usually very useful to complete the routing portion of the MCM layout task, but they are not especially suited to handle large amounts of data, particularly certain MCM technologies which customize the MCM substrate starting from a generic, prefabricated part which is customized in the last stage of manufacturing. Such parts are mass produced ahead of time and contain a great deal of interconnect which will not be used by the personalization step. (Usually only about 60 percent of available interconnect density are actually used for those substrates). In such cases, the part should be described completely in a hierarchical CAD system.

If a non-hierarchical CAD system is used for the routing in a concurrent engineering approach, only pass the placement information and the netlist, and then to store the interconnect generated back into ROSE. Alternatively, if designers can work effectively in the non-hierarchical system with all the MCM data, they should not store back into ROSE the full design after routing since that would create a flat and large cell containing all the layout data. In any case only the result of the interconnect (routing) step should be stored in a new cell, which will be shared by all the concurrent engineering environment designers. Furthermore, if designers can complete interconnection using a sequence of smaller tasks, they should store the results of each of those tasks as independent cells.

In other cases, all members of the design team might collaborate in defining the basic packages and their placement, and then they would submit the interconnect task to the non-hierarchical system (or systems) as the last step of the layout design.

### UNIX Server

To integrate the users of the concurrent engineering environment, we implemented a mechanism by which the UNIX system will automatically update and distribute the changes to the ROSE database. Essentially, all users have their own usual working environment, but in addition have two extra directories: incoming and outgoing. To update the ROSE database, the user saves the work to the outgoing directory. Once the server is invoked, the directory is "moved" or renamed to a predetermined location, periodically inspected by the UNIX server. If the server finds data there, it makes a backup copy and performs all necessary manipulations to change the new data into the CHOICE form and, from there, translates it to all other integrated systems. Since the server runs independently, the designer is not affected by the server's activity. Typically the server is a SPARCStation 10 with 50+ Megabytes of memory and enough storage space depending on the size of the database and number of designs being managed.

Once the translations are complete, the server copies the ROSE database to a directory and creates a backup copy of the previous data. Because all users and their CAD system types are registered in a special file the server



reads, the server distributes a copy of the translation in all users' incoming directory. Users inspect this directory and evaluate the change.

If the changes are acceptable, users update their designs, move the file in the incoming directory to another location, and prepare to receive any other updates in the incoming directory. If users don't accept or agree with the changes, they must communicate with other design team members and determine how to proceed. Backup copies of the design exist and can be reinstated. Or the designers critical of the change may have to alter their own data and submit it again to the server.

The current server mechanism is an interim solution. Ultimately ROSE needs both a database version control and a design checking/locking mechanism. Once these features are available, the server can invoke them on behalf of the user who is submitting the change or requesting a specific piece of information or version of the data.

### **DDR2 Parts and Netlist**

DDR2 (Digital Drop Receiver, Version 2), the module we designed concurrently with the CHOICE system, is owned by Harris Corporation. The parts were designed using FINESSE MCM and the netlist had been entered into the FINESSE MCM system. From there, that information was made available to the other CAD systems through the ROSE database and the CHOICE system.

### **Installing and Supporting the System at Harris Corporation**

In October, 1992, a team of four software developers, three from MCC and one from Harris EDA, installed the system at Harris Corporation in Melbourne, Florida. There the team translated the DDR2 placement and netlist from Harris EDA's FINESSE MCM to the Allegro 6.1 system, since these two CAD systems were the relevant design systems at Harris Corporation. After the demonstration, Harris Corporation designers used the system to pass information between FINESSE MCM and Allegro for other MCM applications.

### **Concurrent Engineering Design Experience at MCC**

In order to validate the concurrent engineering design environment provided by the CHOICE system, MCC completed a design of the DDR2 Harris module. MCC took the parts description, placement and netlist from the database that Harris delivered in FINESSE MCM form. The ROSE database was created and the Cadence Edge/Opus system read it in. The footprints of the chips and the module I/O were then modified to allow for automatic redundant routing by judicious modification of the padstack definitions. The placement data and the netlist were then read by the Allegro system and routed. The Allegro system also created the power and ground plane data. The routed Allegro database was then sent back to the ROSE database and read in by the Cadence Edge/Opus

system, which was then used to replicate the signal and power/ground layers.

The via entities were also redefined in the Cadence Edge/Opus system to have geometric elements in the normal as well as the redundant routing layers. The replication step is trivial in the Edge/Opus system but not in the Allegro or FINESSE MCM systems.

MCC also wrote special verification software aids to take the netlist, chip placement, and netlist information residing in the ROSE database and then generate a text file whose records list the net names followed by the absolute x- and y-Cartesian coordinate location of the chip and module I/O pins corresponding to the listed net name. Such a text file is read into the Cadence Edge/Opus database using the SKILL language and the corresponding net names written as labels into the native Cadence database in a chosen layer at the x-, y-location recorded in the text file. The software verifying Edge/Opus connectivity depends on this annotation. Through simple textual editing operations on the text file, it is possible to derive a corresponding text file for the redundant net names, which are then also input as labels into the Edge/Opus database (in a different layer than that used for the normal net names). Through straightforward graphical operations, the labels are moved to desired locations on the redundant pads and then moved to the same layer as the normal net name labels. At that point the Edge/Opus database is ready for full connectivity and design rule verification.

This exceedingly powerful design method allows us to perform operations that normally are not allowed in connectivity-based systems, but which are very desirable. Those "forbidden" operations, such as adding layers, replicating design data, adding connections not listed in the original netlist, are practically trivial in the Edge/Opus system. Through the tool integration and verification process, we are assured of the integrity of the design.

In our experiment, we obtained a fully verified database suitable for manufacturing in four designer-days. The design rules used were those of MCC's QTAI thin film MCM interconnect process. In comparison, the same design when processed through the standard non-concurrent approach takes one designer-month of effort. These factors contributed to the time savings:

- 1) The ability to use and re-use previously designed data elements. In our case, we used the chip and module I/O footprint definitions contained in the initial FINESSE MCM database. The reuse of data eliminates transcription errors and saves a great deal of design time.
- 2) The ability to use the best features of each and every integrated tool.

## **Standards considerations**

Standards organizations have special interest in setting up tools, application protocols, information models and guidelines to facilitate the transfer of information among different parties. The DICE program from which the CHOICE environment has evolved is compliant with the PDES/STEP requirement to have the data conform to an EXPRESS information model. After the first phase of the project has been completed, this study appears to indicate that there is renewed interest in evolving the environment to encompass a promising emerging standard information model for PCB data which is being developed by the EDIF PCB committee. In addition, the ongoing coordinated efforts between the PDES/STEP AP210 working group, the EDIF community and the CFI promote integration and further research. The ARPA-sponsored ASEM CAD Alliance project at MCC is actively working with all these groups in extending the PCB information model to the MCM realm. As the CHOICE technology moves into its projected commercialization stage, it will continue to evolve and will adopt the chosen information model standard.

## **Rensselaer Object Storage Environment (ROSE)**

ROSE is a system that allows applications written in object-oriented programming languages to interact directly with databases that have been defined using the EXPRESS modeling language. Different ROSE systems are available that support different object-oriented programming languages. For example, ROSE++ is a class library for C++ applications [Hardwick 92].

In order to evaluate the ROSE database system we must look at several features of the system including:

- Logical Database Architecture
- Data Definition Language (DDL)
- Tools Built On the Database System
- Work With ROSE

### ***Logical Database Architecture***

ROSE is built using an object-oriented database architecture. This architecture is well suited for modeling design data and is actually capable of capturing more semantics in the database than other database models. In order to understand what the object-oriented architecture provides we should consider how this compares to the more common relational architecture.

### ***Relational Database Architecture***

Relational databases arrange data in a collection of relations, each of which is represented in a tabular form that is easily understood [Date 86]. The rows of a relation or a table are called tuples, while columns are called attributes. In the

relational model, entities and relationships between entities are both represented in the same way - as a relation.

Relational databases are extremely good for performing ad hoc queries. For example, consider the part table in Figure 3.3. In the PARTS table queries listing all the sources for particular package type seems quite natural. The database structure lends itself well to generating queries that perform directed searches over well defined combinations of relations. This capability may indeed make relational databases very well suited for the maintenance of library data.

Company:_____			
Part Number	Manufacturer	Package	Material
7400-1	JK Semi	14-DIP	Plastic
7400-2	JK Semi	14-DIP	Ceramic
7400-3	JK Semi	20-FP	Ceramic
7400-4	SJ Semi	14-DIP	Plastic
7400-5	SJ Semi	20-FP	Ceramic

Figure 3.3. PARTS Table

In the relational model there is no method for storing explicit links between the data items. As discussed earlier the relational architecture makes use of the relation as its principle data structure. Hence, while performing ad hoc queries may be quite intuitive, database traversals can be quite complex. Although the relational model can handle queries centered around focused entity types (e.g., what is the resistance value for the part with part number R12345), queries concerning entities related to other entities could present a problem (e.g., which nets are the pins on component U1 connected to, what component is above component U1).

However, this lack of explicit links between the items in multiple relations is not always a weakness. The relational database architecture also provides a high degree of data independence. The data in the database is not restricted to particular location since there are no predefined access paths or explicit links. Less emphasis is placed on the actual location of data within the database than that found in other database systems therefore fewer problems may be encountered during database restructuring.

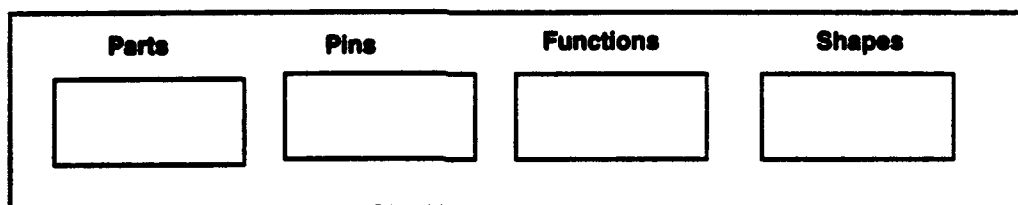
Another important aspect of relational database architectures is the maturity of the technology. Maturity of a technology can bring with it some significant advantages, for example:

- Relational database systems have been in use for a long period of time and there have been a large number of tools being built on them in many diverse problem domains.
- Relational database management systems are quite robust in areas such as concurrent processing, transaction processing and security.
- Standard query languages have been defined and agreed upon. Moving from one relational database systems to another may pose a minimal impact.
- Interoperability in relational database environments is nearly a reality. This is not meant to imply application interoperability. Rather, data that is defined in one relational database system can be accessed from another relational database system of a different type.

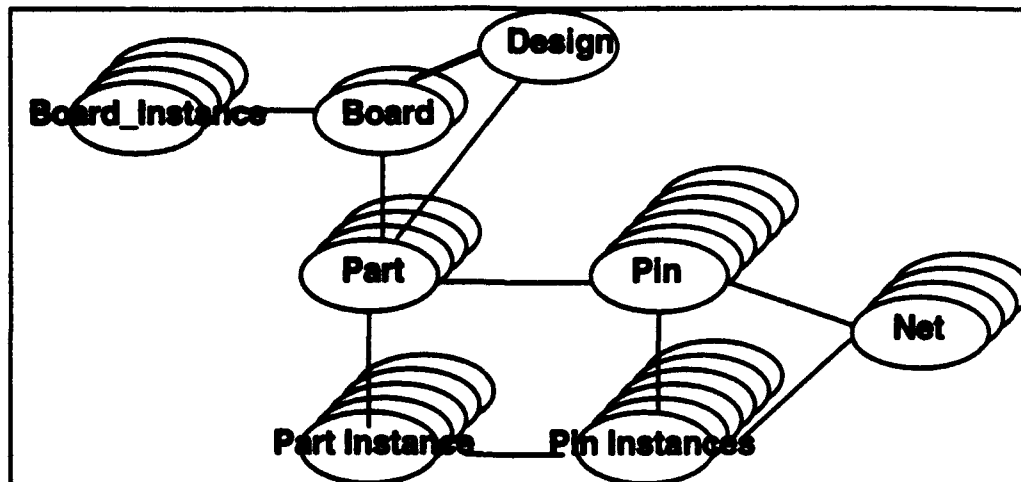
### ***Object-Oriented Database Architecture***

Object-oriented databases are based on the notion of objects and the relationships between objects. This architecture is a move toward more of a traversal oriented database architecture where less emphasis is placed on the ad hoc query structure. Object-oriented databases attempt to capture more of the semantics of the data being modeled as well as semantics about the entity interactions, unlike the CODASYL network databases which are also traversal oriented

Relational database systems can be viewed as modeling data in a flat tabular view with multiple entry points for data retrieval. While object-oriented database systems on the other hand can be viewed as modeling large complex networks of interconnecting objects and entities with fewer well defined entry points for data retrieval. Where the relational database is good for the library definitions of entities, envisioned as lookup tables, the object-oriented database is well suited for design databases with many interconnected design entities or objects (Figures 3.4 and 3.5).



***Figure 3.4 Objects***



**Figure 3.5. Objects and Explicit Links**

The maintenance of explicit links between entities in the database allows the application to efficiently traverse through the database. These explicit links also reduces the amount of data independence. Now the database structure is much more stressed and relied upon that may make structural redesigns more difficult.

One area of concern for object-oriented databases is the maturity of the technology. There are few standards currently available that allow for data to be transferred between different systems. Also, in many cases moving from one object-oriented database system to another requires considerable effort in moving the data and in learning the new system.

However, there are standard committees that have been active now for some time addressing these concerns. This concern is continuing to fade as it ultimately did with the relational database technology.

To say that one database architecture in all cases is superior to another is quite inappropriate. The relational database architecture is positioned well and it is clearly the tool of choice when the application domain is appropriate. The object-oriented database architecture, similarly, has strengths that position it well for the appropriate application domain. For the maintenance, interchange and manipulation of design data the object-oriented database architecture is currently the architecture of choice.

### ***Data Definition Language (DDL) and EXPRESS***

The Data Definition Language is the language used to define the logical structure of a database [Loomis 87]. This is sometimes referred to as the "schema definition language".

Most database management systems in use today, including most relational database management systems, use proprietary DDL's. There are efforts underway by commercial relational database vendors to standardize the DDL's in the database community; however, this work is not complete. Hence, the migration from one database system to another can be quite challenging.

One of the most important aspects to the ROSE database is its use of EXPRESS for its DDL. EXPRESS is an extremely powerful modeling language for engineering design data. EXPRESS describes data structures as well as the constraints that must be met by instance of those structures. The EXPRESS language is object oriente and definitions can inherit from one another.

The EXPRESS language is included in the ISO 10303 PDES/STEP Standard (ISO 10303-11). Part 21 of the standard describes the STEP file format. Part 22 of the standard, the STEP Data Access Interface (SDAI), defines Application Programmers Interfaces to share the data. Also part of the standard are application specific data exchange protocols called Application Protocols. Application Protocols are normalized database definitions, written in EXPRESS, that allow many different applications to share data. The STEP standard has reached Draft International Standard (DIS) status. This means that the STEP development process has been validated, along with 2 Application Protocols (201 and 203). Some other Application Protocols under development include:

- AP210 - Electronic Printed Circuit Assembly: Design and Manufacture
- AP211 - Electronic Printed Circuit Assembly: Test, Integrated Diagnostics and
- Remanufacture

EXPRESS has been accepted by other standards groups, such as EDIF, as the modeling language of choice. Since EXPRESS is such a widely accepted form for representing complex engineering schemas and since many of existing standard data formats have EXPRESS representations already defined for them, this makes the task of moving those schemas into ROSE easier.

This tight integration between an accepted engineering data modeling language such as EXPRESS and an object-oriented database has the potential to provide an environment of interoperability for both MCM end-users and MCM design tool vendors.

### **Tools Built on the Database System**

Through STEP Tools there have been a variety of tools build to aid in the development and manipulation of databases built on ROSE. EXPRESS compilers, translators and editors. STEP editors, browsers and conformance checkers. IGES, DXF and ACIS Translators. ORACLE, ObjectStore, Versant and HP OpenODB database interfaces are commercially available. There is also a database manager for AP203 and versioning tools available from STEP tools, a necessary element for concurrent engineering, all with the intent of providing a superior engineering/database development environment.

## **CFI Overview**

The CAD Framework Initiative (CFI) was formed as a not-for-profit industry consortia in 1988. CFI is an international, market-driven organization whose mission is to define interface standards that facilitate the integration of design automation tools and design data for the benefit of end-users and vendors worldwide. Within CFI, a broad spectrum of international EDA (Electronic Design Automation) users and vendor companies collaborate to identify the industry's most pressing integration requirements.

From these requirements, CFI members identify relevant existing standards, define new areas for standardization, and work cooperatively to develop specifications for the most urgently needed integration interfaces. CFI plays a pivotal role in moving the EDA industry toward the ultimate goal of seamless "plug-and-play" assembly of EDA systems by championing the inter-operability and interchangeability of EDA tools through common framework interface standards.

CFI membership consists of over 41 major corporate users of design automation products, computer system manufacturers, vendors of integrated design automation environments, and design tool developers, as well as government, research, and academic institutions in North America, Europe, and Asia. CFI corporate headquarters is located in Austin, Texas.

## **CFI 1.0 Standards Support**

The ultimate functional goal of CFI is to provide an easy to use interchange of individual EDA tools in a standards-compliant framework and enabling all these tools to interoperate in the framework. To achieve this ambitious goal, CFI released the Version 1.0 Standards in January, 1993. The 1.0 Standards address the following key areas:

- Design Representation
- Inter-Tool Communication
- Tool Encapsulation Specification
- Computing Environment Services

## **Overview of Design Representation Standard 1.0 (DR 1.0)**

The 1.0 Design Representation Standard defines an information model and programming interface for netlist manipulation. DR 1.0 provides a common methodology for standard-compliant EDA tools and databases to represent, access, and manipulate electrical connectivity information. The number of individual interfaces among CAE tools required is expected to be dramatically reduced with industry-wide support for CFI's DR 1.0.

A designer using DR 1.0-compliant tools should be able to mix-and-match tools without having to worry about writing and debugging point-to-point netlist translators, since all of the tools share a common information model and programming interface. Tool integration at the netlist level becomes much simpler and less expensive for both users and vendors.



### **Overview of Inter-Tool Communication Standard 1.0 (ITC 1.0)**

The 1.0 Inter-Tool Communication Standard defines a standard programming interface and information model which defines the functionality required for passing messages and information from one CAD tool to another. More recently, there has been a collaborative effort between CFI and Sun Microsystems to address the possibility of replacing the ITC 1.0 Standard with *de facto* standard of Sun's ToolTalk communications manager. This represents a very positive activity, since this same combination was showcased in another CFI-sponsored pilot project at DAC '92. Irrespective of the final decision, design tools which conform to the ITC 1.0 Standard can communicate with other standards-conforming tools via a message server. With a standard mechanism for communicating among tools, interoperability and data interchange will become much simpler for concurrent process information sharing and feedback among tools.

### **Overview of Tool Encapsulation Specification 1.0 (TES 1.0)**

The 1.0 Tool Encapsulation Specification provides a set of format standards for information required to encapsulate CAD design tools into a single, consistent CAD framework. Given this TES Specification, tools from a variety of vendors can be incorporated and invoked in a consistent manner. Framework tool-users won't have to be concerned with tool location, command syntax, or arguments required to invoke the tool. All this information is captured in each tool's respective encapsulation, allowing the user to concentrate on the design process rather than tool details.

Tool encapsulation simplifies tool integration, since each specification-compliant tool conforms to a standard encapsulation, which the tool-user or vendor can reuse when integrating with any additional CFI-compliant framework.

### **Overview of Computing Environment Services Standard 1.0 (CESS 1.0)**

The 1.0 Computing Environment Services Standards address base system services, system network services, user interface guidelines, extension languages and error-handling. Defining standards for platforms and networks makes moving and interoperating tools and frameworks across platforms much simpler and less expensive. This standard is intended primarily for framework vendors. Integrators within each of the various vendors' frameworks will benefit if these vendors are in compliance with these environment services.

### ***The STEP standard for product data exchange***

In a global manufacturing environment, product data needs to be communicated using a language that is global. STEP, the ISO 10303 Standard for the exchange of product data, became that language when it reached Draft International Status in February of 1993. It is expected to become a full International Standard in 1994.

A standard that seeks to communicate complete, unambiguous, accurate definitions of products around the world cannot avoid being complex. However, the

basic organization of STEP is relatively simple. As shown in Figure 3.6, the standard can be broken into three parts: an infrastructure shown by the bucket at the base and sides of the figure, a library of engineering product model definitions shown in the center of the figure, and a set of application protocols shown at the top of the figure.

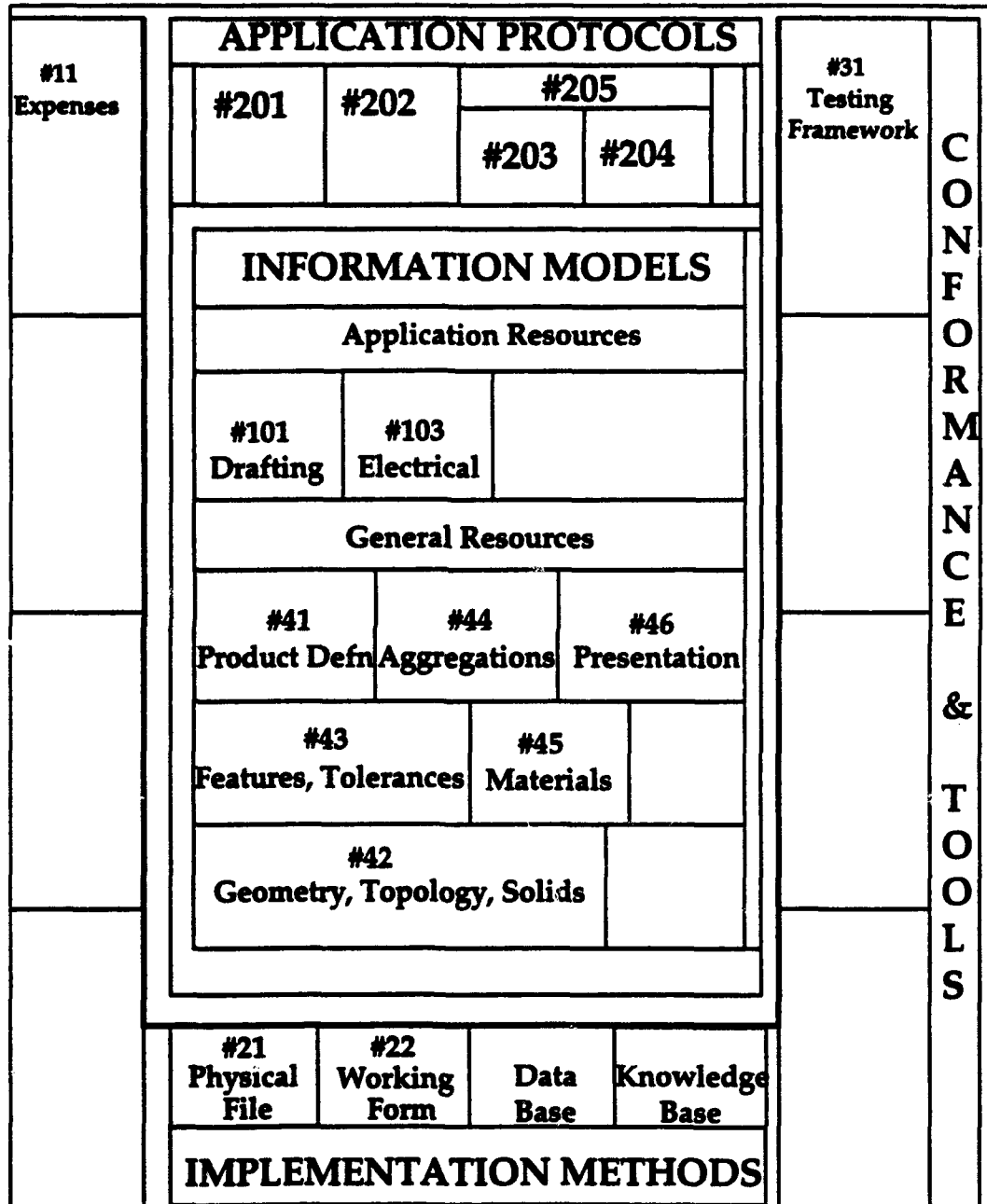


Figure 3.6 STEP Standard

The STEP infrastructure consists of the EXPRESS language, implementation methods and testing methods. In STEP< EXPRESS is used to describe information models. An information model is a formal description of the information requirements of an application or set of applications. Information models can be described using several different languages including Entity-Relationship diagrams, NIAM diagrams and IDEF diagrams. EXPRESS information models use a program-like notation as their primary form and a diagram notation called EXPRESS-G as an illustrative form. EXPRESS is distinguished from other information modeling languages by its use of a program-like notation, by its extensive use of inheritance and by its ability to describe user-defined constraints. Some examples of EXPRESS are given in the fourth section.

EXPRESS describes the properties required in a body of information, now how they are represented in a system. This leaves applications free to describe databases that use this information in many different ways. Applications that want to use this information in standard ways use one of the STEP implementation methods. Currently, they consists of a file format (Part 21) and an application programmers interface (Standard Data Access Interface-SDAI). The SDAI is an abstract description of a set of operations that can be applied to a database defined by an EXPRESS information model, and bindings for these operations in the C, C++ and FORTRAN programming languages.

The library of engineering product model definitions shown in the center of the figure will eventually contain one definition for every kind of entity used in engineering applications. The library is divided into a series of parts that describe definitions for particular kinds of engineering data. For example, Part 41 contains definitions for configuration management, Part 42 contains definitions for geometry, and Part 45 contains definitions for materials. The library is large and growing. Whenever a new Application Protocol is added to STEP the designers of that protocol must first make sure that the library contains the resources that will be needed by the protocol. If it does not, then a new Part must be added to the library.

The global library is too comprehensive for any single application or set of applications. Therefore, the definitions in the global library are assembled into useful subsets by the Application Protocols. Each Application Protocol contains all the definitions that are necessary and sufficient to describe a particular kind of product for a particular range of applications. For example, AP203 contains all the definitions needed to describe configuration controlled mechanical assemblies and AP207 contains all of the definitions needed to describe sheet metal dies.

The global library and the Application Protocols in STEP are described using EXPRESS. New application Protocols are added to STEP using a three stage process. In the first stage, the applications that will be using the Application Protocol are identified using an Application Activity Model (AAM). In the second stage, the entities that need to be shared by these applications are identified by application experts. These experts produce a preliminary model called the Application Resource Model. Normally, the application experts produce an

EXPRESS model, but at this stage they may also choose to use NIAM. Finally in the third stage STEP experts normalize this model to create a final model called the Application Interpreted Model (AIM). These models are always written in EXPRESS.

In the normalization process, the STEP experts select an entity from the global library to represent every entity in the ARM model produced by the domain experts. If an appropriate entity does not exist then one is added. They also reorganize the ARM model so that as many constraints as possible are represented by the standard data structures and constraints of EXPRESS. Next they try to express as many of the remaining constraints as possible using "local" user defined rules that apply to a single entity. Finally, the remaining constraints are represented by "global" user defined rules that apply to a database of entities.

The STEP normalization process produces Application Protocols for well defined sets of applications. Currently approximately 25 Application Protocols are in various stages of the standardization process. Many of these Application Protocols contain overlapping subsets. Therefore, the STEP community has created Application Interpreted Constructs (AIC's) to formalize these subsets. For example, the boundary representation geometry in Application Protocol 203 is defined by an Application Interpreted Construct so that other protocols can use this geometry.

If an AIC is the same as a generic resource in the global library, then the definition of that AIC is simple. However, in practice AIC's are different to generic resources because the former are instantiations of the latter in specific contexts. For example, Part 42 of STEP contains definitions for many different kinds of geometry. Some, but not all, of this geometry is used in boundary representation models. Therefore, the geometry model in Part 42 is distinct from the boundary representation AIC.

### ***Electronic Design Interchange Format (EDIF)***

EDIF is a representation of electronic design data that primarily addresses CAE data representation including electronic logic, schematic diagrams, electronic simulation data. EDIF is endorsed by the Electronic Industries Association (EIA) and Electronic Design Automation Companies (EDAC).

Since 1988, EDIF has been maintained using the EXPRESS language. An EXPRESS information model of the EDIF format has been established. Changes or additions to EDIF submitted for implementation are accepted only as new or modified EXPRESS information model.

The CHOICE EXPRESS information model could be expanded to include EDIF. Conversely, the CHOICE information model contains MCM design and manufacturing information that could be an extension to the EDIF model.

### ***Initial Graphics Exchange Specification (IGES)***

Initial Graphics Exchange Specification (IGES) defines a file structure format, a language format, and the representation of geometric, topological, and non-geographic product definition data in these formats. It provides a digital representation and communication of product definitions. Use of the IGES specification permits the compatible exchange of product definition data used by various CAD/CAM systems.

IGES is used extensively in the mechanical design and CAD industry and to a lesser extent in the electronic design automation industry. It serves as one means to transfer data between electronic design and mechanical design systems.

An EXPRESS information model for IGES has been developed. CHOICE uses the IGES format as output by Cadence Allegro to interface with ROSE. This implementation is a small subset of the total IGES format.

## **Current Commercial Products**

### ***Mentor OpenDoor***

Mentor Graphics Corporation offers the "Open Door" program that allows EDA Software vendors the ability to incorporate software tools with Mentor Graphics software tools. OpenDoor gives its participants access to Mentor's Falcon Framework product, select applications within the framework and software toolkits to access the selected applications data.

The OpenDoor program allows participants to perform the following tasks to integrate their tools with Mentor Graphics' tools and environment.

- *Tool encapsulation.* This allows a participant to register tools in the Falcon Framework. This encapsulation is accomplished via an AMPLE script, which is Mentor's extension language. Execution of the tool from the framework is then possible.
- *Data Access.* Data access is accomplished via Programming Toolkits that allow participants to read and write Mentor application data. An example of one of Mentor's toolkits is DFI. This toolkit provides a procedural interface to the Design Architect database.
- *Interprocess communication.* Participants can pass messages to and from Mentor applications. These messages can be passed either via a File or via Berkeley sockets. The file based method of passing messages is accomplished through AMPLE scripts. The socket based method is accomplished through a procedural interface.
- *Design Data Management.* Design data management is accomplished in a similar fashion to tool encapsulation. Any application's data files can be encapsulated into the framework similar to tools. Once the different data files are encapsulated, tools can be executed through the data, versions of the

data can be created, and references can be created between different versions of data files. These versions and references can be created manually by the user or automatically when a tool completes execution.

### ***Viewlogic PowerPartners***

Viewlogic Corporation offers the "PowerPartners" program that allows EDA Software vendors the ability to incorporate software tools along with Viewlogic software tools. PowerPartners gives its participants access to Viewlogic's framework product PowerView, selected applications and software toolkits to access the selected applications data.

The PowerPartners program allows participants to perform the following tasks to integrate their tools with Viewlogic's tools and environment.

- *Tool encapsulation.* This allows a participant to register tools in PowerView. This encapsulation is accomplished via CFI TES 1.0 standard. Execution of the tool from the framework is then possible.
- *Data Access.* Data access is accomplished via Programming Toolkits that allow participants to read and write Viewlogic application data. An example of one of Viewlogic's toolkits is PCB Toolkit. This toolkit provides a procedural interface to the Viewdraw database for the purposes of interfacing with PCB CAD products.
- *Interprocess communication.* Participants can pass messages to and from Viewlogic applications. These messages can be passed either via a File, X-events or UNIX fifo's. The file based method of passing messages is accomplished through a product call CPROBE.
- *Design Data Management.* Design data management is accomplished with a product call PowerViewDM. The design data is described to PowerViewDM through a text file. Any application's data files can be encapsulated into the framework similar to tools. Once the different data files are encapsulated then versions of the data can be created either manually by the user or automatically when a tool completes execution.

### ***Cadence Connections***

Cadence Corporation offers the "Connections" program that allows EDA Software vendors the ability to incorporate software tools along with Cadence software tools. Connections gives its participants access to Cadence's Design Framework II product, selected Cadence applications and software toolkits to access the selected applications data.

The Connections program allows participants to perform the following tasks to integrate their tools with Cadence's tools and environment.

- *Tool encapsulation.* This allows a participant to register tools in Design Framework II. This encapsulation is accomplished via a SKILL program, which is Cadence's extension language. Execution of the tool from the framework is then possible.
- *Data Access.* Data access is accomplished via Programming Toolkits that allow participants to read and write Mentor application data. An example of one of Cadence's toolkits is CAEViews. This toolkit provides a procedural interface to the Concept database.
- *Interprocess communication.* Participants can pass messages to and from Cadence applications. These messages can be passed via Berkeley sockets.
- *Design Data Management.* Design data management is accomplished with a product call Teamwork. Any application's data files can be encapsulated into the framework similar to tools. Once the different data files are encapsulated then versions of the data can be created, and relationships can be created between different versions of data files.

## DICE Programs

### *MCM Concurrent Engineering Environment*

ROSE has been exercised in a variety of application environments. ROSE has been positioned as a mechanism for design data interchange and has demonstrated its ability to move data between dissimilar design environments (e.g., FINESSE MCM, Valid Allegro, AutoCad, Cadence Edge).

ROSE is also being used in more of an interactive tool environment within Raytheon. In the Raytheon environment the data is being moved from their internal database to ROSE in order to perform manufacturing yield/cost analysis on the data.

This diversity of working environments has exercised the ROSE environment in many different ways. The diversity of the environments has demonstrated that ROSE has the potential to be used for many applications within engineering domain.

A review of the DICE Project involving the use of ROSE as the underlying database will discuss the benefits and shortcomings of the DICE technology as compared with the other commercially available database and concurrent engineering technology.

An assessment of how DICE could be further developed to meet the needs and expectation of the end-users will be stated.

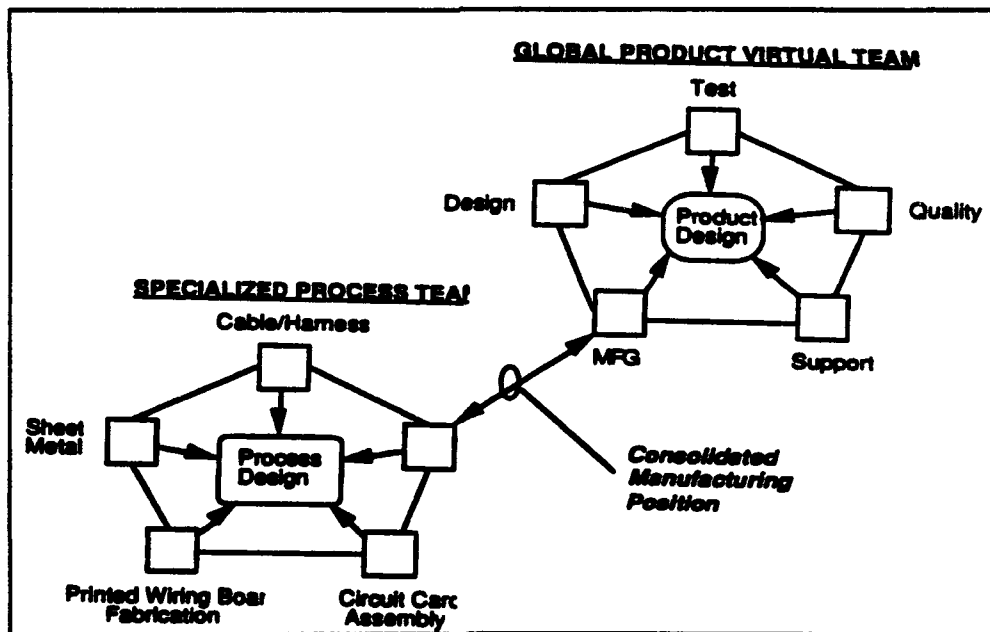
## ***Manufacturing Optimization***

Raytheon Company Manufacturing Optimization (MO) System was developed under DICE funding and will be delivered by 1st quarter 1994.

The MO System was developed to enable manufacturing engineers and specialists the opportunity to participate as a group in the design process. (Figure 3.7) The system consists of a set of tools that model printed circuit board manufacturing processes and then centralizes the various tradeoffs caused by the manufacturing processes. (Figure 3.8)

The manufacturing team, using the MO System, can pass recommendations based on the number of results created by the MO System back to the product design team. These recommendations come from the multidisciplined manufacturing team as opposed to a select few manufacturing representatives. In this way, processes like pc board fabrication, drilling, component pick and place, soldering, automatic test, and many other disciplines can have their unique experience included in the analysis and feedback.

The MO System utilizes the same ROSE database and STEP Tools, Inc. environment as the CHOICE concurrent engineering environment. (Figure 3.9)



**Figure 3.7 Raytheon Manufacturing Optimization Concept**



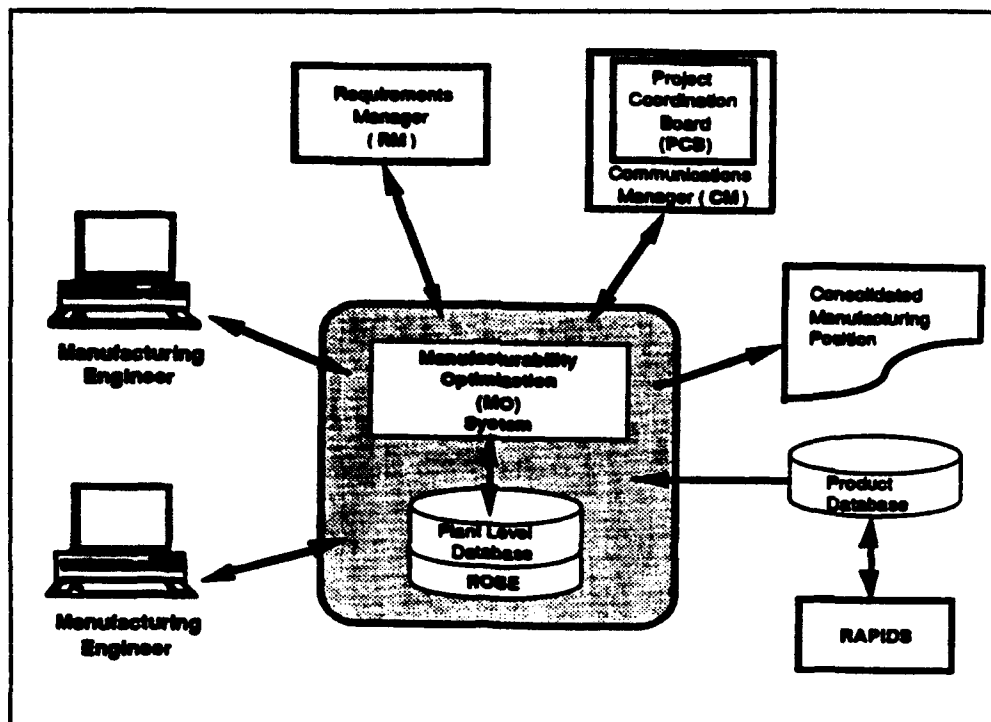


Figure 3.8 Raytheon Concurrent Engineering Environment

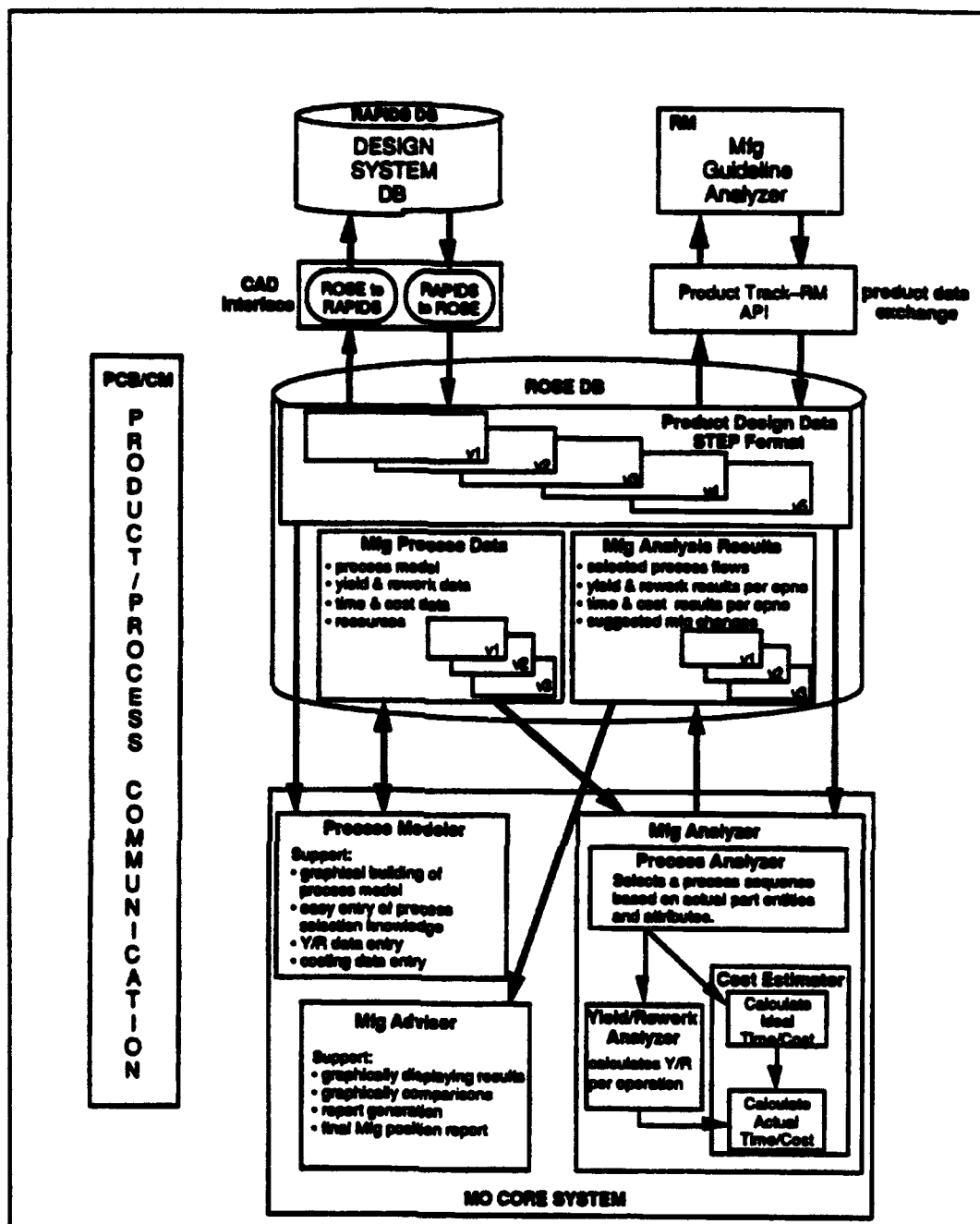


Figure 3.9. Raytheon Manufacturing Optimization Architecture

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## Section 4 — Case Study

### Introduction

#### *Harris GASD Experience*

Harris GASD Government Aerospace Systems Division (Harris GASD) is a major designer and supplier of advanced electronics for the DoD and NASA communities. Harris GASD has actively engaged in the design and development of state-of-the-art multichip modules for use in military systems. Starting in 1990, Harris GASD has completed designs for fourteen different MCMs for use in five major military programs.

The systems include the F-22 Advanced Tactical Fighter for the U.S. Air Force, and the RAH-66 Comanche Light Helicopter for the U.S. Army. For the F-22, Harris GASD is supplying all of the aircraft's Fiber-Optic (F-O) avionics interfaces using three F-O MCMs. These MCMs are excellent examples of mixed technology MCMs which combine the digital, analog and mixed signal features of CMOS, Bipolar, GaAs and Fiber-Optic circuit technologies into a single module. The wise exploitation of this evolving MCM technology will help to the manage costs while improving the technical performance of future weapon systems.

Harris GASD has identified MCMs as a core technology. Harris GASD has made a commitment to the use of MCMs, because they provide an important key to the success of future programs.

### Background

#### *Concurrent Engineering Overview*

Traditional functional organizations such as engineering, testing, product assurance and manufacturing have maintained their expertise by concentrating their skills in one area. The functional organizational structure has the advantage of maintaining and enhancing expertise in a given area and enabling good communication within that area. The difficulty with this structure is that projects progress serially and the communication is inefficient among the larger organizations. These deficiencies maybe rectified by establishing program teams with people from each of the functional organizations working together on a concurrent engineering team. Harris GASD has used this multi-discipline concurrent engineering approach to successfully complete fourteen MCM designs. The application of concurrent engineering teams has reduced design cycle times and helped to contain costs.

In the design of the MCMs, the program team members work in parallel to complete the product design within the minimum amount of time. Since an optimal MCM design environment is still emerging, a Cadence/Valid Logic platform was used as the MCM design baseline. Other ancillary tools were used in a piecemeal fashion to analyze analog functions and other behavioral performance

characteristics not fully supported by the Cadence toolset. The design effort for these complex MCM devices has required the use of multiple software tools from a variety of different tool suppliers.

### ***Scope of Report***

This application of the concurrent engineering environment will be described in this report as we discuss the various MCM projects in detail. This report will describe the MCM design methodology and software tools used at Harris GASD to complete electronic systems design projects that utilize MCM technology. Case studies taken from various Harris GASD programs will be used to explore the software tools features, design database capabilities, data transfer requirements, design to manufacturing issues, MCM test data generation, and timelines to project completion.

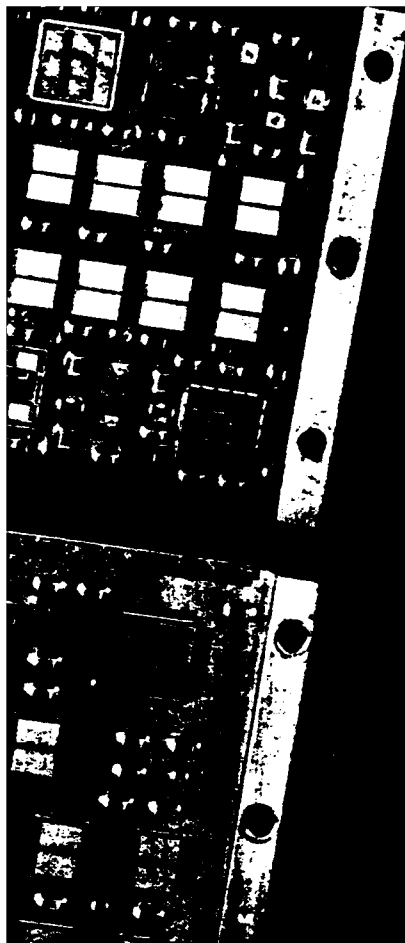
This report will also describe the desired MCM Design Environment that would support an efficient and effective MCM design methodology. The report will then highlight the expected improvements in terms of reduced MCM design cycle time, fewer design iterations, greater product performance and reduced overall product costs. The desired MCM Design Environment will include a description of desired automatic features, software requirements, concurrent engineering, data integration among applications and manufacturing, and other aspects of this "should be" environment.

### ***MCM Applications***

Using the concurrent engineering concept, Harris GASD has designed fourteen different MCMs that are used in five major military programs. Over the next twelve months Harris GASD will be delivering military systems which contain over 3,000 MCMs. These fourteen MCMs can be classified into three categories: Digital, Mixed Digital/Analog and Fiber-Optic/Mixed Signal.

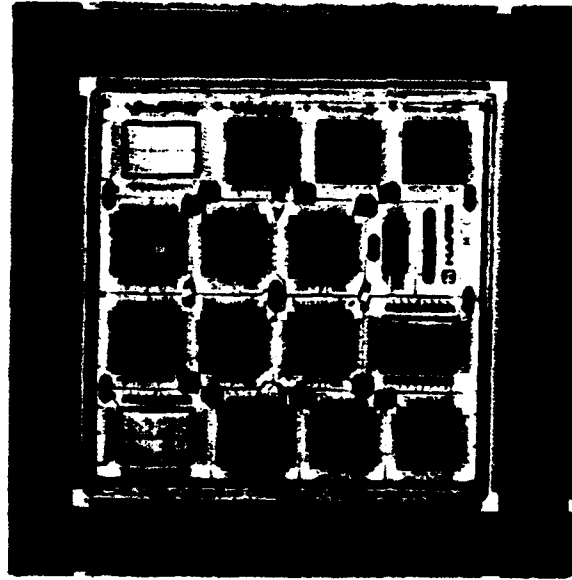
Harris GASD Digital MCMs by Program		
PROGRAM	MCM DESCRIPTION	COMMENTS
Advanced Hardened Avionics Technology (AHAT) demonstrated for high radiation environments.	3 MCMs 2.7" x 2.7" 10 MHz SOS CMOS ASICs, SRAMS 320 I/Os	Thin Film Multilayer (TFML) MCMs assembly, burn-in, and test completed at Harris GASD GASD. Aluminum/polyamide substrates fabricated by Hughes. MCMs completed in September 93.
Brilliant Eyes	2 MCMs 2.1"x 1.8" 20 MHz Memory Module 100 I/Os 2.1"x 2.5" Cache Module 172 I/Os	Low Temperature Cofired Ceramic (LTCC) Substrates Metal Packages. MCMs Design, layout, and testing completed at Harris GASD GASD. LTCC substrates and MCM assembly performed by CTS, a Harris GASD GASD partnership supplier. MCM working prototypes completed in November 93.
DDR-2 Harris GASD GASD/MCC Co-development Harris GASD GASD interdivisional concurrent IR&D Engineering Project.	Digital Drop Receiver 2.8"x2.8" MCM 25 MHz 15 ASICs 1 EE PROM 408 I/Os	Project built a base for military qualifiable MCM processes and piece parts for both Class H and K. MCMs being fabricated in LTCC, HTCC, and TFML. Electrical testing, burn-in, and qualification testing being performed by Harris GASD GASD. MCMs completed in November 93.
Comanche U.S. Army Light Helicopter	Processor MCM 1.8"x1.8" 25 MHz 3-CMOS ASICs, 304 I/Os	Low temperature cofired ceramic (LTCC) substrate with integrated package. Design, layout, and testing performed at Harris. LTCC substrates and MCM assembly performed by CTS, a Harris GASD partnership supplier. MCM working prototypes completed in July 93. First production MCMs completed Nov. 93.

Table 4.1 Description of Harris GASD Digital MCMs by Program

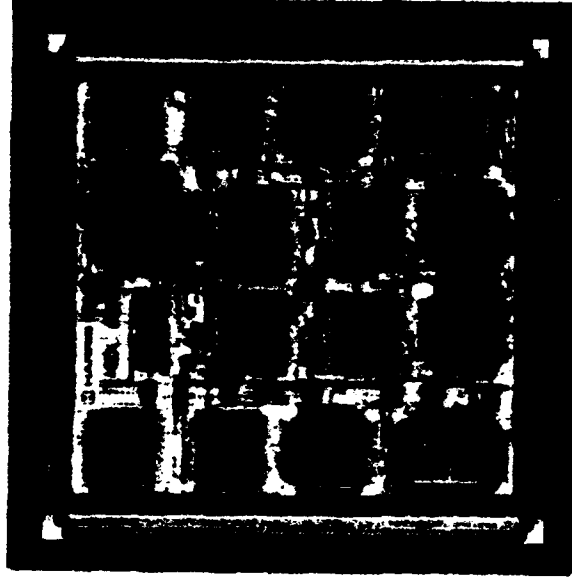


# HARRIS DDR-2 BUILT IN THREE MCM TECHNOLOGIES

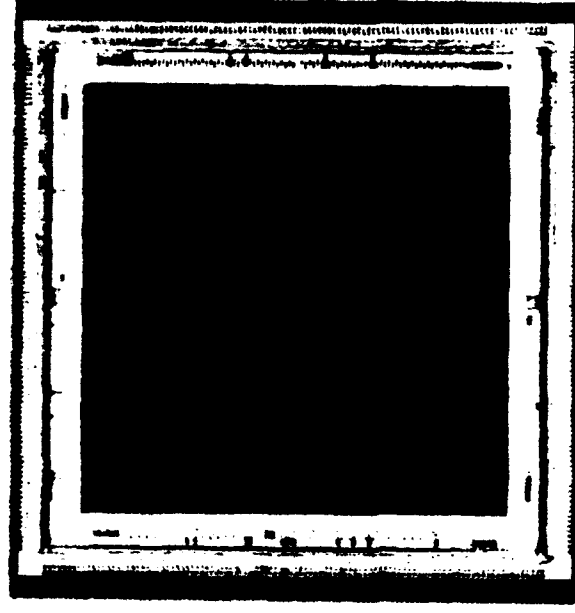
## 408 PIN MCM



LOW TEMPERATURE CO-FIRED  
CERAMIC SUBSTRATE



HIGH TEMPERATURE CO-FIRED  
CERAMIC SUBSTRATE



MULTI-LEVEL THIN FILM GE  
OVERLAY PROCESS

Figure 4.2 Harris DDR-2  
Built in three MCM Technologies

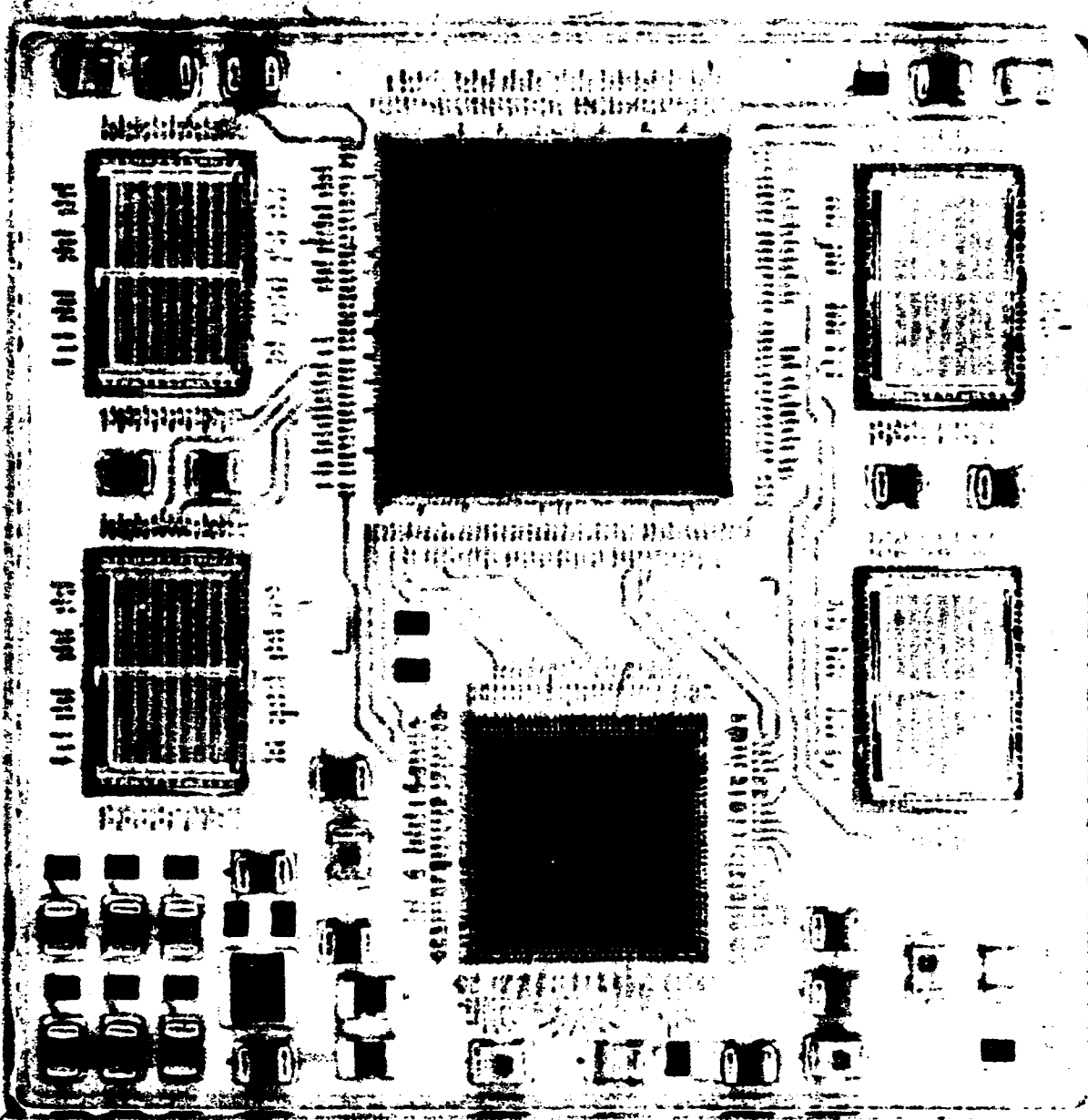


Figure 4.3 93-2100CMR-1-6A  
Comanche Processor Module



Harris GASD Mixed Signal MCMs by Program		
PROGRAM	MCM DESCRIPTION	COMMENTS
Comanche U.S. Army Light Helicopter	<p>2 MCMs 1.8"x Harris GASD GASD304 I/Os</p> <p>Sensor Data Distribution Network (SDDN) - 500 MHz - 1 CMOS ASIC - 2 ECL ASICs - 1 Analog ASIC</p> <p>High Speed Data Bus (HSDB) - 100 MHz - 1 CMOS ASIC - 1 ECL ASIC - 4 SRAMS</p>	Low temperature cofired ceramic (LTCC) substrate with integrated package. Design, layout, and testing performed at Harris GASD GASD. LTCC substrates and MCM assembly performed by CTS, a Harris GASD GASD partnership supplier. MCM working prototypes completed in July 93. First production MCMs completed Nov. 93.
Sub-Miniature Telemetry (SMT)	<p>2 MCMs 2.0" x 2.0" 40 I/Os 2 MHz to 2.4 GHz 1 RF ASIC 2 Analog ASICs 1 Digital ASIC</p>	Low Temperature Cofired Ceramic (LTCC) Substrates in metal packages. MCMs Design, layout, assembly and testing accomplished at Harris GASD GASD. Modules were successfully completed in February 1993.

Table 4.2 Description of Harris GASD Mixed Signal MCMs by Program

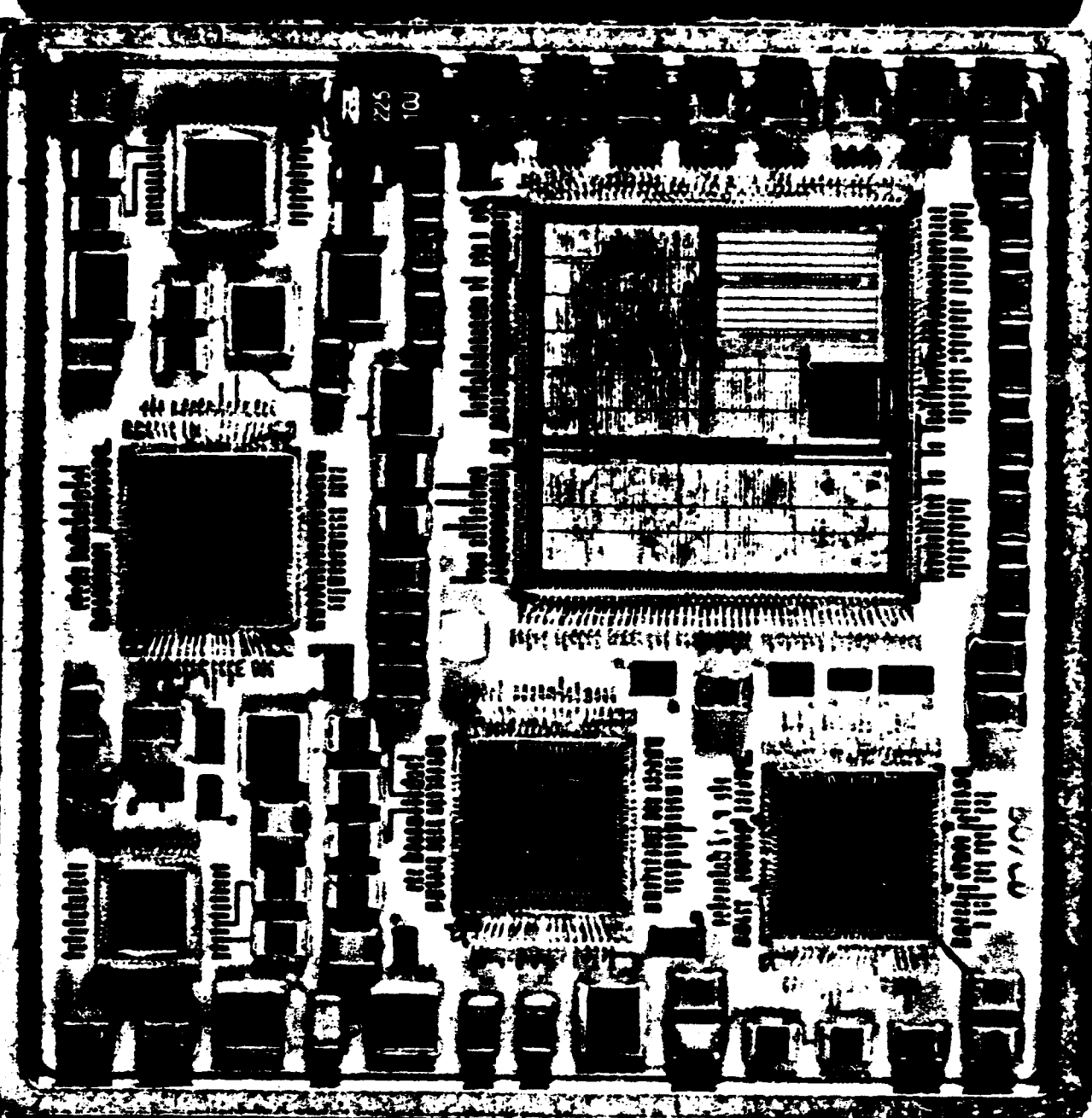


Figure 4.4. 93-21000-1-DA  
Comanche SDDN

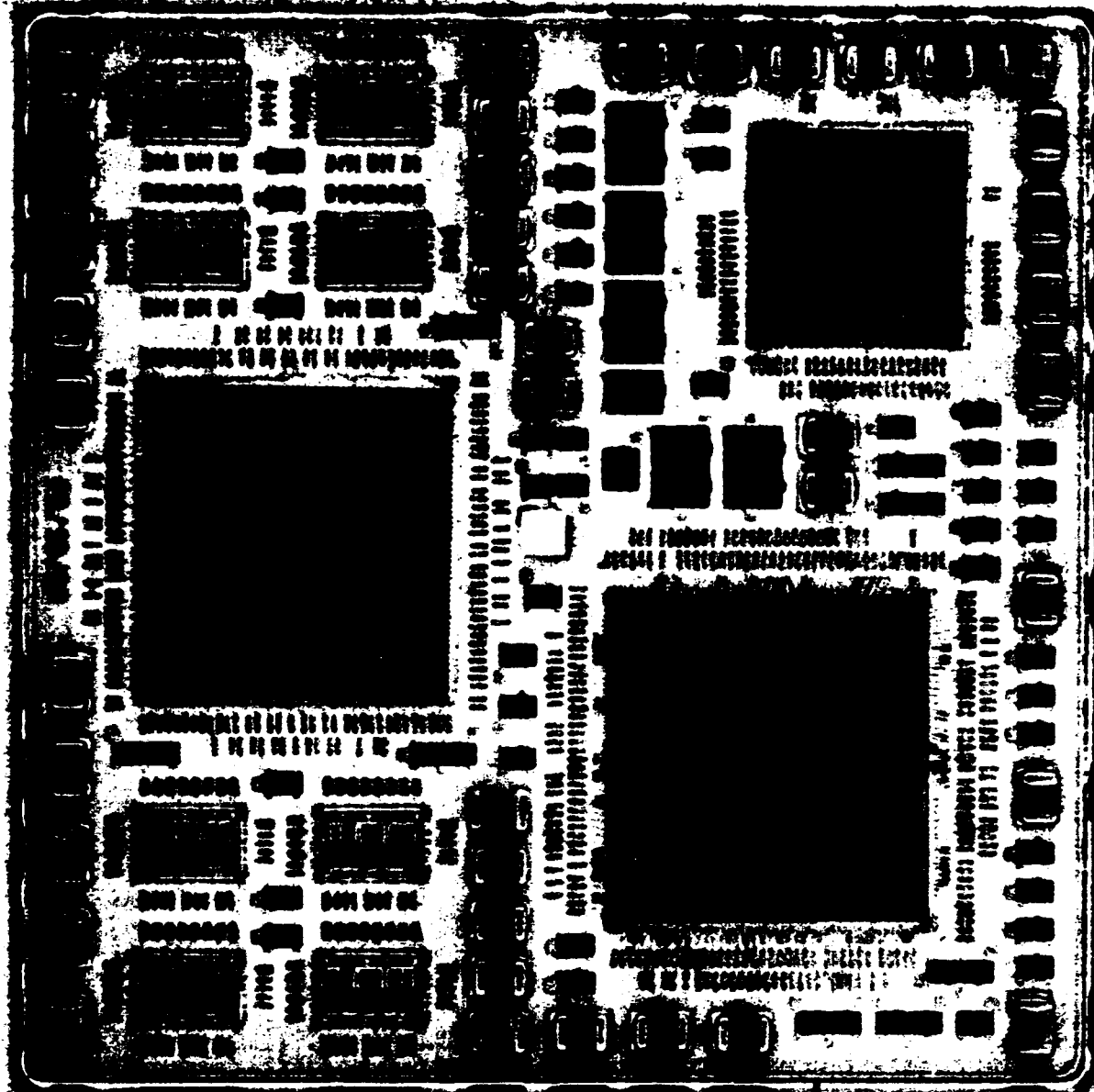
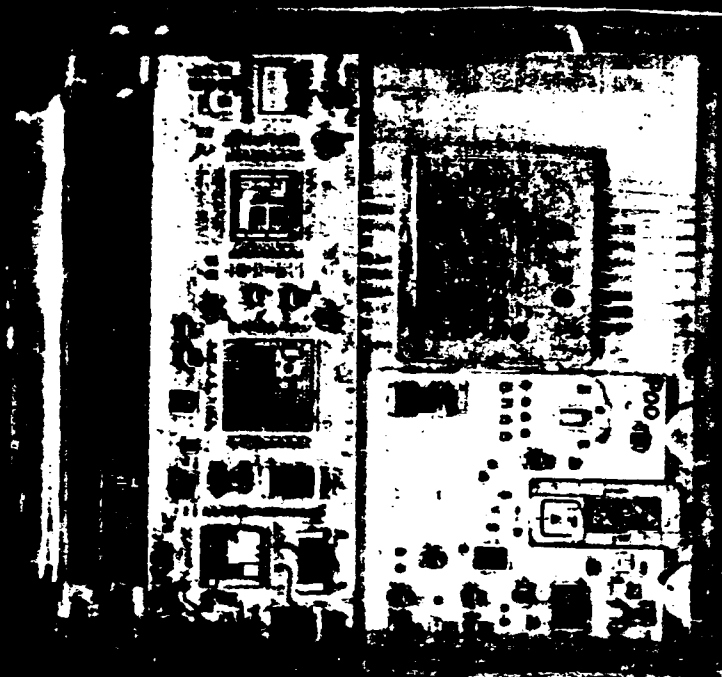
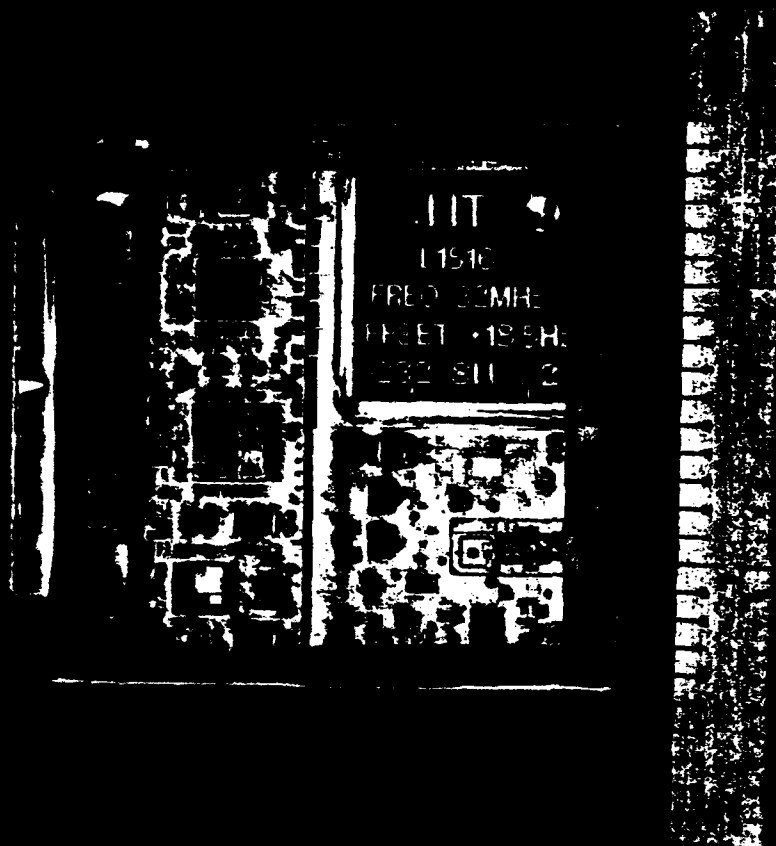


Figure 4.5 .93-2100C-1-8A  
Comanche HSDB



## **SMTT Peel-and-Stick Configuration**

Figure 4.6.93-1918C-1-4  
SMTT Peel-and-Stick Config.



## **SMTT Smart Weapon Module Configuration**

Figure 4.7.93-1918C-1-12  
SMTT Smart Weapon Module Config.

Fiber-Optic/Mixed Signal MCMs by Program		
PROGRAM	MCM DESCRIPTION	COMMENTS
F-22 U.S. Air Force Advanced Tactical Fighter (ATF)	3 MCMs	First production implementation of Fiber-Optic MCMs. Military screened MCMs to be built by CTS, a Harris GASD partnership supplier. Prototype MCMs were successfully completed in Feb. 93. First production MCMs scheduled for completion Feb. 94
	Fiber-Optic Transmitter (FOTX) - 100 I/O - 1.0"x1.5" - 500 MHz - 1 CMOS ASIC - 1 ECL ASIC - 1 Analog ASIC	
	Fiber-Optic Receiver (FORX) - 100 I/O - 1.0"x1.5" - 500 MHz - 1 CMOS ASIC - 1 ECL ASIC - 2 Analog ASICs - 1 GaAs ASIC	
	High Speed Data Bus (HSDB) - 260 I/O - 2.5"x2.5" - 100 MHz - 1 CMOS ASIC - 1 ECL ASIC - 4 SRAMS - 4 Analog ASICs - 4 Detachable Fiber-Optic cables	

Table 4.3 Description of Fiber-Optic/Mixed Signal MCMs by Program

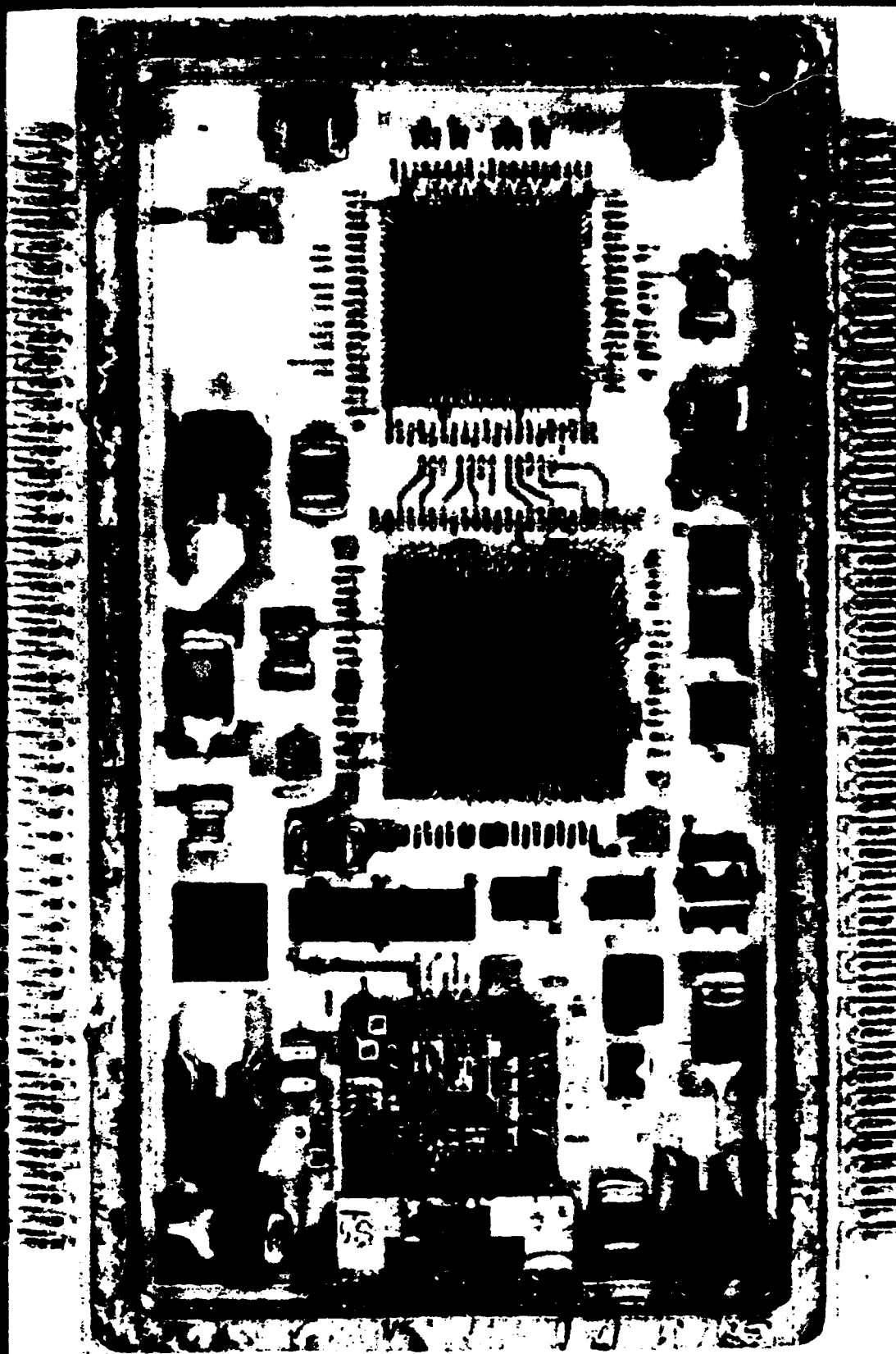


Figure 4.8 93-0838C  
F22 Transmitter

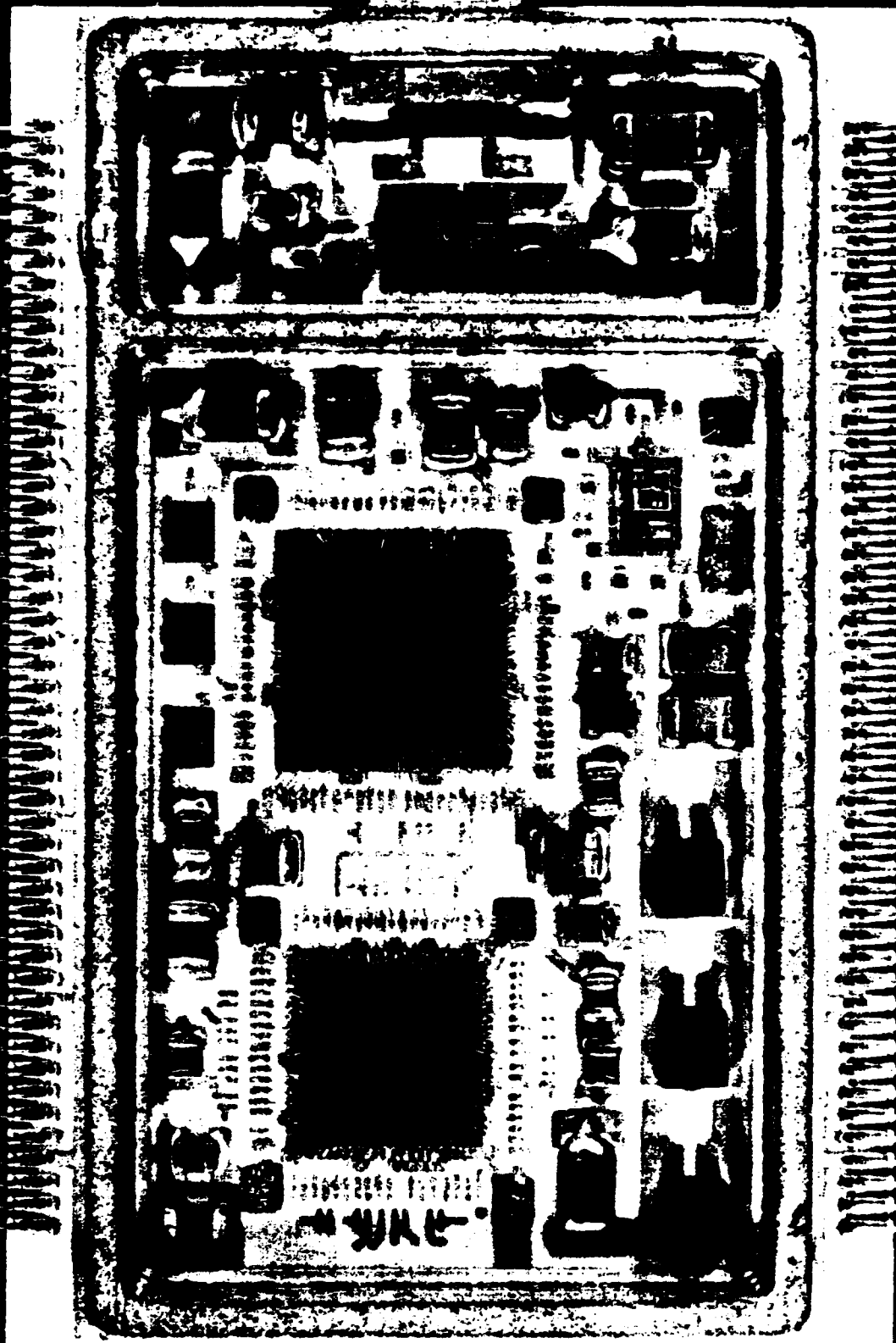


Figure 4.9.93-0834C  
F22 Fiber Optic Receiver



## **Design Environment**

### **Design Environment Overview**

Figure 4.10 shows a diagram of the current MCM design environment at Harris GASD. The "MCM Constraints" and the "Chipset and Electrical Interconnect" requirements provide the input data which drive the toolset of MCM design process. The MCM constraints include the MCM supplier's design rules, the performance characteristics which flow from the customer's requirements, and other constraints on the MCM design.

Under the concurrent engineering model, the MCM fabrication and assembly, test vector generation, MCM test and rework, Proof-of-Design (POD) evaluation and the transition to system level manufacturing are all considered to be a part of the MCM design process. All of the engineering disciplines, including design, test, manufacturing and product assurance are closely coupled during all stages of this process.

Managing the material and parts aspects of an MCM assembly is also an integral part of the design environment. The Approved Parts Interactive Management System (APIMS) provides a general database with extensive information regarding approved suppliers and standard parts for use in deliverable hardware. APIMS also creates a direct link into our purchasing organization and aids in device procurement activity. The Parts Control and Tracking System (PCATS) manages the parts lists at the module, PWB and box level for each individual assembly effort required to complete a Harris GASD contract. The Integrated Manufacturing Operating System (IMOS) coordinates and manages the overall manufacturing effort, using parts status information extracted from PCATS plus real-time assembly status information.

The PCATS and APIMS tools were both developed internally at Harris, because we could not find commercial software which met our needs. The IMOS tool was purchased as a standard software product.

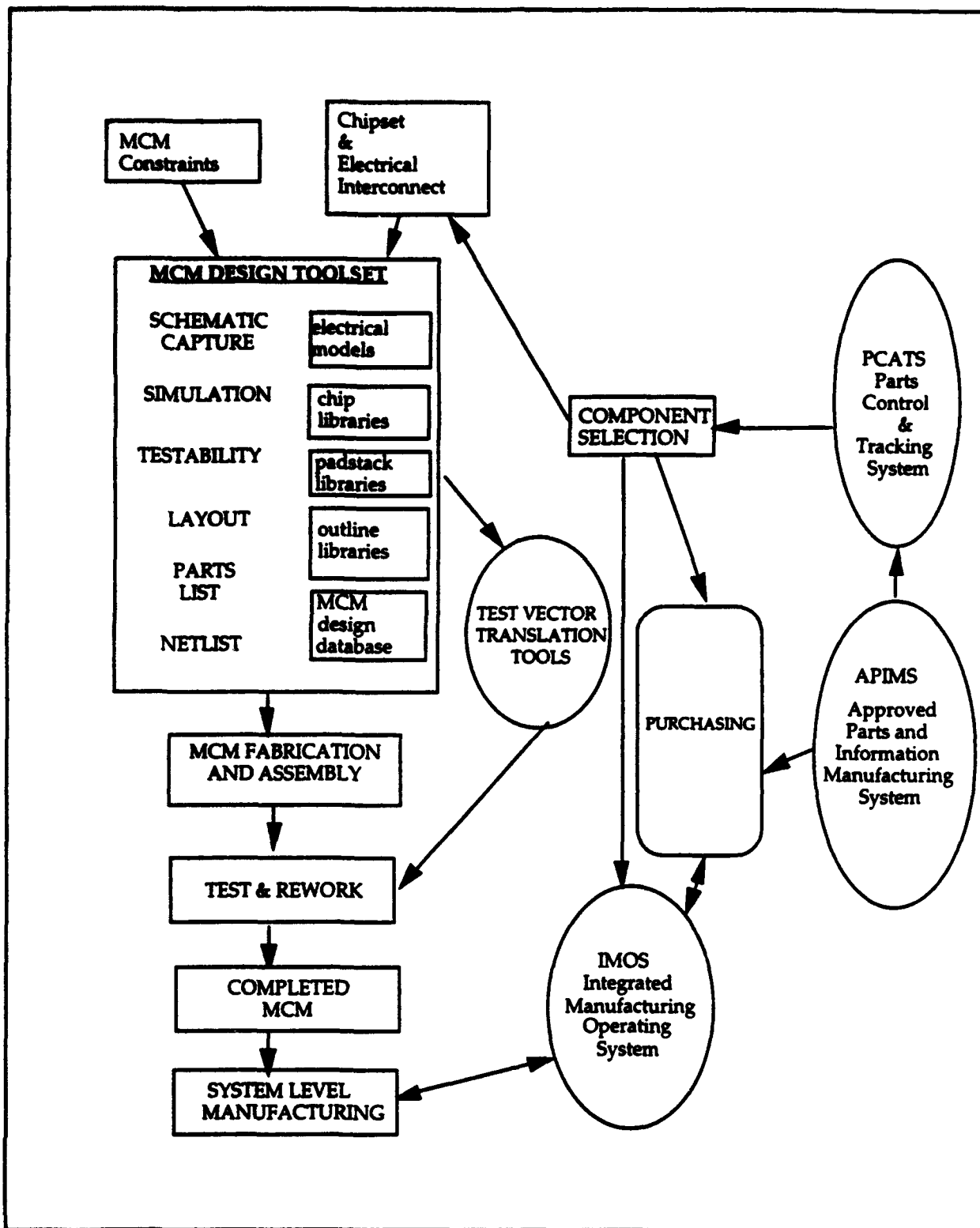


Figure 4.10 Harris GASD MCM Design Environment

As is illustrated by Figure 4.11, there is a plethora of constraint systems which drive the MCM design and layout process. The essence of the MCM design process is the application of the design tools towards the goal of achieving the compromise solution which best satisfies these constraints. The customer requirements drive the selection of devices and technologies which define the "Chipset and Electrical Interconnect" criteria. The required electrical performance characteristics, mechanical restrictions, and thermal issues all push the design features (what is desired), while the chipset requirements and MCM supplier's rules constrain the MCM layout process (what can be built). The tools themselves add another layer of constraints, and the design process cannot ignore the limitations imposed by these simulation tools. The MCM assembly capabilities and the test hardware add a final layer of restrictions: the design must be buildable and testable.

The essence of concurrent engineering is to manage all of these various constraints in parallel, to avoid design iterations. This is accomplished at Harris GASD by bringing together the disciplines responsible for each of the individual constraint systems, and assembling them into a design team.

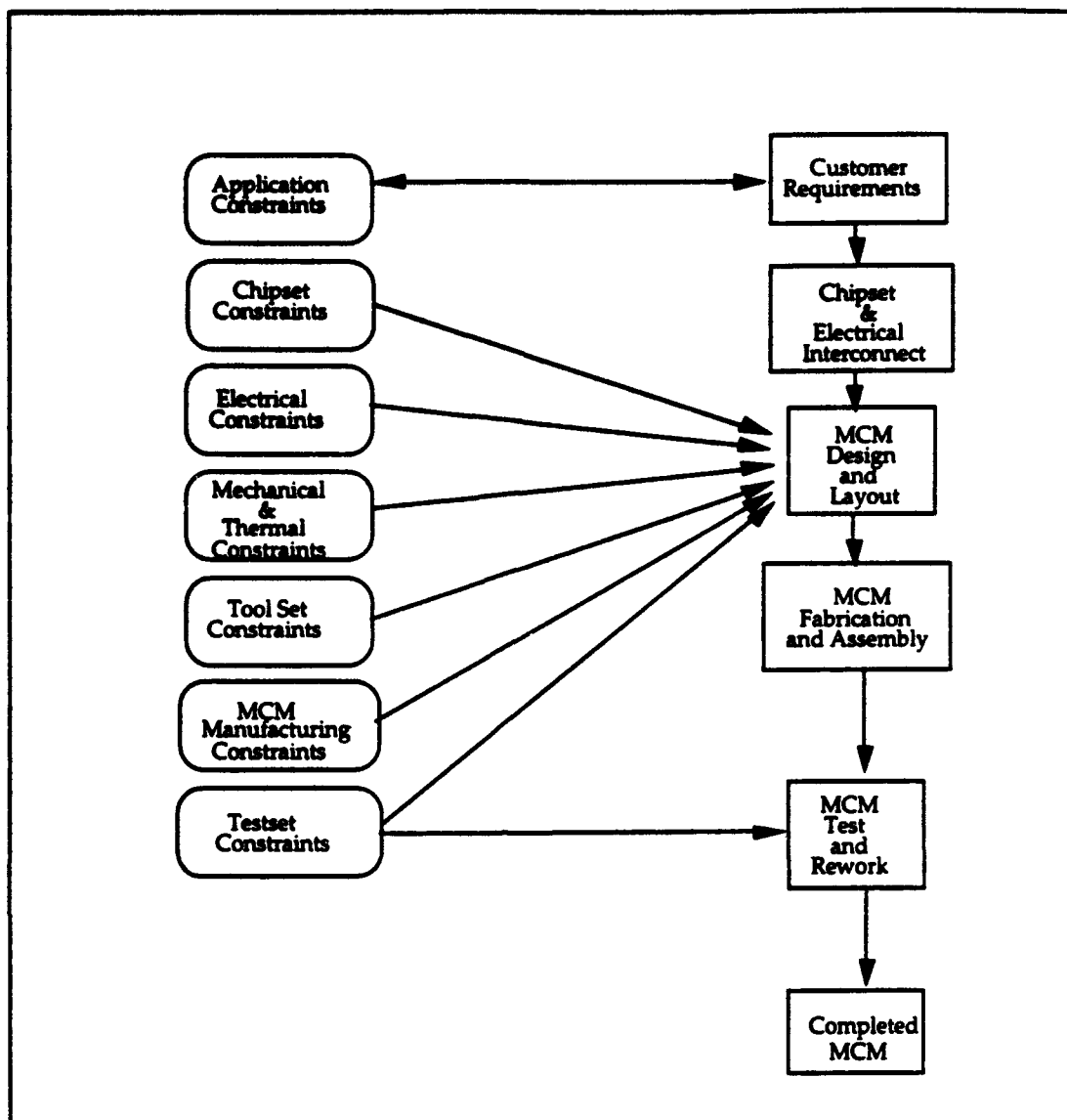


Figure 4.11. MCM Design Flow Showing Interaction with External Constraint Systems

### Software Tool Sets

To manage a plethora of constraint systems, one needs a plethora of tools. Figure 4.12 shows an example of the key software tools which are currently applied to a typical MCM design at Harris GASD. This software tool set may be modified or extended to meet specific program requirements.

The Cadence/Valid Logic design platform forms the core of the MCM design environment. For most of our digital ASIC devices, the Synopsis tool is used to synthesize an ASIC design from VHDL or another high level model, for a target ASIC technology. The resulting ASCII netlist is ported into the Cadence platform using SYNLINK. Hardware modelers are used to bring in standard IC devices. Functional and behavioral simulations are performed using the Valid Logic Rapidsim timing simulator and the LMSI tools. TESTSCAN or SIMUTEST (or other) tools are used to generate scan sequences for structural testing. The

MCM layout is managed using Allegro. TSSI is used to translate the simulation results into test vector patterns for use on the HP82000 test system. A variety of other tools are required to simulate mixed signal and analog circuitry, and to address thermal and mechanical issues. The APIMS, PCATS and IMOS tool sets are needed to manage the manufacturing effort from parts procurement through final assembly and testing.

Each of these tools requires an elaborate database structure to manage the vast quantities of data associated with the design of a complex MCM device. Some of these tools have limited capability to share information, but as a general rule each tool has an independent database. Data is carried from one tool to another via dedicated translation tools. This lack of synergy makes multiple chip simulation efforts at the MCM level very tedious. Different technologies within the MCM must be simulated with different tools in a piecemeal fashion, and the results must then be ported over to other simulation tools. While this segmented design approach has been successful on the MCM designs completed by Harris GASD, the lack of truly concurrent design platform has limited the ability to perform rigorous MCM level simulations. The existing tools cannot simulate all of the digital, analog and fiber-optic functions of the MCM simultaneously.

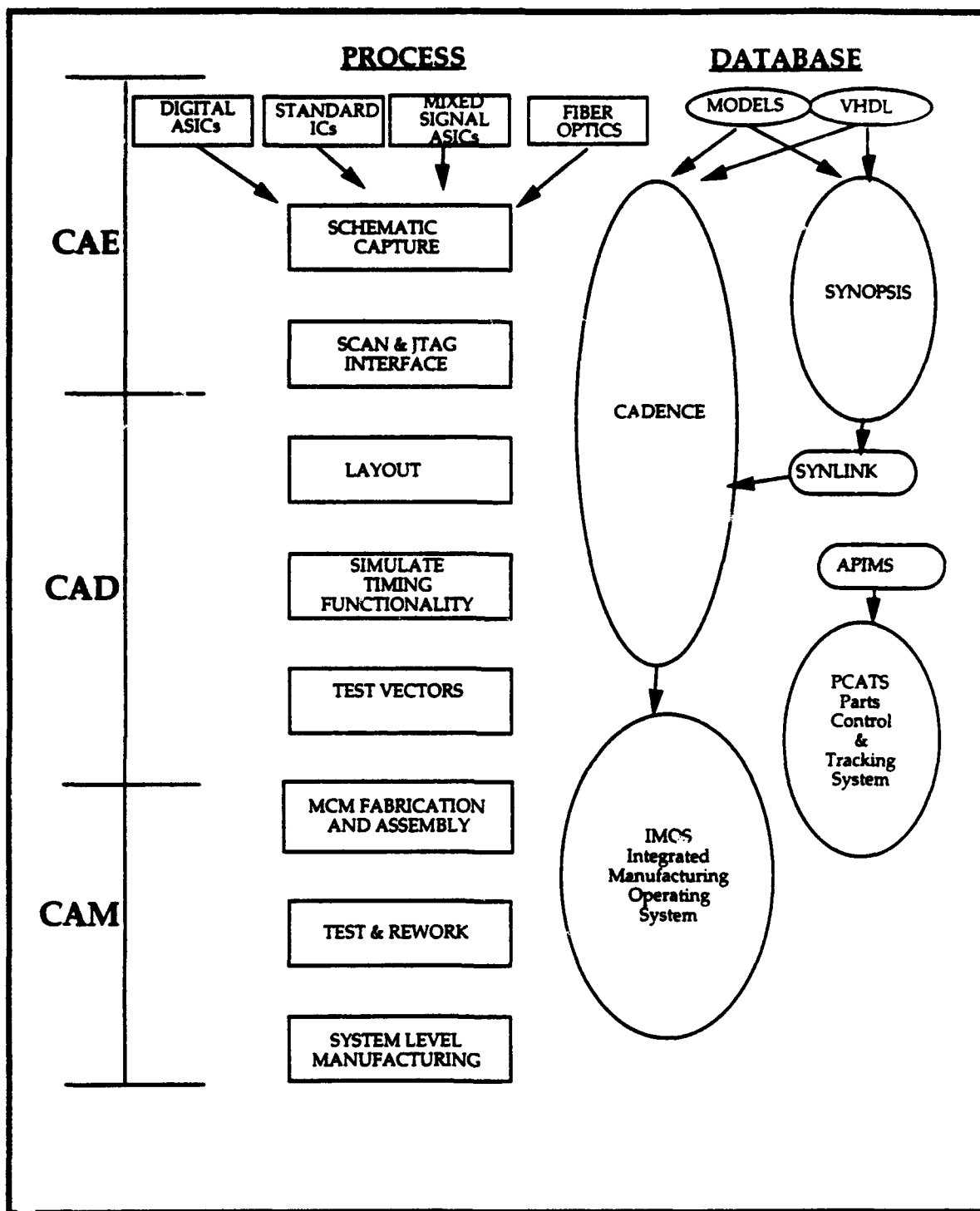


Figure 4.12 Software Tool Set Interaction

## **MCM DESIGN ENVIRONMENT CASE STUDIES**

### **Design to Manufacturing Issues**

There are two sets of manufacturing issues which are salient to MCM designs:

1. The MCM itself must be producible and testable as a stand-alone device.
2. The behavior of the MCM must be fully understood at the next highest assembly level; which is usually a printed wiring board.

The narrative which follows provides a detailed study of how MCM technology has been implemented for Harris GASD programs.

### **Brilliant Eyes MCMs**

In the "Brilliant Eyes" program, Harris GASD designed very dense radiation-hardened main processor memory and cache memory modules for application on space platforms. We were able to develop or obtain sufficiently accurate functional and timing models for all the memory and logic elements used in the MCM designs, in formats compatible with the Cadence/Valid Logic platform. This allowed electrical design, layout, simulation and back annotation to be performed on one common design platform. The advantage was that the same suite of design and simulation tools could be applied to the different levels of hierarchy from the die level behavior up to the total MCM function.

There were no difficult thermal issues, so the design constraints were driven by the rules of the module supplier (CTS) and by the system performance requirements (size, memory access and cache speed, power and weight). The application of a concurrent engineering methodology was straightforward. Representatives from the various Harris GASD design disciplines (electrical, mechanical, quality and reliability) worked with the manufacturing engineers at CTS to develop a set of manufacturing rules. These rules were summarized by Harris GASD and entered into the Valid Logic layout tools. This approach allowed the Valid platform to operate as a constraint driven design system.

This constraint driven design environment allowed the use of technical level specialists to perform the detailed MCM layout, with only minimal supervision from engineering level personnel. This use of less expensive personnel reduced the NRE costs of the MCM design. The Allegro tool was able to export the layout netlist information in a format compatible with the CTS process. The first Proof-of-Design (POD) units delivered by CTS had good substrates and functioned correctly.

### **AHAT MCMs**

The intent of the Advanced Hardened Avionics Technology (AHAT) Program is to demonstrate digital processor technology for extremely high radiation environment military space applications (actual levels are classified). The MCM design employed a combination of Silicon-on-Sapphire (SOS) ASIC devices, and standard CMOS/epitaxial technology chips such as memory and a MIL-STD-1553 bus controller.

The MCM and ASIC level designs needed to be performed in parallel because of very tight schedule and budget constraints. Design iterations could not be tolerated. The logic partitions and die footprints were frozen early in the MCM design process, requiring the ASIC level designs to fit into the allocated substrate areas. The die level gatecount estimates which were designed to be conservative later proved to be low, which caused painful tradeoffs between die size and desired functions.

The digital ASICs were all designed using the Genesil Silicon Compiler on a Mentor Graphics platform, with libraries for the Harris GASD Semiconductor TSO54 technology. There was good linkage between the target technology and the simulation tools at the die level, but the Mentor Graphics tools proved immature at the multiple chip simulation level. We experienced reasonable success in migrating circuit models from the die to module level, but the total gate count exceeded the capacity of the simulation tools. We also needed to develop behavioral models for the standard logic parts, which included memory chips, and a MIL-STD-1553 bus controller.

Throughout the ASIC and MCM level design cycles, weekly meetings were held with all disciplines represented, including the ASIC supplier (Harris Semiconductor) and the substrate suppliers (Raychem, later replaced by Hughes). The Thin-Film Multi-Layer (TFML) substrate design was passed off to Hughes, who delivered bare aluminum/polyamide module substrates. Non-standard ground planes were required for radiation hardness, which caused negotiation of design rules with the substrate supplier. The subsequent assembly, testing and rework, burn-in and final testing were all performed at Harris GASD. Five prototype sets of the three MCM designs were completed in September 1993. These modules are currently in radiation testing. No production quantities are planned.

The concurrent engineering practices served the project well. The main design problems encountered were the lack of sufficient gate count capacity for the simulator, the lack of models to support the standard parts, and non-standard design rules for substrate design and process.

### **Comanche MCMs**

The digital portions of the Comanche ASIC designs were captured using the VHSIC Hardware Description Language (VHDL), and converted to the applicable Technology Libraries for the selected ASIC supplier (VLSI Technology, Inc.). The EDIF netlist format was used to port the design between various tools. The Valid Logic "RapidSim" tool on the Cadence design platform was used for timing simulations, with validated timing models provided by the ASIC supplier. The LMSI Hardware Modeler tool set was used to carry the digital ASICs up to the multi-chip simulation level.

MCM layout was performed using the Allegro MCM tool from Valid Logic. Unfortunately, due to schedule pressures, the layout effort was started before the design rules were negotiated with the module supplier, CTS. These rules started as a loose set of verbal rules, and then later matured into formal constraints which were incorporated into the Allegro tools. This allowed a parallel design



effort and a faster turn time, but also caused some wasted effort because of minor layout changes which were driven by Design Rule Checks (DRCs) being run late in the design cycle. The lesson learned here is to get the rules for the prospective MCM suppliers into a technology database in the beginning of the design process.

The Allegro tools provided a netlist output in a format consistent with the MCM supplier, CTS. This handoff was accomplished smoothly for the Comanche Program. Prototype MCMs were successfully produced in July 1993. The first production modules are now nearing completion.

### **F-22 MCMs**

The digital aspects of the F-22 MCM designs used the same methodology and toolset as the Comanche MCM designs. The results were also similar. The tools provided a good environment for the use of concurrent engineering practices.

The analog aspects of the F-22 MCM designs have been piecemeal, as compared to the digital designs. The Cadence design platform provides an "Analog Workbench" tool, but it is not directly linked to the Allegro layout tool. The result is that the constraint driven design approach used for purely digital designs cannot be incorporated for mixed signal designs. There are no tools which can adequately extract the required geometric information from the layout database to support correct simulation of transmission line properties, noise, crosstalk and other parasitic effects introduced by the MCM substrate.

Our designers have been able to use the Greenfield Analysis tool to extract circuit models from the MCM netlist, but the result is a simplified lumped parameter model. This lumped parameter model is sufficient for quantifying switching noise from the digital devices, and is good for determining the requirements for power and ground decoupling capacitors for each digital ASIC. The Greenfield tool has also been used to analyze the effects of high numbers of simultaneously switching outputs between large digital ASIC. However, the tool has proved ineffective for analyzing high frequency analog performance.

The result of the lack of synergy of the analog tools has been a reliance on manual calculations; and on the experience and intuition of the analog designers. The "Harris GASD Fastrack" tools did prove adequate for modeling the performance of the analog ASICs supplied by Harris Semiconductor. The problem was in developing good models for the effects of the passive elements of the substrate circuitry, and how the analog chips interacted with the substrate and with each other. Tools were not available which could provide the 3 dimensional analyses required for MCM level simulations. This lack of tools made the analysis of signal noise difficult and tedious.

Despite the lack of synergistic analog tools, the application of concurrent engineering methodology did prove effective for the F-22 mixed signal MCMs. GASD was able to get good information from the MCM supplier (CTS) on the passive circuit characteristics of interest, such as the dielectric constant, the electro-magnetic properties of the MCM substrates, and the manufacturing constraints (line width, pitch, etc). The primary problem was that after this

information was collected, there were no analog tools to fully exploit this information.

After the mixed signal MCM layout was completed, the Allegro tools provided a direct netlist output for CTS, the MCM supplier. As with Comanche, this hand-off was accomplished smoothly for the F-22 Program. MCM prototype modules were successfully delivered in February 1993.

### **MCM Test Data Generation**

The narrative which follows provides a background discussion of the Design-for-Test (DFT) features used by Harris GASD. This discussion includes descriptions of the various implementations used for different Harris GASD programs.

### **Design for Testability (DFT)**

Harris GASD has developed a Design-for-Test (DFT) methodology for the digital logic in complex MCMs, which is based on reusable BIT/BIST scan test modules. In its full implementation, each individual digital ASIC chip incorporates Built-in-Test (BIT) internal scan logic for all scannable register elements (such as flip flops), and boundary scan to control the ASIC I/O signal pins. This design-for-test methodology is modular. Each program considers their own need and selects either a complete or a partial implementation to achieve the testability level required for a given application.

Each ASIC design usually includes logic for an "On-Chip-Monitor" (OCM), which is a control port used to load up to scan paths to their initial states, control device testing sequences, and read back the resultant scan states.

At least one ASIC device per MCM usually incorporates an "On-Board-Monitor" (OBM) which is a semi-autonomous test controller. This OBM device communicates with the OCM ports via a shared ETM-Bus internal to the MCM. The OBM has the capability to control Built-in-Self-Test (BIST) sequences for each of the ASIC devices with an OCM port. The BIST controller in the OBM uses Linear Feedback Shift Register (LFSR) logic to generate pseudo-random scan patterns, and compares the final results to a known good test signature. This OBM device communicates with the world outside the MCM via a TM-Bus which is compatible with DoD JTAGs and IEEE 1149 standards.

This method allows very high structural fault coverage of all the digital logic and electromechanical interconnects in an MCM to be accomplished by simply issuing a few simple commands over the JTAGs bus to the OBM, and then giving the OBM the required number of clocks to complete a given BIST sequence (usually on the order of 1 to 10 million clocks). The combination of a master OBM and several slave OCMs allows a complete BIT and BIST solution without excessive overhead. Most of our designs realize greater than 95 percent detection of "stuck-at" faults with less than 10 percent total circuit overhead for the internal scan, boundary scan and OBM/OCM logic.

The OBM/OCM provides a unified structural test methodology which can be exploited first at the die level, and then used again for MCM level testing, again

at the PWB level, and be finally used to support system level diagnostics. This structural testing is necessary but does not fully cover all the test requirements. What structural testing does is assure that there are no point defects caused by errors in the MCM substrate, the MCM manufacturing process, or by latent defects in the integrated circuits. Behavioral and functional testing must also be performed to ensure the reliability of the final product.

The purpose of functional testing is to validate that the MCM can correctly perform all of its intended state machine functions in its target application. Behavioral testing establishes that the MCM functions correctly for all specified conditions. This includes factors such as timing margins and voltage noise margins for signals, power supply levels and the module temperature.

An important part of the design process is deciding how much testing rigor to impose at the die level versus the module level. The cost of rework versus the cost of die level testing is one part of this tradeoff. Another concern is that the MCM level testing cannot establish how much timing and voltage margin there is for chip to chip interconnects after the MCM is assembled. For both of these reasons, GASD has made a significant effort to develop "at-speed" testing techniques for use at the wafer and die level. Our current wafer probe capability can support speeds up to 600 MHz for a limited number of pins (up to 32), and 100 MHz for the remaining pins (practical limit is about 300).

After the MCM is assembled; structural, functional and behavioral and must be accomplished at the MCM level. The structural testing relies on the OBM/OCM architecture described earlier. Functional and behavioral testing often require a piecemeal approach. Digital testing requires MCM level functional and timing simulations, which are translated for use by the tester. The testing of analog I/O pins and Fiber-Optic interfaces may require the careful insertion of either analog multiplexers or loop-back structures to allow analog functions to be isolated and tested at the MCM level. In the concurrent engineering model, the test engineers are part of the MCM design team, so that such concerns are not neglected. This combination of built in test features has allowed Harris GASD to deliver reliable product for a variety of military applications.

### **Brilliant Eyes MCMs**

The success realized by GASD in the use of concurrent engineering for design to manufacturing can be sustained through to test generation, for purely digital designs. On the "Brilliant Eyes" program, we were able to translate a Boolean representation of the memory modules into a "C" code model, and then write "C" procedures which generated exhaustive test patterns. Because memory modules designs use tightly structured logic, module level test generation is relatively trivial, but it does nevertheless illustrate how concurrent engineering applies to test generation. The timing and format limitations of the target test system, in the case an HP82000, were formally captured in technical narrative and given to design team. The generation of the "C" code was performed as a joint effort by the design engineers and test engineers. The Valid Logic simulation tools were used to establish that the Boolean model of the module stayed closely coupled with the electrical design. This allowed the test generation effort, which was driven from the same Boolean model, to proceed in parallel with the detailed

MCM design and layout effort. The output of the "C" model was then translated via TSSI tools into the format required for the HP82000. The resulting MCM level test patterns have been verified on the Proof-of-Design (POD) units delivered by the module supplier, CTS.

### **Comanche MCMs**

The digital aspects of MCM level testing for the two Comanche Mixed Signal MCMs were managed using the SYNOPSIS tool. SYNOPSIS was used at the VHDL level to inject scan paths for both internal scan of the digital ASICs, and boundary scan to test the chip to chip interconnects. The MCM and ASIC designs for Comanche used a partial implementation of Built-in-Test (BIT) which included internal chip level scan plus boundary scan only.

The TESTSCAN tool was used to the structural test vectors for validation of the assembled MCM. Functional and behavioral test vectors were generated using the LMSI tools. These various test vector pattern sets were translated by the TSSI tools for the target test system. Testing was accomplished on the transmitter and receiver circuitry using loop-back test techniques.

### **F-22 MCMs**

The testing approach used for the F-22 MCMs was similar to that used for Comanche. The main difference is that a full implementation of OCM and OBM structures was used. This allowed full Built-in-Self-Test (BIST) to be accomplished at the MCM level, in contrast to the BIT methodology used for Comanche. This allowed 98 percent coverage of stuck at faults at the die level to be accomplished during MCM level testing. The BIT/BIST approach also allowed 100% coverage of the chip to chip interconnects on the substrate, and 100% for the signal paths from the MCM I/O pins back to the chips. The combination of BIT and BIST also reduced the required number of test vector to reduced from about 8 million down to about 2 million, while still achieving 98% fault coverage.

### **Next Assembly Level for MCMs**

The printed wiring boards (PWBs) used on the F-22 and Comanche Programs were designed using the Allegro layout tool. During board design, this tool had serious problems handling thermal vias and buried electrical vias. There was no provision for identifying vias placed only as thermal conduits, and the layout system would attempt to remove them because they were not related to the electrical netlist. A patch was added to the software to identify the thermal vias as power vias, but this caused problems with the power simulation. These nuisance factors made the design process awkward. The tools for modeling thermal effects were not sufficient to handle the thermal interface from the MCM to the board. These calculations were required to be performed manually.

The PWB layout tools also do not provide an easy path to extract the information needed to develop thermal models for power dissipation, and analog models needed for power and ground routing.

Another problem lies in the area of test vector generation. The multiple chip simulations supported on the Valid Logic platform emphasize two aspects of rigorous testing. One aspect is worst case device behavior modeling to establish timing and voltage margins. The other is the generation of rigorous test patterns with high fault coverage to rule out any random point defects and verify functionality. The use of BIT and BIST via scan path testing was used to establish good fault detection at both the die and module level. All of these test approaches assume that the purpose of testing is verify functionality and timing at actual system clock speeds with a high speed tester such as the HP82000. The problem comes after a fault is detected.

This combination of structural, functional and behavioral tests are sufficient for verification and screening, but are not necessarily sufficient for isolating failures for either module or board level rework. At this point, there will be many possible failure mechanisms to be considered. The failure could be caused by a latent defect in the MCM or PWB, opens or shorts induced by the MCM attachment to the PWB, a die failure induced by handling or temperature stresses during solder reflow, or a host of other possibilities.

There are really two issues in the area of fault isolation. First, the board level testing usually uses in-circuit board testers which are designed to use "guided probe" style diagnostics. However, the diagnostic software currently available for in-circuit testers does not support devices with the complexity of these MCMs. The second issue is the test patterns generated for MCM and board level testing. The boundary scan patterns, if cleverly designed, could be organized into a set of small stand-alone patterns which test the various levels of interconnects both inside and outside of the MCM. Existing simulation tools would provide at least limited support of such diagnostic patterns. Future test tools should be upgraded to fully support fault isolation in addition to fault detection.

### **Time Lines to Project Completion**

The successful experience by Harris GASD programs using MCMs in the use of concurrent engineering for design to manufacturing and testing also carried through to the management of the MCM production. The plan for module level production of the MCMs was developed using the Integrated Manufacturing Operating System (IMOS) software tool. IMOS was used to manage and track the pilot production of the Proof-of-Design (POD) modules by CTS, our MCM supplier. Harris GASD procures all of the ASIC die used for the MCM assemblies, and delivers "known good" die to the MCM suppliers. The material management and part procurement activity is managed with the Parts Control and Tracking System (PCATS) software tool. The IMOS and PCATS tools share a common technical database with the Cadence design environment. This system has proven successful for the delivery of both Proof-of-Design (POD) modules and production MCMs.

### **Data Transfer Requirements**

The process of designing an MCM requires data from many different sources. This information includes customer requirements, performance and constraint data from chip foundries and substrate suppliers, and simulation results from

software tools outside of the MCM design platform. This section offers an overview of the various categories of data which must be ported into the MCM design platform, for use by the various engineering disciplines.

### **Mechanical Design**

- Supplier Base Capabilities
- Die Size
- Die Footprints
- Environmental requirements
- Vendor design rules
- Thermal Analysis

### **Thermal Design**

- Chip Supplier data sheets
- Environmental requirements
- Vendor design rules
- MCM size, lead count, power
- Package Thermal Characteristics

### **Reliability**

- Chip Supplier data sheets
- Environmental requirements
- Vendor design rules
- MCM size, lead count, power
- Thermal Analysis
- MCM manufacturers historical data

### **Electrical Design**

- Functional specification
- Simulation data
- I/O numbers
- Electrical guide lines
- Netlist
- Vendor design rules
- Gate driver/receiver models
- Chip specifications and models

### **Layout Design**

- Chip specifications and models
- Critical signals
- Layout constraints
- Die Size

- Die Footprints
- MCM size, lead count, power
- Electrical schematic
- Netlist
- Vendor design rules
- Gate driver/receiver models
- Thermal Analysis

#### **MCM Manufacturer**

- Electrical schematic
- design database
- Manufacturing procedures
- plots and drill tape
- parts lists
- documentation
- test fixtures
- test vectors
- test spec and procedure

#### **Manufacturing Systems**

- Electrical schematic
- design database
- parts lists
- documentation( drawings, plots)
- test fixtures
- Manufacturing procedures

#### **Current Process Problems**

The following narratives and tables discuss problems, causes and "should be" solutions for issues encountered in our MCM design experiences.

#### **Ability to Perform Simulations**

MCMs sometimes use parts not designed at Harris GASD (off the shelf die). There are rarely good simulation models available for these off the shelf die. This leaves the designer with three choices, either to write a new software model for simulation, to use a hardware modeler, or to forgo simulation.

We can easily simulate ASICs, but we cannot easily simulate MCMs. MCMs may have mixed technology designs (e.g., CMOS, ECL, TTL, GaAS). Current simulators have a hard time handling mixed technology designs, primarily because of the lack of coherent libraries. A designer may have access to a CMOS library and an ECL library, but the two libraries won't play together unless both libraries use simulation parameters in the same way.

MCMs, like the F-22 modules, may have mixed signal designs (digital and analog). Mixed signal simulators do not exist, and simulations can not take into account the effects of analog signals on digital data and visa versa. Typically there simulations are done separately and the results manually integrated.

MCMs have a higher total gate count than ASICs because they use ASICs as building blocks. Simulation time is usually proportional to gate count, so MCMs simply take longer to simulate than ASICs.

MCM simulations are needed not only to prove out designs but more importantly to generate behavioral and functional test vectors. An overview of the typical multi-technology MCM behavioral and functional test vector generation is shown in Figure 4.13. A "should be" solution with a single simulation environment is shown in Figure 4.14.

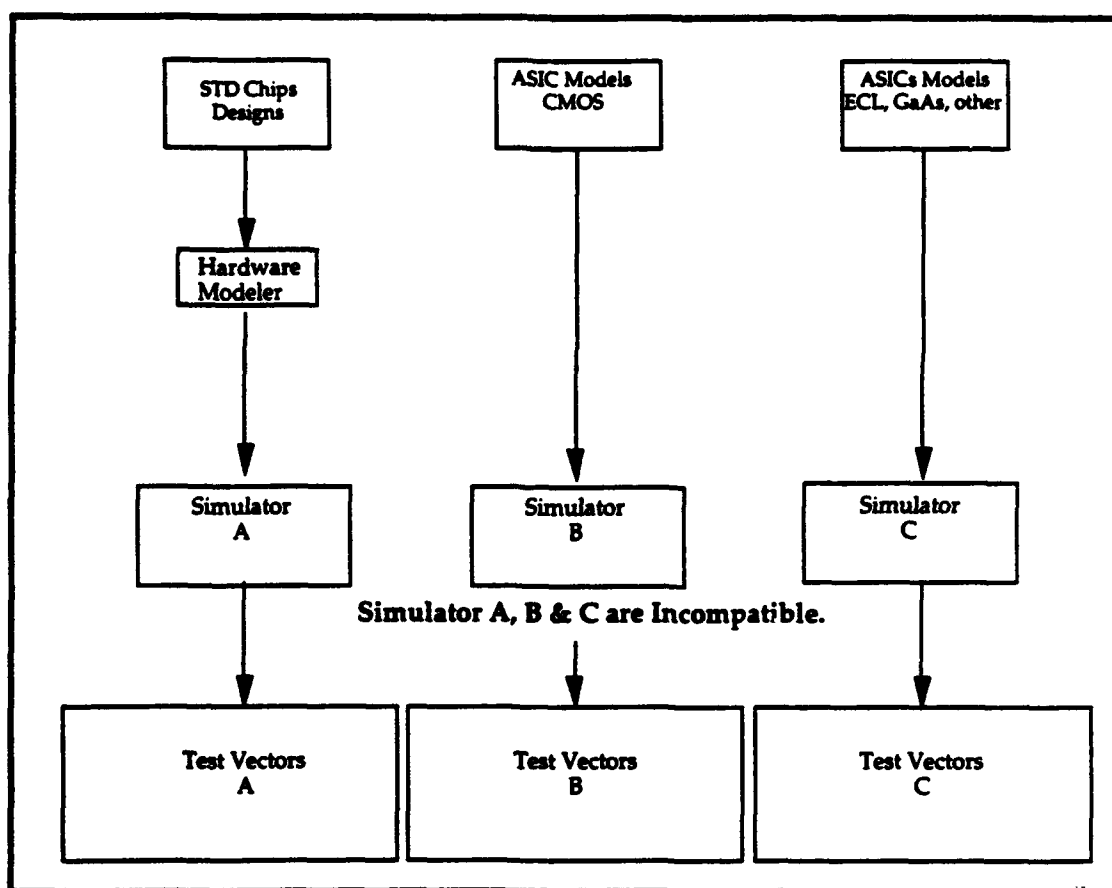


Figure 13 Multi-Technology MCM Simulations (As Is)

These and other MCM simulation problems are summarized with the "cause" and the "should be" in Table 4.4.



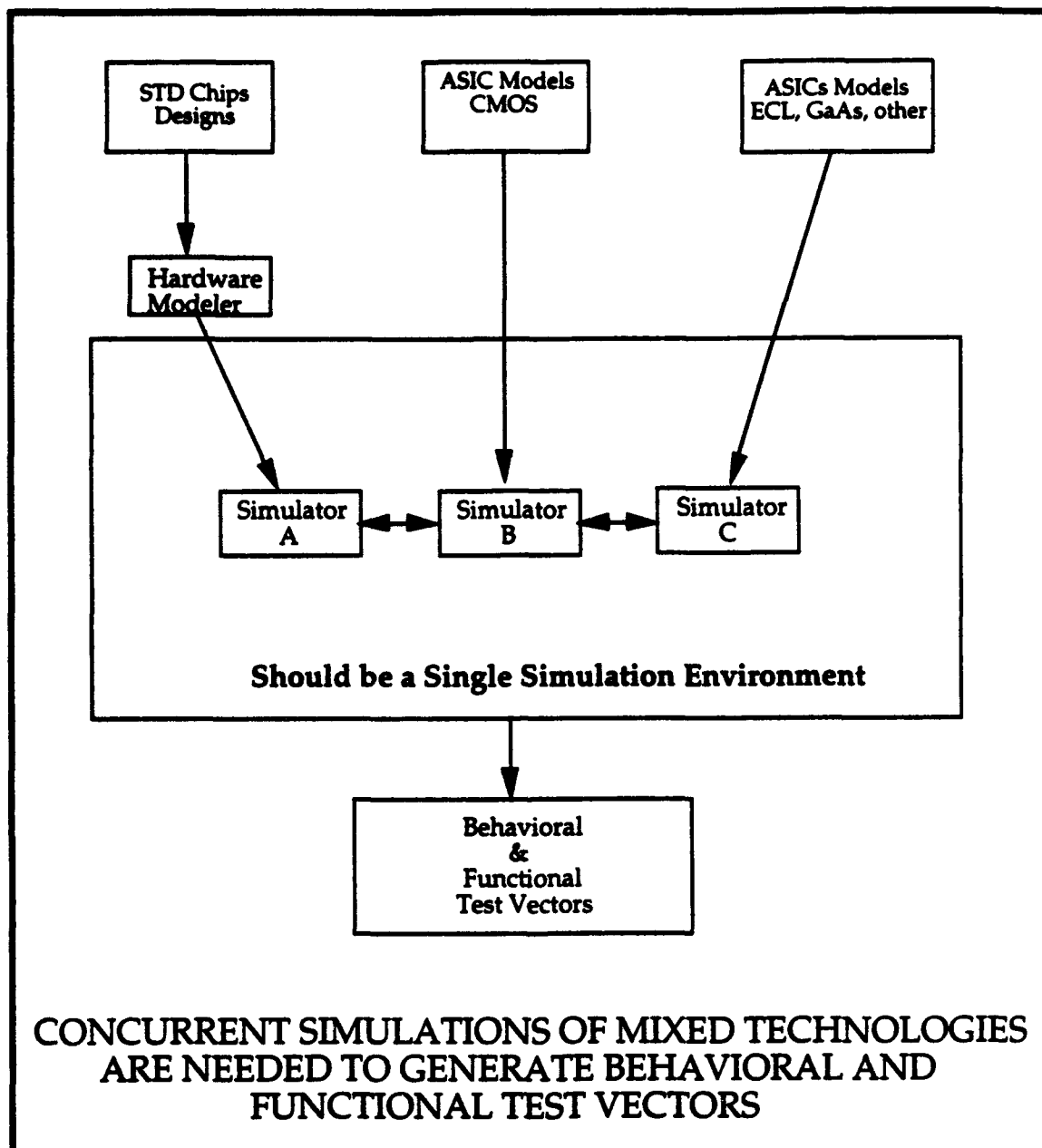


Figure 4.14 Multi-technology MCM Simulations (Should be)

PROCESS PROBLEMS, Ability to Perform MCM Simulations			
ITEM	PROBLEM	CAUSE	SHOULD BE
Gate Model Library from Different Suppliers	Incompatibility between suppliers models.	Unable to get timing information between ASICs from different suppliers.	Heterogeneous Library Models in one simulation environment.
Analog Signals	Lumped parameter models.	Simulations lack sufficient accuracy.	Need distributed parameter models.
Mixed Signal MCM's	Incompatible tool for digital and analog simulations.	Tool sets do not handle mixed analog/digital.	Compatible tool sets that will handle analog and digital ASICs.
Tool Interfaces	Incompatibility between high level design languages and simulators.	Different models are used by high level tools versus simulator tools.	Need to provide better interfaces between tools.
Multiple Asic MCM's	Tools cannot simulate many Asics.	Simulators can't handle MCM's with many Asics.	Tools with multi-chip simulation capability.
Model Hierarchy Level	Cannot perform multiple chip simulation with different ASICs and standard logic devices represented with different model types.	Each simulator is focused on its own preferred model type (gate level model, VHDL, behavioral model, etc.), and models must be translated.	Need a true multi-level hierarchy simulation tool which does not require translations between model styles.
Worst Case Temperature Analysis of mixed technologies.	Cannot perform true worst case temperature analysis of mixed CMOS/ECL/GaAs.	Simulators rely on worst case corners approach, which does not properly model how each technology really changes over temperature.	Need simulators designed for mixed technologies, which can exploit temperature performance models for the various technologies. Also need standardized model format for entering this information into technology databases.
Hardware Accelerators	Models for different hardware accelerators not compatible (for example IKOS versus ZYCAD).	Models are developed by silicon suppliers for each technology for a particular target accelerator.	Standardized model format for hardware accelerators, and set of translation tools for each accelerator to/from the standard format.

Table 4.4 Ability to Perform MCM Simulations

## Design for Testability (DFT)

The software tools should automatically handle insertion of JTAG interface to MCMs.

The current reality is that incomplete, improperly formatted, or incorrect data is handed off between Design and Test, mostly because no good definition exists of what the hand-off package should be. The result is the Designer and the Test Engineer must both spend a great deal of time iterating on the test data until the test program is complete. Figure 4.15 illustrates the difficulty of using multiple simulation tools to generate the MCM test programs. Figure 4.16 shows an improved environment with additional tools to ease the translation effort.

An overview of the design for testability (DFT) problems are summarized with the "as is" and the "should be" in Table 4.5.

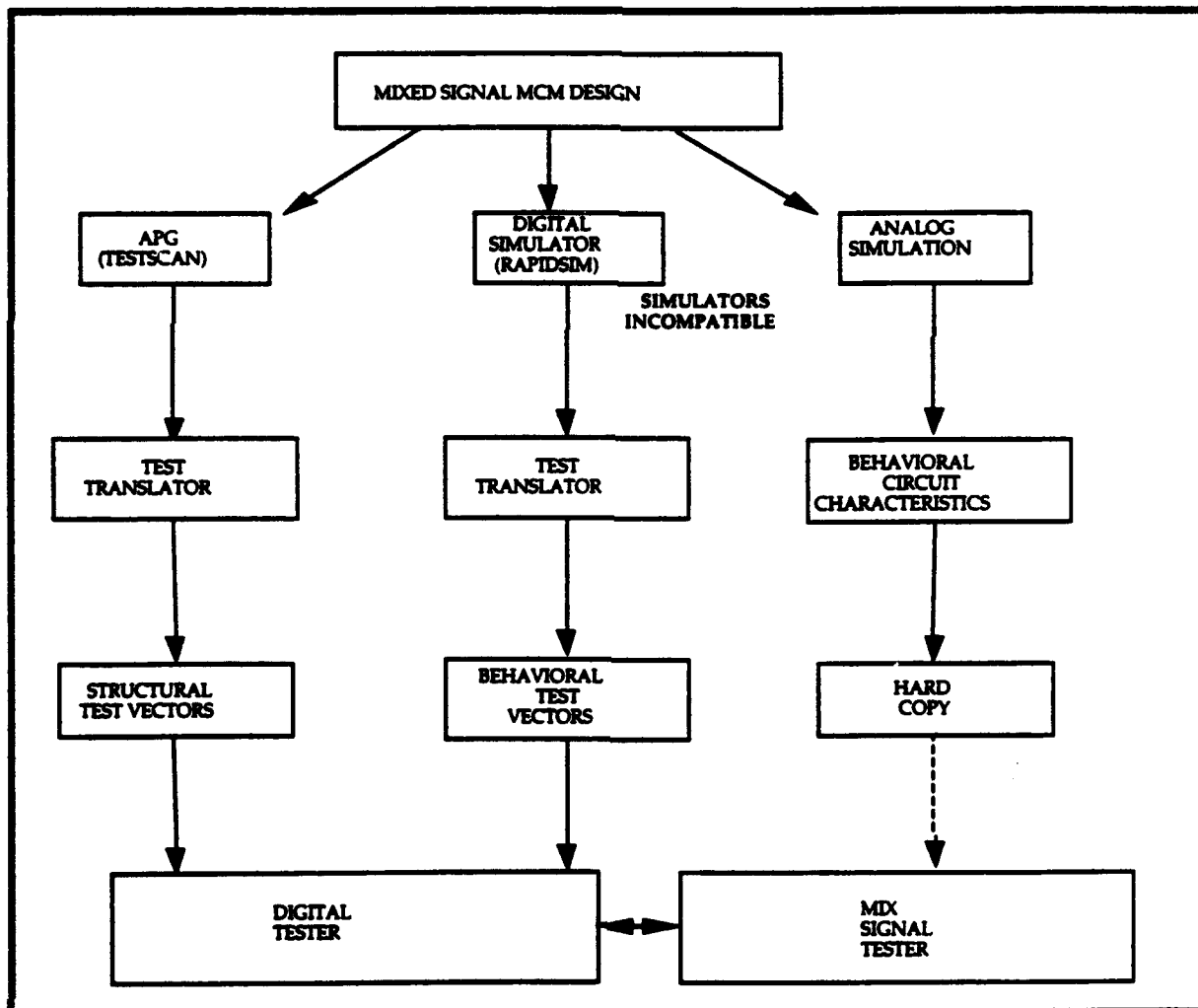


Figure 4.15 Design for Testability and Test Vector Generation (As Is)

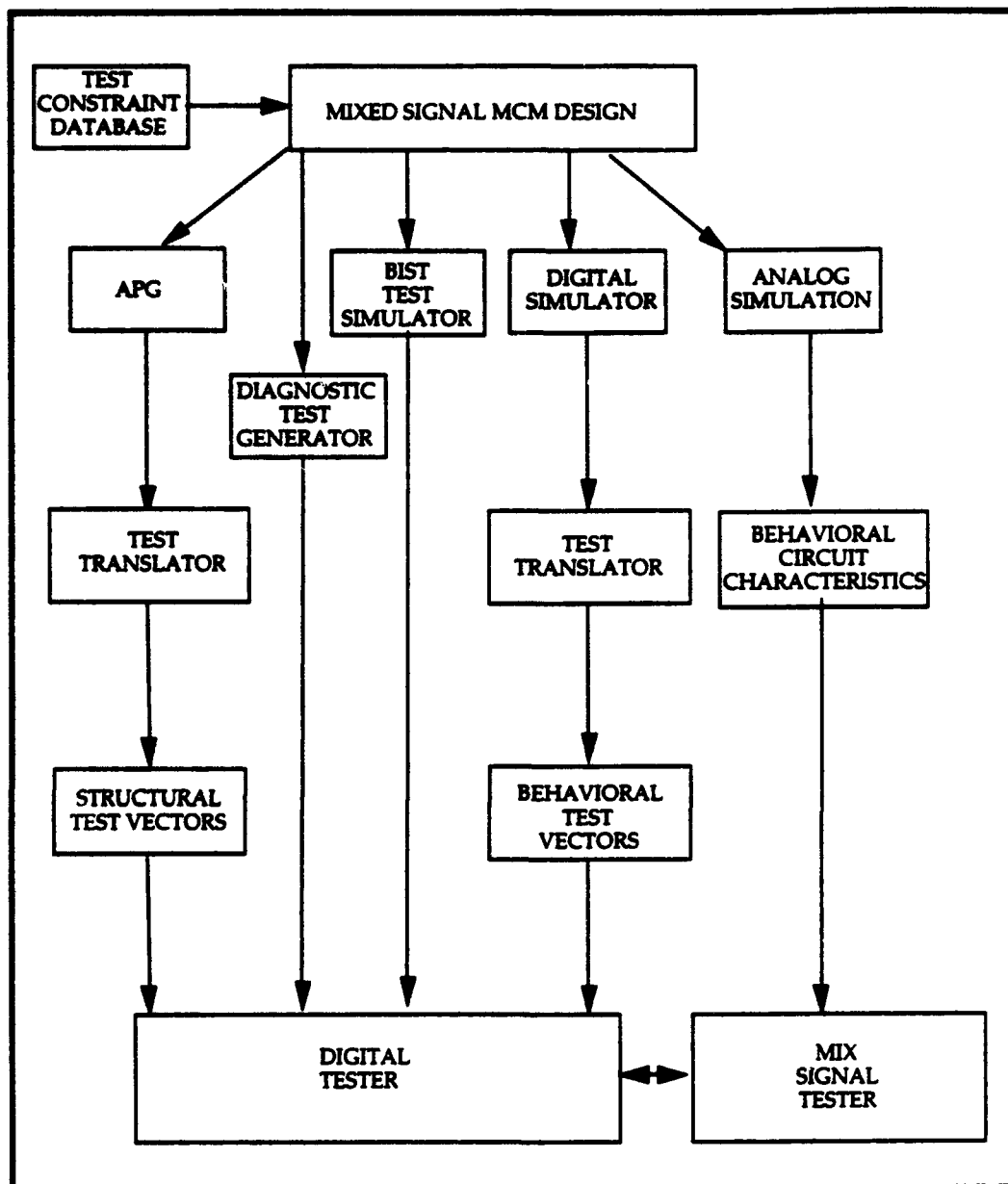


Figure 4.16. Design for Testability and Test Vector Generation (Should be)

PROCESS PROBLEMS, Design for Testability (DFT)			
ITEM	PROBLEM	CAUSE	SHOULD BE
Analog and Mixed Signal Testing	Design for Test tools neglect analog behavior, emphasize structural testing of digital functions.	Difficult to describe analog behavior, lack of standards.	Simulation tools which can describe MCM level analog behavior in a form compatible with analog test equipment.
Diagnostic Testing	Test patterns difficult to use for fault isolation of bad MCM, to support rework.	Structural test tools such as TESTSCAN emphasize total fault coverage, but ignore diagnostics and fault isolation.	Tool which supports a multi-segmented approach: a set of independent test patterns to test each chip to chip and chip to module I/O pin interconnect path. Also need real-time diagnostic test software (guided probe) which can operate at MCM level of complexity.
Acceptance Testing	Test patterns too large for acceptance testing (many millions of test vectors).	Structural test tools such as TESTSCAN emphasize total fault coverage for each ASIC, plus the entire MCM (millions of vectors). Behavioral and functional testing is exhaustive (many more millions of vectors).	Tool which generates a limited set of structural, behavioral and functional test patterns; based on compromise between cost of testing and level of testing rigor required.
Proof-of-Design (POD) Testing	Limited by concerns for cost of acceptance testing.	Tools such as TESTSCAN cannot distinguish between various levels of required testing rigor.	Tool which can generate limited diagnostic and acceptance testing as described above, and then "pull out all the stops" and generate a set of many of millions of vectors for Proof-of-Design (POD).
Built-in-Self-Test (BIST)	Existing simulators cannot predict "signature" for BIST based on LFSR and internal SCAN paths. "Signature" is unknown until ASIC or MCM level testing is completed.	Software cannot handle large number of calculations needed to calculate "signature" based on LFSR and internal SCAN paths.	Better simulator software, which can create a compressed Boolean model of BIST circuitry and calculate the "signature".

Table 4.6. Design for Testability (DFT)

## **Automatic Test Vector Generation**

The current reality is that incomplete, improperly formatted, or incorrect data is handed off between Design and Test, mostly because no good definition exists of what the handoff package should be. The result is that Design and Test spend a great deal of time iterating on the test data until the test program is complete. The next generation of tools should support functional and behavioral simulations constrained by the limitations of the tester hardware. Currently, these problems are often detected by the tester translation software, such as TSSI, after the simulations have been completed. Some of these test vector generation are summarized in Table 4.7.

The tools should also allow the generation of different groups of test vectors for acceptance and fault coverage testing versus diagnostic and fault isolation testing. The existing combination of functional, behavioral and structural patterns is adequate for verifying that a module has been assembled with no manufacturing defects at chip or MCM level. Tools are needed which facilitate the diagnostic and fault isolation tests required to support repair and rework of a bad MCM.

The generation of functional vectors is currently a compromise between cost of test and sufficient testing rigor. Exhaustive simulations are often needed to address specific aspects of MCM performance. The result is a very expensive test program with many millions of test vectors. Future simulation tools should support limited subsets of functional tests, to control the costs of acceptance testing. Clever use of BIT/BIST design can cover the risk that die were damaged during MCM assembly, without repeated all the exhaustive testing for each MCM. The exhaustive testing could then be limited to Proof-of-Design testing, with significant cost reduction.

Without better linkage to tester specific parameters such as vector timing, strobing and edge placement, the designer cannot know if these parameters are sufficiently covered in the functional testing. This is an important issue to the generation of test vectors for performance verification and Proof-of-Design testing. Future simulation tools should be better coupled to the target tester to close the loop on these issues. For example, the designer may be concerned with checking the MCM circuit design for layout induced noise which could cause functional errors. A provision to "back-annotate" the actual timing of the tester could be used to validate the intended purpose of specific test vectors pattern sets.

PROCESS PROBLEMS, Automatic Test Vector Generation			
ITEM	PROBLEM	CAUSE	SHOULD BE
Behavioral Testing	Simulated timing environment exceeds ability of tester hardware. Simulation not coupled to target test systems.	Tester hardware has limitations on asynchronous behaviors, high data or clock rates, data waveform formats, etc. Simulation tools have no provisions to enforce timing rules based on tester limitations.	Tools should have features which enforce constraints for those simulations which are performed for test generation. Need ability to distinguish design only simulations versus those intended for test vector generation.
Functional Testing	Test patterns too large for cost effective acceptance testing at MCM level. Problem gets worse at next level of assembly, such as PWB.	Simulation software encourages exhaustive testing.	Tool which supports several levels of rigor for simulation, and allows generation of subset sufficient for acceptance testing.
Structural Testing	Structural test patterns not adequate for diagnostics and fault isolation to facilitate rework of bad MCMs.	No distinction between fault coverage (acceptance testing) versus fault isolation (diagnostic testing).	Tool which automates the generation of a set of independent test patterns to test interconnect paths: chip to chip, chip to module I/O pin, etc. Need ability to couple these patterns with real-time diagnostic test software (guided probe).

Table 4.7. Automatic Test Vector Generation

### Transfer of Design Rules

The start of the design process involves evaluation of the system requirements against the MCM supplier's design rules. The MCM design evolves from this evaluation, and it is constrained by the MCM supplier's process design rules. These limitations are often informal specifications in a non-standardized form. The restrictions are often negotiable in nature and usually represent what is easiest for the supplier to produce. If the buyer can't live with these limitations, compromise solutions are negotiated.

The supplier and the MCM designer (buyer) negotiate design rules which make it possible to produce the system requirements and at the same time are not too yield restrictive to build. These rules are captured and formalized. These rules are then distributed to the design team. The dissemination of this information is often informal. In many cases there is no centralized database to store and update this information.

Figure 4.17 illustrates the difficulty in getting information from the suppliers for use in the design process. Figure 4.18 shows a "should be" environment with the

information in a common database in machine readable form, and with standardized formats. Table 4.8 summarizes these and other transfer of design problems.

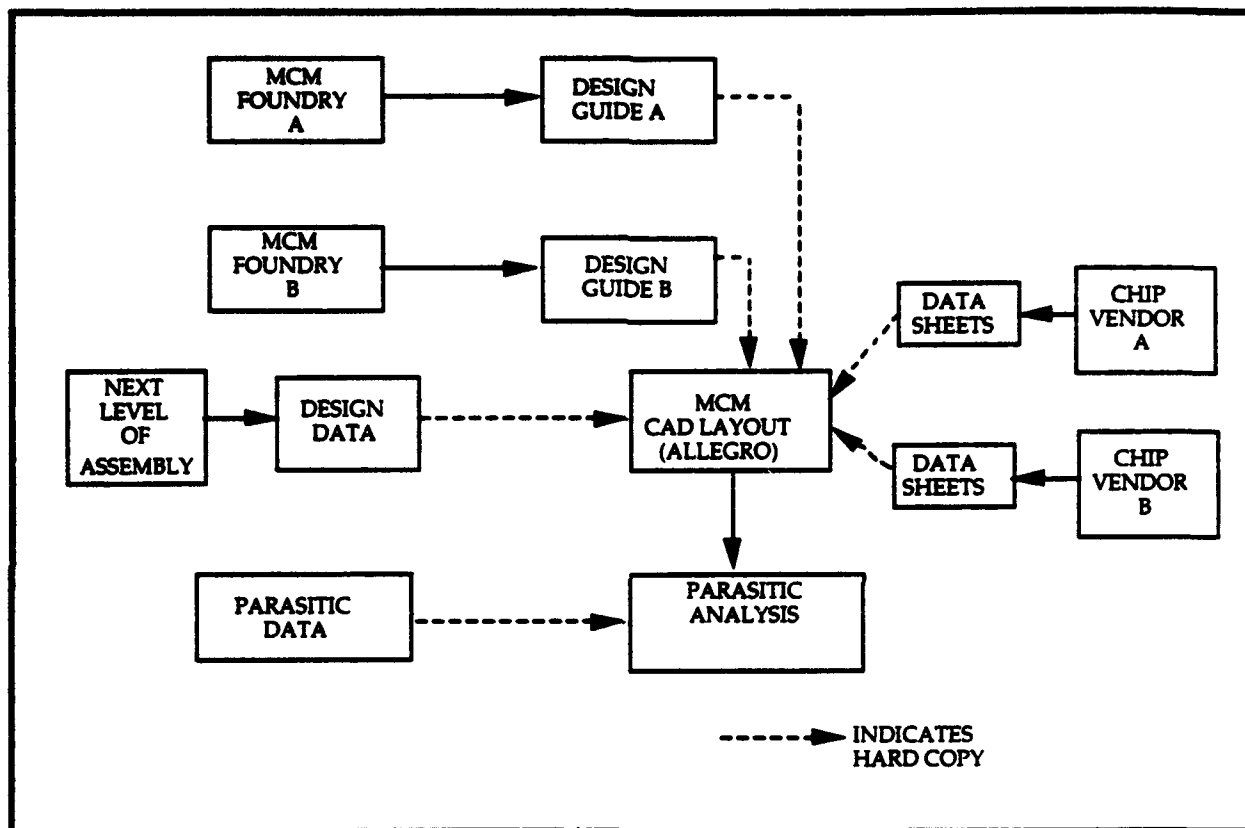


Figure 17. Transfer of MCM Design Rules and Mechanical Data (As Is)



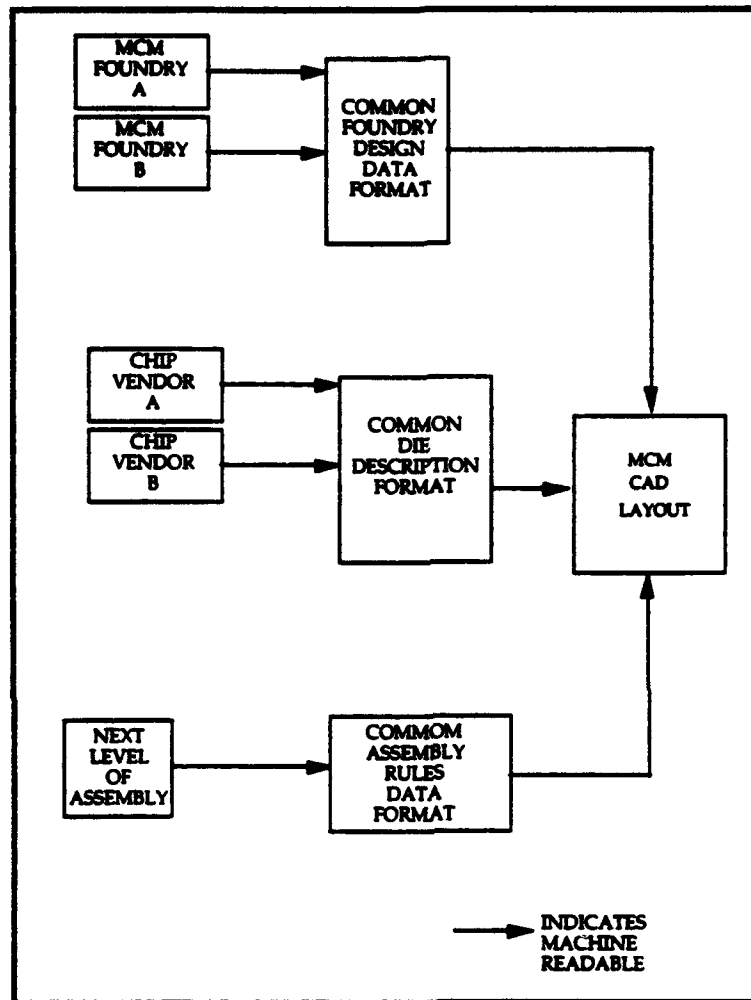


Figure 18. Transfer of MCM Design Rules and Mechanical Data

CESS PROBLEMS, Transfer of Design Rules			
ITEM	PROBLEM	CAUSE	SHOULD BE
MCM Process Foundry Data	Documentation is often informal.	No standardized documentation method	Standardized data in CAD Database.
MCM circuit parasitics	Layout tools do not include information on passive characteristics needed to calculate parasitic effects.	Layout tools are exclusively constraint driven (size, line width, pitch, etc.)	Technology database for each MCM supplier should include circuit characteristics in addition to layout constraints.

Table 4.8. Transfer of Design Rules

### Transfer of Mechanical Data

The chip supplier has the mechanical specifications for each chip. The MCM designer may select chips from several different suppliers to design the MCM. These different suppliers may have different mechanical data, in different units and in a different forms. This means that the data must be translated and formatted as required by the MCM layout tools. This translating leads to errors and delays, and increases the risk of design iterations.

Figure 4.19 illustrates the difficulty in getting chip and next level assembly data into the design process in machine readable form. Figure 4.20 shows a "should be" environment with the information in a common database in machine readable form, and with standardized formats. Table 4.9 summarizes the problems of mechanical data transfer.

PROCESS PROBLEMS, Transfer of Mechanical Data			
ITEM	PROBLEM	CAUSE	SHOULD BE
Chip Data	Information is available in differing formats requiring manual entry, which may cause errors or design delays.	Different vendors supply parameters differently.	Define a standard method to supply die mechanical information.
Data for Next Level of Assembly	Database does not include performance information needed for next level of assembly (such as PWB or SEM-E module).	Database is MCM specific. Information on external characteristics restricted to: footprint, size and weight.	MCM Database should include other information needed at next level, such as required soldering constraints, thermal factors, handling, etc.

Table 4.9 Transfer of Mechanical Data

## Applications Problems

The *schematic capture* tool relies on models of the chip to accurately define each integrated circuit. This data includes pin names, output type, function, electrical parasitics and driver and receiver models. This information is often difficult to obtain from the manufacturer because of its proprietary nature. The information, if obtained, still may not be formatted in a standardized form. Parameter values may be presented in different formats, which causes data incompatibility issues between suppliers. This has been a common problem with MCM designs.

The *schematic capture* tool may work well for chip level designs; however, MCM designs having several chips from different manufacturers may have multiple ground references with different naming conventions. The grounds may have different names but the same voltage potential. This problem causes manual editing of the netlist names. This added step adds both time and risk to the MCM design process. A similar but more serious problem is having the same name on different voltage potentials. This problem is much harder to detect because it requires manual review of the netlist.

The *auto routing* of an MCM may not always be a realizable. The auto router in many cases can't handle the additional requirements of stacked or spiral vias or the multiple padstack definition. Often the parameters necessary to setup the router are overwhelming to the layout designer. That lack of understanding of all the parameters and how they function may be a major reason why the designs are still routed manually. The designer may think it is easier to route manually than it is to understand all the parameters. There is also the perception that a highly constrained design is an unroutable design.

In the recent past *thermal vias* were only considered as part of the design if they are defined as a part and assigned a net name. The software usually attempts to minimize the number of nets with the same potential not recognizing the unique function of the thermal vias. The software must be able to incorporate these unique structures such as thermal vias into the layouts. Thermal vias could be handled to allow their properties to be quantified into a thermal parameter database so their thermal effects could be automatically used in the placement and layout of the MCMs.

*Noise analysis* which has been built into the layout software of several manufacturers handles noise analysis on a net by net basis. An module needs to be added to increase that analysis for the effects of power and ground switching noise. This software would consider the effects of bypass capacitors in the circuit and sheet resistance of the leads. An automated constraint system would address the power and ground noise effects taking into account the switching of the other components in the MCM.

Figure 4.19 illustrates the problems caused by using a multitude of tools, on different software platforms, and with incompatible formats. Each software tool is selected because it performs some necessary function not performed by the tools on the baseline design platform. This environment requires tedious translations to be performed to port data between the different tools.

Figure 4.20 below illustrates how a concurrent database could solve this problem, if each software tool could have a standard link into a shared database which contained both the design constraints and the MCM design information.

These application problems are summarized in Table 4.10.

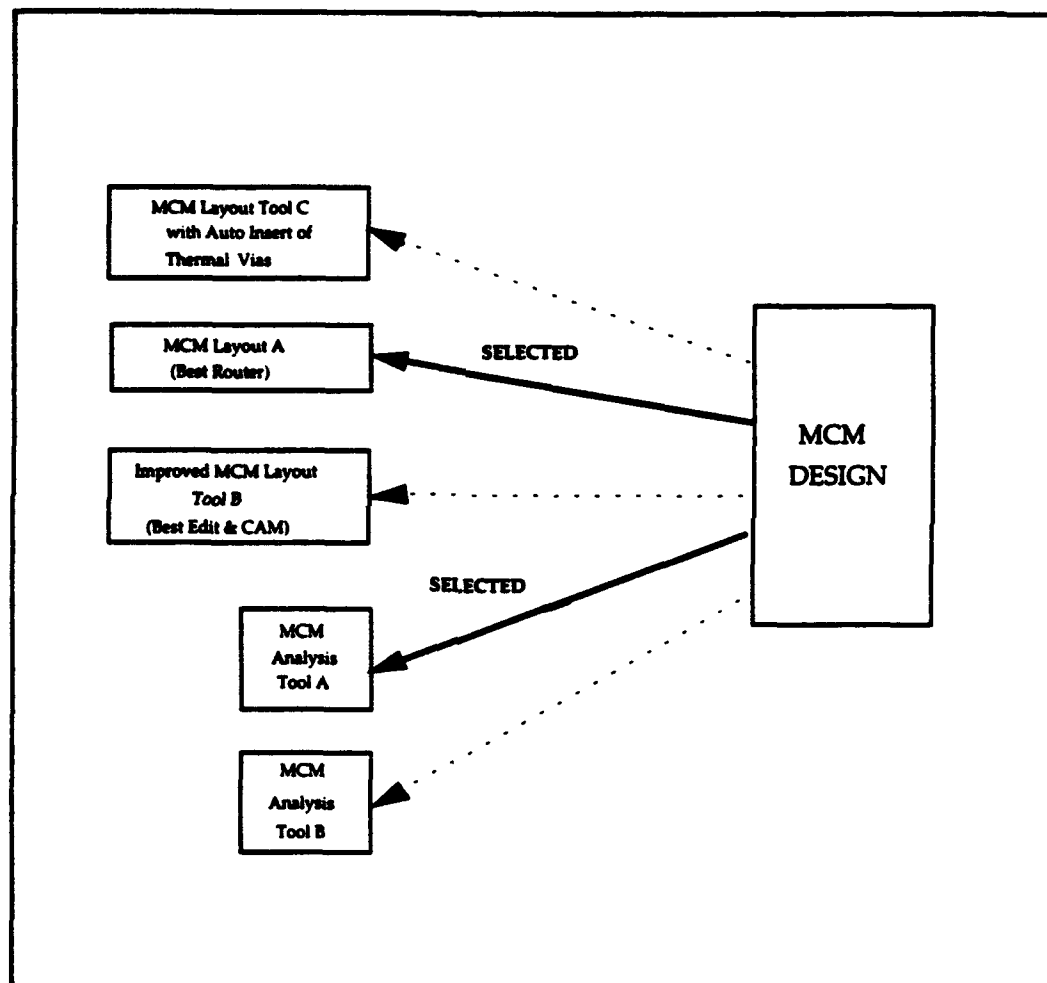


Figure 19. MCM Application Environment (As Is)

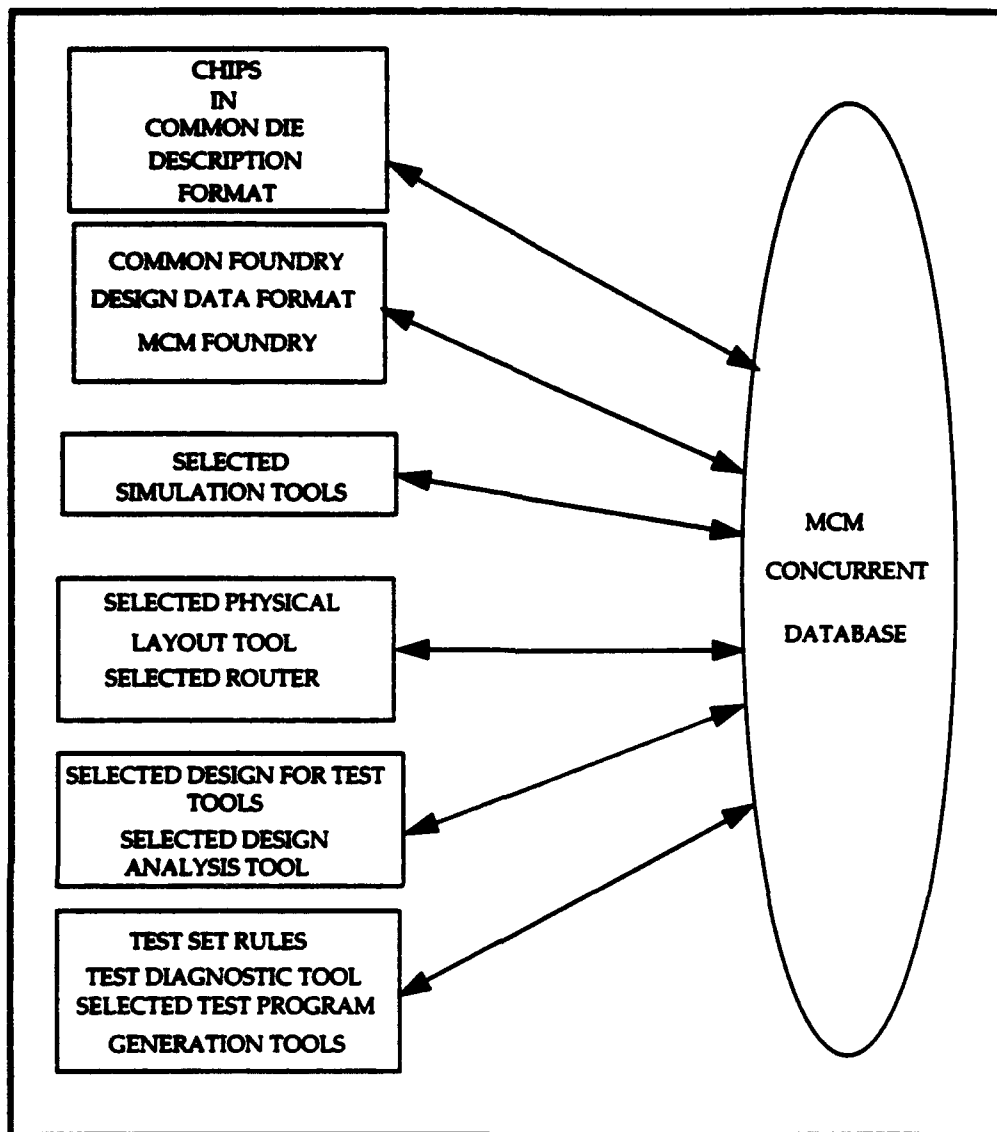


Figure 4.20. MCM Application Environment (Should be)

PROCESS PROBLEMS, Applications Problems			
ITEM	PROBLEM	CAUSE	SHOULD BE
Schematic Capture-Chip Models	Chip signal model not in library	Models difficult to obtain.	Have signal models in chip library.
Schematic Capture-Multi-Chip Grounds	Tool doesn't handle multiple grounds well.	Grounds can't be easily separated on MCM's.	Tool should handle redefining grounds for MCM's.
Router	Some manual routing	Tool not mature. Designer not comfortable with tool.	Better router tool. Standard data format so other more mature tools could be used. Education of designers.
Thermal Vias	Layout tools cannot consider effects of vias of heat transfer.	Layout tools have no provisions for other than electrical circuitry.	Need constraint driven features of layout tools to include thermal effects.
Power/Ground Switching Noise	Analysis of power and ground routing, switching noise, decoupling capacitors, etc., is tedious manual effort.	Greenfield analysis and other similar analog tools are not fully integrated into design platform.	MCM layout tools should be coupled with analog tools with automated constraint drive features to address power and ground noise issues.

Table 4.10 Applications Problems

## Desired MCM Design Environment

The desired MCM design environment needs to provide the way to share two types of information: parts management information and MCM design related tools and data.

Figure 4.21 illustrates how an MCM Concurrent Database could provide a shared platform to provide the various engineering disciplines access to this information using a common format. The management system tools we are using (PCATS, APIMS, and IMOS) work very well for managing the parts related data. These tools, which are on our shared computer network (LAN/MetroNet/InterNet), keep each member of the concurrent engineering team well informed on what parts have been selected, their availability, and delivery status.

One additional system we are in the process of adding to our data base is the Information Handling Services (IHS) on-line component data base. This system gives the user immediate access to supplier data books, military specifications, and other related component data. Each of these management system tools; however, are isolated islands within themselves.

The MCM concurrent data base would pull all of these tools together into a common design environment. This would allow the data to be passed among all of the management information and design tools. This would also provide all members of the design team immediate access to all pertinent data and design and analysis tools during the MCM design implementation process. The MCM concurrent database would store all MCM foundry data in a common foundry design data format. The chip data would be in a common die description format. The rules for the next level assembly would also be stored in the database. This would allow the team to have instant access to the latest design rules for both the foundry and the system level manufacturing.

On the design tool side, the MCM concurrent database would be able to pull in system design data, all available simulation tools, layout and analysis tools, and test tools. By using the MCM concurrent data base the MCM designer would only need to enter the required data once or directly import the requirements from any of the parts management tools. As part of the MCM concurrent database a translator would resolve simulation incompatibilities and differences between library models. This would allow the MCM design to be simulated accurately and more importantly would allow the behavioral and functional test vectors to be generated without repeating the simulations to meet the test system rules. The MCM concurrent database would be able to take advantage of the best features of any router and any layout tool available in the user's tool suite. The MCM concurrent database would also resolve the differences between analysis tools.

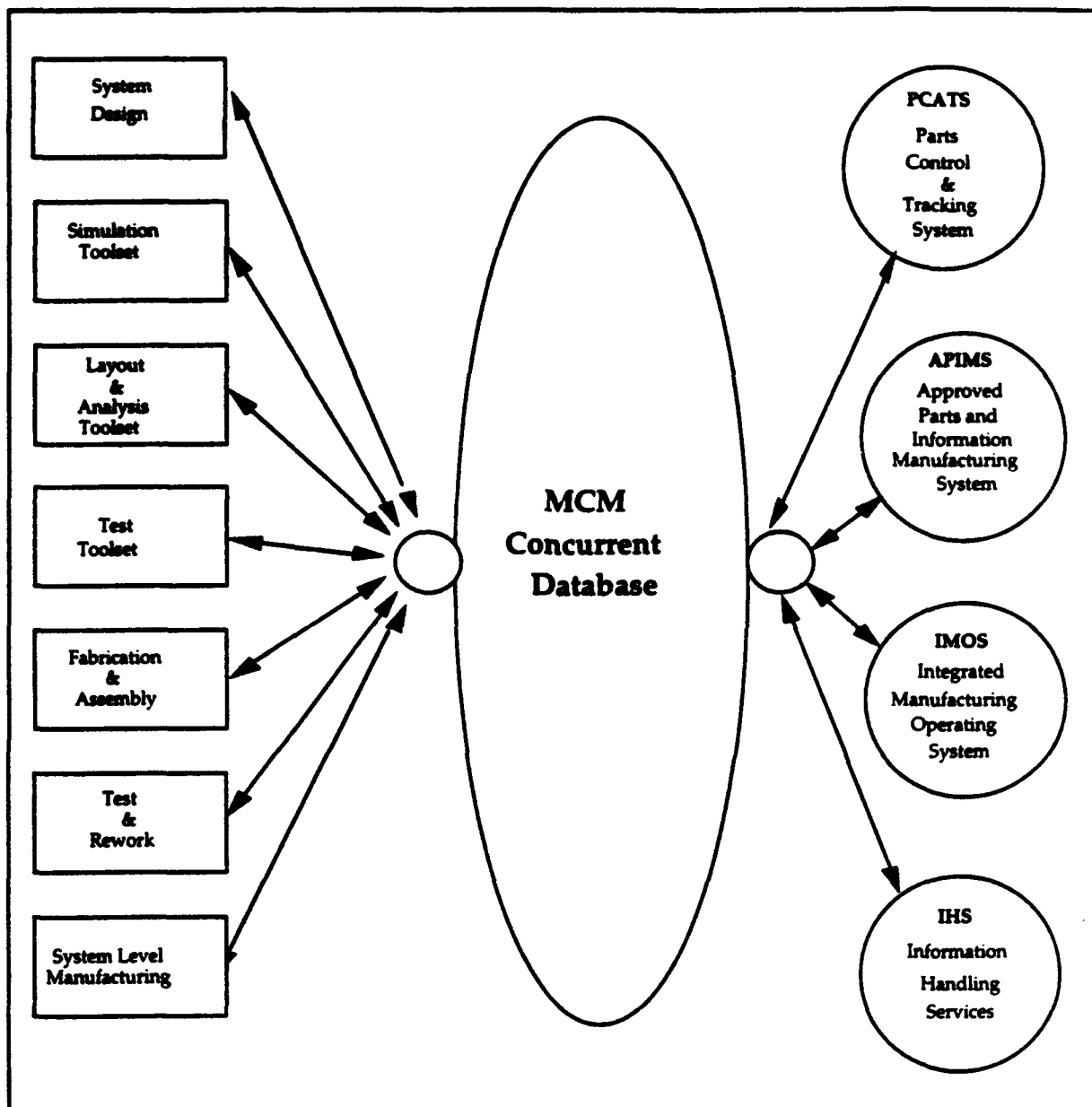


Figure 4.21. Harris GASD MCM Design Environment (Should be)

### Expected Improvement for Reduced MCM Design Cycle

In the current MCM design environment, too much time is spent gathering the supplier's design rules and translating this information into a format which is compatible with the software design platform. The sooner this information is available, the more efficient the design process can become. Ideally, this information should be in the MCM concurrent engineering environment and available to all of the engineering disciplines, before the MCM design effort is started.



A prime example of this issue is the efforts required to assure Design-for-Testability (DFT), and the subsequent simulation efforts required to generate test vectors for structural and behavioral testing. The DFT constraints are a mature part of the MCM design process at GASD, and the tools required to support testability are integrated into the Cadence design platform. The simulation constraints imposed by the Automated Test Equipment (ATE); however, are delivered to the MCM design engineers only in narrative form, and are less sharply defined than the general testability rules. Tester oriented problems are not detected until the translation from simulation results into test vector pattern sets. In an ideal design environment, these tester rules would be entered into the MCM Concurrent data engineering, and would be used to constrain the design of the simulation stimuli, for those MCM simulations which are intended to be used for test vector generation.

### **Fewer Design Iterations**

Design iterations are often caused by a misunderstanding of the supplier's design constraints early in the MCM design process. As the design rules mature, formal Design Rule Checks (DRCs) are performed, and violations surface which require design iterations to correct. The MCM concurrent engineering environment could be used to constrain the design process in the early stages so that the risk of required design iterations would be reduced.

There are other MCM design errors which are caused by incomplete simulations, or by modeling errors. The MCM concurrent engineering environment is not a panacea which can prevent all such problems from occurring. Nevertheless, the concurrent engineering database can ease the burden of performing some of the exhaustive simulations, which will allow a more robust design environment.

### **Greater Product Performance**

Both chip foundries and substrate suppliers tend to protect their yields by imposing conservative specifications for performance parameters. This conservatism flows down to the MCM designs which incorporate these chips and substrates. Potential system features are sometimes sacrificed or compromised because they exceed the supplier's specifications for the applied technologies.

Tighter limits are often negotiated with the suppliers, based on either system level requirements or knowledge learned during chip and MCM testing. These tighter limits could be added to the MCM concurrent engineering environment, and used to ease the constraints on subsequent design efforts. The availability of realistic parameter specifications in the MCM concurrent engineering environment will allow the designers to be more aggressive, and produce MCMs with extended performance characteristics.

### **Reduced Cost**

There are several reasons why the full exploitation of an MCM concurrent engineering environment should be expected to reduce costs. First, the Non-Recurring Engineering (NRE) costs of the design will be reduced because the design cycle times and the required iterations should both be reduced, saving

manpower costs. The material costs associated with the Proof-of-Design (POD) units will also be reduced because of fewer design iterations.

Second, the manufacturing costs should be reduced. The use of an MCM concurrent engineering environment should couple the design more closely to manufacturing constraints, which should result in a more producible design and better manufacturing yields. The Design-for-Testability (DFT) methodology discussed previously in Section will also produce a benefit to the manufacturing effort. The intelligent application of this DFT philosophy, together with the generation of more efficient test vectors for both diagnostic and acceptance testing, should help to contain the increasingly high cost of MCM testing.

### **Should be Flow**

The design flow already in place at Harris GASD has served us well in the design of fourteen MCMs. Concurrent Engineering practices have been used wherever they have been applicable, and this approach has been successful on five major military programs. This Concurrent Engineering methodology; however, has been taken to the point of diminishing returns, given the existing design platform. Further improvements will require the next generation of software tools.

### **Should be Tools**

The next natural step in the software tools for MCM design should be the application of a real-time concurrent engineering environment. From its initial inception, such an environment will aid the design process by providing a consistent source of information for all of the engineering disciplines. This will eliminate the redundant efforts of different engineers collecting the same data, but in differing formats. If the various engineering disciplines make their updates, additions and changes to this common database in "real-time", then this information can be available to other members of the design team instantly.

As the format standards for the design information mature, suppliers can be encouraged to provide the constraints and performance characteristics for the chips in substrates in a form compatible with these standards. This maturation of standard formats will reduce the required translations between different design and simulation tools.

As the software design tools evolve and begin to support true multiple technology simulations, the MCM concurrent engineering environment will provide a single repository for the various modeling information required to perform these MCM level simulations.

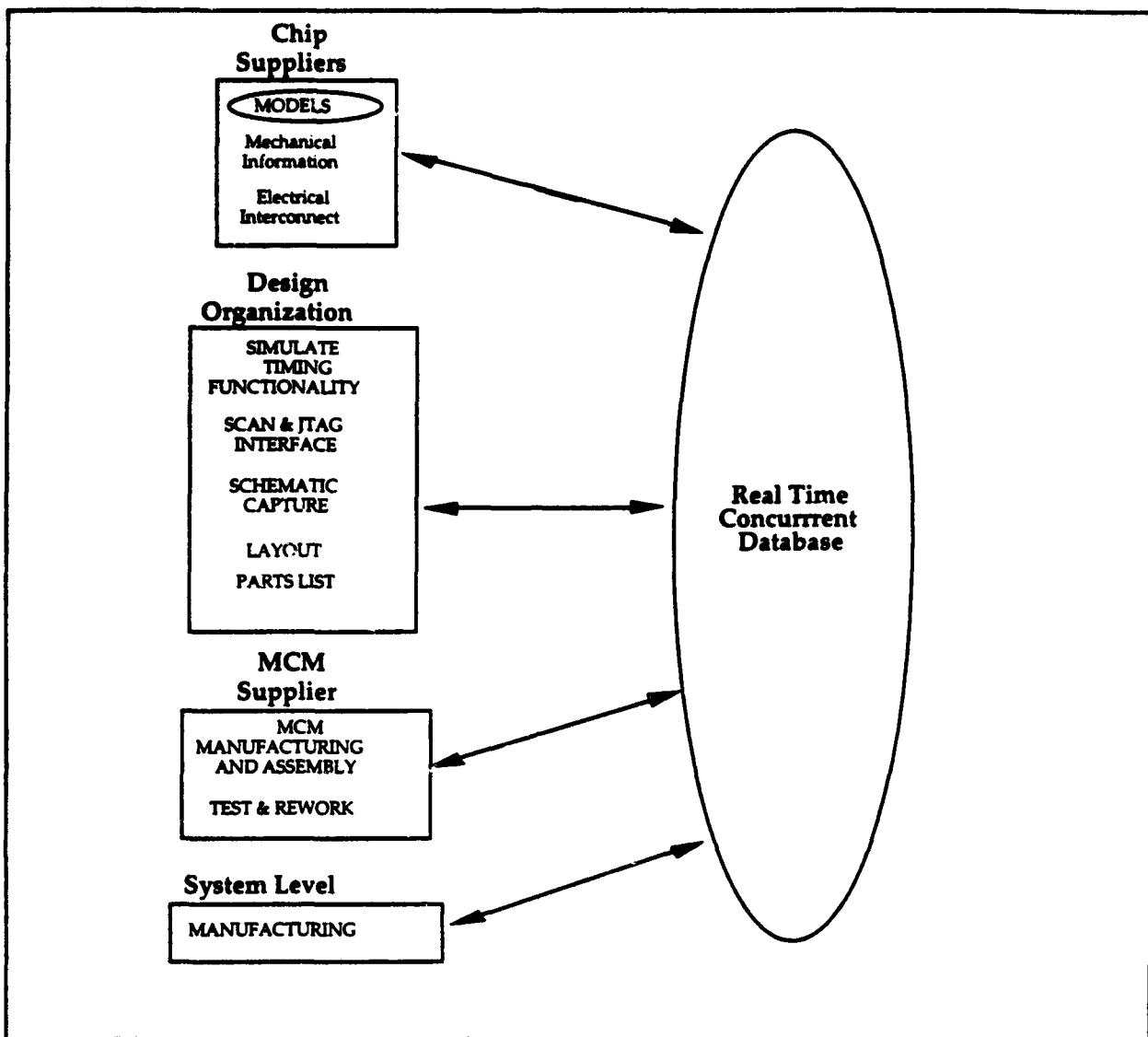


Figure 4.22. Harris GASD Software Tool Sets (Should be)

## Conclusions

The availability of an MCM concurrent engineering environment has the potential to provide a number of direct benefits to the MCM design process. Some of these benefits would be seen immediately. Other benefits would be fully realized only after improvements to the tool set environment.

This MCM concurrent engineering environment would provide an environment where all of the engineering disciplines could share design related information in "real-time" during the design process. The MCM concurrent engineering environment would also provide a common repository for the constraints imposed by the various chip and substrate suppliers.

This improved design environment can be expected to reduce design cycle times and decrease the number of required design iterations. These improvements should help to contain the NRE associated with each MCM design. This environment will also help to control the manufacturing costs for both the MCM and the next assembly level, by better coupling producibility issues to the MCM design process.

In addition to these immediate benefits, the MCM concurrent engineering environment also provides a structure which allows the expected features of future software tools to be fully exploited. It is expected that software tools will mature in the area of true multiple technology design and simulation. The MCM concurrent engineering environment will encourage the development of such tools in the future, and will allow the potential of these features to be fully realized. The result will be a more robust design and simulation environment, which can produce higher performance MCMs while containing the design and manufacturing costs.

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## Section 5 — Market Evaluation

### Overview

The purpose of the market evaluation is to assess the needs, problems, opinions and expectations of those who are currently participating in MCM design and fabrication or who will be doing so shortly. The questions used were broad in scope in order to establish both the sentiments toward MCMs and the industry in general as well as more specific topics such as the design environment that might be impacted by ROSE.

### Questionnaire

A set of 19 multi-part questions were drawn up. Each person was asked to answer 101 individual questions. A complete questionnaire is provided in the accompanying Appendices. The questionnaire was designed to determine:

- If the contacts were current or future user of MCMs
- MCM technologies being used or considered
- The phases of MCM design and fabrication with which they were involved
- Their use of concurrent engineering practices and willingness to invest in design systems that support that paradigm
- Important issues regarding MCM design environment
- Their collection of design tools
- Important issues in design and manufacturing of MCMs
- Important issues regarding data transfer and storage
- Opinions regarding various existing data transfer standards

### Gap Analysis

For 30 of the questions, ratings of importance and satisfaction were recorded.

For instance, from Question #10: *"Please rate the following issues relative to the design and manufacturing of MCMs"*, an individual might have responded.....

	Importance	Satisfaction
A. Design automation software	9	6

Both importance and satisfaction ratings are valuable pieces of information. But additionally, using importance and satisfaction scores, a third value would be calculated called the gap. For each line of questioning, the gap represents a measure of the pleasure or dissatisfaction with the current situation. Gaps can be either positive or negative.

Positive gaps larger than 1 indicate a problem exists that is worthy of attention. The larger the gap, the greater the level of dissatisfaction and frustration and the

greater the opportunity to improve satisfaction (and productivity) if the obstacles are removed. Negative gaps greater than 1 indicate that the available services or solutions are more than adequate and that improvement investments in these areas might be de-emphasized.

## Methods

Using the questionnaire as a guide, a professional telemarketing group made the phone calls to each of the potential respondents. After identifying themselves as a representative of a marketing services group collecting data for an ARPA study, they established the willingness of the contact to proceed. If they were willing to proceed, about 20 minutes was spent collecting answers to the prescribed questions and collecting any associated comments.

## Respondents

A list of 60 engineers and managers who were believed to be involved with MCMs either as designers and end users or fabricators was compiled. Using this list, a professional telemarketing group contacted as many individuals as possible by phone and filled out the survey. A total of 28 individuals agreed to complete the questionnaire.

The titles of the individuals who responded and the identity of their organization is listed in Figure w. Four of the respondents wished to remain anonymous.

## Statistics

The data collected during the phone interviews was entered into a computer data base for statistical reporting and analysis. A complete set of sorting and reporting was generated for each of the groupings of "All respondents", "Current Users" and "Future Users".

The basic demographics of the respondents are shown in the following Table 5.1.

	Current	Future	
MCM Manufacturer	6	1	
MCM Designer	15	6	
TOTALS	21	7	28

*Table 5.1 User Demographics*

A complete set of reports and statistics is provided in the accompanying Appendices.

## Critical Analysis

### Summary

Within the questionnaire there were 30 questions that evaluated the respondents' opinions about various aspects of design and fabrication. Each of these items were scored in terms of importance, satisfaction, and gap as explained previously.

Tables 5.2, 5.3 and 5.4 provide a quick but representative summary of the market evaluation. They show the five items of greatest importance, the five items of lowest satisfaction, and the five items with the largest gap.

These three tables indicate that data transfer and storage is indeed of high importance, that satisfaction with current capabilities is very low, and that there is a large gap between what people would like to do and are actually capable of performing.

Subject	Importance	Satisfaction	Gap	Count
1. MCM Test	9.6	6.6	3.0	14
2. Substrate Fabrication	9.4	7.5	1.9	10
3. Design Methods	9.4	8.0	1.3	25
4. Access to chip and component data	9.3	5.2	4.1	23
5. Data transfer standards	9.2	6.0	3.2	24

Table 5.2: Top Five Importance Items

Subject	Satisfaction	Importance	Gap	Count
1. Store MCM data in neutral file format	4.4	7.6	3.3	20
2. Move design data	4.5	7.8	3.3	20
3. Bi-directional translation	4.6	7.1	2.5	20
4. Support of MCM foundries & design kits	4.6	7.5	2.9	17
5. Design kit available for CAE	4.6	7.1	2.5	16

Table 5.3: Lowest Five Satisfaction Items

Subject	Gap	Importance	Satisfaction	Count
1. Access to chip data	4.1	9.3	5.2	23
2. Bi-directional translation of data	3.4	7.8	4.5	23
3. Neutral data storage	3.3	7.6	4.4	23
4. Data transfer standards	3.2	9.2	6.0	24
5. Unit Production costs	3.2	8.4	5.1	20

**Table 5.4: Largest Five Gap Items**

### ***Specific Question Responses***

The following pages highlight responses collected for individual questions and conclusions that can be drawn.

### ***MCM Technologies - Question 6 and 8***

The respondents indicated they were working with all types of MCM technologies.

MCM Type	Currently using	Future Users
A MCM-L: Laminate	13	5
B. MCM-C: Ceramic Thick Film	12	1
C. MCM-C: LTCC	13	2
D. MCM-D: Thin film on silicon or ceramic	11	1
E. MCM-HDI: Chips first	5	4

**Table 5.5: MCM Technologies - Question 6 and 8**

### ***Question 10***

Questions in section 10 were designed to establish the issue importance and solution satisfaction with various aspects of design software, tool integration, testing, data transfer and chip data.

The numeric responses are summarized in Tables 5.6, 5.7 and 5.8.

One thing these charts demonstrate is that there is not a substantial difference between current and future users of MCMs. Therefore, composite results represent the opinions of both groups in a balanced fashion.



Category	Count	Importance	Satisfaction	Gap
A. Design Automation software	25	8.5	6.9	1.6
B. MCM tool Integration	24	8.3	6.5	1.8
C. Standards for data transfer between design and manufacturing	24	9.2	6.0	3.2
D. Access to chip and component data	23	9.3	5.1	4.2
E. Knowledge of design methodologies to implement MCMs	25	9.4	8.0	.6
F. Automated testing & quality methods	22	8.7	6.4	2.3

*Table 5.6: MCM Issues: Composite of Current & Future Users - Question 10*

Category	Count	Importance	Satisfaction	Gap
A. Design Automation software	20	8.5	6.9	1.6
B. MCM tool Integration	20	8.3	6.6	1.7
C. Standards for data transfer between design and manufacturing	21	9.2	6.0	3.2
D. Access to chip and component data	20	9.3	5.2	4.1
E. Knowledge of design methodologies to implement MCMs	21	9.4	8.0	1.3
F. Automated testing & quality methods	19	8.6	6.4	2.2

*Table 5.7: MCM Issues: Current Users*

Category	Count	Importance	Satisfaction
A. Design Automation software	5	9.1	7.0
B. MCM tool Integration	4	8.7	8.0
C. Standards for data transfer between design and manufacturing	3	8.7	5.3
D. Access to chip and component data	3	10.0	5.0
E. Knowledge of design methodologies to implement MCMs	4	9.0	8.0
F. Automated testing & quality methods	3	9.0	5.3

Table 5.8a: MCM Issues: Future Users

### Data Exchange Standards - Question 10C

Satisfaction with existing data exchange capabilities is very low and there is generally no expectation of improvements.

<ul style="list-style-type: none"> <li>• "There are no standards."</li> <li>• Nothing in place yet, lots more to be done.</li> <li>• Uses existing standards for other product domains that don't meet MCM needs.</li> <li>• Vendors prefer using their own internal formats instead of establishing standards.</li> <li>• "Participating in ARPA ASEM at MCC" to work on improvement for this.</li> </ul>	<ul style="list-style-type: none"> <li>• No standard for this really, except for Gerber.</li> <li>• Necessary to achieve low cost and first time success, and standards are not widely available.</li> <li>• CAD vendor output incompatible with manufacturing.</li> <li>• Are no standards in the market and no one is working hard enough on them.</li> <li>• Not well developed yet.</li> <li>• Never as transparent as people claim.</li> </ul>
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Table 5.8b: Comments

### Design Environment - Question 11

Question 11 was targeted directly at data transfer and storage. Average importance was moderately high but satisfaction was rather low resulting in large gaps. Surprisingly, the respondents feel that it was **not** important or desirable to buy all software from one vendor. *There was a strong preference that heterogeneous software work together and that data be stored in non-proprietary format.*

Comments to questions 11A and 11D were especially indicative of emotions where the gaps were 3.4 and 3.3 respectively.

Phase	Responses	Importance	Satisfaction	Gap
A. Bi-directional translation	23	8.0	4.6	3.4
B. Concurrent design	21	7.0	5.3	1.7
C. Data transfer	23	7.1	4.7	2.5
D. Neutral storage	23	7.7	4.4	3.3
E. Best application	24	7.7	6.9	0.8
F. Single Vendor	22	5.2	6.4	-1.2

Table 5.9a: Data Capability Assessment - Question 11

<ul style="list-style-type: none"> <li>• Data transfers difficult, i.e. , Cadence-to-Mentor.</li> <li>• No existing standard satisfies this need.</li> <li>• Nearly impossible to do this.</li> <li>• Vendors are too proprietary.</li> <li>• No standard for this capability that he is aware of.</li> <li>• CAD and CAE standards not firm yet. Software is unproven. Industry is heading right way, most not smooth yet. Point solution integration's is "not there yet."</li> </ul>	<ul style="list-style-type: none"> <li>• Lack of standards. CAD/CAE vendors slow to adopt existing standards.</li> <li>• Foundries need to accept data from many CAD systems.</li> <li>• Not one on market. Still needs to be developed.</li> <li>• Still not fully developed yet.</li> <li>• Will implement further down the road.</li> <li>• Not as transparent as people claim.</li> </ul>
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Table 5.9b: Bi-directional Data Translation - Question 11A - Comments

- Formats not well-standardized.
- Advent of STEP standard will require the delivery of STEP for MCM products.
- Neutral file is not defined to cover different MCM design levels. Will be a challenge to get vendor support once they are defined.
- Doesn't exist, really.
- No real standard for this.
- Technology is still evolving.
- Neutral format, CAD system independent.
- Still needs developing.
- Not aware it can be done.
- Will implement later.
- Can't be done.

*Table 5.9c: MCM Data in Neutral Format - Question 11D - Comments*

### **Question 12**

Within section 12 several questions were asked regarding the MCM design environment. The numeric responses are summarized in Table 5.10a.

Phase	Responses	Importance	Satisfaction	Gap
A. System Specifications	19	8.2	6.6	1.6
B. System Partitioning	21	8.0	5.8	2.2
C. Autorouting	23	8.5	7.2	1.3
D. Packaging Technology selection	21	8.4	6.2	2.1
E. Design kits	21	7.8	4.9	2.9
F. Optimization of manufacturing data	19	8.1	5.9	2.2

*Table 5.10a MCM Design Environment - Question 12*

- |  |  |
|--|--|
| <ul style="list-style-type: none"> <li>• Few vendors offer</li> <li>• It's just becoming available. "Just not there."</li> <li>• "Not much there." Foundries just beginning to build kits.</li> <li>• Not nearly enough interconnection, and not enough design kits.</li> <li>• "Hasn't gone all too smooth."</li> </ul> | <ul style="list-style-type: none"> <li>• Not many design kits available for technology.</li> <li>• Emerging Technology.</li> <li>• Don't have any real design kits yet.</li> <li>• Very few kits available. Those that are available are geared to specific designs.</li> <li>• Don't do it; when they do, won't guarantee. Cost.</li> </ul> |
|--|--|

*Table 5.10b List comments specific to questions 12E - Comments*

### **Concurrent Engineering - Questions 13 and 16**

In response to question 13, 24 interviewees said that they are using Concurrent Engineering. From question 16 we assess the importance of "investing in Design automation systems to meet concurrent engineering requirements" was quite high.

Extremely Important	11
Very Important	6
Important	6
Not Important	1
Total	24

Using a rating scale of:

Extremely Important	10
Very Important	8
Important	5
Not Important	1
Total	24

Gives a composite importance of 8.0

This supports commentary collected in response to related lines of questioning that design automation systems are very important to success in MCM design and that investments in this area are seen as very beneficial.

The general message obtained from Question 18 on data exchange standards is that they are not a very important element of the MCM design process and that standards useful for MCM generally don't exist.

While several people condemned older standards like Gerber and GDSII, and some people are not familiar with STEP/PDES, *there was a rather favorable view of the STEP/PDES potential.*

Phase	Count	Importance	Satisfaction	Gap
A. CFI	20	6.8	4.8	2.0
B. STEP/PDES	14	6.4	4.5	1.9
C. IGES	16	7.3	6.5	0.8
D. EDIF	22	7.7	5.7	2.0
E. IPC-350	13	5.5	4.5	0.9
F. Gerber	23	8.0	7.1	0.9
G. GDSII stream	22	8.0	7.5	0.6
H. DXF	21	7.3	6.9	0.5

Table 5.11a: Data Exchange Standards - Question 18

- |  |   |
|--|---|
| <ul style="list-style-type: none"> <li>• Looks promising.</li> <li>• Not familiar with.</li> <li>• "On right track."</li> <li>• Has right info. content, but not useful until vendors support it.</li> <li>• Don't use.</li> </ul> | <ul style="list-style-type: none"> <li>• Not familiar with.</li> <li>• Not familiar with.</li> <li>• Not familiar with.</li> <li>• Don't use these standards. Does not support MCM now.</li> <li>• No standards yet.</li> </ul> |
|--|---|

Table 5.11b: STEP/PDES - Comments

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## Section 6 — Market Analysis

### MCM Market Overview

The market for MCM technology has now touched upon all segments of the electronics industry.

The Defense/Aerospace and Government electronics market is using MCM technology for its high-performance at a reduced size, weight and power consumption. Government-funded programs for defense and aerospace related projects have stimulated the development of new materials and new MCM substrate manufacturing.

Computer systems are turning to MCMs for new microprocessor architectures, memory subsystems, and wireless communications capabilities.

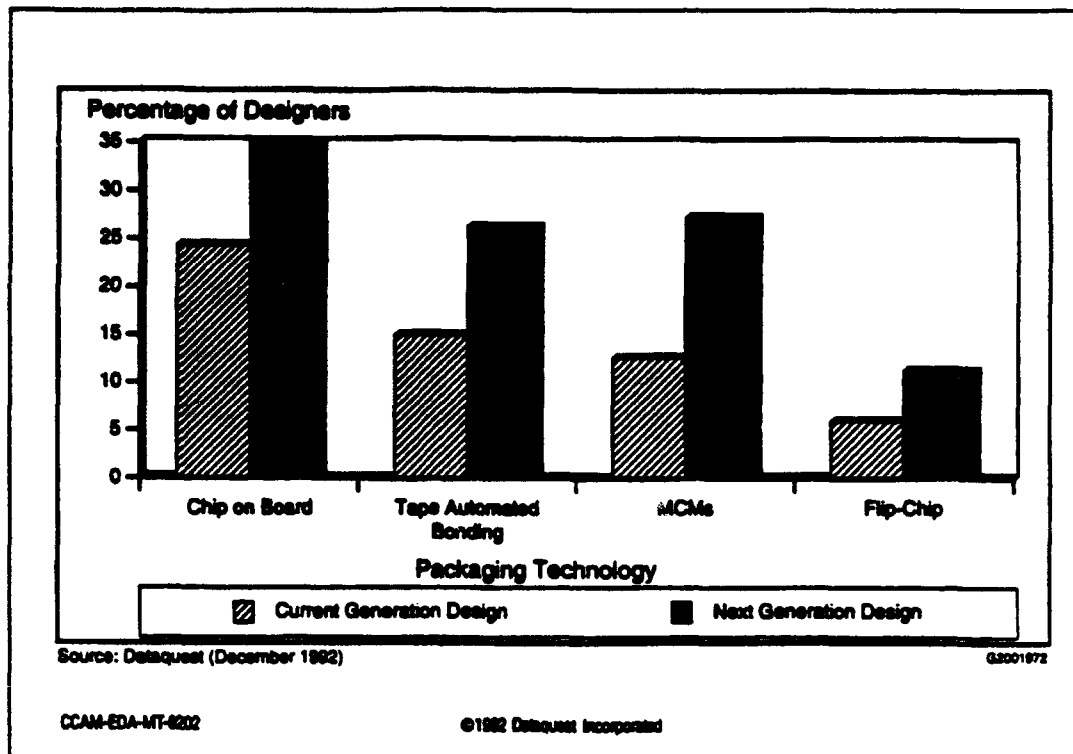
Consumer products apply low-cost MCM technologies for hand-held and portable products.

Telecommunications systems are pushing for greater levels of performance and the integration of communications and computers.

Automotive applications are growing as the industry adds electronics to provide new safety features, engine management, and driver conveniences.

Each industry segment has a broad range of applications for MCMs that cover various price and performance points.

MCM technology adds another level of complexity to the systems design process. MCM packaging influences the final cost, performance, and competitive positioning of a product; therefore, systems design engineers must consider the wide range of choices early in the design cycle.



*Figure 6.1 Anticipated Usage of Advanced Packaging Techniques*

MCM technology acceptance demands new design automation tools. Many forces are driving the systems design engineer to include MCM packaging in the next generation product such as:

- System interconnect of ICs with large I/O (pin) counts of 400 or more pins.
- Clock speeds above 50 MHz (i.e., Digital Equipment Corporation's Alpha processor operates at 175 MHz).
- Mixed signal applications allowing for optimal combination of analog and digital ICs.
- Reduction in system size, power, and weight while increasing functionality and the number of active devices.



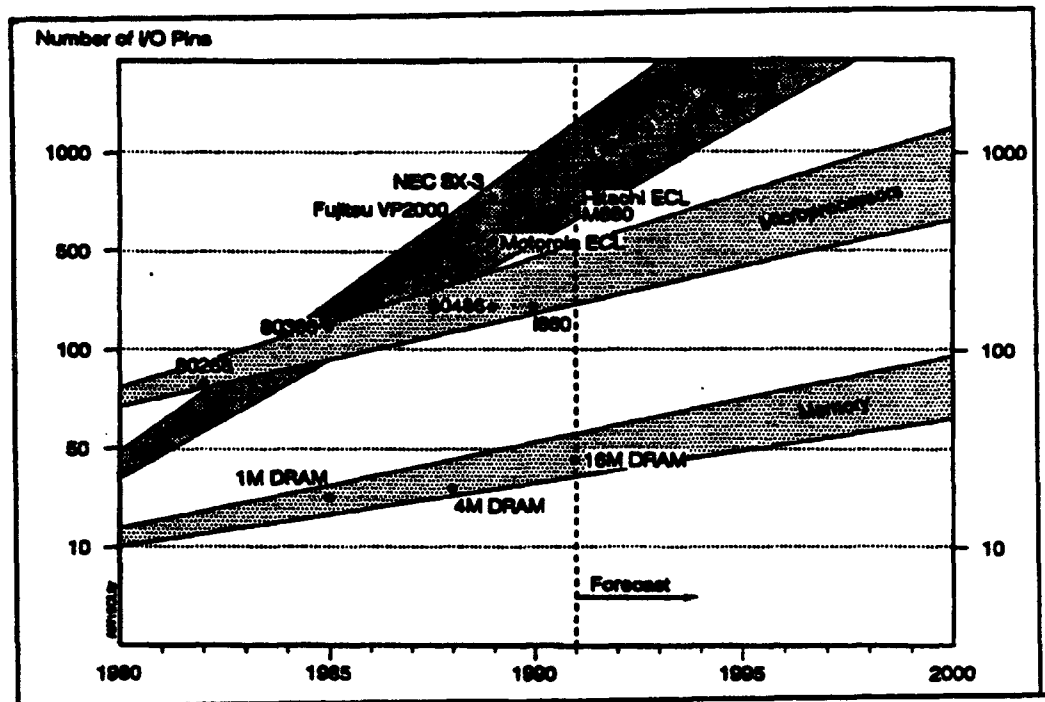


Figure 6.2 Pin Count Per Integrated Circuit

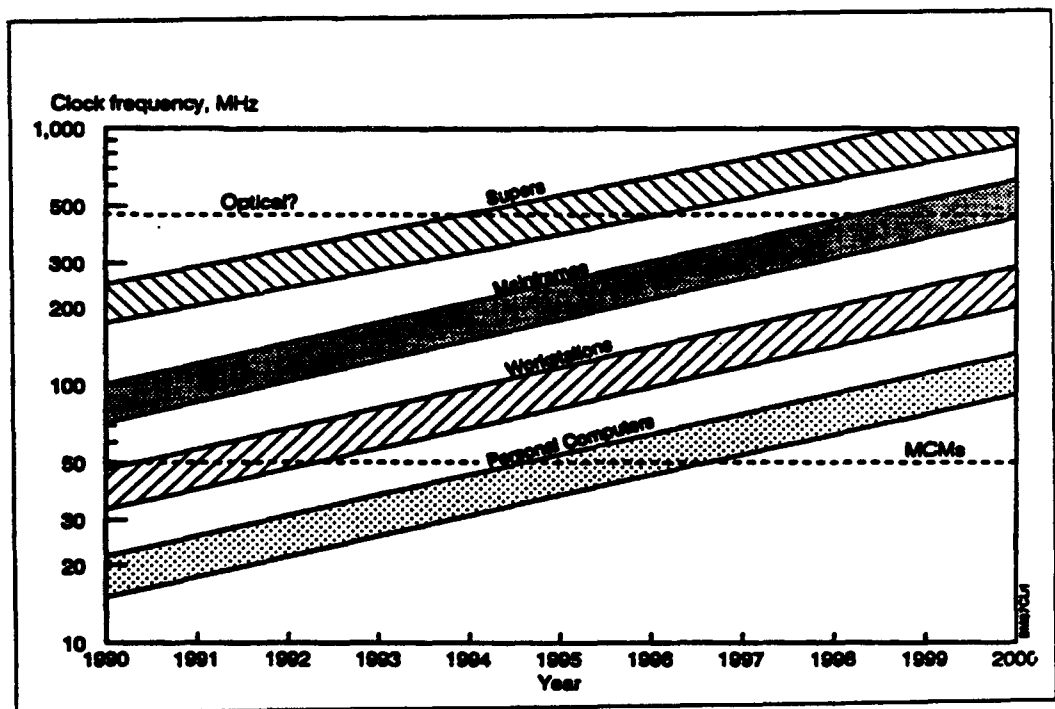


Figure 6.3 Clock Speeds (Leading Edge)

The MCM market is being held back due to economic issues associated with MCM design.

- MCM technology adds risk to schedules and costs as engineers learn how to best apply the new technologies.
- New design automation tools require additional investment and those new tools must operate within the existing design environment.
- New data types and greater amounts of design, manufacturing, and analysis data must be shared among design groups and their associated EDA applications.
- The cost of many MCM processes is too high for price sensitive applications such as consumer electronics.

Industry projections from market surveys such as *Dataquest* and *BPA System 2000* forecast that significant growth in MCM technology usage will occur in 1994 (see references).

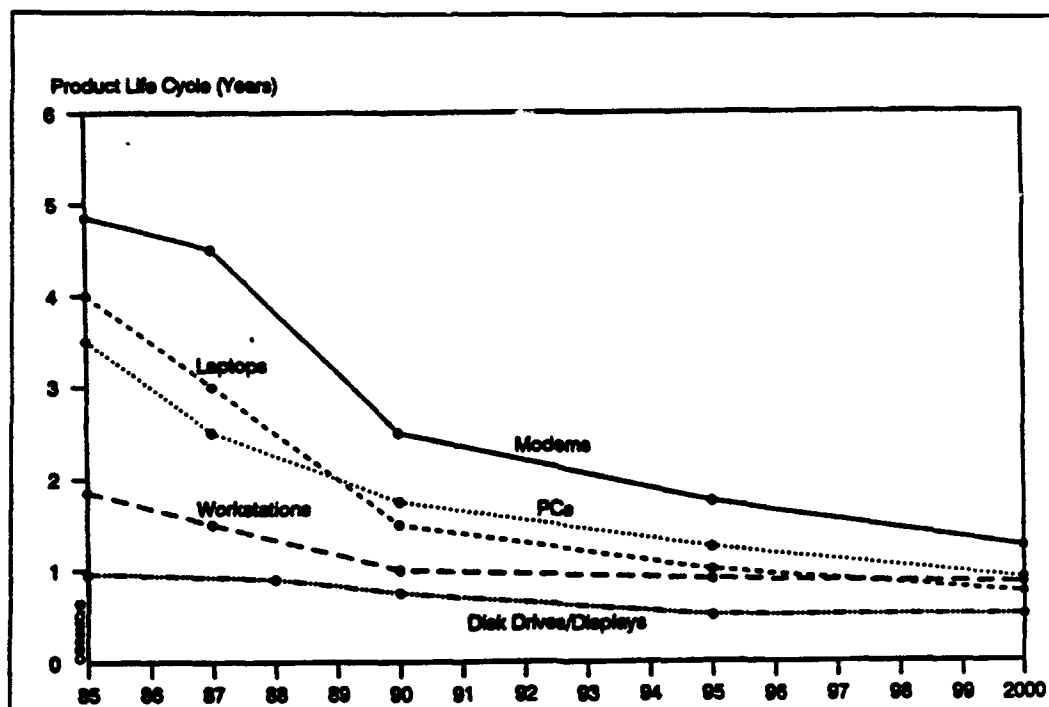


Figure 6.4 Decreasing Product Life Cycles

EDA environments must progress to support these new packaging choices. At the same time, product life cycles are shrinking. This drives the need for concurrent engineering teams made up of multiple disciplines from engineering and manufacturing.

## EDA Market

Dataquest reports that 1992 and 1993 were years of transition for the EDA market as a whole. Competitive pressures in the end-user environment forced a higher level of integration and system complexity with fewer people.

Approximately 140 companies participate in the EDA market according to Dataquest. The total revenue from software licenses for 1992 was \$1.3 billion (hardware added another \$1.4 billion).

The end-user must select specific applications from this large number of niche and broad line suppliers to create an efficient and effective design environment.

The EDA industry and its products are very dynamic. New design automation tools, user environments, and companies are created or disappear each year. Existing design automation tools are continuously, incrementally improved while entirely new tools emerge from university research, government-sponsored programs and industry product development.

This dynamic environment has caused the end-user great expense in the support of existing design databases and in merging the best functions of existing design automation tools with new products as they become available. Products that are no longer supported by a commercial EDA company must also continue to operate in the overall design environment if they continue to serve a useful purpose.

An MCM concurrent engineering environment, built around an international standard such as STEP could provide valuable, cost saving glue among past, present, and future EDA tools. Data can be preserved and made accessible to the end-user to reduce the time, effort, and money spent on maintaining that data.

The availability of expert EDA design data management and programming services would provide the end-user the option of purchasing additional assistance when necessary. And with an open system of the concurrent engineering environment, other third-party suppliers of programming services could compete for and then supply services to the end-user.

Future revenue growth opportunities for EDA suppliers will come from new software applications that improve productivity and reduce the cost of designing electronic systems. Products suggested by this market survey are in demand by end-users and include the development of advanced physical design tools (including MCMs) that include analysis capabilities, architectural-level tools that improve designer productivity, and an increased level of services.

Services will include integration and consulting services that are targeted at optimizing the overall design environment, and support of concurrent engineering design methodologies.

## Market Potential

The market for EDA software, including concurrent engineering environments, software tools, and services is illustrated in Figure 6.5.

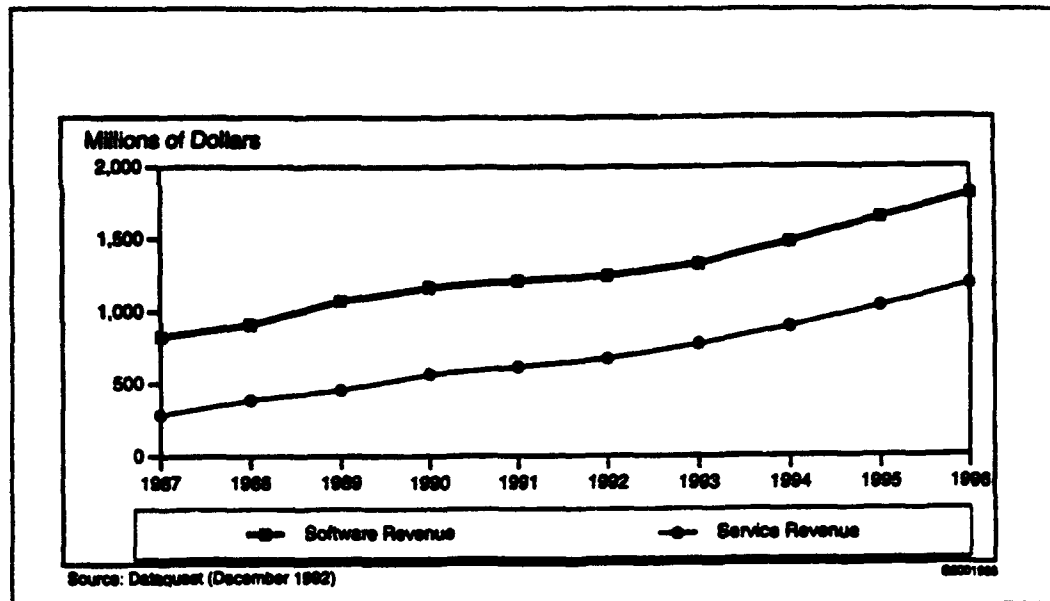


Figure 6.5 Worldwide EDA Software and Service Market History and Forecast

The following areas are forecast to experience significant growth:

- Advanced physical design tools (including MCMs) that include analysis capabilities
- Architectural-level tools that improve designer productivity
- Services, including integration and consulting, are targeted at optimizing the overall design environment, support of concurrent engineering design methodologies.
- Concurrent engineering environments and frameworks.

Although the leading market studies do not highlight the specific forecast in these areas, the following estimates are derived by comparing multiple sources of data and interpolating these numbers.

Year	1993	1994	1995	1996
Concurrent Engineering environments	\$13M	\$28M	\$43M	\$58M
% of EDA market revenue	1%	2%	3%	4%
MCM design software applications	\$17M	\$34M	\$52M	\$80M
% of PCB/MCM/Hybrid revenue	5%	10%	15%	20%
Services in support of concurrent engineering environments	\$21M	\$40M	\$80M	\$120M
% of EDA services revenue	3%	5%	8%	11%

Table 6.1 Market Forecast for MCM design automation

Calculations used in Table 6.1 are based on data from *Dataquest, BPS System 2000* and Harris EDA internal proprietary market research data.

An initial, rough order of magnitude estimate of the market potential for CHOICE is offered in Table 6.2 and Figure 6.6.

Year	1993	1994	1995	1996	1997	1998	1999	2000
Software License fees	0.00	2.10	2.73	3.55	4.61	6.00	7.80	10.14
Software maintenance	0.00	0.21	0.27	0.35	0.46	0.60	0.78	1.01
Services	0.00	2.50	3.25	4.23	5.49	7.14	9.28	12.07
<b>Total</b>	<b>0.00</b>	<b>4.81</b>	<b>6.25</b>	<b>8.13</b>	<b>10.57</b>	<b>13.74</b>	<b>17.86</b>	<b>23.22</b>

Table 6.2 CHOICE Market Forecast

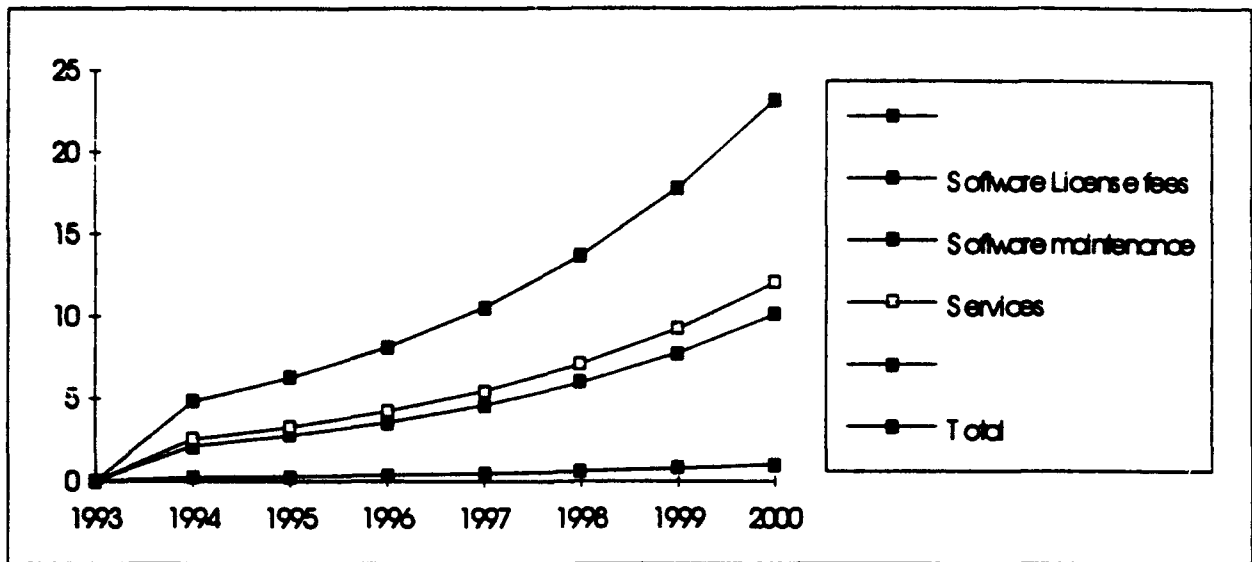


Figure 6.6 Forecast for MCM Concurrent Engineering Company

The following assumptions were made when estimating market forecasts illustrated in Figure 6.6:

1. Additional development and productization as proposed in this Market Study begins by January 1, 1994.
2. Commercial company has technical staff capable of delivering, training and custom software development services.
3. Support of ARPA and leading electronic systems and MCM user companies.
4. MCM market doubles in 1994 and follows aggressive revenue growth rates as projected by studies referenced in this Market Study.
5. Potential of market for concurrent engineering environments and associated services, as calculated in this Market Study are correct. It is recognized by the Program Team that has assembled this market study that additional market data and further analysis of that data is required.

These market estimates suggest that a significant opportunity exists for a commercial EDA vendor who offers a concurrent engineering environment for MCM design tools.

## **Market Segments**

Each electronics segment may require specific functions and will have their unique priority on the importance of each feature. A summary of the most important features required for each segment, based on our telemarketing survey and interviews:

- MCM manufacturers and substrate foundries.
- End-users of multivendor design automation software environments.
- End-users of single vendor design automation environments.
- End-users of analog and mixed signal MCMs
- Concurrent operation among departments (electrical design, mechanical design, product assurance material planning, purchasing, etc.).
- Government agencies.

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## Section 7 — Commercialization

### Market Positioning

A concurrent engineering environment based upon a commercially available object oriented database will have specific benefits to the markets being served. Success of the product depends upon accurate positioning to clearly highlight the unique benefits of this environment over other similar technologies.

It is an advantage for the company that markets and supports this technology if it also markets complementary EDA software. However, environments offered by broad line suppliers force end-user customers to consider the software tools offered by the broad line supplier. The commercial company supporting the concurrent engineering environment must be application-neutral for the majority of the EDA applications available from which the end-user has to choose.

CHOICE must be positioned against commercially available EDA frameworks. The following benefits could differentiate CHOICE:

- The use of STEP international standards and EXPRESS as the basis of the CHOICE environment.
- Data is translated automatically, eliminating time consuming and error prone manual conversion of data.
- The end-user and MCM manufacturers are free to select the optimal application software from their EDA software supplier.
- All EDA software suppliers must compete based on functionality, services, and support and cannot lock-in an end-user to inferior tools.
- The end-user may use the best features from a particular tool. For example, an autorouter capable of handling a specific design may be used even if an MCM CAD tool from another vendor is used for placement, editing, design rule checking, and CAM outputs.
- Existing environments that do not have an integrated set of software tools can be brought together and made to operate within a concurrent engineering environment. The end-users are able to preserve their investment in software tools, each of which may be very capable of handling specific design functions, and yet gain the advantages of supporting a concurrent engineering design methodology.
- Most, if not all commercially available products employ multiple proprietary databases and provide little or no direct access to them. The CHOICE concurrent engineering environment could provide a window into these "single vendor" environments to allow the addition of new tools or the integration



and sharing of data with other agencies or companies that may use other tools.

## Cost of Marketing and Promotion

The level of promotion of CHOICE that is required to realize the sales projection in this market study is significant. It includes advertising, trade show support, technical articles, technology seminars, sales literature, and the collection of end-user case studies.

The actual amount invested in promotion varies, depending upon the overall business plan; however, an initial allotment of \$735,000 per year is proposed for marketing and promotion (refer to Table 7-1).

Advertising, development of an ad campaign and ten placements in electronic industry trade magazines.	\$60,000
Trade show support: Design Automation Conference, four additional trade shows for five total includes fees, travel expenses and promotion.	\$100,000
Sales literature including product descriptions, customer case studies, services descriptions (design and printing).	\$30,000
Technology seminars and road shows with product demonstrations. Preparation costs and the cost of two road shows per year with visits to eight major cities during each show (preparation, travel and expenses).	\$70,000
Technical articles and case studies, the development of partnership programs, sales aids including presentation materials.	\$25,000
Product demonstrations, preparations and equipment	\$150,000
Promotion staff salary, benefits, and travel	<u>\$300,000</u>
Total	\$735,000

Table 7-1 Promotion

## Pricing

Product pricing is determined by the pricing for similar products and services available in the commercial market and the value to the end-user. Value is measured by intangible benefits such as improved engineering productivity, reduced design cycles, more accurate designs, and higher quality products.

The product could be delivered in a modular form that provides maximum customization and pricing flexibility. Operation across networks will be assumed and no node locked pricing will be considered.

Pricing is proposed in Table 7-2. The recommended list prices are comparable to fees charged by leading EDA suppliers for design frameworks, procedural languages, data toolkits and services:

<b>Product offered:</b>	<b>Fees charged:</b>
The basic concurrent engineering environment without applications interfaces	\$5,000
Each applications interface allowing for bi-directional movement of data.	\$5000 per unique interface
Database technology used within the concurrent engineering environment	STEP TOOLS pricing
Procedural Interface (PI) pricing including PI and debugging tools	\$10,000

*Table 7-2 Product Pricing*

## **Distribution**

CHOICE requires a sophisticated sales process that requires educating the customer and strong pre- and post-sales technical support. Therefore it is recommended that sales will be directed through a focused, direct sales force of highly technical sales professionals and applications support teams. OEM resale agreements may be considered with companies involved with selling EDA applications; however, one must avoid sales channel conflicts.

## **Services**

CHOICE requires a high level of technical support. The company that markets CHOICE is also responsible for multi-level customer training, installation, software support, integration services, and whatever the customer requires in the form of support services.

The commercial company must be expert in EDA software technologies, database technology, engineering productivity issues, and MCM technology.

Proposed pricing for services are provided in Table 7-3:

<b>Service offered:</b>	<b>Fees charged:</b>
Software support including software upgrades and telephone hotline (800) service	15% of the software license list price, charged annually
Training for beginner, intermediate, advanced levels.	\$1000 per student per course
Integration services where customer specifies the development of additional applications interfaces, new features, customization of the environment	Quoted per job at an average rate of \$125 per hour

*Table 7-3 Services Pricing*

## **Product Packaging**

The product will be modular to allow for maximum flexibility and customization.

Included with a license fee is product user guide, systems administration manual, on-line HELP system, and a 90-day warranty.

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## Section 8 — Conclusions

All new and successful software technologies address a specific set of end-user problems. This Market Study has identified end-user problems and concerns, and it is the opinion of the Program Team that CHOICE could be positioned to resolve or lessen these problems. The information collected in this Market Study highlights issues as true:

- MCM technology is being adopted by most leading systems electronics companies.
- The revenue spent on MCM technology – including MCM assemblies, MCM design automation, and manufacturing equipment is – forecast to double in 1994 – and may reach \$10 billion by the year 2000.
- End-users highlight issues involving the access and movement of design- and component-data as those areas needing the greatest amount of improvement in commercial technology
- MCM technology has added a level of complexity that requires a concurrent engineering design methodology that depends upon efficient interaction of multi-disciplined design and manufacturing teams.

These statements taken together identify a growing market that has an associated problem that can be partially resolved with the availability of a commercial product based on the CHOICE concurrent engineering environment.

CHOICE has the potential to satisfy many of the technical and product features problems that underlie these statements. The market forecasts suggest that a large potential reward could be realized by any company that is prepared to invest the time and resources necessary to produce a commercial-quality product that satisfies some of the end-users' needs.

Government assistance through the DICE program has produced valuable core software technology.

- CHOICE demonstrates the feasibility of integrating multiple EDA software applications to allow multi-disciplined teams to work in a cooperative, time-efficient manner.
- CHOICE uses the internationally accepted STEP/PDES standard and the EXPRESS modeling language. This provides for comprehensive design data modeling which meets or exceeds the current proprietary capabilities offered by broad-line EDA suppliers of design framework technology.

- CHOICE is an open systems that can share data among proprietary MCM design tools.
- CHOICE promises end-users the freedom to choose the best and most recent technology for individual EDA software tools by eliminating problems with data integration. CHOICE does not limit the scope of the data model and allows for a complete data transfer limited only by the capabilities of the individual software application.
- CHOICE is highly expandable and may encompass the electronic design, manufacturing, and mechanical engineering models that are necessary to support a concurrent engineering approach for the complete MCM design- and manufacturing-process.

Other programs funded under DICE have also provided similar benefits. For example, the Manufacturing Optimization system developed by Raytheon, demonstrates the ability to bring manufacturing teams into the design process at an early stage and before investment is made in prototype- or production-tooling.

For the United States, marketplace advantages such as low-cost product manufacturing, higher quality products, more feature rich products, and being first to enter new markets can be realized partly through efficient and effective concurrent engineering methodologies and its supporting software technology.

## **Commercialization**

Commercialization of CHOICE will require additional engineering effort as well as an investment in a product launch. It is proposed that further development of the technology be completed prior to committing to a commercial product launch. The additional product development effort would focus on the issues raised by end-users and would validate the technology in production beta test sites.

Once proven in beta test sites, a commercial EDA company would then be much better positioned to justify the allocation of internal funds or could raise capital for a product launch.

For commercialization, we propose that additional development efforts, as outlined in the following sections, be completed.

### **Freedom of data among physical design automation tools**

CHOICE must be demonstrated to be capable of handling a broad range of MCM technologies.

The demonstration of the CHOICE environment used a low-temperature cofired ceramic MCM as a demonstration vehicle. Laminate, silicon, chips-first technology, and surface mount technology examples must also be proven to operate.

CHOICE must support the products offered by the leading MCM design tool vendors, including Harris EDA, Cadence, Mentor and Intergraph. Further development could produce commercial quality interfaces with products from each of these companies. The MCM application model may be expanded to encompass physical design data supported by all of these companies.

The development of an application model for MCM physical design data should be submitted to the international standards committee on STEP to have the MCM AP endorsed and published.

CHOICE must also be enhanced to include the functionality of ROSE DELTA files. ROSE DELTA files are used for data management, version control, and data locking features.

#### **MCM Design Kit Process Models**

The CHOICE environment provides functionality to create Process Models for each MCM technology and each MCM supplier. This has been demonstrated for printed circuit manufacturing in the Raytheon Manufacturability Optimization program.

MCM design is dependent upon designers understanding the specific manufacturing and assembly rules of the selected MCM technology and supplier. All EDA vendors supplying physical CAD tools are building proprietary Design Kits to support MCM design.

Process Models should be created that validate the design data against MCM process characteristics. These Process Models would provide a central location for Design Kits that would make the data available -- described in the international standard modeling language EXPRESS -- to all MCM CAD tools and MCM manufacturers.

#### **Support of standard format interfaces**

The CHOICE environment supports any standard that can be represented in EXPRESS. This capability could be demonstrated for EDIF and IGES based on the current EXPRESS representation of these standards. The CHOICE EXPRESS model must be expanded to include the portion of the EDIF and IGES models necessary to support MCM design.

In addition to EDIF and IGES, EXPRESS models should be developed for the following formats:

- The Logic Modeling DIE Format being developed under ARPA/ESTO ASEM Contract MDA972-93-C.
- EDA software - MCM manufacturing interface formats to be proposed by the ASEM CAx Interface Specification Alliance formed under ARPA-sponsored USAF WL Contract: F33615-92-C-1134.

#### **Addition of data validation software algorithms**

The CHOICE environment assumes that data integrity is maintained through multiple cycles among software applications. However, end-users are greatly concerned with corrupted design data, inconsistent data, and error detection and correction. Validation is required for the users' peace of mind and to avoid costly prototype tooling regardless of the level of quality of the CHOICE concurrent engineering environment.

Harris EDA has developed Design Integrity Management software that validates electronic design data that originates from multiple sources. The Design Integrity Management software could be integrated within CHOICE to:

- Validate the data originating from multiple applications programs including EDA, material planning, and manufacturing.
- Alert the project team of potential inconsistencies in the data.
- Correct erroneous data and update the individual databases of the software applications that are included in the CHOICE environment.
- Generate a history of changes that were made in the design cycle.

#### **Addition of a Graphical Procedural Interface (GPI) environment**

A commercial product must allow end-users the option of programming and integrating software applications without depending upon the commercial vendor. An easy-to-learn and easy-to-use Graphical Procedural Interface must be made available to those technical users who are not software programmers (i.e., designers, electrical engineers, etc.).

### **Increase Scope of CHOICE**

CHOICE could also be expanded to further demonstrate the feasibility of developing a concurrent engineering environment for the MCM design environment. Specific areas of concern identified by end-users include MCM test, MCM manufacturing process modeling, and system simulation. These areas would expand the appeal of CHOICE as a commercial product. However, they should not be considered of secondary impor-

### **Integration of test software and automatic test equipment**

The integration of test into the design process and an approach that emphasizes Design-for-Test (DFT) was highlighted by many end-users. The Harris GASD Case Study in particular, points to the importance of including test issues within the concurrent engineering environment.

The CHOICE concurrent engineering environment could be enhanced to demonstrate a concurrent design and test environment that includes:

- A Test Process Model that evaluates the testability of an MCM design, including support of structural, functional, and behavioral test.
- Test pattern and test vector generation.
- The development of SCAN, BIT and BIST circuit cells and standard test component descriptions that could be maintained in the CHOICE database and be made available to the applications that are integrated in CHOICE.

### **Addition of parts and material management software**

The largest gap in end-user satisfaction identified by the survey listed the relative importance of access to chip data with what is currently available. The Harris GASD Case Study highlighted that managing materials and parts is an integral part of the concurrent engineering design environment.

The Approved Parts Interactive Management System (APIMS) provides a general database with extensive information regarding approved suppliers and standard parts for use in deliverable hardware. APIMS is linked into the purchasing organization and is used to manage component procurements.

The Parts Control and Tracking System (PCATS) manages the parts list at the MCM, PCB, and overall system levels for each assembly within a product or project.

These two programs, developed by Harris GASD, provide valuable functions that could not be acquired in the commercial market.

The CHOICE concurrent engineering environment could be enhanced to incorporate APIMS and PCATS. In addition, to expand the scope of the CHOICE implementation, we propose that the Logic Modeling Corporation DIE format specification be modeled in EXPRESS to offer a complete part description, procurement and management system with the physical design tools.



This solution provides design and material procurement capability that, to the best of our knowledge, does not exist in the commercial marketplace. Therefore, this set of enhancements has the potential to be a successful commercial product.

#### **Integration of an MCM design optimization system**

Design Optimization software needs to be developed to assist systems engineer in partitioning an electronic system into chips, MCMs, and printed circuit boards. The Design Optimization technology being developed by Harris EDA could be integrated into CHOICE to allow for system floorplanning concurrent with MCM CAD layout.

System floorplanning will select components in the appropriate surface mount or bare die format, depending upon the MCM or PCB technology. The Design Optimization technology also includes Design Advisors that calculate routability, electrical delay calculation, and thermal data.

#### **Application of a concurrent engineering environment for multilevel and mixed signal applications**

MCM design cannot be easily simulated due to the complexity involved with simulating multiple chips interconnected on an MCM. CHOICE could be expanded to provide an application model for MCM simulation that allows concurrent operation of multiple simulators on the concurrent (parallel) operations of a single simulator in order to simulate an MCM.

It was also reported and highlighted by Harris GASD, that there is a lack of synergy between analog and digital EDA software tools that causes difficulties during the design process. Manual calculations performed by analog design engineers are often required.

The CHOICE concurrent engineering environment will support the data required for both analog and digital simulation. Integration of multiple simulators that operate on a single database could relieve the problem and allow for concurrent simulation of mixed signal MCMs.

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