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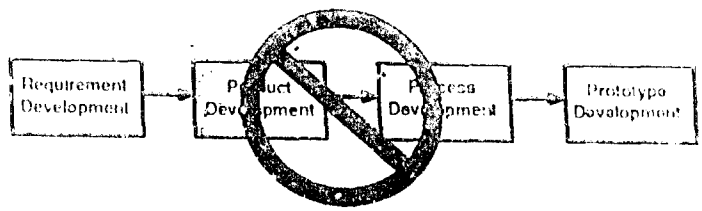

CRTA-WCCA

(1)

Worst Case Circuit Analysis Application Guidelines

RAC

Reliability Analysis Center

A DoD Information Analysis Center

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Worst Case Circuit Analysis Application Guidelines

1993

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Reliability Analysis Center

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13. ABSTRACT (Maximum 200 words)

This document presents an overview of Worst Case Circuit Analysis. Worst Case Circuit Analysis is a method for determining circuit performance under extreme (worst case) conditions. This process is accomplished by analyzing a circuit's variability with respect to part parameter tolerance extremes. Part parameter variation is the result of both internal and external factors. This document also presents general guidelines for implementing and performing a worst case circuit analysis.

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1.0 INTRODUCTION

1.1 Purpose of WCCA

Worst case circuit analysis (WCCA) is a method for determining circuit performance under extreme conditions by accounting for component variability. Sources of component variability include component quality level, drift due to component aging, the stress applied to each circuit component (including humidity, temperature, or radiation), and external electrical inputs.

Analyzing the circuit at its extreme limits gives an indication as to how the circuit will perform under a worst case scenario. WCCA is a valuable tool that aids in design assurance and safety. Furthermore, implementing a WCCA can help identify ways to reduce financial, legal and safety risks to the manufacturer. This technical report provides the reader with structured approaches to performing WCCA.

1.2 Value of WCCA

Performing a WCCA can provide the design team with valuable insight into sources of variability which affect circuit performance. When circuit variability is identified and quantified it can be most likely controlled. Consider the following scenario:

> Company X is planning to manufacture a voltage regulator. This company has manufactured regulators for 10 years. It plans to use a previous design as the basis for the new production model. After bread-boarding the circuit, Company X decides that it will start production. After production units have been fielded, it is realized that only 80% of the regulators meet a rise time specification required for the new design. The problem in this case is a filter capacitor that has a wide tolerance range. Had a WCCA been performed, the problem would have been realized before it surfaced in production or the field. Company X repaired the units in production while field maintenance personnel spent time and money troubleshooting the host system.

Finally, the output of a WCCA allows a comparison of actual applied part stresses against part rated values which can be used to ensure ample derating has been applied to meet design requirements.

2.0 BACKGROUND AND PRELIMINARY WCCA INFORMATION

2.1 Basic Guidelines and Overview of WCCA

WCCA provides a means for predicting system performance under extreme conditions and examines a system at a detailed level to determine the effects of component variability. Variability can be influenced by the quality of components used, combinations of components working together, the environment, circuitry external to the system being analyzed, aging of components over time, and other internal and external influences. Variability resulting from these effects can cause unexpected system behavior.

In the classical approach to circuit analysis, models and equations are implemented to determine whether or not a circuit is designed to properly operate under ideal conditions. In a typical design process, environmental conditions are not usually taken into consideration within a WCCA. The results of the classical analysis are then evaluated against these deficiencies that are being compensated for.

In comparison, WCCA also implements the techniques used in classical analysis; however, the analyst takes all extreme (worst case) conditions and applies them to the given circuit. Furthermore, these conditions are employed simultaneously. The circuit is then analyzed under these stringent conditions. The result is that overall circuit performance is evaluated at its worst possible conditions.

It should be noted that although the worst case scenario is a possibility, it is highly improbable that all circuit parameters will vary to extremes simultaneously. However, WCCA is predicated on a degree of conservatism which ensures that if the circuit passes the WCCA, the circuit will always perform as designed.

There is one question that needs to be addressed before commencing a worst case analysis. When should a WCCA be performed? A worst case analysis should be performed on all circuitry that is safety and/or financially critical. For instance, fly-by-wire circuitry is extremely critical to ensure the safety of a pilot, therefore, it should be subjected to a thorough WCCA. If circuit failure could cause extensive damage to expensive machinery or systems that would cause financial loss then a WCCA should be performed.

3.0 WORST CASE CIRCUIT ANALYSIS GUIDELINES

Prior to starting a WCCA, guidelines have to be established based on time and budget constraints. In many instances, the circuit will be partitioned in a manner such that only critical functions will be analyzed. Other factors influencing the analysis approach are: tools available to complete the analysis, availability of component data, and design technology. The following paragraphs outline the order in which a typical WCCA is completed. These guidelines have to be tailored to an actual analysis as they are generic in nature.

3.1 WCCA Initialization

The first step in performing a WCCA involves data acquisition in the following areas:

Performance Requirements and Specifications
Schematics and Block Diagrams
Interconnection Lists and Wiring Diagrams
Full Parts Lists
Theory of Operation
Mission Environments
Mission Mode (System Configuration)
Thermal Design Analysis

3.1.1 Review of System Requirements and Specifications

The analyst must have a complete comprehension of the system requirements and specifications prior to starting the analysis. Failure to review this information could result in the failure to examine relevant system parameters.

There are certain steps/guidelines that should be followed when interpreting the specifications and requirements. First, are there military and/or other governing documents referenced in the specifications? For instance, MIL-STD-785 (Reliability Program For Systems And Equipment Development And Production), Task 206 (Electronic Parts/Circuits Tolerance Analysis) is often cited as the governing military document (refer to Figure 1). Specifics related to the system are then addressed in the Statement Of Work (SOW). It is essential to eliminate ambiguities that may arise from the specifications. This specifically applies to specifications or requirements that contain "...where appropriate," "...et cetera," "...when necessary," or other similar statements. By eliminating ambiguities from the specifications, unnecessary difficulties and delays can be avoided.

MIL-STD-785B
15 September 1980

Task 206

ELECTRONIC PARTS/CIRCUITS TOLERANCE ANALYSIS

206.1 PURPOSE. The purpose of task 206 is to examine the effects of parts/circuits electrical tolerances and parasitic parameters over the range of specified operated temperatures.

206.2 TASK DESCRIPTION

206.2.1 Parts/circuits tolerance analyses shall be conducted on critical circuitry as defined in the contract. These analyses shall verify that, given reasonable combinations of within-specification characteristics and parts tolerance buildup, the circuitry being analyzed will perform within specification performance. In making these analyses the contractor shall examine the effect of component parasitic parameters, input signal and power tolerances, and impedance tolerances on electrical parameters, both at circuit nodes (component interconnections) and at input and output points. Since all of the stated factors may not be significant to all circuits, only the critical factors for that circuit shall be considered.

206.2.2 Component characteristics, (life-drift and temperature) shall be factored into the analyses. These characteristics or values shall include resistance, capacitance, transistor, gain, relay opening or closing time, et cetera.

206.2.3 The inductance of wire-wound resistors, parasitic capacitance, and any other similar phenomena shall be taken into account, where appropriate. Maximum variations in input signal or power supply voltage, frequency, bandwidth, impedance, phase, et cetera shall be used in the analyses. The impedance characteristics of the load shall be considered as well. Circuit node parameters (including voltage, current, phase, and waveform), circuit element rise time, timing of sequential events, circuit power dissipation, and circuit-load impedance matching under worst case conditions shall also be considered. These parameters shall be analyzed for their effect on the performance of circuit components.

206.2.4 A list of those functions/circuits to be analyzed shall be presented at PDR. The most unfavorable combination of realizable conditions to be considered in the parts/circuits tolerance analyses shall be defined for approval by the procuring activity. Results of the analyses and actions taken as a result of analyses findings shall be made available to the procuring activity upon request.

206.3 DETAILS TO BE SPECIFIED BY THE PA (reference 1.2.2.1)

206.3.1 Details to be specified in the SOW shall include the following, as applicable:

(R) a. Identification of range of equipment operating temperatures.

(R) b. Specification of criteria for selection of parts/circuits to be analyzed.

c. Delivery identification of any data items required.

TASK 206
15 September 1980

FIGURE 1: MIL-STD-785B TASK 206

Once the analyst comprehends the requirements and specifications, the identification of critical circuit functions should be developed. In many analysis efforts, there is not enough time to analyze all functions or circuitry within the system. Therefore, critical circuit functions must be analyzed initially.

After there is a firm understanding of the specifications and requirements, the analyst should review the documents with the customer to obtain concurrence. This allows for modifications and changes that the customer may have made. If the customer concurs with the analyst's perspective of the specifications, then the analyst can move to the next step. It is vital that the customer be aware of the analyst's interpretation of the specifications and requirements. If not, time and budget difficulties may occur due to misunderstandings.

3.2 WCCA Profile

After the groundwork has been established for the WCCA, it is necessary to plan and execute the analysis. Figure 2 is a flowchart showing the general overview of a WCCA. It demonstrates the interrelationship of the various tasks required for completion of a WCCA. The following sections will outline guidelines that can be used in the production and documentation of a WCCA.

3.2.1 Functional Breakdown/Theory of Operation

Developing a functional breakdown and theory of operation serves two purposes. First, it should be assumed that the individual reviewing the document has very little knowledge of the system. If the reader/customer is unfamiliar with the circuit/system, the functional breakdown will describe each of the major functions performed by the system, giving the reader a better understanding as to why certain circuits were chosen for analysis.

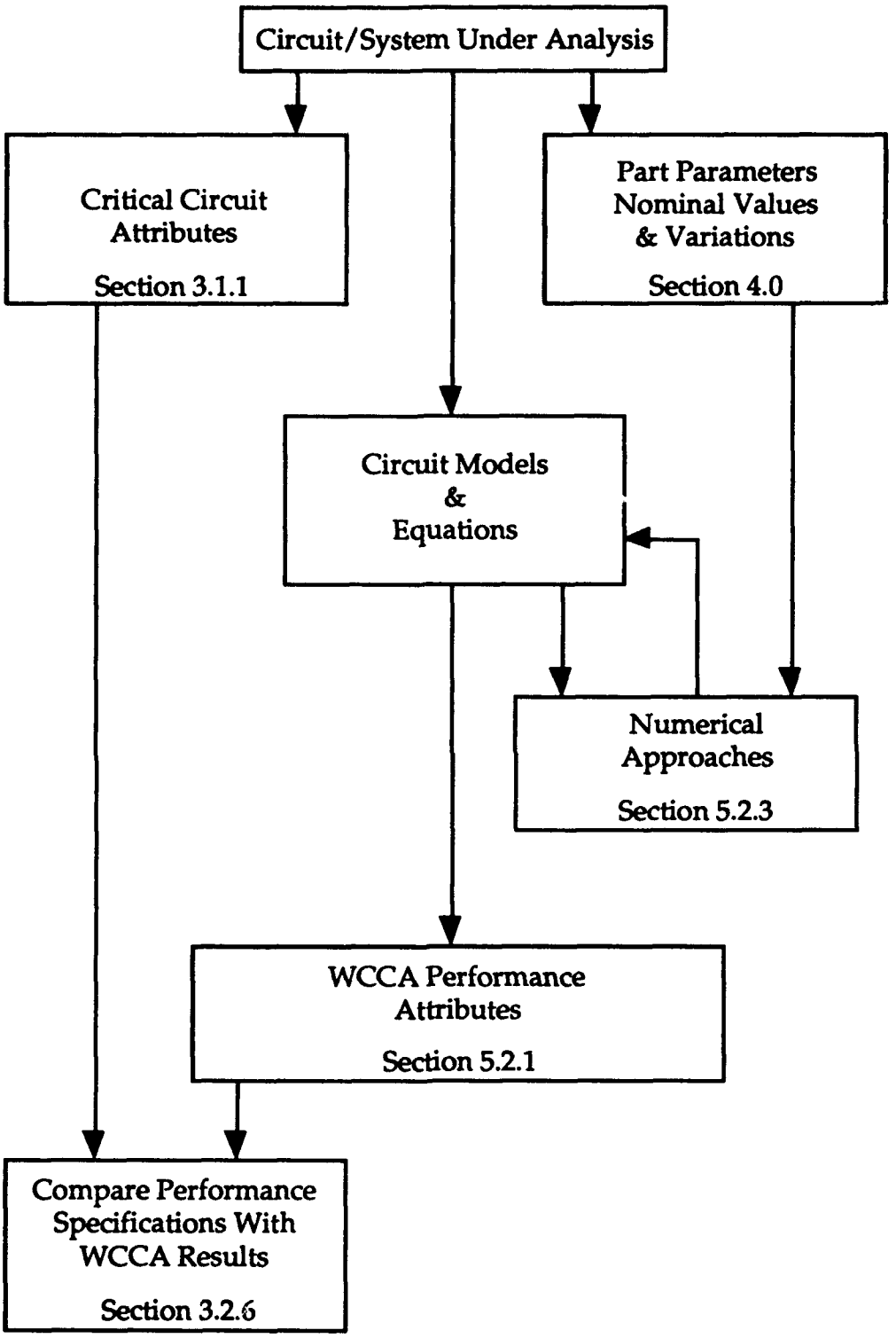


FIGURE 2: GENERAL WCCA FLOWCHART

A functional breakdown should include block diagrams that outline the major subfunctions. This gives the reader a visual representation of the system analyzed in the report. The block diagram should detail all functional interactions; i.e., all inputs and outputs. For instance, a block should include feedforward/feedback signals, power supply signals, and external input or output signals.

Figure 3 shows a simple diagram demonstrating circuit/function partitioning.

INPUT VOLTAGE SPECIFICATION: 20 - 30 V_{DC}
OUTPUT VOLTAGE SPECIFICATION: V_{OUT1} = 5V ± 2% @ I_L = 150mA TO 400mA
V_{OUT2} = 12V ± 5% @ I_L = 100mA TO 150mA

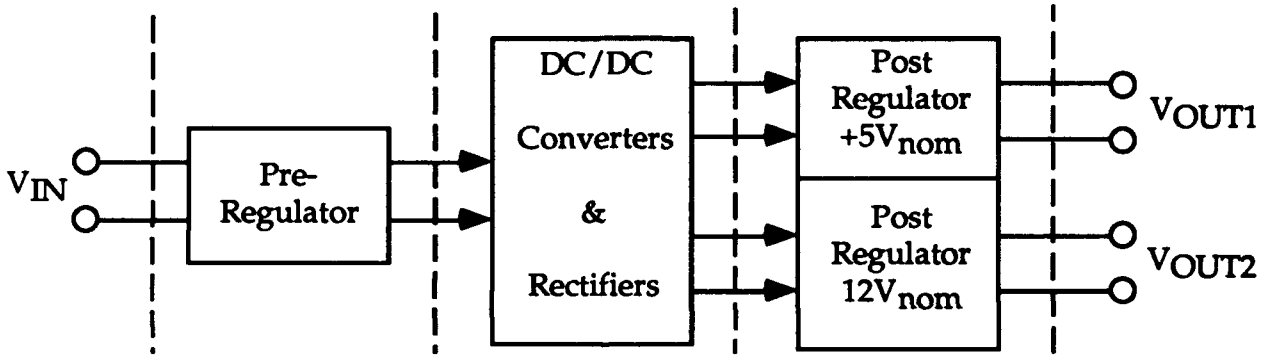


FIGURE 3: FUNCTIONAL BLOCK DIAGRAM OF A POWER SUPPLY

A theory of operation should be included as part of the report. If the reader is unfamiliar with the particulars of the system, the operational theory will provide needed background material.

3.2.2 Establishing Scope of Analysis

Developing the scope of the analysis involves the review of specifications, requirements and the functional breakdown prior to a decision as to which performance parameters should be examined.

Functionally, the scope of the analysis can be structured based on primary and secondary considerations. Primary considerations include the analysis of the worst case performance of a circuit and an analysis of proper part application (worst case stress vs. rated stress and derating requirements). Secondary considerations may include a mechanical assembly analysis which could directly affect shielding, noise, EMI, ground loops, and temperature control. Of course, the more complex the project becomes, the higher the cost.

WCCA characteristics to be examined can be influenced by various factors. Typically, the parameters highlighted in the analysis are directly related to the function/type of circuit/system to be examined. For instance, input impedance to a power supply circuit could be irrelevant, while it is a critical factor for RF amplifiers. There are numerous reasons why specific performance characteristics may be examined or ignored.

It is important that the customer is aware of what circuit/system characteristics are to be examined in the WCCA. The analyst should review the chosen performance characteristics with the customer and the designer. This assures that relevant parameters are examined and nonrelevant parameters are de-emphasized, thereby maximizing the benefits of the analysis.

A partial list of circuit performance parameters for a variety of circuit functions can be found in Section 5.2.1.

3.2.3 Part Database Development

Developing a part parameter database is the most critical task in producing an effective WCCA. It is also one of the most time-consuming tasks of the analysis. The part database can be compared to the foundation of a house. Without a solid foundation, the house collapses; without a solid part database, the WCCA may be invalid. Therefore, it is imperative that the database be as accurate as possible.

A large portion of the analyst's time will be spent compiling part parameter information. Critical parameters for the part database include environmental considerations. These should include but are not limited to temperature (ambient and self-heating), vibration, humidity, and radiation. Component aging can also

play a role in calculating parameter variation. Information sources for part data include both military and commercial specifications. Specifics related to the actual calculation of part parameters is detailed in Section 4.0.

A helpful procedure is to computerize the part database process. A computer can be used to store and retrieve part information or to calculate part tolerances for selected components based on projected operating temperature.

3.2.4 Method of Analysis

The analyst must decide which numerical method is to be used to complete the analysis. The method of analysis is then applied in the stress or performance calculations. There are three fundamental analytical methods used for WCCA: Extreme Value Analysis, Root-Sum-Squared, and Monte Carlo Analysis.

The Extreme Value Analysis (EVA) method is probably the most common and easiest to apply. It involves the analysis of a given circuit/system under the worst case realizable limits for individual parts. Whether the maximum or minimum foreseeable value of a part parameter is used is dependent on the directional sensitivity of that parameter on overall circuit performance (refer to Section 5.2.2). The results of an EVA represent the worst possible performance characteristics and are, therefore, conservative. It is unlikely that all part parameters will shift, simultaneously, to the worst case limits. The obvious benefit is that if the circuit meets performance criteria under these conditions, the customer can be confident of proper circuit operation under standard operating conditions.

The Root-Sum-Squared (RSS) analysis is another approach to performing a WCCA. This method is less common than either the EVA or the MCA. Fundamentally, the RSS method is a statistical approach to analyzing circuit performance. The random and bias portions of the part data (refer to Section 4.3) are considered separately. The bias terms contribute to a worst case baseline while the random terms are used to assist in calculating a standard deviation. Combining the two terms produces the worst case results. The results of an RSS analysis are more realistic than an EVA, but the technique is more labor intensive.

A Monte Carlo Analysis (MCA), as its name implies, involves randomly choosing part parameters and analyzing the circuit with the chosen parameters. This type of analysis is feasible only with the assistance of a computer. To enhance statistical results a large number of simulations must be made. Spence and Soin in Tolerance Design of Electronic Circuits, presents information on determining the number of needed simulations. A typical value for the number of simulations may be between 1,000 and 50,000 runs. Of course the number of simulations is dictated by number of components and variables. The exact number of simulations needed should be determined by the analyst. For the MCA to be accurate, it is necessary to know piece-part parameter distributions. This information is not always easy to obtain. If parameter distributions are not known, a Gaussian (Normal) distribution is typically assumed. The MCA is most appropriate if field performance part parameter distributions are known.

For more information regarding the various numerical methods utilized for WCCA, refer to Section 5.2.3.

3.2.5 Worst Case Stress Analysis

A worst case stress analysis serves to identify any component that may be overstressed under worst case conditions. If there are program derating guidelines, the stress analysis will also demonstrate whether or not the parts meet the program derating guidelines during worst case conditions.

The basic principle behind derating is that a component which is not stressed to its full potential should exhibit increased reliability. For instance, a general rule-of-thumb is that resistors should be derated by 50%. Therefore, if the resistor is rated for 1 Watt of power dissipation, then a maximum of .5 Watts should be dissipated.

If stress derating is not required, the worst case stress analysis still serves a very useful function. If unanticipated factors cause a component to be overstressed, the stress analysis should identify the overstressed component.

The part stress analysis should also be used to identify if the component is correctly applied; i.e., is sufficiently robust to meet the needs of the application. Since each component may exhibit various properties in many types of circuits and

environments, it is necessary to examine whether the correct component or component type is used. Of course, any misapplied or overstressed component must be brought to the attention of the designer. Refer to Section 5.1 for specifics regarding worst case stress analysis.

3.2.6 Worst Case Performance Analysis

The worst case performance analysis, as the name implies, analyzes the circuit to determine if it will perform as specified under worst case conditions. All environmental conditions and part parameters are simultaneously changed to their worst realizable extremes. The circuit is then analyzed to determine if the circuit performs correctly.

Although Section 5.0 deals with the specifics regarding worst case performance analysis, there are some general points that should be made.

As stated previously, it is imperative that the analyst partition the circuit into smaller units. Typically, this would involve minimizing the active components to as few logical blocks as possible.

Circuit diagrams and, if appropriate, timing diagrams should be included with the analysis so that the reader is knowledgeable of the circuit and parameters being examined. Also, all assumptions and parameters should be stated at the beginning of each analysis section so that the reviewer understands the performance parameters/variables considered during the analysis.

With the analysis complete, the analyst must compare the results of the WCCA with the specifications. All inconsistencies then need to be documented in the final WCCA report.

3.2.7 Document Production

Documenting the WCCA and its results is fundamental to presenting the analysis. Although there may be no specified format for the final document, there are some important points that should be made.

First, consistency among reports is extremely helpful if the WCCA is to be used as an integral part of product development or troubleshooting. The consistency of developing the analysis and the final report will save both time and money.

There is fundamental information that should be included as part of any analyses. First and foremost, the analysis results must be verifiable. Therefore, all information used to develop the analysis should be included or referenced in the report. This could include circuit equations, part data sources, and circuit simulation tools used, if applicable. Definition of the critical attributes analyzed and the reason(s) why these particular attributes were chosen must be documented.

In general, the report should include the appropriate schematics, functional block diagrams, and a functional description/theory of operation. The report should also have sufficient narrative material throughout the analysis describing what parameters are being analyzed and verified. All equations and models used during the analysis should be explained. This will assist the reviewer in understanding the approach used during the analysis. Graphics can also be an excellent method of concisely conveying information or a principle. Graphics could include outputs from computer simulations, performance matrices, histograms (if an MCA is utilized), timing diagrams, and part parameter graphs.

If problem areas are found during the worst case stress and performance analysis, the analyst should be prepared to address potential fixes to the problem. If possible, various solutions should be presented to allow choices for management and engineering to correct or minimize the problem.

4.0 PART DATABASE DEVELOPMENT AND GUIDELINES

One of the most critical steps involved in completing a WCCA is the development of a part database. A part database contains a composite of information for quantifying sources of component variation. Once the most probable sources of component parameter variation have been identified, the database can be used to calculate worst case component drift for critical parameters. Establishment of a component database is recommended for all analysis complexity levels.

4.1 Sources of Component Tolerance Variation

Actual field performance indicates that components tend to drift beyond initial tolerance levels. Therefore, the basis for establishing component variability limits must be organized and presented in the analysis assumptions. Analysis assumptions should describe component tolerance level, as well as effects due to environmental conditions and aging on each component type. In some cases, the magnitude and direction of variation can be predicted. For most parts, variation is assumed to be normally distributed around the nominal value based on a predicted standard deviation.

The magnitude of component tolerance variation is dependent upon a variety of sources. Table 1 illustrates a number of part types and the principal sources of variation for each.

TABLE 1: PART TYPES VS. PRINCIPAL SOURCES OF VARIATION

	Transistor	Diode	Zener Diode	DIGITAL/ IC	LINEAR/ IC	Resistor	Capacitor	Inductor	RELAYS
Temp.	X	X	X	Note 1	Note 1	X	X	X	X
Aging	X	X	X	X	X	X	X	X	X
Radiation	X	-	-	X	X	-	-	-	-
Mechanical	-	-	-	-	-	X	X	X	X
Humidity	-	-	-	-	-	X	X	-	-
Life (U/P), P	-	-	-	-	-	X	X	-	-
Vacuum	-	-	-	-	-	X	X	-	-

Note 1: Performance limits usually specified over entire range and interpolation usually not possible.

X: Part is significantly affected by environment (P): Powered (U/P): Unpowered

The sources of variation presented in Table 1 have specific effects on component electrical characteristics. Table 2 is an expansion of Table 1; it describes the component parameters that are affected by specific variation.

TABLE 2: AFFECTED PARAMETERS VS. SOURCE OF VARIATION

Component Type	Environmental Source of Variation	Parameter Affected
Bipolar Transistors Field Effect Transistors	Temperature	H_{FE} (Bias), V_{BE} (Bias) I_{CBO} (Bias) RDS_{ON} (Bias), V_{TH} (Bias)
	Radiation	H_{FE} (Bias), I_{CBO} (Bias) U_{CE} (Sat) (Random & Bias) U_{TH} (Bias)
Rectifiers/Switching Diodes	Temperature	V_F (Bias), T_S (Bias), I_R (Bias)
	Radiation	I_R (Bias), U_F (Bias)
Zener Diodes	Temperature	V_Z (Bias), (Sometimes Random) Z_Z (Bias)
Resistors	Temperature Humidity Aging (P) Life (U/P) Vacuum Mechanical	Resistance (Bias & Random, Random) Resistance (Bias) EC Carbon Comp Resistance (Bias & Random) Evaporation of Entrapped Humidity (Bias) Resistance (Bias & Random)
Capacitors	Temperature Aging Mechanical Electrical Vacuum Humidity	Capacitance (Bias and/or Random) ESR (Bias), DF (Bias, Non Linear) ESR (Bias), Capacitance (Bias and/or Random) Capacitance Voltage Coefficient Capacitance (Bias, Non Hermetic) Capacitance (Bias)
Linear ICs	Radiation Temperature	V, I offset (Random), A_{OL} (Bias) V, I offset (Bias & Random), Random A_{OL} (Bias)
Digital ICs	Radiation	Propagation Delay (Bias)
Magnetics (strongly dependent on materials)	Temperature Aging Mechanical	Saturation flux density (Bias) Permeability (Bias) Core Loss (Bias, Non-linear, Non Mono) Saturation flux density (Bias, very small) Permeability (Bias) Sat flux density (Bias)
Relays	Temperature	Pull in/Prop out current/volts (Bias) Contact resistance (Bias, Secondary effect, not material aging) Mechanical Contact Resistance (Bias)

(P): Powered

(U/P): Unpowered

It can be seen from Table 2 that temperature has a direct impact on the magnitude of component variation. The determination of case temperature for components is complex due to the fact that:

Temperature = Local Ambient + Self Heating

Local Ambient = Ambient + Internal Delta

The formulas above look simplistic. However, component temperature cannot be determined independently given the radiation of heat from other components on the board. Therefore, it is recommended that a thermal analysis be done prior to completing the WCCA. Levels of thermal analysis options can be determined as:

1. Perform a detailed thermal analysis early in the design to establish the upper limit of part body temperatures; usually not possible due to immaturity of design.

2. Perform a preliminary thermal analysis and, based on the analysis results, establish an upper-bound component body temperature criterion. This criterion will then be used in defining the body temperature limits used for assessing part variations and for specifying the thermal design. This is the most practical approach since it permits early definition and does not penalize the parts in favor of the thermal design, or vice versa.

3. Define a worst case body temperature limit based on either reliability or WCCA limits and let this dictate the thermal design. The significant risk here is that the temperature extremes chosen are too "extreme" thereby leading to conservative circuit performance or compromised reliability.

4.2 Part Statistics

There are two types of component variation: random and bias. Random variation is not predictable in direction. Bias, on the other hand, is predictable given known inputs. All sources of component variation can be grouped into one

of these effects. Bias and random effects are combined to give an overall indication of part variability. Addition of individual random and biased variables is as follows:

Bias Effects - Added Algebraically

Random Effects - Root Sum Squared (usually assumed to be expressed as the 3σ limits of a normally distributed population)

Determination of the minimum and maximum limits of component value due to drift is as follows:

$$\text{Worst Case Minimum} = \text{Nominal Value} - \Sigma\,|\,\text{Biases}\,| - \sqrt{\Sigma\,(\text{Randoms})^2}$$

$$\text{Worst Case Maximum} = \text{Nominal Value} + \Sigma\,|\,\text{Biases}\,| + \sqrt{\Sigma(\text{Randoms})^2}$$

Table 3 presents the results of a computation of a CLR capacitor limit based on multiple effects. The 1200µF CLR capacitor, is affected by initial tolerance, temperature, vacuum stability, radiation, and aging.

TABLE 3: DETERMINATION OF MIN AND MAX VALUES FOR CLR CAPACITORS

Parameters: Capacitance	Bias %		Random %
	Neg.	Pos.	
Initial Tolerance at 25°C	--	--	20
Low Temp. (-20°C)	28	--	--
High Temp. (+80°C)	--	17	--
Other-Envt's (Hard Vacuum)	20	00	00
Radiation (10KR, 10E 13 N/CM2)	--	12	--
Aging	--	--	10
TOTAL VARIATION	48	29	$\pm\sqrt{(20)^2 + (10)^2} = 22.4$

WORST CASE, CAPACITANCE MIN. -70.4%: MAX. +51.4% OF NOMINAL

Once the magnitude of random and bias effects are established, it is relatively easy to calculate component variation limits.

Worst Case Minimum: 1200 µF -.48 • 1200 µF - .224 • 1200 µF
Worst Case Minimum = 355.2 µF

Worst Case Maximum: 1200 µF + .29 • 1200 µF + .224 • 1200 µF
Worst Case Maximum = 1816.8 µF

4.3 Part Tolerance Calculations

Quantifying the contribution of environmental effects on component variability is a critical step in the development of a WCCA. The analyst does not want to be overly pessimistic or optimistic when establishing component limits. There are a number of sources that can be reviewed to establish random and biased contributions to variability. These are summarized by the following:

1) MIL Specifications
   - Conservative - Minimum requirements that all vendors must meet to be on QPL

2) Vendor Data
   - Must be able to justify use
     - Vendor documentation of test conditions, sample size, number of lots, etc.
     - Procurement restricted to that vendor

3) Company Data
   - Historical test data from previous programs
   - Special test programs (e.g., radiation tests)

4) Outside Sources
   - e.g., JPL for radiation data

At present, there are few data sources beyond published military documents that describe component requirements for durability. These documents typically portray a pessimistic approach to calculating component variability because they do not necessarily reflect actual conditions. The following sections discuss methods for establishing worst case parameters at the component level.

Briefly, passive components are discussed in the form of examples while active components and ICs are addressed through general discussion. Sections 4.3.1 - 4.3.6 are presented in this manner for the following reasons:

1) Passive components are typically selected based on style, power rating and value. Therefore, construction standards are often not reviewed

prior to selection. Sections 4.3.1 and 4.3.2 illustrate how component variation can be determined using military specifications for the component.

2) Active components and ICs are tested for critical parameters. Often, designers are familiar with the device characteristics through data sheet review prior to the selection of the device. Therefore it is assumed that the majority of readers are familiar with extrapolating component data from vendor sheets. This skill is required for calculating component variation.

4.3.1 Resistor Example: (RNR50)

The following example illustrates the derivation of component drift parameters based on the following:

Part Type: RNR50H1002FS
Description: 1%, .05 Watts
Value: 10K
Temperature: 0°C - 80°C
Expected Operational Hours: 10,000
Failure Rate Level: S

MIL-STD-199C, "Resistors, Selection and Use of" contains the information required to develop the component drift parameters for an RNR resistor. It is important to note that the values for drift found in this document are component requirements as opposed to measured values. Therefore, the variation calculation is most likely going to be pessimistic. Figure 4 is an excerpt from MIL-STD-199C. Developing the magnitude of variation is as follows:

The initial component tolerance is typically given. In this example, the initial tolerance can also be found by cross-referencing the part type designation with the information provided in Figure 4. In this case, the letter F, in the part type designation, signifies a 1% resistor.

MIL-STD-199C
28 AUGUST 1981

SECTION 302
RESISTORS, FIXED, FILM, ESTABLISHED RELIABILITY

STYLES RNR50, RNR55, RNR60, RNR65, RNR70, RNR75, AND RNC90 (SEE NOTE 1/)
(APPLICABLE SPECIFICATION: MIL-R-55182)

1. SCOPE. This section covers established reliability, film, fixed resistors, including both hermetically and nonhermetically sealed types. These resistors possess a high degree of stability, with respect to time, under severe environmental conditions, with an established reliability. These resistors provide life failure rates ranging from 1.0 percent to 0.001 percent per 1,000 hours. The failure rates are established at a 60-percent confidence level (initial qualification) and maintained at a 10-percent producer's risk. ***The failure rate is referred to operation at full-rated wattage and temperature with a maximum change in resistance of ±2.0 percent at 0 to 10,000 hours of life test.***

These resistors are designed for use in critical circuitry where high stability, long life, reliable operation, and accuracy are of prime importance. They are particularly desirable for use in circuits where high frequencies preclude the use of other types of resistors. Some of the applications for which these film-type resistors are especially suited are as follows: high-frequency, tuned circuit loaders, television side-band filters, rhombic antenna terminators; radar pulse equipment; and metering circuits, such as impedance bridges and standing wave-ratio meters.

2. APPLICATION INFORMATION.

2.1 Construction. In these resistors the resistance element consists of a metal film element on a ceramic substrate. The element is formed by the condensation of a plated metal under vacuum conditions. Following spiralling to increase the available resistance values and the attachment of leads, the element is protected from environmental conditions by an enclosure. Due to the reliability requirements of MIL-R-55182, processes and controls utilized in manufacturing are necessarily more stringent. MIL-STD-790, "Reliability Assurance Program for Electronic Parts Specifications", provides for monitoring and documentation of these requirements.

2.2 Derating at High Temperatures. The power rating is based on operation at 125°C. However, when a resistor is to be used in a circuit where the surrounding temperature is higher than 125°C, a correction factor must be applied to the wattage rating so as not to overload the resistor. The correction factor may be taken from the curve shown in Figure 302-1.

2.3 Derating for Optimum Performance. Because all of the electrical energy dissipated by a resistor is converted into heat energy, the temperature of the surrounding air is an influencing factor when selecting a particular resistor for a specific application. The power rating of these resistors is based on operation at specific temperatures; however, in actual use, the resistor may not be operating at these temperatures. When the desired characteristic and the anticipated maximum ambient temperatures have been determined, a safety factor of 2, applied to the wattage, is recommended in order to insure the selection of a resistor having an adequate wattage-dissipation potential.

2.4 Design Tolerance. ***Combined effects of use and environment may result in a ±2 percent change from nominal*** value in a resistor of the preferred ±1 percent nominal resistance tolerance. Circuits, therefore, should be designed to accept this ±2 percent variation in resistance while continuing to operate properly.

2.5 Moisture Resistance. Metal film resistors are essentially unaffected by moisture. *The specification allows only a 0.4 percent change in resistance value as a result of exposure to a standard 10-day moisture resistance test.*

Third letter is variable, dependent upon lead material or capability (see 3.4).

302 (MIL-R-55182)
28 August 1981

FIGURE 4: EXCERPT FROM MIL-STD-199C

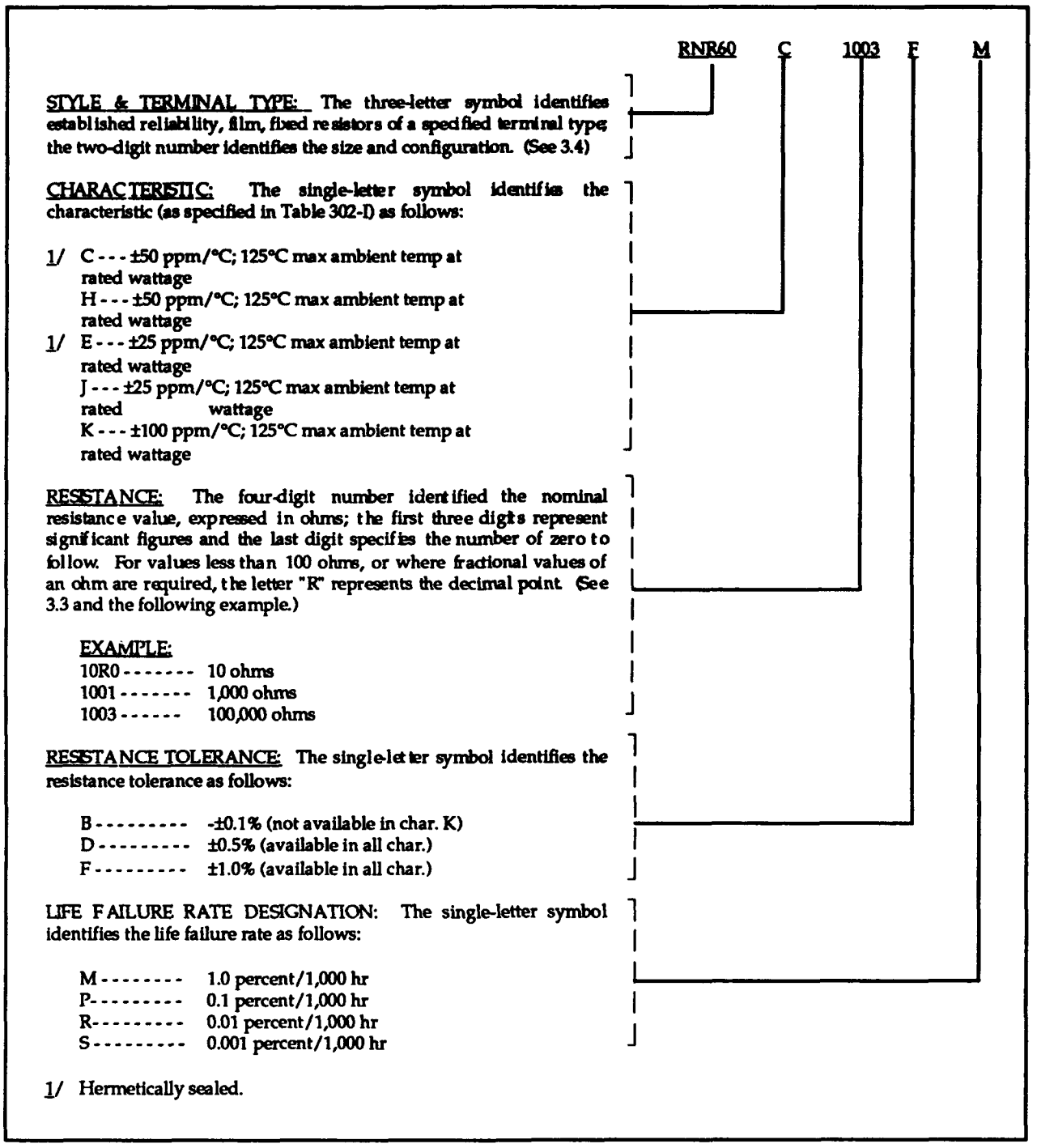


FIGURE 4: EXCERPT FROM MIL-STD-199C (CONT'D)

TABLE 302-I. Performance Characteristics.

Features	H (Nonhermetically sealed)	Y (Nonhermetically sealed)
Max resistance-temperature characteristic:		
Percent per degree C	*±0.005*	*±0.0005*
Parts/million/°C	*±50*	*±5* 1/
Max ambient temperature at rated wattage	125°C	125°C
Max ambient temperature at zero wattage derating	125°C	175°C
Power rating in watts and max dc or rms voltage at 125°C		
Style RNR50	1/20 W, 200V	Not Available
Style RNR55	1/10 W, 200V	Not Available
Style RNR60	1/8 W, 250V	Not Available
Style RNR65	1/4 W, 300V	Not Available
Style RNR70	1/2 W, 350V	Not Available
Style RNR75	Not Available	Not Available
Style RNC90	Not Available	.3W, 300V
Power rating in watts and max dc or rms voltage at 70°C		
Style RNR50	1/20 W, 200V	Not Available
Style RNR55	1/8 W, 200V	Not Available
Style RNR60	1/4 W, 300V	Not Available
Style RNR65	1/2 W, 350V	Not Available
Style RNR70	3/4 W, 500V	Not Available
Style RNR75	Not Available	Not Available
Style RNC90	Not Available	.6W, 300V
Min and max resistance values:	Min Max	Min Max
Style RNR50	49.9 .796M	Not Available
style RNR55	49.9 .796M	Not Available
Style RNR60	2.0 3/ 4.02M	Not Available
Style RNR65	1.0 3/ 8.06M	Not Available
Style RNR70	1.0 3/ 15M	Not Available
Style RNR75	Not Available	Not Available
Style RNR90	Not Available	30.1
Max percent change in resistance values: 1/		
Temperature cycling	0.2	0.05
Overload		
Low temperature operation	0.15	0.05
Low temperature storage	0.15	0.05
Terminal strength	0.2	0.02
Dielectric withstanding voltage	0.15	0.02
Resistance to soldering heat	0.1	0.02
Moisture resistance	0.2	0.05
Shock (specified pulse)	0.2	0.01
Vibration, high frequency	0.2	0.02
Life	*See* 5/	*See* 6/
High temperature exposure	0.5	0.05
Insulation resistance (dry)	10,000 M Ω, min	10,000 M Ω, min
Insulation resistance (wet)	100 M Ω, min	100 M Ω, min
Resistance tolerance (± percent)	*1.0*, 0.5, 0.1	1.0, 0.5, 0.1 0.05, 0.01, 0.005

1/ Where total resistance change is 1 percent or less, it shall be considered as ± (Percent +0.01 ohm).
2/ *The DR requirements shall be ±0.05 percent (qualification,* 2,000 hr duration); ±0.5 percent (10,000 hr duration).
3/ Minimum is 10 ohms for B (.1%) tolerance.
4/ Where total resistance change is 1 percent or less, it shall be considered as ±(percent +0.01 ohm)
5/ *The DR requirements shall be ±0.5 percent (qualification, 2,000 hour duration); ±2.0 percent (10,000 hour duration).*
6/ the DR requirement shall be ±0.05 percent (qualification, 2,000 hour duration); ±0.5 percent (10,000 hour duration).

FIGURE 4: EXCERPT FROM MIL-STD-199C (CONT'D)

The next step involves determining component variability due to temperature. From Figure 4 this resistor has a temperature factor of 50 ppm/°C. This translates into .005%/°C.

Since ambient temperature is typically assumed to be 25°C, the resistor variability due to temperature fluctuations can be calculated as follows:

$$\text{High Temp } \%\Delta = (80°C - 25°C)(.005\%/°C) = .275\%$$

$$\text{Low Temp } \%\Delta = (25°C - 0°C)(.005\%/°C) = .125\%$$

The analyst then needs to determine resistor variability due to additional factors given in MIL-STD-199C. For this example, temperature cycling, low temperature operation and storage, terminal strength, dielectric withstanding voltage, resistance to soldering heat, moisture resistance, shock, vibration and high temperature exposure effects were included in the calculations.

The percent resistance change values can be found in Figure 4. Since these factors are random variables the calculation is as follows:

$$\text{Other Factors } \%D = \sqrt{5(.2\%)^2 + 2(.15\%)^2 + (.1\%)^2 + (.5\%)^2} = .71\%$$

Another factor that needs to be included is variability due to aging. The first step involves determining the failure rate percentage per time. Since this is a Class S device, MIL-STD-199C states that the failure rate is .001%/hour. The failure rate criteria is defined as 2% drift over 10,000 hours. Since the expected operational time of the device is 10,000 hours the adjusted failure rate is:

(.001%/1000 hours)(10,000 hours) = .01% fail

Hence, 99.99% of the resistors do not fail beyond the 2% drift limit.

Component variation limits are typically based on a 3σ limit. The 3σ limit represents 99.7% of observed effects that behave according to a Normal Distribution. Since 99.99% of the resistors do not fail, they fall within the 3.8σ limits. This is determined as follows:

$$\frac{.9999}{2} = .49995 \qquad \text{(Due to symmetry of distribution)}$$

Table 4 is an excerpt from an area of a Standard Normal Distribution table. Locate .49995 in the table and reference the values in the left column and top row. Again, in this case, .49995 corresponds to the 3.8σ limit.

The aging factor can now be calculated by using the following ratio:

$$2\% \left(\frac{3\sigma}{3.8\sigma}\right) = 1.58\%$$

The component data sheet for this example is presented in Table 5.

4.3.2 Capacitor Example: (CKR05)

The following example illustrates the derivation of component drift parameters based on the following:

Part Type: CKR05
Description: 10%, 200 volts
Value: 10pF
Temperature: -55°C to 125°C
Expected Operational Hours: 50,000
Failure Rate Level: R
Stress Level: 50%

TABLE 4: AREAS OF NORMAL PROBABILITY CURVE

t	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
0.0	.0000	.0040	.0080	.0120	.0160	.0199	.0239	.0279	.0319	.0359
0.1	.0398	.0438	.0478	.0517	.0557	.0596	.0636	.0675	.0714	.0753
3.7	.4999	.4999	.4999	.4999	.4999	.4999	.4999	.4999	.4999	.4999
3.8	.4999	.4999	.4999	.4999	.4999	.4999	.4999	.4999	.4999	.5000
3.9	.5000	.5000	.5000	.5000	.5000	.5000	.5000	.5000	.5000	.5000

TABLE 5: EXAMPLE RESISTOR DATA SHEET

Parameter: Resistance	Bias %		Random %	Data Source/ Comments
	Neg.	Pos.		
Initial Tolerance, 25°C			1.0	MIL-STD-199
High Temp. (80°C)			0.275	MIL-STD-199 (±50 ppm/°C)
Low Temp. (0°C)			0.125	MIL-STD-199 (±50 ppm/°C)
Other			0.71	MIL-STD-199 (RSS)
Aging (10,000 hrs.)			1.58	MIL-STD-199 Class "S"
Totals:	0	0	±2.02 ±2.00	High Temp. Low Temp.

W.C. Tolerance: Min -2.02% Max +2.02%

MIL-STD-198E, "Capacitors, Selection and Use of", provides the requirements for military capacitors. An excerpt from MIL-STD-198E is presented in Figure 5. Using the excerpt, the following component variation calculation can be made. The capacitor tolerance calculations are similar, but not the same, as the resistor calculations.

As stated, the initial tolerance is stated to be ±10%. Manufacturer specifications will probably indicate that ±10% tolerance, but it is also explicitly stated in MIL-STD-198E in the section for CKR05 capacitors. Refer to Figure 5 for an excerpt from MIL-STD-198E for CKR capacitors.

MIL-STD-198E

SECTION 901

CAPACITORS, FIXED, CERAMIC DIELECTRIC, (GENERAL PURPOSE), ESTABLISHED RELIABILITY STYLES CKR05, CKR06, CKR11, CKR12, CKR14, CKR15, CKR22, AND CKR23 (APPLICABLE SPECIFICATION: MIL-C-39014)

1. SCOPE. This section covers established reliability, general purpose, ceramic dielectric, insulated, fixed capacitors. *These capacitors have failure rate levels ranging from 1.0 to 0.001 percent per 1,000 hours. The failure rate levels are established at a 90-percent confidence level and are based on operation at full rated voltage at the maximum rated temperature. NOTE: A failure is defined as a drift ≥ 20% (±).*

2. APPLICATION INFORMATION

2.1 Use. These capacitors are primarily designed for use where a small physical size with comparatively large electrical capacitance and high insulation resistance is required. Ceramic capacitors are substantially smaller than paper or mica units of the same capacitance and voltage rating. General-purpose ceramic capacitors are not intended for precision use but are suitable for use as by-pass, filter, and non-critical coupling elements in high-frequency circuits where appreciable changes in capacitance, caused by temperature variations, can be tolerated. These units are not recommended for use directly in frequency-determining circuits. Typical recommended applications include resistive-capacitance coupling for audio and radio frequency, RF and intermediate frequency cathode bypass, automatic volume control filtering, tone compensation, volume-control RF bypass, antenna coupling, and audio-plate RF bypass. All of these applications are of the type where dissipation factor is not critical, and moderate changes due to temperature, voltage, and frequency variations do not affect the proper functioning of the circuit. For example: An emitter bypass for 100 megahertz (MHz), having a nominal capacitance of 680 picofarads (pF), will give a capacitance reactance of 2.34 ohms. Since this reactance is very small compared with the emitter resistor, there would be no measurable effect on the 2.34-ohm value if the capacity should change by several percent due to a temperature variation, nor would a dissipation of 4 percent be noticeable.

Disk and thin-plated subminiature types are extremely compact and have an inherent low-series inductance due to their construction. The placement of the leads facilitates making close-coupled low-inductance connections and these capacitors are suitable for printed-circuit applications. High insulation resistance allows these capacitors to be used in vacuum-tube grid circuits; their extremely low leakage and small physical size make them suitable for use in transistor circuitry.

During circuit design, consideration should be given to the changes in dielectric constant caused by temperature, electric field intensity, applied frequency, and shelf aging.

2.1.1 Humid Operating Conditions. Ceramic dielectric materials are nonhygroscopic, effectively impermeable, and have practically no moisture absorption even after considerable exposure to humid conditions. Thus, these units are intended to operate, through their full temperature range, at relative humidities up to 95 percent. Nevertheless, the termination materials under moisture conditions are subject to ionic migration which can cause capacitor failure (see 2.8).

2.2 Construction. A ceramic capacitor consists of a ceramic dielectric on which a thin metallic film, usually silver, has been fired at very high temperatures. Terminal leads are attached to the electrodes by a pressure contact or by soldering. Ceramic capacitors are encapsulated to protect the dielectric from the environment and to electrically insulate the capacitor. The disk types are covered by an insulating resin, plastic, or ceramic; the thin-plated subminiature types may be in dipped, molded, or performed cases. The feed-through units are made of ceramic tubes modified for their required mounting. Because the constituent materials have molecular polar moments, the dielectric constants of some mixes reach hundreds (even thousands), of times the value of paper, mica, and plastic films. This results in ceramics having the largest capacitance-to-size ratios of all high-resistance dielectrics.

901 (MIL-C-39014)

901.1

FIGURE 5: EXCERPT FROM MIL-STD-198E

2.3 DC voltage rating. These capacitors are available in a wide voltage range which varies with the capacitor style. The voltage range varies from 50 volts dc to 200 volts dc.

2.4 Soldering. Care should be used in soldering the leads. Excessive heat may damage the encapsulation and weaken the electrode to terminal lead contact. Sudden changes in temperature, such as those experienced in soldering, can crack the encapsulation or the ceramic dielectric. Leads should not be bent close to the case nor should any strain be imposed on the capacitor body to avoid fracturing the encapsulation or ceramic dielectric.

2.5 Dissipation factor. For the recommended applications, the dissipation factor is negligibly low. The power factor decreases as temperature is increased; this provides an advantage where operation above room temperature is required.

2.6 Case insulation. It is not intended that the case insulation be subjected to sustained voltage in excess of 150 percent of the dc rated voltage of the capacitor. Supplementary insulation should be provided where the case may come in contact with higher voltage.

2.7 Capacitance as a function of operating conditions. The dielectric constant of these capacitors exhibits a considerable dependence on field strength. Large variations in capacitance may be experienced with changes in ac or dc voltages. The dielectric constant may decrease with time and may be as low as 75 percent of the original value after 1,000 hours. The dielectric constant is dependent on frequency and decreases as the frequency is increased; it also decreases with temperature.

2.8 Silver migration. When silver electrodes in the ceramic capacitor are expand to high humidities and high dc potentials, silver ion migration may take place and short circuit capacitors after relatively short periods of time. Excessive moisture during periods of storage should be avoided since the encapsulation material may absorb moisture and silver ion migration may occur when the capacitors are later put into service.

2.9 Operating temperature range. These capacitors are suitable for operation over a temperature range of -55° to +125°C.

2.10 Failure-rate level determination. The curves presented on figure 901-1 are the best engineering approximation of the reliability characteristics (random failures) for these capacitors when employed repeatedly, within their specification ratings, in complex electronic equipment. These reliability characteristics are based on ground-level severity experience. Failures are considered to be opens, shorts or radical departures from initial characteristics. The failures are considered to be occurring in an unpredictable manner and in too short a period of time to permit detection through normal preventive maintenance. The curves shown on figure 901-1 are based on "catastrophic failures" and will differ from the failure rates established in the specification, since the established failure rates are based on "parametric failures" over long term life tests at rated conditions. This figure has been extracted from MIL-HDBK-217, "Reliability Stress and Failure Rate Data for Electronic Equipment." The curves have been modified from their original versions that the ordinate has been normalized in order to provide multiplier factors in place of discrete failure rate levels and in order that the multiplying factor for a failure rate at rated conditions is unity. As indicated, these curves are the best estimate based on "catastrophic failure;" however, they can provide an estimate of the relative effect of operating under conditions other than rated.

3. ITEM IDENTIFICATION

3.1 Standard capacitors. The standard capacitors available in this section are shown in figure 901-2. (The figure gives the electrical characteristics, failure rate levels, and Military part numbers which are standard for design).

FIGURE 5: EXCERPT FROM MIL-STD-198E (CONT'D)

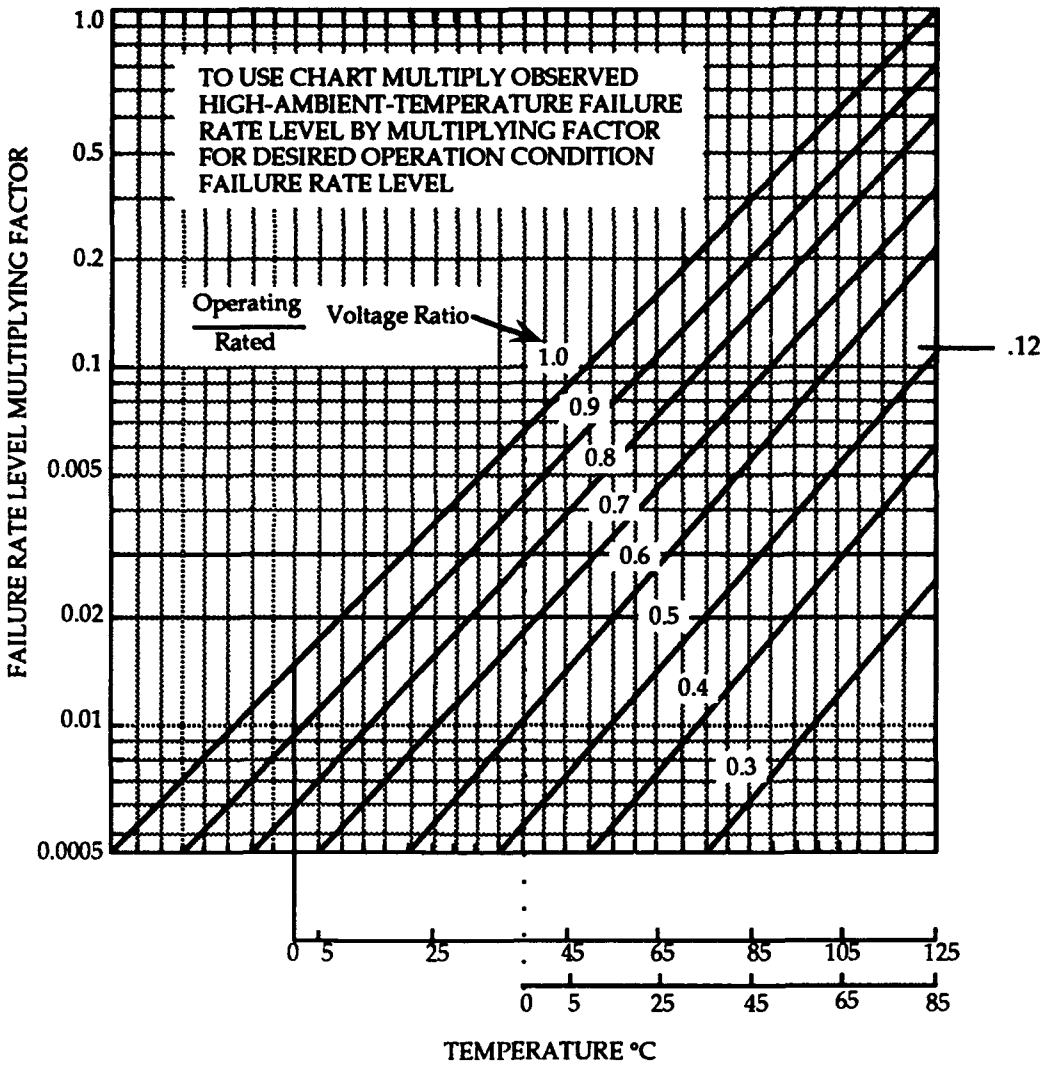


FIGURE 901-1 Failure Rate Level Curves

901.3 901 (MIL-C-39014)

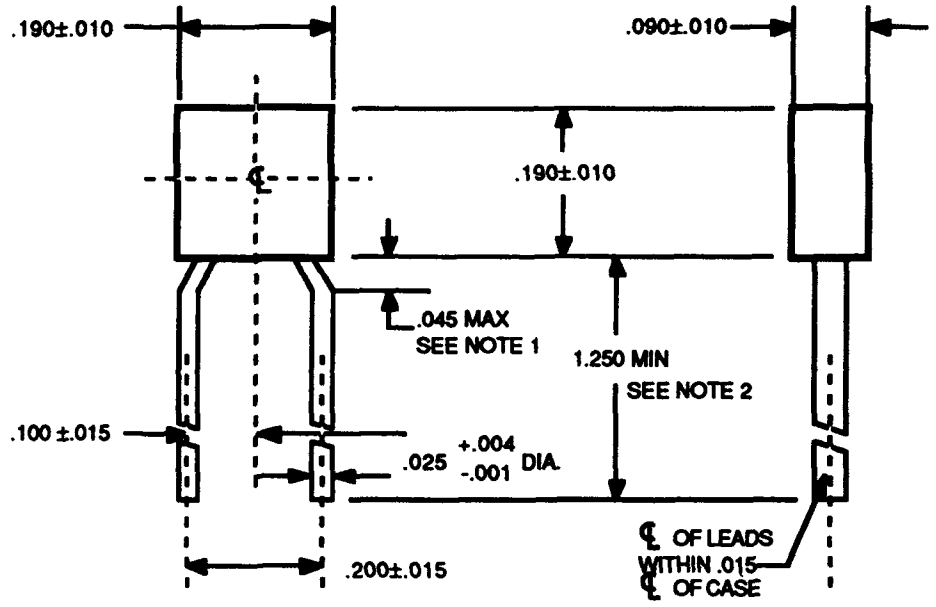
FIGURE 5: EXCERPT FROM MIL-STD-198E (CONT'D)

MIL-STD-198E

STANDARD CAPACITORS

STYLE CKRO5 (MIL-C-39014/1)
NATO TYPE DESIGNATION: NCC61

OPERATING TEMPERATURE RANGE -55° TO +125°C –VOLTAGE TEMPERATURE LIMITS (CAP. CHANGE WITH REFERENCE TO +25°C) ±15 PERCENT WITH ZERO VOLTS APPLIED AND +15, -25 PERCENT WITH DC RATED VOLTAGE APPLIED



INCHES	MM
.001	.03
.004	.10
.01	.25
.015	.38
.025	.64
.045	1.14
.090	2.29
.100	2.54
.190	4.83
.200	5.08
1.250	31.75

NOTES:

1. For flush mounting, a .078(1.98 mm) printed-circuit hole diameter is required to clear shoulder.
2. Lead length may be a minimum of one inch long for use in tape and reel automatic insertion equipment, when specified.

FIGURE 5: EXCERPT FROM MIL-STD-198E (CONT'D)

MIL-STD-198E STANDARD CAPACITORS

DC Rated Voltage	Capacitance Value	Capacitance Tolerance	Part number M39014/01- Failure Rate Level in %/1,000 Hrs.			
			1.0(M)	0.1(P)	0.01(R)	0.001(S)
Volts	pF	Percent				
200	10	±10	1201	1241	1281	1321
↓	10	±20	1202	1242	1282	1322
↓	12	±10	1203	1243	1283	1323
↓	15	±10	1204	1244	1284	1324
↓	15	±20	1205	1245	1285	1325
↓	18	±10	1206	1246	1286	1326
↓	22	±10	1207	1247	1287	1327
↓	22	±20	1208	1248	1288	1328
↓	27	±10	1209	1249	1289	1329
↓	33	±10	1210	1250	1290	1330
↓	33	±20	1211	1251	1291	1331
↓	39	±10	1212	1252	1292	1332
↓	47	±10	1213	1253	1293	1333
↓	47	±20	1214	1254	1294	1334
↓	56	±10	1215	1255	1295	1335
↓	68	±10	1216	1256	1296	1336
↓	68	±20	1217	1257	1297	1337
↓	82	±10	1218	1258	1298	1338
↓	100	±10	1219	1259	1299	1339
↓	100	±20	1220	1260	1300	1340
↓	120	±10	1221	1261	1301	1341
↓	150	±10	1222	1262	1302	1342
↓	150	±20	1223	1263	1303	1343
↓	180	±10	1224	1264	1304	1344
↓	220	±10	1225	1265	1305	1345

FIGURE 901-2. Established Reliability, General Purpose, Ceramic Dielectric, Fixed Capacitors.

FIGURE 5: EXCERPT FROM MIL-STD-198E (CONT'D)

The analyst now needs to calculate/determine the temperature/voltage effects. First, MIL-STD-198E states that with zero volts applied to the capacitor at 25°C there is a ±15% swing in the capacitance.

Next, the dielectric experiences a direct (bias) affect due to temperature and voltage. It is assumed from the information in Figure 5 that as the temperature increases the capacitance will decrease. The actual stress on the capacitors is 50% of the rated voltage, therefore, the temperature/voltage tolerances will be decreased in half. Thus the negative bias tolerance is 12.5% and the positive bias tolerance is 7.5% using the information provided in the excerpt from MIL-STD-198E.

It is also necessary to calculate tolerance limits due to aging effects. This is identical to the resistor calculation except for two things. First, the 3s life requirement is to be equal or less than the initial tolerance (according to MIL-C-39014/1-81349); this is not stated in MIL-STD-198E for CKR capacitors. Also, there is an adjustment factor based on a 50% stress level. For 50% stress, at maximum temperature, there is a .12 multiplier for the failure percentage calculation. Refer to the Failure rate level curve graph in Figure 5 to locate this value. Therefore, the aging calculation is as follows:

$$\% \text{ Fail} = (0.01\%/1000 \text{ hours})(0.12)(50{,}000)$$
$$= .06\%$$

$$\therefore \% \text{ Pass} = 99.94\% \rightarrow 3.44\sigma$$

$$3\sigma \text{ Drift} = (10\%)\left(\frac{3}{3.44}\right) = 8.7\%$$

The component data sheet for this example is presented in Table 6.

TABLE 6: EXAMPLE CAPACITOR DATA SHEET

Parameter: Resistance	Bias %		Random %	Data Source/ Comments
	Neg.	Pos.		
Initial Tolerance, 25°C			10.0	MIL-STD-198
Temp./Voltage	12.5	7.5	15.0	MIL-STD-198 Class "R"
Aging (50,000 Hrs.)			8.7	MIL-STD-198 Class "R"
Totals:	-12.5	7.5	20	

W.C. Tolerance: Min - 32.5% Max +27.5%

4.3.3 Semiconductors

Semiconductor performance under worst case conditions can be extrapolated from vendor data sheets in most instances. Aging parameters can also be derived from vendor data. It is important to note that aging of semiconductors has a significant effect (±15%/10,000 hrs.) on critical parameters. This fact is further emphasized in MIL-STD-701 entitled "Semiconductors, Selection and Use Of".

4.3.4 Digital IC's

In many cases, the analyst is concerned with minimum and maximum propagation delay, the voltage compatibilities between chips, drive capability and supply variation when considering worst case digital performance. Much of the information required to perform a digital worst case analysis can be obtained from vendor data sheets. However, typical data sheets present worst case data based on an operating temperature of 25°C, R_L = 400Ω (load resistance), C_L (load capacitance) = 15pF and V_{CC} = 5V or 12V.

In many cases this data needs to be enhanced to account for the following:

- Temperature Effects
- Supply Voltage Variations
- Load Capacitance Effects
  - Device Capacitance
  - Interboard Capacitance
  - Connector Capacitance
- Line Delays
- End-of-Life Derating Effects
- CMOS Device Considerations

4.3.4.1 Temperature Effects on Digital Circuits

Most vendors supply propagation delay information based on a temperature range from -55°C to 125°C. If the case occurs when rated qualifying temperatures are specified beyond the boundaries of the analysis, the following formula should be used:

$$T_p = \frac{T_p \text{ (Full Temp.)} - T_p \text{ (25°C) Max}}{\Delta \text{ Temp °C (Full Range)}} \bullet (T \text{ (actual)} - 25°C) + T_p \text{ (25°C) Max}$$

where

T_p = Maximum propagation delay at the analysis temperature

As an example, a 54LS00 device has propagation delay characteristics of 17nS at 25°C and 24nS at 125°C. If analysis boundaries were based on an 80°C maximum, the maximum propagation delay for the device would be calculated as:

$$T_p \text{ (80°C)} = \frac{24nS - 17nS}{125°C - 25°C} \times (80°C - 25°C) + 17nS$$

$$= 20.85nS$$

4.3.4.2 Supply Voltage Variations

Most vendors publish the operating supply voltage range required for operation. However, very few vendors detail the effects of varying supply voltage on propagation delay. These general guidelines for adjusting the propagation delay vs. supply voltage are as follows:

LSTTL, TTL, STTL	+2% per .1VDC
CMOS	typically presented by vendor
ECL	+2% per .1VDC

4.3.4.3 Load Capacitance Effects

Increased load capacitance increases propagation delay. If vendor data sheets specify propagation delay based on a load capacitance which is lower than the calculated value, adjustments must be made.

The following are guidelines for estimating load capacitance.

1) Device Loading Capacitance:

LS, ALS, F Series	Minimum capacitance is typically 1.6 pF, maximum capacitance is typically 5 pF. For an input which serves more than 1 internal (unbuffered) function each additional function adds 2.3 pF maximum, 0.7 pF minimum
S Series	9.6 pF maximum, 3.2 pF minimum
CMOS	Internal functions - 6.9 pF typical, 2.3 pF minimum, 7.5 pF maximum

2) Output Capacitance of Tri-State Devices:

	ALS	F	LS	S	CMOS
Hi-Drive	15pF	12pF	12pF	12pF	15pF
Lo-Drive	10pF	5pF	12pF	12pF	15pF

3) Board Capacitance:

Board capacitance can be calculated from the equation for a line above a ground plane:

$$C_{TOT} = \frac{E_R}{CN}\left(\frac{5}{3} \times \frac{W}{H} + \frac{2.7}{\text{LOG}\frac{4H}{T}}\right)$$

where

C_{TOT} = board capacitance
W = trace width
T = trace thickness
H = distance from ground plane to trace
E_R = relative medium dielectric constant
C = speed of light = 1.1811×10^{10} inch/sec.
N = free space impedance + 377 ohms

For a typical 2-sided board, this yields a value of 2 pF per inch of interconnection trace.

4) Connector Capacitance:

Capacitance between pins on a printed circuit board connector have a typical value of 5 pF.

The effects of added capacitance from device loading, tri-state output capacitance, board capacitance, or connector capacitance on standard chip style propagation delays are as follows:

54LS	.08 Nsec./pF
54S	.06 Nsec./pF
54F (Standard)	.033 Nsec./pF
54F (Buffers)	.02 Nsec./pF
54ALS (Standard)	.046 Nsec./pF
54ALS (Buffers)	.023 Nsec./pF
CMOS	Use Vendor Data Book Curves

4.3.4.4 Line Delays

For critical timing paths, transmission line delays should be considered. A typical value for a 12 inch line with 6 TTL loads and a PCB with 100W transmission impedance is 2.9 nSec. Refer to VHSIC Technologies and Tradeoffs by Arpad Barna for additional information pertaining to transmission line propagation delay effects.

4.3.4.5 End-of-Life Derating

A typical derating factor for end-of-life is to increase the maximum propagation time by 5%.

4.3.4.6 CMOS Considerations

Due to slow rise times of CMOS circuits, the time spent for transition must be treated as a period of unknown device operation. This is the time between V_{IL} maximum (input low level maximum voltage) and V_{IH} minimum (input high level minimum voltage) as shown in Figure 6.

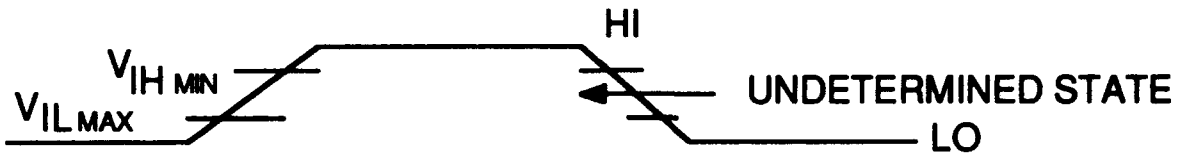


FIGURE 6: CMOS TRANSITION POINTS

The rise and fall times must be considered when calculating worst case propagation delays. Logic inputs must be stable during CMOS transition periods.

For clocking circuits, typical values for uncertainty times are:

Positive-edge clocking - uncertain from V_{IL} maximum to 45% of V_{DD} (Supply Voltage)

Negative-edge clocking - uncertain from V_{IH} minimum to 55% of V_{DD}

4.4 Linear IC's

Deriving worst case parameters on linear IC's is application dependent. Relative data can be obtained from vendor data sheets. Present day software packages allow for accurate modeling of most linear IC's. Depth of analysis may require various modeling approaches based on application. For instance, for an op amp used as a voltage follower, one may want to pay particular attention to the DC offset voltage and output current.

4.5 Applicable Documents

The following is a list of documents that provide insight into the derivation of component variation:

MIL-STD-198	Capacitors, Selection & Use Of
MIL-STD-199	Resistors, Selection & Use Of
MIL-STD-1346	Relays, Selection & Use Of
MIL-STD-1286	Transformers, Induction And Coils Selection & Use Of
MIL-STD-200	Electron Tubes, Selection & Use Of
MIL-STD-1132	Switches & Assoc. Hardware, Selection & Use Of

MIL-STD-701	Semiconductors, Selection & Use Of
MIL-T-39013	Transformers and Inductors, Audio and Power
MIL-T-39016	Transformers, Pulse, Low Power
MIL-T-27	Transformers and Inductors
MIL-T-21038	Transformers, Pulse
MIL-HDBK-175	Microelectronic Devices Data Handbook
MIL-HDBK-39000	Series Of Established Reliability Military Specifications

Copies of the above documents can be obtained from:

Department of the Navy
Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120

5.0 WORST CASE CIRCUIT ANALYSIS (WCCA) TECHNIQUES AND METHODS

This section describes worst case circuit analysis techniques and outlines a structure for performing a WCCA. There are essentially two analysis procedures required to complete a WCCA. The first is the part stress analysis where each component is examined at worst case extremes to verify that maximum ratings are not exceeded. The second analysis is a much more involved circuit performance analysis where transfer functions, digital timing, filter characteristics, etc. are investigated under worst case conditions.

The performance analysis can be approached using three techniques. These techniques include Extreme Value Analysis (EVA) and two statistical approaches - Root Sum Square (RSS) Analysis and Monte Carlo Analysis (MCA). Any of the above techniques can be completed efficiently with the use of a computer. The following paragraphs describe the analyses mentioned above and indicate characteristic data necessary for using computer simulation software to aid in the analysis.

5.1 Worst Case Part Stress Analysis

The purpose of a worst case part stress analysis is to examine each component in a circuit under worst case extremes to determine whether component ratings have or have not been exceeded. If the ratings have been exceeded, the part must be identified as overstressed. Overstress conditions can be induced by steady-state and transient conditions which adversely affect component operation.

The stress analysis is performed by simultaneously varying all components within the circuit such that the effect on a single component is the worst achievable state that it will experience. The parts and conditions which should be varied in the circuit include:

1) Component piece-part tolerances - worst case parameter value based on all factors affecting component variation (Refer to Section 4.1).

2) Supply voltages - takes into consideration both instantaneous and supply limits.

3) Load conditions - includes both steady-state and transient conditions.

4) Environmental factors - these include temperature extremes induced in a circuit. Also, various components may be affected by environmental factors such as humidity, altitude, exposure to the elements, etc. These factors must be evaluated for each component analyzed.

5) Transients and switching conditions - surges and on/off cycles.

6) The effects of radiation exposure.

These are the major variables affecting component worst case stress conditions. Other variables exist as well; the rule of thumb is that any parameter or condition which can degrade circuit performance should be examined under worst case conditions.

Once the component drift limits have been established, stress application boundaries may be determined. It should be noted that each component parameter is calculated independently. Conditions resulting in worst case stress application for one component may not be the worst case scenario for an identical component in a different application.

Calculated worst case stress values are usually placed in a tabular format comparing component to calculated stress values. By formatting the results in a table, the overstressed components may be readily identified. After completing the stress analysis, the circuit performance analysis may be conducted.

Each component type has associated parameters which exhibit sensitivity to stress conditions and contribute to overstressed component conditions. These parameters are generally defined by the part type and construction characteristics. Table 7 shows common component parameters calculated in a worst case stress analysis.

Some manufacturers specify a derating factor for components or groups of components in the circuit being analyzed. This derating factor is specified as a percentage of the maximum rated value. The life of a component is a function of the applied stress realized by that component. Derating adds to the life of the components and, consequently, to the life of the system. In the case where derating levels are required, calculated stress values are compared to the derated stress ratings as opposed to the maximum ratings. Furthermore, transient conditions may also require a derating factor under certain design constraints. Although components may not be overstressed with respect to the maximum ratings, values exceeding derating levels should be identified as overstressed. A good source for general derating guidelines is AFSC Pamphlet 800-27 "Part Derating Guidelines."

TABLE 7: TYPICAL COMPONENT FACTORS TO BE EVALUATED

TRANSISTORS

- Applied Voltage (Vce, Vbe)
- Base/Collector Current
- Power Dissipation
- Forward/Reverse Bias

MAGNETIC COMPONENTS

- Max Induction Levels (Saturation)/Losses
- Reset Conditions/Drive Imbalance
- Winding-to-Winding Voltages
- "Hot Spot" Temperature

INTEGRATED CIRCUITS (LINEAR/DIGITAL)

- Power Dissipation
- Applied Voltage (VCC)
- Common Mode Voltage
- Loading
- Fan-In/Fan-Out
- Differential Input Voltage
- Min/Max Input Voltage

Important guidelines which lead to the completion of a successful worst case stress analysis are as follows: First, develop a worksheet which contains fields for all required component parameters requiring stress calculations. Utilization of the worksheet ensures all relevant parameters have been evaluated. Second, create entries for all maximum and/or derated ratings based on components within the same functional groups; this is easier than following reference designators. Third,

analyze similar component types within the same functional group together, i.e., first analyze the resistors in one filter together, then the capacitors within the same filter, and so forth.

A special case occurs when pulsed power/current situations are present. Instantaneous peaks of current are of concern as well as the instantaneous temperature rise. The RMS values must be used in stress calculations - not the average values.

When dealing with pulsed power/current scenarios, the analyst is primarily concerned with current density and temperature rise. Temperature rise is a fur n of the total energy dissipated.

The following example demonstrates the difference between results using the RMS and averaging method.

Resistance = 10Ω
Applied Voltage = 5V, 1000 Hz, 50% Duty Cycle, Square Wave

The following calculations determine the average power dissipated in the resistor:

$$I_{AVG} = \frac{1}{2}\left[\frac{5V}{10\Omega}\right]$$
$$= .25A$$

$$P_{AVG} = I_{AVG}^2\, 10\Omega$$
$$= .625W$$

The total energy dissipated during each cycle is calculated by integrating the power over the time for one complete cycle. The energy calculation is as follows:

$$E_{TOTAL} = \int_0^{.001} P_{AVG}\, dt$$

$$E_{TOTAL} = \int_0^{.001} P_{RMS}\, dt$$

$$= P_{AVG} \bullet t \Big|_0^{.001}$$

$$E_{TOTAL} = .625mJ$$

Now it is necessary to calculate the power dissipated using the RMS method. The RMS voltage of a square wave is the voltage times the square root of the duty cycle.

$$V_{RMS} = 5\sqrt{.5}$$

$$= 3.5355$$

Thus:

$$P_{RMS} = \frac{V_{RMS}^2}{10\Omega}$$

$$= 1.25W$$

The total energy dissipated is determined in the same manner as for the average dissipation calculation.

$$E_{TOTAL} = \int_0^{.001} P_{RMS}\, dt$$

$$= P_{RMS} \bullet t \Big|_1^{.001}$$

$$E_{TOTAL} = 1.25\ mJ$$

As demonstrated the RMS calculation resulted in a power dissipation that is twice as great as the calculation using average values.

To prove that the calculation using RMS values is correct the energy dissipated is calculated as follows:

The instantaneous power dissipated is:

$$P_{INST} = \frac{V_{PEAK}^2}{10W}$$
$$= 2.5W$$

The power is actually dissipated during 50% of the 1000 Hz cycle. Therefore, the actual total energy dissipated occurs during half of one complete cycle. The actual energy calculation is as shown:

$$E_{ACTUAL} = \int_0^{.0005} P_{INST}\, dt$$

$$E_{ACTUAL} = P_{INST} \cdot t \Big|_0^{.0005}$$
$$= 1.25\ mJ$$

Therefore, the calculation using RMS values yielded the correct result. Thus, always use RMS values in dynamic situations (pulsed signals).

An example of a worst case stress analysis performed on a voltage comparator circuit follows. The example circuit can be found in Figure 7. The Piece-Part Stress Data Sheet for this example can be found in Figure 8.

First, some assumptions are made for this example:

1) All resistors are 0.25W max rated at 25°C, except R2 which is rated at 10W.
2) Ambient temperature is 25°C.
3) Worst case part derating required = 90% resulting in 0.25W x 0.9 = 0.225W derated capability (10W x 0.9 = 9W for R2).
4) No temperature derating is required (i.e., local part temperature is the same as the ambient temperature).

Note: For ambient temperatures above 25°C, place the vendor derated limit in column (5) and apply the program derating (column 6) to this number. The result is the allowable limit applicable to the specified temperature. The stress analysis is tied into the results of a thermal analysis as is the case for the worst case circuit analysis.

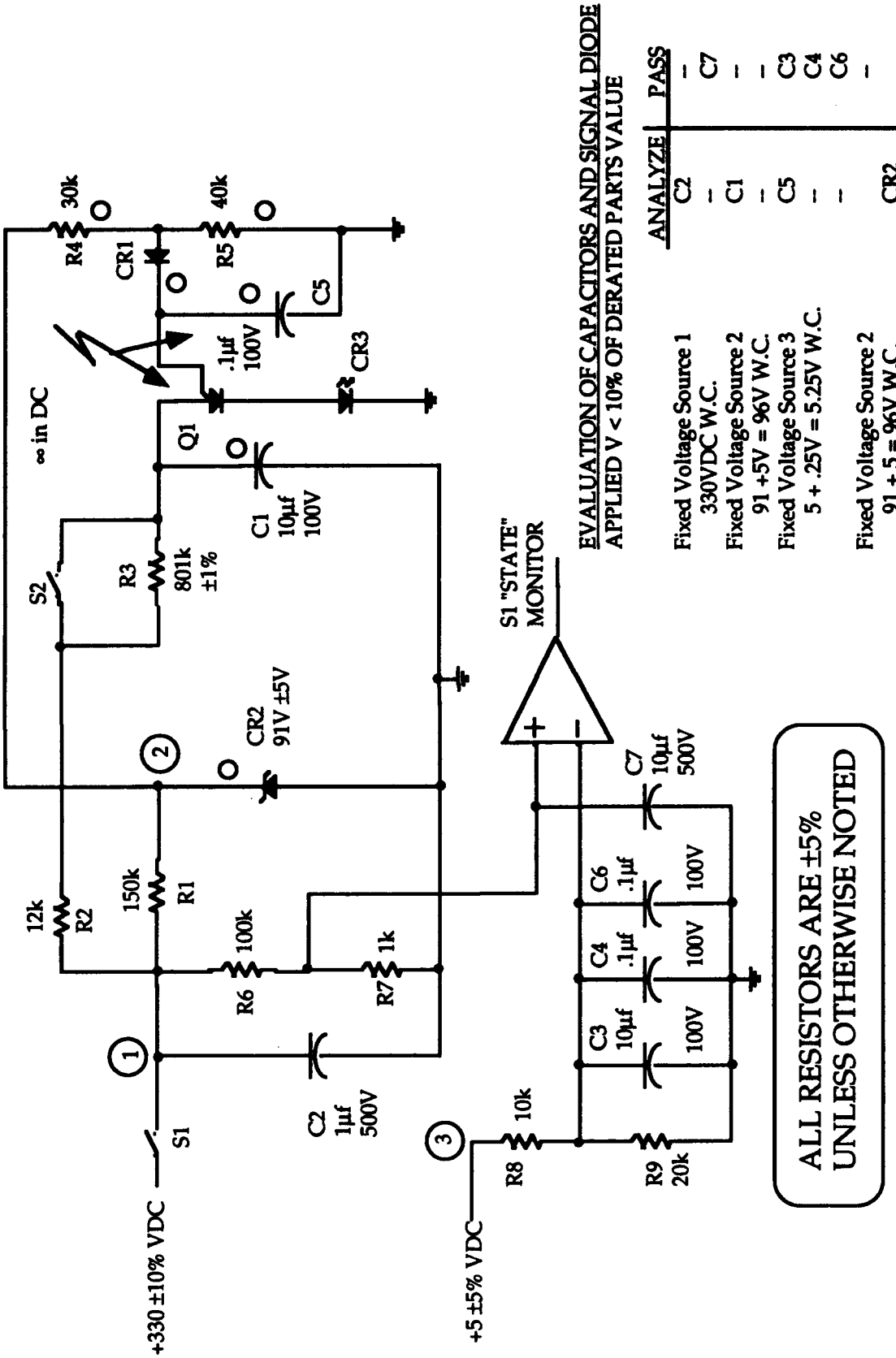


FIGURE 7: CIRCUIT FOR WC STRESS EXAMPLE

PIECE PART STRESS DATA SHEET

Customer _____ Schematic Dwg. # _____ Date _____

System _____ Parts List # _____ Analyst _____

Sub-system _____ Environment _____ Checked _____

Ambient Temperature _____ Page _____ of _____

(1) ITEM	(2) DESIGNATOR	(3) PART NUMBER	(4) DESCRIPTION (Value, Tolerance)	(5) VENDOR RATING AT 25°C %	(6) ALLOWABLE LIMIT AT TEMP %	(7) PROGRAM DERATINGS V	(8) MAXIMUM APPLIED VOLTAGE MA	(9) MAXIMUM APPLIED CURRENT %	(10) DUTY CYCLE mS	(11) PULSE WIDTH A, W	(12) PULSE LIMIT W	(13) ACTUAL POWER %	(14) % OF DERATING %	(15) % OF VENDOR RATING	(16) NOTES
	R1	RCR 150K	Res. 150K, 5%	.25W	90	.225W						.418	167	185.7	overstress
	R2	RNR 12K	Res. 12K, ±1%	10.0W	90	9.0W						9.39	104.3	93.9	overstress
	R3	RNR 801K	Res. 801K, ±1%	.25W	90	.225 W	≤ 96						<10	<10	
	R4	RCR 30K	Res. 30K, 5%	.25W	90	.225W						0.0601	26.7	24.0	
	R5	RCR 40K	Res. 40K, 5%	.25W	90	.225W						0.0792	35.2	31.7	
	R6	RCR 100K	Res. 100K, 5%	.25W	90	.225W						1.124	499.5	449.6	overstress
	R7	RCR 1K	Res. 1K, 5%	.25W	90	.225W						0.0124	<10	<10	
	R8	RCR 10K	Res. 10K, 5%	.25W	90	.225W	<5.25V						<10	<10	
	R9	RCR 20K	Res. 20K, 5%	.25W	90	.225W	≤5.25V						<10	<10	
	Q1	2N6136	Thyristor	5A	90	4.5A		0.0033					<10	<10	
	C1	CZ -	Cap. 10µf, 100V	100V	90	90V	4.0V						<10	<10	
	C2	Not on P/L	Cap. 1µf, 500V	550V	90	450V	330V						73.3	66.0	ck in rush current
	C3	CZ -	Cap. 10µf, 100V	100V	90	90V	5.25V						<10	<10	
	C4	CKR/02	Cap. .1µf, 100V	100V	90	90V	5.25V						<10	<10	
	C5	CKR/02	Cap. .1µf, 100V	100V	90	90V	56.5V						62.7	56.5	
	C6	CKR/02	Cap. .1µf, 100V	100V	90	90V	5.25V						<10	<10	
	C7	Not on P/L	Cap. 10µf, 500V	500V	90	450V	3.61V						<10	<10	
	CR1	1N4858	Diode	100V	90	90V	0V						<10	<10	
	"	"		.2a	90	.18a		0.0030					<10	<10	
	CR2	1N9848	Zener Diode	.4w	90	.36W						.158	43.8	39.5	
	CR3		LED	0.049a	90	0.0369							79.7	71.7	

FIGURE 8: PART STRESS DATA SHEET

Calculate C5 maximum voltage:

$$V_{C5max} = \left(\frac{R5max}{R4min + R5max}\right)(V_{CR2max}) - V_{F(CR1)}$$

$$= \left(\frac{42K\Omega}{28.5K\Omega + 42K\Omega}\right)(96V) - .7V$$

$$= 56.49V$$

Calculate C1 maximum voltage:

$$V_{C1max} = V_{CR3max} + Q_1 \text{ Cathode - Anode (Maximum)}$$

$$= 2.2V + 1.8V$$ where these values are worst case at the operating point

Calculate P_{CR2} Worst Case:

Assume all current through CR2. The power is calculated by:

$$P_{CR2\ w.c.} = \left(\frac{V_{1\ max} - V_{2max}}{R_{1min}}\right)(V_{2\ max})$$

$$= \left(\frac{363V - 96V}{142.5KW}\right)(96V)$$

$$= .180W$$

Calculate C2 Maximum Voltage:

Device C2 maximum voltage is by inspection

$$V_{C2max} = V_{1max} = 330V$$

Calculate P_{R1} Worst Case:

$$P_{R1\ w.c.} = \frac{(V1_{max} - V_{2\ min})^2}{R1_{min}}$$

$$= \frac{(363V - 86V)^2}{142.5KW}$$

$$= .538W$$

R1 is overstressed under worst case conditions.

Calculate P(R6) Worst Case:

Maximum power dissipation occurs with maximum current in R6.

$$P_{R6} = \left[\frac{V_{1max}}{R6_{min} + R7_{min}}\right]^2 \bullet R6_{min}$$

$$P_{R6\ w.c.} = \left[\frac{363V}{95000W + 950W}\right]^2 \bullet 95000W$$

$$P_{R6\ w.c.} = 1.124\ Watts$$

Calculate P(R7) Worst Case:

Maximum power dissipation occurs with maximum voltage across R7.

$$P_{R7} = \left[\frac{V1_{max}}{R6_{min} + R7_{max}}\right]^2 \bullet R7_{max}$$

$$P_{R7\ w.c.} = \left[\frac{363V}{95000W + 1050W}\right]^2 \bullet 1050W$$

$$P_{R7\ w.c.} = .0149\ Watts$$

Calculate V_{C7} Worst Case:

The voltage across C7 is the same as that across R7:

$$V_{C7} = \frac{R7}{R6 + R7} V1$$

$$V_{C7} = \frac{1}{1 + \frac{R_{6min}}{R_{7max}}} V1_{max}$$

$$V_{C7\ w.c.} = \frac{1}{1 + \frac{95000W}{1050W}} 363V$$

$$V_{C7\ w.c.} = 3.968V$$

Calculate P(R2) Worst Case:

Assume that switch S2 is closed and that $V_{Q1min} = 1.2V$ and $VF_{CR3min} = 1.6V$.

$$P_{R2} = \frac{(V_{1max} - V_{Q1min} - V_{CR3min})^2}{R_{2min}}$$

$$P_{R2\ w.c.} = \frac{(363V - 1.2V - 1.6V)^2}{11400\Omega}$$

$$P_{R2\ w.c.} = 11.38W$$

R2 is overstressed under worst case conditions.

Calculate I(CR3) Worst Case:

$$I_{CR3max} = \frac{V_{max} - V_{Q1min} - V_{CR3min}}{R2_{min}}$$

$$I_{CR3max} = \frac{363 - 1.2 - 1.6}{11400}$$

$$I_{CR3max} = .0316A$$

Calculate P(R4) Worst Case:

The power dissipation in R4 is comprised of steady state and pulsed components. The pulsed power is due to the presence of C5. The pulsed portion will be assumed negligible due to the circuit time constant and the fact that it is a non-repetitive pulse.

If this were not the case, the pulse power would have to be calculated and this result would be evaluated relative to the resistor's pulse power capability. The average power is then calculated (including the pulse portion) and compared to the steady state capability of the resistor.

$$P_{R4\ w.c.} = \left[\frac{V_{CR2max}}{R4_{max} + R5_{min}}\right] R4_{max}$$

$$P_{R4\ w.c.} = \left[\frac{96V}{31500\Omega + 38000\Omega}\right]^2 31500\Omega$$

$$P_{R4\ w.c.} = 0.060101W$$

Calculate P(R5) Worst Case:

The equation for R5 dissipation is:

$$P_{R5\ w.c.} = \left[\frac{V_{CR2max}}{R_{4min} + R_{5min}}\right]^2 . R5min$$

$$P_{R5\ w.c.} = \left[\frac{96V}{28500\Omega + 38000\Omega}\right]^2 38000\Omega$$

$$P_{R5\ w.c.} = 0.079192W$$

$$I_{CR1} = \frac{V2_{max} - VF\ (CR1)}{R4_{min}}$$

use the minimum forward voltage at the appropriate analysis temperature.

$$I_{CR1} = \frac{96V - 0.75V}{28500\Omega}$$

$$I_{CR1} = 0.003342A$$

Calculate VR(CR1) Worst Case:

By inspection, CR1 reverse voltage will be 0 volts.

5.2 Worst Case Circuit Performance Analysis

Worst case circuit performance analysis uses worst case values and techniques to determine whether a circuit will perform the required functions under extreme operating and environmental conditions. Since component parameters are affected by worst case extremes, the functionality of the circuit will be affected as well.

In worst case performance, the experience of the analyst plays a key role in determining which factors are critical. Schedule and cost constraints may dictate the intensity of the analysis. In many instances, it may be necessary to limit the analysis to key functions or sections of the circuit.

5.2.1 Circuit Performance Parameters To Be Examined

When conducting a worst case circuit performance analysis, the key elements examined within the system depend on the functionality of the circuit. Critical timing of digital circuits, transfer functions of filtering networks, and characteristics of amplifiers are examples of circuit performance elements.

When verifying the performance of digital circuits under worst case conditions, the following aspects should be examined: The logic of a digital circuit must be verified. Truth tables, state tables, Karnaugh maps, and timing diagrams provide a means for examining the logic of each functional block. Unwanted floating states and logical lock-up must not occur under extreme conditions. The board must be decoupled by a minimum number of capacitors to inhibit self-induced logic switching. The state of the circuit must be verified on power-up and reset, especially on processor controlled circuits.

Another function which must be evaluated is circuit timing. A timing analysis examines the effects of worst case propagation delay (maximum and minimum) to determine whether data control lines are active during the correct time of the cycle. Board and load capacitance can also influence the timing of digital circuitry and must therefore be investigated. The read/write and access cycles for memory circuit timing must take worst case propagation delay into account. Data to and from these ICs has to be present when the ICs are enabled.

Many ICs require signal inputs of specified pulse width set-up and hold time - especially those with clock inputs. Also, timing characteristics change due to radiation effects or transients depending on the conditions imposed upon the circuit. Typically, a worst case timing diagram is created for the functional group under analysis. This diagram shows all worst case component characteristics.

Digital performance analysis also examines the current draw of ICs to determine whether fanout limits exceed maximum specifications or derating requirements for each IC. The state with the lowest fanout capacity is used as the worst case fanout. Along these lines, the analyst must review the load requirements of all the digital ICs relative to the output of the supply. As a guideline, a 10% buffer should be observed between required power and actual power supply output as a minimum.

Finally, compatibilities between logic families (TTL, CMOS, etc.) may have been overlooked when the circuit was designed. Timing, logic thresholds, and fanout incompatibilities may exist but not be readily apparent. Many digital families are only partially compatible with other logic types resulting in performance problems when used together.

Analog circuits have various functions and therefore require different analytical approaches. For example, consider an oscillator circuit. Component drift may cause frequency and phase instability. Noise can cause timing anomalies. Table 8 contains most forms of analog circuits and the parameters which should be analyzed in a worst case performance analysis.

5.2.2 Circuit Sensitivity And Monotonicity

Circuit sensitivity is a measure of how a circuit will react to an incremental change in a single component parameter when all other parameters are held constant. Sensitivity is measured by magnitude and sign (direction). If a parameter change directly affects circuit function then the sensitivity has a positive directionality. If the parameter change inversely affects circuit function, the sensitivity has a negative directionality.

Sensitivity determines the worst case minimum and maximum values for a circuit response. The sensitivity can be expressed in terms of the calculated variation of all the simultaneous piece part values. To identify circuit sensitivity the directionality (+/-) of a circuit attribute must be known. Then, the worst case maximum value is found by setting all proportional parameters to their maximum values and all inversely proportional values to their minimum values. Conversely, the worst case minimum values are calculated by setting all directly proportional parameters to their minimum values and the inversely proportional parameters to their maximum values.

A very important aspect of sensitivity that needs discussion is monotonicity. A non-monotonic function results in a sensitivity sign change over the range of the parameter variable. By default, a monotonic function's sensitivity does not undergo a sign change when parameters are moved from a nominal to extreme value. Figure 9 shows a simplified drawing of a monotonic and non-monotonic function.

TABLE 8: ANALOG CIRCUIT PARAMETERS

1) Comparator Parameters A. Threshold Precision B. Switching Speed/Time Constant C. Hysteresis D. Offset Stability	6) Oscillator Parameters A. Frequency Stability, Accuracy, Setability B. Output Power Level, Stability C. Self-Starting D. Noise and Spurious Output E. Phase Stability F. Output Impedance and Load Impedance (Mag. & Phase)
2) Filter Parameters A. Insertion Loss B. Frequency Response, Bandwidth C. Input/Output Impedance D. VSWR, I/O - In Band And Out Of Band E. Phase Response - Propagation Delay F. Linearity G. Spurious or Out-of-Band Feed-Through	7) Detector Parameters A. Bias Voltage B. Frequency Range C. Input & Output Impedance D. VSWR - Input
3) Modulator Parameters A. Frequency Response B. Input/Output Impedance C. Insertion Loss D. Deviation E. Phase Response & Linearity F. Output Level G. VSWR	8) RF Switch (Solid State/Mechanical) Parameters A. Drive Requirements B. Power Dissipation C. Power Handling Capability D. Switching Speed tR, tF E. VSWR F. Insertion Loss G. Frequency Response H. Video Feed Through I. Switch Cycles - Duty Cycle J. I/O Impedance (Mag. & Phase)
4) Multiplier Parameters A. Input/Output Impedance B. Input Drive C. Output Power D. Frequency Response	9) Coupler, Circulator Parameters A. Insertion Loss B. Frequency Response C. Power Handling Capability D. Directivity E. Magnetic Leakage F. VSWR G. Input/Output Impedance (Mag. & Phase)
5) Mixer (Converter) Parameters A. Noise Figure B. Frequency C. Drive Requirements D. Compression Points E. Intercept Points F. Group Delay G. Power Dissipation H. Output Spectrum I. Conversion Loss J. Terminating Impedance (Mag. & Phase)	10) Stripline, Waveguide, Cavity Parameters A. Mode Suppression B. Insertion Loss C. Dimensional Stability, Aging & Environments D. Special Processes, Plating, Machining E. Adjustment Range, Resolution Stability F. Input/Output Impedance G. VSWR H. Material Stability (Stripline), Peel Strength Of Conductors

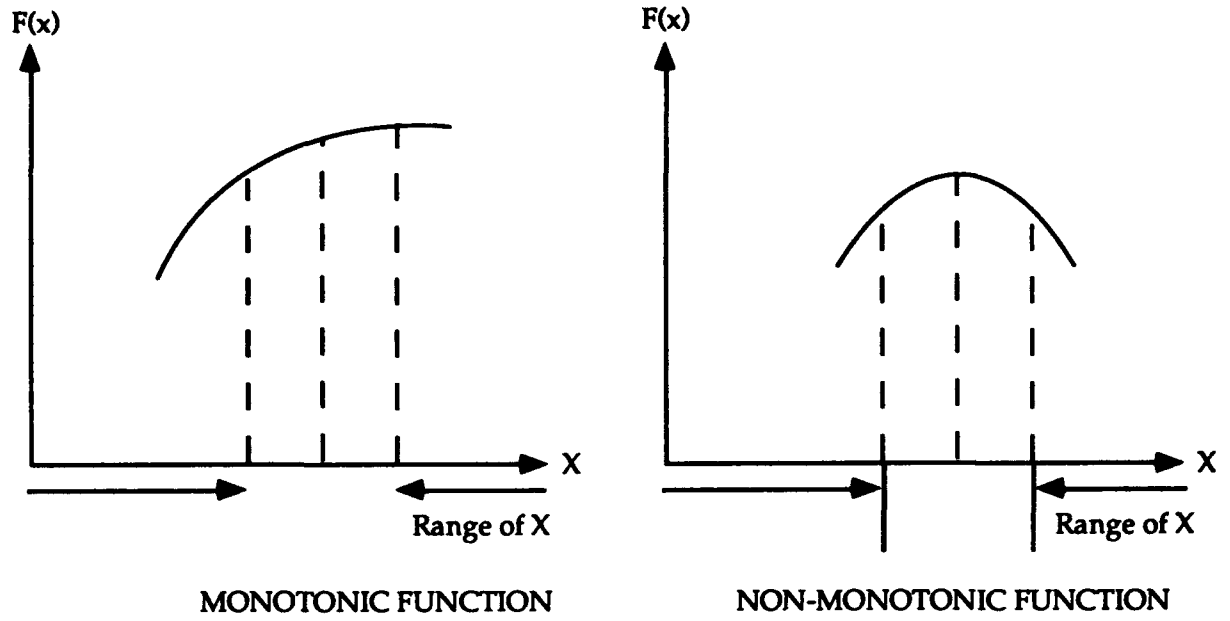


FIGURE 9: MONOTONIC AND NON-MONOTONIC FUNCTIONS

If the analyst is using a circuit simulator which has a worst case analysis feature, the analyst must exercise caution. Most circuit simulators are not capable of determining a circuit's monotoncity with respect to piece part values; therefore they could generate erroneous worst case results.

The problem with non-monotonic functions is that the worst case performance limits are not necessarily found by the procedure given above. In this case, an iterative procedure must be used which examines a function much more closely until the worst case performance limits are determined.

5.2.3 Numerical Analysis Techniques

Worst case analysis can be performed using three different approaches: Extreme Value Analysis (EVA), Root-Sum-Square (RSS) Analysis, and Monte Carlo Analysis. Each method will be examined and its advantages and disadvantages will be discussed.

Table 9 is a cross reference guideline that can be used to assist in deciding on an appropriate analysis method.

TABLE 9: ANALYSIS METHOD CROSS REFERENCE

	Advantages	Disadvantages
EVA	• Permits most readily obtainable estimate of worst case performance. • Does not require statistical inputs for circuit parameters. • Data base need only supply part parameter variation extremes.	• Results in pessimistic estimate of circuit worst case performance. • If circuit fails, there is insufficient data to assess risk.
RSS	• Results in more realistic estimate of worst case performance than EVA. • Knowledge of parameter PDF not required. • Provides some degree of risk assessment in terms of percentage of units to pass or fail.	• Standard deviation of piece part parameter probability distribution is required. • Assumes circuit sensitivities remain constant over range of parameter variability. • Uses approximation: circuit performance variability is normally distributed (central limit theorem).
Monte Carlo	• Provides the most realistic estimate of true worst case performance of the three methods. • Provides additional information which can be applied to risk assessment.	• Requires the use of a computer. • Consumes large amount of CPU time. • Requires accurate knowledge of piece part parameter PDF. • Requires significant parts procurement controls (such as source and specification control drawings) to insure long-term validity of results.

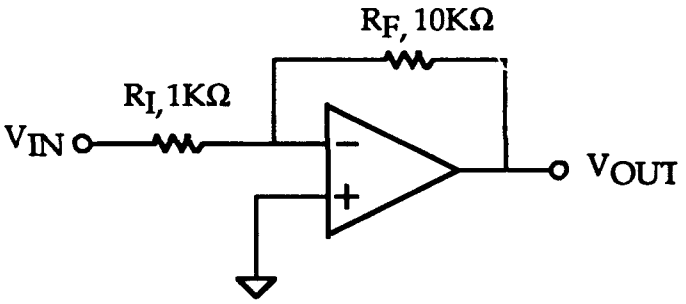
5.2.3.1 Extreme Value Analysis

The EVA technique is considered the best initial approach to worst case circuit analysis; if the circuit passes EVA, it will always function properly. If the circuit fails, modify the circuit until it meets the EVA requirements or apply Root-Sum-Square or Monte Carlo Analysis for a less conservative approach. EVA uses the limits of variability and the circuit directional sensitivities to determine the worst case results.

EVA is the most conservative approach of the three techniques. Although possible, the chances of all piece-part parameter swings being at their extreme values simultaneously is highly improbable. However, for circuits used in medical, safety, or life-threatening situations, EVA allows the designer to be highly confident that the circuit will function as required.

The Extreme Value Analysis (EVA) is by far the easiest of the numerical analysis techniques to apply. EVA simultaneously implements the worst case extremes of all components for the circuit parameter under evaluation. Once the circuit extremes have been applied, the component parameter is evaluated using standard circuit analysis techniques. The conclusions of the analysis are then compared to expected results.

The following is a short example of an EVA:



Resistors are ± 5% Worst Case

$$\frac{V_{IN}}{V_{OUT}} = \frac{-R_F}{R_I}$$

$$\text{Extreme Worst Case Minimum Gain} = \frac{9.5K\Omega}{1.05K\Omega}$$

$$= 9.05$$

$$\text{Extreme Worst Case Maximum Gain} = \frac{10.5K\Omega}{950\Omega}$$

$$= 11.05$$

5.2.3.2 Root-Sum-Squared (RSS)

The Root-Sum-Squared (RSS) approach to worst case circuit analysis provides a more realistic evaluation technique by employing a statistical approach. A RSS analysis provides a probability that manufactured circuits will work within specification (the manufacturing yield). The results are in the form of parameter bias and standard deviation, so that the three-sigma limits of performance can be determined.

The method is based on the central limit theorem which states that if a large number of independent variables are statistically combined, the resulting distribution is a normal distribution independent of the form of the distributions of the combined variables. RSS combines the standard deviation of each piece-part tolerance based on the sensitivity produced in a circuit due to that piece-part.

The RSS approach assumes that all variables have normal distributions. RSS results are most commonly evaluated from a manufacturing perspective. The analysis allows the manufacturer to statistically estimate the quantity of "bad" circuits produced.

The following is an example of the RSS approach for a two-stage amplifier:

The function for the amplifier is given as, A, where:

$$A = \frac{R4}{R3}\left(1 + \frac{R2}{R1}\right)$$

$$A = A_{nom} \pm \Delta A$$

ΔA = Deviation from nominal (3σ limit)

$$\Delta A_{limits} = \pm 3\sigma \text{ of } A$$

The specification states that $97 \leq A \leq 103$.

Using RSS techniques:

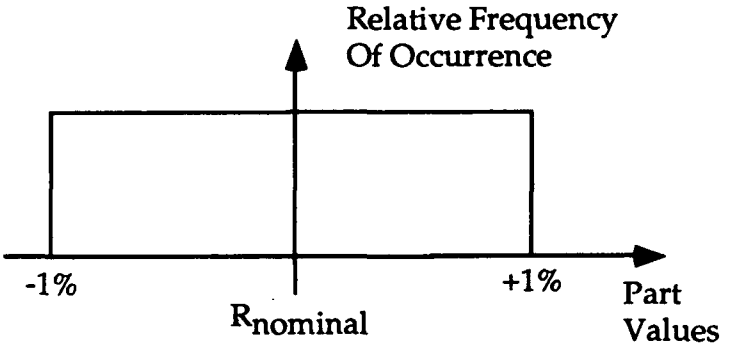
$$\sigma A = \sqrt{\left(\frac{\partial A}{\partial R1}\,\sigma R1\right)^2 + \left(\frac{\partial A}{\partial R2}\,\sigma R2\right)^2 + \left(\frac{\partial A}{\partial R3}\,\sigma R3\right)^2 + \left(\frac{\partial A}{\partial R4}\,\sigma R4\right)^2}$$

The resistor values are:

R1 = 1KΩ R3 = 1KΩ
R2 = 10KΩ R4 = 9.09KΩ

The resistor tolerances are known to be uniformly distributed.

(Maximum values = ±1%)



For a uniform distribution, the standard deviation is equal to the maximum limit divided by $\sqrt{3}$.

$$\sigma_R = \frac{1\%}{\sqrt{3}} = 0.577\%$$

Sample Problem Solution:

To calculate the standard deviation of A the analyst must first calculate the standard deviation of the components. For R1 the calculation is as follows:

$$\sigma R1 = 1K\Omega \bullet 0.577\%$$
$$= 5.77\Omega$$

The standard deviation for the other components is calculated in the same fashion. Next the analyst, needs to determine the sensitivity for each component. The sensitivity calculation for R1 is as follows:

Since,

$$A = \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)$$

$$\frac{\partial A}{\partial R_1} = \frac{-R_2 R_4}{R_3 R_1^2}$$

$$= -0.0909/\text{Ohm}$$

Sensitivity calculations for the other components are similar, but the partial derivative will be different for each component. The following tables summarize the results of the calculations.

SENSITIVITY

R_1	-0.0909/Ω
R_2	0.00909/Ω
R_3	-0.1/Ω
R_4	0.011/Ω

COMPONENT STANDARD DEVIATION

R_1	5.77Ω
R_2	57.7Ω
R_3	5.77Ω
R_4	52.45Ω

Therefore, the standard deviation for A can be found by the following equation:

$$\sigma_A = \sqrt{\sum_{i=1}^{4}\left(\frac{\partial A}{\partial R_i} s_i\right)^2}$$

$$= \underline{\underline{1.103}}$$

RSS results:

$\sigma_A = 1.103$

If the 3σ limits (99.7%) are the worst-case criteria:

$A_{max} = 100 + 3\,(1.103) = \mathbf{103.3}$

$A_{min} = 100 - 3\,(1.103) = \mathbf{96.7}$

Comparing to the spec. limits:

Upper tolerance limit = **103**

Lower tolerance limit = **97**

The resulting distribution of A is as follows:

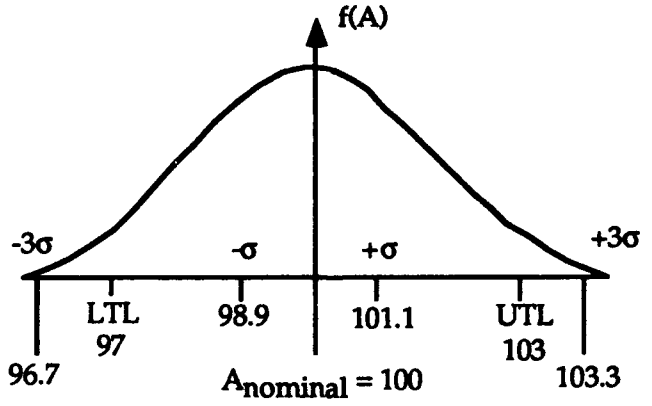


FIGURE 10: PROBABILITY DENSITY OF GAIN

$Z = \frac{(103 - 100)}{1.103} = 2.72\sigma$. Therefore, 99.3% of the circuits fall within the specified limits.

5.2.3.3 Monte Carlo Analysis (MCA)

The last approach to worst case circuit analysis to be discussed is Monte Carlo Analysis (MCA). The MCA technique uses actual part tolerance distributions, if available. If these distributions can be utilized, then this approach is the most realistic of the three. Otherwise, a distribution must be assumed and this method will be no more accurate than the RSS method.

The results of the MCA are typically displayed using a histogram for the circuit parameter under analysis. As in the RSS method, the probability of "good" circuits manufactured based on statistics is estimated. The major disadvantage of this technique is that hundreds of iterative calculations must be made in order to achieve statistically significant results, making it necessary to utilize a computer to perform the Monte Carlo Analysis.

Figure 11 shows a MCA program, while Table 10 gives the results of an MCA for the two-stage amplifier example presented in Section 5.2.3.2.

TABLE 10: RESULTS OF MCA

NO. OF SIMULATIONS	MEAN	STD. DEV.
500	100.021	1.081
1000	99.962	1.082
1500	99.976	1.102
2000	99.977	1.102
2500	99.971	1.104
3000	99.979	1.102
3500	99.990	1.101
4000	99.993	1.099
4500	99.998	1.105
5000	100.007	1.102

The above results can be used to calculate, using standard statistical approaches, the percentage of circuits within specification limits.

```
REM        ***** MONTE CARLO ANALYSIS OF AMPLIFIER *****
REM                          ****** PRINT HEADINGS ******
LPRINT: LPRINT: LPRINT TAB(25) "AMPLIFIER M.C. ANALYSIS"
LPRINT TAB(25) "-----------------------": LPRINT: LPRINT: LPRINT
LPRINT TAB(20) "  NO. ", "MEAN ", "STD. DEV."
LPRINT TAB(20) "  ----",  -------", " ------------": LPRINT
A$="####.###       ####.###"

REM          ******CHOOSE RANDOM VALUES FOR RESISTORS*****
DIM R1(5000),R2(5000),R3(5000),R4(5000),A(5000)
R1=1000:  R2=10000:  R3=1000:  R4=9090
RANDOMIZE TIMER:  FOR I=1 TO 5000:  R1(I)= R1*(.99+.02*RND): NEXT I
RANDOMIZE TIMER:  FOR I=1 TO 5000:  R2(I)= R1*(.99+.02*RND): NEXT I
RANDOMIZE TIMER:  FOR I=1 TO 5000:  R3(I)= R1*(.99+.02*RND): NEXT I
RANDOMIZE TIMER:  FOR I=1 TO 5000:  R4(I)= R1*(.99+.02*RND): NEXT I

REM          ****** CALCULATE GAIN, MEAN, STD. DEV. ******
ASUM=0:  AMAX = 0:  AMIN = 1000
FOR I=1 TO 5000
    A(I) = R4(I)/R3(I)*(1+R2(I)/R1(I)):  ASUM=ASUM+A(I)
    IF A(I) > AMAX THEN AMAX = A(I)
    IF A(I) < AMIN THEN AMIN = A(I)
    IF I MOD 500 = 0 THEN
      MEAN = ASUM/I: A2SUM=0
      FOR J=1 TO I:  A2SUM = A2SUM+(A(J)-MEAN)^2:  NEXT J
      SD = SQR(A2SUM/I)
      LPRINT TAB(20) I,;: LPRINT USING A$; MEAN, SD
    ELSE
    END IF
NEXT I
LPRINT:  LPRINT:  LPRINT
LPRINT TAB(25) "MIN GAIN     MAX GAIN"
LPRINT TAB(25) "----------      ----------": LPRINT
LPRINT TAB(16) "LIMITS  ";:   LPRINT USING A$; AMIN,AMAX

REM ****** CALCULATE 99.7% POINTS ******
CT=0:  A1=AMIN:  A2=AMAX
FOR J=1 TO 200
    A1=A1 + .005:  A2=A2-.005:  CT=0
    FOR I = 1 TO 5000
      IF A(I) > A2 THEN CT=CT+1
      IF A(I) < A1 THEN CT=CT+1
      IF CT>7.5 THEN J=200:  I=5000
    NEXT I
NEXT J
A1 = A1-.005:  A2=A2+.005
LPRINT:  LPRINT TAB(16)  "99.7% ";:  LPRINT USING A$;  A1,A2

REM ****** CALCULATE % PASS ******
CT=0
FOR I=1 TO 5000
IF A(I) >=97 THEN IF A(I) <=103 CT=CT+1
NEXT I:  PASS = 100*CT/5000
LPRINT:  LPRINT:  LPRINT
LPRINT TAB(26)  "% PASS = ";:  LPRINT USING "###.##"; PASS
END
```

FIGURE 11: MCA PROGRAM

5.2.4 Computer Aided Tools

Circuit simulation using computers remains an integral part of circuit design and analysis techniques, particularly as the speed and accuracy of simulators and hardware continue to improve. These improvements come not only from smaller, faster machines, but also from more accurate simulator subroutines.

The principal advantage to using computer simulation techniques is that they allow the characteristics of complex circuits having many components and nodes to be computed accurately and in a relatively short time, as compared to manual techniques. With the evolution of desktop personal computing capabilities these tools can be effectively utilized by every engineer.

A circuit simulator is one part of an integrated computer aided design/computer aided engineering (CAD/CAE) environment. Schematic capture programs allow the generation of required input files from circuit drawings in order to provide the appropriate input for the simulator. The same schematic capture program can typically interface with and run Printed Circuit Board (PCB) layout programs, and PCB generating equipment on the manufacturing end.

Many of the available circuit simulator packages are universally accepted in industry. The SPICE family of simulators, for example, are similar regardless of computing platform or software package. Schematic netlists (circuit model), component models, analysis routines, and options are entered into the simulator in a text file (or a group of smaller text files) which is "compiled by" or run through the simulator. A text file is created at the end of the run, which contains the analysis results. Some of these simulators also create data files for post-processing tools to create high quality graphs.

Most simulators allow the adjustment of detailed component parameters. The better simulators allow manufacturer databook information to be used in the circuit model. For worst case purposes, these parameters can have the necessary tolerances added to them when analyzing the circuit. Many component manufacturers provide libraries for use in circuit analysis packages. These libraries are based on the manufacturer's databook information for the listed components. Extremely

accurate and realistic circuits can be constructed on the simulator using these libraries in lieu of generic component parameters.

Most packages provide detailed, graphical outputs for characteristic and analysis plots. Many of these post-processing graphics tools allow the user to examine the analysis results in a variety of different output formats. Currents, voltages, and mathematical combinations of the two can be quickly and accurately plotted. Typically the post-process graphical tools allow oscilloscope like output, with cursor traces and axis range adjustments. Axis range adjustments allow the user to magnify points of interest.

There are also many mathematical modeling software packages available to the analyst. These packages can typically be used to solve both differential and integral calculations. Differential and integral formulas are fundamental to circuit analysis. Therefore, math packages are useful analysis tools using either numerical or symbolic techniques. If the response function of a circuit is desired than a symbolic solution would be appropriate. If an exact result is required, then the analyst would utilize a numerical solution.

Another useful automated tool is the database management system (DBMS). There are many DBMS software packages available. A DBMS allows the user to store common data items together in templates called records. The records themselves are constructed from individual pieces of related information called fields. The component database created for the worst case part stress analysis can be built with one of these automated DBMS systems.

Each part to be analyzed is stored as a separate record within the database structure. Each field contains parametric data about the given part. For example, the first field could contain the part number, the next the reference designator, followed by a brief description, initial tolerances, aging tolerances, nominal value, and so on. Once the information is input to the database, software routines can be written to do the calculations of worst case final tolerances, lower values, and upper values. Once all values are calculated, the analyst can arrange the data into any output format desired in the WCCA report.

The final computer analysis method to be discussed involves the use of a high-level programming language in which the analyst programs his/her own techniques. The computerized routines are the same electrical equations which have been developed by hand, yet are complicated enough to make the use of a computer necessary to reduce the time required to complete an analysis. This technique can be used to solve any linear, non-linear, or time variant circuit. If the analyst can write an equation to describe the given circuit, no matter how complicated, then this method can be used.

With this method of automated WCCA, numerical analysis techniques are used to solve integral or differential equations. The equations can contain as many parameters and variables as are necessary to compute the required results. However, this method assumes that the analyst has a good working knowledge of the circuit being analyzed and a high-level programming language, such as Fortran or C. As with commercially available simulators, the analysis results will only be as accurate as the models used.

6.0 WORST CASE CIRCUIT ANALYSIS (WCCA) EXAMPLES

To reinforce the techniques described in the previous sections, digital and analog circuit examples have been included to demonstrate various analysis techniques. These examples are not comprehensive. Instead, they are intended to demonstrate the techniques and methodology behind a worst case circuit analysis.

The first circuit is a digital circuit example which involves the timing analysis of a clock generator circuit which is used as an input to an alphanumeric display. This example employs the Extreme Value Analysis (EVA) approach to analyze the circuit.

The second circuit is an analog 10 KHz band-pass filter. In this example, the worst case deviation of the center frequency of the filter will be analyzed. This example demonstrates both the EVA and Root-Sum-Squared (RSS) analysis methods.

6.1 Digital Circuit Example

The first example is the clock generator circuit. Figure 12 is a schematic representation of the circuit.

6.1.1 General Circuit Description

It is beneficial to include a functional description of the circuit/system. By doing so, individuals that are not familiar with the circuit/system are given a brief overview of the circuit/system function. In this case, the circuit is relatively small so the functional description is actually a general circuit description. The following highlights provide a general circuit/functional description for the Clock Generator Circuit:

- The clock generator provides timing signals for a multiplexed 16-character alphanumeric display.

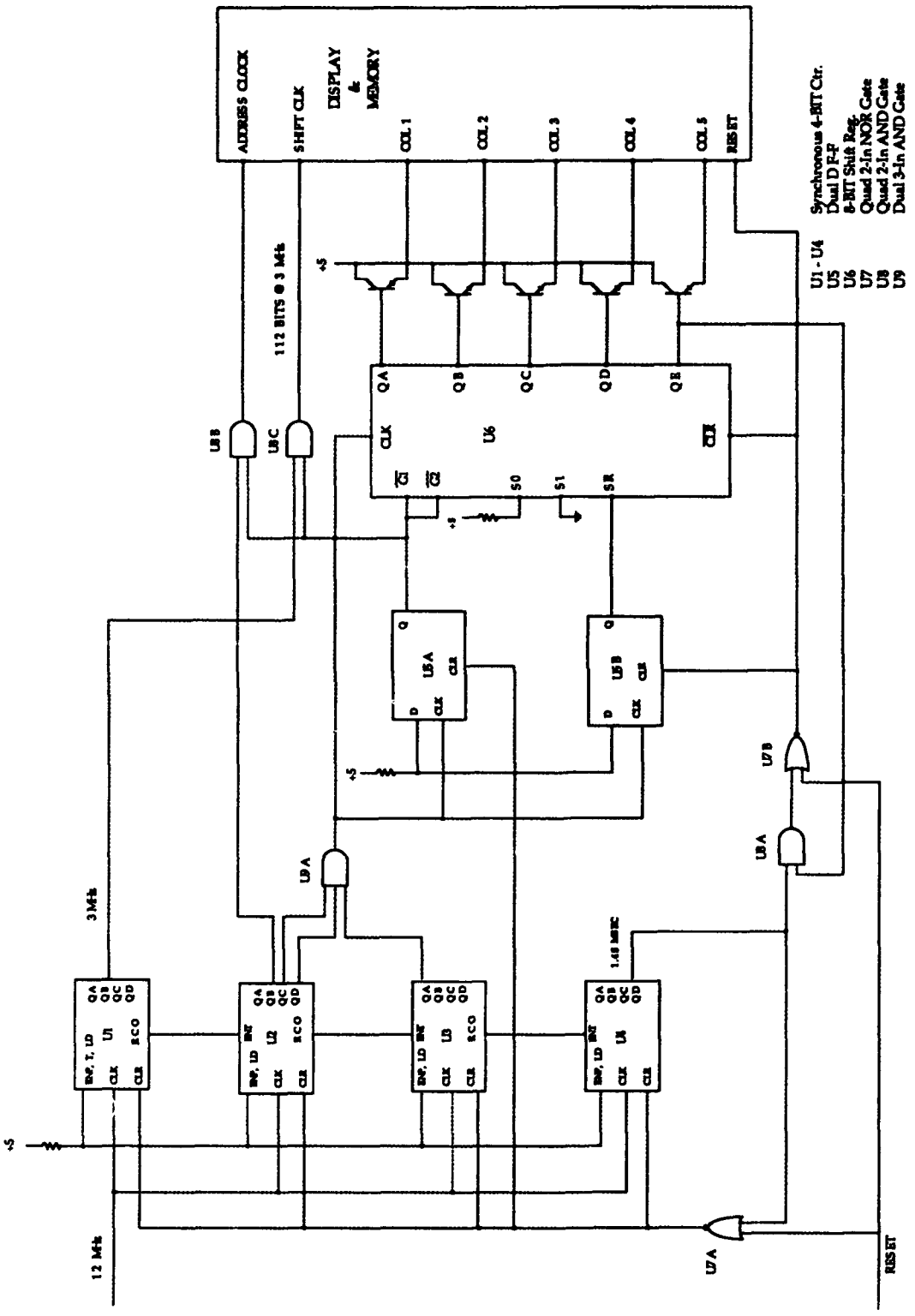
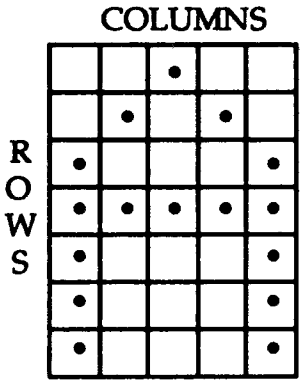


FIGURE 12: CLOCK GENERATOR CIRCUIT

- Each character of the display consists of a 5 column x 7 row LED (Light Emitting Diode) matrix.

  Example:



- The display is multiplexed such that 1 column in any character is illuminated at a given time.

- Each column requires 7 bits of data (7 LEDs) per character in the display.

- The total data per column for 16 characters is 112 bits; a 112-bit FIFO (First In - First Out) register in the display holds the column data.

- The data to be displayed is stored in a 1K x 8 RAM (Random Access Memory). An 8-bit parallel-load, serial shift register transfers the data to the display FIFO within the Display/Memory chip.

- The clock generator provides (1) the timing signals to transfer data from memory to the display, and (2) the column strobe signals to multiplex the display.

- The clock generator input is from a external 12 MHz system clock.

- The clock generator provides a gated 3 MHz clock which is used to load the 112 bits of data from each column from memory.

- A 1.45mS column strobe signal illuminates each of the columns.

- A counter clock signal is used to advance the RAM address after each 8-bit data block is shifted into the FIFO register.

6.1.2 Overview Of Theory Of Operation

A worst case circuit analysis should also include a theory of operation. As described in Section 3.0, the theory of operation provides additional background information for the user. The theory of operation should be concise and convey to the reader the operational characteristics of the circuit. The following are highlights of the theory of operation for the Clock Generator/Display Circuit. Reference the schematic, Figure 12, to follow the circuit theory description:

- ICs (Integrated Circuits) U1 thru U4 are 4-bit, synchronous counters operating at a 12 MHz clock rate.

- The QB output from U1 provides a 3 MHz clock rate for loading the display FIFO.

- The QB output from U2 provides a clock pulse to the RAM address counter after 8 bits are shifted.

- The QC and QD outputs from U2 and the QA output from U3 are gated to indicate when 112 bits have been shifted; this signal clocks F-F (Flip-Flop) U5A & U5B and shift register U6.

- U5A controls the loading of data and the column strobing:

  - $\overline{Q}$ high enables loading of data (through U8B)

  - $\overline{Q}$ low enables column strobing ($\overline{G1}$ & $\overline{G2}$ of U6)

- U5B provides a single high input to shift register U6; this is shifted thru U6 to enable each column in turn

- The QC output from U4 terminates each column strobe after 1.45mS and resets the counters and U5A.

- After the fifth column strobe, U4-QC resets U5B and U6 to start the process over again.

6.1.3 Critical Timing Parameters

The first step of the analysis is to identify the performance parameters that need to be examined. These parameters should be determined before the part database development and analysis begins. The following timing parameters for the Clock Generator Counter will be examined:

- **Clock Frequency**
- **Clock Pulse Width**
- **Set-up Time - Enable Input to Clock**
- **Hold Time - All Inputs**

6.1.4 Worst Case Timing Analysis

An integral part of this analysis is the development of the part parameter database. Typically the part database is a stand-alone item. Since the circuit in this example is not very complex, the timing parameters have been developed concurrently. This example, therefore, represents worst case performance analysis coupled with the parts analysis for the synchronous 4-BIT Counters (U1-4).

SYNCHRONOUS 4-BIT COUNTER PARAMETERS

Recommended Operating Conditions:

Clock Frequency	25MHz, Maximum
Width Of Clock Pulse	25nS, Minimum
Width Of Clear Pulse	20nS, Minimum
Set-Up Times: - ENP or ENT - $\overline{\text{CLR}}$	 20nS, Minimum 20nS, Minimum

Propagation Delay Times:

t_{PLH} (CLK-RC0)	35nS, Maximum
t_{PLH} (CLK-ANY Q)	24nS, Maximum
t_{PLH} (ENT - RC0)	14nS, Maximum

The maximum propagation delay times specified are based on the following conditions:

V_{CC} = +5.0 VDC
TEMP = 25°C
C_L = 15 pF
R_L = 2KW

The following conditions and assumptions were also used for the analysis:

- The effects due to loading will be neglected, since the assumption is made that the actual load is within the specified limits.
- Power Supply (V_{CC}) range is ±10%.
- Worst case temperature range of -55°C to +125°C.

To calculate the maximum increase in propagation delay for a low-to-high transition, examine Figure 13. The maximum increase will occur at high temperature.

DDelay = 1.25nS (From Figure 13)

Nominal Delay = 9nS (Assumed from specifications)

The percent change in propagation delay due to temperature effects is calculated using the following formula:

$$\% \text{ Change} = 100 \bullet \frac{\Delta \text{Delay}}{\text{Nominal Delay}}$$

$$\% \text{ Change} = 100 \bullet \frac{1.25\text{nS}}{9\text{nS}} = +14\%$$

Therefore, the percent change in propagation delay is +14%.

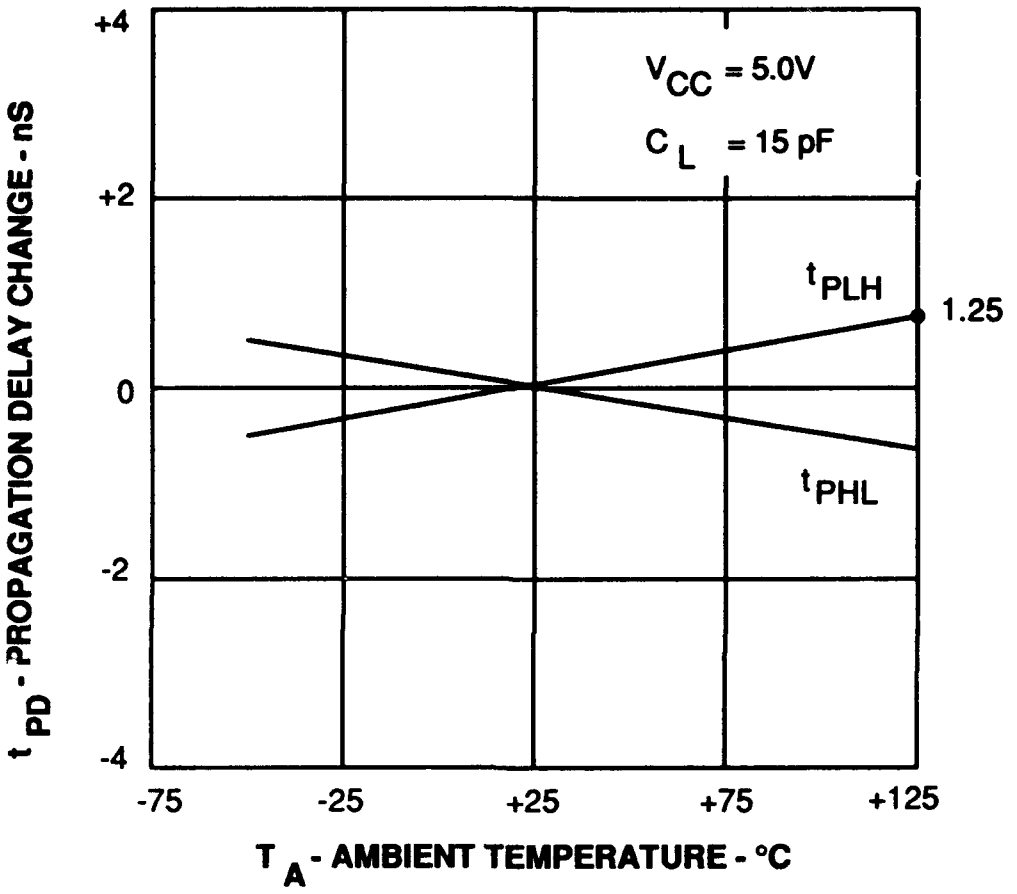


FIGURE 13: TEMPERATURE EFFECTS ON PROPAGATION DELAY

To calculate the maximum increase in propagation delay for a low-to-high transition, examine Figure 14. Using Figure 14 the maximum increase in propagation delay will occur at the minimum supply voltage.

ΔDelay = 0.7nS (From Figure 14)

Nominal Delay = 9.0nS (Assumed from specifications)

The percent change in propagation delay due to supply voltage effects is calculated using the following formula:

$$\% \text{ Change} = 100 \bullet \frac{.7\text{nS}}{9\text{nS}} = +8\%$$

Therefore, the percent change in propagation delay is +8%.

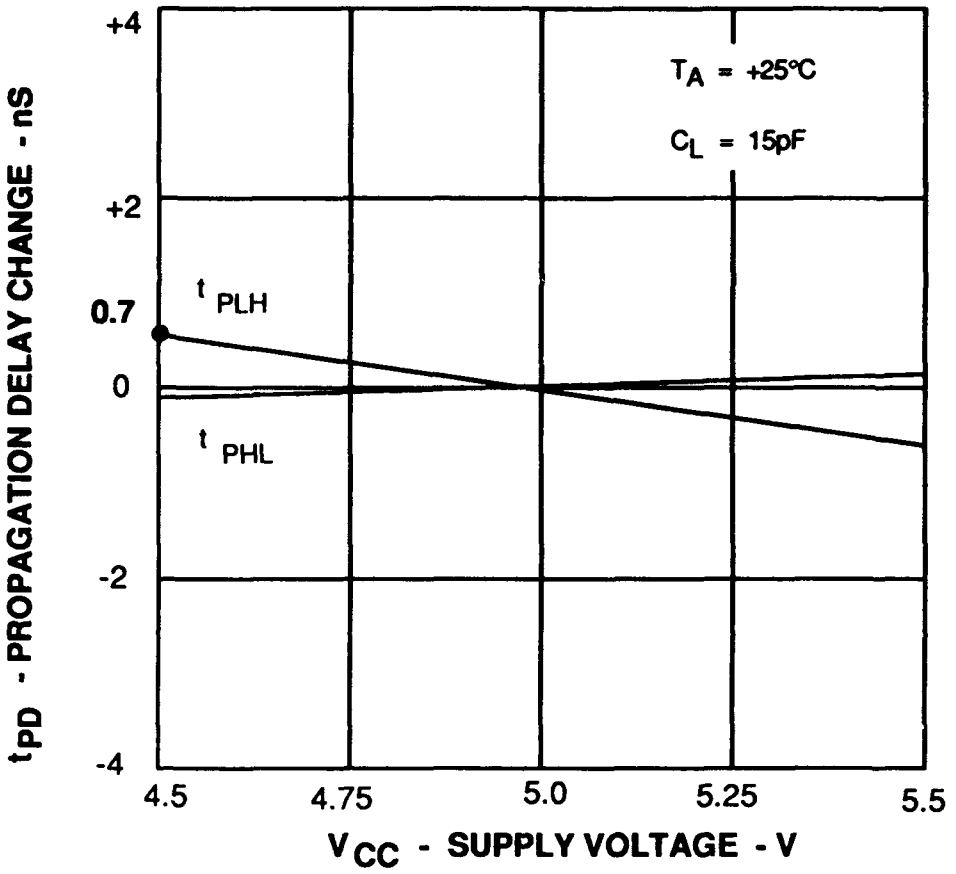


FIGURE 14: POWER SUPPLY EFFECTS ON PROPAGATION DELAY

The temperature and power supply propagation delay effects are additive and can be combined. Therefore, the propagation delay will increase by +22% under worst case conditions.

This factor can be used to calculate various worst case timing characteristics for the Synchronous 4-BIT Counter:

Propagation Delay - Clock to Any Q Output:

Worst Case Delay = 24nS + (22% • 24nS)
≅ 29nS

Propagation Delay - Clock To Carry Output:

Worst Case Delay = 35nS + (22% • 35nS)
≅ 43nS

Propagation Delay - Enable To Carry Output:

Worst Case Delay = 14nS + (22% • 14nS)
≅ 17nS

Another critical timing parameter considered during this analysis is the clock frequency. The table below details the component specification versus the actual clock frequency.

Clock Frequency

Specification	25MHz Maximum
Actual (System)	12MHz

Therefore, the actual clock frequency is within specification of the maximum allowable frequency. This analysis did not consider variations in clock frequency or clock pulse width. It would be highly unlikely that the 12 MHz clock frequency would exceed the 25 MHz specification.

It is also necessary to calculate the clock pulse width. The table below summarizes clock pulse width information.

Clock Pulse Width

Specification	25nS Minimum
Actual	41.7nS

To calculate the pulse width, it was assumed the clock signal had a 50% duty cycle.

Actual Clock Pulse Width = .5 • Period

$$= .5\left(\frac{1}{12\text{MHz}}\right) = 41.7\text{nS}$$

Therefore, the actual clock pulse width is within specification of the minimum allowable pulse width.

It is also necessary to analyze the worst case set-up times. The first set-up time to be analyzed is the clear set-up time. The following considerations were used for the analysis:

- $\overline{CLR}$ set-up time requirement is 20nS minimum.

- The clear input delay is the sum of the U4-QC delay and the delay thru NOR gate U7A.

- The maximum high-to-low propagation delay for U7A is assumed to be 24nS (high to low is assumed to be unaffected by supply voltage and the temperature coefficient is assumed negative).

The clear delay is calculated as follows:

Clear Delay = U4-QC Delay + U7A Delay
= 29nS + 24nS
= 53nS

The clear set-up time can now be calculated using this delay time with the following equation:

Clear Set-up Time = Clock Period - Clear Delay
Clock Period = Clock Pulse Width • 2
= 83.3nS - 53nS
= 30.3nS

Therefore, the minimum required set-up time of 20nS is met.

The same approach can also be employed for calculating the set-up time for the enable input to the clock. The following considerations were used to analyze the set-up time:

- 20nS minimum set-up time requirement.

- The enable inputs to U2, U3 and U4 are the ripple carry outputs (RCOs) from the preceding stage.

- The RCO outputs go high one clock pulse early.

Calculate the U2 set-up time by using the following formula:

U2 Set-Up Time = Clock Period - U1 Clock To Carry Out Delay
= 83.3nS - 43nS = 40.3nS

Therefore, the minimum set-up time of 20nS is met for U2. By continuing to use the worst case propagation delays, the enable delay to U3 can be calculated as follows:

U3 Enable Delay = U2 Enable Delay + U2 Enable To Carry Out Delay
= 43nS + 17nS = 60nS

The result of calculating the U3 enable delay can now be used to calculate the U3 worst case set-up time. The calculation is as follows:

U3 Set-Up Time = Clock Period - U3 Enable Delay
U3 Set-Up Time = 83.3nS - 60nS = 23.3nS

Thus, the U3 set-up time meets the minimum required set-up time of 20nS. Proceed by calculating the U4 enable delay. The calculation is as follows:

U4 Enable Delay = U3 Enable Delay + U3 Enable To Carry Out Delay
= 60nS + 17nS = 77nS

Use this result to calculate the set-up time for U4. The calculation is similar to the calculation for the U3 set-up time:

U4 Set-Up Time = Clock Period - U4 Enable Delay
U4 Set-Up Time = 83.3nS - 77nS = 6.3nS

Under worst case conditions, **the minimum required set-up time for U4 is not met.**

6.1.5 Digital Example Conclusions and Recommendations

Upon completing the analysis, conclusions and recommendations need to be made. In this example, the clock generator circuit fails the worst case set-up time requirement for U4. This worst case failure occurs at high temperature and at a low power supply voltage.

It should be noted that by using the manufacturer specifications at 25°C and a 5 VDC supply, the clock generator circuit does not fail as is shown below:

U4 Enable Delay = U3 Enable Delay + U3 Enable To Carry Out Delay
= (35nS + 14nS) + 14nS = 63nS

U4 Set-Up Time = Clock Period - U4 Enable Delay
= 83.3nS - 63nS = 20.3nS

Therefore, the set-up time for U4 would meet the minimum required set-up time of 20nS using the standard manufacturer specifications.

There are a variety of potential solutions to this problem. Devices with shorter delay times or shorter required set-up times could be used. The recommended solution should balance cost and performance considerations to maximize the benefits gained.

6.2 Analog Circuit Example

As stated previously, the analog circuit example consists of a 10KHz Sallen-Key band pass filter. In this example, the circuit will be analyzed using the EVA, RSS, and Monte Carlo Techniques.

The analog circuit for this example can be found in Figure 15.

6.2.1 Circuit Description/Theory Of Operation

Since this circuit is a fundamental building block, it is not necessary to have a circuit overview and a theory of operation. It is sufficient to describe the circuit as a band-pass filter.

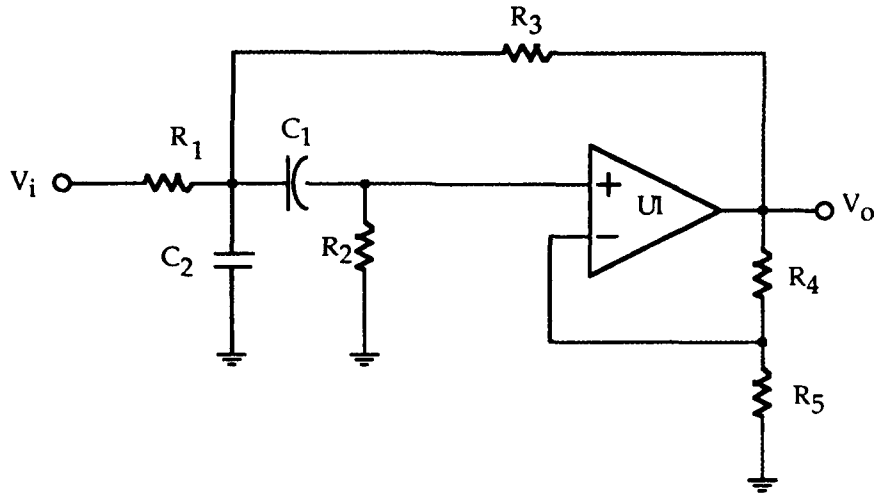


FIGURE 15: 10-KHZ SALLEN-KEY BAND PASS FILTER CIRCUIT

6.2.2 Analog Part Database

The results from the component database are presented in Table 11, which gives the random and bias variations for the resistors and capacitors. Table 12 summarizes the worst case part parameter tolerance extremes. For this example, the operational amplifier was modeled as an ideal device.

TABLE 11: BIAS AND RANDOM COMPONENT VARIATION

COMPONENT	NEGATIVE BIAS	POSITIVE BIAS	RANDOM
RESISTORS	--	.43%	1.16%
CAPACITORS	.1%	--	5.6%

TABLE 12: WORST CASE PART PARAMETER TOLERANCE EXTREMES

PART DESIGN.	PARAMETER	NOMINAL VALUE	TOLERANCE		ANALYSIS VALUE	
			MIN %	MAX %	MIN	MAX
C1	CAPACITANCE	1000pf	5.7	5.6	943	1056
C2	CAPACITANCE	1000pf	5.7	5.6	943	1056
R1	RESISTANCE	22.1KΩ	1.16	1.59	21844	22451
R2	RESISTANCE	22.1KΩ	1.16	1.59	21844	22451
R3	RESISTANCE	22.1KΩ	1.16	1.59	21844	22451
R4	RESISTANCE	40.2KΩ	1.16	1.59	39733	40839
R5	RESISTANCE	10KΩ	1.16	1.59	9884	10159

6.2.3 Band-Pass Requirement/Specification

The primary circuit parameter being examined in this example is the center frequency. The circuit specification is as follows:

f_o = 10KHz ±.7KHz

f_o max = 10.70KHz f_o min = 9.3KHz

6.2.4 Worst Case Analysis

This analysis will examine the worst case shift in the center frequency of the band-pass filter. To simplify the analysis, the equation for the center frequency is given as:

$$f_o = \frac{1}{2\pi}\left(\frac{R_1 + R_3}{R_1R_2R_3C_1C_2}\right)^{1/2} \quad \text{or} \quad f_o = \frac{1}{2\pi}\left(\frac{1}{R_2R_3C_1C_2} + \frac{1}{R_1R_2C_1C_2}\right)^{1/2}$$

The directional sensitivity of each part, by inspection, is negative (-).

6.2.4.1 Extreme Value Analysis

First it is necessary to calculate the maximum center frequency. Set all part values to their extreme **minimum** limits and solve the circuit equation for f_o.

Therefore:

$R_1min = R_2min = R_3min = 21{,}844W$ and,

$C_1min = C_2min = 943$ pF

Using these values and the given equation the maximum center frequency is found to be:

f_o max = 10.93 KHz

Next, calculate the minimum center frequency. To do this, set all part values to their extreme **maximum** limits and solve the circuit equation for f_o.

Therefore:

$R_1max = R_2max = R_3max = 22{,}451W$ and,

$C_1max = C_2max = 1056$ pf

f_o min = 9.49 KHz

A comparison of the worst case calculated results and performance requirements show that **the circuit fails the maximum center frequency swing.**

The next step is to utilize the RSS analysis method for this circuit.

6.2.4.2 Root-Sum-Squared Analysis

The center frequency, f_o, can drift out of specification (using the EVA results) by a small amount. Therefore, the RSS method may yield more realistic results. The frequency determining components are in Table 13.

TABLE 13: PIECE-PART PARAMETER VARIATIONS FROM DATABASE

COMPONENT	NOMINAL VALUE	NEGATIVE BIAS	POSITIVE BIAS	RANDOM
C	1000pF	.1%	--	5.6%
R	22100Ω	–	.43%	1.16%

It should be noted that the random portion tabulated in the data base represents the 3σ variation assuming a normal distribution.

The C and R parameter variations can be resolved into a **bias** and a **spread**. The spread is the maximum variation from the nominal. The equivalent parameter variations for the bias and spread can be found in Table 14.

TABLE 14: EQUIVALENT PARAMETER VARIATIONS

PARAMETER	NOMINAL	BIAS	SPREAD (3s)
C	1000pF	-1pF(.1%)	+/-56 pF (5.6%)
R	22100W	+95W(.430%)	+/-256W (1.16%)

Any biasing of the components away from the nominal value will result in an offset of f_o from nominal.

f_o bias (minimum) is the value of the center frequency when the components assume their positive biased value.

Use:

$R_1 = R_2 = R_3 = 22195\Omega$

$C_1 = C_2 = 1000$ pF

Calculate f_o given:

$$f_o = \frac{1}{2\pi}\left(\frac{R_1 + R_3}{R_1 R_2 R_3 C_1 C_2}\right)^{1/2}$$

$$f_{o\ bias}\ \text{min} = 10.14\ \text{KHz}$$

$f_{o\ bias}$ (maximum) is the center frequency value when the components assume their negative biased value.

Use:

$$R_1 = R_2 = R_3 = 22100\text{W}$$

$$C_1 = C_2 = 999\ \text{pF}$$

Calculate f_o with the given equation. Therefore, the calculated maximum value is found to be:

$$f_{o\ bias}\ \text{max} = 10.20\ \text{KHz}$$

Figure 16 is a distribution of f_o about its nominal value if component parts did not experience bias offsets.

While Figure 17 demonstrates the shift in center frequency due to bias variations in the component's parameters.

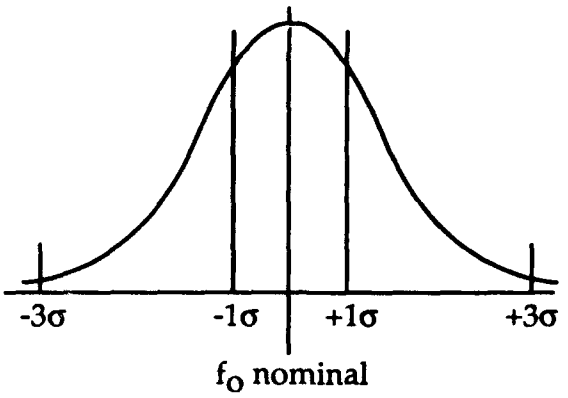


FIGURE 16: f_o DISTRIBUTION WITH NO BIAS OFFSETS

After the bias calculations have been completed, the analyst needs to consider the f_o random variables.

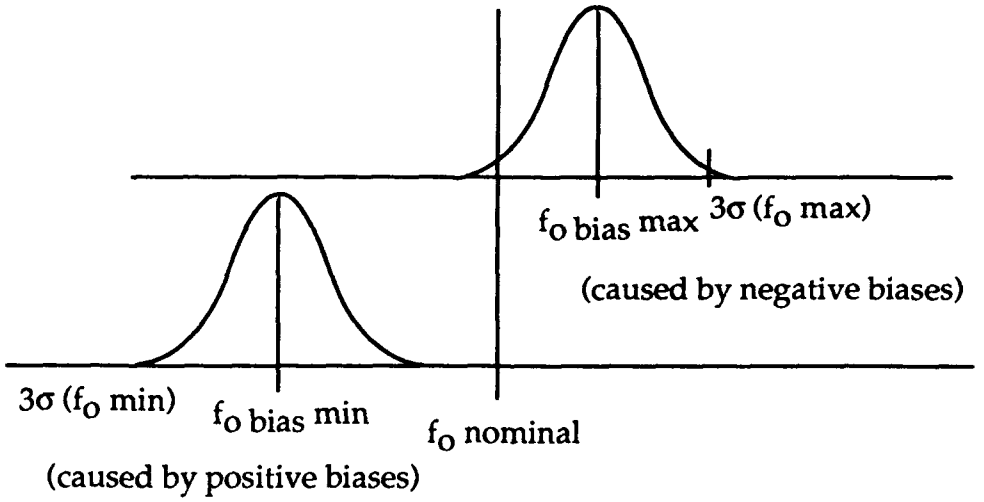


FIGURE 17: FREQUENCY SHIFTS DUE TO BIAS VARIATIONS

The variation of the center frequency is normally distributed and symmetrical about f_o nominal.

Knowing this, it is necessary to determine the magnitude of sensitivity of f_o to each component. First, determine the standard deviation of the component parameter values and sensitivity at f_o (minimum).

The sensitivity calculation for C_1 is shown below. The calculations for the other components is similar.

Since the distribution of the components was unknown, the 1σ limit was considered to be 1/3 of the 3σ limit. The part parameter variation data was assumed to be 3σ limits.

Therefore, the 1σ limit is calculated by the following equation:

$$1\sigma = \frac{5.6\%}{3}$$
$$= 1.866\%$$

Thus the 1s deviation for C_1 is:

$$\sigma_1 = 1000\ pF \bullet 1.866\%$$
$$= 18.66\ pF$$

The sensitivity of frequency due to variations in C_1 is calculated by taking the partial derivative of the governing equation for C_1.

$$\frac{\partial f_o}{\partial C_1} = \frac{\partial}{\partial C_1}\left(\frac{1}{2p}\sqrt{\frac{R_1 + R_3}{R_1R_2R_3C_1C_2}}\right)$$

$$= -\frac{1}{4p}\sqrt{\frac{R_1 + R_3}{R_1R_2R_3C_2}} \bullet C_1^{-\frac{3}{2}}$$

By substitution:

$$\frac{\partial f_o}{\partial C_1} = 5.092E + 12/F$$

Table 15 summarizes the sensitivity and standard deviation information for the circuit.

TABLE 15: POSITIVE COMPONENT SENSITIVITY AND STANDARD DEVIATION

PARAMETER	SENSITIVITY $\left(\frac{\partial fo}{\partial x}\right)$	STANDARD DEVIATION	
C_1	-5.092E + 12/F	18.66E-12F	σ1
C_2	-4.982983E + 12/F	18.66E-12F	σ2
R_1	-.115/Ω	85.33Ω	σ3
R_2	-.23/Ω	85.33Ω	σ4
R_3	-.115/Ω	85.33Ω	σ5

Using the data from Table 15, the standard deviation of f_o around f_o bias (minimum) can be found using the following equation:

$$\sigma_{min} = \left[\sqrt{\left(\frac{\partial f_o}{\partial c_1} s1\right)^2 + \left(\frac{\partial f_o}{\partial c_2} s2\right)^2 + \left(\frac{\partial f_o}{\partial R_1} s3\right)^2 + \left(\frac{\partial f_o}{\partial R_2} s4\right)^2 + \left(\frac{\partial f_o}{\partial R_3} s5\right)^2} \right]$$

σ_{min} = 136.5 Hz

Once the standard deviation is known a minimum frequency can be calculated using the formula:

f_o minimum = f_o bias min - $3\sigma_{min}$

= 10141 - 3(136.5) Hz = 9731 Hz

= 9731 Hz

The procedure for determining f_o (maximum) is similar to the procedure for calculating f_o (minimum). See the previous calculation for an example. Again, determine the magnitude of sensitivity of f_o and the standard deviation for each component parameter value at f_o bias. See Table 16 for sensitivity and standard deviation information.

TABLE 16: NEGATIVE COMPONENT SENSITIVITY AND STANDARD DEVIATION

PARAMETER	SENSITIVITY $\left(\frac{\partial fo}{\partial x}\right)$	STANDARD DEVIATION	
C_1	-5.092E + 12F	18.66E-12F	σ1
C_2	-5.092E + 12F	18.66E-12F	σ2
R_1	-.115/Ω	85.33Ω	σ3
R_2	-.23/Ω	85.33Ω	σ4
R_3	-.115/Ω	85.33Ω	σ5

Using the data from Table 16 the standard deviation of f_o around f_o bias (maximum) can be calculated using the formula:

$$\sigma_{max} = \left[\sqrt{\left(\frac{\partial f_o}{\partial c_1} s1\right)^2 + \left(\frac{\partial f_o}{\partial c_2} s2\right)^2 + \left(\frac{\partial f_o}{\partial R_1} s3\right)^2 + \left(\frac{\partial f_o}{\partial R_2} s4\right)^2 + \left(\frac{\partial f_o}{\partial R_3} s5\right)^2} \right]$$

σ_{max} = 136.5 Hz

Again, once the standard deviation is known, the maximum center frequency can be calculated:

f_o max = f_o bias max + $3\sigma_{max}$

= 10195 + 3(136.5) Hz = 10604.5 Hz

= 10604.5 Hz

6.2.5 Monte Carlo Analysis

To perform the Monte Carlo analysis a small C++ program was written to analyze the circuit. The program listing can be found in Figure 18. The results of the Monte Carlo analysis can be found in Table 17.

```
//
// Monte Carlo Analysis Of Sallen-Key Bandpass Filter
//
#include <stream.hpp>
#include <stdlib.h>
#include <math.h>
#include <time.h>
#define pi 3.14159
main()
{
        int index1, iter1, iter2, ct;
        double temp, con, fsum, f2sum, fmax, fmin, mean, sd, pass;
        double r1[500], r2[500], r3[500], c1[500], c2[500], f[500];
        con = 1/(2*pi);
        cout << '\n'<<  "Sallen-Key Bandpass Filter Monte Carlo Analysis\n";
        cout  <<  "-----------------------------------------------";
        cout << "\n \n";
        cout << "Enter number of iterations (<=500) ";
        cin >> iter1;
        cout << '\n';
//
// Generate Random Resistance and Capacitance Values
//
        srand(time(NULL)); iter2 = iter1 - 1;
        for (index1=0;  index1<=iter2; index1++) {
                        r1[index1]=22100*(.99+.0159*rand()/32676);
                        r2[index1]=22100*(.99+.0159*rand()/32676);
                        r3[index1]=22100*(.99+.0159*rand()/32676);
                        c1[index1] = 1000E-12*(.99+.057*rand()/32676);
                        c2[index1] = 1000E-12*(.99+.057*rand()/32676);
       }
//
// Calculate Monte Carlo Frequency, Mean, and Standard Deviation
//
        fsum = 0; fmax = 0; fmin = 10184.58;
        for (index1=0; index1<=iter2; index1++) {
                        temp = r1[index1]*r2[index1]*r3[index1]*c1[index1]*c2[index1];
                        f[index1] = con*sqrt((r1[index1]+r3[index1])/temp);
                        fsum += f[index1];
                        if (f[niex1] > fmax)
                            fmax = f[index1];
                        if (f[index1] < fmin)
                            fmin = f[index1];
          }
// Calculate mean of circuit
        mean=fsum/iter1;
// Calculate standard deviation of circuit
          f2sum = 0;
          for (index1=0; index1<=iter2; index1++)
                f2sum += (f[index1]-mean)*(f[index1]-mean);
          sd=sqrt(f2sum/iter1);
// Calculate percentage of units meeting specification
          ct = 0;
          for (index1=0; index1<=iter2; index1++) {
                        if (f[index1] >=9300)
                                if (f[index1] <=10700)
                                   ct++;
          }
          pass = 100*ct/iter1;
          cout << "Minimum Gain: " << fmin << '\n';
          cout << "Maximum Gain: " << fmax << '\n';
          cout << "Mean: " << mean << '\n';
          cout << "Standard Deviation: " << sd << '\n';
          cout << "Pass Percentage:" << pass << '\n';
}
//
// Written using the Zortech 2.1 Small Model C++ Compiler
//
```

FIGURE 18: SALLEN-KEY BANDPASS FILTER MONTE CARLO PROGRAM

TABLE 17: MONTE CARLO RESULTS

# Simulations	Min. Gain	Max. Gain	Mean	Standard Deviation	% Pass
25	9729	10304	9989	117.2	100
50	9817	10287	10001	119.758	100
75	9764	10291	10017	114.6	100
100	9760	10275	10009	112.8	100
125	9766	10258	10023	111.6	100
150	9753	10312	10039	118.14	100
175	9791	10281	10015	109.7	100
200	9730	10305	10012	119.9	100
225	9776	10330	10026	109.2	100

It should be noted that there is a major deficiency with this simulation. The number of simulations is far too limited. More simulations are necessary to get statistically significant results. The reason for the low number of simulations is due to the small model C++ compiler. This problem could be circumvented with additional programming and compiler settings. This program serves as one possible method of performing a Monte Carlo analysis.

6.2.6 Analog Circuit Conclusions

The analog circuit example utilized the EVA, RSS, and Monte Carlo methods of analysis. This example demonstrated that although the circuit did fail to meet the requirements using the EVA approach, it did pass the requirements using the RSS method. A summary of the results can be found in Table 18.

TABLE 18: SAMPLE WCCA RESULTS

Frequency	Requirement	EVA Results	RSS Results	Monte Carlo Results
Lower Limit	9.3KHz	9.49KHz	9.7KHz	9776 Hz
Center Frequency	10KHz	-	-	10026 Hz
Upper Limit	10.7KHz	10.93KHz	10.6KHz	10330 Hz

It should be noted that the RSS results dictate that greater than 99.7% of all filters will meet the requirements which represents the 3σ limits of circuit operation. In cases where the circuit marginally fails the EVA analysis, such as this filter circuit, the RSS or Monte Carlo analyses may be useful to quantify the deviation.

The Monte Carlo analysis also demonstrated that the circuit met its requirements. The results lack confidence boundaries due to the small number of simulations, but the analysis does demonstrate one possible Monte Carlo technique.

APPENDIX A
RAC PRODUCTS

RAC Product Order Form

(DP92-2)

		U.S.	Non-U.S.	Qty	Item Total
217	MIL-HDBK-217F, Notice 1 (Microsoft Word Version 4.0)	75.00	85.00		
338	MIL-HDBK-338B (Draft) (Microsoft Word Version 4.0)	95.00	105.00		
ATH	Analog Testing Handbook	100.00	120.00		
CRTA-CE	Introduction to Concurrent Engineering	75.00	85.00		
CRTA-FMECA	Failure Mode, Effects and Criticality Analysis	75.00	85.00		
CRTA-GAAS	An Assessment of GaAs Device Quality and Reliability	50.00	60.00		
CRTA-PEM	Plastic Microcircuit Packages: A Technology Review	50.00	60.00		
CRTA-PSA	Parts Selections, Application and Control	50.00	60.00		
CRTA-QML	Qualified Manufacturer's List: New Device Manufacturing and Procurement Technique	50.00	60.00		
CRTA-TEST	Testability Design and Assessment Tools	50.00	60.00		
CRTA-WCCA	Worst Case Circuit Analysis Application Guidelines	75.00	85.00		
DSR-4	Discrete Semiconductor Device Reliability	100.00	120.00		
FMD-91	Failure Mode/Mechanism Distributions	100.00	120.00		
FTA	Fault Tree Analysis Application Guide	80.00	90.00		
MDR-21	Microcircuit Device Reliability Trend Analysis Databook	100.00	120.00		
MDR-22	Microcircuit Screening Analysis	125.00	145.00		
MFAT-1	Microelectronics Failure Analysis Techniques - A Procedural Guide	140.00	180.00		
MFAT-2	GaAs Microcircuit Characterization & Failure Analysis Techniques	100.00	120.00		
MFAT-1&2	Combined set of MFAT-1 and MFAT-2	200.00	260.00		
NONOP-1	Nonoperating Reliability Databook	150.00	170.00		
NPRD-91	Nonelectronic Parts Reliability Data 1991	150.00	170.00		
NPRD-91P	Nonelectronic Parts Reliability Data 1991 (IBM PC database)	400.00	440.00		
NPS-1	Analysis Techniques for Mechanical Reliability	60.00	70.00		
PRIM-92	A Primer for DoD Reliability, Maintainability, Safety and Logistics Stds	120.00	140.00		
QML-1	QML Workshop Proceedings	25.00	35.00		
QREF	RAC Quick Reference Guides	39.00	49.00		
RAC-NRPS	Nonoperating Reliability Prediction System (Includes NONOP-1)	1400.00	1450.00		
RMST-93	Reliability and Maintainability Software Tools 1993	50.00	60.00		
RQ	RAC Quarterly (Annual Subscription- 4 issues)	30.00	35.00		
SOAR-2	Practical Statistical Analysis for the Reliability Engineer	40.00	50.00		
SOAR-4	Confidence Bounds for System Reliability	50.00	60.00		
SOAR-5	Surface Mount Technology: A Reliability Review	60.00	70.00		
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SOAR-7	A Guide for Implementing Total Quality Management	75.00	85.00		
SOAR-8	Process Action Team (PAT) Handbook	80.00	90.00		
VPRED	VHSIC Reliability Prediction Software	150.00	170.00		
VZAP-91	Electrostatic Discharge Susceptibility Data 1991	150.00	170.00		
VZAP-91P	Electrostatic Discharge Susceptibility Data 1991 (IBM PC database)	400.00	440.00		
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ZSG	RAC User Guide (Description of RAC consulting services)	0.00	0.00		
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