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The Impact of ASIC Devices on the SEU Vulnerability of Space-Borne Computers

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Application specific integrated circuits (ASICs) offer a number of advantages over traditional multi-component microcircuits including reductions in both size and power dissipation, and are therefore prime candidates to replace such microcircuits in space-borne electronics systems. The results of recent tests of the susceptibilities of various ASIC devices to cosmic ray and trapped proton induced single event upset (SEU) and latchup are reported here and are compared to the susceptibilities of the devices that they would replace. This comparison leads to a discussion of the impact of ASIC devices on the SEU susceptibility of space-borne computers.

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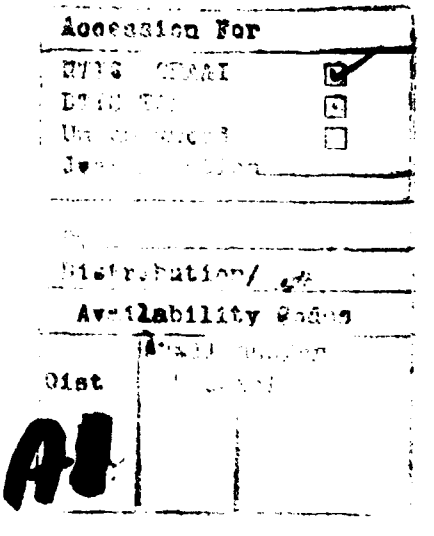

FIGURES

TABLES

Abstract

Application specific integrated circuits (ASICs) offer a number of advantages over traditional multi-component microcircuits including reductions in both size and power dissipation, and are therefore prime candidates to replace such microcircuits in space-borne electronics systems. The results of recent tests of the susceptibilities of various ASIC devices to cosmic ray and trapped proton induced single event upset (SEU) and latchup are reported here and are compared to the susceptibilities of the devices that they would replace. This comparison leads to a discussion of the impact of ASIC devices on the SEU susceptibility of space-borne computers.

Introduction

Application specific integrated circuits (ASICs) are large scale integration (LSI) microelectronic devices that can emulate complex circuits consisting of numerous small and medium scale integration (SSI and MSI) devices. The class of ASICs currently includes field-programmable gate arrays (FPGAs), process-programmable gate arrays (PPGAs), programmable logic devices (PLDs), and programmable array logic (PAL) devices. (Process-programmable gate arrays are sometimes called mask-programmed gate arrays.) The functions of these various ASIC device types overlap as well as complement one another. For example, field-programmable and process-programmable gate arrays differ primarily in that the former may be electrically programmed whereas the latter requires programming as part of the fabrication process.

ASIC devices offer a number of advantages over traditional multi-component microcircuits including reductions in both size and power dissipation. These advantages become particularly important when designing electronics systems for use in space. ASIC devices form integral parts of the designs for control circuits on NASA's upcoming ISTP (International Solar Terrestrial Program) and SAMPEX (Solar Anomalous Component Magnetospheric Particle Explorer) spacecraft. Clearly the suitability of these devices as components in complex, high-speed, low-power, space-borne systems depends critically on their tolerance of the space radiation environment.

The results of recent tests of the susceptibilities of various ASIC devices (mostly gate arrays) to cosmic ray and trapped proton induced single event upset (SEU) and latchup are reported below, followed by a discussion of techniques for reducing the SEU vulnerability of ASIC devices. The suitability of ASIC devices to space applications is then discussed, with an emphasis on the similarities and differences between these devices and those they would replace in space-borne computers.

Test Devices

Within the last few years we have investigated the SEU and latchup susceptibilities of the ASIC device types listed in Table 1. These parts are high-speed, low-power devices that have been selected for possible use in space. None of the FPGAs or PLDs were radiation-hardened, whereas all of the PPGAs except LL7320Q were.

The Altera PLDs were programmed in-house prior to testing. The memory elements in these devices incorporate CMOS floating-gate technology and are therefore very similar to some EPROMs (Electrically Programmable Read-Only Memory).

All of tested FPGA samples were manufactured by Actel in two-level metal (n-well) CMOS (with epitaxial layer) technology, using Matsushita dies. The Actel ACT1010 (ACT1020) FPGA consists of 295 (546) combinatorial logic modules (C-modules), each of which contains about 50 transistors. Each module can be individually programmed to form a simple logic building block such as a gate, latch, flip-flop, etc. These modules can then be tied together to produce combined logic/storage systems. A complex electronics board with many microcircuits (such as 54HC or CD4000 series devices) can thus be replaced by a single field-programmable

Table 1. ASIC Devices Tested for SEU and Latchup

Device	Mfr.	Technology	#Elements	Features
FPGA				
ACT1010	Actel	CMOS (epi)	295 modules†	2.0 µm
ACT1020	Actel	CMOS (epi)	546 modules†	2.0 µm
ACT1280	Actel	CMOS (epi)	1200 modules†	1.2 µm
PLD				
EP910	Altera	CMOS	900 gates	2.0 µm
EP1210	Altera	CMOS	1200 gates	4.0 µm
EP1800	Altera	CMOS	2100 gates	2.0 µm
PPGA				
LL7320Q	LSI	CMOS	~1k gates	2.0 µm
LRH9320Q	LSI	CMOS (epi)	~3k gates	1.5 µm
LRH91000	LSI	CMOS (epi)	~10k gates	1.5 µm
LRH10038Q	LSI	CMOS (epi)	~38k gates	1.5 µm
HP03	UTMC	CMOS (epi)	Test chip	1.5 µm
RA20K	UTMC	CMOS (epi)	Test chip	1.0 µm

† A module consists of about 10 PLD - equivalent gates.
Actel: Actel Corporation; Altera: Altera Corporation;
UTMC: United Technologies Microelectronics Center;
LSI: LSI Logic Corporation.

gate array. The Actel ACT1280 is a second generation FPGA that combines C-modules with modules that can implement sequential as well as combinatorial logic (S-modules).

The PPGA samples were manufactured by LSI Logic and United Technologies Microelectronics Center (UTMC). These devices were fabricated utilizing two-level metal (n-well) CMOS (with epitaxial layer) technology, with the exception of LL7320Q, which does not include an epitaxial layer. However, LL7320Q is not radiation-hardened, as are the others.

Commercial grade versions of the non-radiation-hardened devices (FPGAs, PLDs, and LL7320Q) were utilized in order to generate test results quickly. While the recommended operating temperature of commercial grade devices is between 0°C and 70°C, tests were conducted at temperatures up to 100°C, as well as at room temperature, with no abnormality of function. It would have taken a longer time to procure high reliability grade devices, whose operating temperature ranges exceed 125°C.

Test Techniques

Device Configurations

The PPGA test devices were programmed either as a series of memory elements (latches or flip-flops) or as a static random access memory (SRAM), as shown in Table 2. The devices were then tested for SEU susceptibility while the memory elements were dynamically operated.

The FPGAs were programmed as multiple twisted ring counters. These counters had a common CLEAR input and CLOCK input. Each ACT1010 (ACT1020) was programmed to emulate 4 (5) 10-bit long ring counters (10 master-slave flip-flops), and therefore contained 40 (50) vulnerable bits. The ACT1280s were programmed as four sets of 60-bit long twisted ring counters. Each PLD was programmed as a string of D flip-flops.

SEU and Latchup Measurement

SEU and latchup tests were conducted at the Lawrence Berkeley Laboratory 88-inch cyclotron facility using Xe (603 MeV), Kr (380 MeV), Cu (290 MeV), Ar (180 MeV), Ne (90 MeV), and N (67 MeV) ion beams. The test devices were oriented at various angles to the incident beams in order to obtain "effective LET" values (the effective LET is found by dividing the actual LET by the cosine of the exposure angle). Care was taken to ensure close agreement among cross-section values obtained from different particle beams having the same effective LET. The beam monitor and the mechanism for rotating and positioning the test devices were located within a vacuum chamber at the end of the beam pipe. Additional information on the test set-up may be found in [1].

SEU measurements were obtained with a device-independent tester called the Bus Access Storage and Comparison System (BASACS). BASACS is a logic analyzer, operated via a Macintosh II computer, that can record the correct output signature of a test device while the device is not in the beam line ("dry run"). Later, during exposure to a particle beam, BASACS compares the device outputs with the recorded signature and flags any differences as errors. More specifically, the SEU test procedure is as follows:

1. At the start of the test, the correct signature of the device under test (DUT) is transferred from the Macintosh II computer to BASACS.
2. The CLEAR inputs to the DUT are held low for 10 ms while the beam shutter opens.
3. The DUT is then run through one complete cycle (20 clocks cycles). This is done to ensure that the circuit was initialized properly. If an error occurs in this test cycle, it is flagged as a synchronization error and is not counted as an upset. The DUT is then reset and the test cycle is restarted. (Synchronization errors could result for the FPGA ring counters from setup times not being met, because the reset input is asynchronous to the clock.)
4. After a successful comparison of the first cycle, the DUT is cycled continually while the outputs are monitored.
5. When BASACS finds an error (an output does not match the prerecorded pattern), the states of all outputs, position in the cycle, and other necessary information are transmitted to, and stored in the Macintosh computer. The DUT is then reset for 10 ms, and the test starts again after running one test cycle to make sure the device has completely recovered from the upset.

During testing the upset rate was kept between 1 and 3 per second. This made the dead time caused by resetting the test device negligible compared to the total test time. In addition, because the device cycled thousands of times between upsets, no part of the device was checked more often than any other.

After a sufficient number of errors had been stored, the test was stopped and the total fluence of particles, F, and total number of errors, N, were recorded. The device error probability or cross-section, σ, was then calculated as:

$$\sigma = (N/F) \sec \theta$$

where θ is the incident angle of the beam measured with respect to the chip-surface normal.

Latchup was detected by monitoring the device power supply for any abrupt increase in current. This was done automatically using a computer-controlled power supply.

SEU measurements were taken at elevated temperatures (for example, 80°C and 100°C for FPGAs) as well as at room temperature (25°C). The commercial grade devices used in these tests functioned normally at the elevated temperatures.

Table 2. Configuration of LSI Logic and UTMC PPGAs for SEU Testing

Series	Equivalent Circuits for SEU Testing	# of Bits
LL7320Q	D Latches	16 x 4
LRH9320Q	D Latches	16 x 4
LRH91000	D Flip-Flops	600
LRH10038Q	6 Trans. SRAM Cells	128 x 8
HP03	D Latches	840
RA20K	D Flip-Flops	64 x 16

Test Results

SEU Test Results

The vulnerability of a given device type is summarized by two measures: the upset "saturation" cross-section (S_{Sat}) and the linear energy transfer threshold (LET_{Th}), defined to be the LET at which the cross-section is reduced to 1% of the S_{Sat} value. Table 3 lists the S_{Sat} and LET_{Th} values obtained for the test devices. As can be seen, latchup was observed in only three of the tested ASIC device types: LL7320Q, EP910, and EP1800; none of the radiation-hardened devices exhibited latchup.

Room temperature SEU test results for the ACT1010, ACT1020, and ACT1280 FPGAs are shown in Figs. 1–3, respectively. In these graphs the abscissa gives the effective LET as determined by the ion energy and the ion beam orientation with respect to the test device, and the ordinate represents the probability of upset, or upset cross-section. As is apparent from the figures, the SEU susceptibilities of the ACT1010, the ACT1020, and the C-modules of the ACT1280 are all very similar (the ACT1280 S-modules are more susceptible to SEU). The test results at elevated temperatures (80°C and 100°C) were essentially identical to those obtained at room temperature.

SEU test results for LL7320Q, LRH9320Q, LRH91000, LRH10038Q, HP03, and RA20K PPGAs are shown in Figs. 4–9, respectively. The statistical errors are very small and are buried in the data points. For LL7320Q and HP03 only one device each was tested. As expected, the non-radiation-hardened LL7320Q had a large SEU cross-section. Among the radiation-hardened devices, LRH9320Q had the largest upset cross-section – much higher than any of the other PPGAs.

The PLDs were tested mainly for latchup since they are not radiation-hardened. Only one PLD device type, EP910, was tested for SEU. Unfortunately, the high latchup rate of this device precluded precise determination of the SEU cross-section.

Total Dose Considerations

In a recent independent total dose test of the Actel FPGAs conducted in our laboratory, both the ACT1010 and ACT1020 passed the 500 kRad(Si) level. (For this test the FPGAs were biased during irradiation; both parametric and functional tests were conducted.) The second generation ACT1280 is expected to have a lower total dose limit. The radiation-hardened LSI Logic PPGAs have been tested for total dose susceptibility in other laboratories and have passed the 500 kRad(Si) level [2]. The UTMC devices reportedly have a total dose limit of about 1 MRad(Si) [3].

Mechanisms of SEU Sensitivity

There are four sensitive transistors in an ACT1010 flip-flop, as illustrated in Fig. 10 (this figure displays as much detail as possible without revealing proprietary information). In this circuit the drains of the off-transistors in the two inverters (a and b) and the off-transistors at c and d are vulnerable to upset. Assuming a rectangular sensitive region for each transistor and

Table 3. Test Results for ASIC Devices

Device Type	SEU LET_{Th}	SEU S_{Sat}	Latchup LET_{Th}	Latchup S_{Sat}
FPGA				
ACT1010	25	5×10^{-6}†	– No latchup –	
ACT1020	25	5×10^{-6}†	– No latchup –	
ACT1280	23	3×10^{-6}†	– No latchup –	
" "	5	8×10^{-5}‡	– No latchup –	
PLD				
EP910	4	No Data	15	7×10^{-4}
EP1210	No Data*	No Data	– No latchup –	
EP1800	No Data*	No Data	15	2×10^{-3}
PPGA				
LL7320Q	20	1×10^{-4}	25 (25°C)	1×10^{-2}
" "	No Data*	No Data	20 (80°C)	1×10^{-2}
LRH9320Q	30	4.7×10^{-6}	– No latchup –	
LRH91000	50	3×10^{-8}	– No latchup –	
LRH10038Q	30	1×10^{-7}	– No latchup –	
HP03	45	1×10^{-7}	– No latchup –	
RA20K	55	1×10^{-6}◊	– No latchup –	

* Latchup test only.
† C-modules tested at 25°, 80° and 100°C.
‡ S-modules tested at 25°, 80° and 100°C.
◊ Test chip; tested at 25°, 80° and 100°C.

LET is measured in MeV/(mg/cm^2), and S_{Sat} in cm^2/bit for SEU and cm^2/device for latchup. By "No latchup," is meant that LET_{Th} is higher than about 100 MeV/(mg/cm^2) and the cross-section is below 10^{-7} cm^2/device.

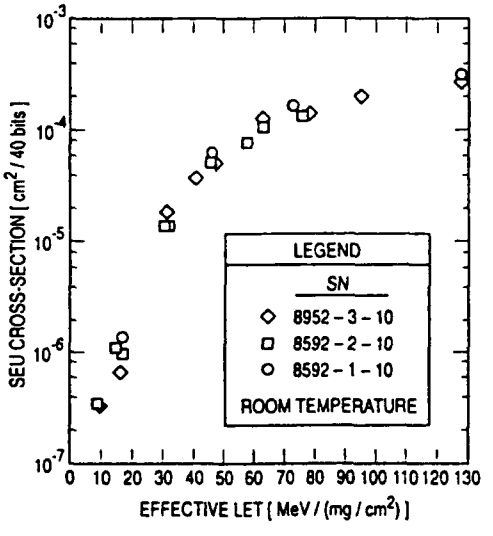

Fig. 1. SEU Test Results for ACT1010

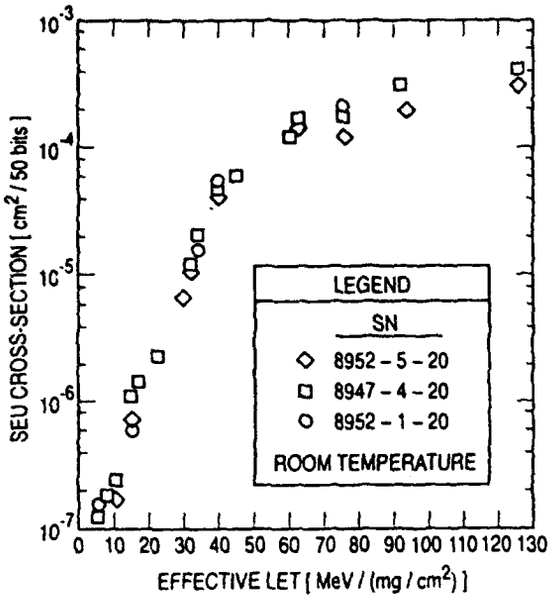

Fig. 2. SEU Test Results for ACT1020

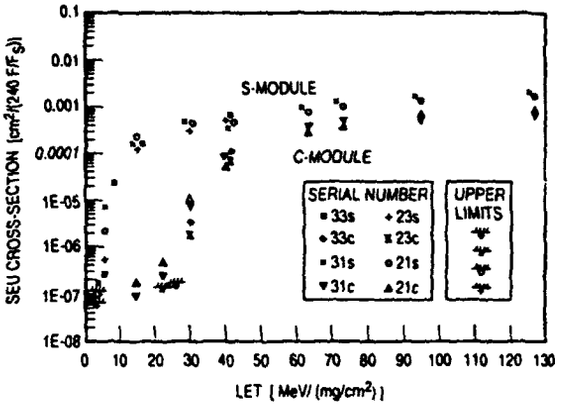

Fig. 3. SEU Test Results for ACT1280

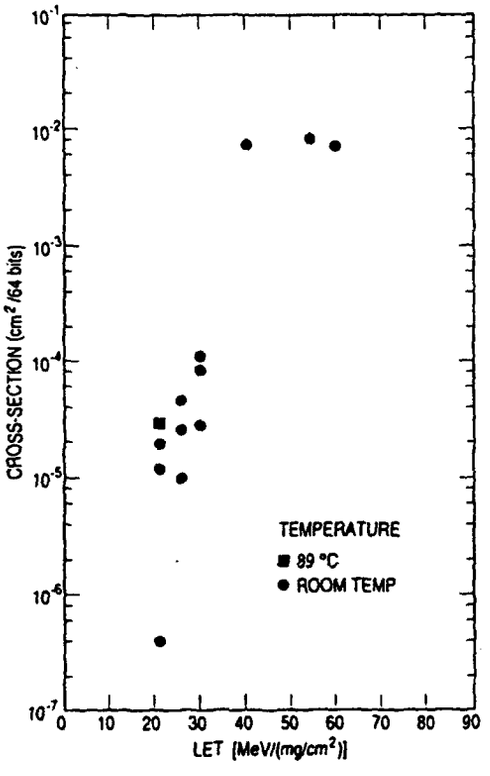

Fig. 4. SEU Test Results for LL7320Q

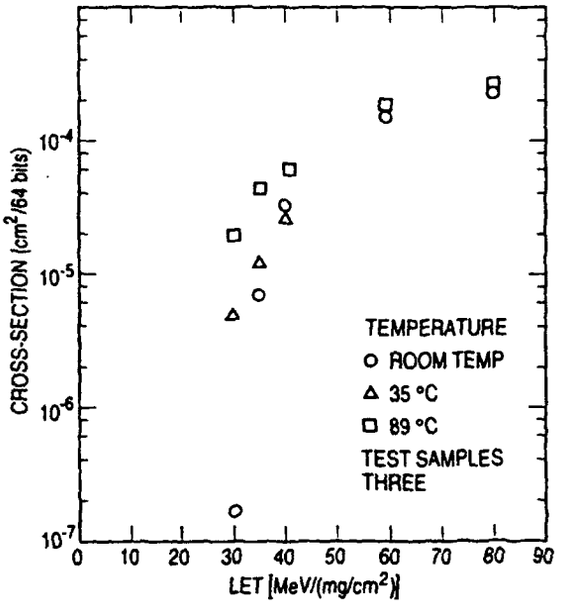

Fig. 5. SEU Test Results for LRH9320Q

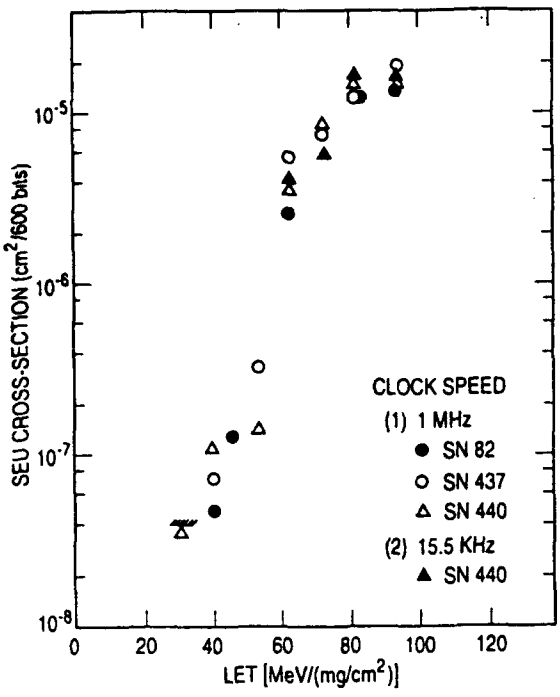

Fig. 6. SEU Test Results for LRH91000

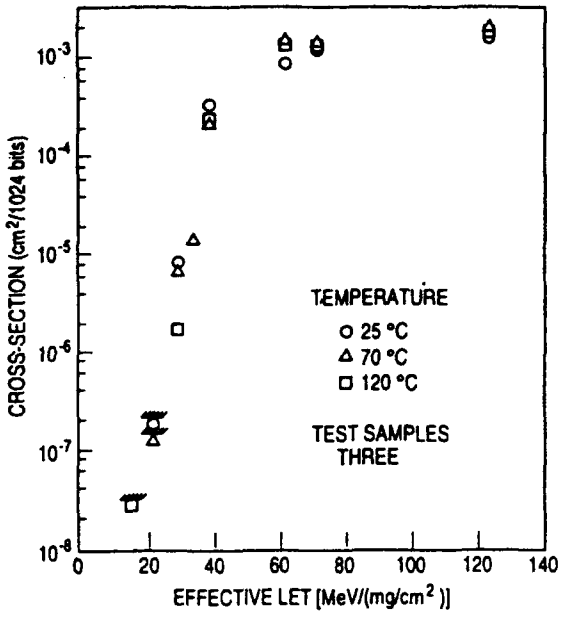

Fig. 7. SEU Test Results for LRH10038Q

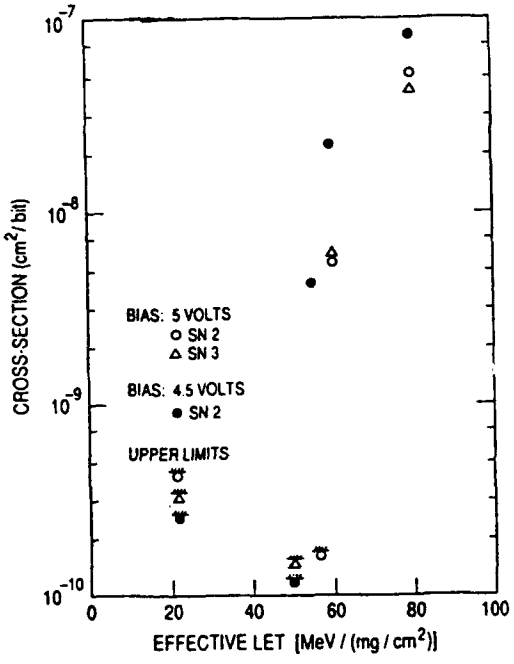

Fig. 8. SEU Test Results for HP03

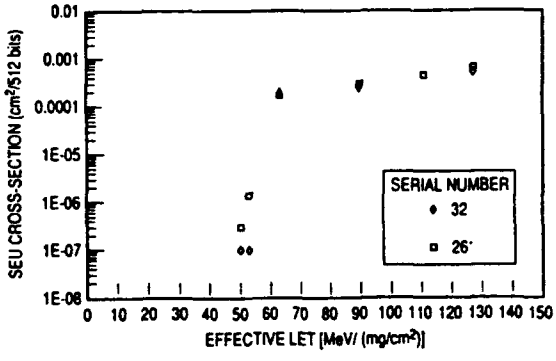

Fig. 9. SEU Test Results for RA20K

L and W values of about 2 and 50 μm, respectively, yields a predicted saturation cross-section of 100 μm^2/transistor for the ACT1010. The SEU saturation cross-section measured for this device was approximately 500 μm^2/(flip-flop), or about 125 μm^2/transistor, which is in good agreement with the predicted value. Similar results were obtained for the ACT1020 FPGA.

The physical properties of a C-module in the ACT1280 are quite similar to those in the ACT1010 and ACT1020. It is not surprising, therefore, that the SEU response of an ACT1280 C-module resembles that of an ACT1010 or ACT1020 C-module. An ACT1280 S-module consists of circuits similar to those in C-modules and extra storage elements. We attribute the low LET threshold of this device to the storage elements. (We have not been supplied with detailed circuit diagrams or layout information for the ACT1280.)

LSI Logic's radiation-hardened LRH9320Q and LRH91000 PPGAs have different memory cell designs and therefore different sensitive regions. The LRH9320Q incorporates a set of rather simple cross-coupled inverters, as shown in Fig. 11. This device is susceptible to SEU only when the clock pulse (CP) is logical "low." In this condition the off-state p- and n-channel drains (in the inverters) are sensitive. When CP is "high" the inverters are driven by the input signal and the latch is not sensitive to SEU. In contrast, the LRH91000 is constructed of master-slave shift registers (D flip-flops), as shown in Fig. 12. Each latch consists of cross-coupled NAND gates (a single NAND gate is shown in Fig. 13). For this device the two sections (master and slave) are alternately susceptible, depending upon the level of the clock pulse: when the clock pulse is "high" the master section is sensitive and when the clock pulse is "low" the slave section is susceptible. Each cross-coupled NAND gate has a higher capacitance load for the output transistors, which makes it difficult to upset.

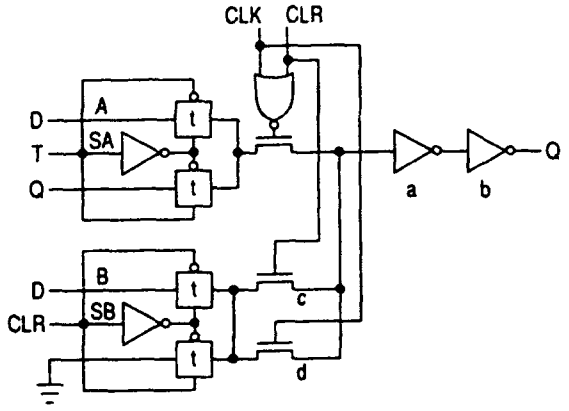

Fig. 10. Actel Module Programmed as Latch
During normal operation, CLR is "low" and T is "high." In this state the module is susceptible to SEU when CLK is "low"; when CLK is "high" the module is in the "driven" state and is therefore essentially immune to SEU. The SEU sensitive regions are located at the drains of the off-transistors in the two inverters (a and b) and the off-transistors at c and d.

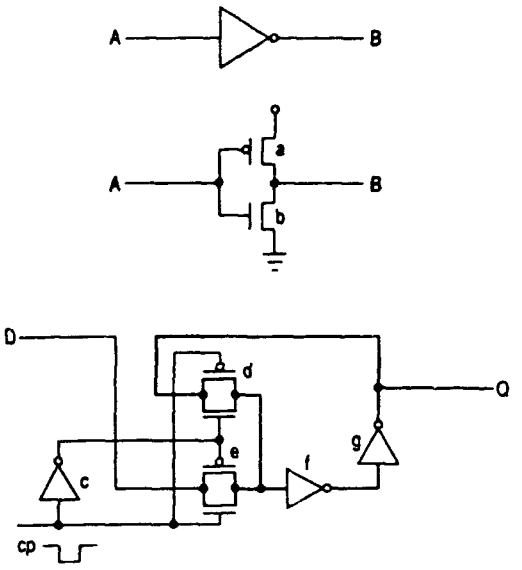

Fig. 11. Sensitive Transistors in Simple D Latch
The cross-coupled inverters combine to store a single bit of information. Each inverter (top figure) consists of two transistors (middle figure). The bottom figure shows the cross-coupled inverters while the clock pulse is "low." When the clock pulse becomes "high," the Q output is driven by the input and the latch is essentially SEU immune.

The remaining radiation-hardened LSI Logic PPGA, the LRH10038Q, is made up of standard 6-transistor SRAM cells, each of which consists of a four transistor flip-flop and two address transistors. In a standard CMOS cell there are two sensitive regions, located at interior nodes [4].

The UTMC HP03 PPGA stores information while CP is "high" (see Fig. 14). When Q is "high" transistors j, l, and m are susceptible, and when Q is "low" transistors i, k, and p are susceptible.

For RA20K, the master and slave sections are alternately susceptible, depending on the level of the clock pulse, as shown in Fig. 15. The memory cell structure of this device is very similar to that of the LRH91000 (cf. Fig. 12).

SEU Reduction and Tolerance

One method for reducing the SEU susceptibility of ASIC devices is based on the fact that memory elements can be created using many different types of bistable circuits, and the observation that the different types display a range of SEU susceptibilities. For example, the D flip-flop shown in Fig. 12 has a much greater tolerance to SEU than does the D latch shown in Fig. 11. Once the susceptibilities of various bistable circuit types have been determined, the more SEU tolerant of them can be chosen for use in critical areas. Of course, device designers will need to balance any possible reduction in SEU susceptibility against other factors, such as complexity, power and speed considerations.

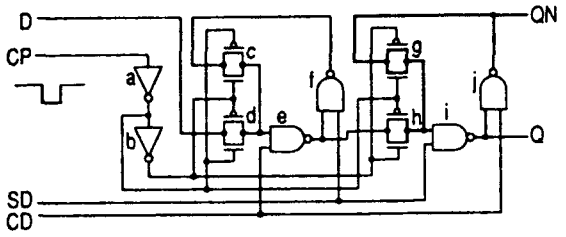

Fig. 12. Sensitive Regions in Master-Slave Shift Register
The locations of the SEU sensitive regions depend on the clock level. While the clock pulse (CP) is "high," the SEU sensitive regions are located in the cross-coupled NAND gates e and f (in the master portion of the register). Gates i and j (in the slave portion) become sensitive only when CP is "low."

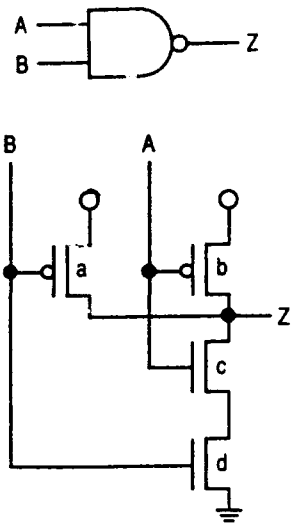

Fig. 13. Transistor Structure of NAND Gate in Master-Slave Shift Register

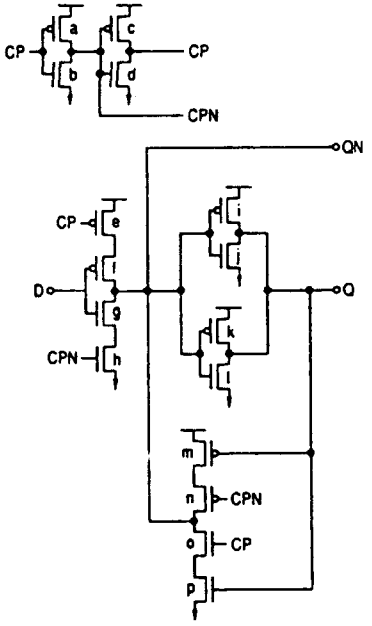

Fig. 14. UTMC HP03 PPGA Memory Element
When the clock pulse (CP) is "low" the D input drives the rest of the circuit thereby determining the state of the Q output. Once the clock pulse becomes "high," the information is stored in the cross-coupled inverters. One inverter consists of transistors i, j, k, and l, while the other consists of m, n, o, and p.

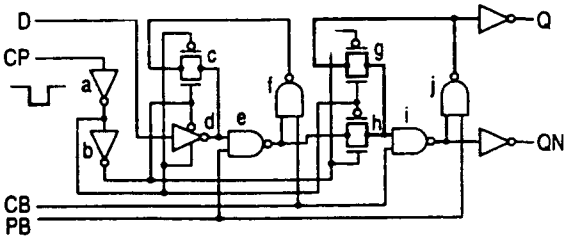

Fig. 15. Sensitive Regions in Master-Slave Shift Register
The locations of the SEU sensitive regions depend on the clock level. While the clock pulse (CP) is "high," the SEU sensitive regions are located in the cross-coupled NAND gates e and f (in the master portion of the register). Gates i and j (in the slave portion) become sensitive only when CP is "low."

Because of the high density of programmable modules in gate arrays, simple error detecting and correcting (EDAC) circuits can easily be incorporated into FPGA and PPGA designs. For example, triplets of flip-flops can be programmed to perform redundant operations in parallel, with an additional circuit to calculate the "majority vote" of their outputs. An erroneous output resulting from the upset of any single flip-flop can thereby be effectively corrected (actually, ignored). In other words, designers can easily integrate on-chip SEU protection (fault-tolerance) into memory circuit designs.

In a secondary test, majority vote programming of Actel FPGAs produced a dramatic (approximately two orders of magnitude) decrease in the efficacy of SEU to cause output errors. Because BASACS monitors device outputs exclusively, this decrease appears as a reduction in the measured SEU rate.

Discussion

Table 4 compares the SEU susceptibilities of gate arrays with those of high-speed (HC) and advanced (AC) CMOS device types. As shown in this table, the SEU susceptibilities of HC CMOS devices and Actel FPGAs (C-modules only) are very similar, and greater than those of either AC CMOS devices or PPGAs [5,6]. The threshold LET values obtained for PPGAs (excluding LSI Logic's LL7320Q and LRH9320Q) and AC devices are also very similar, but the saturation cross-section is about an order of magnitude smaller for the gate arrays. In any case, the SEU tolerance of the gate arrays is at least as great as that of HC and AC CMOS devices, and in the case of PPGAs the SEU tolerance is much greater. Thus it appears that electronics systems based on gate arrays will, in general, provide greater SEU tolerance than equivalent systems constructed from large numbers of SSI and MSI microcircuits.

While PPGAs appear to be more SEU resistant than FPGAs, they also tend to be a bit more difficult to program. Because of this, a preliminary step might be to replace SSI and MSI component circuits with FPGAs. If further reductions in SEU susceptibility are needed, selected PPGAs should be used to replace either SSI and MSI based circuits or FPGAs.

Finally, it should be noted that the probability of latchup appears to be vanishingly small for gate arrays fabricated with an epitaxial layer.

Conclusion

We tested several ASIC device types (FPGAs, PLDs, PPGAs) for SEU and latchup susceptibility. Our findings may be summarized as follows. The SEU tolerance of the Actel FPGAs is roughly comparable to that of HC and AC CMOS devices; the PPGAs we tested exhibited even greater SEU tolerance. The FPGAs and PPGAs fabricated in epitaxial-layer CMOS technology were essentially immune to latchup, whereas the non-epi PPGAs and PLDs latched-up frequently.

The advantages offered by ASIC devices over traditional multi-component circuits are not limited to the reduced size and power consumption of the ASIC devices, but also extend to considerations of the system's tolerance to SEU. Our results indicate that in many cases a significant reduction in SEU susceptibility can be achieved by replacing multiple AC or HC CMOS devices with a single gate array (FPGA or PPGA). SEU tolerance can be further increased through intelligent design methods such as incorporating redundancy into critical circuits. The large number of modules in ASIC devices and the ease with which they may be programmed make designing such fault-tolerant systems relatively simple.

Table 4. Comparison of SEU Susceptibilities of Several Technologies

Technology	LET_{Th}	S_{Sat}
CMOS/HC	25	$(10^{-6} - 10^{-5})$
CMOS/AC	50	$(10^{-7} - 10^{-5})$
Actel FPGA†	25	5×10^{-6}
PPGA	45	$(10^{-8} - 10^{-6})$

† S-modules are not included.
LET_{Th} is measured in MeV/(mg/cm^2);
S_{Sat} is measured in cm^2/bit [5,6].

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