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# Temperature Dependence of Single-Event Burnout in N-Channel Power MOSFETs

15 March 1994

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## CONTENTS



## FIGURES

# TEMPERATURE DEPENDENCE OF SINGLE-EVENT BURNOUT IN N-CHANNEL POWER MOSFETs †

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*ABSTRACT*

The temperature dependence of single-event burn out (SEB) in n-channel power metal-oxide-semiconductor field effect transistors (MOSFETs) is investigated experimentally and analytically. Experimental data are presented which indicate that the SEB susceptibility of the power MOSFET decreases with increasing temperature. A previously reported analytical model that describes the SEB mechanism is updated to include temperature variations. This model is shown to agree with the experimental trends.

## I. INTRODUCTION

It has been known for some time that single-event burnout (SEB) of power metal-oxide-semiconductor field effect transistors (MOSFETs) is a catastrophic failure mode that can be triggered by the passage of a single heavy ion through the device [1]. This phenomenon is of concern to space-born system designers since heavy ions are ubiquitous in the space-radiation environment [2]. In addition, the broad range of temperatures that may occur on board a system in flight necessitates an investigation of the temperature dependence of the SEB mechanism.

Power MOSFET burnout has been attributed to the turn-on of the parasitic bipolar-junction transistor (BJT), inherent to the double-diffused metal oxide semiconductor (DMOS) structure, when the power MOSFET is turned off (blocking a large drain-source bias) [3]. Previous burnout modeling has been performed for an ambient device temperature of 300 K. This paper reports the temperature dependence of the burnout mechanism in n-channel power DMOS devices.

Observation of SEB in p-channel power MOSFETs has not been reported in the literature. It is believed that the much lower impact-ionization rate for holes than electrons is responsible for the apparent hardness to SEB seen in p-channel power MOSFETs [3]. For this reason, the temperature dependence of SEB in p-channel devices will not be presented in this paper.

The non-destructive burnout experiment method, with a means to control the ambient temperature of the device, was performed on IR6766 and IRF150 power MOSFETs. The SEB cross-section was measured as a function of drain-source voltage and temperature. The temperature was varied from 300 K to 373 K. Due to the difficulty (or impossibility) of cooling devices within the experimental chamber, only temperatures at and above room temperature are investigated herein. The experimental results indicate that the burnout susceptibility of a given device decreases with increasing temperature for a given applied drain-source voltage.

The details of the testing technique are given in Section II. The experimental results are presented in Section III. The burnout mechanism for the power DMOS device structure is reviewed, and the temperature dependence of the model is discussed in Section IV. The temperature dependence of the SEB threshold is then calculated for a typical DMOS device in Section V. Finally, conclusions are given in Section VI.

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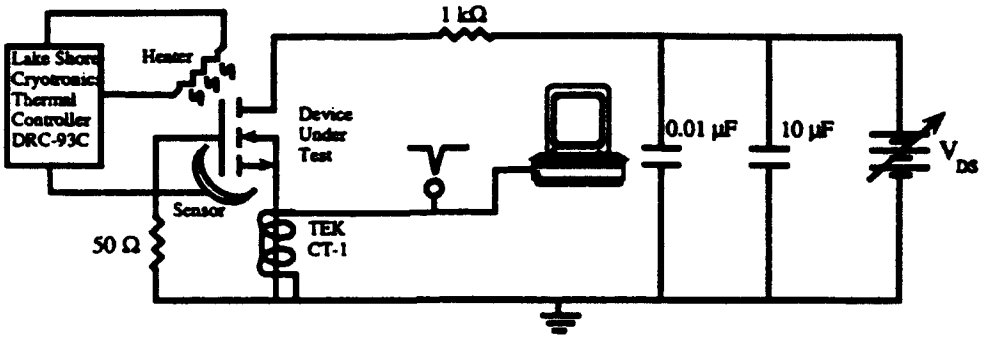


Figure 1: Non-destructive, temperature controlled SEB test set-up.

## II. Burnout Experiment

The IR6766 and IRF150 n-channel power MOSFETs with breakdown voltages, $BV_{DS}$, of 200 V and 150 V, respectively, were subjected to heavy ion bombardment in the 88-inch cyclotron facility at Lawrence Berkeley Laboratories. A monoenergetic beam of 380 MeV Kr ions at a fixed LET of 41 MeV-cm²/mg was used to characterize the devices. The devices were de-lidded prior to heavy ion exposure. Each test was performed until a total fluence of $10^7$ ions/cm² was obtained, or an error of ~ 100 pulses were counted.

The ambient device temperature was maintained using the Lakshore Thermal Controller DRC-93C. The temperature controller consisted of a resistive heater and thermal sensors connected in a feedback loop. The heater and sensors were attached directly to the TO-240 package of the device under test, (DUT). It was determined that if the temperature was allowed to equilibrate for several minutes, the temperature was very uniform across the surface of the chip. This provided a reliable indication of the device temperature.

The non-destructive burnout test method was used in order to obtain SEB cross-sections for a given device type [4, 5]. The non-destructive test technique employs a current limiting resistor in the drain lead of the DUT so that the drain-source current can not rise sufficiently to induce second breakdown of the parasitic bipolar transistor and consequently burnout. The current-limited pulses were monitored at the drain terminal of the DUT using a Tektronix TEK-CT1 current transformer. SEB cross-section measurements were made by varying the applied drain-source voltage, since the SEB cross-section increases with increasing drain-source voltage. The SEB cross-section was found by the usual method of dividing the total number of nondestructive current pulses per device by the beam fluence to yield units of cm²/device. The experimental test set-up is shown in Figure 1.

## III. Experimental Results

SEB cross-section measurements were obtained for the devices at device temperatures of 300 K, 333 K, 353 K, and 373 K. The cross-section versus drain-source voltage for the IR6766 and IRF150 are shown in Figures 2 and 3, respectively. In each case, the $V_{DS}$ threshold for burnout increases with increasing temperature. Also note that in each case, for a given applied drain-source voltage, the SEB cross-section decreases with increasing temperature. Furthermore, as the drain-source bias

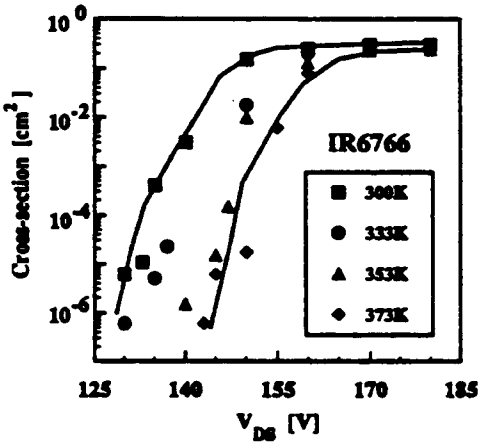


Figure 2: SEB Cross-section versus $V_{DS}$ and temperature for the IR6766 power MOSFET (solid lines drawn to guide the eye).

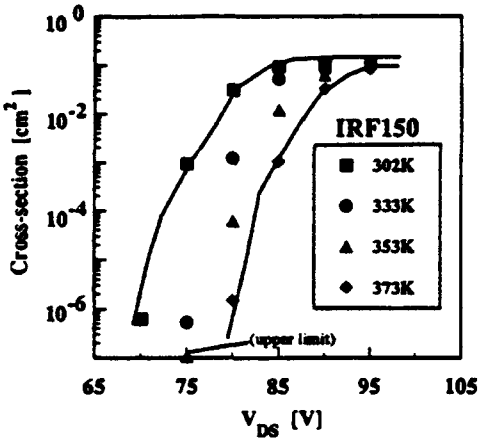


Figure 3: SEB Cross-section versus $V_{DS}$ and temperature for the IRF150 power MOSFET (solid lines drawn to guide the eye).

increases, the amount of change in the cross-section decreases. In other words, the burnout susceptibility decreases with increasing temperature, and the change in burnout susceptibility due to temperature decreases with increasing drain-source bias. This can be explained physically through the dependence of the impact ionization rate for electrons on temperature and electric field. The impact ionization rate for electrons decreases with increasing temperature and decreasing electric field. The data presented in Figures 2-3 are consistent with previously reported data [6]. These points and their relevance to the SEB mechanism will be explained in more detail in the next section.

## IV. Burnout Modeling

This section will focus on the physical model of the burnout mechanism. First, the mechanism leading to burnout via the turn on of the parasitic bipolar transistor will be reviewed. Next, the manner in which temperature dependence is incorporated into the model will be discussed.

### *IVA. Burnout Mechanism of DMOS Structure*

The cross-section of one cell in an n-channel DMOS power transistor is shown in Figure 4. A positive bias applied to the gate forms an inversion layer in the p-body region below the gate oxide, allowing electrons to flow from the source to the drain. Inherent to the DMOS structure is a parasitic npn bipolar transistor, as shown in Figure 4. The source, body, and drain regions of the MOSFET comprise the emitter, base, and collector regions of the parasitic BJT, respectively. In normal operation of the power MOSFET, this parasitic BJT is always turned off. This is accomplished by the common source-body metallization, which shorts out the base-emitter junction of the parasitic BJT.

If lateral current flows in the body (base) below the source (emitter) region, the base-emitter junction becomes forward biased and the parasitic BJT turns on. Single-event burnout of the DMOS structure has been attributed to the turn on of this parasitic BJT [3]. If the parasitic BJT is turned *ON* when the MOSFET is turned *OFF*, second breakdown of the BJT and hence thermal meltdown (burnout), may occur. The mechanism leading to SEB will now be discussed.

Figure 4 shows the DMOS structure with a heavy ion passing through the parasitic BJT. As the heavy ion traverses the device, electron-hole pairs are generated along its track length, creating an ionized plasma filament. This plasma filament supports a short-lived current source in which holes flow up towards ground via the lateral base region, and electrons flow down towards the positively biased collector. The short-lived current source initially drives the parasitic BJT, locally turning on one cell of the DMOS structure [7].

Depending on how 'hard' the BJT is initially turned *ON*, the currents within the device will either regeneratively increase until burnout occurs, or the currents will die out leaving the

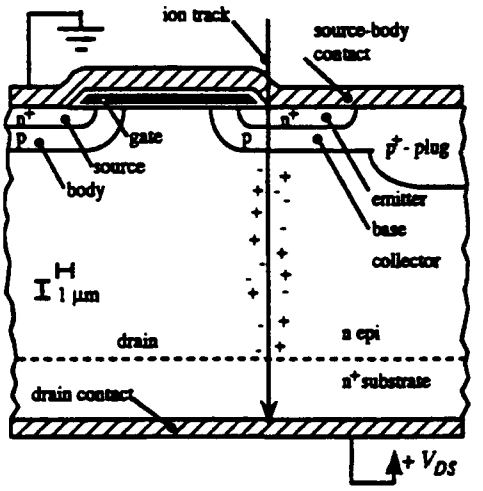


Figure 4: DMOS structure showing parasitic BJT and ion track.

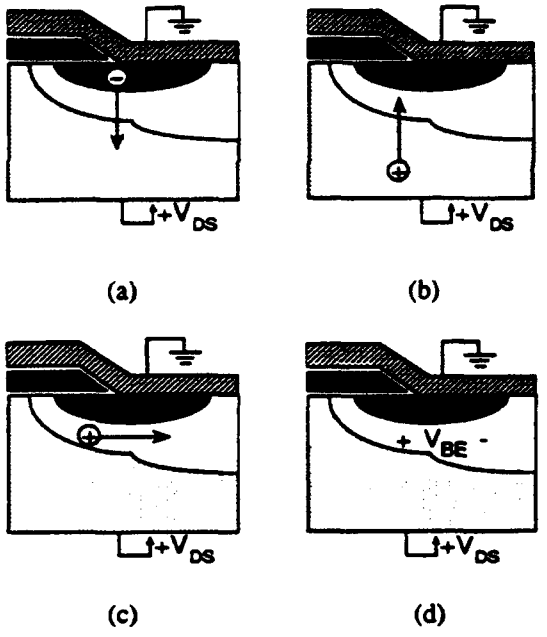


Figure 5: Components in feedback mechanism: (a) electron injection; (b) avalanche generated holes; (c) base current; (d) base-emitter voltage.

device unharmed. A feedback mechanism inherent to the vertical structure of the parasitic BJT will determine whether the currents will regeneratively increase or die out. The feedback mechanism consists of four basic components. These components in terms of the parasitic BJT are: (1) electron injection from the emitter across the active base into the collector; (2) avalanche-generated hole current returning from the collector into the base; (3) subsequent lateral hole current through the base to its contacts; and (4) the induced base-emitter voltage resulting from the lateral base current. The four components of the feedback mechanism are illustrated in Figure 5.

When the equations governing the feedback mechanism are solved, electron and hole current density distributions within the parasitic BJT are obtained which define the threshold for burnout [8]. The current density distributions at the threshold for burnout are called the critical condition. If the parasitic BJT is initially driven by the heavy-ion-generated current source such that currents are larger than the critical condition, then burnout occurs. If not, then the currents within the parasitic BJT die out and burnout does not occur [8].

It should be noted that in this model it seems that the position of the incident ion strike may influence how hard the parasitic BJT is driven. Incidence at the outer edge of the source region is worst case in the sense that an incident ion with the lowest LET capable of initiating burnout must strike there. At the source edge, an incident ion with a relatively low LET may induce burnout, but the same ion could not induce burnout if it were incident closer to the ground edge of the source. As one moves to positions more interior in the source region, incident ions must have higher and higher values of LET to initiate burnout. Positions more interior in the source region correspond to larger effective sensitive regions. Experimental cross-section versus LET curves show a similar trend. As the LET of the incident ion is increased, the measured cross-section increases. This same argument can be made with the cross-section versus drain-source bias curves for a constant LET that are given in this paper. As the drain-source bias is increased, an ion with the same LET can strike futher into the source region and still initiate burnout. Thus, as the drain-source bias increases, so does the sensitive region.

The temperature dependence of the burnout mechanism can be readily introduced into this feedback mechanism and will now be outlined.

### *IVB. Temperature Dependence*

In the foregoing discussion, it should be emphasized that the primary component of the burnout mechanism is the base current density flowing in the parasitic BJT. In order for the parasitic BJT to turn on and remain turned on, it must have a source of base current. Unlike 'normal' BJT operation, the base current is not supplied from a device terminal; rather, the base current is supplied through avalanche multiplication in the base-collector space charge region (SCR). It will later be shown that the hole current generated in the base-collector SCR is a function of the doping density and thickness of the collector region, the applied drain-source bias, and the local injected electron density [8]. In the following discussion on the temperature dependence of the burnout mechanism, the focus will be on the base current generated through avalanche multiplication. In other words, the injected electron density will be held 'constant' as a function of temperature, and the change of avalanche generated holes will be

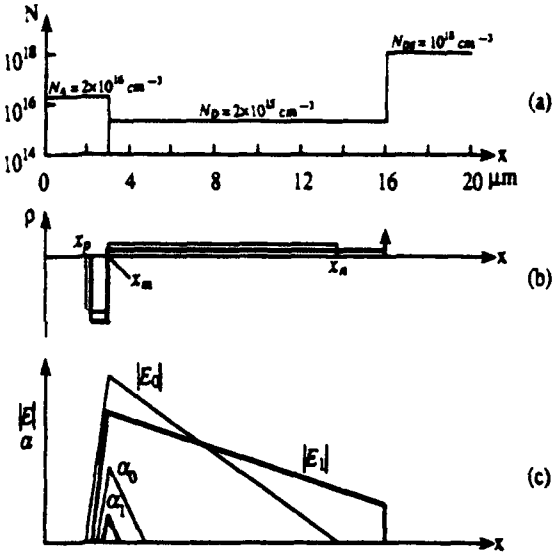


Figure 6: (a) idealized doping densities in base-collector space charge regions; (b) charge densities for zero and nonzero currents; and (c) electric field and impact ionization rate profiles for zero and nonzero currents.

monitored as a function of temperature. This is equivalent to accounting for the 2-3mV/°C decrease of base-emitter voltage in the parasitic BJT.

As mentioned previously, the avalanche generated hole current is a function of the doping density and thickness of the collector region, applied drain-source voltage, and the local injected electron density within the base-collector space charge region. The complete details for calculating the avalanche generated hole current appear in [8]. Only the major points will be described here.

The one dimensional Poisson equation is solved across the base collector depletion region taking into account the space charge associated with the mobile carriers. When the space charge of the mobile carriers is considered, the electric field across the base collector space charge region will be somewhat altered, depending on the density of mobile charge compared to the density of background impurity charge. A qualitative illustration of how the electric field is changed is shown in Figure 6 [8]. An idealized impurity profile through the base, collector, and substrate of the parasitic BJT in a typical power MOSFET is shown in Figure 6a. The two cases of zero and non-zero current are depicted in Figures 6b and 6c. The light lines correspond to the zero current case, and the heavy lines correspond to the non zero current case. The electric field and ionization rate plots are further labelled with the subscripts 0 and 1 to distinguish between zero and non-zero currents respectively. The total charge density for the non-zero current case, shown in Figure 6b, has changed to reflect the electrons in transit across the junction. The total charge density to the left of the metallurgical junction, $x_m$, is more negative (the electrons add to the total charge), and the total charge density to the right of the metallurgical junction is less positive than for the zero current case (the electrons subtract from the total charge).

The change in the total charge density is also reflected in the electric field distribution, shown in Figure 6c. Since the total charge density is more negative to the left of $x_m$ for non-zero current, the electric field in this region will have a steeper slope than for the zero current case. This effectively lowers the peak electric field at $x_m$ and moves $x_p$ to the right. Similarly, since the total charge density is less positive to the right of $x_m$ for non-zero current, the electric field in this region will have a lower gradient than for the zero current case. Since the reverse bias for each case is the same, the area under each electric field plot must be equal. This equal area constraint and the lower slope to the right of $x_m$, push the right edge of the electric field, $x_n$, deeper into the collector region. In the example shown in Figure 6c, $x_n$, has reached the epi-substrate boundary at which point the electric field can penetrate no further. The electric field will assume a non-zero value at the epi-substrate boundary to satisfy the equal area constraint imposed by the boundary conditions of the Poisson equation. Therefore, two important phenomena occur in the reverse biased base collector junction when non-zero current flows: (1) the peak electric field at the metallurgical junction decreases, and (2) the electric field assumes a non-zero value at the epi-substrate interface. These two consequences significantly affect the avalanche multiplication, as will be shown later.

The impact ionization rate, $\alpha$, throughout the depletion region for zero and non-zero current is also shown in Figure 6c. The impact ionization rate, $\alpha$, is exponentially related to the local electric field [8]. This is why the value of $\alpha$ decreases significantly when the peak electric field drops with increasing current. The avalanche multiplication rate, $M$, significantly decreases with increasing current as well. The functional relationships between carrier densities, electric field, ionization rate, applied

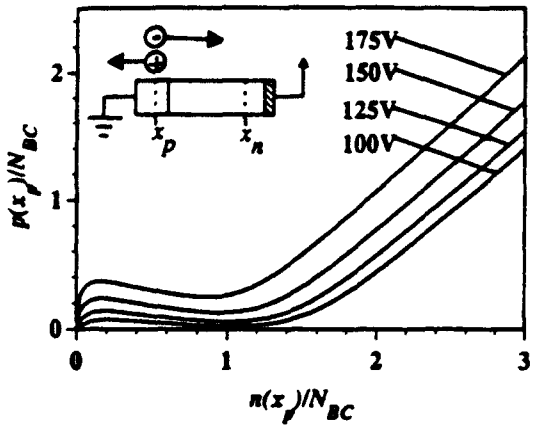


Figure 7: Avalanche curves at 300K for 100 V, 125 V, 150 V, and 175 V for device with nominal breakdown voltage of 190 V.

voltage, and the physical geometry of the parasitic BJT must be simultaneously solved to determine the avalanche multiplication rate, i.e., the density of avalanche generated holes returning to the neutral base for a given injected electron density.

Recall that the desired result is the hole concentration at $x_p$, $p(x_p)$, as a function of electron concentration at $x_p$, $n(x_p)$, or:

$$M = \frac{p(x_p)}{n(x_p)} \qquad (1)$$

There are six arrays of typically 300 points used in the calculation (the depletion region is discretized into 300 points). These arrays are: (1) space charge, $\rho(x)$; (2) electric field, $E(x)$; (3) potential, $V(x)$; (4) ionization rate, $\alpha(x)$; (5) electron concentration, $n(x)$; and (6) hole concentration, $p(x)$. Given the impurity profile, the applied drain to source voltage, $V_{DS}$, and the electron concentration at $x_p$, the profiles of $\rho(x)$, $E(x)$, $V(x)$, $n(x)$, $p(x)$, and $\alpha(x)$ are calculated for self-consistency [8].

The equations, sample calculations of electric field, ionization rate, potential, carrier densities, and other details of this calculation appear in [8]. The end result is plotted in Figure 7, which shows the calculated avalanche curves for a device with a nominal $BV_{DS}$ of 190 V. There are three distinct regions present in each avalanche curve shown in Figure 7. The first region is the distinct hump appearing for values of $n(x_p)/N_D < 1$. This corresponds to an initial decrease in the avalanching rate with increasing current. The second region is the valley region or local minimum appearing for values of $n(x_p)/N_D \approx 1$. This corresponds to a near zero avalanching rate at a current level where the injected electron density and collector doping density are comparable. The third region of the avalanche curve appears for values of $n(x_p)/N_D > 1$, where the hole concentration increases at approximately the same rate as the electron concentration.

In terms of the feedback mechanism for SEB, the appropriate value for $M$ can be obtained from a curve similar to Figure 7. Note that it is necessary to calculate a separate avalanche curve for each device structure and each applied drain-source bias when solving the equations governing the feedback mechanism.

The temperature dependence is included in the aforementioned calculation via the impact ionization rate. The impact ionization rate (number of electron-hole pairs generated per unit path length) decreases with increasing temperature [9]. This is attributed to the shorter mean free path of the carriers. Since the impact ionization rate is used explicitly in the solution to the Poisson equation, the avalanche-generated hole current density decreases with increasing temperature for the same injected electron current density and applied drain-source bias. A measure of the reduction in hole current density is shown in Figure 8. The ratio of the hole density returning to the base at 400 K, $p_{400}$, and the hole density at 300 K, $p_{300}$, is plotted as a function of the electron density, $n$, injected into the base-collector space charge region of the parasitic BJT. The electron density has been normalized to the doping density in the collector, $N_D$. Note that the hole density at 400 K ranges from 30% to 90% of the hole

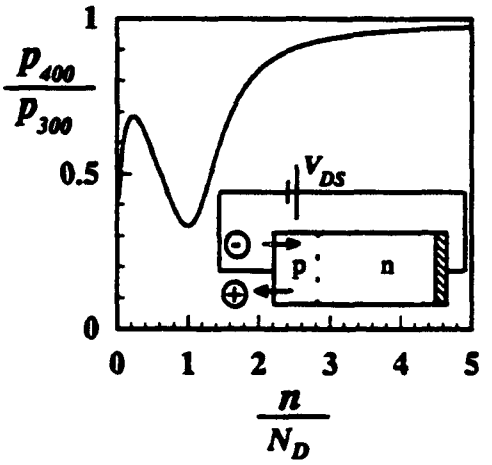


Figure 8: Ratio of avalanche curves at 400 K and 300 K.

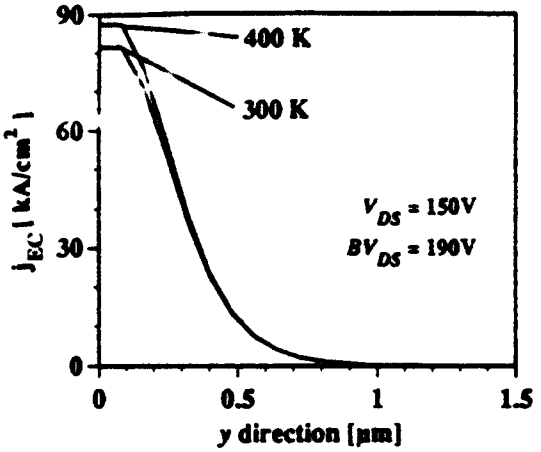


Figure 9: Critical electron current density distribution in the collector at the threshold for burnout with drain-source bias of 150 V at 300 K and 400 K.

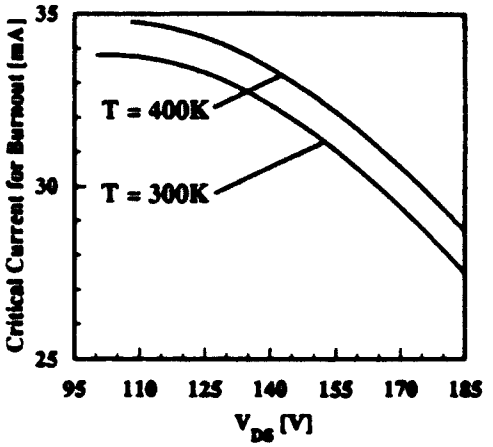


Figure 10: Calculated SEB threshold as a function of temperature and drain-source bias.

density at 300 K over much of the operating region. This reduction of the source of base current at higher temperatures is equivalent to an increase of the burnout threshold of the device (ie, in order to achieve the same level of base current, the electron current density in the collector must increase). The calculated temperature dependence of the burnout threshold will be presented in the next section.

## V. Calculated Temperature Dependence

The relationships governing the feedback mechanism can be solved to yield a collector current density distribution at the threshold for burnout, $j_{EC}$, for a given DMOS device structure [8]. Figure 9 shows the threshold $j_{EC}$ plotted against position in the parasitic BJT for temperatures of 300K and 400K. These calculations indicate that the peak $j_{EC}$ increases from 81.5 kA/cm$^2$ to 87.5 kA/cm$^2$ when the temperature increases from 300K to 400K. When the critical collector current density is integrated around one cell of the DMOS structure, a critical collector current for burnout is obtained. The critical collector current for burnout, calculated as a function of drain-source voltage and for ambient temperatures of 300K and 400K, is plotted in Figure 10. The device structure used in these calculations has a nominal breakdown voltage of 190V. The device structure used in the calculations is similar to the experimental samples only in the sense that they each have similar values of $BV_{DS}$. No attempt was made to determine actual dimensions and doping distributions of the experimental samples. For the calculations, the average doping densities in the source, p-body, p$^+$-plug, and drain region are $10^{21}$ cm$^{-3}$, $2\times10^{17}$ cm$^{-3}$, $2\times10^{19}$ cm$^{-3}$, and $2\times10^{15}$cm$^{-3}$, respectively. The thickness of the drain region is 13 μm. As shown in Figure 10, the SEB threshold increases with increasing temperature and decreasing voltage. Note that an increase of the critical current increases the SEB threshold. Furthermore, the increase of the SEB threshold is more pronounced at the lower drain-source biases. Once again, this is a result of the temperature and electric field dependence of the impact ionization rate for electrons. Therefore, the SEB threshold has increased by approximately 2.9% for a 100 degree temperature increase at the higher drain-source biases, and the SEB threshold has increased by approximately 4.4 % at the lower drain-source biases. These results are consistent with the experimental trends previously discussed.

## VI. Summary and Conclusions

In this paper, the temperature dependence of SEB in power DMOS devices was discussed. Experimental data for the IR6766 and IRF150 power MOSFETs were presented. The data indicate a definite temperature dependence of the burnout cross-section and in the threshold value of drain-source bias required for burnout. Temperature dependence was included in an existing SEB model through the impact ionization rate, and the

calculated results agreed with the experimental trends.

From the results presented in this paper, one can conclude that power DMOS devices are more resistant to SEB when operated at an elevated temperature. This is an important issue for systems that may be operated outside of the 300 K regime in the space radiation environment.

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## TECHNOLOGY OPERATIONS

The Aerospace Corporation functions as an "architect-engineer" for national security programs, specializing in advanced military space systems. The Corporation's Technology Operations supports the effective and timely development and operation of national security systems through scientific research and the application of advanced technology. Vital to the success of the Corporation is the technical staff's wide-ranging expertise and its ability to stay abreast of new technological developments and program support issues associated with rapidly evolving space systems. Contributing capabilities are provided by these individual Technology Centers:

**Electronics Technology Center:** Microelectronics, solid-state device physics, VLSI reliability, compound semiconductors, radiation hardening, data storage technologies, infrared detector devices and testing; electro-optics, quantum electronics, solid-state lasers, optical propagation and communications; cw and pulsed chemical laser development, optical resonators, beam control, atmospheric propagation, and laser effects and countermeasures; atomic frequency standards, applied laser spectroscopy, laser chemistry, laser optoelectronics, phase conjugation and coherent imaging, solar cell physics, battery electrochemistry, battery testing and evaluation.

**Mechanics and Materials Technology Center:** Evaluation and characterization of new materials: metals, alloys, ceramics, polymers and their composites, and new forms of carbon; development and analysis of thin films and deposition techniques; nondestructive evaluation, component failure analysis and reliability; fracture mechanics and stress corrosion; development and evaluation of hardened components; analysis and evaluation of materials at cryogenic and elevated temperatures; launch vehicle and reentry fluid mechanics, heat transfer and flight dynamics; chemical and electric propulsion; spacecraft structural mechanics, spacecraft survivability and vulnerability assessment; contamination, thermal and structural control; high temperature thermomechanics, gas kinetics and radiation; lubrication and surface phenomena.

**Space and Environment Technology Center:** Magnetospheric, auroral and cosmic ray physics, wave-particle interactions, magnetospheric plasma waves; atmospheric and ionospheric physics, density and composition of the upper atmosphere, remote sensing using atmospheric radiation; solar physics, infrared astronomy, infrared signature analysis; effects of solar activity, magnetic storms and nuclear explosions on the earth's atmosphere, ionosphere and magnetosphere; effects of electromagnetic and particulate radiations on space systems; space instrumentation; propellant chemistry, chemical dynamics, environmental chemistry, trace detection; atmospheric chemical reactions, atmospheric optics, light scattering, state-specific chemical reactions and radiative signatures of missile plumes, and sensor out-of-field-of-view rejection.