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Quarterly R&D Status Report No. 2

March 24, 1994

Reporting Period: 19 November 1993 - 18 February 1994

Optoelectronic Processing Component Development

Contractor:

Honeywell Technology Center
10701 Lyndale Ave. S.
Bloomington, MN 55420

ARPA Order No.: unknown

Program Code No.: S216300sro01

Contract No.: N00014-93-C-0138

Effective Contract Date: 19 August 1993

Contract Expiration Date: 31 August 1994

Contract Amount: $400,000

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Honeywell

LETTER OF TRANSMITTAL

23 March 1994

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Contract No: N00014-93-C-0138
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OPTOELECTRONIC PROCESSING COMPONENT DEVELOPMENT

Quarterly R&D Status Report
August 19-November 18, 1993
Honeywell, Inc.

I. Summary of Progress

The goal of the "Optoelectronic Processing Component Development" program is to develop an Optoelectronic Integrated Circuit (OEIC), consisting of electronic logic and optical I/O, as a critical element for computing and processing systems in which two dimensional planes of processing elements are connected in the third dimension Our approach to this OEIC consists of monolithically integrating vertical cavity surface emitting lasers (VCSELs), GaAs ion implanted photodetectors, and GaAs Field Effect Transistor (FET) based electronic logic into a two-dimensional array of "smart pixels". We will be collaborating with one or two groups doing research in the area of computing or processing architectures in order to define the logic functions which would be incorporated into the chips. Chips fabricated under the program would then be provided to these architecture research groups for use in subsequent system experiments. The main challenge to be addressed under this program involves the development of the fabrication techniques required to monolithically integrate these dissimilar devices.

During the first quarter of this program, our effort was concentrated on demonstrating a VCSEL structure which can be monolithically integrated with a GaAs FET based integrated circuit. This structure incorporated a method for forming ohmic contact to both sides of the p-n junction from the top surface of the wafers, as will be required by monolithic integration. The effort carried out in the second quarter, and reported here, was to develop the re-growth and planarization procedure required to produce a planar surface as will be required for high yield I.C. processing.

The approach we are taking to monolithic integration of these dissimilar devices is shown in Figure 1. The epitaxial layers required for the VCSEL are grown first. A large mesa will be etched and epitaxial material will be regrown around this mesa in order to provide the necessary substrate material for the FET devices. The thickness of this regrown material must be controlled accurately in order to maintain wafer planarity. Later, etching of a smaller diameter mesa is carried out to reach an n-type intracavity layer where the n-ohmic metal is deposited. The structure is again planarized with a polyimide layer, and a p-ohmic contact is formed to the top surface of the original VCSEL epitaxial growth.

Experiments to planarize the epitaxial surface have been carried out using both OMVPE and MBE as the epitaxial techniques for the regrown layer. The experiment is carried out by depositing a silicon dioxide masking layer on top of the epitaxial material for the vertical cavity surface emitting lasers. The oxide is patterned with circular dots, and then reactive ion etched down to the substrate. After removing the photoresist, the wafers were returned to the OMVPE or MBE reactor, and a GaAs or AlGaAs buffer layer, followed by a FET layer is regrown. Photomicrographs of the cross-sections of the resulting structures are shown in Figures 2 and 3. Single crystal material has grown on the exposed substrate regions, while polycrystalline material grows as expected on the surface of the nitride mask. The following paragraphs will discuss the observations of the morphology after re-growth for these two cases.

Figure 2 contains a micrograph of a mesa from the sample where the re-growth was carried out using OMVPE. The silicon dioxide mask which protected the VCSEL mesa is clearly

visible, and it can be seen that polycrystalline material grew on top of it. However, single crystalline material grew around the mesa. It can be seen that the thickness of the regrown layer is well matched to the thickness of the original mesa. The polycrystalline material on top of the dielectric can be easily removed. The only challenging aspect will be to remove the excess material which extends over the edge of the dielectric where there is no natural etch stop. The difficulty will be in removing this material without overetching and creating a trough next to the mesa.

Figure 3 contains a micrograph of the region surrounding a mesa after MBE was used to regrow material around the mesa. Again, the material which is deposited on top of the silicon dioxide mask protecting the VCSEL mesa appears polycrystalline. However, a somewhat different morphology appears than in the case of the OMVPE regrowth. In the MBE case, a trench has appeared around the edge of the mesa which is about 3μm deep. Next to this trench (at a larger diameter), the growth rate appears to be slightly enhanced (1-2μm) when compared to the growth rate in an open area. We must determine whether these variations in planarity are large enough to create problems during subsequent processing, or whether they can eliminated or reduced during the planarizing step which removes the polycrystalline material.

An initial planarization experiment has been carried out on a sample with an MBE regrown layer. The results are illustrated in Figure 4. In this particular case, the regrown thickness was not well matched to the original mesa height, due to a programming error for the MBE reactor. However, the results are still illustrative of what one might expect.
The sample was processed by spinning a self-levelling polymer onto the sample. After etching away some of this polymer, protrusions from the surface, such as the polycrystalline material on top of the mesas, is left exposed, while the rest of the surface is still protected by polymer. We then used reactive ion etching to remove the polycrystalline material from the surface of the mesa, with the silicon dioxide acting as an etch stop layer. As can be seen from Figure 4, we are left with a smooth surface on the mesa top. However, some polycrystalline material remains on the sidewall of the mesa. In addition, the trench around the edge of the mesa still remains after this process. However, assuming the regrown thickness had been correct to begin with, we would have reduced a potential non-planarity of 6.5μm down to one with a maximum magnitude of around 3μm.

Although we have performed initial experiments in replanarization, additional work will be carried out during the next quarter to replanarize samples regrown with both OMVPE and MBE material. In addition, we hope to evaluate the quality of the regrown material by fabricating and testing FETs during the next quarter. Although there appear to be advantages with the OMVPE regrown layer in terms of the planarity which can be achieved, using MBE for the regrown layer has the advantage that we have previously optimized the growth of FET layers in MBE and could leverage off this previous work. After the experiments to be carried out next quarter, i.e. the replanarization experiments and the evaluation of FETs fabricated in re-grown material, we should be in a better position to make a choice as to the appropriate approach.

II. Changes in Key Personnel.

One change in key personnel has occurred this quarter. Dr. David Grider, who was in charge of the development of the monolithic integration process, has left the company. He will be replaced by Mr. James Nohava. In addition, Honeywell has extended an offer of employment to Dr. Robert Morgan, currently of AT&T. Dr. Morgan, who has been

developing VCSEL technology at AT&T, has accepted and will begin work next quarter. He will be responsible for the design and characterization of VCSEL devices.

III. Summary of Substantive Information Derived from Special Events.

Dr. Mary Hibbs-Brenner and Mr. Richard Schulze, section head for the Photonics group at Honeywell, visited the Honeywell Micro Switch division in early March to discuss a joint project in the development of VCSELs which, if successful, would eventually result in the transfer of this technology from Honeywell Technology Center to Micro Switch. Micro Switch is one of the two largest producers of optoelectronic modules in the United States. While this particular meeting and activity was funded by internal Honeywell resources, it is a direct result of BMDO/ONR and ARPA funding in this and other government contracts.

IV. Problems Encountered And/Or Anticipated.

To date, no technical problems impacting our ability to achieve the end objectives of the contract have been encountered.

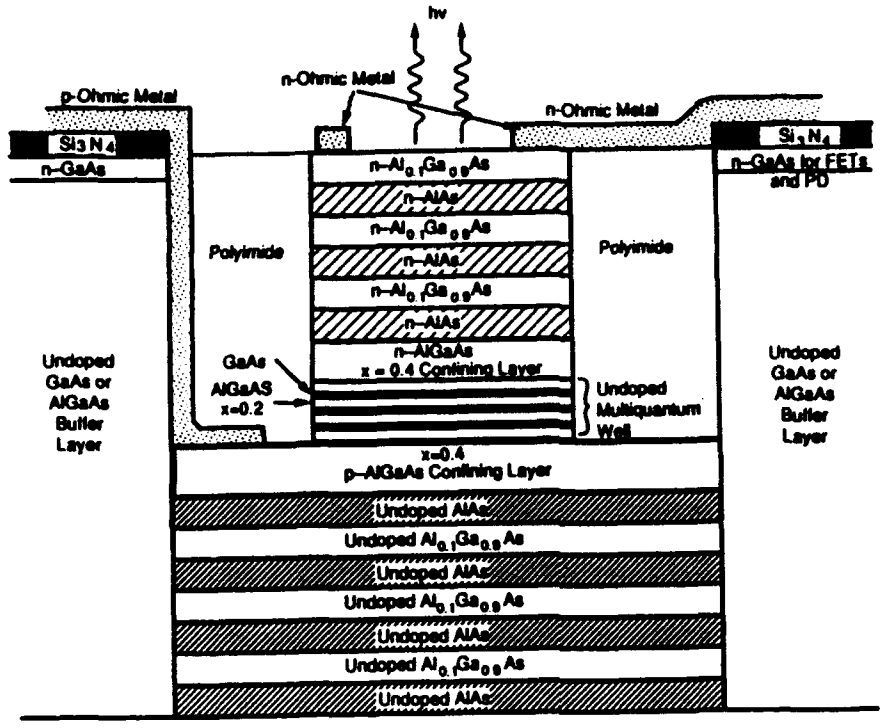
V. Action Required by the Government.

No problems requiring government assistance have been encountered.

VI. Financial Status.

A summary of costs incurred by task may be found in Figure 5. A contract for $400,000 was negotiated. Overall, $250,000 has been authorized to date. As of 2/6/94, actuals plus commitments totalled $196,284. We have submitted the required paperwork to ONR procurement stating that more than 75% of the authorized funding has been expended, and requesting that the next increment of funding be released, but have not yet received that increment of funding.

The contract that was negotiated provided $400K against a statement of work which was valued at around $1.2M (including selected optional tasks). This approach was taken because Honeywell and the local DCAS auditor were anticipating a change in Honeywell rates due to a reorganization of the reserach centers. That reorganization is complete, and DCAS has made a recommendation for rates which is close to those proposed by Honeywell. Honeywell will therefore be submitting a revised proposal for the remainder of the program using our new rate structure.



- Separate epitaxial layers for laser and electrical circuit allow independant optimization
- Approach adaptable to a variety of devices (Laser, LED, SEED) and circuit technologies (MESFET, HEMT, C-HIGFET)

Figure 1. Schematic diagram of the VCSEL structure which is compatible with integration with an FET based I.C.

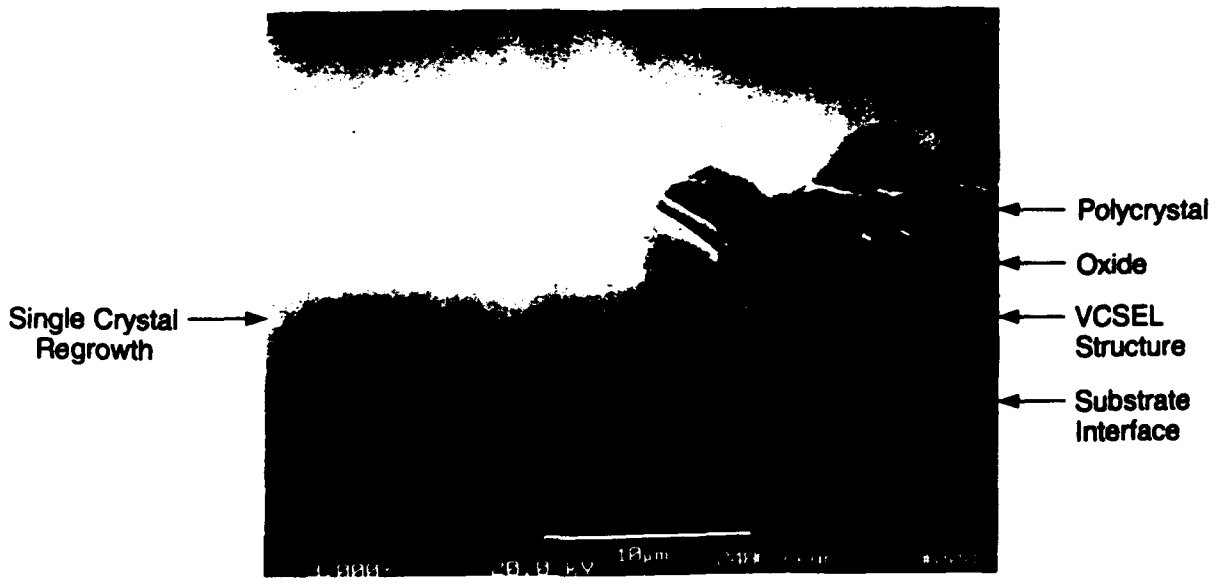


Figure 2. A scanning electron micrograph of a VCSEL epitaxial structure which was etched into a mesa. Additional epitaxial material was regrown around this mesa using OMVPE.

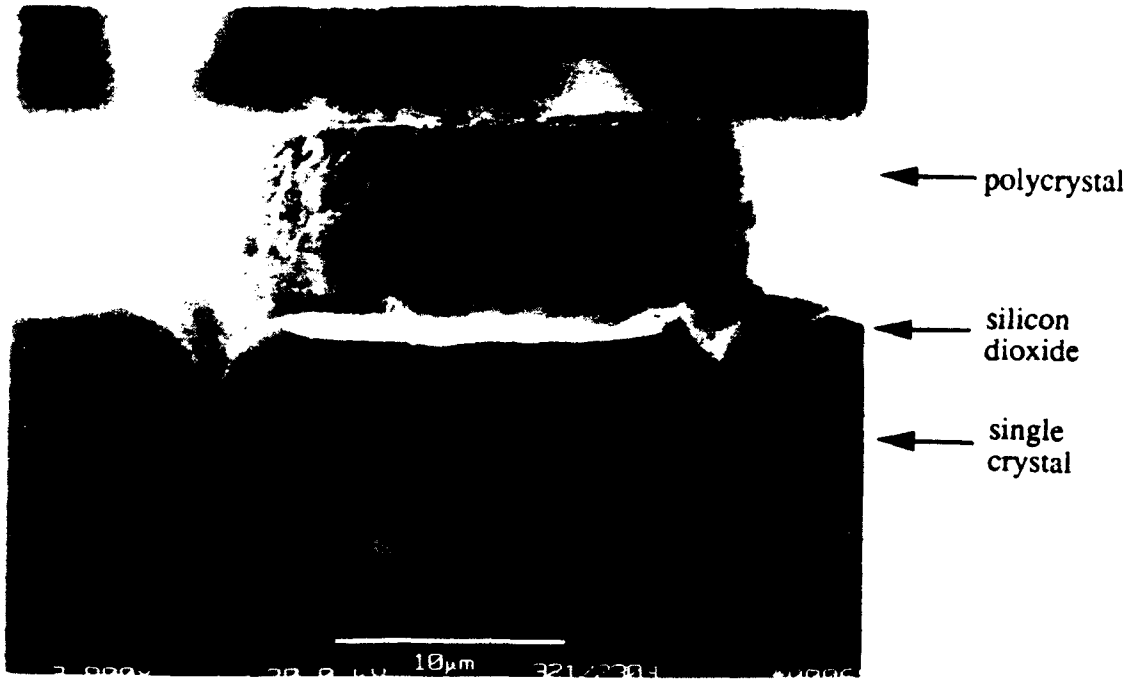


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Figure 3. A scanning electron micrograph of a VCSEL epitaxial structure which was etched into a mesa. Additional epitaxial material was regrown around the mesa using MBE.

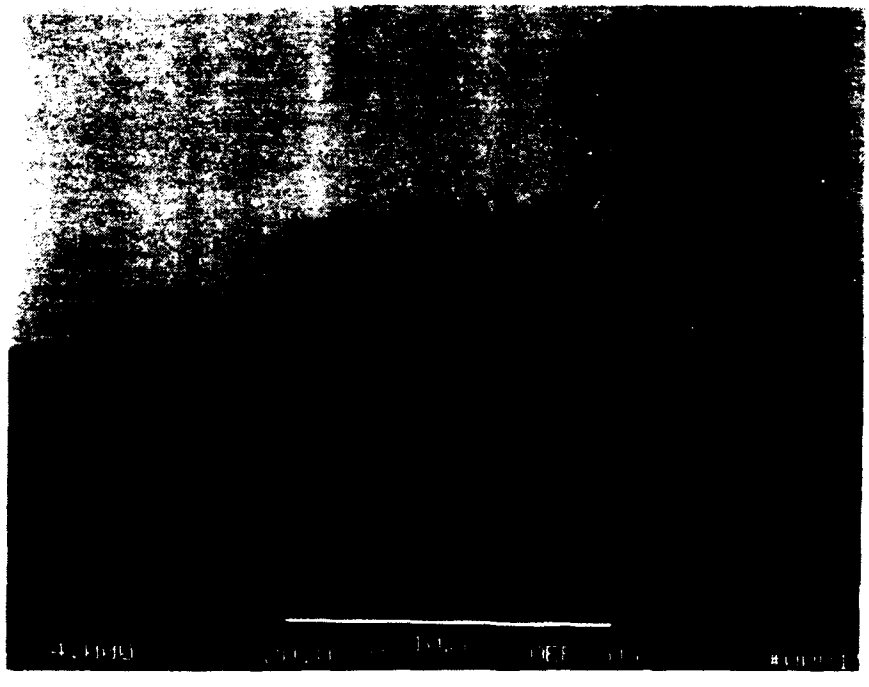

Figure 4. A scanning electron micrograph of a VCSEL mesa with an MBE regrown layer. This micrograph was taken after removing polycrystalline material from the top surface of the mesa.

Performance & Cost Report

HONEYWELL INC.
10701 LYNDALE AVE. S.
BLOOMINGTON, MN 55440

CONTRACT TITLE: Optoelectronic Processing
CONTRACT NUMBER: N00014-93-C-0138
PERIOD ENDING: 2/6/94

		COST	COM	FEE	ITD ACTUALS	BUDGET @ COMPL	% COMPLETE	ITD HOURS
F3632-1000	Int Process Development	114,626	3,905	7,997	126,528	211,460	59.84%	958
F3632-2000	Circuit Des/Lay - Pass 1	510	17	36	563	77,278	0.73%	5
F3632-3000	Int Chip Fab - Pass 1	0	0	0	0	25,085	0.00%	0
F3632-4000	Testing - Pass 1	0	0	0	0	0	0.00%	0
F3632-5000	Circuit Des/Lay - Pass 2	0	0	0	0	0	0.00%	0
F3632-6000	Int Chip Fab - Pass 2	0	0	0	0	0	0.00%	0
F3632-7000	Testing - Pass 2	0	0	0	0	0	0.00%	0
F3632-8000	Program Management	8,566	292	598	9,455	34,160	27.68%	64
F3632-9000	Materials/Consult/Subs	22,310	760	1,557	24,626	52,015	47.34%	18
	ITD Actuals	146,011	4,975	10,187	161,173	400,000	40.29%	1,045
	Committments	31,808	1,084	2,219	35,111			
	ITD Actuals+Committments	177,819	6,058	12,406	196,284	400,000	49.07%	

Figure 5. Performance and cost report.