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GRANT NUMBER AND TITLE:# N00014-91-J-1441, "DLTS and Dynamic Transconductance Analysis of Deep-Submicron Fully- Depleted SOI MOSFET's".

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SCIENTIFIC OFFICER:Dr. Alvin M. Goodman

1.PROGRESS THIS PERIOD

Progress this period was accomplished (a) in the study of temporal behavior of hot carrier induced oxide traps in both partially and fully depleted inversion mode transistors, mainly with the use of the sequential stressing technique and (b) the analysis of accumulation mode transistors supplied by IBM-Manassas, in particular electric field profile mapping along the channel for various drain designs.

Work was also initiated to carry out similar studies on technologies supplied by Honeywell (poc Dr Bill Jenkins, NRL).

Some of the most interesting results on hot carrier degradation are summarized in the attached manuscript "Hot-Carrier-Induced Degradation of SOI(SIMOX) MOSFET's", which was submitted for publication in IEEE Trans. on Electron Devices.

Useful results were also obtained for the accumulation mode (IBM) devices and a joint IBM-GEORGE MASON UNIVERSITY presentation is scheduled to be given at the Electrochemical Society Meeting in San Francisco in May, later this year.

Following the initial work on the Honeywell samples, several problems were identified regarding the bonding arrangements of the chips' which make it difficult to stress the devices independently from each other. Solutions to these problems have now been thought out and proposed.

Two research students are working on the project, Mr. Andrzej Zaleski and Mr. Sinha Shankar.

2.PLANS FOR NEXT PERIOD

(a) Continue the exploitation of our sequential front/back channel stressing technique in the study of hot-carrier degradation mechanisms, in particular as it relates to device geometry and technology, and obtain information about the trap kinetics by analyzing the observed temporal variations.

(b) Continue the work on accumulation mode, fully depleted devices supplied by IBM and compare depletion mode technologies.

(c) Prepare and submit for publication in IEEE EDL a paper on the nature of the observed traps.

3.POTENTIAL PROBLEM AREAS

(a) Technical:None

(b) Funding:None

Hot-Carrier-Induced Degradation of SOI(SIMOX) MOSFET's

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Abstract

An experimental study of the degradation mechanisms in hot-carrier stressed partially- and fully-depleted SOI(SIMOX) nMOSFET's has been carried out as a function of device (drain) design and fabrication technology, in an effort to develop hot-electron resistant devices that are suitable for space and satellite applications. A multitude of experimental techniques were used for this purpose, including the newly developed sequential front/back channel stressing measurement technique, which makes use of the hot-hole injection into the opposite channel that occurs in hot-electron stressed SOI MOSFET's. In addition, copious PISCES simulations were performed for the correct interpretation of the experimental results. It was shown that the hot-carrier degradation is mainly caused by a two step process: a rather slow oxide electron trap generation followed by a fairly fast electron filling of these traps. Moderate amounts of interface state generation may also take place under some bias conditions. The detailed analysis of the hot-hole injection into the opposite gate oxide leads to new insights on the role played by the hot-holes in the overall degradation process.

1. Introduction

As progress is being continuously made on various SOI technologies [1], there is an increasing need to address the reliability of MOSFET devices and circuits made by these technologies. With ever decreasing device dimensions, degradation caused by hot-carriers is especially important. Hot-carrier degradation of bulk MOSFET's has been studied extensively and it has been established that the two most common degradation mechanisms are interface state generation and oxide charge trapping [2]. The relative importance of these two mechanisms depends on the bias levels applied during stress and on technological details and continues to be the subject of intense investigations [3]. Several studies of hot-carrier degradation of SOI MOSFET's have also been reported [4]-[11], but the existence of two gates, the nature of the buried oxide, and the possibility of partially- and fully-depleted device operation make the situation considerably more complicated and at the same time provide new opportunities.

This paper is an experimental study of the relative importance of interface state generation and oxide charge trapping in hot-carrier stressed, SOI MOSFET's fabricated on SIMOX wafers. These devices are designed for applications in space. Both partially- and fully-depleted devices of varying geometries and drain designs are studied. Standard static transistor characteristics [12] and dynamic transconductance [13] measurements were complemented by the newly developed sequential front/back channel stressing technique [11] and extensive PISCES simulations [14]. In the sections that follow, the sample selection and the measurement techniques are first briefly described. The experimental results obtained from static transistor characteristics measurements are then compared with PISCES simulations and dynamic transconductance measurements. Further insight into the degradation mechanisms is gained by presenting and discussing the results obtained by the sequential front/back channel stressing measurement technique.

2. Sample Selection and Measurement Techniques

Four different lots of partially-depleted (PD) and two different lots of fully-depleted (FD) n-channel MOSFET's with varying drain designs and channel lengths in the range 0.6 to 1.2μm were investigated in the present studies, in an effort to develop hot-carrier resistant device structures. The SIMOX SOI wafers were prepared by oxygen implantation (1.8×10^{18} O^+/cm^2, 200 keV) and high-temperature annealing in an argon ambient. The buried oxide thickness was 400nm and the gate oxide 20 nm and 15-20nm for the PD and FD devices, respectively. The silicon film thickness and doping were 300nm and $2\times10^{17}cm^{-3}$ for the PD and 140-185nm and $4\times10^{16}cm^{-3}$ for the FD transistors.

Both the front and the back channels of the transistors were subjected to hot-carrier stressing under varying bias conditions. The front channel was stressed in the impact ionization region of operation with gate voltages in the range $0.25\times V_D \leq V_{G1} \leq V_D$, whereas the back channel was stressed at gate voltages significantly higher than the drain voltage. In all cases, the opposite interface was kept in accumulation during stress.

The static transistor $I_D(V_{G1}, V_{G2}, V_D)$ characteristics were monitored with a computer controlled HP4145B semiconductor parameter analyzer throughout the duration of the stress to obtain the threshold voltage shift ΔV_T (where the threshold voltage is defined as the V_G for which $I_D=1\mu A/\mu m$ for $V_D=0.1V$), the maximum transconductance shift Δg_m and the subthreshold slope shift ΔS.

The dynamic transconductance measurements of the interface state density vs. energy profiles $D_{it}(E)$ were performed with a computer controlled HP4192 impedance meter [13], [15]. The devices were measured both before and after the stress. For FD devices in particular, the entire forbidden gap (from accumulation through depletion to inversion) can be probed with this technique with high sensitivity and resolution, by making the measurement first with the current flowing through

the channel next to the interface under investigation and then through the opposite channel. Additional interface state measurements were carried out by the high-low frequency transconductance method [16], and for the (narrower) energy range probed the results were comparable to dynamic transconductance.

The sequential front/back channel stressing measurement technique has been recently developed specifically for the study of the degradation mechanisms in hot-carrier stressed SOI MOSFET's [11]. In this technique sequentially applied hot-electron injection conditions to the front (FEI) and back (BEI) channels cause the corresponding threshold voltages V_{T1}/V_{T2} first to increase/decrease and then decrease/increase, respectively. Electron injection conditions are achieved by applying sufficiently large gate and drain voltages, while keeping the opposite interface accumulated. The observed threshold voltage recovery is caused by hot-holes created by impact ionization at one interface and injected into the gate oxide of the opposite interface, aided by the favorable direction of the electric field there. The possibility of other mechanisms of recovery (such as Fowler-Nordheim electron de-trapping across the gate-to-drain overlap region, for instance) is ruled out by demonstrating that any significant $V_{T1,2}$ recovery requires the actual opening of the opposite channel.

3. General Evaluation

3.1 Front channel stressing: Depending on the gate voltage during stress and the device lot under consideration, the shape of the resulting front channel I_D vs. V_{G1} characteristics generally resembled one of the three cases shown in Fig. 1. Fig. 1(a) shows typical characteristics of devices stressed under low front gate voltages ($V_{G1} \leq 0.5 \times V_D$), where the threshold voltage V_{T1} and (not shown) the subthreshold slope S_1 increase, whereas the transconductance g_{m1} decreases. Figs. 1(b) and (c) show typical results for devices stressed under high front gate voltage ($V_{G1}=V_D$) conditions, where V_{T1} and S_1 always increase considerably, but g_{m1} may remain either unchanged (b) or increase substantially (c). Occasionally, however, type (a) characteristics were also measured for transistors

stressed under high V_{G1}. The extent of the observed parameter changes was different for different device lots and channel lengths, and a summary of the general trends for 0.8μm devices is shown in Table I.

3.2 Back channel stressing: For the back interface, the gate voltage required to form the channel is much larger than the maximum drain voltage that can be safely applied to the transistor, leading to electron injection into the buried oxide. As shown in Table I, depending on the device lot measured, two distinctly different types of degraded back channel characteristics were observed. In both cases the threshold voltage V_{T2} increases within a wide range, depending on the device lot under consideration, the transconductance g_{m2} may either increase or decrease and the subthreshold slope S_2 may increase or remain unchanged.

4. PISCES Simulations

In order to investigate the mechanisms responsible for the various types of the observed degradation of the device static characteristics described above copious PISCES simulations were carried out [14]. Following bulk device practice [17]-[21] and some recent work on SOI devices [10], two-dimensional, one- and two-carrier simulations were performed for various amounts and locations of oxide trapped charge along the interfaces. The effect of interface states is taken into account indirectly in such studies, by using the appropriate mobility models [17], [19], [20], [22], [23]. The establishment of trends, rather than actual fittings of the experimental curves was sought in the present study.

The effect of localization and amount of negative oxide-trapped charge on the front channel subthreshold slope and transconductance is shown in Fig. 2, where the plots reflect changes due to -1×10^{12}, -2×10^{12}, and -3×10^{12}cm^{-2} uniformly distributed oxide charge above the channel and covering up to 40% of the channel from the drain end. It is seen that significant changes in the subthreshold slope are only induced when the charges are narrowly localized within $\sim$15% of the

channel (Fig. 2(a)). By contrast Fig. 2(b) shows that the transconductance can change substantially even when the oxide charge occupies as much as 40% of the channel.

Similar analysis for positive charges showed that in order to cause significant change in the subthreshold slope the charges must occupy over 90% of the channel. Equal amounts of narrowly localized positive charges cause a much smaller change in the threshold voltage than negative charges, and both kinds of charges affect the transconductance in the same way (see Table II). An interesting analogy can be drawn here between the negative and positive localized oxide charges by noticing that the changes induced by the positive charges become more important when the area they occupy extends closer to the source region. This situation results in a small part of the channel adjacent to the source having bigger threshold voltage than the rest of the channel and is analogous to the case where negative charges cause the threshold voltage to decrease adjacent to the drain.

To investigate the effects of the specific drain designs (mainly with varying LDD doping levels) and the oxide spacer various amounts of oxide charge were assumed to be trapped in the oxide just above or below the LDD, and their effect on the transistor static characteristics was simulated. Some of these results are shown in Table II from which it can be concluded that this effect is significant only for negative charges, which tend to degrade the transconductance. The effect is more pronounced for the lower doped LDD's, since in this case they can become completely depleted. This can for instance be seen in Fig. 3 where the linear front channel characteristics are plotted for several densities of negative oxide charge located above the LDD, for a 80nm thick silicon film FD transistor with (a) grounded back gate and (b) strongly accumulated back gate by applying -30V. It is seen here that the degradation is much worse in the case of accumulated back interface, because in this case the LDD gets fully depleted and the drain series resistance increases very much.

PISCES does not explicitly account for the effects of interface states. Instead, a mobility degradation factor g_{surf} can be included in the simulation and used to indirectly study these effects.

On the basis of this factor the surface mobility μ_{surf} is recalculated as $g_{surf} \times \mu_{bulk}$. The transistor characteristics simulateded for g_{surf} values in the range 0.3 to 0.75 closely resemble those in Fig. 3(a), obtained for various amounts of oxide charges. Thus, when interpreting experimental current vs. voltage transistor characteristics it is very difficult to ascertain whether oxide charge or interface states are responsible for the degradation and independent D_{it} measurements (by dynamic transconductance for instance) must be carried out.

A comparison of these simulation results and the experimental results presented in the previous section suggests that the degradation in Fig. 1(a) could be caused by either oxide charges trapped above the LDD region or interface states, in Fig. 1(b) by a simultaneous presence of negative oxide charges above the channel and LDD and interface states, and in Fig. 1(c) mainly by localized electron trapping in the gate oxide above the channel, near the drain. For the back channel (Table I) the degradation of lots 3A and 12A could be due to the localized electron trapping in the buried oxide below the channel, near the drain, whereas for lot 15A electrons trapped below the LDD could be the reason.

5. Dynamic Transconductance Measurements

To examine possible interface state generation, dynamic transconductance [13], [15] measurements were performed before and after the stress. In most of the cases studied, provided that appropriate care was taken to correctly bias the device for the measurement at hand, well behaved, bell shaped G_p/ω vs. ω experimental curves were obtained. Before hot-carrier stressing these curves always led to U shape $D_{it}(E)$ profiles with interface state densities ranging from mid 10^{11} cm^{-2} eV^{-1} near the middle of the band-gap to upper 10^{12} cm^{-2} eV^{-1} near the band edges. After stress, the D_{it} level increased considerably only in the case of low gate voltage V_{G1} stressing. It should be noted at this point, that the increase in D_{it} occurred at the upper portion of the band-gap, similar to observations made in bulk devices by Doyle at al [24]. For high gate voltage V_{G1} stressing no

observable change in D_{it} was recorded.

With regard to the back interface, the gate voltage during stress was always significantly larger than the drain voltage, of course, and no changes in the $D_{it}(E)$ profile were detected. This is shown in Fig. 4, obtained for a FD device stressed under V_{G1}=-2.5V, V_{G2}=25V and V_D=5.8V, for 4 hours.

6. Sequential front/back channel stressing

From the above experimental and simulation results it can generally be concluded that for high gate voltage stressing the degradation is dominated by local electron trapping in the gate oxides above/below the front/back channel close to the drain and possibly also above/below the LDD, whereas for the low gate voltage front channel stressing interface state generation also occurs. To examine this general conclusion in more detail and obtain further insight into the degradation mechanisms, sequential front/back channel stressing measurements were performed by making use of the hot-hole injection into the opposite gate oxide during hot-electron stressing of a SOI MOSFET [11].

Representative results of sequential stressing measurements of the front(1) and back(2) channel device parameters $V_{T1,2}$, $S_{1,2}$, and $g_{m1,2}$ are shown in Figs. 5 and 6, respectively. For these measurements, the devices were sequentially stressed under front channel hot-electron injection conditions, FEI, with biases V_{G1}=8V, V_{G2}=-20V and V_D=8V (periods I, III, V) followed by back channel hot-electron injection conditions, BEI, with V_{G1}=-2V, V_{G2}=75V and V_D=7.5V (periods II and IV). In Fig. 5, V_{T1} and S_1 increase during the FEI periods I, III and V and they recover during the BEI periods II and IV. The maximum transconductance g_{m1} decreases during the first FEI period and then remains unchanged during periods II-V. The back channel parameters (Fig. 6), do not change during FEI period I, but follow changes similar in nature to the front channel for periods II-V: V_{T2}, S_2, and g_{m2} all increase in the BEI periods and recover during the subsequent FEI periods.

The stress conditions in the above measurements suggest that for both interfaces the observed device parameter recovery is caused by hot-holes created by impact ionization at one interface during the corresponding hot-electron injection periods and injected into the opposite interface, kept in accumulation (Fig. 7). That this is indeed the case can be seen in Fig. 8, were the threshold voltage changes are plotted throughout a rather involved stressing sequence: BEI is followed by a period of all terminals shorted (0's), followed by a period with both channels accumulated and high drain voltage (ACC1), FEI, 0's, ACC2, and finally BEI. For ACC1 and ACC2 stress periods the exact voltage values were V_{G1}=-2V, V_{G2}=-20V, V_D=8V, and V_{G1}=-2V, V_{G2}=-20V, V_D=7.5V, respectively. It is clear from Fig. 8 that significant $V_{T1,2}$ recoveries require the actual opening of the opposite channel, i.e. BEI for V_{T1} and FEI for V_{T2}. For example, a close look at the results in the "box" in Fig. 8(a) shows that during FEI V_{T1} increases significantly, in the 0's that follow immediately V_{T1} recovers very little, then recovers a little more during the ACC2 that follows, and a major recovery is only observed when finally BEI conditions are applied. Although a drop of 9.5V is sustained across the gate-to-drain overlap region during ACC2, apparently no significant Fowler-Nordheim [25] electron de-trapping occurs. The situation is similar for the back channel parameters (Fig. 8(b)).

From Fig. 5 several important observations and conclusions can be made regarding the degradation mechanism. First, the front channel parameters that degraded during FEI (periods I, III, and V) recovered fully during periods II and IV (BEI) during which hot-holes were injected into the front gate oxide. This clearly suggests that FEI conditions resulted almost exclusively in electron trapping in the front gate oxide, which was subsequently neutralized by hot-holes. Second, the subthreshold slope degrades significantly during FEI, but it recovers completely during the subsequent BEI periods II and IV (Fig. 5(b)). This rules out any significant interface state generation during FEI according to the hydrogen model of the generation mechanism [26], since such interface states once formed could not be removed by hot-holes. Third, no significant interface state

generation was caused by the hot-holes [27], [28] injected into the front gate oxide during BEI either, because if this was the case the subthreshold slope S_1 rather than recover by BEI (Fig. 5(b), periods II and IV), it would degrade further. Similar conclusions can be drawn in the case of the back interface (Fig. 6). The slight residual threshold voltage V_{T2} and transconductance g_{m2} degradations following FEI periods III and V (Fig. 6(a)) could be attributed to oxide electron trapping in the buried oxide below the LDD.

A better understanding of the gate oxide charging/discharging process can be achieved by making a more careful analysis of the threshold voltage $V_{T1,2}$ changes with time observed in the sequential stressing experiments. These time changes (compare periods I and III in Fig. 5(a), for example) suggest a two step degradation mechanism, i.e. a relatively slow trap generation process (dominating period I) and a fairly fast trap filling (dominating the initial stage of period III). Since both front and back threshold voltages are affected simultaneously, more information can be extracted here than in bulk devices [29]. For instance, during stress period V (FEI) in Figs. 5(a) and 6(a) both $V_{T1,2}$ changes are induced by hot-electrons/holes generated at the front interface and injected into the front/back gate oxides, respectively, as it has already been explained. By noting from these figures that the changes in $V_{T1,2}$ tend to saturate after some time, due to the limited number of traps and assuming the same trapping mechanisms in both gate oxides (justified by the same character of changes of the $V_{T1,2}$), an estimate of the ratio of the hole/electron trap capture cross sections σ_p/σ_n will be derived. Following Hu et al [26] the gate currents $I_{G1,2}$ can be expressed by

$$I_{G1} = C\ I_D\ exp(-\phi_{be}/q\ \lambda_e E_m) \tag{1}$$

$$I_{G2} = C\ I_D\ exp(-(\phi_{bh} - 2\phi_F)/q\ \lambda_h E_m) \tag{2}$$

where C is a proportionality constant, $\phi_{be,bh}$ (in eV) are the barrier heights for electrons, holes, ϕ_F is the Fermi potential, E_m is the maximum value of the electric field in the channel and $\lambda_{e,h}$

are electron, hole mean free paths. Assuming ϕ_{be}=3.2eV and ϕ_{bh}=4.7eV [30], concentrating on the initial part of the stress period V and expressing σ as equal to $q(\tau I_G)^{-1}$ [29], Equations (1) and (2) lead to the following expression for the ratio σ_p/σ_n:

$$\frac{\sigma_p}{\sigma_n} = \frac{\tau_n}{\tau_p} exp\left(\frac{\phi_{bh} - 2\phi_F}{q\lambda_h E_m} - \frac{\phi_{be}}{q\lambda_e E_m}\right) \tag{3}$$

where τ_n and τ_p are defined by

$$\Delta V_{T1,2} = \Delta V_{Tmax1,2}\left[1 - exp\left(-\frac{t}{\tau_{n,p}}\right)\right] \tag{4}$$

Fig. 9 is a plot of the quantity $\log(1 - \Delta V_{T1,2}/\Delta V_{Tmax1,2})$ vs. time according to Equation (4), from the slope of which it is found that τ_n=108s and τ_p=57s. Using now typical values [31] for λ_e=6.2nm and λ_h=3.8nm the ratio σ_p/σ_n is finally calculated to be equal to 4×10^5. It is thus seen that a trap filled with an electron acts as a Coulomb-attractive center for holes and has approximately 4×10^5 times larger capture cross section σ_p, than an empty one acting as a neutral trap for electrons (σ_n). If a value for the gate current $I_{G1}=10^{-14}$A/μm is assumed [9] and the charge injection takes place in a region extending 0.2μm from the drain [32], then typical values for the cross sections $\sigma_n \approx 0.3\times10^{-17}$cm^2 and $\sigma_p \approx 1.2\times10^{-12}$cm^2 are obtained [3].

Fig. 10 repeats the FEI/BEI experiment of Fig. 5, but with a lower front gate voltage during front channel stress (=2V). Such gate voltage values are known to generate interface states in bulk devices [33], and the present experiment was designed to examine whether this is also true in SOI devices. Comparing this to Fig. 5, it is seen that the extend of degradation is smaller for the smaller gate voltage. However, unlike Fig. 5, here the degradation introduced during the front channel stressing did not recover fully during the following back channel stressing, especially with regard to S_1. This suggests, that there was measurable interface state generation for this gate bias value, consistent with the dynamic transconductance results (section 5). The partial recovery of V_{T1} and g_{m1} observed in Fig. 10(a) and (c) can be attributed to electron trapping within the

spacer area, subsequently neutralized by hot-holes injected during the back gate stressing.

To investigate the overall degradation as well as the relative importance of charge trapping in the oxide vs. interface state generation for different gate bias levels as a function of device fabrication technology, the front channel parameters of the four different lots of PD devices were studied as a function of the gate voltage V_{G1} applied during stress. As mentioned earlier, the main difference of the devices of these lots were in the drain design, in an effort to develop hot-electron resistant circuits for space/satellite applications. Four separate front channel bias levels 2V, 4V, 6V, and 8V were used. The extent of the degradation, as well as the subsequent recovery during BEI of V_{T1} and S_1 as a function of the V_{G1}/V_D ratio during stress is shown in Fig. 11. Recovery takes place in each and every case, but the amount varies with device lot and is greatest for lots 3A and 12A. Generally, the smallest amount of recovery was observed following low front gate voltage V_{G1} stressing, the reason being the interface state generation. It is also clear from Fig. 11 that the amount of the electron trapping, represented by the recoverable part of the damage, can vary very significantly depending on the technology under consideration. The situation is similar for the back interface, as seen in Fig. 12 where the V_{T2} is shown degraded after BEI and then recovered by FEI conditions, for three different device lots.

5. Conclusions

A multitude of experimental techniques as well as PISCES numerical simulations were used to study hot-carrier degradation of several lots of SIMOX MOSFET's as a function of fabrication technology and device (mainly drain) design. It was found that (a) the degradation is mainly due to generation and subsequent filling of electron traps in the gate oxides near the drain above/below the channel and/or the LDD; (b) moderate interface state generation also occurs, but only for low gate voltage stressing; (c) hot-hole injection does not lead to generation of interface states; (d) charge trapping above/below the LDD is especially important since it may completely deplete the

lower doping LDD designs and lead to large series resistances. The vulnerability of the oxides to hot-carrier stress was found to vary significantly with the technology under consideration. However no clear pattern was established as to whether the front gate or buried oxide is more vulnerable.

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Figure captions

Fig.1. Typical front channel I_D vs. V_{G1} characteristics measured throughout the duration of the stress, obtained for (a) devices stressed under low V_{G1} ($V_{G1} \leq 0.5 \times V_D$), and (b) and (c) devices stressed under high V_{G1} ($V_{G1}=V_D$) bias conditions. Stress conditions: (a) V_{G1}=2V, V_{G2}=-20V, V_D=8V for 10h (0.8μm channel length, lot 15A), (b) V_{G1}=8V, V_{G2}=-20V, V_D=8V for 10h (0.8μm, lot 12A), and (c) V_{G1}=8V, V_{G2}=-20V, V_D=8V for 10h (0.8μm, lot 1A).

Fig.2. Simulated normalized subthreshold slope S_1 (a), and transconductance g_{m1} (b) vs. % of the channel length over which negative charges are trapped in the oxide, for charge densities: $-1\times10^{12}cm^{-2}$, $-2\times10^{12}cm^{-2}$, and $-3\times10^{12}cm^{-2}$. Channel length 1μm.

Fig.3. Simulated front channel characteristics of a 1μm FD MOSFET vs. charge density of negative charges trapped above the larger part of the LDD away from the channel, with grounded back gate(a) and with accumulated back gate (V_{G2}=-30V) (b), respectively.

Fig.4. Typical back interface state density D_{it} vs. energy profile before and after back channel stress for a 0.6μm FD device.

Fig.5. Front channel threshold voltage (a), subthreshold slope (b) and maximum transconductance (c) normalized to to their pre-stress values, throughout the high front V_{G1}/high back V_{G2} sequential stressing of a 0.8μm PD device. Stress conditions: V_{G1}=8V, V_{G2}=-20V, V_D=8V (periods I, III, V), and V_{G1}=-2V, V_{G2}=75V, V_D=7.5V (periods II, IV).

Fig.6. Back channel threshold voltage (a), subthreshold slope (b) and maximum transconductance (c) normalized to their pre-stress values, throughout the sequential stressing cycle of Fig. 5.

Fig.7. SOI MOSFET biased under back channel hot-electron injection conditions. Hot-electrons

flow into the drain (a) or are injected into the buried oxide (b), whereas hot-holes are directed towards the front gate oxide (c).

Fig.8. "Cross-check" stressing sequence applied to the front (a) and back (b) gates, to clarify the mechanism responsible for the observed parameter recovery during sequential stressing. The bias conditions are described in the text. Comparison of the $V_{T1,2}$ changes during ACC 2 and BEI periods for the front (a), and ACC 1 and FEI for the back (b) reveals that major parameter recovery requires the opening of the opposite channel.

Fig.9. Time analysis of the data in Figs. (8a) and (9a) where the $V_{T1,2}$ changes during period V yield two time constants: τ_n=108s for electron capture and τ_p=57s for hole capture.

Fig.10. Front channel threshold voltage (a), subthreshold slope (b) and maximum transconductance (c) normalized to their pre-stress values, throughout low front V_{G1}/high back V_{G2} sequential stressing of an identical MOSFET to that of Fig.8. Stress conditions: V_{G1}=2V, V_{G2}=-20V, V_D=8V (periods I, III, V), and V_{G1}=-2V, V_{G2}=75V, V_D=7.5V (periods II, IV).

Fig.11. Front threshold voltage and subthreshold slope degradation (after front channel stress) and recovery (after back electron injection, BEI) as a function of the V_{G1}/V_D (V_D=8V) ratio during front channel stress. Results are presented for three different lots of 0.8 μm PD devices (denoted 3A, 12A, 15A). For high V_{G1}, both the V_{T1} and S_1 can be recovered almost completely but only partial recovery is seen after low V_{G1} front channel stress.

Fig.12. Back channel threshold voltage degradation (after back channel stress) and recovery (after front electron injection, FEI), as a function of technology, for three lots of 0.8 μm PD devices (denoted 3A, 12A, 15A).

Table captions

Table I. General degradation trends obtained for four lots of 0.8μm PD devices stressed under identical bias conditions ("Low V_{G1}": V_{G1}=2V, V_{G2}=-20V, V_D=8V; "High V_{G1}": V_{G1}=8V, V_{G2}=-20V, V_D=8V; and "High V_{G2}": V_{G1}=-2V, V_{G2}=75V, V_D=7.5V). The extent of parameter degradation is shown with respect to their pre-stress values: "↗"("↘") denotes increase(decrease) less than 15%, "↗↗"("↘↘") increase(decrease) 15 to 50%, "↗↗↗"("↘↘↘") increase(decrease) over 50%, "unch" - unchanged, and "n/a" - no data available.

Table II. PISCES simulation of parameter degradation caused by localized negative/positive charges of density $2\times10^{12}cm^{-2}$ in the front/buried gate oxide. The device is a 1μm PD MOSFET with a 0.1μm LDD. The charges are positioned left (-) and right (+) of the channel/LDD boundary, as shown in parentheses. "Slight" denotes changes below 1%, and "large" - above 10%.

TABLE I

Lot	Low V_{G1}			High V_{G1}			High V_{G2}		
	V_{T1}	S_1	g_{m1}	V_{T1}	S_1	g_{m1}	V_{T2}	S_2	g_{m2}
1A	↗	↗	↘↘	↗↗↗	↗↗↗	↗↗	n/a	n/a	n/a
3A	↗↗	↗↗	↘↘↘	↗↗↗	↗↗↗	↘↘	↗↗	↗↗↗	↗↗
12A	↗↗	↗↗	↘↘	↗↗↗	↗↗↗	↘	↗↗	↗↗↗	↗↗
15A	↗	↗	↘↘	↗	↗	↘↘	↗	unch	↘

TABLE II

Cause	Resulting parameter shift		
	$V_{T1,2}$	$S_{1,2}$	$g_{m1,2}$
1. Negative charge in the oxide placed:			
1.1. above/below channel (-0.07÷0.0μm)	large increase	large increase	large increase
1.2. above/below LDD (0.03÷0.1μm)	unchanged	unchanged	decrease
1.3. 1.1.and 1.2. together (-0.07÷0.1μm)	large increase	large increase	large increase
2.Positive charge in the oxide placed:			
2.1. above/below channel (-0.07÷0.0μm)	slight decrease	slight increase	increase
2.2. above/below LDD (0.03÷0.1μm)	unchanged	unchanged	slight increase
2.3 2.1.and 2.2. together (-0.07÷0.1μm)	slight decrease	slight increase	increase

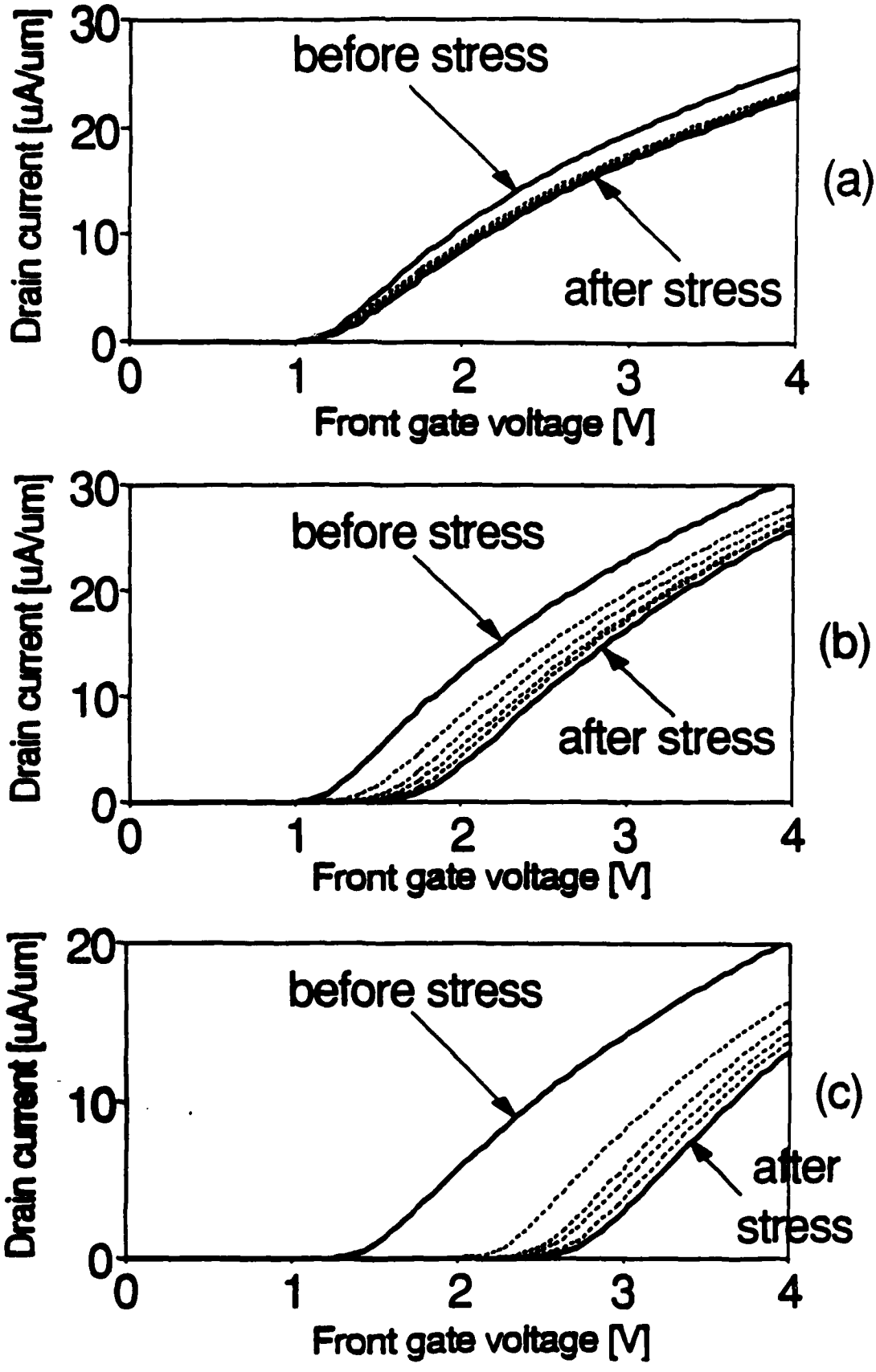
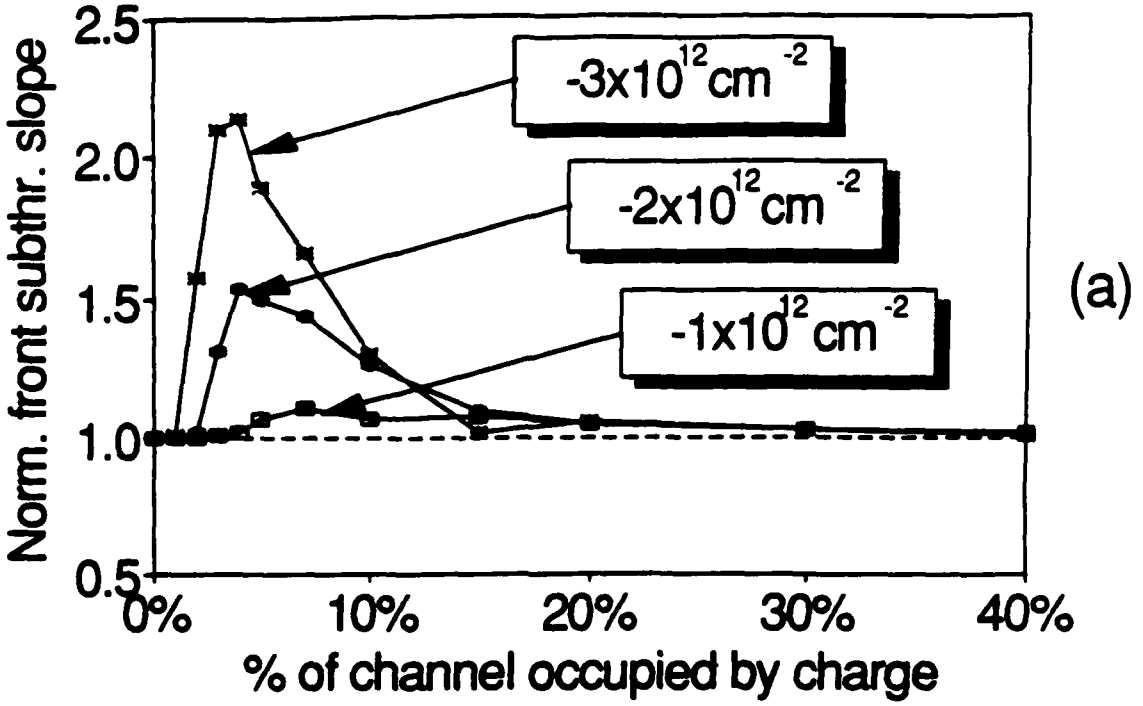

Drain current [uA/um]
30
20
10
0
before stress
after stress
0
1
2
3
4
Front gate voltage [V]
(a)
Drain current [uA/um]
30
20
10
0
before stress
after stress
0
1
2
3
4
Front gate voltage [V]
(b)
Drain current [uA/um]
20
10
0
before stress
after
stress
0
1
2
3
4
Front gate voltage [V]
(c)

Fig.1


Norm. front subthr. slope
2.5
2.0
1.5
1.0
0.5
-3x10^12cm^-2
-2x10^12cm^-2
-1x10^12cm^-2
0%
10%
20%
30%
40%
% of channel occupied by charge
(a)

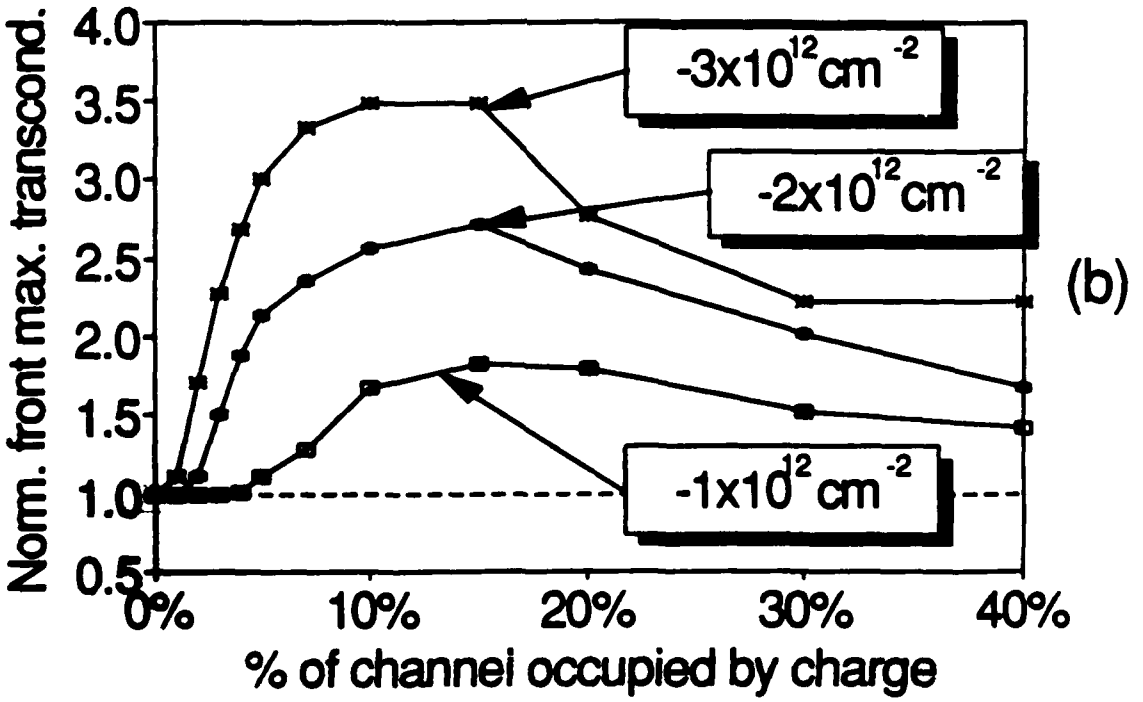

Norm. front max. transcond.
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
-3x10^12cm^-2
-2x10^12cm^-2
-1x10^12cm^-2
0%
10%
20%
30%
40%
% of channel occupied by charge
(b)

Fig.2

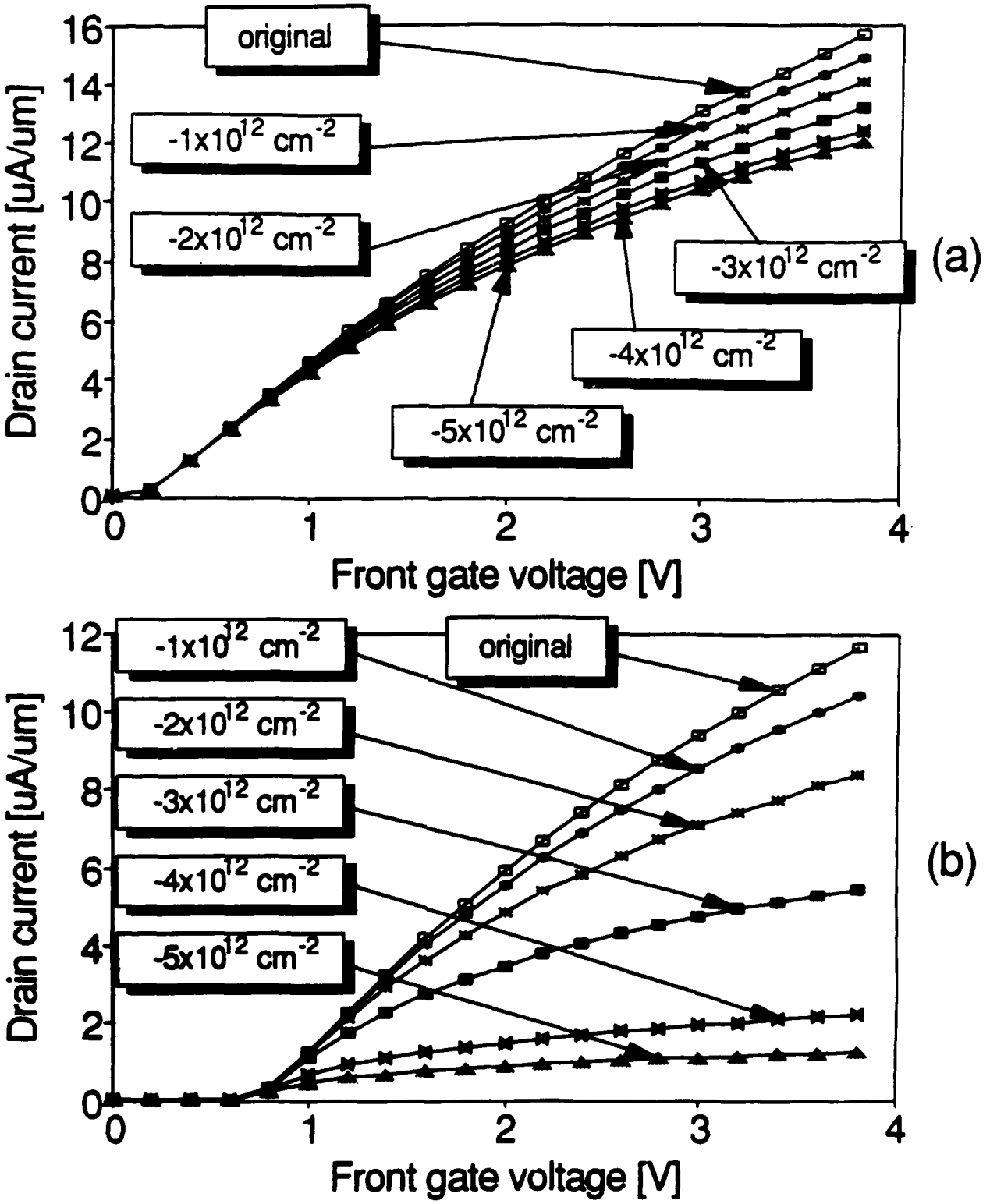

original
-1x10^12 cm^-2
-2x10^12 cm^-2
-3x10^12 cm^-2
-4x10^12 cm^-2
-5x10^12 cm^-2
Drain current [uA/um]
Front gate voltage [V]
(a)
(b)

Fig.3

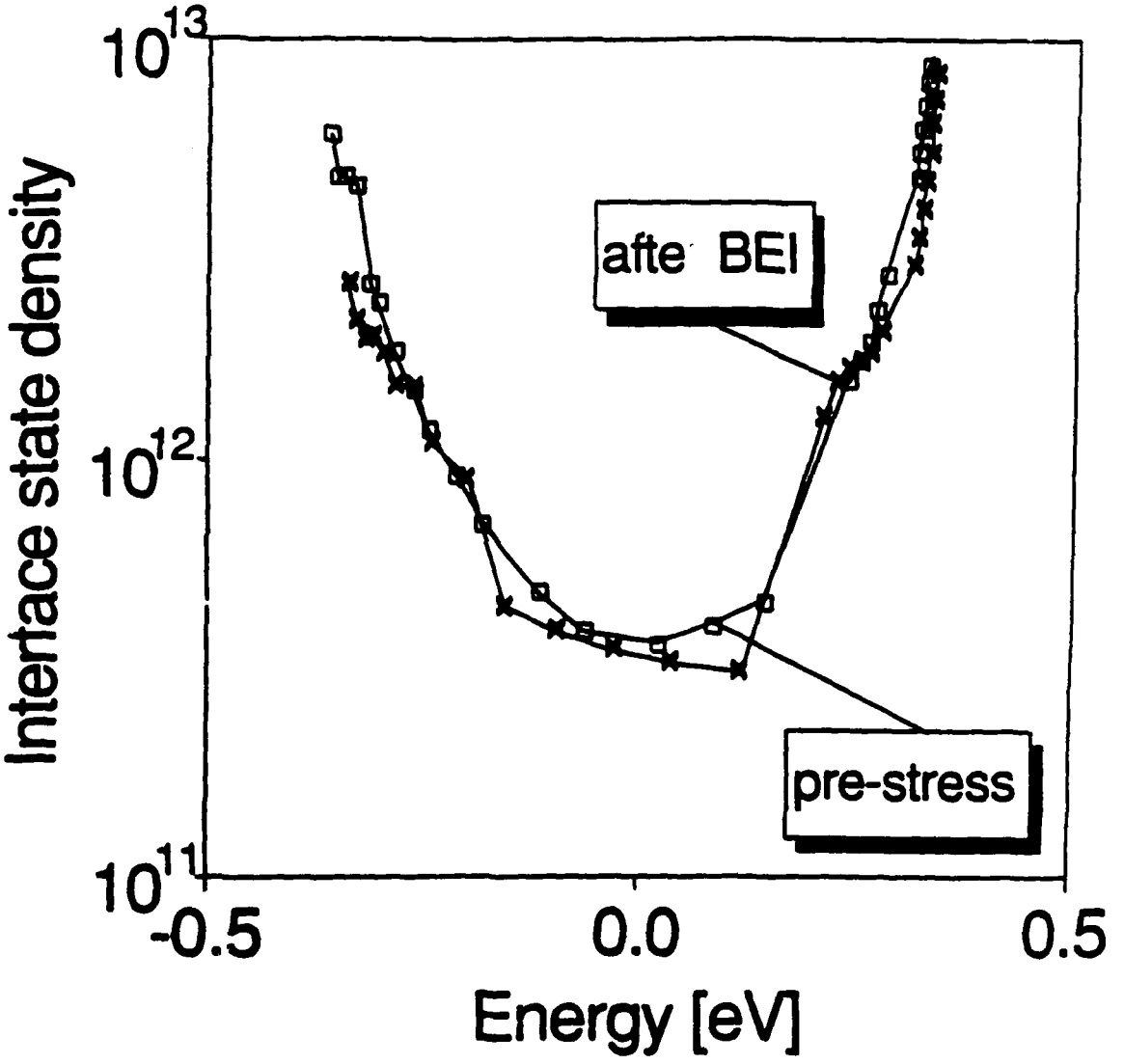

10^{13}
10^{12}
10^{11}
Interface state density
afte BEI
pre-stress
-0.5
0.0
0.5
Energy [eV]

Fig.4

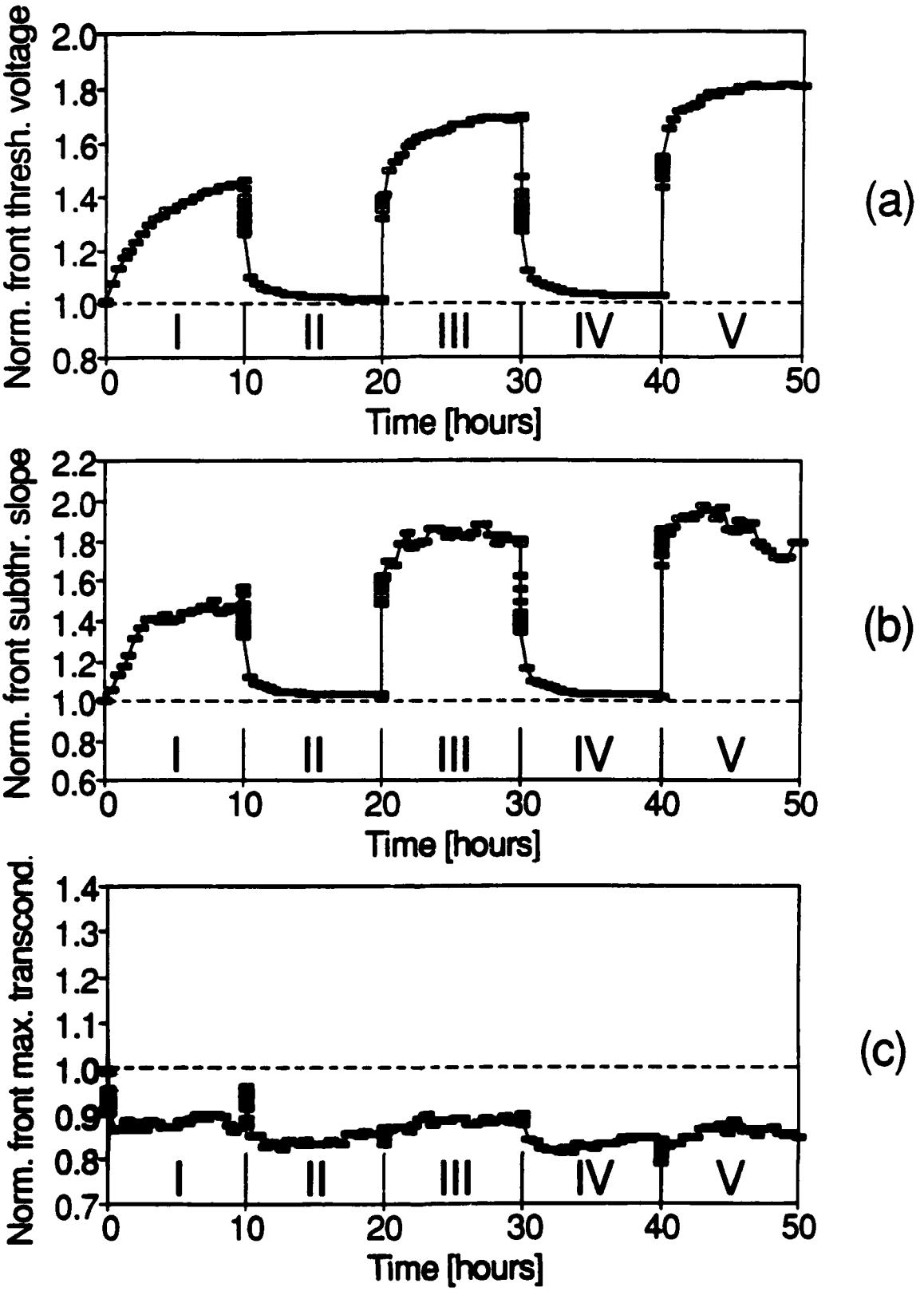

Norm. front thresh. voltage
2.0
1.8
1.6
1.4
1.2
1.0
0.8
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(a)
Norm. front subthr. slope
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(b)
Norm. front max. transcond.
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(c)

Fig.5

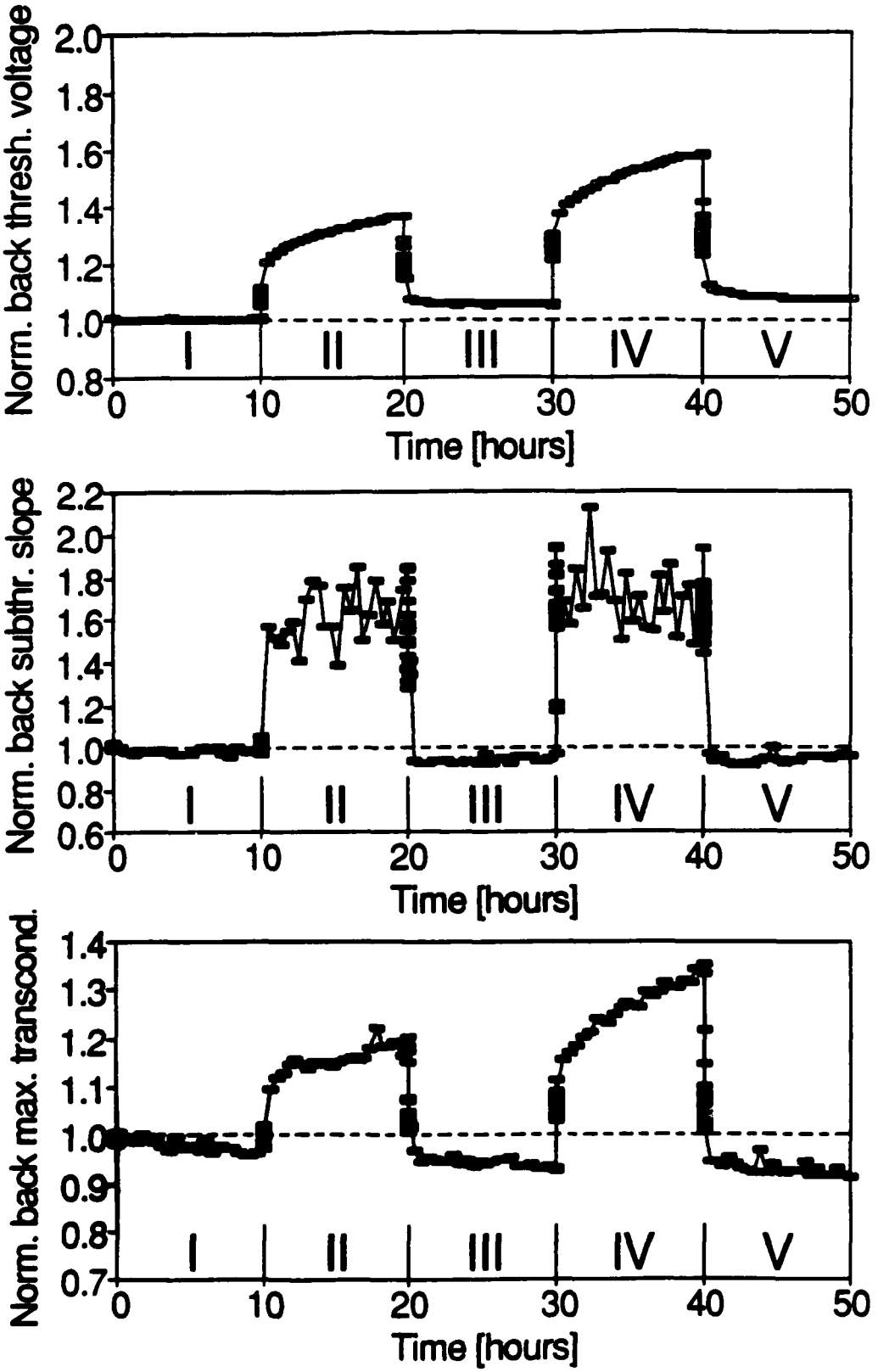

Norm. back thresh. voltage
2.0
1.8
1.6
1.4
1.2
1.0
0.8
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(a)
Norm. back subthr. slope
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(b)
Norm. back max. transcond.
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(c)

Fig.6

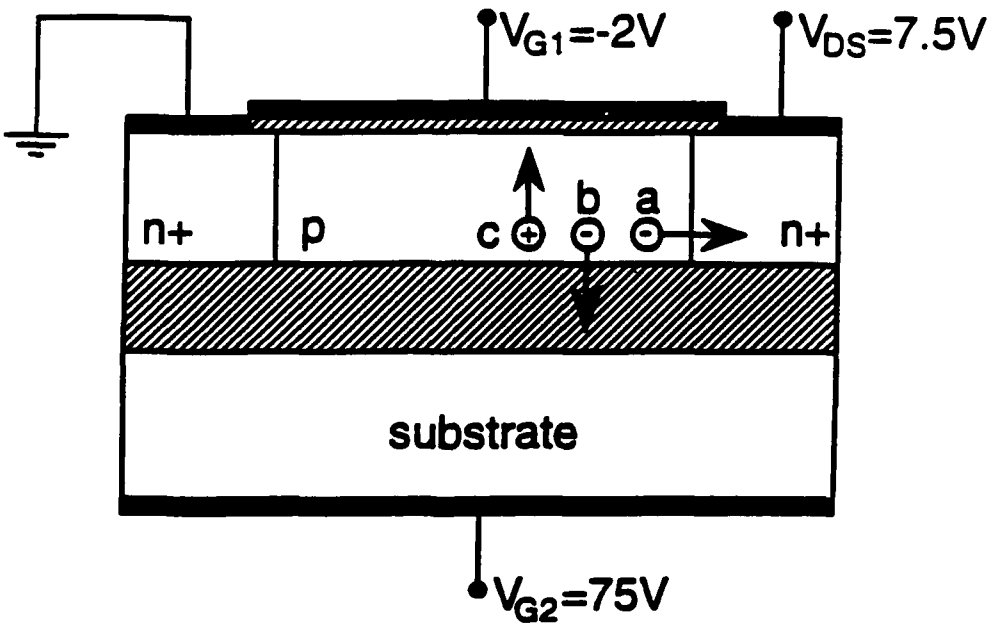
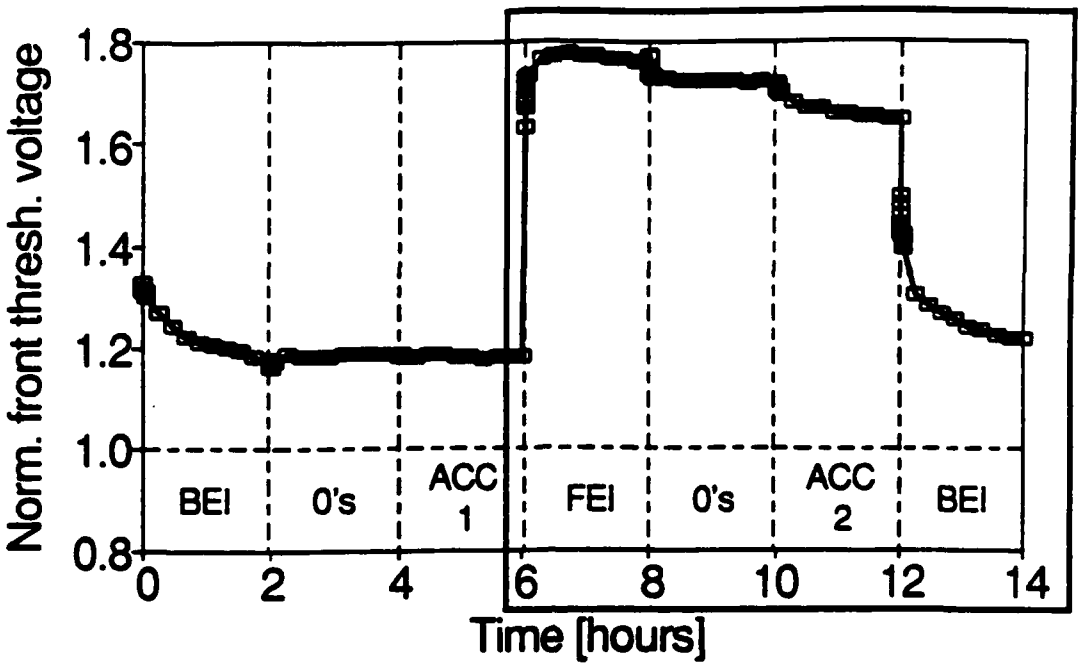
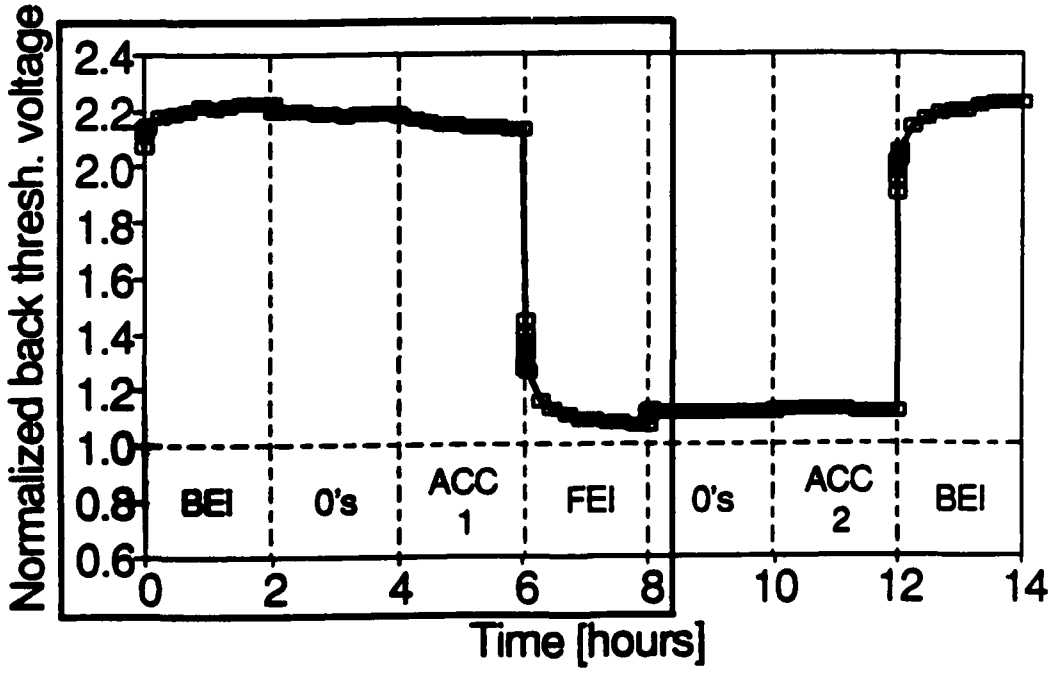


Fig.7


Norm. front thresh. voltage
1.8
1.6
1.4
1.2
1.0
0.8
BEI
0's
ACC 1
FEI
0's
ACC 2
BEI
0
2
4
6
8
10
12
14
Time [hours]

(a)


Normalized back thresh. voltage
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
BEI
0's
ACC 1
FEI
0's
ACC 2
BEI
0
2
4
6
8
10
12
14
Time [hours]

(b)

Fig.8

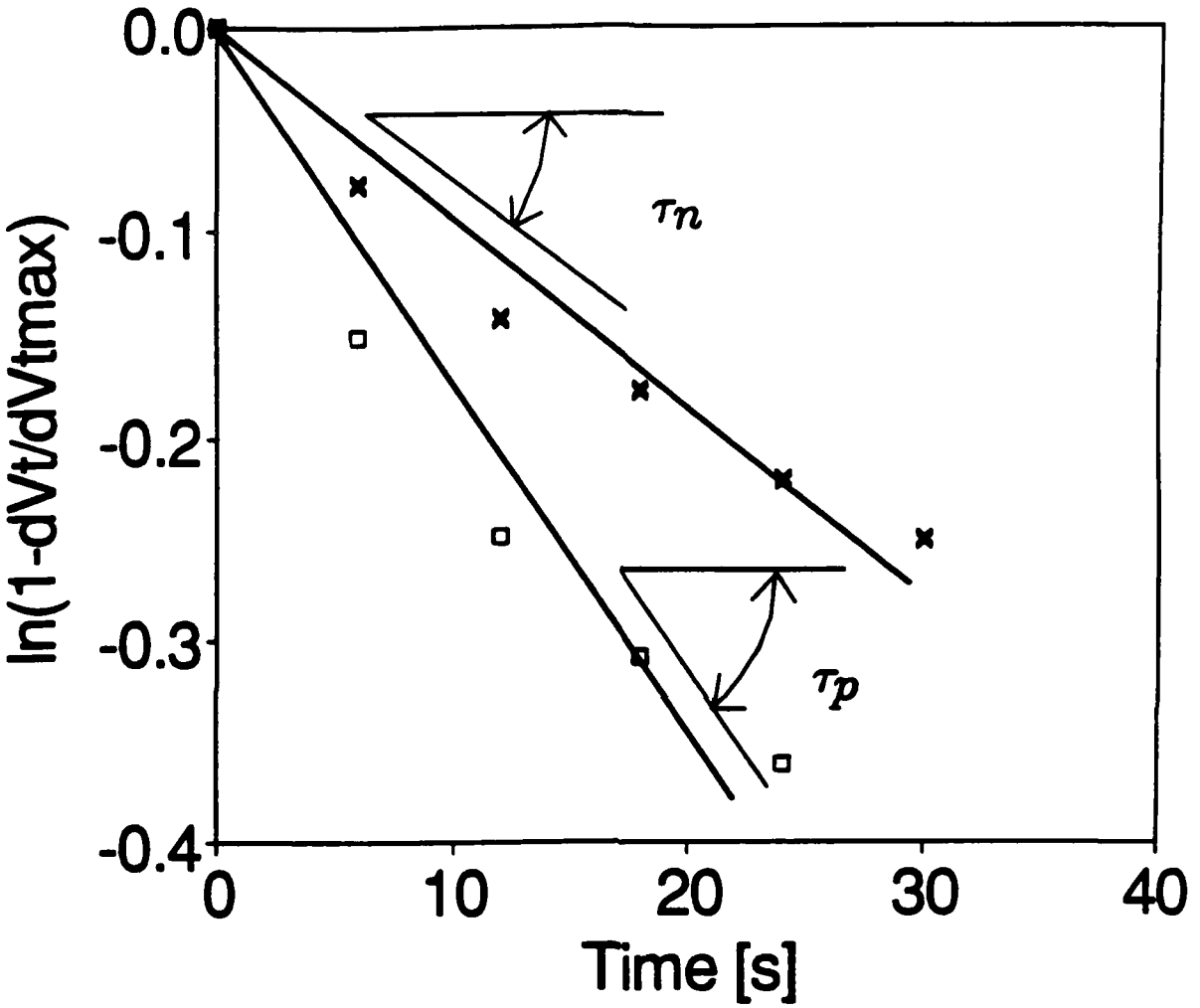


Fig.9

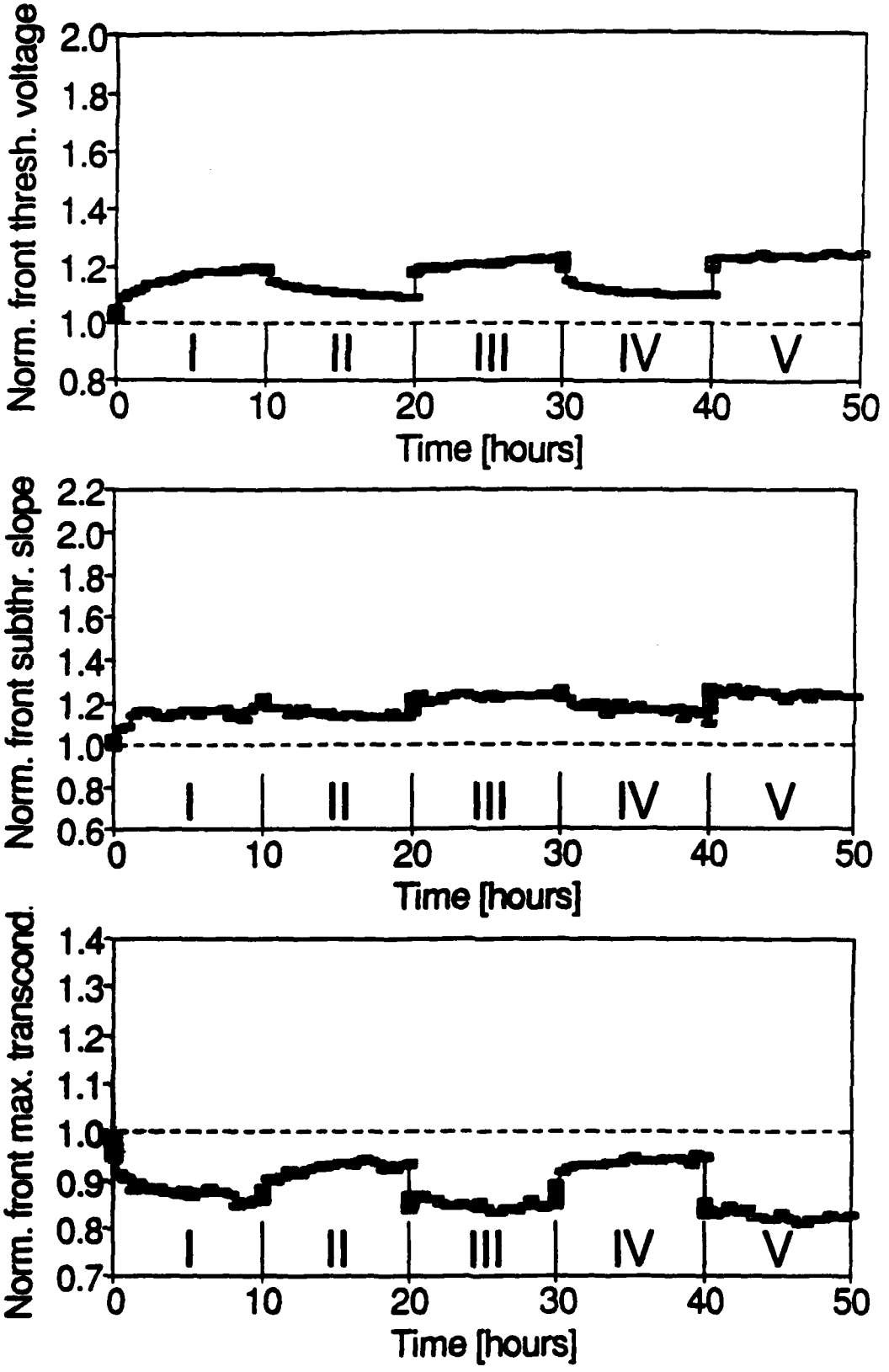
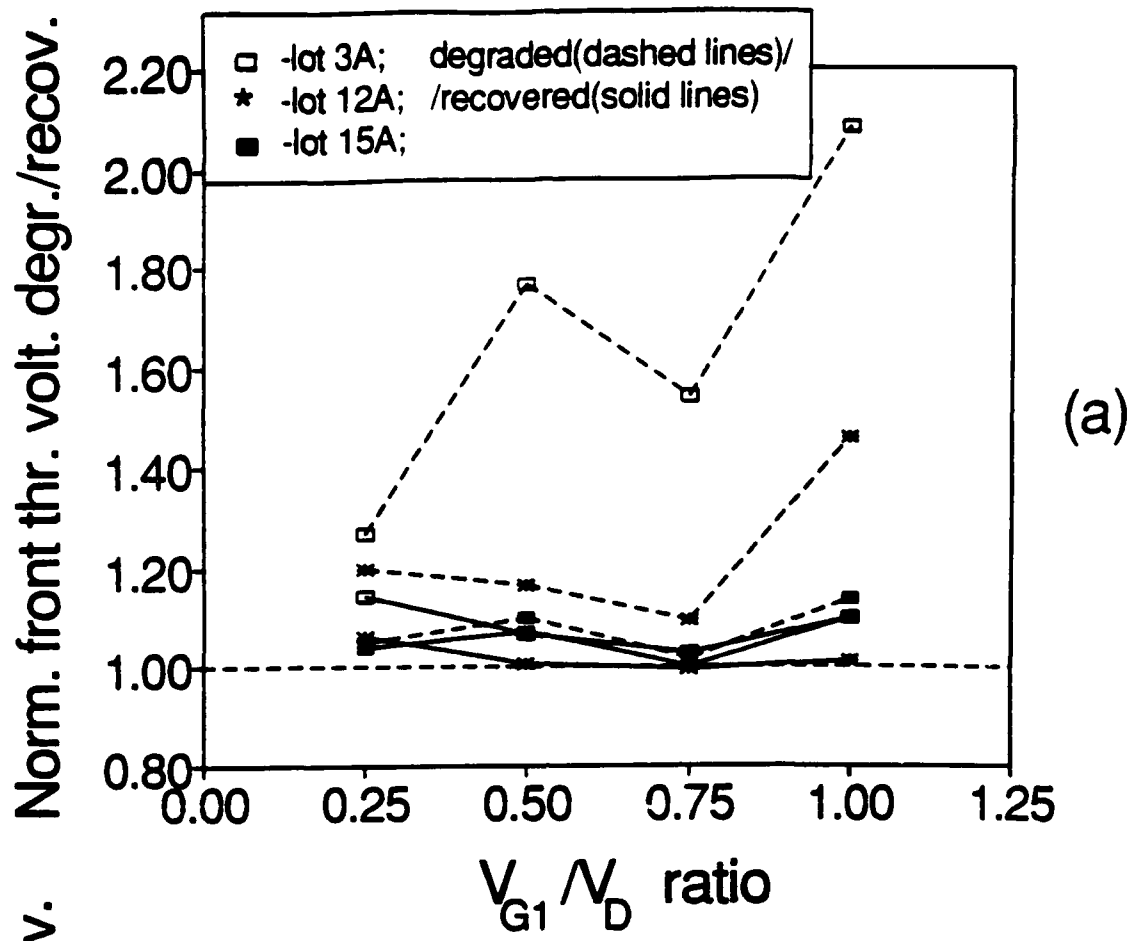
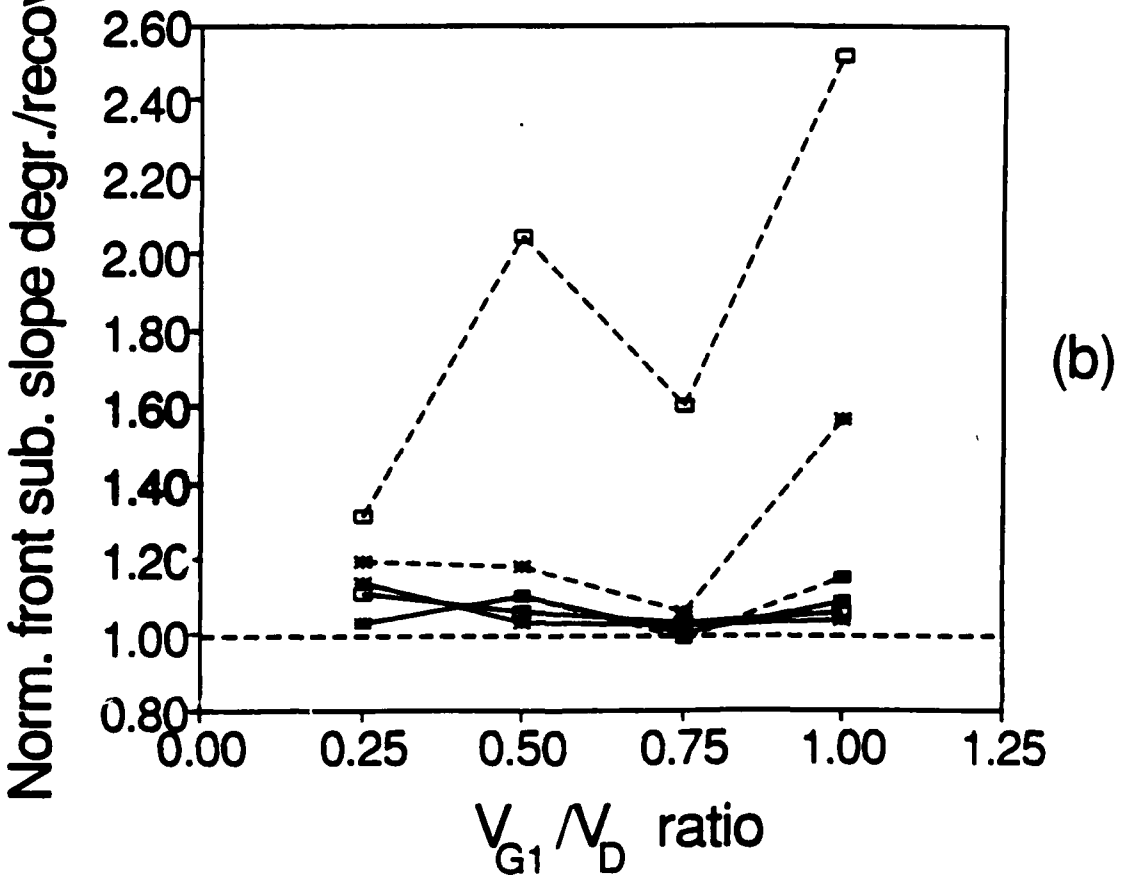

Norm. front thresh. voltage
2.0
1.8
1.6
1.4
1.2
1.0
0.8
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(a)
Norm. front subthr. slope
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(b)
Norm. front max. transcond.
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
I
II
III
IV
V
0
10
20
30
40
50
Time [hours]
(c)

Fig.10


-lot 3A; degraded(dashed lines)/
-lot 12A; /recovered(solid lines)
-lot 15A;
Norm. front thr. volt. degr./recov.
2.20
2.00
1.80
1.60
1.40
1.20
1.00
0.80
0.00
0.25
0.50
0.75
1.00
1.25
V_{G1}/V_D ratio

(a)


Norm. front sub. slope degr./recov.
2.60
2.40
2.20
2.00
1.80
1.60
1.40
1.20
1.00
0.80
0.00
0.25
0.50
0.75
1.00
1.25
V_{G1}/V_D ratio

(b)

Fig.11

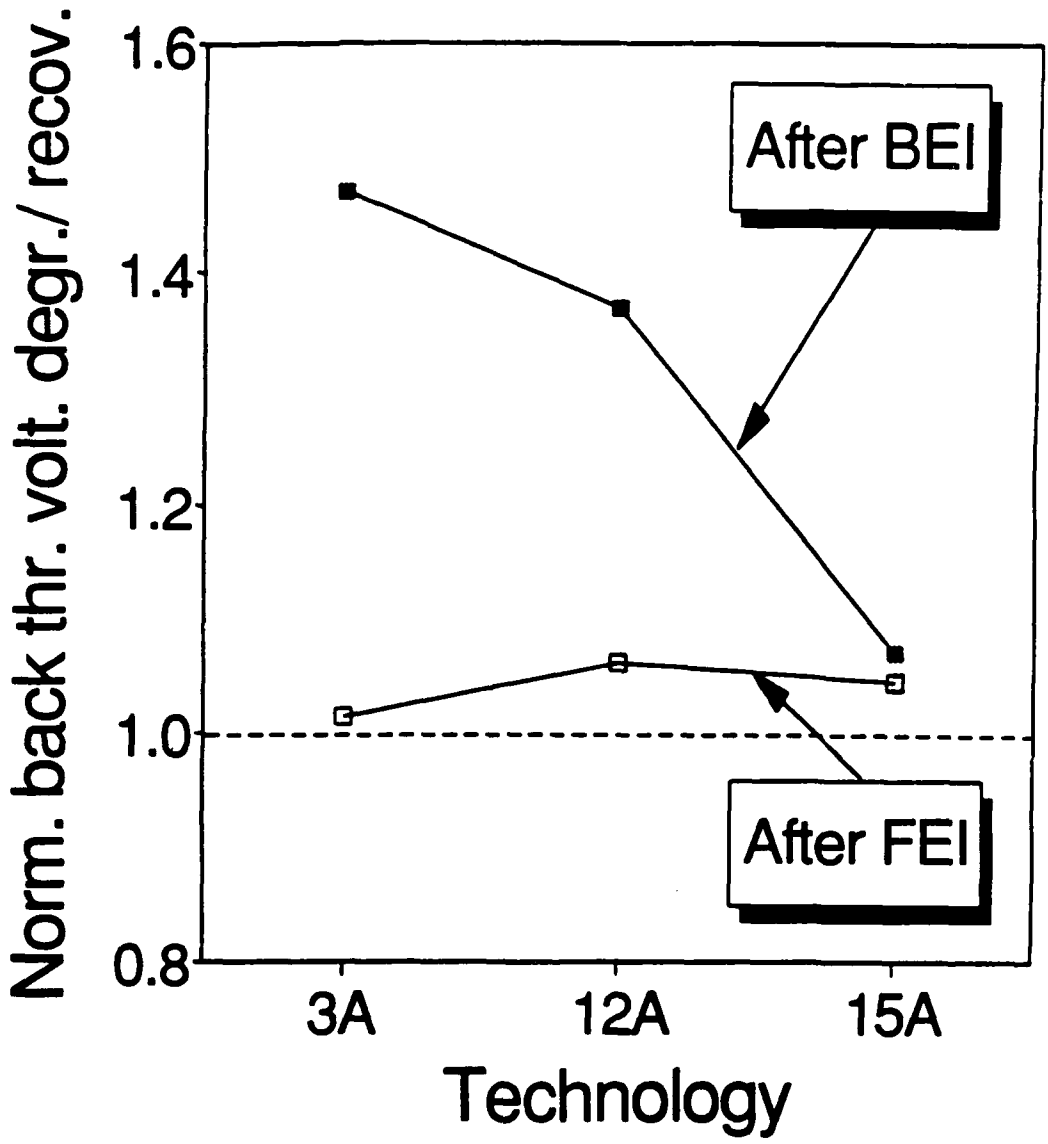

Norm. back thr. volt. degr./ recov.
1.6
1.4
1.2
1.0
0.8
After BEI
After FEI
3A
12A
15A
Technology

Fig.12

1993 IEEE INTERN. SOI CONF.

SUCCESSIVE CHARGING/DISCHARGING OF GATE OXIDES IN SOI MOSFET's BY SEQUENTIAL HOT ELECTRON STRESSING OF FRONT/BACK CHANNEL

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George Mason University, Fairfax, VA 22030
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As progress is being continuously made on various SOI technologies, there is an increasing need to address the reliability of MOSFET devices and circuits made by these technologies. With ever decreasing device dimensions, degradation caused by hot carriers is especially important. The ability to bias the front and the back gate independently, and the interaction of these two gates, makes the study of hot carrier degradation very challenging, and at the same time provides new opportunities. This interaction may for example result in degradation of a channel during hot carrier stressing of the opposite channel. However, opinion varies as to whether the opposite interface sustains actual damage, or it appears to be degraded through electrostatic coupling. The purpose of this work is to demonstrate that stressing one channel can in fact inject charges into the other channel, and discuss two important applications of this phenomenon: namely, that it can be used as a new tool for the study of the mechanisms of degradation, and for designing erasing schemes for SOI based flash memories. Our measurements were performed on partially and fully depleted SIMOX MOSFET's with LDD and channel lengths down to 0.6 μm.

Figures 1 and 2 show results obtained for a 0.8 μm channel length PD device, which was sequentially stressed for two hours under front channel hot-electron injection conditions (FEI), followed by two hours of back channel hot-electron injection conditions (BEI), and repeating the cycle for a total of thirty six hours. The full recovery of the front channel static characteristics rules out interface state generation during FEI and is caused by hole trapping during the BEI stress. This hole injection into the front gate oxide during back channel stressing is also responsible for the recovery of the front gate threshold voltage to its prestress value. From these and other experimental results as well as PISCES simulations it is concluded that the main cause of degradation is oxide charges trapped by intrinsic and/or induced oxide traps, and that the degradation is a two step process, of trap generation and trap filling. However, under low front gate voltage stress conditions, significant interface state generation also occurs.

Finally, the ability to inject hot-holes and discharge the opposite gate oxide may be explored for possible use in designing SOI flash memory cells with back-channel-based erasing schemes.

The work at George Mason University is supported by DNA through ONR Grant # N00014-91-J-1441.

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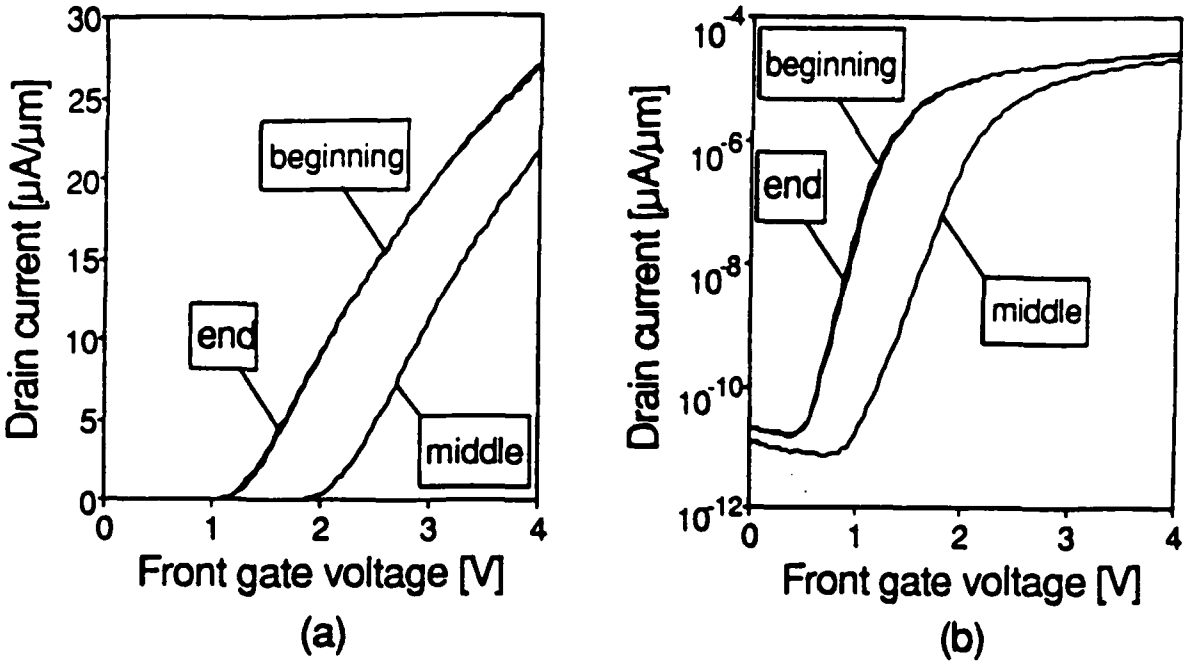

Fig.1: Static (a) I_D vs. V_{G1} and (b) I_D vs. V_{G1} characteristics of a 0.8 μm channel length PD transistor, at the beginning, middle, and the end of the third stress cycle, following hot-electron stressing of the back, front and back channel, respectively. V_D=0.1 V, and V_{G2}=-20 V.

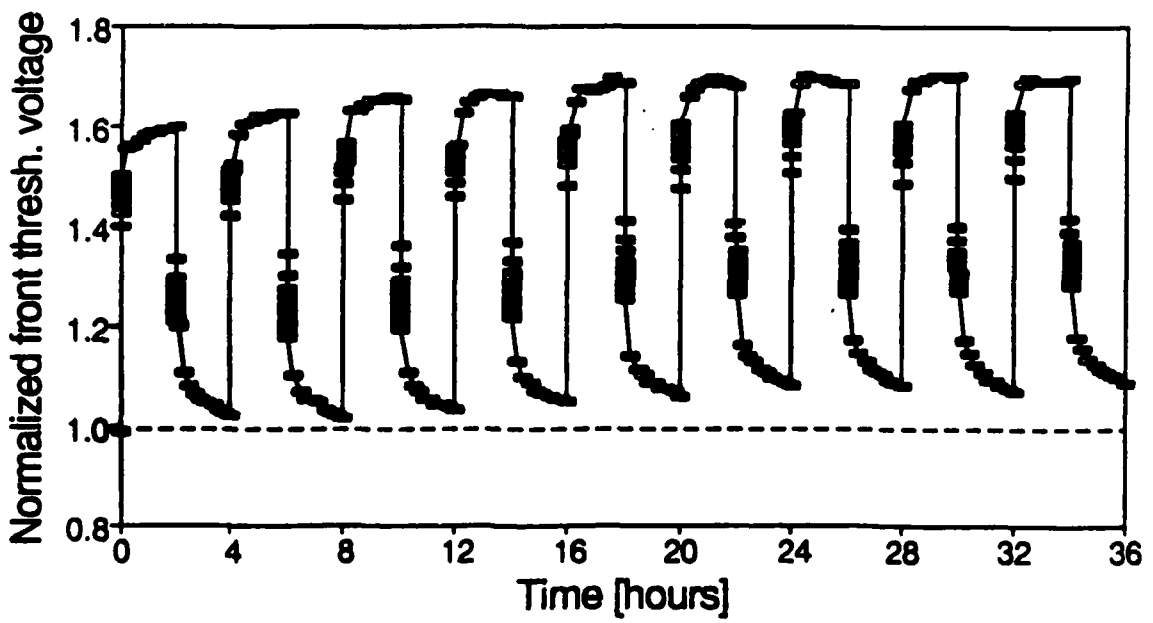

Fig.2: Front threshold voltage, normalized to its prestress values, throughout the duration of stress (nine stress cycles) for the same device as in Fig.1.

1993 IEEE INTERN. SOI CONF.

GENERATION LIFETIME MEASUREMENTS IN FULLY DEPLETED ENHANCEMENT AND ACCUMULATION MODE SOI MOSFETS

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Several techniques to measure the generation lifetime in SOI MOSFET's have been reported recently, based on the dual-gate Zerbst-type analysis[1]. For partially depleted devices the required deep depletion condition is easily achieved and the measurement is fairly straightforward[2]. For fully depleted devices, however, a more elaborate approach is required to obtain the required generation volume. A method was reported recently for enhancement mode fully depleted transistors[3], where the transients were analysed by using the temporal carrier distributions. The application of this technique, however, requires complicated measurements and data analysis. To our knowledge, no analysis has been reported for accumulation mode devices.

In this work we present a unified analysis for both enhancement and accumulation mode devices, by considering the temporal variation of the quasi-Fermi levels. This leads to an accurate determination of the generation volume, and to the following Zerbst-type expressions for the drain current transients for enhancement eqn.(1) and accumulation eqn. (2) mode devices, respectively:

$$\frac{(C_{oxb}+C_{si})}{2qn_iC_{si}^2}\frac{d}{dt}(KI_d+(V_{gf}-2\phi_f)C_{oxf})^2=\frac{t_{si}K}{\tau_gC_{si}}(I_{d\infty}-I_d) \qquad (1)$$

$$\frac{(C_{oxb}+C_{si})}{2qn_iC_{si}^2}\frac{d}{dt}(KI_d+V_{gf}C_{oxf})^2=\frac{t_{si}K}{\tau_gC_{si}}(I_{d\infty}-I_d) \qquad (2)$$

where $K=\frac{L}{\mu Z V_d}$ and the symbols have their usual meaning.

In accordance with the Zerbst methodology plotting the left-hand side (LHS) of the above equations as a function of $I_{d\infty}-I_d$ results in a straight line, the slope of which gives τ_g, the generation lifetime. Fig. 1 shows the drain current transient for an enhancement mode device obtained by stepping the back gate voltage from -6V to -20V, while keeping the front gate voltage at 2V and the drain voltage at

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.05V. The inset shows the corresponding Zerbst-type straight line fit according to eqn.(1), from the slope of which the lifetime is found to be $\tau_g = .7\mu s$. Fig. 2 shows the corresponding drain current transient for an accumulation mode device obtained from PISCES simulations assuming a lifetime of $\tau_g = .1\mu s$. The value obtained from the Zerbst-type straight line plot (inset) is $\tau_g = .09\mu s$, which is clearly in very good agreement with the assumed value.

The work at George Mason University is supported by DNA through ONR Grant # N00014-91-J-1441.

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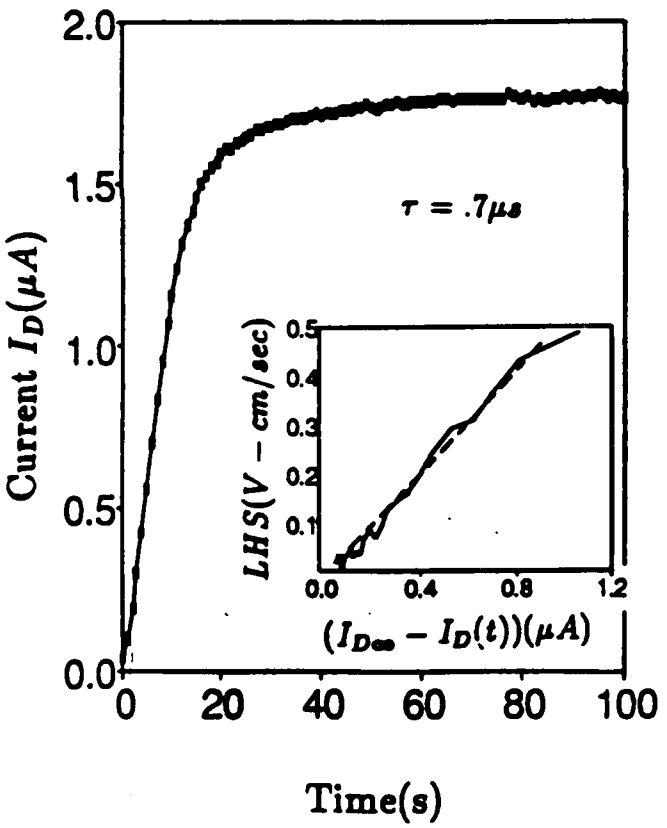

Fig. 1. Typical current transient and (inset) numerical analysis according to (1) for an enhancement mode device.

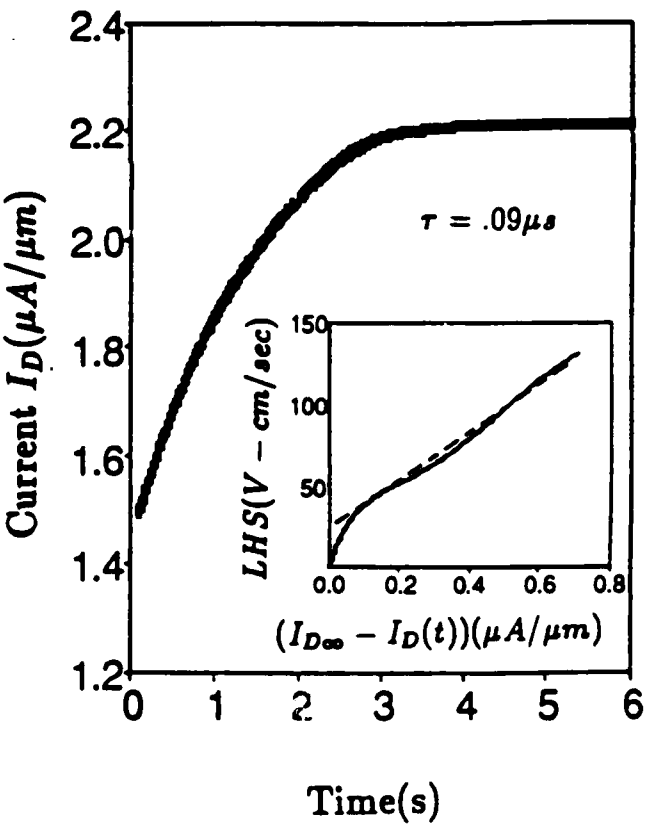

Fig. 2. Simulated (PISCES) current transient and (inset) numerical analysis according to (2) for an accumulation mode device

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Sequential Stressing of Front/Back Gate Oxides in SOI MOSFET's for Device Characterization and Applications

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Introduction

As progress is being continuously made on various SOI technologies, there is an increasing need to address the reliability of MOSFET devices and circuits made by these technologies. With ever decreasing device dimensions, degradation caused by hot-carriers is especially important [1]. The ability to bias the front and the back gate independently and the interaction of these two gates makes the study of hot-carrier degradation in SOI MOSFET's very interesting and provides new opportunities. For example this interaction may result in degradation of a channel during hot-carrier stressing of the opposite channel. However, opinion varies as to whether the opposite interface sustains actual damage, or does it appear to degrade through electrostatic coupling. The purpose of this work is to demonstrate that stressing one interface can inject charges into the opposite interface, and to discuss two important applications of this phenomenon: namely, that it can be used as a new tool for studying of the mechanisms of degradation, and it can be applied to the design of novel erasing schemes for SOI-based flash memories. Our experiments were performed on partially and fully depleted SIMOX MOSFET's with LDD's and channel lengths down to 0.6 μm.

Results and discussion

Figure 1 demonstrates how the sequential stressing of front/back gate oxide influences the front/back threshold voltages $V_{T1,2}$ [2]. Sequentially applied front high V_{G1} electron injection (FEI) and back electron injection (BEI) conditions cause V_{T1} and V_{T2} to increase and decrease respectively. For the sample in Fig.1, V_{T1} increases during FEI (period I) and recovers completely during the following BEI (II). Similarly, the V_{T2} increases during BEI (II) and shows partial recovery during the subsequent FEI (III). Stress conditions suggest that the reason for the observed threshold voltages recovery is hot-holes created by impact ionization at one interface and injected into the gate oxide of the opposite interface, accumulated during stress. To eliminate other possible mechanisms of electron detrapping (i.e. Fowler-Nordheim detrapping across the gate-to-drain overlap region [3]), an additional "cross-check" is performed by making the experiments described in Fig.2. It is clear in Fig.2 that a significant $V_{T1,2}$ recovery requires the actual opening of the opposite channel which confirms that the recovery is by hot-holes created at the opposite interface. Figures 3 and 4 show examples of the extent of the transistor parameters recovery for different technologies. From Fig.3 we conclude that the electron trapping dominates other degradation mechanisms during front channel stressing, especially at high V_{G1}. The ability to overshoot the V_{T1} recovery for two other technologies (Fig.4) indicates that a very

efficient hot-holes injection can be obtained using the described procedure. In Fig.5, D_{it} for the front interface increases after low V_{G1} front channel stressing (FHI). This is consistent with the results in Fig.3. for which a part of the damage was not recoverable after the low V_{G1} stressing. Finally, in Fig.6 we determine the trapping time constants that are observed in Fig.1a. The changes of V_{T1} during period I (FEI) can be best fit [4] with one time constant, whereas for the following FEI period III a second time constant has to be added, suggesting two processes involved in the electron trapping. The identical situation occurs at the back interface. From these and other experimental results as well as PISCES simulations it is concluded that the main cause of degradation is oxide charges trapped by intrinsic and/or induced oxide traps, and that the degradation is a two step process, of trap generation and trap filling. On the other hand, under low V_{G1} stress conditions, significant interface state generation also occurs.

The ability to inject hot-holes and discharge the opposite gate oxide may be explored for possible use in designing a SOI flash EPROM memory cell [5] with a back-channel-based erasing scheme. This approach may offer several important advantages with respect to the front-interface-based erasing schemes presently used in bulk technology: (1) no big electric field is required across the tunneling (front) oxide, or across the front channel (result: bigger endurance), (2) the erasing scheme is built-in into the cell (result: smaller dimensions), (3) because channel hot-holes (rather than Fowler-Nordheim ones) are being used, this back-channel-based erasing might have self-convergence capabilities [6]. We see also some challenges due to the: (1) big voltages required to bias the back interface (they should be greatly reduced with buried oxide thicknesses going below 1000 Å), (2) significant electron trapping in the buried oxide (clearly technological disadvantage that should disappear with advancing technology), (3) poor yield (comparing to bulk) obtained for device fabrication on SOI substrates presently.

Conclusion

A new evaluation methodology to study the hot-carrier effects in SOI MOSFET's was presented. The metodology takes advantage of front/back gate coupling effects and enables to separate charge trapping from interface state generation. Also, it provides further insight into the oxide traps generation process. Ability to exploit hot-hole injection from the back interface in SOI MOSFET's to erase information in flash EPROM memories was also demonstrated and discussed.

Acknowledgements

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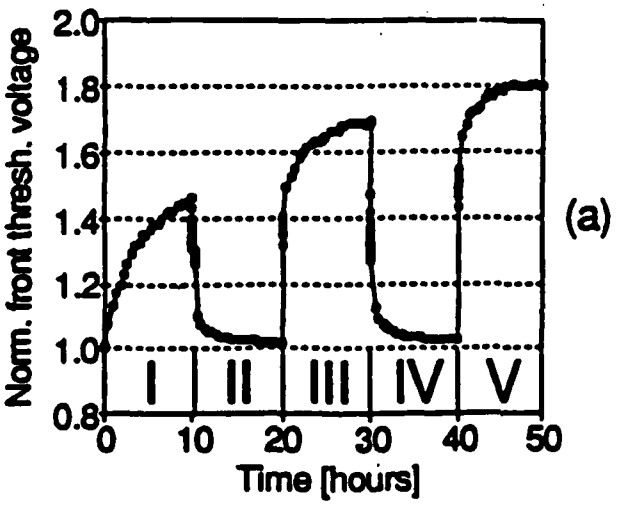
	FEI	BEI	FEI	BEI	FEI
Vd [V]	8	7.5	8	7.5	8
Vg1 [V]	8	-2	8	-2	8
Vg2 [V]	-20	75	-20	75	-20



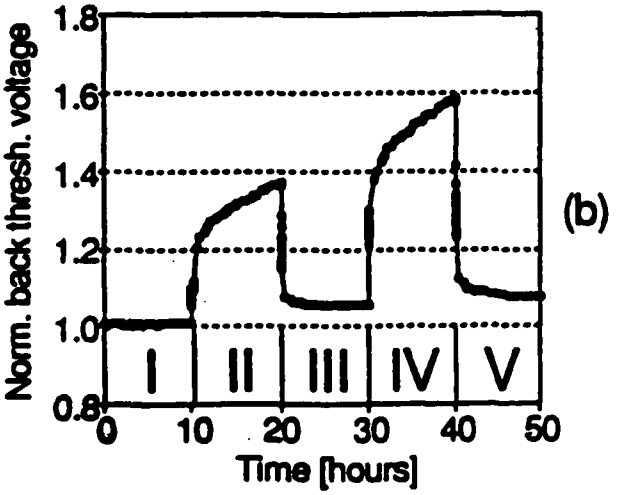
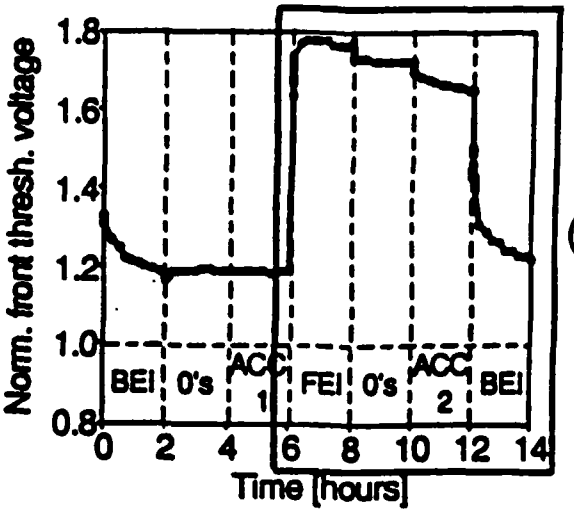


Fig.1. Demonstration of the sequential stressing effect: front (a) and back (b) channel normalized threshold voltage changes during sequential front/back channel hot-electron stressing (I, III, V - FEI, II, IV - BEI; values are at the top of the figure).

	BEI	0's	ACC 1	FEI	0's	ACC 2	BEI
Vd [V]	7.5	0	8	8	0	7.5	7.5
Vg1 [V]	-2	0	-2	8	0	-2	-2
Vg2 [V]	75	0	-20	-20	0	-20	75



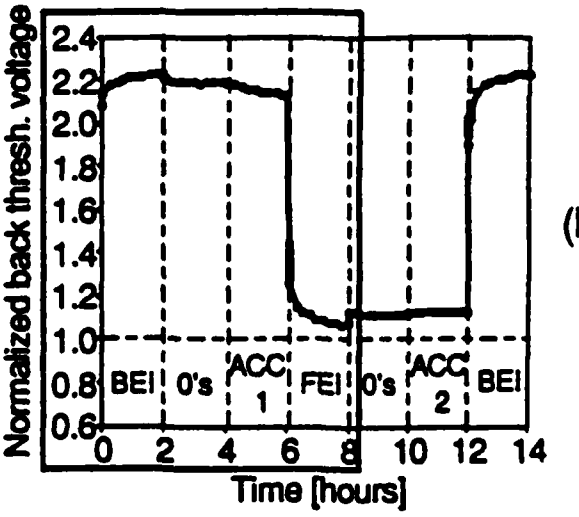


Fig.2. Check-up stressing sequence for the front (a) and back interface (b), to pinpoint the reason of the $V_{T1,2}$ recovery in Fig.1. The applied voltages are at the top of the figure. Comparison of the $V_{T1,2}$ changes during stresses ACC 2 and BEI for the front (a), and ACC 1 and FEI for the back (b) clearly identify opening of the opposite channel as a condition for the significant threshold voltage recovery.

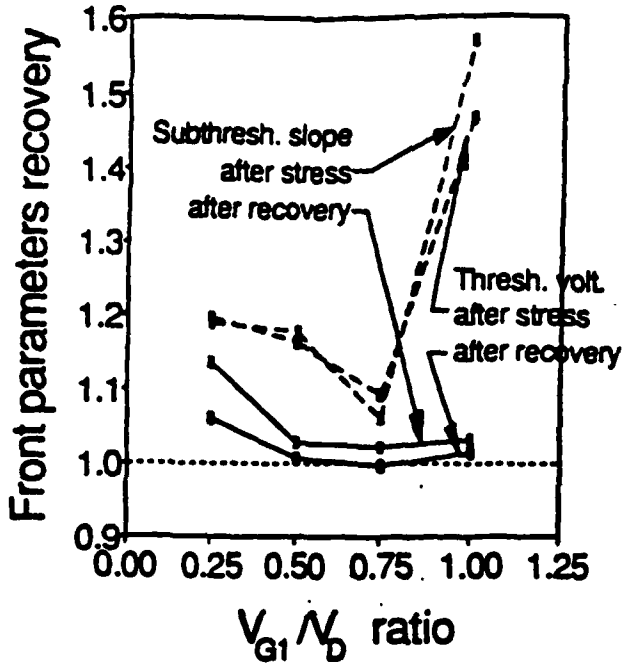


Fig.3. Front threshold voltage and subthreshold slope changes following front channel stress and subsequent BEI as a function of V_{G1}/V_D ratio during the front channel stress. For high V_{G1} both V_{T1} and subthreshold slope recover almost completely but only partial recovery is observed for low V_{G1} stress.

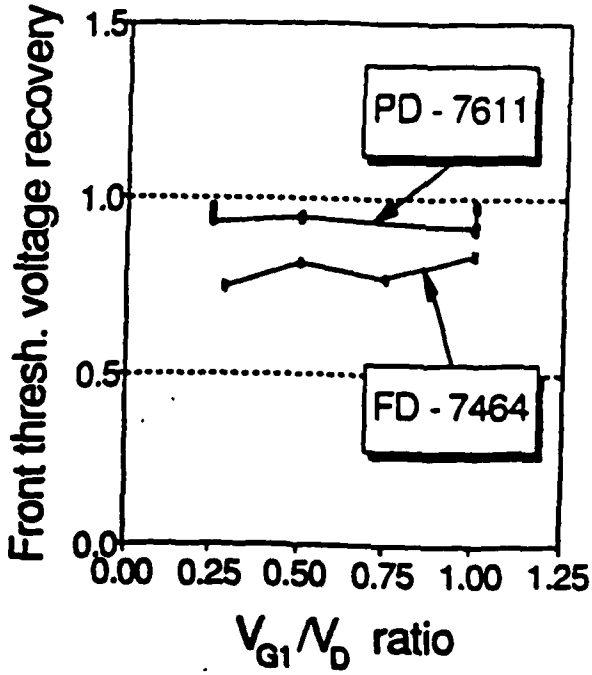


Fig.4. Front threshold voltage recovery of two technologies for which V_{T1} overshoots below its pre-stress value after BEI following front channel stress, as a function of V_{G1}/V_D ratio during the front channel stress.

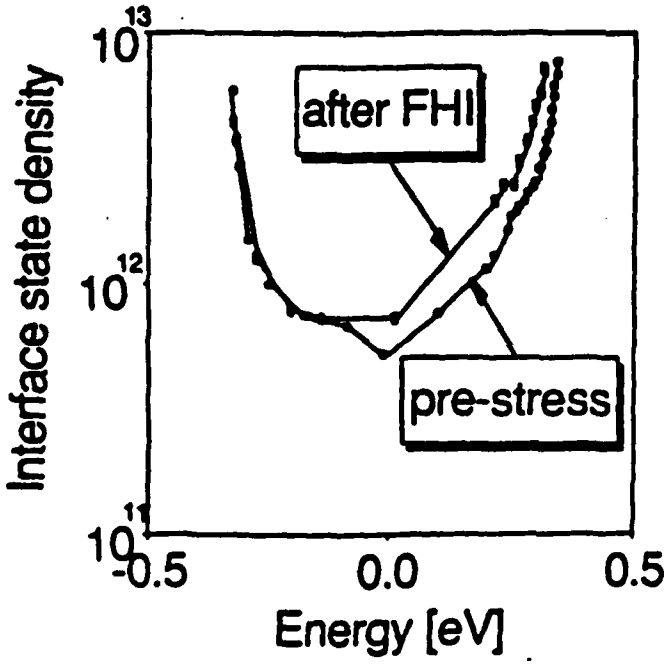


Fig.5. Typical front interface state density D_{it} vs. energy profile *before* and after front low V_{G1} hole-injection stress (FHI).

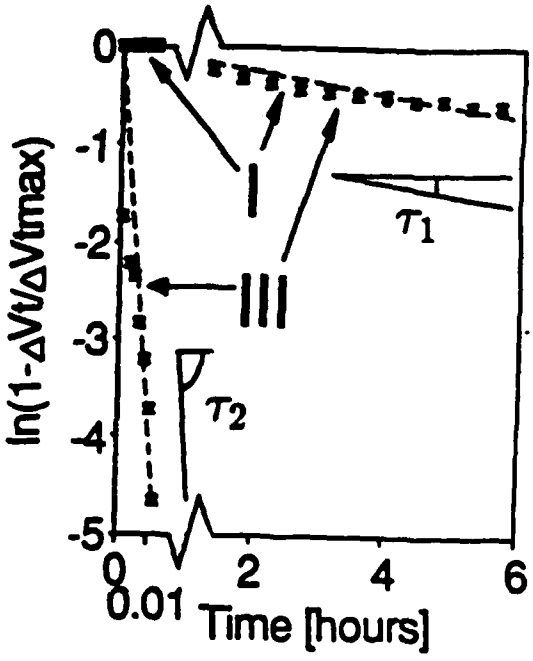


Fig.6. Analysis of data from Fig.1a (periods I and III). Best fit is obtained for period I with one time constant τ_1. For period III two different time constants are required $\tau_{1,2}$. We link these both time constants with oxide trap creation τ_1, and oxide trap filling τ_2 processes. As it can be seen oxide trap creation constants τ_1 overlap for stresses I and III.

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Investigation of Carrier Generation in Fully Depleted SOI MOSFETs

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Introduction

The recent progress achieved in the quality of fully depleted SOI crystals is in part due to the development of adequate techniques of characterization . However, little information is available on the generation/recombination properties of SOI material, which are known to affect greatly the performance of both CMOS and Bipolar devices. Techniques based on dual gate Zerbst type analysis has been presented for partially depleted devices [1], where obtaining the generation volume is fairly straightforward. For fully depleted devices, however, a more elaborate approach is required to obtain this generation volume. Recently a technique for enhancement type fully depleted devices was presented which analyzed the temporal carrier distribution across the silicon film [2]. The application of this technique requires complicated measurements and data analysis.

In this paper we present a simple unified approach to determine the generation lifetime in both enhancement as well as accumulation mode SOI MOSFETs based on analysis of the temporal variations of the quasi-Fermi levels , leading to Zerbst type expressions for the drain current transients. PISCES simulations have been performed to obtain simulated transients and the validity of the analysis is verified by applying the technique to the simulated transient and comparing the extracted lifetime to the one used in simulation. Finally , experimentally obtained transients are presented for both kinds of devices and they are analyzed by the technique to extract the lifetime.

Analysis

We consider an accumulation mode N^+NN^+ structure biased with a positive voltage at the front gate such that the front surface is accumulated and a negative voltage is applied at the back gate such that the back surface is inverted. This ensures that in equilibrium the front surface potential is pinned at zero and the back surface potential is pinned at $2\phi_F$. A negative step voltage is now applied to the back gate. This disturbs the structure from equlibrium and creates a demand for holes at the back surface. Since there can be no supply of holes from the source/drain regions the demand can be met only by the generation of holes in the silicon film which relaxes the structure towards equilibrium. The generation rate can be expressed as

$$G = \frac{n_i}{\tau_g} W_g = \frac{d}{dt} N_{hole} \tag{1}$$

where W_g is the effective generation width, N_{hole} is the net hole concentration in the silicon film, and τ_g is the generation lifetime of the material. For devices with moderate doping and thin films, which are typical of modern SOI material, the linear potential variation (LPV) approximation has been shown to be valid [3]. Hence assuming a linear variation of the potential across the silicon film the effective generation

width, at any instant of time, can be expressed as

$$W_g(t) = \frac{t_{si}}{\psi_b(t)}(\psi_b(t) - \psi_{bo\infty}) \tag{2}$$

where $\psi_b(t)$ is the back surface potential at any instant and $\psi_{bo\infty}$ is its equilibrium value and t_{si} is the silicon film thickness. Applying Gauss's law at the front interface we get (with front surface potential as zero),

$$-\psi_b C_{si} - C_{ox f} V_{gf} = -qN_{elec} \tag{3}$$

Similarly applying Gauss's law at the back interface we get

$$C_{oxb}(\psi_b - V_{gb}) + C_{si}\psi_b = qN_{hole} \tag{4}$$

where N_{elec} and Q_{hole} are the total electron and hole concentrations in the silicon film respectively and other symbols have their usual meanings. Using eqn.(3) the drain current can be expressed as

$$I_d = -\frac{1}{K}(\psi_b C_{si} + V_{gf} C_{ox f}) \tag{5}$$

where $K = \frac{L}{\mu Z V_d}$. Using this expression the effective generation width, W_g in eqn.(2) can be expressed in terms of the drain current as

$$W_g = t_{si}\frac{(I_{do\infty} - I_d(t))}{I_d(t)} \tag{6}$$

where $I_{do\infty}$ is the equilibrium value of the drain current. Fig.1 shows a comparison of the effective generation widths as obtained from eqn.(6) with its value extracted from PISCES , as a function of time during which the structure relaxes towards equilibrium. Using eqns.(4), (5) and (6) the continuity equation for holes, eqn.(1), can be expressed as

$$\frac{(C_{oxb} + C_{si})}{2qn_i C_{si}^2}\frac{d}{dt}(KI_d + V_{gf}C_{ox f})^2 = \frac{t_{si}K}{\tau_g C_{si}}(I_{do\infty} - I_d) \tag{7}$$

Using a similar analysis for the enhancement mode devices the continuity equation for electrons can be expressed as

$$\frac{(C_{oxb} + C_{si})}{2qn_i C_{si}^2}\frac{d}{dt}(KI_d + (V_{gf} - 2\phi_f)C_{ox f})^2 = \frac{t_{si}K}{\tau_g C_{si}}(I_{do\infty} - I_d) \tag{8}$$

In accordance with the Zerbst methodology plotting the left-hand side(LHS) of the above equations as a function of $(I_{do\infty} - I_d)$ results in a straight line, from the slope of which τ_g, can be evaluated.

Simulation and Experiment

Simulations of transients were performed, using the PISCES device simulator, on typical accumulation and enhancement mode device structures. Fig.2 shows a typical transient obtained from PISCES for an accumulation mode N^+NN^+ structure assuming a lifetime of $\tau_g = .1\mu s$. The back gate was stepped from -6V to -20V while the front gate was biased at 2V.The inset shows the corresponding Zerbst-type straight-line fit according to eqn.(7), from the slope of which the lifetime is found to be $.09\mu s$ which is clearly in good agreement with the assumed value. Experimental transients were obtained for both accumulation and enhancement mode devices as shown in Fig.3 and Fig.4 respectively. The conditions of the experiment for both devices were same as that used in the simulations above. Zerbst type plots (shown in the insets) were made according to eqn.(7) and eqn.(8) for the accumulation and enhancement mode devices respectively. The lifetime obtained for the accumulation mode device was $\tau_g = .1\mu s$ and that for the enhancement mode device was $\tau_g = .7\mu s$.

Conclusion

An unified Zerbst-type technique has been developed to extract the generation lifetimes in both accumulation and enhancement mode fully depleted SOI MOSFETs. PISCES simulations have been performed to verify the validity of the technique which has been shown to give reasonably accurate results. Finally the technique has been applied to measured transients of both types of devices to extract the generation lifetimes.

Acknowledgements

The work at George Mason University is supported by DNA through ONR Grant # N00014-91-J-1441.

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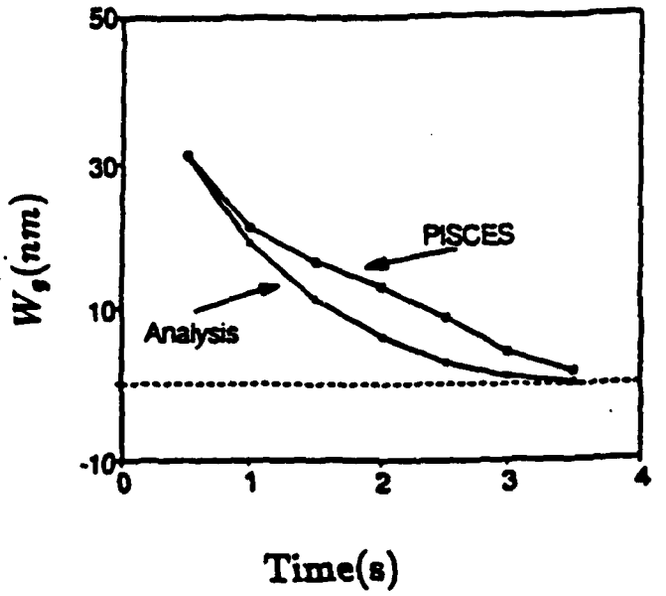

Fig. 1. Temporal variation of effective generation width W_g as predicted by the analysis and that obtained from PISCES.

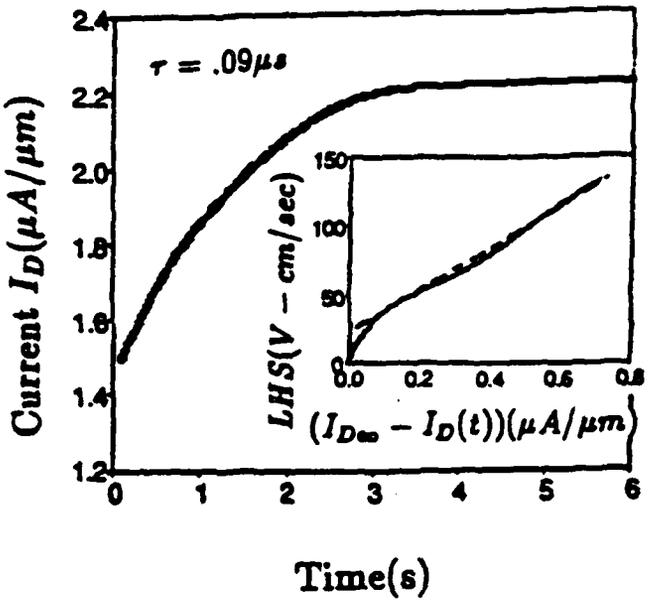

Fig. 2. Simulated (PISCES) current transient and (inset) numerical analysis according to (7) for an accumulation mode device

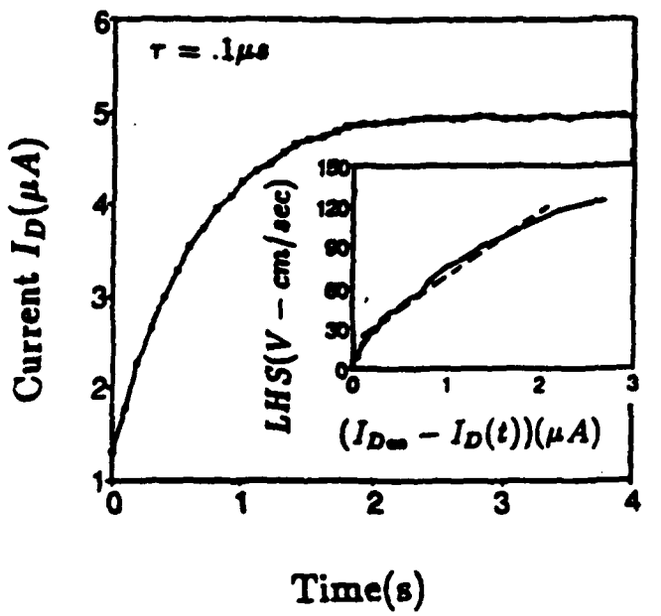

Fig. 3. Measured current transient and (inset) numerical analysis according to (7) for an accumulation mode device

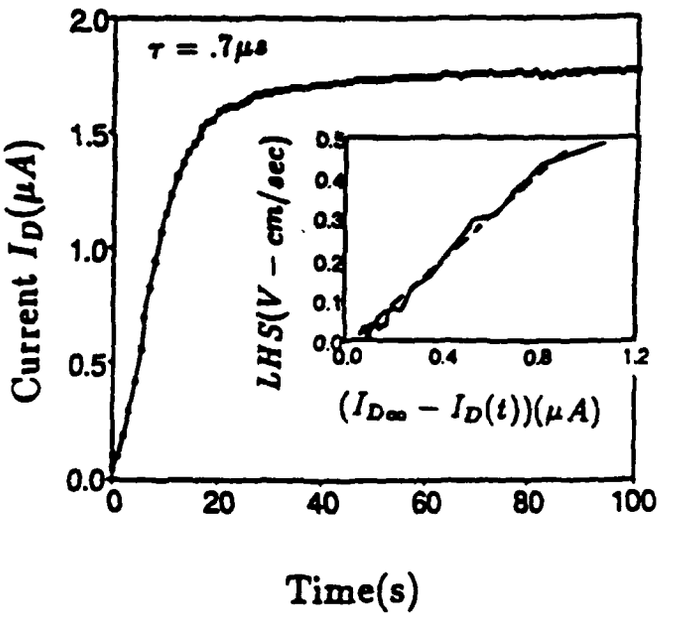

Fig. 4. Measured current transient and (inset) numerical analysis according to (8) for an enhancement mode device.