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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The contract was given tentative funding approval on November 8, 1993. At that time work on Phase 1 of the contract started. The contract was formally approved December 30, 1993. During the first three months of the contract efforts have centered on planning and scheduling the Phase 1 projects and beginning work on the defined tasks. Progress was made in the definition and design of the CNAPS/PC hardware board (image processing accelerator board that plugs into a PC) that will be developed during Phase 1. Likewise, progress was made in the initial design and prototyping of the software to be developed in this phase of the project.

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22a. NAME OF RESPONSIBLE INDIVIDUAL: Wendell Henry	22b. TELEPHONE (Include Area Code): (503) 690-1236
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R & D Status Report

February 22, 1994

ARPA Order No.:

A407

Contractor:

Adaptive Solutions, Inc.

1400 NW Compton Drive, Suite 340

Beaverton, OR 97006

Contract No.:

N00014-93-C-0234

Contract Amount:

$1,299,714.00

Effective Date of Contract:

November 8, 1993

Expiration Date of Contract:

June 7, 1996

Principal Investigator:

Wendell A. Henry

Telephone Number:

(503) 690-1236

Title of Project:

High Performance Hardware and Software for Pattern Recognition and Image Processing

Title of Work:

R&D Status Report

Reporting Period:

November 8, 1993 through January 31, 1994

Disclaimer

The views and conclusions contained in this document are those of the authors and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the Advanced Research Projects Agency of the U. S. Government.

Project Summary:

The contract was given tentative funding approval on November 8, 1993. At that time work on Phase 1 of the contract started. The contract was formally approved December 30, 1993. During the first three months of the contract efforts have centered on planning and scheduling the Phase 1 projects and beginning work on the defined tasks. Progress was made in the definition and design of the CNAPS/PC hardware board (image processing accelerator board that plugs into a PC) that will be developed during Phase 1. Likewise, progress was made in the initial design and prototyping of the software to be developed in this phase of the project.

Phase 1 (11/8/93 - 6/30/94) Deliverables

Ten working copies of the CNAPS/PC board each configured with 64 processors.

Ten user licenses to the PC version of the CNAPS-C software development environment.

Support and maintenance for one year with each hardware board and software license.

Phase 2 (7/1/94 - 4/30/95) Deliverables

Ten user licenses to the PC version of the CodeNet software development environment.

Ten user licenses to the PC version of the BuildNet software development environment.

Support for one year with each CodeNet and BuildNet software license.

Phase 3 (5/1/95 - 6/7/96) Deliverables

Ten copies of source code and documentation for an application library of C++ functions to facilitate the development of applications utilizing neural network, pattern recognition, and image processing algorithms for execution on the CNAPS/PC hardware board.

Description of Progress:

This is the first reporting period of the project. Progress was made in both the hardware and software areas. The following sections discuss the specific progress in each area.

Hardware

Definition and planning:

The project scheduling and plan for the CNAPS/PC board was completed. Also, revision 2.0 of the functional specification document for the CNAPS/PC board was completed. High-level block definition, cost, power, and area estimates for the CNAPS/PC board were completed. An ISA driver Verilog model for use during the CNAPS/PC board design and logic simulation was located and obtained.

Design:

Significant progress on the design of the CNAPS/PC board was made. Implementation details and complete schematics were entered into the Cadence Schematic editor. Significant progress was made on the RTL-level modeling and simulation of the design. The logic required to perform bus access to DRAM, SRAM, and the CSC from the

ISA bus and the mezzanine board interface was modeled and simulated. The netlist of the board design was generated and the design was prepared for component place and route. Initial logic synthesis of the FPGA and its place and route was also completed.

Testing:

A simulation verification test plan was developed and test generation began. The logic simulation test environment was defined and put into place. Data accesses from the ISA bus and from a mezzanine board to/from DRAM, SRAM, and the CSC were successfully tested and verified.

Software

Definition and planning:

The first version of the functional specification document for the preprocessor for the CNAPS-C compiler (C compiler for the CNAPS architecture) was completed. The project plan and functional specification document for the port of the CNAPS/PC control software (OEMlib) to the DOS/Windows environment was completed. Also, the first version of the functional specification document for the (non-graphical) CNAPS-C source-level debugger was completed.

Design and implementation:

The engineer working on the graphical interface to the CNAPS-C debugger attended a week-long training class on the use of the Galaxy graphical interface builder which will be used to port the current CodeNet tool to the DOS/Windows environment.

The re-design of the CNAPS-C debugger to operate in the OEMlib environment was completed. Implementation of the command-line version of the redesigned debugger has been started. Work on the control software (OEMlib) required to interface the software with the CNAPS/PC board was started.

Plans For Next Reporting Period:

During the next three months work will continue on Phase 1 of the contract and the following is expected to be achieved:

1. Complete the design of the CNAPS/PC board
2. Complete fabrication and assembly of the first prototype of the CNAPS/PC board
3. The CNAPS/PC board will be undergoing debug and test
4. The preprocessor for the CNAPS-C compiler will have been completed and in test
5. The control software for the CNAPS/PC board will have been completed and in test
6. The CNAPS-C source-level debugger will still be in implementation.

Fiscal Status:

Amount currently provided on contract:	$1,299,714.00
Expenditures and commitments to date:	67,277.17
Funds required to complete work:	$1,232,436.83

Phase 1 funding:	$300,000.00
Expenditures and commitments to date:	67,277.17
Phase 1 funds remaining:	$232,722.83