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The first workshop on nanostructures for optoelectronics was held as scheduled. The abstracts are contained in the final report.

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FIRST WORKSHOP ON NANOSTRUCTURES FOR OPTOELECTRONICS

ABSTRACTS & PROGRAM

August 13-15, 1992
Griffin Commons, Sunset Village
University of California, Los Angeles
330 DeNeve Drive

Sponsored by the US Army Research Office

ARO Nanostructure Workshop
University of California, Los Angeles
Griffin Commons, Sunset Village
Los Angeles, CA 90024

Program

August 13, 1992 (Thursday)

1:00 - 5:00 p.m. Registration/Check-In

5:00 - 7:00 p.m. Dinner - Rieber Hall Dining Room

August 14, 1992 (Friday)

Study Lounge Room, Second Floor

7:00 - 8:00 a.m. Breakfast - Rieber Hall Dining Room

8:15 a.m. Introduction: Dr. John Zavada

8:30 a.m. A1. Nanoelectronics: Past, Present, and Future
Robert T. Bate, Texas Instruments (Retired)

9:15 a.m. A2. Nanostructures for Microelectronics and Integrated Optoelectronics: How to Insert Nanoscale without Giga $$
Richard Higgins, Georgia Institute of Technology

10:00 a.m. BREAK

10:30 a.m. B1. Light-Emitting Properties of Porous Silicon
Joe C. Campbell and Dim-Lee Kwong, Microelectronics Research Center, University of Texas at Austin

11:00 a.m. B2. Fabrication of Si Nanostructures for Light Emission Study
H.I. Liu, N.I. Maluf, R.F.W. Pease, Stanford Solid State Lab, Stanford University

11:30 a.m. B3. Effect of Doping on Photoluminescence in Porous Silicon Nanostructures
Andrew J. Steckl, J. Xu, and H.C. Mogul, Nanoelectronics Laboratory, University of Cincinnati

12:00 - 1:00 p.m. LUNCH - Rieber Hall Dining Room

1:00 p.m. C1. NNF Lithography Technologies for Nanoscale Optoelectronics
J.M. Ballantyne, School of Electrical Engineering, Cornell University

1:30 p.m. C2. X-ray Nanolithography for Optoelectronic Integrated Circuits
Henry I. Smith, Dept. of ECE, MIT

2:00 p.m. C3. Field Ion Emission of Silicon Adatoms from Different Sites of Si(111) 7x7 by STM
H. Uchida, D.R. Huang, F. Gray, and **Masakazu Aono**, Surface and Interface Laboratory, RIKEN Institute, Saitama, Japan

2:30 p.m. BREAK

3:00 p.m. D1. Integration of STM-Based Nanofabrication/ Characterization and Electronics Device Processing
John A. Dagata and W. F. Tseng, NIST, Gaithersburg, Madison

3:30 p.m. D2. Fabrication and Characterization of Metal-Semiconductor Nanostructures
Dror Sarid and S. Howells, Optical Science Center, University of Arizona at Tuscon

4:00 p.m. D3. Atomic Layer Epitaxy for Nanostructures
Salah M. Bedair, ECE Dept., No. Carolina State University

4:30 p.m. D4. In-Situ Growth Controlled Approaches to Semiconductor Nanostructures: An Assessment
Anupam Madhukar, Photonic Materials & Devices Laboratory, USC

5:00 p.m. D5. Mesoscopic Band Gap Engineering in Quantum Well Structures by Molecular Beam Epitaxy-Focused Ion Beam In Situ Processing
Pierre Petroff, Materials Dept., UC, Santa Barbara

5:30 p.m. D6. Silicon Germanium Superlattices and Meso Structures
Kang L. Wang, Electrical Engineering Dept., UCLA

6:00 - 6:30 p.m. COCKTAILS/ RECEPTION (Terrace - Third Floor)

6:30 - 8:00 p.m. DINNER (Terrace - Third Floor)

August 15, 1992 (Saturday)

West Coast Conference Room, Third Floor

7:00 - 8:00 a.m. Breakfast - Rieber Hall Dining Room

8:30 a.m. E1. Serpentine Superlattice Quantum Wires--Growth and Optical Properties
James L. Merz, Dept. of ECE, UC, Santa Barbara

9:00 a.m. E2. Ferroelectronic Thin Films Based Devices and Structures in Optoelectronic Computing System
Volkan H. Ozguz, ECE Dept., UC, San Diego

9:30 a.m. E3. Atomic Asperity Tunnel Junction Devices
Steve Gregory, Physics Dept., University of Oregon

10:00 a.m. BREAK

10:30 -11:00 a.m. Short Unscheduled Talks

11:00 -11:20 a.m. F1. Report on Si Workshop by Joe C. Campbell
11:20 -11:40 a.m. F2. Report on ALE Conference by Salah Bedair
11:40 -12:00 a.m. F3. Report on Santa Barbara Workshop by Louis Lome

Closing Remarks
by John Zavada

12:00 - 1:00 p.m. LUNCH, Rieber Hall Dining Room

A1.

Nanoelectronics: Past, Present, and Future

Robert T. Bate

Texas Instruments (retired)
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Richardson, TX 75081-9664

Abstract

The major driving force behind the progress in electronic systems and the continuing pervasiveness of integrated circuits has been the ability to downscale minimum feature sizes. This had permitted the cost, size, and power dissipation of integrated circuits to remain relatively constant while their functionality has increased by many orders of magnitude. Anticipated physical limitations indicate that this trend cannot continue beyond the end of the century, unless a revolutionary technology permits downscaling to continue.

In response to this need, a potential IC technology employing nanoscale tunneling devices in limited interconnect architectures is being developed at Texas Instruments and elsewhere. In this talk, I will review the history of this activity, with emphasis on how the constraints dictate the choices of technology, discuss the current status, and project progress over the next decade, concluding with some suggestions concerning systems which this technology may enable.

Since individual devices in this scheme will be 10 - 50 times smaller than the wavelength of light, one might be tempted to conclude that optics has no role to play in it. To the contrary, I will show that optical techniques may provide the solutions to two difficult problems: synchronization and enabling the programming mode.

Probably one of the most important considerations is temperature of operation. Present military integrated circuits function up to 125C. However it is not clear that all classes of quantum devices can ever meet this requirement. The

need for significant additional cooling capacity for quantum devices would negate the cost advantages of increased functional density.

In order to keep the cost of integrated circuits from rising substantially while downscaling continues, it would appear necessary to use, insofar as is possible, the manufacturing facilities already in place when the current technology matures to manufacture the new circuits. Since these are based on silicon technology, a silicon-based quantum device technology would have a much greater chance of success in supplanting the mature technology. Thus, a successful effort to develop a silicon-based non-equilibrium quantum device technology would substantially improve the outlook for a "post-shrink" generation of quantum integrated circuits.

A2.

Nanoscale Structures for Microelectronics and Integrated Optoelectronics: Nanoscale without Gigadollars

T. J. Drabik, R. J. Higgins, and K. P. Martin

School of Electrical Engineering and Microelectronics Research Center
Georgia Institute of Technology
Atlanta, Georgia

Abstract

Nanometer-scale control of critical dimensions has resulted in real opto/electronic and photonic devices with novel properties based on quantum and classical mechanisms. This has extended the interests of university-based microelectronics research centers (MRCs) into the nanometer regime. This talk will briefly describe some of the areas being studied at the Georgia Tech MRC that involve nanometer scale structures. These include: [1] electron wave optical devices described by analogies with dielectric thin film filters, [2] coulomb blockade effect devices that exhibit spatially and temporally correlated single electron charging, [3] ballistic electron emission studies in semiconductor superlattices, [4] holographic diffraction elements for optical interconnects in massively parallel systems, [5] large area, nanometer period surface gratings for integrated optics, [6] epitaxial liftoff for incorporating nanoscale devices into conventional, more coarsely defined optoelectronic circuitry, and [7] damage free etching of semiconductor devices. This word will be discussed in terms of the modest additions to the facilities of a MRC not otherwise concerned with nanometer-scale opto/electronics and photonics.

B1.

Light-Emitting Properties of Porous Silicon

Joe C. Campbell and Dim-Lee Kwong

Microelectronics Research Center
University of Texas
Austin, Texas 78712

Abstract

Recent observations of efficient, room-temperature visible emission from porous Si have stimulated extensive research activity because the realization of practical, low-cost Si-based emitters would impact several key technologies including optoelectronic integrated circuits, optical memories and logic, and advanced display systems. Indentification of the physical mechanisms involved in the luminescence is, at present, a primary thrust. The luminescence phenomenon has been attributed to (1) quantum-size effects or (2) the formation of wide-bandgap material such as a-SiH or siloxene. We have characterized luminescent porous Si using photoluminescence (PL), transmission Fourier-transform spectroscopy, X-ray photoelectron spectroscopy, atomic force microscopy, and transmission electron microscopy. We have observed thermal and photoassisted degradation of the PL intensity. In both cases the decrease in PL coincides with the desorption of hydrogen from the SiH surface species. We have also observed that the PL can be repetitively switched between "green" and "red" by changing the composition of the electrolyte in which the anodized wafer is immersed. This change in the surface chemistry does not appear to alter the characteristic feature size of the porous Si and would appear to be at odds to the quantum-confinement explanation for the luminescence. Recently, however, we have found that when the porous Si is annealed in air to temperatures in the range 800½C to 1100½C, the luminescence returns, sometimes to its original strength. This effect has not been fully explained byt a likely mechanism involves nanoscale Si clusters imbedded in glassy (SiO) shells. FTIR measurements show that hydrogen is not involved in the luminescence of these wafers

and it is probable that quantum confinement is involved. These annealed wafers also exhibit a strong photoresponse. We have fabricated Al Schottky-photodiodes which exhibit an absorption response similar to that of single-crystalline Si. To achieve electroluminescence it may be necessary to inject high-energy carriers into the porous layers. A viable method to accomplish this is to utilize a wide-bandgap heterojunction injector such as GaP. Toward that end we have formed porous Si buried underneath GaP islands without degrading the photoluminescence.

B2.

Fabrication of Si Nanostructures for Light Emission Study

H.I. Liu, N.I. Maluf, R.F.W. Pease
Stanford Solid State Lab, Stanford, CA

D.K. Biegelsen, N.M. Johnson, F.A. Ponce
Xerox PARC, Palo Alto, CA

Abstract

The recent observation of room temperature visible photoluminescence [Canham, *Appl. Phys. Lett.* **57**, 1046 (1990)] and electroluminescence [Koshida and Koyama, *Appl. Phys. Lett.* **60**, 347 (1992)] from electrochemically etched porous silicon has rekindled interest in the potential of using silicon as an optical material. In addition, it raises many fundamental questions regarding the possibility of the luminescence originating from the sub-5 nm silicon crystallites in porous silicon. However, because of the problems associated with the size distribution and control of structures in porous silicon, many aspects of this material are not understood, and a consistent model has yet to be found. Therefore, to explore the potential of electron confinement induced radiative transitions in silicon, it is essential to study the intrinsic properties of well characterizable silicon nanostructures.

To this end, we have fabricated silicon columnar structures with diameters less than 5 nm using a combination of high resolution electron beam lithography, reactive ion etching, and thermal oxidation. A transmission electron microscopy (TEM) technique was developed to track the evolution of individual quantum wires. Among the various interesting oxidation phenomena are the non-monotonic oxidation rate with respect to the column size and an unexpectedly slow change of the outer diameters of the oxidized columns. Because of the close relationship between the structural configuration and the electronic band structure of silicon, unveiling the mechanisms responsible for these unusual oxidation phenomena is important in understanding the optical and electrical properties of silicon nanostructures. Moreover, this could also contribute to the effort in

analyzing the oxidation of small trench and isolated silicon structures used in current and future VLSI technology.

In this presentation, details regarding the fabrication of the silicon nanostructures and the TEM technique used to monitor their oxidation progress will be described. Moreover, the likely oxidation mechanisms and the photoluminescence results will be discussed. The current effort to obtain electrical contacts to the nano-pillars will also be presented.

B3.

Effect of Doping on Photoluminescence in Porous Silicon Nanostructures

A. J. Steckl, J. Xu and H. C. Mogul
Nanoelectronics Laboratory
University of Cincinnati
Cincinnati, Ohio
45221-0030

Recent developments [1, 2] have indicated that so-called porous Si with nanometer-scale structure produces a surprising photoluminescence (PL) under ultra-violet (UV) excitation. The PL, observable at 300°K with the naked eye at orange-red wavelengths (~600-750nm), corresponds to energies considerably greater (~1.6-2.0eV) than the bandgap of crystalline Si (1.1eV). Two basic mechanisms for this effect have been proposed : charge carrier quantum confinement in the porous Si skeleton or molecular bonding of Si, H and O atoms in the porous Si layer.

In order to identify the primary mechanism responsible for photoemission we need to compare nanostructures of well-defined dimensions in isolated regions which are fabricated in conventional Si and porous Si. We have previously reported [3] on the fabrication of isolated nanostructures in conventional Si using ultra-shallow focused ion beam (FIB) implantation followed by selective and crystallographically anisotropic chemical etching. We are investigating the effect of Si doping on the photoemission properties of porous Si. The porous Si is obtained by purely chemical ("stain") etching. We have observed that an initiation time delay (t_i) occurs between the insertion of the Si into the etching solution and the onset of porous Si production. The accompanying photoemissive spectrum exhibits a large signal in a broad band centered at 715nm, corresponding to an energy of 1.73eV. For p-type Si, t_i was found to decrease significantly with increasing doping level of the substrate. This effect is consistent with the basic Si etching mechanism which is controlled by the concentration of holes at the etching surface. We have used this doping dependence effect to obtain *selective area photoemission* in porous Si. Localized 37keV B^+ broad beam ion implantation and 5-15keV Ga^+ focused ion beam implantation into n-type Si followed by rapid thermal annealing resulted in selective porous Si formation in the implanted regions during stain etching. Upon UV excitation, photoemission from the implanted regions only was clearly observable. It is interesting to point out that at the low implantation energies used, the 37keV B^+ and, especially, the 5keV Ga^+ ions have very shallow penetration depths of 130 and 8 nm, respectively. It can be, therefore, concluded that nanometer-thin doped layers are sufficient for providing area selectivity in porous Si formation and localized photoemission.

[1] L. T. Canham, Appl. Phys. Lett., 57, 1046 (1990).

[2] Papers contained in " Light Emission from Si ", Mat. Res. Soc. Symp. Proc. 256, S. S. Iyer, R. T. Collins and L. T. Canham, eds. (Dec. 1991).

[3] A.J. Steckl, H.C. Mogul and S. Mogren, Appl. Phys. Lett., 60, 1833 (April 1992).

C1.

NNF Lithography Technologies for Nanoscale Optoelectronics

J.M. Ballantyne

School of Electrical Engineering
Cornell University

Abstract

Progress in nanolithography processing technologies at the National Nanofabrication Facility (NNF) at Cornell now makes possible the reproducible fabrication of optical structures in rather arbitrary geometries with feature size of order 100 nm along with accuracy and roughness of order 10 nm. The range of techniques includes reactive ion and chemically assisted ion beam etching, various masking materials and etch gases, together with binary lenses, curved and linear phase gratings, and curved and straight waveguides in combination with etched mirrors. Examples of those structures and their processes are described, with particular emphasis on some process combinations and recent innovations most useful for fabricating in III/V compounds combinations of ridge waveguides and etched mirrors. The properties of wavelength diode ring lasers utilizing these structures are briefly described, including the potential for geometry-dependent non-reciprocal optical structures.

C2.

X-Ray Nanolithography for Optoelectronic Integrated Circuits

Henry I. Smith

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA 02139

Abstract

Future optoelectronic integrated circuits (OEIC) will require minimum features of 100nm and below, often arranged in periodic arrays, with positional tolerances much finer than optical wavelengths. Moreover, substrates will have significant topography. In the past, gratings for DFB lasers and filters were fabricated using holographic lithography or e-beam lithography. The former is too inflexible for OEIC manufacturing. E-beam, on the other hand, is too slow for manufacturing, has difficulty dealing with substrate topography, suffers from problems due to electron backscattering, and requires special provisions to ensure pattern placement accuracy. That is, the scan field of an e-beam system is normally distorted, and placement accuracy is inadequate. For several years we have been developing a lithographic technique that is compatible with manufacturing at feature sizes below 100 nm, and that circumvents the problems of direct write e-beam lithography. The technique is called x-ray nanolithography. It is capapble of 30 nm resolution over 30mm-diameter fields, essentially free of distortion, and can pattern over topography without backscattering or proximity effects. We will report on our efforts to make x-ray masks that contain patterns with spatial-phase fidelity for DFB lasers and channel-dropping filters; our progress on sub-10 nm mask alignment; and assert that this technology is compatible with requirements for OEIC manufacturing.

C3.

Field Ion Emission of Silicon Adatoms from Different Sites of Si(111) 7x7 by STM

H. Uchida*, D. H. Huang*, F. Grey*, and M. Aono*,**

*Aono Atomcraft Project, ERATO, JRDC, Japan
**RIKEN Institute, Wako, Saitama 351, Japan

Abstract

Using a scanning tunneling microscope (STM), single adatoms can be extracted from a Si(111) 7x7 surface by field ion emission, when the sample voltage is pulsed at 6V in either polarity. Statistically, adatoms at the center of the 7x7 unit cell are found to be more easily removed than those near the corner holes, by a ratio of about 3:2. This difference can be explained by an about 0.01 eV lower activation energy for field ion emission at the center adatom site. The relationship of this result to previous observations of enhanced chemical reactivity at center adatom sites is discussed.

D1.

Integration of STM-Based Nanofabrication/Characterization and Electronics Device Processing

John A. Dagata and Wen F. Tseng

National Institute of Standards and Technology
Gaithersburg, MD 20899

Abstract

The emerging field of nanoelectronics will soon demand innovative methods for the fabrication and characterization of nanometer-scale structures. For such structures to exhibit quantum-confined behavior in a manner which will be sufficiently reliable and reproducible to carry out a serious investigation of room temperature quantum device physics, it is already clear that the electrical, chemical, and structural properties of the surface and interface of these nanostructures must be measured and controlled with unprecedented precision in both lateral and vertical dimensions. In our talk, we will describe collaborative efforts at NIST to develop an integrated approach to nanometer-scale fabrication and characterization of III-V semiconductor structures using STM/MBE/RIE. In addition to reviewing our results for nanometer-scale STM pattern generation and pattern development of ultrathin oxide masks on silicon and GaAs, novel methods of GaAs surface passivation and etch-damage repair, and STM-based I-V spectroscopy of III-V alloys under ambient conditions, we will discuss the implementation of these elements in the fabrication of quantum dots and other simple device structures and the outstanding problems which remain to be solved.

D2.

Fabrication and Characterization of Metal-Semiconductor Nanostructures

Dror Sarid and Sam Howells

Optical Sciences Center
University of Arizona, Tuscon AZ 85721

Abstract

Nanoscale metal structures fabricated on semiconductor surfaces by a scanning tunneling microscope (STM) are of interest because they exhibit a multitude of phenomena that offer technological opportunities [1-4]. The unique feature of these clusters derive from their size which makes their behavior fall in between that of a single metal atom and that of a metal film. We present experimental results were the degree of metallicity of nanoscale metal clusters fabricated on semiconductor surfaces was probed using STM and laser excitation.

1. D. Sarid, T.D. Henson, N.R. Armstrong and L.S. Bell, Appl. Phys. Lett. **52**, 2252 (1988).

2. T.D. Henson, D. Sarid and L.S. Bell, *J. Microscopy* **152**, 467 (1988).

3. P.N. First, J.A. Strocio, R.A. Dragoset, D.T. Pierce and R.J. Celotta, Phys. Rev. Lett. **63**, 1416 (1989).

4. H.J. Mamin, P.H. Guethener and D. Rugar, Phys. Rev. Lett. **65**, 2418 (1990).

D3.

Atomic Layer Epitaxy for Nanostructures

S. M. Bedair

Electrical and Computer Engineering Department
North Carolina State University
Raleigh, North Carolina

Abstract

Atomic layer epitaxy offers the ultimate control of the growth process for semiconductor films and structures. The deposition process is self-limiting, that is only one monolayer is deposited per growth cycle independent of the flux of the reactant gases. ALE is thus able to offer exact control of layer thickness and uniformity and provide very abrupt interfaces. Such features are critical in the fabrication process of nanostructures such as quantum wells and quantum wires.

ALE is characterized by the conformal growth, and side wall epitaxy on nonvicinal planes and etched groves and structures. Another potential of ALE is its ability to achieve highly ordered ternary alloys with bandgap much smaller than their random counterpart. Combining the conformal ALE growth with the synthesis of ordered ternary alloys can allow both lateral and vertical carrier confinements. We will outline several unique features of the ALE process and their impact on the fabrication of nanostructures.

D4.

In-Situ Growth Controlled Approaches to Semiconductor Nanostructures: An Assessment

Anupam Madhukar

Photonic Materials & Devices Laboratory
Department of Materials Science & Engineering
University of Southern California

Abstract

Broadly categorized, two generic approaches to the realization of 2- and 3-dimensional arrays of 2- and 3-dimensionally confined nanostructures are (1) post-growth patterning and etching of appropriate, as-grown, 1-dimensionally confined structures or (2) *in-situ* creation via growth control on vicinal or pre-patterned (planar or non-planar) substrates with pattern sizes larger than the nanostructure length scales. A primary anticipated advantage of the latter approach is that, in principle, it circumvents issues relating to the pattern transfer/etching induced damage and contamination faced in the former. However, equally serious issues relating to control, uniformity, reproducibility of the growth conditions, and identification of the needed growth kinetics are faced by *in-situ* growth controlled approaches. In this presentation we will elucidate some of these serious issues and approaches to reproducibly achieving the desired growth kinetics. A particular emphasis will be on distinguishing between *intrinsic limits* versus *extrinsic limits* (such as, e.g. imposed by the design of the present day molecular beam epitaxical growth chambers). Specifically, examples from the work at USC on growth on patterned (100), (111), and (h11) (h=1) surfaces will be used to illustrate both the commonality of fundamental principles of growth kinetics as well as differing consequences between orientations and/or growth conditions. In particular the significance of surface crystallographic symmetry in permitting 2-D confinement (i.e. quantum wires) versus 3-D confinement (i.e. quantum boxes) will be illustrated through the example of the USC work which, for the first time, has led to realization of 3-D confined structures via purely *in-situ* growth control on non-planar prepatterned (111)B

surfaces. Time permitting, issues of throughput and scalability will also be commented upon.

D5.

Mesoscopic Band Gap Engineering and Quantum Well Structures By Molecular Beam Epitaxy - Focused Ion Beam In Situ Processing

P. M. Petroff

Materials Department
University of California, Santa Barbara
Santa Barbara, CA 93106

Abstract

We introduce several methods based on the use of ion implantation using a foucsed ion beam (FIB) for producing either band bending or band gap modulation on a mesoscopic scale in III-V compound semiconductors. We apply these techniques to the *in situ* fabrication of ultra small channel quantum devices. The fundamental radiation damage processes involve in *in situ* MBE-FIB processing will be reviewed. We show that by ion induced enhanced interdiffusion and ion defined buried stressors, a blue shift or a red shift of the band gap (up to 100 mev) can respectively be obtained in GaAs-AlGaAs quantum well structures. Modulation doping of heterostructures using Si+ ions is also demonstrated. The characteristics of an inverted MODFET and of a novel resonant tunneling device fabricated by this *in situ* processing will be presented.

D.6.

Silicon Germanium Superlattices and Meso Structures

Kang L. Wang
Department of Electrical Engineering
University of California, Los Angeles
Los Angeles, CA 90024-1594

Recent progress in the growth of pseudomorphic strained and controlled relaxed SiGe films makes it possible the realization of many advanced heterojunction devices. Among them, there are heterojunction bipolars, modulation doped transistors, and more recently multiple quantum wells and superlattices. In this talk, we will review the state of the art in the growth of the compositional and doping multiple quantum wells and superlattices. The optical properties of the quantum wells and superlattices and their potential optoelectronics application will be discussed. Using strain engineering, the Stark effect for both inter-band and the intersubband transitions can be made to be much larger than that of type-I AlGaAs/GaAs structures. SiGe quantum wells offer are many advantages. Among them are the convenience of energy tuning and process control as well as potential affordable cost. Owing to the unique features of the band structure, more significantly, several normal incidence detection mechanisms will be illustrated for intersubband transition: namely, from nonvanishing off- diagonal elements of the effective mass tensor in n-type, free carrier absorption, and intervalence band transition for p-type. These mechanisms alleviate the major drawback of the selection rule of the Γ valley intersubband transition, which forbids the detection of normal incident light, as in the case of AlGaAs/GaAs multiple quantum well structures. The experimental observation of normal incident intersubband transition in SiGe/Si quantum wells and δ-doped Si layers will be discussed. In the case of SiGe, the effect of the strain in determining the occupancy of the valleys will be described. The importance of many-body effects in determination of transition energy of very heavily doped structures and δ-doped layers, will also be shown for tuning a wide range of transition energy (from μm to tens of μm and perhaps longer). Infrared detector structures using SiGe/Si multiple quantum well structures will be illustrated using such structures. Finally, the use of meso structures as potential wire detectors and possible laser sources will be discussed.

E1.

Serpentine Superlattice Quantum-Wires – Growth and Optical Properties

J. L. Merz

University of California
Santa Barbara, CA 93106

Abstract

The growth of AlAs/GaAs tilted superlattices (TSL) on GaAs (100) vicinal substrates has provided a promising way to fabricate quantum wire arrays with a lateral width of just a few nm. However, there are two problems with this approach: (1) the thermodynamic and kinetic difficulty of having the Al incorporate only at the step edge, resulting in incomplete segregation, and (2) the fact that the tilt angle is not a well-controlled parameter, which changes the electronic confinement energy. Recently we have presented a way to avoid this problem by purposely changing the tilt angle to achieve a crescent-shaped well. the resulting "serpentine superlattice" (SSL) accommodates the geometric sensitivity to absolute growth rates. In this paper we present a detailed luminescence study of a SSL, and report the first observation of linear polarization effects both in PL and PLE. The polarization dependence of the emission has been measured with a photo-elastic modulation technique, showing a pronounced anisotropy in both PL and PLE due to the alteral confinement. It is found that about 30% of the Al intended for the barrier ends up in the well. The polarization of the PL is found to be nearly constant over large areas of the wafer indicating uniform quantum wire states.

E2.

Ferroelectronic Thin Films Based Devices and Structures in Optoelectronic Computing System

V. H. Ozguz

University of California, San Diego
Electrical and Computer Engineering Department
La Jolla, CA 92093-0407

Abstract

The role of ferroelectric thin film in the realization of components for optoelectronic computer systems is considered. System, device and material interactions are discussed. Optoelectronic components considered are smart spatial light modulators and holographic storage modules. Material and device development efforts based on PLZT, KTN and SBN films for these modules are presented. Future developments and applications are outlined.

E3.

Atomic Asperity Tunnel Junction Devices

Steve Gregory

Physics Department, University of Oregon
Eugene, OR 97403-1274

Abstract

As is well-known in connection with scanning tunneling microscopy, tunneling currents can be confined to regions of atomic scale in junctions formed between "asperities" on the tunneling electrodes. These asperities define the distance of closest approach of the the electrodes and, at present, occur naturally. Although lithographic techniques are incapable of defining junctions on the truly atomic scale there are, nonetheless, reasons for attempting to microfabricate them. Molecular self assembly might hold some promise in this regard.

Confinement of the tunnel current leads to the possibility of greatly increasing the interaction of tunneling electrons with scatterers within the junction. A single scattering entity can, in fact, control the junction conductance. I shall discuss instances in which the conductance shows clear evidence of the presence of a single scatterer. The "crossed-wire" geometry used in the experiments can be adapted for photonic control of electron tunneling using optical fibers coated with optically thin metallic films and depositing a suitable film to act as the tunnel-barrier material.

A Resonant Tunneling Metal Base Hot Electon Transistor

Mark V. Weckwerth

Stanford University
Stanford, CA 94305

Abstract

Recent work has demonstrated single crystal epitaxial growth of aluminum on aluminum arsenide as well as crystalline growth of aluminum arsenide on top of aluminum. A well behaved metal/semiconductor system opens the door towards a functional metal base hot electron transistor. A novel transistor composed of a gallium arsenide/aluminum arsenide resonant tunneling emitter, an aluminum base and collector, and a gallium arsenide collector barrier is proposed as a realizable hot electron transistor.

The high speed of this device is assured by the small dimensions of the transport region (100-200 angstrom base and 300-400 angstrom collector barrier), the absence of minority carrier injection, and the low resistance of the aluminum base. A high electron transport factor from emitter to collector (and thus high gain) can be achieved by exploiting a combination of the narrow energy distribution of the electrons injected by the resonant tunneling emitter and the low reflection of these hot electrons at the base/collector barrier interface due to resonances over the collector barrier. Room temperature, of near room temperature operation of such a device should be achievable because of the large thermionic Al/GaAs/Al collector barrier.

Although easily fabricated once grown, problems experienced during growth will be addressed; specifically those issues addressing incompatible growth conditions for aluminum and GaAs. The use of migration enhanced epitaxy for low temperature growth of gallium arsenide has been employed to avoid the problems

of aluminum faceting and diffusion. The device as proposed takes advantage of Al/GaAs/AlAs system, yet attempts to avoid problems associated with the lower quality GaAs on Al.

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