(2)

MCNC

FIELD EMITTER ARRAY RF AMPLIFIER DEVELOPMENT PROJECT

ARPA CONTRACT #MDA 972-91-C-0028

PHASE ONE, OPTION 1

QUARTERLY R&D STATUS/TECHNICAL REPORT #9

10/16/93 - 01/15/94

SPONSORED BY:
DR. BERTRAM HUI
ARPA / DSO

MCNC ELECTRONIC TECHNOLOGIES DIVISION
POST OFFICE BOX 12889
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GARY McGUIRE, PRINCIPAL INVESTIGATOR

February 1, 1994

Dr. Bertram Hui
ARPA/DSO
3701 North Fairfax Drive
Arlington, VA 22203-1714
(703) 696-2239
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Dear Dr. Hui:

Enclosed are two copies of the ninth quarterly R&D status/technical report for the Field Emitter Array RF Amplifier Development Program funded by ARPA, covering the contract period from October 16, 1993 to January 15, 1994. We have also forwarded copies to the ARPA/OASB/LIBRARY and Defense Technical Information Center as specified in the contract requirements. This report covers work done during the third quarter of Option 1 contract funding. Please do not hesitate to call me at (919) 248-1837 if I can provide additional information.

Thank You,

Dev Palmer

Dev Palmer

cc: Robert Parker
Elaine Ely
William Joines
Robert Symons

QUARTERLY R&D STATUS/TECHNICAL REPORT #9
10/16/93 - 01/15/94

Title of Work: Field Emitter Array RF Amplifier Development Project
ARPA Contract #MDA 972-91-C-0028
Phase One, Option 1

Sponsor: Dr. Bertram Hui
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Arlington, VA 22203
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Effective Date of Contract: 4/16/93

Contract Expiration Date: 4/15/94

Contract Amount: $454,965.00

MCNC Field Emitter Array RF Amplifier Development Project

Phase One, Option 1: Cathode Technology Development

ARPA Contract MDA 972-91-C-0028

Ninth Quarter – January 1994

Key Ideas

Develop field emitter arrays with a cutoff frequency above 1 GHz, total current greater than 5 mA, and 5 A/cm^2 current density with the gate electrode potential less than 250V. Demonstrate these characteristics for greater than 1 hour lifetime.

Reduce capacitance and increase transconductance of field emitter arrays to improve frequency response. Focus on development of tall emitter columns to minimize capacitance. Evaluate low work function materials and metals as emitter surface coatings, reduce gate dimensions, and improve tip sharpening to increase transconductance. Fabricate large arrays with dense tip spacing to increase total current.

Examine various test methods to permit characterization of more devices per test cycle.

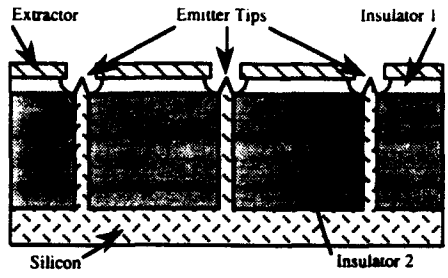
Major Accomplishments:

First fabrication run of 4 μm column devices with the new mask is complete. The remaining contract runs are proceeding on schedule, with consideration for equipment delays. Lot origination for the final two runs is complete and one is in processing.

Data indicating modulation of anode current at a frequency of 1 GHz by a 4 μm column device was recorded on two occasions. Modulation was measured at lower frequencies (between 1 and 50 MHz) to validate estimates of f_T and measured gain at higher frequency. An array of 232,230 tips operated for 18 hours with anode current of between 1 and 2 mA at a gate potential of < 200 V.

Devices incorporating low work function and metal coating processes have been electrically tested.

MCNC Silicon Field Emitter with Column



Major Milestones – This and upcoming quarter:

Deliver sample devices for testing and SEM inspection data from device fabrication run of 4 μm column emitters. Characterize DC performance of devices from this run. Complete processing on device fabrication run of 6 μm column devices. Incorporate low work function and metal coatings into fabrication process flow.

Continue the DC characterization and reliability testing program for Option 1 devices. Prepare 6 μm column devices for testing when completed.

Prepare and deliver Phase One Final Report.

Field Emitter Array RF Amplifier Development Project
Phase 1, Option 1

I. Executive Summary

- Modulation of anode current at 1 GHz was observed on two different devices. The devices tested were 1,197-tip arrays of 4 μm column emitters. Net signal gain of 0.84 dB was recorded at a DC anode current of 172 μA. Fabrication of the 4 μm devices was completed in early January. As more devices are tested, it is expected that higher DC currents will be observed, resulting in increased RF gain.

- An identical array was tested at lower frequencies (1 – 50 MHz). Extrapolating from the gain measured in this frequency range shows reasonable agreement with the gain measured at higher frequency. The lower frequency data also reinforces the calculated value of f_T for devices produced at MCNC.

- A 232,630-tip array operated for 18 hours with anode current between 1 and 2 mA at a gate potential of < 150 V.

- The first fabrication run of 4 μm column devices is complete. Arrays of up to 232,630 tips have been successfully fabricated, electrically tested, and have produced significant anode current. The second fabrication run of 4 μm column devices is proceeding on schedule. The lot origination process for the 6 μm column devices is complete, and the devices are now in processing.

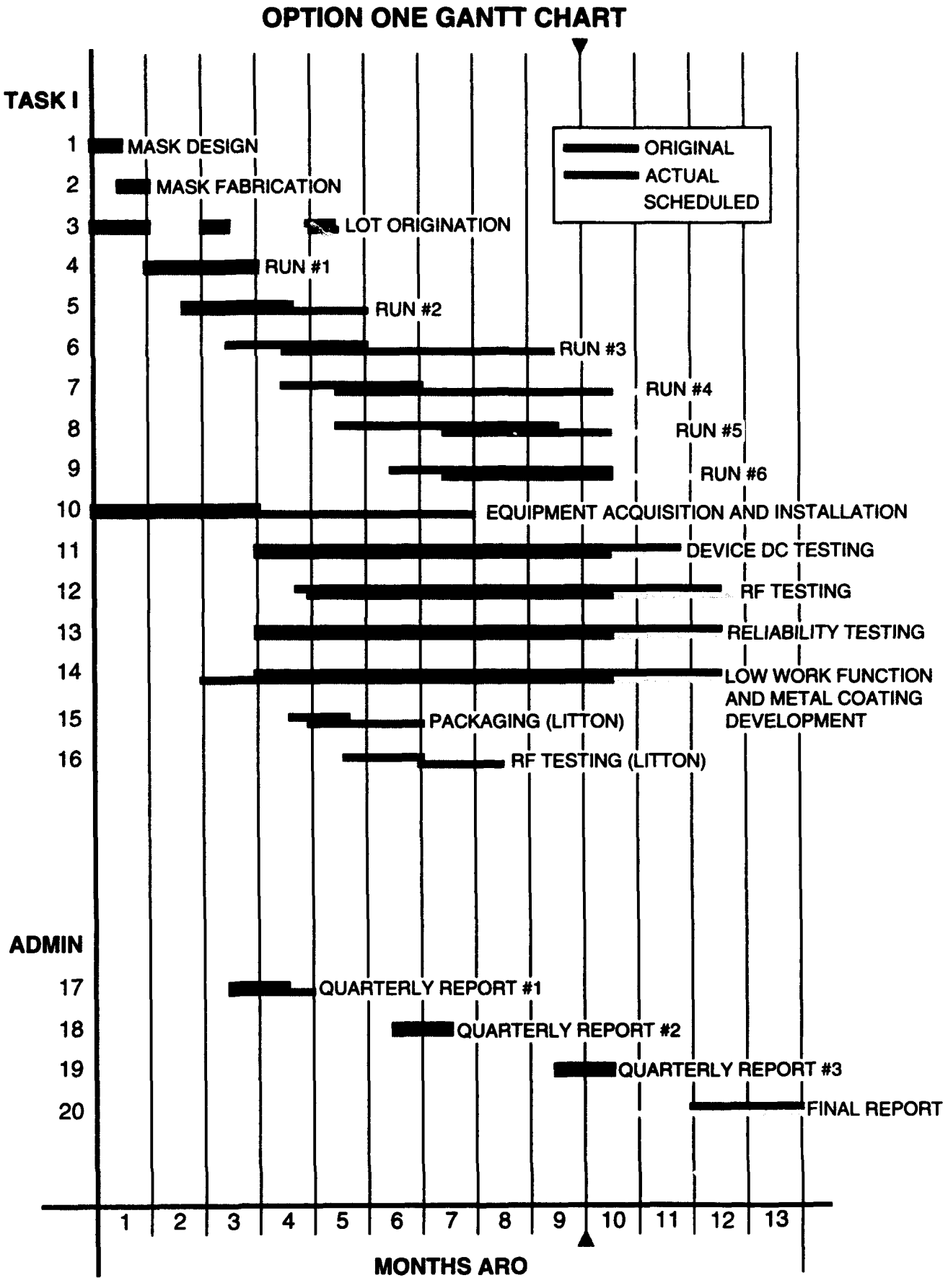
- Devices with low work function and metal coatings were electrically tested. Good electrical results were obtained from Pt coated tips, validating the technique of applying coatings as the last device processing step.

- TEM analysis of tip radii was performed. Tip radii in the range of 50 to 100 Å were typically observed.

II. Milestone Status:

Task	Completion Date	
Milestones	Original	**Complete** Expected
Complete design and fabrication of new reticle set. Complete lot origination process for two runs of 2 μm column emitter arrays. (MCNC)	5/93	**5/93**
Complete first run of field emitter arrays (2 μm column). Complete lot origination process for two runs of 4 μm column field emitter arrays. (MCNC)	7/93	**8/93**
Complete acquisition and installation of whole wafer DC test and RF measurement equipment. Begin in-house device DC characteristics and reliability testing program. (MCNC and Duke)	7/93	**12/93**
Begin low work function and metal coating development. (MCNC)	7/93	**6/93**
Complete second run of field emitter arrays (2 μm column). Deliver devices to Litton subprogram for packaging and RF testing. (MCNC)	9/93	**10/93**
Begin in-house device RF testing program. (MCNC)	8/93	**8/93**
Complete third run of field emitter arrays (4 μm column). Complete lot origination process for two runs of 4 or 6 μm column field emitter arrays. (MCNC)	10/93	**12/93**
Complete packaging, begin RF testing of field emitter amplifier modules. (Litton)	9/93	**10/93**
Complete fourth run of field emitter arrays (4 μm column). (MCNC)	10/93	2/94
Complete RF testing of field emitter amplifier modules. (Litton)	10/93	**12/93**
Complete fifth run of field emitter arrays (4 or 6 μm column). (MCNC)	1/94	2/94
Complete sixth run of field emitter arrays (4 or 6 μm column). (MCNC)	2/94	3/94
Complete all contract activities. Deliver devices, data, and other related material to ARPA. Complete and deliver final report according to contract stipulations. (MCNC)	4/94	4/94

Task	Completion Date	
Deliverables	Original	**Complete** Expected
Plots of new mask design set available for inspection by ARPA personnel if desired.	5/93	**5/93**
Sample devices from the first run of field emitter arrays (2 μm column) with SEM inspection data.	7/93	**8/93**
First quarterly R&D status/technical report.	8/93	**8/93**
Sample devices from the second run of field emitter arrays (2 μm column) with SEM inspection data. Performance data from first run.	8/93	**12/93**
Sample devices from the third run of field emitter arrays (4 μm column) with SEM inspection data. Performance data from second run.	9/93	2/94
Sample devices from the fourth run of field emitter arrays (4 μm column) with SEM inspection data. Performance data from third run.	10/93	2/94
RF amplifier module performance data from Litton subcontract.	10/93	**12/93**
Second quarterly R&D status/technical report.	11/93	**11/93**
Sample devices from the fifth run of field emitter arrays (4 or 6 μm column) with SEM inspection data. Performance data from fourth run.	1/94	2/94
Sample devices from the sixth run of field emitter arrays (4 or 6 μm column) with SEM inspection data. Performance data from fifth run.	2/94	3/94
Third quarterly R&D status/technical report.	2/94	**2/94**
Low work function and metal coating development results. Performance data from sixth run. Reliability test data for all devices. Final Technical Report – Option 1.	4/94	4/94


OPTION ONE GANTT CHART
TASK I
1 MASK DESIGN
2 MASK FABRICATION
3 LOT ORIGINATION
4 RUN #1
5 RUN #2
6 RUN #3
7 RUN #4
8 RUN #5
9 RUN #6
10 EQUIPMENT ACQUISITION AND INSTALLATION
11 DEVICE DC TESTING
12 RF TESTING
13 RELIABILITY TESTING
14 LOW WORK FUNCTION AND METAL COATING DEVELOPMENT
15 PACKAGING (LITTON)
16 RF TESTING (LITTON)
ADMIN
17 QUARTERLY REPORT #1
18 QUARTERLY REPORT #2
19 QUARTERLY REPORT #3
20 FINAL REPORT
ORIGINAL
ACTUAL
SCHEDULED
1 2 3 4 5 6 7 8 9 10 11 12 13
MONTHS ARO

III. Technical Progress:

1.0 Electrical testing and high-frequency performance measurements.

1.1 Continuous-wave modulation at 1 GHz of field emitter array anode current was observed on a 1,197-tip array of 4 μm column emitters. The device produced a net signal gain of 0.84 dB with DC anode current of 172 μA. Since then, this result has been duplicated and improved upon with several other devices. A detailed description of the test procedure and results was given in a Special Technical Report dated 17 JAN 94, included here as Appendix A. The more recent results occurred outside of the reporting period for this report, and will be detailed in another special technical report to ARPA. Oscilloscope screen hardcopy of the modulated signal is shown in Figure 1. Screen hardcopy of the background signal as calibrated is shown in Figure 2.

1.2 A 232,630-tip array, serial number DOP3-1425-06-H1, operated for 18 hours with anode current between 1 and 2 mA at a gate potential of < 150 V. Previous device runs had not produced electrical yield on arrays of this size. The improved performance is due in part to the thicker oxide required on the taller columns. Increased oxide thickness reduces the likelihood of a defect penetrating through and shorting the gate electrode to the substrate. A graph of the device performance over the test is shown in Figure 3. An I-V curve showing the average anode current versus gate voltage is shown in Figure 4.

2.0 Device processing.

2.1 As part of the ongoing improvement of the device processing, the oxide backfill process used to support the gate electrode was examined. Initially, the process was done in two stages, with extensive inspections of each wafer at every process step to determine processing targets for the next step. Each stage consists of the following process steps: a 2 μm evaporation of SiO_2, a photoresist planarization, and a photoresist etchback to prepare the wafer for the next stage of deposition. Now, the process steps have been standardized to eliminate the intervening inspection steps so that batch processing is possible. This enhances the manufacturability of tall column devices.

2.2 Adhesion of the backside metalization layer was improved by the addition of an extra wet clean step immediately prior to the metal evaporation.

2.3 With the taller column structure, a thicker nitride etch mask is required for column formation. Because of these thicker nitrides, stress on the silicon wafer is increased. The added stress tends to cause slip lines to form in the crystal structure of the silicon, which in turn cause cracking in the evaporated oxide after deposition. The slip lines are unavoidable in the current process with the current materials. The use of lower-stress films such as LPCVD oxide are under investigation as a possible solution.

Some stress relief is provided using the current process and materials by etching the nitride film from the backside of the wafer after the column formation and prior to the evaporated oxide backfill. The slip lines will still be present in the silicon crystal

structure, but the evaporated oxide film will be exposed to less overall stress and so cracking will be reduced.

3.0 Vacuum testing and microencapsulation bonding system.

3.1 After initial testing of the *in-situ* plasma cleaning system, the mass flow controller malfunctioned. Further development of the process will be delayed until repair is complete.

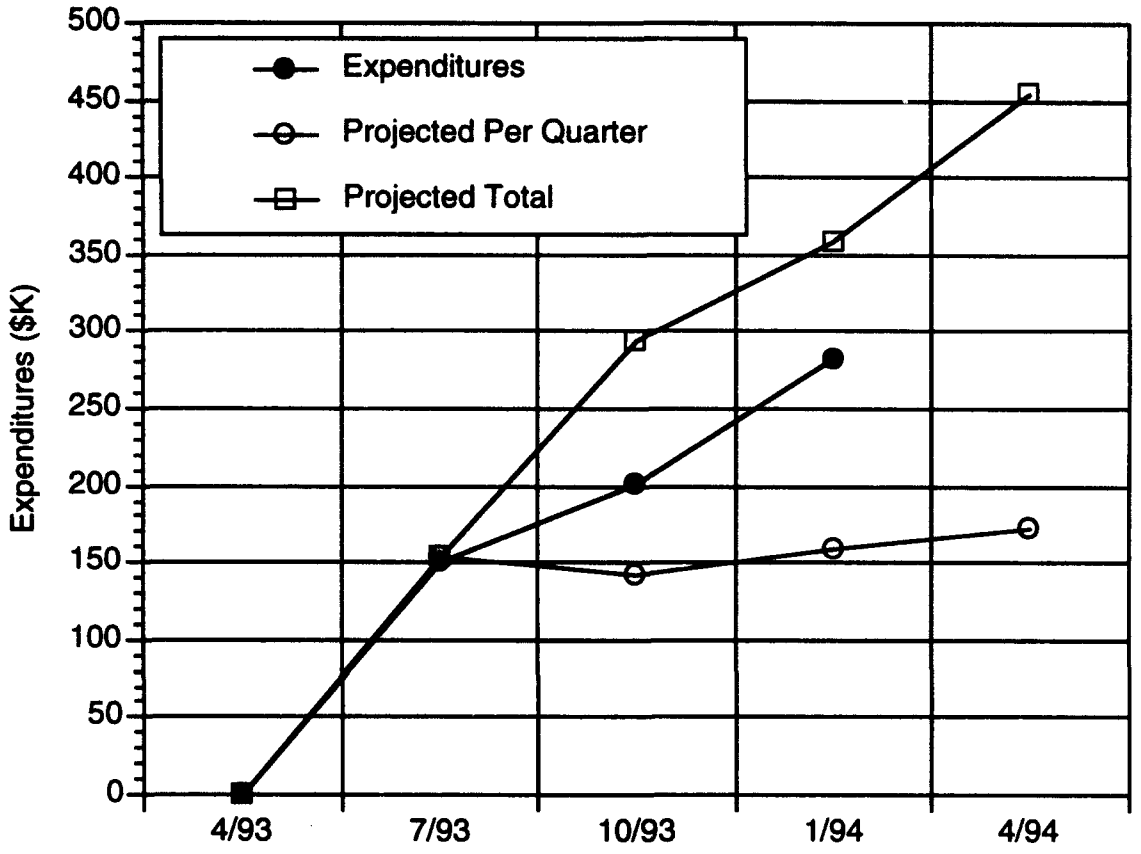
4.0 Other Developments.

4.1 Devices with low work-function and metal coatings applied as the last processing step were electrically tested. Four types of materials were evaluated: TaN, diamond-like films, LaB_6, and Pt. The TaN and diamond-like films short-circuited the gate electrodes to the substrates on all the devices that were evaluated. The devices coated with the LaB_6 film showed no measurable gate or anode current. This demonstrates that the LaB_6 film can be applied without shorting the gate electrode. The lack of emission current could have been due to the initial emitter structure rather than the coating.

Good electrical results were obtained from the Pt coated devices. The best results, from a 44,460 tip array of 2 μm columns, are shown in Figure 5. Peak anode current of over 2 mA was observed. This successful test demonstrates that the devices can be coated with platinum as the last processing step. Investigation continues on how these films can improve electrical performance, with respect to both turn-on voltage and emission stability.

4.2 TEM analysis of the tip radius of the finished structure was conducted. In general, the tip radius is below the measurement resolution of a scanning electron microscope. Not enough tips were measured on the TEM to generate a statistically significant distribution of tip radii. A TEM photograph of a representative tip is shown in Figure 6.

IV. Fiscal Status



Expenditures this quarter (10/16/93 - 01/15/94)	$81,697.79
Total expenditures to date (4/16/93 - 01/15/94)	282,273.12
Contract Amount (Option 1)	$454,965.00

Note: Quarterly expenditures are based on financial data and contract commitments through 12/31/93 and estimated processing costs through 01/15/94.

V. Problem Areas

Several problem areas are under examination. One great concern is the reduced DC performance of arrays in the RF test fixture as compared to performance of identical arrays in the DC test fixture. Modifications to the RF test fixture have improved the performance, and further modifications are expected to bring enhanced performance.

Stress-related cracking of the thick evaporated oxide required for the taller column structures has also been observed. Alternate materials and processing steps are being evaluated as a means to minimize the occurrence. The deposition process for low work function and metal coatings is being refined in an attempt to reduce the likelihood of gate electrode to substrate electrical shorts.

VI. Visits and Technical Presentations

Weekly closed meetings were held between MCNC staff and its subcontractors. An abstract entitled "Large Arrays of Gated Silicon Field Emitters as RF Active Device Cathodes", has been accepted for presentation at the 1994 Tri-Service/NASA Cathode Workshop in Cleveland, Ohio March 29–31.

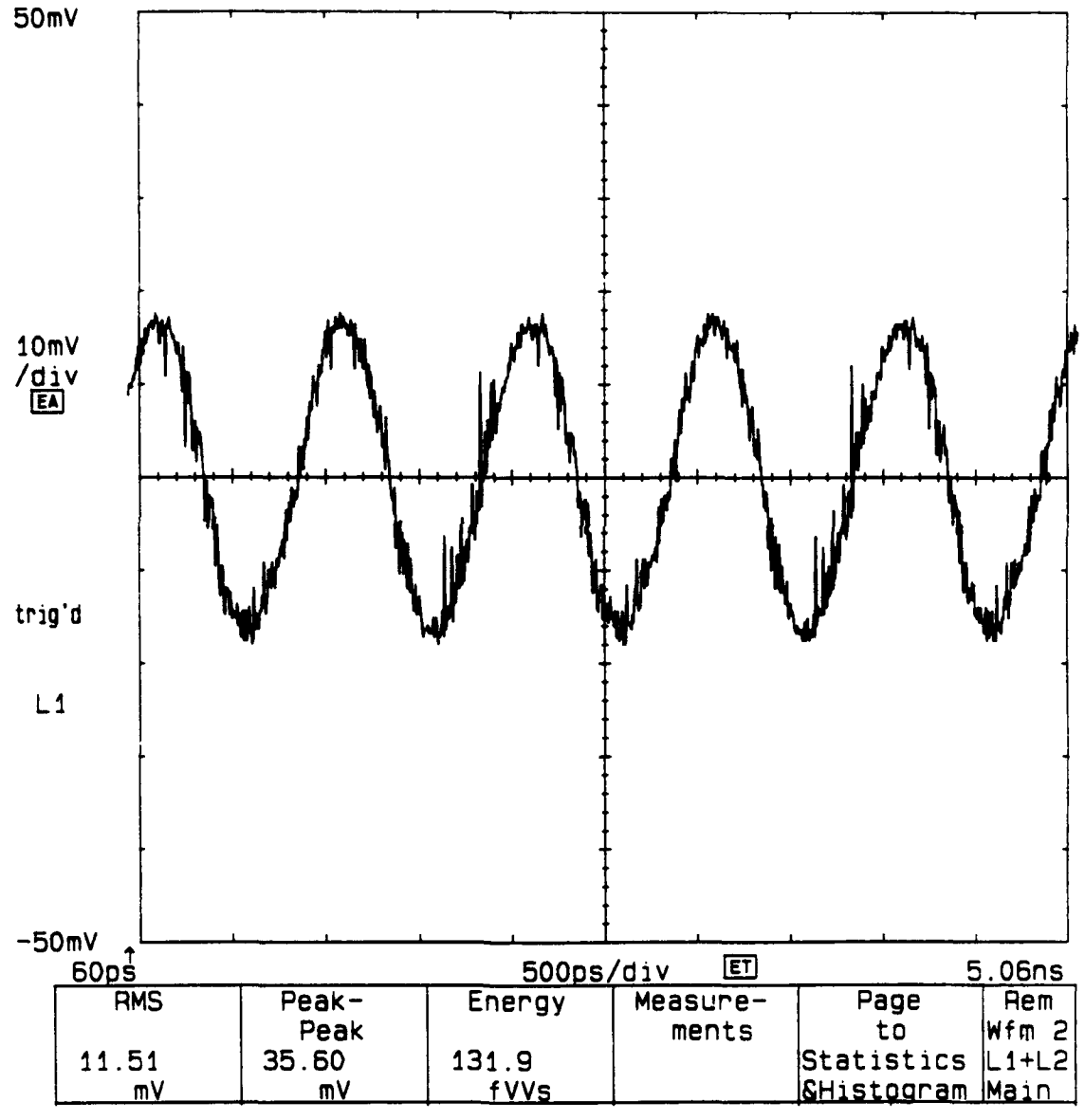


Figure 1: Printout of the DSA602A oscilloscope screen displaying the voltage signal due to modulated field emitter array current at 1 GHz.

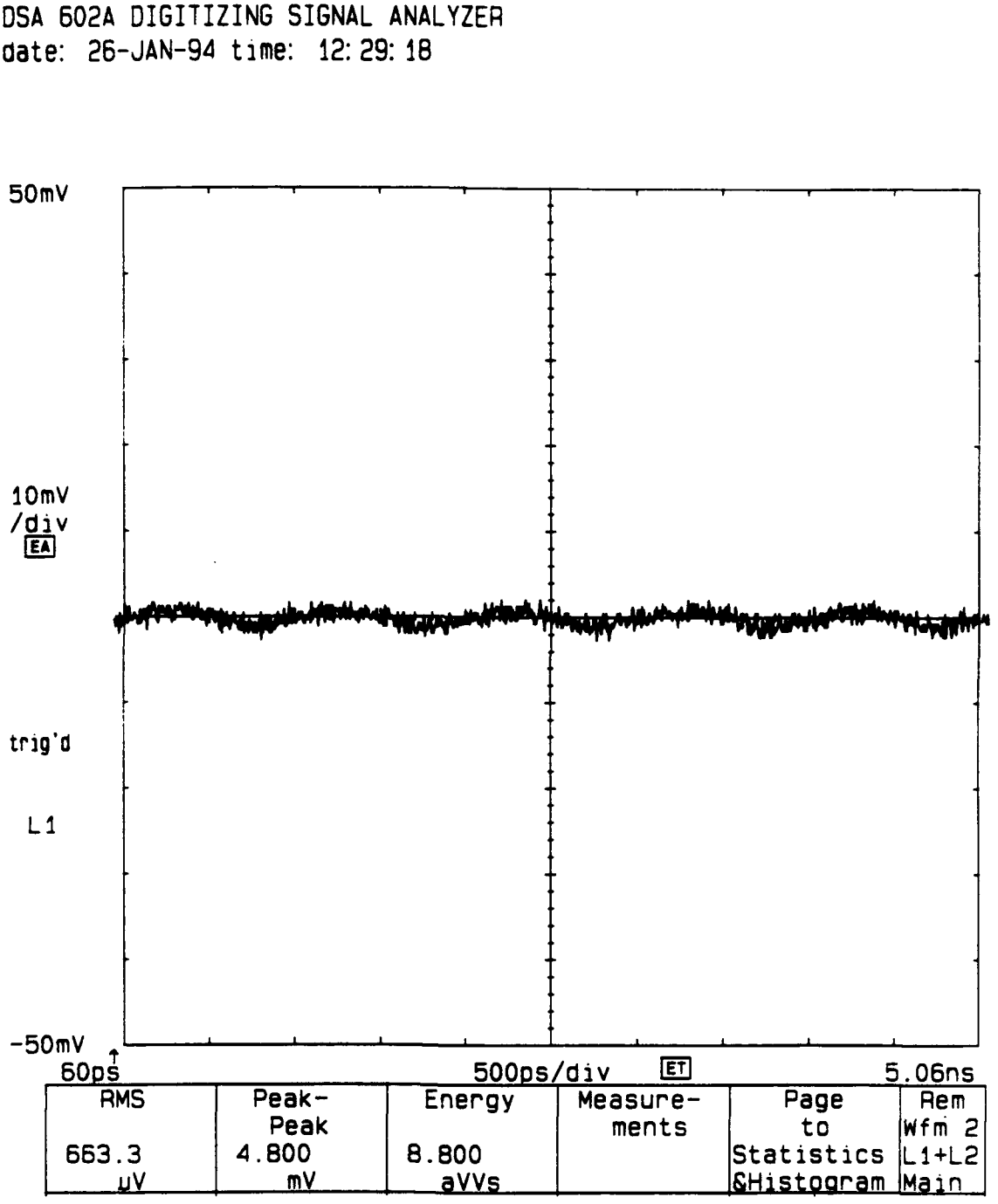


Figure 2: Printout of the DSA602A oscilloscope screen displaying the feedthrough signal after calibration due to the cathode-to-anode capacitance.

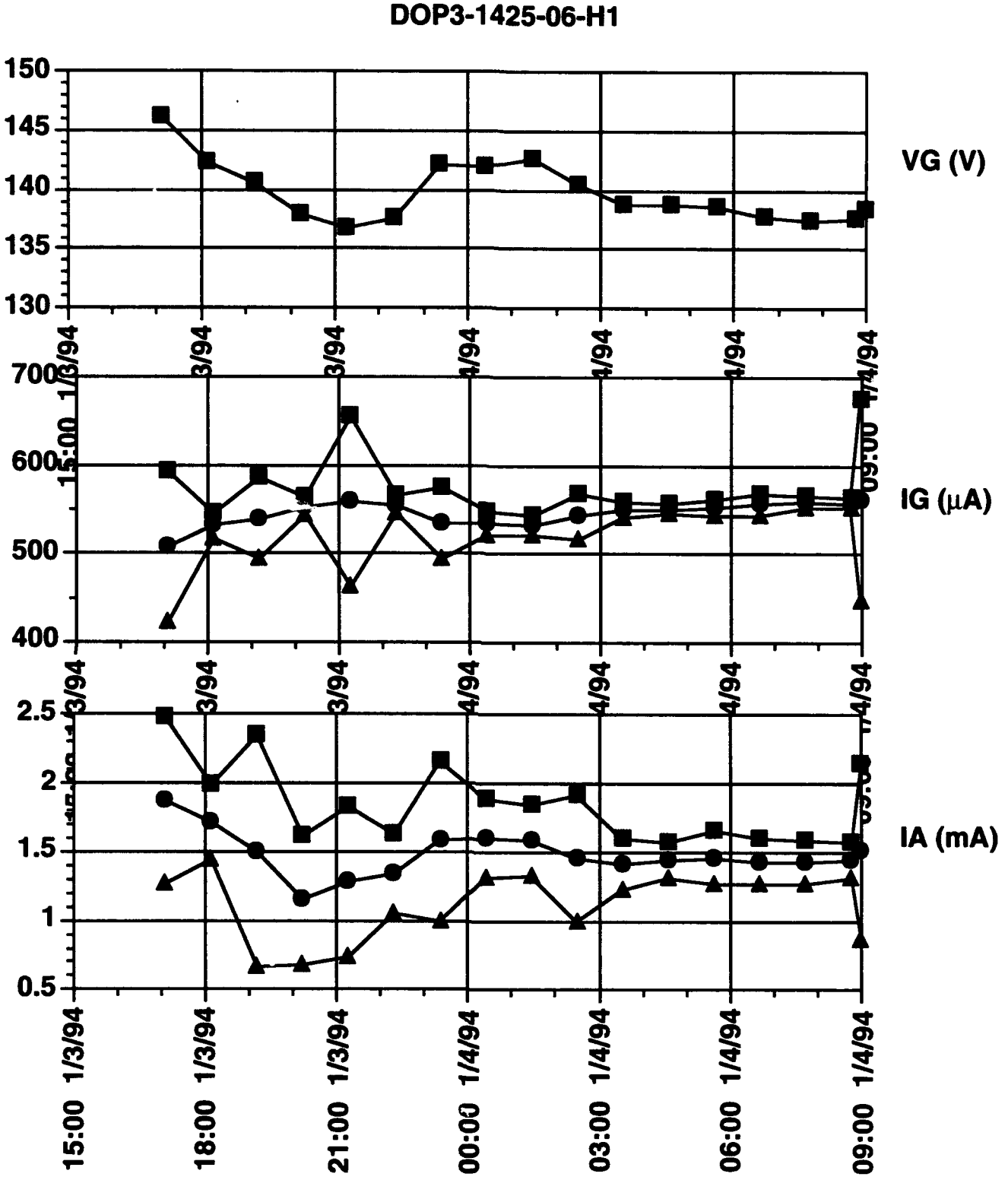


Figure 3: Lifetime test for 232,230-tip array of 4 μm column emitters with 6 μm tip-to-tip spacing. Upper chart shows corrected gate potential in volts. Center chart shows gate current in microamps, and the lower chart shows anode current in milliamps. These two charts show the mean and +/- 3 standard deviation values of the measured current.

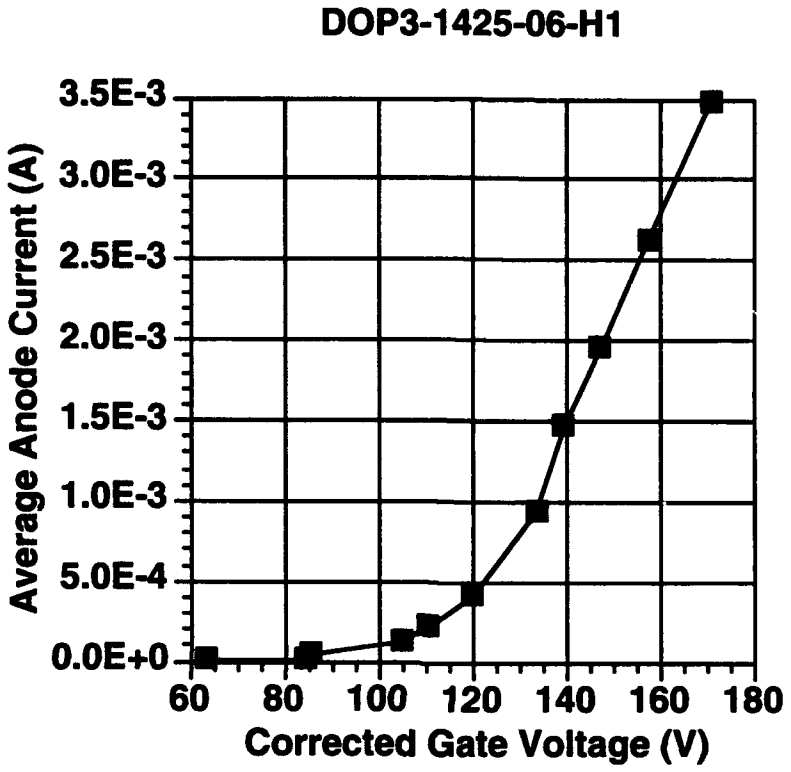


Figure 4: I-V curve for device in Figure 4 calculated from data collected during 18 hour operation. Average anode current versus corrected gate voltage is shown.

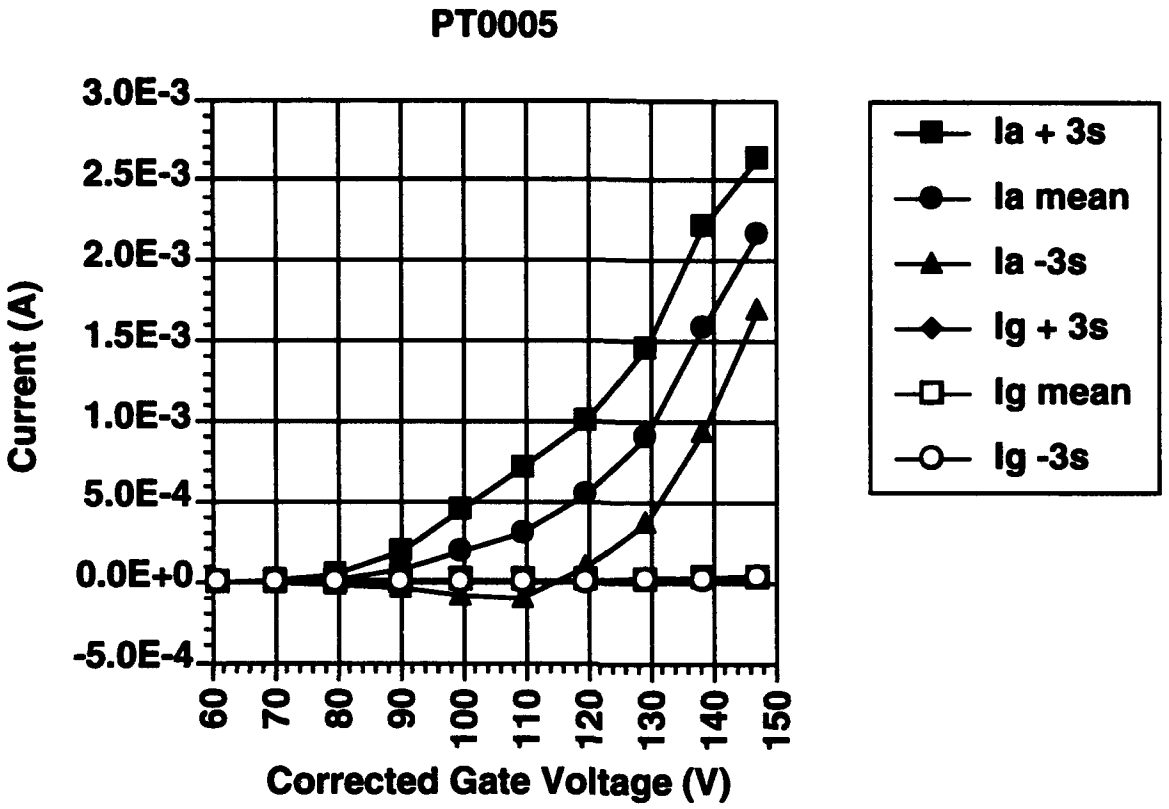


Figure 5: I-V curve generated from 44,460 emitter array with Pt coating. The chart shows the mean and +/- 3 standard deviation values of the measured current.

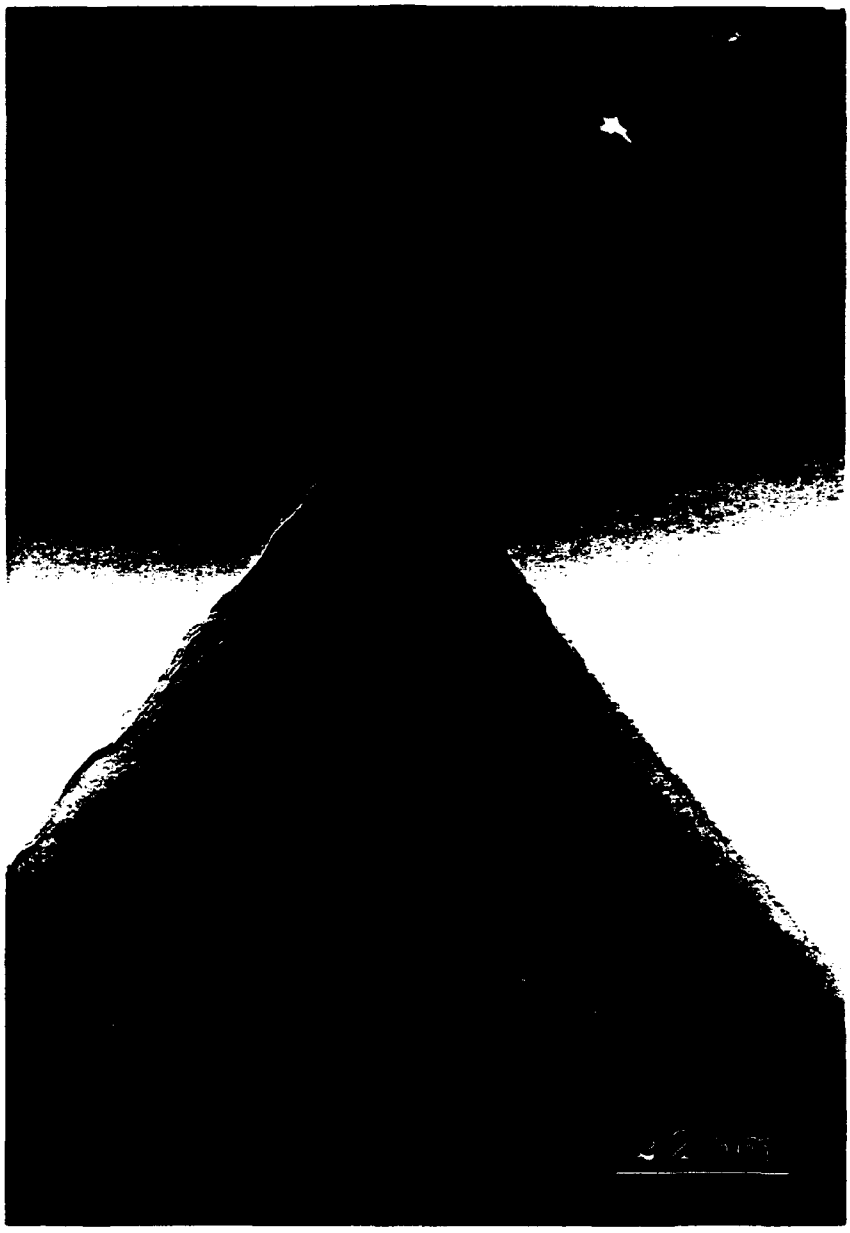


Figure 6: TEM photograph of typical field emitter tip.

LIST OF ATTACHMENTS

Attachment A: "Special Technical Report", 8 pages.
Attachment B: Duke Subprogram Report, 6 pages.

ATTACHMENT A

ATTACHMENT A

FIELD EMITTER ARRAY RF AMPLIFIER DEVELOPMENT PROJECT
ARPA CONTRACT #MDA 972-91-C-0028
PHASE ONE, OPTION 1

SPECIAL TECHNICAL REPORT
17 JAN 94

SPONSORED BY:
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ARPA/DSO

MCNC ELECTRONIC TECHNOLOGIES DIVISION
POST OFFICE BOX 12889
RESEARCH TRIANGLE PARK, NC 27709-2889

GARY MCGUIRE, PRINCIPAL INVESTIGATOR

INTRODUCTION

MCNC is pleased to report successful demonstration of continuous-wave modulation of field emitter array anode current at 1 GHz. A 1,197-tip array produced a net signal gain of 0.84 dB with DC anode current of 172 μA. Thus we feel that we have satisfied all of the performance milestones for Phase I of the program.

TEST METHOD

Figure 1 shows a schematic diagram of the test equipment used for high-frequency testing. An rf generator is connected to a directional coupler with power meters attached to monitor forward and reflected power. A second directional coupler is attached. The reflected power port of the second coupler is terminated in a 50 Ω load, while the forward power port is fed through a variable attenuator and phase shifter and connected to one input of the Tektronix DSA602A oscilloscope. The forward power signal with attenuation and phase shifting is used as a calibration signal.

The main output of the second coupler is connected to the gate bias tee on the device under test. The gate and anode bias circuits are identical to those used in DC testing as reported earlier. The output of the device is connected through another bias tee to the input of a buffer amplifier. The buffer amplifier output is connected to the other input of the oscilloscope. The buffer is inserted to protect the input of the oscilloscope from the high voltages used on the anode bias, as well as transients generated from the operation of the device under test. The effect of the buffer amplifier, as well as the other components of the test fixture, is removed from the data before the gain is calculated.

Before a measurement is made, the oscilloscope is configured to subtract the calibration signal from the device bleedthrough signal with the emitter off. The variable attenuator and phase shifter are adjusted so that the calibration signal cancels the bleedthrough signal on the oscilloscope display. Since the attenuator is variable in steps of only 1 dB, complete nulling of the bleedthrough signal is not possible. However, calibration of the system in this manner is insensitive to drift in the rf generator. When the field emitter is turned on, a modulated signal appears. This method gives a clearer indication of anode current modulation than the s-parameter measurement used by other programs.

RESULTS

A table comparing MCNC results and test conditions with those reported in the literature by programs at SRI and Raytheon is shown in Table 1. Results from the MIT-Lincoln Labs program are not included, because to our knowledge, they have not reported anode current modulation at 1 GHz. Data for this table was gathered from each program's Phase I summary, as well as data reported at the 1993 International Electron Devices Meeting. Maximum reported and projected performance for MCNC devices is shown in Table 2. This table includes an itemization of the device performance meeting the program goals. Figure 2

shows a timeline listing the progress of MCNC device DC performance. Continuing improvement is expected, and this improvement will be reflected in the rf device performance.

Table 1 shows that comparable net gains at 1 GHz have been achieved by each program. Note, however, that MCNC reports this gain at a much lower anode current than SRI, and with a much smaller array than Raytheon. Further, both rf and DC testing at MCNC are performed with the device operating continuous-wave (CW), that is, at a 100% duty cycle. SRI operates the device in 1-second pulses, in order to prevent damage to the anode. Raytheon also performs rf testing CW, but operates their device at a lower applied gate voltage.

The size of the array used in the tests is also in Table 1. The programs at SRI and Raytheon used the largest arrays that they have been capable of fabricating in their testing. MCNC, on the other hand, uses an array which is relatively small compared to some that have given good results at DC. The total current and transconductance will scale with the number of tips in an array. Larger arrays can also operate at a given anode current level with lower electrical stress on the device. This should result in improved test lifetimes.

Calculated and measured input capacitance is shown for devices produced at MCNC. Raytheon also gives a measured value, while SRI gives an estimate of capacitance neglecting fringing fields in the dielectric. Because of package and test fixture parasitic capacitances, the practical value of the device capacitance is generally quite a bit higher than the calculated value. In practice, this will limit the high-frequency performance of the device. The inherent capacitance of a device with given area and tip spacing is dependent on the specifics of the fabrication process and the materials used. Neither SRI or Raytheon have a process which allows substantial reduction of the device capacitance. The MIT-Lincoln Labs process limits their devices to 300 – 1000 Å of oxide, decreasing as the tip density increases. Eventually, this will produce problems not only with device capacitance, but also with dielectric breakdown. MCNC has the option of increasing column height and oxide thickness to 6 μm or greater, causing a further drop in device capacitance and a proportional increase in f_T.

The devices used for rf testing at MCNC have a 4 μm insulating layer between the substrate and the gate electrode. While DC testing on devices with column heights of 2 μm or less has been ongoing, these devices were not tested at rf because of the anticipated higher device capacitance. Fabrication of the 4 μm devices was completed in early January, and even at this early stage of testing we were able to demonstrate modulation at 1 GHz. As we test more devices we fully expect to observe higher DC emission currents, consistent with the 2 μm column devices, and as a result, higher gain at 1 GHz rf modulation.

The total transconductance for the arrays tested by each program is also shown in Table 1. The value reported by MCNC, 8.7 μS, is calculated from the I-V curve measured during the rf test. The value included for the SRI program, 660 μS, is the only value reported, and applies to a device that was used in another test. The value for Raytheon, 30 μS, is the value used in their equivalent circuit as

shown at IEDM. Using these values with the values given for device capacitance allows calculation of f_T for each device.

Measured input impedances for MCNC and Raytheon devices at 1 GHz are comparable, and close to 50 Ω. SRI does not report input impedance, but based on the given value of capacitance, the magnitude should be around 1.6 kΩ, which gives a much larger impedance mismatch at the input of the device.

To verify that the gain was measured accurately at 1 GHz, an identical device was tested using the same test methods, but at lower frequencies (1 – 50 MHz). The resulting data is shown as gain as a function of frequency and anode current in Figure 3. Extrapolating to 1 GHz from this data using the same anode current as in the higher frequency test shows reasonable agreement with the measured data. The gain curves also reinforce the calculated value for f_T for devices produced at MCNC.

SUMMARY

Based on test performance data, MCNC has satisfied all of the performance milestones for Phase I of the ARPA Field Emitter Array RF Amplifier Development Project. We understand that competing programs have also met the criteria, but by comparison with the data that has been published, we have exceed their performance in many respects. As better data is collected, it will be promptly reported. Based on these preliminary results, we feel that the device produced at MCNC is the best choice for high-frequency operation.

FIGURES

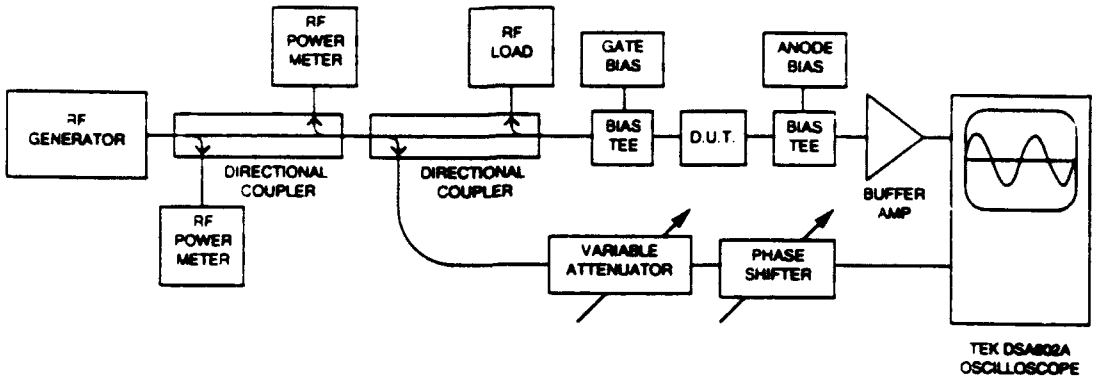


Figure 1: Schematic diagram of the equipment used for high-frequency testing.

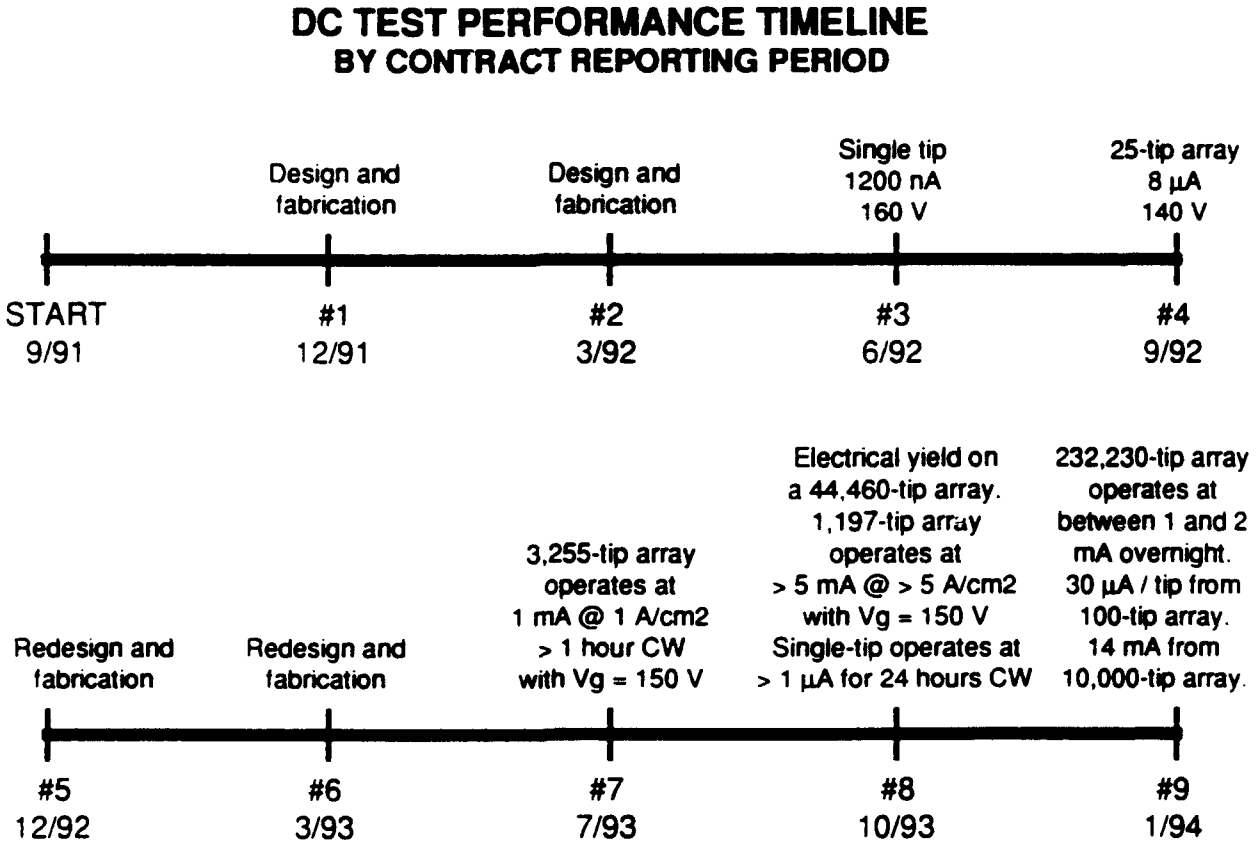


Figure 2: Timeline showing progress of MCNC device DC performance.

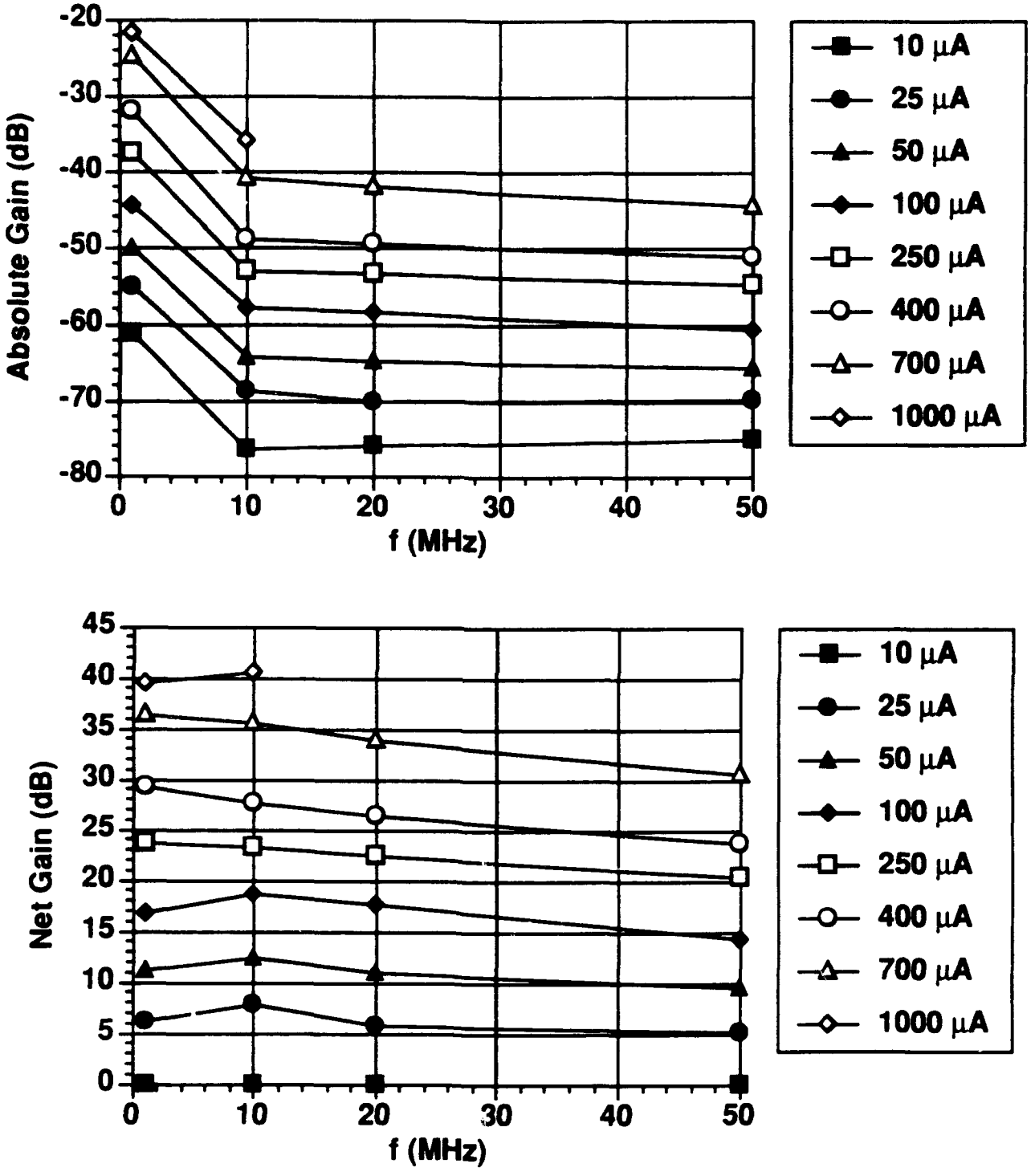


Figure 4: Gain as a function of frequency and anode current at low rf frequencies.

TABLES

	MCNC	SRI	Raytheon
Net Gain at 1 GHz	0.84 dB	0.7 dB	~ 1 dB
Test Mode	CW, rf and DC	1 sec pulse rf, 60 Hz DC	CW rf, 2% duty cycle DC
Anode Current	172 μA	1 mA	150 μA
Gate Voltage	147.4 V	Not Reported	72.3 V
Array Size	1,197	625	26,248
Per-tip Current	144 nA	1.6 μA	5.7 nA
Oxide Thickness	4 μm	1 μm	1 μm
Input Capacitance	1.7 pF (calculated) 4.5 pF (measured)	0.1 pF (estimated)	8 pF (measured)
Total gm	8.7 μS	660 μS	30 μS
f_T	0.308 MHz	1.05 GHz	0.597 MHz
Input Impedance at 1 GHz	20 - j19 Ω	Reported as "high" 1.6 kΩ estimated	6 - j20 Ω

Table 1: Comparison of test conditions and results reported by MCNC and other programs.

	MCNC	SRI	Raytheon
Maximum Anode Current	14 mA	25 mA	70 mA
Maximum Current Density	7 A/cm^2	1000 A/cm^2	8 A/cm^2
Test Lifetime	15 minutes CW rf 24 hours CW DC	> 10 hours of 1 second pulses at 1 GHz > 8700 hours at low duty cycle 60 Hz DC testing	Not Reported
Maximum Per-tip Current	30 μA	100 μA	14 μA
Maximum Per-tip g_m	4.5 μS	5.0 μS	0.8 μS
Typical Emission Efficiency	> 99%	Not Reported	Not Reported
Projected Input Impedance at 10 GHz	20 + j190 Ω	- j160 Ω	6 - j2 Ω
projected net gain at 1 GHz with Ia = 10 mA	15 dB	5 dB	Insufficient information given.

Table 2: Maximum reported and projected performance for MCNC and other program devices.

Duke Subcontract Report:
Input Impedance of Field Emitter Arrays

1 Introduction

Recently, high frequency measurements made at MCNC have shown modulated emission current at frequencies up to 1 GHz. The testing is performed at a constant DC bias voltage and anode current level. Since the RF source may drift somewhat during measurement, the test setup is designed to eliminate drift as a source of measurement error. A new RF test fixture has been employed for these recent measurements. In this report, the devices in the new RF test fixture are characterized.

2 Measurement setup

In order to show modulation of the emission current at a frequency of 1 GHz, a test procedure was devised that allows cancellation of the feedthrough signal with an attenuated and phase shifted sample of the input signal. In addition to providing stability with respect to the generator, this method of cancelling the feedthrough signal allows for accurate measurement of incremental changes in the modulated current with changes in bias current. Another change is a buffer amplifier now inserted between the bias tee and the oscilloscope at the output. This circuit serves two functions, giving a modest amount of gain for the RF signal and protecting the oscilloscope should a device fail during testing. The effects of this buffer circuit are removed in the analysis of device performance. A detailed description of the test setup and equipment is given in another section of this quarterly report. A new high frequency package was purchased for these measurements as well. This package is built by Kyocera and is made only of metal and ceramic.

The 4 μm column devices are deemed most appropriate for operation at high frequencies as a result of their lower capacitance. With the recent completion of the manufacturing of the 4 μm column devices, testing has begun at a fast pace. DC measurements on the arrays have shown more stable emission and fewer problems during testing. In the current test setup, the chips containing the emitter arrays are connected to the RF package by a fluxless solder or an epoxy paste. Then the leads of the SMA bulkhead connectors mounted to package are connected to an individual array with a gold wire bond. S-parameter measurements of these devices are described in the next section.

3 Device measurements

The s-parameters, input impedances, and capacitances of the devices in the Kyocera packages are measured with a Hewlett Packard 8753A Network Analyzer to determine an input equivalent circuit. Similar measurements are made for the output. By connecting the device in the foward direction, S_{11} and S_{21} are measured. By reversing the connections, S_{22} and

S_{12} are measured. The devices measured are 1197-tip arrays, with 10 μm spacing between adjacent emitters and hexagonal packing. The emitter pedestal or column height is 4 μm making the gate-to-base spacing 3.8 μm (the column height minus half of the gate metal thickness).

Since the output impedance is determined solely by the capacitance between the anode and the substrate, it is large in magnitude and reactive (capacitive). Thus, the output impedance is mismatched into 50 Ω. At 1 GHz, the measured input impedance is

$$Z_{in} = 0.9 - j49.5\ \Omega \tag{1}$$

The capacitance of the device in the test setup is measured as 2.2 pF at low frequencies (around 10 MHz). The input impedance is real, $Z_{in} = 10.83\ \Omega$, at 1.83 GHz. This indicates that the lead inductance of the wire bond is resonant with the capacitance of the device at this freqency. Assuming a simple series RLC input equivalent circuit, the resonance corresponds to a lead inductance of

$$L = \frac{1}{\omega^2 C} = \frac{1}{(2\pi \times 1.83 \times 10^9)^2\ 2.2 \times 10^{-12}} = 3.45\ nH \tag{2}$$

The inductance of the wire bond over the ground plane can be approximated by the inductance of a two conductor transmission line. The wire bond to the gate pad is made with a 1 mil diameter gold wire. The radius in mm is $0.5 \times 10^{-3}\ in \times 25.4\ mm/in = 1.27 \times 10^{-2}\ mm$. The bond wire is approximately 4 mm long and is about 1 mm above a ground plane. For a two conductor transmission line with conductor radius a and separation $2h$, the inductance is given by

$$L = \frac{\mu_o}{\pi} \ln\left(\frac{2h}{a}\right)\ (H/m) \tag{3}$$

The inductance of the single wire bond is half of this value, or

$$L = \frac{1}{2}\left(\frac{4\pi \times 10^{-7}}{\pi}\right) \ln\left(\frac{2\ mm}{1.27 \times 10^{-2}\ mm}\right) = 1.01\ nH/mm \tag{4}$$

This equation gives an inductance of about 4.0 nH, close to the expected value. Thus, the value of measured inductance is consistent with the calculated value for a wire bond of the size indicated for a simple series RLC equivalent circuit.

The capacitance is only slightly larger than the expected value. To calculate the capacitance for the field emitter arrays, the total capacitance is separated into three components, the parallel plate capacitance of the gate metal, C_{pp}, the fringing capacitance of the outer edge of the array, C_{fr}, and the fringing and tip capacitance of the gate apertures, C_{tip}. Calculations yield a capacitance of

$$C_{tot} = C_{pp} + C_{fr} + C_{tip} = 1.713\ pF + 0.076\ pF + 0.131\ pF = 1.920\ pF \tag{5}$$

only slightly less than the measured value.

The measurements on 2 μm column devices yield similar results. The input impedance of a 2 μm column device is generally around $18 - j18\Omega$. The input impedance is real at

1.39 GHz and the capacitance is measured as 3.8 pF. Using these numbers, the calculated series inductance is again 3.45 nH. The array capacitance is calculated to be

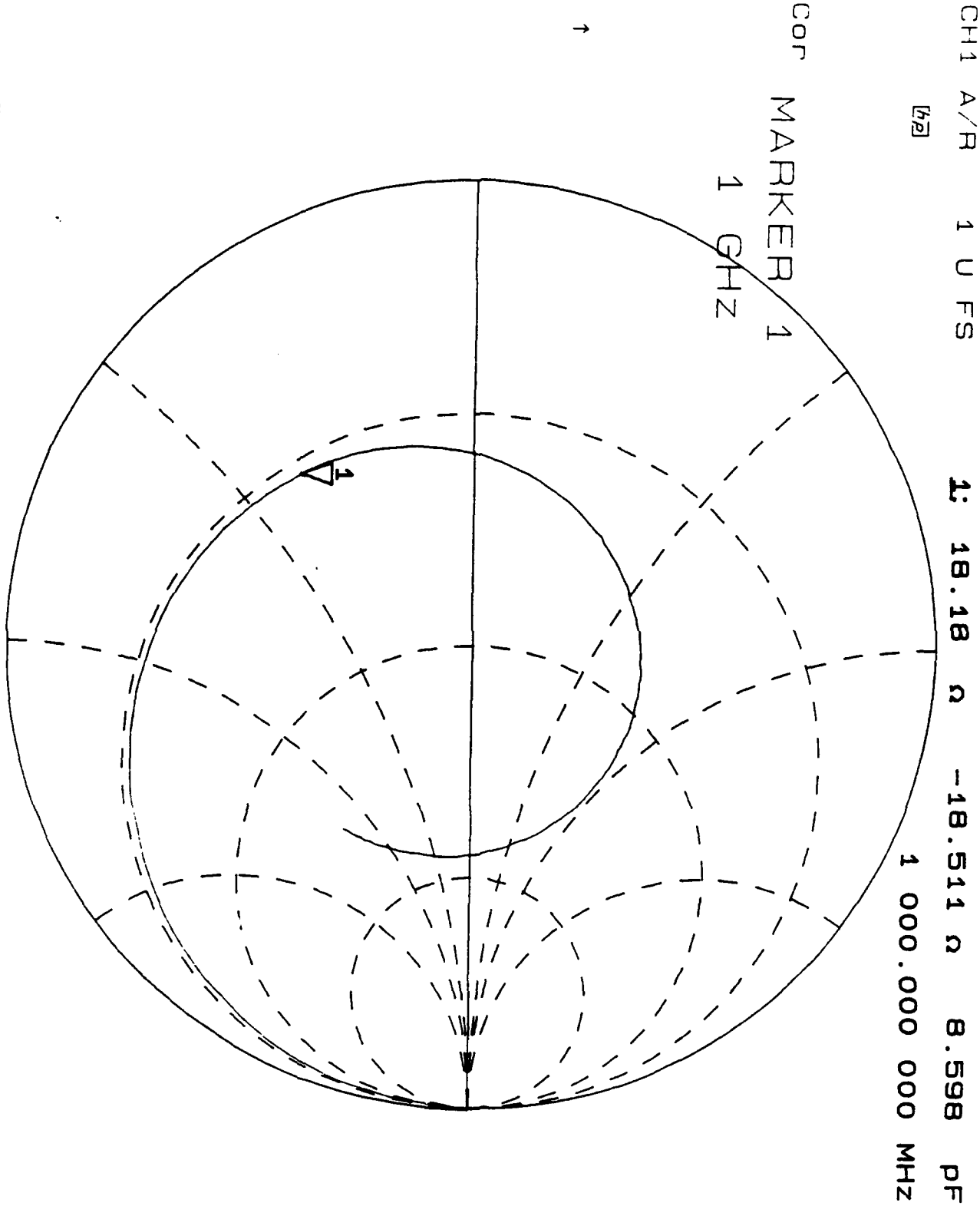
$$C_{tot} = C_{pp} + C_{fr} + C_{tip} = 3.616\ pF + 0.090\ pF + 0.144\ pF = 3.850\ pF \quad (6)$$

This value of capacitance is essentially the same as the measured value. Attached to this report is the Smith chart plot of the input impedance for a typical 2 μm device showing its input impedance and reactance versus frequency. The frequency range for this plot is 300 kHz to 3 GHz. The curve for the input impedance increases in frequency as it progresses counter clockwise. The marker is at 1 GHz.

4 Conclusion

The input and output impedances of the devices in the new high frequency test fixture have been measured. The output impedance is a large capacitive reactance indicating a relatively small parallel capacitance between the anode and ground. Thus, the output circuit is highly mismatched into 50 Ω. The capacitances and inductances in the input equivalent circuits of the 2 μm and 4 μm column arrays are close to the calculated values. The high frequency test procedure and test fixture have been successfully employed to measure modulated current from field emitter arrays at frequencies from 1 MHz to 1 GHz.

ATTACHMENT B



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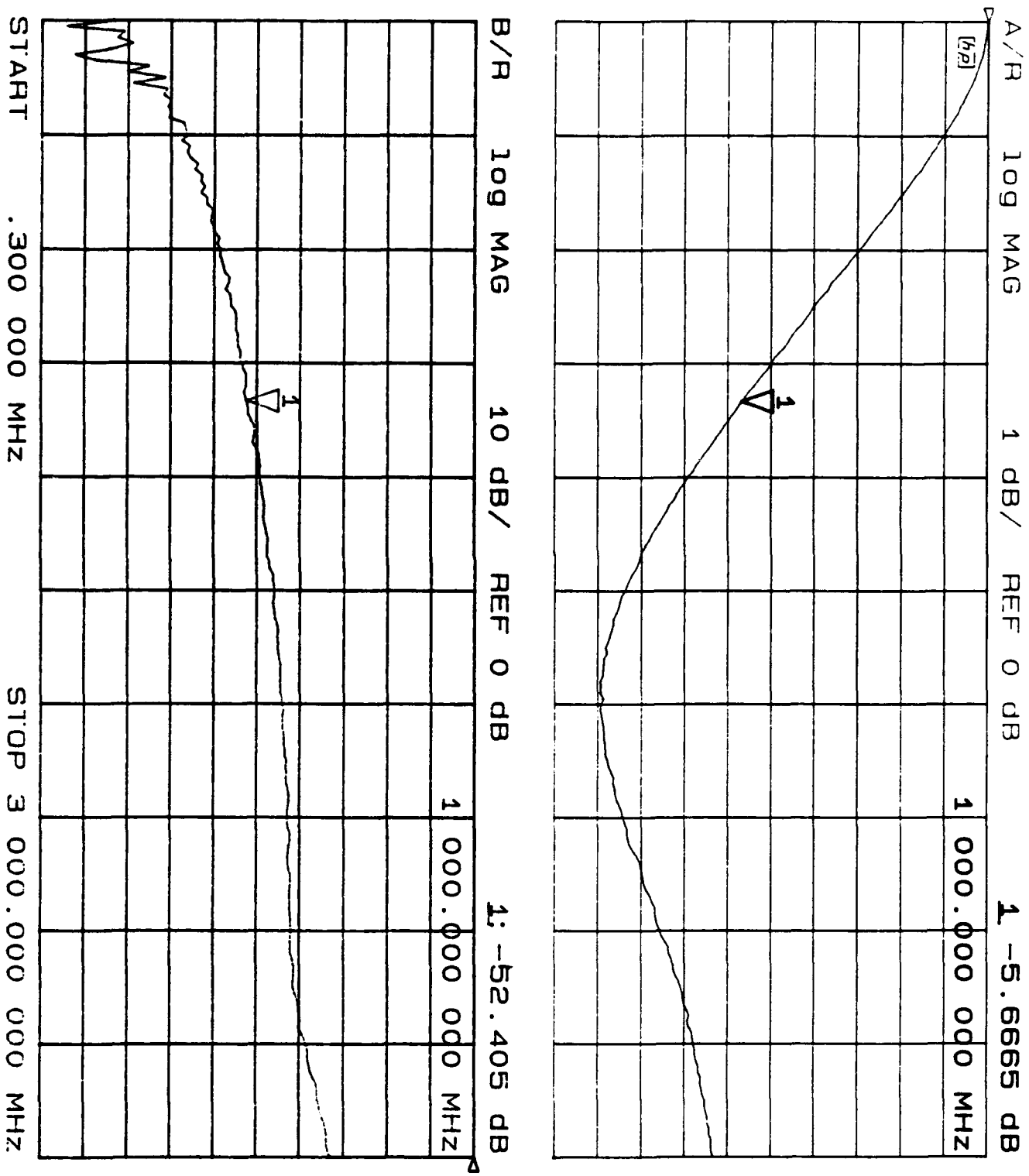

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