FINAL REPORT

US ARMY SBIR PHASE II

THE INFLUENCE OF TEMPERATURE ON MICROELECTRONIC DEVICE FAILURE MECHANISMS

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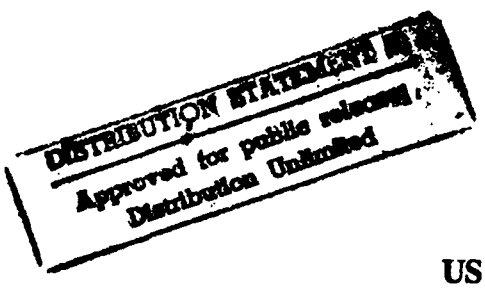

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PREFACE

There has been a common belief that reliable electronics can be achieved by lowering temperature. Elevated temperature has in the past been considered a dominant stress that lowers reliability, so every effort has been made to lower operating temperature until the desired reliability is achieved. The belief in the harmful effects of temperature has woven itself into today's screening and thermal derating processes. High-reliability applications require that the microelectronic device be subjected to high-temperature stress screens, like burn-in, to improve the reliability of the product. Moreover, thermal derating measures for microelectronics often involve lowering temperature.

A problem arises when there is no way to evaluate the temperature sensitivity of device design. The design team has no choice but to follow the prescription of lowering temperature when there is no scientific tool to answer the questions:

- Is there a need for lowering temperature?
- If there is need for lowering temperature, what is the value of the lower temperature as a function of device architecture?
- How does the maximum operating temperature vary with microelectronic device

design?

- What device design modifications are necessary to vary the maximum allowable operating temperature for a desired mission life?
- How do manufacturing defect magnitudes affect the time to failure under temperature stress?
- Is it possible to change any other form of stress instead of temperature to achieve the desired mission life and still escape the penalty of the added cost and weight of a cooling system? This book attempts to address these questions.

The purpose of this book is to raise the level of understanding of thermal design criteria beyond simply lowering the operating temperature to achieve reliability. The goal is to provide the design team with sufficient knowledge to help them evaluate device architecture trade-offs and the effects of operating temperature, rather than just cooling the system to a lower temperature in expectation of higher reliability. The penalty of added cost and weight associated with lowering temperature can be minimized by exploring cost effective options in terms of derating other non-temperature stresses. This book will also assist with evaluating the effects of certain classes of manufacturing defects on operating life for high-temperature operation in order to tailor existing screens for maximum defect detection and overall device quality.

This book is directed to the reader interested in the damage mechanisms associated with various forms of temperature stress in microelectronic packages. The microelectronic package considered for the purpose of this investigation is assumed to consist of a bipolar or MOSFET (silicon) semiconductor device; first-level interconnects that may be wirebonds, flip-chip, or tape automated bonds; die attach; substrate; substrate attach; case; lid; lid seal; and lead seal. Failure mechanisms actuated under various forms of temperature stress, including steady-state temperature, temperature cycling, temperature gradients, and time-dependent temperature change, have been identified for each of the package elements. The temperature effects on electrical parameters of both bipolar and MOSFET devices have been investigated, and models quantifying the temperature effects on package elements have been identified. Temperature- related models have been used to derive derating criteria for determining the maximum and minimum allowable temperature stresses for a given microelectronic package architecture. The reader should have prior knowledge of bipolar and MOSFET device fundamentals, semiconductor device physics, fracture mechanics, and elasticity dynamics.

This book does not address damage mechanisms in device technologies other than bipolar and MOS, or assemblies such as circuit cards, printed wiring boards, sub-assemblies, and assemblies. This investigation covers damage mechanisms in

the temperature range of -55°C to 125°C. At temperatures much higher or lower than this temperature range, the damage mechanisms in the microelectronic package can change considerably with respect to their stress dependencies.

In Chapter 1, we discuss the motivation for the research work presented in this book. The existing strategies for modeling the effects of temperature on microelectronic device reliability have been discussed. Some of the problems with the existing modeling strategies have been outlined.

In Chapter 2, we discuss microelectronic device failure mechanisms in terms of their dependence on steady state temperature, temperature cycle, temperature gradient, and rate of change of temperature. The microelectronic package is considered to be an assembly of package elements, including the chip, chip metallization, operating devices on the chip, die attach, substrate, substrate attach, first-level interconnects (wirebond interconnects, tape automated bonds, flip-chip bonds), leads, lid, lead seal and lid seal. Common models used to characterize these failure mechanisms are identified and the variability in temperature dependence of each of the failure mechanisms is characterized. We also discuss the existence of temperature thresholds below which various failure mechanisms are not significantly activated.

In Chapter 3, the effect of temperature on the performance characteristics of MOS and bipolar devices is examined. The parameters investigated for bipolar devices include the current gain, I-V characteristics, collector-emitter saturation voltage, and voltage transfer characteristics. The parameters investigated for MOS devices include threshold voltage, mobility, drain current, time delay, leakage currents, chip availability, dc voltage transfer characteristics and noise margins.

In Chapter 4, the applicability of using high-temperature stress screens, including burn-in, for high-reliability applications is discussed. The burn-in conditions used by some manufacturers are examined, and a physics-of-failure approach is proposed. The proposed physics-of-failure approach addresses the dominant failure mechanisms in the device architecture and tailors the screening stresses to effectively remove defective devices.

Chapter 5 briefly overviews existing guidelines for thermal derating of microelectronic devices, which presently involve lowering the junction temperature. Then, the models presented in Chapter 2 for various failure processes, are used to evaluate the sensitivity of device life to variations in manufacturing defects, device architecture, temperature, and non-temperature stresses. Derating curves for constant device life are derived for mechanisms with complex dependencies on stresses and defects. The cumulative effect of competing failure processes on device life is used to determine the values of operating temperature and non-temperature related stresses. We give special thanks to

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6.2. Derating curve for mission life versus steady state temperature for dominant failure mechanisms, at a specified values of non-temperature operational stresses. This derating plot an be used to derate non-temperature operational stresses for cost-effective designs which are reliable at high temperature.

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INTRODUCTION

1.1 MICROELECTRONIC DEVICE PERFORMANCE AND RELIABILITY: ROLE OF TEMPERATURE

Temperature is a fundamental parameter associated with the performance and reliability of electronic equipment. Performance is defined by electrical parameters such as threshold voltage, propagation delay, leakage currents, and noise margins. Performance failures (out of specification limits), typically do not render the device non-operational, and must therefore be characterized most generally by impairment of electrical functionality resulting from parameter drifts. Temperature dependence of performance is thus, quantified by the variation of electrical parameters versus temperature stress including steady state temperature, temperature cycle, temperature gradient, time dependent temperature change.

Reliability is defined by the ability of a device to fulfill its intended function. Reliability is a function of failure mechanisms operative in the package architecture which results in circuit malfunction causing equipment failure. Reliability related failures render the device non-operational because of damage resulting from failure mechanisms. Reliability temperature dependence is thus

quantified by the dominance of failure mechanisms versus temperature stress. While operation at high temperature may not affect the reliability of a device, it may reveal that at high temperature, the device does not meet performance requirements, due to threshold voltage drift, increased leakage currents, and increased propagation delay. This may indicate the need for a design change, or the unsuitability of the technology for high-temperature operation. [Semiconductor Reliability News 1990, BT 1984, CNET 1983, MIL-HDBK-217, NTT 1985, RPP 1988]

1.2 SINGLE ACTIVATION ENERGY ARRHENIUS MODELS: WHAT IS THE PROBLEM?

In the past, effect of temperature in its many forms has been neglected in terms of the effect on overall device reliability of steady-state temperature, temperature change, rate of temperature change, or spatial temperature gradient [Wong 1990, Blanks 1990, Witzmann and Giroux 1991]. Temperature-dependent models, such as the Eyring and Arrhenius models, originally proposed to model the effect of temperature on chemical reaction rates, have been widely applied to model overall microelectronic device reliability. The governing equation assigns an activation energy to the device which is used to predict reliability over all temperatures. These models are often used to show the effect of temperature on electronic component failure rates, under the assumption that the dominant component failure mechanisms depend on steady-state temperature. This assumption is carried further to derive activation energies or thermal acceleration factors for the device based on a weighted averaging methodology, and to characterize the device failure rate as an exponential function of temperature.

The use of a single activation energy to describe the thermal acceleration of device failure rate, in which failure mechanisms have temperature accelerations varying from 6.5 to 503, has been observed to be inappropriate and misleading [Setliff 1991, O'Connor 1990, Hakim 1990]. Moreover, new failure mechanisms can become dominant, depending on manufacturing processes, and the actual failure mechanism experienced by the device can vary. No failure mechanism can remain dominant, or even significant, for very long [Witzmann and Giroux 1991]. The continual use of a single activation energy of 0.7 eV for a device when hot electrons (with an activation energy of -0.06eV) are the dominant failure mechanism will actually predict a decrease in the mean time between failures (MTBF) with rising temperature, when actually the MTBF will increase with increasing temperature; this causes the system designer to lower the temperature further, unintentionally decreasing reliability [Setliff 1991]. Due to the

multiplicity of temperature dependencies of failure mechanisms, geometric and structural variables, device materials, and processing variables, and because of the non-exponential dependence of lifetimes on temperature, it is not possible to derive meaningful models for thermal variation of lifetimes with a single activation energy for the device.

1.3 RELIABILITY PREDICTION METHODOLOGIES: WHAT IS THE PROBLEM?

The Arrhenius model derives its importance from the fact that it has been embedded in the part failure-rate prediction models of MIL-HDBK-217, "Reliability Prediction of Electronic Equipment." Most microelectronic failure rate models in MIL-HDBK-217 are of the form

$$\lambda_p = \lambda_B \prod \pi_i \quad (1.1)$$

where λ_p is the device failure rate, λ_B is the base failure rate, and π_i are the various factors for quality, temperature, and voltage. The temperature acceleration factor (π_T), which is an exponential function of temperature, is often the only stress term that determines the part failure rate. Lower temperature is thus associated with higher reliability, supporting the steady-state temperature dependence of device failure rates.

1.4 VARIABILITY OF LIFE VERSUS ACTIVATION ENERGY

The Arrhenius functional relationship between the MTBF and temperature is such that a variation of 0.1 eV may vary the MTBF by an order of magnitude. This is worsened by the wide variation in the activation energies described in the literature for various failure mechanisms and manufacturing defects. The variability of activation energy for the same failure mechanism is so great that the predicted reliability has little meaning (Table 1.1).

1.5 SCREENING AND ACCELERATED TESTING: WHAT IS THE PROBLEM?

The effects of temperature on microelectronic devices are often assessed by accelerated tests carried out at high temperatures. The results are then extrapolated to operating conditions (-55°C to 125°C) to obtain a value for the thermal acceleration of device failures. Implicit in the test strategy is the assumption that all the device failure mechanisms are exponential functions of

temperature, and that the failure mechanisms active at higher temperatures are also active in the equipment operating range of -55°C to 125°C. But the high temperature failure mechanisms (> 125°C) that do not exist in the equipment operating range can be operational at higher temperatures.

The reliability of electronic devices has often been represented by an idealized plot called the bathtub curve (Figure 1.1), which consists of three regions. In region A, the failure rate decreases with time, and is called the infant mortality or early-life failure region. In region B, the failure rate has reached a relatively constant level, and is called the constant failure rate or useful life region. In region C, the failure rate increases again, and is called the wearout region. Many modern semiconductors have been improved to the point where the infant mortality and useful life regions have failure rates so near zero that the bathtub curve "no longer holds water" [Wong 1990, Beasley 1990]. Indeed, the result of continuous reliability improvement is that most mature semiconductor products and integrated circuits do not require screens such as burn-in. Modern semiconductors should not reach the wearout portion of the curve when operated within specification limits and within reasonable equipment lifetimes. In fact, for many failure mechanisms the wearout portion of the curve has been delayed beyond the useful life of many devices [Hakim 1990, McLinn 1990, O'Connor 1990].

Over the years, the process of burn-in has deteriorated into an insurance policy used to check reliability or satisfy customer-imposed requirements. Burn-in procedures are often conducted without any prior identification the nature of the defects to be precipitated, the failure mechanisms active in the device, or their sensitivity to steady-state temperature stress, or without any quantitative evidence of the improvement achieved by the process. Current failure data indicates that burn-in prior to use does not remove many failures and, on the contrary, may cause failures due to additional handling. Chapter 4 discusses the applicability of high-temperature stress screens, such as burn-in, for improvement of overall product quality for high-reliability applications. It also proposes an approach to address the dominant failure mechanisms in a device architecture to tailor the burn -in stresses for effective removal of defective devices.

The Bathtub Curve

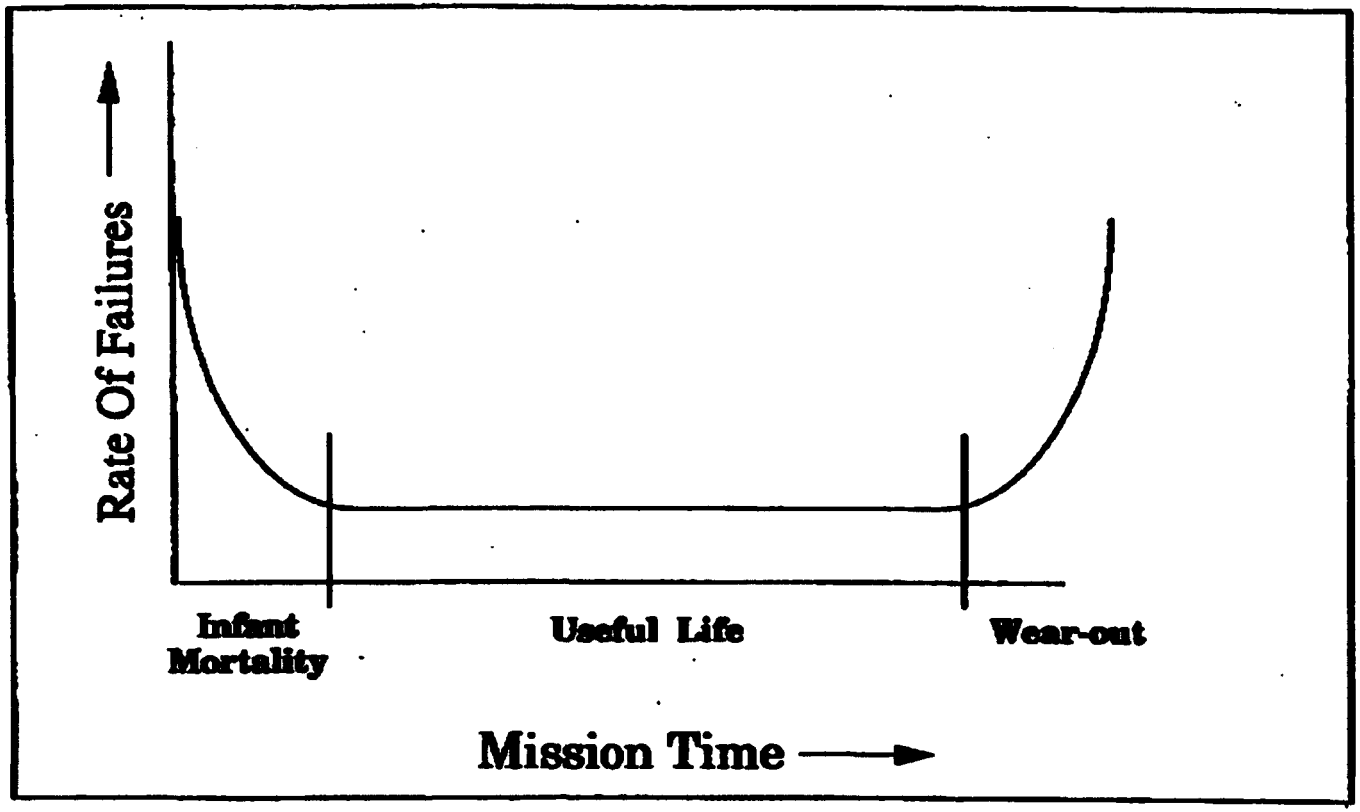


Figure 1.1 The reliability of electronic devices has often been represented by an idealized graph called the Bathtub Curve.

Table 1.1 Activation Energies For Common Failure Mechanisms

Failure mechanism/ manufacturing defect	Activation energy (eV)	Reference
Die Metallization Failure Mechanisms		
Metal corrosion	0.3 - 0.6 eV 0.77 - 0.81 eV	[Hakim 1989, Jensen 1982, Amerasekera 1987] [Peck 1986]
Electromigration	0.5 eV (Small grain Al) 0.43 eV (Al) 0.35 - 0.85 eV (Al) 1.0 eV (Large grain glassivated Al) 0.24 - 0.57 eV (Al) 0.7 eV (Al) 1.67 - 2.56 eV (Al-1%Si) 0.58 eV (Al-1%Si) 0.96 eV (Al-1%Si)	[Black 1982] [Ghate 1981, Towner, 1983] [Lloyd, 1987] [Nanda 1978, Jensen 1982] [Reimer, 1984] [Siato, 1974] [Suehle, 1989] [Schafft, 1985] [Fantini, 1989]
Metallization migration	1 eV 2.3 eV	[Abbott 1976] [Jensen 1982]
Stress-driven diffusive voiding (constraint cavitation)	0.4 eV 1.0 - 1.4 eV	[McPherson and Dunn, 1987] [Tezaki, *et.al.*, 1990]
Device and Device Oxide Failure Mechanisms		
Ionic contamination (surface, bulk)	0.6 - 1.4 eV 1.4 eV	[Amerasekera 1987] [Jensen 1982]
Hot carrier	-0.06 eV	[Hakim 1989]
Slow trapping	1.3 - 1.4 eV	[Jensen 1982]
Gate-oxide breakdown A. ESD B. TDDB C. EOS	 0.3 - 0.4 eV; 0.3 eV 1 eV 0.3 eV 2.1 eV 0.3 - 1.0 eV 2 eV	 [Baglee 1984, Crook 1979] [Hokari 1982] [Crook, 1979] [Anolick and Nelson, 1979] [McPherson, 1985] [Anolick 1979]
Surface-charge spreading	1.0 eV 0.5 - 1.0 eV	[Hakim 1989] [Jensen 1982, Amerasekera 1987]
First-level Interconnection Failure Mechanisms		
Au-Al intermetallic growth	0.5 eV 1.0 eV 1.1 eV 2.0 eV	[Irvin 1978] [Hakim 1989, Jensen 1982] [Mizugashira 1985] [White 1978]

1.6 THERMAL DERATING GUIDELINES: WHAT IS THE PROBLEM?

Belief in the harmful effects of temperature and dependence on the Arrhenius equation have also woven itself into the thermal derating criteria. Existing guidelines for thermal derating of devices often suggest lowering the operating temperature [MIL-STD-883, Brummet 1982, Eskin 1984, Naval Air Systems Command AS-4613 1976, Westinghouse 1986]. Such derating criteria, in addition to misleading the designer to believe increased reliability has been obtained with lowered temperatures, also rule out the possibility of using cost-effective designs at elevated temperature. Furthermore, hard low-temperature values specified for a device's derating criteria do not account for the effects of device architecture and design modifications on the required operating temperature for a given reliability. Chapter 5 uses the models investigated for various failure processes in Chapter 2 to evaluate the sensitivities of device life to variations in manufacturing defects, device architecture, temperature, and non-temperature stresses. Derating curves for constant device life are derived for mechanisms with complex stress and defect dependencies.

1.7 THE OBJECTIVE

A global methodology is presented here to address the effect of temperature on microelectronic reliability through a rational design approach to temperature and cost-effective reliability dictating the following elements in sequence:

- determining the dominant failure mechanisms in the microelectronic device;
- determining the dominant temperature dependencies of various failure mechanisms in terms of steady-state temperature, temperature cycle magnitude, temperature gradient, and time dependent-temperature change;
- providing derating guidelines for determining an upper temperature limit — based on actual negative effects of steady-state temperature, temperature cycling, temperature gradient, and time-dependent temperature change — that must be avoided for failure mechanisms having temperature dependencies.

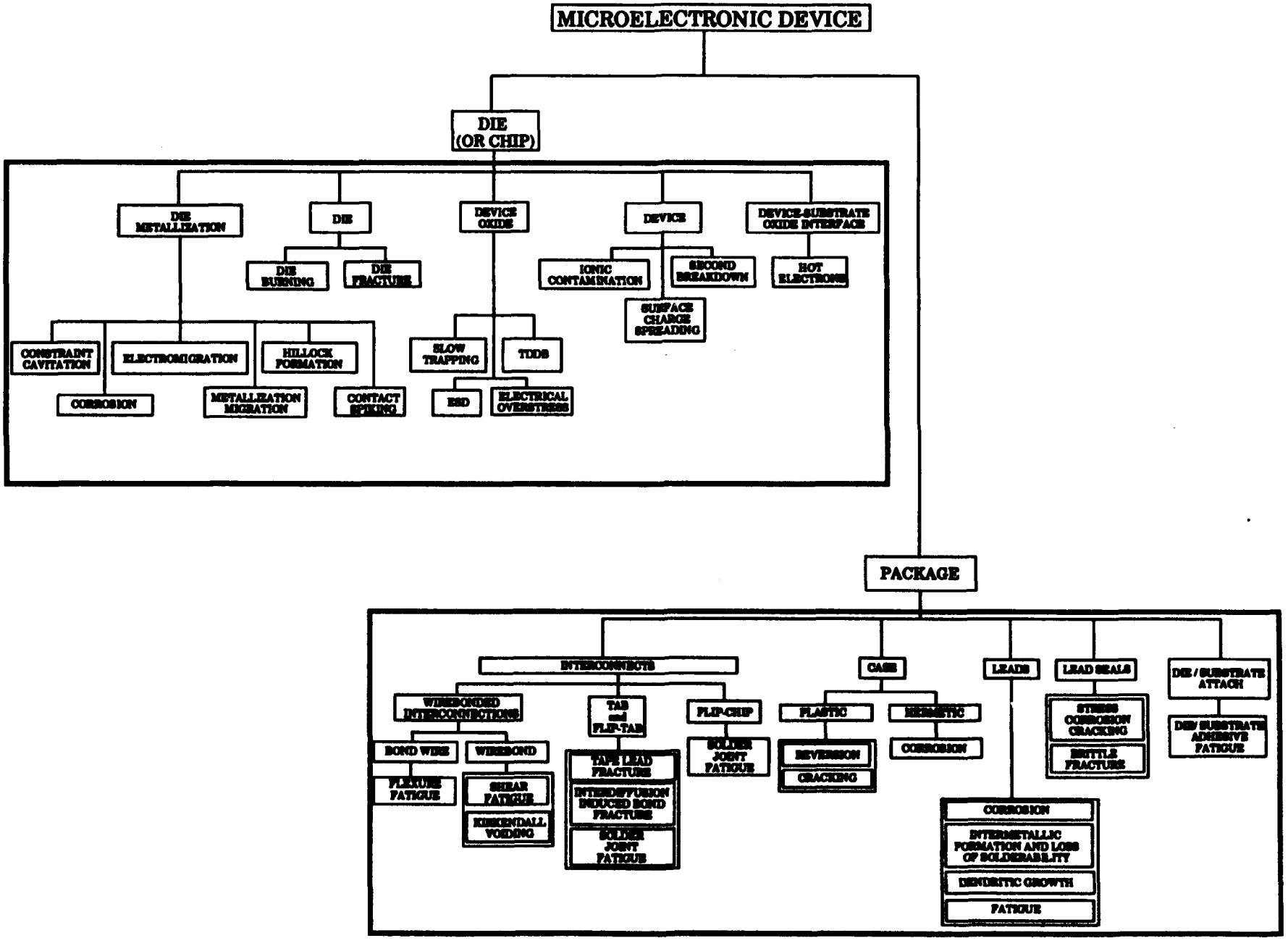
2

TEMPERATURE DEPENDENCE OF MICROELECTRONIC DEVICE FAILURE MECHANISMS

2.1 INTRODUCTION

This chapter examines failure mechanisms for various package elements in terms of their temperature dependencies (Figure 2.1). Temperature effects have been broadly classified as steady-state temperature, temperature cycling, temperature gradient, and time-dependent temperature change. The microelectronic components examined here are the chip (die) and the device packaging. The chip has been further subdivided into die metallization, device oxide, device, and device-oxide interface. Device packaging has been subdivided into first-level interconnects, package case, leads, lead seals, die, and substrate attaches. First-level interconnects include wirebonded interconnects, TAB, flip-TAB, and flip-chip.

Figure 2.1 Failure mechanisms in microelectronic devices have been classified according to failure sites at die (or chip) level and first level package



Failure mechanisms occurring predominantly at the die level include slow trapping, hot electrons, electrical overstress, electrostatic discharge, dielectric failure, oxide breakdown, and electromigration. First-level package failure mechanisms generally arise from corrosion, differential thermal expansion between bonded materials, large time-dependent temperature changes, and large spatial temperature gradients, all of which can cause tensile, compressive, bending, fatigue, and fracture failures. Corrosion-induced failure mechanisms include electrolyte formation and galvanic and ionic corrosion. Corrosion failures are complex functions of contamination, temperature, humidity, and bias. All failure mechanisms have been discussed here in terms of their dominant temperature dependencies. Failure mechanisms with a dominant temperature dependence in the range of -55 to 125 °C have also been identified.

2.2 TEMPERATURE DEPENDENCIES OF FAILURE MECHANISMS IN THE DIE METALLIZATION

2.2.1 Corrosion of Metallization and Bond Pads

Electrolytic Corrosion. Corrosion is typically defined as the chemical or electrochemical reaction of a metal with the surrounding environment. The mechanisms of corrosion can be divided into two types: dry -- such as oxidation of aluminum in air, and wet -- in which the reaction occurs in the presence of an electrolyte, a moist environment, and an electromotive force. Dry corrosion is of minor importance in semiconductor devices, since the corrosion process is self-passivating, forming a thin oxide film that prevents further oxidation. Wet corrosion, in the presence of an ionic contaminant, and moisture can provide a conductive path for electrical leakage between adjacent conductors, dendritic growth, or corrosion of the device metallization or bond pads. The ions most commonly found on the die surface that, in the presence of water, give rise to the electrolytic solution required to trigger the corrosion process include:

- halogens (especially Cl^-) deriving their origin both from inadequate removal of fabrication process residue and from plastic containers;
- alkalines (especially Na^+) derived from the diffusion ovens, glass containers, and the hands of operators; and
- phosphorus, which, unlike contaminating ions, is specially incorporated in the surface passivation glass to improve its mechanical characteristics and restrict the effects of Na^+.

The importance of passivation in microcircuit metallization corrosion versus temperature has been evaluated by Commizolli, who found that the dependence of corrosion current on temperature appeared linear between 60°C and 100°C. The corrosion current at 90% relative humidity using passivated chips decreased with a decrease in temperature between 60°C and 100°C [1980].

Pecht modeled the time to failure due to corrosion as the sum of moisture ingress time and the time for corrosion attack and failure. The moisture ingress time for a hermetic package was determined based on the internal volume and the leak rate. The method for calculating the worst-case operation-independent moisture ingress time was based on standard testing procedures. After sufficient moisture ingress, a critical moisture content will be reached inside the package, and corrosion can initiate once the non-operating sealed package is exposed to temperatures below the dew point. At this time, the moisture inside the package condenses and combines with any ionic contaminant present to provide a conductive path between adjacent metallic conductors. The conductive path serves as a medium for the transfer of ions in the corrosion process. When the package is operating, the heat dissipated inside the package will typically elevate the temperature above the dew point. Consequently, the electrolyte will evaporate and no longer provide an electrolytic path between conductors. Elevated temperature due to device power thus acts as a mechanism to slow the corrosion process [Pecht and Ko 1990, RAC Report SOAR-3 1985].

When a packaged component is in the off mode, it can equilibrate with the ambient RH. However, when the packaged component reaches its operating temperature, the same moisture content results in a lower relative humidity. The low relative humidity at operating temperature may prevent the formation of an electrolyte and may negate exposure to corrosion entirely. The MTF is shorter for longer ON times, if device dissipation is large. For small—power devices, the MTF is not much affected by the ON:OFF ratio (Figure 2.2). The amount of moisture absorbed increases with an increase in OFF time (Figure 2.3), but the average amount of moisture, remains the same as long as the ON:OFF ratio is the same (Figure 2.4). Higher-power dissipating devices evaporate moisture due to junction temperature rise regardless of environmental conditions (Figure 2.5) [Ajiki 1979, Macheils 1991, Shirley 1991].

Figure 2.2 MTF is shorter for longer ON times, if device power dissipation is large [Ajiki, 1979]. MTF is not much affected by ON:OFF time ratio when device power dissipation is small

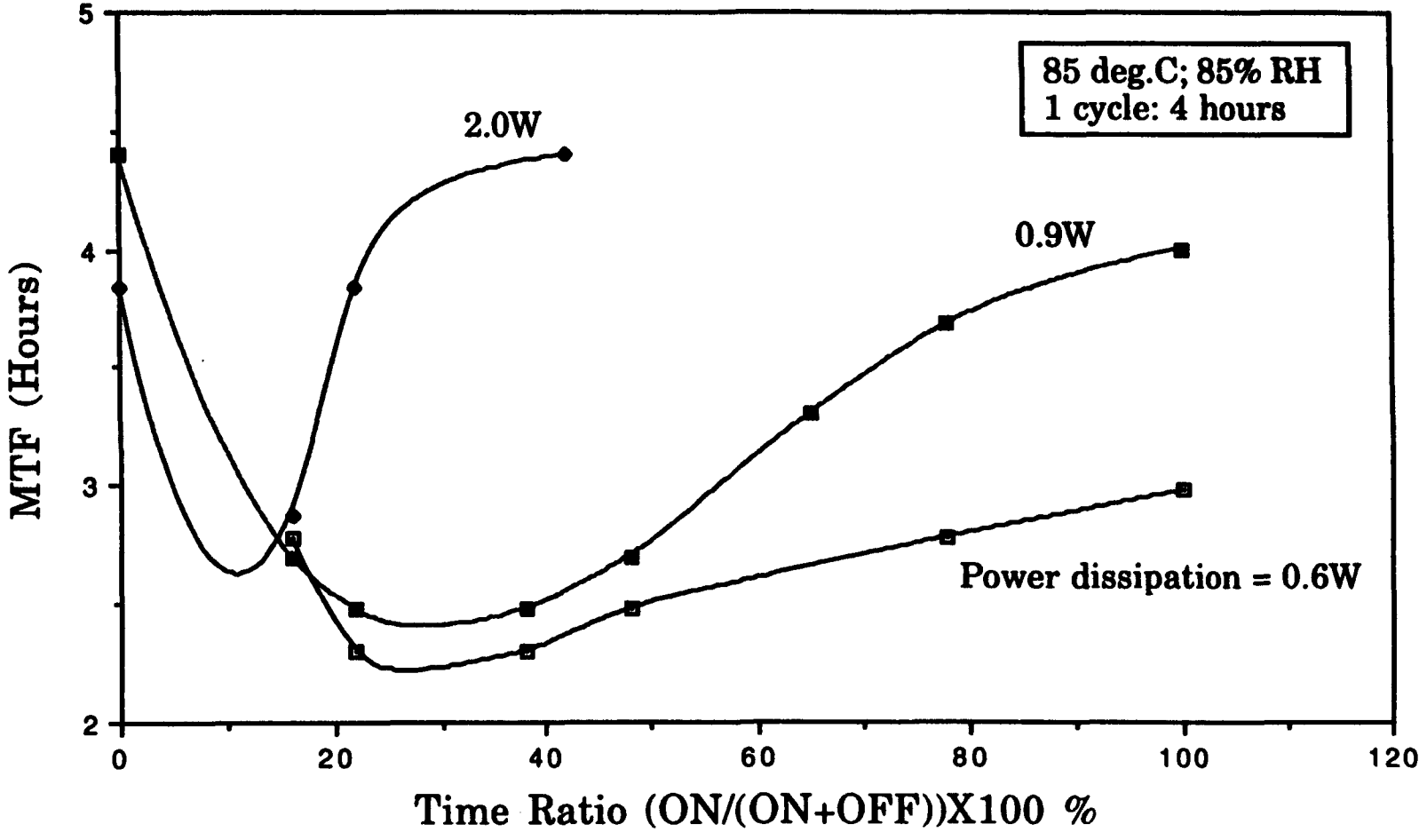


Figure 2.3 The amount of moisture absorbed increases with increase in the OFF time, i.e., the more the time spent at lower temperature, the larger is the amount of moisture absorbed [Ajiki, 1979]

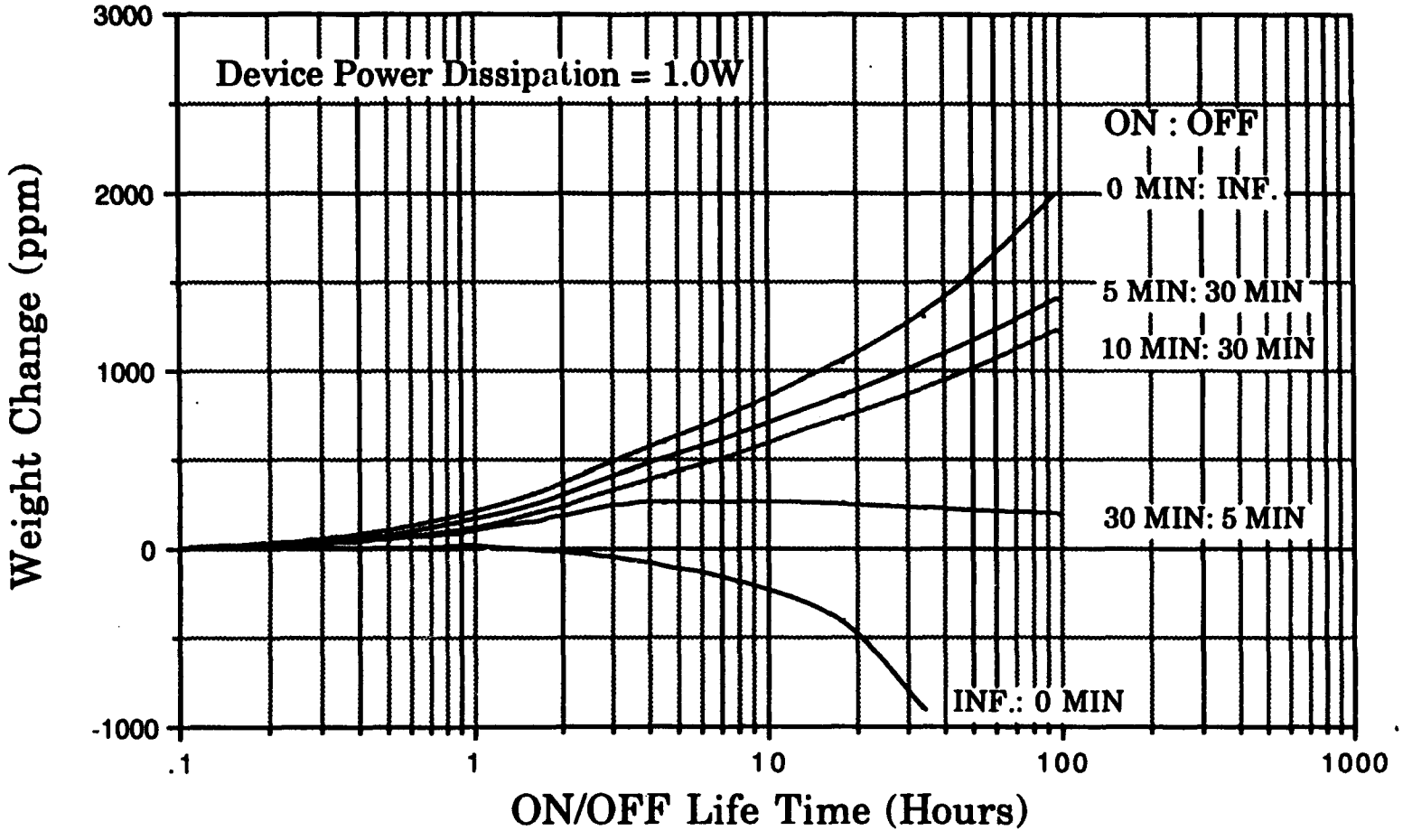


Figure 2.4 The average amount of moisture remains the same as long as ON:OFF ratio is the same [Ajiki, 1979]

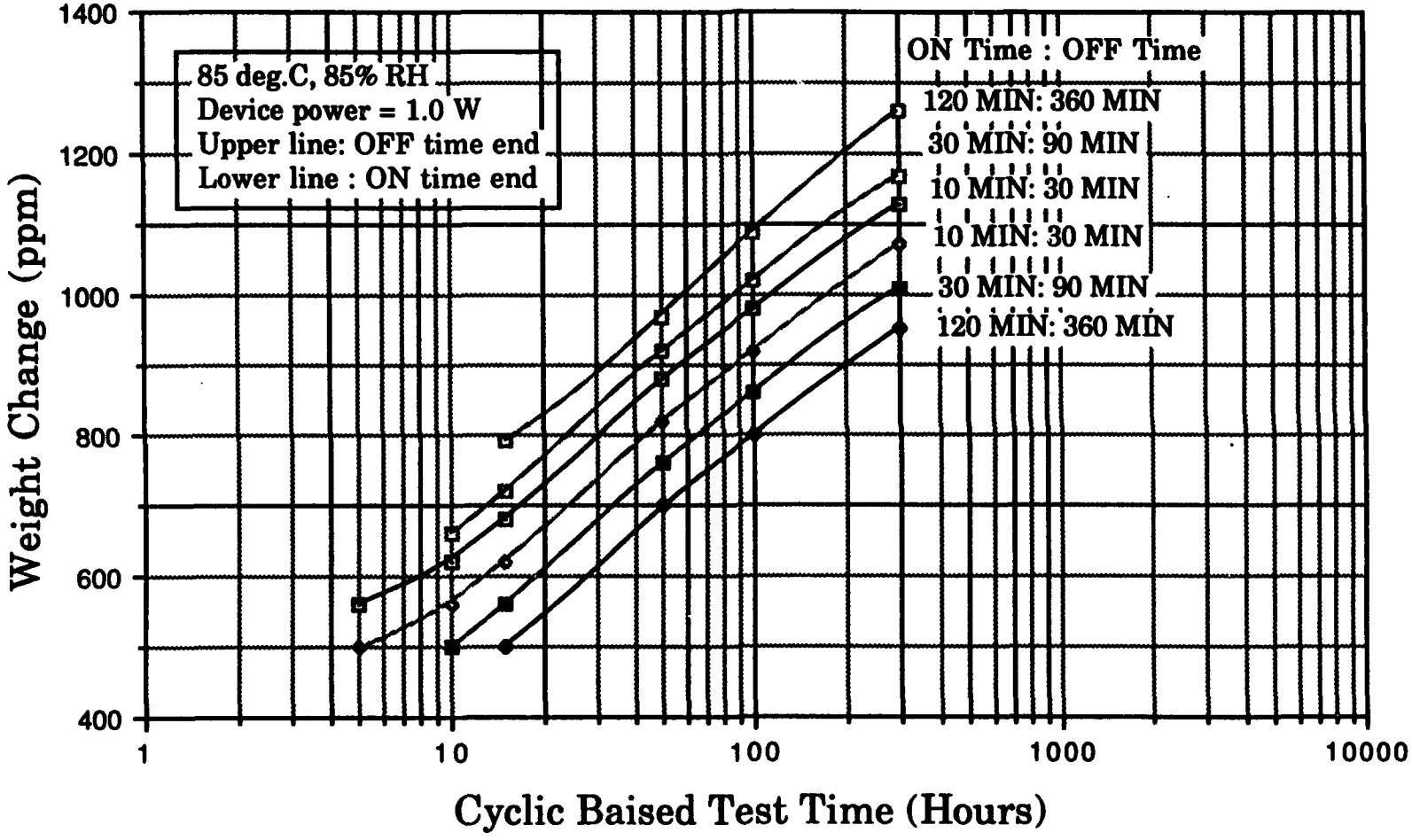
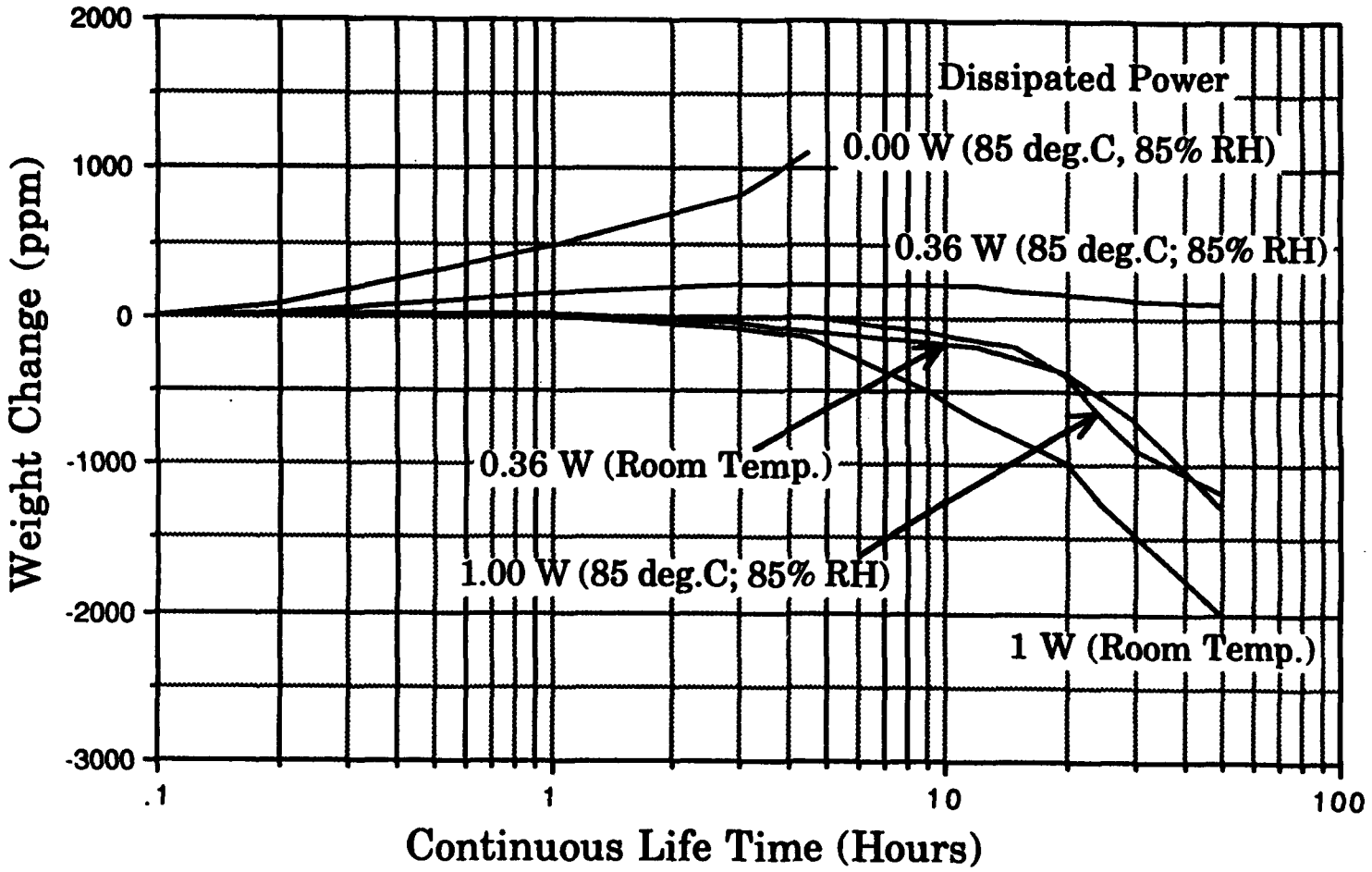


Figure 2.5 Higher power dissipating devices evaporate moisture due to junction temperature rise, irrespective of environmental conditions. [Ajiki, 1979]



The time to failure as a result of corrosion failure is given by

$$\tau_c = \left(\frac{K_1 K_2 K_3}{K_4}\right)\left[\frac{w^2 hndF\rho}{4MVZ}\right] \tag{2.1}$$

where M is the atomic weight of a metal conductor of density d, width w, height h, and chemical valence n; ρ/Z is the sheet resistance of the electrolyte; and V is the voltage applied. K_1 represents the physical and chemical properties of the metallization materials, K_2 is the coating integrity index, K_3 is the mission profile correction factor, and k_4 is the environmental stress correction factor. The effect of the environmental stress factor on the MTF is represented in Figure 2.6.

The only temperature-dependent k term is the environmental correction factor, K_4, utilized to determine the time to failure for various temperature and humidity conditions. The K_4 term is modelled as

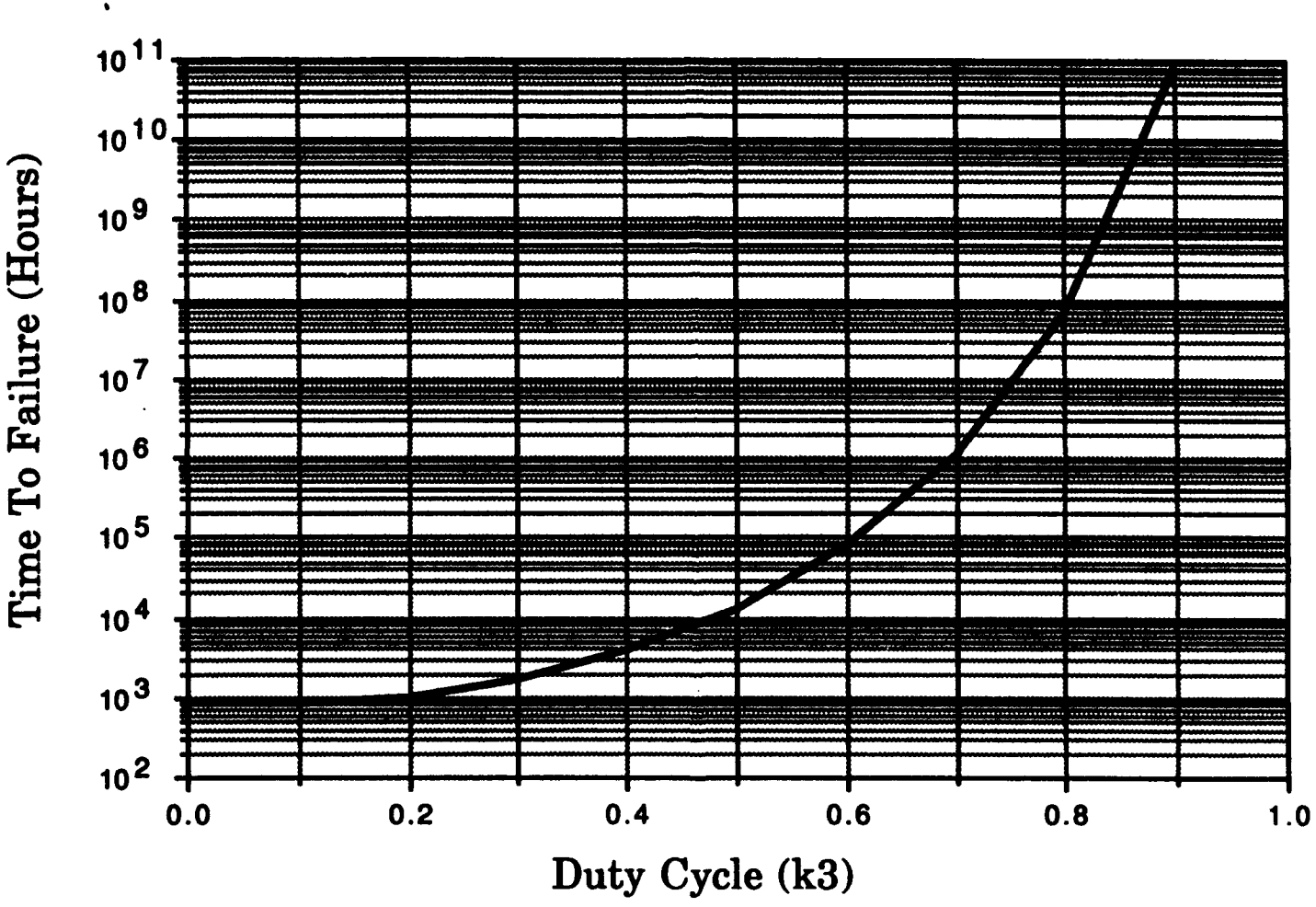
$$K_4 = \frac{(RH_R)^n \exp(E_a/KT_R)}{(RH)^n \exp(E_a/KT)} \tag{2.2}$$

where RH_R is a reference relative humidity (%), E_a is an activation energy (eV), K is the Boltzmann constant (eV/° K), n is a material constant, and T_R is a reference temperature (°K).

2.2.2 Electromigration

A major VLSI failure mode is mass transport resulting from a momentum exchange between conducting electrons and the metal atoms in the conductor. The phenomenon of electrotransport, or "electromigration," is the result of high current density (typically of the order of 10^6 amperes/cm^2 in aluminum) in metallization tracks, which produces a continuous impact on the grains in the metallization, causing the metal to pile up in the direction of the electron flow and produce voids upstream with respect to the electron flow [Schnable 1988]. The result is a net flux of metallization atoms that generally migrate in the same direction as the electron flux. Electromigration-induced damage in thin-film conductors usually appears in the form of voids and hillocks. Voids can grow and link together to cause electrical discontinuity in conductor lines, leading to open circuit failure. Hillocks can also grow and extrude materials, causing short-circuit failure between adjacent conductor lines on the same level, or in adjacent levels in multi-level interconnecting structures. Alternatively, electromigration can break through the passivation or the protective coating layers and lead to subsequent corrosion-

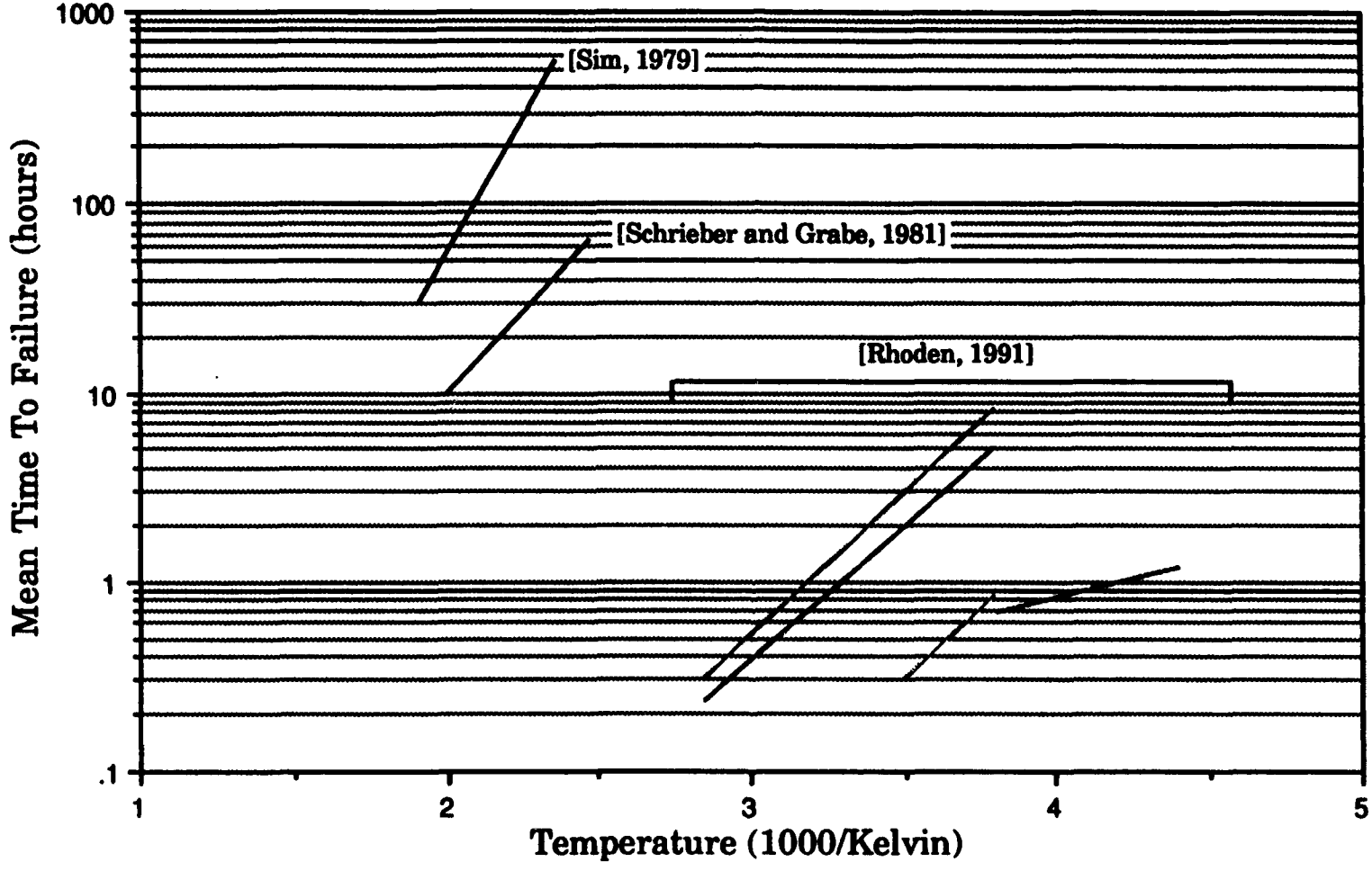
Figure 2.6 Time To Failure Due to Corrosion vs. Duty Cycle [Pecht, 1990]



induced failures. Void-induced open-circuit failures usually occur earlier than extrusion-induced short-circuit failure in thin-film conductors using Aluminum-based metallurgies.

The role of temperature in electromigration is extremely complex, especially within normal operating temperatures 125°C. The lifetime limitation due to electromigration is a complex function of temperature and cannot be represented by a simple activation energy. The temperature acceleration can, however, be represented by an apparent activation energy that changes with operating temperature (Figure 2.7). There have been insufficient tests on electromigration at temperatures less than 125°C, due to the difficulty in conducting such tests. Most tests have been performed at elevated temperatures in the neighborhood of 150°C or higher, with the results extrapolated to normal operating or room temperatures. Extrapolation of failure rates from stress results at higher temperatures to provide reliability estimates at lower temperatures will not be

Figure 2.7 Higher reliability cannot be attributed to lower temperature, since electromigration occurs with the same order of magnitude lifetimes at all temperatures



accurate, since the physics-of-failure phenomenon is not the same.

Electromigration damage forms at sites of atomic flux divergence, of which the three main sources are structural defects, microstructural inhomogeneities, and local temperature gradients. Electromigration failures tend to be localized near sites of maximum temperature gradient [Lloyd 1988, Schwarzenberger 1988], even though typical field failures are characterized by structurally induced flux divergences, rather than temperature-gradient-induced flux divergences [Shatzkes 1986].

Modelling temperature effects on electromigration. The phenomenon of electromigration-induced mass transport is attributed to atomic flux resulting from electromigration in the lattice and at grain boundaries during the passage of current through a polycrystalline thin-film conductor. Diffusivity (D), exponentially dependent on temperature, is the only temperature-dependent term in the flux equation. The contribution due to electromigration in the lattice is [Huntington 1961]

$$J_l = \frac{1}{kT} N_l D_l j \rho e Z_l^* \tag{2.3}$$

The contribution of electromigration in the grain structure is given by

$$J_b = \frac{1}{kT} \frac{N_b \delta}{d} D_b j \rho e Z_b^* \tag{2.4}$$

where N is the atomic density, D is the diffusivity, j is the current density, ρ is the resistivity, eZ^* is the effective charge, k is the Boltzmann constant, and T is the steady-state temperature [Ho 1974a]. The subscripts l and b represent lattice terms and grain boundary, respectively. The quantity δ is the effective boundary width (10 Å) for mass transport, and d is the average grain size. In aluminum, the transport is via the grain boundary, so grain boundary parameters, such as diffusivity, are important.

Electromigration damage can occur only where there is divergence in the electromigration flux, J, caused by variations in any of the parameters on the right-hand side of Equations (2.3) and (2.4). For instance, if the grain size of the metallization changes, perhaps due to a change in the substrate, the flux-carrying capacity of the track is altered and flux divergence results. Cross-section changes in themselves do not lead to flux divergences, because a reduction in the cross-sectional area leads to a higher current density in the remaining section. However, a section change can cause a change in local self-heating and consequently, a

temperature-induced divergence.

Temperature changes in the stripe are important sources of flux divergence, because the flux depends exponentially on temperature [Schwarzenberger 1988]. Temperature changes may arise from changes in the thermal properties of the substrate as the metallization passes over other features on the substrate, or by changes in self-heating caused by section changes for instance, at steps over substrate features. Temperature changes can also lead to thermomigration (transport of material in a temperature gradient), though the magnitude of thermomigration is small compared to electromigration [Schwarzenberger 1988].

At moderate temperatures (much lower than $0.5T_m$, where T_m is the melting temperature of the materials), the atomic flux from electromigration in the lattice is minute compared with that from the grain boundaries, so grain boundary electromigration becomes the dominant mode of mass transport for temperatures much lower than $0.5T_m$ [Ho 1989[b]]. The mass transport in the grain boundaries in most metals occurs by vacancy diffusion [Kwok 1981]. The relative contributions of the atomic flux due to lattice diffusion and grain boundary diffusion can be estimated from the ratio of J_l and J_b, given by [Ho 1989[b]]

$$\frac{J_l}{J_b} = \frac{N_l}{N_b}\frac{d}{\delta}\frac{D_l}{D_b}\frac{Z_l^*}{Z_b^*} \tag{2.5}$$

The subscripts l and b denote the electromigration parameters of the lattice and grain boundary, respectively. The measured values of Z_l^* and Z_b^* usually do not differ by more than one order of magnitude. For thin films with $1\mu m$ grain size at $0.5T_m$, where T_m is the melting temperature of the materials [Ho 1989[b]],

$$\frac{N_l}{N_b} \approx 1 \qquad \frac{d}{\delta} \approx 10^3 \qquad \frac{D_l}{D_b} \approx 10^{-7} \qquad \frac{J_l}{J_b} \approx 10^{-4} \tag{2.6}$$

Attardo, while conducting experiments on 0.4-0.6 - mil wide and 10-12 mil long Aluminum films on silicon wafers with 800 Angstroms of thermally grown silicon dioxide and 2,000 Angstroms of sputtered quartz, found that mass transport during electromigration shifted from grain-boundary diffusion to lattice at threshold temperatures higher than $0.5T_m$ [1970]. The rate of electromigration was determined by the film's degree of preferred orientation.

Diffusion rates are highly anisotropic. The diffusion parallel to dislocations constituting tilt boundaries proceeds at several orders of magnitude greater than the diffusion perpendicular to the dislocation. The vacancy flux in the grain boundary, with contributions from electromigration and diffusion via grain

boundary are given by

$$J_v = -D_v \nabla C_v + J_b \tag{2.7}$$

where D_v is the vacancy diffusivity in the grain boundary [Ho 1989[b]]. The local variation of the vacancy concentration is given by the equation

$$\frac{dC_v}{dt} = -\nabla J_v + \frac{C_v - C_v^*}{\tau} \tag{2.8}$$

where the last term expresses the local deviation of the vacancy concentration from thermal equilibrium [Ho 1989[b]]. The quantity τ is the average lifetime of the vacancy, determined by the efficiency of the source and the sinks in creating and annihilating vacancies. Under a steady-state condition, $dC_v/dt=0$,

$$C_v - C_v^* = \tau \nabla J_v \tag{2.9}$$

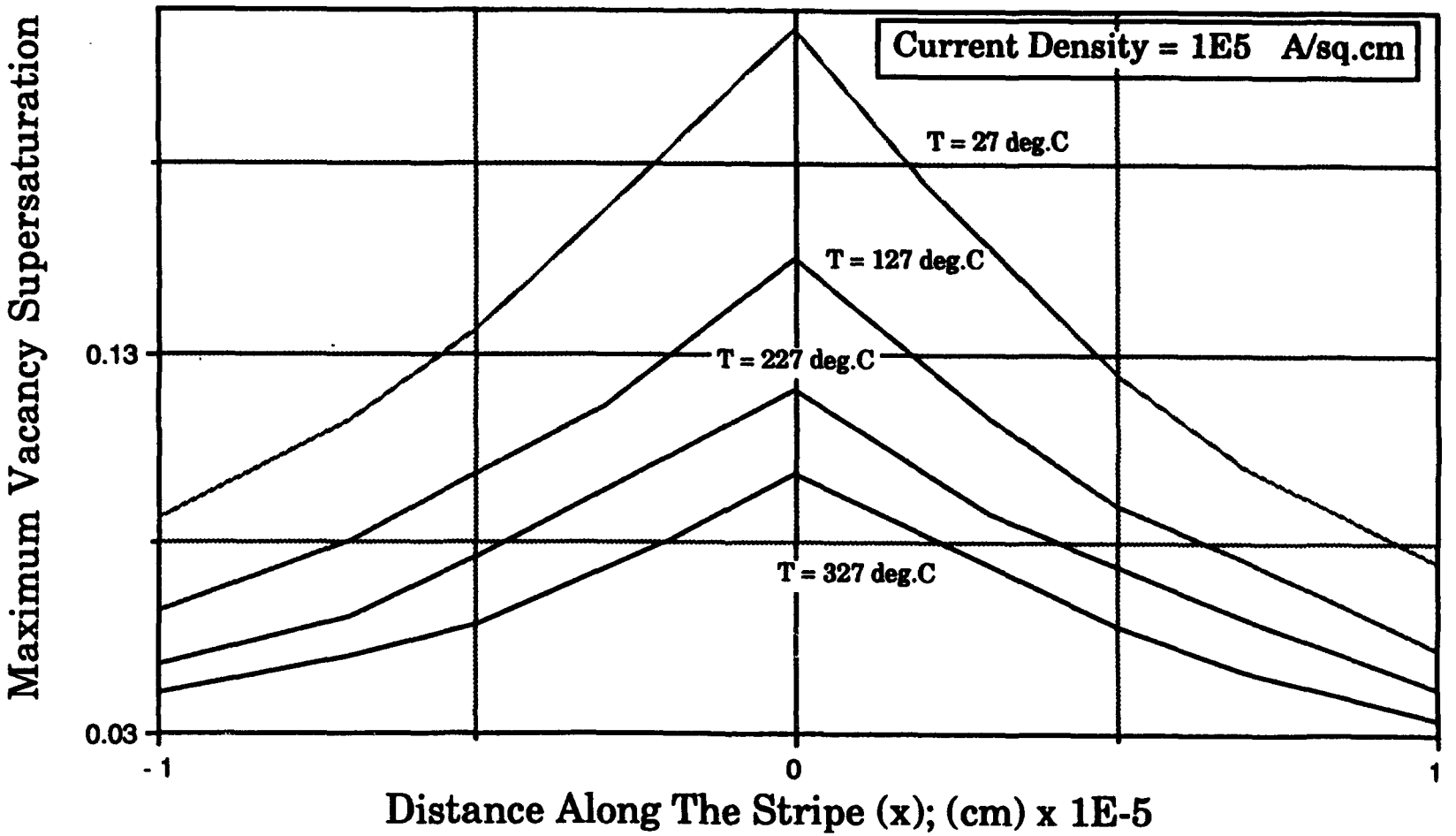
The vacancy flux is represented as

$$\frac{dC_v}{dt} = D\left(\frac{d^2C_v}{dx^2} - \frac{dC_v}{dx}\frac{Z^*eE}{kT}\right) - \left(\frac{D}{kT}\frac{dC_v}{dx} - \frac{DC_vZ^*eE}{(kT)^2}\right) \left(\frac{\Delta H_b}{T}\left(\frac{dT}{dx}\right) + \frac{d(\Delta H_b)}{dx}\right) + \frac{C_v - C_v^*}{\tau_e} \tag{2.10}$$

where ΔH_b is the activation energy for the grain boundary diffusion [Attardo 1970]. The solution of this equation provides the rate of vacancy buildup at the point of divergence and the maximum vacancy concentration that can be achieved during steady-state electromigration. It is evident from Equation (2.10) that the damage from vacancy supersaturation can arise from any number of discontinuities other than temperature, such as structural variations between boundaries or between regions of the stripe with different structures [Attardo 1970]. The actual process of hole formation is a void growth process, and the time required for vacancy buildup to maximum supersaturation is orders of magnitude less than that needed for observation of holes. Rosenberg and Ohring calculated the vacancy supersaturations by considering the case of two boundaries of differing diffusion characteristics located in the isothermal region $dT/dx=0$ and joining at $x=0$, which is the accumulation site [1971]. The steady-state solution is represented in Figure 2.8, which demonstrates the effects of temperature on vacancy supersaturation. Assuming a product, for aluminum D_eZ^* to be $3 \pm 0.5 \times 10^{-2}$ cm^2/sec, for current density of 1×10^6 A/cm^2, Rosenberg and Ohring found the maximum

vacancy supersaturation to decreased from 27°C to 327°C [1971]. Once the maximum supersaturation is reached, the driving force for vacancy diffusion due to concentration gradient is lost. Rosenberg and Ohring observed

Figure 2.8 Temperature Dependence of Vacancy Supersaturation Distribution [Rosenberg and Ohring, 1970]



that, under current densities of 1 x 10^6 A/cm^2 and steady state temperature of 127°C, the maximum supersaturation was between 0.1 and 1.

Generally, electromigration has a linear dependence on temperature gradient, an exponential dependence on temperature for temperatures greater than 150°C, and a dependence on current density whose order varies from 2 to 14. The combinations of current density and temperature, which will produce electromigration damage in titanium-platinum-gold metallizations, have been characterized in Figure 2.9. The characteristics have been derived for not more than 0.14% cumulative failures (an average of eight failures/10^9 stripe hours) after twenty years, which is the three-sigma limit of the lifetime distribution. In figure 2.9, the lifetimes are assumed to have a fourth dependence on the current density [English 1974].

In an ideal case of a structurally uniform conductor with no temperature gradient, there is no flux divergence, so that electromigration damage will not occur [Ho 1974[a], Ho 1989[b]]. The extent of deviation of vacancy concentration from equilibrium is proportional to the vacancy flux divergence. Whenever there is spatial variation in any of the parameters affecting the grain boundary electromigration, which may include structural defects in the form of non-uniform thickness of the conductor or temperature gradient, a divergence in the atomic flux occurs, giving rise to a local vacancy supersaturation or depletion (void formation).

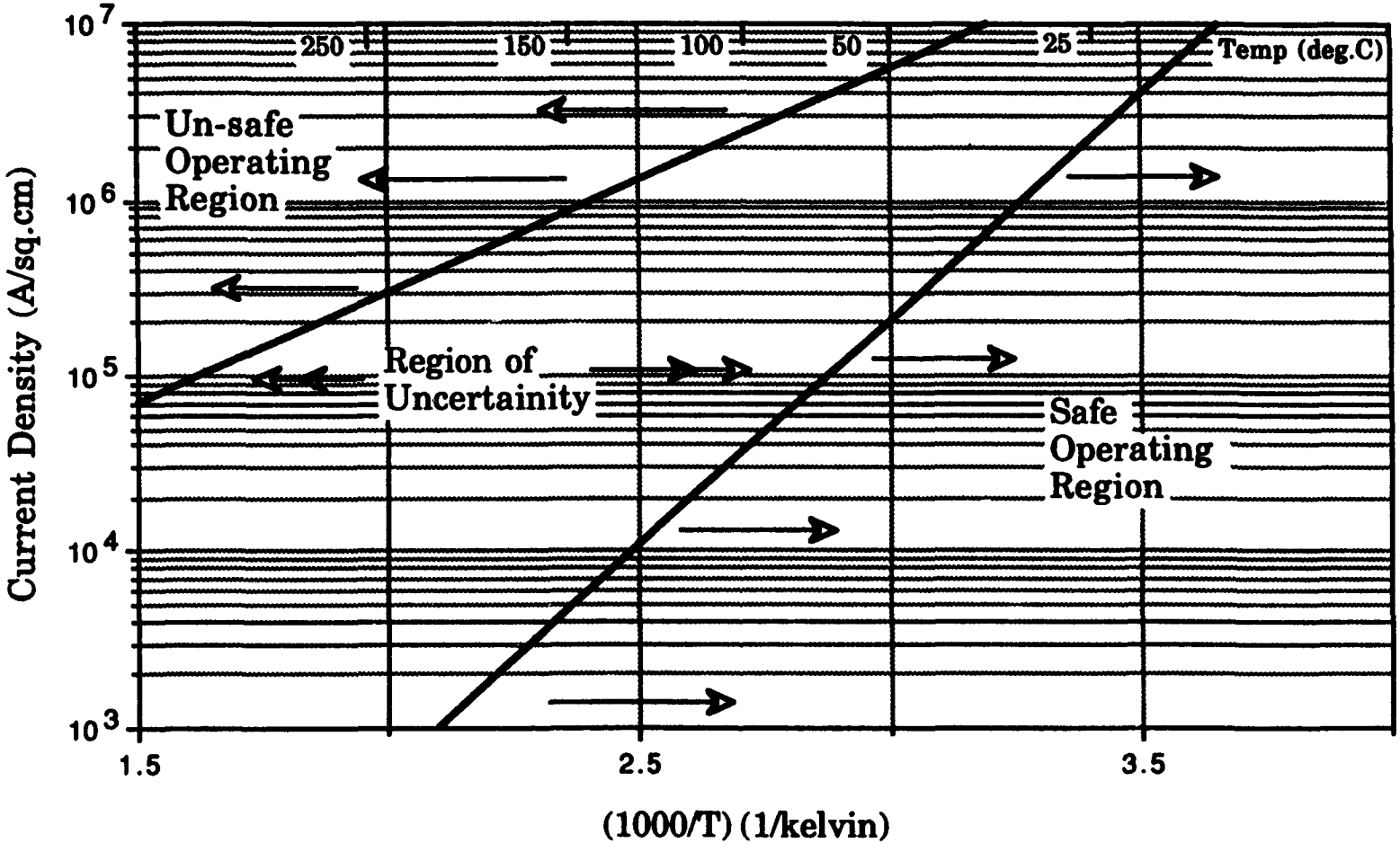
Temperature Dependence of Electromigration in Thin-film Vonductors.

Steady-State Temperature Effects in the Presence of Cracks: The effect of cracks in the conductor metallization perpendicular to current flow direction as correlated with temperature, has been predicted by Sigsbee [1973]. Grain-boundary electromigration, internal heat generation, and current crowding at growing voids dominate the rate processes that lead to failure. Assuming that the bottom interface below the substrate is held at a constant temperature, T_e, and that the conductor experiences a temperature rise ΔT_0, above T_e due to joule heating, for a crack perpendicular to the current direction, the current crowding is approximated by

$$J_e(X) = \frac{J_{eo}}{\left(1-\frac{X}{W}\right)} \qquad (2.11)$$

Joule heating of the stripe causes an initial temperature rise, resulting in instability in the stripe, causing the vacancies in the stripe to migrate along grain boundaries

Figure 2.9 Combinations of current density and temperature which will produce electromigration damage in Ti-Pt-Au metallization. [English, 1974]



and precipitate on a suitable boundary, forming elongated voids. The crack grows long by the accumulation of vacancies flowing along nearby grain boundaries. The atomic flux of vacancies in the crack is represented as

$$J_v = J_{vo}\left(\frac{1}{1-L}\right)\left(1-\frac{\Delta H \Delta T_o[\ln(1-L)+L]}{kT^2 L}\right) \tag{2.12}$$

where $L = l/W$, l is the crack length, W is the conductor width, T_e is the bottom interface temperature, and ΔT_0 is the temperature rise due to joule heating in the metallization. J_{vo} is evaluated at initial film temperature ($T_e + \Delta T_o$). The second term in brackets is due to current crowding; the third term in brackets is due to self-heating. Assuming that only the grain-boundary migration contributed to crack growth, the lifetime is calculated as

$$\tau_f = \frac{cWkT}{\delta N_a q^* \rho J_e D_o \exp\left(-\Delta \frac{h}{kT}\right)} 2\left(1+\left(\frac{0.2\Delta H}{kT^2}\right)\Delta T_o\right) \tag{2.13}$$

where c is the crack width, W is the line width, k is the Boltzmann constant, T is the steady-state temperature, δ is the effective grain-boundary width for transport, N_a is the atomic density, q^* is the effective charge, ρ is the resistivity, J_e is the current density at the crack tip region, D_o is the diffusion coefficient, ΔH is the activation energy, and ΔT_o is the initial temperature rise due to joule heating. This model neglects the effects due to the coefficient of resistance and the temperature sensitivity of q^*; Sigsbee showed that these factors had negligible effect on the life prediction estimate. The lifetimes were found to have a J_e^{-n} dependence, with n varying from unity at low ΔT_o levels to 15 for high ΔT_o. The model has been shown to model grain-boundary electromigration for temperatures in the neighborhood of 260°C [Sigsbee 1973]. The above grain boundary grooving mechanism is typically noticed in silver metallizations [Venables and Lye 1972].

Steady-State Temperature Effects in the Presence of Voids: The atomic flux is dependent on temperature; therefore, local temperature gradients will cause a divergence in atomic flux. The depletion of mass occurs wherever the electron flow is in the direction of increasing temperature. Conversely, the accumulation of mass occurs wherever the electron flow is in the direction of decreasing temperature [Venables and Lye 1972]. Metallized stripes in good thermal contact

with their substrates have negligible temperature gradients [Venables and Lye 1972]. Electromigration in thin-metallized films is confined mainly to grain boundaries [Blech 1967, Agarwala 1970, Rosenberg 1968]. Thus, the steady-state temperature dependence of electromigration is of the same magnitude as that of grain-boundary diffusion [Blech 1967, Rosenberg 1968].

Voids form as a consequence of flux divergences at non-symmetrical nodes, and grow with time, eventually coalescing to form a gap across the conductor. The effect is particularly severe in films with a small grain size, because a large number of nodes are available to act as nuclei for void formation. On the other extreme, if the grain size is comparable to stripe width, the probability that a single grain will cover the entire stripe increases, which introduces an additional source of flux divergence acting as a barrier to atoms migrating from the negative side, and preventing the replacement of atoms transported away from connecting boundaries on the other side of the grain [Attardo 1970, Blair 1970].

The flow of current through stripes creates voids at grain-boundary nodes that are suitably oriented relative to the current flow direction and longitudinal temperature gradient. The resulting porosity increases as a function of the density of the grain-boundary nodes, current density, resistivity, and mobility of metal ions along grain boundaries, and is represented by

$$\frac{dp}{dt} = Cnj\rho\mu \tag{2.14}$$

where C is a constant of proportionality, p is the porosity, n is the grain-boundary node density, j is the current density, ρ is the resistivity, and μ is the mobility of metal ions along grain boundaries. Pore formation reduces the cross-sectional area of the metal stripe available for carrying the current, thereby increasing the local current density within the remaining section [Venables 1972].

$$j = \frac{j_o}{(1-p)} \tag{2.15}$$

where j_o is the initial current density in the pore-free stripe. The increased current density causes an increase in the current - enhanced motion of the metal atoms in the stripe, at the same time increasing the joule heating within the remaining conducting portions of the stripe. The local temperature in the stripe increases above the ambient temperature, T_o, by an amount that is proportional to joule heating, given by [Venables 1972]

$$\Delta T = T - T_o = \frac{j^2 \rho}{h} \tag{2.16}$$

The temperature rise leads to a corresponding increase in mobility, μ, of the metal atoms along grain boundaries [Venables 1972].

$$\mu = \frac{D}{kT} = \left(\frac{D_o}{kT}\right) e^{-Q/kT} \tag{2.17}$$

where D is the diffusion coefficient for motion along grain boundaries, and Q is the activation energy for this process. The increase in temperature leads to a change in the resistivity, ρ, of the metal [Venables 1972]:

$$\rho = \rho_o(1 + \alpha(T - T_o)) \tag{2.18}$$

where α is the temperature coefficient of resistance. At a constant total current, the increase in resistivity causes an additional increase in the local rate of joule heating and in the effective electric field ($j\rho$) experienced by the atoms. Electromigration failure occurs where the grain-boundary migration and temperature gradient combine to create suitable conditions for porosity to develop until it exceeds the critical value, resulting in the melting of the stripe. Venables and Lye [1972] combined the above equations to give the time to failure as

$$T_F = \frac{1}{2Cn}\left(\frac{\tau_o k T_o}{j_o \rho_o D_o e^{-Q/kT}}\right) \int_{x_o}^{x_1} \frac{e^{-Qx/kT_o}}{x^2(1 - x + x\alpha T_o)} dx \tag{2.19}$$

where

$$\tau_o = \frac{\Delta T_o}{T_o} = \frac{j_o \rho_o}{h T_o} \tag{2.20}$$

and

$$x = \frac{\tau_o}{(1-p)^2+\tau_o(1-\alpha T_o)} = 1 - \left(\frac{T_o}{T}\right) \tag{2.21}$$

$$x_o = \frac{\tau_o}{1-\tau_o(\alpha T_o - 1)} \qquad @t=0$$

$$x_1 = 1-\left(\frac{T_o}{T_m}\right) \qquad @t=T_F \tag{2.22}$$

where T_m is the melting temperature of the metal. They showed that time to failure versus current density varied complexly, and that a simple power-law dependence (as shown by Black) was inadequate to describe the experimental conditions over more than a small range of current densities. The results of Attardo [1970], Black [1968], and Blair [1970] were tangential to the results from the Venables and Lye model at a temperature of 210°C and current densities ranging from 1 x 10^4 A/cm^2 to 2 x 10^6 A/cm^2 (Figure 2.10). Venables and Lye [1972] showed that when the temperature dependence of times to failure due to electromigration was represented as an Arrhenius plot, although the curves appeared as accurate straight lines, the slopes yielded only apparent activation energy, which varied with test conditions, indicating that the time to failure was a complex function of baseline temperature and could not be represented by an Arrhenius plot to give an activation energy (Figures 2.11 and 2.12).

Steady-State Temperature Effects Without Assumption Defect Magnitudes: A general, but not universal, expression for the mean time to failure MTF(or t_{50}, which is the time to reach failure of 50% of a group of identical conductor lines) is given in Equation (2.23). This is not a failure-rate expression, as the failure times are typically observed to follow a lognormal distribution:

$$MTF = A\, j^{-n}\, e^{E/kT} \tag{2.23}$$

where A is a parameter depending on sample geometry, physical characteristics of the film and substrate, and protection coating; j is the current density (A/cm^2);

Figure 2.10 Mean Time to failure varies with current density in complex manner. Simple power laws can represent experimental observations over a small range of current densities [Venables and Lye, 1972]

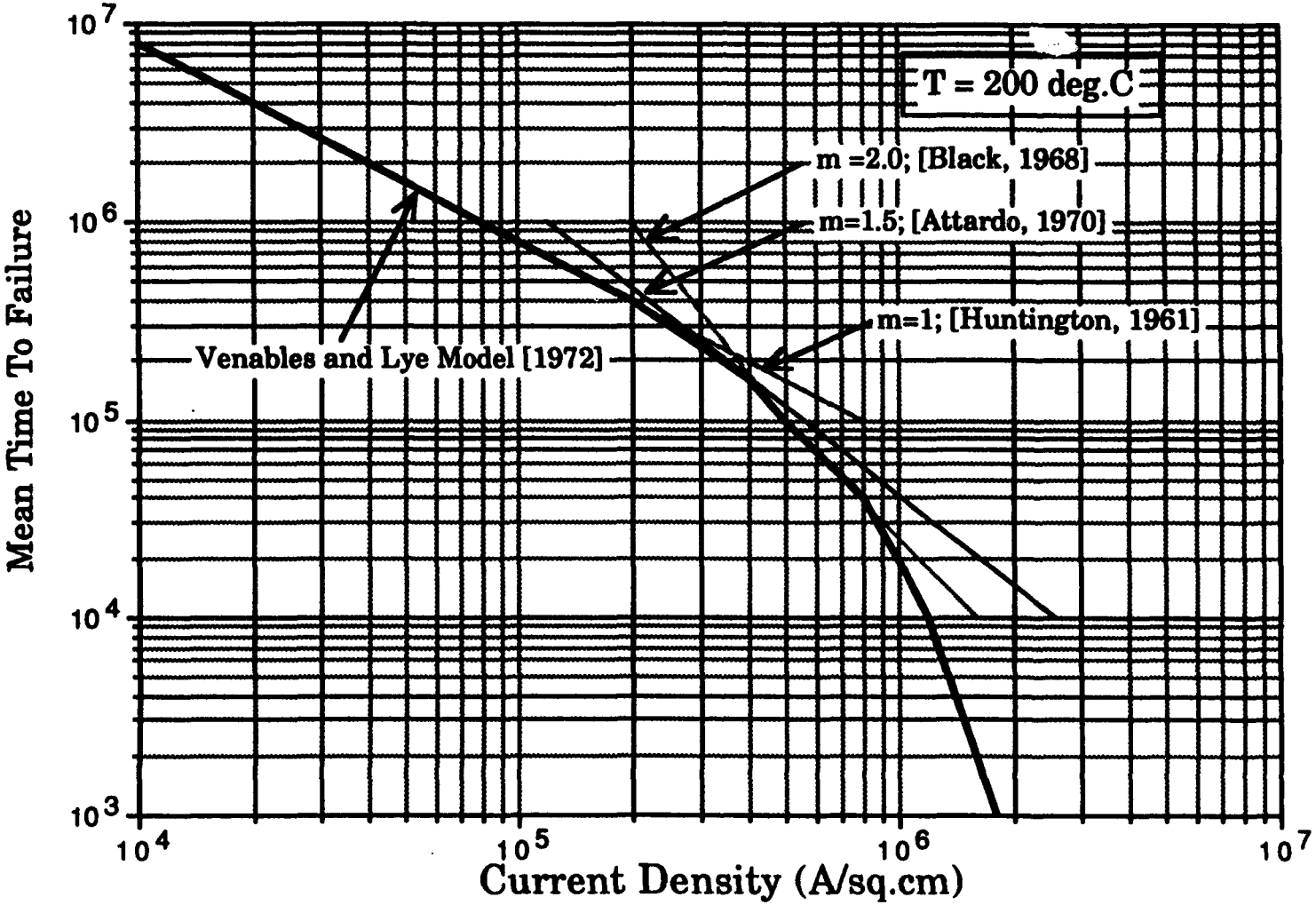


Figure 2.11 Temperature dependence has been represented by an apparent activation energy which changes with test conditions [Venables and Lye, 1972]

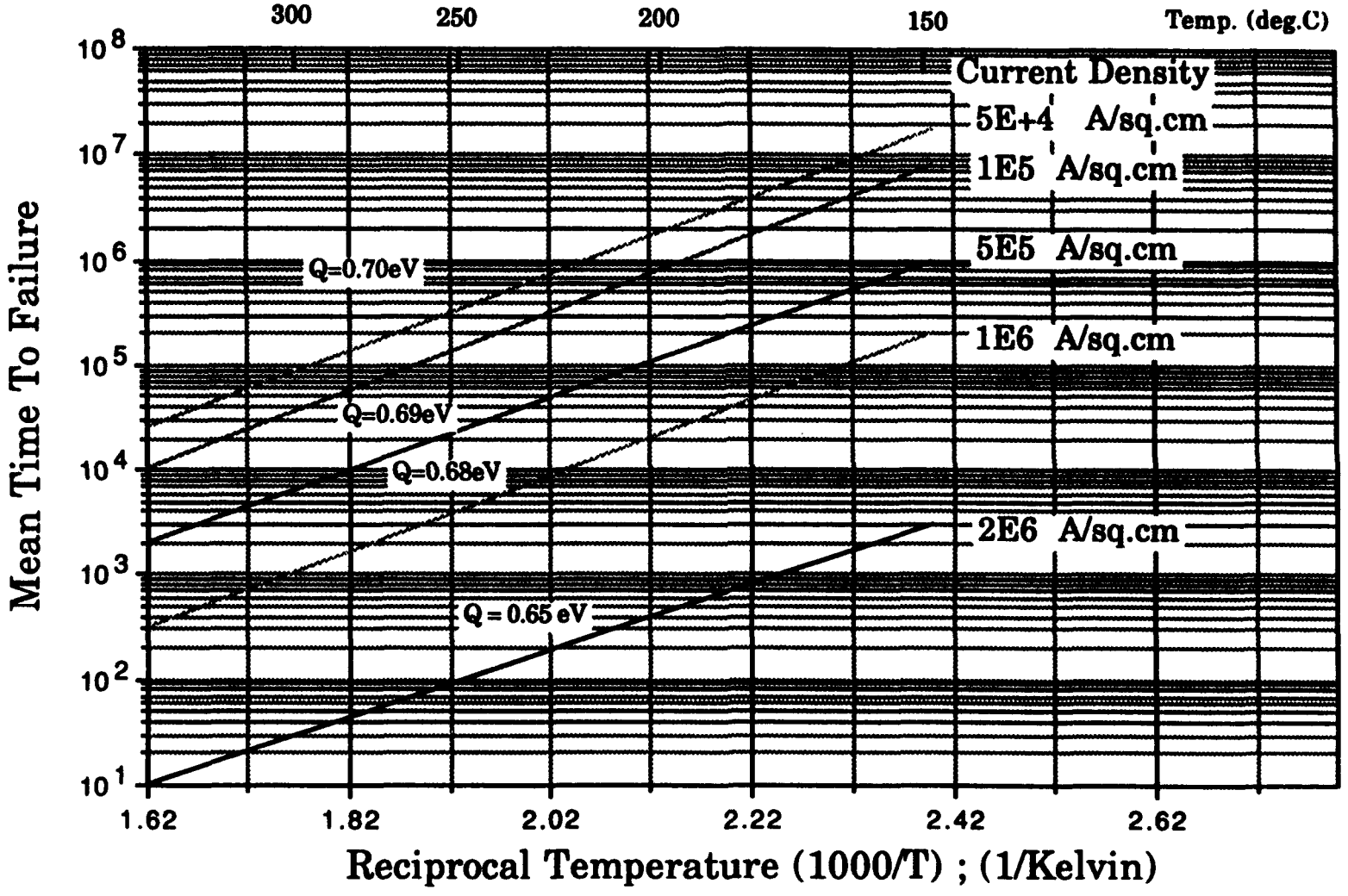
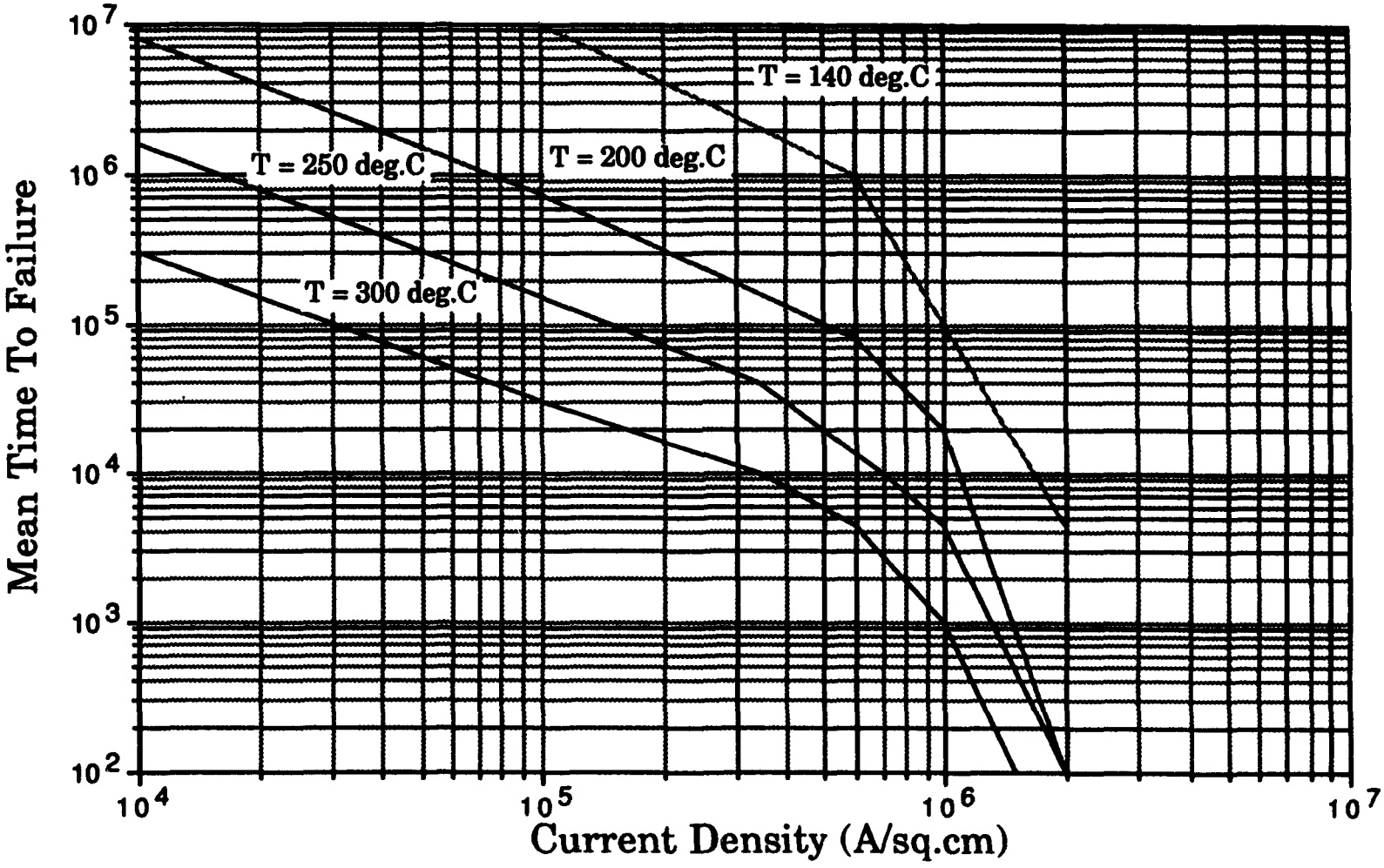


Figure 2.12 Influence of Baseline Temperature on Mean Time to Failure [Venables and Lye, 1972]



and n is an experimentally determined exponent. This model is applicable only to conductor films that are wider than the average grain size of the aluminum film from which they are constructed. As the conductor width is reduced and approaches or becomes less than the average grain size, the structure begins to "bamboo," that is, most of the grain boundaries become normal to the electron flow. Black's relationship does not apply when bambooing starts to occur [Black 1982].

The electromigration lifetime test is carried out under a set of accelerated test conditions at elevated temperatures and with-high-current-density stressing. The data are then extrapolated to device operating conditions, with current-density stressing below 5×10^5 A/cm^2, using the Arrhenius-like empirical equation cited above (originally formulated by Black [1969a,b]). Values of n that have been reported are

n = 1 to 3	Chabra and Ainslie [1967]
n = 1.5	Attardo [1972]
n = 1.7	Danso and Tullos [1981]
n = 2	Black [1983]
n = 6 to 7	Blair et al. [1970]

Black characterized his data in the range $0.5 \times 10^6 < j_o < 2.8 \times 10^6$, with an exponent of $n=2$. Attardo reported $n=1.5$ on the range $10^5 < j_o < 10^6$ A/cm^2. Blair reported a value of $n=4$-5 in the range of $10^6 < j_o < 2 \times 10^6$ A/cm^2. Venables found that the simple power-law dependence of time to failure on current density could be used to describe experimental observations in a small range of current densities [Venables 1972].

Lloyd [Shatzkes 1986] treated electromigration failures by superimposing Fickian diffusion and mass transport due to electromigration force, and derived a modification of Black's equation:

$$t_f = \left(\frac{2C_f}{D_o}\right)\left(\frac{k}{Z^* e \rho}\right)^2 T^2 j^{-2} e^{\Delta H/kT} \qquad (2.24)$$

where C_f is the critical value of vacancy concentration at which failure occurs, D_o is the pre-exponential factor for grain-boundary self-diffusivity, k is the Boltzmann constant, Z^* is the effective charge, e is the electronic charge, ρ is the resistivity, T is the steady-state temperature, j is the current density, and ΔH is the activation energy. Equation (2.24) differs from Black's equation in that it has

a T^2 pre-exponential term, but it fits Black's data equally well.

Table 2.1 shows the estimated MTF of titanium:wolfram/aluminum (Ti:W/Al) and titanium: wolfram/aluminum + Copper (Ti: W/Al + Cu) film conductors at 85°C for 5×10^5 and 2×10^5 A/cm^2 current densities at 100% duty cycle. Even for the worst case $n = 1$, it has been anticipated that the actual time to failure will be greater than those predicted in Table 2.1 [Ghate 1981]. For current densities of 2×10^5 A/cm^2, temperatures of 125°C will not lead to failure in less than ten years with a typical exponent of $n = 1.7$.

Few studies at lower temperatures have been performed on unpassivated stripes, but these have shown that the phenomenon of electromigration shifts from grain-boundary migration to surface migration, with detachment of the stripe from the chip, at temperatures in the neighborhood of 223K to 347K [Rhoden 1991].

In order to improve the resistance of the conductor to surface electromigration, passivations consisting of glass overlays, metallic coatings, or natural oxides are used to cover the thin-film conductor. Typically, the electromigration lifetime of most conductors increases by one order of magnitude or more with complete surface coverage [Lloyd 1983, Felton 1985, Yeu 1985]. The use of transition layers such as titanium nitride (TiN) [Grabe 1983], chromium (Cr) [Levine 1984], and titanium-wolfram (Ti-W) [Fried 1982], has been reported to improve the lifetime of thin-film conductors by one order of magnitude. The transition layer provides a redundant structure, allowing void healing, and also acts as a metal diffusion-layer.

Temperature Gradient Dependence of Electromigration Lifetimes: Temperature gradients exist both globally and locally in thin-film conductors, due to heat generation from joule heating and power dissipation from active devices on the chip. The global temperature gradient is small, except near electrodes or contact pads. Large local temperature gradients or hot spots can be caused by poor adhesion or contaminations at the interface between the metal film and the substrate, or by the variations in thickness of the metal film.

Temperature gradients are important sources of atomic flux divergence, since the flux depends exponentially on temperature. For example, at 200°C in aluminum, a 5°C change in temperature results in a change of more than 10% in the electromigration flux [Schwarzenberger 1988]. Studies on electromigration damage due to temperature gradients have revealed that void formation occurs in regions where the electron flow is in the direction of increasing temperature, and hillocks form in locations where the electron flow is in the direction of decreasing temperature [Blech 1967]. Temperature gradients can also lead to thermomigration, although migration due to thermomigration, compared to

electromigration, is small for aluminum tracks in ICs.

Table 2.1 Estimated MTF Values for Electromigration at 85°C, as a Function of the Exponent Used in Black's Equation

Current Density	Exponent	Ti: W/Al (years)	Ti: W/Al + Cu (years)
5×10^5 A/cm^2	n = 1.0	4	12
	n = 1.5	5	17
	n = 2.0	8	24
2×10^5 A/cm^2	n = 1.0	10	30
	n = 1.5	23	68
	n = 2.0	50	152

The temperature gradient dependence of electromigration failures has been confirmed by Lloyd [1988] and Schwarzenberger [1988]. Lloyd noticed that the electromigration failure location was typically near the location of the maximum temperature gradient, whereas the location of non-temperature-gradient-induced failure was randomly distributed for chromium/aluminum-copper (Cr/Al-Cu) conductors covered with polyimide passivation. He modeled the temperature of the stripe carrying current to produce significant joule heating as the balance between the heat generated in the stripe and the heat conducted away from the stripe to the surrounding thermal sinks, such as substrate, passivation, and the non-conducting portion of the metal stripe. The heat balance relation is given by

$$\rho j^2 = K\left(\frac{d^2\Delta T}{dx^2}\right) - h\Delta T \tag{2.25}$$

per unit volume, where ρ is the metal resistivity, K is the metal's thermal conductivity, h is the parameter characterizing the thermal efficiency of the heat sinks, and ΔT is the temperature rise due to joule heating [Lloyd 1988]. The term on the left of Equation (2.25) is the heat generated due to current passing through the metal element; the first term on the right is the heat conduction along the metal stripe away from the heating element; and the last term is the heat conduction to the environment. If the heat conduction through the oxide (of thickness l_{oxide}) is considered alone, the value of h is of the order

$$h = \left(\frac{K_{oxide} K}{l_{oxide} l} \right) \tag{2.26}$$

where K_{oxide} is the thermal conductivity and l is the stripe thickness [Lloyd 1988]. The heat sink is assumed to be at the ambient temperature. The solution to the heat conduction equation for a stripe with the origin in the center was given by Lloyd [1988] as

$$T = A\left(1 - \left(\frac{Cosh(Bx)}{Cosh(\frac{BL}{2})}\right)\right) \tag{2.27}$$

where

$$B = \sqrt{\left(h - \frac{\rho_o \alpha j^2}{K}\right)} \tag{2.28}$$

$$\rho = \rho_o (1 + \alpha \Delta T) \tag{2.29}$$

$$A = \frac{\rho_o j^2}{B^2 K} \tag{2.30}$$

The location of failure was argued to be near the position of maximum flux divergence. The atomic flux is

$$J = \frac{DF}{kT} \tag{2.31}$$

where D is the diffusivity; F is the driving force for diffusion; the point of maximum flux divergence is

$$\frac{dJ}{dx} = \frac{dC}{dt} = \left(\frac{dJ}{dT}\right)\left(\frac{dT}{dx}\right) \tag{2.32}$$

and the condition of failure is when

$$\frac{d^2J}{dx^2} = \frac{d}{dx}\left(\frac{dJ}{dT}\right)\left(\frac{dT}{dx}\right) = 0 \tag{2.33}$$

The location of electromigration failure calculated from Equation (2.33) is near the location of maximum temperature gradient [Lloyd 1988]. The points of maximum flux divergence move from the edges, for higher current densities, to the middle for lower current densities. The change in the failure location was due to an exponential dependence of flux divergence on temperature, with only linear dependence on temperature gradient.

Figures 2.13 and 2.14 show the variation in the location of failure sites versus distance along the stripe, for low and high current densities. At high current densities ($> 10^6$ A/cm^2) accompanied by high joule heating, the highest flux divergence is very close to the location of highest temperature gradient, which is near the edge. The failure site is thus closer to the site of maximum temperature gradient. At lower current densities ($< 10^6$ A/cm^2), the failure location is more randomly distributed, since the effect of temperature gradient becomes small compared with other flux divergences induced by structural discontinuities.

The variation of flux between different regions of the conductor may lead to failure due to depletion in some regions. The time to failure is inversely proportional to the flux gradient within that region. The flux gradient, in terms of the temperature gradient, is given as

$$\frac{dU}{dX} = \frac{N\epsilon I D_*}{k} e^{-E/kT} f(\rho, Z, T) \frac{dT}{dX} \tag{2.34}$$

where N is the density of the ions, ϵ is the electronic charge, ρ is the resistivity, Z is the effective ionic valency and represents the net effect of momentum exchange and electric field forces, $D_* \exp(-E/kT) = D$ is the diffusion coefficient for ions in the conductor, k is the Boltzmann constant, T is the average steady-state conductor temperature, and E is the activation energy. Schwarzenberger et al. demonstrated the importance of temperature gradient as a source of electromigration flux divergence in metallization tracks and, therefore, the necessity of controlling the temperature profile in the integrated circuit to optimize its lifetime [Schwarzenberger, 1988; Oliver and Bower, 1970].

Temperature Dependence of Electromigration in Multilayered Metallizations. The definition of electromigration failure has changed with the introduction of multilayered interconnection metallizations with sensitive electrical circuits [Onduresk 1988]. Many studies on single-layer metallizations have used the

opening of the conductor as a criterion for failure, ignoring functional failures, including the resistance change of the metallization. The open criterion for layered metal systems may not be achievable in a test environment if one of the layers is not susceptible to electromigration.

Ondrusek derived a void-formation model for multilayered metallizations that allows calculation of void length from measured resistance and temperature coefficients [Onduresk 1988]. The temperature coefficient of resistance was

Figure 2.13 Temperature as a Function of Distance for High Current Condition [Lloyd, 1988]

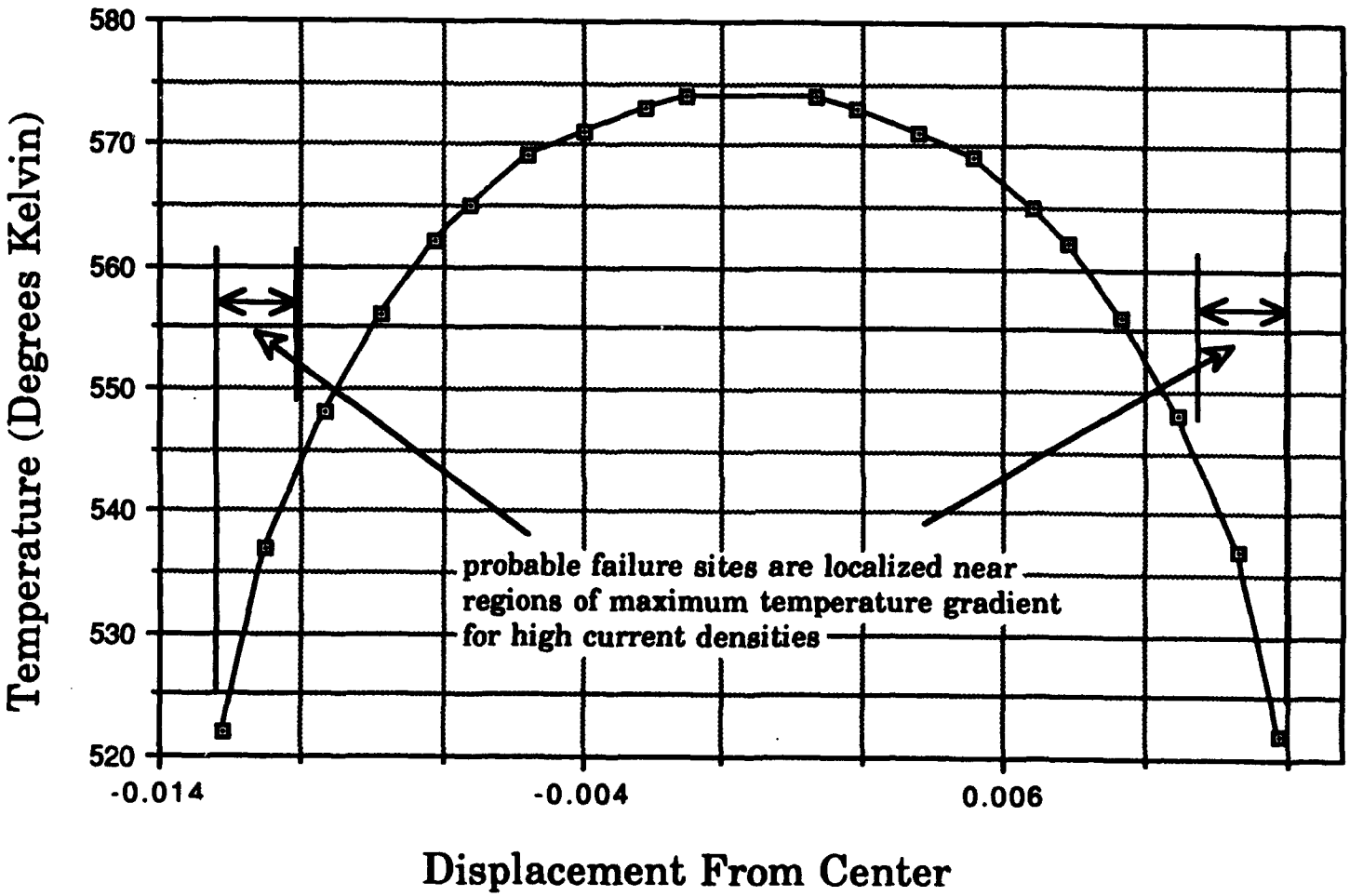
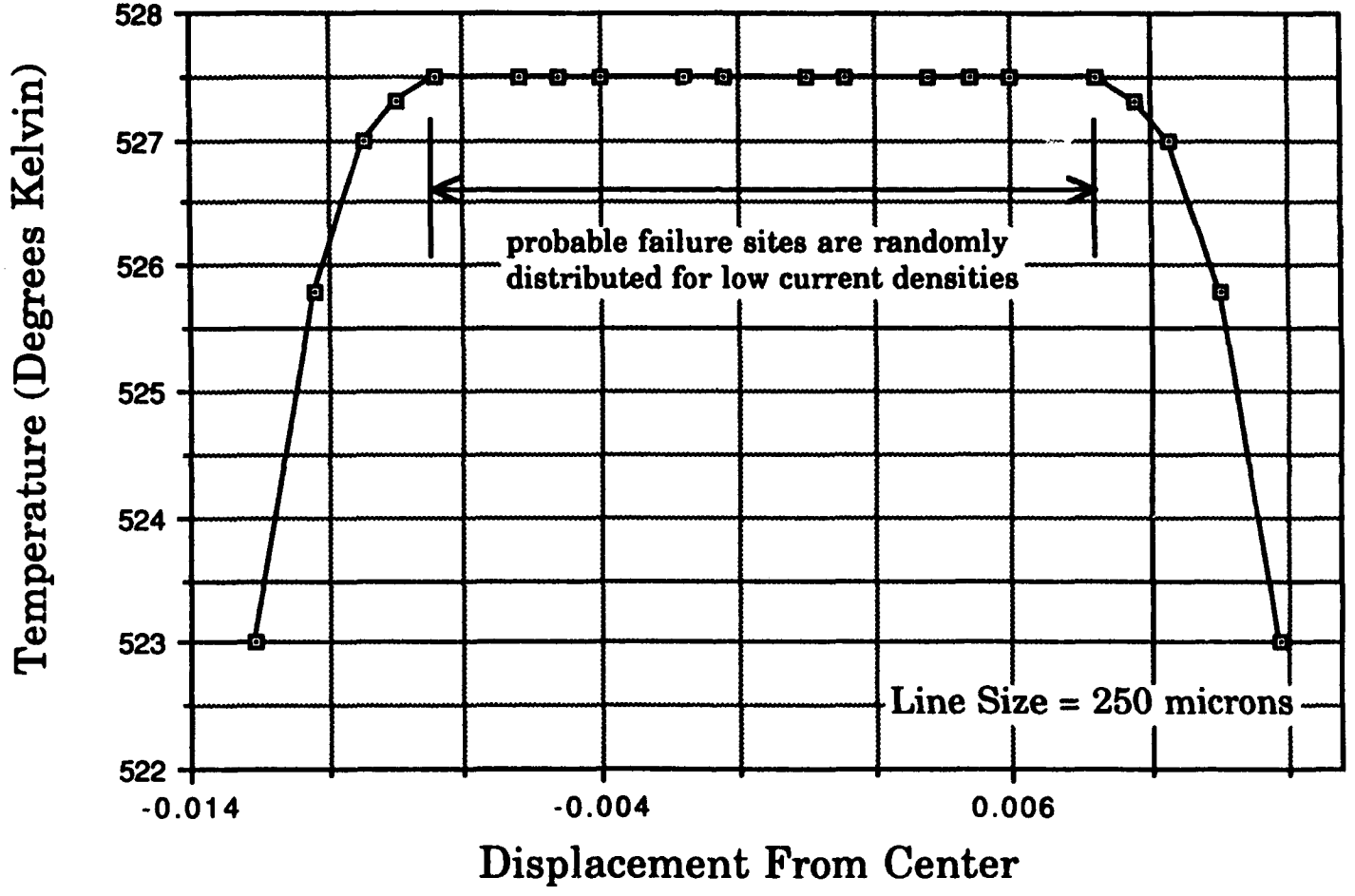


Figure 2.14 Temperature as a Function of Distance for the Low Current Condition [Lloyd, 1988]



investigated to verify that the refractory layer remains undamaged throughout the voiding process. The temperature coefficient, C, for metal is defined by the equation

$$R = R_i [1 + C(T - T_i)] \tag{2.35}$$

where R is the resistance at temperature T and R_i is the resistance at some fixed initial temperature, T_i. In a simplified case of a void extending through the aluminum layer, all of the current must pass through the refractory metal layer. The total resistance of the metal stripe is the sum of the initial component due to the refractory material-metal/aluminum sandwich plus the additional series refractory metal resistance that results from the void. This is represented by the following expressions:

$$R(v) = R_1 + R_2 \tag{2.36}$$

where

$$R_1 = R_{im}\frac{L-v(t)}{L}[1+C_m(T-T_i)] \tag{2.37}$$

and

$$R_2 = R_{ir}\frac{v(t)}{L}[1+C_r(T-T_i)] \tag{2.38}$$

Taking the derivative of Equation (2.25) with respect to temperature gives

$$\frac{\partial R(v)}{\partial T} = R_{im}C_m\frac{L-v(t)}{L}+R_{ir}C_r\frac{v(t)}{L} \tag{2.39}$$

where R_{im} is the initial resistance of the composite, R_{ir} is the initial resistance of the refractory metal layer, C_m is the initial composite temperature coefficient, C_r is the refractory metal temperature coefficient, L is the total metal line length, and v is the void length. Deviation from this model can occur due to intermetallic compound formation.

Reducing Electromigration Damage in Metallization Stripes. Solutions to reducing of electromigration do not lie in reducing steady-state temperature. The basic requirement for reducing electromigration damage is to reduce the local divergence of atomic flux. This can be accomplished, in principle, by reducing the magnitude of the atomic flux and/or the inhomogeneity of the parameters

controlling the mass transport. The magnitude of atomic flux is determined by the electromigration driving force and the grain-boundary diffusivity. Thus, to reduce the atomic flux, the option is to reduce either the driving force and/or the diffusivity. Reducing the driving force has some inherent difficulties, since it requires either a change in the scattering process responsible for the effective charge or a reduction in the current density. Because the current density is dictated by device functional requirements, the only choice is to reduce the grain-boundary diffusivity. The most common approach is by solute addition, which also results in improvements in conductor properties due to grain structure modification. Common examples are the addition of copper (Cu) or other solute elements such as manganese (Mn), magnesium (Mg), and titanium (Ti) to aluminum stripes [Ho 1989[b]].

There is a strong correlation between microstructure and electromigration lifetime in thin metal lines, which is particularly noticeable in VLSI technology when the line width and thickness of the metal lines are reduced to a submicron range comparable to the grain size. Larger lifetimes have been reported in large-grained aluminum (Al) films [Attardo and Rosenberg 1970] and in large-grained aluminum-copper films with bamboo structure [Vaidya 1980, Pierce 1981] (Figure 2.15). Annealing aluminum-copper (Al-Cu) lines at elevated temperature has been found to induce grain growth, increasing the electromigration lifetime. Structural modification of aluminum-copper (Al-Cu) films by adding titanium (Ti) and chromium (Cr) *which is at about 400°C, results in the formation of intermetallic compounds such as (Al_3Ti) and (Al_7Cr)*, improves electromigration lifetimes, due to changes in microstructure that reduce damage formation and block void growth through the use of a redundant barrier that maintains current continuity [Kwok 1987].

Line width has a strong influence on electromigration lifetimes. Agarwala reported a linear relationship between line width and lifetime of aluminum wide lines with line widths down to 5μm [1970]. Subsequent studies have indicated that as line width reduces to below a critical value, lifetime is found to level off or reach a minimum and then increase, reversing the trend in wider lines (Figure 2.16). The critical width decreases with decreasing film thickness. Kwok found the critical line width to be about 0.75 μm for the 0.5-μm line thickness for aluminum-copper (Al-Cu) lines (Figure 2.17) [Kwok 1989]. The critical line width is sensitive to the thickness of the metal lines. Lifetime increases by a factor of 5 as line width increases from 1μm to 2 μm. The lifetime of aluminum-copper-silicon (Al-Cu-Si), chromium-silver-chromium (Cr-Ag-Cr), and aluminum/titanium (Al/Ti) lines levels off beneath critical line widths of around 2.0 μm, 1.5μm, and 1.2μm, respectively. The line width dependence is much

Figure 2.15 MTF Due to Electromigration vs. Grain Size @ 150 deg. C [Attardo and Rosenberg, 1970]

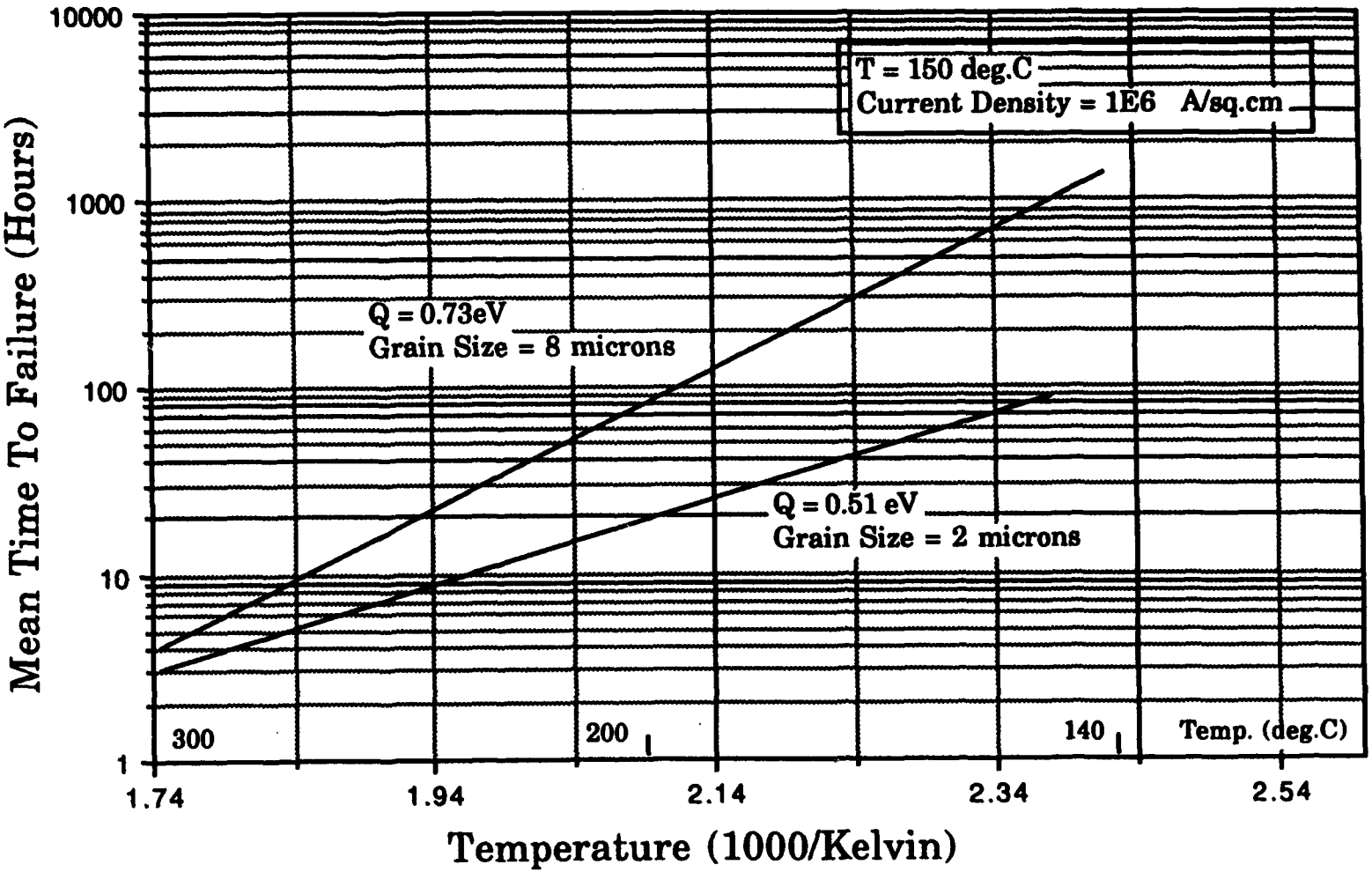


Figure 2.16 MTF Due to Electromigration vs. Metal Line Width @ 182 deg. C for Al lines. [Kwok, 1989]

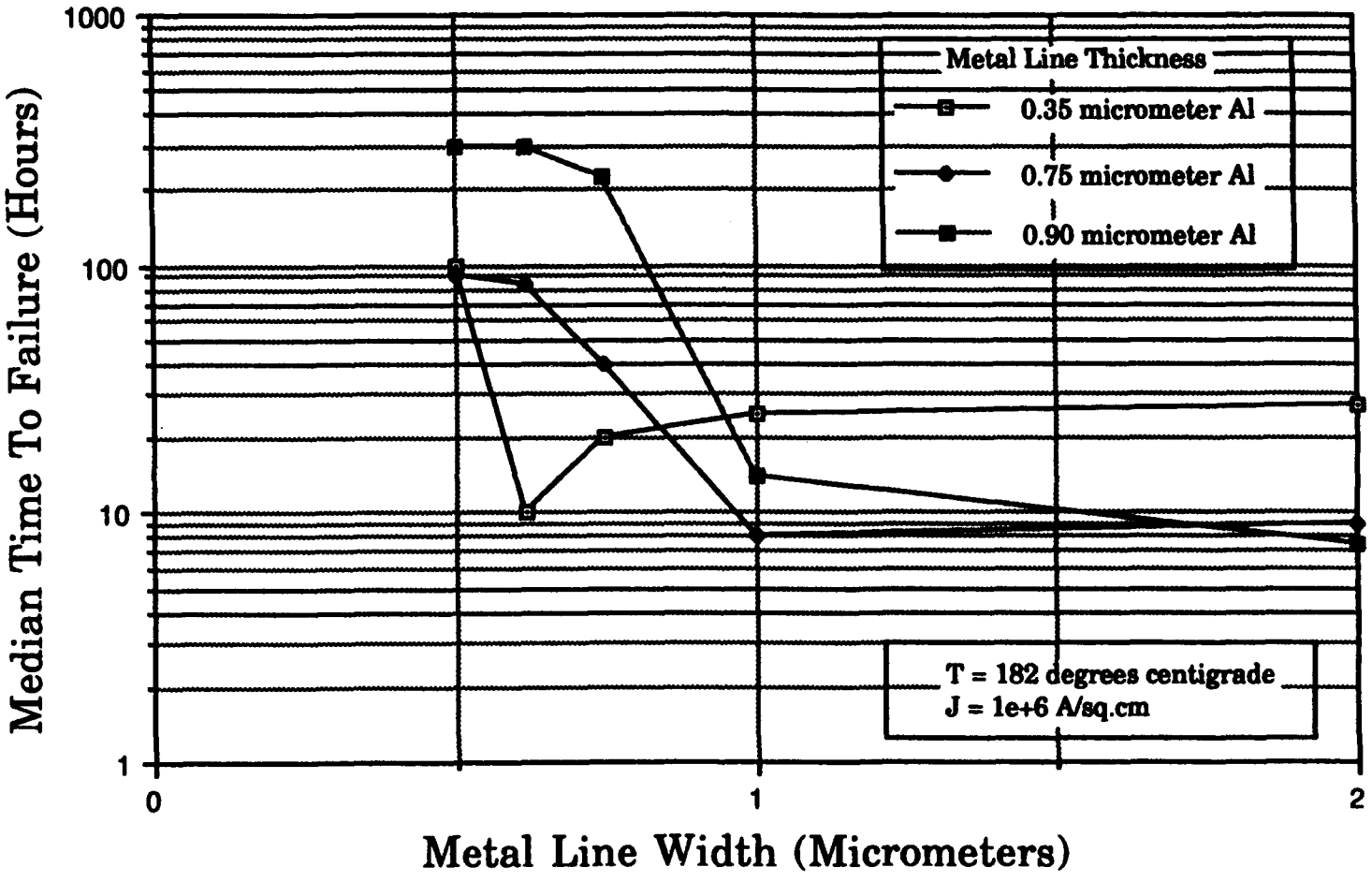
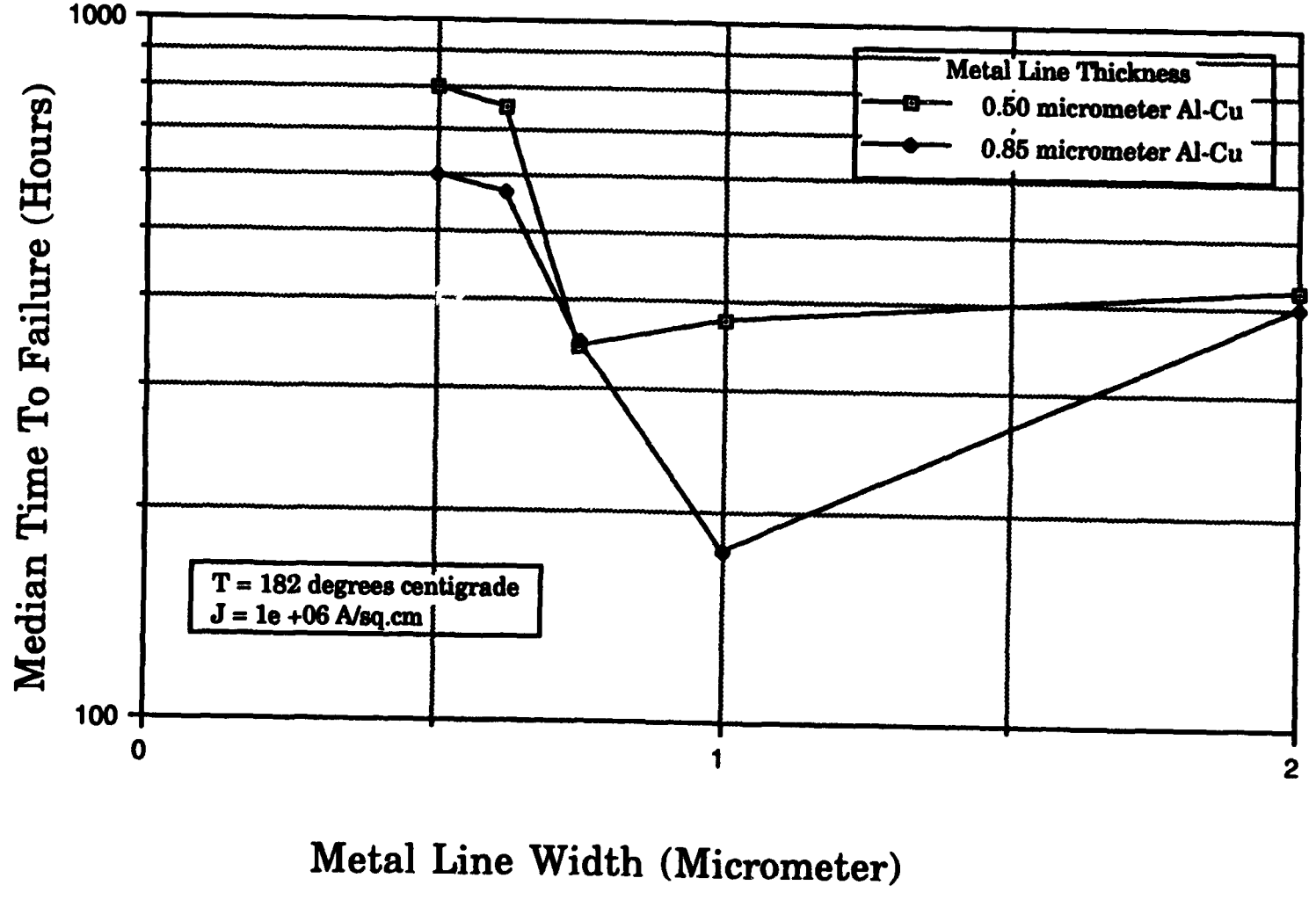


Figure 2.17 MTF Due to Electromigration vs. Metal Line Width @ 182 deg. C for Al-Cu lines. [Kwok, 1987]



stronger for aluminum-copper (Al-Cu) and aluminum-copper-silicon (Al-Cu-Si) lines than for chromium-silver-chromium (Cr-Ag-Cr) lines. The probability of alignment failure causing defects across a wide line is lower than for a narrow line; thus, it is more difficult for a crack to propagate across a wide line, and the expected lifetime increases. The dependence of lifetime on line width is also a function of pattern technique, metallurgy, and metal deposition conditions. Scoggan found that aluminum-copper (Al-Cu) lines patterned by chemical etch reached a minimum lifetime for line widths in the neighborhood of 5.5μm [1975]. The lifetime of aluminum-copper (Al-Cu) lines of the same dimension, patterned by metal lift-off, show a minimum lifetime for widths in the neighborhood of 3.5μm. Electromigration lifetime increases with decreasing thickness. The critical width decreases from 2.5 to 1.5μm when the film thickness decreases from 1.1 to 0.8μm in aluminum-copper-silicon (Al-Cu-Si) lines [Scoggan 1975].

Predicted interconnection failure rates at current density and temperature use conditions typically vary by several orders of magnitude, as they strongly depend on accelerated test data and model parameter selection. Generally, the failure time depends inversely on the temperature gradient and current density. Temperature acts as an strong accelerator of electromigration above temperatures of 150°C. Electromigration failures in structurally uniform conductors cannot be accelerated in reasonable time frames at temperatures lower than 150°C. The simple Black-type equation used for extrapolation of failure to use conditions can be used only over a small range of current densities. Moreover, the current exponent changes over various densities while the actual dependence of lifetime has been shown to be a complex function of current density and temperature that cannot be represented by an activation energy, the lifetime can be represented by an apparent activation energy that changes with operating conditions.

Electromigration damage forms at sites of maximum atomic flux divergence, of which the three main sources are structural defects, microstructural inhomogeneities, and local temperature gradients. Because typical field failures are characterized by structurally induced flux divergences, geometric configurations, and metallization grain structures - but not reduced steady-state temperature - can reduce electromigration damage.

2.2.3 Hillock Formation

Hillocks in die metallization can form as a result of electromigration or extended periods under temperature cycling conditions (thermal aging) [LaCombe Christou 1982, Thomas 1983]. Hillock formation as a result of electromigration often occurs upstream in the electron flow from the area of voiding, but hillocks grow

fastest at the downstream edge closest to the source of the migrating metallization. Both voiding and hillock formation sometimes occur on top of each other at temperatures in the neighborhood of 140°C to 200°C [Thomas 1983].

Hillock formation due to extended periods under temperature cycling conditions (thermal aging) is believed to be due to a self-diffusion process that occurs in the presence of strains within the metallization [LaCombe Christou 1982]. These strains may be due to a mismatch in the thermal expansion coefficients of the metallizations gold (Au), titanium-tungsten (Ti-W), underlying refractory layer, silicon (Si), and (SiO_2). Hillock growth is more extensive in films deposited on room temperature substrates than on heated substrates, indicating that the effect may vary with grain size. Coating the metal with silicon nitride prevents failures and voids and hillocks from forming for at least 500 hours at 360°C. Hillocks form at random in aluminum films when heated to temperatures around 400°C during fabrication, and can cause electrical shorts between adjacent lines and fracture of the overlying dielectric film. In double-level metallized devices, hillocks can result in shorts between the underlying and overlying metal layers. Hillocks, which can be caused by electromigration, can result in thin dielectric sites that are susceptible to subsequent breakdown of the intermetal dielectric. Hillock formation is largely remedied by using alloyed metal, such as aluminum-copper (Al-Co) and improvements in the technologies of passivation and packaging. Hillock formation is more function of Δ T and temperature gradient, and is mildly dependent on temperature (in the neighborhood of 400°C).

2.2.4 Metallization Migration

Metal migration occurs between biased lands under conditions conducive to electrocrystallization. Dendritic growth is a common cause of failure. Conditions for metal migration include a level of around 10 A/cm^2 current density at the tip of the dendrite through spheroidal and parabolic diffusion, sufficient liquid medium such as condensed water, applied voltage that exceeds the sum of anodic and cathodic potentials in equilibrium with the electrolyte, and materials with defects that allow water condensation to satisfy the current density requirement.

For a given material and pore frequency distribution, the ionic current density or rate of mass transport per unit area is proportional to the fraction of the pore area containing condensed water. Diagiacomo proposed a model to predict failure as a function of environmental conditions and the physical properties of the package, and verified the predictions on the basis of migration failure data from accelerated tests [1982]. The fractional area in which condensation occurs can be represented by

$$A_{fractional} = \frac{1}{2} erfc\left(\frac{1}{2\sigma}\right) \ln\left(\frac{r_{average}}{r}\right)^2 \tag{2.40}$$

where

$$r = \frac{2\gamma v}{kT \ln\left(\frac{p}{p_o}\right)} \tag{2.41}$$

$$erfc\left(\frac{1}{2\sigma}\right) = 1 - \frac{2}{\sqrt{\pi}} \int_{o}^{(1/2\sigma)} e^{-u^2}\, du \tag{2.42}$$

γ	= surface tension,
$A_{fractional}$	= fractional area of condensation,
v	= molar volume,
r	= pore radius,
$r_{average}$	= average radius,
p	= saturated vapor pressure above meniscus,
p_o	= saturated vapor pressure above flat surface,
p/p_o	= H (relative humidity at which condensation occurs),
σ	= ln (r_{50} / r_{16}), sigma.

The average current density is expressed as a function of ionic concentration, electric field, diffusivity, temperature, fractional condensed area, and overpotential, using the Butler-Volmer equation of electrode kinetics and assuming diffusion control [DiGiacomo 1982, Barton and Bockris 1962, Price 1958, Adamson 1990].

$$j = \frac{(Zf)^2 CDE}{2kT} erfc\left(\frac{1}{2\sigma}\right) \ln\left(\frac{kT\,(\ln H) r_{average}}{2\gamma v}\right)^2 \tag{2.43}$$

where

C	= ionic concentration in bulk,

r = pore radius,
$r_{average}$ = average pore radius,
z = valence of the metal ions,
F = Faraday's constant,
D = diffusivity of metal ions,
E = the overpotential, proportional to V_{pot}/r_d where v is the voltage applied and r_d is the radius of curvature of the dendrite,
γ = surface tension,
v = molar volume,
p = saturated vapor pressure above meniscus,
p_o = saturated vapor pressure above flat surface,
H = p/p_o relative humidity at which condensation occurs,
σ = ln (r_{50} / r_{16}), sigma,
T = steady-state temperature,
k = Boltzmann's constant.

To produce a metal dendrite, the current density at the whisker's tip should be orders of magnitude higher than the average current density [DiGiacomo 1982]. The growth is possible only through parabolic and spheroidal diffusion focussing the ionic current on the dendrite tip, which can be expressed in terms of the radius of curvature:

$$j_{tip} = \frac{(ZF)^2 CD}{2kT} \frac{V_{pot}}{r_d} erfc\left(\frac{1}{2\sigma}\right).\ln\left(\frac{kT\,(lnH)r_{average}}{2\gamma v}\right)^2 \qquad (2.44)$$

for dendritic growth $j_{tip} > j_{critical}$, the critical value of current density, or a mass transport rate of $\partial Q_{tip}/\partial t > \partial Q_{critical}/\partial t$. The mass transport rate is represented as $Q_{tip} = j_{tip} / ZF$. Integrating the equation with respect to time and substituting for $D = D_o\, exp\,(-\Delta H/kT)$ gives the critical value of the mass transport rate - that is, i.e, the number of ions that must be transported to achieve dendritic growth across the gap as $\partial Q_c/\partial t = l\rho/Mt$, where l = distance between electrodes, ρ = density of dendrite, and M = atomic weight. The time to failure can be given as [Diagiacomo 1982]

$$t_f = \frac{(\frac{\rho}{MC})(\frac{2r_d}{ZFD_o})l}{\beta(V_{pot} - V_t)\frac{1}{kT}e^{-\frac{\Delta H}{kT}}erfc\frac{1}{2\sigma}\ln(\frac{kT\ln Hr_{average}}{2\gamma v})^2} \quad (2.45)$$

where

ρ = the density of the dendrite,
M = the atomic weight,
C = the ionic concentration,
z = the ionic charge or the valence of the metal ions,
D_o = the diffusivity coefficient,
l = the distance between electrodes,
r_d = the dendrite radius,
$r_{average}$ = the average pore radius,
γ = the surface tension,
v = the molar volume,
ρ = the saturated vapor pressure above the meniscus,
ρ_o = the saturated vapor pressure above the flat surface (H approaching ρ/ρ_o is the relative humidity at which condensation occurs and
σ =ln $[r_{50} / r_{16}]$ sigma).
β = the fraction of metal surface at the anode which is susceptible to metal oxidation and therefore promoting metal migration
V_{pot} = potential difference applied
V_t = critical value of potential difference for dendritic growth

The average current, j, is expressed as a function of ionic concentration, electric field diffusivity, temperature, and condensed area β is the fraction of metal surface at the anode which is susceptible to metal oxidation, and therefore promotes metal migration in regions satisfying current density requirements. β varies from metal to metal because of differences in device passivation and solubility, and also with testing time and temperature. Diagiacomo performed tests on silver (Ag) migration between tinned silver-palladium (Ag-Pd) leads in encapsulated packages with a polyimide surface coating, aluminum (Al) cap, and silicone rubber or epoxy backseal [1982]. The test was carried out under temperature/relative humidity conditions under bias. A failure was defined as a

resistance of less than $5x10^6$ Ω.

Metallization migration involves the formation of aluminum growths beneath the silicon dioxide layer. Metallization migration occurs during deposition of conductors on silicon dies due to the combined effects of elevated temperature and electrical stress. It has been reported that triangular aluminum growths causing local short-circuits form beneath the silicon dioxide layer when conductor metallization is deposited at high temperature on silicon substrate [Bart 1969, Lane 1970]. Lane [1970] found that triangles form within minutes after deposition of an 8,000-Angstrom-thick aluminum layer on silicon at temperatures from 500°C to 577°C. The time for growth formation decreases with increasing temperature. The high temperatures (500°C to 577°C) at which this failure phenomenon occurs makes it a recessive mechanism in the normal operation of microelectronic devices.

2.2.5 Contact Spiking

Contact spiking is the penetration of metal into the semiconductor in contact regions at temperatures typically above 400°C, causing increased leakage current or shorting. This failure mechanism is accompanied by solid-state dissolution of the semiconductor material into the metal or alloy of the metallization,with the metal semiconductor interface moving vertically or laterally into the semiconductor. Contact spiking in chips is observed at high chip temperatures or localized high contact temperatures. Localized high temperatures may cause failure of the chip-to-substrate bond, thus increasing the thermal resistance, producing a thermal runaway of the device, or resulting in a large magnitude of electrical overstress.

Contact spiking can occur when the device is exposed to high temperatures during fabrication. This failure mechanism can be minimized by using silicon containing aluminum alloys, such as Al-1%Si, or using barrier metals such as titanium-tungsten (Ti-W) [Chang 1988, Farahani 1987, T.I. 1987]. It is not possible to characterize such interdiffusion failure mechanisms by an activation energy because of their irregular behavior.

Migration of aluminum (Al) along silicon (Si) defects has been observed in NMOS LSI devices (logic gates), due to contact migration, also known as electrothermomigration. Failures are accelerated by elevated ambient temperatures in the neighborhood of 400°C. Contact migration is a major cause of failure in (GaAs) devices [DeChairo 1981, Christou 1982, Ballamy 1978, Christou 1980]. This failure mechanism may be dominant during VLSI manufacture and packaging when temperatures exceed 400°C.

2.2.6 Constraint Cavitation of Conductor Metallization

This failure mechanism is marked by the opening of the conductor metallization through the formation of slit-like voids or edge voids. Hinode and Owada while examining stress driven diffusive voiding (SDDV) failures in 0.9 μm wide Al-2% Si metallization stripes deposited on thermally oxidized silicon substrate, aged for various times at temperatures in the range of 200-295°C, found that open circuit failures occurred typically in passivated stripes. SDDV failure rate increases with increase in aging time and temperature till a critical storage temperature above which the failure rate decreases with further increase in temperature. The time to failure increases with increase in line width. Lifetime dependence on line width is characterized as: $t \alpha w^{2.7}$ (for line widths in the range of 1-2.5 μm). Stress driven diffusive voiding failures also manifest themselves in the form of resistance increase. Metallization stripes failing in high resistance mode are not broken, however, the resistance of the line increases stepwise during aging. Typical resistance increase steps are in the range of 1 kΩ to 50 kΩ. The resistance increase steps increase in magnitude with increase in aging temperature. [Hinode and Owada 1987; McPherson and Dunn 1987]

There seems to be major disagreement in the microelectronic community as to the source of the stresses causing these voids. Various theories have been proposed to explain this failure mechanism, including:

- large silicon nodules in aluminum lines, causing metal voiding during room temperature storage;
- Coble and Nabaro-Herring creep of the conductor metallization;
- compressive stress of the plasma-enhanced silicon nitride passivation, combined with intrinsic stresses in nitrogen (N_2) - contaminated aluminum (Al) metal, causing voids at elevated temperatures [Klema 1984]
- compressive stresses of the overlying passivation, induced by cooling.

Nitrogen (N_2) Contamination Induced Voiding. Klema et.al., [Klema 1984] while evaluating MOS integrated circuits found that Al/Si metallization films deposited under conditions of nitrogen contamination coupled with subsequent silicon nitride (Si_3N_4) passivation resulted in open metal stripes. The opens occurred primarily at steps in narrow metal lines.

Failures were explained by the tendency of the metallization film to lower its energy. Energy stored in metallization includes: free surface energy equivalent

to the surface tension; interface energy; axial or compressive strain; and grain boundary or surface energy. Grain boundary were treated as cuts in a larger crystal. The atoms on the cut surface are chemically bonded to the solid on one side and not on the other, and thus sit in equilibrium potential wells that are at higher than the atoms in the bulk lattice. This extra potential energy constitutes the grain boundary or surface free energy. Smaller grain size thus indicates a greater potential for chemical reaction in order to minimize the overall film surface energy. Reactive species such as nitrogen (N_2) accumulate at grain boundaries by grain boundary diffusion both during and after deposition, and reduce metallization film free energy principally by compound formation and strain relief. Compound formation involves the spurious reactive species chemically bonding to the available atomic orbitals of higher energy grain boundary edge atoms to produce compounds of host metal with typically large negative free energies. For aluminum metallization the compounds include aluminum nitride (AlN) and aluminum oxide (Al_2O_3). Compound formation during sputter deposition thus reduces the driving force for grain growth. However, compounds such as aluminum oxide and aluminum nitride stop grain boundary motion and increase the metallization resistivity and hardness.

Metal voiding was determined to be the result of the combination of intrinsic metal stress produced by increased brittleness of metallization due to nitrogen contaminated sputtering process and thermal mismatch between the metallization and overlying passivation. The failure rate due to stress driven diffusive voiding was found to be dependent on steady state temperature for temperatures below 180°C, and inversely dependent on steady state temperature for temperatures above 180°C. [Klema 1984]

Silicon Nodule Formation Theory. Curry et.al., [Curry 1984] while evaluating 64k dynamic rams, observed a mechanism of metallization failures in both the flat and steep areas of the metallization [1984]. The failures had two distinct morphologies: clean sharp breaks, and large, irregularly spaced voids. The observed failure mechanism was not affected by voltage and current density, and could be generated by high-temperature storage, though no failures were noticed in thermal cycling. The silicon content of the metal films was much greater than the solid solubility of silicon and aluminum, with the precipitates in the neighborhood of a quarter of a micrometer in diameter. The failures were attributed to the presence of impurities and silicon defects in aluminum films. The mechanisms responsible for the failures were speculated to be grain-boundary diffusion, temperature-assisted creep, and hydrogen-embrittlement fracture enhancement.

The failure of the metallization due to silicon nodule formation was also recognized by Donnell et.al. who stated the problem in terms of the presence of large silicon nodules in aluminum which, in comparison to the cross-sectional area of the aluminum metallization, were large enough to restrict the current flow [1984]. Based on experimental evidence, they proposed the silicon nodule formation theory to explain the phenomenon of constraint cavitation. The theory is based on the fact that silicon alloys with aluminum at relatively low temperatures, and the solubility increases with temperature. The higher the temperature, the more silicon can be dissolved in the aluminum metallization before precipitates form. At normally high wafer-processing temperatures (aluminum is annealed at temperatures in the neighborhood of 475°C), more silicon can be dissolved in aluminum than can be retained at room temperature. Thus, as the wafer cools the excess silicon precipitates and forms nodules, epitaxial mounds, and epitaxial layers. The nodules form preferentially at dislocations in grain boundaries, and at stress points. The IC metallization was considered as a one-dimensional diffusion path, since in most applications the metallizations were long stripes. The diffusion of silicon in aluminum for thin films was found to be forty times that of bulk aluminum at elevated temperatures. This behavior was attributed to the polycrystalline nature of the aluminum metallization, which provided an enhanced diffusion path due to the larger number of grain boundaries. Silicon dissolved into the aluminum at the contact points, diffused throughout the strip, and was transported outward in all directions. The diffusion length of silicon into aluminum is expressed by the following equation:

$$L = [DT_a]^{1/2} \tag{2.46}$$

where L is the length silicon can be transported through aluminum, D is the diffusion coefficient expressed in $cm^2\ sec^{-1}$, and T_a is the annealing time. The diffusion coefficient of silicon is dependent on temperature. In these super-saturated aluminum films, the silicon nodules form on cooling, and further exposure to the high temperatures of glass deposition causes the precipitates to act as nucleation sites. Large nodules form by adsorbing smaller ones, and deplete the adjacent aluminum of its silicon. The size and shape of these precipitates depend on the crystalline structure of the aluminum and the rate of cooling. Slow cool-down results in large precipitates, while quick cooling results in the formation of numerous small precipitates. The temperature required to form appreciable precipitates is 200°C or higher, but the process is time-and temperature-dependent and can continue at room temperature, even though at a much reduced rate.

Coble and Nabaro-herring Creep Theory. The failures in long metallization lines

less than 4 micron wide, in the form of voids and cracks have also been attributed to Coble and Nabarro-Herring creep of the aluminum metallization [Turner 1985]. The source of this creep is a thermal expansion mismatch between the aluminum and the underlying silicon and silicon dioxide. The mechanism was complicated by the presence of silicon precipitates in the metallization. Turner et al. [1985] noted that the current density in the lines failing from this mode was much less than that noticed in electromigration failures; moreover, the failure rate characteristic decreased with time, unlike the electromigration failures. Turner tried to refute the earlier theory of Curry et al., which attributed the voids in the metallization to silicon nodule formation. The silicon nodule precipitate, being resistive, would give the metallization the electrical appearance of an open. Further, it was assumed that the precipitate would be removed in the top removal of the glass, leaving the appearance of a void or an open.

Turner et al. explained the failure of the metallization by reference to the thermal expansion mismatch between the aluminum and the silicon chip. The coefficient of thermal expansion of aluminum is about 26ppm/°C, while that of silicon is about 3ppm/°C, and that of silicon dioxide (SiO_2) is about 0.5 ppm/°C. Aluminum alloys are typically deposited onto a substrate heated to about 300°C, then alloyed at 425°C, packaged at temperatures between room temperature and 350°C, burned in at 125°C, and operated at less than 70°C. Every time the temperature of the metal-substrate system is changed, the significant thermal expansion mismatch induces a stress in the system. If the temperature is raised, the metal is held in compression. If the system is cooled, the metal is pulled in tension. This stress is equal in both dimensions of the interface plane. The force generated by the thermal expansion mismatch is proportional to the length of the line, while the strength of the line is proportional to its width. At high temperatures, the stress in the aluminum is relieved by grain boundary migration, in which the atom in one lattice site jumps to an adjacent vacancy. In order for an atom to jump, it must have enough energy to overcome the energy separating the two sites. In equilibrium, this occurs frequently, but there is no migration because the electron jumps are at random; thus, there is no net mass flow. However, if the metal line is subjected to a stress field, some mass flow will occur to relieve the stress. Since grain boundaries have the highest vacancy density, migration along grain boundaries is most rapid. According to Gibbs, the stress relaxation rate by grain-matrix diffusion of thin polycrystalline films in tension is given by

$$\frac{d\sigma}{dt} = \frac{-B_0 \Omega M D}{ghkTf}\sigma \tag{2.47}$$

where $d\sigma/dt$ is the stress rate, M is the elastic modulus, Ω is the atomic volume, B_o is the geometric factor (approximately equal to 10), g is the grain size, h is the film thickness, D_l is the lattice diffusion coefficient, f is the correlation factor for diffusion, k is the Boltzmann constant, T is the steady-state temperature, and σ is the stress [Turner 1985]. The stress relaxation rate by grain boundary migration (Coble creep) is

$$\frac{d\sigma}{dt} = \frac{-B_1 \Omega M D_g \delta}{gh^2 kT}\sigma \tag{2.48}$$

where B_1 is the geometric factor (approximately equal to 15), and $D_g\delta$ is the combined grain-boundary diffusion parameter [Turner 1985]. These two mechanisms work together in a thin film on substrate.

The stress may be relieved by two mechanisms - grain-boundary migration activated by grain matrix diffusion, and plastic deformation. Because there are few vacancies within the grain, grain matrix diffusion is relatively slow. Plastic deformation is fast, but operates only when the stress exceeds the yield stress of metal. Since grain-boundary migration can rapidly reduce the grain-boundary normal stress at higher temperatures, the metal rarely reaches the yield stress. Thus, at higher temperatures, grain-boundary migration rapidly relieves the grain-boundary normal stress, while grain-matrix diffusion slowly relieves the intra-grain stress. In unpassivated films, the edges of the lines act as vacancy sinks. In passivated films, the vacancies are trapped beneath the glass; if these vacancies collect in one location, they will form a void. Such voids are the first step in the formation of open metal lines, weakening the metal line and concentrating line stress in the metal around the void. At lower temperatures, neither grain-boundary diffusion nor grain-matrix diffusion can progress at appreciable rates [Turner 1985].

McPherson and Dunn Model: McPherson and Dunn model [McPherson and Dunn 1987] assumes vacancy to be an elemental unit of failure. The movement of vacancies results in clustering which results in void formation, void growth and conductor failure. Three primary sources of vacancies in VLSI Al-1%Si metallization are:

- Vacancy super saturation during metallization anneal in the neighborhood of

450°C

- Solid solubility of silicon in aluminum at room temperature is 0.5% therefore excess silicon during cool down from annealing temperature precipitates forming new nodules or increase size of existing nodules.
- Grain boundaries serve as potential sources and sinks for vacancies. Under passivation stress, gradients develop in the metallization transverse and parallel to the grain boundaries. Stress gradient serve as driving force for vacancy migration.

McPherson and Dunn model [McPherson and Dunn 1987] does not account for the effect of local yielding and work hardening during stress relaxation, and thus does not predict whether voiding will continue until the lead is totally severed. Stress concentration developed locally due to a void can result in local yielding. Further power cycling below recrystallization temperature can result in work hardening of metal and produce breakage. Further later stage of stress driven diffusive voiding can be dominated by rapid electromigration or fusing due to local rises in current. The time to failure is represented by: [McPherson and Dunn 1987]

$$TF = B_o \sigma^{-1} e^{Q/K_B T} \tag{2.49}$$

where

$$B_o = \frac{\ln\left(\frac{1}{f_c}\right)}{\left(\frac{(\phi(b,t) - \phi(a,t)A_o}{N(t)}\right)} \tag{2.50}$$

where Q is the activation energy for vacancy diffusion ($\approx$ 0.558 eV), K_B is the boltzmann constant (8.617 x 10_{-5} eV/K or 1.38 x 10_{-23} J/K), σ is the tensile stress in metallization (typical value 4 x 10_9 dyne/cm_2), f_c is the N(t=TF)/N_o, N(t) is the number of vacancies at time t, A_o is the area of surface bounding the volume of interest, a and b represent the void area in the metallization. The transport of vacancies in metallization is assumed to be Fickian and is represented by:

$$J(x,t) = \mu n(x,t)F - D\left(\frac{\partial n(x,t)}{\partial x}\right) \tag{2.51}$$

where J is the vacancy flux, μ is the mobility, and n is the density of vacancies,

$$J(x,t) = D\left(1 - \frac{\frac{\partial n(x,t)}{\partial x}}{\beta n(x,t)\sigma}\right)\beta n(x,t)\sigma \qquad (2.52)$$

$$= \phi(x,t)\sigma e^{-\frac{Q}{K_B T}}$$

F is the force acting on the vacancies due to stress gradients, and D is the diffusivity. The first term in equation (2.51) represents drift transport due to stress gradients, second term represents back diffusion due to concentration gradient. The model assumes that the force for vacancy transport, F, is derived from and proportional to the tensile stress σ in metallization, and that the drift component is much larger than the back diffusion component (Φ). Further the temperature dependence of Φ is assumed to be negligible compared to the exponential temperature dependence of the activation energy term.

Passivation Constraint Theory. Hinode [Hinode, Asano, Homma 1989] while examining stress driven diffusive voiding failures in Al-Cu-Si lines found that stress causing aluminum transport has two origins: thermal expansion mismatch between the aluminum and passivation films; compressive stress of the passivation. In fine lines, voids form due to thermal expansion mismatch, and in wide lines, voids form mainly due to compressive stress of the passivation. In wide lines (in the neighborhood of 30 μm) stress relaxation at higher temperatures is in form of bulge formation in the passivation containing the metallization, which causes a large deformation at the metallization edges. The temperature dependence of void growth rate is attributed to the temperature dependence of the deformation rate of passivation and mobility of aluminum. In fine lines (in the neighborhood of 2 μm), passivation has a lower compressive stress, and bulge formation in passivation becomes less dominant. Thermal expansion mismatch between the metallization and the passivation is the rate controlling process in fine lines. Voids in fine lines disappear when the lines are heated to a higher temperature and reappear during the cooling period [Hinode, Asano, Homma 1989]. The following models have been proposed based on the passivation constraint theory of stress driven diffusive voiding.

Yue Model: Yue et al. [Yue 1985] noticed that the voids in metallization were a result of certain device fabrication conditions, and that the density of these voids had a strong functional dependence on the compressive stress of the passivation film [1985]. They examined the effect of the overlying passivation and the rate

of cooling, and found that the rate of cooling from the passivation temperature had a significant effect on the void formation mechanism. The wafers, when cooled from 350°C to room temperature, developed a stress in the passivation, due to the difference in the coefficients of thermal expansion between the passivation and silicon. The maximum compressive stress was reached at room temperature and was independent of the cooling rate. The cooling rate of 22°C/min. allowed void formation, but a rapid temperature quench (approximately 65°C/min) did not allow sufficient time for the diffusion to form voids in aluminum. Yue hypothesized that since the missing aluminum from the voids was not found at any other location, as in hillock formation, the void space was a result of the coalescing of vacancies under a driving force. This driving force is comprised of large internal stresses and stress gradients developed in aluminum under cooling and enhanced by large applied passivation stress. In this process, aluminum (Al) covered by passivation is in a state of tension at room temperature. Annealing at 350°C causes the stress to become compressive, inducing multiaxial and localized stress gradients in the aluminum, especially near the line edges. A biaxial state of stress, consisting of both tension and compression, then coexists in the metal. Intergranular vacancy diffusion can occur from the boundaries in tension to the boundaries in compression diffusion creep. The coalescing of voids and vacancies can be expected to be greatest at the corners.

The metal void density can be analyzed by line fitting D_l (metal void density) with the following expression:

$$D_l \propto \left| \frac{\sigma_{passiv}}{G} \right|^n \tag{2.53}$$

where G is the shear modulus of aluminum (Al), and σ_{passiv} is the compressive stress in the passivation film at room temperature [Yue 1985]. The steady-state creep - the strain rate, de/dt - of bulk metal is related to the stress in the metal, σ_{metal}, by the following [Yue 1985]:

$$\frac{de}{dt} \propto \left| \frac{\sigma_{metal}}{G} \right|^n \tag{2.54}$$

For $n=1$, diffusion creep processes, such as Nabarro-Herring or Coble creep, take place; for the values of $n=4$ to 7, dislocation creep dominates. The volume of voids is proportional to the product of de/dt (strain rate) and the fixed time and volume of the line. The stress in the metallization is not a result of silicon

formation, since even pure aluminum (Al) films yield metal void formation [Yue 1985]. The reduction in density and size of the voids in hot substrate-sputtered aluminum/silicon (Al/Si) films is explained through the grain-size dependence of diffusion creep. In diffusion creep, the steady-state rate is related to the grain size by

$$\frac{d\epsilon}{dt} \propto \left|\frac{b}{d}\right|^{n} \cdot \left|\frac{\sigma_{metal}}{G}\right| \tag{2.55}$$

where n=2,3 for Nabarro-Herring and Coble creep, respectively; b is the Burger's vector; and d is the average grain size.

Kato and Niwa Model: Kato and Niwa theoretically estimated the stresses in an aluminum metallization under passivation arising from different coefficients of thermal expansion of the aluminum track and passivation film, using Eshelby's method-of-inclusion problem [Kato et al. 1990, Niwa et al. 1990]. The phenomenon of stress relaxation was found to be different at low and high temperatures.

Diffusion was practically inoperative at low temperatures, (defined as the temperature at which the time for diffusional relaxation is greater than 10^3 seconds; see Equations (2.81), (2.82), and (2.83)) and only instantaneous plastic deformation by dislocation glide was conceived as the relaxation mechanism. [Kato et al. 1990, Niwa et al. 1990]. Kato et al. found that the stresses did not become hydrostatic after relaxation due to plastic deformation. The stresses and strains after plastic deformation as a function of aspect ratio are as follows.

For $r > 0$ and $r < 1$:

For aspect ratios, r, such that $r > 0$ or $r < 1$, the strains after relaxation by plastic deformation are:

$$\epsilon_{11}^{P} = \frac{-((C_6+C_2C_7)\epsilon^{T}+C_1(C_3+C_2C_5))}{(C_2(2C_3+C_2C_5)+C_4)} \tag{2.64}$$

and

$$\epsilon_{22}^{P} = C_1+C_2\epsilon_{11}^{P} \tag{2.65}$$

where

$$C_1 = \frac{(1+r)^2}{4r^2(1-\nu)+r(5-4\nu)+2}\left(\frac{2(1+\nu)\epsilon^T}{1+r} + \frac{(1-\nu)\sigma_y}{\mu}\right) \tag{2.66}$$

$$C_2 = \frac{2(1+r)^2(1-\nu)+r}{4r^2(1-\nu)+r(5-4\nu)+2} \tag{2.67}$$

$$C_3 = \frac{2r^2(1-\nu)+r(5-4\nu)+2(1-\nu)}{(1+r)^2} \tag{2.68}$$

$$C_3 = \frac{2r^2+r(5-4\nu)+4(1-\nu)}{(1+r)^2} \tag{2.69}$$

$$C_3 = \frac{4r^2(1-\nu)+r(5-4\nu)+2}{(1+r)^2} \tag{2.70}$$

$$C_6 = -\frac{2r(1+\nu)}{1+r} \tag{2.71}$$

$$C_6 = -\frac{2(1+\nu)}{1+r} \tag{2.72}$$

Here, μ is the shear modulus of the metallization, ν is Poisson's ratio of the metallization, ϵ^T is the thermal strain given by Equation (2.85), σ_y is the yield strength of the metallization, and r is the aspect ratio of the metallization line ($r = a_2/a_1$; $2a_2$ is the metallization thickness and $2a_1$ is the metallization width) [Kato et al. 1990, Niwa et al. 1990]. Stresses resulting from plastic deformation are:

$$\sigma_{11}^R = -\frac{\mu}{(1-\nu)}\left(\frac{2(1+\nu)}{(1+r)}\epsilon^T + \frac{r(1-2\nu)+2(1-\nu)}{(1+r)^2}\epsilon_{11}^R + \frac{r(1-2\nu)-2\nu}{(1+r)^2}\epsilon_{22}^R\right) \tag{2.73}$$

$$\sigma_{22}^R = -\frac{\mu}{(1-\nu)}\left(\frac{2r(1+\nu)}{(1+r)}\epsilon^T + \frac{r(1-2\nu)-2\nu r^2}{(1+r)^2}\epsilon_{11}^R + \frac{r(1-2\nu)-2r^2(1-\nu)}{(1+r)^2}\epsilon_{22}^R\right) \tag{2.74}$$

$$\sigma_{33}^R = -\frac{\mu}{(1-\nu)}\left(2(1+\nu)\epsilon^T + \frac{-2r-2(1-\nu)}{(1+r)}\epsilon_{11}^R + \frac{-2-2r(1-\nu)}{(1+r)}\epsilon_{22}^R\right) \tag{2.75}$$

where σ_{ii} for $i = 1, 2, 3$ are the stresses in the metallization line along its width, thickness, and length, respectively.

For $r \approx 1$:

For aspect ratios, r, such that $r \approx 1$, the strains after relaxation by plastic deformation are:

$$\epsilon_{11}^P = \epsilon_{22}^P = -\frac{1}{2}\epsilon_{33}^P = -\frac{(1+\nu)\epsilon^T + \dfrac{(1-\nu)\sigma_y}{\mu}}{(4\nu-5)} \tag{2.76}$$

where μ is the shear modulus of the metallization, ν is Poisson's ratio of the metallization, ϵ^T is the thermal strain given by Equation (2.85), σ_y is the yield strength of the metallization, and r is the aspect ratio of the metallization line ($r = a_2/a_1$; $2a_2$ is the metallization thickness and $2a_1$ is the metallization width) [Kato et al. 1990, Niwa et al. 1990]. Stresses resulting from plastic deformation are:

$$\sigma_{11}^P = \sigma_{22}^P = -\frac{\mu}{(1-\nu)}((1+\nu)\epsilon^T(1-2\nu)\epsilon_{11}^P) \tag{2.77}$$

$$\sigma_{33}^{P} = \frac{-2\mu}{(1-\nu)}((1+\nu)\epsilon^{T}+(-2+\nu)\epsilon_{11}^{P}) \tag{2.78}$$

where σ_{ii} for i = 1, 2, 3 are the stresses in the metallization line along its width, thickness and length respectively.

For $r \approx 0$:

For aspect ratios, r, such that $r \approx 0$, the strains after relaxation by plastic deformation are:

$$\epsilon_{11}^{P} = \epsilon_{33}^{P} = -\frac{1}{2}\epsilon_{22}^{P} = -\epsilon^{T} - \frac{(1-\nu)\sigma_{y}}{2\mu(1+\nu)} \tag{2.79}$$

where μ is the shear modulus of the metallization, ν is the Poisson's ratio of the metallization, ϵ^{T} is the thermal strain given by Equation (2.85), σ_{y} is the yield strength of the metallization, and r is the aspect ratio of the metallization line ($r = a_2/a_1$; $2a_2$ is the metallization thickness and $2a_1$ is the metallization width) [Kato et al. 1990, Niwa et al. 1990]. Stresses resulting from plastic deformation are:

$$\begin{aligned} \sigma_{11}^{P} &= \sigma_{33}^{P} = \sigma_{y} \\ \sigma_{22}^{P} &= 0 \end{aligned} \tag{2.80}$$

where σ_{ii} for $i = 1, 2, 3$ are the stresses in the metallization line along its width, thickness, and length, respectively.

At higher temperatures, (defined as the temperature at which the time for diffusional relaxation is less than 10^3 *seconds; see Equations (2.81), (2.82), and (2.83)*) further relaxation of stresses after plastic deformation was possible due to diffusional relaxation. [Kato etal. 1990, Niwa etal. 1990]. The stress state after diffusional relaxation (a function of metallization grain structure) was completely hydrostatic. Bamboo-structured metallization lines showed negligible diffusional relaxation at lower temperatures, while equiaxed grain structures demonstrated diffusional relaxation at all temperatures. The relaxation times for lattice, interfacial, and grain-boundary diffusion are given by

$$\tau_{L} = \frac{\lambda^{2}kT}{8ED_{L}\Omega} \tag{2.81}$$

$$\tau_I = \frac{a_2 \lambda^2 kT}{8ED_I w_I \Omega(1+r)} \tag{2.82}$$

$$\tau_B = \frac{d^3 kT}{32ED_B w_B \Omega} \tag{2.83}$$

where λ is the length of grain along line axis (meter), k is Boltzmann's constant (8.617×10^{-5} eV/k or 1.38×10^{-23} Joule/Kelvin), T is temperature (Kelvin), E is the Young's modulus of metallization line, r is the aspect ratio of the metallization line, Ω is the atomic volume for conductor atoms (meter^3), D_L is the lattice diffusion coefficient, D_I is the interfacial diffusion coefficient, and D_B is the grain-boundary diffusion coefficient. Further relaxation of hydrostatic stresses was conceived to be due to several mechanisms, including decohesion or sliding at the aluminum (Al) line-passivation interface, and nucleation and growth of voids [Kato et al. 1990, Niwa et al. 1990].

The completely relaxed stress state was represented by

$$\sigma_{11}^R = \sigma_{22}^R = \sigma_{33}^R = \sigma^R = \frac{-6\mu r(1+\nu)\epsilon^T}{(2r^2 + r + 2) - 4r\nu - 2(1-r^2)\nu^2} \tag{2.84}$$

where

$$\epsilon_{11} = \epsilon_{22} = \epsilon_{33} = \epsilon^T = \Delta\alpha(T - T_p) \tag{2.85}$$

where μ is the shear modulus of the metallization line (Pascal or N/m^2), r is the aspect ratio of the metallization line [r = (metallization thickness)/(metallization width)], ν is the Poisson's ratio of the metallization line, $\Delta\alpha$ is the difference in coefficients of thermal expansion between the metallization line and the passivation (per°Kelvin), T is the temperature (Kelvin), T_p is the deposition temperature of the passivation, ϵT is the thermal strain resulting from the mismatch between passivation and metallization, and $\epsilon_{ii}S$ is the strains in directions 1,2,3 (direction 1 = along line width; direction 2 = along line thickness; direction 3 = along line length) [Kato et al. 1990, Niwa et al. 1990]. The time to failure due to stress-driven diffusive voiding was considered to be the time during which the area fraction, A, increases from A_{min} to A_{max} (Area fraction = r_o^2/l^2; r_o *is the void radius, and 2l is the void separation).*

$$\text{For} \quad \sigma \geq \frac{2\Gamma}{r_o}$$

$$T_f = \frac{kTl^3}{20D_B w \sigma \Omega} \tag{2.86}$$

$$l = \frac{a_2}{r} \qquad \text{for } r \geq 1$$

$$l = a_2 \qquad \text{for } 0 \leq r \leq 1$$

$$\text{For} \quad \sigma < \frac{2\Gamma}{r_o} \tag{2.87}$$

no void growth

where T_f is the time to failure in seconds, k is Boltzmann's constant (8.617×10^{-5} eV/k or 1.38×10^{-23} Joule/Kelvin), Γ is the surface energy per unit area (J/m^2), T is the temperature in Kelvins, D_B is the grain-boundary diffusivity ($meter^2/sec$), w is the grain-boundary thickness (meter), Ω is the atomic volume for conductor atoms ($meter^3$), and σ is the stress in metallization given by the following:

for equiaxed grain structure:

$$\sigma = \sigma_R$$

for bamboo grain structure: (2.88)

$$\sigma = \sigma_{33} \qquad t_{relax} \leq 1000 \text{ seconds}$$

$$\sigma = \sigma_R \qquad t_{relax} \geq 1000 \text{ seconds}$$

where σ_R is the hydrostatic stress after diffusional relaxation given by Equation (2.84), and σ_{33} is the stress along the metallization length given by Equations (2.75), (2.78), and (2.80).

2.3 EFFECT OF HYDROGEN (H_2) AND HELIUM (HE) AMBIENTS ON DEVICE METALLIZATION VERSUS TEMPERATURE

Reductions in the solid-state transport have been found possible through the interaction of active gases with thin-film metal conductors and bi-metallic diffusion couples (see Table 2.3). Studies indicate that a hydrogen ambient results in an improvement in electromigration rates, and stabilizes the intermetallic

formation due to interdiffusion.

Pasco and Schwarz considered several pathways for the gaseous ambients to affect mass transport mechanisms in metallization, including external surface diffusion, grain-boundary diffusion of metal atoms, and diffusion of vacancies into the bulk from defects present on external and internal surfaces, and from dislocations [Pasco 1983]. They studied the effects of heating rates in pure hydrogen and He-8.5%H_2, relative to an inert helium environment, on the electromigration of Al-2%Cu conductors. For a heating rate of 1°C/min, the electromigration rate decreased by a factor of 10 for the hydrogen versus helium ambient. A decrease in the electromigration rate by a factor of five is achieved with only an 8 1/2% H_2 in the ambient. At higher heating rates (5°C/min), an increase in the degree of damage before the onset of failure increases with an increasing hydrogen constant. Table 2.2 shows the effect of heating rate on hydrogen and helium ambients [Pasco and Schwarz 1983]. The activation energy is constant, while the pre-exponential A varies, indicating that the ambient effects are independent of heating rate, since the activation energy is constant.

The process of electromigration is a combination of two processes: nucleation of voids, and growth of voids. Davis has shown that the nucleation of dislocation loops, with the quenching in the vacancy supersaturation, is a low-temperature process [1967]. At low temperatures in the neighborhood of 25°C, the process of nucleation of voids is transport-limited, and at moderately high temperatures (in the neighborhood of 100°C), the process is limited by a low driving force, due to the effectively lower supersaturation of vacancies. Dislocation loops can be precursors to the formation of microscopic voids in electromigration. Under current stressing, ions are transported along the grain-boundary generally, in the direction of the electron flow for aluminum (Al) alloys. In addition, vacancies flow in the opposite direction, producing local vacancy supersaturation. These vacancies can cluster to form dislocation loops and microscopic voids, given sufficient time at lower temperatures. The effect of the active ambient is to promote uniform nucleation and an increase in the nucleation rates. The ambient increases the rate of electromigration damage, up to the point where the growth of voids becomes the rate-limiting factor. This increase in the nucleation rate is actually beneficial, since many small voids are less likely to be harmful than a few large voids.

Void growth is decreased by the hydrogen ambient through a number of mechanisms [Pasco and Schwarz 1983]. Adsorbed hydrogen can become bound to vacancies, decreasing their migration rates, pinning them, or effectively reducing their concentration. In addition, the segregation of hydrogen to grain-boundaries decreases the grain-boundary energy and diffusion rates. These effect

a decrease in the overall transport and electromigration rates, due to the hydrogen ambient [Pasco 1983]. Higher heating rates decrease the time for nucleation and shift the electromigration damage to higher temperatures, which is reflected in the lowered pre-exponential A for higher heating rates (Table 2.2) [Pasco and Schwarz 1983]. In addition, hydrogen promotes uniform nucleation and, therefore, increases the amount of the damage that can be sustained before the rapid onset of failure in all cases.

Black observed that the cracking of the passivating glass overlayer as a result of hillock formation during electromigration damage could lead to a sudden increase in electromigration rates, due to the release of the compressive stresses in the conductor [1978]. These sudden increases in the electromigration rate can be avoided if the device is packaged in hydrogen ambient.

2.4 TEMPERATURE DEPENDENCIES OF FAILURE MECHANISMS IN THE DEVICE OXIDE

2.4.1 Slow Trapping (Oxide Charge Trapping and Detrapping)

Slow trapping is a failure mechanism, observed only in standard MOS transistors and certain types of memory devices, programmed by the transport of charge from the source or the drain through the gate oxide to the gate interface. High temperatures, combined with a high electric field, provide electrons with enough energy to cross the silicon-silicon dioxide ($Si-SiO_2$) interface [Nicollian 1974, Woods 1980]. Interstitial states at the silicon-silicon dioxide ($Si-SiO_2$) interface trap electrons and hold them in the oxide, permanently shifting the threshold voltage of the device. The presence of electrons permanently trapped at the oxide interface decreases the speed at which the device can be programmed by creating a field that opposes further electron flow through the oxide interface. The failure mechanism of slow trapping decreases the circuit speed and causes functional failures.

The trapped charge within the MOS oxide results in a C-V curve identical to that of the ideal structure, but shifted along the voltage axis by an amount equal to the flatband voltage shift. The flatband voltage shift is a function of the location of the oxide-trapped charge with respect to the silicon-silicon dioxide ($Si-SiO_2$) interface. The charges in the oxide induce equal and opposite charges divided between the silicon substrate and the metal gate. The closer the charge is to the silicon-oxide interface, the larger the charge induced in the silicon. The charge in the silicon alters the charge stored at thermal equilibrium, and thus alters

Table 2.2 Summary of Kinetic Parameters for Electromigration and Extent of Damage Sustained by Al-2%Cu Thin Stripes (current stressed at 3 x 10^6 A/cm^2). An Almost Constant Activation Energy at Different Heating Rates Suggests that the Phenomenon is Temperature Rate-Independent in Hydrogen and Helium Ambients)

Heating Rate	He(Helium)	He-8 1/2%H_2	H_2
1 K/min	Q = 0.67 eV	Q = 0.67 eV	Q = 0.67 eV
	A = 7.0 x 10^3 s^{-1}	A = 1.4 x 10^3 s^{-1}	A = 6.7 x 10^2 s^{-1}
	$\Delta R/R_{o\ failure}$ = 0.67	$\Delta R/R_{o\ failure}$ = 0.96	$\Delta R/R_{o\ failure}$ = 1.2
5 K/min	Q = 0.67 eV	Q = 0.67 eV	Q = 0.67 eV
	A = 1.4 x 10^3 s^{-1}	A = 4.2 x 10^3 s^{-1}	A = 1.1 x 10^4 s^{-1}
	$\Delta R / R_{o\ failure}$ = 0.28	$\Delta R / R_{o\ failure}$ = 0.56	$\Delta R / R_{o\ failure}$ = 0.62

Table 2.3 Effect of H_2, He, Ar, and N_2, Ambients v. Temperature

Atmosphere	Stripe Composition	Failure Mechanism/ Failure Definition	Observation	Reference
argon(Ar), hydrogen(H_2)	aluminum	electromigration /resistivity	Electromigration rate ($dR/R_o\ dt$) decreased by a factor of 10 for hydrogen(H_2); atmosphere compared to argon(Ar) at j= 0.7 x 10^6 A/cm^2 and 200°C.	Shih and Ficalora [1981]

hydrogen(H_2), helium(He)	aluminum(Al), aluminum-copper(Al-Cu)	electromigration /resistivity	Al stripes: H_2 improves (decreases) electromigration rate by a factor of 13 to 16, as compared with helium(He). Al-Cu Stripes: H_2 improves electromigration rate by a factor of 4 to 7, compared with helium (He) environment.	Sardo [1981]
nitrogen(N_2), hydrogen(H_2) and H_2O	aluminum(Al)	hillock formation /reflectivity	Hillock formation at elevated temperatures during film deposition was greatly decreased for high partial pressures of H_2 and H_2O relative to that of N_2.	McLeod and Hartsough [1977]
hydrogen incorporated during E-beam deposition	aluminum(Al)	hillock formation	TTF of 40 hours at 7 x 10^6 A/cm^2 for hydrogen incorporated samples; an anneal at 550°C produced fewer hillocks in the E-beam film.	Meyer [1983]
hydrogen(H_2), argon(Ar), oxygen(O_2), nitrogen(N_2), helium(He), and air	Au-Al thin-film diffusion couple	intermetallic compound formation	Au-Al intermetallic compound is formed at 350 to 400°C for all environments except H_2.	Shih and Ficalora [1978]
hydrogen(H_2), air	Cu-Sn, Ag-Sn, Ni-Sn thin-film diffusion couple	intermetallic compound formation	Rates of intermetallic formation reduced dramatically in H_2 environment compared to air. Reduction of rate by a factor of 3 to 10 observed.	Shih and Ficalora [1979]
oxygen(O_2), argon(Ar)	Au-Al thin-film diffusion couple	intermetallic compound formation	After 250°C anneal in 0.5 atm of either O_2 or Ar, SEM photography was used to evaluate the character of the intermetallic formation. Grain-boundary diffusion appears to be the dominant failure mechanism in O_2 environment; surface diffusion dominated in Ar environment.	Shih and Ficalora [1978]

the flatband voltage. The maximum value for the flatband voltage shift occurs when the charge is located at the silicon-oxide interface ($x_m = t_{ox}$), because the charge induced is contained entirely in silicon. In contrast, if the charge is located adjacent to the metal-oxide interface ($x_m = 0$), there is no effect on the flatband voltage (Equation (2.89)). The flatband voltage shift of C-V curves is expressed by Balland and Barbottin [1989] and Muller and Kamins [1986] as:

$$\begin{aligned} \Delta V_G = \Delta V_{FB} &= -\frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x'}{t_{ox}} \rho(x') dx' \\ &= -\frac{1}{\epsilon_o \epsilon_{ox}} \int_0^{t_{ox}} x' \rho(x') dx' \\ &= -\frac{1}{\epsilon_o \epsilon_{ox}} x_m Q_{ot} \end{aligned} \tag{2.89}$$

The gate bias voltage shift of the I-V curve is also a function of the distribution and location of the oxide-trapped charge. When a positive voltage is applied to the metal gate, the gate bias voltage shift is given by

$$\Delta V_G^+ = -\frac{x_m Q_{ot}}{\epsilon_o \epsilon_{ox}} \tag{2.90}$$

When a negative voltage is applied to the metal gate, the gate bias voltage shift is given by

$$\Delta V_G^- = -\frac{t_{ox}}{\epsilon_o \epsilon_{ox}} \left(1 - \frac{x_m}{t_{ox}}\right) Q_{ot} \tag{2.91}$$

where ϵ_o is the free space permittivity (8.85 x 10^{-14} F cm^{-1}), ϵ_{ox} is the relative permittivity of oxide [dielectric constant $\approx$ 3.9 (typical value)], t_{ox} is the oxide thickness (cm), x' is the distance away from the metal-silicon dioxide interface, X_m is the centroid of charge contained in the oxide (between 0 and t_{ox}), Q_{ot} is the density of the oxide-trapped charge over the thickness of the oxide per unit area of the silicon-silicon dioxide (Si-SiO_2) interface ($C\,cm^{-2}$), and ΔV_{FB} is the flatband voltage shift. The prime distribution moment ($X_m Q_{ot}$) increases or decreases with the increase or decrease in X_m or Q_{ot}. If the trap distribution in the oxide is uniform parallel to the interfaces, the C-V curve shifts without distortion. For a non-uniform trap distribution parallel to the interfaces, the C-V curve distorts.

First-order Trapping Model. Balland and Barbottin [1989] related the drift and deformation in C-V and I-V characteristics to trap parameters in the oxide (N_T, the spatial density of traps; E_T, the fundamental energy level of traps; and σ_c, the capture cross-section of traps). The first-order model assumed that the capture cross-coefficient and trap density remain constant during trapping.

Trap-Filling Kinetics: Trap-filling kinetics when re-emission is negligible can be predicted based on the following assumptions:

- the oxide has only one form of electron traps;
- the electron traps possess a single discrete level, E_T;
- the electron traps do not act as generation-recombination centers; they can exchange electrons only with the conduction band;
- during the trap-filling phase, no re-emission takes place, i.e., $e^{th}_n=0$, $e^{opt}_n=0$.

The oxide-trapped charge resulting from trap filling is given by

$$\begin{aligned} Q_{ot} &= qn_{TT}(t) \\ &= q\left(1-e^{-t_{inj}/\tau_c}\right)\int_0^{t_{ox}} N_T(x)dx \end{aligned} \tag{2.92}$$

where N_T is the spatial density of traps possessing level E_T (cm^{-3}), q is the absolute value of the electronic charge (1.6×10^{-19} Coulomb), t_{inj} is the length of the injection phase (second), τ_c is the capture time constant (second) in the trap-filling experiment (Equation (2.93)), and t_{ox} is the oxide thickness (cm). The capture time constant is given by the equation [Balland and Barbottin 1989]

$$\tau_c = \frac{qv_d}{\sigma_n J_{inj} v_{th}} \tag{2.93}$$

where v_d is the drift velocity ($cm\ s^{-1}$), v_{th} is the thermal velocity ($cm\ s^{-1}$), σ_n is the capture cross-section for electrons (cm^2), and J_{inj} is the density of injected current ($A\ cm^{-2}$).

Trap Emptying: Trap emptying is represented as a separate process once the traps have been filled partially or totally [Balland and Barbottin 1989]. The emptying kinetics of traps when re-trapping is negligible can predicted based on the following assumptions:

- only one type of carrier takes part in the exchange;
- only free electrons are released thermally or optically by traps;
- traps can exchange electrons only with the conduction band;
- the density of electrons is zero at the onset of depopulation;
- at all times, the density of free electrons is small compared to the density of carriers still trapped.

The charge trapped at time t decreases exponentially with time

$$Q_{ot}(t) = \left(Q_{ot_{(t=0)}}\right) e^{-te_n^{th}} \tag{2.94}$$

where e_n^{th} is the thermal emission coefficient (sec^{-1}), t is the time in seconds (Equation (2.97)), and $Q_{ot(t=0)}$ is the density of the oxide-trapped charge integrated over the thickness of the oxide per unit area of silicon-silicon dioxide (Si-SiO_2) interface at time t=0, i.e., at the onset of trap emptying given by Equations (2.95) and (2.96).

Two cases can exist at time t=0. First, the traps may be filled to saturation; and second, the traps may not be filled to saturation. If the traps are filled to saturation at time t=0 [Balland and Barbottin 1989],

$$Q_{ot_{(t=0)}} = q \int_0^{t_{ox}} N_T(x)dx \tag{2.95}$$

If the traps are not filled to saturation at time t=0,

$$Q_{ot_{(t=0)}} = q \int_0^{t_{ox}} n_T(x)dx \tag{2.96}$$

where q is the absolute value of electronic charge(1.6×10^{-19} Coulomb), N_T is the spatial density of traps possessing level E_T (cm^{-3}), n_T is the spatial density of filled traps of energy E_T, and t_{ox} is the oxide thickness [Balland and Barbottin 1989]. The thermal emission coefficient is a function of temperature given by

$$e_n^{th} = \left(\frac{2\sqrt{3}(2\pi)^{3/2} m_n^* k^2}{h^3}\right) \sigma_n T^2 e^{-E_o/kT} \tag{2.97}$$

where m_n^* is the effective mass of the electrons in silicon dioxide (SiO_2), k is the Boltzmann constant (8.617 x 10^{-5} eV/K or 1.38 x 10^{-23} J/K), and h is Planck's constant (6.62 x 10^{-34} J.s) [Balland and Barbottin 1989].

Hickmott Model: Hickmott [1975] presented a model for thermally stimulated ionic conductivity due to trapped charges. The model is based on the assumption that at the start of the measurement, all the ions are present in the ion traps near one of the interfaces. When the temperature of the MOS capacitor is increased, the emission of ions from traps takes place at an increasing rate, which results in an increase in ionic current. After most of the ions have been emitted, the ionic current decreases. The flux of the ions emitted at time t, based on the assumption that ion traps corresponding to one type of ions have a single energy, E_o, is represented by

$$-\frac{dN(t)}{dt} = s\, N(t)\, e^{-E_o/kT(t)} \tag{2.98}$$

where $N(t)$ is the density of ions trapped at time t (cm^{-2}), E_o is the single activation energy, s is the proportionality constant (sec^{-1}), and k is the Boltzmann constant (8.617 x 10^{-5} eV/K) . The current density is represented by

$$J_G(t) = q\frac{dN(t)}{dt} \tag{2.99}$$

where q is the magnitude of electronic charge (1.6 x 10^{-19} coulomb), $N(t)$ is the density of ions trapped at time t (cm^{-2}), and t is the time. The density of the ions still trapped follows from integration of Equation (2.98):

$$N(t) = N_o\, e^{-s\int_0^t e^{-E_o/kT(t')}\, dt'} \tag{2.100}$$

and the current density is represented by

$$J_G(t) = q\, s\, N_o\, e^{-E_o/kT(t) - s\int_0^t e^{-E_o/kT(t')}\, dt'} \tag{2.101}$$

The solution to equation (2.101) depends on how the temperature varies as a function of time, and exist for hyperbolic variation of temperature ($1/T = 1/T_o - at$) [Hickmott 1975, Stagg 1977], and linear variation of temperature with time ($T = T_o + bt$) [Hillen 1981]. Typically, temperature transients and temperatures in the neighborhood of 175°C or greater result in failures due to slow trapping [Gottesfeld 1984].

2.4.2 Gate Oxide Breakdown

Two forms of oxide breakdown can result from electrostatic discharge and electrical overstress or from time-dependent breakdown which occur during operation within rated conditions of voltage, temperature and power dissipation.

Electrostatic discharge. An integrated device can be considered equivalent to a circuit with multiple paths to the ground. When one pin is grounded, potentials sufficient to cause dielectric breakdown, junction shorts, or cracks between isolated regions may be discharged through the device. ESD discharges typically last less than 50 μs.

Electrostatic pulses can arise from contact with air, skin, glass or charge-carrying particles. Typically, ESD pulses damage gate oxides or melting of small amounts of the device, creating minute explosions, voids, cratering, and subsequent short circuit or open circuit on the device surface. Higher temperature result in a significant reduction in the electrostatic discharge resistance of the component [Kuo 1983, Hart 1980].

Typically, ESD failures result in fracture of the gate oxide in MOS devices,since voltage is in excess of the breakdown voltage (in bipolar devices, breakdown bulk occurs predominantly in the device). High currents through the breakdown site cause localized heating and usually produce a metal silicon alloy through the gate fracture site, forming a resistive short across the gate. The short can be a gate to drain short, source short, or substrate short, depending on the structure of and imperfections in the oxide. Most likely sites for ESD damage in defect-free oxides are the source or drain sites, depending on the polarity of the transient and biasing of the device. Gate-to-substrate shorts are more prevalent in devices with pre-existing oxide defects in the form of geometrical or dopant irregularities [McAteer 1989]. Typical PN-junction ESD damage occurs in reverse-biased conditions in the form of degraded PN-junction characteristics. The failed PN junction is characterized as cracked glass across the junction on the surface of the chip.

Metallization-open Voltage Threshold for ESD Failures: Typically, vaporized metal lines are indicators of EOS failures, but sufficiently large ESD pulses can also result in such failures. Open-circuit sites typically are at points of constriction, such as oxide steps. ESD failures causing metallization vaporization are uncommon, however, due to the presence in the discharge current path of other energy-absorbing elements which reduce the transient current through the metal below damaging current densities [McAteer 1989]. The condition for melting of non-stepped metallization stripes under adiabatic conditions is

$$J^2 t_m = K_m \tag{2.111}$$

where t_m is the time to melt in seconds, J_m is the current density in metallization (A/cm^2), and K_m is a constant (Equation (2.112)).

$$K_m = \frac{(\Delta T)H_c + H_f}{0.239\rho} \tag{2.112}$$

where ΔT is the temperature rise (= 660°C - 25°C = 635°C), H_c is the heat capacity per unit volume ($\approx$ 0.637 cal/cm^3 °C @ 240°C), H_f is the heat of fusion per unit volume (248.5 cal/cm^3), and ρ is the volume resistivity of metallization ($\approx$ 5.1 x 10^{-6} Ω cm). The time constant of the RC circuit can be calculated based on resistance and capacitance (R = 1500 Ω; C = 100 pF) values for a standard human-body model. The time to stripe melting can be approximated as five time constants:

$$t_{m(\max)} = 5\,\tau \tag{2.113}$$

The average current in the circuit can thus be calculated from

$$J^2 = \frac{I^2}{A^2} = \frac{K_m}{t_m} = \frac{K_m}{5\tau}$$

$$I^2_{average} = \frac{K_m A^2}{5\tau} \tag{2.114}$$

The peak discharge current can be estimated from the modified Speakman model (Equation (2.108)) since the first term containing V_d does not apply):

$$P_{av} = (I_{average})^2 R_{average} = \frac{R_b I_p^2}{10}$$
$$I_p^2 = \frac{10(I_{average})^2 R_{average(circuit)}}{R_b} \quad (2.115)$$

where $R_{average(circuit)} = (R_b + R_{stripe} + R_{series})$, and R_{series} is any series load resistance in the circuit. The ESD voltage threshold then required for metallization melting is

$$V = I_p R_{average(circuit)} \quad (2.116)$$

Devices are typically protected against ESD by protection structures shorting the ESD pulse voltage to ground or to the supply voltage to limit the current entering the critical junction. The damage voltages for protected devices are in the range of 3,000 to 9,000 V, depending on protection, as compared to as low as 100V for unprotected devices. However, on-chip protection can reduce device performance.

Time-dependent Dielectric Breakdown. Time dependent dielectric breakdown (TDDB) is the formation of low-resistance dielectric paths through localized defects in dielectrics, such as thermally grown or other oxides in MOS devices only. Failures typically occur at weaknesses in the oxide layer due to poor processing or uneven oxide growth. Various studies have demonstrated a correlation between the low breakdown strength and the presence of stacking faults in the oxides [Lin 1983, Liehr 1988]. Other studies have attributed early oxide breakdown to charge accumulation in the oxide [Lee 1988, DiStefano 1975, Harai 1978, Ricco 1983, Holland 1984] and to local thinning and discontinuities in the oxide caused by metal precipitates [Honda 1984, 1985, Wendt 1989]. The mechanism is characterized by sudden, usually permanent, d.c. conduction in the dielectric of MOS capacitors. Typically, thin FET dielectric materials exhibit this breakdown failure mechanism, depending on latent defect density, temperature, electric field intensity, the ratio of the device operating potentials to the intrinsic dielectric strength, and the distances between the conductors in electronic packages defined by technology limits or electrical requirements.

Fowler-Nordheim Tunneling-based Models for TDDB: Fowler-Nordheim tunneling models are based on the failure of oxides due to TDDB as a consequence of

charge accumulation in the oxide. Breakdown of the oxide occurs when a critical charge density is reached in the oxide to trigger the breakdown process [Lee 1988, DiStefano 1975, Harari 1978, Ricco 1983, Holland 1984]. The critical charge density is proportional to the total number of electrons injected in the oxide and the probability of holes being generated by these electrons and trapped in the oxide [Chen 1985]:

$$Q_{critical} = J\, t_{BD}\, \alpha\, \eta \tag{2.117}$$

where

$$\begin{aligned} J &\propto e^{-B/E_{ox}} \\ \alpha &\propto e^{-H/E_{ox}} \end{aligned} \tag{2.118}$$

where $Q_{critical}$ is the critical charge density, J is the Fowler-Nordheim tunneling current, t_{BD} is the time to oxide breakdown, α is the hole-generation coefficient, and η is the hole-trapping efficiency (constant). Based on experimental data, the time to breakdown has been shown to be an exponential function of reciprocal of electrical field (E_{ox}) [Moazzami 1988, Lee 1988]:

$$\begin{aligned} t_{BD} &= \tau_0\, e^{G/E_{ox}} \\ &= \tau_0\, e^{G\, X_{ox}/V_{ox}} \end{aligned} \tag{2.119}$$

where τ_0 is the intercept of the $\ln(t_{BD})$ versus $1/E_{ox}$ plot, G is the slope of the $\ln(t_{BD})$ versus $1/E_{ox}$ plot ($G = B+H$, in Equation (2.118)), X_{ox} is the oxide thickness, and V_{ox} is the voltage across the oxide. In the case of defective oxides, the defects are modeled as localized oxide thinning. The electric-field dependence of time to breakdown for defective oxides is modeled as [Lee 1988]:

$$t_{Bd} = \tau_0\, e^{G\, X_{eff}/V_{ox}} \tag{2.120}$$

where X_{eff} is the effective oxide thickness at the weakest spot in the oxide. This concept is also used to model asperities at the interface and localized areas having modified chemical composition, which may increase the charge-trapping rate or reduce the barrier height at the silicon/silicon dioxide (Si/SiO_2) interface. The natural logarithm of time to breakdown, $\ln(t_{BD})$, is a linear function of $1/E_{ox}$, and non-linear function of E_{ox} [Moazzami 1988, Lee 1988]. The electric-field acceleration factor is defined as the tangential slope of the $\log_{10}t_{BD}$ versus E_{ox} plot [Lee 1988]:

$$\gamma = -\frac{d(\log_{10}(t_{BD}))}{dE_{ox}} = \frac{G}{(\ln 10)\ (E_{ox})^2}\left(\frac{decades}{MV/cm}\right) \tag{2.121}$$

where γ is the electric field acceleration factor, t_{BD} is the time to oxide breakdown, E_{ox} is the electric field across the oxide, and G is the slope of the $\ln(t_{BD})$ versus $1/E_{ox}$ plot.

Recent studies have modeled the pre-exponential term, τ_0, in Equations (2.119) and (2.120) as an exponential function of temperature with an activation energy E_b [Moazzami 1989, Moazzami 1990]:

$$\tau_0(T) = \tau_0\, e^{-\frac{E_b}{k}\left(\frac{1}{T}-\frac{1}{300}\right)} \tag{2.122}$$

where τ_0 is the room temperature value of the pre-exponential, $\tau(T)$; E_b is the activation energy of the pre-exponential, $\tau(T)$; and k is Boltzmann's constant (8.617×10^{-5} eV/K). The slope of the plot of $\ln(t_{BD})$ versus $1/E_{ox}$ G, is also modeled as a Taylor expansion of a temperature exponential [Moazzami 1989, 1990]:

$$G(T) = G\left(1 + \frac{\delta}{k}\left(\frac{1}{T} - \frac{1}{300}\right)\right) \tag{2.123}$$

where

$$\delta = \frac{k}{G}\frac{d\ G(T)}{d\ (1/T)} \tag{2.124}$$

and G represents the room temperature value. Moazzammi et al. represented G by Equation (2.124) to allow t_{BD} to follow the Arrhenius relationship [1989]. The time to breakdown is thus represented by an apparent activation energy represented as follows:

$$t_{BD}(T) = \tau_0 e^{\frac{GX_{ox}}{V_{ox}}\left(1 + \frac{\delta}{k}\left(\frac{1}{T}-\frac{1}{300}\right)\right)-\frac{E_b}{k}\left(\frac{1}{T}-\frac{1}{300}\right)}$$

$$t_{BD}(T) \propto e^{\frac{E_{shd}}{kT}} \tag{2.125}$$

where E_{shd} is the apparent activation energy represented by

$$E_{tbd} = \frac{G}{E_{ox}} \frac{X_{eff}}{X_{ox}} \delta - E_b \tag{2.126}$$

The following values for E_b and were δ determined from experimental data:

$$\begin{aligned} &\delta = 0.0167\ eV && \text{for} \quad 25^\circ C < T < 125^\circ C \\ &E_b = 0.28\ eV \\ &\delta = 0.024\ eV && \text{for} \quad T > 150^\circ C \\ &E_b = 0.28\ eV \end{aligned} \tag{2.127}$$

Thermodynamic Models for TDDB: McPherson proposed a thermodynamic model based on the assumption that when the dielectric breaks down, it undergoes an irreversible phase transition that transforms the material from an insulating phase to a conducting phase [1985]. The driving force for this transformation is the difference between the free energies of the conducting phase and of the insulating phase. The rate at which the reaction occurs is controlled by the free energy of activation associated with the growth of the conductive poly filament. McPherson represented a dielectric stored at a fixed field by a reaction rate constant, k:

$$k \propto \exp\left(\frac{-\Delta G^*}{K_B T}\right) \tag{2.128}$$

where ΔG^* represents the free energy if activation associated with the breakdown processes. By treating the components as reactants and the broken-down components as reaction products, the time to failure of the dielectric is represented by McPherson as

$$T_F \propto \frac{1}{k} \propto \exp\left(\frac{\Delta G^*}{K_B T}\right) \tag{2.129}$$

where T_F is the time to failure, k is the rate constant, ΔG^* represents the free energy if activation is associated with the breakdown process, k is Boltzmann's constant (8.617×10^{-5} eV/K), and T is the steady-state temperature.

The internal energy, E, of the dielectric under applied field stress is represented as

$$E = E(S,V,N,P) \tag{2.130}$$

where S represents the entropy of the system, V is the dielectric volume, N is the number of dipoles induced and/or oriented, and P is the dielectric polarization. The Gibbs free energy is obtained from internal energy, using the Legendre transformation

$$\begin{aligned} G(T,E,\mu,p) &= E - \left(\frac{\partial E}{\partial S}\right)_{V,N,P} - \left(\frac{\partial E}{\partial V}\right)_{S,N,P} - \left(\frac{\partial E}{\partial N}\right)_{S,V,P} - \left(\frac{\partial E}{\partial P}\right)_{S,V,N} \\ &= E - TS + pV - \mu M - EP \\ &= H_o - TS - \mu N - EP \end{aligned} \tag{2.131}$$

where H_o is the enthalpy of the dielectric. The Gibbs free energy is expressed in terms of intensive parameters including temperature, T; electric field, E; chemical potential, μ; and pressure, p (constant during dielectric stressing). On rearranging,

$$-TS - EP - \mu N = K_B T f(T) g(E) h(\mu) \tag{2.132}$$

where f, g, h, are functions of T, E, and μ respectively. Using thermodynamic relationships, the entropy, dielectric volume, and number of dipoles can be characterized by

$$S = -\left(\frac{\partial G}{\partial T}\right)_{E,\mu} = K_B g h\left(f + T\frac{df}{dT}\right) \tag{2.133}$$

$$P = -\left(\frac{\partial G}{\partial E}\right)_{T,\mu} = -K_B T f h \frac{dg}{dE} \tag{2.134}$$

$$N = -\left(\frac{\partial G}{\partial \mu}\right)_{T,E} = -K_B T f g \frac{dh}{d\mu} \tag{2.135}$$

Substituting the thermodynamic relationships into the above equation for Gibb's free energy,

$$\frac{T}{dT}\frac{df}{F} + \frac{E}{dE}\frac{dg}{g} + \frac{\mu}{d\mu}\frac{dh}{h} = 0 \tag{2.136}$$

Solving the above equation,

$$G(T,E,\mu) = H_o + K_B T \sum_m \sum_n \frac{C_{mn} E^n \mu^{m-n}}{T^m} \tag{2.137}$$

Considering the linear terms, McPherson represented the Gibbs free energy as

$$\begin{aligned} \Delta G^* &= \Delta H_O^* + K_B T \left(\frac{C_{01}}{\mu} + \frac{C_{11}}{T}\right) S \\ &= \Delta H_O^* + K_B T \left(B + \frac{C}{T}\right) S \end{aligned} \tag{2.138}$$

where ΔH_o^* is the change in enthalpy required to activate the poly filament growth at breakdown, B and C are constants, $S = E_B - E_S$, E_B is the breakdown strength of the dielectric, and E_S is the stressing in the dielectric. Thus,

$$TF(f\%) = Ae^{\left(\Delta H_O^* / K_B T\right)} e^{[\gamma(T)S]} \tag{2.139}$$

where the field acceleration parameter, γ, is the steady-state temperature-dependent parameter given by

$$\gamma = B + \frac{C}{T} \tag{2.140}$$

The effective activation energy of the field is given by

$$(\Delta H)_{eff} = \Delta H_o^* + K_B C S \tag{2.141}$$

Empirical Models for TDDB: Anolick [1981], Crook [1979], and Berman [1981] have proposed models to predict the time to failure based on these parameters. Secondary effects - especially dielectric thickness, electrode shape, materials, and other processing parameters - may also affect the dielectric breakdown mechanism. Anolick and Nelson [1979] modeled the time to failure as

$$t_f(F) = Ae^{\Delta H/kT}e^{\gamma(V_B(F)-V_A)} \quad (2.142)$$

where $t_f(F)$ is the time to failure for F percent of the population, γ is the voltage form factor (determined by life testing), ΔH is the activation energy, k is Boltzmann's constant, T is steady- state temperature, $V_B(F)$ is the breakdown voltage for F percent of the population, V_A is the applied voltage, and A is a constant. The following table compares various models of time- dependent dielectric breakdown.

Table 2.4 Comparison of Various Time Dependent Dielectric Breakdown Models

Reference	Oxide Thickness	Experimental Conditions	Observations	Model Predictions
Anolick, Nelson 1979	700 Å	E_s = 1.3 MV/cm E_B - E_s = 7 MV/cm	$(\Delta H)_{50\%}$ = 2.1 eV $\gamma = B + \frac{C}{T}$	$(\Delta H)_{50\%}$ = 1.8 eV $\gamma = B + \frac{C}{T}$
Crook 1979	1100 Å	E_s = 3.5 MV/cm E_B - E_s = 3 MV/cm	$(\Delta H)_{50\%}$ = 0.3 eV γ = 7 @ 25°C	$(\Delta H)_{50\%}$ = 0.34 eV γ = 6 @ 25°C
Berman 1981	≥400 Å	linear ramp	$(\Delta H)_{50\%} = 0.29 (E_B - E_s)$ $\gamma = -5.4 + \frac{0.29}{T}$	$(\Delta H)_{50\%} = 0.29 (E_B - E_s)$ $\gamma = -5.4 + \frac{0.29}{T}$
Hokari 1982	100 Å	E_s = 5 -7 MV/cm E_B - E_s = 5 MV/cm	$(\Delta H)_{50\%}$ = 1.0 eV @ 6 MV/cm γ = 1.7 @ 250°C	$(\Delta H)_{50\%}$ = 1.0 eV @ 6 MV/cm γ = 1.5 @ 250°C
McPherson 1985	100 Å	E_s = 6 - 8 MV/cm E_B - E_s = 3 - 5 MV/cm	$(\Delta H)_{50\%}$ = 0.3 - 1.0 eV $\gamma = B + \frac{C}{T}$	$(\Delta H)_{50\%}$ = 0.3 eV $\gamma = B + \frac{C}{T}$

Time-dependent dielectric breakdown has been a significant failure mechanism in

metal-gate MOS integrated circuits, silicon-gate transistors and integrated circuits with two or more levels of polysilicon, and circuits with trench capacitors. The dielectric breakdown phenomenon has also been shown to be an important factor affecting the early life of dynamic memory devices [Barrett 1978]. TDDB is a function of voltage stress in thin-gate oxides, and also a function of temperature (Figure 2.18). TDDB has both a dominant voltage dependence and a weak temperature dependence. Typically, TDDB has a very low thermal activation energy (say 0.3 eV) but a very large voltage acceleration 10^7 /megavolt/cm [Crook 1978, 1979, Schnable 1988]. The activation of TDDB is a function of stressing

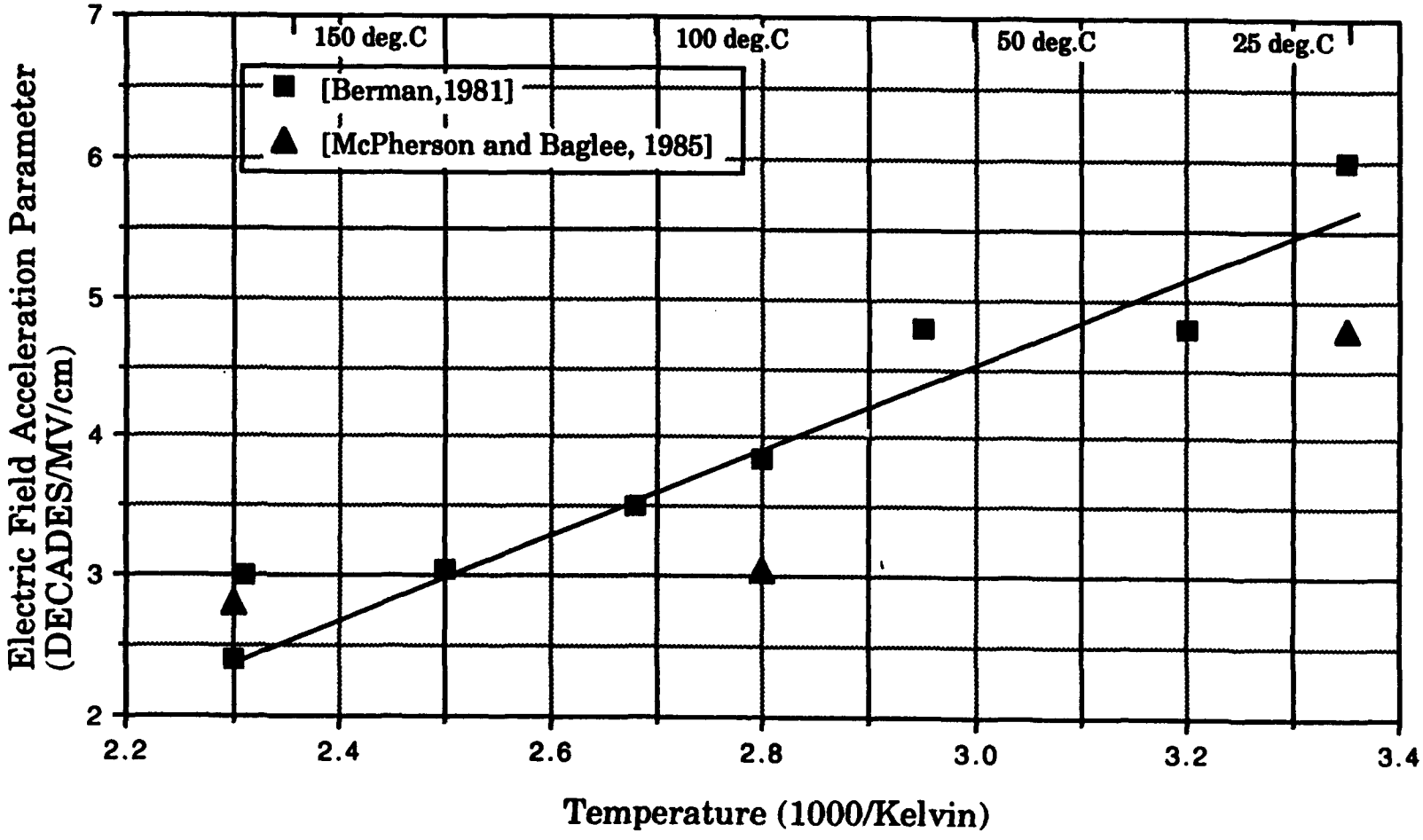
the electric field. The field acceleration is itself a function of temperature [McPherson 1985]. The apparent activation energy of TDDB decreases from 1eV at low field stressing (E_b-E_s > 5 MV/cm) to 0.3 eV at higher fields (E_b-E_s < 3 MV/cm) (where E_b is the dielectric breakdown strength and E_s is the stressing electric field). The field acceleration also reduces from 6 decades/MV/cm at 25 °C to 2 decades/MV/cm at 150 °C [McPherson 1985] (see Figure 2.19). The projected failure rate due to time-dependent dielectric breakdown under temperature stress was found to be too low to be of any importance for 10V and 55°C. At 10V and 200°C operation, the projected lifetime was 30 x 10^6 years, which represents a failure rate of 10^{-2} failures in 10^9 years [McPherson 1985, Boyko 1989, Swartz 1986]. For this reason, device screening procedures involve stressing the devices at higher voltages and room temperature, rather than at normal biases and higher temperatures [Crook 1978, 1979, Schnable 1988].

2.4.3 Electrical Overstress

Electrical overstress occurs when a higher-than-rated voltage or current induces a hot-spot temperature beyond specifications for short periods of time [Alexander 1978, Canali 1981, Smith 1978]. Hot-spot development typically occurs at a semiconductor junction as the current flow increases to accommodate the additional stress in the device. As the junction heats up, the increased temperature encourages even greater current flow, as the silicon resistance lowers at higher temperature; this in turn further heats the junction. The fundamental cause of failure is joule heating due to power dissipation along current-conducting paths. If the material reaches its melting temperature or its eutectic temperature, permanent damage may result. In a typical device, the greatest power dissipated per unit volume is either in the depletion region of the junction or in the lightest doped material. The temperature rises due to power dissipation, resulting in decreased silicon resistivity.

Runayan [1965] plotted the resistivity of silicon as a function of temperature for a variety of doping concentrations. Silicon initially exhibits a positive temperature coefficient of resistivity but reaches a peak value in the neighborhood of 160°C, and thereafter exhibits a large negative temperature coefficient of resistivity. As the temperature of a region rises, the initial increase in the resistance of the region tends to spread the current to the cooler region (Figure 2.20). If the situation continues, the hot-spot temperature may exceed the intrinsic temperature of silicon, beyond which the resistivity of silicon decreases greatly. This allows more current to pass through the hot spot, further increasing the temperature, and resulting in thermal runaway. That is, the temperature of the hot spot rises suddenly, while

Figure 2.19 The Electric Field Acceleration Parameter is inversely dependent on temperature [McPherson and Baglee, 1985]



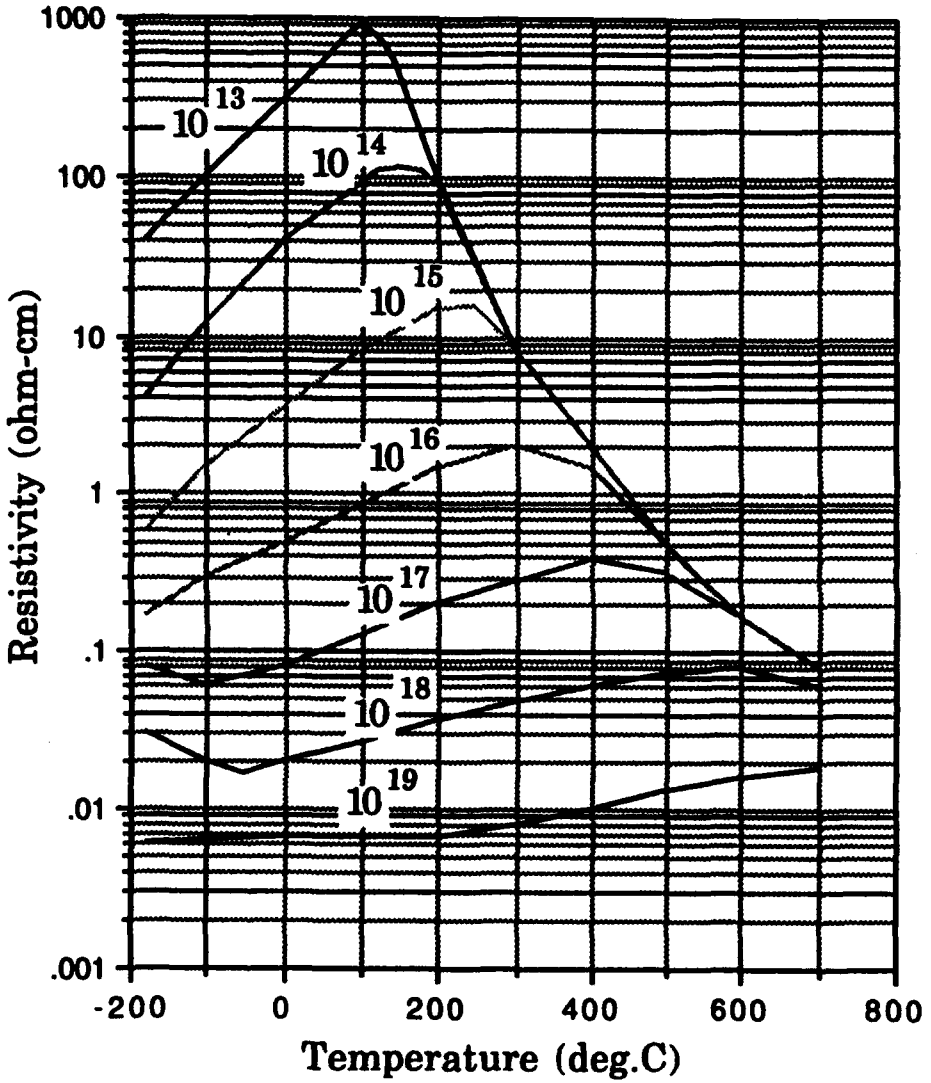


Figure 2.20 Silicon resistivity versus temperature. [Runayan, 1965]

the resistance of the device drops. The process continues until the silicon in the hot spot melts, destroying the silicon crystal structure. If the electrical transient continues, the interconnects melt as well. If the transient is of high voltage, an electrical arc may occur when the metallization opens. The temperature in the vicinity of the arc can cause the metallization to vaporize. The energy required to raise the junction to an unstable temperature can be calculated using a power model [Pancholy 1978].

2.5 TEMPERATURE DEPENDENCIES OF FAILURE MECHANISMS IN THE DEVICE

2.5.1 Ionic Contamination

Ionic contamination causes reversible degradation phenomena, such as threshold voltage shift and gain reduction, due to the presence of mobile charge ions within the oxide or at the device-oxide interface, typically at temperatures above 100°C [Schnable 1988, Brambilla 1981, Johnson 1976].

P-channel devices are less sensitive to ionic contamination than n-channel devices. Figure 2.21 shows the variation of ionic current versus temperature in devices with Na^+ and K^+ ion implants (the curves have been generated using TSIC technique[1]). The ionic current increases until 100°C for Na^+ ions, and decreases to a negligibly low value for temperatures higher than 200°C. The K^+ ion, on the other hand, shows two peaks in ionic current at temperatures in the neighborhood of 100°C and 300°C (Figure 2.21). The ionic current due to mobile ions is thus a complex function of steady-state temperature [Hillen 1986, Boudry 1979, Nauta 1978, Derbenwick 1977].

The mobility of the ions is temperature-dependent [Hemmert 1980, 1981]. Consequently, high-temperature storage bake and exposure to high temperature during burn-in screen out ionic contamination failures [Hemmert 1980, 1981, Bell 1980]. In particular, the position of ionic charges relative to the silicon-silicon dioxide (Si-SiO_2) interface greatly influences the effectiveness of altering the threshold voltage, V_T. A uniformly distributed contaminant (Na^+) within the oxide is redistributed to the silicon (Si) channel surface due to the influence of an electric field, E, and thermal activation energy. The change in threshold voltage as a function of steady-state temperature, T, has been modeled by Wager [1984]:

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[1] Three techniques are generally used to measure the ionic current due to mobile charges versus temperature. These include BTS (Bais temperature stress), TSIC (Thermally stimulated Ionic Current), and TVS (Triangular Voltage Sweep).

$$\Delta V_T \propto E^{1/2} t^{1/2} e^{-\Delta H/KT} \tag{2.143}$$

where E is the electric field, t is the time under bias, ΔH is the activation energy, and K is the Boltzmann constant. Higher chip temperature would result in more rapid ΔV_T change and shorter times to saturation [Wager 1984].

N-channel MOSFETs are covered with phosphosilicate glass films to stabilize the threshold voltage against changes resulting from ionic contaminants (sodium). Hemmert investigated the temperature bias kinetics for sodium ion drift in phosphosilicate glass [Hemmert 1980, 1981]. Microelectronic devices may be subject to a variety of defects; one such defect is exposed gate oxide resulting from extraneous etched holes contiguous to the gate that subject the phosphosilicate glass film to either a high local ionic concentration or physical damage. The temperature at which ionic drift occurs in defective devices is not as large as in non-defective devices. Hemmert conducted experiments to measure ionic stability on a 1.5-mm MOS consisting of gate oxide, phosphosilicate glass film, and aluminum-copper (Al-Cu) metallurgy. He found that below 250°C, the plot of voltage versus temperature shows a polarization plateau that represents saturation PSG polarization voltage. The activation energy, ΔH, was 2.0 eV. This value is uncharacteristically high, compared to the value usually reported for sodium-related failure mechanisms (ΔH=1.0 eV); the cumulative percent defect predictions were found to be more accurate assuming a temperature-dependent defect level. In the temperature range of 250-350°C, flatband voltage shifts occurred. This temperature, called the break temperature, occurs when the contribution of flatband voltage shift to ionic drift and to polarization are equal. The maximum variation in the flat-band voltage is related to the mobile charge by the relation

$$Q_m = C_{ox} \Delta V_{FB} \tag{2.144}$$

where c_{ox} and Q_m represent the oxide capacitance and the mobile charge per unit area. The threshold voltage, V_T, and the flatband voltage, V_{FB} are related by the equation

$$V_T = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \tag{2.145}$$

where ϕ_F is the difference in the Fermi level and the intrinsic Fermi level in the bulk of the semiconductor. It is evident that the threshold voltage depends on the

flatband voltage. Thus, the usual assumption that the defect level is temperature-independent was found to be invalid.

A common characteristic of contamination failures is reversibility under high temperatures (in the neighborhood of 150 to 200°C), which partially or fully restores device characteristics [Hemmert 1980, 1981, Bell 1980]. However, this simply reflects a disordering of charge accumulations resulting from ion mobility and applied bias. The problem of ionic contamination has been solved to a large extent by the use of high-purity materials and chemicals for processing, use of HCl during oxidation [Robinson and Heiman 1971], and use of phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG) over the polysilicon to getter the ions [Schnable 1988]. Passivation layers can provide additional protection against the ingress of alkali ion contamination in completed devices [Schnable 1988].

2.5.2 Second Breakdown

Second breakdown is the transition to a state of higher conductance in a reverse-biased avalanching semiconductor junction. Second breakdown occurs predominantly in bipolar devices when the bias current density reaches a threshold value; in this case, the operating temperature in some region of the pn junction becomes high enough that thermally generated carriers can take over the conduction process. The avalanche is thus thermally quenched, and second breakdown occurs. A negative temperature coefficient of resistance, associated with thermally generated current, results in the current constricting and flowing through a narrow region in the junction, where the temperature rises significantly. If the temperature of the constriction is higher than T_ρ, (the temperature at which the resistivity of semiconductor materials is the highest), the high-power density region at the perimeter of the constriction will heat up, becoming intrinsic, and the constriction will elongate into the ohmic region. If the constriction temperature is less than T_ρ, the constriction will not extend itself into the ohmic region, and the current will flow through the constriction in the junction and fan out. Second breakdown is a limiting phenomenon in power transistors that are switched in the presence of inductive loads, and typically involves three stages [Budenstein 1972, Sunshine 1970, Schafft and French 1966, Reich and Hakim 1966, Chiang and Lauritzen 1970, Thornton and Simmons [1958]:

- nucleation of filament;
- growth of a relatively broad filament across the high resistivity region;
- growth of a second filament interior to the first, in which material is in molten state.

While, nucleation and growth of filament are non-destructive processes, formation of melt is damaging and irreversible. Typically, nucleation is accompanied by a negligible voltage drop. In reverse-biased diodes, the p-n junction is the hottest region and the place where the filaments nucleate. The increase in the temperature of the p-n junction increases the avalanche voltage, due to decrease in the collision ionization coefficients. However, as the temperature rises, the reverse saturation current decreases rapidly. Total saturation current is insensitive to the size of reverse saturation current until the latter is eight-tenths of the former; then the avalanche voltage drops to zero, and the reverse saturation current density equals the total current density, resulting in the initiation of filamentation [Budenstein 1972, Sunshine 1970, Chiang and Lauritzen 1970].

Filament growth involves the development of a moderately hot filament across the high- resistivity region. When the broad filament completely bridges the high resistivity region, melt initiates. Formation of melt involves the development of a melt channel through the hot central portion of the broad filament. The melt channel alters the device irreversibly, the degree of degradation depending on the size and location of melt. Broad filaments typically range from 25 to 50 μm across, while the melt channel, at currents near its formation threshold, is about 1 μm in diameter. Growth and formation of melt, however, is accompanied by appreciable voltage drop. Junction nucleation occurs when the reverse saturation current density at the local site on the junction becomes equal to the total current density at that site [Budenstein 1972, Sunshine 1970, Chiang and Lauritzen 1970]. Typically there is a time difference between the application of the high current pulse and second breakdown, called the delay time.

Second breakdown is characterized by two different failure mechanisms: forward second breakdown, and reverse second breakdown. Both forward-and reverse-bias second breakdown of diodes is accompanied by current filamentation and a high current transition. In reverse bias, the filament typically starts at the junction and reaches into the high-resistance side of the junction to the electrode. In forward bias, the filament typically starts well within the interior of the high-resistance region. The transition from avalanche to second breakdown of the base-collector junction occurs at a lower V_{CE} when the emitter is forward-biased than when it is reverse-biased. Second breakdown damage manifests itself in the form of changes in I-V characteristics due to resistive shorts of one or both transistor junctions. The critical condition for filament formation occurs when the temperature in the high-resistance side of the junction reaches the value at which the resistivity of the semiconductor material is at maximum. Filaments are formed during forward and reverse bias at the same current levels. The onset of negative resistance occurs before the filament is clearly distinguishable from its

surroundings. The failure mechanism of second breakdown is characterized by an abrupt reduction in voltage and increased localized current density. The consequence is high temperature and permanent device damage or degradation [Budenstein 1972, Sunshine 1970, Chiang and Lauritzen 1970, Beatty 1976, Chen 1983, Hower 1970, Hu 1982].

Forward Second Breakdown. Forward second breakdown is typically a result of thermal runaway at a point in the transistor. Current density and temperature increase jointly till thermal runaway occurs. A power transistor can be considered an aggregate of many elementary transistors that operate under different conditions. When a power pulse is applied to the transistor, the junction temperature rises. Since the resistivity of the silicon increases with temperature, the temperature rise causes the current to increase:

$$dP_1 = V_{CE} dI_C \tag{2.146}$$

The increase in temperature causes an increase in the power dissipation:

$$dP_2 = \frac{dT}{R_{th}} \tag{2.147}$$

If $dP_1 < dP_2$, a thermal equilibrium is reached. If, on the contrary, $dP_1 > dP_2$, the temperature and current increases enhance each other and thermal runaway occurs, causing transistor destruction.
Usually temperatures above 160°C are required to cause device failure due to second breakdown. The major cause of device destruction is localized heating. Second breakdown has also been found to occur in vertical power MOSFETs.

Reverse Second Breakdown. Reverse second breakdown is an internal phenomenon that occurs in power transistors during switching operations on an inductive load, and is characterized by a precipitous drop in voltage and a rapid increase in current. The second breakdown voltage increases mildly with an increase in temperature in the range of 25°C to 150°C. The breakdown voltage increases from 650v to 680v when the temperature increases from 25°C to 150°C [Beatty 1976].

Mathematical Model for Second Breakdown: Budenstein's model [1972] assumes that the formation of a melt channel within the broad filament that spans the high-resistivity region marks the initiation of second breakdown. The model assumes that:

- the central portion of the filament is at the melting point of the silicon and the filament grows radially, while keeping a constant length. This allows the use of a cylindrical geometry for the heat transfer problem.
- the filament is about 1 μm in diameter at the end of transition for current amplitudes close to the threshold for filamentation.
- the filament is in parallel with a fixed resistance R_b, of the remainder of the device.

The power dissipated in the filament is equal to the rate that the energy is absorbed in the latent heat of fusion plus the rate at which the energy is lost by conduction through the boundary surface of the filament:

$$P_f = \frac{d(LM_f)}{dt} + CA_s \tag{2.148}$$

where P_f is the electrical power dissipated in the filament, L is the latent heat of fusion for the semiconducting material, M_f is the mass of the molten filament (Equation (2.149)), C is the heat transfer coefficient (heat flow per unit time per unit area), A_s is the lateral surface area of the filament, and

$$M_f = DH\pi r^2 \tag{2.149}$$

$$R_f = \frac{\rho_f H}{\pi r^2} \tag{2.150}$$

$$A_s = 2\pi rH \tag{2.151}$$

$$R_b = \frac{\rho H}{A} \tag{2.152}$$

$$P_f = I_f^2 R_f = \frac{I^2 R_b R_f}{(R_b + R_f)^2} \tag{2.153}$$

Substituting Equations (2.155) to (2.159) into Equation (2.154),

$$\frac{dr}{dt} = \frac{C}{LD}\left(\frac{I^2 R_b \rho_f}{2C} \frac{r}{(R_b \pi r^2 + \rho_f H)^2} - 1\right) \tag{2.154}$$

where r is the radius of the filament, C is the heat transfer coefficient, L is the latent heat for fusion of the semiconducting material, D is the mass density of the semiconducting material, I is the total current (sum of the currents through the filament and the semiconductor device, ρ_f is the resistivity of the filament, H is the length of the filament. The steady-state condition ($dr/dt = 0$) is assumed to be reached when power dissipated in the filament is at a maximum -that is, when $R_f = R_b$ (obtained by differentiating Equation (2.153) with respect to R_f). The power dissipated in the filament in a steady-state condition is given by

$$P_f' = CA_s' = \frac{V_f'^2}{R_f} \tag{2.155}$$

where the primes represent the steady-state values of the respective quantities. At steady-state (dr/dt = 0), the total threshold value of current for filamentation is

$$I_t = 2\sqrt{2C}\left(\frac{\rho_f H^3}{R_b^3}\right)^{1/4} \tag{2.156}$$

Substituting Equation (2.151) and (2.152), into Equation (2.155) and using the steady-state condition, $R_b = R_f$,

$$J_t = K\rho^{-3/4}, \text{ where } K = 2\sqrt{2C}\rho_f^{1/4} A^{-1/4} \tag{2.157}$$

where J_t is the threshold current density for filamentation, ρ is the resistivity of the semiconducting material outside the filament, and A is the area of the remainder of the device.

2.5.3 Surface-Charge Spreading

Surface-charge spreading, largely observed in MOS and memory devices, involves the lateral spreading of ionic charge from the biased metal conductors, along the oxide layer or through moisture on the device surface [Edwards 1982, Blanks 1980, Stojadinovic 1983]. An inversion layer outside the active region of the transistor is formed due to the charge, creating a conduction path between the two diffused regions or extending the p-n junction through a high-leakage region, resulting in leakage currents between neighboring conductors. The rate of charge spread increases with temperature. Surface-charge spreading failure, a wear-out mechanism, is usually observed at temperatures around 150°C to 250°C [Lycoudes 1980]. There are no existing physics-of-failure models to predict surface-charge spreading failures.

2.6 TEMPERATURE DEPENDENCIES OF FAILURE MECHANISMS IN THE DEVICE OXIDE INTERFACE

2.6.1 Hot Electrons

Hot electrons, or holes, are charge carriers that acquire energies from very high electric fields in excess of those that would be indicated by lattice or ambient temperature. Hot electrons are a phenomenon largely prevalent in high-density, small geometry, MOS memory devices because of small conduction channels and high voltages. It is accelerated at temperatures below 0°C [Stojadinovic 1983, Woods 1980]. Threshold voltage shifts or transconductance degradation can occur as renegade charge concentrations build up over time [Ning 1979]. Penetration of the oxide by hot electrons can lead to excess gate and substrate currents [Takeda 1983]. There are three possible mechanisms by which the electrons or holes are injected from silicon into the silicon dioxide (SiO_2) [Garrigues and Balland 1986]:

- *Direct tunnel emission*: Injection of electrons by direct tunneling is possible in thin oxides (< 100 Å) and large electric fields ($\epsilon_{ox} > 5 \times 10^5$ V cm^{-1}).
- *Field assisted tunneling*: Electrons of energy close to but less than the energy barrier at the silicon-silicon dioxide ($Si\text{-}SiO_2$) interface may tunnel through the triangular energy barrier resulting from field in the oxide. For larger electric fields, the energy bands of silicon are so slanted that direct tunneling can occur, regardless of oxide thickness (field emission or Fowler-Nordheim tunneling).
- *Injection over the barrier*: Electrons may gain high potential energy due to high electric fields present in the conduction channel and cross the potential barrier at the substrate-oxide interface. An electron in conduction band of silicon (Si)

can be injected over the energy barrier into the conduction band of silicon dioxide (SiO_2) if its energy ΔE is greater than the difference in the conduction band energies of the conduction bands in the silicon (Si) and silicon dioxide SiO_2.

Electron injection through field-assisted tunneling or injection over the barrier is possible by stimulating the electron thermally, optically, or with an electric field; field stimulation is the most common form of electron stimulation [Garrigues and Balland 1986].

Figure 2.22 shows the effect of ambient temperature on the hot carrier mechanism [Matsumoto 1981]. The temperature dependence of substrate current at fixed bias can have three origins: temperature-dependent channel current, temperature-dependent local electric field, and temperature-dependent ionization rate. The low field mobility follows -3/2 power dependence on the temperature for typical n-channel MOSFETs [Sze 1981]. The reduced mobility increases the saturation voltage, which lowers the maximum-channel electric field at fixed-drain bias and results in a lower substrate current [Ko 1980, Hu 1983]. Tam et al. [1983] proposed that the device degradation rate can be related to the substrate current by

$$\Delta V_t = C_1[C_2[I_s]^{\alpha}]^{\beta} \tag{2.158}$$

where C_1 is a structure-related factor, C_2 is a material-related factor, α is the energy factor (typically 2.9), and β is the factor from general kinetics (typically 0.6). The device degradation due to hot electrons very mildly decreases with the increase in temperature for temperatures between 20°C and 100°C, as shown in Figures 2.23 and 2.24 [Hsu 1984]. A plot of device lifetime as a function of temperature and substrate current is shown in Figure 2.25 [Hsu 1984]. A calculation of energy and proportionality factors in Tam's equation [1983] indicate that they are constant over the temperature range, suggesting that the physical mechanism for device degradation is the same over the temperature range 20°C to 100°C. The variation of lifetime versus substrate current for temperatures 20°C and 100°C, shown in Figure 2.25, indicates that hot-electron degradation is temperature-independent in this range.

The increase in the ambient temperature decreases the observed ΔV_T shift from the channel hot- electron effect. For a given device design, Matsumoto has described this behavior as [1981]:

$$\Delta V_T = AN_T(1-e^{-BN_{inj}}) \tag{2.159}$$

where N_T is the effective oxide-trap density, N_{inj} is the density of injected electrons, and A and B are constants. From the equation, it is evident that the hot-electron threshold voltage shift increases with both the electrons injected into the oxide and the availability of traps to capture the electrons. Both these quantities decrease with increasing temperature, giving rise to reduced threshold shift due to hot electron trapping at elevated temperatures [Matsumoto 1981].

The Lucky Electron Model: This model ignores the overall description of the hot-carrier energy distribution and focusses on the distribution tail corresponding to those electrons with sufficient energy to overcome the potential barrier. The lucky electron model accounts for the influence of the electric field profile in silicon, the oxide field, and the lattice temperature.

A free electron is injected into silicon dioxide (SiO_2) if it reaches the interface with a component of its momentum, normal to the surface, greater than a critical value, p_c, corresponding to the barrier energy, ϕ_{BS}. The probability of tunnel injection through the top of the barrier for an electron with momentum slightly lower than p_c is momentarily neglected. The electron can reach the interface with momentum p_c after travelling various possible trajectories. The trajectory consists of a series of free flights interrupted by various interactions that can be elastic or inelastic, during which the electron energy is modified by the electric field. The lucky electron model assumes that the most probable trajectories are those for which energy, ϕ_{BS}, is gained by the electron in the last free flight without any collisions before reaching the interface. The emission probability is thus close to

Figure 2.21 Influence of Temperature on Ionic Current due to Sodium and Potassium Ions [Hillen, 1986]

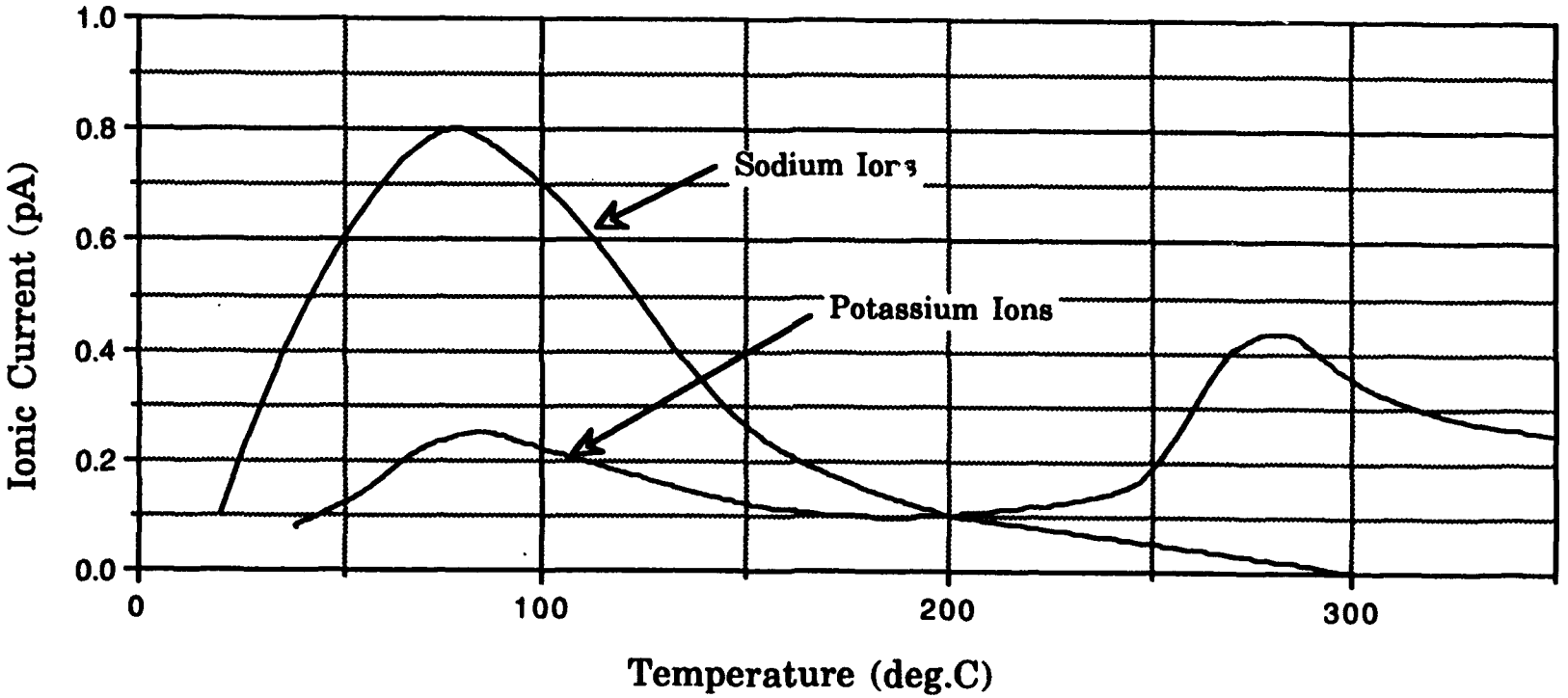


Figure 2.22 Change in threshold voltage due to hot electrons is much greater at lower temperature than at high temperatures. [Matsumoto, 1981]

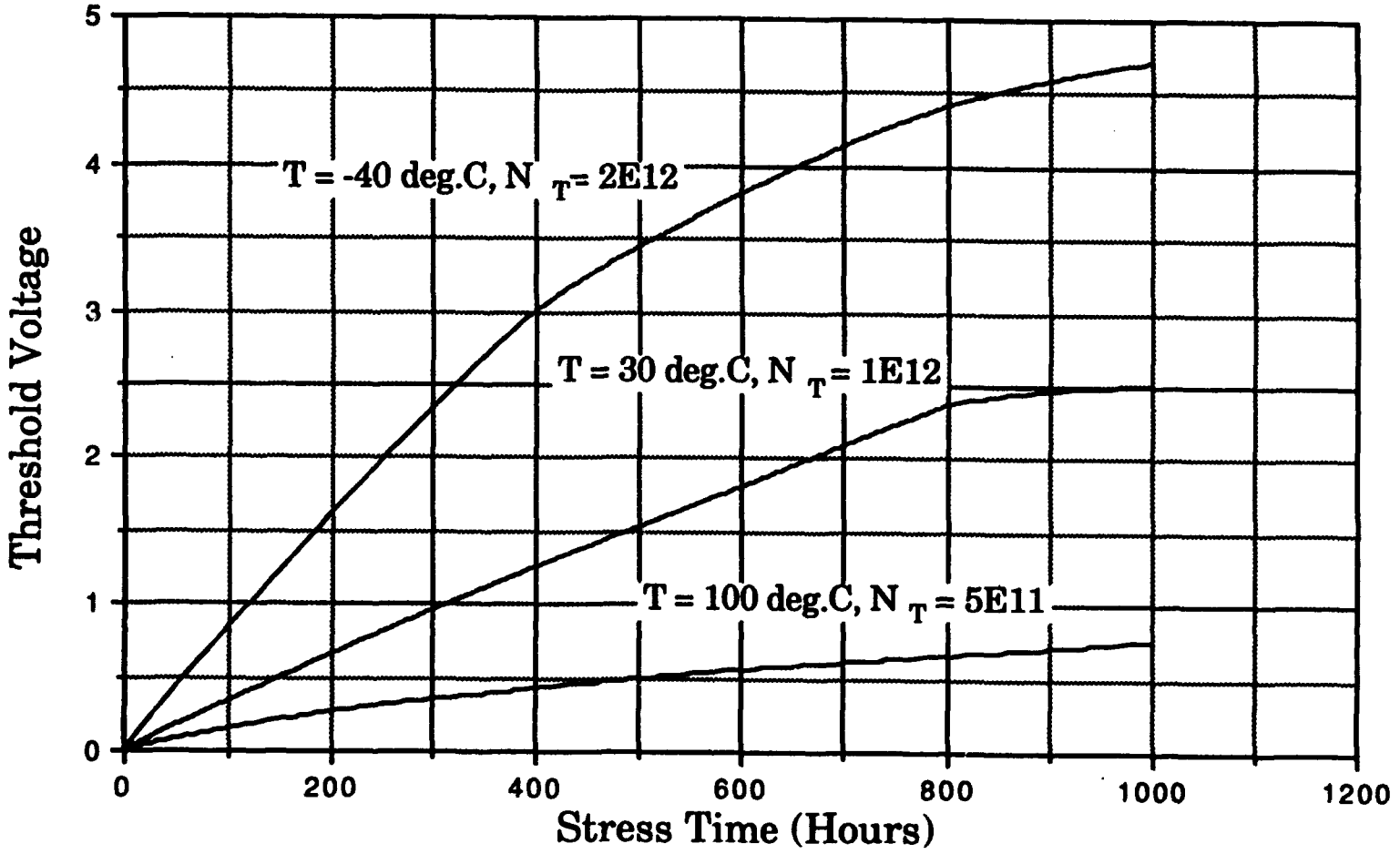


Figure 2.23 Substrate characteristics for a 5 μm device at 20 deg.C and 100 deg.C V_g = 3V and 7V, V_t = 0.9V [Hsu, 1984]; The variation in device characeristics between 20 and 100 deg.C indicates that degradation due to hot electrons is almost temperature independent in this range.

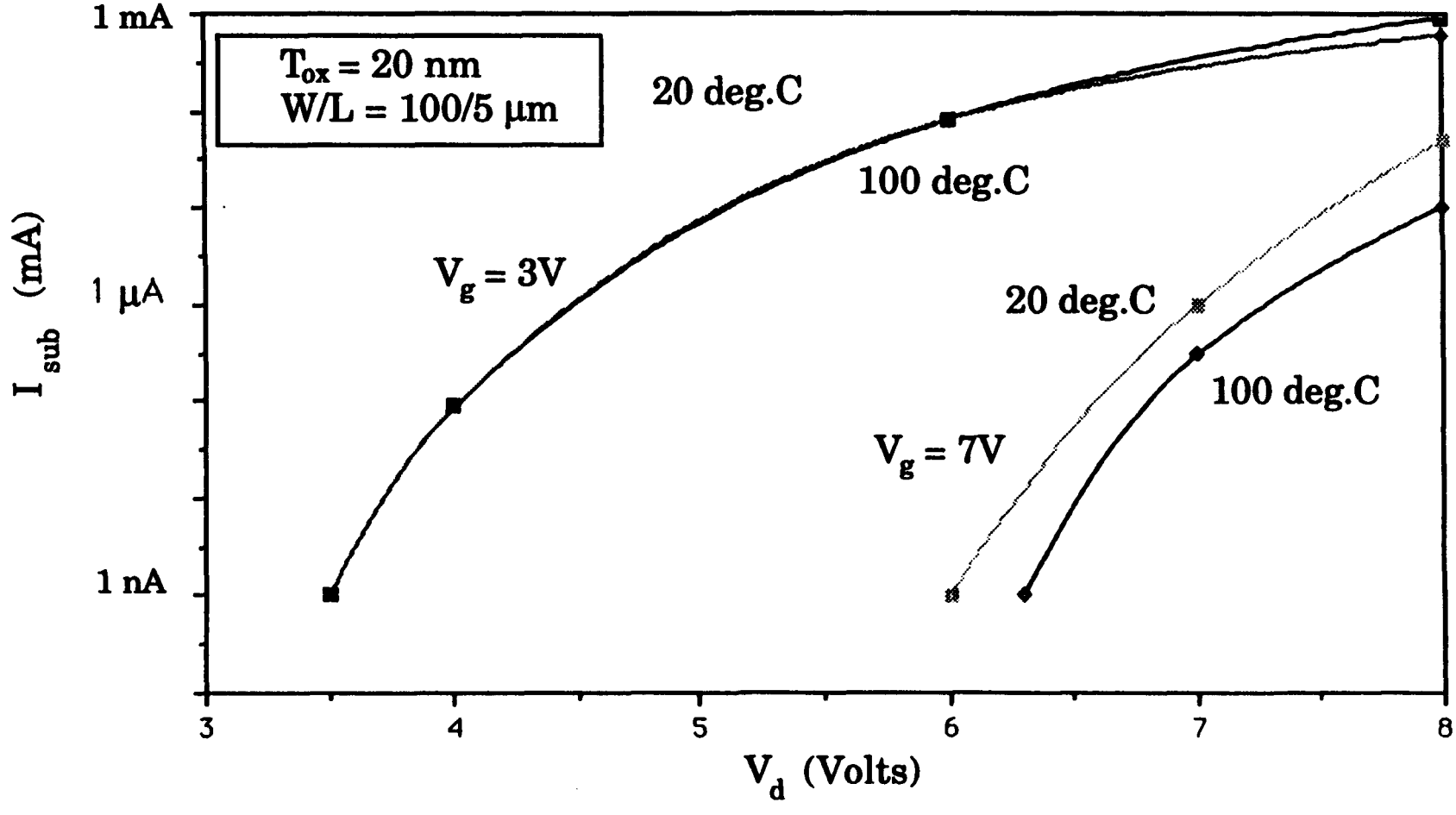


Figure 2.24 Drain characteristics for a 5 μm device at 20 deg.C and 100 deg.C V_g = 3V and 7V, V_t = 0.9V [Hsu, 1984]
The variation in device characteristics between 20 and 100 deg.C indicates that degradation due to hot electrons is almost temperature independent in this range.

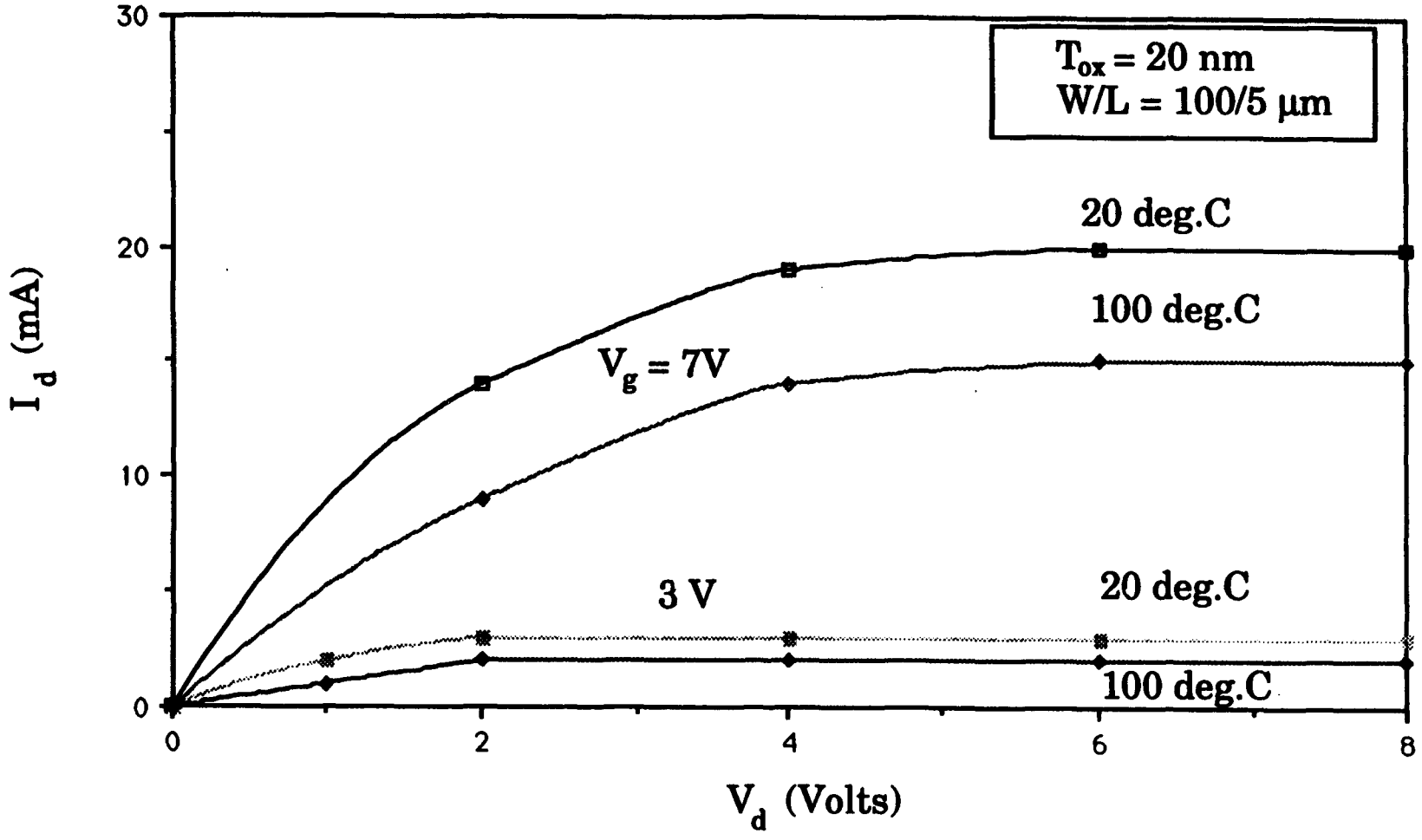
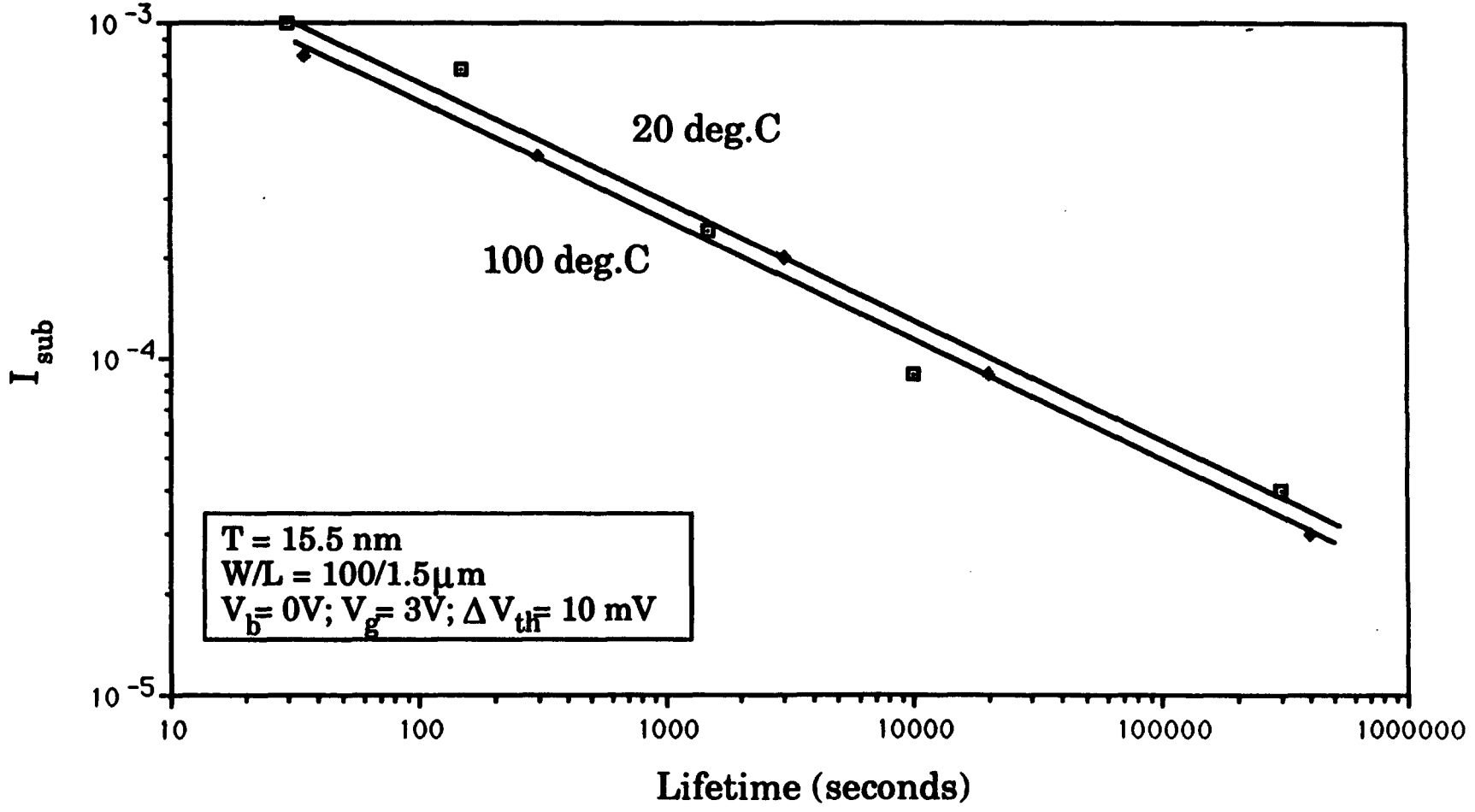


Figure 2.25 Substrate current dependence of device lifetime at 20 deg.C and 100 deg.C [Hsu, 1984]; The small variation in device lifetime for temperature variation between 20 deg.C and 100 deg.C clearly indicates that the degradation due to hot electrons is temperature independent in this range



the probability of the electron making such a trajectory. The minimum path length required to gain energy, before reaching the interface equals d, the horizontal distance between the top of the barrier and the lower edge of the conduction band. It is assumed that the emission probability for an electron that has collision within a distance, d, is negligible, irrespective of its previous energy. According to the lucky electron model, the emission probability of an electron is thus equal to its probability of travelling a distance greater than d without a collision [Ning 1977, Garrigues 1981]:

$$P_e = P_o e^{-\frac{d}{\lambda_o \tanh\left(\frac{E_a}{2KT}\right)}} \tag{2.160}$$

where

$$d = \sqrt{\frac{2\epsilon_{SC}\epsilon_o}{qN_A}}\left(\sqrt{\Psi_S} - \sqrt{\Psi_S - \frac{\Phi_{BS}}{q}}\right) \tag{2.161}$$

and P_e is the emission probability of an electron, P_o is a constant ($\approx$ 2.9 @ 300°K; 4.3 @ 77°K), d is the minimum path length of an electron required to attain critical energy ϕ_{BS}, T is the steady-state temperature, E_a is the activation for mean free-path length (0.063 eV), λ_o is a constant ($\approx$ 108 Å), λ is the electron mean free path between lattice interactions, K is Boltzmann's constant (8.617×10^{-5} eV/K or 1.38×10^{-23} J/K), ϵ_{SC} is the dielectric constant of the semiconductor (F cm^{-1}), ϵ_o is the free-space permittivity (8.85×10^{-14} F cm^{-1}), N_A is the concentration of acceptor doping atoms, q is the magnitude of electronic charge (1.6×10^{-19} Coulomb), Ψ_S is the surface potential (volts), and Φ_{BS} is the silicon-silicon dioxide ($Si\text{-}SiO_2$) barrier height for electrons, taking into account lowering due to the Schottky effect.

Table 2.5 Steady State Temperature Dependence of Device Failure Sites (normal operation is assumed at -55°C to 125°C) [Pecht, Lall, Hakim 1992]

Failure site	Failure mechanism	Dominant temperature dependence	Nature of steady state temperature dependence	References
wire	flexure fatigue	ΔT	Independent of steady-state temperature function under normal operation	[Gaffeny 1968], [Villela 1970], [Ravi 1972], [Phillips 1974], [Pecht 1989], [Harman 1974]
wirebond	shear fatigue	ΔT	independent of steady-state temperature	[Philosky 1973], [Pecht 1989], [Newsome 1976], [Philosky 1970, 1971], [Gerling 1984], [Khan 1986] [Pinnel 1972], [Feinstein 1979], [Pitt 1982]
	Kirkendall voiding	T	independent of steady-state temperature below 150°C; independent of steady-state temperature above lower temperatures ($T < 150°C$) in presence of halogenated compounds	[Newsome 1976], [Philosky 1970, 1971], [Gerling 1984], [Khan 1986] [Pinnel 1972], [Feinstein 1979], [Pitt 1982], [Khan 1986], [Villela 1971]
die	fracture	ΔT, ∇T	primarily dependent on temperature cycle	[Tan 1987], [Hawkins 1987]
die adhesive	fatigue	ΔT	independent of steady-state temperature under normal operation	[Chiang 1984], [Mahalingham 1984]
encapsulant	reversion	T	Independent of steady-state temperature below 300°C (glass transition for typical epoxy molding resin for plastic packages)	[Tummala 1989]
	cracking	ΔT	independent of steady state temperature (T) below the glass-transition temperature of the encapsulant; a ΔT, ∇T-driven mechanism.	[Nishimura 1987], [Fukuzawa 1985], [Kitano 1988]
package	stress corrosion	dT/dt	mildly steady-state temperature dependent under normal operation	[Tummala 1989]

	corrosion	dT/dt	only occurs above dew point temperature; mildly steady-state temperature dependent under normal operation	[Pecht 1990], [Commizalli 1980], [Inayoski 1979], [Sim 1979], [White 1969], [Schnable 1969]
	electromigration	∇ T, T	steady-state temperature dependent above 150°C	[Schnable 1988], [Ondureek 1988], [Oliver 1970], [Schwarzenberger 1988], [Chabra and Ainslie 1967], [Attardo 1972], [Danso 1981], [Black 1983], [Blair 1970], [Ghate 1981], [Partridge 1982], [LaCombe 1986], [Canali 1984], [Kinsborn 1978]
die metallization	hillock formation	T	Hillocks in die metallization can form as a result of electromigration or extended periods under temperature cycling conditions (thermal aging). Extended periods in the neighborhood of 400°C produce hillocks.	[LaCombe 1982], [Thomas 1983], [Amerasekera 1987]
	metallization migration	T	independent of steady-state temperature below 500°C	[Diagiacomo 1982] [Bart 1969], [Lane 1970]
	contact spiking	T	independent of steady-state temperature below 400°C	[Chang 1988], [Farahani 1987], [T.I. 1987] [DeChairo 1981], [Christou 1980, 1982], [Ballamy 1978],
	constraint cavitation	T	steady-state temperature dependent above 25°C	[Yost 1988, 1989]
die	electrical overstress	T	independent of steady-state temperature below 160°C(the temperature at which the coefficient of thermal resistance changes sign)	[Alexander 1978], [Canali 1981], [Smith 1978], [Runayan 1965], [Pancholy 1978]

device oxide	slow trapping	T	steady state temperature dependent above 175°C	[Nicollian 1974], [Woods 1980], [Gottesfeld 1984]
	electrostatic discharge	T	ESD voltage (resistance to ESD) reduces with temperature increase (from 25°C to 125°C); not a dominant mechanism in properly protected devices.	[Kuo 1983], [Hart 1980], [Moss 1982], [Amerasekera 1986, 1987], [Scherier 1978]
device oxide (contd.)	Time Dependent Dielectric Breakdown	T	steady-state temperature dependence is very weak; TDDB is a dominant function of voltage	[Anolick 1979], [Crook 1979], [Crook 1978], [Schnable 1988], [McPherson 1985], [Boyko 1989], [Swartz 1986], [Lee 1983]
device	Ionic Contamination	T^{-1}	steady-state temperature-dependent above 200°C	[Brambilla 1981], [Johnson 1976], [Hemmert 1980, 1981], [Bell 1980], [Wager 1984]
	Forward Second Breakdown	T	independent of steady-state temperature below 160°C	[Beatty 1976], [Chen 1983], [Hower 1970], [Hu 1982]
	Reverse Second Breakdown	T^{-1}	insignificant dependence of steady-state temperature; the breakdown voltage increases from 650v to 680v when the temperature increases from 25°C to 150°C	[Beatty 1976], [Chen 1983], [Hower 1970]
	Surface Charge Spreading	T	steady-state temperature dependent above 150°C	[Edwards 1982], [Blanks 1980], [Stojadinovic 1983], [Lycoudes 1980]
device substrate-oxide interface	Hot Electrons	T^{-1}	steady-state temperature dependence decreases above -55°C. Temperature-independent in range of 20°C to 100°C.	[Stojadinovic 1983], [Woods 1980] [Ning 1979], [Takeda 1983], [Matsumoto 1981], [Ko 1980], [Hu 1983], [Sze 1981], [Tam 1983], [Hsu 1984]

Table 2.6 T, ΔT, ∂T/∂t, ∂T/∂x Dependence of Failure Mechanisms and Failure Models in the Temperature Range -55°C to 125°C

Failure mechanism	Nature of temperature dependence
bondpad-substrate shear fatigue	$N_s = C_{p'} \tau_{max}^{-n_{p'}}$ $\tau_{max} = Q \Delta T$ $Q = \left(\frac{G_p \Delta T}{b_p Z}\right)\left[(\alpha_w - \alpha_s) - \frac{(\alpha_s - \alpha_p)}{\left(1 + \frac{E_s A_s}{E_p A_p}\right)(1 - \nu_s)}\right]$ Δ T-dependent, T-independent
constraint cavitation	$\log D_s = 5.07 - \frac{1.09x10^4}{(273+T)} + \frac{2.89x10^6}{(273+T)^2} - \frac{3.24x10^8}{(273+T)^3}$ T^{-1} for temperatures above 25°C
corrosion	$\tau_c = \left(\frac{K_1 K_2 K_3}{K_4}\right)\left[\frac{w^2 h n d F \rho}{4MVZ}\right]$ $K_4 = \frac{(RH_p)^n \exp(E_a/KT_p)}{(RH)^n \exp(E_a/KT)}$ ∂T/∂t dependent

die and substrate adhesion fatigue	$N_f = 0.5\left(\frac{\gamma_o}{\gamma_f}\right)^{\frac{1}{m}}$ $\gamma_o = \frac{L\lvert\alpha_s-\alpha_d\rvert\Delta T}{X}$ $N_f = 0.5\left[\frac{L_s(\alpha_s - \alpha_s)\Delta T}{h_m\gamma_f}\right]^{\frac{1}{c}}$ Δ T-dependent, T-independent
die fracture	$\Delta\sigma_{app} = 10^{-6}k\lvert\alpha_s-\alpha_d\rvert\Delta T\sqrt{\frac{E_sE_dL}{X}}$ $\frac{da}{dN} = A\left(\Delta\sigma_{app}(\pi a)^{\frac{1}{2}}\right)^n$ $N_f = \frac{2}{(n-2)A(\Delta\sigma_{app})^n\pi^{\frac{n}{2}}}\left(\frac{1}{a_i^{\frac{(n-2)}{2}}} - \frac{1}{a_f^{\frac{(n-2)}{2}}}\right)$ Δ T-dependent, T-independent

electromigration	*thin film metallizations* $$T_f = \frac{1}{2Cn}\left(\frac{\tau_o k T_o}{j_o \rho_o D_o e^{-\frac{Q}{kT}}}\right)\int_{x_o}^{x_1} \frac{e^{\frac{-Qx}{kT_o}}}{x^2(1-x+x\alpha T_o)}dx$$ where $$\tau_o = \frac{\Delta T_o}{T_o} = \frac{j_o \rho_o}{k T_o}$$ and $$x = \frac{\tau_o}{(1-p)^2+\tau_o(1-\alpha T_o)}$$ $$= 1 - \left(\frac{T_o}{T}\right)$$ $$x_o = \frac{\tau_o}{1-\tau_o(\alpha T_o - 1)} \quad @ t=0$$ $$x_1 = 1-\left(\frac{T_o}{T_m}\right) \quad @ t=T_f$$ *multilayered metallizations* $$\frac{\partial R(v)}{\partial T} = R_{sq} C_m \frac{L-v(t)}{L} + R_b C_r \frac{v(t)}{L}$$ Dependent on structural non-uniformity and temperature gradient at temperatures lower than 150°C. Steady-state temperature-dependent for temperatures above 150°C, even though dependencies on structural non-uniformity and temperature gradient still exist.
hillock formation	ΔT-dependent, steady-state temperature dependent in the neighborhood of 400°C
hot electrons	$$\Delta V_t = C_1[C_2 I_o]^{\beta}$$ T^{-1}-dependent in the neighborhood of -55°C, and independent of steady-state temperature at higher temperatures (20°C to 100°C)

wire-bondpad shear fatigue	$N_f = C_w \tau_{w,M}^{-m_w}$ $N_f = C_s \tau_{s,M}^{-m_s}$ $\tau_{w,M} = \left(\frac{r^2}{4Z^2 A_w^2} \left(\frac{Cosh(z\,x)}{Cosh(z\,l_w)} - 1 \right)^2 + \frac{Sinh^2(Z\,x_w)}{Cosh^2(Z\,l_w)} \right)^{\frac{1}{2}} Q \Delta T$ $\tau_{s,M} = \left(\left(\frac{W_p Q}{2Z^2 A_s^2} \left(1 - \frac{Cosh(Zx_w)}{Cosh(Zl_w)} \right) + \frac{(\alpha_s - \alpha_p)}{\frac{(1 - \nu_s)}{(E_s A_s)} + \frac{1}{(E_p A_p)}} \right)^2 + Q^2 \frac{Sinh^2(Zx_w)}{Cosh^2(Zl_w)} \right)^{\frac{1}{2}} \Delta T$ $Z^2 = \frac{G_p}{b_p} \left(\frac{r}{E_w A_w} + \frac{(1 - \nu_s) W_p}{E_s A_s} \right)$ Δ T-dependent, T-independent
wire fatigue	$N_f = A(\epsilon_f)^n$ $\epsilon_f = \frac{r}{\rho_o} \left[\frac{Cos^{-1}((Cos\lambda_o)(1 - (\alpha_w - \alpha_p)\Delta T))}{\lambda_o} - 1 \right]$ Δ T-dependent, T-independent

Table 2.7 Dominant Temperature Dependency over Steady-state Temperatures from -55°C to 500°C

		Temperature	-55°C < T < 150°C	150°C < T < 400°C	T > 400°C
Package element	Mechanism		Nature of temperature dependence	Nature of temperature dependence	Nature of temperature dependence
wire	flexure fatigue		Δ T	Δ T	Δ T
wirebond	shear fatigue		Δ T	Δ T	Δ T
	Kirkendall voiding		temperature-independent	T-dependent for T > 150°C	T-dependent
die	die fracture		Δ T	Δ T	Δ T
	electrical overstress		Temperature-independent	T-dependent for T > 160°C	T-dependent
die adhesive	die adhesive fatigue		Δ T	Δ T	Δ T
encapsulant	encapsulant reversion (plastic package only)		Temperature-independent	T-dependent for T > 300°C	T-dependent
	encapsulant cracking (plastic package only)		Δ T , ∂ T/∂ t (≥ 25°C/sec.)	T-dependent (for T > 215°C), Δ T, ∂ T/∂ t, (≥ 25°C/sec.)	T-dependent Δ T ∂ T/∂ t
package	stress corrosion		∂ T/∂ t	∂ T/∂ t	∂ T/∂ t
die metallization	corrosion		mildly T-dependent, ∂ T/∂ t	∂ T/∂ t	∂ T/∂ t
	electromigration		structural non-uniformity dependent, ∇ T	T-dependent (for T > 150°C), ∇ T-dependent	T-dependent (for T > 150°C), ∇ T-dependent

	hillock formation	ΔT	ΔT	T-dependent (for T > 400°C)
	metallization migration	Temperature-independent	Temperature-independent	T-dependent (for T > 500°C)
	contact spiking	Temperature-independent	Temperature-independent	T-dependent (for T > 400°C)
	constraint cavitation	T-dependent	T^{-1}-dependent	T^{-1}-dependent
	slow trapping	Temperature-independent	T-dependent (for T > 175°C)	T-dependent
	electrostatic discharge	Temperature-independent (in presence of protection circuits)	Temperature-independent (in presence of protection circuits)	Temperature-independent (in presence of protection circuits)
	time-dependent dielectric breakdown	voltage-dependent, weak T dependence	voltage-dependent, weak T dependence	voltage-dependent, weak T dependence
Device	ionic contamination	T^{-1}-dependence (device not operational)	T^{-1}-dependence (device not operational)	T^{-1}-dependence (device not operational)
	forward second breakdown	Temperature-independent	T-dependent (for T > 160°C)	T-dependent
	reverse second breakdown	Mild T^{-1}-dependence	mild T^{-1}-dependence	mild T^{-1}-dependence
	surface-charge spreading	Temperature-independent	T-dependent (for T > 150°C)	T-dependent (for T > 150°C)
Device / Oxide interface	hot electrons	T^{-1}-dependent	Temperature-independent	Temperature-independent

Table 2.8 Variation of the Nature of Temperature Dependency of the Device from -55°C to 500°C

Nature of stress dependence	-55°C < T < 150°C	150°C < T < 400°C	T > 400°C
	Number of Mechanisms	Number of Mechanisms	Number of Mechanisms
steady-state temperature (T)	1	8	11
temperature cycle (Δ T)	6	6	5
temperature gradient (∇ T)	1	1	1
time dependent temperature change (∂ T/∂ t)	3	3	3
voltage (V)	1	1	1
inverse temperature dependent (T^{-1})	3	3	3
temperature independent (form of temperature dependence)	9	4	2

3

TEMPERATURE RELATED PARAMETER VARIATIONS

3.1 INTRODUCTION

This chapter discusses the temperature dependence of electrical parameter variations in bipolar and MOSFET devices. The parameters investigated for bipolar devices include intrinsic carrier concentration, thermal voltage, mobility, current gain, leakage current, collector-emitter saturation voltage, and VTC shift. The parameters investigated for MOSFETs include threshold voltage, mobility, drain current, time delay, strong inversion leakage, subthreshold leakage, and chip availability. The temperature thresholds above which temperature dependence renders the device inoperable have been identified for each of the parameters.

3.2 TEMPERATURE DEPENDENCE OF BIPOLAR JUNCTION TRANSISTOR PARAMETERS

3.2.1 Intrinsic Carrier Concentration, Thermal Voltage and Mobility

The ideal p-n junction (ideal diode equation) is affected by temperature due to variations in the saturation current, which is a function of the intrinsic carrier concentration and thermal voltage. Intrinsic carrier concentration is exponentially dependent on steady-state temperature (Equation (3.3), and thermal voltage is linearly dependent on steady-state temperature ($V_T = kT/q$). The ideal diode equation is represented by

$$I = I_s\left(e^{\eta V_T} - 1\right) \tag{3.1}$$

where I is the total forward bias diode current, V is the voltage across the diode, V_T is the thermal voltage ($=kT/q$), and I_s is the saturation current given by

$$I_s = qA\left(\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right) \tag{3.2}$$

where q is the electron charge (= 1.6×10^{-19} Coulomb); A is the cross-sectional area of the p-n junction; D_p and D_n are the diffusion coefficients of the p and n regions, respectively; L_p and L_n are the diffusion lengths of the p and n regions, respectively (one diffusion length is the distance in the neutral region at which the minority carrier concentration is 0.37 of its value at the edge of the depletion, or space-charge, region); P_{no} is the minority hole concentration in the n-region; and N_{po} is the minority electron concentration in the p-region. The effect of temperature on saturation current derives its origin from the variation in intrinsic carrier concentration, N_i, which increases dramatically with temperature and is given as

$$n_i = \sqrt{N_C N_V}\; e^{-E_g/2KT} \tag{3.3}$$

where N_V and N_C are the valence and conduction-band effective densities, respectively, given by

$$N_V=2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2} \tag{3.4}$$

$$N_C=2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2} \tag{3.5}$$

Furthermore, the temperature dependence of the intrinsic carrier concentration may also be represented by

$$n_i^2(T) = KT^{-3}e^{-V_{g0}/V_T} \tag{3.6}$$

where K is a constant, T is the absolute temperature (Kelvin), V_{g0} is the band gap voltage (for silicon at 300 K, V_{g0} is 1.11 V), and V_T is the thermal voltage (at 300K, $V_T \approx 26$ mV) [Hodges and Jackson 1988].

The temperature rate of change of the saturation current is represented by the temperature coefficient of saturation current, which describes the fractional change for I_s per unit change in temperature, represented by Hodges and Jackson [1988] as

$$\begin{aligned}\frac{1}{I_s}\frac{dI_s}{dT} &= \frac{1}{n_i^2}\frac{dn_i^2}{dT} \\ &= \frac{3}{T} + \frac{1}{T}\frac{V_{g0}}{V_T}\end{aligned} \tag{3.7}$$

For silicon near-room temperature, the first term in Equation (3.7) is $\approx$ 1% per Kelvin, and the second term is 14% per Kelvin. In other words, the saturation current approximately doubles for every 5°C rise. Moreover, the band gap voltage, E_G, also varies with temperature:

$$E_G(T)=E_G(0)-\frac{\alpha T^2}{T+\beta} \tag{3.8}$$

where $E_G(0)$ is the band gap energy at T=0 [Roulston 1988]. For silicon, α is $7.02\text{x}10^{-4}$ and β is 1108 [Pierret 1989]. The band gap energy decreases with temperature.

Carrier mobility, a function of steady-state temperature, is a ratio of carrier

velocity to the electric field causing carrier motion. Mobility decreases with temperature and is represented by Roulston [1990] as

$$\mu_p = 54\left(\frac{T}{300}\right)^{-0.57} + \frac{1.36x10^{8}T^{-2.33}}{1+\left(\frac{N_d}{2.35x10^{17}\left(\frac{T}{300}\right)^{2.4}}\right)0.88\left(\frac{T}{300}\right)^{-0.146}} \qquad (3.9)$$

$$\mu_n = 0.88\left(\frac{T}{300}\right)^{-0.57} + \frac{7.4x10^{8}T^{-2.33}}{1+\left(\frac{N_A}{1.26x10^{17}\left(\frac{T}{300}\right)^{2.4}}\right)0.88\left(\frac{T}{300}\right)^{-0.146}} \qquad (3.10)$$

The temperature characteristics of these parameters is, however, of minor importance, because signal voltages in most cases are much larger than the variation of the diode voltage over the temperature range -55°C to 125°C [Hodges and Jackson 1988].

3.2.2 Current Gain

The current gain of the bipolar junction transistor is the collector current divided by the base current, otherwise known as β. The d.c. current gain is expressed as

$$B = \frac{I_C}{I_B} \qquad (3.11)$$

The common emitter d.c. current gain increases appreciably with increasing temperature because of improved emitter efficiency at higher temperatures. Emitter efficiency is exponentially dependent on steady-state temperature (Equation (3.12). The exponential term, represented by exp $(-\Delta E_g/kT)$, arises due to the energy-gap reduction of a highly doped emitter [Kauffman and Bergh 1968,

Buhanan 1969, RCA 1978].

$$\gamma_E = \frac{D_n}{D_p}\left(\frac{\int_0^{W_E} N_D e^{-\Delta E_g/kT}}{\int_0^{W_B} N_A dx}\right) \tag{3.12}$$

For moderately or lightly doped emitters (concentrations below 5 x 10^{19} cm^{-3}), ΔE_g is very small, and the temperature effect on current gain is negligible. For doping concentrations above 10^{19} cm^{-3}, the hole mobility in the emitter is relatively constant with respect to temperature. Einstein's relationship ($D_p/\mu_p = kT/q$) predicts that the diffusion constant must increase with temperature. The minority carrier lifetime in the emitter, τ_p, increases with temperature, which causes the diffusion length, L_p, to also increase with temperature. The increase in the diffusion length of minority carriers adds to the ΔE_g effect by increasing the current gain. The variation in the d.c. current gain is depicted by Figure 3.1. The temperature sensitivity of current gain is a contributing factor to hot-spot formation and affects the second breakdown energy limit. It is therefore advantageous to reduce the current gain temperature dependence by lightly doping the transistor base and limiting the phosphorus-doped emitter surface concentration to about 7 x 10^{19} cm^{-3} [Kauffman and Bergh 1968, Buhanan 1969, RCA 1978].

Ebers-Moll equations for emitter and collector current are represented as [Hodges and Jackson 1988]

$$I_E = I_{ES}\,(e^{V_{BE}/V_t} - 1) - \alpha_R\, I_{CS}\,(e^{V_{BC}/V_t} - 1) \tag{3.13}$$

$$I_C = \alpha_F I_{ES}(e^{V_{BE}/V_t} - 1) - I_{CS}(e^{V_{BC}/V_t} - 1) \tag{3.14}$$

where I_{ES} and I_{CS} represent the saturation currents for emitter and collector junctions, respectively; V_{BE} and V_{BC} represent the base-emitter and base-collector bias voltages; V_T is the thermal voltage ($= kT/q$); and α_R and α_F are the common base current gains ($=I_C/I_E$). Here, α_R corresponds to the common base current gain with the base-emitter junction reverse-biased and the base-collector junction forward-biased; α_F corresponds to the common base current gain with the base-emitter junction forward-biased and the base-collector junction reverse-biased.

The base current is obtained by substituting for I_E and I_C from Equations (3.13) and (3.14) [Marazas 1992]:

$$I_B = I_E - I_C \tag{3.15}$$

$$I_B = qAn_i^2\left(\frac{D_E}{L_E N_E}\right)\left(e^{\frac{qV_{BE}}{kT}} - 1\right) + qAn_i^2\left(\frac{D_C}{L_C N_C}\right)\left(e^{\frac{qV_{BC}}{kT}} - 1\right) \tag{3.16}$$

The expression for common emitter d.c. current gain, beta = I_C/I_B, holds only for the active region of BJT operation. In the active region, the base-collector junction is reverse-biased, making the exponent $\ll 1$. On the assumption that the exponential base-collector term is negligible, the previous equations reduce to

$$I_B = q\,A\,n_i^2\,\frac{D_E}{L_E\,N_E}\,e^{V_{BE}/V_T} \tag{3.17}$$

$$I_C = q\,A\,n_i^2\,\frac{D_B}{W_B\,N_B}\,e^{V_{BE}/V_T} \tag{3.18}$$

where n_i is the intrinsic carrier concentration; A is the area of the base region; q is the electron charge (= 1.6×10^{-19} C); D_B and D_E are the diffusion coefficients of the base and emitter, respectively; W_B is the base width; L_E is the diffusion length of the minority carriers in the emitter; and V_T is the thermal voltage.

Substituting the explicit temperature dependence into the above equations and dividing I_C by I_B, β is given as [Marazas 1992]

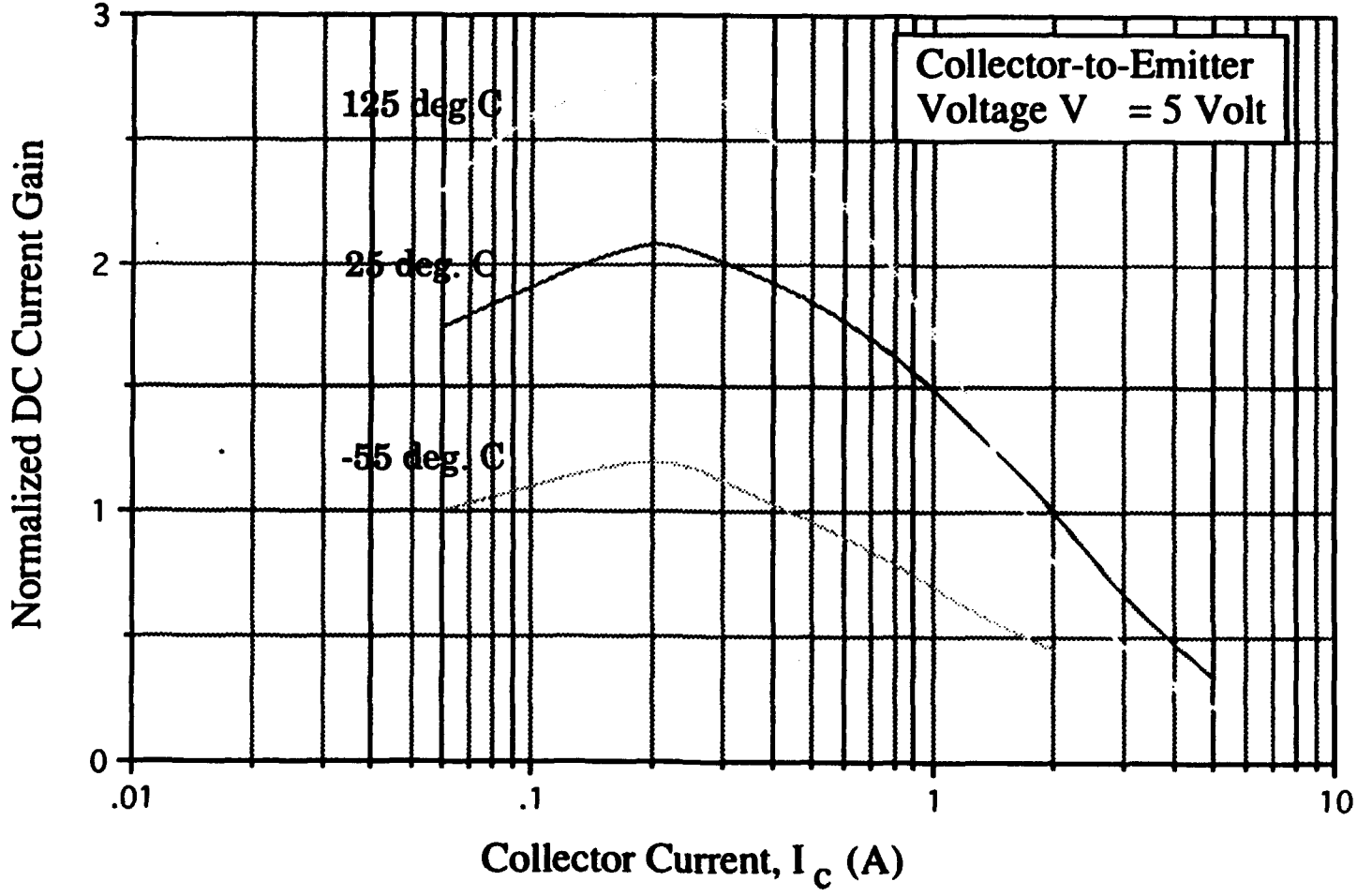
$$\beta = \frac{N_E k}{qN_B W_B}\sqrt{T\mu(T)\tau(T)} \tag{3.19}$$

3.2.3 BJT Inverter Voltage Transfer Characteristic (VTC)

Steady-state temperature alters the voltage transfer characteristic of the bipolar junction transistor (BJT). Typically, the transistor moves from the cutoff region to the active region, in the neighborhood of 27°C, when a voltage of

approximately 0.7 volts (V_{bes}) is applied across the base-emitter junction V_{in}. The

Figure 3.1 Temperature dependence of current gain for a bipolar transistor. The temperature sensitivity of current gain is a contributing factor to hot spot formation and effects the second breakdown energy limit. It is therefore advantageous to reduce the current gain temperature dependence by lightly doping the transistor base and limiting the phosphorous doped emitter surface concentration to about 7 x 10 cm [Kaufmann and Bergh, 1968; Buhanan, 1969; RCA, 1978]



minimum base-emitter voltage, (V_{beo}), required to obtain the same I_{bo} decreases with an increase in temperature. The temperature dependence of V_{beo} can be derived from Equation (3.17). This value, I_{bo}, represents the minimum current necessary to turn on the transistor at 27°C. The equation for V_{beo} is [Hodges and Jackson 1988, Muller and Kamins 1986]

$$V_{BEon}(T) = \frac{kT}{q}\log\left[\frac{I_{BO}L_E N_{DE} q}{q n_i^2(T) A \mu_E(T) kT}\right] \tag{3.20}$$

There are three regions of operation for the BJT inverter, known as the cut-off, active, and saturation regions. In the cut-off region, the input voltage, V_{in}, is less than the BJT turn-on voltage, V_{beo}. The base current, I_b, is zero, and thus the collector current and the emitter current are also zero. The output voltage is therefore equal to V_{CC}:

$$V_{out} = V_{CE} = V_{CC} \tag{3.21}$$

where V_{out} is the output voltage, V_{CE} is the collector-emitter voltage, and V_{CC} is the collector supply voltage. In the active region, V_{in} is greater than V_{BEon}. The base current can be found from the voltage drop across the base resistor

$$I_B = \frac{V_{in} - V_{BE(on)}}{R_B} \tag{3.22}$$

where R_B is the base-load resistor, V_{in} is the input voltage to the BJT inverter, $V_{BE(on)}$ is the turn-on voltage for the BJT, and I_B is the base current. The collector current can be calculated from the base current and the BJT current gain (β_f).

$$I_C = \beta_f I_B \tag{3.23}$$

The output voltage, V_{CE}, is given by

$$V_{out} = V_{CC} - R_C I_C \tag{3.24}$$

The temperature dependence of the output voltage is calculated from Equations (3.22) through (3.24).

$$V_{out}(T)=V_{CC}-\left(\frac{R_C}{R_B}\right)\beta_f(T)\left(V_{in}-V_{BE(on)}(T)\right) \tag{3.25}$$

The third region of operation for the BJT is the saturation region. The collector current is given by

$$I_C=\frac{V_{CC}-V_{CE}}{R_C} \tag{3.26}$$

where V_{CC} is the collector supply voltage and V_{CE} is the collector voltage. However, when the transistor is not actually in the saturation region but on the edge of saturation, $V_{CB}=0$, so

$$I_C=\frac{V_{CC}-V_{BE(on)}}{R_C} \tag{3.27}$$

Equation (3.27) represents the maximum amount of current allowed in the collector before the transistor actually goes into saturation. Additionally, the maximum allowed base current is

$$I_B=\frac{I_C}{\beta} \tag{3.28}$$

The input voltage can be derived from Equation (3.22):

$$V_{in}=I_BR_B+V_{BE(on)} \tag{3.29}$$

The temperature dependence of the critical input voltage that would push a BJT into saturation is represented as [Marazas 1992]

$$V_{crit}(T) = \frac{R_B}{R_C}\left(\frac{V_{CC}-V_{BE(on)}(T)}{\beta(T)}\right) + V_{BE(on)}(T) \tag{3.30}$$

where V_{crit} is the critical input voltage. In bipolar devices operating high-voltage current-switching applications, the collector current plays a major role in

determining transistor losses; Bromstead represents this by I_{CE} in the following equation [1991]:

$$I_o = qA\left(\frac{D_N}{L_N}\frac{n_i^2}{N_A} + \frac{D_P}{L_P}\frac{n_i^2}{N_D}\right) \tag{3.31}$$

The approximate fractional change in leakage current versus temperature is represented by

$$\frac{1}{I_o}\left(\frac{\partial I_o}{\partial T}\right) = \frac{1}{2}\left(\frac{3}{T} + \frac{E_G}{\sqrt{N_C N_V}}\right) \qquad @\ V_R = constant \tag{3.32}$$

where E_G is the activation energy in eV, N_C is the density of the conduction band, N_V is the density of the valence band, and T is the steady-state temperature in degrees Kelvin [Severns and Armijos 1984]. The change in the collector leakage current is approximately 8 °C for every 12 °C rise in steady-state temperature at the junction for the temperature range 150 °C to 200 °C. Below steady-state temperatures of 150 °C, the leakage current exhibits a plateau-i.e., it does not change at temperatures of up to 150 °C ($I_{CE}(150°C) = 1.2 \times 10^{-4}$ amp, and $I_{CE}(200°C) = 1.5 \times 10^{-3}$ amp)[Bromstead 1991]. Emitter-base leakage current exhibits saturation in the lower temperature region (under 150°C). For temperatures higher than 150°C, the emitter base leakage current exhibits doubling for every 12°C rise in steady-state temperature($I_{EB}(150°C) = 1.3 \times 10^{-4}$ Amp, and $I_{EB}(200°C) = 2.3 \times 10^{-3}$ Amp)[Bromstead 1991].

3.2.4 Collector-Emitter Saturation Voltage

In high-voltage and current-switching applications, the saturation voltage, $V_{CE(sat)}$, is vital for determining transistor losses. Under normal switch or inverter conditions, the major part of the voltage drop across the transistor occurs in the non-conductivity-modulated region close to the n^+ epitaxial layer. Assuming that both the base and the collector have entered high-level injection, the total value of the C-E saturation voltage can be written as [Roulston 1990]

$$V_{CEsat} = \frac{I_c \rho_{epi} W_R}{A} - 2V_t \ln\left[\frac{p(W_b)}{n_i}\right] + 2V_t \ln\left[\frac{n(0)}{n_i}\right] \tag{3.33}$$

where $W_R = W_b - X_O$ (W_b - base width, X_O - oxide thickness), $p(W_b)$ is the

hole concentration at the base-collector (B-C) junction, and $n(0)$ is the electron concentration at the base-emitter (B-E) junction [Roulston 1990]. The resistivity of the epitaxial layer is given as

$$\rho_{epi} \approx \frac{1}{q\mu_n N_{epi}} \tag{3.34}$$

where μ_n is the electron mobility and N_{epi} is the epitaxial layer density. The temperature dependence of electron mobility is represented as

$$\mu_n = 88\left(\frac{T}{300}\right)^{-0.57} + \frac{7.4x10^{8}T^{-2.33}}{1+\left(\frac{N}{1.26x10^{17}\left(\frac{T}{300}\right)^{2}.4}\right)0.88\left(\frac{T}{300}\right)^{-0.146}} \tag{3.35}$$

where N is the electron density, and T is the steady-state temperature in degrees Kelvin [Roulston 1990]. The temperature dependence of V_{CEsat} is related to the intrinsic carrier concentration, n_i, by

$$n_i = \sqrt{N_c N_v}\, e^{-E_G/2kT} \tag{3.36}$$

where N_c is the effective density of the conduction band, N_v is the effective density of the valence band, E_G is the activation energy in eV, k is Boltzmann's constant ($8.617x10^{-5}$ ev/K), and T is the steady-state temperature in degrees Kelvin [Pierret 1987]. Table 3.1 represents the variation of intrinsic carrier concentration, epitaxial resistivity, and collector-emitter saturation voltage for temperatures between 20 °C and 200 °C [Bromstead 1991].

3.3 TEMPERATURE DEPENDENCE OF MOSFET PARAMETERS

3.3.1 Threshold Voltage

The threshold voltage is the minimum gate voltage at which the channel starts conducting. The closed-form value of the threshold voltage is derived from the current voltage characteristics. MOSFET behavior with respect to temperature can be derived by finding the incremental voltage drop along the channel, as a function of the channel current. At a distance y along the channel, the voltage with respect to the source is $V(y)$ and the gate-to-channel voltage is $V_{GS}-V(y)$. Assuming that the gate voltage exceeds the threshold voltage, the charge per unit area in the conducting channel at a point, y,is represented by

$$Q_i(y) = C_{ox}(V_{GS}-V(y)-V_{th}) \tag{3.37}$$

where C_{ox} is the oxide capacitance per unit area, V_{GS} is the gate-source voltage, $V(y)$ is the voltage induced in the channel with respect to source, and V_{th} is the threshold voltage [Muller and Kamins 1986, Hodges and Jackson 1988]. The resistance, dR, of this channel of length, dy, is

$$dR = \frac{dy}{W\mu_n Q_i(y)} \tag{3.38}$$

where W is the width of the channel perpendicular to the length, and μ_n is the average mobility of the electrons in the channel [Muller and Kamins 1986, Hodges and Jackson 1988]. The voltage drop along the channel of length dy is [Muller and Kamins 1986, Hodges and Jackson 1988]

$$dV_C = I_D dR = -\frac{I_D dY}{W\mu_n Q_n(y)} \tag{3.39}$$

Integrating along the path from the source to the drain for I_D as a function of applied voltage (for $V_{GS} \geq V_{th}$; and $V_{DS} \leq (V_{GS}-V_{th})$),

$$I_D = \frac{k}{2}\left(2(V_{GS}-V_{th})-V_{DS}^2\right) \tag{3.40}$$

where V_{th} is the threshold voltage, and k is the transconductance parameter ($k=(\mu_n C_{ox} W)/L$) [Muller and Kamins 1986, Hodges and Jackson 1988]. Equation (3.40) is the expression for drain current in the linear region of operation. In the saturation region, where $V_{GS} \geq V_{th}$; $V_{DS} \geq V_{GS}-V_{th}$, the drain current is represented as [Muller and Kamins 1986, Hodges and Jackson 1988]

$$I_D = \frac{k}{2}(V_{GS}-V_{th})^2 \tag{3.41}$$

The total mobile electron charge is represented as [Muller and Kamins 1986, Hodges and Jackson 1988]

$$Q_n = -C_{ox}(V_G - V_{FB} - V_B - 2|\phi_p|) + \sqrt{2\epsilon_s q N_a (2|\phi_p| + V_C - V_B)} \quad (3.42)$$

The threshold voltage is then represented by

$$V_{th} = V_{FB} + V_C + 2|\phi_p| + \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_a (2|\phi_p| + V_C - V_B)} \quad (3.43)$$

where V_{FB} is the flatband voltage, V_C is the voltage in the MOS channel, ϕ_p is the potential in the p-type material (i.e., the difference between the fermi level and the intrinsic concentration), C_{ox} is the oxide capacitance, N_a is the number of acceptors, q is the electronic charge (1.6×10^{-19} C), V_B is the base voltage, and ϵ_s is the silicon permittivity. The temperature dependence of threshold voltage is represented as

$$V_{TN} = P_o T + Q_o \quad (3.44)$$

$$V_{TP} = -P_o T - Q_o \quad (3.45)$$

where the constant P_o = -2.4 x 10^{-3} and Q_o = 1.72 (for the temperature range of 25-250°C) [Shoucair 1986]. This equation applies to a typical MOSFET with V_t equal to 1 volt at 27°C. Typically, the threshold voltage of both NMOS and PMOS enhancement-mode transistors decreases in magnitude by 1.5 to 2 mV/°C with increasing temperature. Figure 3.2 shows the threshold voltage variation versus temperature for n- and p-channel MOSFETs with bulk concentration 10^{15} cm^{-3}; 37(b) shows this for bulk concentration 3 x 10^{16} cm^{-3} [Wang 1971]. However, the change in threshold voltage does not produce a very significant change in circuit performance, because even a 200 mV change in V_T does not cause a very large percentage change in $V_{GS} - V_T$ [Hodges and Jackson 1988]. The threshold voltage of devices with heavily doped bulk is more sensitive to temperature variation than lightly doped substrates [Blicher 1981].

3.3.2 Mobility

The mobility of carriers in a channel of an MOS transistor is an inverse function of absolute temperature. The temperature dependence is represented by

$$\mu_{eff_n} = \mu_{no}\left[\frac{T}{T_0}\right]^{-1.5} \tag{3.46}$$

$$\mu_{eff_p} = \mu_{po}\left[\frac{T}{T_o}\right]^{-1.5} \tag{3.47}$$

where μ_o is the mobility at 27°C in both cases and T_o is 27°C [Shoucair 1986, Tsividis and Antognetti 1985, Muller and Kamins 1986, Hodges and Jackson 1988]. Thus, a 100°C rise in temperature may decrease the mobility by as much as 40%. The result is a proportional decrease in the drain current, I_D, for fixed applied voltages. The current consumption of the whole circuit may decrease considerably at high temperature (Figure 3.3). The maximum speed of operation thus decreases in proportion. The change in threshold voltage and mobility affect the drain current, the transconductance, and the drain-source on resistance (Figures 3.4 and 3.5).

3.3.3 Drain Current

The drain current decreases with temperature. The temperature dependence of the drain current can be represented by

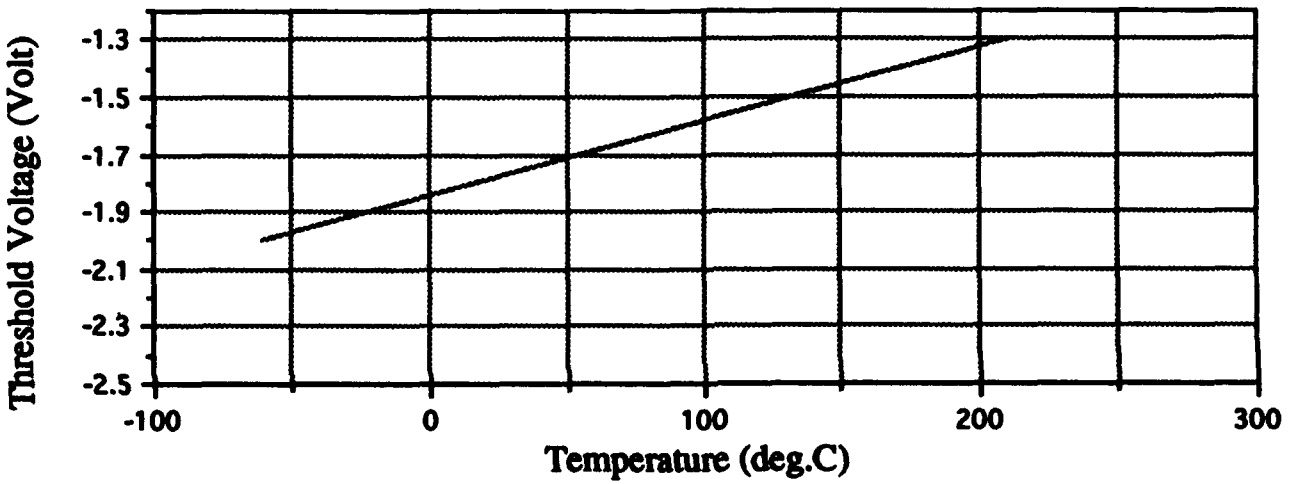
$$I_{ds} = \frac{A}{1+BT} \tag{3.48}$$

where I_{ds} is the drain current, A and B are empirical constants, and T is the temperature (centigrade) [Chang 1987]. The temperature degradation coefficient, B, in Equation (3.48), is a function of gate voltage (V_{gs}) and drain voltage (V_{ds}) (Figure 3.6). Typical values of the temperature degradation coefficient, B, range from 1.03 x 10^{-3}/°C to 6 x 10^{-3}/°C. This model fits experimental data for variations in drain current versus temperature for 10°C to 120°C. Theoretically, the temperature dependence of drain current versus temperature is represented by

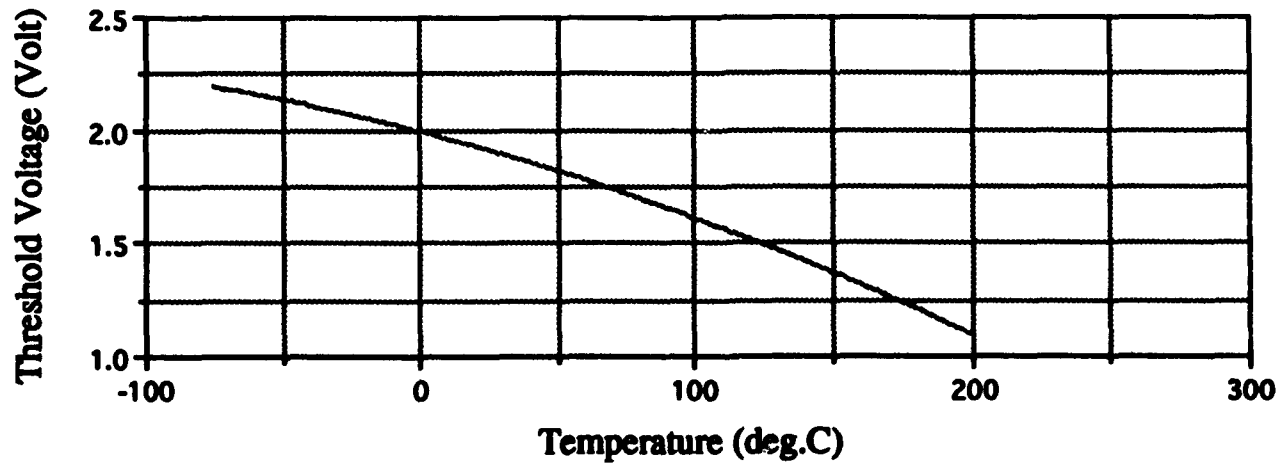
$$I_{ds} = C(T+273)^{-D} \tag{3.49}$$

where C and D are fitting parameters and T is the temperature (centigrade). The relationship between the experimental data represented by Equation (3.48) and

Figure 3.2 Threshold voltage variation of n- and p- channel MOSFETs (a). With bulk concentration $10^{15}cm^{-3}$ and (b). With bulk concentration $3 \times 10^{16}cm^{-3}$ [Wang, 1971]. The change in threshold voltages does not produce a very significant change in circuit performance, because even a 200 mV change in V_T does not cause a larger percentage change in $V_{GS}-V_T$. [Hodges and Jackson, 1988]



(a).



(b).

Figure 3.3 Effective channel mobility characteristics for n and p channel MOSFETs. Mobility is an inverse function of absolute temperature [Shoucair, 1986]

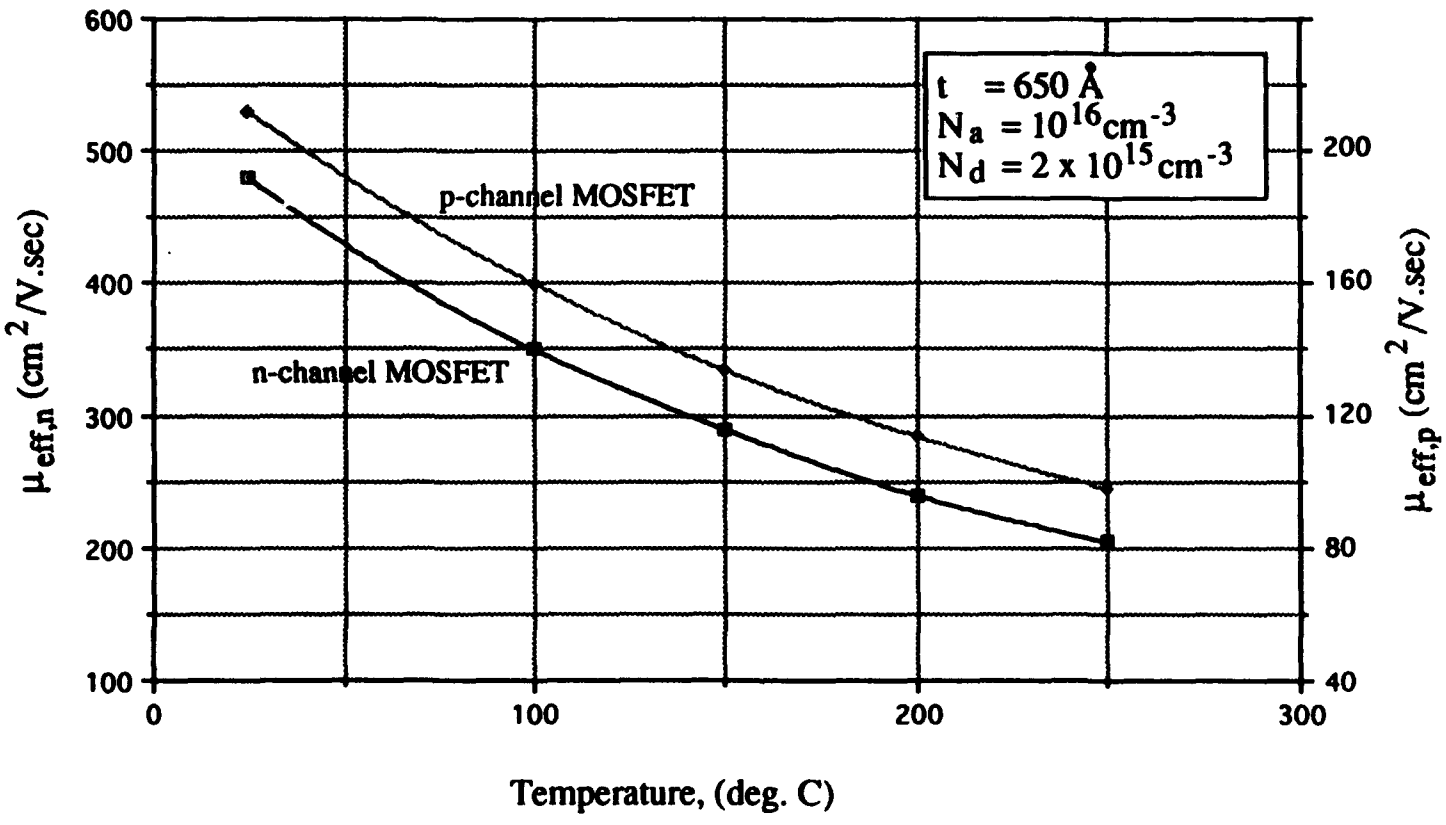


Figure 3.4 The variation in the drain-to source ON resistance. The ON resistance increase by a factor of 3 over a temperature range of -40 to 120 deg.C [Blicher, 1981]

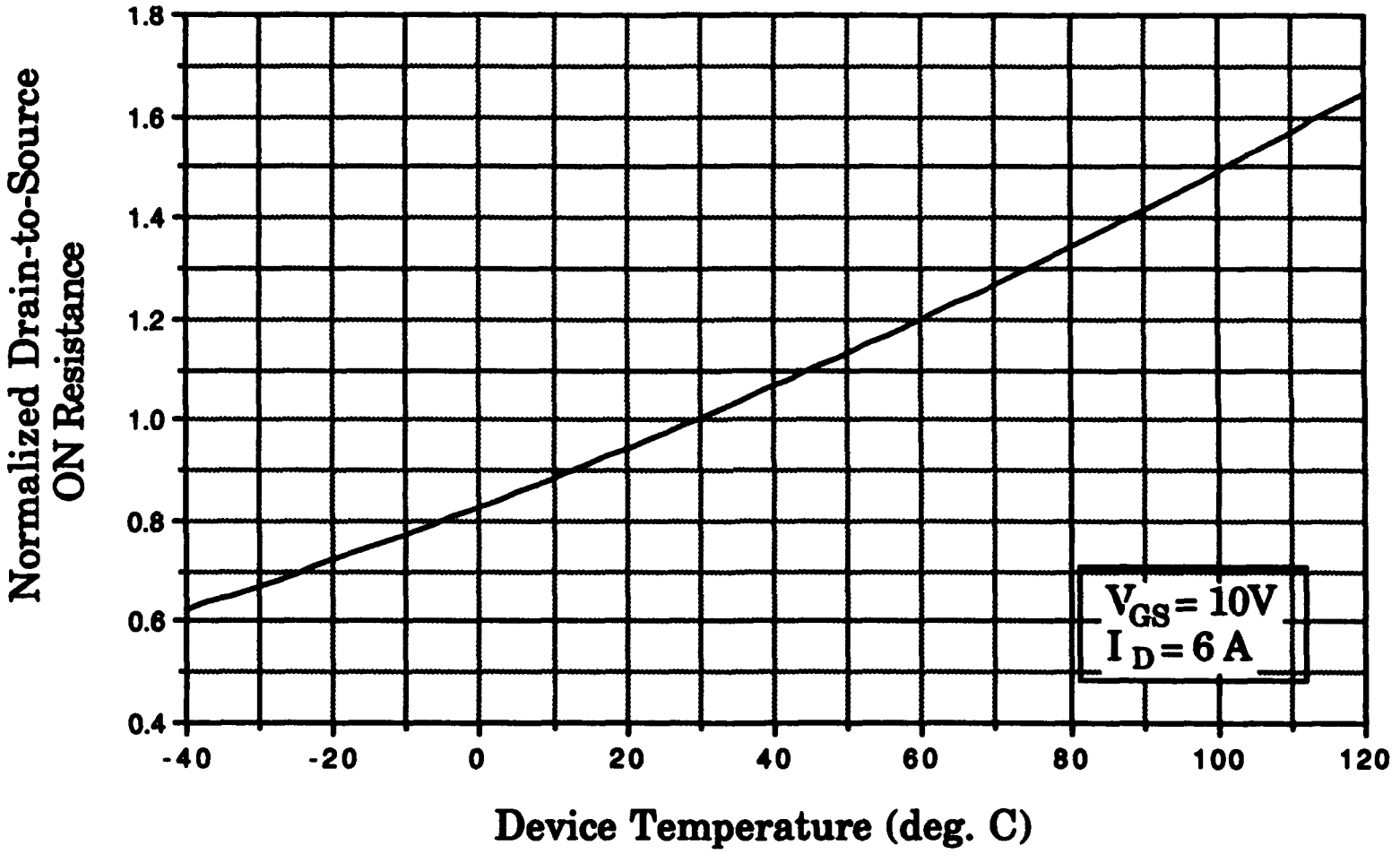
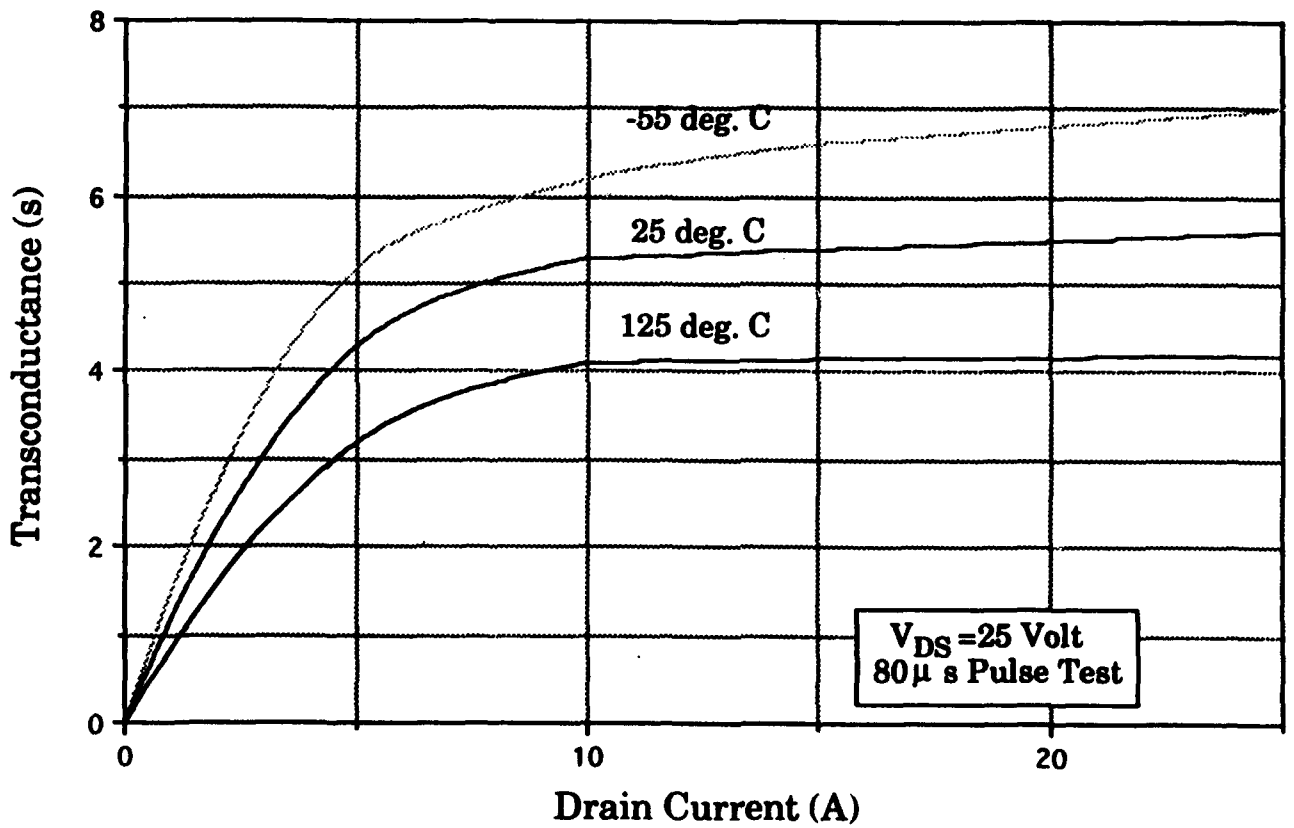


Figure 3.5 The variation in transconductance versus temperature in the temperature range of -55 to 125 deg. C. [Blicher, 1981]



theoretical calculations represented by Equation (3.49) is

$$D = 203B + 0.25 \tag{3.50}$$

The correlation between the simplified first-order experimental equation and the theoretical equation is 0.998. The variation in drain current with temperature is not very significant in the temperature range of -55°C to 125°C (Figure 3.6) [Blicher 1981].

3.3.4 Time Delay

In a MOS circuit, the delay time due to charging and discharging of the load capacitor through a turn-on has been represented by Chang as [1987]:

$$t_d = C_l \int \frac{dV_{ds}}{I_{ds}(V_{ds}, T)} \tag{3.51}$$

where C_l is the load capacitance, V_{ds} is the drain voltage, I_{ds} is the drain current, and T is the temperature. The temperature dependence of time delay is represented by the linear temperature coefficient of delay time, K, which is the time-change rate of delay time versus temperature

$$K = \frac{dt}{t_o \, dT} \tag{3.52}$$

where t_o is the time delay at reference temperature [Chang 1987]. Substituting into Equation (3.52) for I_{ds} from Equation (3.48) and for delay time, t_d, from Equation (3.51),

$$K = \frac{\int_{V_l}^{V_{dsat}} \frac{B}{I_o} dV_{ds} + \int_{V_{dsat}}^{V_h} \frac{B}{I_o} dV_{ds}}{\int_{V_l}^{V_{dsat}} \frac{dV_{ds}}{I_o} + \int_{V_{dsat}}^{V_h} \frac{dV_{ds}}{I_o}} \tag{3.53}$$

where I_o is the I_{ds} at 0°C, $V_l = F x V_{cc}$, $V_h = (1-F) x V_{cc}$ for $0 < F < 1$; V_l and V_h are the lower and upper bounds for the voltage swing used in delay-time calculation [Chang 1987]. The total swing during device switching has been

divided into linear and saturation regions. Equation (3.53) is simplified as

$$K = \frac{B_o\left(\ln\left(\frac{V_{dsat}}{V_l}\right)V_{dsat} + V_l\right) + B_{sat}\left(V_{dsat} - V_l + \ln\left(\frac{V_{cc}-V_{dsat}}{V_{cc}-V_h}\right)(V_{cc}-V_{dsat})\right)}{\left(\ln\left(\frac{V_{dsat}}{V_l}\right) - \ln\left(\frac{V_{cc}-V_{dsat}}{V_{cc}-V_h}\right)\right)V_{dsat} + \ln\left(\frac{V_{cc}-V_{dsat}}{V_{cc}-V_h}\right)V_{cc}} \quad (3.54)$$

where K is the linear temperature coefficient of delay time (the rate of delay time with respect to temperature), B_o is the temperature degradation coefficient at temperature 0°C, V_{dsat} is the drain voltage at saturation, V_l and V_h is the lower and higher bounds of the voltage swing during device switching [Chang 1987]. The model can be extended to calculate the delay time for a CMOS ring oscillator, which consists of either seventeen or thirty-seven stages of directly coupled inverters. Each inverter consists of a pair of n-channel and p-channel MOSFETs. The total delay time, T_{fr}, of a CMOS inverter can be represented by

$$t_{fr} = t_f + t_r = t_{fo}(1 + K_r T) \quad (3.55)$$

where the subscripts represent the rise and fall times, respectively, and t_{fo} and t_{ro} are the corresponding delay times at 0°C [Chang 1987]. The total time-delay coefficient, K_{fr}, is

$$K_{fr} = \frac{K_f}{1 + \frac{t_{ro}}{t_{fo}}} + \frac{K_r}{1 + \frac{t_{fo}}{t_{ro}}} \quad (3.56)$$

Another model for gate delay versus temperature dependence is given by Shoucair [1987]. The gate delay is defined as the time between the input and output waveforms at the $V_{dd}/2$ points of the gate in the ring oscillator (V_{dd} is the drain supply voltage) at temperature T. The gate delay as a function of temperature is given by

$$t_d(T) = \frac{1.8C_L(T)V_{DD}}{\mu_N(T)C_{ox}\left(\frac{W}{L}\right)_N} X \left(\frac{1}{\left(1 - \frac{V_{THN}(T)}{V_{DD}}\right)^2} + \frac{1}{\left(1 - \frac{|V_{THP}(T)|}{V_{DD}}\right)^2}\right) \quad (3.57)$$

$$t_D(T) = t_D(T_o)(1 + c(T)(T - T_o)) \tag{3.58}$$

where T_o is the reference temperature, $c(T)$ is the temperature rate of change of gate delay (also called the delineation factor, $1/K$ or 1/°C), V_{THN} is the threshold voltage for n-channel, V_{THP} is the threshold voltage for the p-channel, and $C_L(T)$ is the total load capacitance. The delay increases linearly with temperature and can be calculated using the delineation factor, $c(T)$, at any temperature ranging from 0.004/°C to 0.006/°C. At 250°C, the cell is half as fast as at 25°C. The delineation factor quantifying the temperature dependence is larger for cells driving loads dominated by temperature-dependent junction capacitances than for temperature-independent capacitive loads. The delineation factor is constant for a given cell over a temperature range of 25°C to 250°C [Shoucair 1987]:

$$c(T) = \frac{1}{t_D(T_o)} \frac{dt_D(T)}{dT} \tag{3.59}$$

$$\frac{dt_D(T)}{dT} = t_D(T)\left(\frac{1.5}{T} + \frac{2}{V_{DD} - V_{TH}(T)} \frac{d_{TH}(T)}{dT}\right) \tag{3.60}$$

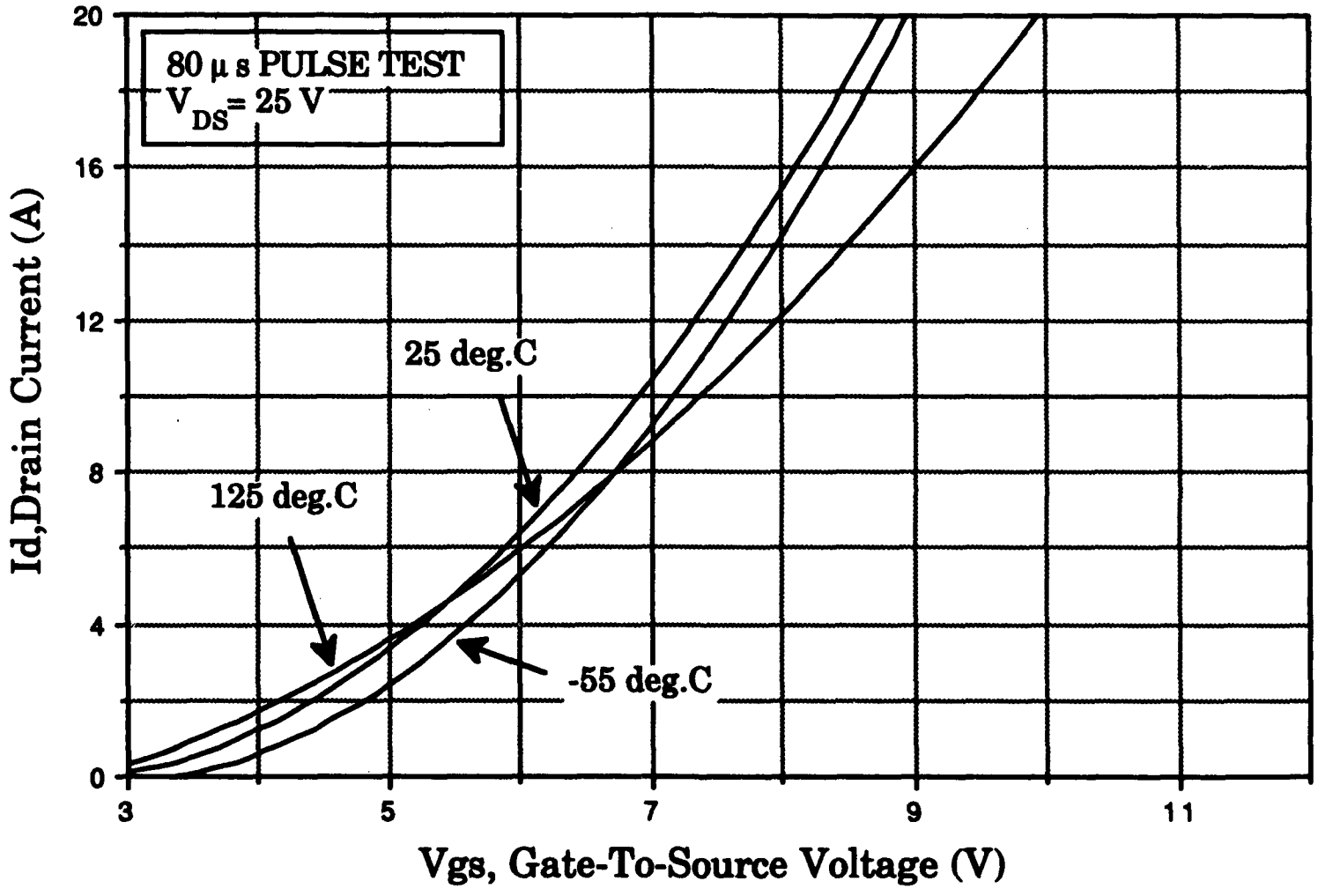
Shoucair estimated the temperature dependence of the rise and fall times, *t1* and *t0*, on a sample size of seven inverters [1984]. Assuming that $|V_{TH}(27°C)| \simeq 1.5$ V; $|dV_{th}(T)/dT| = 3.5$ mV/°C, $V_{DD} = +5$V, the ratio of rise and fall times, *t1* and *t0* , at 27°C and 250°C was estimated to be 1.67 (*R0 = t0(250°C)/t0(27°C); R1 = t1(250°C)/t1(27°C); (R1+R2)/2 = 1.67*). This is the factor by which the speed of the stage will decrease in a high-clock-rate application.

3.3.5 Leakage Currents

Leakage currents represent the limiting factor for high temperature functionality of MOSFETs. I_D versus V_{GS} curves represent a significant upward trend at temperatures above 250°C because drain leakage currents have become comparable to drain channel currents. The drain leakage current is typically four to five orders of magnitude smaller at 25°C than at 250°C. The drain or source junction leakage current is generally dominated by generation-recombination

leakage over a temperature range of 25°C to $T_{transition}$ °C, and by diffusion leakage

Figure 3.6 The variation in drain current in the equipment operating range of -55 to 125 deg. C is not very significant. [Blicher, 1981]



above $T_{transition}$ °C. Typically, in most CMOS processes, $T_{transition}$ °C lies in the range of 130°C to 150°C.

Leakage Currents in Strong Inversion and Deep Depletion. The leakage current components in an n-channel MOSFET in strong inversion comprise a drain and source well-bottom wall component, $I_B(T)$, which may be expressed as

$$I_B(T) = J_B(T).A_B \approx J_B(T).(W.d) \tag{3.61}$$

where $I_B(T)$ is the component of leakage current through the bottom wall of the well, W is the well width, and d is well length; a drain and source well-sidewall component, $I_{SW}(T)$, given as

$$I_{SW}(T) = J_{SW}(T).A_{SW} \approx J_{SW}(T).(W.x_j) \tag{3.62}$$

where W is the well width, and x_j is the well depth; a channel inversion-layer to body-junction leakage current component, $I_{CH}(T)$, given as

$$I_{CH}(T) = J_{CH}(T).A_{CH} \approx J_{CH}(T).(W.L_{eff}) \tag{3.63}$$

where L_{eff} is the effective channel length; and a substrate-to-well component, $I_{npwt}(T)$, which can be resolved into bottom and side wall components. For a device biased in deep depletion, no inversion layer is formed; thus the channel component of leakage current is eliminated. In a temperature range where the leakage currents are non-negligible, $T >$ 200°C, the temperature dependence of drain-to-body leakage currents, is represented as [Shoucair 1984]

$$I_R(T) = qA\frac{D_p}{L_P}.\frac{n_i^2(T)}{N_d}.\alpha AT^3 e^{-E_g(T)/kT} \tag{3.64}$$

where A is the area of the drain-to-body p-n junction, D_p is the diffusion constant (subscript p for p-channel or n for n-channel), L_p is the diffusion length (subscript p for p-channel or n for n-channel), $N_i(T)$ is the intrinsic carrier concentration, N_d is the substrate donor doping concentration (donor for p-channel or acceptor for n-channel), α is the constant of proportionality, and $E_g(T)$ is the band-gap energy, $\approx 1.2 - 2.73 \times 10^{-4} T$.

Subthreshold Leakage Currents. Subthreshold leakage current flows in a leakage path through the transfer device channel while the cell (word line) gate voltage is down and the device is off. The magnitude of the leakage current depends on how

well the transfer device channel can be turned off during standby, which in turn depends on the gate voltage and threshold voltage of the device. Even at the threshold voltage, the drain current is not truly zero and is of a 10^{-8} order of magnitude, multiplied by the width-to-length ratio of the device channel [Noble 1984]. Subthreshold leakage current is highly temperature-sensitive. In the subthreshold bias region, $|V_{GS}| < |V_{TH}(T)|$, and $|V_{DS}| >> kT/q$, the channel of the MOSFET is weakly inverted, and the drain current results from carriers diffusing from source to drain. The temperature dependence of drain current is represented by

$$I_D(T) \approx \mu(T)\left(\frac{W}{L}\right)\frac{C_{ox}^2}{C_{ox}+C_d}(n_o(T)kT)^2.e^{\frac{q(V_{GS}-V_{TH}(T))}{n_o(T)kT}-1} \qquad (3.65)$$

where C_d is the depletion capacitance of the space-charge region per unit area; and the temperature-dependent parameters are mobility $\mu(T)$, threshold voltage

Table 3.1 Variation in Intrinsic Carrier Concentration, Epitaxial Resistivity, and Collector-Emitter Saturation Voltage for Temperatures Between 20°C and 200°C. [Bromstead 1991]

Temperature (°C)	Intrinsic carrier concentration, n_i (cm^{-3})	Epitaxial resistivity (ohm-cm)	V_{CEsat} (volts)	
			Measured value	Calculated value
20	4.85×10^{9}	0.1103	0.55	0.2371
80	3.68×10^{11}	0.1486	0.60	0.3396
140	8.42×10^{12}	0.1952	0.72	0.4709
200	9.07×10^{13}	0.2496	0.85	0.6287

$V_{TH}(T)$, and subthreshold parameter $n_o(T)$ [Shoucair 1989]. The value of $n_o(T)$ increases exponentially with temperature beyond temperatures in the neighborhood of 150°C to 200°C (Figure 3.7). Beyond this range, the diffusion leakage currents completely dominate the weak inversion drain-current characteristics. Thus, the temperature at which the subthreshold parameter starts to increase exponentially denotes the reasonable upper operating limit of the device, above which no turn-off can be achieved. To make sure that the device does not make a significant contribution to node leakage at high temperatures, the device off-current must be maintained at 10^{-13} A, or five decades below the current at the voltage threshold level [Noble 1984].

3.3.6 Chip Availability

The signal loss due to leakage current is proportional to time. To prevent the signal from falling below the magnitude needed for sensing, the cells in a dynamic random access memory (DRAM) need to be refreshed periodically. Chip availability is defined as the time that the chip is actually available for read and write operations, mathematically represented as

$$Availability = \frac{t_1 - 2n.t_{cy}}{t_1}.100\% \tag{3.66}$$

$$t_1 = \frac{V_1.C_s}{I_{LJ}} \tag{3.67}$$

where t_1 is the refresh interval for a given cell, and t_{cy} is the amount of time spent actually performing the refresh operation [Noble 1984]. If a device with a 30-nm cell-oxide thickness and a 200-mV loss of cell voltage due to leakage is maintained at temperatures below 85°C to 95°C, the chip availability is in the neighborhood of 98% to 99%. Once a chip designed for operation at 85°C to 95°C is operated at temperatures greater than 100°C, the chip leakage current becomes so high that most of the time is used just to maintain the data in the cells [Noble 1984].

3.3.7 DC Transfer Characteristics

D.C. transfer characteristics maintain their integrity up to temperatures in the neighborhood of 270°C [Shoucair 1984, Marazas 1992, Zhu 1992]. At 275°C, the transfer characteristic degrades into a flat line, due to the onset of pn-pn latchup phenomenon (Figure 3.8). The peak low-level output voltage, V_{OLP}, decreases and the peak high-level output voltage, V_{OHP}, increases with temperature in the range of -50°C to 150°C. The noise margins thus increase with an increase in temperature (Figures 3.9 and 3.10).

The safe operating area of a typical MOSFET is shown in Figure 3.11. The d.c. or pulse drain currents are limited only by the power dissipation slope (I_D = max, allowable power dissipation/V_{DS}) and maximum allowable temperature. The slope in Figure 3.11 is for a device protected from second breakdown by either an external or a built-in clamp like the zenner diode, which breaks in advance of the MOS transistor drain breakdown.

Figure 3.7 Subthreshold parameter versus temperature. At temperature greater than 150-200 deg.C, diffusion leakage currents completely dominate the weak inversion drain characteristics, causing the subthreshold parameter n_o (T) to exponentially increase with temperature. Depending on the device design, the temperature at which the subthreshold currents start to increase exponentially, typically represents the practical upper operation junction temperature above which no reasonable device turn-off can be achieved. [Shoucair, 1989]

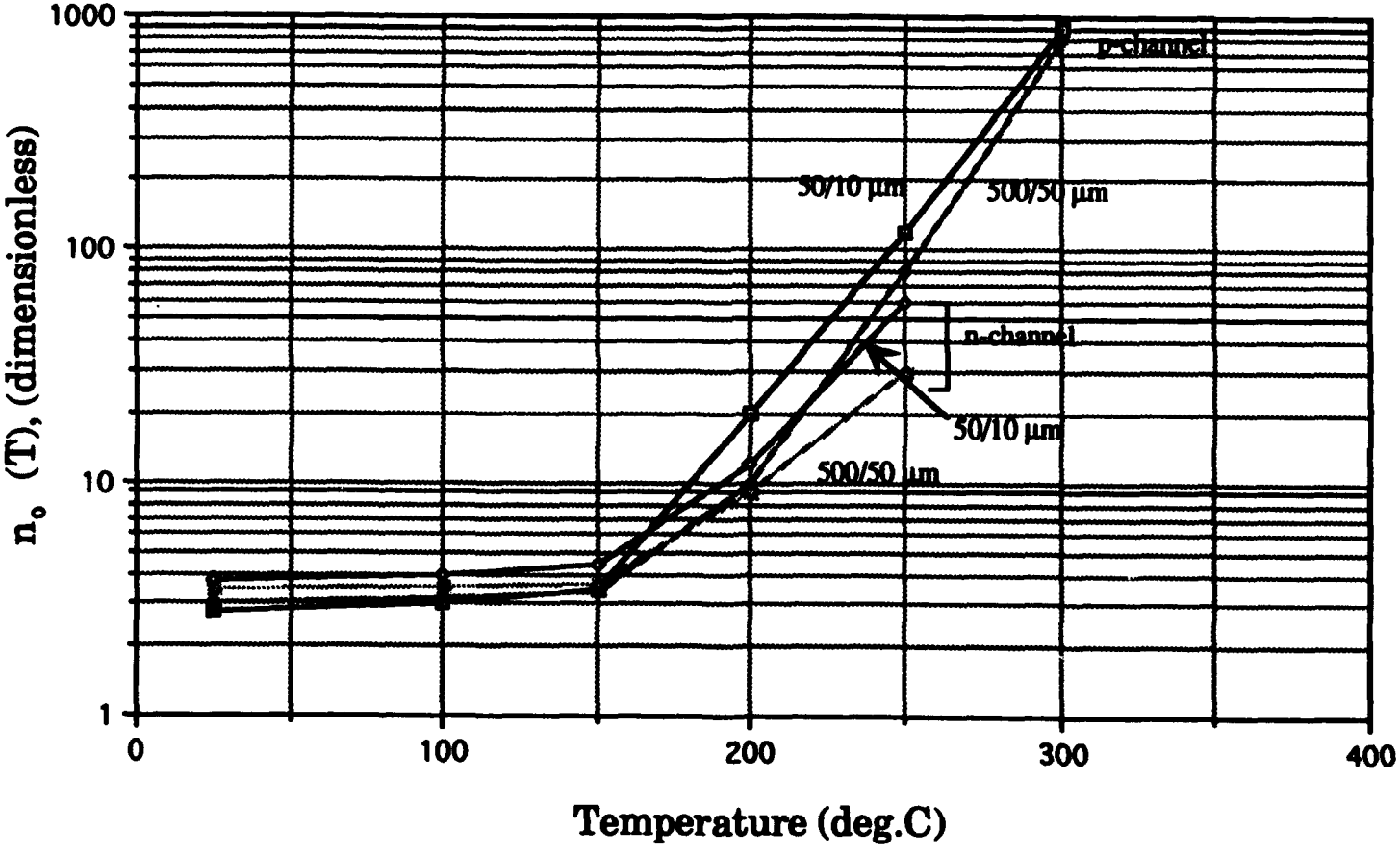


Figure 3.8 DC transfer characteristic of a typical CMOS inverter with temperature as a parameter. At temperature >270 deg.C, curves degenerate into a flat line due to onset of pnpn latchup phenomenon. [Shoucair, 1984]

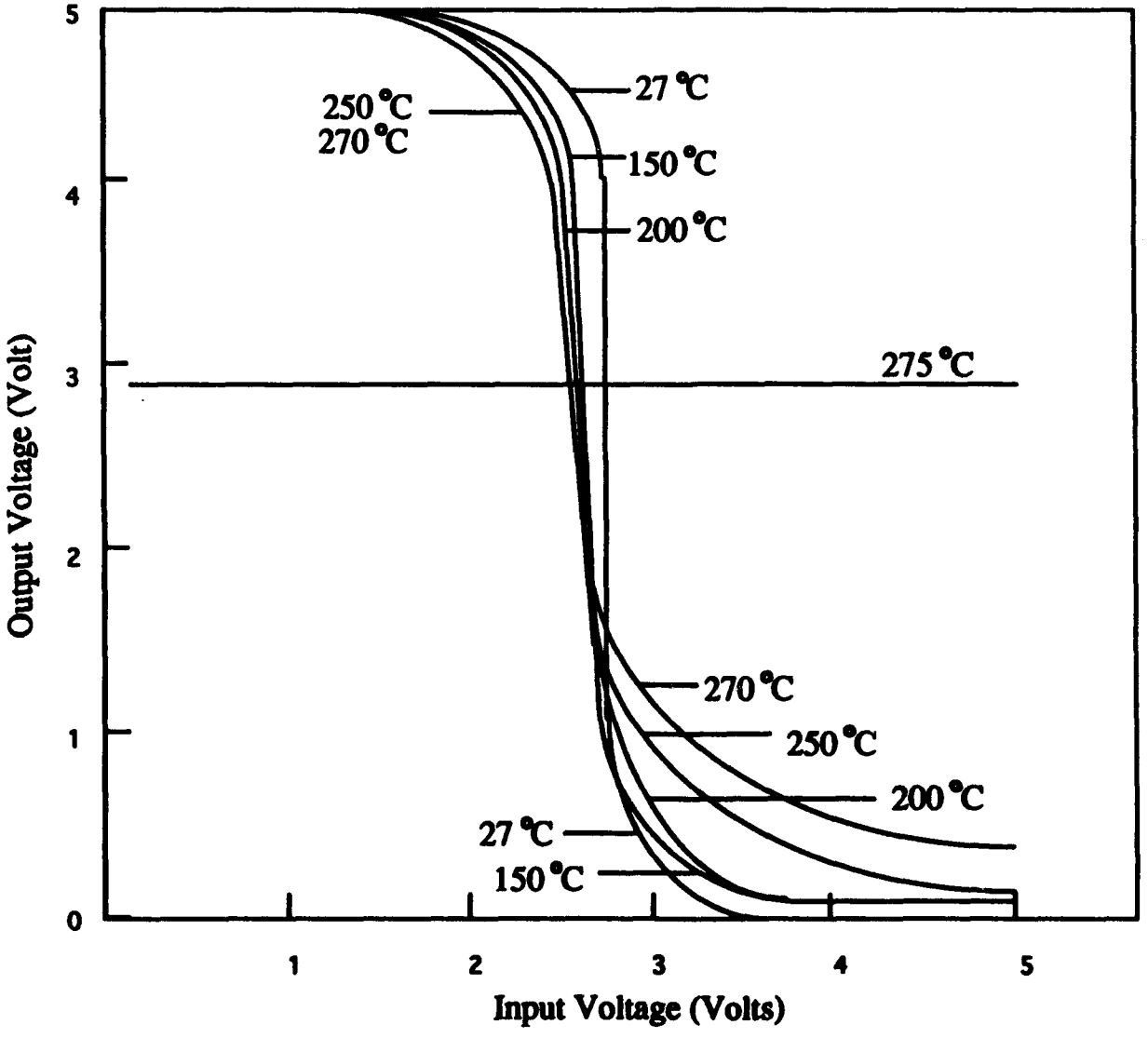


Figure 3.9 The variation in the peak low-level output voltage versus steady state temperature. The reduction in output indicates an increase in the noise margins at higher temperatures. [Texas Instruments, 1987]

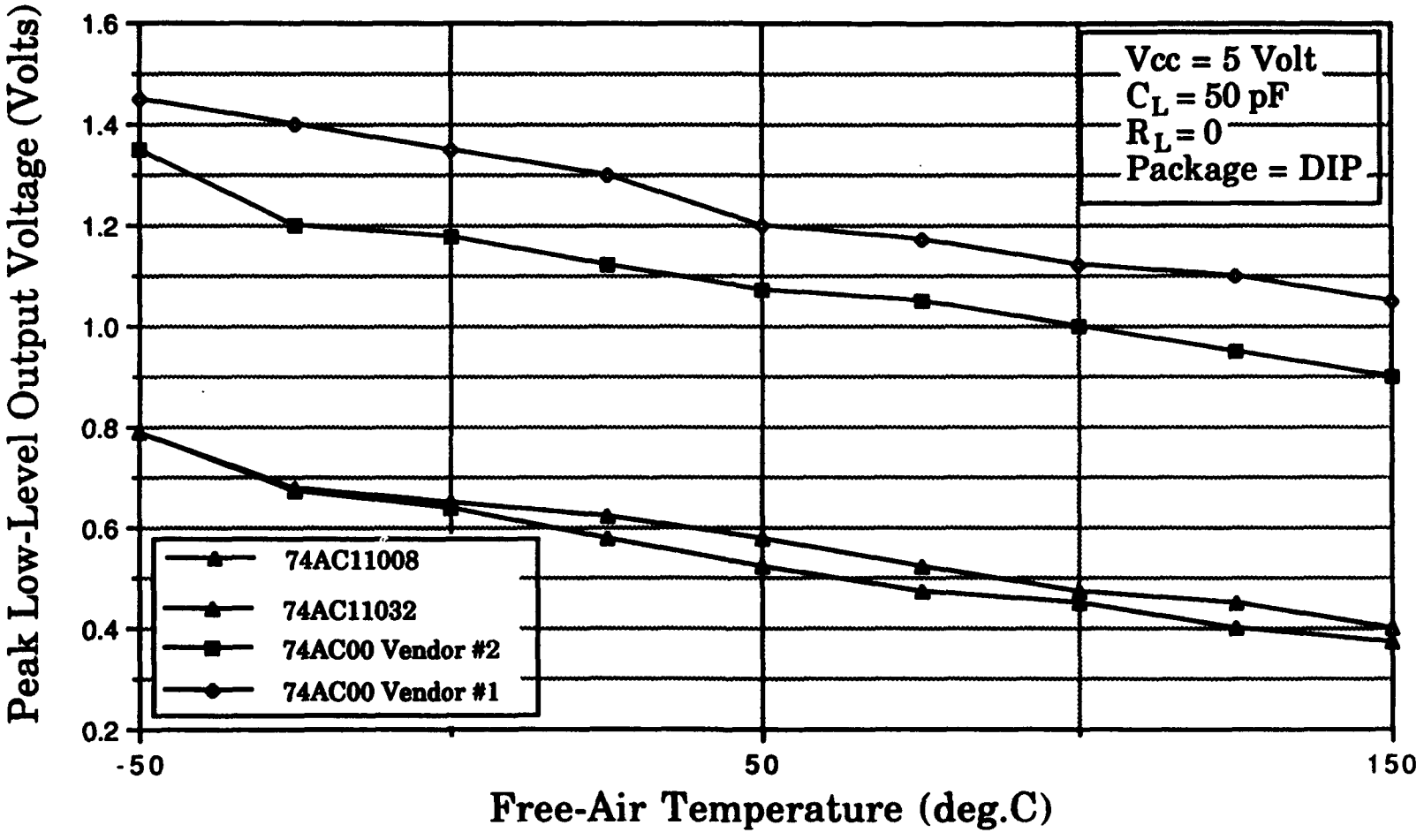


Figure 3.10 The variation in the peak high level output voltage versus steady state temperature. The increase in the output indicates an increase in noise margins at high temperatures. [Texas Instruments, 1987]

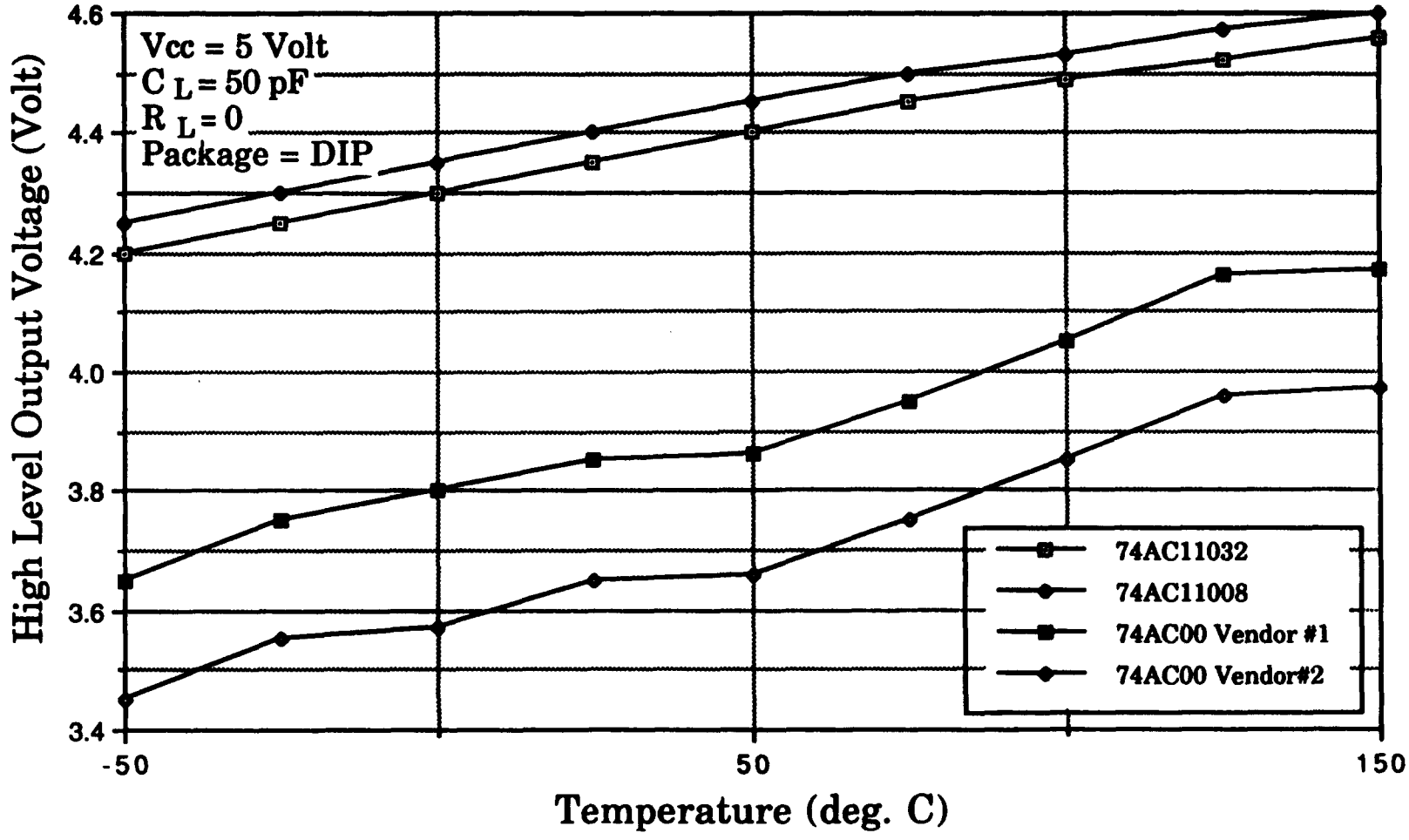
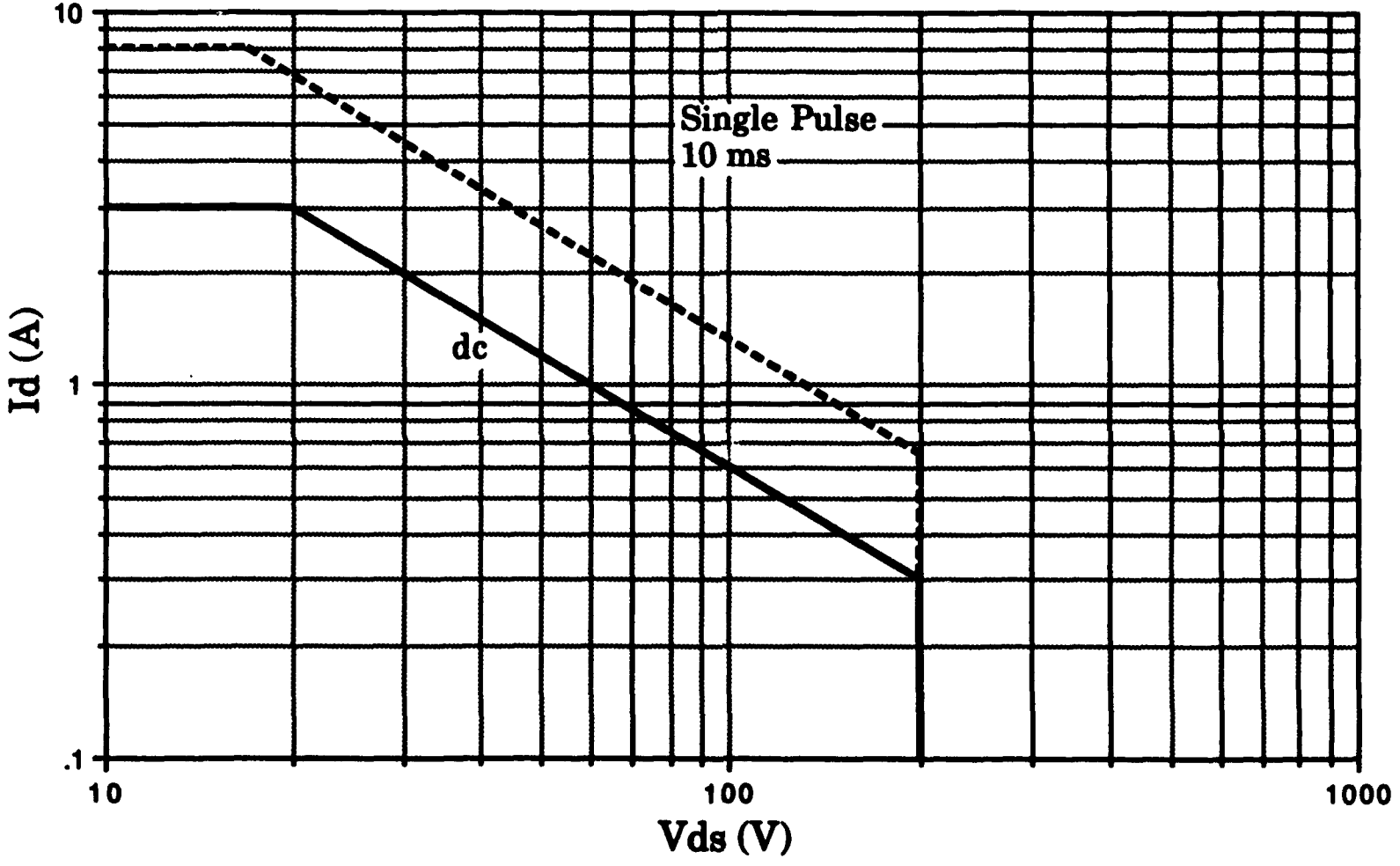


Figure 3.11 Typical Safe Operating Area (SOA) of a power MOST, with device protected from second breakdown [Blicher, 1981]



4

A PHYSICS-OF-FAILURE APPROACH TO IC BURN-IN

4.1 INTRODUCTION

Generally associated with microelectronic devices screening is a process that detects defects in a sub-population of devices that may exhibit early failure characteristics unlike the main population. Such defects occur due to variabilities in materials, manufacturing process, assembly process, workmanship, handling, or poor design. Defects are detected either through non-stress screens, like visual inspection and other non-destructive evaluation methods, or by stress screens, including burn-in, which involve the application of stress to precipitate defects on an accelerated basis.

Over the years, the process of burn-in has deteriorated into an insurance policy used to check reliability or to satisfy customer-imposed requirements. Burn-in procedures are often conducted without any prior verification of the nature of the defects to be precipitated, the failure mechanisms active in the device, their sensitivity to steady-state temperature stress, or quantitative evidence of the improvement achieved by the process. In fact, current failure data indicate that

burn-in prior to use does not remove many failures; on the contrary it may cause failures due to additional handling. This section examines the problems with existing burn-in methods and presents a physics-of-failure approach to burn-in.

4.2 BURN-IN PHILOSOPHY

Screening is a process to detect defects in devices in order to reduce or eliminate failures in the field, often under the assumption that the population of parts which fails early exhibit failure characteristics different from the main population, which lasts the designed-for life. Defects are either detected by non-stress screens, like visual inspection and other non-destructive evaluation methods, or by stress screens, which involve the application of stress (not necessarily service stresses) to precipitate defects often on an accelerated basis. Defects occur in devices due to variabilities in materials, manufacturing, process, assembly process, workmanship, handling, or poor design causing early occurrence of failures.

Good screens cause minimal damage to properly designed and manufactured components, while precipitating the defects that cause early failures in the life of the product. Additionally, the screen can aid in product development during prototype design, manufacture, assembly, handling, storage, and transportation, and arrive at the optimal combination of manufacturing and assembly process parameters. The development of a screen should be based on failure criteria and the results of a root-cause analysis. The failure criteria define device failure as an open, a short, or a limit on performance parameters, and the root-cause analysis determines the actual source of the failure in terms of improper manufacturing process parameters, design inconsistencies, failure mechanisms, and failure sites.

4.3 PROBLEMS WITH PRESENT APPROACH TO BURN-IN

Burn-in is a screen that subjects devices to extended operation at high temperatures in order to precipitate defects. A review of the burn-in practices used by some leading IC manufacturers reveals that even though burn-in has been regarded as a method for eliminating margir devices with defects from manufacturing aberrations, the specifics of burn-in vary (Table 4.1). Most companies have their own burn-in specifications for commercial products; MIL-STD-883 is used to satisfy burn-in requirements for military products. Other companies use only MIL-STD-883, but the selection of Method 1015 burn-in procedures for quality assurance also seems to be arbitrary.

Burn-in at present is a generic procedure consisting of a combination of time,

steady-state temperature, and electrical stress, not targeted toward any specific defect types or failure mechanisms. The emphasis is on empirical analysis, without any pointers to cost-effective application or subsequent manufacturing or assembly process modifications. The low precipitation of defects from burn-in results because very few microelectronic device failure mechanisms are steady-state temperature dependent. Yet, increased steady state temperature for prolonged periods seems to be the common approach to burn-in.

The misapplication of burn-in has its roots in the association of higher reliability with lowered steady-state temperature, which is generally considered a key parameter in the design of electronic equipment. Cautions about steady-state temperature are widely dessiminated. The widespread trust placed in the burn-in process is based on the assumption that failure mechanisms are steady-state temperature-dependent, even though it has generally not been determined whether steady-state temperature, temperature change, the rate of temperature change, or temperature gradients induce failure. Burn-in is typically a requirement imposed by the manufacturer demonstrate higher product reliability; manufacturers have different burn-in procedures for the same class of components for military and commercial customers. For example, TriQuant Semiconductor [Allen 1991] found while testing their GaAs ICs that burn-in was ineffective in actuating any failure mechanisms. The reasons were traced to device architecture and failure mechanisms that had no dependence on steady-state temperature. Components inserted into and extracted from sockets, temperature chambers, and pre-and post-test procedures can suffer additional handling damage in the form of bent leads and electrostatic discharge. An example of burn-in-actuated failures was observed by Swanson and Licari [1986], who examined the effects of burn-in on hybrid package hermeticity. They found that low leak rates before screening in many hybrid packages increased by over an order of magnitude after burn-in. Packages that maintained a leak rate of 10^{-9} atm-cc/sec after burn-in had a moisture content of 3,000 to 5,000 ppm after screening, compared with less than 1,000 ppm before. The increase in leak rates was attributed to the failure of glass-to-metal lead seals and lid seals, which were found to open during burn-in and close again. The increase in moisture was further attributed to outgassing of die and substrate attach epoxies inside the package.

Historically, ionic contamination has been the dominant mechanism precipitated by burn-in [Allen 1991]. Sodium, potassium, or ions in the oxide of silicon MOS devices under bias and temperature lead to junction leakage and threshold voltage shifts that cause failure. Cool-down under bias and retest within 96 hours of burn-in produces a relaxation of bias-induced charge separation. GaAs MESFET-based ICs have no oxide between the gate metallization and the surface of the channel -

- the interface is a Schotkky diode. Similarly, the MESFET device is unipolar, majority-carrier conducting, and reliant on the semi-insulating bulk material to achieve device isolation. There are no junctions and no leakage to consider.

In an effort to improve reliability, microelectronic manufacturers have often subjected devices to increasingly longer periods of burn-in. However, Motorola noted that most of the failures precipitated by burn-in occur in the first 160 device hours, with few or no failures over the next 1,000 hours. This is controlated by the fact that the long-term projected failure rate, based on the number of failures over 1,000 hours, is of the same order of magnitude as the actual measured failure rate over 1,000 hours [Motorola 1990].

4.4 A PHYSICS-OF-FAILURE APPROACH TO BURN-IN

4.4.1 Understanding Steady-State Temperature Effects

Microelectronic reliability is typically modeled with steady-state temperature-dependent models, such as the Eyring and Arrhenius models, originally proposed to model the effect of steady-state temperature on chemical reaction rates. These models predict electronic component failure rates under the assumption that the dominant component failure mechanisms depend on the steady-state temperature. However, most microelectronic device failure mechanisms are not highly steady-state temperature-dependent in the equipment operating range [Pecht, et al. 1991]. The use of burn-in without attention to the dominant failure mechanisms and the nature of their temperature dependencies is a misapplication of reliability concepts. Such use of burn-in may cause failure avoidance efforts, without yielding anticipated overall results, or expensive system implementations whose costs and complexities exceed the anticipated benefits in reliability. While burn-in can be used for certain types of failures that can be accelerated by steady-state temperature effects, more insight into the failure mechanism can yield better solutions in terms of design and processes.

Microelectronic design and corrective action are often misdirected because of the confusion between reliability and performance. Reliability is a measure of the ability of a device to fulfill its intended function. Device performance, defined by electrical parameters such as threshold voltage, leakage currents, and propagation delay, is dependent on steady-state temperature. While burn-in may not affect the reliability of the device, it may uncover the fact that at high temperature, the device does not meet performance requirements. This may serve as an indicator for a design change, or for the unsuitability of the technology for high-temperature operation. Burn-in, where performance is checked after the temperature is

lowered, will not uncover this type of problem.

Temperature-cycle dependence is often confused with steady-state temperature dependence. Temperature cycle is a change in temperature that may impose a cyclic stress on the component, due to thermal mismatch at the interfaces of package elements; accelerate intermetallic formation at bimetallic interfaces; or cause stress-induced diffusive voiding in metallization, due to creep-stress relaxation mechanisms. Temperature-cycle stress imposes cumulative damage on the component in the form of thermo-mechanical fatigue. Burn-in is currently only a single temperature cycle.

4.4.2 Setting Up The Burn-In Profile

A physics-of-failure approach to burn-in considers the potential material defects, design inconsistencies, and manufacturing variabilities for each process that could cause defects in the product. The burn-in methodology is an iterative process consisting of the following major steps:

- *Identify failure mechanisms, failure sites and failure stresses:* Development of a burn-in program encompasses identifying potential failure mechanisms, failure sites, and failure stresses, active in a device technology. The burn-in process must be tailored to specific failure mechanism(s) at specific potential failure site(s) in order to be effective. The failure mechanism(s) and failure sites(s) depend on the materials and product processing technologies. Burn-in conditions are therefore specific to the manufacturing technology and hardware. The manufacturing sequence should be studied and possible defects, introduced due to the processing variabilities at each manufacturing stage, should be identified. The dominant failure stresses accelerating the failure mechanisms can be identified based on knowledge of the damage mechanics. The burn-in stress sequence will encompass those stresses that serve as dominant accelerators of the failure mechanisms.
- *Identify the combination of stresses to activate the identified failure mechanisms cost-effectively:* Typically, there may be a number of failure mechanisms dominant in a device technology; each may have a dominant dependence on a different stress. Thus, in order to activate all the failure mechanisms, the dominant stresses need to be applied simultaneously and cost-effectively. To quantitatively determine the magnitude of stresses necessary to activate the failure mechanisms and arrive at the desired cost-effective combination of stresses, models must be developed for each failure mechanism, as a function of stresses, device geometry, material, and magnitude of defects and design

inconsistencies. The quantitative models, however, can aid only in relating the magnitude of a particular type of stress to manufacturing flaws and design inconsistencies, based on physics-of-failure concepts. The real case is more complex, involving interactions of stresses causing failure earlier than predicted by superposition of different stresses acting separately. There may be more than one failure mechanisms in a device technology. Each of the mechanisms will have its own dependence on steady state temperature, temperature cycle, temperature gradient, and time dependent temperature change. An ideal case will be when an optimized combination of the relevant stresses is used to activate the failure mechanisms in a cost effective manner. The desired combination of stresses is a function of the physics of the failure mechanism, and response of package material and configuration. The approach to arriving at the desired stress level consists of subjecting the components to discrete stress levels of steady state temperature, temperature cycle, temperature gradient, time dependent temperature change, and voltage. The selection of the temperature stress level should be based on knowledge of designed-for temperature of the device, the temperature of the device during operational life and the thresholds for various failure mechanisms. Conducting step stress and HAST tests for various magnitudes of each type of stress applied separately will give failure results in terms of number of cycles to failure, failure mechanisms activated, and failure sites. From the test results the stress levels required for activation of failure mechanisms will be identified.

- *Conduct burn-in and evaluate effectiveness:* Burn-in should be assessed based on root cause failure analysis of the failed components, revealing the failure mechanisms, failure modes, and failure sites. Inappropriate burn-in stresses will either damage good components by activating mechanisms not otherwise noticed in operational life, or allow defective parts to go through. To make sure the stress level is right, the amount of damage (or the life consumed) in the case of the products without defects ("good" products) must be evaluated and the stress levels modified if necessary. Product reliability (due to the design improvements) must be used as the index for subsequent burn-in decisions. Physics of failure approach is used to determine the effective acceleration of device dominant failure mechanisms and is given by: $A_{eff} = (A_T A_v A_x \ldots)$. Acceleration factors for dominant failure mechanisms are used to determine burn-in time (t_{bi}) and temperature (T_{bi}). The effective burn-in time is given by: $t_{eff} = (A_T A_v A_x \ldots) t_{bi}$. [Jensen 1982]
- *Decisions regarding burn-in modifications and in-process monitors:* The above steps should be repeated until all products have the required expected life, with an optimized return on investment. The burn-in process should be augmented

(supplemented or complemented) with in-line process controls to attain the desired quality and reliability. The physics of failure models along with the burn-in results will determine the optimal manufacturing stress levels and process parameters for minimal defect levels. The in-line process controls will ensure that the process parameters are maintained at their optimal values to minimize the occurrence of defects.

Economic analysis should indicate whether the burn-in should be continued or modified. A cost-effective burn-in program addresses all the relevant failure mechanisms by employing a minimum set of devices. Burn-in is recommended for all products which are in the development stage and do not have a mature manufacturing process. Burn-in at this stage not only improves the reliability of the products but also assists in determining product and process (manufacturing, assembly, testing) corrective actions. Products with a standardized design and a relatively mature process need burn-in only if the field failure returns indicate infant mortality. A cost analysis and return on investment is conducted to calculate the economics of the burn-in program. Analysis of cost and return of investments based on the customer satisfaction and the hidden factory costs (the costs associated with the factory-inputs which do not add value to the product, like product inspection, testing, rework, etc.) determine the profits to an organization. Burn-in economics are critical in convincing management about the benefits that accrue from burn-in and provide a benchmark for making improvements in the next burn-in "cycle".

Table 4.1 Burn-in Time and Temperatures

Source	Min. Temp. T_A (°C)	Time (hours)	Test Condition	Comments
MIL-STD-883 Method 1015	100, 105, 110, 115, 120	Class B: 352, 300, 260, 220, 190	Hybrids Only	Either of the combinations of the cited temperature and time is used for burn-in of hybrids.
	125	Class S: 240 hours Class B: 160 hours	A - E	Any of the specified combinations of temperature and time can be used for burn-in according to Method 1015 of MIL-STD-883. The various conditions of burn-in are defined by the electrical stress, steady state temperature (ranging from 100°C to 250°C), and time period (12 to 352 hour). Conditions include: • Test Condition A: Steady state temperature, reverse bias • Test Condition B: Steady state temperature, forward bias • Test Condition C: Steady state temperature, power and reverse bias • Test Condition D: Parallel excitation • Test Condition E: Ring excitation • Test Condition F: Temperature accelerated test [MIL-STD-883C, 1983; last revision incorporated 1990]
	130	Class S: 208 hours Class B: 138 hours	A - E	
	135	Class S: 180 hours Class B: 120 hours	A - E	
	140	Class S: 160 hours Class B: 105 hours	A - E	
	145	Class S: 140 hours Class B: 92 hours	A - E	
	150	Class S: 120 hours Class B: 80 hours	A - E	
	175	Class B: 48 hours	F	
	200	Class B: 28 hours	F	
	225	Class B: 16 hours	F	
	250	Class B: 12 hours	F	
INTEL Corporation Intel Spec. MIL-STD-883 Method 1015,	125°C 125°C	Memory Products: 48 hours Military Products: 160 hours	Method 1015, Condition C, or D	Dynamic burn-in [Intel, 1989; Intel, 1990]

Advanced Micro Devices Inc. **MIL-STD-883 Method 1015**	125°C Min.	Military Products: 240 hours	Method 1015, Condition C or D	[Advanced Micro Devices, 1990]
LSI Logic Corporation **MIL-STD-883 Method 1005**	125°C	48 hours	Static or DC burn-in; Dynamic burn-in	The results of production burn-in are measured as a percentage fallout rate or PDA (Percent Defective Allowable). The PDA calculation is simply the reject rate, the number of failures divided by the total number of devices in the lot, and the result compared against target PDA. [LSI Logic, 1990]
Texas Instruments Inc. **MIL-STD-883 Method 1015** **MIL-STD-883 Method 1015** **Power Burn-in MIL-STD-750, Method 1039**	125°C Min. 25°C	MOS Memory and LSI JAN S, Monitored line, SEQ: 240 hours Optocoupler screening: JAN, JANTX, JANTXV 4N22, 4N23, 4N24JAN, JANTX, JANTXV 4N22A, 4N23A, 4N24A; 168 hours	 V_{CC} = 20 Vdc V_{CE} = 10±5 Vdc PT = 275±25 mW I_F = 40 mA	PDA = 5% [Texas Instruments, 1988]

Motorola Inc.				
Monitored Burn-in	125°C 85°C	6 hours 10 minutes	Electrical and parametric measurement	Monitored burn-in is a technique in which devices are operated at elevated temperature and voltage for an extended period, followed by short duration at a lower temperature and voltage during which parametric and functional tests are performed [Eachus, MOTOROLA, 1984]. The test sequence consists of two stages which include: • Temperature is increased from ambient to 125°C in 15 minutes and kept at that temperature for 6 hours. • Temperature is lowered from 125°C to 85°C and allowed to stabilize for 10 minutes before electrical and parametric measurements are performed.[MOTOROLA, 1991]
Integrated Device Technology Inc.				
MIL-STD-883 Method 1015	125°C Min.	Military Products: 160 hours	Method 1015, Condition D	[Integrated Device Technology, 1989]
IDT Spec.	125°C Min.	Commercial Products: 16 hours	Method 1015, Condition D	
MIL-STD-883 Method 1015	125°C Min.	Military Hermetic Modules: 44±4 hours		
Cypress Semiconductor Inc.				
Cypress Semiconductor Spec.	150°C	Level 2 plastic and hermetic parts: 12 hours		Either of the conditions is used [Cypress Semiconductor, 1990]
MIL-STD-883 Method 1015	125°C Min., or 150°C	JAN, SMD/Military Grade Products: 160 hours 80 hours	Method 1015, Condition C or D	
	125°C	Military Grade Modules: 48 hours		

5

DERATING GUIDELINES FOR TEMPERATURE-TOLERANT DESIGN OF MICROELECTRONIC DEVICES

5.1 INTRODUCTION

Derating is a technique through which either the stresses acting on a part are reduced, or the strength of the part is increased, in correspondence with allocated or rated strength stress factors. Manufacturers of microelectronic devices often specify supply voltage limits and threshold values for power dissipation, junction temperature, frequency, and output current. Given these rated values, the equipment designer often elects to arbitrarily derate, or lower the allowed values, to provide a safety factor or "factor of ignorance". When the equipment designer decides to select an alternative component or make a design change that maintains the operational condition for a specific parameter, such as temperature, consistently below the rated level, the component is said to have been derated for thermal stress. Thermal derating is one of the most common derating methodologies, but is not the only one. The reliability of electronic systems is,

obviously, very sensitive to component derating and exactly how the derating is applied.

5.2 PROBLEMS WITH THE PRESENT APPROACH TO DEVICE DERATING

Currently, the thermal derating criteria vary among government acquisition agencies. Westinghouse has a set of derating guidelines for electronic components, in which ECL, TTL, and CMOS digital components, linear devices, and hybrids are equally derated for thermal stress. Derating for thermal stress involves reducing the maximum operating temperature to around $0.6T_j$ (maximum junction temperature). Rome Laboratories has a set of derating guidelines in which microcircuits that have been grouped as: complex, digital, hybrid, linear, and memory are derated to operate at a lower operating temperature. The exact value of the operating temperature depends on the derating level. There are three derating levels, depending on the level of criticality of the component. In all cases, derating for thermal stress involves lowering the maximum junction temperature.

Implicit in such a derating methodology is the assumption that steady-state temperature is a dominant accelerator of microelectronic device failure mechanisms. Even in microelectronic technologies where temperature is a dominant failure accelerator, steady-state temperature thresholds, affecting device sensitivity to various forms of temperature stress, are a function of device architecture, materials, manufacturing defects, and other non-temperature-related operational stresses. Assigning a generic value of lower temperature to a technology, based on the assumption that all devices operating at that lower value of temperature will be reliable, is thus arbitrary.

Thermal-stress derating guidelines rule out the option of reliable system designs at higher temperatures. In addition, they give the designer a false sense of security about achieving increased reliability at lower temperatures. Lower temperatures may not necessarily increase reliability, since some of the failure mechanisms are inversely dependent on temperature; for example, device technologies with hot electrons as the dominant mechanism may have lower reliability at lower temperatures.

Current thermal derating guidelines do not account for the dominant failure mechanisms or their temperature dependencies. Temperature-cycle effects that have not been accounted for in device derating criteria are failure accelerators at mating interfaces. The maximum number of temperature cycles that the device can endure is a function of fatigue failure mechanisms, such as wire-interconnect

fatigue, die fracture, or die and substrate attach fatigue. These mechanisms may or may not be dominant in the device architecture, depending on the stresses generated at the mating interfaces, which are a function of interface geometry, and on material characteristics, including CTE mismatches.

Typically, localized temperature gradients exist in the chip metallization, chip, substrate, and package case, due to sudden variations in the conductivities of material produced by defects in the form of voids or cracks. The locations of maximum temperature gradients in chip metallization are sites for mass transfer mechanisms, including electromigration. Electromigration is also accelerated by temperature and current density. Therefore, device reliability, for mechanisms with a dominant dependence on more than one operating stress, (temperature and non-temperature) complicated by dependence on magnitudes of manufacturing defects, needs to be maximized by more than just lowering temperature, as existing derating criteria do.

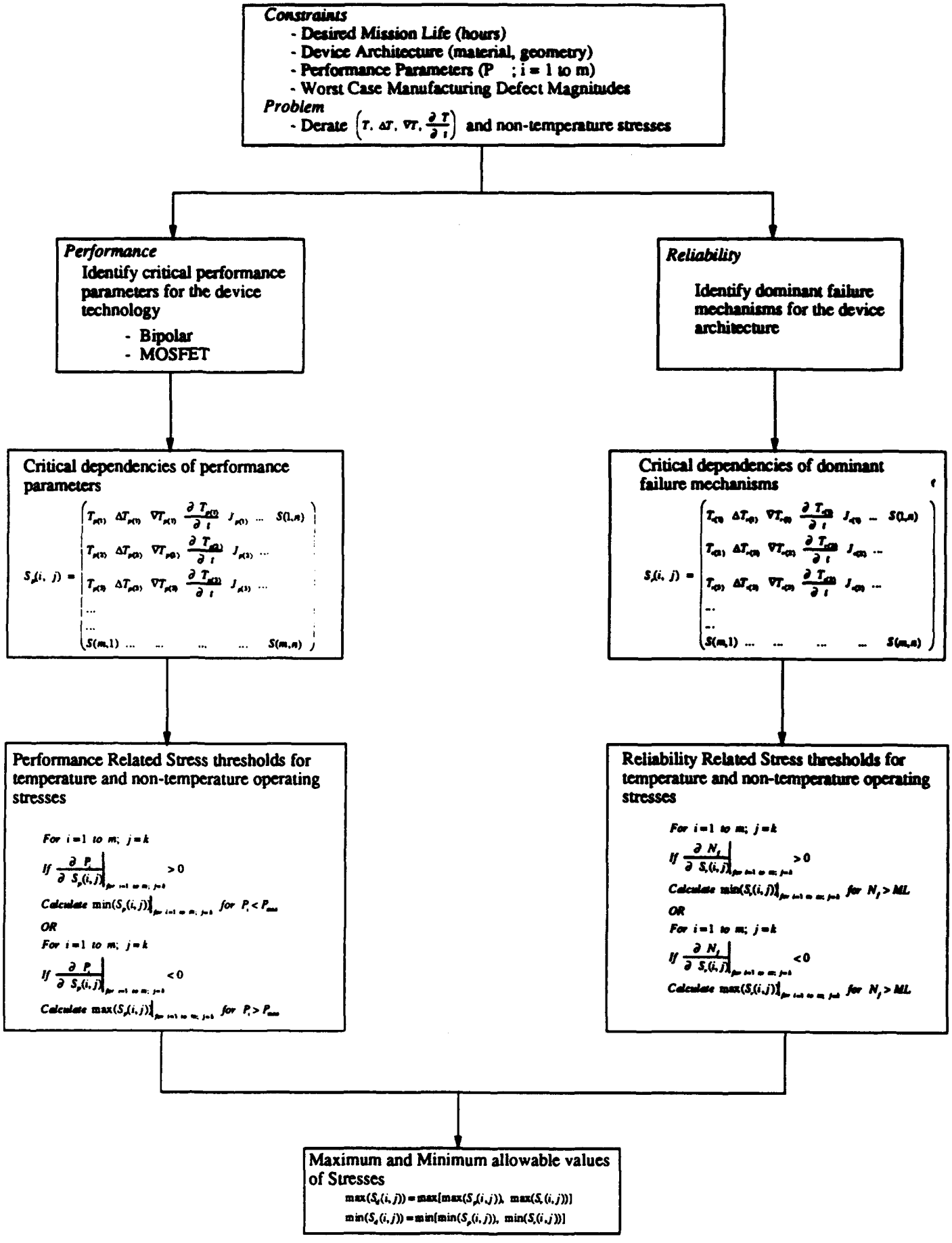
The interaction of various temperature and non-temperature stresses modifies the dominant dependence of the failure mechanisms on one or more of the stresses. Temperature transients generated by the duty cycle (ON/(ON+OFF)) modify the dependence of the metallization corrosion on steady-state temperature. At low duty cycle values, metallization corrosion has a dominant dependence on steady state-temperature. However, at higher values ($\approx$ in neighborhood of 1.0), metallization corrosion has a dominant dependence on duty-cycle and a mild dependence on steady-state temperature.

5.3 A PROPOSED APPROACH TO DEVICE DERATING

The derating problem for dominant stress acclerators for a particular device architecture requires derating the stress with maximum sensitivity with respect to life in order to achieve optimization. Some stresses can be easily controlled, while others may be hard to derate because they are a function of device architecture. Therefore, the practical situation may disclose that the most effective parameter is not the easiest to derate. The approach presented here allows the evaluation of the relative sensitivity of operating life to various stresses. Once the dominant stresses have been identified, the stresses which dramatically effect life, and which are also the easiest to control, are derated (Figure 5.1).

The derated values of steady-state temperature, temperature cycle magnitude, temperature gradient, and time-dependent temperature change, including non-temperature operating stresses, are determined for a desired device mission life.

Figure 5.1 Derating Methodology for Temperature Tolerant Design



Calculated derated levels of temperature and non-temperature operating stresses for devices using approach are specific to a design architecture and cannot be generalized to a device technology. The derating problem can thus be stated as follows:

$$\begin{aligned} &\textit{constraints:} \\ &\quad \textit{desired mission life(hours)} \\ &\quad \textit{device architecture (material, geometry)} \\ &\quad \textit{performance parameters}(P_i;\ i=1 \textit{ to } m)) \\ &\quad \textit{worst case manufacturing defect magnitudes} \\ &\textit{problem:} \\ &\quad \textit{derate}\left(T,\ \Delta T,\ \nabla T,\ \frac{\partial T}{\partial t}\right) \textit{and non-temperature stresses} \end{aligned} \tag{5.1}$$

where $P_i(i=1 \textit{ to } m)$ are the critical device performance parameters. Derating stress values involves addressing both performance and reliability requirements. While derating for performance evaluates stress influence on critical device parameters, derating for reliability involves evaluation of stress influence on device life under dominant failure mechanisms.

Device parameters considered in derating for performance are a function of device technology, which, for BJT devices, includes device thermal voltage, current gain, and the invertor voltage transfer characteristic and for MOSFET devices includes, threshold voltage, the invertor voltage transfer characteristic, and the invertor propagation delay:

$$\textit{Performance} = \begin{cases} f(V_{thermal},\ \beta,\ IVTC) & \textit{for BJT devices} \\ f(V_{threshold}, IVTC, IPD) & \textit{for MOSFET devices} \end{cases} \tag{5.2}$$

where $V_{thermal}$ is the thermal voltage, β is the device current gain, $V_{threshold}$ is the threshold voltage, $IVTC$ is the invertor voltage transfer characteristic, and IPD is the invertor propagation delay. Threshold values for temperature and non-temperature stresses that cause the critical parameters of the device technology to exceed acceptable ranges are calculated based on closed-form models relating device architecture to critical parameters.

$$S_p(i,j) = \begin{pmatrix} T_{p(1)} & \Delta T_{p(1)} & \nabla T_{p(1)} & \frac{\partial T_{p(1)}}{\partial t} & J_{p(1)} & E_{p(1)} & \cdots & S(1,n) \\ T_{p(2)} & \Delta T_{p(2)} & \nabla T_{p(2)} & \frac{\partial T_{p(2)}}{\partial t} & J_{p(2)} & E_{p(2)} & \cdots & \cdots \\ T_{p(3)} & \Delta T_{p(3)} & \cdots & & & & & \cdots \\ \cdots & & & & & & & \cdots \\ \cdots & & & & & & & \\ S(m,1) & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & S(m,n) \end{pmatrix}$$

where S_p is a (m x n) matrix of threshold stress values for device performance. The m rows correspond to m (i.e., $p(i)$, for $i = 1$ to m) critical parameters for the device technology (such as threshold voltage, the invertor voltage transfer characteristic, and the invertor propagation delay, for MOSFET devices). The n columns correspond to the n temperature and non-temperature stresses that affect the critical parameters. The acceptable range of stress values for device performance is calculated as follows:

$$For\ i = 1\ to\ m;\ j = k$$
$$If\ \left.\frac{\partial P_i}{\partial S_p(i,j)}\right|_{\substack{for\ i = 1\ to\ m \\ j=k}} > 0\ ;\ calculate\ \min(S_p(i,j))\Big|_{\substack{for\ i = 1\ to\ m \\ j=k}}\ for\ P_i < P_{max} \tag{5.4}$$

$$For\ i = 1\ to\ m;\ j = k$$
$$If\ \left.\frac{\partial P_i}{\partial S_p(i,j)}\right|_{\substack{for\ i = 1\ to\ m \\ j=k}} < 0\ ;\ calculate\ \max(S_p(i,j))\Big|_{\substack{for\ i = 1\ to\ m \\ j=k}}\ for\ P_i > P_{min} \tag{5.5}$$

where k represents a particular stress value.

The device life, determined by dominant failure mechanisms actuated by temperature and non-temperatures stresses, is used to derate for reliability. The influence of stresses on device life is quantified by closed-form models. The threshold stress values that result in a device life less than the desired mission life are calculated by

$$S_r(i,j) = \begin{pmatrix} T_{r(1)} & \Delta T_{r(1)} & \nabla T_{r(1)} & \frac{\partial T_{r(1)}}{\partial t} & J_{r(1)} & E_{r(1)} & \cdots & S(1,n) \\ T_{r(2)} & \Delta T_{r(2)} & \nabla T_{r(2)} & \frac{\partial T_{r(2)}}{\partial t} & J_{r(2)} & E_{r(2)} & \cdots & \cdots \\ T_{r(3)} & \Delta T_{r(3)} & \cdots & & & & & \cdots \\ \cdots & & & & & & & \cdots \\ \cdots & & & & & & & \\ S(m,1) & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & S(m,n) \end{pmatrix}$$

where S_r is a matrix of threshold stress values for device reliability (m x n). The m rows correspond to m (i.e., $p(i)$, for i = 1 to m) dominant failure mechanisms. The n columns correspond to the n temperature and non-temperature stresses that affect device life limitations resulting from the different failure mechanisms. The acceptable range of stress values for device reliability is calculated as follows:

$$\textit{For } i = 1 \textit{ to } m;\ j = k$$
$$\textit{If } \left.\frac{\partial N_f}{\partial S_r(i,j)}\right|_{\substack{\textit{for } i = 1 \textit{ to } m \\ j=k}} > 0 \ ; \ \textit{calculate } \min(S_r(i,j))\big|_{\substack{\textit{for } i = \textit{to } m \\ j=k}} \ \textit{for } N_f > ML \tag{5.7}$$

$$\textit{For } i = 1 \textit{ to } m;\ j = k$$
$$\textit{If } \left.\frac{\partial N_f}{\partial S_r(i,j)}\right|_{\substack{\textit{for } i = 1 \textit{ to } m \\ j=k}} < 0 \ ; \ \textit{calculate } \max(S_r(i,j))\big|_{\substack{\textit{for } i = \textit{to } m \\ j=k}} \ \textit{for } N_f > ML \tag{5.8}$$

where k represents a particular stress value, i represents a particular failure mechanism, N_f is the predicted time to failure due to a failure mechanism, and ML is the required device mission life. The maximum and minimum allowable values of stresses are then determined as:

$$\begin{aligned} \max(S_d(i,j)) &= \max[\max(S_p(i,j)),\ \max(S_r(i,j))] \\ \min(S_d(i,j)) &= \min[\min(S_p(i,j)),\ \min(S_r(i,j))] \end{aligned} \tag{5.9}$$

where $\max(S_r(i,j))$ is the maximum allowable stress value derived from reliability

considerations, $\max(S_p(i,j))$ is the maximum allowable stress value derived from performance considerations, and $\max(S_d(i,j))$ is the maximum allowable stress value for the device. Min represents the minimum values of the individual stresses. Maximum values are specified for stresses directly proportional to detrimental effects on package reliability and performance. Minimum values are specified for stresses with an inverse influence on package performance or reliability.

Physics-of-failure concepts have been used to relate allowable operating stresses to design strengths through quantitative models for failure mechanisms. Failure models have been used to assess the impact of derating on the effective reliability of the component for a given load. The quantitative correlations outlined between derating and reliability will enable designers and users to tailor the margin of safety more effectively to the level of criticality of the component, leading to better and more cost-effective utilization of the functional capacity of the component.

5.4 DERATING FOR FAILURE MECHANISMS IN DIE METALLIZATION

5.4.1 Corrosion of Die Metallization

Metallization corrosion has a dominant dependence on two temperature stresses - steady-state temperature and time-dependent temperature change. Temperature transients generated by the duty cycle (ON/(ON+OFF)) modify the dependence of the metallization corrosion on steady- state temperature. At low values of the duty cycle, metallization corrosion has a dominant dependence on steady-state temperature; however, at higher values ($\approx$ in neighborhood of 1.0), metallization corrosion has a dominant dependence on the duty cycle and a mild dependence on steady-state temperature. Time to failure due to metallization corrosion has been modelled as the sum of induction time and corrosion time [Pecht 1990]. Calculate T_{max} and $(\partial T/\partial t)_{max}$ such that:

$$T_{operation} < T_{max}$$
$$\frac{\partial T}{\partial t} < \left(\frac{\partial T}{\partial t}\right)_{max} \qquad (5.10)$$

Table 5.1 Derating Guidelines For Thermal Derating

Microcircuit Manufacturer/ Acquisition Agency	Component Type		Derating Criteria (max. allowable junction Temperature)
Westinghouse Electric [Westinghouse 1986]	digital: TTL/ECL		0.6 $T_{J(Rated)}$
	digital: CMOS		0.6 $T_{J(Rated)}$
	linear, amplifiers		0.6 $T_{J(Rated)}$
	linear, regulators		0.6 $T_{J(Rated)}$
Rome Laboratories [RADC-TR-82-177 RADC-TR-84-254]	complex (LSI, VLSI, VHSIC)	derating level 1	85°C
		derating level 2	100°C
		derating level 3	125°C
	digital	derating level 1	85°C
		derating level 2	100°C
		derating level 3	110°C
	hybrid	derating level 1	85°C
		derating level 2	100°C
		derating level 3	125°C
	linear	derating level 1	80°C
		derating level 2	95°C
		derating level 3	105°C
	memory	derating level 1	85°C
		derating level 2	100°C
		derating level 3	125°C
Naval Air Systems Command [AS-4613, 1976]	digital: TTL/ECL	class C	$T_{max(rated)}$ - 20°C
		class B	$T_{max(rated)}$ - 25°C
		class A	$T_{max(rated)}$ - 30°C
	digital: CMOS	class C	$T_{max(rated)}$ - 20°C
		class B	$T_{max(rated)}$ - 20°C
		class A	$T_{max(rated)}$ - 30°C
	linear, amplifiers	class C	$T_{max(rated)}$ - 20°C
		class B	$T_{max(rated)}$ - 25°C
		class A	$T_{max(rated)}$ - 30°C

$$T_{f(corr)} > \textit{mission life} \tag{5.11}$$

where

$$T_{f(corr)} = \tau_{INDUCTION} + \tau_{CORROSION}$$

$$\tau_{INDUCTION} = -\frac{4L^2}{\pi^2 D}\ln\left(1 - \frac{P_{in}}{P_{out}}\right) \quad \textit{For nonhermetic package} \tag{5.12}$$

$$= \textit{From figure} \quad \textit{For hermetic package}$$

$$\tau_{CORROSION} = \frac{k_1 k_2 k_3}{k_4}\frac{w^2 hndF}{4MV}\frac{\rho}{Z}$$

and

$$k_3 = \frac{1}{(1 - DC)^{10DC - 1}} \tag{5.13}$$

$$K_4 = \frac{(RH_R)^n \exp(E_a/KT_R)}{(RH)^n \exp(E_a/KT)} \tag{5.14}$$

where:

RH_R	is a reference relative humidity (%);
E_a	is an activation energy (eV);
K	is the Boltzmann constant (eV/° K);
n	is a material constant;
T_R	is a reference temperature (°K);
DC	is the duty cycle;
M	is the atomic weight of a metal conductor of density d, width w, height h, and chemical valence n;
ρ/Z	is the sheet resistance of the electrolyte;

Table 5.2 Physical and Chemical Properties of Metallization Materials [Pecht and Ko 1991]

Material	Physical Property Index (k_1)	Atomic Weight (M)	Density (d)	Chemical Valence (n)
Aluminum	0.1	27	2.7	3
Copper	0.7	64	8.9	2
Gold	1.0	197	19.32	3

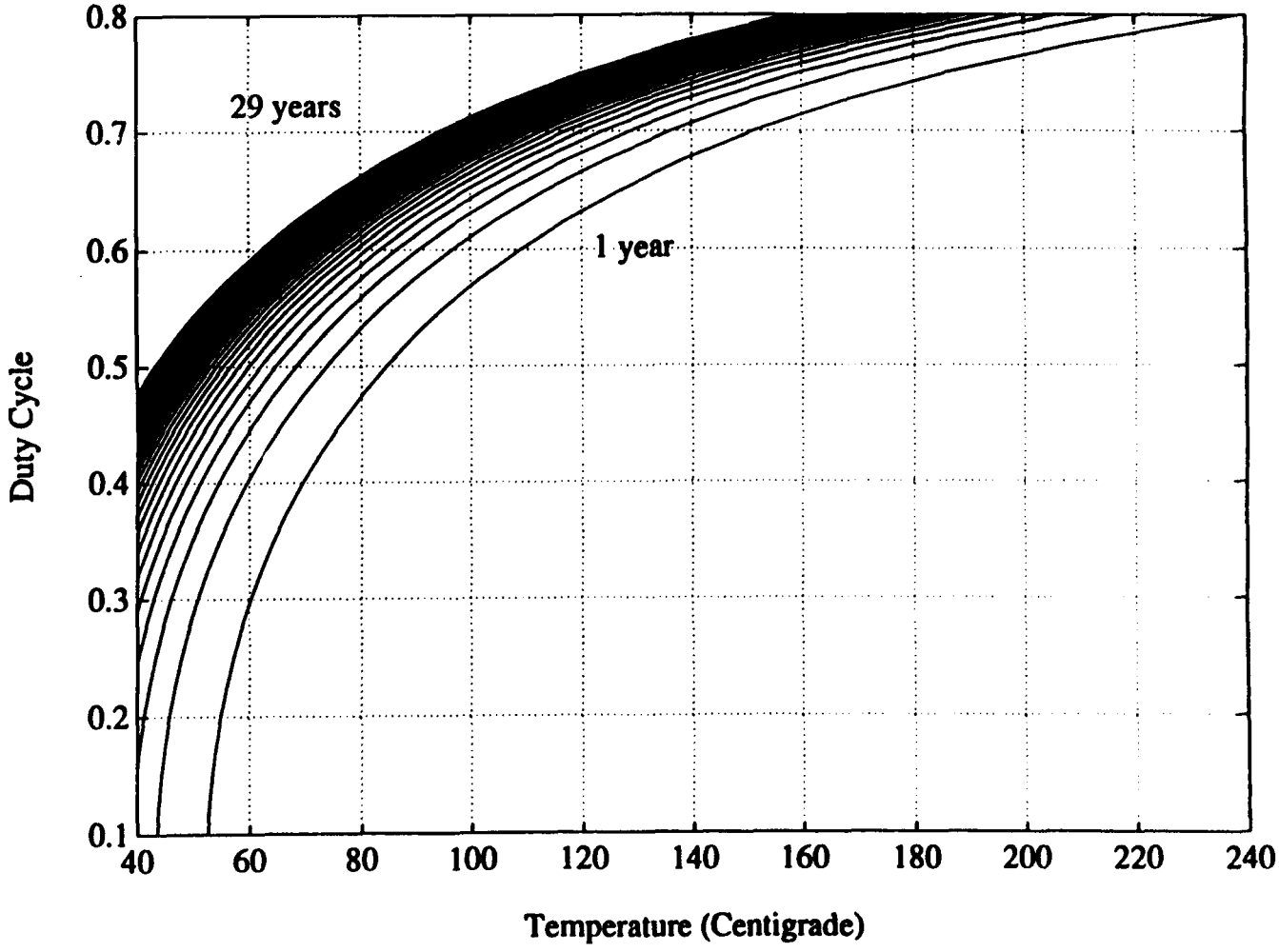
V is the voltage applied;
$K1$ is the physical and chemical properties of the metallization material (from Table 5.2);
$K2$ is the coating integrity index (from Table 5.3);
$K3$ is the mission profile correction factor; and
K_4 is the environmental stress correction factor.

Derated stress values can be calculated from the curve of constant life versus temperature and duty cycle, obtained from Equation 5.12. (Figure 5.2 shows curves of constant life versus temperature and duty cycle.) It is evident that dependence of metallization corrosion on steady- state temperature and duty cycle . non-linear, and that reducting dominant stress magnitudes beyond a certain limit may not produce any observable benefit in terms of added reliability, because the time to failure is far beyond the wear-out life of the device. The paradigm of associating higher reliability with lower temperature is also misleading, since the same mission life of twenty-nine years can be obtained for any temperature from 40°C to 160°C, depending on the duty cycle (Figure 5.2).

Table 5.3 Coating Integrity Index [Pecht and Ko 1991]

Coating Type	Coating Integrity Index (k_2)
No coating	1
Partially bonded	10 - 50
Completely bonded	100

Figure 5.2 Derating curves of life under corrosion versus temperature and duty cycle. The curves identify the various combinations of temperature and duty cycle which will result in desired life. The paradigm of higher reliability associated with lower temperature is misleading, since the same mission life of 29 years can be obtained for any temperature from 40°C to 160°C depending on the duty cycle. [Pecht, 1990]



5.4.2 Electromigration

Electromigration, a mass-transfer mechanism with a dominant dependence on current density, steady-state temperature, and temperature gradient, is a grain-boundary diffusion mechanism. The time to failure due to temperature stress for $T < 150°C$ is much greater than the wear-out life. Typically, electromigration failures at $T < 150°C$ occur at sites of maximum temperature gradient or structural non-uniformity. Steady-state temperature is a dominant stress accelerator for electromigration at $T > 150°C$ for typical metallization geometries. The maximum temperature and current density combination that can be used for a given metallization can be calculated from the following models:

- Black's Model [Black 1982]
- Shatzkes and Lloyd Model [Shatzkes and Lloyd 1986]
- Venables and Lye Model [Venables and Lye 1972]

Calculate T_{max} (max. temperature) and j_{max} (current density), where

$$T_{operation} < T_{max}$$
$$j_{operation} < j_{max} \tag{5.15}$$

such that

$$MTF > mission\ life \tag{5.16}$$

where

$$MTF = \frac{wt}{j^2 A e^{-\frac{E_A}{kT}}} \tag{5.17}$$

and

MTF	is the mean time to failure (hours);
w	is the metallization width (cm);
t	is the metallization thickness (cm);
A	is a parameter depending on sample geometry, physical characteristics of the film and substrate, and protective coating;
j	is the current density (A/cm^2);
n	is an experimentally determined exponent;
E_A	is the activation energy (eV); and

T is the steady-state temperature (Kelvin).

Table 5.4 Black's Constants For Various Metallization Materials

Metallization Material	A	E_A (eV)
Al-2%Si	0.3119×10^{-14}	0.558
Al-4%Cu-4%Si	7.292×10^{-15}	0.703

The value of the current exponent derived in recent studies varies from 1.5 to 7. The commonly used current exponents are:

$n = 1$ to 3	Chabra and Ainslie [1967]
$n = 1.5$	Attardo [1972]
$n = 1.7$	Danso and Tullos [1981]
$n = 2$	Black [1983]
$n = 6$ to 7	Blair et al. [1970]

The pre-exponential, current exponent, and activation energy for some common metallization materials reported in literature are presented in Table 5.5. Figure 5.3 shows the derating curves for electromigration stress; these identify various combinations of current density and temperature that will result in desired life.

Shatzkes and Lloyd Model [Shatzkes and Lloyd 1986]

Calculate T_{max} (maximum temperature) and j_{max} (current density), where

$$T_{operation} < T_{max}$$
$$j_{operation} < j_{max} \qquad (5.18)$$

such that

$$T_f > \textit{mission life} \qquad (5.19)$$

where

$$t_f = \left(\frac{2C_f}{D_o}\right)\left(\frac{k}{Z^* e \rho}\right)^2 T^2 j^{-2} e^{\frac{\Delta H}{kT}} \qquad (5.20)$$

and where

C_f is the critical value of vacancy concentration at which failure occurs;

occurs;

D_o is the pre-exponential factor for grain-boundary self-diffusivity;

k is the Boltzmann constant;

Z^* is the effective charge;

e is the electronic charge;

ρ is the resistivity;

T is the steady-state temperature;

j is the current density; and

ΔH is the activation energy.

Equation 5.20 differs from Black's equation in that it has a T^2 pre-exponential term, but it fits Black's data equally well. *Venables and Lye Model [Venables 1972]*

Given the allowable temperature rise of ΔT_R in the metallization stripe, calculate T_{max} (maximum temperature) and j_{max} (current density), where

$$\begin{aligned} T_{operation} &< T_{max} \\ j_{operation} &< j_{max} \end{aligned} \tag{5.21}$$

such that

$$T_F > \textit{mission life} \tag{5.22}$$

where

$$T_F = \frac{1}{2Cn}\left(\frac{\tau_o k T_o}{j_o \rho_o D_o e^{-\frac{Q}{kT}}}\right)\int_{x_o}^{x_1} \frac{e^{\frac{-Qx}{kT_o}}}{x^2(1-x+x\alpha T_o)}dx \tag{5.23}$$

and

$$\tau_0 = \Delta T_R(1+\alpha(T_0-300))\left(\frac{1}{T_0}\right)\left(\frac{j_0}{1x10^6}\right)^2 \tag{5.24}$$

and

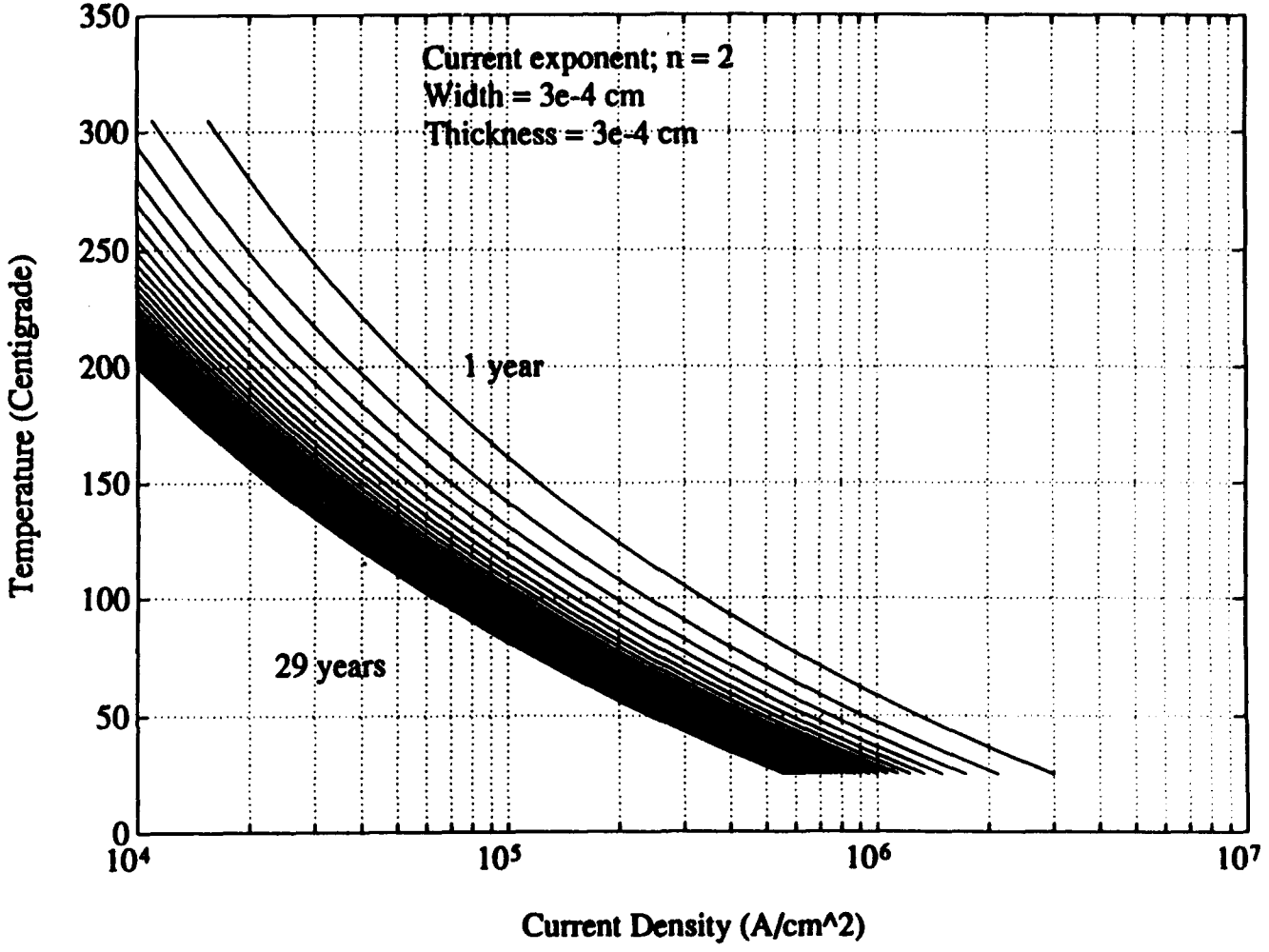
$$x = \frac{\tau_o}{(1-p)^2+\tau_o(1-\alpha T_o)} = 1 - \left(\frac{T_o}{T}\right) \tag{5.25}$$

$$x_o = \frac{\tau_o}{1-\tau_o(\alpha T_o - 1)} \qquad @t=0$$

$$x_1 = 1-\left(\frac{T_o}{T_m}\right) \qquad @t=T_F \tag{5.26}$$

where ΔT_R is the temperature increase in the metallization stripe: α is the thermal coefficient of resistivity for metallization (/°C); T_o is the ambient temperature (°K); T_m is the melting temperature of the metallization stripe (°K); Q is the activation energy for grain-boundary diffusion ($\approx$ 0.558 eV); K is Boltzmann's constant (8.617 x 10^{-5} eV/K or 1.38 x 10^{-23} J/K); p is the porosity of the metallization stripe ($0.1 < p < 1.0$); j is the current density (A/cm^2); C is the constant for the metallization material; n is the density of grain-boundary nodes (/cm^3); ρ_o is the resistivity of metallization material at ambient temperature (Ω cm); and D_o is the grain-boundary diffusivity of the metallization material (cm^2/s).

Figure 5.3 Derating curves for electromigration stress. The curves identify various combinations of current density and temperature which will result in desired life [Black, 1982].



The current exponent for Black's equation (Equation 5.17) changes with the current density, j, in the metallization stripe. A constant value of the current exponent, n, is valid only over a small range of current densities [Venables 1972]. The Venables and Lye model accounts for the relationship of time to failure and baseline temperature, which is often simplistically represented by an Arrhenius relationship to give an activation energy. The model also addresses the dependence of current exponent on current density.

5.4.3 Hillock Formation

Hillocks in die metallization can form as a result of electromigration or extended periods under temperature cycling conditions (thermal aging). The phenomenon of simultaneous voiding and hillock formation occurs at temperatures in the neighborhood of 140 to 200°C [Thomas 1983]. Hillock formation due to extended periods under temperature cycling conditions is believed to be due to a self-diffusion process that occurs in the presence of strains within the metallization [LaCombe and Christou 1982]. Coating the metal with silicon nitride prevents failures from occurring and voids and hillocks from forming for at least 500 hours at 360°C. Hillocks form at random in aluminum films heated to temperatures around 400°C during fabrication.

5.4.4 Metallization Migration

Calculate the maximum allowable steady-state temperature to avoid metallization migration, where [DiGiacomo 1982].

$$T_{operation} < T_{max} \tag{5.27}$$

and

$$j_{tip} > j_{critical}$$

$$\frac{\partial Q_{tip}}{\partial t} > \frac{\partial Q_{critical}}{\partial t} \tag{5.28}$$

such that

$$t_f > mission\ life \tag{5.29}$$

where

Table 5.5 Temperature Acceleration and Current Exponents For Various Metallization Materials

Material	Metallization Dimensions (μm) w = width l = length t = thickness	Average Grain Size (μm)	Test Conditions		Activation Energy E_A, (eV)	Current Density Exponent (n)	Reference
			Current Density (A/cm^2)	Steady-State Temperature (°C)			
Single Layer Metallizations							
Aluminum (Al)	w = 10 l = 400 t = 1.2		1.3 - 3	75-350°C	0.41		[Satake 1973]
	w = 15.4 t = 0.6	8	0.55 - 2.02	109-260°C	0.84	2	[Black 1969]
	t = 1.0	-	-	-	0.56	2	[Black 1982]
	w = 1.3 l = 1524 t = 0.8	0.1	0.75	175-275°C	0.34		[Wu 1983]
	w = 2.3	0.1	-		0.47		[Wu 1983]
	w = 3.3	0.1	-		0.58		[Wu 1983]
	t = 0.7	0.7-1.8	2	125-300°C	0.24-0.57		[Reimer 1984]
	w = 4.5 l = 2000 t = 0.75	-	2	125-300	0.43		[Towner 1983]
	w = 10 l = 800 t = 1	-	1	160-250°C	0.57		[Schreiber 1981]
	w = 37 t = 1.2	8	0.46 - 0.99	109-260°C	1.2	2	[Black 1969]
	w = 15-25 l = 800 t = 0.5	0.3	2	105-180°C	0.55	3	[Van Gurp 1971]
	w = 7-20 l = 500-580 t = 1	0.8	0.5-2	130-200°C	0.7	2.5-4	[Saito 1974]

	w = 10 l = 25000-32000 t = 1	10	0.2-3	110-245°C	0.55	2	[Sim 1979]
		3.5	0.2-3	110-245°C	0.6	2	[Sim 1979]
		2	0.2-3	110-245°C	0.4	2	[Sim 1979]
	w = 6 l = 380 t = 0.8	0.7-1.4	1	150-215°C	0.43		[Ghate 1981]
	w = 7.5 l = 275 t = 0.5	-	0.13-1	82-192°C	0.35-0.85		[Lloyd 1987]
	-	-	1.3-2.9	30-141°C	0.56	2.5	[Wild 1988]
	w = 12.5 l = 1390 t = 0.7	1.2	0.5-2.88	109-260°C	0.48	2	[Black 1969]
Al-(0.79-3%)Si	w = 10 l = 762 t = 0.7-0.73	1.4	0.66-2	110-210°C	0.54-0.55	2	[Black 1978]
Al-1%Si	w = 5 l = 400 t = 1.1	-	0.5-2.5	162-215°C	0.58	1.53	[Schafft 1985]
	w = 3 l = 1000 t = 1	-	3.3	200°C	-	-	[Maiz 1989]
	w = 3.7-4.1 l = 400 t = 1.2	-	0.8-3	277°C	1.67-2.56	0.5	[Suehle 1989]
	w = 1.4 l = 160 t = 1.1	-	3.2	205-261°C	0.96	1	[Fantini 1989]
Al-1.5%Si	-	3.5	1	145-210°C	0.71		[Tatsuzawa 1985]
Al-2%Si	w = 1.2-2.2 l = 100-1600 t = 0.8	-	10-60	240-360°C	0.33	7.5	[Liew 1989]
	w = 10 l = 1000 t = 1	0.3	1.3-3.2	150-250°C	0.4 - 0.56	1.8 (j < 2)	[Nagasawa 1980]
	w = 10 l = 1000 t = 1	0.8	1.3-3.2	150-250°C	0.4	2.2	[Nagasawa 1980]

Al-0.3%Cu	w = 7-8 l = 250 t = 0.5-1	-	4	121-222°C	0.65		[d'Heurle 1972]
	w = 12.7 l = 1270 t = 1	2-3	-	-	0.63-0.7	-	[Rodbell 1983]
Al-0.5%Cu	w = 1-4 l = 25000 t = 0.8-1.1	1.2-4.5	1.6-2	195-250°C	0.5	2	[Sim 1979]
	w = 2-5 l = 1000 t = 1	1.8	2.1	209-264°C	0.73	-	[Levi 1985]
	w = 2-5 l = 1000 t = 1	2.9	1.62	232-304°C	0.84	-	[Levi 1985]
	w = 2-5 l = 1000 t = 1	1.8	1.82	205-283°C	0.68	-	[Levi 1985]
	w = 7.5 l = 275 t = 0.5	-	0.13-1	173-238°C	0.53-0.92	-	[Lloyd 1987]
Al-2%Cu	w = 6 l = 380 t = 0.8	1-2.3	1	150-215°C	0.7	-	[Ghate 1981]
Al-4%Cu	w = 7-8 l = 250 t = 0.5-1	-	4	105-175°C	0.83	-	[d'Heurle 1972]
	w = 15 l = 1250 t = 1	-	0.8	220-275°C	0.76	-	[Learn 1975]
Al-(5.1-5.4)%Cu	w = 10 l = 250-3380 t = 1.5	-	1.3-1.5	142-157°C	0.48	-	[Kakar 1973]
Al-1%Si-2%Cu	w = 6 l = 380 t = 0.8	0.25	1	150-215°C	0.5	-	[Ghate 1981]
Al-2%Si-4%Cu	t = 1.0	-	-	-	0.7	2	[Black 1982]
Al-Si-0.5%Cu	w = 3.3-7.7 t = 0.62-0.67	1.8-3.6	0.5-1	200-240°C	0.76	-	[Bukkett 1984]

Al-Si-2%Cu	w = 2.2-7.7 t = 0.28-0.71	1.5-3.1	0.5-1	180-240°C	0.86	-	[Bukkett 1984]
Al-1%Si-(0.35-1.1)%Ti	w = 4 l = 2000	-	2	125-300°C	0.5-0.7	-	[Towner 1986]
Double-Layer Metallizations							
Al-1%Si/TiW	w = 5.5 l = 2550 t = 0.6/0.22	-	0.5-2.2	100-200°C	0.49	2.5	[Onduresk 1988; Hoang 1988]
Al-0.3%Cu/TiW	w = 12.7 l = 1270 t = 0.8/0.2	2-3	1.4	100-300°C	0.65	-	[Rodbell 1983]
Al-4%Cu/TiW	w = 12.7 l = 1270 t = 0.8/0.2	5	1.4	100-300°C	0.75	-	[Rodbell 1983]

$$t_f = \frac{(\frac{\rho}{MC})(\frac{2r_d}{ZFD_o})l}{\beta(V_{pot} - V_T)\frac{1}{kT}e^{-\frac{\Delta H}{kT}} erfc\frac{1}{2\sigma}\ln(\frac{kTlnHr_{average}}{2\gamma v})^2} \tag{5.30}$$

where

$$r = \frac{2\gamma v}{kT \ln\left(\frac{p}{p_o}\right)} \tag{5.31}$$

$$erfc\left(\frac{1}{2\sigma}\right) = 1 - \frac{2}{\sqrt{\pi}}\int_o^{\left(\frac{1}{2\sigma}\right)} e^{-u^2}\,du \tag{5.32}$$

and where ρ is the density of the dendrite; M is the atomic weight; C is the ionic concentration; z is the ionic charge or the valence of the metal ions; D_o is the

diffusivity coefficient; l is the distance between electrodes; r_d is the dendrite radius; $r_{average}$ is the average pore radius; γ is the surface tension; v is the molar volume; p is the saturated vapor pressure above the meniscus; p_o is the saturated vapor pressure above the flat surface (H approaching p/p_o is the relative humidity at which condensation occurs; $\sigma = \ln [r_{50} / r_{16}]$ sigma; β is the fraction of metal surface at the anode that is susceptible to metal oxidation and promotes metal migration; V_{pot} = potential difference applied; V_T = critical value of potential difference for dendritic growth; j_{tip} = current density at the whisker's tip; $j_{critical}$ = critical current density at the whisker's tip; $Q_{tip} = j_{tip} / ZF$ = mass transport rate; and $Q_{critical}$ = critical mass transport rate.

5.4.5 Constraint Cavitation of Conductor Metallization

The lifetime due to SDDV becomes minimum at a certain temperature T_m. The increase in lifetime when T increases or decreases from T_m (temperature where the minima occurs) results from a decrease in stress in the metallization for $T \geq T_m$, or a decrease in diffusivity for $T \leq T_m$, respectively. The allowable operation temperatures are calculated from

$$\begin{aligned} T_{operation} &< T_{max} && for\ T < T_{passivation} \\ T_{operation} &> T_{max} && for\ T > T_{passivation} \end{aligned} \qquad (5.33)$$

such that

$$\tau > mission\ life \qquad (5.34)$$

where

$$\tau = \frac{kGLWT\, e^{\frac{Q_d}{kT}}}{2AED_0(n-1)}\left(\left(\frac{\sigma(0)}{G} - \frac{EW \tan\psi}{GL}\right)^{1-n} - \left(\frac{\sigma(0)}{G}\right)^{1-n}\right) \qquad (5.35)$$

$for\ n \neq 1$

$$\tau = \frac{kGLWT\, e^{\frac{Q_d}{kT}}}{2AED_0}\left(\ln\frac{\sigma(0)}{G} - \ln\left(\frac{\sigma(0)}{G} - \frac{EW\tan\psi}{GL}\right)\right) \qquad (5.36)$$

for $n = 1$

where

$$\sigma(t) = \sigma_o(T_d - T)\left(\frac{W_o}{W}\right)^m\left(\frac{H_o}{H}\right)^p \qquad (5.37)$$

and where

k	is Boltzmann's constant;
G	is the shear modulus of metallization;
$L/2$	is the distance over which the stress due to void formation is relaxed;
W	is the width of the metallization;
T	is steady-state temperature;
A	is a factor independent of stress, temperature, and time;
E	is Young's modulus of metallization;
D_o	is the diffusivity constant;
Q_d	is the activation energy for diffusion;
n	is the stress dependency exponent;
$\sigma(0)$	= stress at $t = 0$;
$\sigma(t)$	= stress at time t ;
m	= p = 0.5;
T_d	= passivation deposition temperature;
W_o	= normalization width;
H_o	= normalization thickness;
W	= line width;
H	= line thickness; and
σ_o	= stress induced by temperature change of 1 degree centigrade, and
Ψ	= half the angle of the void.

Kato and Niwa Model [Kato et at. 1990, Niwa et al. 1990]. This model accounts for plastic deformation and diffusional relaxation. While plastic deformation

occurs almost instantaneously after the passivation is laid on the metallization, diffusion is practically inoperative at low temperatures. (Low temperature has been defined as the temperature at which the time for diffusional relaxation is greater than 10^3 seconds) [Kato et al. 1990, Niwa et al. 1990]. Kato et al. found that stresses did not become hydrostatic after relaxation due to plastic deformation. Time to failure due to stress-driven diffusive voiding is considered to be the time during which the area fraction, A, increases from A_{min} to A_{max} (Area fraction = r_o^2/l^2; r_o is the void radius, and 2l is the void separation). The variation in time to failure versus aspect ratio and temperature shows that SDDV changes its temperature dependence from steady-state to inverse temperature dependence at a temperature threshold which is a function of passivation temperature (Figure 5.4). The steady-state temperature limits to avoid SDDV can be calculated from

$$\begin{aligned} T_{operation} &< T_{max} && \text{for } T < T_{passivation} \\ T_{operation} &> T_{max} && \text{for } T > T_{passivation} \end{aligned} \tag{5.38}$$

such that

$$T_f > \text{mission life} \tag{5.39}$$

where

$$\text{for} \quad \sigma \geq \frac{2\Gamma}{r_o}$$

$$T_f = \frac{kTl^3}{20D_B w \sigma \Omega} \tag{5.40}$$

$$\begin{aligned} l &= \frac{a_2}{r} && \text{for } r \geq 1 \\ l &= a_2 && \text{for } 0 \leq r \leq 1 \end{aligned}$$

$$\text{for} \quad \sigma < \frac{2\Gamma}{r_o} \tag{5.41}$$

$$\text{no void growth}$$

where

$$\sigma_{33}^{R} = -\frac{\mu}{(1-\nu)}\left(2(1+\nu)\epsilon^{T} + \frac{-2r-2(1-\nu)}{(1+r)}\epsilon_{11}^{R} + \frac{-2-2r(1-\nu)}{(1+r)}\epsilon_{22}^{R}\right) \tag{5.56}$$

For r ≈ 1:

$$\epsilon_{11}^{P} = \epsilon_{22}^{P} = -\frac{1}{2}\epsilon_{33}^{P} = -\frac{(1+\nu)\epsilon^{T} + \dfrac{(1-\nu)\sigma_{y}}{\mu}}{(4\nu-5)} \tag{5.57}$$

$$\sigma_{11}^{P} = \sigma_{22}^{P} = -\frac{\mu}{(1-\nu)}((1+\nu)\epsilon^{T}(1-2\nu)\epsilon_{11}^{P}) \tag{5.58}$$

$$\sigma_{33}^{P} = \frac{-2\mu}{(1-\nu)}((1+\nu)\epsilon^{T}+(-2+\nu)\epsilon_{11}^{P}) \tag{5.59}$$

For r ≈ 0:

$$\epsilon_{11}^{P} = \epsilon_{33}^{P} = -\frac{1}{2}\epsilon_{22}^{P} = -\epsilon^{T} - \frac{(1-\nu)\sigma_{y}}{2\mu(1+\nu)} \tag{5.60}$$

$$\begin{aligned}\sigma_{11}^{P} &= \sigma_{33}^{P} = \sigma_{y} \\ \sigma_{22}^{P} &= 0\end{aligned} \tag{5.61}$$

where

T_f	is the time to failure in seconds;
k	is Boltzmann's constant (8.617×10^{-5} eV/k or 1.38×10^{-23} Joule/Kelvin);
Γ	is the surface energy per unit area (J/m^2);
T	is the temperature in Kelvin;
D_B	is the grain-boundary diffusivity ($meter^2/sec$);
D_L	is the lattice diffusion coefficient ($meter^2/sec$);

D_I is the interfacial diffusion coefficient (meter^2/sec);
λ is the length of grain along line axis (meter);
w is the grain-boundary thickness (meter);
Ω is the atomic volume for conductor atoms (meter^3);
σ_R is the hydrostatic stress after diffusional relaxation;
σ_{33} is the stress along metallization length;
σ_y is the yield strength of metallization;
σ_{ii} for i = 1, 2, 3 are the stresses in the metallization line along its width, thickness, and length, respectively;
ϵ^T is the thermal strain resulting from mismatch between passivation and metallization, and
ϵ_{ii}/S are the strains in 1,2,3 directions (direction 1 = along line width; direction 2 = along line thickness; direction 3 = along line length);

μ is the shear modulus of the metallization line (Pascal or N/m^2);
r is the aspect ratio of metallization line (r = (metallization thickness)/(metallization width)); $2a_1$ is the metallization width; $2a_2$ is the metallization thickness;
ν is the Poisson's ratio of metallization line;
$\Delta\alpha$ is the difference in coefficients of thermal expansion between the metallization line and passivation (per deg Kelvin);
T is the temperature (kelvin); and
T_P is the deposition temperature of passivation.

5.5 DERATING FOR FAILURE MECHANISMS IN DEVICE OXIDE

5.5.1 Slow Trapping

Slow trapping, a phenomenon of MOS devices only, has a dominant dependence on the trap density of oxide. The trapping and detrapping kinetics of electrons cause threshold voltage shifts. The magnitude of threshold voltage shift is a function of oxide permittivity, oxide thickness, density, and location of oxide charge. Electrons, or holes trapped in oxide traps, are excited by the application of high steady-state temperature. The highest steady-state temperature for a maximum allowable flatband voltage shift can be calculated from

$$T_{operation} < T_{max} \tag{5.62}$$

such that

$$\Delta V_{FB} < \Delta V_{FB(max)} \tag{5.63}$$

where

$$\Delta V_G^+ = \Delta V_{FB} = -\frac{x_m Q_{ot}}{\epsilon_o \epsilon_{ox}} \qquad \textit{for positive gate voltage}$$

$$\Delta V_G^- = \Delta V_{FB} = -\frac{t_{ox}}{\epsilon_o \epsilon_{ox}}\left(1-\frac{x_m}{t_{ox}}\right)Q_{ot} \qquad \textit{for negative gate voltage}$$

$$Q_{ot}(t) = \left(Q_{ot_{(t=0)}}\right) e^{-e_n^{th}} \tag{5.65}$$

and

$$e_n^{th} = \left(\frac{2\sqrt{3}(2\pi)^{\frac{3}{2}} m_n^* k^2}{h^3}\right) \sigma_n T^2 e^{-\frac{E_n}{kT}} \tag{5.66}$$

where

T	is steady-state temperature (Kelvin);
ΔV_{FB}	is the flatband voltage shift;
ϵ_o	is the free-space permittivity (8.85 x 10^{-14} F cm^{-1});
ϵ_{ox}	is the relative permittivity of oxide (dielectric constant ≈ 3.9 (typical value));
t_{ox}	is the oxide thickness (cm);
x'	is the distance away from the metal-SiO_2 interface;
x_m	is the centroid of charge contained in the oxide (between 0 and t_{ox});
$e_n th$	is the thermal emission coefficient (sec^{-1});
t	is the time (seconds);
E_n	= E_C-E_T(eV); E_C is the conduction band energy level and E_T is the trap energy;level .
σ_n	is the capture cross-section for electrons (cm^2);
$Q_{ot(t=0)}$	is the density of oxide-trapped charge integrated over the thickness of the oxide, expressed per unit area of Si-SiO_2 interface at time t=0;
Q_{ot}	is the density of the oxide-trapped charge over the thickness of the oxide, expressed per unit area of the Si-SiO_2 interface (C cm^{-2});

m_n^* is the effective mass of the electrons in SiO_2;
k is Boltzmann constant (8.617×10^{-5} eV/K or 1.38×10^{-23} J/K); and
h is Planck's constant (6.62×10^{-34} J.s).

The prime distribution moment, $(X_m Q_{ot})$, increases or decreases with the increase or decrease in x_m or Q_{ot}. If the trap distribution in the oxide is uniform parallel to the interfaces, the C-V curve shifts without distortion.

5.5.2 Gate Oxide Breakdown

Electrostatic Discharge. Electrostatic discharge in MOS devices can produce gate-to-drain shorts, gate-to-source shorts, or gate-to-substrate shorts, depending on the nature of imperfection. The most likely sites for ESD damage in defect-free oxides are source or drain sites depending on the polarity of transient currents and the biasing of the device. Gate-to-substrate shorts are more prevalent in devices with pre-existing oxide defects, in the form of geometrical or dopant irregularities. For bipolar devices, typical ESD junction damage occurs in the device bulk under reverse-biased conditions resulting in degraded p-n junction characteristics. Failed p-n junctions appear as cracked glass across the junction on the surface of the chip. The device operating temperature affects the ESD damage threshold. The higher the operating temperature, the lower the damage threshold. The maximum allowable temperature for the device can be calculated from the Wunsch-Bell model [Wunsch and Bell 1968]

$$T_{operation} < T_{max} \qquad for\ V_{ESD} > V_{protection} \qquad (5.67)$$

where T_{max} is calculated from

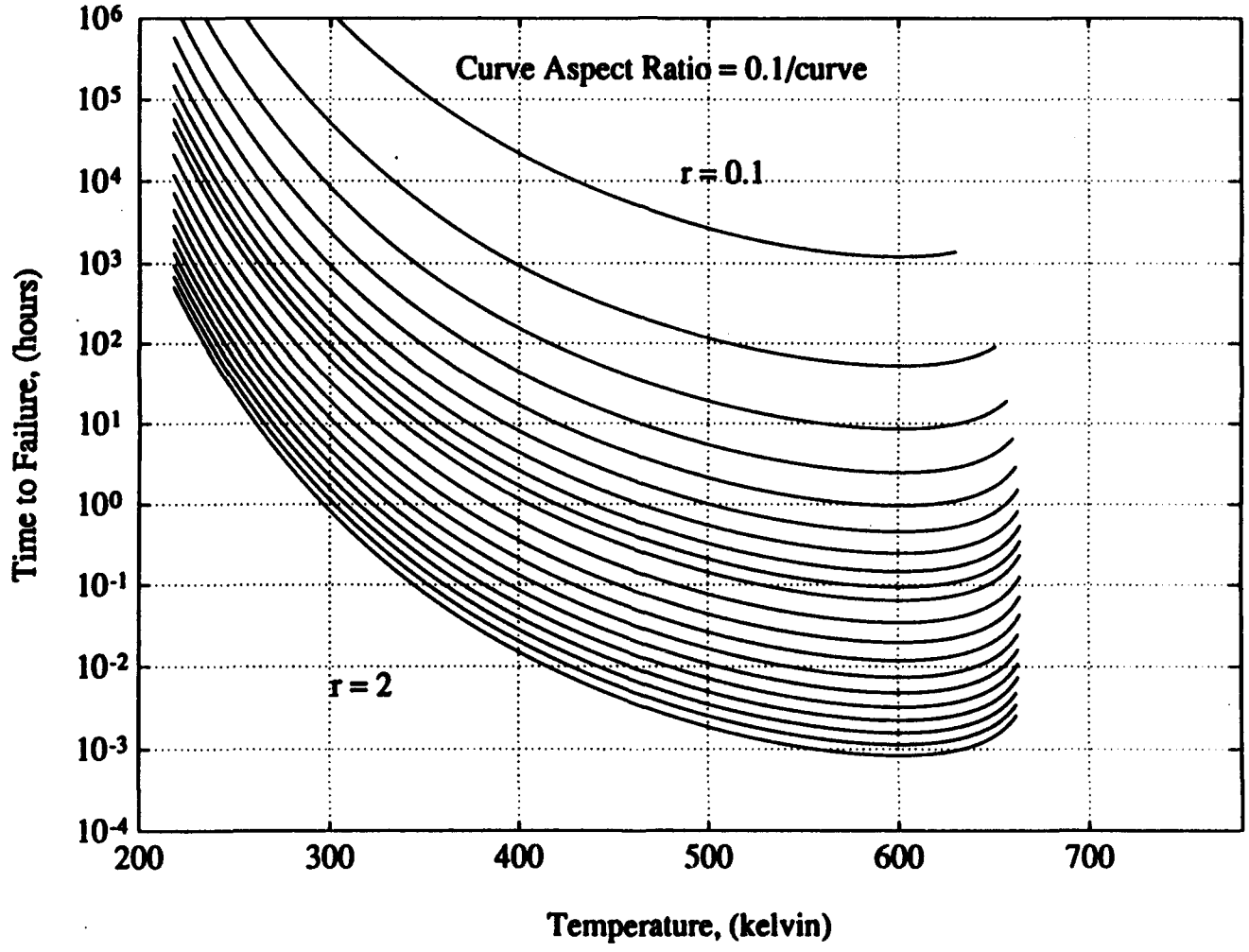
$$T_l = T_m - \frac{P\sqrt{t}}{A\sqrt{\pi k \rho C_p}} \qquad (5.68)$$

and where

P/A is the power per unit junction area, calculated from the protection structure breakdown voltage;
k is the thermal conductivity of the semiconductor;
ρ is the density of the semiconductor;
C_p is the specific heat of the semiconductor;
T_m is the melting point of the semiconductor;
T_l is the operating ambient temperature; and

t is the ESD pulse time (seconds).

Figure 5.4 The variation in time to failure versus aspect ratio and temperature shows that SDDV changes its temperature dependence from steady state to inverse temperature dependence, at a temperature threshold which is a function of the passivation temperature. [Kato, 1990; Niwa, 1990]



The threshold voltage and power density, P/A, for the circuit can be calculated from the Speakman model [Speakman 1974]:

$$A = D_{base} \; x \; L_{emitter} \tag{5.69}$$

$$\tau = (R_b + R_d + R_c)C_b \tag{5.70}$$

$$I_p = \frac{V_b - V_d}{R_b + R_d + R_c} \tag{5.71}$$

$$P_{av} = \frac{1}{5\tau}\int_0^{5\tau} V_d I_p \, e^{-\frac{t}{\tau}} dt + \frac{1}{5\tau}\int_0^{5\tau} R_b I_p^2 \, e^{-\frac{2t}{\tau}} dt$$

$$= \frac{V_d I_p}{5}(1 - e^{-2}) + \frac{R_b I_P^2}{10}(1 - e^{-10}) \tag{5.72}$$

$$\approx \frac{V_d I_p}{5} + \frac{R_b I_P^2}{10}$$

$$R_d = R_{sheet\text{-}base} \; x \; \frac{t_{b\text{-}e}}{L_{emitter}} \tag{5.73}$$

where

D_{base}	is the depth of the base region;
$L_{emitter}$	is the length of the emitter region;
$T_{b\text{-}e}$	is the base-emitter separation;
I_p	is the peak current of the discharge waveform;
V_d	is the device voltage;
V_b	is the discharge voltage on the human body;
C_b	is the body capacitance;
$R_{base\text{-}sheet}$	is the base-sheet resistance;
R_i	are resistance components; where $i = b,c,d$ for body, contact, and device resistances, respectively;
t	is the time (seconds);

τ is the time constant of the RC circuit; and

$V_{protection}$ is the voltage capacity of the device protection circuit (Table 5.6).

Table 5.6 Comparison of Typical ESD Protection Thresholds

Protective Circuit Device	Device Technology	Protection Voltage Threshold (Volt)	Reference
double implant field isolation device in well	CMOS	8000 volts	[Nischizawa 1975]
thick oxide-diffused resistor-field plate	DRAM junction depth : 0.4 μm breakdown voltage : 20 V field oxide : 1 μm	5000 volts	[Duvvury 1983]
	EPROM junction depth : 0.8 μm breakdown voltage : 26 V field oxide : 1.4 μm	6000 volts	[Duvvury 1983]
diode-diffused resistor-field plate	EPROM junction depth : 0.8 μm breakdown voltage : 26 V field oxide : 1.4 μm	4500 volts	[Duvvury 1983]
thick oxide polysilicon resistor-field plate	EPROM junction depth : 0.8 μm breakdown voltage : 26 V field oxide : 1.4 μm	3000 volts	[Duvvury 1983]
diffused resistor-gated diodes and spark gap	CMOS/SOS type A CMOS/SOS type B	800 volts	[Palumbo and Dugan 1986]
diode-resistor circuit	CMOS/SOS type C	1800 to 2000 volts	[Palumbo and Dugan 1986]
thick oxide	CMOS, NMOS	> 6000 volts	[Rountree 1988]
diode-resistor-diode	CMOS gate array	4000 volts	[Hull and Jackson 1988]

Time-Dependent Dielectric Breakdown. Time dependent dielectric breakdown (TDDB) is the formation of low-resistance dielectric paths through localized defects in the MOS oxide. TDDB has a very weak dependence on temperature and a dominant dependence on the electric field across the oxide. The field acceleration itself is a function of steady-state temperature. The field acceleration is inversely dependent on steady-state temperature, and has been found to reduce

from 6 decades/MV/cm at 25°C to 2 decades/MV/cm at 150°C. The maximum allowable temperature and electric field across the oxide can be calculated from:

- Fowler-Nordhiem Tunneling-based Models [Lee 1988, Moazzami 1989, Moazzami 1990]
- Thermodynamic Model [McPherson 1985]
- Empirical Models [Anolick 1981, Crook 1979, Berman 1981]

Fowler-Nordheim Tunneling-based Models for TDDB. The maximum allowable temperature and electric field can be evaluated by calculating predicted life versus steady-state temperature, worst-case manufacturing defect magnitude (X_{eff}), and electric field (Figures 5.5 a and b). Due to the non-linear dependence of life under TDDB on temperature, defect magnitude, or electric field, derating the stress below a particular value may not result in a noticeable benefit in terms of increased life, because the time to failure is much greater than the wear-out life of the device. Furthermore, because of the multiplicity of dependencies of TDDB, reducting the temperature to a pre-specified value for a device technology, as is done now (Table 5.1), may not result in the desired reliability. The dependence of time to failure under TDDB is given by

$$\begin{array}{ll} T_{operation} < T_{max} & \textit{weak acceleration} \\ V_G < V_{ox(max.)} & \textit{strong acceleration} \end{array} \qquad (5.74)$$

such that

$$t_{BD} > \textit{mission life} \qquad (5.75)$$

where

$$t_{BD}(T) = \tau_0 e^{\frac{GX_{eff}}{V_{ox}}\left(1 + \frac{\delta}{k}\left(\frac{1}{T}-\frac{1}{300}\right)\right)-\frac{E_b}{k}\left(\frac{1}{T}-\frac{1}{300}\right)} \qquad (5.76)$$

$$\begin{array}{lll} \delta = 0.0167\ eV & for & 25^\circ C < T < 125^\circ C \\ E_b = 0.28\ eV & & \\ \delta = 0.024\ eV & for & T > 150^\circ C \\ E_b = 0.28\ eV & & \end{array} \qquad (5.77)$$

where

$$\delta = \frac{k}{G}\frac{d\ G(T)}{d\ (1/T)} \tag{5.78}$$

and where

T	is the steady-state temperature (Kelvin);
G	is the slope of the $\ln(t_{BD})$ versus $1/E_{ox}$ plot ($\approx$ 350 x 10^6 volt/cm);
X_{ox}	is the oxide thickness (cm);
X_{eff}	is the effective oxide thickness at the weakest spot in the oxide (cm);
V_G	is the gate voltage across the oxide (Volt);
V_{ox}	is the voltage across the oxide (Volt);
τ_0	is the room-temperature value of the pre-exponential, $\tau(T)$ ($\approx$ 1 x 10^{-11} sec);
E_b	is the activation energy of the pre-exponential (eV); and
k	is Boltzmann's constant (8.617 x 10^{-5} eV/K).

Thermodymanic Models [McPherson 1985]. The thermodynamic model is based on the assumption that when the dielectric breaks down, it undergoes a irreversible phase transition transforming the material from an insulating phase to a conducting phase. The driving force for this transformation is the difference between the free energies of the conducting phase and the insulating phase. The maximum temperature and electric field for desired mission life can thus be calculated as follows:

$$\begin{aligned} T_{operation} &< T_{max} && \textit{weak acceleration} \\ V_G &< V_{ox(max.)} && \textit{strong acceleration} \end{aligned} \tag{5.79}$$

such that

$$t_{BD} > \textit{mission life} \tag{5.80}$$

where

$$TF(f\%) = Ae^{\left(\frac{\Delta H_Q^*}{K_B T}\right)} e^{[\gamma(T)S]} \tag{5.81}$$

The field acceleration parameter, γ, is the steady-state temperature-dependent parameter given by

$$\gamma = B + \frac{C}{T} \tag{5.82}$$

where

T	is the steady-state temperature;
K_B	is the Boltzmann constant (8.617×10^{-5} eV/K or 1.38×10^{-23} J/K);
ΔH_o^*	is the change in enthalpy required to activate the poly filament growth at breakdown;
B	and C are constants, $S=E_B - E_S$;
E_B	is the breakdown strength of the dielectric; and
E_S	is the stressing in the dielectric.

Empirical Models [Anolick 1981, Crook 1979, Berman 1981]. The maximum temperature or the electric field across the oxide can be calculated from

$$\begin{aligned} T_{operation} &< T_{max} && \textit{weak acceleration} \\ V_G &< V_{ox(max.)} && \textit{strong acceleration} \end{aligned} \tag{5.83}$$

such that

$$t_{BD} > \textit{mission life} \tag{5.84}$$

where

$$t_f(F) = Ae^{\frac{\Delta H}{kT}} e^{\gamma(V_B(F)-V_A)} \tag{5.85}$$

where

$t_f(F)$	is the time to failure for F percent of the population;
γ	is the voltage form factor (determined by life testing);
ΔH	is the activation energy;
k	is Boltzmann constant;
T	steady-state temperature;
$V_B(F)$	is the breakdown voltage for F percent of population; V_A is the applied voltage; and A is a constant. (Some typical values are given in Table 5.7)

Table 5.7 Empirical Models for TDDB

Reference	Oxide Thickness	Experimental Conditions	Observations	Model Predictions
Anolick and Nelson 1979	700 Å	E_s = 1.3 MV/cm $E_B - E_s$ = 7 MV/cm	$(\Delta H)_{50\%}$ = 2.1 eV $\gamma = B + \frac{C}{T}$	$(\Delta H)_{50\%}$ = 1.8 eV $\gamma = B + \frac{C}{T}$
Crook 1979	1100 Å	E_s = 3.5 MV/cm $E_B - E_s$ = 3 MV/cm	$(\Delta H)_{50\%}$ = 0.3 eV γ = 7 @ 25°C	$(\Delta H)_{50\%}$ = 0.34 eV γ = 6 @ 25°C
Berman 1981	≥400 Å	linear ramp	$(\Delta H)_{50\%} = 0.29 (E_B - E_s)$ $\gamma = -5.4 + \frac{0.2}{T}$	$(\Delta H)_{50\%} = 0.29 (E_B - E_s)$ $\gamma = -5.4 + \frac{0.2}{T}$
Hokari 1982	100 Å	E_s = 5 -7 MV/cm $E_B - E_s$ = 5 MV/cm	$(\Delta H)_{50\%}$ = 1.0 eV @ 6 MV/cm γ = 1.7 @ 250°C	$(\Delta H)_{50\%}$ = 1.0 eV @ 6 MV/cm γ = 1.5 @ 250°C
McPherson 1985	100 Å	E_s = 6 - 8 MV/cm $E_B - E_s$ = 3 - 5 MV/cm	$(\Delta H)_{50\%}$ = 0.3 - 1.0 eV $\gamma = B + \frac{C}{T}$	$(\Delta H)_{50\%}$ = 0.3 eV $\gamma = B + \frac{C}{T}$

5.6 DERATING FOR FAILURE MECHANISMS IN THE DEVICE

5.6.1 Ionic Contamination

Ionic contamination occurs predominantly in MOS devices and results in reversible degradation, in the form of threshold voltage shift and gain reduction due to the presence of mobile ions within the oxide or at the device-oxide interface. P-

channel devices are less sensitive to ionic contamination than n-channel devices. The mobility of ions is steady-state temperature dependent. The threshold voltage shift increases with an increase in the steady-state temperature. However, a high-

Figure 5.5 Due to the non-linear dependence of life under TDDB on temperature, worst case manufacturing defect magnitude, or electric field, derating the stress below a particular value may not result in noticeable benefit in terms of increased life because the time to failure is much beyond wear-out life of the device.

Figure 5.5a Derating curve for TDDB versus steady state temperature and effective oxide thickness. The curves identify the various combinations of temperature T, and effective oxide thickness x_{eff}, which will result in desired life. [Lee, 1988; Moazzami, 1989; Moazzami, 1990]

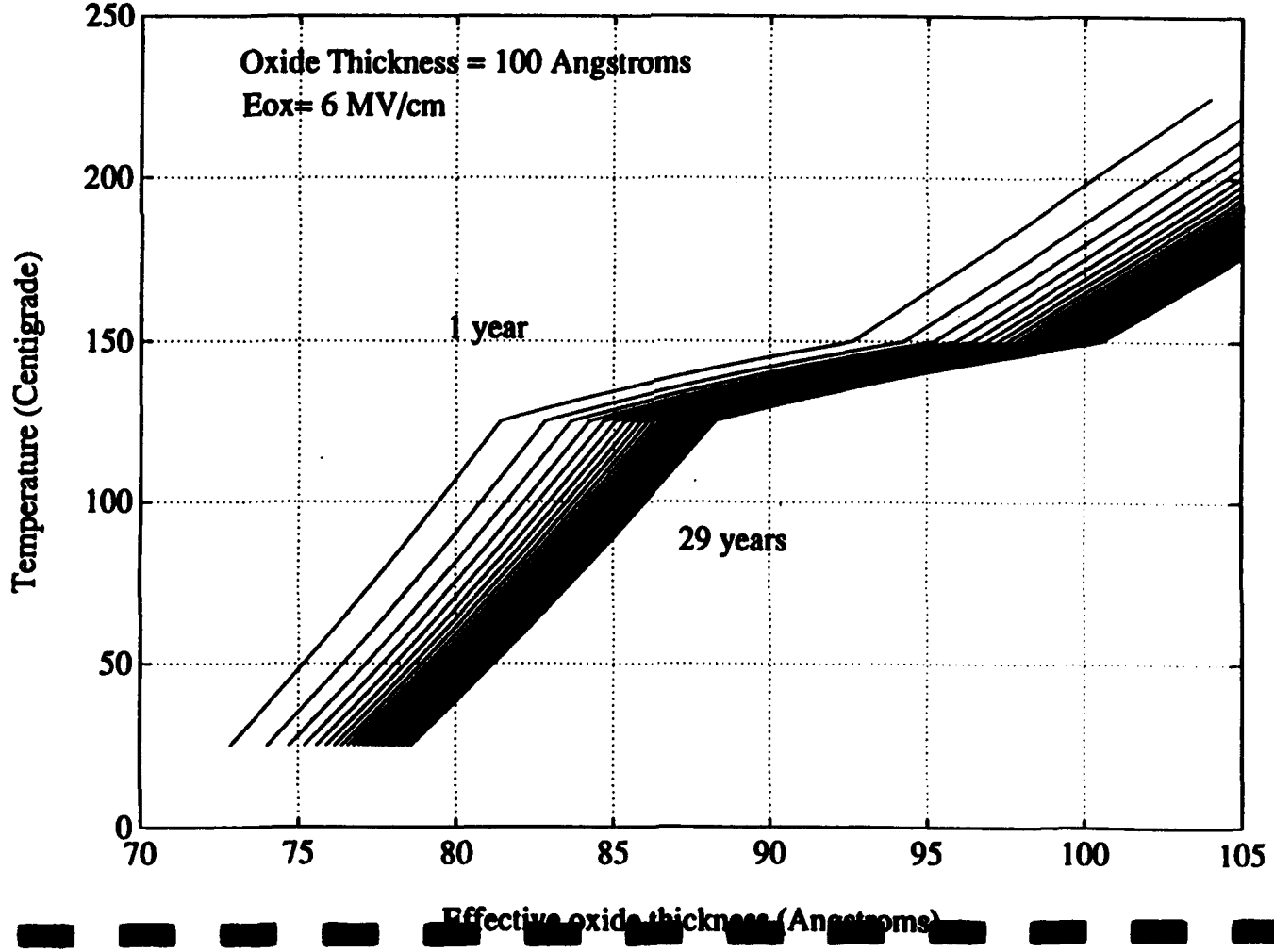
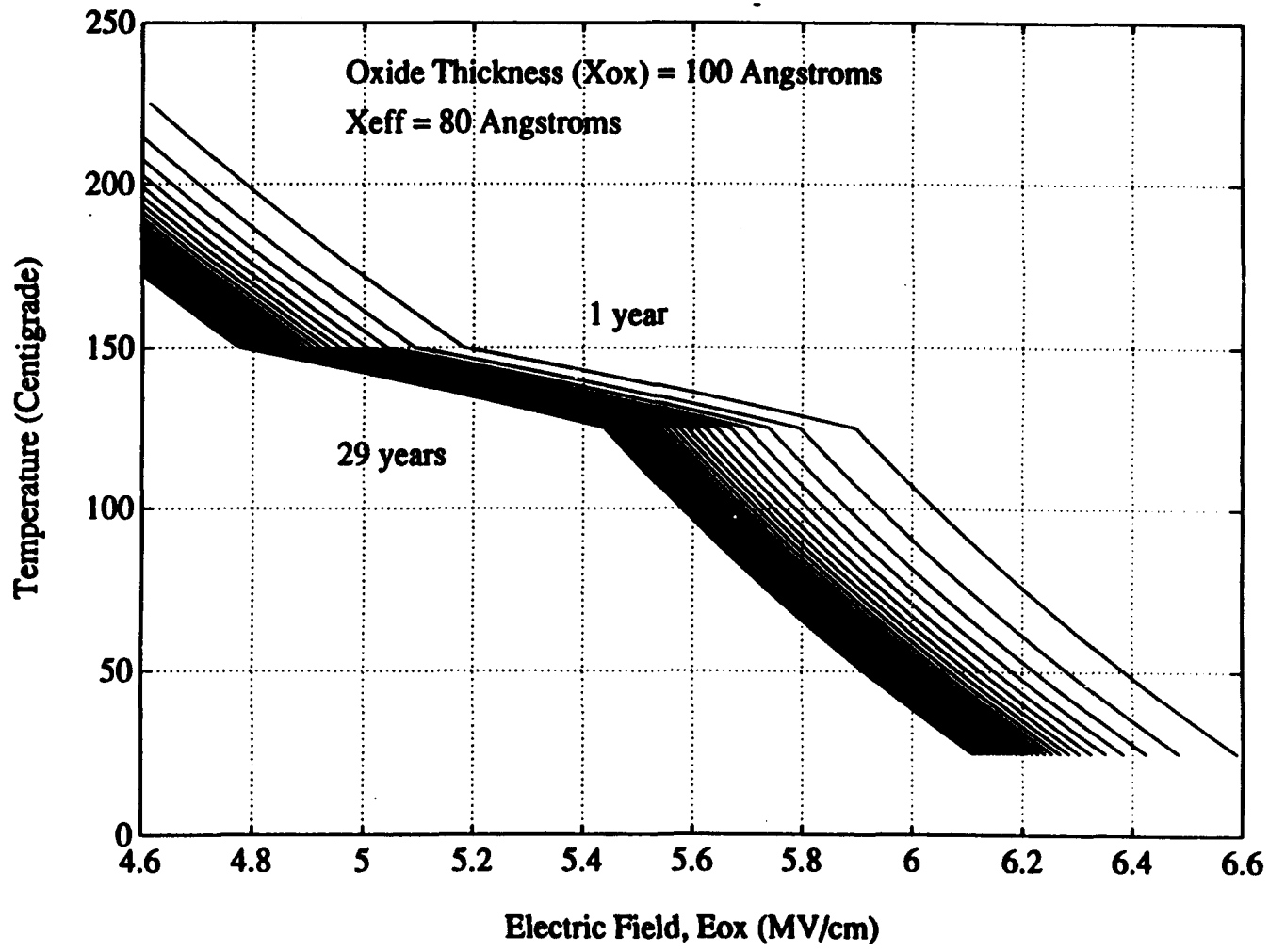


Figure 5.5 Due to the non-linear dependence of life under TDDB on temperature, worst case manufacturing defect magnitude, or electric field, derating the stress below a particular value may not result in noticeable benefit in terms of increased life because the time to failure is much beyond wear-out life of the device.

Figure 5.5b Derating curve for TDDB versus steady state temperature and electric field. The curves identify the various combinations of temperature T, and electric field E_{ox}, which will result in desired life. [Lee, 1988; Moazzami, 1989; Moazzami, 1990]



temperature storage bake in the neighborhood of 150°C to 250°C restores device characteristics. The maximum allowable steady-state temperature for the device is a function of the concentration of ionic contaminants in the oxide:

$$T_{operation} < T_{max} \tag{5.92}$$

such that

$$\Delta V_T < \Delta V_{T(max)} \tag{5.93}$$

where

$$\Delta V_T \propto E^{\frac{1}{2}} t^{\frac{1}{2}} e^{-\frac{\Delta H}{KT}} \tag{5.94}$$

and where

ΔV_T	is the change in threshold voltage (volt);
E	is the electric field across the oxide (volt/cm);
t	is the time under bias (seconds);
ΔH	is the activation energy (eV); and
K	is the Boltzmann constant (8.617×10^{-5} eV/K or 1.38×10^{-23} J/K);

N-channel devices are often covered with phosphosilicate glass films to stabilize the threshold voltage against changes resulting from ionic contamination.

5.6.2 Surface-Charge Spreading

This failure mechanism, occuring mostly in MOS devices, involves the lateral spreading of charge from the biased metal conductors along the oxide layer or through moisture on the device surface. The failure mechanism is manufacturing-defect-activated, due to the presence of ionic contaminants on the die surface. Derating for this failure mechanism involves controlling the amount of contaminant on the die.

5.7 DERATING FOR FAILURE MECHANISMS IN THE DEVICE OXIDE INTERFACE

5.7.1 Hot Electrons

The mechanism of hot electrons in MOS devices is inversely dependent on steady-state temperature. The minimum allowable steady-state temperature to avoid hot electrons can be calculated using the Lucky Electron Model [Ning 1977, Garrigues 1981]

$$T_{operation} < T_{min} \tag{5.95}$$

such that

$$P_e = P_o e^{-\frac{d}{\lambda_o \tanh\left(\frac{E_a}{2KT}\right)}} \tag{5.96}$$

where

$$d = \sqrt{\frac{2\epsilon_{SC}\epsilon_o}{qN_A}}\left(\sqrt{\Psi_S} - \sqrt{\Psi_S - \frac{\phi_{BS}}{q}}\right) \tag{5.97}$$

and where

P_e	is the emission probability of an electron;
P_o	is a constant ($\approx$ 2.9 @ 300°K; 4.3 @ 77°K);
d	is the minimum path length of an electron required to attain the critical energy, ϕ_{BS};
T	is the steady-state temperature (Kelvin);
E_a	is the activation for mean free-path length (0.063 eV);
λ_o	is a constant ($\approx$ 108 Å);
λ	is the electron mean free path between lattice interactions;
K	is Boltzmann's constant (8.617 x 10^{-5} eV/K or 1.38 x 10^{-23} J/K);
ϵ_{SC}	is the dielectric constant of the semiconductor (F cm^{-1});
ϵ_o	is the free-space permittivity (8.85 x 10^{-14} F cm^{-1});
N_A	is the concentration of acceptor doping atoms (cm^{-3});
q	is the magnitude of electronic charge (1.6 x 10^{-19} Coulomb);
Ψ_S	is the surface potential (volt); and
Φ_{BS}	is the Si-SiO_2 barrier height for electrons, taking into account the

lowering due to the Schottky effect.

5.8 DERATING FOR FAILURE MECHANISMS IN THE DIE AND DIE/SUBSTRATE ATTACH

5.8.1 Die Fracture

Westgaard-Bolger-Paris Equation-based Formulation. The maximum allowable temperature cycle should be less than the calculated temperature cycle magnitude:

$$\Delta T_{operation} < \Delta T_{max} \tag{5.98}$$

such that

$$N_f > \textit{mission life} \tag{5.99}$$

where

$$\Delta\sigma_{app} = 10^{-6}k|\alpha_s - \alpha_d|\Delta T\sqrt{\frac{E_s E_d L}{X}} \tag{5.100}$$

$$N_f = \frac{2}{(n-2)A(\Delta\sigma_{app})^n \pi^{\frac{n}{2}}}\left(\frac{1}{a_i^{\frac{(n-2)}{2}}} - \frac{1}{a_f^{\frac{(n-2)}{2}}}\right) \tag{5.101}$$

and where

A	is the die-material coefficient;
n	is the die-material exponent;
α_s	is the CTE of the substrate (/°C);
α_d	is the CTE of the die (/°C);
$\Delta\sigma_{app}$	is the mode I applied-stress amplitude (psi);
a_i	is the initial crack size (inch); and
a_f	is the final crack length at failure, which may be taken to be equal to the critical crack size (inch).

Suhir-Paris Equation-based Formulation. The maximum allowable temperature cycle should be less than the calculated temperature cycle magnitude:

$$\Delta T_{operation} < \Delta T_{max} \tag{5.102}$$

such that

$$K_{v\text{-}die} < K_{C\text{-}die} \tag{5.103}$$

$$K_{h\text{-}die} < K_{C\text{-}die} \tag{5.104}$$

and

$$\begin{aligned} \sigma &< \sigma_{Rupture\text{-}die} && @\ die\ middle \\ \sigma_1 &< \sigma_{Rupture\text{-}die} && @\ die\ edge \end{aligned} \tag{5.105}$$

and

$$\min(N_{f(v\text{-}die)}, N_{f(h\text{-}die)}) > N_{required} \tag{5.106}$$

where

$$N_{f(v\text{-}die)} = \frac{1}{(1-\frac{n_d}{2}) A_d^{n_d} \sigma^{n_d} \pi^{\frac{n_d}{2}}} [a_{f\text{-}die}^{1-\frac{n_d}{2}} - a_{i\text{-}die}^{1-\frac{n_d}{2}}] \tag{5.107}$$

$$N_{f(h\text{-}die)} = \frac{1}{(1-\frac{n_d}{2}) A_d^{n_d} p^{n_d} \pi^{\frac{n_d}{2}}} [a_{f\text{-}die}^{1-\frac{n_d}{2}} - a_{i\text{-}die}^{1-\frac{n_d}{2}}] \tag{5.108}$$

and

$$K_{v\text{-}die} = \sigma \sqrt{\pi\ a_{v\text{-}die}}\ F \tag{5.109}$$

$$K_{h\text{-}die} = p \sqrt{\pi\ a_{h\text{-}die}}\ F \tag{5.110}$$

$$F = \frac{2.85\left[0.953 - 2.369\left(\frac{a}{t_d}\right) + 2.74\tan\left(\frac{a}{t_d}\right)\right]}{3 + \frac{a^2}{c^2}} \tag{5.111}$$

$$\sigma = \frac{\frac{1}{t_d} + 3(t_d+t_s)\frac{E_d t_d}{12(1-\nu_d^2)D}}{\frac{1-\nu_d}{E_d t_d} + \frac{1-\nu_s}{E_s t_s} + \frac{(t_d+t_s)^2}{4D}}\left[1 - \frac{1}{\cosh(AL)}\right](\alpha_s - \alpha_d)\Delta T \tag{5.112}$$

$$p = -\left[\frac{t_s t_d^3 E_d}{12(1-\nu_d^2)} - \frac{t_d t_s^3 E_s}{12(1-\nu_s^2)}\right]\left[\frac{t_d}{3G_d} + \frac{2}{3}\frac{t_a}{G_a} + \frac{t_s}{3G_s}\right]^{-1}\frac{1}{2D}(\alpha_s - \alpha_d)\Delta T \tag{5.113}$$

$$\tau = \left[\frac{1-\nu_s}{E_s t_s} + \frac{1-\nu_d}{E_d t_d} + \frac{(t_d+t_s)^2}{4D}\right]^{-\frac{1}{2}}\left[\frac{t_d}{3G_d} + \frac{2t_a}{3G_a} + \frac{t_s}{3G_s}\right]^{-\frac{1}{2}}\tanh(AL)(\alpha_s - \alpha_d)\Delta T \tag{5.114}$$

$$A = \sqrt{\frac{\frac{1-\nu_s}{E_s t_s} + \frac{1-\nu_d}{E_d t_d} + \frac{(t_d+t_s)^2}{4D}}{\frac{t_d}{3G_d} + \frac{2t_a}{3G_a} + \frac{t_s}{3G_s}}} \tag{5.115}$$

$$D = \frac{E_d t_d^3}{12(1-\nu_d^2)} + \frac{E_a t_a^3}{12(1-\nu_a^2)} + \frac{E_s t_s^3}{12(1-\nu_s^2)} \tag{5.116}$$

$$\sigma_1 = \frac{p}{2} + \sqrt{\frac{p^2}{4} + \tau^2} \tag{5.117}$$

and where

$E,G,\nu,$	and α are the modulus of elasticity, the shear modulus, Poisson's ratio, and the coefficients of thermal expansion (CTE), respectively; t is the thickness. The subscripts $d,a,$ and s denote the die, attachment, and substrate, respectively. ΔT is the temperature change;
L	is the half-diagonal length of the die;
σ	is the tensile stress in the middle of the die;
p	is the peeling stress at the die-attachment interface;
τ	is the shear stress at the die-attachment interface;
σ_1	is the principal stress at the die edge;
$\sigma_{Rupture}$	is the modulus of rupture of the die;
K_v	and K_h are the stress-intensity factors for vertical cracks on the top surface of the die and for horizontal cracks at the edge of the die;
K_C	is the fracture toughness of the die;
a_{v-die}	is the depth of the vertical crack on the top surface of the die; and
a_{h-die}	is the length of the horizontal surface crack at the edge of the die.

5.8.2 Die Thermal Breakdown

The calculated junction temperature should be less than the allowable junction temperature of the device:

$$T_{junction} < T_{junction,allowable} \tag{5.118}$$

where $T_{junction,allowable}$ is the allowable junction temperature. $T_{junction}$ is the effective junction temperature calculated from

$$T_{junction} = T_{max} + Q \sum_{i=1}^{3} \theta_i \tag{5.119}$$

where T_{max} is the mean value of the maximum ambient temperature, and Q is the power dissipated by the devices. The effective thermal resistance of each layer, θ_i (die, attachment, and substrate), is determined from

$$\theta_i = \frac{1}{2k_i(L_i - W_i)} \left[\ln \frac{L_i(W_i + 2t_i)}{W_i(L_i + 2t_i)} \right] \tag{5.120}$$

where L_i, W_i, t_i are the lengths, widths, and thicknesses of each layer, and k_i is the thermal conductivity of each layer.

5.8.3 Die and Substrate Adhesion Fatigue

Suhir-Paris-(Coffin-Manson) Equation-based Formulation.

For brittle-attach materials: The maximum allowable temperature cycle should be less than the maximum calculated value, such that:

$$\Delta T_{operation} < \Delta T_{max} \tag{5.121}$$

such that,

$$K_{h\text{-}attach} < K_{C\text{-}attach} \tag{5.122}$$

where

$$K_{h\text{-}attach} = p\sqrt{\pi\, a_{h\text{-}attach}}\, F \tag{5.123}$$

$$N_{f(h\text{-}attach)} = \frac{1}{(1-\frac{n_a}{2}) A_a^{n_a} p^{n_a} \pi^{\frac{n_a}{2}}} \left[a_{f\text{-}attach}^{1-\frac{n_a}{2}} - a_{i\text{-}attach}^{1-\frac{n_a}{2}} \right] \tag{5.124}$$

and where

$a_{i\text{-}attach}$ is the initial attach-crack size;
$a_{f\text{-}attach}$ is the final attach-crack depth;
A_a and n_a are fatigue properties of the brittle attachment material;

p is the cyclic peeling stress determined in Equation 5.113;
F is the geometric correction factor given by Equation 5.111;
$K_{c\text{-}attach}$ is the fracture toughness of the attachment; and
$K_{h\text{-}attach}$ is the stress intensity factor for horizontal crack in the edge of the brittle attachment material.

For Ductile-attach Materials: The maximum allowable temperature cycle should be less than the maximum calculated value, such that:

$$\Delta T_{operation} < \Delta T_{max} \tag{5.125}$$

such that

$$\begin{aligned} C_f' \sigma_1 &< \sigma_{U\text{-}attach} \\ C_f'' \tau_M &< \tau_{U\text{-}attach} \end{aligned} \tag{5.126}$$

where

$$\begin{aligned} C_f' \sigma_1 &= \frac{3p}{2} + \sqrt{\left(\frac{3p}{2}\right)^2 + (4\tau)^2} \\ C_f'' \tau_M &= \sqrt{(3p)^2 + 3(4\tau)^2} \end{aligned} \tag{5.127}$$

$$\begin{aligned} N_{f\text{-}attach}(t) &= C_{attach} (C_f' \sigma_1)^{m_{attach}} \\ N_{f\text{-}attach}(s) &= C_{attach} (C_f'' \tau_M)^{m'_{attach}} \end{aligned} \tag{5.128}$$

and where

p and τ are the peeling and shear stresses given by Equations 5.113 and 5.114;
$\sigma_{U\text{-}attach}$ and $\tau_{U\text{-}attach}$ are the tensile strength and the shear strength of the attachment material;
C and m are the tensile fatigue constants;
C'_{attach} and m'_{attach} are the shear fatigue constants of the attachment material;
$C_f'\sigma_1$ is the local cyclic principal stress; and

$C_f''\tau_M$ is the local cyclic von Mises' stress.

5.9 DERATING FOR FAILURE MECHANISMS IN FIRST-LEVEL INTERCONNECTS

5.9.1 Wirebonded Interconnections

Wire Fatigue. The mechanism of wire fatigue involves the flexure of the wire about the reduced wire cross-section at the heel during temperature cycling. The mechanism has a dominant dependence on the magnitude of the temperature cycle and is independent of steady-state temperature. The maximum temperature cycle ($\Delta T_{operation}$) that the wire can be subjected to should be less than the calculated temperature cycle magnitude (ΔT_{max})[Pecht 1989],

$$\Delta T_{operation} < \Delta T_{max} \tag{5.129}$$

such that

$$N_f > \textit{mission life} \tag{5.130}$$

where N_f can be calculated from either of the following models: *Pecht et al. Model [Pecht et al. 1989]*

$$N_f = A(\epsilon_f)^n \tag{5.131}$$

and

$$\epsilon_f = \frac{r}{\rho_o}\left[\frac{Cos^{-1}((Cos\lambda_o)(1 - (\alpha_w - \alpha_s)\Delta T))}{\lambda_o} - 1\right] \tag{5.132}$$

and where

r	is the wire radius;
λ_o	is the angle of the wire with the substrate;
α_w	is the coefficient of thermal expansion of the wire;
α_s	is the coefficient of thermal expansion of the substrate;
ΔT	is the temperature cycle encountered by the structure;
ρ_o	is the initial radius of curvature of the wire;
N_f	is the mission life requirement; and
A	and n are material constants.

Hu et al. Model [Hu, Pecht, Dasgupta 1991]

$$N = C_w \sigma^{-m_w} \tag{5.133}$$

where

$$\sigma = 6\, E_w \frac{r}{D}\left(\frac{L}{D} - 1\right)^{\frac{1}{2}}\left(2\alpha_s + \frac{\alpha_s - \alpha_w}{1 - \frac{D}{L}}\right)\Delta T \tag{5.134}$$

and where

$2L$	is the wire length;
$2D$	is the wire span;
E_w	is the elastic modulus of the wire;
α_w	and α_s are the coefficients of thermal expansion of the wire and the substrate materials, respectively;
ΔT	is the temperature change encountered during operation;
σ	is the bending stress (already calculated); and
C_w	and m_w are fatigue properties determined by tensile fatigue tests of the wire material.

Wirebond Fatigue.

Bond Pad Shear Fatigue: The maximum temperature cycle ($\Delta T_{operation}$) that the wire-wirebond assembly can be subjected to without causing shear fatigue failure of the bondpad should be less than the calculated temperature cycle magnitude (ΔT_{max}) [Hu, Pecht, Dasgupta 1991]:

$$\Delta T_{operation} < \Delta T_{max} \tag{5.135}$$

$$\Delta T_{max} = \frac{\left(\frac{N_s}{C_p'}\right)^{-\frac{1}{m_p'}}}{\left(\frac{G_p}{b_p Z}\right)\left[(\alpha_w - \alpha_s) - \frac{(\alpha_s - \alpha_p)}{\left(1 + \frac{E_s A_s}{\frac{E_p A_p}{(1 - \nu_s)}}\right)}\right]} \qquad (5.136)$$

and

$$Z^2 = \frac{G_p}{b_p}\left(\frac{r}{E_w A_w} + \frac{(1 - \nu_s)W_p}{E_s A_s}\right) \qquad (5.137)$$

and where

N_R	is the mission profile requirement for the number of cycles to failure;
C_p'	and m_p' are the shear fatigue properties for the bond-pad materials;
G_p	is the shear modulus of the bond-pad material;
b_p	is the bond-pad thickness;
Z	is given by Equation 5.137;
ΔT	is the temperature cycle magnitude;
α_s,	α_p, α_w, are the coefficients of thermal expansion for the substrate, pad, and wire, respectively;
E_p,	and E_s are the modulus of elasticity of the pad and the substrate, respectively;
ν_s	is Poisson's ratio for the substrate materials;
A_p	is the cross-sectional area of the pad;
A_s	is the effective cross-sectional area of the substrate, equal to $b_s(W_p+W_s)/2$; and
W_p	is the width of the bond pad.

Wire Shear Fatigue: The maximum temperature cycle ($\Delta T_{operation}$) that the wire-wirebond assembly can be subjected to without causing shear fatigue of the wire should be less than the calculated temperature cycle magnitude ($z\Delta T_{max}$) [Hu, Pecht, Dasgupta 1991]:

$$\Delta T_{operation} < \Delta T_{max} \tag{5.138}$$

where

$$\Delta T_{max} = \frac{\left(\frac{N_R}{C_w'}\right)^{-\frac{1}{m_w'}}}{\left(\frac{r^2}{4Z^2A_w^2}\left(\frac{Cosh(z\,x)}{Cosh(z\,l_w)} - 1\right)^2 + \frac{Sinh^2(Z\,x_w)}{Cosh^2(Z\,l_w)}\right)^{\frac{1}{2}}Q} \tag{5.139}$$

$$Z^2 = \frac{G_p}{b_p}\left(\frac{r}{E_wA_w} + \frac{(1 - \nu_s)W_p}{E_sA_s}\right) \tag{5.140}$$

$$Q = \left(\frac{G_p\Delta T}{b_p Z}\right)\left((\alpha_w - \alpha_s) - \frac{(\alpha_s - \alpha_p)}{\left(1 + \frac{E_s A_s}{\frac{E_p A_p}{(1 - \nu_s)}}\right)}\right) \tag{5.141}$$

and where

N_R is the mission profile requirement for the number of cycles to failure;

C_w and m_w are the Coffin-Manson coefficients for wire material;

r is the wire radius;

Z is given by Equation 5.140;

A_w is the effective cross-sectional area of the wire at the bond = (0.6 wire diameter) x (1.5 wire diameter);

x is the position along the length of the bond (x=0 is the center of the bond);

l_w = half the length of the bond (total bonded length = 2 l_w);

Q is given by Equation 5.141;

G_p is the shear modulus of the bond pad;

b_p is the bond-pad thickness;

W_p is the width of the bond pad;

E_w is the elastic modulus of the wire;

E_p is the elastic modulus of the bond pad;
E_s is the elastic modulus of chip;
A_s is the effective cross-sectional area of the substrate, equal to $b_s(W_p+W_s)/2$;
A_p is the cross-sectional area of the pad; and
α_s, α_p, α_w, are the coefficients of thermal expansion for the substrate, pad, and wire, respectively.

Chip Shear Fatigue Leading to Cratering: The maximum temperature cycle ($\Delta T_{operation}$) that the wire-wirebond assembly can be subjected to without causing shear fatigue of the chip should be less than the calculated temperature cycle magnitude (ΔT_{max}) [Hu, Pecht, Dasgupta 1991]

$$\Delta T_{operation} < \Delta T_{max} \tag{5.142}$$

where

$$\Delta T_{max} = \frac{\left(\frac{N_R}{C_s'}\right)^{-\frac{1}{m_s'}}}{\left(\left(\frac{W_p Q}{2ZA_s}\left(1 - \frac{Cosh(Zx_w)}{Cosh(Zl_w)}\right) + \frac{(\alpha_s - \alpha_p)}{\frac{(1-\nu_s)}{(E_s A_s)} + \frac{1}{(E_p A_p)}}\right)^2 + Q^2 \frac{Sinh^2(Zx_w)}{Cosh^2(Zl_w)}\right)^{\frac{1}{2}}}$$

$$Z^2 = \frac{G_p}{b_p}\left(\frac{r}{E_w A_w} + \frac{(1-\nu_s)W_p}{E_s A_s}\right) \tag{5.144}$$

$$Q = \left(\frac{G_p \Delta T}{b_p Z}\right)\left((\alpha_w - \alpha_s) - \frac{(\alpha_s - \alpha_p)}{\left(1 + \frac{E_s A_s}{\frac{E_p A_p}{(1-\nu_s)}}\right)}\right) \tag{5.145}$$

and where

N_R is the mission profile requirement for the number of cycles to failure;
C_w and m_w are the Coffin-Manson coefficients for the wire material;
r is the wire radius;
Z is given by Equation 5.140;
A_w is the effective cross-sectional area of the wire at the bond = (0.6 wire diameter) x (1.5 wire diameter);
x is the position along the length of the bond (x=0 is the center of the bond);
l_w is half the length of the bond (total bonded length = 2 l_w);
Q is given by Equation 5.141;
G_p is the shear modulus of the bond pad;
b_p is the bond pad thickness;
W_p is the width of the bond pad;
E_w is the elastic modulus of the wire;
E_p is the elastic modulus of the bond pad;
E-s is the elastic modulus of the chip;
A_s is the effective cross-sectional area of the substrate, equal to $b_s(W_p+W_s)/2$;
A_p is the cross-sectional area of the pad; and
α_s, α_p, α_w, are the coefficients of thermal expansion for the substrate, pad, and wire, respectively.

Intermetallic Formation. The maximum operating temperature for a bimetallic wirebond system can be obtained by using the parabolic relationship [Kidson 1961]:

$$t = \frac{x^2}{k} \tag{5.146}$$

The maximum allowable operating temperature is less than the calculated operating temperature:

$$T_{operation} < T_{max} \tag{5.147}$$

where

$$T_{max} = -\frac{Q}{R \ln\left(\frac{x^2}{D_0 t}\right)} \qquad (5.148)$$

$$k = D_0 e^{-\frac{Q}{RT}}$$

and where

x is the critical intermetallic layer thickness (from Tables 5.8 and 5.9);

t is time to failure due to intermetallic formation;

k = rate constant, depending on the interdiffusion coefficients of the bonded materials (from Table 5.9).

Table 5.8 The Dominant Intermetallic Compounds for Common Bimetal Combinations

Bimetal Combination	Intermetallic Compounds Formed	Dominant Intermetallic Compounds
gold-aluminum (Au-Al)	Au_5Al_2, Au_2Al, $AuAl_2$, AuAl, Au_4Al [Philosky 1970, Philosky 1971]	Au_5Al_2, Au_2Al
copper-aluminum (Cu-Al)	$CuAl_2$, CuAl, $CuAl_2$, Cu_9Al_4 [Olsen and James 1984, Pitt and Needes 1981, Gershinskii 1977, Campisano 1978, Funamizu and Watanabe 1971]	$CuAl_2$
gold-silver (Au-Ag)	significant silver diffusion into the wire bulk along the wire length. Rapid silver surface diffusion resulted in depletion at bond periphery [James 1977].	
copper-gold (Cu-Au)	Cu_3Au, CuAu, $CuAu_3$ [Hall 1975, Tu and Berry 1972]	Cu_3Au

Table 5.9 Rate Constants and Activation Energies for Common Material Combinations

Material Combination	Q (cal mol^{-1})	Critical Layer Thickness (t_i = thickness of i th element)	Rate constant (k) ($cm^2\ sec^{-1}$); R = 1.98719 cal $mol^{-1}\ K^{-1}$
gold-aluminum (Au-Al)	15,900	gold bond pad [Philosky 1970, Philosky 1971]: $t_{Au} + (2/5)\ t_{Au}$ aluminum bond pad: $t_{Al} + (2.5)\ t_{Al}$	$k = 5.2 \times 10^{-4}\ e^{-\frac{Q}{RT}}\ \frac{cm^2}{sec}$
gold-silver (Au-Ag)	15,000	t_{Ag} [James 1977]	$k = 7.65 \times 10^{-4}\ e^{-\frac{Q}{RT}}\ \frac{cm^2}{sec}$

The critical intermetallic layer thickness is calculated based on the intermetallic compounds that form the fastest for the bimetallic combination. The dominant compounds for some of the common material combinations are given in Table 5.8. The composition of the intermetallic compound when critical layer thickness is reached, and rate constants for various material combinations, are given in Table 5.9. The time to failure is calculated as the time for complete consumption of the bond pad in the intermetallic reaction. For example, in gold-aluminum bonds, the compound Au_5Al_2 forms the fastest and is the dominant product during intermetallic formation. Thus, for gold bond pads, the critical layer thickness is defined as the time to reach an intermetallic compound thickness of $t_{Au} + (2/5)\ t_{Au}$, where t_{Au} is the thickness of the gold bond pad.

The time to failure versus temperature is then plotted, based on Equation 5.146. The maximum operating temperature of the device for a given mission life is calculated from the graph (Figures 5.6 a,b, and c). A similar procedure can be followed for each of the intermetallic combinations. Based on Philosky's observations of the layer thicknesses of intermetallic compounds at various temperatures (Table 5.10), a graph of intermetallic layer thickness versus square-root time to failure can be drawn (Figure 5.7) [1971]. A horizontal line on the graph at a thickness equal to the wire thickness at the bond pad gives the time-temperature product that will result in failure after time equal to the abscis. The allowable time-temperature for a desired mission life can thus be computed. The slope of each of the lines in Figure 5.7 gives rate constants at various

Figure 5.6 Time for heel of the wire to transform to intermettalic versus temperature. The temperature at which intermetallic formation has a dominant dependence on steady state temperature is a function of the bond geometry [Philosky, 1970, 1972]

Figure 5.6a For gold wire bonded to aluminum metallization

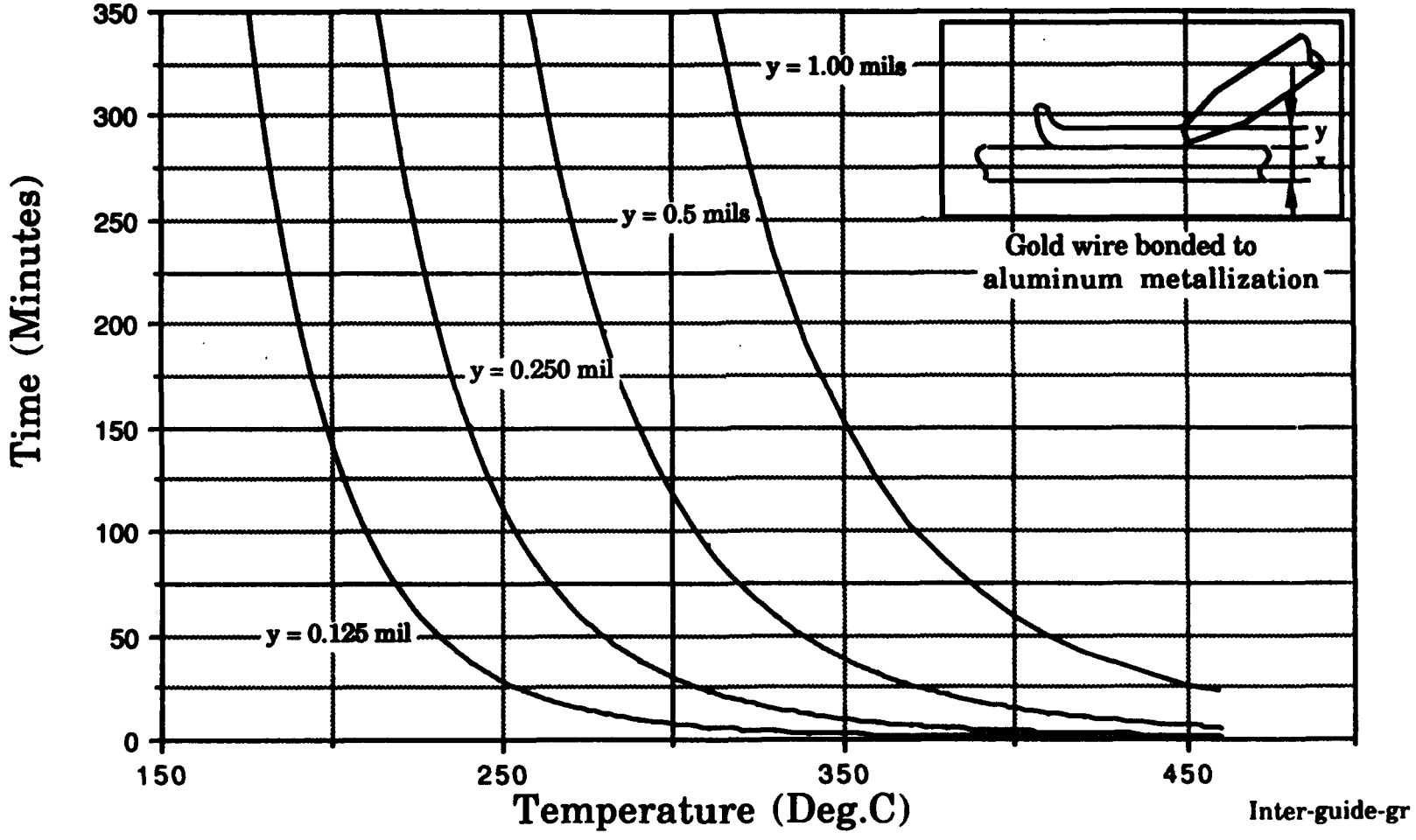


Figure 5.6 Time for heel to transform to intermettalic versus temperature. The temperature at which intermetallic formation has a dominant dependence on steady state temperature is a function of the bond geometry [Philosky, 1970, 1971]

Figure 5.6b For aluminum wire bonded to gold metallization

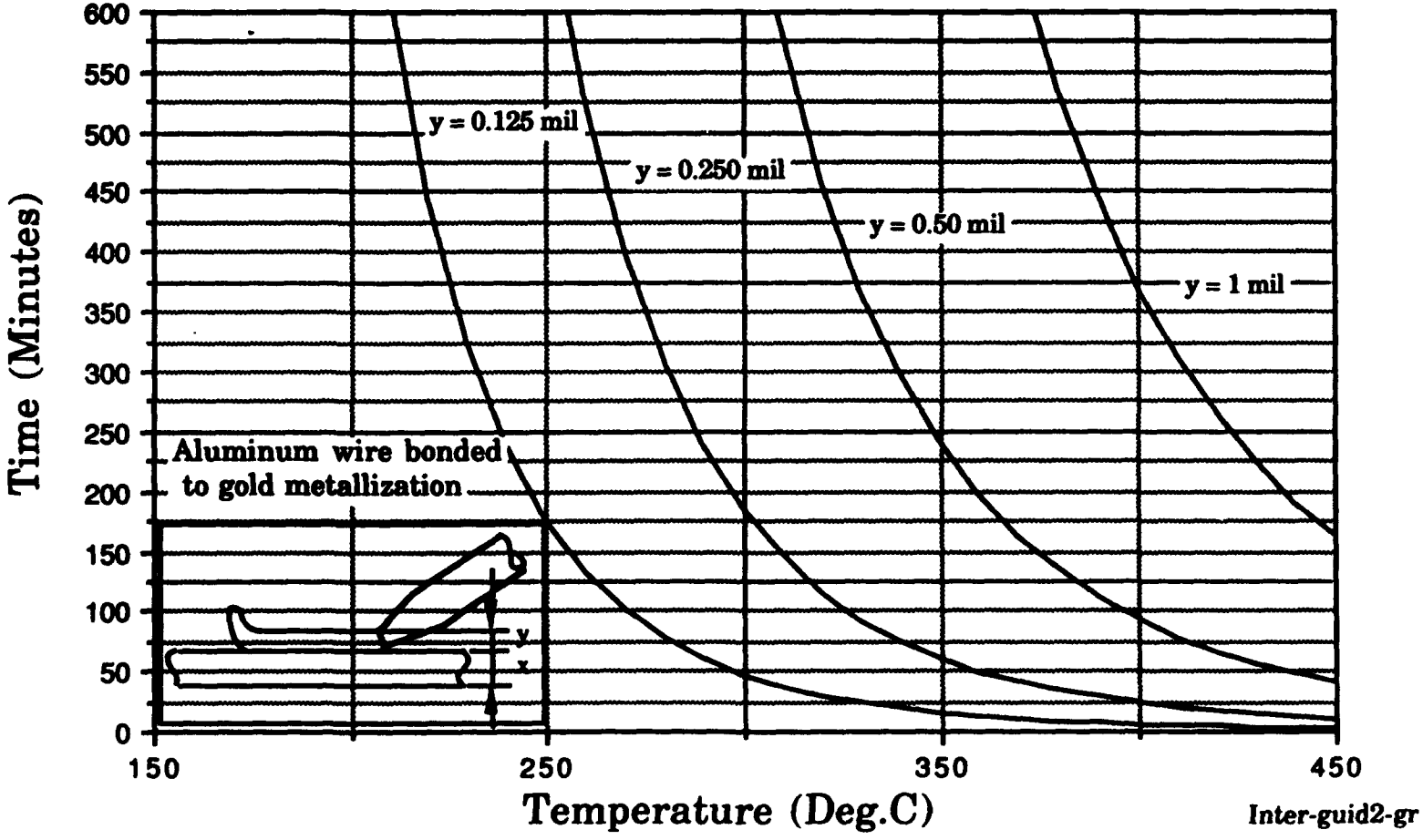


Figure 5.6c Time to failure versus temperature and bond pad thickness. The time to failure at any temperature may be much greater than the mission life depending on the bond pad thickness. [Philosky, 1970, 1971]

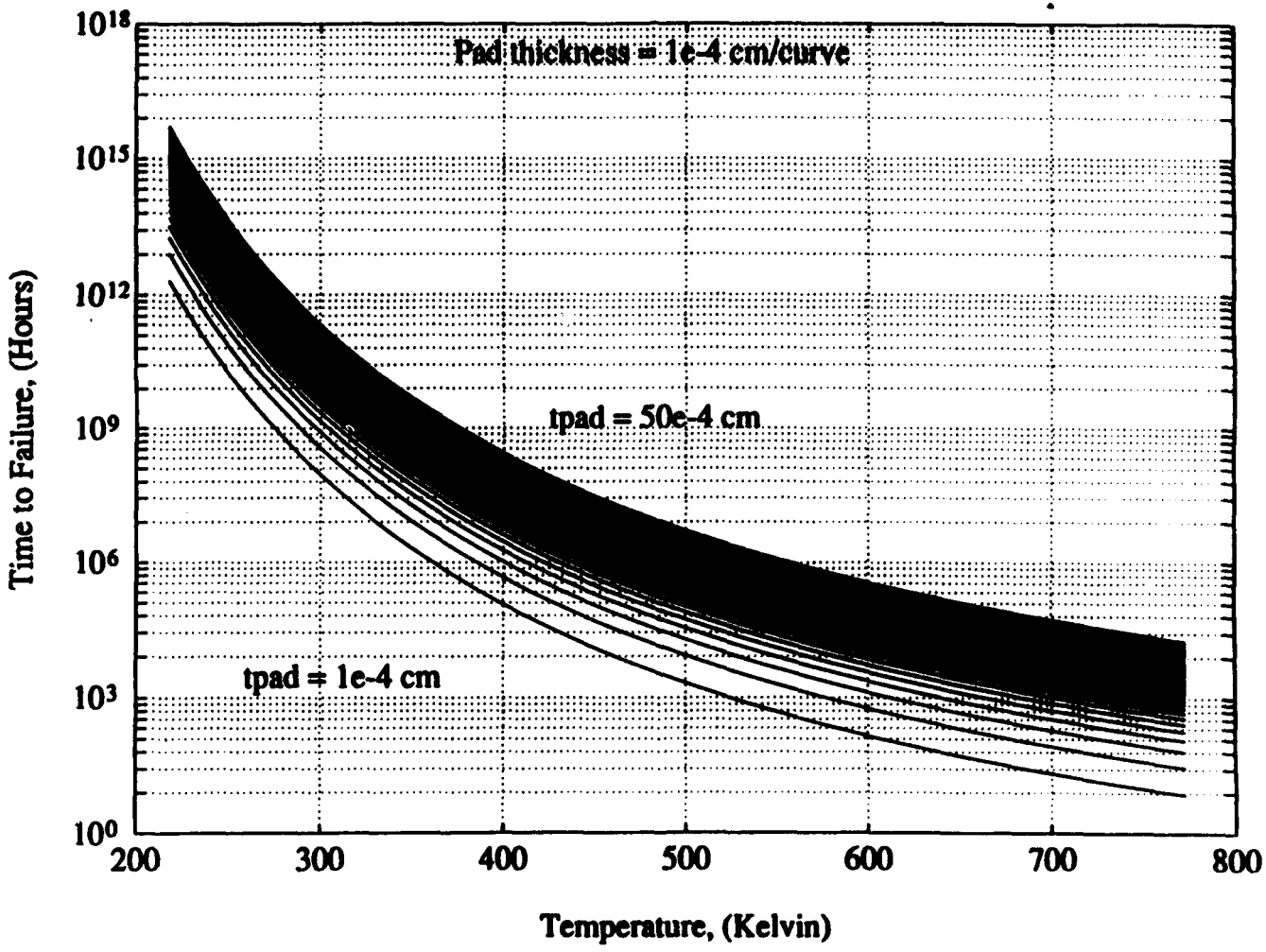
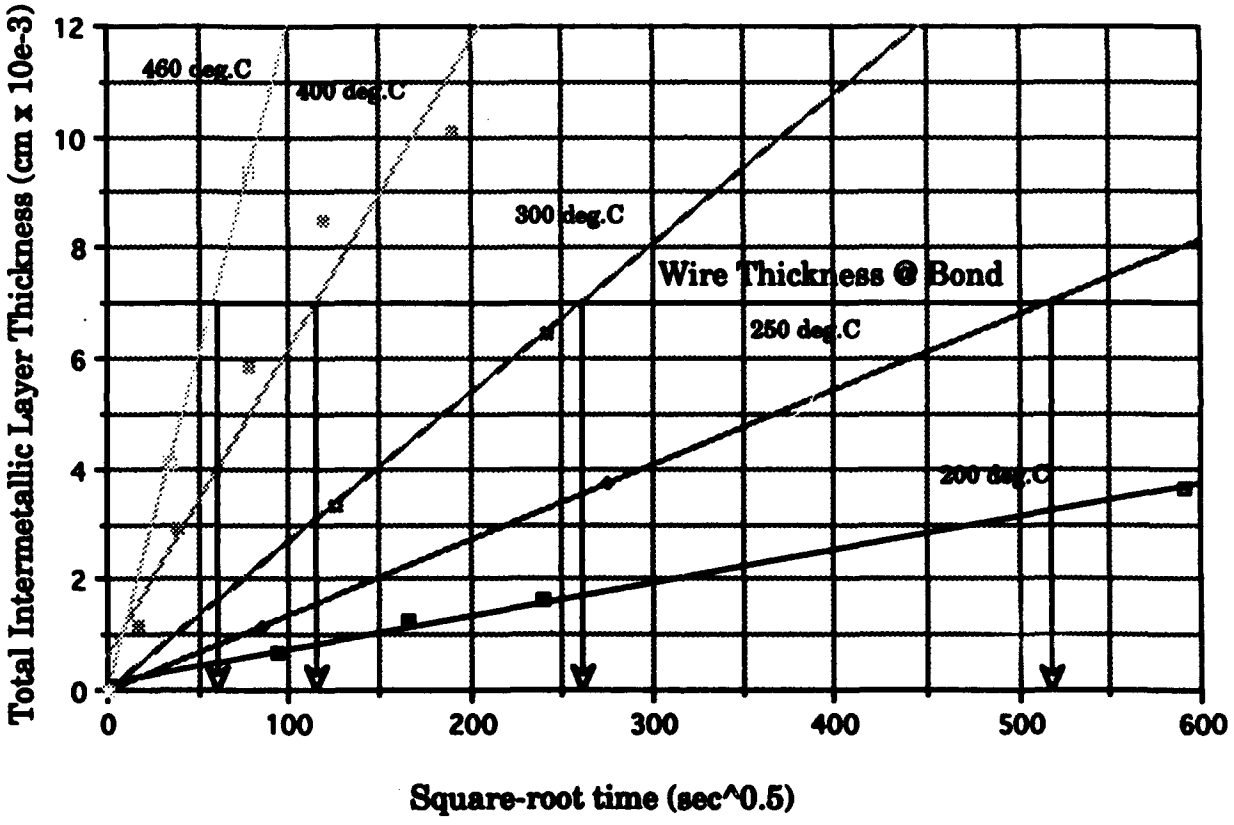


Figure 5.7 Various time-temperature products which will result in gold-aluminum intermetallic growth [Philosky]. A horizontal line on the graph at a thickness equal to the wire thickness at the bond pad gives the time-temperature product which will result in failure after time equal to the abcissa. The slope of each line gives the rate constants at various temperatures.



temperatures. Intermetallic formation in aluminum-gold systems can be eliminated either by using a fritless gold composition that impedes intermetallic formation or by using diffusion barrier disks attached between the aluminum (Al) wire and thick film [Palmer and Gaynard 1978].

Table 5.10 Measured Thickness of Gold-Aluminum (Au-Al) Intermetallic Compounds. [Philosky, 1971]

Temperature (°C)	Time (Seconds)	$AuAl_2$ cm x 10^{-3}	AuAl cm x 10^{-3}	Au_2Al cm x 10^{-3}	Au_5Al_2 cm x 10^{-3}	Au_4Al cm x 10^{-3}	Total cm x 10^{-3}
200	8700	0	0	0	0.68	0	0.69
200	27300	0	0	0	1.22	0	1.25
200	57600	0	0	0	1.57	0	1.63
200	349200	0.21	0	0.53	2.68	0.21	3.63
250	7200	0	0	0	1.09	0	1.13
250	75600	0.24	0	0.8	2.47	0.24	3.75
300	15900	0.11	0	0.72	2.38	0.17	3.38
300	58200			1.29	4.75	0.23	6.5
350	22200	0.27	0	0.1	1.65	0.11	2.13
350	24000	0.42	0	0.52	6.31		7.38
400	300	0.15	0	0.09	0.89	0	1.14
400	1500	0.32	0	0.29	2.32	0	2.94
400	6000	0.36	0	0.93	4.57	0	5.88
400	14400	0.33	0.12	1.48	6.46	0.11	8.5
400	36000	0.26	0.27	2.36	7.03	0.21	10.13
460	1200	0.26	0.27	1.24	2.36	0	4.13
460	6000	0.21	0.35	1.4	7.14	0.28	9.38

5.9.2 Tape Automated Bonds

Thermally Induced Solder-joint Fatigue. The temperature cycle magnitude to which the device is subjected should be less than the maximum allowable:

$$\Delta T < \Delta T_{max} \tag{5.151}$$

such that

$$N_f > \textit{mission life} \tag{5.152}$$

where

$$N_f = \frac{1}{2}\left(\frac{1}{2\epsilon_f'}\frac{K(L_D \Delta\alpha\, \Delta T_e)^2}{200 A_{eff} h_{solder}}\right)^{\frac{1}{c}} \tag{5.153}$$

$$c = -0.442 - 6\times10^{-4} T_{sj} + 1.74\times10^{-2} \ln\left[1 + \left(\frac{360}{t_D}\right)\right] \tag{5.154}$$

and

$$T_{sj} = \frac{1}{4}(T_c + 2T_o + T_s) \tag{5.155}$$

and where

- T_S and T_C are the steady-state operating temperatures of the substrate and component, respectively;
- T_O is the temperature during off half-cycle;
- t_D is the half-cycle dwell time in minutes;
- K is the diagonal flexural stiffness of the unconstrained lead, determined by finite element analysis [Barker 1991] or strain-energy methods;
- $\Delta\alpha$ is the difference in the coefficients of thermal expansion of the die and the substrate;
- ΔT_{max} is the maximum allowable equivalent temperature range;
- ϵ_f' is the fatigue ductility coefficient;
- A_{eff} is the effective solder-joint area, which is two-thirds of the vertical projection of the solder-wetted lead area;
- h_{solder} is the height of the solder joint; and
- t_D is the half-cycle dwell time in minutes.

5.9.3 Flip-Chip Bonds

The temperature cycle magnitude to which the device is subjected should be less than the maximum allowable:

$$\Delta T < \Delta T_{max} \tag{5.156}$$

such that

$$N_f > \textit{Mission Life} \tag{5.157}$$

where

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma}{2\epsilon_f}\right]^{\frac{1}{c}} \tag{5.158}$$

$$c = \alpha + \beta\, T_{SJ} + \gamma\, \ln\left(1+\frac{360}{t_D}\right) \tag{5.159}$$

$$\begin{aligned}\Delta\gamma &= k_g\delta \\ &= k_g d\left[\alpha_c\{T_{jc}-T_{amb}\}-\alpha_{st}\{T_{jc}-\theta_{sol}\left(\frac{P_{chip}}{n}\right)-T_{amb}\}\right]\end{aligned} \tag{5.160}$$

$$k_g = \frac{1}{(\pi r_{critical}^2)^{1/\beta}\int_0^h \frac{dy}{[\pi(R^2-y^2)]^{1/\beta}}} \tag{5.161}$$

$$T_{SJ} = \frac{1}{4}\left[2T_{jc}-\theta_{sol}\left(\frac{P_{chip}}{n}\right)+2T_{amb}\right] \tag{5.162}$$

$$\theta_{sol} = \frac{h}{K A_{eff}} \tag{5.163}$$

and where

ϵ_f is the fatigue ductility coefficient of the solder material;
α, β, and γ are factors to be determined empirically;
T_{SJ} is the mean cyclic solder-joint temperature (°C);
t_D is half-cycle dwell time in minutes;
k_g is the geometric parameter;
δ is the total displacement;
d is the distance of farthest solder joint from neutral axis;
α_c and α_{st} are the coefficients of thermal expansion of the chip and the substrate, respectively;
T_{jc} is the junction temperature;
T_{amb} is the ambient temperature;
θ_{sol} is the thermal resistance of the solder;
P_{chip} is the chip power rating;
n is the number of solder bumps on the chip;
h is the height of the solder;
$r_{critical}$ is the critical interface radius;
K is the thermal conductivity of the solder; and
A_{eff} is the effective area of cross section of the solder;

5.10 DERATING FOR FAILURE MECHANISMS IN THE PACKAGE CASE

5.10.1 Cracking in Plastic Packages

The maximum temperature during thermal shock to which the device can be subjected can be calculated from:

$$T < T_{max} \tag{5.164}$$

such that

$$\sigma_{max} < \sigma_{crit}(T_{max}) \tag{5.165}$$

where

$$\sigma_{max} = 6K\left(\frac{a}{t}\right)^2 P \tag{5.166}$$

$$P = H_1 P_{sat}(T_{max}) \tag{5.167}$$

and where

H_1 is the relative humidity of the saturation ambient prior to temperature shock;

T_{max} is the peak temperature of the thermal shock;

K is a dimensionless stress concentration factor that depends on the aspect ratio of the die pad (K=0.05 for a square pad);

a is the length of the short side of the die pad;

t is the thickness of the molding compound under the pad;

P is the vapor pressure in the cavity; and

σ_{crit} is the value of critical stress.

5.10.2 Reversion or Depolymerization of Polymeric Bonds

Reversion is a steady-state temperature-dependent phenomenon that actuates above the reversion temperature for the encapsulant or molding compound. Derating for reversion involves limiting the maximum temperature for device operation to lower than the depolymerization temperature:

$$T < T_{depolymerization} \tag{5.168}$$

5.10.3 Whisker and Dendritic Growth

Cases coated with tin are prone to whiskers and dendrites. Whiskering can, however, be reduced by increasing the coating thickness during manufacture. Typically, hot-dipping is used to obtain a stress-free tin coating. If electroplating is used, tin is reflowed to remove residual stress, and 2 to 3% lead is added to the tin to retard whisker growth. This is a contamination- actuated mechanism and has no temperature dependence.

5.10.4 Modular Case Fatigue Failure

The temperature cycle magnitude to which the device is subjected should be less than the maximum allowable:

$$\Delta T < \Delta T_{max} \tag{5.169}$$

such that

$$N_f > \textit{mission life} \tag{5.170}$$

where

$$\tau_{max} = 2\sigma_f(2N_f)^b \tag{5.171}$$

and

$$\tau_{max} = \left[\frac{1-\nu_h}{E_h t_h} + \frac{1-\nu_w}{E_w t_w} + \frac{(t_w+t_h)^2}{4D}\right]^{-\frac{1}{2}} \left[\frac{t_w}{3G_d} + \frac{2t_a}{3G_a} + \frac{t_h}{3G_h}\right]^{-\frac{1}{2}} \tanh(AL)\Delta\alpha\Delta T \tag{5.172}$$

$$A = \sqrt{\frac{\dfrac{1-\nu_h}{E_h t_h} + \dfrac{1-\nu_w}{E_w t_w} + \dfrac{(t_w+t_h)^2}{4D}}{\dfrac{t_w}{3G_w} + \dfrac{2t_a}{3G_a} + \dfrac{t_h}{3G_h}}} \tag{5.173}$$

The flexural rigidity of the structure, D, is defined as

$$D = \frac{E_h t_h^3}{12(1-\nu_h^2)} + \frac{E_a t_a^3}{12(1-\nu_a^2)} + \frac{E_w t_w^3}{12(1-\nu_w^2)} \tag{5.174}$$

and

ν is Poisson's ratio;
E is the modulus of elasticity;
t is the thickness;
G is the shear modulus;
L is the length of the joint;

$\Delta\alpha$ is the difference in the CTEs of the case wall and header materials; and Subscripts h, w and a denote the header, wall and attach material, respectively

5.11 DERATING FOR FAILURE MECHANISMS IN LID SEALS

5.11.1 Thermal Fatigue of Lid Seal

Lid and Case Material are the Same. Most lid-seal failures are overstress failures, fatigue is not a concern in most applications. The temperature cycle magnitude to which the device is subjected should be less than the maximum allowable:

$$\Delta T < \Delta T_{max} \tag{5.175}$$

such that

$$\sigma_1 < \sigma_{ult(seal)} \tag{5.176}$$

The maximum principal stress in the seal is calculated using Mohr's circle, where the shear stress at any seal cross-section at a distance, x, from the center cross-section is

$$\tau = \frac{\Delta\alpha\Delta T}{\sqrt{\kappa\lambda}} \frac{\sinh\left(\sqrt{\frac{\lambda}{\kappa}}x\right)}{\sinh\left(\sqrt{\frac{\lambda}{\kappa}}l_{seal}\right)} \tag{5.177}$$

and the normal stress at any cross-section at a distance x from the mid-section of the seal is

$$\sigma(x) = \frac{\Delta\alpha\Delta T}{\lambda t_{seal}}\left[1 - \frac{\cosh\left(\sqrt{\frac{\lambda}{\kappa}}x\right)}{\cosh\left(\sqrt{\frac{\lambda}{\kappa}}l_{seal}\right)}\right] \tag{5.178}$$

where

$\Delta\alpha$ is the difference in the coefficients of thermal expansion of the lid and case material and the seal material;

ΔT is the difference between the sealant melting point (stress-free

temperature) and operating temperature;

λ is the in-plane compliance of the joint ($=[(1-\nu_{case})/E_{case}(h_{cavity}+t_{lid})] + [(1-\nu_{seal})/E_{seal}t_{seal}]$);

κ is the interfacial compliance, given as the sum of the individual compliances for the seal and the case or lid material; that is, $\kappa = \kappa_{seal} + \kappa_{case}$, while $\kappa_{seal} = 2(1+\nu_{seal})t_{seal}/3E_{seal}$ and $\kappa_{case} = 2(1+\nu_{case})(h_{cavity}+t_{lid})/3E_{case}$. l_{seal} is half the seal length (or width).

Lid and Case Material are Different. The temperature cycle magnitude to which the device is subjected should be less than the maximum allowable:

$$\Delta T < \Delta T_{max} \tag{5.179}$$

such that

$$\sigma_1 < \sigma_{ult(seal)} \tag{5.180}$$

where the principal stress in the seal is

$$\sigma_1 = \frac{p}{2} \pm \sqrt{\frac{p^2}{4}+\tau^2} \tag{5.181}$$

$$\tau = \left[\frac{1-\nu_c}{E_c t_c} + \frac{1-\nu_l}{E_l t_l} + \frac{(t_c+t_l)^2}{4D}\right]^{-1/2} (G')^{-1/2} \tanh(Al_{seal})\ \Delta\alpha\Delta T \tag{5.182}$$

$$p = -\left[\frac{t_c t_l^3 E_l}{12(1-\nu_l^2)} - \frac{t_l t_c^3 E_c}{12(1-\nu_c^2)}\right]\frac{1}{2G'D}\Delta\alpha\Delta T \tag{5.183}$$

and where

p is the peeling stress;

τ is the shear stress in the seal;

ν, E, l, and t denote Poisson's ratio, Young's modulus of elasticity, the length, and the thickness, respectively; subscripts l, c and s denote that the symbols refer respectively to the lid, case, and seal;

$\Delta\alpha$ is computed as $(\alpha_c - \alpha_l)$, where α is the coefficient of thermal expansion;

ΔT is the temperature excursion with respect to the stress-free state of the seal, or the sealing temperature; A, D, and G' are defined as

$$A = \sqrt{\frac{\frac{1-\nu_c}{E_c t_c} + \frac{1-\nu_l}{E_l t_l} + \frac{(t_c+t_l)^2}{4D}}{G'}} \tag{5.184}$$

$$D = \frac{E_c t_c^3}{12(1-\nu_c^2)} + \frac{E_l t_l^3}{12(1-\nu_l^2)} + \frac{E_s t_s^3}{12(1-\nu_s^2)} \tag{5.185}$$

$$G' = \frac{t_c}{3G_c} + \frac{2t_s}{3G_s} + \frac{t_l}{3G_l} \tag{5.186}$$

where G is the shear modulus of elasticity.

6

CONCLUSION

The temperature dependencies of the failure mechanisms existing at various package elements have been investigated in terms of steady state temperature, temperature cycle, temperature gradient, and time dependent temperature change (Tables 2.8, 2.9). It has been found that temperature dependencies for the same mechanism are not the same at all operating temperatures. The mechanisms have been broadly grouped into the steady state temperature ranges of -55°C to 150°C, 150°C to 400°C, and T > 400°C (Tables 2.10, 2.11). The investigation demonstrates that there is no steady state temperature dependence for any of the failure mechanisms in the equipment operating range of -55°C to 125°C, but the steady state temperature dependence increases for temperatures above 150°C as more mechanisms assume a dominant steady state temperature dependence. An overview of the effects of temperature on microcircuits can be categorized as follows:

Steady State Temperature Effects

- Changes in semiconductor characteristics due to
  - steady state temperature dependence of semiconductor characteristics such as resistivity which can lead to failures in form of thermal runaway (*e.g. electrical overstress*).

- steady state temperature dependence of contaminants in the semiconductor that affect electronic functions or compatibility with the circuit parameters (*e.g. ionic contamination*).

- manufacturing defects which will cause device failures after prolonged operation under voltage and steady state temperature (*e.g., TDDB*).

- Increase in susceptibility to failure due to an environmental stress, at higher temperatures (T dependence)

(*e.g. electrostatic discharge*).

- Increase in susceptibility to failure due to a failure mechanism at lowered temperature, i.e the failure mechanisms are inversely dependent on steady state temperature (*e.g., stress driven diffusive voiding, and hot electrons*).
- Increase in susceptibility to failure under steady state temperature stress above a threshold value of temperature (*e.g., hillock formation, metallization migration, contact spiking, encapsulant reversion, electromigration*).

Temperature Cycle Magnitude Effects

- Temperature cycles result in cyclic fatigue failures due to mechanical stresses and dimensional changes caused by thermal mismatches between mating surfaces (*e.g., wirebond shear and flexure fatigue, die fracture, die adhesive fatigue*).

Temperature Gradient Effects

- Sites of maximum temperature gradient provide most probable sites for failure due to mass transport mechanisms. (*e.g., electromigration damage at high current occurs at sites of maximum temperature gradient*)

Time Dependent Temperature Change Effects

- Time dependent temperature changes produce very large stress transients resulting in material failure. (*e.g., encapsulant cracking*)
- Temperature change in time may activate or de-activate a failure mechanism. (*e.g., duty cycle serves as an ON/OFF switch for the corrosion process by evaporation of the electrolyte at higher temperatures*)

The use of a simple Arrhenius expression to model microelectronic device reliability at all steady state temperatures is not correct because the temperature dependencies of the device are different at different steady state temperatures. It also improper to assess the thermal acceleration of the device by stress tests at elevated temperatures and extrapolate the results to lower temperatures, because the failure mechanisms (Table 2.10) are not uniformly active for all steady state temperatures.

The generalized association of lowered temperature with higher reliability may not be true for all device technologies. Two possible exceptions may exist. First,

the mechanism may not be dependent on steady state temperature, and second, the mechanism may have an inverse dependence on steady state temperature. In either case the steady state temperature will not be a driver for microelectronic reliability.

In cases where temperature can be directly related to parameter drift, premature aging, and even catastrophic failure, the temperature influence on reliability can be inarguable. Although examinations of case histories indicate that temperature's relationship to reliability may be more a case of exposing incompatibilities between operational requirements and design or manufacturing processes. In other words, the product as designed is not suitable for operation in the desired environment without changes. Failures mechanism such as reversion or depolymerization, contact spiking, metallization migration occur at high temperatures encountered during fabrication or assembly are well above normal operating temperatures. In such cases certain questions must be addressed before taking action:

- Will lowering the maximum operating temperature by itself avoid or de-accelerate the experienced failures? If so, how much should it be lowered and how is the conclusion reached?
- Will lowering the magnitude of the temperature cycle or change avoid the experienced failures? If so, how much should it be lowered and how is the conclusion reached?

Thus, for technologies exhibiting an obvious dependence of reliability on temperature, lowering the maximum operating temperature may be one of the measures of for enhanced reliability, however a generalization of the concept for universal application is incorrect.

Burn-in has been routinely used as a screen, with higher reliability attributed to burned-in parts without questioning the objectives, necessity or benefits. It has been used as a customer imposed requirement to supposedly ensure higher reliability. The emphasis has been on empirical analysis, without any analysis as to the real or "root" cause of failure in terms of improper manufacturing parameters or design inconsistencies. The stresses applied in the burn-in process have not been tailored to the dominant stress dependencies of the failure mechanisms in the device technology.

The goal of screening, and burn-in in particular, is to remove defective devices which would fail abnormally early in the field, and to implement corrective actions to avoid the occurrence of defects. Devices with mature design and manufacturing processes should experience few if any such failures. In many cases current material manufacturing and processing have reached such a state of maturity that few failures occur within the specified device lifetime.

The device derating criteria have been critically evaluated. A physics of failure based device derating criteria has been proposed to aid the designer enhance device life by means other than lowering steady state. The Derating approach allows the user to examine the critical stresses in the multichip module package and reduce their value to obtain a desired mission life. The acceptable values of stress are represented as graphs of life versus magnitudes of dominant operating stresses. Such graphs are called derating curves. Derating to achieve desired life involves examining the dominant failure mechanisms. By varying the operating point on the derating curve, different stress combinations which would result in desired life can be identified. The operating point can be the functionally most acceptable combination.

To evaluate the sensitivity of device life towards the temperature and non-temperature stresses, the user can plot the device life versus percentage change from a nominal stress value (Figures 6.1, 6.2). This menu allows the user to identify stress derating thresholds below which lowering stress magnitudes will produce no additional benefit in terms of added life. These thresholds can be identified as values of stresses for which the projected time to failure is well beyond the specified mission life of the module.

Figure 6.1 Derating curve for mission life versus operational parameters for dominant failure mechanisms, at a constant operating temperature of 125°C. This derating plot an be used to derate non-temperature operational stresses for cost-effective designs which are reliable at high temperature.

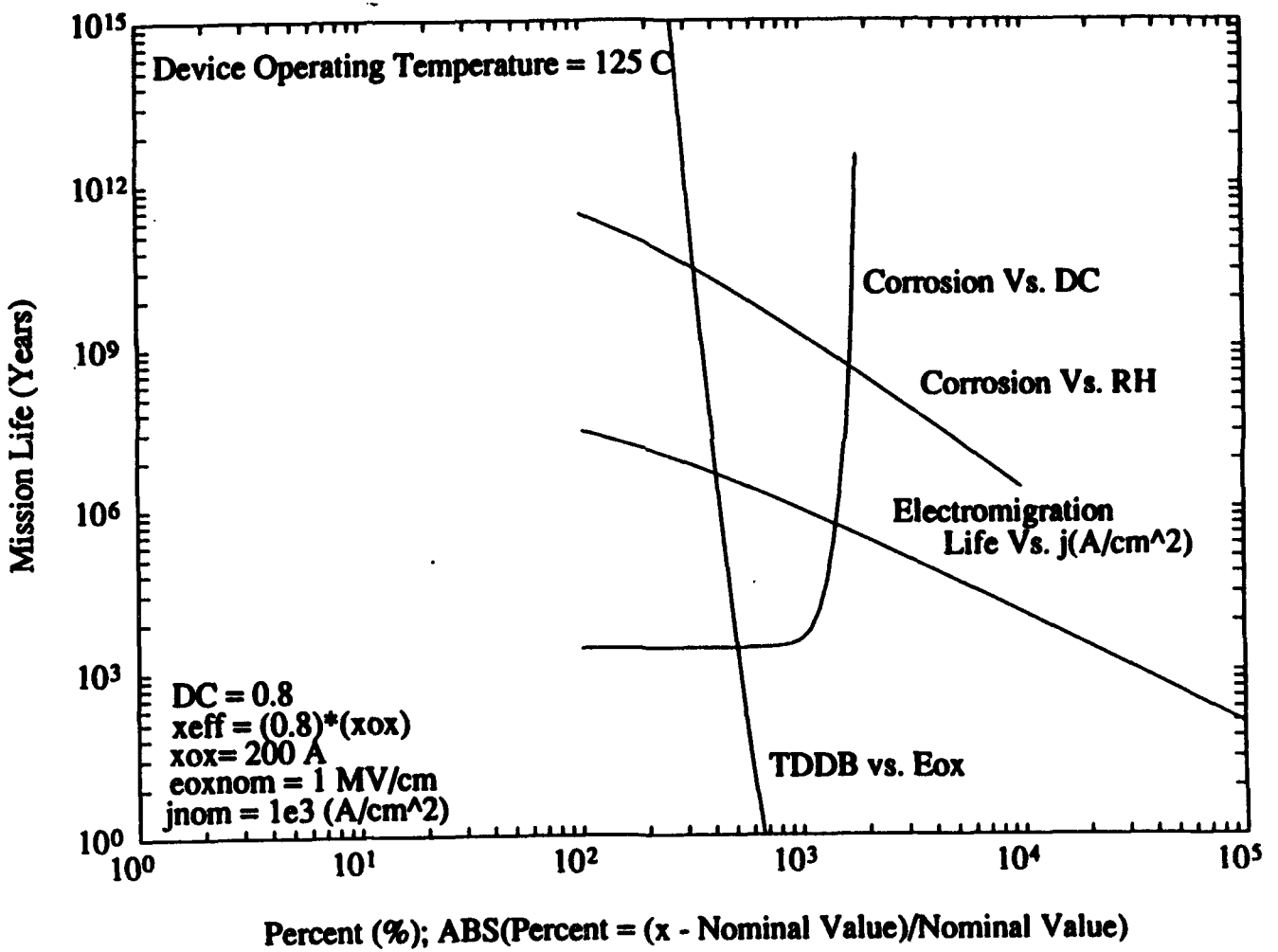
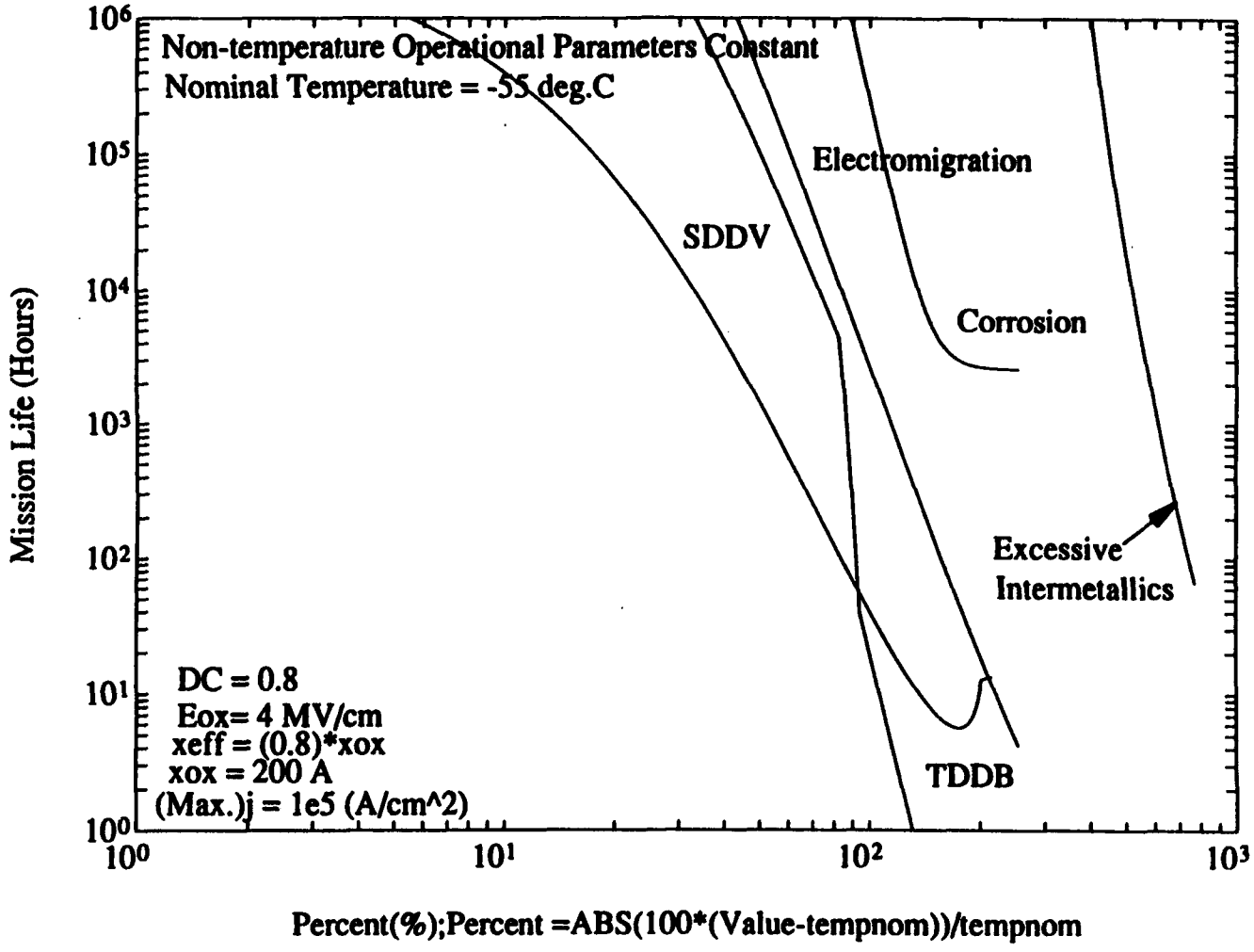


Figure 6.2 Derating curve for mission life versus steady state temperature for dominant failure mechanisms, at a specified values of non-temperature operational stresses. This derating plot an be used to derate non-temperature operational stresses for cost-effective designs which are reliable at high temperature.



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