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DTIC ELECTE DEC 27 1993 S A

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DTIC ELECTE DEC 27 1993 S A

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Research during this period was conducted at Westinghouse Science and Technology Center on deposition and production of microbridges of SNS high T_c superconductor devices. DC and microwave properties were measured at Westinghouse. At Yale University, an electronic test system was contructed to allow flexible testing of devices produced at Westinghouse.

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Final Technical Report for AFOSR 90-0306
(for the period June 1, 1990 - May 31, 1993)

During the final year of this program, graduate student Jim McCambridge conducted research primarily at the Westinghouse Science and Technology Center (STC) in Pittsburgh, PA, though some work was also done at Yale. McCambridge spent a total of three months at the STC in '92-'93.

The work at Westinghouse for the three year contract period focused on the reproducible fabrication of step-edge bilayer (SEB) Josephson junctions made from high critical temperature superconductors (HTS) and compatible materials. The work at Yale concentrated on testing and refinement of the cryostat which had been designed and built for electrical measurements of the junctions.

The initial work at the STC during this period was to implement the SEB process (described in the Annual Technical Report for '91-'92) with normal (non-superconducting) overlayers other than Au. A 50-50 alloy of Au-Ag was chosen as a candidate because of the success of the NIST-Boulder and Biomagnetic Technologies groups at obtaining high critical currents (I_C) and normal state resistances (R_n).[1] Heavily doped (metallic) Lanthanum Strontium Copper Oxide (LSCO) was also tested as a normal metal overlayer because of its compatibility with the high deposition temperature for Yttrium Barium Copper Oxide (YBCO)--nc cool-down period would be necessary between superconductor and normal metal deposition.

We tried several times to fabricate YBCO/LSCO SEB junctions using a variety of step heights (110 nm - 330 nm) on Neodymium Gallate (NGO) substrates. NGO was chosen as a substrate because of its excellent lattice match to YBCO and its lack of crystal twinning Twinning had been a drawback of Lanthanum Aluminate (LAO) substrates. None of the LSCO SEBs displayed Josephson characteristics down to 4.2 K. SEM micrographs were taken of the step edge which indicated the source of the problem: the large lattice mismatch between YBCO and LSCO and the difficulty in growing over the step caused large strains at the interface. This lead to cracking and discontinuous films. No further attempts were made

[1]R. H. Ono et al., "High-Tc SNS Junctions for Multilevel Integrated Circuits," IEEE Trans. Appl. Supercond., 3, p. 2389, 1993; M. S. DiIorio et al., "Low-Noise High-Tc DC SQUIDS at 77 K," ibid., p. 2011.

with LSCO. We switched to an Au-Ag alloy as the normal layer since we had much more experience with Au and Ag. Again, a number of step heights were used (200 nm - 400 nm) with more success. A number of Au-Ag SEB junctions had high I_C and R_n, though some were simply ohmic. High frequency AC (8 - 12 GHz) measurements were made as well. The Au-Ag junctions showed little or no Josephson response. This indicated that the Au-Ag devices were minishorts of the YBCO underlayer (the S layer was continuous across the step, under the Au-Ag bridge) rather than true SNS Josephson junctions. In order to better control and understand junction properties, we decided to study the morphology of the step-edge itself.

A number of step structures were prepared on NGO by ion milling with and without substrate rotation at various angles. Cross-sectional SEM micrographs were then taken of the step-edges. The steps milled with rotation were quite well-defined for milling angles $\theta < 20°$ ($\theta = 0°$ is normal incidence), but became increasingly pathological with increasing θ. Typically, this meant pronounced shoulders at the top of the step and long tails at the bottom. We suspect that redeposition effects are the cause of these problems. Steps milled without rotation were not as sharply defined as the rotated, low θ steps, but they had acceptable shapes. We therefore decided to fabricate YBCO/Au SEB junctions on steps milled without rotation at a variety of angles to see how the step-edge morphology affected YBCO growth across the step and device characteristics.

We deposited 100 nm YBCO/300 nm Au over 120 nm - 200 nm steps in NGO. The step angles were between 0° - 45°. From our electrical measurements and previous SEM work, a consistent, but pessimistic, picture emerged for the step-edge growth of YBCO. For very sharp steps ($\theta < 10°$), the HTS film was electrically discontinuous over the height of the step. However, the SNS devices had very small or no I_C and Josephson junction yield was poor. For broad steps ($\theta >$ 40°), the YBCO film could grow continuously across the step, creating a minishort, not a Josephson junction. Only in the intermediate regime were Josephson junction yield (> 80% at 77 K) and characteristics ($I_C R_n > 100$ μV) acceptable. The YBCO morphology across the step was not clear, however. The inferred device lengths (from electrical measurements) were much shorter than the step heights, indicating that the YBCO may cover some of the step.

Another possible explanation is a damaged metallic or insulating region of YBCO forms on the step itself.

For multijunction applications, rotation during ion milling would be necessary for ease of circuit design, because junctions can then be oriented in arbitrary directions on the substrate. Unfortunately, the intermediate angle regime where the best devices can be made is exactly where ion milling with rotation fails to produce usable steps. We presented these results at the 1992 Applied Superconductivity Conference in Chicago.[2] Future research could explore the problem of obtaining reproducible step topography. We believe these are issues which can be solved with further work.

[2] J. D. McCambridge et al., "Optimizing YBCO Step-Edge S-N-S Junctions for Digital Electronics," presented at the 1992 Applied Superconductivity Conference, Chicago, IL; M. G. Forrester et al., "Development of a Digital Circuit Process Based on Step-Edge YBCO/Au S-N-S Junctions," ibid.