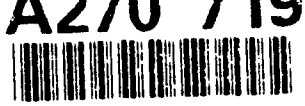

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VLSI DESIGN FOR RELIABILITY-CURRENT DENSITY

University of Illinois at Urbana-Champaign

I.N. Hajj, G. Stamoulis, P. Li, H. Kriplani, and G. Kamath

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APPROVED: Martin J. Walter

MARTIN J. WALTER
Project Engineer

FOR THE COMMANDER: John J. Bart

JOHN J. BART
Chief Scientist, Reliability Sciences
Electromagnetics and Reliability Directorate

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University of Illinois
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Urbana IL 61801

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This effort emphasizes the computation of the average and variance current density waveforms in the metal buses for estimating the MTF for electromigration effects. That effort is composed of two parts: The probabilistic simulation methods and software for computing the statistics of the current waveform at contact points to the buses; and the accurate extraction of the equivalent RC model of the bus for analyzing the bus currents.

In addition, probabilistic methods have been applied to the calculation of the hot electron degradation in digital CMOS circuits, and the problem of estimating the maximum current (as opposed to the average) in the bus for worst case voltage drop analysis.

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VLSI DESIGN FOR RELIABILITY-CURRENT DENSITY

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Abstract

This work summarizes the work accomplished during the period May 17, 1991, through September 19, 1992, on the reliability analysis of VLSI CMOS circuits. The work is a continuation of research on the same subject supported during the previous year by Rome Laboratory. The main emphasis of the work has been the computation of the average and variance current density waveforms in the bus for estimating mean-time-to-failure (MTF) due to electromigration effects. The work involves two subtasks. One is the development of probabilistic simulation methodologies and software for computing the statistics of the current waveforms at contacts to the bus under all possible inputs. The current waveforms at the contact points are then used to compute the statistics of the current density in various sections of the bus. In this regard, we have developed a hierarchical probabilistic simulator that is more accurate and faster than our previous probabilistic simulator. The second subtask is the development of an accurate bus extractor to obtain the RC model of the bus for analyzing the bus currents. In this regard, we have modified our previous bus extractor to make it more robust and eliminate many geometrical restrictions that were previously placed on the layout.

As an evolution of this work, we have also explored the application of the probabilistic simulation approach to hot-carrier effect estimation in the devices within a VLSI design, and the problem of estimation of maximum (worst-case) current waveforms drawn by the circuit at bus contact point for voltage drop estimation in the bus. Our aim is to include devices, lines, and interconnects in assessing physical reliability which would lead to overall improvements in design for reliability.

VLSI DESIGN FOR RELIABILITY-CURRENT DENSITY

Final Report

Contract F30602-91-C-0054

1. Introduction

This research is concerned with the development of computer-aided methodologies and tools for assessing and improving the reliability of chip-level VLSI circuit designs. Many existing computer-aided design systems tend to ignore physical reliability constraints during the design phase, and rely on assessing circuit reliability by accelerated burn-in tests after manufacture. However, with the increase in chip complexity and the decrease in feature size, reliability issues can no longer be ignored during the design process and need to be addressed rigorously throughout the design cycle.

Reliability considerations include both long-term and short-term effects. Long-term effects are related to the physical aging of integrated circuit elements and lines. They include electromigration effects in the lines, and hot-carrier degradation and oxide breakdown in the devices. Short-term effects include voltage-drop and noise in the lines, electrostatic discharge through input protection circuits, system-noise induced latchup, and charge-particle induced soft errors.

In this task, we have concentrated our efforts on two reliability issues; namely, electromigration detection and prevention and voltage-drop reduction in the power and ground busses. Electromigration is a major reliability problem that is caused by the transport of atoms in metal due to electron flow. This problem is becoming increasingly critical, especially with the reduction in feature size and the increase in the number of transistors on a chip. Almost all existing work on electromigration has dealt with characterizing the phenomenon using experiments on test structures. There are no CAD tools available today that deal with the electromigration problem at the chip level. With the number of transistors on a chip now exceeding one million, such

a need is becoming urgent. The traditional worst-case approach to electromigration estimation may fail to give reliable and area efficient designs at reasonable cost. Our approach, which uses statistical techniques allows design for reliability at a more reasonable cost, without sacrificing performance or adding unnecessary metal area.

The second reliability problem we have considered in this task is voltage-drop in power and ground busses which has also been ignored by existing CAD systems. In contrast to the electromigration problem, voltage-drop is a worst-case phenomenon that is caused by current spikes flowing through the power bus due to RC or RLC effects during switching. A drop in the voltage difference across gates to below some threshold could cause the design to malfunction. This problem becomes even more acute if power supply voltage is reduced or when BiCMOS designs are used.

In addition to the above two reliability problems, we have initiated an investigation into the application of the probabilistic simulation approach to the estimation of hot-carrier effects. Hot-carrier effects are long-term cumulative effects, and the probabilistic approach would provide a cost-effective method to predict the expected value of these effects within reasonable time compared to exhaustive or Monte Carlo simulation.

The above reliability issues can be shown to be related to the current flow in the circuit during switching activities. Electromigration is related to the average (as well as the variance) of the current density waveform in a metal line (averaged over all possible inputs). Hot-electron effects are related to the average current flowing through a device, while maximum voltage-drop is related to the maximum current waveform flowing in the bus.

Before presenting our accomplishment during the past year, we give a brief overview of the CAD system that we are developing to implement and test our methodologies and algorithms. Figure 1 shows a block diagram of the CAD system. Given a design layout specified in CIF (Caltech Intermediate Format), which could be specified hierarchically, program iCHARM extracts SPICE-file from it, including interconnect parasitics, and sorts out the CIF subfiles of

the power and ground busses, with bus contacts labeled to match the corresponding node connections in the extracted SPICE file. The extracted SPICE-file has the same hierarchical structure as the original CIF file.

The SPICE file forms the input to the simulators, iPROBE, iPROBE-d, and iMAX (The SPICE file can also be used as the input file to our other simulators to perform timing and fault simulation using input test vector sets; these other simulators are not indicated in the Figure). iPROBE is a probabilistic simulator which computes the average and variance current waveforms at declared contact points. iPROBE-d estimates the average relative damage due to hot-carrier effects within the circuit devices. iMAX computes an upper bound current waveform envelope at contact points. JET is a bus extractor dedicated to extracting the RC models of the bus. The outputs of JET, iMAX and iPROBE form the inputs to a bus analyzer and optimizer that recommends changes to the bus line widths, if necessary, in order to meet both electromigration and voltage-drop constraints.

In the next section, we describe the new probabilistic simulation techniques used in iPROBE; we will also briefly explain the approach used in iPROBE-d. In Section 3 we report on related work on bus model extraction and on the estimation of maximum current waveform drawn by the gates at bus contact points that can be used for maximum voltage drop estimation. The last section contains summary and discussions, and plans for future work.

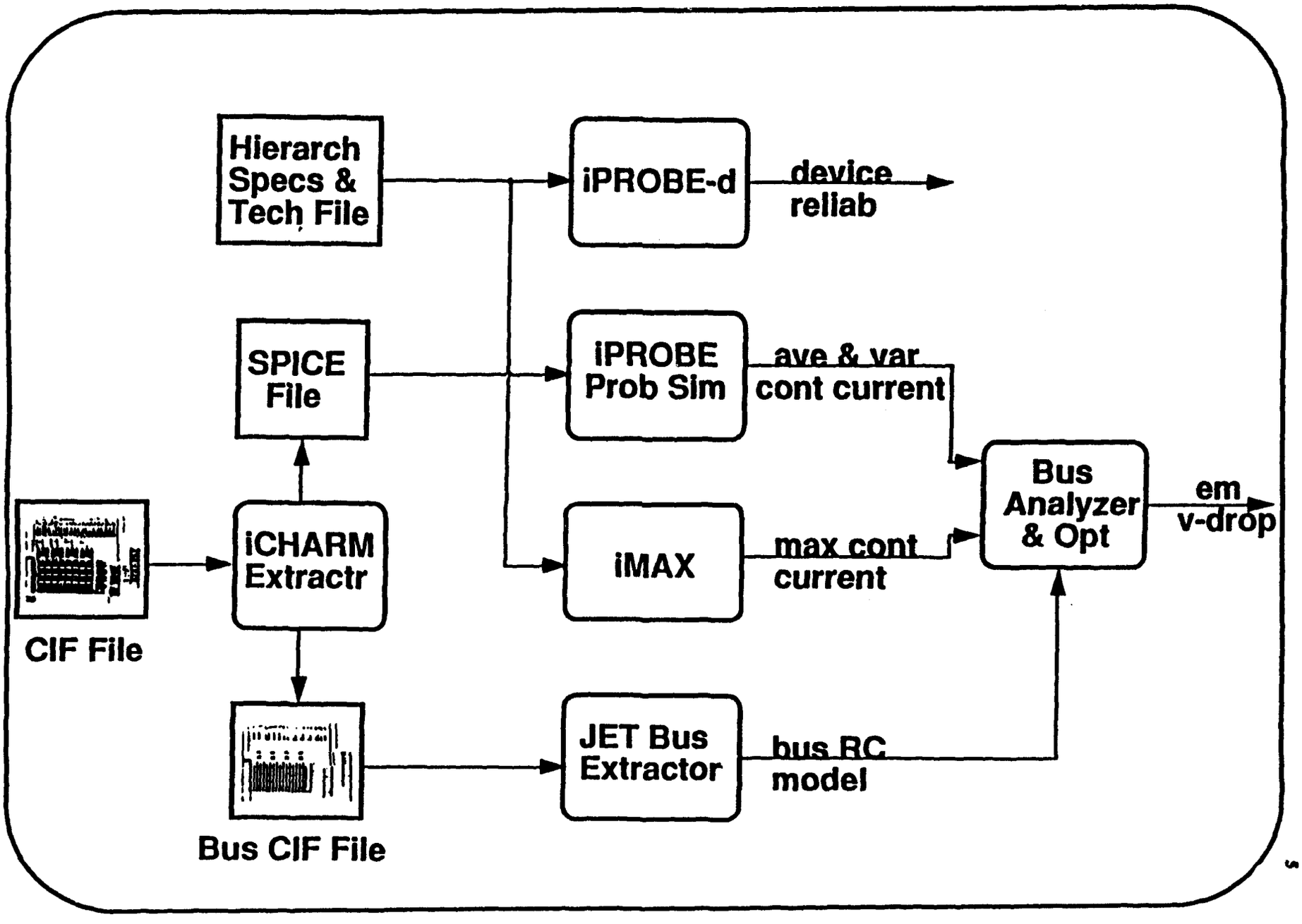

Figure 1. Block diagram of CAD reliability system.

2. New Probabilistic Simulation Techniques

Probabilistic simulation has been shown to be a very cost-effective approach to the computation of voltage and current waveform statistics in CMOS digital circuits compared to exhaustive simulation. This approach is particularly attractive when long-term reliability issues, such as electromigration, hot-carrier effects, and average power, are to be estimated over all possible inputs. CREST [1] was the first program to implement this approach. During the past two years we have been working on improving probabilistic simulation techniques, both in accuracy and in speed. Improvements have been made mainly at the subcircuit level, where the statistics of the current and voltage waveforms and the delays are computed more accurately, as well as at the global level, where signal correlations need to be considered efficiently and accurately. The new algorithms have been implemented in a hierarchical probabilistic simulator, iPROBE, and tested on a number of large benchmark circuits, with the largest one consisting of about 100,000 transistors.

In our annual report last year, we described some aspects of the new algorithms we developed for analyzing individual subcircuits. In this report, we will describe further improvements on subcircuit analysis that we have accomplished since then. We will also describe the accomplishments we made in the simulation of VLSI circuits at the global circuit level and the development of the hierarchical probabilistic simulator.

The improvements that we have done to the original CREST algorithms can be summarized as follows:

(1) At the subcircuit level, the calculation of the equivalent (random variable) conductance of two transistors in series is obtained more accurately, both in terms of the average of the equivalent conductance and its variance. As a result, the graph reduction procedure, which is a basic step in probabilistic simulation, generates a more accurate statistical macromodel, which in turn produces more accurate current waveform statistics and delay information.

(2) The graph elimination at subcircuit switching time during a clock cycle is performed in a different way than in the original algorithm used in CREST. In the original CREST algorithm, all transistors in a subcircuit are assumed to switch at the same time, at the beginning of a clock cycle. As a result, some inaccuracies in the simulation were observed. In our new algorithm, we make the following observations, which produce more accurate results.

Observation 1: The signals arrive at different (n and p) transistor pairs in a subcircuit at different time instances within a clock cycle (this difference could be very small). Even if the signal originates from the same point in the circuit, such as in reconvergent fanout, the differences in the delay along different paths cause the signals to arrive at different times at the reconvergent point.

Observation 2: If the edge (representing a transistor) that switches is in parallel with an edge that is conducting, then the output will not switch and no current will flow through the subcircuit.

Observation 3: It follows from observations 1 and 2 that for the output to switch, one edge must switch, and *all* the conducting paths between the output node and the power node must pass through the edge that has switched, and any path from the output node to the power node that does *not* pass through the switching transistor is not conducting.

Based on the above observations, the calculation of the total equivalent conductance between the output node and the power node at switching time is simplified. The details of calculating the statistics of the equivalent conductance as well as the peak current and the time span of the current waveform are given in Reference [7]. The computation of the equivalent conductance is done for each transistor in a subcircuit during a clock cycle; the total current waveform is then found using superposition. Even when two transistors are specified to be switching at the same time, we assume that there is an arbitrarily small time difference between their switching instances. Transistors in a subcircuit usually switch at close, but different time instances; but in

some cases they switch at widely separate times causing more than one current spike to flow through the subcircuit during a clock cycle.

(3) The above observations also provide a simpler and more accurate approach to the subcircuit delay calculation compared to the original CREST approach. Here we briefly describe the new approach. The deterministic delay model, which applies to both switching from low to high and high to low is given by

$$t_d = ln\ 2\ \frac{C_L}{G}$$

where C_L is the total load capacitance and G the equivalent conductance from the output node to the power (or ground) node. Applying probability theory to the above equation, we get:

$$E[t_{dp}] = ln\ 2 \times C_L \times (\frac{1}{E(G_p)} + \frac{V(G_p)}{(E[G_p])^3})$$

for transition from low to high, and

$$E[t_{dn}] = ln\ 2 \times C_L + (\frac{1}{E(G_n)} + \frac{V(G_n)}{(E[G_n])^3})$$

for transition from high to low. Where $E[t_d]$ is the expected value of the delay; $E(G_p)$,$V(G_p)$ the expected value and variance of the equivalent conductance of the p-part of the CMOS gate; and $E(G_n)$,$V(G_n)$ the expected value and variance of the equivalent conductance of the n-part of the gate. The expected value of the total gate delay is found from the weighted average of the delays from low to high and from high to low:

$$E[t_d] = \frac{E[t_{dn}] \times P_{out.hl} + E[t_{dp}] \times P_{out.lh}}{P_{out.hl} + P_{out.lh}}$$

where $P_{out.hl}$ and $P_{out.lh}$ are the probabilities of the output switching from high to low and from low to high, respectively.

Example 1: This example illustrates the accuracy of calculating the expected value of a gate delay compared to CREST and to exhaustive SPICE simulation. Figure 2(b) shows the graph representation of the n-part of the CMOS gate shown in Fig. 2(a). All inputs are in steady state, except input A to which the probabilistic waveform shown in Fig. 2(c) is applied. There are two numbers associated with each edge of the graph. The top one is the probability that the gate node of the corresponding transistor is *high* and the bottom one represents its *on* conductance in $m\Omega$. The load capacitance used is 10pF.

The average delay, calculated by the new method, is found to be 3.64ns compared to 3.60ns by exhaustive SPICE simulation, while the method used in CREST yields 0.66ns, which shows that our result is much closer to SPICE.

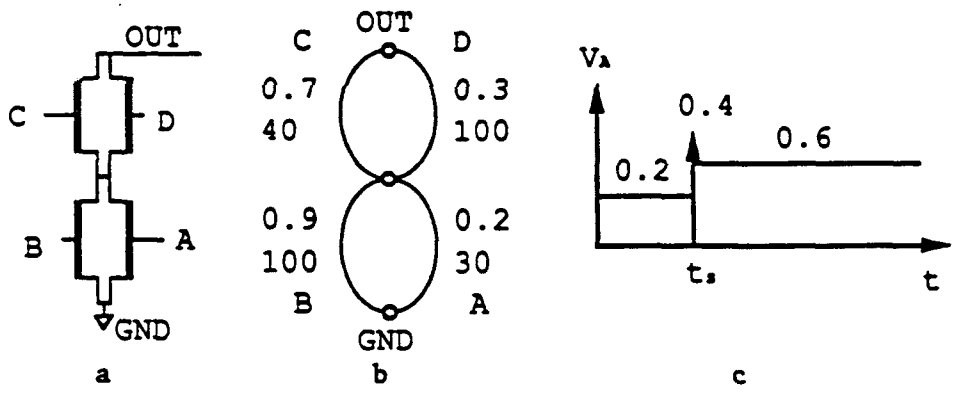

Figure 2. (a) A CMOS gate; (b) Graph of the n-part; (c) Input waveform.

Example 2: This example illustrates the accuracy of calculating the expected value and variance current waveforms using the new method. Figure 3(a) is a two-input NAND gate, with two inputs A and B. Figures 3(b-d) show the expected value of the current waveforms using the new approach for $t_a \cong t_b$ (Fig. 3(b)), $t_b - t_a = 0.4$ns (Fig. 3(c)) and $t_b - t_a = 4$ns (Fig. 3(d)), compared each time with CREST and exhaustive SPICE runs. Note that our results are very close to exhaustive SPICE, while CREST gives the same waveform in all three cases since all transistors

are assumed to switch at the same time. The variance waveforms are of comparable accuracy.

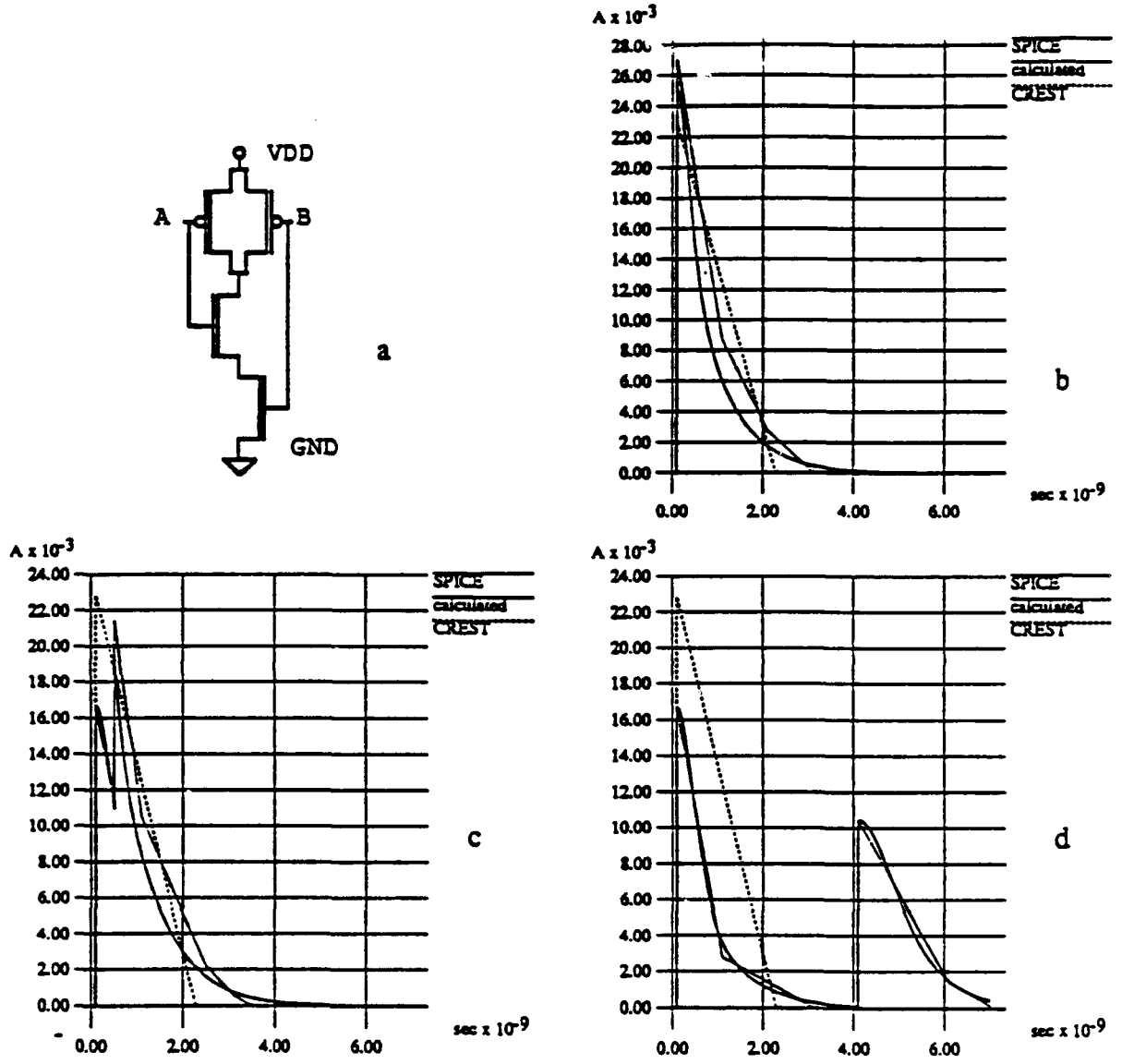

Figure 3. Simulation of transitions within a single interval.

The assumption that each (n and p) transistor pair in a gate switches at its own transition time tend to generate a number of events at the gate output equal to the number of transistor pairs in the gate. In practice, however, the number of gate output events is less, depending on the expected arrival times of the signals to a gate. For example, in Fig. 3(b) and (c), the two input events generated one merged event at the gate output, while in Fig. 3(c), two distinct

events are generated. These additional events are glitches which are known to add to power consumption and current flow in the bus and in the devices that steady-state analysis does not capture. We have devised a merging algorithm based on the arrival time of signals at gate inputs and its delay in order to generate the true output events and at the same time capture any glitches that might occur.

The new algorithms have been implemented in a general purpose hierarchical computer program, iPROBE, and tested on a number of benchmark circuits. It has been observed that simulation times without merging of output events tend to be high for some of the ISCAS85 benchmark circuits. The merging algorithm reduces computation time significantly as shown in Table I.

Table I. Simulation Results.

	Primary inputs	Calls to simulation routine	Time with no merging†	Time with merging†	Memory usage (Kbytes)
c432	37	1543630	388.1	1.5	456
c880	61	183530	31.2	2.1	680
c1355	42	43865760	7856.2	4.1	804
c1908	34	5398570	983.4	7.2	1128
c2670	234	6358748	978.0	7.6	1512
c3540	51	371013994	59201.9	20.9	2316
c5315	179	24300542	4126.5	19.4	2676
c6288	33	-	>24h	95.6	3796
c7552	208	10877190	1809.9	32.2	3620
s38584	12	-	428.8‡	454.1	12352

† In CPU seconds on an HP 9000/730

‡ preprocessing only, s38584 contains about 100,000 transistors

Application of the Probabilistic Approach to Hot-Carrier Effect Estimation

In addition to the computation of contact current statistics for electromigration estimation, as described above, we have applied the probabilistic approach to the problem of hot-carrier effect estimation in devices within large circuit designs. Hot-carrier effects (HCE) in MOS transistors are also long-term reliability issues that occur within devices in the circuit over time and are cumulative in nature. Existing techniques use circuit or timing simulation to estimate HCE and try to predict the age of the design by incorporating device degradation over time As a result, all existing HCE simulators (especially those linked to SPICE-type circuit simulators) are too slow for large circuits. Even if very fast simulation techniques were to be used, user-specified deterministic input waveforms are needed, and hence the results can only represent a small sample of operating conditions. Our approach differs from existing methods. We use probabilistic simulation techniques to estimate the expected damage in each device under all possible operating conditions. We then find those transistors that are most susceptible to HCE degradation. The aim is to modify the design to reduce such degradation, rather than predict the age of the design. The probabilistic simulation approach provides a fast and cost-effective method to estimate HCE without resorting to exhaustive or to Monte Carlo techniques.

In the course of this study, we have found a number of circuit characteristics that contribute to HCE. We summarize these characteristics in the following:

(1) HCE occur mostly when a transistor is in saturation. The duration of a transistor in the saturation region depends on its input slew rate and the loading capacitance. HCE is related to the substrate current, I_{sub}; slower slew rate causes wider I_{sub} time span and hence more degradation; higher loading capacitance results in longer time spent in saturation during switching.

(2) HCE is related to the frequency of transistor switching only when it causes the output to switch. It occurs when current flows through the transistor during transition, which in turn occurs when a transistor's switching from OFF to ON causes the output to switch. Based

on the observations mentioned in the previous section, a transistor draws current during switching when all paths from the output node to the power node that do not include the switching transistor are OFF. In our probabilistic approach, the probability that a transistor's switching causes the output to switch is calculated. The expected value of HCE then depends on this probability, as well as on the time span the transistor stays in saturation.

(3) Transistors connected directly to the output node stay much longer in saturation during switching than other transistors, and thus suffer most from HCE degradation. To save on computation, we therefore concentrate on estimating HCE in the transistors that are connected to the gate output nodes, even though the simulation approach can be used to estimate HCE in any transistor within a subcircuit.

Since the time a transistor stays in saturation is directly related to HCE, and since this time duration is determined by the input slew rate as well as the gate output loading, we have extended our probabilistic simulation technique to include gate input voltage waveform slew rate to compute the average time a transistor stays in saturation, as well as the expected output slew rate, in addition to the expected delay value. The gate output signal merging algorithm, with slew rates taken into account, has also been modified. More detailed description of the algorithm can be found in Reference [6].

The HCE estimation algorithms have been implemented in another version of iPROBE that is dedicated to HCE. The program is called iPROBE-d (d for device). iPROBE-d has been used to simulate several benchmark circuits. Although the program currently can only simulate series/parallel CMOS circuits, it is being extended to handle general nMOS and CMOS circuits.

Example 3: This example illustrates why simulating a given design using one or a few "typical" input signals could give misleading results in estimating HCE.

Figure 4 shows a CMOS circuit with two NAND and one NOR gates. The statistical descriptions of the four input nodes are also shown in the Figure. Table II illustrates the

degradation of the six nMOS transistors using iPROBE-d, SPICE exhaustive simulation, and SPICE one run, respectively. The circuit is simulated for a time period T = 20ns, then we assume the input events repeat periodically and extrapolate the damage to three months. Since for each input node, there are four possible waveforms (staying high, staying low, switching from low to high, from high to low), there are $4^4 = 256$ possible input combinations. Therefore, for the SPICE exhaustive simulation, 256 runs are needed. On the other hand, only one run is necessary when iPROBE-d is employed. The input voltage waveforms of the third row in the Table II, SPICE *one run*, are $A = B = D = V_{DD}$ and C = *a periodical square wave*. From the result, iPROBE-d and SPICE *exhaustive simulation* show the same tendency, while running SPICE with one particular input waveform points to the wrong critical transistor. We have also compared the waveform obtained from iPROBE-d and SPICE *exhaustive simulation*. The slew rate and propagation delay from iPROBE-d are within 5 percent error compared to the average value from SPICE *exhaustive simulation* on all the output nodes.

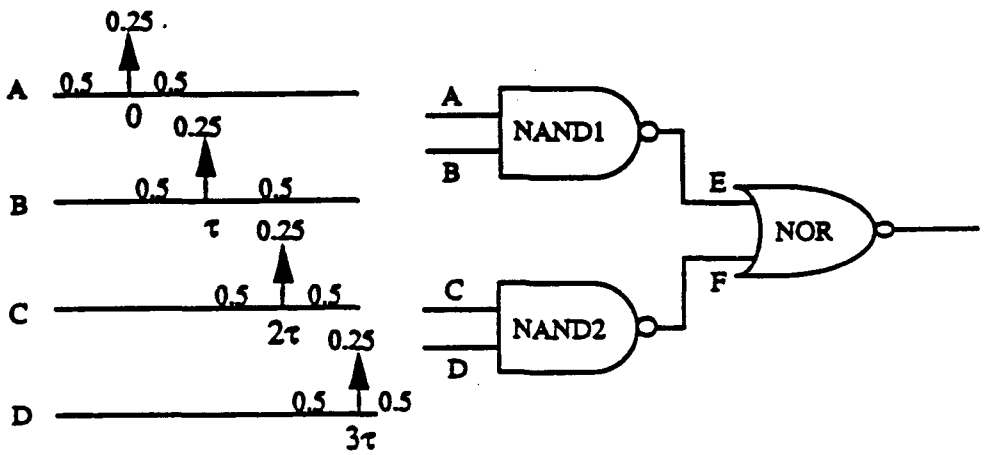

Figure 4. A test CMOS combinational circuit and the input statistical descriptions. t_{HL} and t_{LH} are both 0.2ns for each input event. Simulation period T = 20ns.

	NAND1 top	NAND1 bottom	NAND2 top	NAND2 bottom	NOR left	NOR right
SPICE exhaustive						
$\tau = 5ns$	1.178	0.012	1.177	0.022	1.963	1.898
$\tau = 2ns$	1.178	0.012	1.177	0.399	1.741	1.197
$\tau = 1ns$	1.178	0.011	1.177	0.752	1.740	0.876
$\tau = 0.3ns$	1.178	0.012	1.178	0.015	1.740	0.868
iProbe-d						
$\tau = 5ns$	1.094	0	1.094	0	2.186	2.173
$\tau = 2ns$	1.087	0	1.094	0	1.873	1.554
$\tau = 1ns$	1.094	0	1.094	0	1.795	1.544
$\tau = 0.3ns$	1.094	0	1.094	0	1.795	1.544
SPICE one run *	0	0	2.442	0	0	5.654

Table II. The damage N_{it}(x 10^{11} C/cm^2) of all nMOS transistors in the circuit shown in Fig. 9.
*A = B = D = high (V_{DD}); C = *a periodical square wave.*

Some ISCAS85 benchmark circuits have also been analyzed. These benchmark circuits have been converted to SPICE input file with complementary CMOS transistor circuit implementation of each gate. Table III shows a computation time on a SPARC station2, as well the damage situation after a simulated 3 months continuous operation. Here we assign one event to each primary input node, with 20ns as the simulation period. The results show that iPROBE-d can handle large circuits with reasonable computation time.

ISCAS85 benchmark circuit	number of nMOS transistors in each damage level (Normalized Nit)							Computation time (sec)
	<0.1	0.1 – 1.0	1.0 – 2.0	2.0 – 3.0	3.0 – 4.0	4.0 – 5.0	>5.0	
C432	196	16	52	58	42	16	32	23.87
C499	336	40	48	80	16	56	306	20.75
C880	256	112	103	57	117	115	141	25.14
C1355	512	72	208	16	176	64	106	46.03
C2670	743	95	106	190	440	401	707	77.43

Table III. The computation time of iPROBE-d on several benchmark circuits, and predicted average damage after 3 months continuous operation. The simulation is done on a SUN4 SPARC station2.

3. Related Work

3.1 Introduction

In Section 2, we presented our improved probabilistic simulation approach to the estimation of average, as well as variance, current waveforms drawn by CMOS gates at contact points to the power and ground busses. The purpose of computing these current waveforms is to use them to calculate the average current density in the busses for electromigration estimation. It is interesting to note that the average current waveforms drawn by the gates can also be used to estimate the average power consumed by each gate as well as the total average power.

In order to analyze the bus for electromigration estimation, a reasonably accurate RC model of the bus is needed. For this purpose, a project on RC bus model extraction has been carried out in parallel with the project on current density estimation. The accomplishments of this extraction project are described below. This section also includes a summary of the work we did on another reliability issue related to the bus design; namely, estimation of *maximum* current waveform drawn by the gates at the contact points for estimating *maximum* voltage drop in the bus. Since one of our goals in this research is to generate reliable bus design, we feel that voltage-drop should also be included, in addition to electromigration measures, in optimizing the bus layout. The work on maximum current estimation and voltage drop has been supported by Texas Instruments, Inc., and the Semiconductor Research Corporation.

3.2 Extraction of the Metal Bus Model

Originally we developed program JET to extract the RC model of power and ground busses. However, JET assumed that the bus layout can be decomposed into an interconnection of primitive shapes, such as straight lines, L, T, and four way junctions, with certain restrictions on aspect ratios. When this decomposition was not feasible, the program stopped, unless the user modified the original layout to make the decomposition possible, thus changing the original

problem. In this work we originally planned to modify JET to extract the models of any possible shape obtained from layout decomposition without any modification. That is, we still follow the approach of decomposing the layout into primitive shapes and use precomputed library of RC models of most commonly encountered shapes. However, whenever a shape is encountered that does not fit the primitives in the precomputed library, its RC model will be computed on the fly, rather than modify the geometry to force the partition to match one of the stored primitives. We use the *boundary element method* (BEM), which has been found to be fast and reliable, in computing the resistance parameters of bus regions and shapes. The advantages of the BEM approach is that only the boundary is subdivided, not the interior, and the generation of the grid points on the boundary is much simpler that the generation of triangular meshes in the interior, as is done in the finite element method (FEM). In all the examples we tried, we found that the BEM is three to seven times faster than the FEM.

During the course of this work we decided that it was not easy to modify JET. Hence, a new program was developed using some of the routines found in JET. Currently the program is able to extract the RC model of the layout test circuit sent to us by designers at Rome Laboratory, without having to modify the layout to fit the set of precomputed primitives, as the original JET required. We are also testing the new program on designs generated by students in a VLSI design course at the University of Illinois. The details of the approach with examples will be published in an M.S. thesis report and made available to Rome Laboratory.

3.3 Maximum Current Estimation

Excessive power supply and ground instantaneous currents in integrated circuits can severely affect circuit reliability and performance. Some of the problems arising from excessive current flow are excessive voltage drop on power/ground lines which can lead to soft errors. and large instantaneous power dissipation which causes overheating and ultimately leads to performance degradation. Maximum current estimates are, therefore, needed in the supply lines in

order to determine the severity of these problems, and to modify the design to reduce their effects, if possible. Maximum currents, however, depend on specific input patterns that are applied to the circuit. Previous work in this area estimated maximum current as the maximum dc current drawn by each gate under worst-case conditions. Such an approach is easy to apply, but unfortunately is overly pessimistic. The actual current drawn by a gate is not dc but rather a waveform, and the maximum current points drawn by different gates do not occur at the same time instances. More recent work focuses on using search techniques to attempt to locate the worst-case current by searching the input space to locate the input patterns that produce worst-case current waveforms. Unfortunately, the input space is in most cases very huge, and purely search-based algorithms can take an exponential amount of time.

In our work we have developed a pattern-independent, linear-time algorithm that estimates an upper bound for the *Maximum Envelope Current* waveform. The maximum envelope current waveform is a point-wise maximum on all possible current waveforms that a circuit is expected to draw. The delays in the circuit are taken into consideration in computing these upper bound waveforms.

The algorithm currently operates at the gate-level description of the circuit. It starts by assuming that nothing is known about the specific excitations at the primary inputs, except that they may transition at time zero. We call this an *uncertainty* about these input signals. The basic idea of the algorithm is to propagate the "uncertainty" present at the inputs inside the circuit so as to determine the set of all possible excitations and their associated timing at the output of every logic gate. From this information, the worst-case current waveforms are computed. In general, however, signals at internal nodes of a circuit are *correlated*, which limits the number of possible transitions occurring at the output of the gates. Two types of correlations, namely *spatial* (among various gates) and *temporal* (in time domain) are identified. We have developed novel *partial input enumeration* techniques to resolve signal correlations and significantly improve the upper current waveform bounds. The partial input enumeration algorithm starts by

"intelligently" selecting a enumerating a few primary inputs. The set of inputs selected for enumeration has a direct influence on the quality as well as the cost of the solution obtained. We have developed a *best first search* (BFS) that is found to be very effective in selecting and enumerating the inputs. Because of the best first strategy, there is a gradual reduction in the upper bound waveform, and the search need not be carried out too deep into the search space to obtain good results.

The technique has been implemented in program iMAX and tested on a large number benchmark circuits. A typical combinational circuit containing more than 3500 gates takes about 46 seconds to simulate. In order to check the accuracy of the results, we compared our results with exhaustive simulation on circuits with a small number of inputs. In all cases our upper bound was higher, but close, to the actual envelope waveform. For circuits with moderate to large number of inputs, exhaustive simulation is prohibitively expensive. In this case we use a simulated annealing algorithm to generate a lower bound current envelope. In all cases our upper bound was larger than the lower bound obtained from the simulated annealing algorithm. The true bound should be somewhere between the two bounding waveforms. The details of the algorithms with examples are reported in Reference [4].

4. Summary

In this research we have been working on a number of projects related to the physical reliability assessment of VLSI circuits. These include the development of methodologies and software for estimating the statistics of current waveforms drawn by the circuit at contact points in the bus for electromigration estimation within the bus. The method followed is the probabilistic simulation approach. In this respect, we have developed new algorithms that improve on the accuracy of the original ones. We have also implemented the new algorithms in a hierarchical probabilistic simulator. We have also applied the probabilistic simulation approach to the estimation of hot-carrier effects within devices to pinpoint which devices, on the average, would experience most degradation in a given design over time under all possible operating conditions. So far the new probabilistic simulator handles series parallel CMOS structures. We are currently extending the method to include circuits with pass transistors. We are also in the process of developing new algorithms to handle signal correlations due to reconvergence fanout in a more accurate way.

We have also developed a new bus extractor that is more robust than our original bus extractor JET, in the sense that it is not restricted by the requirement that the bus layout be decomposable into precomputed primitive structures. The new approach decomposed the layout into primitives and uses precomputed models on those shapes that fit the ones in the precomputed library, and computes the models of the ones that do not fit on the fly.

In related work we have also developed a new linear-time approach for estimating upper bound current waveforms drawn by gates in CMOS designs for estimating worst-case voltage drop in the bus. We are currently applying partial enumeration techniques to improve the accuracy of the upper bound waveforms without drastically increasing the computational speed.

Our plans for the coming year calls for continued improvements and extensions on our simulation algorithms. In particular, the probabilistic analysis of circuits with pass transistors need to be done. In addition, the method of handling signal correlations due to reconvergent

fanout and feedback need to be studied further and tested for accuracy. At the same time, we plan to do work on design concepts and techniques for reliability, both at the bus level and at the transistor circuit level. Finally, it is interesting to note that the current waveforms computed at the contact points can also be used to estimate the power consumption of each gate as well as the total power. Thus, we can include the estimation of average and maximum power as part of the objectives of this work.

Publications

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[6] P. C. Li, G. I. Stamoulis, and I. N. Hajj, "A Probabilistic Timing Approach to Hot-Carrier Effect Estimation," *International Conference on Computer-Aided Design*, Santa Clara, Ca, November 1992.

[7] G. I. Stamoulis and I. N. Hajj, "Improved Techniques for Probabilistic Simulation Including Signal Correlation Effects," *30th ACM/IEEE Design Automation Conference*, Dallas, TX, June 1993.

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