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MONDAY, MARCH 15, 1993

GRAND BALLROOM EAST

8:30 am 10:00 am
PMA, PHOTONIC ATM/PACKET SWITCHING
Akira Himeno, *NTT, Japan, Presider*

8:30 am (Invited)
PMA1 Optically processed self-routing for 1- and 2-D photonic switching architectures, Paul R. Prucnal, *Princeton Univ.* The architecture of a 2 × 2 photonic packet switching node using optically processed fixed-directory routing, contention resolution (using deflection routing), and synchronization is presented. **(p. 2)**

9:00 am
PMA2 Photonic ATM cross-connect node-based on cell aggregation and compression, B. Bostica, P. Cinato, M. Calzavara, P. Gambini, M. Puleo, E. Vezzoni, *CSELT, Italy.* A photonic ATM cross-connect is presented, where cell aggregation and compresion are adopted to achieve a high throughput and high performance node. Experimental results on specific subsystems are presented. **(p. 7)**

9:20 am
PMA3 Photonic 2 × 2 packet switch with input buffers, Jonathan Spring, Rodney S. Tucker, *Univ. Melbourne, Australia.* We demonstrate a self-routing 2 × 2 photonic packet switch with two fiber-loop input buffers that provide output contention resolution. The switch operates with asynchronous traffic. **(p. 11)**

9:40 am
PMA4 Variable optical delay line for frame synchronizer in photonic ATM switching system, Takeshi Ozeki, Yukio Shimizu, *Sophia Univ., Japan;* Manish Sharma, Hiroyuki Ibe, *Toshiba Corp., Japan.* A variable optical delay line for frame synchronizer in photonic ATM switching systems is analyzed, and its operation was confirmed experimentally for the first time. **(p. 15)**

10:00 am–10:30 am COFFEE BREAK

GRAND BALLROOM EAST

10:30 am–12:20 pm
PMB, SEMICONDUCTOR MODULATORS AND SWITCHES
Marko Erman, *Alcatel Alsthom Recherche, France, Presider*

10:30 am (Invited)
PMB1 Advances in semiconductor waveguide switches, Hans Melchior, *ETH-Honggerberg, Switzerland.* Abstract not available at press time. **(p. 20)**

11:00 am
PMB2 Polarization independent optical modulation with tensile-strained GaAs-InAlAs QWs grown on GaAs substrate, Yuen-Chuen Chan, Kunio Tada, *Univ. Tokyo, Japan.* Polarization independent optical modulation with tensile-strained GaAs-InAlAs QWs grown on a relaxed InAlAs grid layer is demonstrated by *theoretical simulations and waveguide absoprtion measurements.* **(p. 21)**

11:20 am
PMB3 Lossless and low crosstalk InP based 2 × 2 optical switch with integrated optical amplifier, Toshio Kimhara, Mari Ogawa, Hiroaki Inoue, Shinji Nishimura, Koji Ishida, *Hitachi, Ltd., Japan.* A 2 × 2 carrier-injection type optical switch with traveling-wave amplifiers is presented. Fiber to fiber insertion loss of 0 dB and low crosstalk (40 dB on/off ratio) are demonstrated. **(p. 25)**

MONDAY, MARCH 15, 1993—*Continued*

11:40 am
PMB4 Monolithic integration of quantum well optical waveguides with heterojunction bipolar electronics for wavelength switching, J. E. Zucker, Yi Chen, M. D. Divino, S. Chandrashekar, C. H. Joyner, A. G. Dentai, C. A. Burrus, *AT&T Bell Laboratories.* We report integration of electronic amplifiers with quantum well waveguide photodetectors and intensity modulators in InGaAs/InP and demonstrate the circuit for wavelength conversion near 1.5 μm. **(p. 29)**

12:00 pm
PMB5 Functional photonic switching device by vertical and direct integration of six heterojunction phototransistors and two laser diodes, Susumu Noda, Kimitaka Shibata, Vahid Ahamady, Akio Sasaki, *Kyoto Univ., Japan.* Photonic switching device composed of six heterojunction phototransistors and two laser diodes is developed. The device exhibits an optically controlled multilevel latch and erase functions and a multilevel flip-flop function. **(p. 33)**

12:20 pm–1:30 pm LUNCH BREAK

GRAND BALLROOM EAST

1:30 pm–3:00 pm
PMC, SMART PIXELS
Gareth Parry, *University College London, U.K., Presider*

1:30 pm (Invited)
PMC1 Advances in SEED-based free-space switching systems, Anthony L. Lentine, *AT&T Bell Laboratories.* Advancements in architectures, network control strategy, optical and mechanical system design, laser source design, *SEED array design* that have led to advances in optical switching system demonstrations are discussed **(p. 38).**

2:00 pm
PMC2 Single-mesa optical memory and logic pixels for highly parallel arrays, Xilin An, K. M. Keib, M. J. Hafich, F. R. Beyette, Jr., S. A. Feld, R. Y. Robinson, C. W. Wilmsen, *Colorado State Univ.* The design concept and experimental demonstration for a new family of optically activated logic and memory pixels is presented, along with some discussions for array applications. **(p. 42)**

2:20 pm
PMC3 GaAs/AlGaAs FET-SEED receiver transmitters, T. K. Woodward, A. L. Lentine, L. M. F. Chirovsky, M. W. Focht, J. M. Freund, G. D. Guth, R. E. Leibenguth, L. E. Smith, L. A. D'Asaro, E. J. Laskowski, S. S. Pei, *AT&T Bell Laboratories.* We discuss operating characteristics of FET-SEED receiver/transmitter pairs. **(p. 46)**

2:40 pm
PMC4 Monolithic integration of GaAs/AlGaAs MQW modulators and silicon metal-oxide-semiconductor transistors, K. W. Goossen, J. A. Walker, J. E. Cunningham, W. Y Jan, D. A. B. Miller, *AT&T Bell Laboratories;* S. K. Tewksbury, L. A. Hornak, *Univ. West Virginia.* We demonstrate coexisting operation of a GaAs/AlGaAs MQW modulator and a silicon metal-oxide-semiconductor transistor fabricated on the same chip, for applications in optical interconnects. **(p. 50)**

3:00 pm–3:30 pm COFFEE BREAK

MONDAY, MARCH 15, 1993—*Continued*

GRAND BALLROOM EAST

3:30 pm–5:20 pm
PMD, SPACE SWITCHING
Lars H. Thylèn, *Royal Institute of Technology, Sweden, Presider*

3:30 pm (Invited)
PMD1 High-capacity photonic space-division switching system, T. Sawano, K. Matsuda, S. Suzuki, M. Fujiwara, *NEC Corp.* High-capacity (up to 128-line) photonic space-division switching system prototype development is discussed. **(p. 56)**

4:00 pm
PMD2 Optical crossbar switch with semiconductor optical amplifiers, L. R. McAdams, A. M. Gerrish, R. F. Kalman, J. W. Goodman, *Optivision, Inc.* An 8 × 8 optical switch based on the matrix–vector–multiplier architecture is described. The switch is lossless and has a BER of 10^{-12} at 1.1 Gbit/s. **(p. 60)**

4:20 pm
PMD3 Ti:LiNbO$_3$ photonic switch modules for large, strictly nonblocking architectures, Edmond J. Murphy, Gaylord W. Richards, Timothy O. Murphy, M. T. Fatehi, Shalom S. Bergstein, *AT&T Bell Laboratories.* We report the design, fabrication, packaging, and testing of high-performance lithium niobate switch modules for a robust, guided wave optical switching system. **(p. 64)**

4:40 pm
PMD4 Acousto-optic crossbar photonic switch, Robert McLeod, Robert Weverka, Kuang Wu, Kelvin Wagner, Alan Mickelson, *Univ. Colorado at Boulder;* Richard Roth, *Optivideo Corp.* We have designed an optical crossbar which utilizes a single *anti-tangential, bulk acousto-optic device. The theoretical,* numerical, and experimental operation of the switch are presented. **(p. 68)**

5:00 pm
PMD5 Paper withdrawn.

GRAND BALLROOM EAST

5:30 pm
PPDP, POSTDEADLINE SESSION
Rod Alferness, *AT&T Bell Laboratories, Presider*

TUESDAY, MARCH 16, 1993

GRAND BALLROOM EAST

8:30 am–10:00 am
PTuA, OPTICAL INTERCONNECTS
Thomas J. Cloonan, *AT&T Bell Laboratories, Presider*

8:30 am (Invited)
PTuA1 Optical fiber interconnection links for high-speed switching and computer systems, Takakiyo Nakagami, *Fujitsu Laboratories Ltd., Japan.* Development of optical fiber links for high-speed switching systems and computers is discussed, focusing on parallel links and introducing recent developments in Japan. **(p. 74)**

9:00 am
PTuA2 Low-responsivity GaAs/AlAs asymmetric Fabry-Perot modulators, T. K. Woodward, B. Tell, W. H. Knox, J. B. Stark, M. T. Asom, *AT&T Bell Laboratories.* We find that proton-implanted *p* AlAs/GaAs asymmetric Fabry-Perot MQW modulators exhibit suppressed responsivity while maintaining good modulation performance. **(p. 77)**

9:20 am
PTuA3 High-contrast modulation of asymmetric Fabry-Perot modulators at 20 GHz, C. C. Barron, B. J. Thibeault, C. J. Mahon, L. A. Coldren, *UC–Santa Barbara.* Asymmetric Fabry-Perot modulators (AFPMs) could serve as elements of smart switching arrays for high-speed photonic switching applications. Here we demonstrate high-contrast 20-GHz modulation of AFPMs. **(p. 80)**

9:40 am
PTuA4 Complexity analysis of optically implemented shuffle equivalent interconnection topologies based on computer-generated binary phase gratings, Thomas J. Cloonan, Gaylord W. Richards, Rick L. Morrison, Frederick B. McCormick, Jose M. Sasian, Anthony L. Lentine, Steve J. Hinterlong, H. Scott Hinton, *AT&T Bell Laboratories.* Novel implementations of nodes and space-invariant holographic interconnections are described. Their effect on laser and optical component requirements within photonic EGS networks is examined. **(p. 84)**

10:00 am–10:30 am COFFEE BREAK

GRAND BALLROOM EAST

10:30 am–12:20 pm
PTuB, OPTICAL FDM SWITCHING
Ivan P. Kaminow, *AT&T Bell Laboratories, Presider*

10:30 am (Invited)
PTuB1 Present and future of FDM photonic switching, Tadahiko Yasui, Aritomo Uemura, *Mitsubishi Electric Corporation, Japan.* Present status of photonic FDM switching systems and devices is mentioned. A proposal of a novel FDM photonic switching system follows and problems inherent in the system are considered. **(p. 90)**

11:00 am
PTuB2 Signal transmission characteristics of a photonic FDM multichannel selector, Keishi Habara, Koji Sasayama, *NTT Communication Switching Laboratories, Japan;* Masayuki Okuno, *NTT Opto-Electronics Laboratories, Japan.* This paper describes a photonic multifrequency channel selector using a coherent optical transversal filter. Arbitrary channel selection and signal transmission characteristics are confirmed. **(p. 95)**

11:20 am
PTuB3 Dilated acousto-optic switches for low crosstalk wavelength routing in WDM systems, D. A. Smith, A. d'Alessandro, J. E. Baran, *Bellcore.* We demonstrate that dilated acousto-optic switches, made by suitable cascades of multiwavelength polarization-independent filters, exhibit drastically reduced interchannel crosstalk, with leakage dimished to second order. **(p. 99)**

11:40 am
PTuB4 Intelligent channel selector for wavelength-division and time-division hybrid multiplexed network, Naoki Shimosaka, Takahiro Shiozawa, *NEC Corp., Japan.* Performances of arbitrary channel selector designed for hybrid multiplexed network using digital signal processor for fast and intelligent control operation are confirmed experimentally. **(p. 103)**

12:00 pm
PTuB5 Fast LD wavelength switching with rapid stabilizing control for WDM network, Takahiro Shiozawa, Naoki Shimosaka, Masahiko Fujiwara, Tatsuya Shiragaki, *NEC Corp., Japan.* A novel scheme is proposed for fast LD wavelength switching with rapid stabilizing. Feasibility is confirmed by experiments. Obtained characteristics are suited for 600-Mb/s cell speed WDM network. **(p. 107)**

12:20 pm–1:30 pm LUNCH BREAK

OPTICAL COMPUTING/ PHOTONICS IN SWITCHING/ SPATIAL LIGHT MODULATORS

GRAND BALLROOM EAST

2:00 pm–5:30 pm
JTuC, JOINT OPTICAL COMPUTING/PHOTONICS IN SWITCHING/SPATIAL LIGHT MODULATORS PLENARY SESSION
B. Keith Jenkins, *University of Southern California*
Joseph W. Goodman, *Stanford University, Presiders*

2:00 pm (Plenary)
JTuC1 Extended generalized shuffle networks, G. W. Richards, *AT&T Bell Laboratories.* This talk discusses how extended generalized shuffle networks are useful in dealing with various constraints that are encountered when implementing switching networks with photonic technology. **(p. 112)**

2:45 pm (Plenary)
JTuC2 ATM objectives and requirements for next-generation networks, Kai Y. Eng, *AT&T Bell Laboratories.* An overview of ATM networking is described with emphasis on virtual path transport architectures and features. SDH termination, ATM cell processing, and routing are discussed. **(p. 116)**

3:30 pm–4:00 pm COFFEE BREAK

4:00 pm (Plenary)
JTuC3 Photonics in switching: European systems demonstrators and the long-term perspective, Lars Thylèn, *Royal Institute of Technology, Sweden.* Status in the area of photonics-in-switching in Europe, highlighted by systems demonstrators, is reviewed, and the long-term perspective for photonics-in-switching is discussed. **(p. 120)**

4:45 pm (Plenary)
JTUC4 Transition from optical interconnections to optical computing, Richard C. Williamson, *MIT Lincoln Laboratory.* Optical interconnections will be a foot in the door to the next generation of computer systems and provide an evolutionary path toward the use of opt cs at finer scales. **(p. 125)**

TUESDAY, MARCH 16, 1993—*Continued*

GRAND BALLROOM CENTER

6:30 pm–8:00 pm
PTuD, PHOTONICS IN SWITCHING POSTER SESSION/ CONFERENCE RECEPTION

PTuD1 Holographic perfect shuffle interconnections for planar optics, S. H. Song, E. H. Lee, *Electronics and Telecommunications Research Institute, Korea;* C. D. Carey, D. R. Selviah, J. E. Midwinter, *Univ. College London, U.K.* For perfect shuffle interconnections, a planar optical configuration with two double-imaging deflective-reflective holograms is proposed. Interconnection capacity is derived from an aberration analysis. **(p. 128)**

PTuD2 Optoelectronic hybrid multistage interconnection network, J. Jiang, *Duisburg Univ., Germany;* K.-H. Tietgen, *Siemens AG, Research Laboratories, Germany.* Two new approaches to modularize the multistage interconnection network and a new design concept for optoelectronic hybrid realization are presented. **(p. 132)**

PTuD3 Translation of laser tuning experiments into networks, Josef Giglmayr, *Heinrich-Hertz-Institut für Nachrichtentechnik Berlin GmbH, Germany.* The relationship between laser tuning and networks is made transparent. Several examples (multiplexing on vectors) are evaluated by the number of crossed channels and compared. **(p. 136)**

PTuD4 Practical demonstration of a free-space optical crossbar switch, H. J. White, N. A. Brownjohn, C. Stace, G. M. Proudley; *British Aerospace Sowerby Research Centre, U.K.;* A. C. Walker, M. R. Taghizadeh, B. Robertson, C. P. Barrett, *Heriot-Watt Univ., U.K.;* M. J. Birch, *THORN EMI CRL, U.K.* The design, fabrication, and performance of a free-space single-stage optical crossbar switch, controlled by a liquid crystal SLM, is reported. **(p. 140)**

PTuD5 Efficient implementation methodology for 2-D space-invariant hypercube-based free-space optical interconnection networks, Ahmed Louri, Hongki Sung, *Univ. Arizona.* A new design methodology for constructing optical space-invariant hypercube interconnection networks for connecting 2-D array of inputs to 2-D array of outputs is presented. **(p. 144)**

PTuD6 Role of tunable-transmitter wavelength-division-multiplexing star-coupler architecture in high-performance multigigabit asynchronous-transfer-mode switching, Mario A. Santoro, Kai Y. Eng, *AT&T Bell Laboratories.* A tunable-transmitter wavelength-division-multiplexing design for a 2.5-Gbps/line growable switch architecture offers the best switching performance with the smallest number of wavelengths, independent of switch size. **(p. 148)**

PTuD7 Time domain approach for avoiding crosstalk in multistage interconnection networks (MINs), Chunming Qiao, Rami Melhem, Donald Chiarulli, Steven P. Levitan, *Univ. Pittsburgh.* A time domain approach for avoiding crosstalk in MINs is proposed. It is compared with network dilation. **(p. 152)**

PTuD8 Optoelectronic logic arrays using the light amplifying optical switch (LAOS), K. M. Geib, S. A. Feld, F. R. Beyette, Jr., X. An, H. Alhokail, M. J. Hafich, G. Y. Robinson, C. W. Wilmsen, *Colorado State Univ.* The design and fabrication of a 8 × 8 array of optoelectronic NOR gates is presented. The frequency response, power, and cascadability are analyzed and discussed. **(p. 156)**

PTuD9 Complete all-optical switching of visible picosecond pulses in birefringent fiber, Joshua E. Rothenberg, *IBM T. J. Watson Research Center.* Cross-phase modulation of visible picosecond pulses by an orthogonally polarized control leads to switching with a 50:1 contrast ratio, using a 10-m birefringent fiber in a time division interferometry arrangement. **(p. 160)**

TUESDAY, MARCH 16, 1993—*Continued*

PTuD10 Electrically actuated nanomechanical integrated optical switches, P. Pliska, W. Lukosz, *Swiss Federal Institute of Technology, Switzerland.* We demonstrated modulation, switching, and deflection of guided waves in (nonelectrooptic) waveguides on silicon, the required effective-index changes being induced nanomechanically by electrostatic forces. **(p. 164)**

PTuD11 Resonant III–V semiconductor layer and a grating coupler integrated in a waveguide modulator for far-infrared light, J. Stiens, C. De Tandt, W. Ranson, R. Vounckx, I. Veretennicoff, *Vrije Univ., Belgium;* G. Borghs, *Interuniversity Micro-Electronics Center (IMEC), Belgium;* P. Demeester, *Univ. Gent., Belgium.* The influence of a resonant plasma layer on the grating coupling efficiency in III–V semiconductor waveguides is calculated. Experimental results and applications are discussed. **(p. 168)**

PTuD12 2-D WDM optical interconnects using multiple-wavelength VCSELs for simultaneous and reconfigurable communication between many planes, A. E. Willner, J. E. Leight, *Univ. Southern California;* C. J. Chang-Hasnain, *Stanford Univ.* We propose and analyze a novel interconnect configuration in which one 2-D plane can communicate simultaneously and reconfigurably with many planes by using WDM. This system incorporates arrays of multiple-wavelength VCSELs as well as wavelength-selective detecting planes. **(p. 172)**

WEDNESDAY, MARCH 17, 1993

GRAND BALLROOM EAST

8:30 am–10:00 am
PWA, ALL-OPTICAL SWITCHING
Kunio Tada, *University of Tokyo, Japan, Presider*

8:30 am (Invited)
PWA1 Nonlinear loop mirrors for all-optical switching, Keith J. Blow, *British Telecom Research, U.K.* Abstract not available at press time. **(p. 178)**

9:00 am
PWA2 Ultrafast nonlinear refraction in an active MQW waveguide, M. A. Fisher, H. Wickes, *BT Laboratories, U.K.;* G. T Kennedy, R. S. Grant, W. Sibbett, *Univ. St. Andrews, U.K.* We demonstrate high-speed nonlinear phase shifts in excess of 2 π radians in a 1-mm long transparent active MQW waveguide at sub-watt peak powers. **(p. 179)**

9:20 am
PWA3 Demonstration of a polarization rotation gate in GaAs/AlGaAs MQW waveguides, P. A. Snow, I. E. Day, I. H. White, H. K. Tsang, R. V. Penty, *Univ. Bath, U.K.;* R. S. Grant, Z Su, W. Sibbett, *Univ. St. Andrews, U.K.;* J. B. D. Soole, H. P. LeBlance, A. S. Gozdz, N. C. Andreadakis, C. Cancau, *Bellcore.* Femtosecond optical switching is demonstrated in a nonlinear semiconductor birefringent waveguide. Optically induced polarization rotation increases the normalized gate transmission by a factor of 44. **(p. 183)**

9:40 am
PWA4 All-optical regenerator using a semiconductor laser amplifier in a loop mirror configuration, M. Eiselt, W. Pieper, H. G. Weber, *Heinrich-Hertz-Institut für Nachrichtentechnik Berlin GmbH, Germany.* A decision gate is reported for all-optical data retiming, operating at 1 Gbit/s polarization independent and enabling simultaneously wavelength conversion up to 60 nm. **(p. 187)**

10:00 am–10:30 am COFFEE BREAK

GRAND BALLROOM EAST

10:30 am–12:00 pm
PWB, PHOTONIC HIGH-SPEED SWITCHING SYSTEM
Rodney S. Tucker, *University of Melbourne, Australia, Presider*

10:30 am (Invited)
PWB1 High-speed photonic switching in corporate networks, Thomas M. Martinson, *Ascom Tech, Switzerland.* Two photonic systems applications that bring a new level of performance in broadband corporate networks are presented together with their interfaces to the electronic world. **(p. 192)**

11:00 am
PWB2 Optical add drop multiplexing for cell-switched networks, A. Budman, A. Bugos, J. Schlafer, E. Eichen, *GTE Laboratories Inc.* The experimental and theoretical performance, and optimal design, of a network in which fixed-length optical cells are inserted or removed from a fiber ring or bus using 2 × 2 space division photonic switches is discussed. **(p. 196)**

11:20 am
PWB3 Photonic time-division switching experiment, G. D. Bergland, *AT&T Bell Laboratories.* An experimental switching system is being designed and built for interconnecting broadband circuits through a photonic time-multiplexed switching network under DEFINITY® Communications System call control. Called DISCO (Distributed Switching with Centralized Optics). **(p. 200)**

11:40 am
PWB4 Experimental results for fast, high-capacity optical switching architectures, C. J. Moss, L. J. St. Ville, *GEC-Marconi Research Centre, U.K.*; K. S. Man, I. M. Burnett, *BT Laboratories, U.K.* Novel optical switching architectures have been demonstrated using a technology independent modular testbed. Wavelength-multiplexing techniques facilitate packet switching in the Gbit/s regime with further upgrade potential. **(p. 204)**

12:00 pm–1:30 pm COFFEE BREAK

GRAND BALLROOM EAST

1:30 pm–3:10 pm
PWC, NETWORKS AND SWITCHING
David Smith, *Bellcore, Presider*

1:30 pm
PWC1 Sparsely filled densely wavelength-division-multiplexed networks, J. E. Midwinter, *Univ. College London, U.K.* A DWDM technique to obtain flexible routing and high wavelength re-use in multinode mesh or ring networks is proposed which, when coupled with slow temporal reconfiguration, may bring the "optical aether" concept nearer reality. **(p. 210)**

1:50 pm
PWC2 Broadcast and switch—a new class of WDM networks for high switching-speed, high connectivity applications, Jacob Sharony, *Columbia Univ.* An architecture using star-couplers and wavelength-selective switches is described. This architecture features faster switching, high connectivity, reduced complexity and much fewer wavelengths compared to star-based networks. **(p. 214)**

2:10 pm
PWC3 Ultrafast wavelength switching and wavelength conversion with strained-MQW Y-lasers, W. Idler, D. Baums, E. Lach, G. Laube, M. Schilling, K. Wünstel, *Alcatel SEL, Research Centre, Stuttgart, Germany.* Electrical and optical wavelength switching with 500-psec speed is demonstrated with an interferometric Y-laser. Fast optical wavelength switching/conversion is achieved with 2.5 Gbit/s data across 45 nm. **(p. 218)**

2:30 pm
PWC4 Limits on smart pixel granularity: power dissipation and self-inductance, Charles W. Stirk, *Univ. Colorado.* For high-speed smart pixels on separate chips, the granularity should be large to decrease power dissipation and use chip area most efficiently. **(p. 222)**

2:50 pm
PWC5 Turnover-type free-space multichannel optical switch, Toshikazu Sakano, Kazuhiro Noguchi, *NTT Transmission Systems Laboratories, Japan.* A novel free-space optical switch that is suitable for intraboard chip-to-chip interconnects is proposed. A 64 × 64 switch is fabricated and demonstrated. **(p. 225)**

Photonic ATM/ Packet Switching

PMA 8:30am-10:00am
Grand Ballroom East

Akira Himeno, *Presider*
NTT, Japan

Optically-processed Self-Routing for 1D and 2D Photonic Switching Architectures

Paul R. Prucnal
Electrical Engineering Department, Princeton University, Princeton, NJ 08544

Introduction

In future fiber-optic broadband integrated digital services networks, the large data rates in the fiber-optic transmission links as well as the large number of packets transmitted per second will place severe demands on the required transmission bandwidth and reconfiguration speed of packet switches. Although electronic switching technology has already achieved high switching speeds, it is possible that it will be difficult for electronic switches to match the transmission bandwidths that the fiber-optic links can provide. Thus photonic switches may be needed to provide a transmission bandwidth that matches the aggregate bandwidth of the services carried by the fiber. If packet switching is used, then the reconfiguration speed of the photonic switch must also be fast.

The reconfiguration speed of the photonic switch is determined not only by the time required for the switch to change its state, but the processing time required to determine the appropriate state of the switch. Core-and-edge logical network structures for packet switches distribute the processing burden of low-level functions, such as routing, within the core of the network, and perform high-level functions, such as session setup, at the periphery of the network. The high-level functions require a large amount of slow processing, and can be performed easily with electronics. The low-level functions, on the other hand, require relatively simple processing, but must be performed at high-speed and completed in a time interval t' less than the packet length T_p, so that the switch is ready to route the next packet as soon as it arrives. These high-speed low-level functions include:

1. Routing of packets from input to output by reading the packet address header and setting the switch permutation; in general, packet length information must also be read;
2. Resolving contention of packets at multiple input ports for a single output port according to an established priority scheme, in a manner that minimizes packet loss (e.g., by storing packets in a buffer or misrouting packets); in some architectures such as the banyan, internal contention may occur within the switch as well;
3. Synchronization of packets at the switch input.

To avoid a data flow bottleneck at the switch input, the time t' required to perform the low-level control functions described in (1)-(3) above must be less than T_p. For example, if the data rate is 5 Gbit/sec the length of an ATM packet is T_p=85 ns. As bit rates increase, it will become increasingly difficult for electronic processing to satisfy this requirement. This suggests turning to optical processing of the low-level control functions, to take advantage of its speed, and in some cases, its parallelism.

Optically-processed self-routing, synchronization and contention resolution

The use of optical processing of switch control functions such as routing, contention resolution and synchronization, permits these functions to be completed in a time less than a packet length, so that the switch is ready to route the next packet as soon as it arrives. Routing strategies that are based on simple algorithms are the most feasible to implement with optical processing, because the present capability of optical processing is rather limited. An example of a routing strategy requiring only minimal processing is "deterministic" routing, in which the routes for all source-destination pairs are specified in advance. As a special case, "fixed-directory" routing maintains a routing table at each switch containing an outgoing link for each destination address. Such a routing table is easily implemented with optics.

The structure of a 2x2 photonic packet switching node using optically-processed fixed-directory routing, contention resolution and synchronization is presented in Fig. 1. Recognition of orthogonal (in the time, code or frequency domain) optical signatures, carrying address, packet length and framing pulse information, can be performed with an optical matched filter. The output of the address recognition processor is an address vector, which is converted to the appropriate state control signal by an optical look-up table. The optical look-up table consists of toggles which are closed for the set of elements in the vector that represent addresses that correspond to the bar state, and open for the set of elements in the vector that represent addresses that correspond to the cross state. The toggles can represent fixed connections, or can be programmed, for example, with electrooptic switches.

The incoming packet addresses at both switch inputs result in state control signals at the outputs of the respective routing look-up tables. Since the switch has no *a priori* information concerning the addresses of the incoming packets, the state control signals may be in agreement or in conflict with one another. The optical state conflict resolution processor produces an output state control signal that resolves contention using deflection routing. Deflection routing is well-suited for technologies in which buffers are expensive or not available, as is presently the case with optical technology.

Packet synchronization is required to ensure that the 2x2 switch can simultaneously route packets at both inputs to both outputs. Synchronization can be accomplished by matched-filter recognition of the framing pulse followed by a tunable delay. A tunable optical delay can be implemented with a variable-integer-delay line. This design allows a large number of delays with fast reconfiguration time.

Simplified self-routing procedures can be found for specific network architectures in which the position of each 2x2 switch within the network determines the appropriate path to the destination. For banyan (baseline, shuffle-exchange and crossover) networks, routing can be accomplished optically with one bit per stage and no optical look-up table. Banyan networks have the disadvantage of internal blocking. For lattice networks the optical look-up table can also be eliminated, and routing can be accomplished by simply ordering the magnitudes of the two destination addresses at each 2x2 switch. Although lattice networks require a larger number of switching elements than banyan networks, they can be arranged to avoid internal blocking (by using an "ordering" routing rule [7]). A simple time-domain approach for optical implementation of the "ordering" rule is illustrated at the top of Fig. 2 [7], such that

the first address pulse to arrive triggers a gating or inhibit signal for the duration of the packet. In this way, no additional logic is required to perform nonblocking self-routing through the NxN lattice switch.

Two-dimensional switching architectures are attractive for switch technologies which are readily fabricated in arrays, such as smart pixels. A 2D architecture is easily derived from a 1D architecture (such as the banyan or lattice) by folding each column in the 1D architecture in a serpentine fashion, while preserving the interconnection field, to form each plane of the 2D switch, as illustrated at the bottom of Fig. 2 [7]. In this way, the optically-processed self-routing architectures developed for the 1D architecture apply identically to the 2D architecture. The architecture of a self-routing 2D lattice, using 2x2 switches comprised of smart pixels, will be described in this presentation. Based on the "first-arrival" ordering rule, no additional logic is required to perform routing.

The optically processed routing controller and synchronization processing can be implemented with only passive optical components (fiber-optic delays, summers and splitters), a low-duty-cycle optical clock (e.g., a mode-locked laser), a non-paralyzable gating pulse generator, and fast optical correlators. All of these components are available "off-the-shelf" except for the fast optical correlators. Examples of demonstrations of optically-processed self-routing architectures will be presented in this talk (see Refs. 1-7 for details). In particular, a fast optoelectronic correlation technique was introduced for binary self-routing through a 4x4 banyan-type photonic switch using photoconductive "AND" gate. In order to perform the correlation operation with a speed that matches the bandwidth of the transmission channel, all-optical correlation should be used. If a sufficiently fast optical correlation can be implemented in the future, then the optically-processed routing control and synchronization for packet switching can be performed in real-time.

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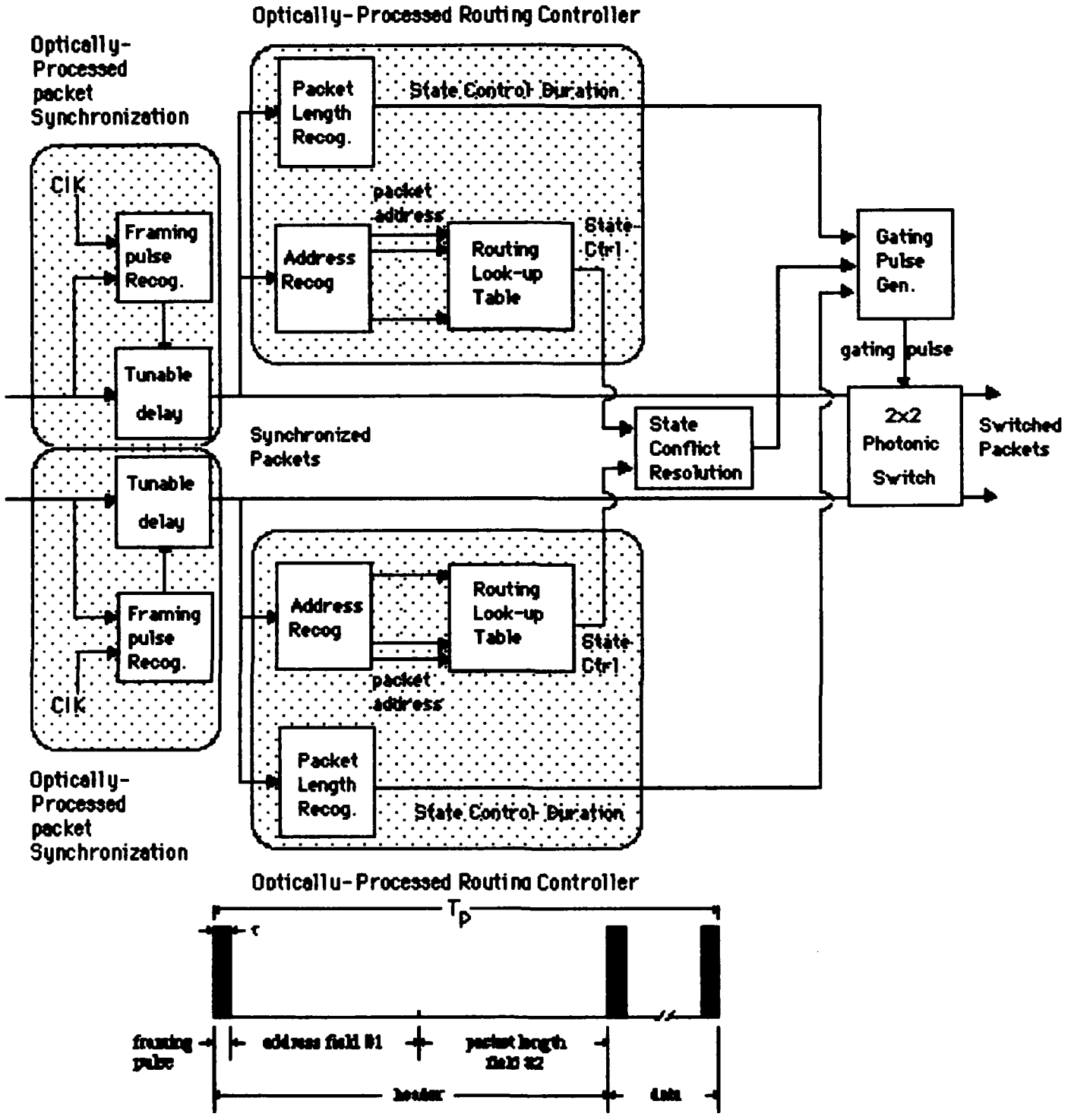
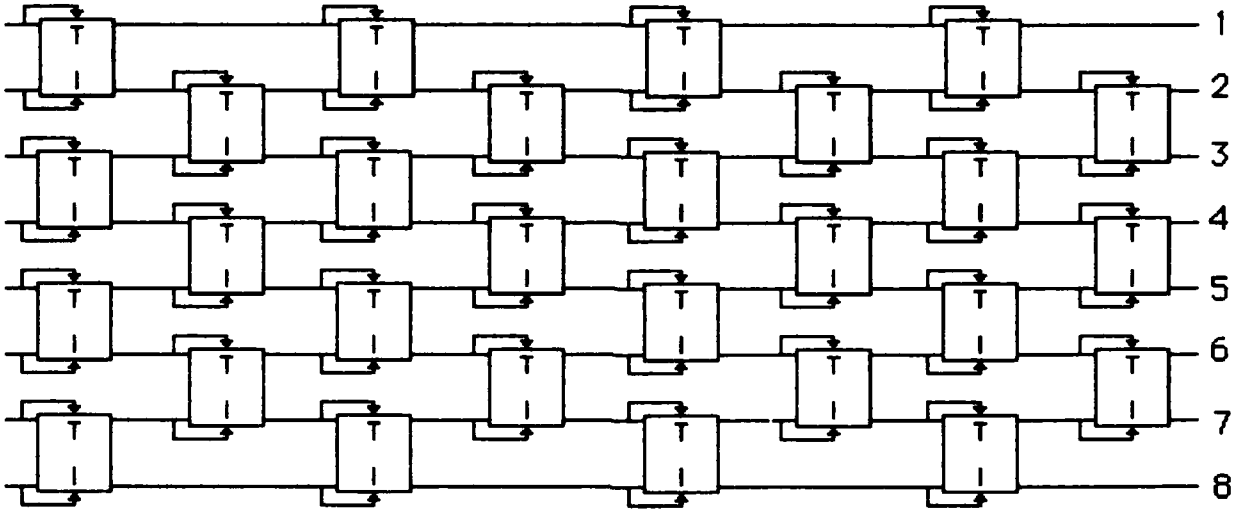
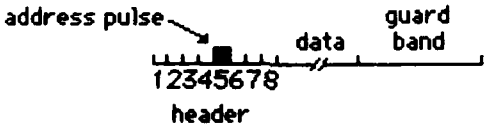


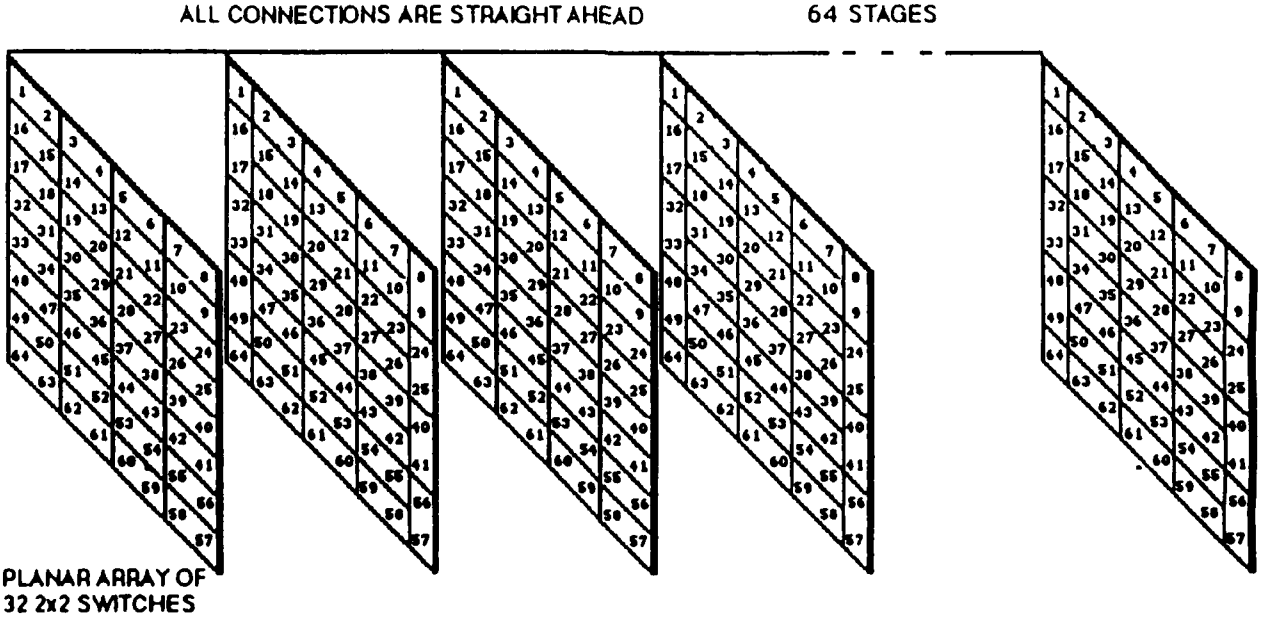
Architecture of a 2x2 photonic packet switching node using optically-processed fixed-directory routing, contention resolution and synchronization: Recognition of orthogonal optical signatures (encoded in the time, code or frequency domain) carrying address, packet length and framing pulse information, is performed with an optical matched filter. The output of the address recognition processor is an address vector, which is converted to the appropriate state control signal by an optical look-up table. The optical look-up table consists of toggles which are closed for the set of elements in the vector that represent addresses that correspond to the bar state, and open for the set of elements in the vector that represent addresses that correspond to the cross state. The incoming packet addresses at both switch inputs result in state control signals at the outputs of the respective routing look-up tables. The optical state conflict resolution processor produces an output state control signal that resolves contention using deflection routing. Synchronization is accomplished by matched-filter recognition of a framing pulse followed by a tunable optical delay.

Non-blocking, first pulse-arrival self-routing scheme, for a 1D NxN lattice switch: Assuming synchronized packets, the first arrival of an address pulse on the upper input of a 2x2 switch triggers the gating pulse generator, which sets the switch in the bar state for the duration of the packet; the first arrival of an address pulse on the lower input inhibits the gating pulse generator, which retains the switch in the cross state for the duration of the packet.





A 2D NxN lattice switch, derived by folding a 1D lattice accordion-style, while preserving the interconnection pattern. N stages are required, which can also be implemented with feedback after the 2nd stage. Each 2x2 switching element has inputs on the front, outputs on the back, and connections straight ahead. The self-routing rule is the same as above.



PHOTONIC ATM CROSS-CONNECT NODE BASED ON CELL AGGREGATION AND COMPRESSION

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1. INTRODUCTION

The telecommunication networks are evolving towards an always growing dimension and transport capability and to meet the requirements of the future broadband services they will have to be able to provide a great flexibility. The Asynchronous Transfer Mode (ATM) seems to be a key technique for switching and transport, to satisfy broadband and flexibility requirements.

With a B-ISDN access of 155 Mbit/s it is reasonable to expect for an ATM cross-connect an input bitrate of 2.5 Gbit/s or more. Photonic ATM switches and cross-connects have been proposed [1-3] to face the high speed and throughput requirements for the future B-ISDN nodes. It will be necessary to limit the physical dimension of the nodes, to keep cost and complexity within reasonable bounds. This could be achieved by keeping the traffic figures very low inside the node, and exploiting the very high speed made possible by optical devices.

The realization of a cross-connect by means of a photonic architecture seems quite attractive for the following reasons:

- the throughput should be in the range of 100÷500 Gbps, which is quite difficult to achieve by using only electrical solutions;
- the number of directions for each cross-connect and the number of Virtual Paths (VP) for each link should be little, whereas the traffic volumes should be very high.

In this paper we present a photonic ATM cross-connect (at VP level), based on the idea of aggregating a number of cells with the same destination, to keep the requirements of reconfiguration and elaboration speed within values that can be handled by electrical control, and compressing in time the cell aggregates, to create internal traffic of the desired value, at very high bitrate.

2. THE PHOTONIC ATM CROSS-CONNECT CONCEPT

The basic idea of the proposed cross-connect is to create very high speed optical flows inside the node, to be able to achieve high throughputs with minimal amount of hardware, relaxing at the same time the traffic figures and the requirements on the node subsystems (i.e. buffer dimensions, electronic control speed, etc). The proposed photonic ATM cross-connect for the B-ISDN can be modelled as shown in fig.1: it is characterized by a set of K external input/output links and N input/output internal links, with ultra-high speed and low traffic profile flows. Considering the subsystems, the Line and Exchange Termination (LT/ET) block provides the line termination functions as well as the exchange termination functions (i.e. label conversion at VP level), and is implemented electrically; the Cell Aggregation and Compression (CAC) block (patent pending) performs the (electrical) cell aggregation and the (optical) time compression and concentration. The Packet Disaggregation and Decompression (PDD) block (patent pending) provides the inverse functions of CAC; the Memory (MEM) block realizes packet storage for dynamic packet contention resolution; the Space Switch (SS) block performs packet switching from one link to another.The cross-connect is electrically controlled by the Switching Node Control (SNC), that gets the routing information from LT/ET and sets the devices within the node.

By aggregating the incoming cells and compressing the aggregates we are able both to concentrate the input flows and reduce the actual internal traffic (keeping the concentration ratio lower than the compression). This allows to minimize the hardware of the node both because the number of the internal links is smaller and because the lower traffic requires a smaller buffer dimension for the same packet loss probability. This architecture utilizes a partially shared buffer and the electrical control is organized by an output queueing structure that automatically solves the output contention. The storing function is realized by a multi-wavelength fiber loop delay line [2,4], where packets are wavelength converted, multiplexed on the storing wavelength and kept circulating synchronously, all equally accessible from the outputs (there is no head of the line block). To exit, they are broadcasted towards all internal outputs and selected by tunable filters on the desired output(s). A proper wavelength conversion and demultiplexing will realize the inner-to-outer stage routing.

Such a memory system is limited in the maximum number of positions, corresponding to the maximum number of wavelengths that can be handled by the devices in the loop and by the tunable filters in the output stage. This limitation can be overcome by reducing the required number of buffer positions, lowering the input traffic and moving towards a multi-stage architecture, keeping the described structure for the basic module instead of the global node. As an example, for a 16x16 module, and a 10^{-10} packet loss probability, a shared buffer dimension of 125 is required with a traffic load of 0.8 E, and a corresponding dimension of 35 with a traffic load of 0.4 E.

3. PACKET COMPRESSION AND DECOMPRESSION

After VPI conversion in the LT/ET subsystem, the cells enter the Cell Aggregation (CA) block, where they are assigned to one of the electrical aggregation queues according to their output destination. The number of cells to create a packet is chosen in the range of 8÷16, to achieve a significant reduction in the number of cells, still keeping the

aggregation delay within reasonable values. A time gap is added between cell aggregates to provide a guard-band gap for optical tunable devices and an internal header is associated to the cell aggregate as well. A time-out mechanism is also introduced to avoid unacceptable delays in case of low traffic. The packet compression, shown in fig.2, is based on a two step process: first, every single electrical bit of the packet is used to modulate (on/off keying) a train of very short pulses, obtaining a packet of very short bits, still with the same initial bit period T_0. The second step is aimed to actually concentrate in time the short pulses: this is obtained by folding a sufficient number of times the packet over itself. Referring to figure 2, let n be the total number of bits in the aggregate, $CR=2^c$ the compression ratio, and T_0 the initial bit time; to obtain the folding of the packet it is necessary to combine the original packet with a delayed copy of it, choosing the amount of delay in order to allow the positioning of the bits of the second half of the packet between those of the first half. By repeating this operation c times, a compression ratio of $CR=2^c$ is obtained. After each folding stage a space switch allows the erasing of the useless replicas.

To be decompressed, the cell aggregates are first routed towards the proper external link by wavelength demultiplexing utilizing either a grating or a combination of a splitter and a set of filters, one per output link. Once demultiplexed the cell aggregates enter the packet decompression block: as a change in speed is associated to the decompression function, a buffer has to be provided to cope with the arrival of consecutive packets. The packet decompression function is shown in fig.3. Each incoming packet, compressed by a factor CR, is split over CR directions and delayed by $i \cdot T_C$, being T_C the duration of a compressed bit and i=0÷(CR-1). These streams are then sampled at the same time by pulses of a period T_0, providing in this way CR different streams of pulses with a period equal to the decompressed bits. Each stream is then delayed by a multiple of the compressed packet length and equal to $i \cdot n \cdot T_C$ (where i=0÷(CR-1) and n=number of bits per packet) and finally optically combined with the others, providing a unique stream of pulses corresponding to the actual expanded cell aggregate. The last operation consists in the conversion into electrical signal, followed by the integration of the electrical pulses.

4. EXPERIMENTAL RESULTS

In this section some of the above mentioned blocks will be analyzed in more detail and latest experiments will be described. The results demonstrate the feasibility of each block and can, in principle, be generalized to apply to higher bit rates, multiwavelength operation, etc.

4.1 Wavelength conversion

An interesting way to produce wavelength conversion, by exploiting the gain modulation induced by saturation in a Semi-Conductor Optical Amplifier (SCOA), has been recently demonstrated [5]: Two carriers (λ_0, λ_1) are fed to the SCOA: the former (λ_0) is intensity modulated, while the latter (λ_1) is Continuous Wave (CW). Provided that the power of the first carrier (λ_0) is high enough to drive the SCOA into saturation, the gain of the amplifier follows the input data, and the amplitude of the carrier at λ_1 is modulated at the amplifier output by an inverted replica of the input data; the converted signal is recovered by optically filtering around λ_1. Wavelength conversion has been demonstrated for optical data up to several Gbit/s. The possibility of a fast wavelength reassignment has also been recently demonstrated (fig.4), using a fast tunable laser switching between λ_1 and a third wavelength λ_2 [6]. The switching behaviour of the converted signal at the SCOA output is very similar to that of the switching laser at the SCOA input, showing that practically no time impairment can be attributed to the wavelength conversion mechanism, at least on the time scale considered in the experiment.

4.2 Fibre loop memory

An optical fibre loop memory test bed (Fig.5) has been implemented [7], and packet storage experiments with a wavelength selective element in the loop have been carried out. To overcome round trip losses and to introduce wavelength selectivity, respectively, a switchable optical gain element (a broad band semiconductor laser amplifier, SCOA) and a narrowband optical filter (a Fibre Fabry-Perot interferometer, FFP) have been inserted in the loop. The packet signal is generated by a programmable 622 Mb/s data generator, whose output modulates the light of a CW operated 1.5 μm DFB (Distributed FeedBack) semiconductor laser, by means of a Mach-Zehnder integrated optics modulator. The SCOA has gain bandwidth of ≈4000 GHz, while the bandwidth of the FFP is ≈10 GHz; the fiber delay is around 1 μs. Once a packet has been sent to the loop memory, it keeps circulating until the gain of the SCOA is turned off to erase the memory. At the output of the loop the circulating packets exiting the loop are monitored (fig.6). Guard bands between adjacent packet circulations allow to switch-off the amplifier for a short time, at every circulation; this avoids the onset of instabilities in the loop. Bit error rate (BER) measurements have been performed at the fibre loop output, by synchronously gating the signal corresponding to the desired circulation. Error free operation ($BER < 10^{-10}$) up to the 12^{th} (instrumental limit) circulation has been measured. The extension to multiwavelength operation is straightforward.

4.3 Space-wavelength switching subsystem

Key devices in the Space-Frequency switching subsystem are the tunable filters, which must select the desired wavelength, rejecting all the others and must be capable of a fast tuning. For this purpose the use of DFB or DBR (Distributed Bragg Reflector) lasers biased below threshold to work as filter/amplifiers can be foreseen. Although more work is needed to improve the performance of these devices, some encouraging results have already been obtained, in terms of tuning range and tuning speed. As an example fig.7 shows the time resolved spectrum recorded at the output of a 1.5 μm multi-electrode strained MQW (Multiple Quantum Well) DFB filter/amplifier when two CW carriers, spaced by ≈20 GHz, are fed to its input and the DFB filter centre wavelength is switched from one carrier to the other, applying a square

wave to its bias currents [8]. Typical measured tuning times are 2-4 ns for a ≈20 GHz wavelength step; larger tunings also require longer times, limited by the carrier lifetime of the device.

4.4 Packet decompression

This decompression function is basically the demultiplexing of a very high bit rate TDM data stream into lower bit rate tributaries. An all optical way of performing this task has been demonstrated exploiting gain saturation in a SCOA [5] in a way similar to the above mentioned wavelength conversion operation explained above; in this case (fig.8) the carrier at λ_c carries the compressed data stream while the output of a "sampling" laser at λ_r is turned on syncronously with the tributary of the data stream to be extracted. Fig.9 reports some significant waveforms observed in a 1:8 demultiplexing experiment at 4 Gbit/s; the upper trace refers to the compressed input data stream at λ_c, while the lower trace shows the output signal, filtered around λ_r, where the higher pulses correspond to the input "zeros" and the lower pulses correspond to the input "ones". Different tributaries can be selected by delaying the turn on time of the sampling laser; multiple tributaries can be extracted in parallel by sending many optical carriers at different wavelengths at the SCOA input and turning them on at the proper time; the output signals are then recovered by filtering with a suitable multichannel optical filter, e.g. a diffraction grating.

5. CONCLUSION

A photonic ATM cross-connect based on cell aggregation and compression techniques has been described, and the hardware implementation of the main blocks has been proposed.

Experiments have been carried out to demonstrate the feasibility of the most critical functions. Fast wavelength reassignment, suitable for multigigabit operation, has been obtained, exploiting fast tunable lasers and SCOA; packet storage up to 12 error free circulations has been demonstrated in a wavelength selective fiber loop memory; fast tuning capability of DFB filters has been shown and all optical demultiplexing of a 500 Mbps period tributary from a 4 Gbps multiplex has been demonstrated, exploiting a gain saturation effect in an optical amplifier.

ACKNOWLEDGMENTS

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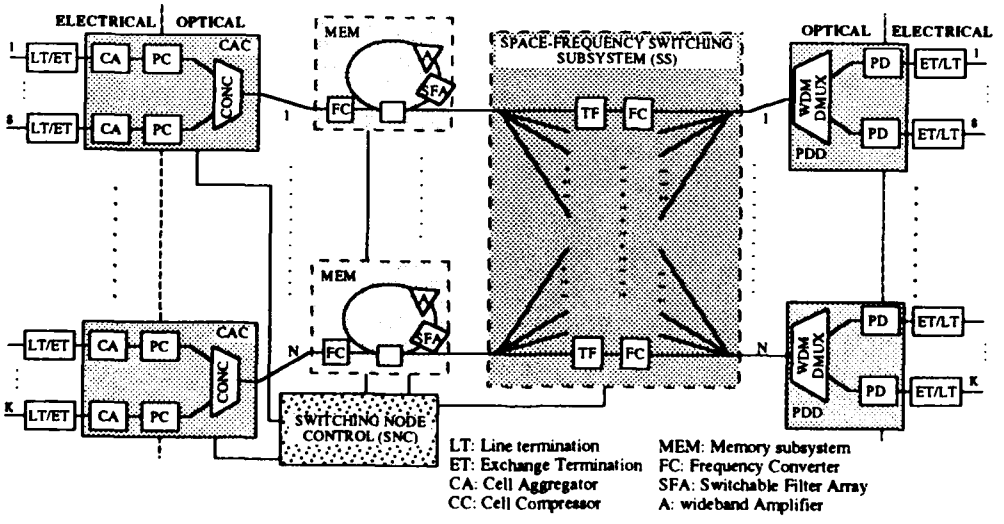

Fig.1: ATM DXC global architecture.

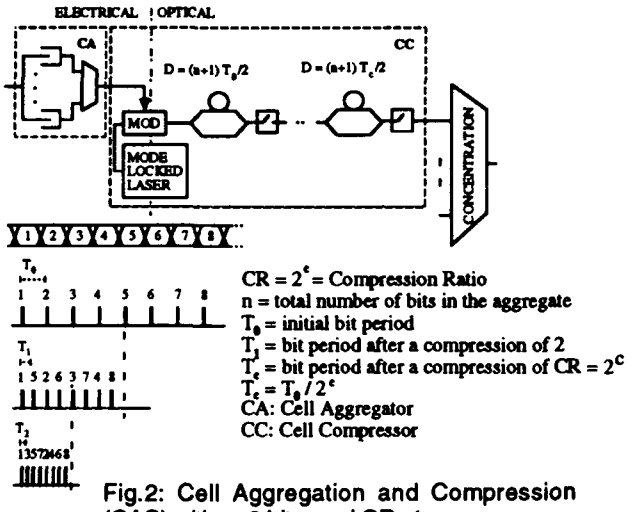

Fig.2: Cell Aggregation and Compression (CAC) with n=8 bits, and CR=4.

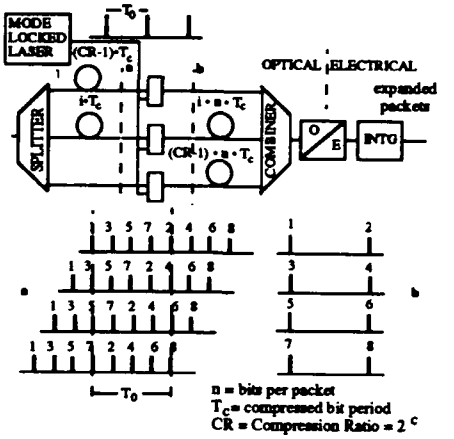

Fig.3: Packet Decompression (PD) with n=8, CR=4.

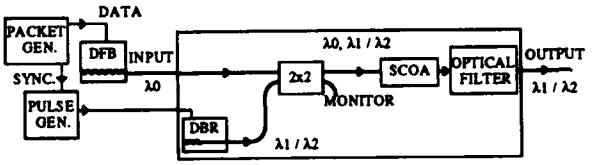

Fig.4: Set-up for wavelength conversion and fast wavelength reassignment.

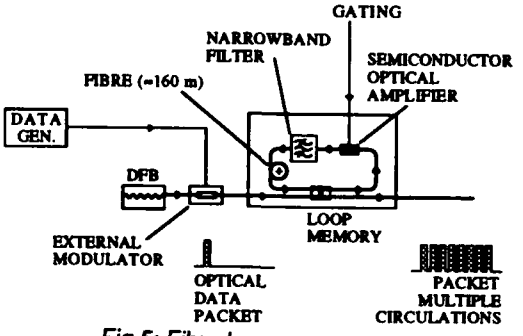

Fig.5: Fibre loop memory set-up.

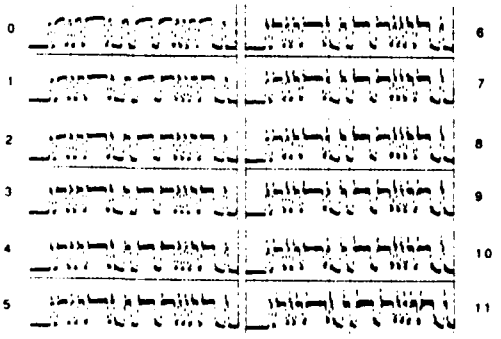

Fig.6: Details of packets exiting the loop for successive circulations

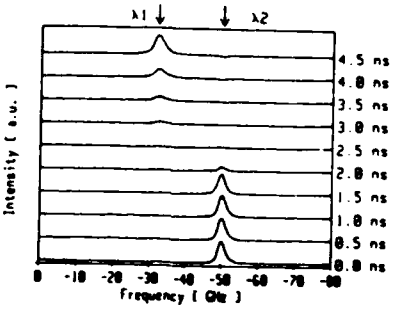

Fig.7: Time resolved spectrum at the output of a fast tunable DFB filter/amplifier.

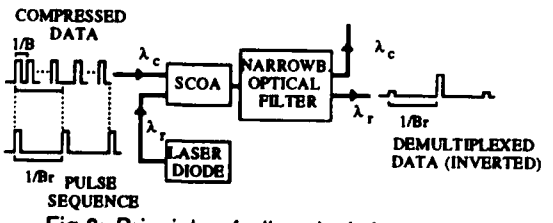

Fig.8: Principle of all optical demultiplexing of compressed data.

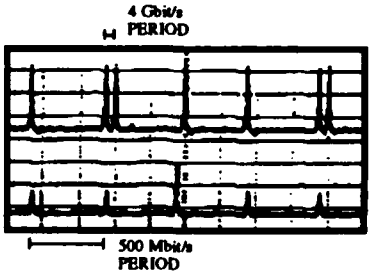

Fig.9: All optical demultiplexing of a 500 Mbit/s channel from a 4 Gbit/s stream.

PHOTONIC 2X2 PACKET SWITCH WITH INPUT BUFFERS

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Introduction

Packet switching is an integral part of Asynchronous Transfer Mode (ATM) switching systems in Broadband ISDN (B-ISDN) and will have a major input on future photonic communications systems. Self-routing packet switches are the basic switching elements in ATM networks. There have been a number of recent demonstrations of self-routing photonic packet switches, for example [1], [2]. A key feature of these switches is that the information content (payload) of a packet can have a data rate which is not limited by electronics [1].

A major limitation of previously reported photonic packet switches is that they are unable to resolve events when input packets are simultaneously targeted for the same output. This is commonly known as output contention. Eiselt et al. [3] demonstrated output contention resolution using a fibre loop at one input of a 2x2 packet switch. However, when a packet is stored in this fibre loop the associated input cannot receive new packets. In addition, Eiselt's experiments could only handle a limited number of synchronous events. However, for ATM systems packet arrival will, in general, be asynchronous. For this reason it is critical that the switching element be able to switch input packets and resolve output contention regardless of the arrival time of the packets and regardless of previous packet flow through the switch. The present paper demonstrates a new 2x2 photonic packet switch with two fibre-loop input buffers (memories) that enable output contention to be resolved. The new 2x2 switch handles fully asynchronous traffic. It uses high-speed electronic control that prioritizes all switching and memory operations and guarantees packet integrity while maximising throughput. We believe that this is the first demonstration of a self-routing photonic packet switch that resolves output contentions and operates asynchronously.

Experimental setup

Fig. 1 shows the architecture of the experimental 2x2 packet switch. A directly modulated DFB laser at 1.3 μm produces packets that are directed through an optical power splitter to the two inputs of the switch. The B input is delayed by an adjustable length fibre delay to simulate asynchronous operation and provide a range of input packet sequences.

Fibre splitters couple 10% of the power at the inputs into optical-to-electrical (O/E) converters (receivers). Following each fibre splitter is a fibre delay line. These delay lines provide sufficient delay for the address header to be read and for the controller to set up the drive conditions to the $LiNbO_3$ switches and the semiconductor optical amplifiers (SOA's) in the 2x2 packet switch. Access to each memory is controlled by an associated $LiNbO_3$ switch directly following each delay line. When the associated memory $LiNbO_3$ switch is in the *cross*

state a packet can be stored into the memory and/or released from the memory. When it is in the *bar* state a packet can be routed to the switching element and/or recirculate in the memory. Regardless of whether a packet is stored in a memory, input packets can be routed through the associated memory $LiNbO_3$ switch. Losses in the memories are compensated by SOA's that are switched on when there is a packet in the memory and are switched off when the packet is removed from the memory. This gating of the memory SOA's ensures that noise build-up in the memories is minimised [4]. Finally a $LiNbO_3$ switch (the switching element) directs packets to the appropriate output. Routing of incoming and stored packets and the timing of packets throughout the 2x2 switch is controlled by the electronic controller (controller). The controller uses very high-speed ECL (Motorola ECLinPS) and can operate at header rates up to 1.5 Gb/s. Precise timing of packets in the switch and the memories ensures packet integrity.

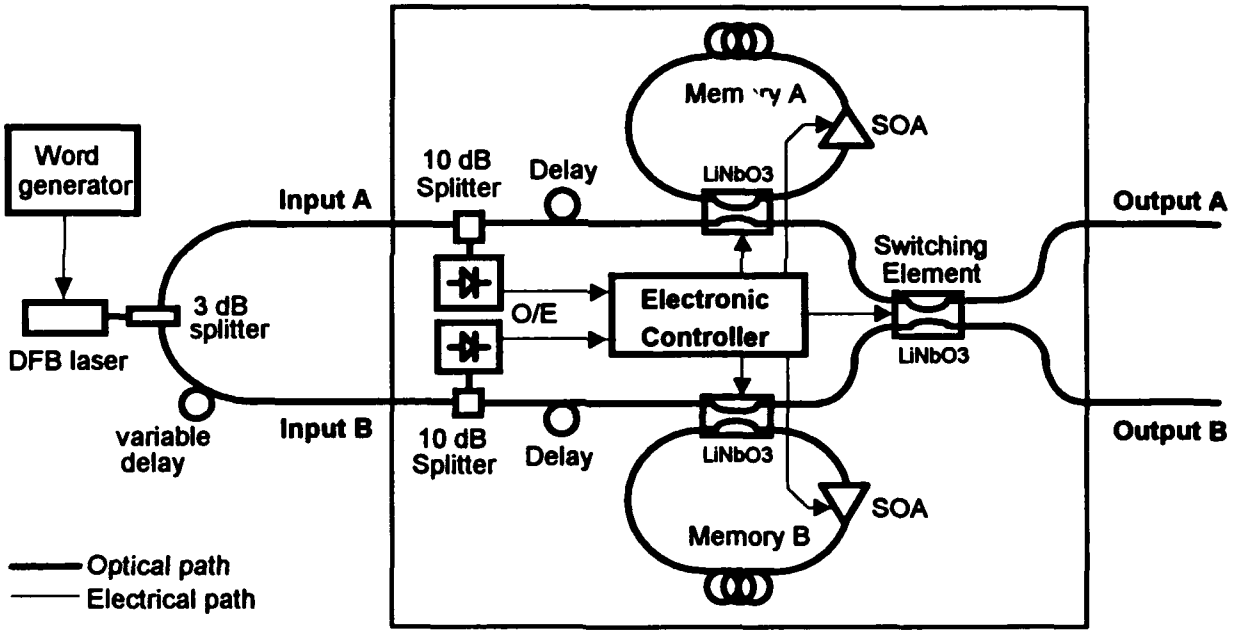

Figure 1: Architecture of the experimental 2x2 packet switch.

The 2x2 packet switch recovers timing information for each packet from a single start bit preceding the header. The address header is then clocked into a buffer and decoded to give the output destination. If packets arrive simultaneously at the two inputs then a predefined queue is enforced to ensure packet contention does not occur. Stored packets in both memories are included in this queue. Thus, output contentions are resolved between incoming packets and packets in the memories. If an input packet arrives while its output destination is busy and the memory at that input is occupied, the packet is routed through the switching element with the current switch state (bar or cross). This event causes the packet to be misrouted and, depending on the system architecture, the associated packet may be redirected to its final output destination. To minimise the probability of this occurring, more than one memory on each input could be used.

The switching element can be used simultaneously by both inputs when the respective packets have opposite output destinations. This exploits the maximum traffic capacity of the $LiNbO_3$ switch and increases the packet throughput. Packets may arrive at any time on either input thus allowing fully asynchronous traffic. For correct operation of the switch, incoming packets on a single input must be separated in time by a minimum guard band. This guard band is the time between the end of one packet and the beginning of the next packet. The switch guarantees that its outputs have this guard band between successive packets, and thus packet integrity will be retained when packets are routed to subsequent switches in a larger network. The guard band is ~39 ns.

Results

The packet format used for initial experiments was a 72-bit payload at 622 Mb/s preceeded by a 6-bit header at 155 Mb/s. Input and output optical packets were measured using high-speed pin photodiodes and a sampling oscilloscope. Fig. 2 gives measured input and output packets and shows an example of contention resolution. The top two traces show the packets at Inputs A & B. Input packets are labelled A1(x) - A4(x) at Input A and B1(x) - B4(x) at Input B, where x is the output destination of the packet (A or B). The bottom two traces show the packets at Outputs A & B with packets labelled to show their origin. Note that the variable optical delay at the input to the switch has been adjusted so that packets at Input A arrive before packets at Input B, thereby simulating asynchronous traffic. Packets A1 and B1, and A2 and B2 pass through the switching element simultaneously because they have opposite output destinations. Packet B3 (with output destination B) arrives just after packet A3, which is already passing through the switch to output B. This constitutes an output contention event. To resolve this output contention, Packet B3 is stored in Memory B. Before packet B3 can exit from Memory B, new Packets A4 and B4 arrive and are routed through the switching element thus forcing packet B3 to recirculate in Memory B a second time. Packet B3 finally exits from Memory B and passes to its desired output at the end of this second recirculation.

The output waveform of B3 includes the spontaneous emission of the Memory B amplifier, which is visible as a pedestal on the output waveform. It has been shown [4] that with a filter in the Memory, the spontaneous emission can be reduced sufficiently to allow up to more than 100 packet recirculations. Note that a small amount of crosstalk from the Memory B $LiNbO_3$ switch appears on Output B. The insertion loss from input to output of the 2x2 switch is about 9 dB, which is mainly due to the $LiNbO_3$ switches.

Conclusions

We have demonstrated a photonic 2x2 packet switch with optical buffering on both inputs and with output contention resolution. The switch operates with fully asynchronous traffic. Payload data rates are not restricted by the control electronics. The control electronics use a high speed ECL family and prioritize all switching and memory operations, thereby guaranteeing packet integrity, while maximising throughput.

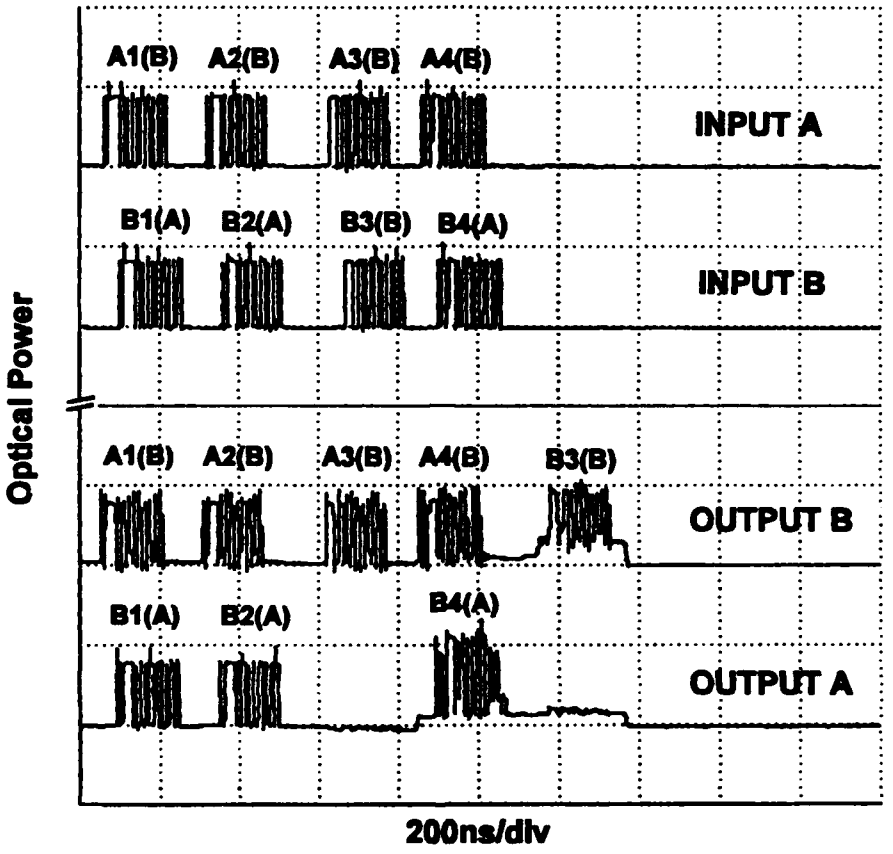

Figure 2: Measured input and output optical packets, showing output contention resolution.

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Variable Optical Delay Line for Frame Synchronizer in Photonic ATM Switching System

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I Introduction

Photonic ATM switching system with hypercube topology is one of the promising photonic switching systems which utilize the high speed transmission ability of photonics technology [1] [2].

The Frame Synchronization is one of the key technology for realizing the photonic ATM switching system [2]. The variable optical delay line is the most important device in the frame synchronizing circuit shown in Fig.1. The variable optial delay line should have a flatten group delay dispersion for a required bandwidth and is desirable to change the delay time contineously.

We will report the realization of variable optical delay line based on the optical circuit synthesis technology, for the first time.

II Basic Structure of Variable Optical Delay Line

The basic structure of optical delay line is shown in Fig.2. The serial connection of two optical circuits with first order group delay dispersions of opposite sign has a flat group delay dispersion. When the optical center frequency of the dispersive optical circuit is shifted, the total group delay time can be changed as shown in Fig.3. The element optical circuits of the first order group delay dispersion can be realized by Chebyshev polynomials optical filters [3] [4] and the transversal optical filters [5].

III Design of the Variable Delay Line

For example, a photonic ATM switching system with ATM cell transmission rate of 10 Gb/s is assumed [2]. The ATM cell with 53 bytes has about 50 ns length so that the one cell buffer of optical fiber has about 10 meters length. The 1/2 bite length orresponds to 50 ps or 1 cm of optical fiber. For the frame synchronization, the variable optical delay line should have the variable range of $\pm 1/2$ bite at least, and the bandwidth of flatten group delay dispersion of more than 15 GHz .

Fig.4 shows the transmittance and the group delay time of the synthesized optical circuits based on the optical transversal filter shown in Fig.2. The transfer function $F(f)$ of an element optical circuit with the first order group delay dispersion is given by Eq.1.

$$F(f) = G(f)\exp(-j2\pi\tau f^2 G(f)) \tag{1}$$

where the window function $G(f)$ is given by Eq.2, τ=12.5 ps/GHz and f_o=25 GHz.

$$G(f) = \left(1 + \left(\frac{f}{f_o}\right)^6\right)^{-1} \tag{2}$$

The weighting coefficients of the transversal filter is determined by the truncated Fourier expansion $F_n(f)$ of the transfer function $F(f)$. The number of the delay elements is 48. The delay time T of the delay elements is 20 ps.

$$F_n(f) = \sum_{n=0}^{n=N} a_n \exp(-j(2\pi T f + \phi)n) + \sum_{n=1}^{n=N} a_{-n} \exp(j(2\pi T f + \phi)n) \tag{3}$$

The weighting coefficients $\{b_n\}$ for the element optical circuit #2 with negative group delay dispersion are given by $\{a_n^*\}$. The optical center frequency of the transversal filter is shifted by changing the optical phase shift ϕ of the delay elements. The group delay time change of the variable optical delay line is shown in Fig.5 and it is estimated by Eq.4.

$$\Delta T_g = \frac{dT_g}{df}\Delta f \simeq 2\tau\Delta f \tag{4}$$

The variable range of the delay time is ±50ps for the center frequency shift Δf of ±2GHz, and the bandwidth is larger than 15 GHz.The pulse distortion of 10 Gb/s ATM signal is negligibly small in simulation.

IV Experimental

The Chebyshev polynomials optical filter [3] [4] employing TeO_2 birefringent crystal is used with the 15 km normal dispersion fiber for checking the operation of the variable optical delay line. Fig.6 shows the schematic structure of the Chebyshev polynomials optical filter used in the experiment. The propagation time difference of two polarization modes in each element is 10 ps for the crystal length of 12 mm. The optical phase shift of each segment is adjusted by a small heater employing a chip resister.

Fig.7 shows the experimental set-up for measuring the group delay of the variable optical delay line. The optical network analyzer [3] measures the modulation envelope delay during the carrier optical frequency scanning. The resolution measuring group delay time is 3 ps for the optical frequency scan width of 180 GHz.

Fig.8 shows the measured group delay time of the variable optical delay line,where the optical frequency is measured from 193.83THz.

The delay time variation of 30 ps is obtained by center frequency shift of 15 GHz.

V Discussion

The variable optical delay line for the frame synchronizer is required to have fast time response. An optical coupler is used for detecting the cell header as shown in Fig.1. The time delay propagating from the coupler to the variable optical delay line should cover the processing time of cell header detecting circuit and the synchronizing controller, and the response time of the variable optical delay line. As an example, the delay time is assumed to be 5 ns (1 m fiber length) so that the optical phase shifter should have some sub-nano second response time. The transversal optical filter configuration based on EO material such as $LiNbO_3$ is desirable for fast response variable delay line.

VI Conclusion

A variable optical delay line is proposed for the frame synchronizer in photonic ATM switching system. By using Chebyshev polynomials filter with 10 km abnormal dispersion fiber,the operation of the variable delay line proposed was confirmed.

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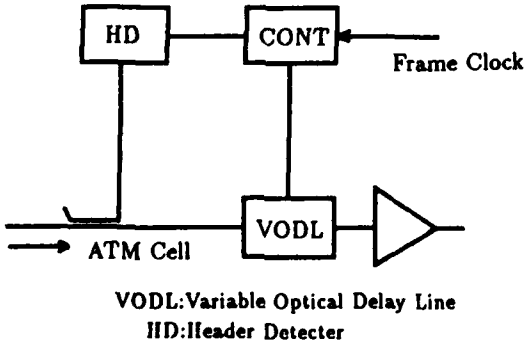

Figure 1: Frame synchronizer

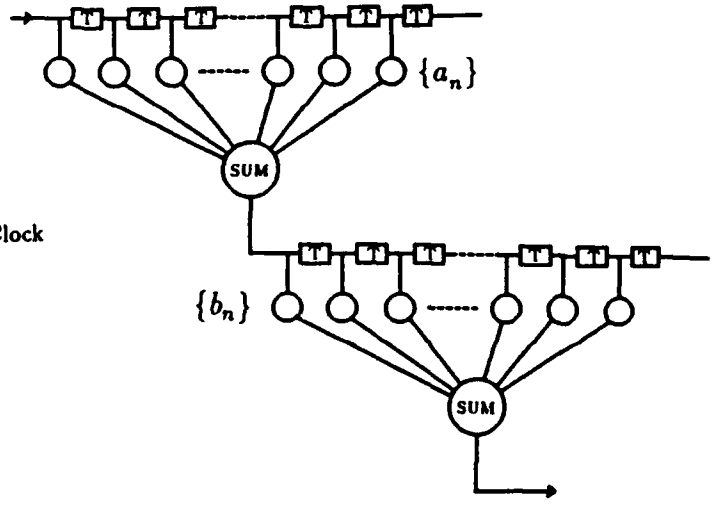

Figure 2: Basic structure of variable optical delay line

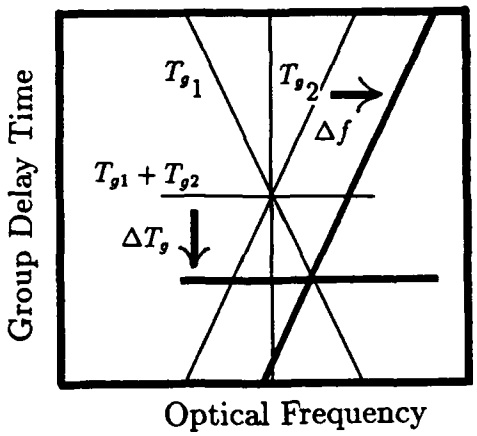

Figure 3: Operation of variable optical delay line

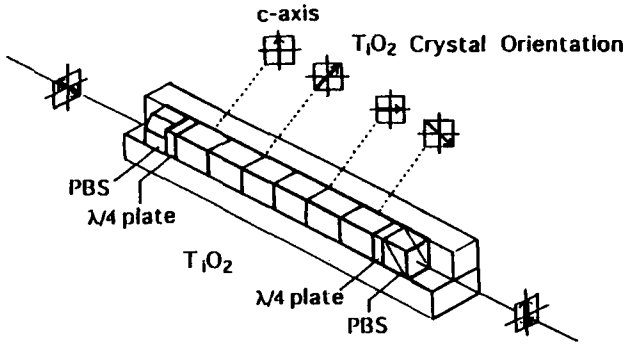

Figure 6: Basic structure of Chebyshev polynomials filter

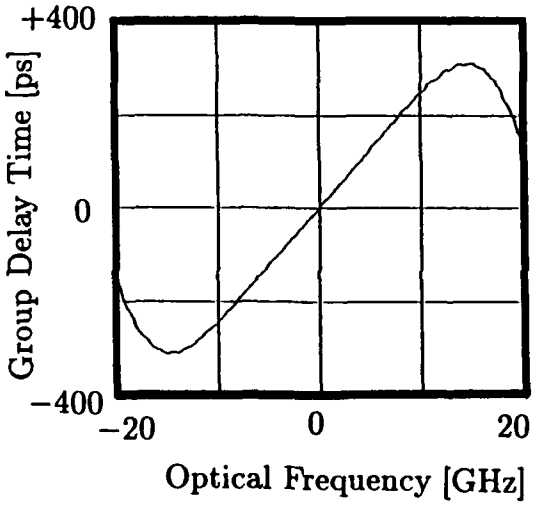

Figure 4: Characteristics of dispersive optical circuit

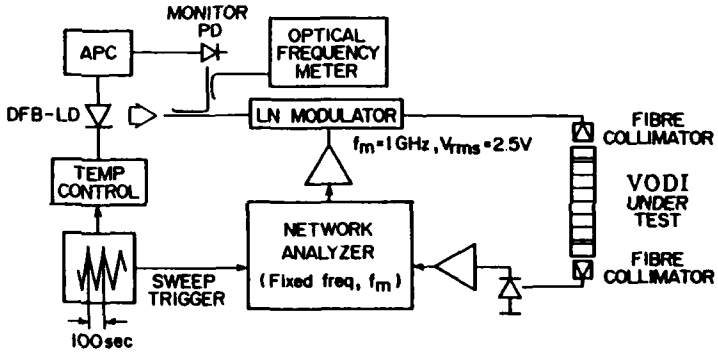

Figure 7: Optical network analyzer

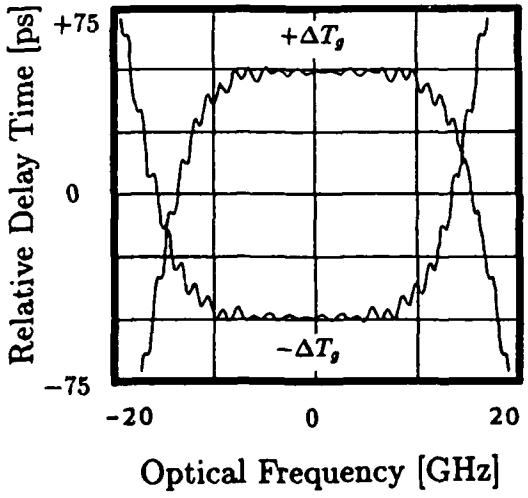

Figure 5: Characteristics of variable optical delay line

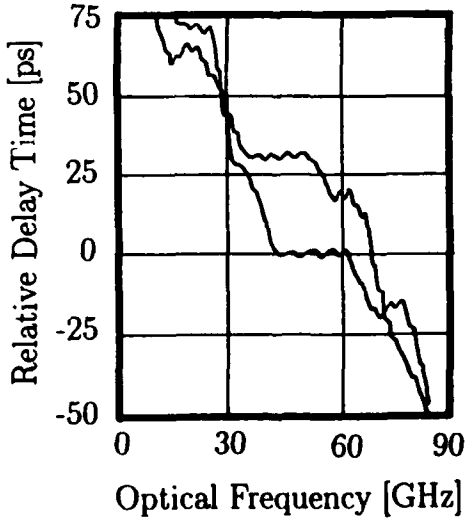

Figure 8: Measured characteristics of variable optical delay line

Semiconductor Modulators and Switches

PMB 10:30am-12:20pm
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Marko Erman, *Presider*
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Advances in Semiconductor Waveguide Switches

Hans Melchior
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Polarization Independent Optical Modulation with Tensile-Strained GaAs-InAlAs Quantum Wells grown on GaAs Substrate

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1. Introduction

Large field-induced optical absorption and refractive index variations through the quantum confined Stark effect in quantum well structures have prompted the development of many high performance compact optical modulating devices[1]. However, several shortcomings are present and one of them is a strong polarization dependent characteristic in lattice-matched systems[2]. This is due to the fact that the dipole moments of electron-heavy/light hole transitions show a strong polarization dependence, such that while TE mode light, with the electric vector parallel to the quantum well layers, interacts with both heavy and light hole transitions, only electron-light hole transitions are involved in the TM mode polarization, where the electric vector is perpendicular to the quantum well layers[3]. Moreover, in an unstrained quantum well, the valence bands for the heavy and light holes are degenerate and hence the electron-heavy hole transition always lead the electron-light hole transition at the absorption edge due to the heavy hole's larger effective mass. As a result, there exists a large difference in the optical absorption and refractive index variation at the absorption edge between the TE and TM mode polarizations.

Polarization independent optical switching utilizing quantum well structures was first demonstrated with parabolic potential quantum wells, where the energy shift is independent of the effective mass of the particle and this leads to an enhanced Stark shift for the light hole related absorption peak[4]. A more effective method of achieving total polarization independence characteristics will be to make the electron-light hole transition peak the leading one with tensile strain[5]. In this way, both TE and TM mode polarizations will display identical absorption edges. This can be easily achieved in the InGaAs-InAlAs-InP material system since both compressive and tensile strain can be achieved by varying the indium content in the layers. In fact, a structure with a tensile-strained InGaAs barrier with a lattice-matched well has been demonstrated to display polarization insensitive optical amplification[6,7], whilst a polarization independent waveguide interferometric switch was also realized with tensile-strained InGaAs-InP quantum wells[8].

In this paper, we propose and demonstrate a novel structure for achieving tensile strain with the GaAs substrate by first growing a relaxed InAlAs grid layer. Theoretical simulations and waveguide absorption measurements using GaAs-InAlAs quantum wells show that polarization independent optical modulation is feasible.

2. Realization of Tensile Strain on GaAs Substrate

To realize tensile strain with the GaAs substrate, it is necessary to lay down a grid layer with a much larger lattice constant. This can be accomplished by growing a thick InGaAs or InAlAs layer so that the lattice spacing at the surface relaxes back to its bulk value, i.e. letting the thickness get above the critical thickness with respect to the substrate. Subsequent growth of layers with a lattice constant smaller than that of the grid will result in tensile strain. However, allowing the thick grid layer to relax back to its bulk lattice constant also means the generation of misfit dislocations. In order to obtain good crystal quality at the surface, these dislocations must be filtered by bending them to the sides of the sample through the interfaces of a strained-layer superlattice structure[9]. In addition, the strained-layer superlattice structure should be designed in such a way that its average lattice constant matches that of the grid so that the structure itself does not introduce any new dislocations. Assuming that the two layers A and B are of the same thickness, this means that

$$a_{grid} = \frac{1}{2}(a_A + a_B),$$

which implies that the strain in the two layers are of opposite sign and they balance themselves out to be a free-standing structure.

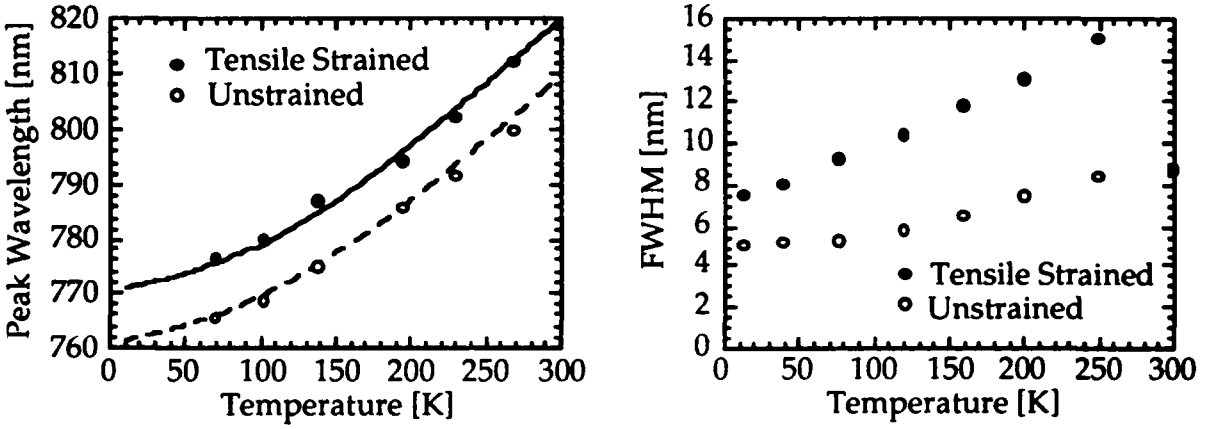

Figure 1 Photoluminescence peak wavelength and its FWHM for tensile-strained and unstrained GaAs-AlAs quantum wells.

To examine the feasibility of such an approach, two samples each with 5 sets of 22ML (monolayer, 1ML=2.83Å)-wide GaAs-AlAs quantum wells were prepared. One sample has a 1μm thick $In_{0.06}Al_{0.94}As$ grid with the appropriate InGaAs-GaAs strained-layer superlattice dislocation filter structure in between, while the other sample is totally unstrained.The temperature dependence of the photoluminescence peak wavelength and its FWHM are shown in Fig. 1. Solid and dashed lines are the theoretical values based on quantum well energy level calculations. Good agreement between the experimental and calculated results is obtained and the tensile-strained sample's peak is shifted by 10nm to the longer wavelength. Moreover, the FWHM obtained for both samples are roughly of the same order, indicating reasonably good crystal quality in the strained GaAs-AlAs quantum wells. Normaski etch-pit microscopy also indicated the effectiveness of the superlattice dislocation filter structure in reducing the amount of threading dislocations up to the quantum well structures.

Under biaxial tension, the strain induced splitting of the bulk valence band pushes the light hole band to a higher energy than the heavy hole one. For large strains and thick wells, the first quantum energy level can be due to the light hole with a high in-plane mass. By controlling the amount of strain and the well width, it is possible to bring both heavy and light hole energy levels together. In such a case, only a single absorption peak is observable.

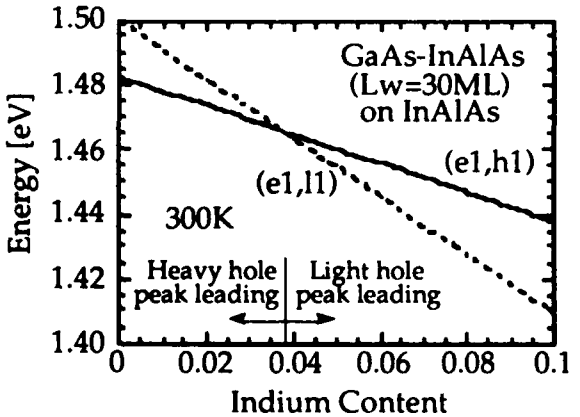

Figure 2 Calculated heavy and light hole energy levels for 30ML-wide GaAs-InAlAs quantum wells on InAlAs grid as functions of indium content in grid and barrier layer.

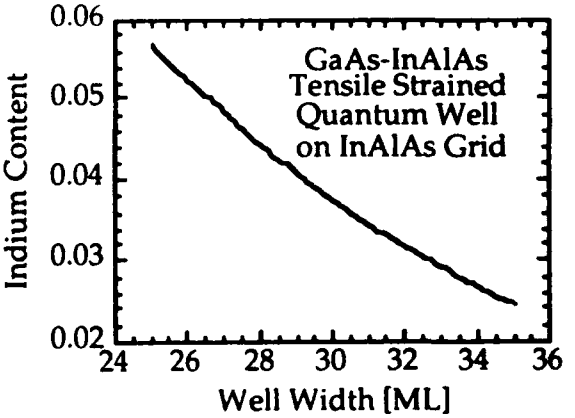

Figure 3 Variation of indium content in grid and barrier layer of tensile-strained GaAs-InAlAs quantum wells with well width for merging of zero-field heavy and light hole energy levels.

Figure 2 shows the calculated heavy and light hole quantum well levels for GaAs-InAlAs quantum wells with a well width of 30ML, grown on an InAlAs grid with the same indium content as the barrier layer. It can be easily seen that the light hole peak could be brought to the absorption bandedge by increasing the strain, i.e. setting the indium content above 0.038. Moreover, the indium content for the merging of the heavy and light hole energy levels decreases as the well width increases as shown in Fig. 3. This is due to a reduction in the energy separation between the two levels as the well widens.

3. Field-Induced Optical Effects in Tensile-Strained Quantum Wells

The field-induced energy shifts of the heavy and light hole quantum energy levels for a 30ML-wide GaAs-InAlAs quantum well on an InAlAs grid with an indium content of 4% is shown in Fig. 4. It can be seen that the shift of the heavy hole peak is larger than that of the light hole and this is due to the difference in their effective masses. The absorption coefficient spectra for both TE and TM modes of Fig. 5 display a single absorption peak at the bandedge, indicating that the two hole energy levels are very close together. Since the heavy and light hole energy levels are kept almost together throughout the entire range of the applied field at a wavelength of 855nm, the absorption spectrum shows very little polarisation dependence. This points out possibility of polarization independent modulation with the above tensile-strained quantum well structure.

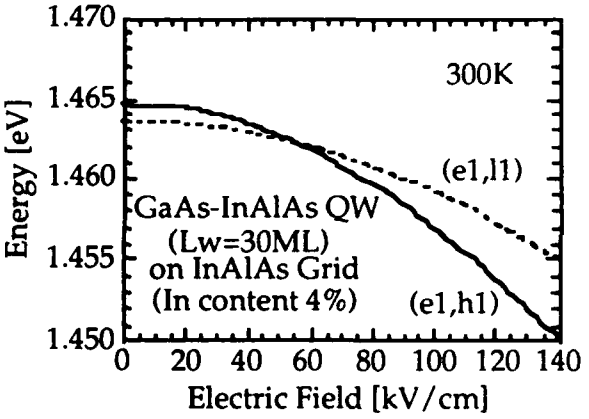

Figure 4 Field-induced energy shifts of heavy and light hole energy levels for tensile-strained GaAs-InAlAs quantum wells.

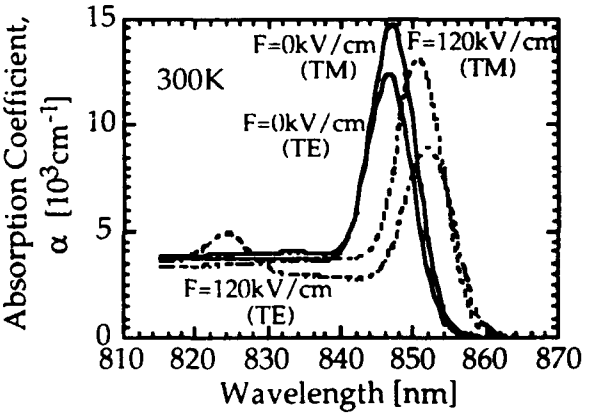

Figure 5 Calculated room temperature absorption spectra of tensile-strained GaAs-InAlAs quantum wells for both TE and TM modes.

Taking into consideration of light wave confinement and the critical thickness limitations, the following p-i-n structure is proposed for incorporating tensile strain in a planar waveguide structure on GaAs substrate. A thick layer of 6000Å of n-InAlAs grid is grown on top of the n^+-GaAs buffer to lay down the lattice constant for the structure above. A strained-layer dislocation filter of InGaAs-GaAs superlattice is included to reduce threading dislocations in the upper layers. Twenty sets of undoped tensile-strained GaAs-InAlAs quantum wells are sandwiched on both sides by a 500Å undoped InAlAs spacer and then a 1μm-thick doped InAlAs clad. The structure is then capped with InGaAs with the same lattice constant as the InAlAs grid to prevent oxidation. Respective AuGe and AuZn thermal evaporation complete the n and p electrodes.

From double-crystal x-ray rocking curve diffraction, the indium content of the InAlAs layers of a grown sample is determined to be 5.1% and thickness of the GaAs wells and InAlAs barriers are 74.0Å and 47.8Å respectively. A double peak structure at the absorption bandedge of the room temperature photocurrent spectra indicates the heavy and light hole peaks are still slightly separated in this quantum well structure. Waveguide absorption measurement is also carried out and the variation of output power of a 410μm-long planar waveguide sample relative to that at zero bias with applied voltage at a wavelength of 860nm is shown in Fig. 6. It can be seen that the TE and TM polarization dependence of the optical absorption is small and a relative output power of -4dB is achieved with -5V. Presently, efforts are being made to improve the

performance of the device.

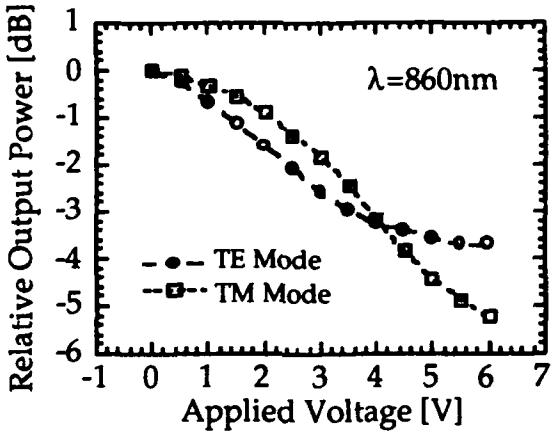

Figure 6 Variation of relative output power of tensile-strained GaAs-InAlAs quantum well waveguide with reverse bias for a waveguide of 860nm.

4. Conclusion

Tensile-strained GaAs quantum wells are experimentally realized on a GaAs substrate by laying down a thick non-pseudomorphic InAlAs grid layer and also inserting an InGaAs-GaAs strained-layer superlattice dislocation filter structure. Photoluminescence measurements confirmed the presence of tensile strain in the quantum wells.

The field-induced optical effects of tensile-strained GaAs-InAlAs quantum wells are studied theoretically and experimentally. Minimal polarization dependence of optical absorption is also demonstrated with a planar waveguide structure comprising InAlAs grid and clad layers and GaAs-InAlAs quantum wells waveguide layer.

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Lossless and Low Crosstalk InP Based 2 X 2 Optical Switch With Integrated Optical Amplifier

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1. Introduction

Photonic space division switching networks are one of the most promising switching systems. In designing such a network on a large scale, C.Burke et al. proposed and demonstrated that use of semiconductor optical amplifiers could reduce optical switch loss[1]. A lossless optical switch unit is most desirable for large scale photonic networks because it enables us to enlarge the network without being concerned about optical loss.

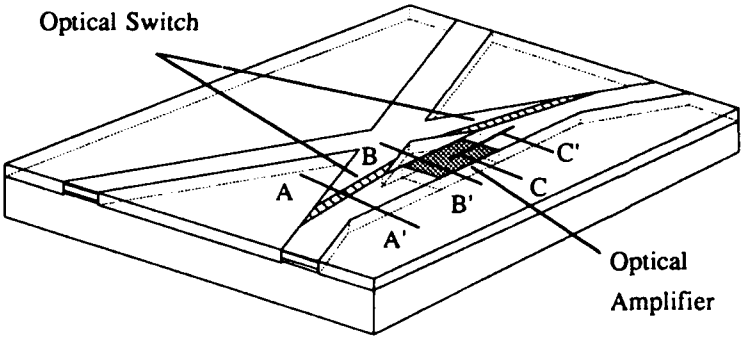
As a means of achieving a lossless optical switch, the integrated semiconductor optical amplifier gate switch has been gaining interest in recent years[2][3][4]. We proposed a carrier-injection type optical single-slip structure (S^3) switch with traveling-wave amplifier (COSTA)[5][6]. The traveling-wave amplifier (TWA) is integrated into a carrier-injection type S^3 switch. This structure can compensate for insertion loss and improve the ON/OFF ratio. Compared with amplifier gate switches, the features of COSTA facilitate the expansion of a switching matrix using a crossbar configuration. The crossbar configuration is most preferable for large scale photonic networks because it is strictly non-blocking and it is easy to arrange the switching pass.

In this paper, we present a 2 X 2 InP/InGaAsP carrier-injection type optical S^3 switch with traveling-wave amplifiers. Fiber to fiber insertion loss of 0dB and low crosstalk (an ON/OFF ratio as high as 40dB) are demonstrated.

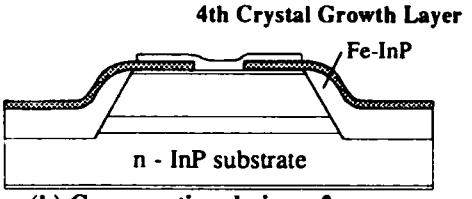
2. Device Structure and Fabrication Procedures

A schematic view of a COSTA as a unit cell is shown in Fig. 1(a). The cell consists of an X-crossing waveguide, two Y-branch switches and an amplifier. The X-crossing angle is 10° and Y-branch angle is 5°. The carrier injection region of the switch, using a grown junction suitable for integration[7], is shown in Fig. 1(b). The integrated TWA has an Fe-doped semi-insulating current blocking layer, shown in Fig. 1(c). A butt coupling structure was adopted for coupling the passive waveguide and the TWA because this allows us to optimize the structures of both the switch and the TWA. It was also expected that coupling efficiency at the interface would be improved.

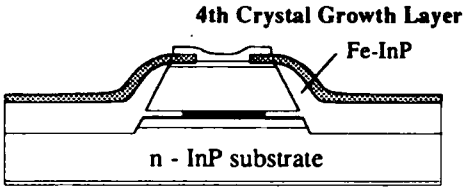
The fabrication procedures are as follows. First, four layers for the amplifier structure were successively grown on an n-type InP substrate using low pressure MOVPE. These layers consisted of an InGaAsP waveguide layer (0.3μm thick, λg=1.15μm, n=2X10^{16}), an InP stop etch layer (0.05μm thick, n=2X10^{17}), an InGaAsP active layer (0.15μm thick, λg=1.3μm, n=2X10^{16}) and an InP cladding layer (1.2μm thick, p=8X10^{17}). Next, an InGaAsP waveguide layer (0.4μm thick, λg=1.15μm, n=2X10^{16}) and an InP cladding layer (0.8μm thick, p=8X10^{17}) were selectively grown to form the passive waveguide and switch structures using a SiO_2 mask to cover the amplifier region, after selectively etching off the upper three layers. After the SiO_2 mask was removed, an InGaAsP cap layer was grown over the entire surface. Then, ridge waveguides 5μm wide and 2.2μm high were formed using reactive ion etching (Cl_2). In the fourth crystal-growth step, an Fe-doped semi-insulating InP layer was selectively grown to embed the waveguides, after reducing the active layer width to about 3μm by selective chemical etching. Finally, the p-side and n-side electrodes were made. The input and output facets were made by cleaving and a SiNx layer was deposited as an anti-reflection (AR) coating.



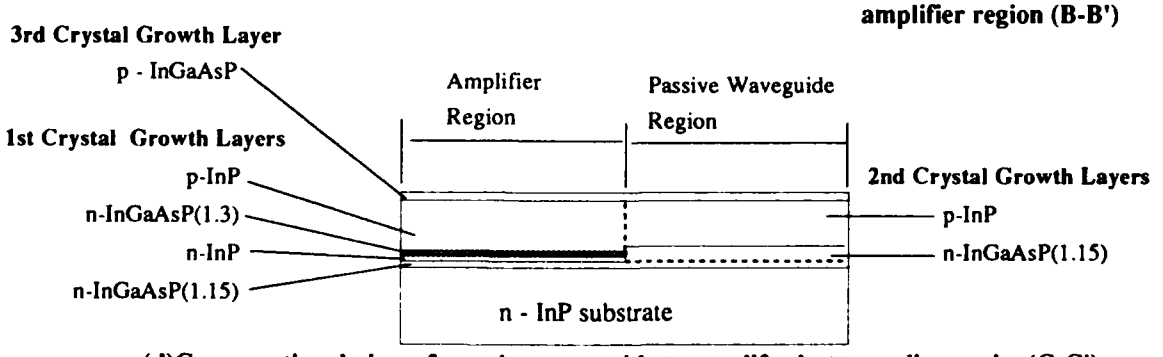
(a)Schematic view of a COSTA as a unit cell



(b) Cross-sectional view of switch region (A-A')



(c) Cross-sectional view of amplifier region (B-B')



(d)Cross-sectional view of passive waveguide to amplifer butt coupling region(C-C')

Fig. 1. Schematic view of a COSTA and cross-sectional views of each region

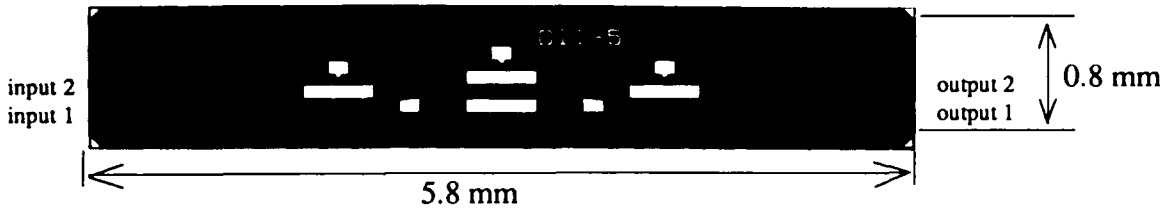


Fig. 2. Top view photograph of a 2 X 2 COSTA

A top view photograph of a 2 X 2 COSTA is shown in Fig. 2. It consists of 4 amplifiers and 8 Y-branch optical switches. The amplifier length is 500μm. The chip is 0.8mm wide and 5.8mm long, almost the same size as the original unit cell without the amplifier[8].

3. Results

First, the performance of the integrated amplifier was examined. The I-L characteristics of the COSTA are shown in Fig.3. Current was injected into only the amplifier. The integrated amplifier displayed good performance, as demonstrated by the threshold current of 85mA, despite the great loss in the laser cavity. The above threshold current was measured with the two Y-branch optical switches being in the off state. (An identical amplifier, left as a cleaved device, on the same wafer showed a threshold current of 30mA.) After AR coating was carried out, lasing of the COSTA was suppressed and it showed superlinear I-L characteristics like a semiconductor amplifier. This shows that lasing of the COSTA as cleaved occurred in the cavity formed by the input and output facets.

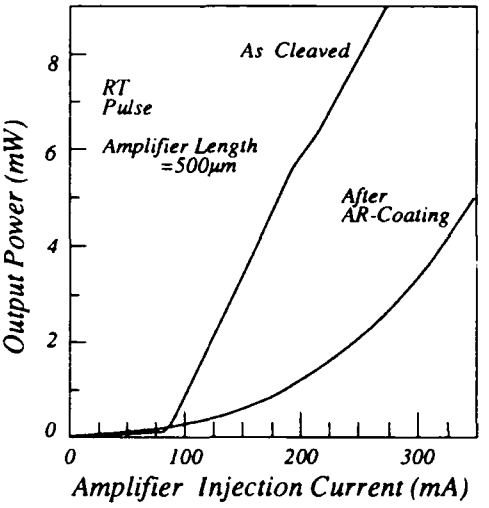


Fig. 3. COSTA I-L characteristics

A plot of the output power as a function of the current on the switch is shown in Fig. 4, with the amplifier current held constant. The output power shown along the vertical axis was normalized against the input light power. The examined switch port was one of the four switch ports, CH12, the port from input 1 to output 2, as shown in Fig. 2. A DFB laser diode (λ=1.30μm) was used as the input light source. Both input and output

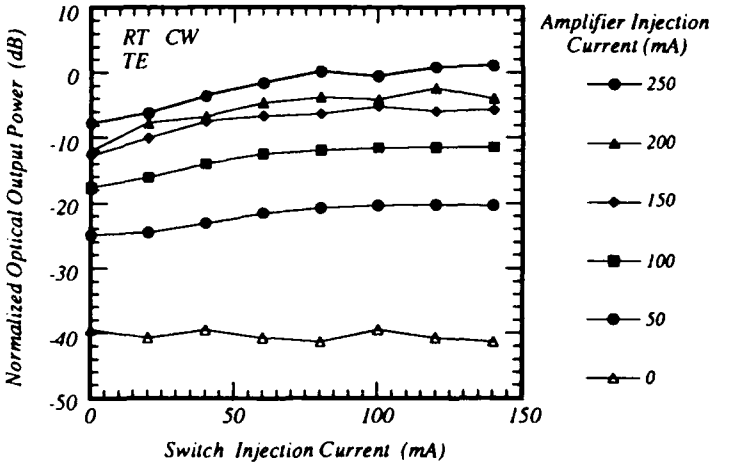


Fig. 4. COSTA switching characteristics of (CH12)

waveguide facets were coupled with spherical lensed (R=12μm) single mode fibers. A 0dB fiber to fiber insertion loss was attained with the switch injection current at 80mA and the amplifier injection current at 250mA. When the switch current was increased to 140mA, a maximum gain of 1dB was obtained. The ON/OFF ratio is defined as the output power difference between two states where both the switch and amplifier are simultaneously either on or off. The ON/OFF ratio of the switch was 40dB. We had never obtained such a high ON/OFF ratio with an original carrier-injection type optical switch[6] without integrating amplifier. Thus, we demonstrate lossless operation and low crosstalk (40dB ON/OFF ratio) as a part of the COSTA capability.

The loss and the gain factors of the device examined are analyzed as follows. The loss in the COSTA can be decomposed into five factors. The propagation loss and the fiber to waveguide coupling loss were 1.2dB/mm and 3.1dB/facet, respectively, as estimated from a cut back measurement of straight waveguides. The propagation loss can be easily reduced to 1/3 or less by optimizing the passive waveguide structure. The switching loss and bending loss were 2.7dB and 3.4dB, respectively, as estimated from the characteristics of the switch without an amplifier. The estimated butt coupling loss was 2.7dB/facet. That loss is almost 3 times as large as the calculated value. However, it can be reduced by improving the fabrication process. To compensate for all these losses, an amplifier gain of 24dB is required. The above mentioned loss improvements should drastically lower the amplifier current because a gain of 24dB is attained in the gain-saturation region of the current-versus-gain characteristics. Moreover, this will allow the size of the lossless matrix to expand to larger than a 4 X 4 matrix.

4. Conclusion

We demonstrated 0dB fiber to fiber insertion loss and low crosstalk (40dB ON/OFF ratio) with a 2 X 2 carrier-injection type optical S^3 switch with traveling-wave amplifiers.

Acknowledgments

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Monolithic Integration of Quantum Well Optical Waveguides with Heterojunction Bipolar Electronics for Wavelength Switching

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Most near-term photonic switching systems exploit optical devices for their large bandwidth but still require electronics for memory, logic, and control functions. Hence there is great interest in monolithically integrating electronics and photonics[1,2]. For example, packet header interpretation and routing can be acheived with an optoelectronic circuit consisting of integrated photodetector, transistor electronics, and space-division switches. If, as an overlay to the space-division fabric, wavelength division multiplexing (WDM) is used, then switching capacity can be tremendously increased. Even greater WDM network flexiblity is attained if there is some means for channel reuse such as wavelength conversion.

In this paper, we demonstrate the monolithic integration of a heterojunction bipolar transistor (HBT) electronic circuit with a high-efficiency space-division switching fabric, InGaAs/InP quantum wells[3].The InGaAs/InP HBT wafer structure used here has previously shown high-speed capability[4] and can be applied to diverse photonic switching circuits such as switch drivers and packet header readers. In the current implementation, we apply this technology to a transimpedance amplifier circuit[4] for wavelength translation . As shown in Fig.1, the control signal is read by a p-i-n quantum well waveguide. Photocurrent thus generated is fed to the input of the amplifier, which drives the second quantum well waveguide modulator. With input optical control power from semiconductor diode lasers (~ 1 mW) we obtain modulating voltages at the output V_O on the order of volts and modulation of the signal beam for a wide range of wavelengths λ_{signal} from 1.54 to 1.59 μm.

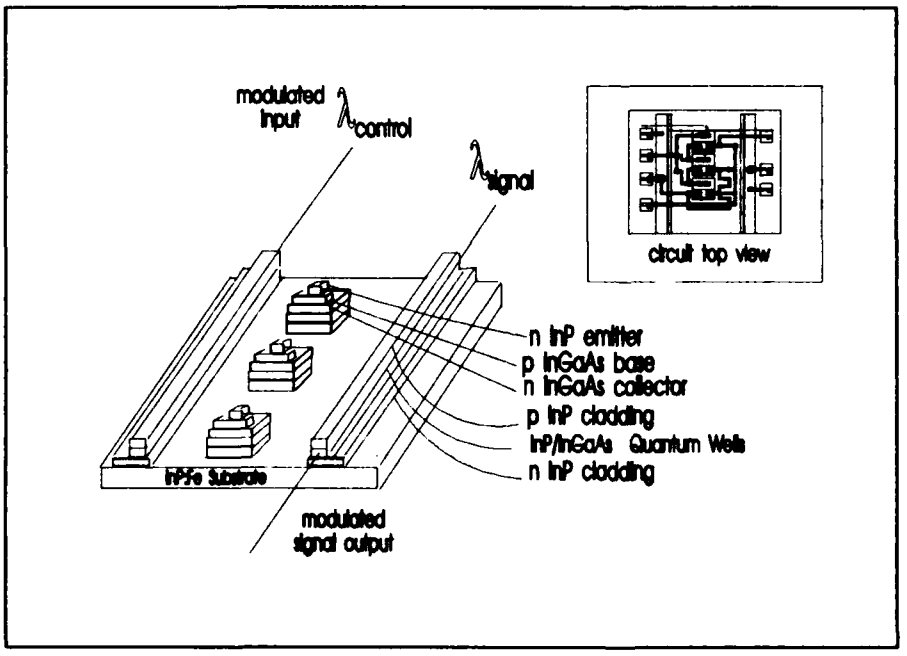

Fig.1 Schematic of monolithically integrated quantum well p-i-n waveguide photodetector, heterojunction bipolar transistor transimpedance amplifier, and quantum well p-i-n waveguide modulator. Current generated by the control beam in the first waveguide stage is transformed by the electronic circuit to a voltage which drives the second waveguide stage. Modulation at wavelength $\lambda_{control}$ is thus converted to wavelength λ_{signal}.

Atmospheric pressure MOVPE at 650 C is used to grow the base wafer with HBT layers above the quantum well p-i-n, separated by a 200 Å thick InP stop etch layer. The p-i-n layers consist of 20 periods of undoped 40 Å InGaAs quantum wells with 40 Å InP barriers on n-InP, covered with 1.69 μm thick p-InP cladding and a 1500 A p^+-InGaAsP top contact layer. The composite collector consists of a 6300 Å thick InGaAs subcollector is followed by 4000 Å InP, 100 Å 1.42-μm-composition InGaAsP and 3400 Å InGaAs.Then the base is 300 Å p+ InGaAs . The 2100 Å thick InP emitter is followed by a 2500 Å n^+InGaAs cap. N-type and p-type dopants are sulphur and zinc.

The total size of the chip is ~ 600X600 μm^2 including the central electronic circuit,the 7.5 μm wide p-i-n rib waveguide detector and modulator, and seven 60X60 μm^2 contact pads for supply voltages and diagnostics. Wet etching is used to form the three HBTs which have 25X25 μm^2 emitters. Then the rib waveguides are dry-etched with methane hydrogen, and the bottom n-type contact area is defined by wet-etching into the semiinsulating substrate. NiCr resistors are evaporated directly onto the substrate. After evaporation of n- and p-type contacts, polyimide is spun on and vias are wet-etched to allow interconnection between the levels. From the bottom resistor level to the uppermost contact on the emitter, there is a difference in height of 4.65 μm.

Before dicing, the wafer is characterised by measuring the reverse bias characteristics of the two p-i-ns and the transimpedance of the circuit, here 1 kΩ. Chips are mounted on copper studs with light coupled in and out of the cleaved faces using 40 X microscope objectives. For the control laser, we used semiconductor laser diodes with output powers ~1 mW with modulation imposed by a mechanical chopper. The wavelength-tunable cw signal input was provided by a color center laser at power of 3 mW.Since both control and signal beam are focussed by the same objective, the coupling efficiency is somewhat limited by chromatic dispersion. Nevertheless, as shown in Fig.2, 1.1 mW input at 1.544 μm produces enough photocurrent to create a V_O=1.5 V swing at the output of the amplifier.

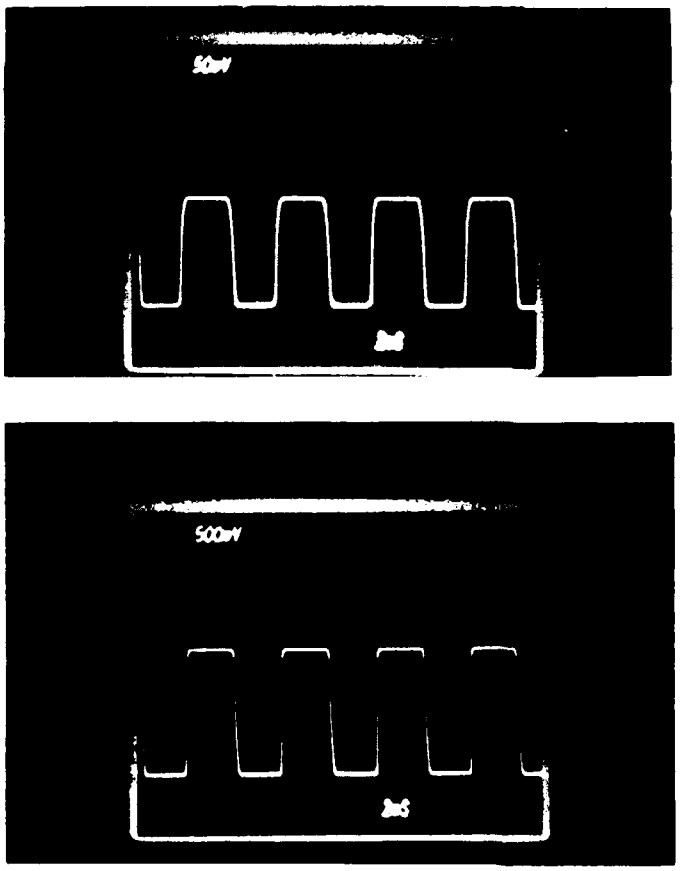

Fig.2 Oscilloscope traces of (top) optical input control power measured on a photodiode and (bottom) electrical output voltage from the transimpedance amplifier V_0 . Control wavelength is 1.544 μm and incident control power is 1.1 mW. Collector supply voltage V_{cc} and reverse bias on detector waveguide V_D are 4V.

The use of quantum wells in the waveguide photodetector and intensity modulator introduces wavelength and polarization dependence for the wavelength translation function.This is shown in Fig.3, where we plot the relative modulation depth impressed on the signal beam by the control beam as a function of signal wavelength.

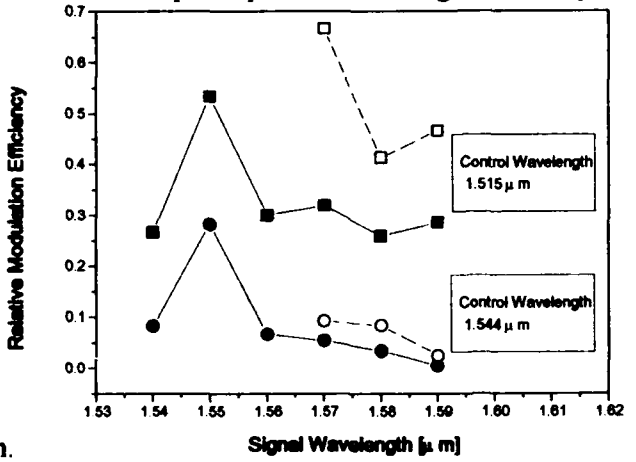

Fig.3 Modulation of the signal wavelength by the control beam for two different control wavelengths, 1.515 (squares) and 1.544 μm (circles) as a function of the signal wavelength. Open symbols are for TE polarization, solid for TM. Input optical control power, supplied by semiconductor diode lasers, is ≤1 mW.

Here the output waveguide modulator stage is reverse-biased at V_1=5 V, so that the absorption edge of the quantum wells is red-shifted from its zero field position, 1.4995 μm. The maximum intensity modulation of the signal occurs just below the absorption edge near λ_{signal}=1.55 μm, and falls off with increasing wavelength.Since the absorption of the quantum wells rises sharply at shorter wavelengths, the wavelength conversion efficiency is nearly twice as high at control wavelength $\lambda_{control}$=1.515 μm than at $\lambda_{control}$=1.544 μm. In fact, since there is ample photoresponse from the quantum wells at 1.3 μm, this same circuit could be used to translate from 1.3 to 1.55 μm[5] or might be employed in a packet switching scheme in which 1.3 μm is used as the header for 1.55 μm data. In addition, we see that the built-in optical ansiotropy of the quantum wells provides the expected polarization dependence, with responsivity greater for TE than for TM polarization. For simplicity in developing our fabrication sequence, we here used a quantum well electroabsorption modulator as the output stage. However, we note that significantly less signal wavelength sensitivity would be obtained with a quantum well electrorefractive modulator[6], and the polarization-dependence could be minimized by using strained quantum wells[7].

In summary, we have demonstrated process compatibilty for InGaAs/InP HBTs and quantum well p-i-n waveguide devices in a simple prototype circuit for wavelength conversion. With standard semiconductor laser diode input, the present circuit design[4] with 1 kΩ transimpedance provides output voltages on the order of 1 V, enough to drive high-performance quantum well switches and modulators.Although the design rules used here for the HBTs are modest, smaller emitter devices on similar wafers have performed at multigigabit data rates.Therefore this scheme ultimately promises higher speeds than wavelength converters based on semiconductor lasers or laser amplifiers.

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Functional Photonic Switching Device by Vertical and Direct Integration of Six Heterojunction Phototransistors and Two Laser Diodes

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I. INTRODUCTION

Much interest has been emerging in optical signal processing and optical computing. In these fields, various functional devices are greatly demanded. A vertical and direct integration of a light-receiving device and a light-emitting device is an attractive method to achieve these functional devices [1-5]. The integrated device exhibits not only the simple combined characteristics of constituent devices but also the more elevated characteristics due to their internal optical couplings. For example, the integrated device composed of four heterojunction phototransistors (HPTs) and one laser diode (LD) offers the functions of light-controlled optical bistability, light-controlled optical thresholding, and optical tristability [6].

In this work, we have developed a vertically and directly integrated photonic switching device composed of six HPTs and two LDs to achieve more elaborated functions. The switching device shows the optically-controlled multilevel latch and erase function and the optically-controlled multilevel flip-flop function. In the following, the device structure, the fabrication, and the characteristics are described.

II. DEVICE STRUCTURE AND FABRICATION

Figure 1 shows the schematic structure of the device developed in this work. In the device, six HPTs are integrated vertically and directly on two LDs. Among six HPTs, the HPT-A and the HPT-B are integrated just above the LD1, and the HPT-E and the HPT-F are integrated just above the LD2. The HPT-C and the HPT-D are integrated on the position between the LD1 and the LD2.

The device wafer was grown by three-step liquid phase epitaxy (LPE). The p-n-p InP current blocking layers were grown on p^+-InP substrate at the first LPE. After the formation of the grooves with 1.5μm width and 300μm separation, p-InP clad, undoped-InGaAsP active, n-InP clad, and n-InGaAsP optical absorptive layers were grown at the second LPE. A stripe geometry LD was grown by these growth processes. The HPT composed of n-InGaAsP optical absorptive, n-InP collector, p-InGaAsP base, and n-InP emitter layers was grown at the third LPE. Then, a square-shaped AuGe-Ni-Au electrode was deposited on the epilayer side, and the wafer was mesa-etched to form six HPTs. The peripheries of the HPTs were coated with a polyimide film to avoid the leakage current due to the formation of the surface states. An AuZn-Au electrode was deposited on the back side, and the wafer was cleaved and bonded on a silver heat sink. The dimension of each HPT mesa was $120\times100\mu m^2$, and the cavity length of the LD was 400μm.

III. CHARACTERISTICS

3-1. Optically-Controlled Multilevel Latch and Erase Function

The optically-controlled latch and erase functions in a switching device are considered very important for various optical signal processing systems. The device fabricated in this work showed the optical latch and erase functions not only in bistable and tristable states but also in tetrastable states.

The equivalent circuit for the tetrastable states latch and erase functions is shown in Fig.2. For the latch operation, the HPT-A, the HPT-B, the HPT-E, the LD1, and the LD2 were utilized. The optical input from an external light source is injected only to the HPT-A. Since the HPT-A and the HPT-B are optically connected through the LD1, the HPT-B can be controlled also by the optical input to the HPT-A. The LD1 and the LD2 are connected in parallel via the thin cladding layer, a part of the current flowing from the HPT-A (or HPT-B) to the LD1 is injected to the LD2. In this case, since the HPT-E is integrated just above the LD2, the light emitted from the LD2 is injected to the HPT-E. Therefore, the input light to the HPT-A can also control the HPT-E. By using these optical and electrical couplings inside the device, the latch operation in tetrastable states becomes possible: when the optical input P_A to the HPT-A exceeds a threshold level, the HPT-A + LD1 part turns to the on-state due to the optical feedback from the LD1 to the HPT-A. When P_A is increased, the optical input to the HPT-B from the HPT-A + LD1 part through the LD1 is increased, and the HPT-B + LD1 part also turns to the on-state. When P_A is increased further, the optical incidence to the HPT-E from the LD2 which is activated by a part of the current through the HPT-A + LD1 part is also increased, and finally the HPT-E + LD2 part turns to the on state.

On the other hand, the erase function is achieved by using the HPT-C (or HPT-D) additionally. Since the HPT-C is shifted away from the LD1 and the LD2, it is not affected by the optical feedback. As seen in Fig.2, the HPT-C is connected in parallel to the LD1 and the LD2, and is biased by the voltage drop. When the optical input is injected to the HPT-C, the current flowing through the LD2 and the LD1 is bypassed through the HPT-C. As a result, the optical feedback from the LD2 to the HPT-E is decreased and the HPT-E + LD2 part turns to the off-state. When the optical input the HPT-C is increased further, the optical feedback from the LD1 to the HPT-B and to the HPT-A is also decreased, and the HPT-B + LD1 part and the HPT-A + LD1 part turn to the off-state sequentially.

The resultant latch and erase operations in tetrastable states is shown in Fig.3, where the output power is the total one emitted from both of LD1 and LD2. If we want to have only one output, it is possible to use a Y-junction LD with two wings instead of two LDs. In the same manner, the latch and erase functions in bistable and tristable states have been achieved by using the HPT-A + LD1 + HPT-C and the HPT-A + HPT-B + LD1 + HPT-C parts, respectively.

3-2. Optically-Controlled Multilevel Flip-Flop Function

Since the device developed in this work has two output portions, it is interesting to switch the output from the LD1 to the LD2 or from the LD2 to the LD1 by the optical input. This function is so called set-reset flip-flop. Here, we consider the case of the simultaneous utilization of the HPT-A + LD1 and the HPT-E + LD2 for this function. Figure 4 shows the equivalent circuit, where each part is biased through the common load resistance R_c. In the

figure, the LD1 and the LD2 are connected by the resistance which is shown by the broken line. For this function, the resistance should be as small as possible to avoid the mutual interaction. This can be achieved by deep mesa etching of the HPT parts. When the optical input is incident only to the HPT-A + LD1, this part is latched to the on-state due to the optical feedback. In this case, the HPT-E + LD2 part is maintained to the off state but the voltage at the both ends is made small V_{A1}, which is equal to the voltage at the both ends of the HPT-A + LD1 part at the on-state. When the optical input is incident to the HPT-E + LD2 part, a current flowing through the HPT-A + LD1 part start to flow through the HPT-E + LD2 part, since the HPT-E has enough gain at the voltage V_{A1}. The reduction of the current through the HPT-A + LD1 part decreases the optical feedback from the LD1 to the HPT-A and finally the HPT-A + LD1 part looses the optical feedback enough to maintain the on-state. On the other hand, the increase of the current through the HPT-E + LD2 induces optical feedback enough to let this part switch on. Therefore, the state becomes reverse, that is, the HPT-A + LD1 turns to the off-state and the HPT-E + LD2 turns to the on-state. Figure 5 shows the resultant bistable set-reset flip-flop operation. We can see that the output has been alternately switched [(P_{LD1},P_{LD2}): $(1,0)\rightleftarrows(0,1)$] by the alternate optical input to the HPT-E and to the HPT-A.

This function has been extended to the set-reset flip-flop operation in tristable states by using the other HPTs (the HPT-B and the HPT-F) additionally. In this case, the equivalent circuit becomes as shown in Fig.6. Where the HPT-A and the HPT-F are biased through a common load resistance R_{c1} and the HPT-B and the HPT-E are biased through a common load resistance R_{c2}. The optical input is incident to the HPT-A or the HPT-E. By utilizing the optical couplings inside the device, the tristable logic set-reset flip-flop operation [(P_{LD1},P_{LD2}): $(2,0)\rightleftarrows(1,1)\rightleftarrows(0,2)$] has been achieved. The detail will be reported at the conference.

IV. SUMMARY

We have developed vertically and directly integrated photonic switching device composed of six HPTs and two LDs. It has been demonstrated that the device has the multilevel latch and erase functions not only in bistable and tristable states but also in tetrastable states by using optical and electrical couplings inside the device. It has been also demonstrated that the device has the bistable set-reset flip-flop function in which the output is switched alternately by changing the input portion. Moreover, the result has been extended to the tristable set-reset flip-flop function by using multiple HPTs and their internal optical couplings. Although it has not been described here, the device has the other attractive functions such as optical amplification and the optical thresholding. Therefore, this device would be considered to become a key device for the future optical signal processing and optical computing.

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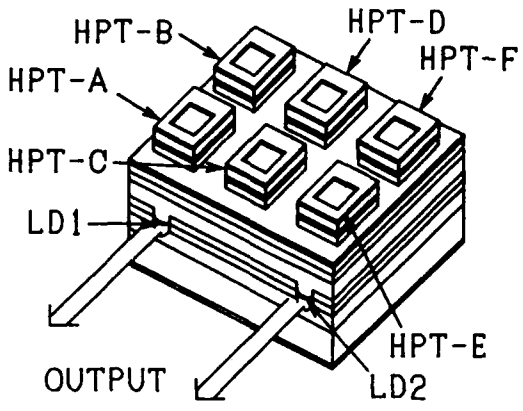

Fig.1 Integrated device structure.

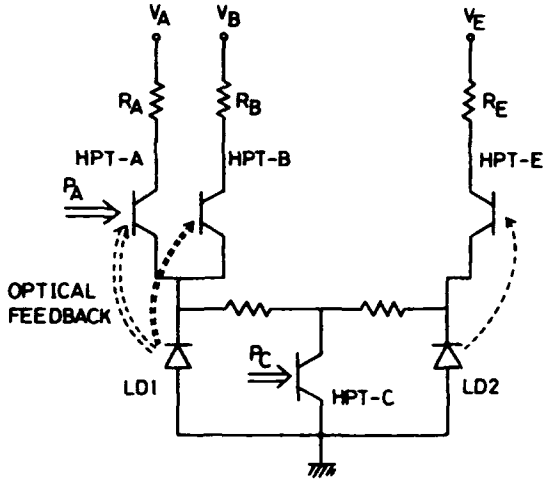

Fig.2 Equivalent circuit for tetrastable latch and erase functions.

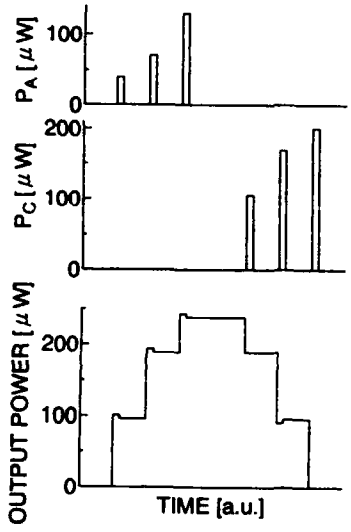

Fig.3 Latch and erase functions in tetra-stable states.

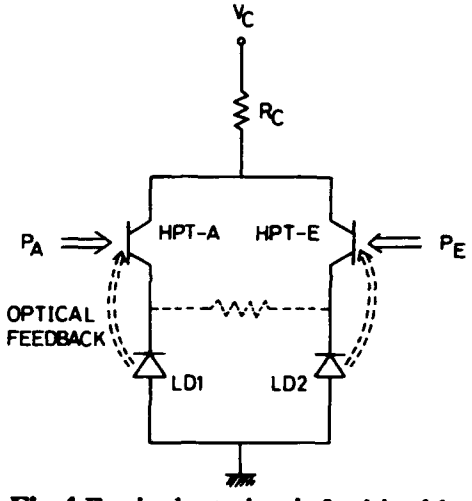

Fig.4 Equivalent circuit for bistable set-reset flip-flop function.

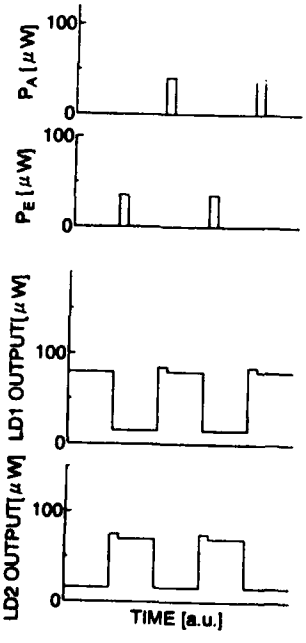

Fig.5 Bistable set-reset flip-flop operation.

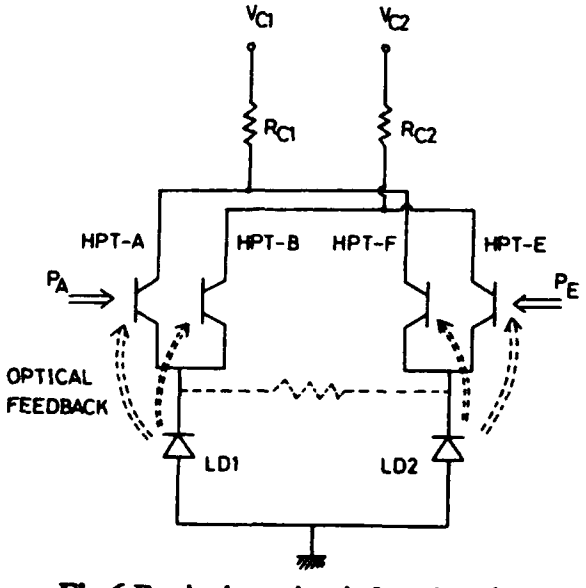

Fig.6 Equivalent circuit for tristable set-reset flip-flop function.

Smart Pixels

PMC 1:30pm-3:00pm
Grand Ballroom East

Gareth Parry, *Presider*
University College London, U.K.

Advances in SEED based free space switching systems

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One approach to increase the interconnection bandwidth between electronic integrated circuits is to interconnect these ICs using beams of light imaged on and off each chip using lenses. This technique is often called free space digital optics. The ICs themselves could be very simple, such as an array of NOR gates, or very complex, such as an array of self-routing switching nodes or other processing elements. The SEED technology, which can incorporate detectors and optical modulators along with traditional electronic components, is a leading candidate for these optically interconnected ICs.

The field of free space digital optics includes a wide variety of topics including architectures and network control strategy, optical system design, optomechanical and thermal design, laser design, and circuit and device design. Progress these areas has contributed to the advancement of free-space photonic switching system demonstrations as a whole. In this talk, I will highlight some of the advancements in these areas that have led to advancements in the free space photonics switching systems and will also discuss required advancements to achieve further progress in this area.

Architectures and Network Control Strategy

A broad class of arhitectures known as extended generalized shuffle networks [1] allows the system designer to trade-off the complexity of the switching elements or nodes, the number of stages and the number of nodes per stage. This has enabled us to design nodes, known as 2-modules, that consist of a single symmetric SEED (S-SEED) [2]. The network control strategy [3] of our demonstration systems has evolved, from using a mask to determine the routing of the data through the network [4] to direct control of the S-SEED bias [5]. A different approach to network control, called embedded control, used the data channels to load control into the switching nodes [6]. A schematic diagram of such a node is shown in Fig. 1. In one demonstration system, the control memory and the data multiplexer were implemented using S-SEEDs on three different arrays [7]. Recently, a 4 x 4 FET-SEED implementation of these nodes has been designed, built and tested [8].

Optical system design

The optical system design of the earliest demonstrations used off the shelf components. In one system, 4 x 8 arrays of devices were operated concurrently [4]. A later system still used off the shelf components, but advances were made that allowed a fourfold increase in the number of devices operating concurrently[7]. One of these advances was the use of a Plossl eyepiece that enabled the relay lenses to be constructed with less aberrations and variability in focal length.

The latest system [5] used a custom designed objective lens. All image planes other than at the devices themselves were eliminated, further reducing the accumulation of optical aberrations and also increasing mechanical stability. This was accomplished by using 50/50 beam splitters to combine the clock and signal beams instead of arrays of patterned mirrors. Also, the prismatic mirror arrays and the optical isolator (beam splitter and waveplates) in the crossover interconnection optics were replaced by a single transmissive binary phase grating implementing a banyan interconnection. These gratings required suppressed orders internal to the array to ensure that unwanted signals were not incident on the S-SEED windows. Significant efforts in building characterization systems allowed the optical components to be thoroughly characterized [22]. These improvements allowed arrays of up to 2048 S-SEEDs to be cascaded [18].

Opto-mechanical design

In the earliest switching system demonstrations [4, 7] there were many adjustments. Because these adjustments can lead to mechanical instability, the latest system [5] incorporated few adjustments, but required greater precision in the individual components. More importantly, the remaining adjustments were not under tension. One example of this was the S-SEED mounts. Instead of the usual 6 axis positioner that is generally required, the S-SEEDs were mounted on a steel cylinder which, along with the lenses and other components, was positioned in a machined slot. The cylinder was ground at an angle to match any tilt in the S-SEED array (after it was mounted to a hybrid IC.) eliminating tilt adjustments. The array was centered to within ~ 20 μm in the x-y directions, and, instead of moving the S-SEEDs, the array of beams were positioned on the S-SEEDs using a pair of 7 minute (~1/9 degree) wedges. The rotation of the device array and the focus of the array were done by hand. The latest system [5] was also maintained at a

constant temperature. This allowed the operating characteristics of the devices to be adjusted and maintained, and provided greater mechanical stability.

Laser power supply

One area of improvement of the laser power supplies has been that the wavefront quality coming from the lasers and collimating optics is now well corrected. The amount of power has also increased, although only moderately from ~30 mW to ~75 mW. One problem in our latest system was laser wavelength stability. Because diffractive optics are used to generate arrays of spots, a shift in wavelength causes a misalignment of the spots on the device windows. Recently, a "laser pen" has been built using an external grating that provides excellent wavelength stability [10].

Circuit and device design.

There has been an evolution in SEEDs occurring in the last few years as well [11]. We have seen the devices change from simple bistable devices to large arrays of simple devices such as S-SEEDs, to larger arrays of more functionally enhanced devices such as L-SEED optical switching nodes, and finally to arrays of devices incorporating field effect transistors and quantum well detectors and modulators (FET-SEEDs). Most of the experiments to date have been with the relatively simple S-SEEDs. One simple advancement in the area of S-SEEDs was to incorporate arbitrary window sizes and shapes. This was key in allowing a 1 x 3 binary phase grating to implement a banyan interconnection [5]. We have also used integrated L-SEED 2 x 1 switching nodes in a system demonstration [12].

One of the more exciting advancements in SEEDs is in the area of smart pixels. The integration of GaAs field effect transistors and quantum well detectors and modulators opens up new possibilities for photonic switching systems. We have recently made a 4 x 4 array of embedded control 2 x 1 nodes using the FET-SEED technology as shown in Fig. 2.

Systems

The advancements in the individual components have allowed photonic switching demonstration systems to be built with more features, greater stability, easier alignment, a greater number of stages, and a greater number of devices per stage. A summary of the progress in this area is shown in Table 1.

Future issues

We have seen much progress in these photonic switching networks. Advancements in the areas desribed above have enabled us to build systems with 6 device arrays having up to 8192 incident light beams and 2048 reflected outputs per array. But what is next? The FET-SEED smart pixels offer us many possibilities, but also many challenges. In addition to general issues such as cost and manufacturability, some issues relating to smart pixels include:

1) Architectures and network control strategies: FET-SEEDs offer a richer assortment of node types and control strategies. We have seen an example in the 4 x 4 array.

2) Optical system design: As the nodes become more complex, they will undoubtedly become physically larger. This requires either new approaches to the optical systems (microchannel or hybrid systems) or will require more complex lenses to image over the large array [23]. As the optical field of view increases, it is tempting to increase the optical window sizes to ease the design. However, the relationship between window sizes and energies is not clear and any increase in window sizes will cause a larger power dissipation.

3) Optomechanics and thermal design: The 4 x 4 arrays of nodes dissipate from 2 to 10 mW per node. For 1000 nodes this can approach 10 W. The problem of heat removal is somewhat more stringent than an electronic system, because of the temperature dependence of the excitonic peak.

4) Laser system design: For projections of 20 fJ switching energies, 17 dB optical losses, 2048 differential signals and 1 ns switching times, a 4W laser would be required. It is imperative that re-timing is done at every stage in the network to compensate for variable delays in the node receivers. Short pulses may be able to reduce the required optical energies compared to 50 percent duty cycle pulses. Other issues include the need for better wavelength stability (because of the increased field of view) and the desire for multiple lasers per stage.

5) Circuit and device design: While the design space for diode-only smart pixels (S-SEEDs, L-SEEDs etc.) is fairly well understood, the design space for FET-SEEDs is not understood as well. Designs must minimize both power dissipation and complexity. Uniformity and yield of the device arrays are other issues.

6) Testing: Both system and SEED testing becomes much more difficult as the devices become complex. For S-SEEDs, a simple forward bias test ensured operation and the device uniformity was good enough that sample device testing was all that was required. System testing consisted of monitoring the output device array at slow speeds on a TV monitor. As a simple example, is there a good method of ensuring that all the devices in a large array are operating at 100s of Mb/s?

Conclusion

To date, we have demonstrated large numbers of optical interconnections between SEED arrays. With the arrival of batch fabricated FET-SEEDs, we will certainly see the bit rate of these systems increase dramatically. Although the challenges are great, rapid progress in the areas outlined here is also likely to continue.

Acknowledgment

I would like to acknowledge many collaborators at AT&T Bell Laboratories listed in the references who are responsible for the advancements and ideas described here.

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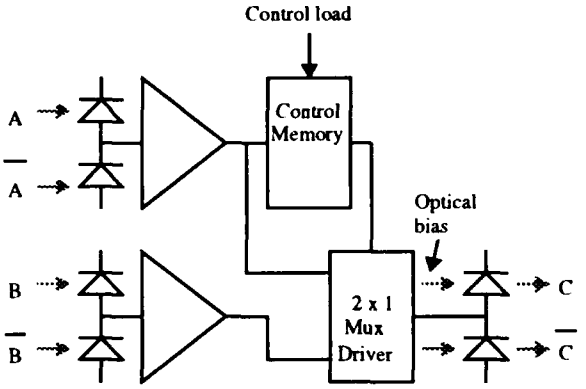

Fig. 1. Embedded control 2 x 1 node

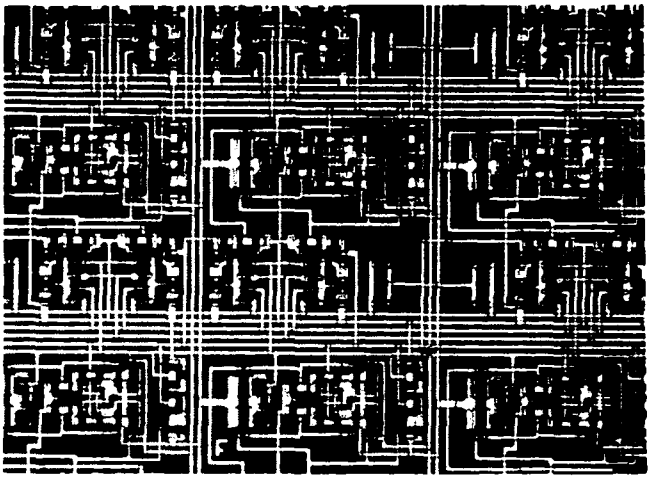

Fig. 2. FET-SEED implementation of Fig. 1.

Demonstration	year	arrays	devices/ array	device type	bit-rate	input	interconnect	comments	ref
Photonic Ring Counter	1987-1990	2	1	S-SEED latch	50 Mb/s	loop	1 to 1	w/ optical sense amplification	14,15
Shift register	1988	1	4	S-SEED latch	20 kb/s	2 laser diodes	1 to 1		16
2 x 1 nodes	1988	2	2	S-SEED logic	5 kb/s	4 laser diodes	crossover prism array	control with masks	17
system 2	1989	4	32	S-SEED latch	55 kb/s	fiber bundle	crossover prism array	control w/ mask - all inputs same	4
optical processor	1989	4	32	S-SEED latch	1 Mb/s	loop	split/shift		19
system 3	1990	3	128	S-SEED logic	33 kb/s	fiber bundle	crossover prism array	Control info. stored in 1st Array, all same	7
system 3'	1991	2	128	L-SEED 2 x 1 node	DC	S-SEED array	crossover prism array	control w/ mirror, all nodes same	12
cascaded S-SEEDs	1991	2	2048	S-SEED latch	DC	none	1 to 1	1st S-SEED set manually	18
system 4	1991	6	1024	S-SEED 2-Module	20kHz	MQW SLM	CGH Banyan	Control bias on SEED, 32 independent.	5
system 4'	1992	6	32	S-SEED 2-Module	1 Mb/s	MQW SLM	CGH Banyan	see above	5
CLIP	1992	2	128	S-SEED program. logic	DC	FLC SLM	1 x 2 CGH	Gate programmed by preset beams	20
cascaded FET-SEEDs	1992	2	128	F-SEED POET	14 Mb/s	2 laser diodes	1 to 1		21

Table 1. Free space SEED-based Systems

Single-Mesa Optical Memory and Logic Pixels for Highly Parallel Arrays

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Summary

Introduction

Optical array processors inherently take advantage of parallelism and show great promise for image/data processing or interconnection networks where electronics has been limited. In order for the optical array processors to compete with electronics, however, they must be ultra-fast (above GHz), highly parallel ($> 10^4$ pixels), or moderate in both, depending upon the application. Since an ultra-high frame rate requires careful circuit design and more electronics needs to be in corporated in each pixel, parallelism has to be trade off for speed. Arrays constructed of simple pixels, on the other hand, provide high parallelism with fairly fast speed ($1 \sim 100$ MHz), which are very suitable for image processing and some other applications.

This paper presents a new family of integrated simple pixels, which can function as optical memory and logic gates. These pixels have the following features: (a) they are optically activated, requiring no electrical pulses or complex driving circuits; (b) they have a single-mesa structure for each pixel, providing the potential of a large pixel density and very high parallelism; (c) they distinguish optical inputs by wavelength rather than by their spatial positions. This wavelength separation makes the arrays directly addressable by their optical inputs with full-frame format. These pixels can provide parallelism as high as 10^5 pixels on a chip with an area smaller than 1 cm^2 and can be operated at relatively high switching speeds, up to 10 MHz, with a switching energy below 10 pJ. Thus, an ultra-high data rate of up to 10^{12} bit per second can be expected with a power dissipation of 10 W/cm^2 for the enter array.

Device Concepts and Design

Each pixel is constructed through the vertical integration of two heterojunction phototransistors (HPTs) and a light emitting diode (LED) with only a single input window. The HPTs serves as input light detectors and the LED provides the output light. The optically absorbing base-collector regions of the two HPTs are fabricated from different bandgap materials such that the two optical inputs can be separated by wavelength. Each of the input wavelengths is chosen to lie within the spectral response range of only one of the HPTs so that the two HPTs can be activated independently.

Two types of single-mesa structures based on the above concepts have been designed as shown schematically in Fig. 1. The differences between the two are: (i) the top HPT is grown with the collector up for one (a) and with the emitter up for the other (b), (ii) the top HPT is interconnected with the lower HPT/LED pair (an optical switch) in parallel (a) and in series (b). The pixels based on the first type of structure can function as an optical set-reset memory and optical inverter or NOR gate, while those based on the second type function as an optical gated latch and an optical AND gate or NAND gate.

Experimental Results

Devices have been fabricated from layers grown by gas-source molecular beam epitaxy nominally lattice matched to a semiinsulating InP substrate. The square shape mesas were wet chemically etched. Two laser beams coupled from GaAs and InGaAsP laser diodes were directed by optical fibers onto the top of the testing device. Signals proportional to the optical inputs and output were sampled by a digitizing oscilloscope.

The experimental results showing the operation of the optical set-reset memory, optical inverter, optical gated latch, optical AND gate and NAND gate are presented in Fig. 2 to Fig. 6, respectively. Output on/off contrast ratios ranging from 6 up to over 50 have been obtained. The lowest required input power levels were below 10 μW. The preliminary results obtained from devices with relatively large mesa dimensions of 380 μm on a side, showed the operating frequencies up to 100 kHz. It is expected that by reducing the mesa size to (25 μm)^2, the frequency can be readily increased into the range of tens of MHz. The output power levels of the LED were also measured, giving a light power of 15 μW at a device current of 5 mA. By thinning and polishing the substrate, applying an antireflection coating, or forming microlenses on the device output window, the light emitting efficiency can be significantly improved. Nevertheless, the current output power level is sufficient to cascade to another stage for multiple array system construction.

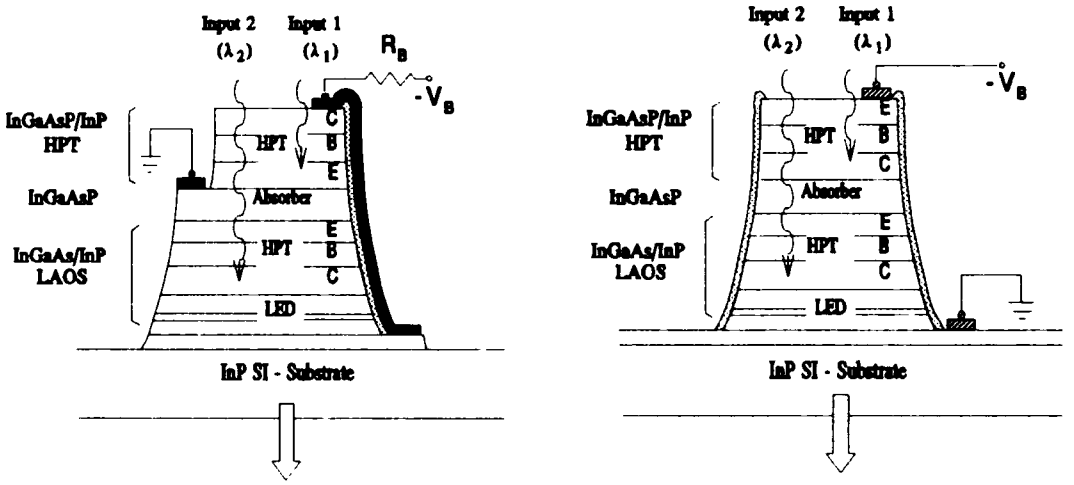

Fig. 1 Schematic device structure of single-mesa pixels : (a) with the top HPT collector up and interconnected in parallel with an optical switch (the lower HPT/LED pair, the LAOS); (b) with the top HPT emitter up and connected in series with the switch.

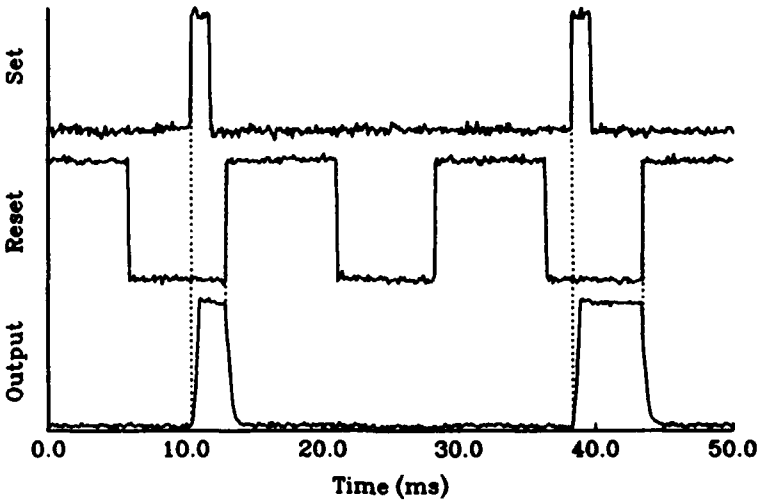

Fig. 2 Experimental demonstration of a single-mesa optical set-reset memory with oscilloscope waveforms proportional to the input and output light signals.

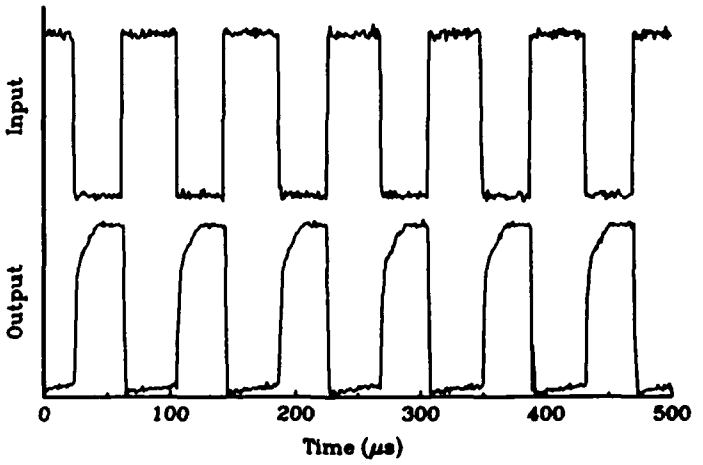

Fig. 3 Experimental demonstration of a single-mesa optical inverter with oscilloscope waveforms proportional to the input and output light signals.

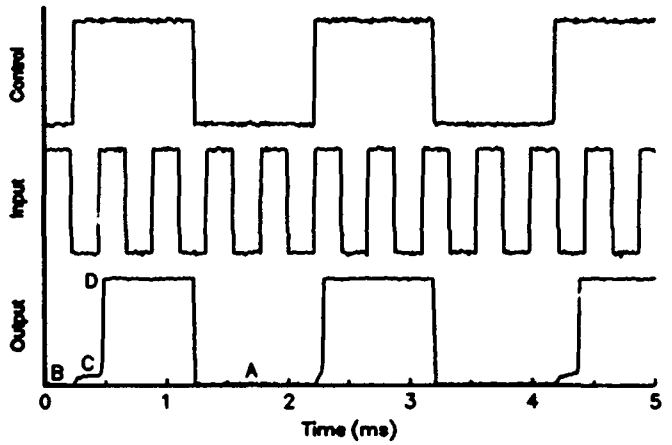

Fig. 4 Experimental demonstration of an optical gated-latch operation with oscilloscope waveforms proportional to the input and output light signals.

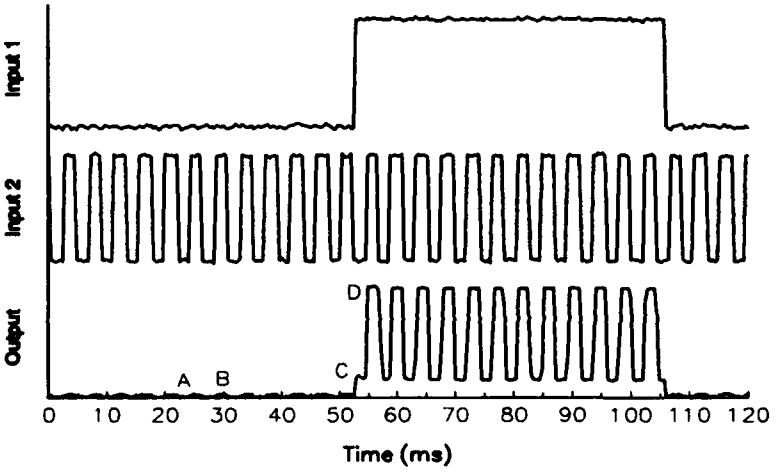

Fig. 5 Experimental demonstration of an optical AND gate operation with oscilloscope waveforms proportional to the input and output light signals.

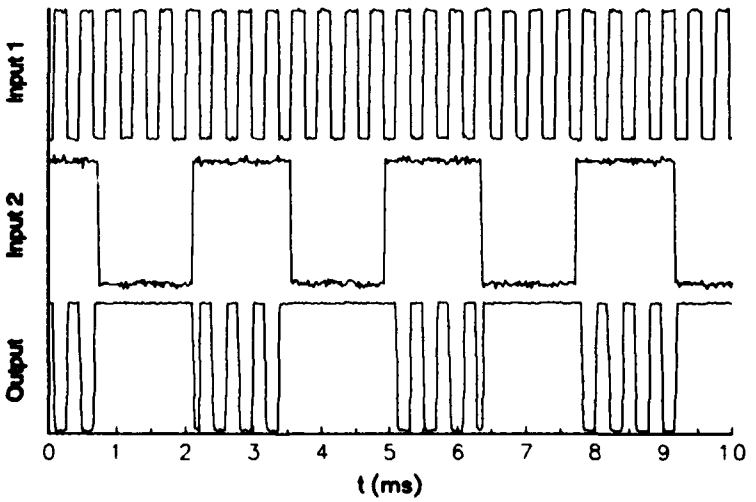

Fig. 6 Experimental demonstration of an optical NAND gate operation with oscilloscope waveforms proportional to the input and output light signals.

GaAs/AlGaAs FET-SEED Receiver/Transmitters

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A critical step toward the realization of optical interconnect between or on electronic chips at the high-density level is the monolithic combination of electronic and optical devices. Toward this end, we have pursued the monolithic integration of GaAs multiple quantum well (MQW) modulators with GaAs-based doped-channel heterostructure field-effect transistors (HFETs). Since the MQW *pin* device functions as both a modulator and a detector, its presence permits optical input and output. We refer to this integrated device structure as a field-effect transistor self-electro-optic effect device (FET-SEED). Such an approach permits the realization of complex circuits (the level of complexity being yield limited) with optical input and output anywhere on the circuit.[1, 2, 3] We have previously described the structure and fabrication of these devices.[1, 3]

Two basic elements of these opto-electronic integrated circuits (OEICs) are the receiver and the transmitter. The simplest method for testing such elements is to connect them together electrical and test the resulting circuit optically, which avoids high speed electrically signalling to the test chip. Alternately, circuits may be tested independently. A basic receiver/transmitter circuit is depicted in Fig.1. Diode elements of this circuit are *pin* MQW diodes, which function as detectors and as output modulators. The transistors are 8 and 10 μm wide FETs for the first and second stage, respectively.

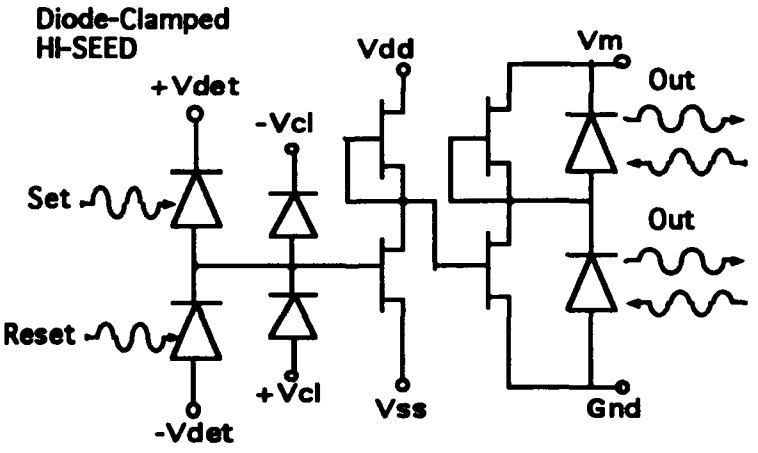

Figure 1: Basic FET-SEED receiver/transmitter.

Basic circuit operation has been explained elsewhere.[4] Briefly, the receiver consists of two input detector diodes and a single gain stage. Light falling on these detectors alternately turns on and off the transistor, depending upon whether it falls on the Set or the Reset input diode. Also connected to gain stage are two 'clamping' diodes, whose purpose is to restrict the voltage excursion of the input FET.[5] The output

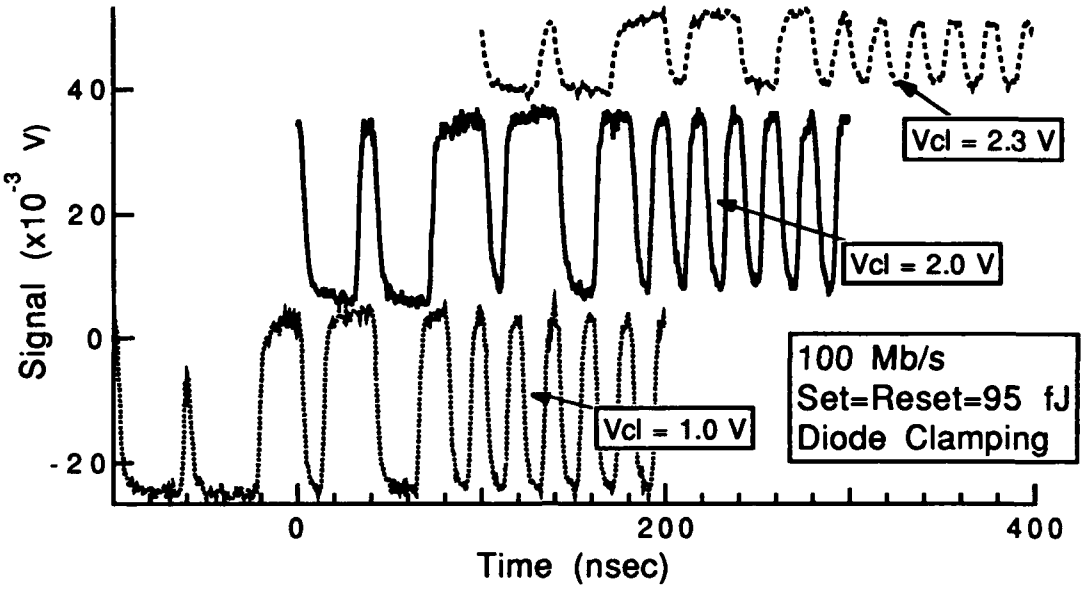

Figure 2: HI-SEED receiver/transmitter output characteristics at 95 fJ input energy for various clamping voltages. Curves have been intentionally offset from one another.

transmitter consists simply of two modulator diodes connected across a HFET output stage. We focus in this abstract on this circuit, although a number of others have been designed and realized.

The utility of the clamping diodes is most clearly evidenced when non-return-to-zero (NRZ) data is supplied to the receiver/transmitter. When 50 % duty cycle laser pulses are supplied to the device, the energies of the two beams can be balanced such that the gate voltage of the input FET does not extend any further than needed to switch the circuit. This 'push-pull' operation is desirable, since the optical energy required for a given voltage swing ΔV is simply $C_{in}\Delta V/S$, where C_{in} is the input capacitance and S is the diode responsivity in A/W. Since the leakage currents of these diodes are low, a string of Set pulses will *overdrive* the input to voltages in excess of that required for switching. If this is followed by a pulse to the Reset diode, the output may not switch completely, resulting in a *pattern dependence* to the receiver/transmitter performance. With clamping diodes, this can be eliminated, because excursions of the input gate voltage to higher or lower values are eliminated by forward conduction through the clamping diodes. For example, if the clamping diodes are biased forward to +2.0 V across the pair, both diodes are near their forward conduction points, and only small excursions of the input voltage are permitted. Further forward biasing of the clamping diodes can restrict the input voltage swing to the point that incomplete switching of the output is observed.

These effects are illustrated in Fig. 2, in which the top readout beams from the circuit are depicted (offset from one another for effect), at various clamping voltages. Inputs were provided from directly modulated laser diodes at roughly 850 nm. The modulation source was an HP 8133A pulse/data generator. A pattern dependence is observed in the data for +1.0 V clamps, and is eliminated at +2.0 V clamps, and decreased output contrast is seen for +2.3 V clamps.

Another important issue is sensitivity. This depends critically on both the circuit design and the intrinsic device performance. Undoubtedly, more sophisticated circuits could improve the voltage gain and increase the sensitivity. However, as these circuits increase in size, the power and the area that they consume increases, which can be detrimental to high-density operation. Pulse energy (E_p) can be expressed as a function of the

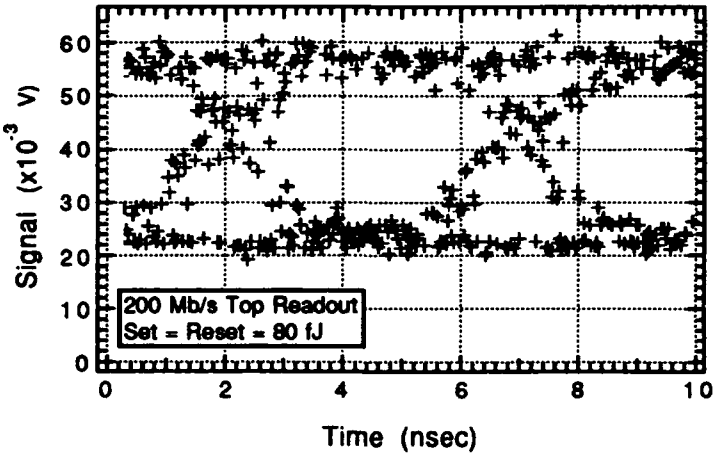

Figure 3: Eye diagram for top diode readout from simple receiver/transmitter pair at 80 fJ pulse energy (-21 dBm average input power).

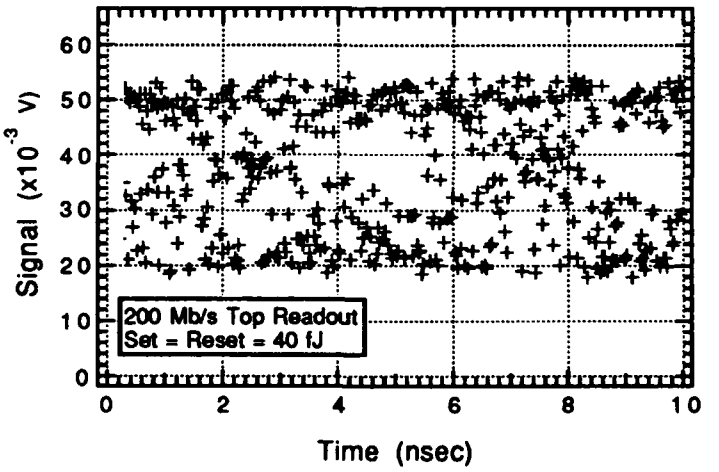

Figure 4: Eye diagram for top diode readout from simple receiver/transmitter pair at 40 fJ pulse energy. Note degradation from 80 fJ case.

average power in the beam (P_{ave}), the fraction of time that light falls on the input during the data cycle, and the bit period (T) as $E_p = P_{ave}TN_b/N_p$, where N_b/N_p is the ratio between the number of bits (N_b) and the number of light pulses N_p (bit 1's perhaps). For example, both random data and fixed 32 bit patterns with 16 ones and 16 zeros have $N_b/N_p = 2$.

In Fig.3 and 4, we present 200 Mb/s eye diagrams for set and reset pulse energies of 80 and 40 fJ. One can clearly see the degradation of the eye pattern at 40 fJ relative to 80 fJ. It should be borne in mind that there is another complementary output from the bottom output modulator, and further that these eye diagrams include noise from the single-ended detector used to monitor the output beams. The fully differential implementation should significantly increase the sensitivity at a given bit rate. Bit error rate measurements have not been performed. The average received power for 80 fJ switching energy at 200 Mb/s

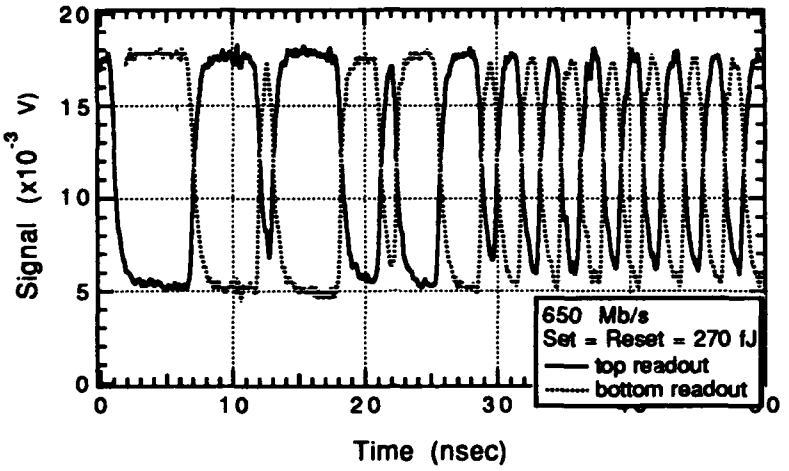

Figure 5: Top and bottom readouts at 650 Mb/s with set and reset pulse energies of 270 fJ.

(5 ns bit period) is 8 μ W (-21 dBm). These same devices could be operated with 130 fJ (-16 dBm) at 400 Mb/s. Still lower switching energy (25 fJ at 200 MHz) is possible for operation with pulsed input.[4]

The highest operation rate obtained to date is 650 Mb/s in a circuit fabricated in a different wafer from those whose data are shown in Fig. 3 and 4. The outputs from both top and bottom readout modulators are shown in Fig. 5. The input optical pulses were 270 fJ for both set and reset (-10 dBm), but we believe lower energies will be possible for this circuit, since the clamping diodes were malfunctioning.

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Monolithic Integration of GaAs/AlGaAs Multiple Quantum Well Modulators and Silicon Metal-Oxide-Semiconductor Transistors

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It is now generally recognized that one likely scenario in which photonics is used in a switching environment is where it is integrated with electronics.[1] This concept takes advantage of the greater capacity of electronics for complexity, functionality, and memory, and the greater capacity of photonics for communications. The most concrete realization of this concept is where photonics functions in the role of optical interconnects between electronic integrated circuit chips (ICs). This entails the monolithic integration of some photonic elements (both receiver and transmitter) on the chip. Also, since an attractive feature of optical I/O is that it can occur normal to the surface of the chip, allowing two-dimensional arrays of interconnects to be formed, surface-normal photonic elements should be used.

Silicon electronics seems to be the most effective technology where complex systems such as microprocessors or memory is concerned. Since the benefit of increased communication capacity to the chip is most attractive when the chip contains a great number of computing elements, it appears that the strongest impact of photonics will be as optical input/output for silicon integrated circuits.

Furthermore, intimate integration of the photonic elements must be achieved with the transistors (i.e., the photonic device must be placed within microns of the electronic device), or else the capacitance of the interconnecting metal lines will degrade the speed advantage that photonics offer. In addition, thousands of photonic devices must be integrated on the chip to take full advantage of the parallelism of optics. Since III-V based photonic elements offer the only high-speed (i.e., GHz), high efficiency operation, and these attributes are necessary for optics to displace electron interconnect technology, it appears that direct heteroepitaxial growth of III-V photonic elements on Si ICs offers the best possibility for the use of photonics in switching systems.

Finally, simultaneous operation of large arrays (e.g., thousands) of surface-emitting lasers has not been demonstrated, and their operation would be thermally problematic, whereas such arrays of surface-normal modulators have been demonstrated.[2] No surface-normal laser heteroepitaxially grown on silicon has been demonstrated at all, whereas reliable surface-normal modulators have been produced on silicon.[3,4] All this information can be summed up with the statement that one logical infiltration of photonics into switching will be in the form of surface-normal modulators grown on silicon ICs functioning as optical interconnects. This function is achieved by modulating the reflectance of beams from an off-chip laser which has been split into an array of spots. This offers the further system advantage over lasers of a global clock (oscillating the off-board laser). Also, quantum well modulators have the advantage of being highly efficient detectors, eliminating the need for integrating two types of photonic devices or using inferior silicon detectors.

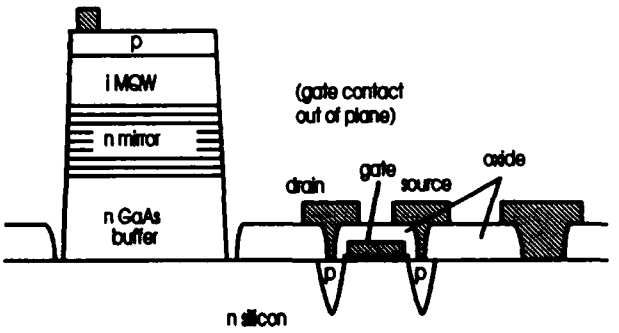

Fig. 1: Schematic of our GaAs/AlGaAs modulator integrated with the PMOS silicon transistor.

Having demonstrated the physical ability of placing reliable modulators on silicon substrates, it remains to show that they may be grown on silicon ICs while retaining the function of the silicon transistors. (It is generally thought that the transistors should be made first since higher processing temperatures are incurred making them, and also since Ga is a notorious impurity for silicon electronics.) In this paper we take the first step toward demonstrating this ability. We have grown and tested a multiple quantum well (MQW) modulator on a silicon IC which was obtained from a standard 0.9 μm linewidth fabrication line. The modulator functioned, although with reduced performance due to spectral misalignment of the integral mirror with the exciton of the MQW. We then metalized and tested a 20 μm gate length transistor on the IC (the reason why the shorter gate length transistors have not been tested will be discussed below) and it functioned near the specifications of the fabrication line.

The modulator growth was performed on a silicon IC obtained from AT&T Microelectronics facility. It had individual test CMOS transistors fabricated on it using 0.9 μm linewidth rules.[5] The transistors had gate lengths ranging from 0.75 to 20 μm, however, all had drain and source openings that were 0.9 X 20 μm. The transistors we used were p-channel devices fabricated in n-"tubs" implanted into the p-type silicon wafer. Their gate oxides were 150 Å thick. The wafer was oriented 3^{o} off-axis from the (100) direction. This is because it has widely been found that off-axis Si substrates are necessary for quality GaAs growth. The wafer was removed from the silicon process line before the final metalization was performed. A SiN_x diffusion barrier was deposited on the chip to protect its field oxide from Ga absorption during growth.[6] Then a window was etched down to the silicon surface for modulator growth (Fig. 1). After dipping in dilute hydrofluoric (HF) acid to remove any non-native oxide from the growth window, the chip was loaded into a Gas-Source Molecular Beam Epitaxy (GS-MBE) reactor. Under vacuum it was heated to 850 ^{o}C to desorb the native oxide. The growth was then performed using a two-step process.

First, a 0.5 μm thick low-temperature (350 ^{o}C) n-type GaAs buffer layer was deposited to make the transition from three-dimensional to two-dimensional epitaxy. Then a 1.5 μm thick standard-temperature (600 ^{o}C) n-type GaAs buffer layer was deposited to reduce defect density. A 14.5 period 722/603 Å AlAs/$Al_{0.07}Ga_{0.93}As$ n-mirror was grown, followed by the i-MQW, which consisted of 60 periods of 95/35 Å GaAs/$Al_{0.3}Ga_{0.7}As$. Finally a 0.5 μm thick p-type $Al_{0.3}Ga_{0.7}As$ layer was grown. At the surface a p^{++} delta-doped GaAs layer was grown. Then the sample was cooled to 100 ^{o}C and a layer of Al was deposited for the top contact.[7] This Al tunneling ohmic contact allows for compatibility with the Al-based metalization of silicon electronics.

After removal from the reactor, the top contact of the modulator was defined by photolithography and etching using a 100:1 H_2O:HF etch. The growth resulted in deposition of non-crystalline material on the area outside the growth window. This was removed by defining a photoresist mask on the modulator and using a wet etch. The final size of the modulator was 60 X 80 μm. As shown in Fig. 1, the bottom contact to the modulator was made by defining a contact to the silicon on the top surface of the chip. We have shown that modulators with contacts independent from the substrate (i.e., isolated) may be grown by using undoped GaAs buffer layers, in the case that several independent modulators must be placed in the same silicon tub.[8]

The gate metal is a doped poly-Si runner that extends out of the plane of Fig.1 to where it is exposed for contact. The gate and runner were fabricated in the silicon processing facility. After defining openings in the silicon nitride diffusion barrier to the gate, source and drain contacts, we deposited Al electrodes as shown. Finally the contacts were annealed at 350 ^{o}C. Note that metalizing to the drain and source contacts requires patterning of photolithographic features nearly the same size as the transistor gate. Because of the height of the modulator above the silicon surface (about 6 μm), there exists a large gap between the photomask and the photoresist on the

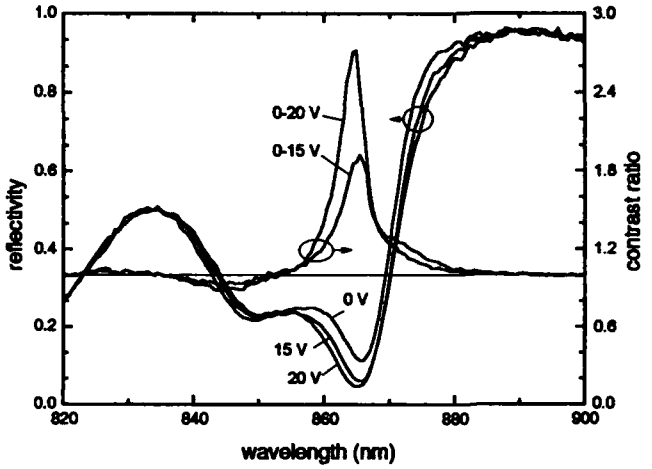

Fig. 2: Reflectivity of our modulator at different biases. Unfortunately the mirror was misaligned with the exciton, reducing performance.

silicon transistor surface during contact lithography. This leads to diffraction of the light during exposure and thus inability to define micron-size features. Therefore, we only report results for the 20 μm gate length transistor here. There are various options that may solve this problem: 1) The modulator could be recessed by etching and growing in a hole.[9] However, the modulator can only be recessed as deep as the n-tub implantation, which is about 1.5 μm. Therefore without modification of the silicon processing technology this is only a partial solution. 2) The mirror may be replaced with an implanted silicide reflector, reducing the total modulator thickness.[10] Again, this is only a partial solution and also requires that the silicide be implanted before the silicon processing.[10] 3) A tri-level resist technology may be used, where thick resist is spun on the wafer, resulting in a planar surface. A metal layer is deposited on this resist, is patterned, and dry-etching is then used to remove the resist around the pattern. This adds a great deal of complexity to the processing. 4) Projection lithography is used. Projection lithography is an expensive technology available in silicon processing lines, and would thus entail re-entering the chip into the silicon processing line after GaAs deposition and therefore introduce possibility of contamination into the line. All of these options are being explored.

The modulator characteristics are shown in Fig. 2. Unfortunately, the mirror was spectrally misaligned relative to the exciton. As can be seen in the figure, the mirror edge is at 863 nm, whereas the exciton is about at 850 nm. It is not clear whether this was a simple error or if recalibration of growth rates must be performed for selective area growth on silicon. Even though the mirror was misaligned, with 15 volts bias the exciton of the MQW shifts far enough to modulate the reflectivity at the mirror edge. With 20 volts bias, we in fact achieve nearly 3 to 1 contrast ratio.

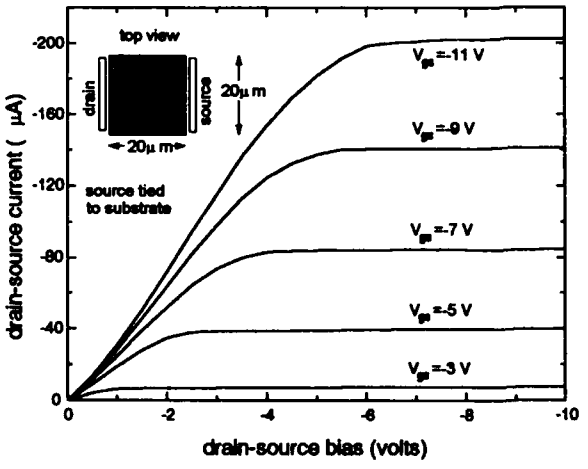

Fig. 3: Common-source characteristics of our PMOS silicon transistor.

The transistor characteristics are shown in Fig. 3. Reasonable field-effect transistor characteristics are obtained, albeit with some contact resistance which can be observed in the negative bowing of the turn-on of the Vgs=-11 V curve. This contact resistance could be due to inadequate coverage of metal in the

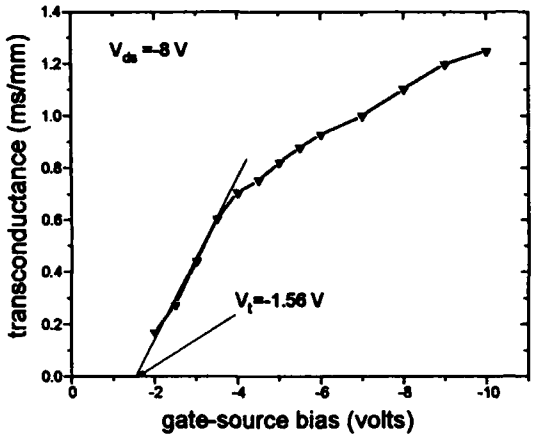

Fig. 4: Transconductance of our transistor as a function of V_{gs}. Threshold voltage is near specified value of -1.1 V.

contact holes or due to damage incurred when the silicon nitride was removed from the contact holes. Fig. 4 shows the transconductance of the transistor ($dI_d/dV_g|V_{ds}=-8V$). The threshold voltage is -1.56 volts. The specified value is -1.1 volts.[5]

In conclusion, we have demonstrated monolithic integration of a GaAs/AlGaAs surface-normal reflection multiple quantum well (MQW) modulator and a silicon metal-oxide-semiconductor transistor. We obtain nearly 3 to 1 contrast for the modulator, whose performance was degraded because of spectral misalignment of the mirror with the MQW exciton. The transistor's characteristics have not shifted greatly from its specified values. This shows that practical integration of modulators on Si IC's may be performed, paving the way for optical interconnects in silicon based switching systems.

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Space Switching

PMD 3:30pm-5:20pm
Grand Ballroom East

Lars H. Thylen, *Presider*
Ericsson Telecom, Sweden

HIGH-CAPACITY PHOTONIC SPACE-DIVISION SWITCHING SYSTEM

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Introduction

Photonic space-division (SD) switching systems are very promising for STM (Synchronous Transfer Modes) broadband switching systems which can provide high speed services such as TV (HDTV) phone and HDTV distribution. An experimental small-capacity (up to 32-line) photonic SD switching system [1] has been already demonstrated. From a viewpoint of practical use, however, further increase in capacity is required. In response to this need, we have developed a prototype high-capacity (up to 128-line) photonic SD switching system. This paper presents the architecture and performance evaluation of the developed photonic SD switching system.

System Architecture

A 128-line photonic SD switching network, shown in Fig.1, consists of 4x4 matrix switches for the 1st-stage switch, 4x8 for the 2nd-stage switch, 8x8 for the 3rd-stage switch, 8x4 for the 4th-stage switch, and 8X4 with a distribution function for the 5th-stage switch. The network is devised to provide both TV (HDTV) phone and HDTV distribution services. TV (HDTV) phone services are provided across the 5-stage switching network. It is designed so that the numbers of matrix switches required are minimized, while holding a blocking probability of 0.1% for 0.1*Erl* which is assumed to be the same blocking probability as telephone services. HDTV distribution services are provided without any blocking probability, using the distribution function in the 8x4 matrix switches for the 5th-stage switch.

Photonic Device Technologies

Three important photonic technologies have been developed for implementing the high capacity network. The first technology is a polarization-independent $LiNbO_3$ matrix switch. Fig.2 shows a 8x8 matrix switch. 64 polarization-independent directional coupler switch elements, where complete coupling length for TE and TM modes are coincident, are integrated on one $LiNbO_3$ chip using a Simplified-Tree-Structure (STS) architecture. The polarization independence of the matrix switch

allows using ordinary single-mode fibers and conventional optical connectors for interconnecting matrix switches, resulting in a practical optical interconnection. By employing STS architecture, a low switching voltage of 70V, low insertion losses of less than 12dB for 8x8, less than 8dB for 4x8 and less than 6dB for 4x4, and a low crosstalk value of less than -18dB are obtained.

The second technology is a semiconductor optical amplifier. The losses of the matrix switches limit the number of matrix switches that can be cascaded. For loss compensation, the 1.3μm band traveling-wave type semiconductor optical amplifiers with a window facet structure have been developed. Fiber-to-fiber gain of 11dB is achieved, irrespective of TE and TM modes. For switching 600Mbps HDTV digital signals, two semiconductor optical amplifiers are necessary to compensate for a 5-stage network total loss. Considering gain saturation characteristics and minimization of power penalty due to SNR degradation, two semiconductor optical amplifiers are placed in the positions before and after 8x8 matrix switch for the 3rd-stage switch, as shown in Fig.1.

The third technology is an optical interconnection. As shown in Fig.1, the interconnection between the matrix switches is very complicated. The higher the capacity of the network, the more severe congestion in the interconnection becomes. A promising solution to the problem is a three-dimensional optical interconnection concept [2] shown in Fig.3. An orthogonal arrangement of the matrix switches can simplify the complicated interconnection to a straight interconnection. This simplified interconnection is achieved by using newly developed board-to-board optical connectors as shown in Fig.4. These connectors allow matrix switch boards to be easily inserted into or removed from the system.

System Implementation and Evaluation

To apply the three-dimensional optical interconnection concept to a 5-stage switching network, partitioning of the network should be optimized. The network is partitioned into three kinds of optical switch boards and an optical amplifier board as shown in Fig.1. Figs.5 and 6 show an optical switch board and an optical amplifier board, respectively. The board-to-board optical connectros are placed on both edges of the boards. Placing the boards orthogonally in a rack, a photonic SD switching system can be realized as shown in Fig.7. Fig.8 shows a prototype high-capacity photonic SD switching system. A part of a 128-line switching network is constructed to evaluate system performance and to provide trial broadband services. Fig.9 shows the measured Bit-Error-Rate (BER) curves for a 600Mbps digital signal. An ample system margin of 3.7dB for BER of 10^{-9} is achieved. For a 150Mbps digital signal, the more system margin is obtained. It is confirmed that the system has been operating in providing 150Mbps TV phone services and 600Mbps HDTV distribution services with high stability.

Conclusions

A prototype high-capacity photonic space-division switching system with a maximum capacity of 128 lines has been developed. All of the developments on the polarization-independent LiNbO3 matrix switches, the semiconductor optical amplifiers and the three-dimensional optical interconnections combine to make possible a high-capacity photonic switching system. The system has been successfully opreating in providing TV phone services and HDTV distribution services with high stability. Therefore, the system took a further step toward practical applications.

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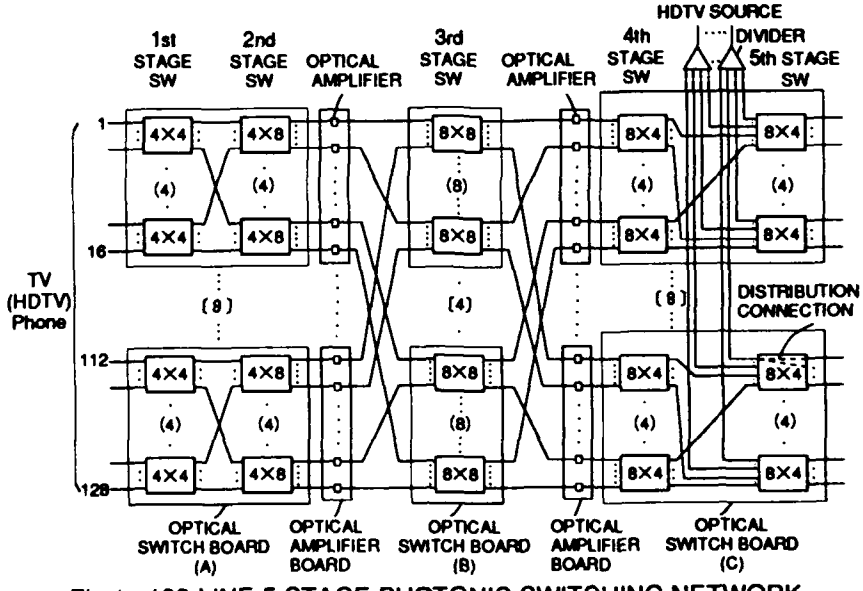
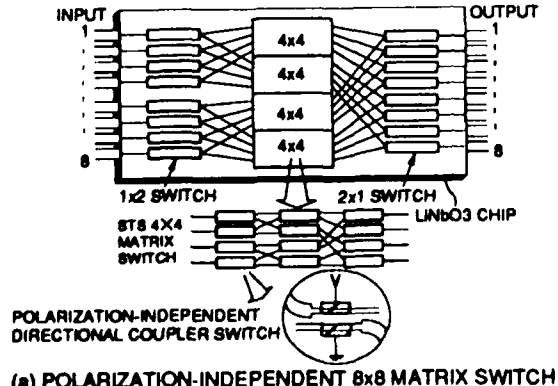
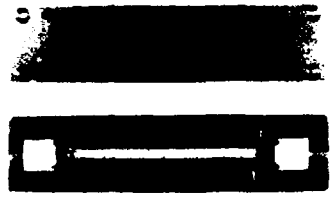


Fig.1 128-LINE,5-STAGE PHOTONIC SWITCHING NETWORK



(a) POLARIZATION-INDEPENDENT 8x8 MATRIX SWITCH USING SIMPLIFIED-THREE-STRUCTURE (STS)



(b) 8x8 OPTICAL SWITCH MODULE

Fig.2 8x8 OPTICAL SWITCH

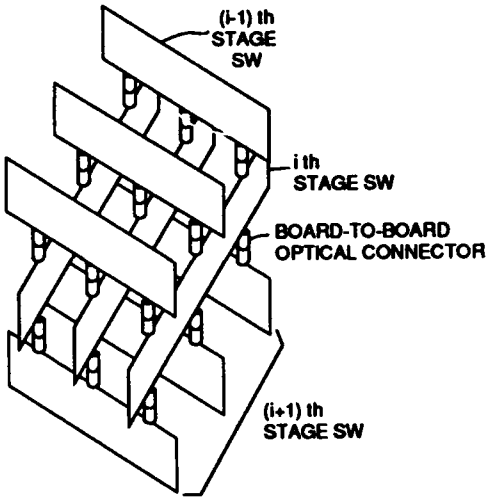


Fig.3 THREE-DIMENSIONAL OPTICAL INTERCONNECTION CONCEPT

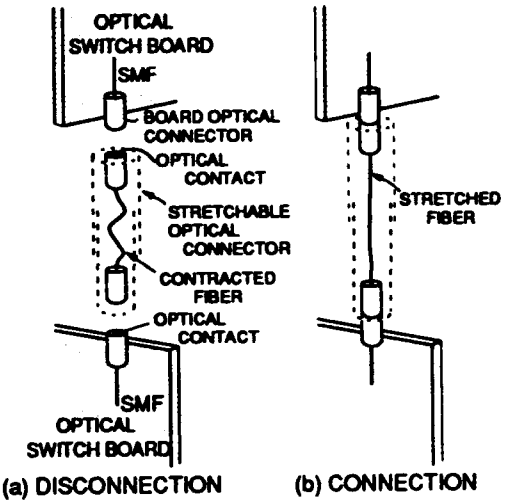


Fig.4 BOARD-TO-BOARD OPTICAL CONNECTOR

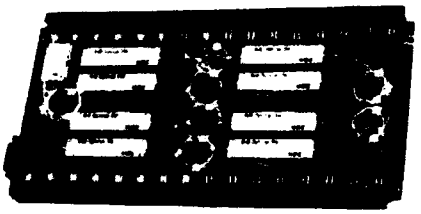


Fig.5 OPTICAL SWITCH BOARD

Fig.6 OPTICAL AMPLIFIER BOARD

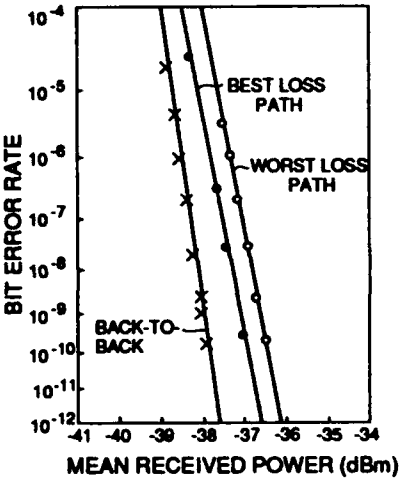


Fig.9 BIT-ERROR-RATE

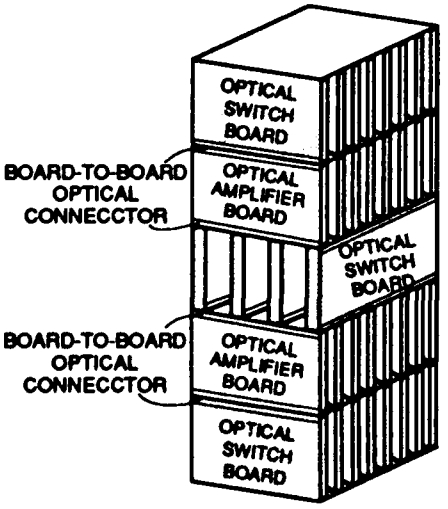


Fig.7 PHOTONIC SWITCHING NETWORK STRUCTURE

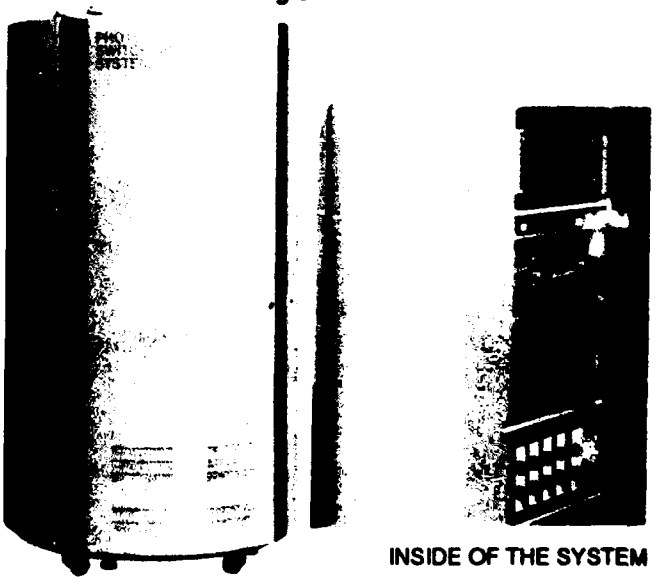


Fig.8 HIGH CAPACITY PHOTONIC SPACE DIVISION SWITCHING SYSTEM

Optical Crossbar Switch with Semiconductor Optical Amplifiers

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Semiconductor optical amplifiers (SOAs) have a number of attractive properties for use in photonic switches. SOAs offer nanosecond switching times, extinction ratios in excess of 40 dB, and small signal gains of approximately 15 dB. In addition they can be monolithically integrated, and thus can potentially be fabricated in volume and used in large switch matrices. Here we report on our recent demonstration of an 8x8 optical crossbar switch based upon discrete SOAs. Other authors [1-3] have reported on SOA-based optical switches at the device level. Our work focuses on the demonstration of the technology at the system level. This demonstration is a significant step towards the widespread use of SOA-based optical switches because it provides a testbed for exploring and identifying the relationships between device parameters and system performance requirements. A block diagram of the optical crossbar switch is shown in Figure 1. The switch is constructed in a modular fashion and consists of optical, digital, analog, and computer modules. Figure 2 shows two photographs of the completed optical crossbar switch.

The optical module contains all the required optics, thermal electric coolers, and front end driver circuitry for the SOAs. The optics consists of SOAs and 1x8 single-mode fiber optic splitters and combiners. These elements are interconnected based upon the matrix-vector-multiplier (MVM) architecture as shown in Figure 3. For demonstration purposes, the optical crossbar switch has been populated with only enough SOAs to fully interconnect four inputs with four outputs. However, since 1x8 splitters and combiners have been used, these paths accurately represent the paths through a fully populated 8x8 optical crossbar switch. Note the second stage of SOAs located after the combiners. These are used because distributing the optical gain throughout the switching fabric, given limited SOA saturation power, maximizes the signal-to-noise ratio [4]. Mechanically, the optics module consists of a 13" by 16" printed circuit board that can hold 72 SOAs and their associated front end driver circuitry. The driver circuitry consists of differential transistor pairs and is collocated with the SOAs to reduce electrical noise in the switch. The assembled printed circuit board is attached to a copper plate for thermal stability. The back side of this copper plate has four thermal electric coolers connected to temperature sensors and feedback circuitry that maintain the temperature of the optics module at 25 ± 1 °C. Temperature stabilization is required because the gain and the bandwidth of the SOAs vary with temperature.

The optics module interfaces to both the analog and digital modules as shown in Figure 1. The analog module contains 72 precision constant current supplies that connect to the emitters of the differential transistors on the optics module. Each of these current supplies can be controlled through software on the computer module. By adjusting the amplitude of the currents, the optical gain of the individual SOAs in the optics module can be set. The digital module consists of a 16x72 multiplexer, 72 latches and 72 ECL drivers. The multiplexer decodes connection instructions from the computer module and places a binary map of the state of the optical crossbar switch in the latches. The output of the latches is connected to the ECL drivers, whose outputs are in turn connected to the bases of the differential transistor pairs on the optics module that drive the individual SOAs.

The analog and digital modules are controlled by the computer module. The computer module is based on a 80386SX processor and supports a graphical interface that allows the user to control the optical crossbar switch in a variety of modes using "out-of-band" techniques. Individual crosspoints can be set in simplex or duplex, or the entire configuration of the crossbar switch can be changed, either in real-time or through time-scheduled macros. In addition, the graphical

interface supports a number of administration and maintenance functions. A password program is in place that prevents unauthorized connections from being established through the crossbar switch. Various hardware checking algorithms are used to periodically verify that the circuitry on the optical, analog, and digital modules is functioning correctly. Key environmental factors are monitored, such as the supply voltages to the electronics and temperatures at various positions in the cabinet. An error log is kept in memory to record any abnormalities that are detected. Finally, the computer module can execute an auto shutdown of the optical crossbar if any key parameters are out of range or significant faults are detected.

Development is presently underway to augment the computer module with an in-band control module. This module is based upon an embedded RISC processor and will enable the optical crossbar switch to receive connection requests directly over the input optical fibers. The in-band module will interface directly to the digital module and, using the inherent broadcast capability of the MVM architecture, poll the input optical fibers for connection requests without interfering with existing connections. The first generation of the in-band module will operate in conjunction with a commercially available HIPPI (High-Performance Parallel Interface) fiber optic extender, and will therefore conform to HIPPI protocol standards. Subsequent generations of the in-band module will incorporate electro-optic conversion circuitry and operate with other optical protocols, such as SONET.

The transmission properties of the 16 paths through the optical crossbar switch have been thoroughly characterized. Each path has an optical rise and fall time of 20 nanoseconds. This switching time is limited by the transistor drivers, not the SOAs. The inherent switching time of the SOAs is at least an order of magnitude faster. Each path has a 3 dB optical bandwidth of approximately 35 nanometers and center wavelength of 1310 nanometers, as shown in Figure 4. The average extinction ratio of the optical signals, as defined by the ratio of the optical signal power level when a crosspoint SOA is on and off, is approximately 40 dB. The drive currents to the SOAs are set to provide 0 dB net optical gain through the optical crossbar switch for average input signal levels of -10 dBm. This level of optical gain ($\approx$11 dB) requires an average current of 60 mA to each SOA. The optical gain through the optical crossbar switch decreases to approximately a net -2 dB for average input signal levels of -3 dBm due to large signal saturation of the SOA gain. Bit error rate (BER) measurements were conducted on each path through the optical crossbar switch. A typical eye diagram is shown in Figure 4. A nominal operating range of -3 dBm to -10 dBm average input signal level was established based upon a minimum acceptable BER of 10^{-12} at 1.1 Gb/s. The operating range is limited on the low signal level side principally by signal-spontaneous and spontaneous-spontaneous beat noise and on the high signal level side by a combination of two types of distortion. One type is due to time dependent optical gain saturation of the SOAs and another is due to a shift in the receiver's photodiode bias point caused by the presence of appreciable optical power levels ($\approx$-4 dBm) of spontaneous emission noise from the SOAs. Though both of these effects can be reduced by the addition of narrowband optical filters, we have elected not to incorporate such filters in an effort to preserve the large intrinsic optical bandwidth of the SOAs.

Further evaluation of the optical crossbar switch is underway. Two copies of the switch described above are being fabricated for alpha testing at customer sites. One will be used to link together a network of high performance computers. The other will be used in an imagery testbed and will transport mixed analog and digital signals. The authors wish to gratefully acknowledge the support of DARPA through contract #N66001-86-C-0382.

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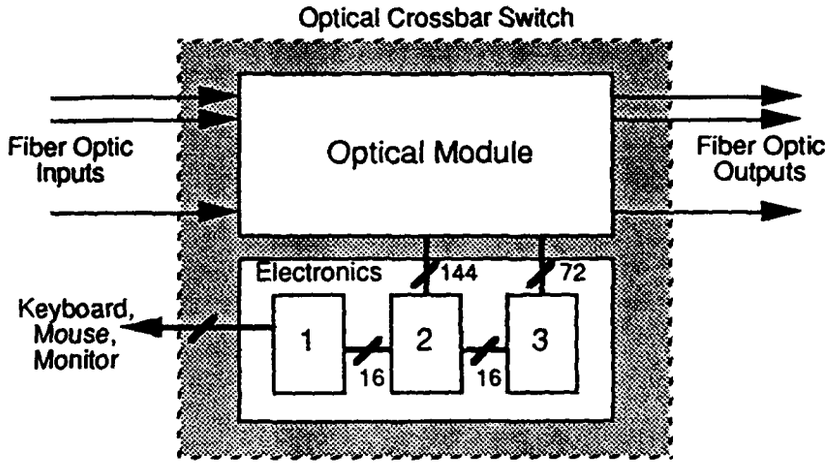
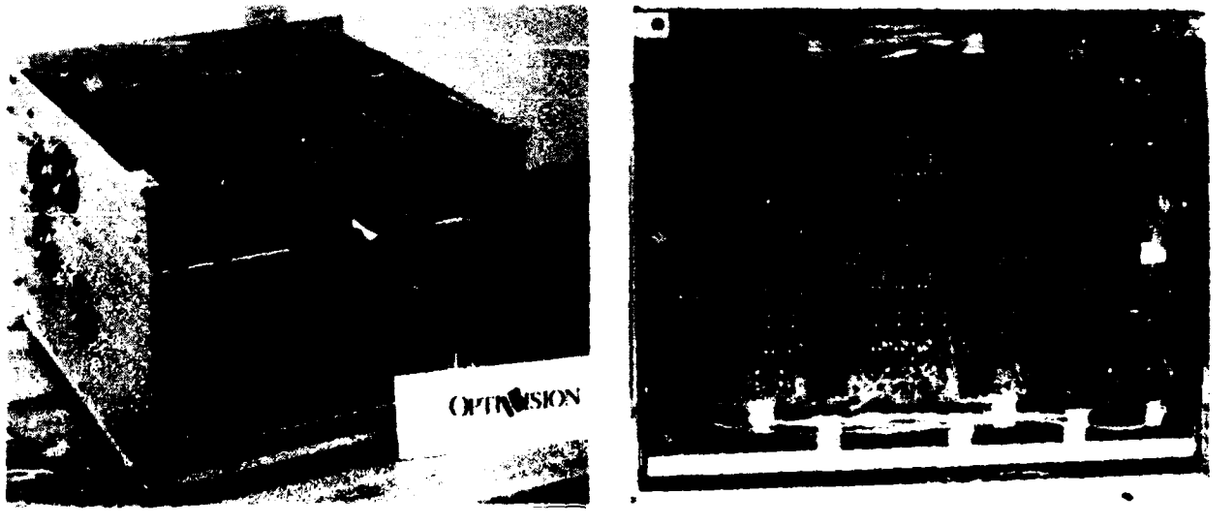


Figure 1. Block diagram of the optical crossbar switch showing the optical, computer (1), digital (2), analog (3) modules.



A **B**

Figure 2. (A) Photograph of the optical crossbar switch showing support electronics and overall size. (B) Photograph of the optical module showing layout of SOAs.

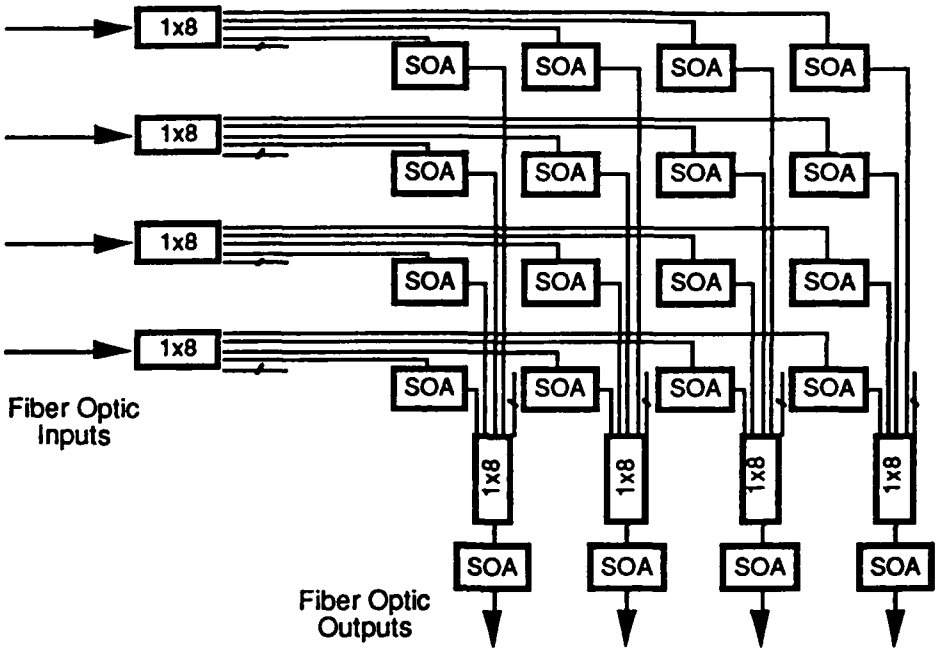
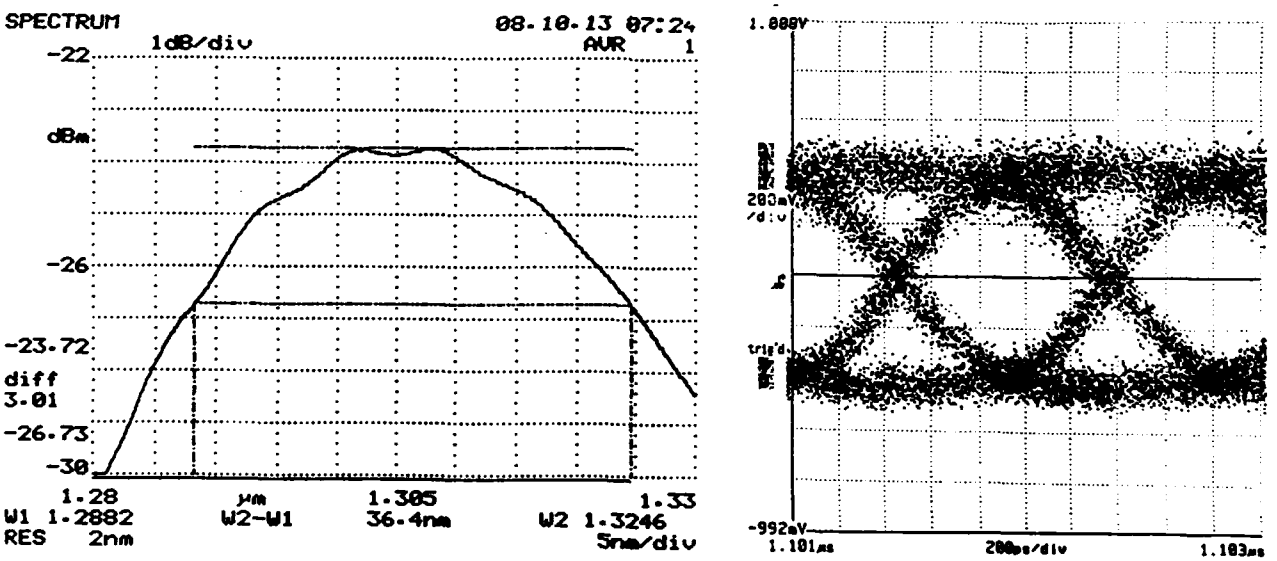


Figure 3. Schematic of the optics showing the matrix-vector-multiplier architecture of the 8x8 crossbar and the locations of the 20 SOAs used to fully interconnect four of the inputs to four of the outputs for the purposes of demonstration.



A B

Figure 4. (A) Typical optical spectrum of a path through the switch showing the 3 dB bandwidth and center frequency. (B) Typical eye diagram of a signal transmitted through the optical crossbar switch. The SOA currents have been adjusted to provide 0 dB net optical gain through the switch. The average optical signal power launch into the switch is -6 dBm. This eye diagram is sufficient to pass data at less than 10^{-12} BER at 1.1 Gb/s.

Ti:$LiNbO_3$ Photonic Switch Modules for large, Strictly Non-blocking Architectures.

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The understanding of guided wave switching devices and optical switching system needs has matured such that it is appropriate to consider optimum system architectures and optimum device topology(1,2,3). Here we report switch modules which simultaneously optimize these constraints. We first describe an architecture that deals with the constraints of guided wave photonic switch arrays. Then we discuss the design, fabrication and testing of the switch modules utilized in this architecture.

We are implementing an Extended Generalized Shuffle (E.G.S.)(4) network to build large photonic switches. This architecture is well suited for large, space division optical switches. E.G.S. networks can be strictly non-blocking, so that new paths can be configured without effecting other active ports. They can be built from 2x2 switch elements and configured to minimize crosstalk by allowing only one active input to each switch element. Also, an E.G.S. network can be designed to minimize the number of swit ch element across the switch array, resulting in the minimization of insertion loss and device length. E.G.S. Networks allow ease of path hunting and network control. Finally, E.G.S. networks can be designed to use the same basic modules as building blocks for larger switch sizes.

Figure 1 shows a schematic of two chip designs which are the two basic modules of a growable E.G.S. network. With only two different modules, manufacturing simplicity is maintained. The input/output modules are "dual 1x8" active splitter/active combiners and the center stage modules have 16 inputs and 16 outputs with one path from every input to every output. These modules have been chosen with a limit of 16 inputs and outputs to facilitate packaging and system use. Also, this limits the number of switches and thus the length of the device to make efficient use of the area on a 100mm diameter wafer. Figure 2 shows architectures using these chips in 16x16 configurations, however, with these same modules 256x256 configurations can be achieved.

For a switching element, both chips use an identical 2x2 directional coupler 8.75 mm in length. The coupler is designed to have low crosstalk, to have only two control electrodes to minimize the number of package pins and to have uniform bias and switching voltages to simplify driver design and setup. This element efficiently switches TM polarized light at $\lambda = 1.5\ \mu m$. The use of a single polarization switch element decreases individual switch element crosstalk, increases ability to meet loss uni formity requirements, and eliminates the possible problem of polarization dispersion for the different polarizations. Use of polarization controllers with photonic switch arrays has been demonstrated(5).

For the center stage modules, waveguide interconnects are designed for low loss by changing the coupler spacings to maximize intersection angles, using large radius of curvature bends, using modified intersections(6), and delaying the start of lower intersection number bends to maximize the intersection

angles. Two different approaches have been taken to minimize path dependent loss differences in order avoid receiver dynamic range issues. One design uses "dummy intersections" in paths with fewer intersections to equalize loss, another uses sharper (i.e. lossier) bends in paths with fewer intersections to equalize the loss in paths with many intersections. The devices are fabricated using standard fabrication conditions reported previously(3). Both Modules have angled interfaces to reduce back reflections. This allows the devices to be used with single frequency laser sources and in fiber amplifier systems. The devices are packaged with arrays of polarization maintaining fiber. A thin film polarizer is used in each package to ensure good polarization extinction ratios.

Several of these devices have been fabricated and tested. Figure 3 snows crosstalk, and voltage data on the devices. For the first devices crosstalk is a minimum of -18 dB and typically -30 to -40 dB. Bias voltages are typically -10 volts and Switching voltages are typically 12 volts. Typical insertion loss is -6 dB for the dual 1x8 and -8 dB for the center stage modules. More detail on the performance of these devices will be given at the conference.

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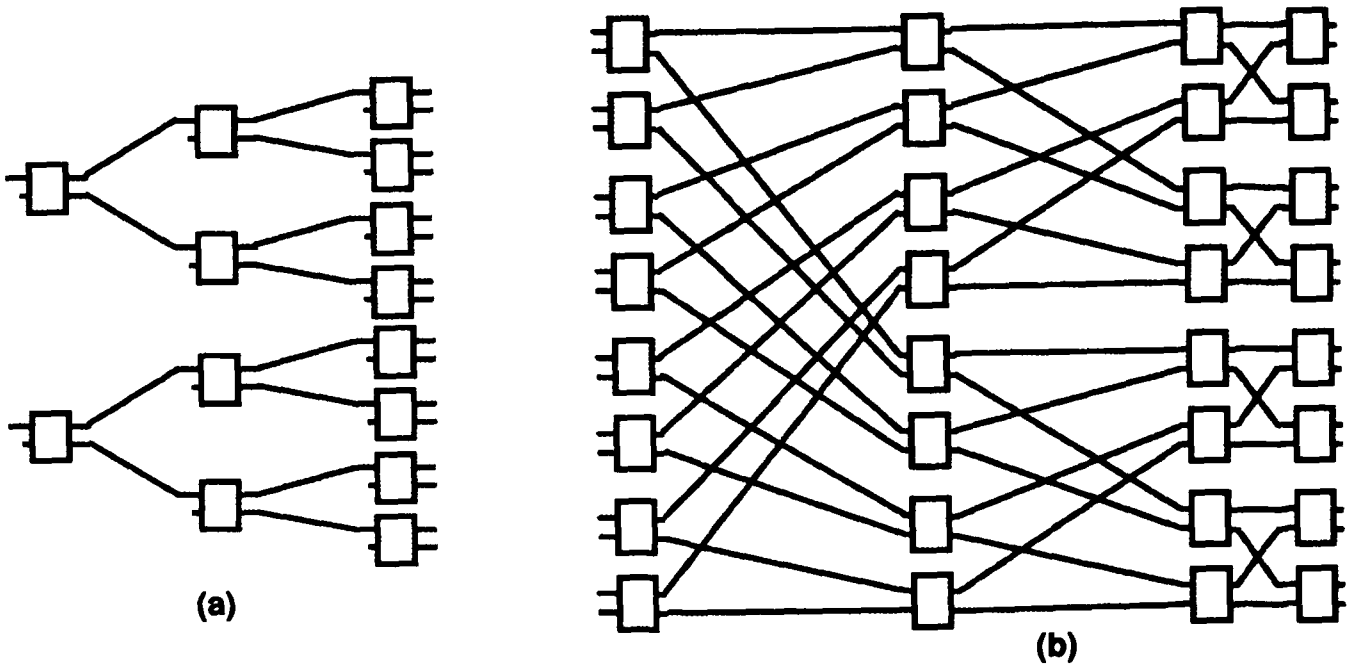

Figure 1. Dual 1x8 (a) and Center Stage (b)

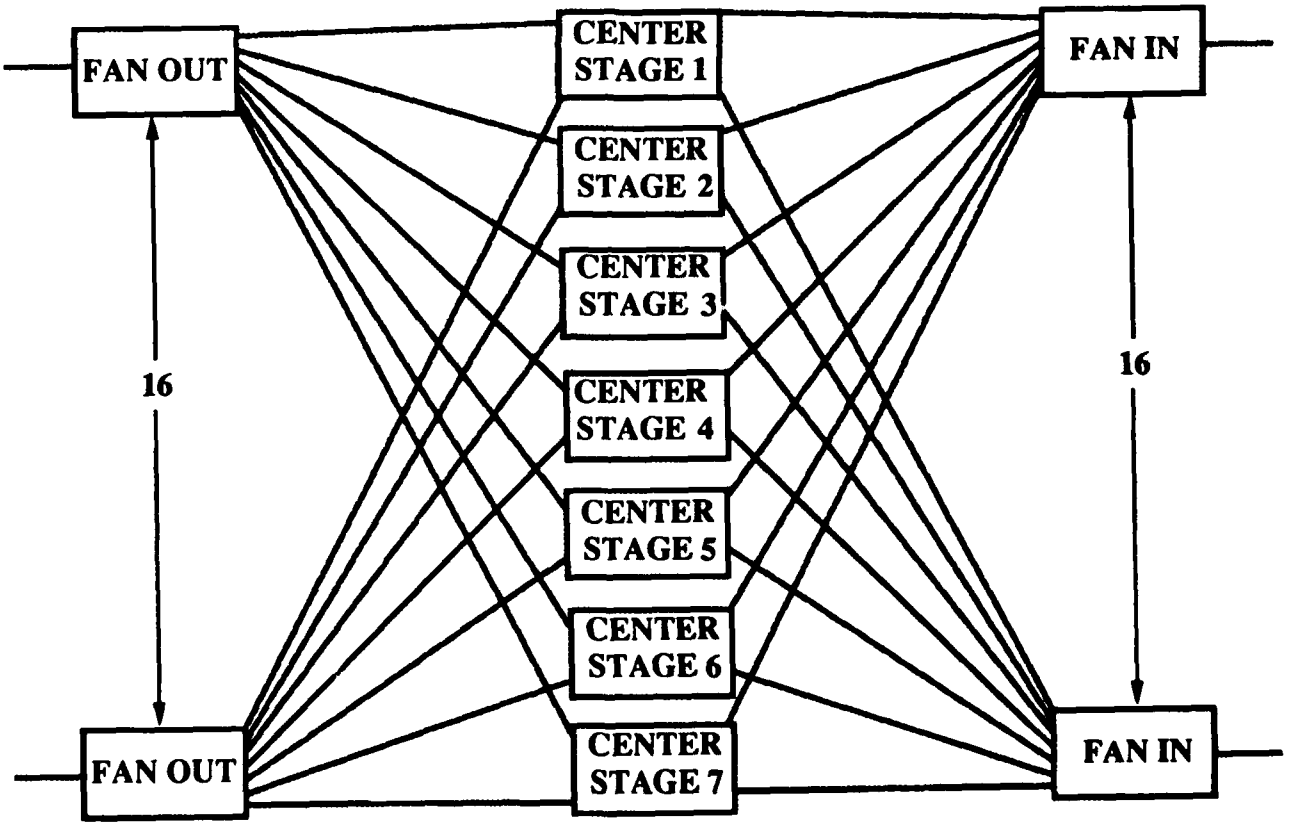

Figure 2. 16x16 Strictly Non-Blocking Extended Generalized Shuffle Network

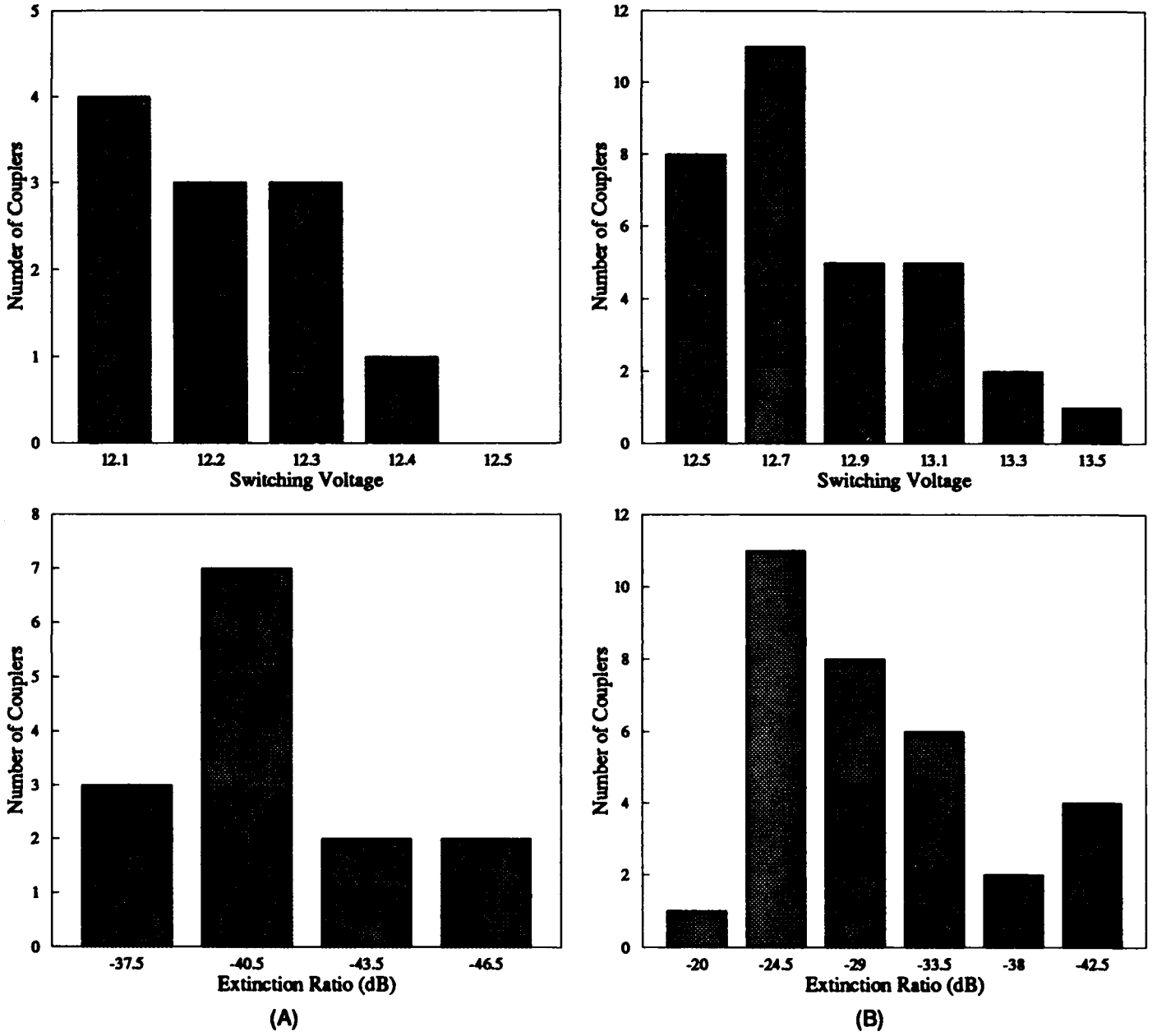

Figure 3. Histograms of Switching Voltage and Bar State Extinction Ratios for Dual 1x8 (A) and Center Stage (B).

Acoustooptic Crossbar Photonic Switch

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Emerging serial optical communication standards such as Fiber Channel require a large optical crossbar (called a "fabric") that routes signals in a circuit-switching manner with a few μsec switching time. The switching fabric must be able to transmit multi-gigabit per second optical signals and should be transparent to wavelength division multiplexing (WDM) protocols, and thus cannot be implemented in existing Silicon or Gallium Arsenide technology. The alternative is to use an all-optical switch which can quickly establish physical connections between fibers.

We have designed such an optical crossbar switch using a single anti-tangential, bulk acoustooptic device to implement the entire N x M crossbar[1, 2]. This acoustooptic photonic switch can rapidly permute, combine, or broadcast an array of optical signals on single-mode fibers without suffering from extraneous fan-in and fan-out losses typically associated with optical crossbars[3]. The switch, controlled by a digital waveform synthesizer, has inherently low optical losses, high bandwidth, microsecond reconfiguration time, and is bi-directional. We have extended the basic crossbar design to include wavelength multiplexing and multiple independent switches within a single acoustooptic crystal (angular multiplexing). The following sections present the operation of these switches and extensions to the basic design. These designs are verified with a numeric computer aided design (CAD) tool. Finally, we present experimental results of the switch operation

1 Operation of the switch

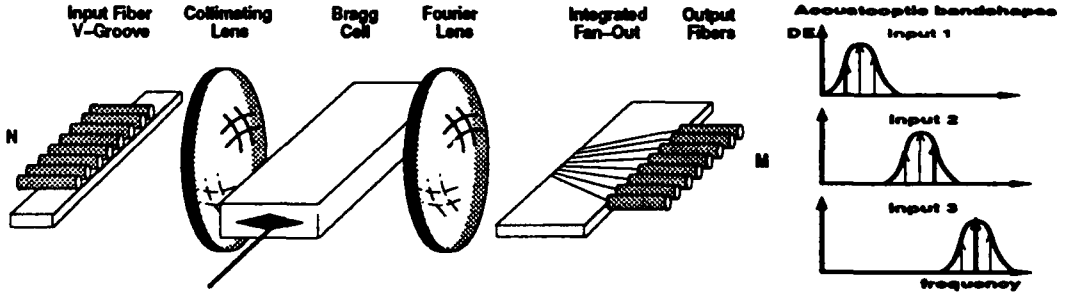

Figure 1: Optical layout of switch and AO bandshapes for each input

The N-input by M-output acoustooptic interconnection system is depicted in Figure 1. The optical input is a uniformly spaced array of N single-mode fibers, which are widely separated (by a 250 μm spacing V-groove array) so that they are resolvable by a factor of M. Thus, the distance between fibers is M times the spot-width of each fiber. The M optical outputs are arranged on an array of wave guides that are just resolved, so the output wave guides are separated by slightly more than the waveguide modal width. A custom integrated fan-out device or a lenslet array is required to spread the optical signals back out to match the V-groove fiber spacing. The input array is collimated by the first lens, producing a set of beams with large angular separation incident on the Bragg cell. The Bragg cell is driven by a superposition of N widely spaced acoustic frequencies, each of which is responsible for directing one particular input towards a selected output. The second lens focuses the acoustically-redirected optical waves onto the destination wave guides, thereby coupling

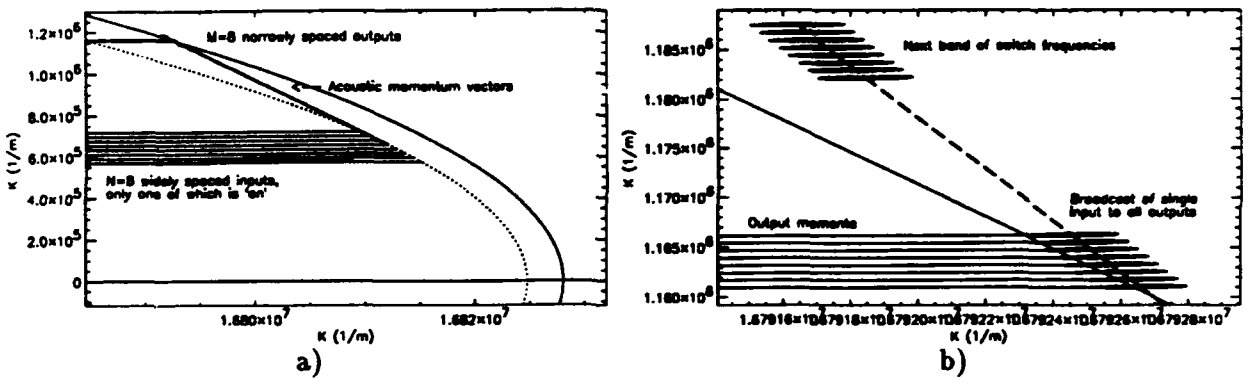

Figure 2: a)Numerical calculation of K-space of 8x8 switch, b) Magnified K-space around output states showing 3 dB acoustic uncertainty contours

the appropriately permuted input optical signals into the output fibers. Mode matching allows this interconnection to avoid extraneous losses. The directions of propagation of the optical inputs are arranged so that each fiber input is Bragg-matched to a narrow RF bandwidth containing only one of the acoustic frequencies and does not interact with any of the others. This is fundamentally different than a normal wide-band acoustooptic device, in which a single optical input is intended to be diffracted by all of the acoustic frequencies which are present.

In this acoustooptic switch, the $O(NM)$ complexity inherent to a generalized N by M crossbar is represented by the frequency content of the driving signal. The device bandwidth is divided into N non-overlapping frequency bands, as shown in Figure 1b. One of M frequencies is chosen out of each band to direct one of the N inputs to one of the M outputs. Since the number of frequencies which can be independently resolved at any instant in an acoustooptic device is equal to the time-bandwidth (TB) product of the device, there is a limit placed on the number of inputs and outputs. For the TeO_2 material used in this design, the TB is approximately 1000. Due to the over-resolved configuration of the inputs (required to avoid crosstalk and loss), this switch requires a TB of $O(N^2M)$ which makes an 8 by 12 switch quite reasonable.

2 Design of the acoustooptic crossbar switch

Figure 2 shows a numerical simulation of the momentum space of an 8 by 8 switch in TeO_2. This switch illustrates most of the design features of this type of switch. In Figure 2a, the acoustics are driven tangential to the inner, input momentum surface. This arrangement, known as anti-tangential Bragg matching, maximizes the angular range available for inputs while driving the acoustic momentum vector across the output surface at an angle, thus minimizing the bandwidth associated with each output state. The entire switch has been acoustically rotated off of the horizontal optical axis by 2.2 degrees (internal) to Bragg mismatch the negative diffraction orders that would couple half the input light to points symmetrical to the output fibers in the unrotated tangentially degenerate design. Acoustic walkoff of 20 degrees can be readily accomodated by increasing the crystal length. Finally, it should be noted that the horizontal axis is not quite the optical (Z) axis of the crystal – the splitting of the eigenstates along the optical axis due to the optical rotary power of TeO_2 results in only a 23 Mhz tangentially degenerate frequency at an optical wavelength of 830 nm. To increase this frequency up to a more convenient range (and also to increase the TB of the cell), the optics have been rotated around the acoustic K vector to a

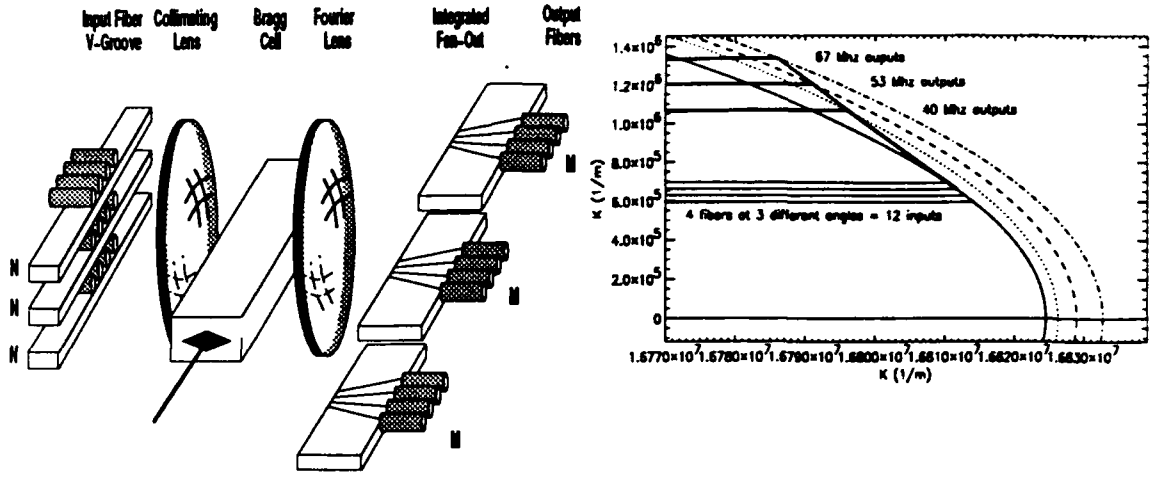

Figure 3: Three angularly multiplexed 4x4 switches: a) real space, b) projection of momentum space

plane 3.06 degrees (internal) away from the optic axis.

Figure 2b shows a close-up of the Bragg coupling to the output optical states. Superimposed on each acoustic momentum vector is the "uncertainty" of the acoustics - the Fourier transform of the optical/acoustic interaction region which defines the spread of acoustic energy in momentum space. To accomplish low-loss switching, the output states must fall within the 3dB contours of this uncertainty (which are shown in the figure). To Bragg mismatch the frequencies responsible for switching other inputs, the uncertainty contours must lie sufficiently far away from the output momentum surface to avoid significant coupling. The size and shape of the uncertainty contours is adjusted by the optical aperture and transducer length and shape which are constrained by acoustic loss and interaction efficiency, respectively.

3 Wavelength and angle multiplexing

The switch in Figure 2 uses only about one half of the octave bandwidth available from a typical piezoelectric transducer, and smaller switches use even less. This fact, combined with the possibility of moving the center frequency of acoustooptic interaction through optical rotation or changes in wavelength, permits several generalizations to the basic switch design still only using a single channel acoustooptic device.

A four by four switch can be constructed which uses only about one third of the available acoustic bandwidth. By rotating the plane of the interaction about the acoustic propagation direction, three such switches could then be operated simultaneously in the same crystal (see Figure 3a.) The ordinary input optical state is nearly unchanged by this rotation, but the extraordinary output state moves increasingly farther away with increasing optical rotation angle, as shown in Figure 3b. The three switches use non-overlaping bandwidths operating at center frequencies of 40, 53, and 67 Mhz. By using a multichannel extension of the multiplexed AO crossbar, and feeding the outputs back to the inputs, one could implement more advanced switching topologies, such as Clos networks, in a single acoustooptic crystal.

Since optical momentum varies with wavelength and dispersion of the optical rotary power,

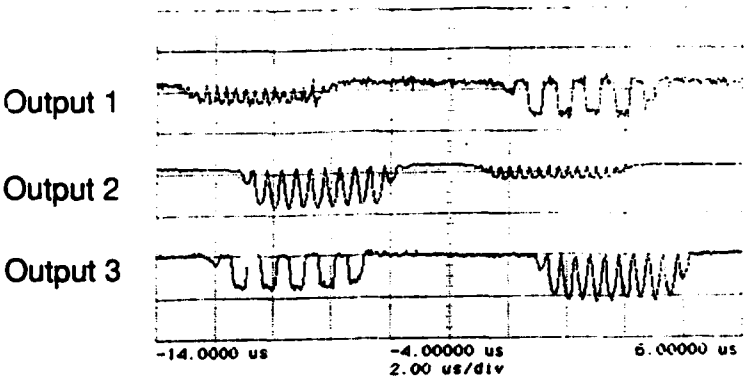

Figure 4: Experimental demonstration of rapid permutation switching

wavelength-multiplexed switching may be implemented in a manner similar to that described in the previous section. In this case, the physical configuration of the switch is identical to that in Figure 1, but each fiber now carries signals at multiple colors. By proper selection of the switch parameters and the colors, the frequency bands of each color can be separated to allow the switching of any input fiber and any color to any output fiber, again controlled by only a single acoustic signal made up of a supperposition of control frequencies.

4 Experimental results

Figure 4 shows switching results from a preliminary demonstration of a three by three switch in a beam-steered flint glass cell. The scope trace shows the signals detected on three outputs as the switch is configured in two different permutation geometries. This system showed appriximately one microsecond reconfiguration time, and 24 dB of isolation between chanels. Results of a similar four by six acoustooptic switch using an anti-tangential TeO_2 cell will be reported at the conference.

5 Summary

A new type of acoustooptic crossbar switch that can rapidly permute, combine, or broadcast an array of optical signals has been described. The switch, controlled by a single line driven with a multitude frequencies, can be generalized to wavelength multiplexed optical signals and to operate multiple switches in a single crystal. The switch is low-loss, bi-directional, and places no detector/modulator limitations on the bandwidth of the optical signals.

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Paper Withdrawn

Optical Interconnects

PTuA 8:30am-10:00am
Grand Ballroom East

Thomas J. Cloonan, *Presider*
AT&T Bell Laboratories

Optical Fiber Interconnection Links for High-Speed Switching and Computer Systems

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I. Introduction

Among the various optical interconnection technologies being researched today, optical fiber interconnection is one of the most practical for near-term applications. [1] It is very effective for solving the recent problem of data transfer bottlenecks in advanced switching systems and computers. [2]-[4] The merits of optical transmission, including wide bandwidth, immunity to electromagnetic interference, ground-isolation capability, and small cable size, also favor in such short-distance applications. Since their circuit boards and units usually have parallel I/O interfaces, multi-fiber parallel transmission has the advantages of compatibility to the conventional system designs as well as the capacity for high overall transmission throughputs. This paper discusses the technical issues associated with the optical fiber interconnection links mainly focusing on parallel links and touching upon recent developments in Japan. [5]-[12]

2. Optical links in advanced telecommunication systems and computers

The ATM (asynchronous transfer mode) switching systems for future broadband ISDN should be able to handle a million channels of 156 Mbit/s wideband services. For the development, it is essential to realize high-speed data channels among subscriber units, switching fabrics, and control processors in the switching system. The next generation telecommunication networks, conforming to a new synchronous digital hierarchy, requires transmission terminals and digital cross-connect systems to accommodate a large number of 156 Mbit/s and higher-speed multiplexed signals. As for advanced computers, today's large-scale main-frames and vector processor systems have many central processing units which are densely packed with ultra-high-speed LSIs. For high-performance in such computers, data communication among processing units, memory units, and I/O controllers should have a huge data transfer capacity, in excess of several Gbytes/s. Flexibility and high-speeds are also needed in distributed computer systems. Introducing optical fiber links is an effective way to meet these requirements as well as to enhance their performance and system flexibility.

3. Technical issues

Much of the basic technology of long-haul systems can be applied to optical links. There are, however, a number of issues unique to the short-distance applications that must also be addressed. For upgrading interconnection wirings by replacing metal cables by optical fibers, essential considerations

include compactness, low cost, and high transmitter and receiver reliability. The special requirement for parallel links is to minimize interchannel skew, the signal delay differences among channels that is caused by the characteristic deviation of fibers, light sources, and electrical circuits. It is also necessary to obtain the extremely low error rate that are comparable to the one in metal wire line transmission. Various approaches are being taken to achieve these goals. Typical recent parallel link development in Japan is summarized in Table 1. [5]-[9][11]

As the link span is less than several hundred meters for most cases, fiber loss is not a significant factor. Multi-mode fibers are convenient for the low-cost and simple coupling to optical elements such as LEDs. [3][4][7] Skew is typically 10 ps/m, or about one tenth of that in coaxial cables. Therefore, multi-mode fibers can be used for numerous applications up to about 200Mb/s. To achieve much higher speed and skew margin, the present trend is to use single-mode fibers since their skew is several times smaller than that in multi-mode fibers. [6] Successful parallel transmission at 2.5 Gb/s over 400 m of single-mode fibers has been carried out recently. [9]

Integrated light source and detector arrays are essential for minimizing module sizes. An LED array is advantageous in terms of its drive circuit simplicity and excellent temperature characteristics. For better output power and higher speed operation, efforts are currently underway to produce high-performance LD arrays. Low-threshold current, high quantum efficiency, and small temperature dependence are basic requirements for a simple and low-power drive circuit without any APC and DC bias. [6][8] Introducing the MQW structure may play a key role in reaching these goals. For achieving wide operating temperature range of LD transmitters, a new idea called Master-Slave APC has been proposed which uses only one output power monitor circuit to control bias currents for all LDs on a chip. [9] A variety of integrated p-i-n photodetector arrays with 4 to 12 elements have been developed. Integration of an array of several receiver circuits has also been attempted using Si and GaAs. Gain, bandwidth, and crosstalk are essential issues, which require careful circuit layout on a chip which includes ground wiring. For minimizing circuit size and reducing tedious mounting procedure in the module fabrication, OEICs have a great deal of promise. Preliminary attempts have already been made to develop arrayed OEIC transmitters and receivers. [10]-[12] In the future, it will be necessary to introduce a data multiplexing scheme to accommodate a large number of channels in one link by taking full advantage of fiber's wide bandwidth and of high-speed characteristics of LDs. However, trade-offs must be done between performance, circuit complexity, cost, and the number of multiplexing.

Module design is another important issue. It is desirable that the module size is as small as that of electrical connectors. A key issue is how to achieve a highly-precise and low-cost parallel optical coupling structure. Direct coupling with butt-end fibers is the most simple one which is suitable for LEDs and photodiodes. Since optical coupling requirements are more stringent for LD arrays, a precise automated alignment method becomes inevitable for the manufacture.

4. Conclusion

The introduction of optical fiber interconnection will remarkably enhance performance and reduce size of advanced switching systems and computers. Current developments aim at to solve data transfer bottlenecks in large-scale high-performance systems by replacing their bulky electrical cables by fibers. In the future, the cost of fiber links will be reduced to expand their applications such as small PBXs, connection cables for distributed office workstations and even personal computers.

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Table 1 Recent parallel link development in Japan

Ch.	Speed (Mb/s)	Fiber	Distance (m)	λ (μm)	Light sources	Detectors	Ref.
12	150	62.5μm MM	100	1.3	LED array	PIN array	5
8	200	SM	100	1.3	LD array	PIN array	6
8	150	62.5 μm MM	200	1.3	EE-LEDs	PIN-PDs	7
4	2,000	50 μm MM	26	1.3	LD array	PIN array	8
4	2,500	SM	400	1.3	LD array	PIN array	9
6	1,000	50 μm MM	—	1.3	LD array	MSM-receiver array OEIC	11

MM : Multi-mode
SM : Single-mode

Low-Responsivity GaAs/AlAs Asymmetric Fabry-Perot Modulators

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Absorption-based light modulators are attractive because they can be made compact and in high densities, operating with light normal to the plane of the device. The *intrinsic* power dissipation of such a modulator is simply the absorbed optical power, which (neglecting radiative recombination) must be dissipated in the device. However, most of the total dissipation in electrically-driven multiple quantum well (MQW) modulators operating with light incident normal to the device plane is *non-intrinsic*, resulting from motion of photo-generated carriers in externally applied electric fields. For example, in a *pin* MQW device biased to 5 V, motion of photo-generated electron-hole pairs through the *total* potential $= V + V_{bi}$ deposits about 6.3 eV of energy, 5 eV of which is *non-intrinsic*. Minimizing the overall dissipation in these devices is important, because it ultimately determines the packing density and the maximum optical input power.

We have studied several MQW *pin* samples, each of which was grown on a quarter-wave dielectric reflecting stack mirror consisting of $Al_{0.11}Ga_{0.89}As$ and AlAs layers. Devices contained 60 periods of GaAs quantum wells 100 Å thick with 60 Å $Al_xGa_{1-x}As$ barriers having mole fractions of x=0.3, 0.45, and 1.0. We have previously reported the behavior of the x=0.3 devices.[1] Devices were implanted with roughly 130 keV protons, focusing the damage into the intrinsic regions, to dose levels of $1 \times 10^{12}\,cm^{-2}$, $1 \times 10^{13}\,cm^{-2}$, and $1 \times 10^{14}\,cm^{-2}$. Large area mesa devices were then fabricated from these structures via standard lithographic techniques. Measurements of reflectivity and responsivity were made on all devices, using a lamp monochromator. Devices were studied both before and after being anti-reflection (AR) coated. Intensity dependent measurements were made on the AlAs barrier samples. We found that photocurrent suppression became more pronounced with increasing Al mole fraction, with AlAs barrier samples showing the highest degree of depressed responsivity. We focus now exclusively on the AlAs barrier sample.

In AlAs barrier samples, responsivity is voltage dependent even in unimplanted samples. When implanted, this suppression becomes very pronounced and remains so to high bias levels. In Fig.1, we illustrate the responsivity at the relevant Fabry-Perot resonance for non-AR-coated devices that were unimplanted and implanted to levels of $1 \times 10^{12}\,cm^{-2}$ and $1 \times 10^{13}\,cm^{-2}$. Clearly, responsivity is strongly depressed with implantation dose. At 12.5 V, responsivity is 57 times lower in $1 \times 10^{13}\,cm^{-2}$-implanted devices relative to unimplanted devices. Measurements with low duty cycle pulses demonstrate that this suppression persists to intensities of at least $60\,kW/cm^2$. Thermal shift of the bandgap with continous illumination tends to increase responsivity, but not dramatically. We have previously interpreted these phenomena as being due to a dramatic reduction in the nonradiative carrier lifetime due to introduction of recombination centers from proton implantation.[1]

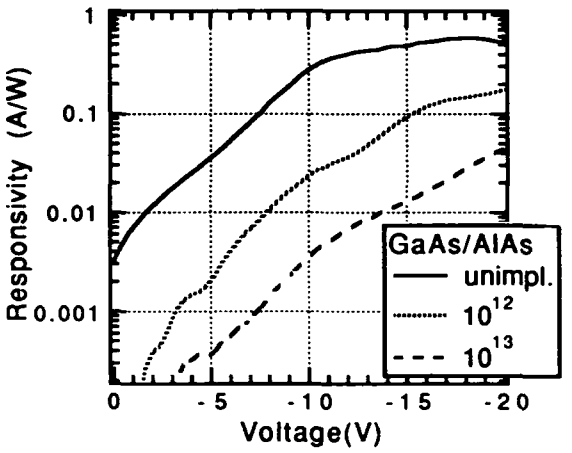

Figure 1.1: Responsivity vs. voltage for AlAs barrier devices implanted to levels of 0, $1 \times 10^{12}\,cm^{-2}$, and $1 \times 10^{13}\,cm^{-2}$ for wavelength near 856 nm.

Non-AR-coated devices form Asymmetric Fabry-Perot (ASFP) Modulators.[2] A Fabry-Perot resonance exists near 856 nm. For laser illumination near this wavelength, Fig. 2 depicts the reflectivity as a function of bias for three devices, unimplanted, implanted to $1 \times 10^{12}\,cm^{-2}$, and implanted

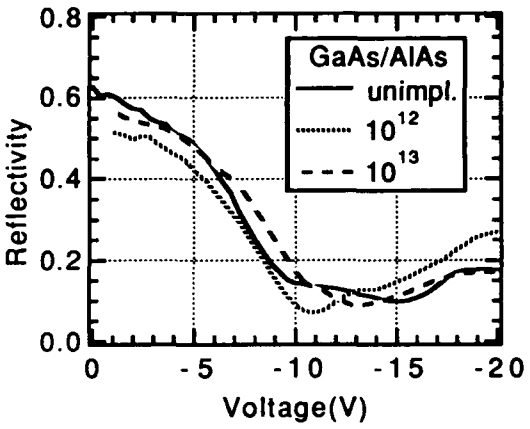

Figure 1.2: Reflectivity vs. voltage for AlAs barrier devices implanted to levels of 0, $1 \times 10^{12}\,\mathrm{cm}^{-2}$, and $1 \times 10^{13}\,\mathrm{cm}^{-2}$ near 856 nm.

to $1 \times 10^{13}\,\mathrm{cm}^{-2}$. As can be seen, reflectivity is essentially similar for the three devices. The penalty paid in terms of modulation performance for implanting these ASFP devices is thus negligible. This performance relies on the presence of the Fabry-Perot resonance. AR-coated (*i.e.* non-Fabry-Perot) devices show degraded modulation performance with implant dose, because of a progressive broadening of the exciton absorption feature. In AR-coated devices, this feature determines the modulation performance, while in ASFP devices it is the Fabry-Perot resonance in conjunction with the exciton and bandedge absorption that determines performance. Experimentally, we find that this performance is tolerant to moderate levels of exciton broadening. This performance is maintained to CW intensities at least 2.2 mW ($\sim 30\,\mathrm{kW/cm^2}$). AR-coated devices and exciton saturation intensities in these structures are discussed in a submission to the Quantum Optoelectronics Topical meeting co-located with this conference.[3]

There are several practical applications for suppressed photocurrent modulators. In general, they may be used in any application where modulation is required, but where photocurrent is non-essential or even detrimental. Without photocurrent, the modulator presents a minimum, purely capacitive, electrical load to its driving circuitry. When photocurrent is present, this load increases in proportion to the photocurrent, thus presenting a larger, and power dependent, load. The result of this is that driving circuitry must be larger (dissipating more power), and must be designed with some idea of the power to be modulated. This is particularly important when driving circuitry is integrated together with the modulator, as in recently described FET-SEED optoelectronic integrated circuits (OEICs).[4]

Point-source heating effects limit the maximum power handling capacity of MQW modulators, with the major component of this being due to ohmic heating (for bias levels greater than a few volts).[5] In these devices, the implanted device has a maximum responsivity of 0.007 A/W at 12.5 V, which, for 1 mW incident power, corresponds to a current of 7 μA. For 50 % duty cycle operation, this would correspond to an excess electrical power dissipation of 44 μW, compared to the average optical power absorption of 650 μW (60 % to 10 % change in reflectivity). By comparison, a conventional MQW modulator device would have high responsivity at 12.5 V (0.5 A/W) which would contribute an additional electrical dissipation of 3125 μW, 4.4 times the optically absorbed power.

When compared to a typical surface emitting laser, the electrical power dissipation issue becomes very striking. The best reported electrical efficiencies of surface emitting lasers are less than 10 %: for 0.5 *mW of output power, more than 5 mW of electrical* power is dissipated in the structure, and must be supplied by electrical drive circuits.[6] For 50 % duty cycle operation, this represents an average electrical load of at least 2.5 mW. This is less than the hypothetical high-responsivity 12.5 V modulator described above, which sinks an average electrical load of about 3.8 mW. This compares favorably to a photocurrentless modulator, which dissipates a *total* power of about 0.7 mW, and presents an electrical load that is *power-independent* and entirely capacitive. Of course, *low-voltage* modulators are also possible, in which case the power consumption advantages of suppressed photocurrent become less pronounced.[7] However, the dissipation of such devices is entirely *electrical* in nature, and their modulation performance is not as good as that which can be achieved with higher voltage designs.

There are a number of applications for OEICs in which there is a need for both modulators and detectors, particularly for FET-SEEDs. The selective nature of this process makes it highly attractive in such applications, because one may produce suppressed responsivity devices selectively on the OEIC, leaving other areas untouched. Unfortunately, the particular case presented here suffers from the drawback that

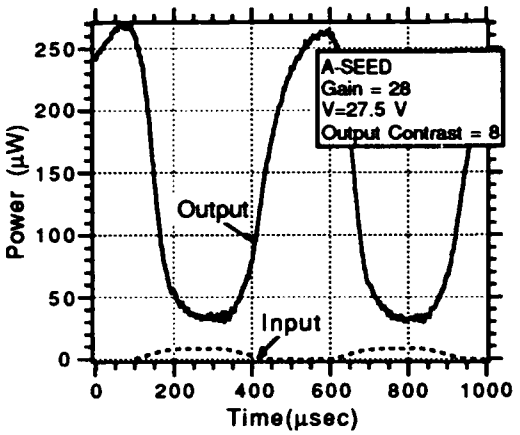

Figure 1.3: Input-Output characterstics of A-SEED device formed with unimplanted and $1 \times 10^{13}\,cm^{-2}$ implanted AlAs barrier devices.

the unimplanted device has relatively poor responsivity at low bias and saturates at low optical power, and is consequently not a very good detector. It is possible that this device could be refined such that unimplanted detection qualities could be improved.

Asymmetric self-electro-optic effect devices (A-SEED) devices are another example of powerful device concepts that are enabled by suppressed photocurrent devices.[1] The current device, since it suffers basically no degradation in modulation performance, makes an excellent A-SEED, as illustrated in Fig. 3. This circuit was formed by combining an unimplanted and an implanted (to $1 \times 10^{13}\,cm^{-2}$) device in series, as described previously.[1] Since the voltage across the series pair will divide based on the currents flowing through the two devices, it is clear that a low power beam incident on the unimplanted device can control a much higher power beam falling on the unimplanted device. For the particular case illustrated a gain of 20 is obtained with an output contrast ratio of better than 5. Since this device allows a low power beam to control a high power beam, it may be viewed as a sort of optical transistor. A drawback of the simple device as demonstrated here is that bias is switched from one device to the other via photocurrent, and when the unimplanted device is in its low absorbing state and the implanted device is in its absorbing state, there is not very much photocurrent generated. Thus, the A-SEED is asymmetric in it's switching properties. This can be remedied by increasing the optical power on the implanted device, or by decreasing the level of photocurrent suppression, or by making a fully differential, four-port device in which two high responsivity detectors are used to control two low responsivity modulators.

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High-Contrast Modulation of Asymmetric Fabry-Perot Modulators at 20 GHz

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Summary—Since their introduction in 1989 [1,2], asymmetric Fabry-Perot modulators (AFPMs) have attracted a great deal of attention because of their high efficiency (high contrast, low insertion loss, and low voltage) and the fact that their surface-normal configuration is particularly compatible with fiber optics and with proposed architectures for parallel optical free-space image processors and interconnection systems. In addition to their other virtues, AFPMs also have the potential for extremely high speed operation. Last year we demonstrated small-signal modulation of AFPMs to 21 GHz [3], and recently we have predicted that speeds in excess of 40 GHz may well be possible. [4] This capacity for high speed operation makes AFPMs suitable for high-speed photonic switching applications in which the optical switches are "smart" — that is, they perform functions on the data stream at the data rate, rather than simply switching packets at some slower rate.

From our 21 GHz small-signal measurements, we concluded that the modulation speed of AFPMs seems to be *RC*-limited (at optical intensities well below the exciton saturation point). We based our speed predictions on *RC* limits alone, surmising that, because the speed of the quantum-confined Stark effect relies on the rate at which the field switches, and not on the collection rate of the carriers, quantum-well modulators in general will not be limited by transit-time at low optical powers. To test whether our hypothesis still holds for large-signal modulation, we designed a layer structure with a wide intrinsic region which minimizes the device capacitance while maintaining high-contrast, low-voltage-swing operation. Then we employed our high-speed modulator fabrication process [3] to realize 16 x 20 μm diodes with low resistance and capacitance. Here we present the optical and electrical characterization of these devices, demonstrating that they are indeed capable of large signal (high contrast, low insertion loss) modulation at frequencies near 20 GHz for moderate optical intensities.

The asymmetric Fabry-Perot modulator (Fig. 1) consists of a MQW *p-i-n* diode sandwiched between mismatched quarter-wave stack mirrors. In the zero-bias, low-absorption state, the reflectivity is high (typically ≥ 50%). Applying an electric field across the *p-i-n* diode increases the cavity absorption via the quantum-confined Stark effect, effectively decreasing the back mirror reflectivity to balance that of the front mirror and null out the reflected signal. The most efficient material structure for an AFPM employs a high front mirror reflectivity to increase the effective interaction length of the device, shortening the MQW intrinsic region width required to reach the critical absorption, and consequently lowering the voltage. [5] Unfortunately, narrowing the intrinsic region also increases device capacitance, so there emerges a basic trade-off between capacitance (speed) and voltage swing. [4] By working well off the absorption edge, however, we were able to obtain a sufficient absorption contrast to guarantee large-signal operation with a relatively small electric field change, and thus a reasonable AC voltage swing.

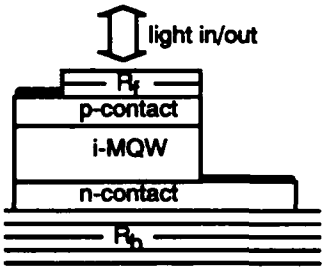

Fig. 1 AFPM structure.

The final material structure, consisting of front and back mirrors with reflectivities of 52% and 99% respectively, a 1-μm MQW operating region composed of 80 100-Å GaAs quantum wells with 45-Å $Al_{0.2}Ga_{0.8}As$ barriers, and 0.6-μm-thick $Al_{0.1}Ga_{0.9}As$ intracavity contact layers doped to $2x10^{18}$ cm^{-3}, was grown by molecular beam epitaxy. We fabricated 16 μm x 20 μm modulators integrated with coplanar microwave probe pads (Fig. 2) using a self-aligned reactive-ion etching (RIE) process, the details of which have been reported previously. [3]

Measured wavelength spectra for the finished devices at various bias voltages (Fig. 3) demonstrate the efficient operation of the modulators at DC. The measured contrast was about 15:1 for a 5 V bias change but in reality the contrast for these modulators is much larger — indeed arbitrarily large at one particular wavelength. In our case much of the measured residual reflection was due to spurious reflections from the periphery of the

laser spot, which was a bit too large for the device, rather than reflection from the device window. Simply adding a length of single-mode optical fiber to serve as a spatial filter increased the contrast to 30 dB or more for a 5 V change in bias, while maintaining an insertion loss of 3 dB.

Fig. 2. Scanning electron micrograph of finished 16 μm x 20 μm device with integrated coplanar microwave probe pad. The optical window is 15 μm x 15 μm.

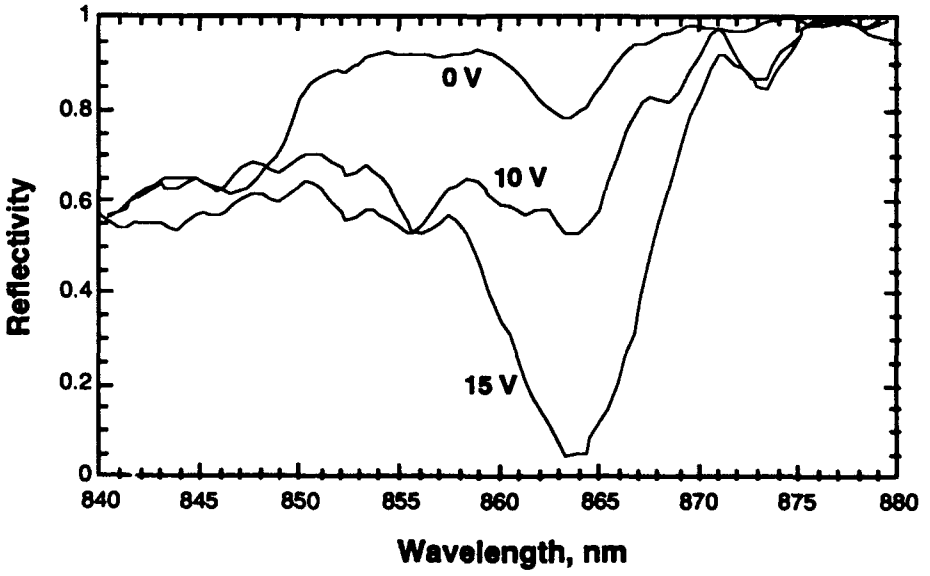

Fig. 3. DC spectra of finished 16 μm x 20 μm device

We extracted the device model in Fig. 4 from network-analyzer meaurements of the devices and probe pad patterns. The RC-limited bandwidth predicted from this model is

$$f_{3dB} = \frac{1}{2\pi[C_d(R_s+Z_o)+C_{pad}Z_o]} = 37\ \text{GHz}.$$

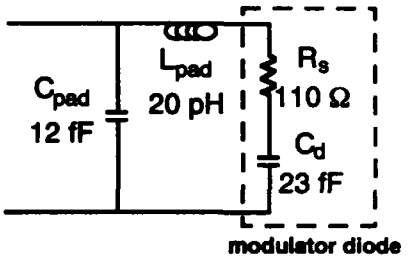

Fig. 4. Equivalent circuit

At optical power levels for which the device is transit-time limited, the bandwidth will be considerably lower, depending on the speed with which the carriers can escape the quantum-well material. Pump-probe measurments suggest that the carrier sweep-out time for comparable quantum-well material and electric fields is about 10 ps, which corresponds to a transit-limited bandwidth of 16 GHz. [6]

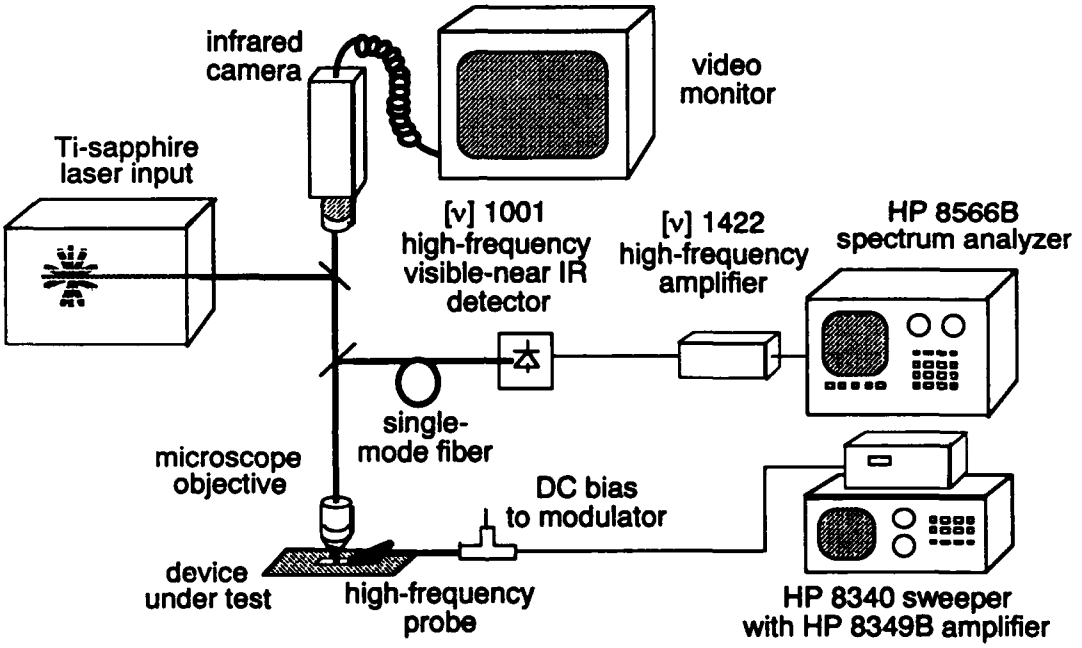

Fig. 5. 2-20 GHz swept-frequency measurement apparatus.

Using the measurement apparatus pictured in schematic in Fig. 5, we measured the frequency dependence of the AFPM's modulation directly by sweeping the frequency of the microwave drive signal and the spectrum analyzer simultaneously. Subsequently, we measured the roll-off of the various active and passive components and subtracted them from the raw data to obtain the calibrated frequency dependence of the AFPM alone (Fig. 6). From the curves in Fig. 6 we see that, just as in our earlier small-signal measurements, the modulators are transit-time limited at the higher optical intensity levels, in this case to a bandwidth of 18 GHz, which corresponds to a transit time of about 9 ps. At lower optical intensities, however, their bandwidth exceeds this transit-time limit, and, indeed, the capabilities of our measurement system.

For this experiment we applied a 11.5 V DC bias, and a 14 dBm microwave drive signal (corresponding to a 6 V swing). At low optical intensities (≈80 μW on the device), they switched about 60 μW at 20 GHz, with 18 dB contrast and 1.5 dB insertion loss. At higher optical intensity levels (≈ 500 μW), the AFPMs switched about about 350 μW with >20 dB contrast and 1.5 dB insertion loss at 2-3 GHz. At 18 GHz, the optical modulation was ≈125 μW. With this high-speed performance, AFPMs should find exciting applications in fast "smart pixel" photonic switching and interconnection systems.

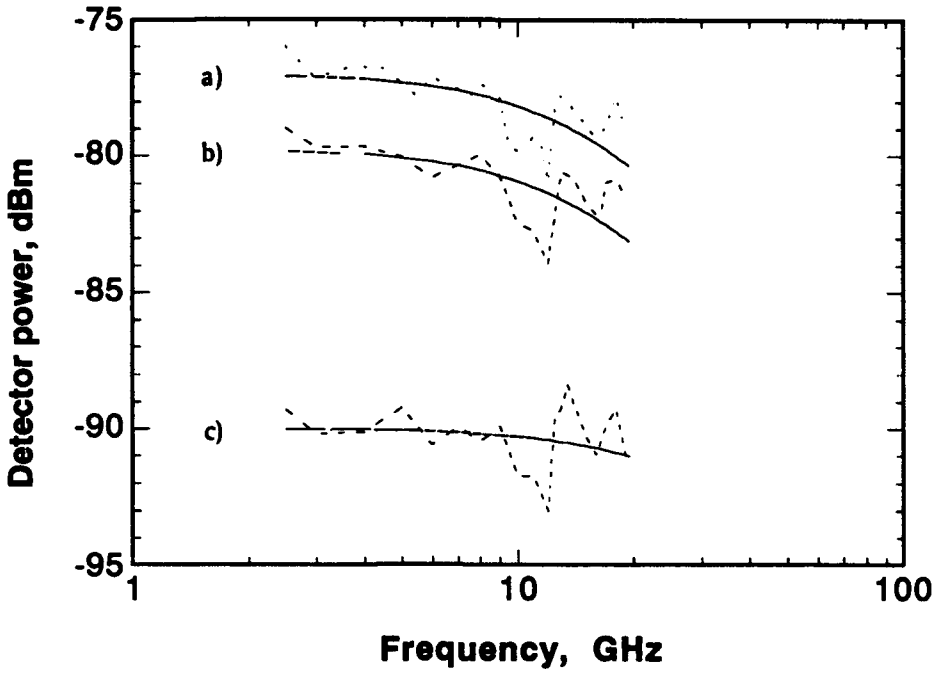

Fig. 6. Swept-frequency modulation measurements at three optical power levels: a) 550 μW, b) 400 μW c) 80 μW. Solid lines are theoretical curve fits corresponding to f_{3dB} = 18 GHz, 18 GHz, and 37 GHz, respectively.

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A complexity analysis of optically implemented shuffle equivalent interconnection topologies based on computer generated binary phase gratings

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I. Introduction

Free-space digital optics (FSDO) is an evolving interconnection technology that may permit signals to be routed between digital integrated circuit chips as beams of light propagating orthogonal to the plane of the device substrates. In switching systems, FSDO can be used to provide high-density, high-bandwidth, low-energy, low-noise connections between the nodes in multi-stage interconnection networks (MINs).[1] In this paper, various MIN architectures are examined and compared to determine the complexity and feasibility of their associated optical implementations. In particular, the paper explores efficient means of implementing two well-known interconnection topologies (the 2-banyan and the 4-shuffle) and two novel interconnection topologies (the segmented-2-shuffle and the 4-banyan) using computer generated, space-invariant binary phase gratings. The paper also studies the effects of node-type and interconnection topology on the laser power requirements and the optical component requirements within the system. The general class of networks known as Extended Generalized Shuffle (EGS) networks will be used as a baseline for the analysis. The results should help identify optimum architectural parameters (node-type and interconnection topology) given the constraints of FSDO technologies.

II. EGS networks based on free-space digital optics

An N-input EGS network is comprised of three distinct sub-sections: the fanout section, the MIN switching section, and the fanin section (Fig. 1).[2] By modifying the number of nodes per stage (M), the number of stages (s), the node-type, and the interconnection topology, many different types of EGS networks can be created. Most of the EGS node-types (except for the simple 2-input crosspoint known as a 2-module) can described using a simple triplet notation (n,m,c), where n represents the number of node inputs, m represents the number of node outputs, and c represents the node capacity.[3] Within this paper, network designs containing five different types of nodes will be analyzed: the 2-module, the (2,1,1) node, the (2,2,2) node, the (4,1,1) node, and the (4,4,4) node. EGS network theory permits designers to determine the actual number of nodes required for strictly non-blocking operation. For example, a strictly non-blocking N=256 EGS network constructed from 2-modules requires M_{2-mod}=3840 nodes per stage and S_{2-mod}=11 stages.[2]

The hardware requirements for all five node-types will be referenced to the hardware requirements for systems based on 2-modules. Values for networks based on other node-types can be approximated from EGS network theory. For (2,1,1) nodes, the network requires s≈S_{2-mod} stages and M_{2-mod}/2 nodes per stage. For (2,2,2) nodes, the network requires s≈S_{2-mod} stages and M_{2-mod}/4 nodes per stage. For (4,1,1) nodes, the network requires s≈S_{2-mod}/2 stages and approximately M_{2-mod}/3 nodes per stage. For (4,4,4) nodes, the network requires s≈S_{2-mod}/2 stages and approximately M_{2-mod}/11 nodes per stage.

III. Interconnection topologies based on binary phase gratings

A very simple arrangement of optical components that can provide many useful interconnection patterns is shown in Fig. 2. This arrangement is based on a simple 2-lens, infinite conjugate, telecentric imaging system set up to provide 4f imaging. However, one or more space-invariant binary phase gratings are added at the pupil plane between the two imaging lenses to diffract the light and provide the necessary beam-steering operations.[4] (For example, the 1x3 grating in Fig. 2 diffracts the light into three distinct orders that are symmetric about the zeroth order). An optional magnification system can also be added at the output of the telecentric imaging system to correct for spacing differences between the object plane

and the image plane. This magnification system sometimes requires anamorphic components. An optional array of lenslets can also be added in front of the receiving device array.

For 2-input, 2-output switching nodes, EGS networks require interconnections that are topologically equivalent to the 2-shuffle (Fig. 1). Two such networks are the 2-banyan (Fig. 3) and the segmented-2-shuffle (Fig. 4). For 4-input, 4-output switching nodes, EGS networks require interconnections that are topologically equivalent to the 4-shuffle. Two such networks are the 4-banyan (Fig. 5) and the 4-shuffle (Fig. 6). If there are 2^m nodes per stage, the 2-banyan is defined by the mapping function from node U in stage i to node Z in stage i+1:

$$Z = U - 2^{m-i-1}\left\lfloor U/2^{m-i-1}\right\rfloor + 2^{m-i}\left\lfloor U/2^{m-i}\right\rfloor + 2^{m-i-1}\theta, \tag{1}$$

where θ is an element of $\{0,1\}$. The segmented-2-shuffle is defined by the mapping function:

$$Z = 2U - 2^{m/2}\left\lfloor 2U/2^{m/2}\right\rfloor + 2^{m/2}\left\lfloor U/2^{m/2}\right\rfloor + \theta, \quad \text{if } 0 \le i < m/2 \tag{2}$$

$$= U - 2^{m}\left\lfloor 2U/2^{m}\right\rfloor + 2^{m/2}\left\lfloor U/2^{m/2}\right\rfloor + 2^{m/2}\theta, \quad \text{if } m/2 \le i < m-1,$$

where θ is an element of $\{0,1\}$. The 4-banyan is defined by the mapping function:

$$Z = U - 2^{m-2i-2}\left\lfloor U/2^{m-2i-2}\right\rfloor + 2^{m-2i}\left\lfloor U/2^{m-2i}\right\rfloor + 2^{m-2i-2}\theta, \tag{3}$$

where θ is an element of $\{0,1,2,3\}$. The 4-shuffle is defined by the mapping function:

$$Z = 4U - 2^{m}\left\lfloor 4U/2^{m}\right\rfloor + \theta, \tag{4}$$

where θ is an element of $\{0,1,2,3\}$. If these interconnection patterns are to be used in networks based on FSDO, they must be modified to capitalize on the 3D nature of optical interconnections that can be used to interconnect 2D device arrays. The 2-banyan and the segmented-2-shuffle can both be implemented as 3D networks. If there are D columns in the planar device array (where $D=2^d$), then the new row-column address (X,Y) of each node U is given by:

$$(X,Y) = \left(\left\lfloor U/2^{d}\right\rfloor, U - 2^{d}\left\lfloor U/2^{d}\right\rfloor\right) \tag{5}$$

The 4-shuffle and the 4-banyan can also be implemented as 3D networks, where the resulting 4-shuffle network has come to be called the separable shuffle.[5] If there are 2^m nodes per stage and the binary address of each node is given by $U=(u_m u_{m-1} \cdots u_2 u_1)$, then the new row-column address (X,Y) of each node U is given by:

$$(X,Y) = (u_m u_{m-2} \cdots u_4 u_2 \quad , \quad u_{m-1} u_{m-3} \cdots u_3 u_1). \tag{6}$$

For brevity, the 3D interconnection patterns are not drawn within this paper, but the interested reader should be able to re-create the patterns using Eq. 5 and Eq. 6.

IV. Analysis of optical interconnection implementations

It can be shown that the interconnection patterns described above can all be provided by the optics in Fig. 2 if appropriate gratings are used (see Table 1). For example, Fig. 7 shows the optics required for a 2-banyan connection between (2,1,1) nodes (which uses the 1x3 grating of Fig. 2). Comparisons can be made between the different optical implementations using power requirements as a measure of the efficiency. In addition, the analysis can consider the type and number of binary phase gratings that are required. Finally, one can assess the need for spacers between nodes within the device array to absorb undesired output spots, the need for an additional magnification system, and the need for anamorphic components. Ten different arrangements of nodes and interconnections are analyzed and compared, and for each arrangement, the power requirements are calculated for a system with output lenslets and a

system without output lenslets. Performance values from actual operating systems are used within the analysis. Thus, it is assumed that the transmittance of any 1xY linear binary phase grating is given by 80 percent and the transmittance of any XxY 2D binary phase grating is given by 65 percent. It is also assumed that the nodes in the analysis are constructed using smart pixels with single-rail data. The size of of the modulator is fixed at a minimum value by the resolution of the optics, so the size of an ideal detector is equal to the modulator size. To drive a detector with this ideal size at the desired bit-rate, the amount of optical power that must arrive at the window is P_{det}. If a larger detector window is required, the capacitance of the detector is proportionally increased. The results of the analysis are outlined in Table 1.

V. Conclusions

Each of the ten arrangements of nodes and optical interconnections in the previous section has its own unique set of advantages and disadvantages. From Table 1, it becomes clear that the choice of a particular node and interconnection pattern can have a very large impact on the performance of the optical implementation. In addition, the use of extra hardware (such as lenslets) within the interconnection optics can oftentimes yield greatly improved power efficiencies within the system. Given the constraints placed on the design problem within this paper, it appears that a network based on (2,1,1) nodes connected by the 2-banyan interconnection or a network based on (2,2,2) nodes connected by the 2-banyan interconnection will yield the best results based on power utilization if lenslets are not added to the system. If lenslets are used, then a network based on (2,2,2) nodes connected by the segmented-2-shuffle yields the highest power utilization, but this interconnection scheme requires anamorphic components to provide additional magnification. Thus, the optimum choice of a node and the associated interconnection optics can only be made after considering the overall system requirements. Given the current state of the technology, smaller node sizes tend to be more desirable for system implementations.

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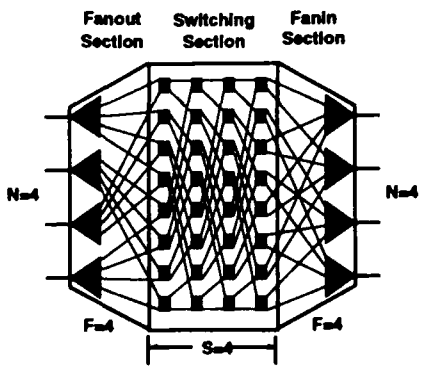

Fig. 1. EGS network.

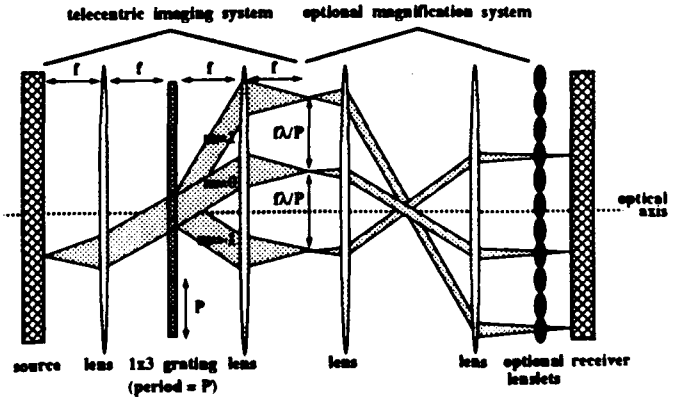

Fig. 2. Optical components used for interconnection.

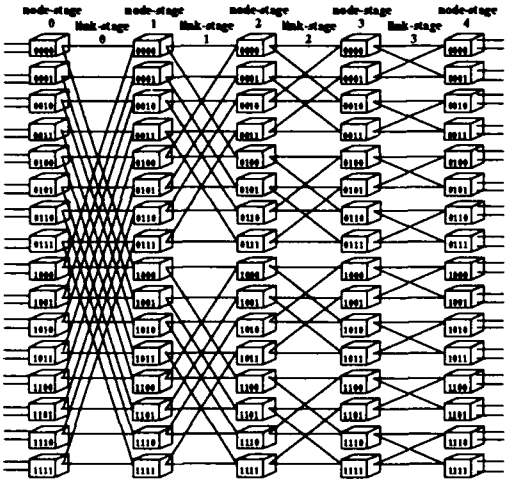

Fig. 3. 2-banyan network with N=32 inputs.

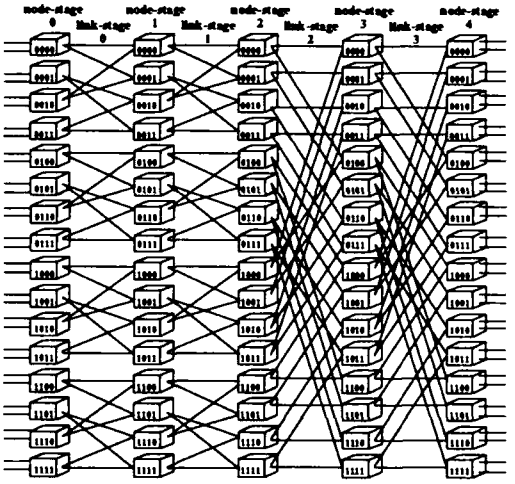

Fig. 4. Segmented-2-shuffle network with N=32 inputs (segment size H=4).

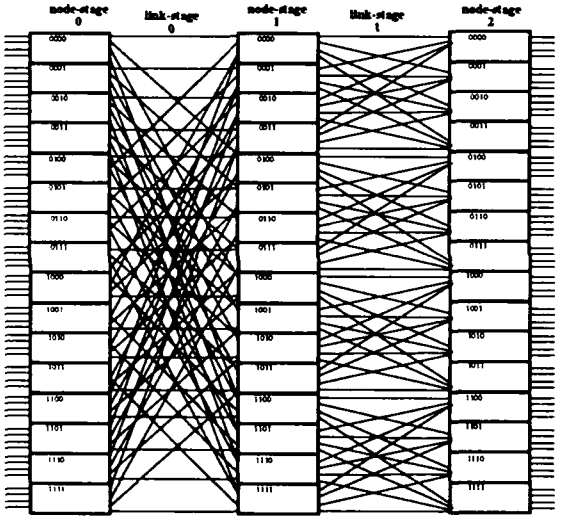

Fig. 5. 4-banyan network with N=64 inputs.

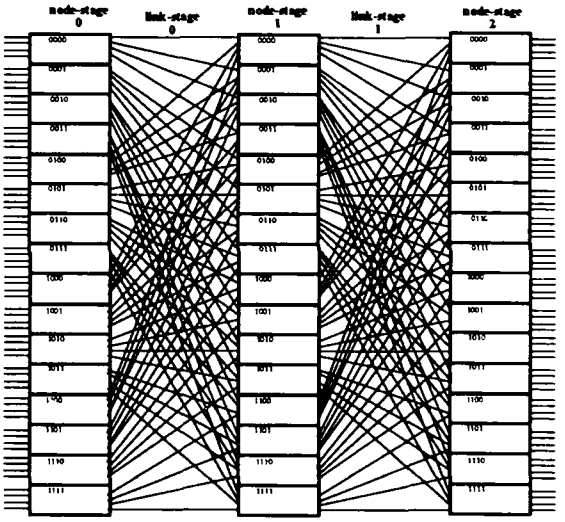

Fig. 6. 4-shuffle network with N=64 inputs.

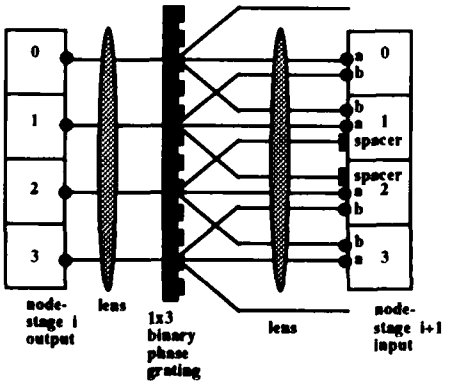

Fig. 7. Schematic representation of optics required for 2-banyan connections between (2,1,1) nodes. (Note: This is not a ray-trace; image inversions not shown).

arrangement	relative power per stage without lenslets ($\propto P_{det} M_{3\times3}$)	relative power per stage with lenslets ($\propto P_{det} M_{3\times3}$)	gratings req'd?	spacers req'd?	add'l magn. req'd?	anamorphic components req'd?
2-mod / seg.-2-shuffle	12.5	6.25	1x2, 1x2	N	Y	Y
2-mod / 2-banyan	7.5	7.5	1x3	Y	N	N
(2,1,1) / seg.-2-shuffle	6.25	3.125	1x2, 1x2	N	Y	Y
(2,1,1) / 2-banyan	1.875	1.875	1x3	Y	N	N
(2,2,2) / seg.-2-shuffle	2.5	1.25	1x2	N	Y	Y
(2,2,2) / 2-banyan	1.875	1.875	1x3	Y	N	N
(4,1,1) / 4-shuffle	50.5	12.625	2x2, 2x2	N	Y	N
(4,1,1) / 4-banyan	4.6	4.6	3x3	Y	N	N
(4,4,4) / 4-shuffle	9	2.25	2x2	N	Y	N
(4,4,4) / 4-banyan	5	5	3x3	Y	N	N

Table 1. Comparison of different node & interconnection arrangements. (P_{det} = detector power, $M_{3\times3}$ = # 2-mod nodes needed for non-blocking)

Optical FDM Switching

PTuB 10:30am-12:20pm
Grand Ballroom East

Ivan P. Kaminow, *Presider*
AT&T Bell Laboratories

PRESENT AND FUTURE OF FDM PHOTONIC SWITCHING

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1. Prologue

An FDM (Frequency Division Multiplexing) photonic switching system is a very promising system in that it is only feasible by photonics. It utilized enormous bandwidth of lightwave and is independent of transmission methods and bit-rate. This system seems more suitable for the coming broadband age than ATM-based systems because in future they will provide us with an infrastructure for more flexible and lower cost telecommunication networks.

In the first half of this paper, we would like to mention about the present status of photonic FDM switching systems and devices. In the latter half of this paper, we will suggest a novel FDM photonic switching system. There are problems inherent in an FDM photonic switching system, and some consideration will be also made to these problems.

2. Photonic technologies for switching

Photonic switching technologies are divided into 4 categories; SD (Space Division, TD (Time Division), free-space and FDM or WDM (Wavelength Division Multiplexing).

Time division requires massive memories and massive logical devices such as LSIs. Fiber delay lines are often used for memories but they cannot substitute memories in that reading-out of informations memorized in fibers cannot be controlled. Bistable devices like SEEDs[1] have a possibility of realizing timing regeneration and waveform regeneration, and might be used for ATM photonic switching systems. But header processing by photonics still remains unsolved, and some electronics will be needed to achieve the functions. Unless we have some unique devices for photonic gates and memories which surpass electronics, we should take advantage of the bandwidth-free and bitrate-free characteristics of photonics.

As far as the switching devices are concerned, photonic SD is rather mature, and comparison with electronic switching is not 'anecdotal'. We might say that space division photonic switching systems are now at the stage of how to introduce into a network.

Free space is an extended version of space division technology. FDM photonic switching is also considered another enhancement technology of SD. FDM increases the multiplicity in transmission lines just as TDM, thus decreases the physical size of SD systems. FDM will decrease SD system cost and will give more possibility of commercial introduction.

One of evolution scenarios of a telecommunication network is

shown in Fig.1.

First, in order to respond to various service demands from subscribers, FDM is to be introduced into local networks for effective use of FTTH. Then, FDM will go to trunk networks to accommodate growing needs for higher bitrate, this neccesitates the introduction of FDM crossconnect, or photonic FDM switching. It is not unreasonable to estimate that the ultimate goal of the telecommunication network be an integration by photonic FDM.

3. Present status of FDM switching

Functions needed to perform FDM switching are frequency synchronization, frequency shifting and spacial switching as is illustrated in Fig.2. These functions correspond to clock synchronization, time switching and space switching in TDM switching systems.

Frequency synchronization means identifying all the carrier frequencies incoming from the different transmission lines, i.e., all incoming frequencies should be converted to the standard frequencies switchable in the system. Frequencies shifting means performing switching between different frequencies, and spacial switching means switching between the same frequency on the differnt fibers.

As for literatures on photonic FDM switching, systems are not found which implement all of the above mentioned functions. FDM (or WDM) is used for a small closed system, such as for buses or for loops. LAMBDANET[2] is a 16 channels bus network, in which frequencies are used as routing tags.

FDM photonic switching systems have been proposed since several years ago[3], in which frequencies are used to increase the multiplicity of the links connecting each switching stage. Some proposed mixed TDM/FDM systems. ATM switching systems using FDM technologies are also reported. Essential devices for a FDM system are frequency converters and frequency filters. There are not so many papers on frequency converters, but we have many papers on variable frequency filters. Studies on passive filters are more active than on active filters. Maximum multiplicity so far realized is 100[4].

4. Proposal of a unique FDM switching system

Here, we would like to propose a unique photonic FDM system which ingeniously avoids frequency synchronization and conversion problems, thus maintaining bitrate-free and transmission method-free characteristics.

The basic idea of this system is to assign a specific frequency to a call, a dialog between a calling and called subscribers. This concept is shown in Fig.3. A specific optical frequency is to be found out by the processor of the network in which all the information about the network resources such as switching systems and transmission lines are centralized. This photonic FDM network consists of n independent sub-networks (n is the number of frequencies used in the proposed photonic network). This network reduces the size of the present network to 1/n. Physical struc-

ture of this proposed network is shown in Fig.5. As is shown, subscriber lines as well as trunk lines are FDM multiplexed, thus the subscriber network is also reduced.

One of the features of the network is an elimination of the frequency conversion devices. Switch matrix structure in this system is shown in Fig. 4., which has only frequency filtering and no frequency conversion. The main target to be aimed in this system is to develop photonic frequency filters. The calling party should be able to send the optical frequency designated by the network. This means that the number of frequencies network should prepare is not necessarily equal to the number of subscribers. Traffic concentration can be done without the concentration stage which are usually equiped for efficient use of switching equipment and transmission equipment.

If we assume concentration ratio is 5, number of available frequencies are 1000, we can easily configure a switching system which accomodates as much as 5 million subscribers with only a 1000 input x 1000 output switching matrix. This is illustrated in Fig. 6.

5. Problems to be considered

The basic device needed to realize this photonic switching system is a frequency filtering device, but there are many problems and following items should be considered.

(1) Frequency stability

When it comes to switching informations on various incoming lines to a specific output line, the modulated various photonic frequencies sent from terminals on different locations should be multiplexed without any overlap on spectral domain. In order to attain this, every frequency generated and sent by all the terminals in the network should be same. Practically, it is impossible to require for all the terminals independently generating the absolutely same frequencies. Therefore, the network should generate and distribute the frequencies to the terminals. At present, in the digital network we have very stable network clock, which is distributed to all the nodes and transmission equipments and terminals. In photonic FDM network exactly the same analogy applys in frequency domain.

(2) Frequency multiplicity

The multiplicity can be decided by various parameters of the network components such as fibers, light sources, receivers and frequency filters etc.. Frequency multiplicity is also dependent on whether the system is applied to the nation-wide network, or only to a local area network or MAN (Metropolitan Area Network). Maximum bitrate, modulation method would be another parameters to determine the frequency multiplicity.

(3) Transmission charactristics

Due to splitting and combining of the light, switching system has some insertion loss, which necessitates optical amplifications. In this sense the semicoductor active devices with some gain are desirable for crosspoints.

At present we have no photonic reshaping devices, and accumulation of noise and waveform distortions are inevitable. Loss

compensation by an optical amplifier unavoidably generates noises caused by spontaneous emission.

We must also consider that in FDM system crosstalks from ajacent channels occur owing to the filtering characteristics of the switch. Allowable loss and crosstalk level will be decided from system and network considerations.

Transmission and switching integration causes another very serious problem. Fourwave mixing occurs when many frequencies are transmitted for a long distance, depending on the fiber characteristics and optical power transmitted etc., this sets a severe requirement for the transmission length and the multiplicity of the frequencies.

(4) Switching time

The FDM photonic switching sysems is essentially SD, so the requirement for the switching time is not so severe, and several milliseconds will be enough. But if we want to use this switch for time division systems such as TDM or ATM switching, a faster switching time is required.

6. Postscript

Present and future of the photonic FDM systems are outlined along with our new proposal. Essenstial device needed to realize FDM photnic system is frequency filters. More efforts should be directed to realize commercially available FDM filters, i.e. cost-effective, small-sized or integrated photonic filters.

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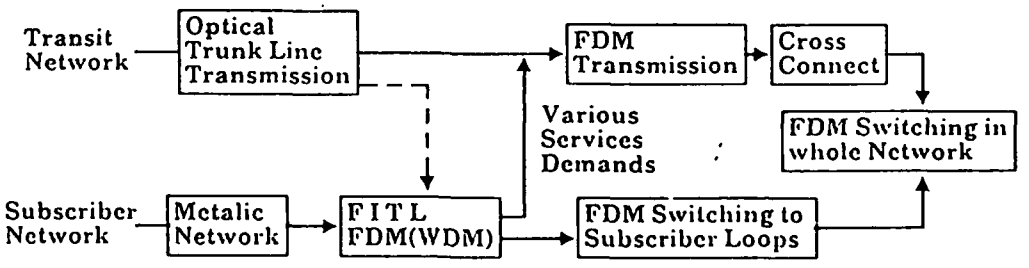

Fig.1 A Network Evolution Scenario

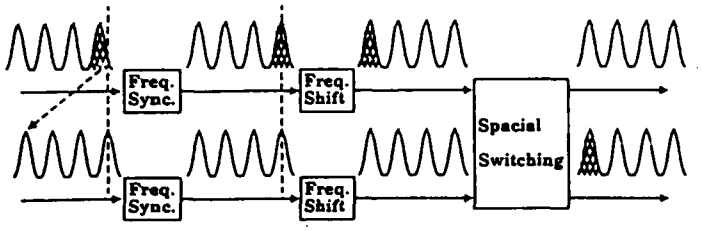

Fig.2 Principle of FDM Switching

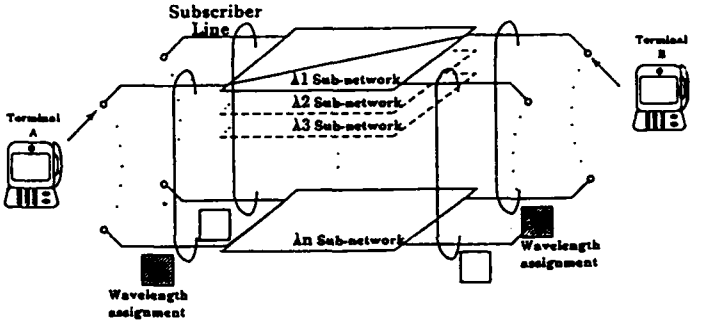

Fig.3 Logical Configuration

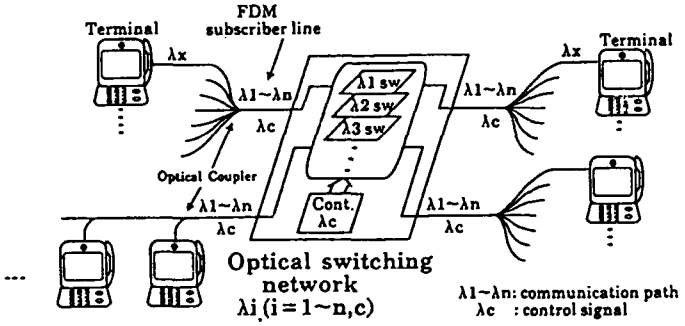

Fig.4 λ-Assignment Network

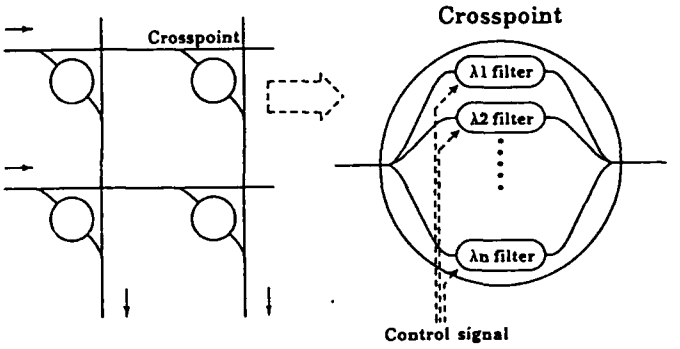

Fig.5 Switch Matrix

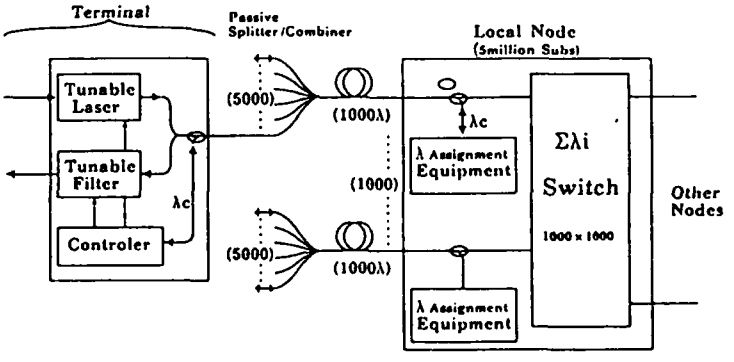

Fig.6 System Configuration

Signal transmission characteristics of a photonic FDM multichannel selector

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Introduction

Photonic frequency-division-multiplexing (FDM) systems have been widely studied recently to achieve large-capacity optical networks. We have previously proposed a multi-frequency-channel selector[1] using a coherent optical transversal filter[2]. This paper describes frequency characteristics and transmission characteristics of an experimental 8-ch multi-frequency-channel selector.

Photonic FDM highway switch

Figure 1 shows an FDM highway switch comprising M FDM input and output highways with N multiplexed frequency channels on each highway and M^2 multi-frequency-channel selectors. Each selector selects several arbitrary frequency channels out of N input frequency channels. For example, channels A and D on input highway 1 are switched to the output highway 1, while channels B and C are switched to the output highway M. Thus, this frequency multiplexed MxM switch matrix can equivalently work as N MxM space-division switch matrices. This system architecture is analogous to the TDM highway switch used in the present commercial network, where timeslots correspond to frequency channels.

FDM multi-channel selector using a coherent optical transversal filter

A multi-channel selector using a coherent optical transversal filter has been developed for use in the photonic FDM highway switch. The selector can select several arbitrary channels out of multiple multiplexed frequency channels, which utilizes that the filter can express arbitrary frequency characteristics. Transversal filters have three essential functions: delay, multiplication, and summation. A schematic diagram of an n-tap coherent optical transversal filter is shown in Fig. 2. The tapped delay-line structure consists of an optical waveguide with taps distributed at constant intervals along its length. Signals introduced into the filter are tapped, weighted, and then coherently combined. The three essential functions are expressible by optical components: optical-waveguide delay lines, tunable splitters and phase shifters, and optical couplers. Tunable splitters distribute optical signals to taps whose electric-field amplitude distribution ratio corresponds to the ratio of the absolute value $|a_k|$ of the complex tap coefficients. Phase shifters shift the optical carrier phase of tapped signals, which corresponds to the argument $\angle a_k$ of the complex tap coefficients.

The filter whose unit delay time is τ and whose number of taps is n can express a multi-channel selector of upto n channels in the frequency range τ^{-1}. The filter tap coefficients are determined using discrete Fourier transformation

$$a_k = \frac{1}{n} \sum_{m=0}^{n-1} t_m \exp(2\pi jkm/n) \quad (k=0 \sim n-1) \qquad (1),$$

where t_m (=1 or 0) is the transmission rate at the m_{th} frequency position. The frequency characteristics are given by

$$H(f) = \sum_{k=0}^{n-1} a_k \exp(-2\pi jk\tau) \qquad (2).$$

Frequency channel independence

For the switching systems application, each frequency channel is required to be switched from OFF to ON, or ON to OFF without effecting the other channels. Equations (1) and (2) can be rewritten as

$$a_k = \sum_{m=0}^{n-1} t_m a_{k,m} \quad (k=0 \sim n-1) \qquad (3)$$

and

$$H(f) = \sum_{m=0}^{n-1} t_m H_m(f) \qquad (4),$$

where

$$a_{k,m} = \frac{1}{n} \exp(2\pi jkm/n) \qquad (k=0 \sim n-1,\ m=0 \sim n-1) \qquad (5)$$

and

$$H_m(f) = \sum_{k=0}^{n-1} a_{k,m} \exp(-2\pi jkf\tau) \qquad (m=0 \sim n-1) \qquad (6).$$

The set of tap coefficients, $\{a_{k,m},\ k=0\sim n-1\}$, gives the frequency characteristic, $H_m(f)$, of 1-channel selection at the m_{th} frequency position. From Eq. (3), the set of tap coefficients, $\{a_k,\ k=0\sim n-1\}$, is a linear combination of orthogonal tap coefficient sets of 1-channel selection. Also from Eq. (4), frequency characteristic for multi-channel selection, H(f), is expressed as a linear combination of orthogonal 1-channel selecting frequency characteristics. Thus, each frequency channel can be independently switched by setting the transmission rate, t_m, to 1 or 0. These operations are illustrated in Fig. 3.

Experiment

An 8-channel selector was designed using a 16-tap coherent optical transversal filter. Optical components of the 16-tap filter (n=16) were constructed using silica-based single-mode waveguides embedded on a silicon substrate[3]. The effective waveguide lengths in the fabricated filter on a silicon wafer reach 60 cm. Its insertion loss, including the coupling loss between fibers and waveguides, is 15 dB. The unit delay-line length is 1 cm (τ is 50 psec), giving the frequency characteristic a periodic shape every 20 GHz.

With this selector, arbitrary s channels (s=0~8) can be selected out of 8 2.5-GHz equally-spaced channels ($f_1 \sim f_8$). The frequency characteristics were measured by sweeping the optical carrier frequency of a frequency-stabilized 1.3-μm YAG laser. The obtained and calculated frequency characteristics are shown in Fig. 4. The solid line shows the measured characteristics, while the dashed line shows the theoretical characteristics calculated from the transfer functions derived using the set tap coefficients. The filter operates as a multi-frequency-channel selector, selecting s channels (s=1, 3, and 7) out of 8 multiplexed frequency channels in the frequency range between f_0 and f_0 + 20 GHz, where f_0 is a frequency position in the 1.3-μm wavelength range. The excess loss is less than 1 dB. The close agreement between the calculated and

measured curves indicates that this filter could work well as a multi-frequency-channel selector.

Single-channel and 2-channel transmission experiments were performed. Figure 5 shows the experimental setup for measuring BER performance. First, the f_1-channel signal was introduced into the selector that selects 3 channels (f_1, f_2, and f_5). In this experiment, a frequency-stabilized YAG laser and a $LiNbO_3$ intensity modulator were used as a transmitter, which was externally modulated at 155 Mbit/s. Next, the f_7-channel signal was also introduced into the 3-channel selection selector using a 3-dB directional coupler to investigate the receiver sensitivity degradation due to interchannel crosstalk. BER measurements on the 155 Mbit/s signal are shown in Fig. 6 as a function of received power. A receiver sensitivity of -38 dBm was observed for one-channel transmission both before and after the selector at BER of 10^{-8}, and -37 dBm for 2-channel transmission. Receiver sensitivity degradation due to transmitting a selector hardly occurred, due to interchannel crosstalk is 1 dB.

Conclusion

A photonic FDM highway switch and a multi-frequency-channel selector using a coherent optical transversal filter have been discussed. The selector can independently select several arbitrary frequency-channels out of multiple FDM input frequency-channels. The BER performance of the selector was measured by transmitting 155 Mbit/s signals. No degradation of BER characteristics was observed in 1-channel transmission. The power penalty due to interchannel crosstalk was less than 1 dB at BER of 10^{-8}.

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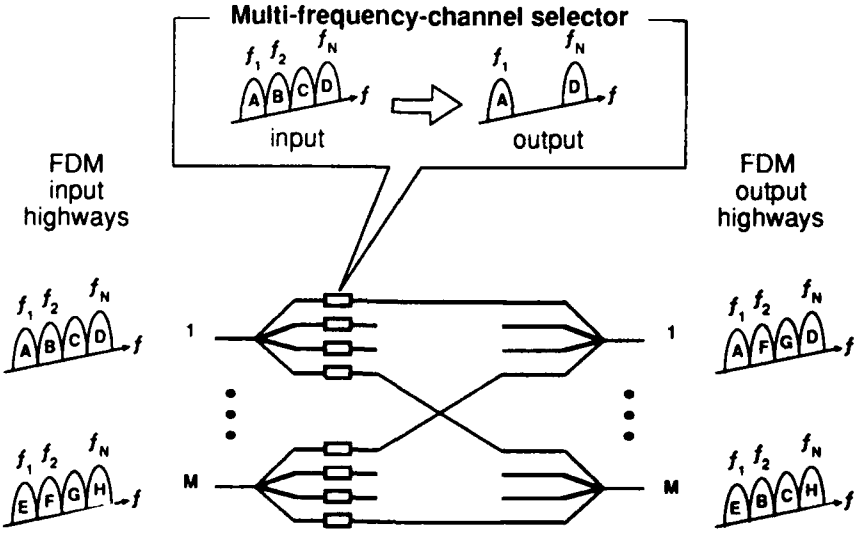


Fig. 1 Photonic FDM highway switch

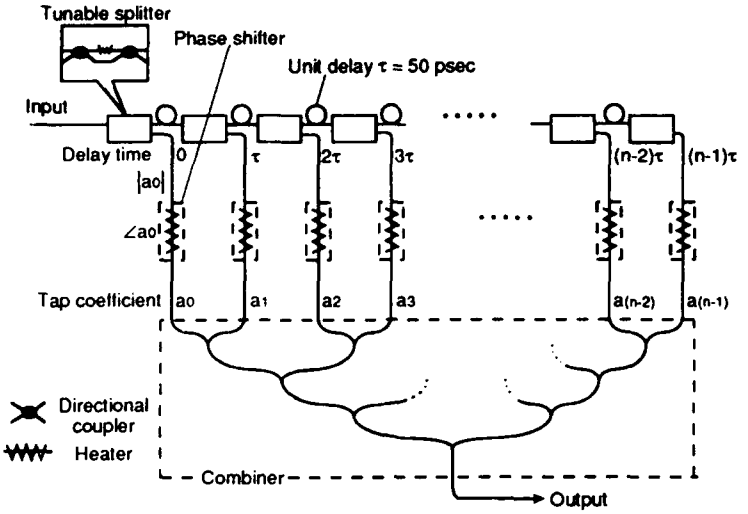


Fig. 2 Coherent optical transversal filter

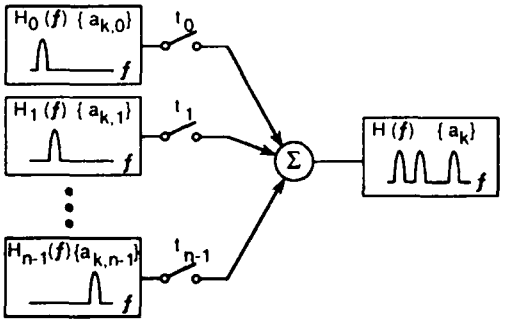


Fig. 3 Linear combinations of orthogonal tap coefficients and frequency characteristics

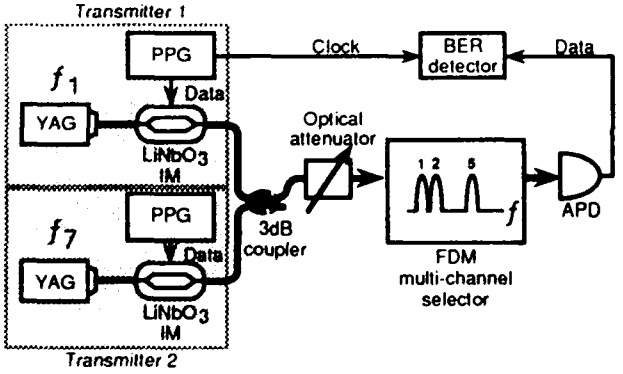


Fig. 5 Experimental setup

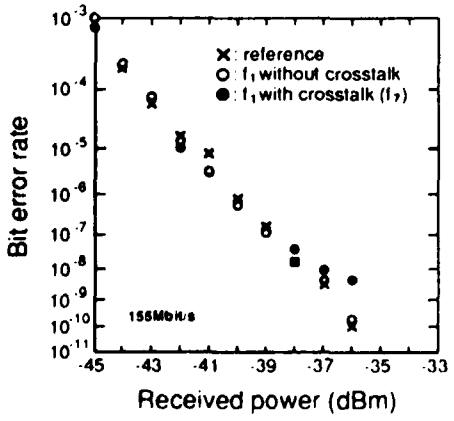
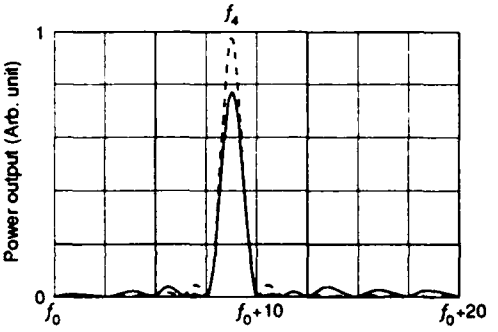
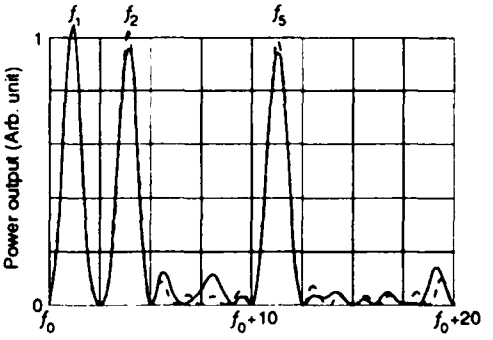


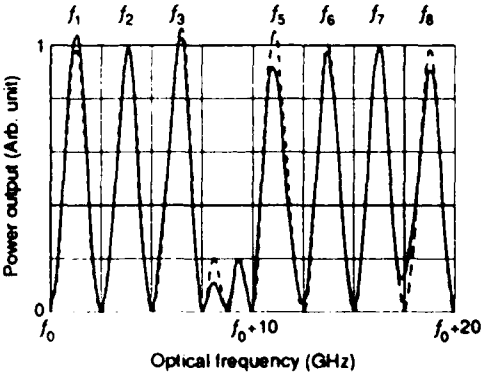
Fig. 6 BER performance



(a) 1-ch selection



(b) 3-ch selection



(c) 7-ch selection

Fig. 4 Frequency characteristics

Dilated Acousto-Optic Switches for Low Crosstalk Wavelength Routing in WDM Systems

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Introduction The goal of dense wavelength-division multiplexed (WDM) networks is to to expand the capacity of high throughput optical networks through parallel processing in the wavelength domain. Thinking of wavelength slots as independent information-bearing channels, one must find means to add or drop wavelengths into the network or, more generally, to overlay independent routing patterns for each separate wavelength channel on top of a single physical fiber network. By far, the integrated acousto-optic filter (AOF) [1] is the most sophisticated component for wavelength-selective filtering and switching in wavelength-routed optical networks. The unique feature of the AOF is its ability to filter or route many wavelength channels simultaneously, unlike other single-state filters, such as the Fabry-Perot and Mach-Zehnder cascade. In this paper we demonstrate a technique to construct very low crosstalk 1×2 and 2×2 AO switches by means of switch dilation [2]. Dilation allows one to obtain nearly ideal switch performance by cascading filter subcomponents, in such a way as to reduce first-order crosstalk to second order. The price paid is switch complexity.

Crosstalk in AO filters. Fig. 1 depicts a one-stage polarization-independent acousto-optic filter/switch. Both input ports 1 and 2 carry independent information-bearing wavelength channels *a*, *b*, and *c*, although only the inputs and outputs of channel 1 are shown for clarity. In this polarization-diversity device configuration, light is decomposed into orthogonal TE and TM polarization channels (see inset of Fig. 1). In an acousto-optic interaction region, selected wavelengths experience a narrowband polarization flip, with the result that interchanged TE and TM states recombine in the opposite port: input 1 goes to 1*F* and 2 to 2*F*. Unselected wavelength channels remain in their original waveguides after recombination: input 1 to 1*U* and 2 to 2*U*. In short, selected wavelengths follow the "cross" state routing of the switch, while unselected wavelengths remain in the "bar" state of the device. In the example of Fig. 1, *a* and *c* are selected and so cross over, while *b* is unselected and remains in the bar state. A small residual signal goes to the wrong port - resulting in interchannel crosstalk. For example, wavelength *a'*, arriving from input port 2, will join with the small leaked portion of *a* (from input port 1) resulting in direct coherent interference of these two unrelated signals. Fig. 2a shows the bar and cross state filter spectra for a passband centered about λ_o, phase-matched by an RF frequency F_o. The cross state (bandpass) transmission shows a residual wavelength-independent leakage ε and sidelobe levels ξ, while the bar state band-reject spectrum shows incomplete depletion on resonance (residual δ) and mimics the sidelobe structure ξ. The underlying processes leading to imperfect extinction include polarization splitter/combiner leakage, imperfect polarization conversion, and out-of-band polarization conversion, as discussed below.

Imperfect polarization isolation. Fig. 2b identifies crosstalk paths due to imperfect polarization isolation in the two polarization splitter/combiners. The TM and TE polarizations (closed and open circles respectively) normally take different paths to the bar state of the overall structure, but TM leakage across the splitter and TE leakage through the splitter result in first-order leakage into the wrong (cross) port even with no filter excitation. The contribution due to second-order leakage of order ε^2 (leaked light in the first splitter leaking again in the second splitter) returns to the bar port and is not included in the figure.

Incomplete polarization conversion. Figure 2c shows the effect of a polarization conversion efficiency which falls short of unity by an amount δ. Ignoring polarizer leakage, the unconverted light makes its way to the undesired bar port as shown. Normally, one adjusts the RF drive power so that maximum depletion is seen in the bar state, but the best conversion efficiencies reported are under 99%.

Finite sidelobe levels. The presence of secondary maxima in the AOF transmission spectrum is a result of the abrupt onset and cutoff of the acousto-optic interaction. These levels are about 10% in the usual filter, located about one filter half-width from line center. Various mechanisms contribute to sidelobe enhancement or suppression [3]. By interchanging the large and small components in Fig. 2c, one obtains the leakage path for sidelobe-resonant light at a fractional intensity ξ.

Dilated acousto-optic filters. The concept of filter dilation is described using the simplified filter schematic and routing diagram shown in Fig. 3a. This figure represents an AOF run as a 1×2 switch with two input wavelengths *S* (a wavelength to be selected) and *U* (a wavelength which is *un*selected). The *S* input goes into the cross state with a little bit of *U* leaked, this small quantity denoted by a lowercase *u*. Similarly, *U* goes primarily into the bar state,

accompanied by a small leakage s from S. The key to dilation is that, in the first stage, the filter peels off the leakage components, directing them not to the undesired port, but to a spare waveguide, thus purifies the input to the second stage, which similarly discards leakage generated in its own stage. Thus, repeat filtering leaves only second-order leakage in the desired path. The dilated version of a 1×2 filter is shown in Fig. 3b, in which the first-order leakages u and s arrive at unused ports. A fully functional 2×2 wavelength-division crossconnect is shown in Fig. 3c, in which inputs S and U from port 1 are cleanly routed to second order, while port 2 inputs S' and U' go to their respective cross and bar states with first-order leakage (s' and u') on the same two unused channels used as a dump by channel 1. By analysis of the 1×2 filter extinction mechanisms, taking polarization extinction and beamsplitter leakage separately, one obtains the following improvements

PROPERTY	ONE-STAGE	TWO-STAGE
conversion efficiency	$1-\delta_1$	$1-\delta_1\delta_2$
beamsplitter leakage	ε_1	$\varepsilon_1\varepsilon_2$
sidelobe levels	ξ_1	$\xi_1\xi_2$
frequency shift	F_1	F_1-F_2
bandwidth	$\Delta\lambda$	$0.72\Delta\lambda$

More subtle is the effect of light which is legitimately passed by the first stage but by the wrong drive frequency, when multiple wavelength channels are routed. This light will be filtered in the next stage by the proper frequency and appears undiluted at the output, reduced by the factor defining the one-stage cross-filtering: $\xi^{1/2}$. The eradication of this persistent coherent crosstalk mechanism [4] requires sidelobe suppression in a single stage, something which remains a requirement for dilated filters [5].

Experiment. The efficacy of dilation for achieving true crosstalk reduction was examined in a experiment employing a pair of identical polarization-independent AOFs separated by 250 μm on a lithium niobate substrate (Fig. 4). The filters were connected externally so that a polarization controller was required to preserve the polarization state between stages (without which there is a double frequency shift component in the output signal). Much of the basic filter design (optical and acoustic waveguides and SAW transducers) has been reported elsewhere [6],[7]. The two AOFs were very well matched in performance. The TE and TM characteristics were *not the same*, primarily due because of differential loss in the polarizing beamsplitters. Table 1 lists many properties of the filters separately and in series. Note that the bar and cross states of the dilated structure were examined with different placements of the output fiber pair: upper guide connections gave the cross state performance, while lower guide coupling produced the cross state.

	upper stage		lower stage		cascaded	
Property	TE	TM	TE	TM	TE	TM
conversion efficiency (%)	98.5	96.2	98.3	97	99.4	98.2
RF drive power (dBm)	13.3	13.3	13.7	13.7	same	same
drive frequency (MHz)	174.5	174.5	174.5	174.5	174.5	174.5
first sidelobe intensity (%)	28	30	32	26	10	10
bar state loss (dB)	9.2	12.4	9.4	12.4	18.4	25.8
cross state loss (dB)	12.2	12.2	12.2	12.2	24.5	24.5
leakage level (dB)	-19	-23	-13	-25	-16	-22
FWHM (nm)	1.6	1.6	1.6	1.6	1.34	1.34

Figure 5 shows the spectral transmission of the one and two-stage filters for a probe wavelength of 1559 nm and an applied RF frequency of 174.5 MHz at about 13 dBm per stage. The lefthand traces are cross (band-reject) and bar (bandpass) spectra for one stage operation, while the righthand traces are cross and bar states of the dilated two-stage filter. Even from Fig. 5, the improvements in cross-state depletion (conversion efficiency) and sidelobe suppression are obvious. Leakage effects were very hard to measure because substrate light coupling into the output fiber acted as an inseparable noise floor. The noise floor for the one-stage device was 40 dB down, making those numbers reliable, but the noise floor was only -16 dB down for the second stage due to accumulated losses in the guided light level. This fact is evident from the inability to measure improvements in leakage as shown in Table 1.

Conclusions. The simple 2×2 AO switch has nowhere to divert residual unconverted or leaked light but as noise into the wrong output port. In dilated switches, light pollution is diverted to unused channels, to first order, making achievable single-stage performances, compensated for by dilation, acceptable for stringent system crosstalk requirements. The main technological improvements demanded of a dilated network are achievement of low loss and development of short beamsplitters, since interaction lengths are usually not negotiable and crystal sizes are limited. We have shown that a combination of single-stage sidelobe suppression and single-substrate dilation will allow high performance acousto-optic switches to be realized.

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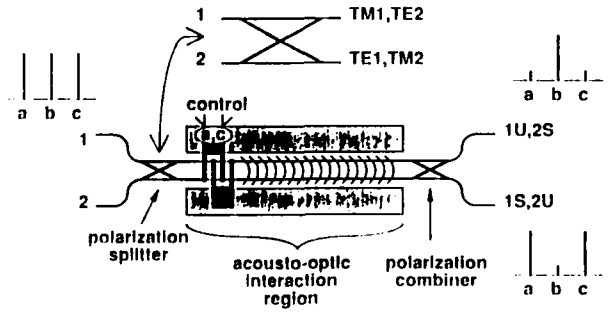

Fig. 1. *Schematic of the 2×2 acousto-optic switch showing detail of the polarization splitter and fate of three wavelength channels arriving at input port* 1.

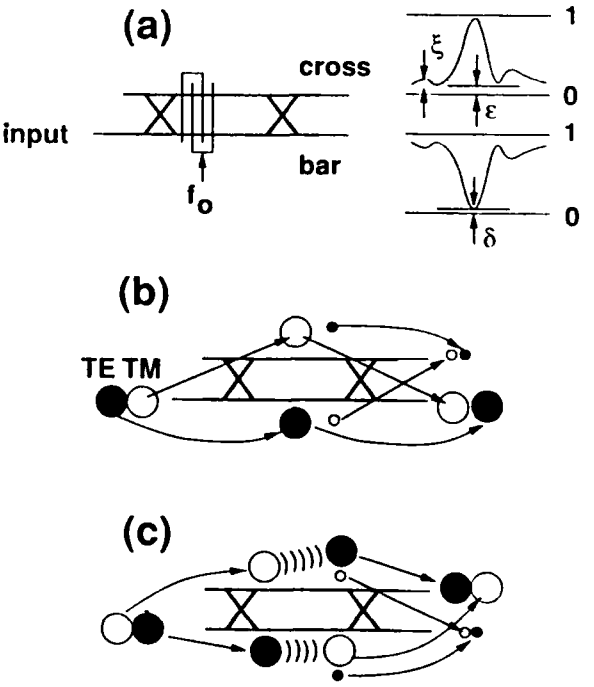

Fig. 2. *(a) Bar (band-reject) and cross (bandpass) state spectral transmissions for a single acoustic grating; TE (open circle) and TM (closed circle) mode paths and leakage paths for (b) beamsplitter leakage and (c) incomplete polarization conversion.*

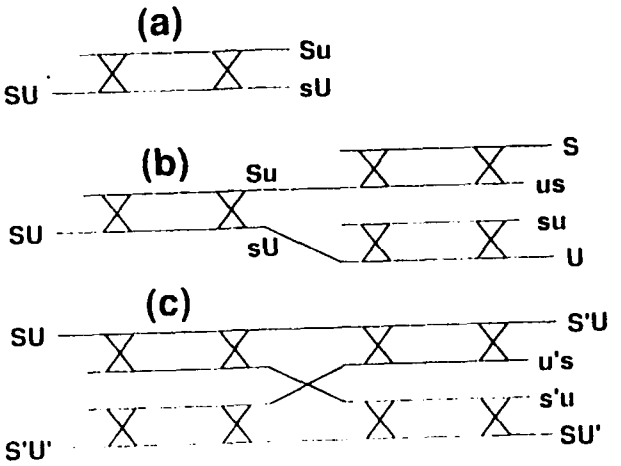

Fig. 3. *AO switch paths for selected S and unselected U wavelengths for (a) a single-stage 2×2 switch, (b) a dilated 1×2 switch and (c) a dilated 2×2 switch.*

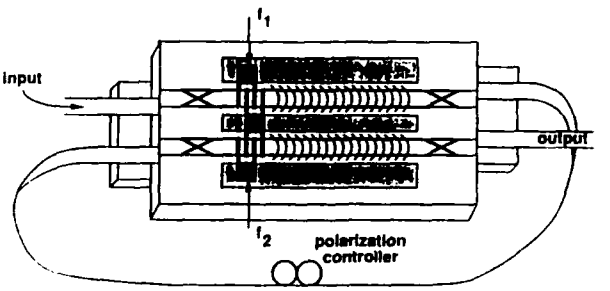

Fig. 4. *Schematic of the experimental pair of devices and their connection to form a dilated 1×2 cross state demonstration.*

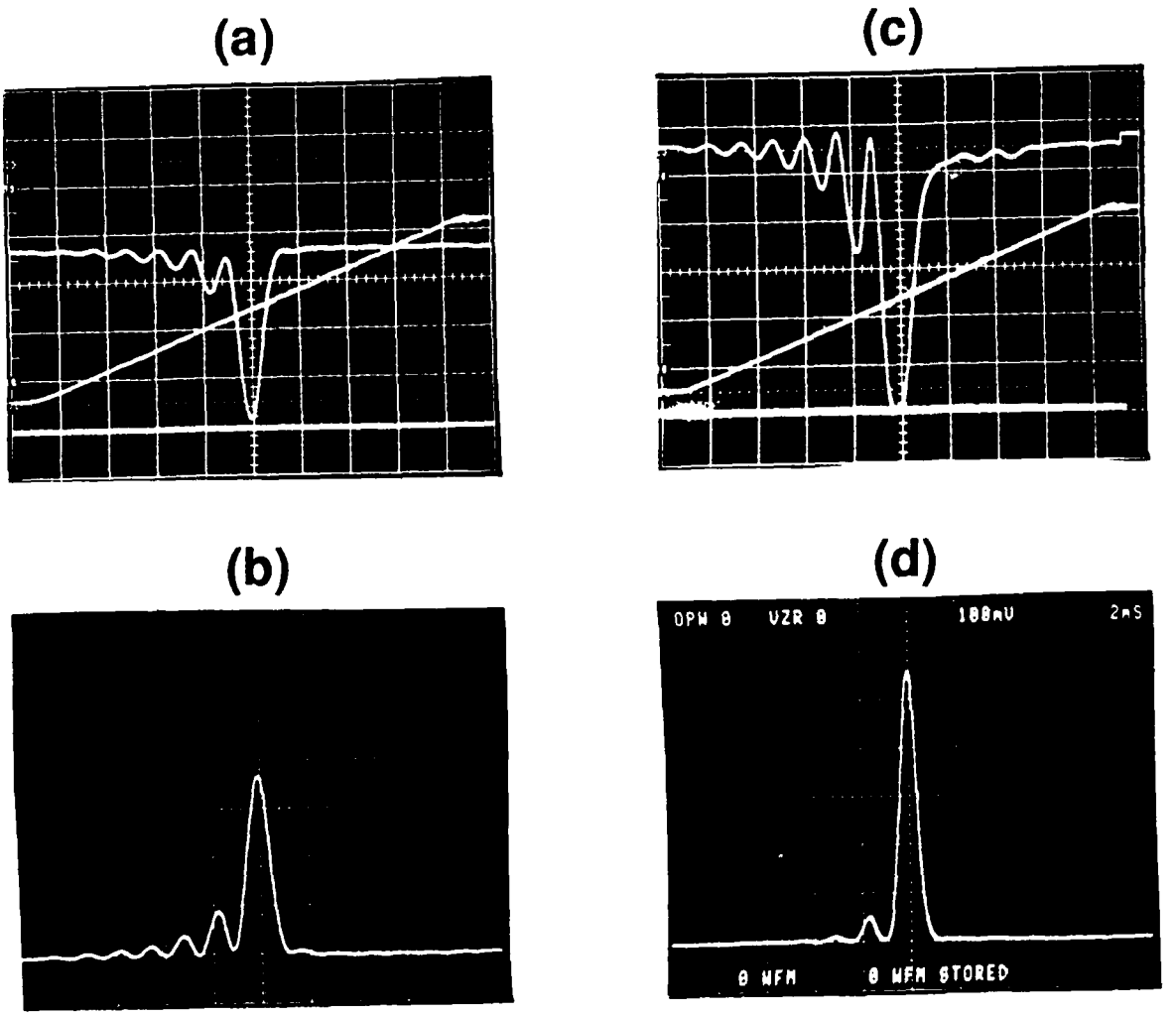

Fig. 5. *Left: one-stage transmissions for 1559 nm source and 3 MHz RF sweep, equivelant to a 27 nm wavelength scan. (a) bar state and (b) cross state. Right: dilated switch in the (c) cross state and (d) bar state.*

AN INTELLIGENT CHANNEL SELECTOR FOR WAVELENGTH-DIVISION AND TIME-DIVISION HYBRID MULTIPLEXED NETWORK

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1.Introduction

Recently, requirement has been increasing for large capacity optical network, for example, for a video signal distribution system in broadcasting studio[1], which has been undergoing a process of complete digitalization. A wavelength-division and time-division hybrid multiplexed (WD/TD) network[2] is an attractive candidate for this purpose, because the attainable multiplexity is given by the product of WD and TD multiplexities. In order to realize WD/TD network, WD/TD channel discrimination and tracking control when receiving a channel are indispensable techniques. In this paper, a highly intelligent WD/TD channel selector is described for practical broadcasting studio application. Results for WD/TD channel selection and tracking control are shown to demonstrate the developed selector performance.

2. WD/TD network configuration

Figure 1 shows WD/TD network configuration. In this network, WD channels of different wavelengths modulated with TD multiplexed signals go to center star coupler for WD multiplexing. In each local center, incoming WD/TD multiplexed signals are first divided for simultaneous monitoring and processing. The divide number should be at least 8 for practical application. From each of the divided WD/TD signal, arbitrary WD and TD channel is selected using tunable wavelength filter (λ-filter) and TD demultiplexer (DMUX). For broadcasting studio application, total multiplexity of 2 to 3 hundreds is required[1]. Adopting the current and standardized video signal format, NTSC (around 150Mb/s), TD multiplexity of up to 20, which leads to around 3Gb/s TD multiplexed signal speed, is easily obtained with the present optical transmission technology. Therefore, WD multiplexity of around 20 is sufficient enough to satisfy the above total multiplexity requirement. Considering the presently available optical amplifier gain bandwidth of around 35nm, which is the narrowest of all the optical components' operation wavelength range included in the WD/TD network, WD channels can be allocated sparsely (several nm channel separation) to relax requirement for strictness of WD channel wavelength separation. Therefore, in this system, strict wavelength control is necessary only for WD channel tracking of λ-filters. For th is relatively sparse WD network, acoustooptic (AO) filter[3] is promising for λ-filter, considering its wide tuning range, transmission bandwidth compatible with directly intensity-modulated laser diode (LD) spectral bandwidth.

For applying the WD/TD network to a video signal distribution system in broadcasting studio, arbitrary WD/TD channel selection is indispensable basic function to be accommodated in each local center.

3.Design consideration for WD/TD channel selector

For realizing the WD/TD network, channel selector should meet several requirements, that is, λ-filter transmission wavelength fluctuation and selection time. Allowable fluctuation for power penalty suppression is as small as several percent of WD channel spacing decided by its transmission bandwidth and spectral width of WD channel[4]. Channel selection should be completed in blanking time, which is several microseconds[1]. In addition, WD/TD channel selector should possess several functions such as, **(1)random access to arbitrary channel, (2)automatic transmission wavelength tracking to selected WD channel, (3)automatic start-up and (4)WD/TD channel discrimination.** Also, in order to construct a compact system, **(5)simultaneous controllability over around ten pairs of λ-filters and TD DMUXes,** each of which treats divided incoming WD/TD signal, is desirable. Though several WD channel selectors have been studied for coherent FDM transmission systems[5] to date, they have realized only a part of the above functions. In order to realize all of the functions from (1) through (5) and the required additional performances, the present selector employs a Digital Signal Processor (DSP), which makes possible fast control operation compared to the conventional microcomputer. This fast operation enables a lot of pairs of λ-filters and TD DMUXes to be controlled under time sharing scheme without stability degradation. Configuration and control algorithm for the selector are shown in Fig.2. Details for the control algorithm are shown below:

(1)automatic start-up

Just after each local center is started up, a controller in each local center starts scanning transmission wavelength of λ-filter to find the relationship between WD channel wavelengths and tuning signals for λ-filter. The relationship is then stored to memory in the controller for responding to forthcoming WD channel access request.

(2)WD/TD channel discrimination

A low frequency tone is applied to each WD channel, which is different from local center to local center, for WD channel identification. The controller detects the tone frequency using Frequency-to-Voltage converter. Also, frame synchronization using a pair of racing counters is performed for TD channel identification. For this purpose, a frame pattern is inserted in one of TD multiplexer input ports.

(3)random access

After receiving channel access request, the controller switches control signal to the λ-filter for WD channel selection according to the stored data, and TD DMUX is controlled to select requested TD channel. Stored data for WD channel selection is replaced by the new one after servo control is completed in order to tolerate drifts of WD channel wavelength and λ-filter transmission wavelength.

(4)automatic transmission wavelength tracking to selected WD signal

After random access is completed, transmission wavelength of the λ-filter should precisely track the selected WD channel. For this purpose, transmission wavelength is slightly dithered with low frequency sine wave. The λ-filter output is synchronous-detected to obtain error signal. Error signal is converted to control signal by DSP, which enables us to program arbitrary formalism for conversion.

A selector has been fabricated, which can realize the above functions. A photograph for the selector with a DSP is shown in Fig.3(a). This selector can control 8 pairs of λ-filters and TD DMUXes simultaneously.

4.Experimental results

The experiments have been performed to confirm the above mentioned functions. As a λ-filter, an AO filter (3dB transmission bandwidth : 1.8nm) was employed. Wavelengths for WD channels were set at around 1.54μm. Fabricated receiver board including AO filter, TD channel selector is shown in Fig.3(b). For filter wavelength tracking, digital 1-type servo system, which is the counterpart of analogue PI controller, was adopted, considering its stable control performance and simplicity.

(1)WD/TD channel selection

Transmission wavelength of the λ-filter was randomly selected out of six WD channels (ranging from 1.53 to 1.55μm). Spectral shapes are shown in Fig.4 for WD channels #1, #3 and #6 selection. These figures indicate that the selection was successfully performed. Wavelength switching time (from selection request to selected WD channel change) was as short as several hundreds of microseconds, which can be reduced to the required several microseconds only by control algorithm optimization. TD channel could also be stably selected.

(2)stability for WD channel tracking

The error signal fluctuations under control are indicated in Fig.5 for two WD channels. Short term fluctuation range was about 0.04nm (several percent of AO filter 3dB bandwidth), while longer term fluctuation was almost completely suppressed. This result meets the stability requirement mentioned above.

Furthermore, signal transmission characteristics were measured with and without tracking control. A WD channel was directly intensity-modulated with 1.418Gb/s NRZ pseudorandom (2^{15}-1) pattern. Receiver input power was adjusted to give bit error rate (BER) of around 10^{-9}. The results are shown in Fig.6. Large BER fluctuation range between 10^{-9} and over 10^{-3} was compressed to 10^{-8} and 10^{-9}. These results indicate the realization of the designed stability.

5.Conclusion

A channel selector for WD/TD network has been designed to rellize the necessary performances for WD/TD network. The performances were confirmed by WD and TD channel selection and tracking experiments.

Acknowledgement

The authors would like to express their gratitude to K.Kobayashi, J.Namiki and M.Fujiwara for continuous encouragement throughout this work. Thanks are also due to Y.Suemura for fruitful discussion.

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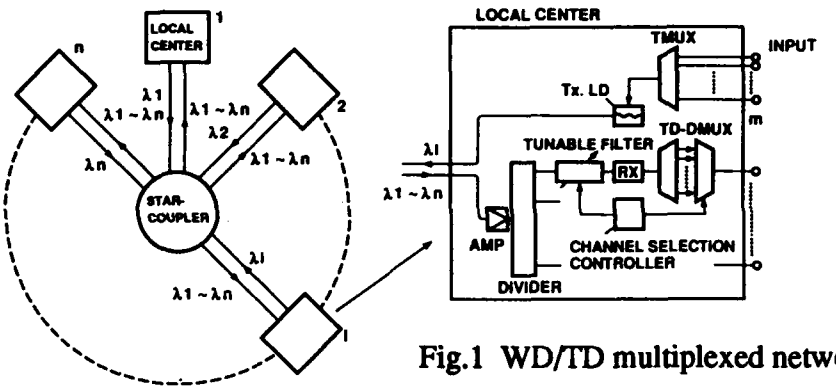
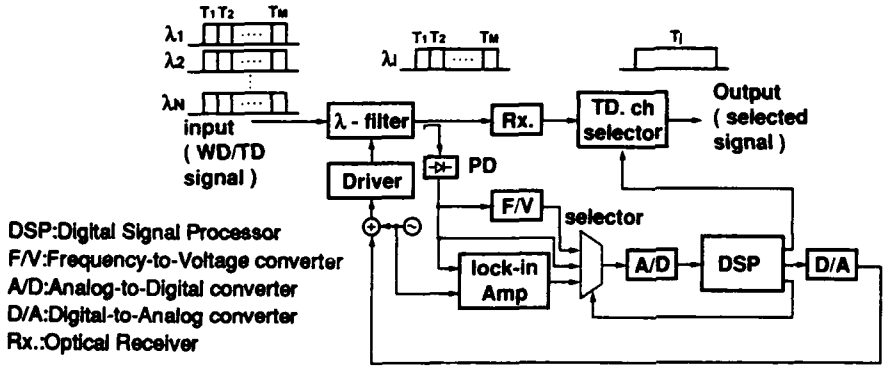
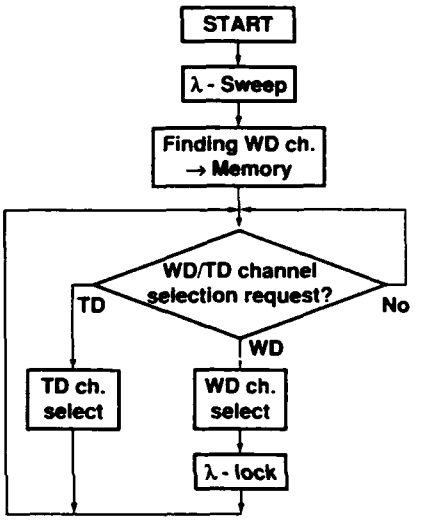


Fig.1 WD/TD multiplexed network



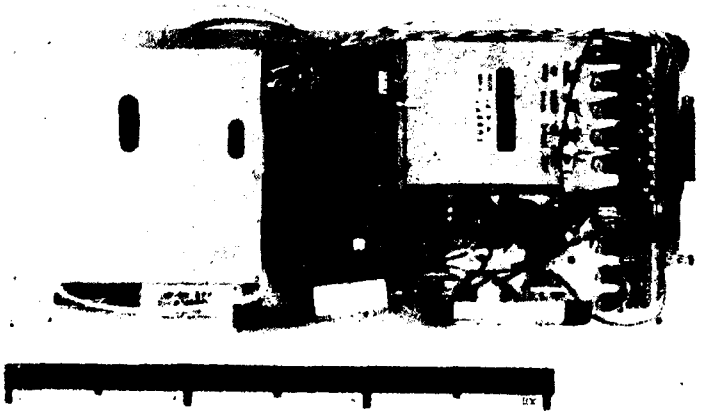
(a) Control system blockdiagram



(b) Control algorithm

Fig.2 WD/TD channel selector

(a) WD/TD channel selector



(b) Receiver board

Fig.3 Fabricated system

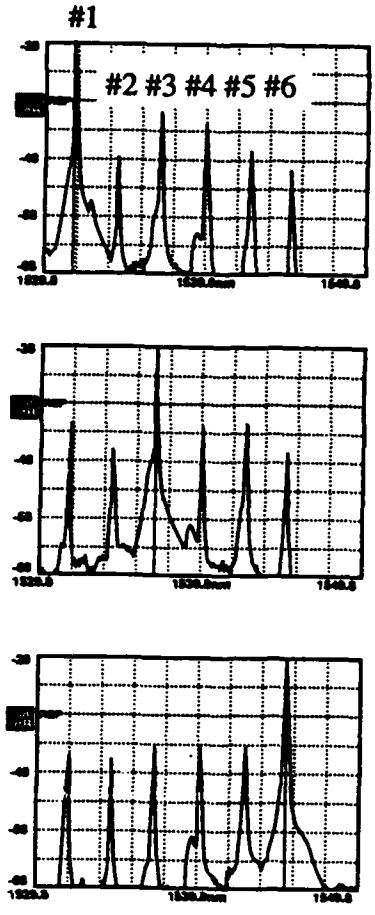


Fig.4 WD channel selection

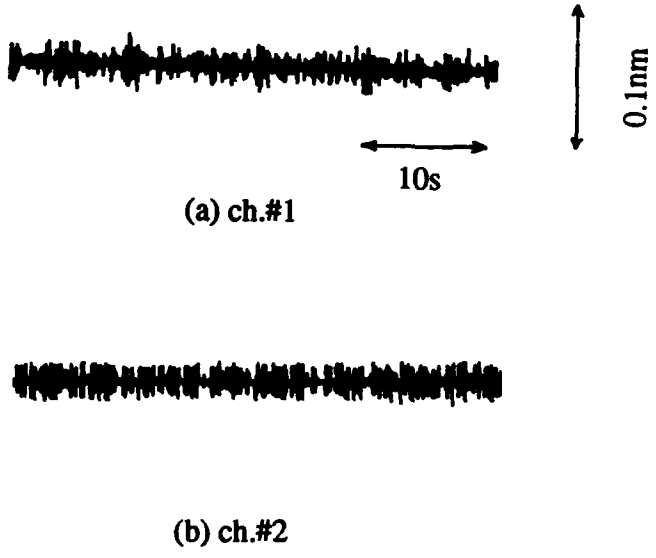


Fig.5 Transmission wavelength fluctuation under control

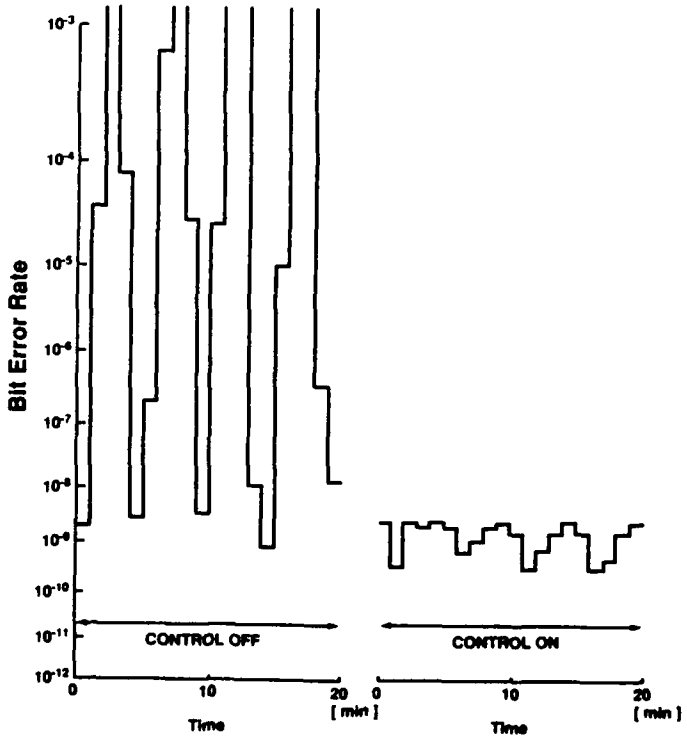


Fig.6 Stabilization of BER characteristics under WD channel tracking

A Fast LD Wavelength Switching with Rapid Stabilizing Control for WDM Network

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Fax: +81 44 856 2222

1. Introduction

Recently, requirements have been increasing for large throughput asynchronous transfer mode (ATM) cell based networks, such as 'transfer networks' [1] and local area networks (LANs) [2]. However, pursuing larger throughput only by improving transmission speed cannot satisfy future requirements. Wavelength-division multiplexing (WDM) optical networks are promising for increasing throughput. For effective utilization of this enlarged throughput, a ring topology with appropriate fairness control (e.g. [2]) is preferable to a star topology [3], considering the latter's inevitably complicated contention-free access control (for example, a token passing protocol) that imposes a delay on each cell. Recently, we have proposed a WDM ring optical network for ATM signals with high throughput and simple access protocol [3]. In this paper, a novel scheme is proposed and experimentally confirmed for fast laser diode (LD) wavelength switching with rapid stabilizing to its predetermined wavelength, which is the key technology for the proposed network.

2. WDM optical ring network

Figure 1 shows the structure of the proposed network. Basically, the network is a "slotted ring" where nodes are addressed with certain wavelengths. A slotted bus is also possible with the proposed network. Each node has two fixed wavelength filters tuned to the preassigned address wavelength and a frame pulse channel (λ_s). Data cells are transmitted on a certain timeslot synchronized with the frame pulse. When a cell transmission-demand arrives, the node first detects the status ('idle' or 'busy') of the destination node. This can be accomplished, for example, by monitoring the control signal imposed on the channel λ_s. On finding it 'idle', the wavelength tunable optical transmitter is tuned to the destination node address wavelength and a cell is sent out to the highway on the idle timeslot. Each node drops out and receives only its preassigned wavelength channel from the highway. The proposed network has many advantages. Firstly, high throughput is expected from employing this WDM technology. The second feature is its simple and high speed communication protocol. In this network, an idle slot to the desired destination can be immediately accessed and no address processing is required at each node. This simplified protocol can significantly improve the delay-throughput characteristics. Finally, this network can be constructed using presently available devices, requiring only tunable wavelength transmitters and fixed wavelength filters for receivers.

3. Fast wavelength switch/control scheme

One of the important technologies needed by this network is fast wavelength switching in the transmitters. Assuming a cell length of 53bytes, and 5% guard time between timeslots, wavelength switching time should be reduced to below 350ns, 18ns, 8.8ns, and 2.1ns for 600Mb/s, 1.2Gb/s, 2.4Gb/s, and 10Gb/s cell speeds, respectively. In addition, stable wavelength holding during one cell transmission is required. Allowable wavelength fluctuation for power penalty suppression is as small as several percent of WD channel spacing [4]. In order to achieve this, we propose the transmitter structure as shown in Fig.2. An optical switch selects one of two LD outputs, whose wavelengths are different from each other [5]. During the holding period of the optical switch, non-selected LD wavelengths can be switched and stabilized for the next data transmission. In this transmitter structure, required wavelength switching and stabilizing time for each light sources is below 700ns, 350ns, 170ns, and 42ns for 600Mb/s, 1.2Gb/s, 2.4Gb/s, and 10Gb/s cell speeds, respectively. A switching time of 0.6ns, which is

short enough even for 10Gb/s cell transmission, has been achieved [3]. Thus, the high speed wavelength stabilizing is one of the most important technologies. However, conventional transmission peak detection method can not be used, because its operation speed is limited by the speed of synchronous detection.

Figure 3 (a) shows the proposed control scheme. Wavelength comb of optical resonator (Fabry-Perot (FP) etalon) transmission characteristic is used for wavelength standard. (Fig. 2 (b)) The transmitter LD wavelength is fast switched to be on a slope of the transmission peak. Just after the transmitter LD wavelength is switched, high speed servo circuits lock the wavelength to the middle of the slope. In this control scheme, wavelength error signal can be detected directly and proportional action can be adopted for the servo controller. Thus, the high speed wavelength stabilizing can be achieved by the wide bandwidth servo controller.

For example, for the finesse of 9.94, pull-in range as wide as 20% of FSR and 10 dB noise compression ratio (defined by $(\Delta\nu/FSR)/(\Delta V/V)$) are achievable. With these values, the loss probability of ATM cells, caused by wavelength fluctuation, can meet the practical system requirement.

4. Experiment

The proposed control scheme has been experimentally confirmed. Figure 4 shows the experimental setup. Fabry-Perot etalon (FSR=0.08nm (10GHz)) was used for frequency standard. Widely wavelength tunable 1.5μm 3-section distributed feedback (DBR) LD [6] was used as a light source. Controller for wavelength switching and servo consisted of ECL logic gates and wide bandwidth operational amplifiers, which offer over several tens of MHz bandwidth servo circuits for over 600Mb/s cell speed.

Figure 4 indicates wavelength transient response for switched LD (a) with and (b) without servo control. Figure 5 shows the block diagram of wavelength transient response measurement system. LD is periodically driven by wavelength switching signal. The output power transmitted through the scanning FP interferometer (FSR=1.6nm (200GHz), FWHM=0.016nm (2GHz)), controlled by a personal computer, is detected by a high speed photodiode (PD). Transient responses at each wavelength are collected and reconstructed by the personal computer. In Fig. 4 (a), there are large over-shoots caused by current switching waveform. In Fig. 4 (b), optical frequency is stabilized within 700ns and wavelength steps are accurately 0.08nm (10GHz), using servo control. These characteristics are suited for 600Mb/s cell speed. By broadening the servo control bandwidth, this control scheme can be applied to over 10Gb/s cell speed networks.

5. Conclusion

LD wavelength control scheme for rapid stabilizing after wavelength switching has been proposed. Obtained characteristics are suited for 600Mb/s cell speed WDM ring network. The proposed control scheme can be applied to over 10Gb/s cell speed networks and WDM cross-connect systems.

Acknowledgement

The authors would like to express their gratitude to K. Kobayashi, J. Namiki for their continuous encouragement throughout this work. The authors also wish to thank S. Murata for providing DBR LDs.

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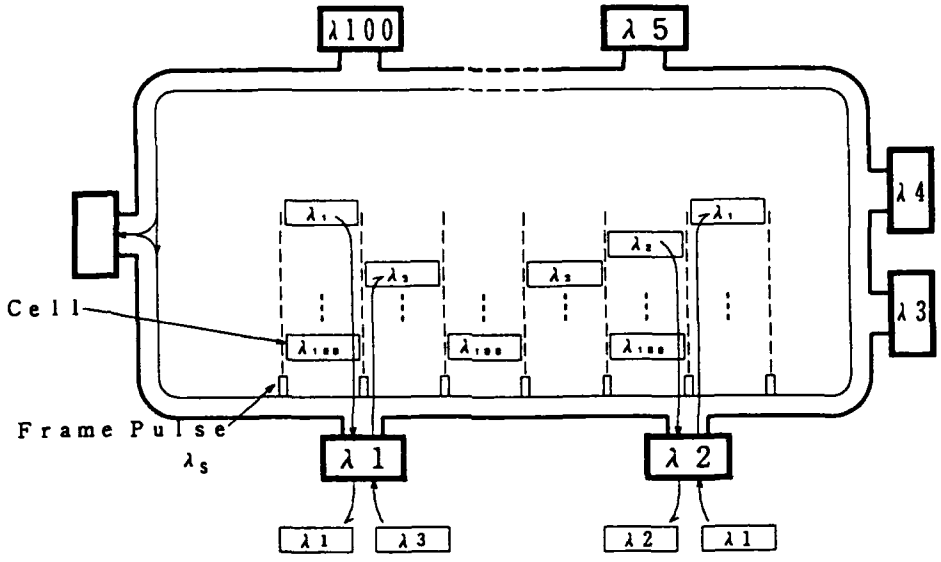
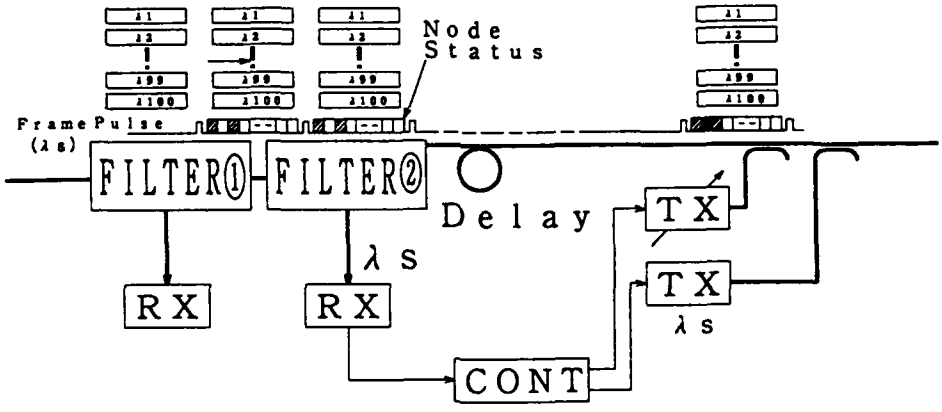


(a) Network configuration.



(b) Node structure.

Fig. 1 Wavelength addressed optical network using slotted ring.

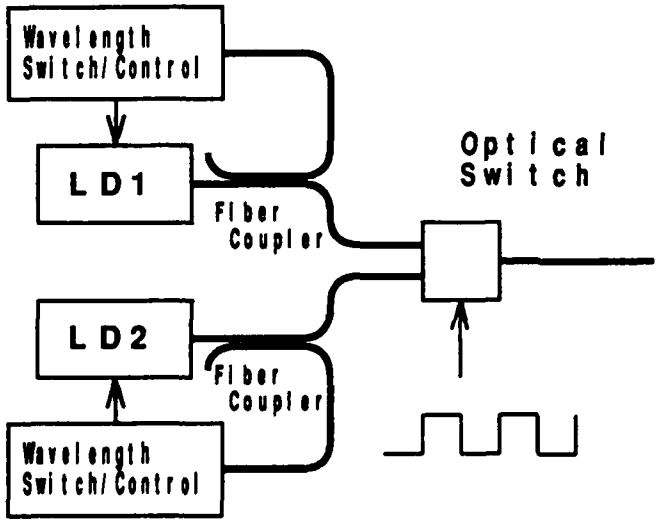
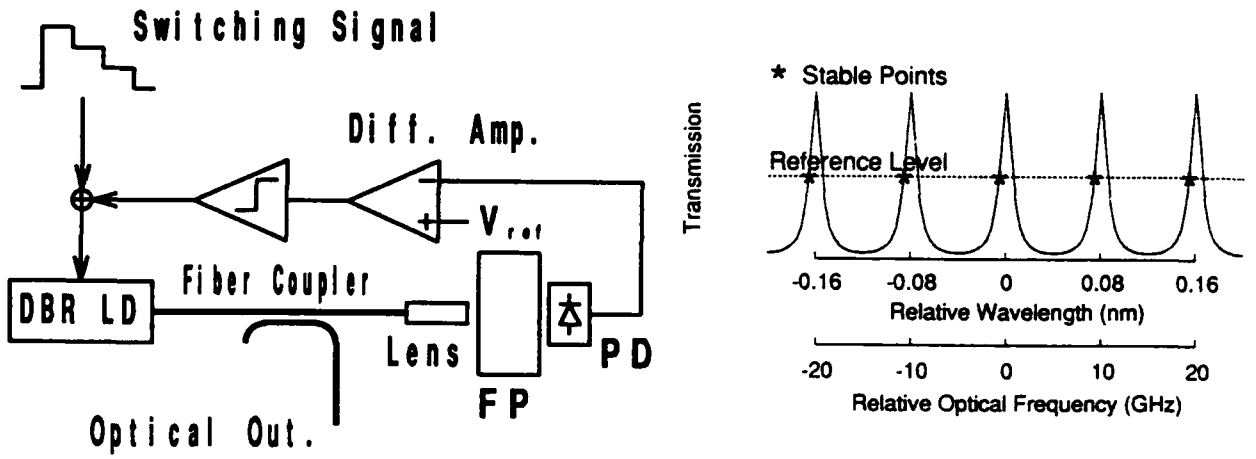


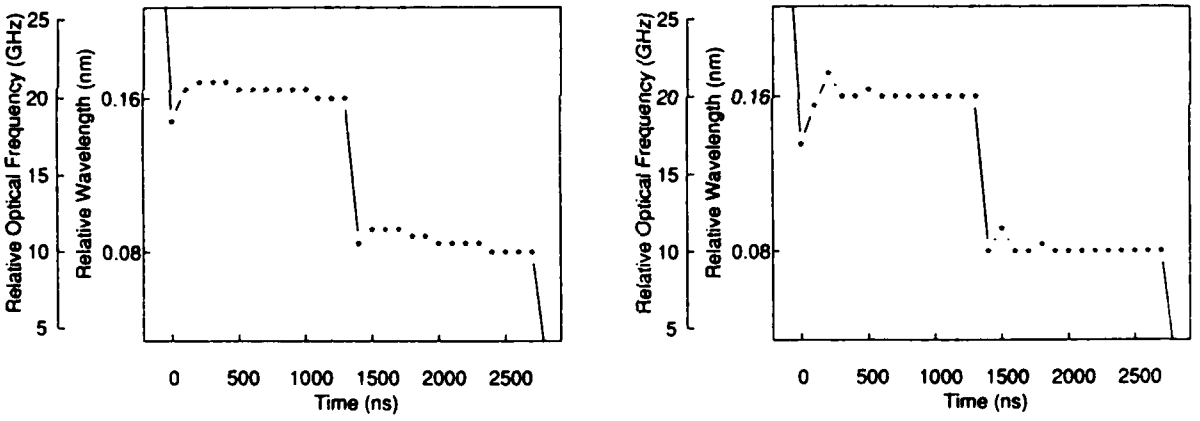
Fig. 2 Configuration for wavelength switched optical transmitter using optical switch.



(a) Block diagram for the proposed control scheme.

(b) Transmission characteristic for a Fabry-Perot etalon.

Fig. 3 Wavelength control scheme.



(a) Control off.

(b) Control on.

Fig. 4 Transient response of wavelength switched LD.

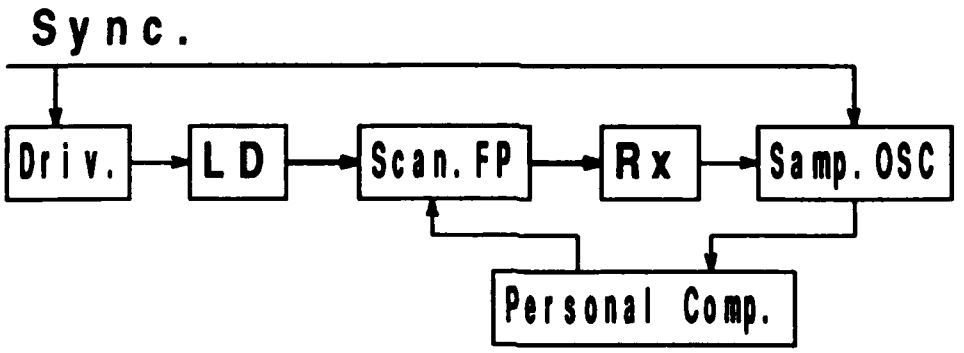


Fig. 5 Optical frequency transient response measurement system.

Joint Optical Computing/ Photonics in Switching/ Spatial Light Modulators Plenary Session

JTuC 2:00pm-5:30pm
Grand Ballroom East

B. Keith Jenkins, *Presider*
University of Southern California

Joseph W. Goodman, *Presider*
Stanford University

Extended Generalized Shuffle Networks

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1.0 Introduction

A successful network architecture generally must consider the technology being proposed for implementation. A design suitable for an electronic application may prove to be unwieldly or even impossible to implement in the photonic domain. Basically this is due to the limitations and constraints imposed by the optical technology at hand.

The talk provides an overview of a new class of networks called Extended Generalized Shuffle (EGS) networks[1],[2] and considers how various attributes of these networks can address some photonic switching constraints. From a purely mathematical and topological viewpoint EGS networks are technology independent and they will be handled as such in subsequent more detailed papers[3],[4]. However, our current focus is on photonic switching and we will thus limit most of our discussion to those aspects of EGS networks that primarily impact the implementation of photonic switching networks. The talk is primarily intended to bridge some of the gap between photonic switching technology and switching network theory.

The following two sections catalog some constraints imposed by free-space and guided-wave photonics, respectively. The fourth section briefly summarizes how EGS networks can deal with such contraints.

2.0 Some Free-Space Photonic Switching Constraints

Free-space photonic network implementation assumes the use of symmetric self electro-optic devices (S-SEEDs)[5] as logic gates in the switching modules of the network.

2.1 Switching Module Fan-Out/Fan-In Limitations

There are several reasons for preferring small values of fan-out and fan-in when dealing with free-space optics[6]. If the fan-out in a particular system is large, then the optical power that is emitted from a single S-SEED must be divided before being routed to the many detecting S-SEEDs, and the optical power arriving at any one of the detecting S-SEEDs will be relatively low. Since the maximum switching speed of an S-SEED is directly proportional to the amount of optical power that sets the device, smaller fan-outs will yield faster switching speeds.

Smaller values of fan-in are also desirable within a system because the signal-to-noise ratio at the input of any S-SEED will increase as more signals are fanned into the device. The bit error rate of the system will also increase. In addition, larger values of fan-out and fan-in will typically require more complicated beam-steering optics which tend to increase the overall system cost.

Reference [6] reports a lossless beam splitting and recombination technique that suggests advantages for limiting fan-out and fan-in to values of two between stages of logic. This in turn suggests the use of switching modules having no more than two inputs and two outputs. Such modules may or may not be conventional crossbar switches; an issue we consider next.

2.2 Switching Module Functionality

The functionality provided in switching modules should consider overall network implementation complexity and efficiency. For example, consider two switching modules A and B and suppose that more B modules than A modules are required to construct a non-blocking NxN network. We next consider the implementation complexity (no. of S-

SEEDs, no. of stages, no. of control beams, etc.) of the two module types. If the complexity of module B is less than that of module A, we may find that a network using B modules has less overall complexity than one using A modules (in spite of the fact that more B modules than A modules are required to construct the network).

2.3 Switching Stage Uniformity

One important advantage in having uniform or identical switching stages is that only one type of switching stage needs to be fabricated. However, such uniformity requires that each switching stage has equal numbers of inputs and outputs (because to fully interconnect all of the outputs of a given stage with all of the inputs of the next stage requires that these numbers of inputs and outputs are equal and hence, via uniformity, that the numbers of inputs and outputs on all stages are equal). Thus, switching stage uniformity implies that the number of interconnections between stages is the same throughout the network. We consider this further in the next section.

Efficient, high performance EGS networks can be designed with uniform switching stages. In fact this constraint carries with it almost no disadvantages.

2.4 Interstage Interconnection

The "free-space" descriptor for photonic switching networks refers to the means of interconnecting successive stages of switching modules. It is advantageous for this technique to have constant numbers of interconnections between stages (as mentioned above). Two additional interconnection attributes, which have been found to be particularly convenient when employing free-space optics, are symmetry and stage-to-stage pattern invariance.

The so called "crossover"[7] interconnection pattern has constant numbers of interconnections between stages and exhibits symmetry, but does not result in stage-to-stage invariance. However, the stage dependent variations are such that they can be achieved by selecting an appropriate prismatic mirror array for each stage. We are willing to accept these stage-to-stage variations because the crossover interconnection pattern can be shown to yield EGS networks.

2.5 Switching Stage Size and Number of Stages

There are usually advantages in keeping both the switching stage size and the number of stages small. These advantages relate to such aspects as efficiency, reliability, and power. For example, as the switching stage size is increased, the size of the S-SEED array that implements the logic of the switching stage must also increase. As a result, the optical components (lenses, beam-splitters, etc.) within a stage must be capable of providing diffraction-limited imaging over larger fields of view. In addition, system lasers must provide more optical power if larger S-SEED arrays are used. Both of these requirements will increase the cost of a single stage within the system.

If, on the other hand, the number of stages is increased, then the overall system cost will begin to increase. Also, the expected availability of the system will decrease as the number of stages is increased, because the components within the multiple stages have non-zero failure rates. Unfortunately, it is usually not possible to have small values simultaneously for both switching stage size and number of stages. What sort of compromises are possible?

S-SEED photonic EGS switching networks generally exhibit the following helpful attribute. For a given number of input and output terminals and for a given probability of blocking (including zero), as the S-SEED array size increases (decreases), the required number of stages of S-SEED arrays tends to decrease (increase). Thus, these networks give the designer the capability to trade-off between switching-stage size and number of stages.

3.0 Some Guided-Wave Photonic Switching Constraints

Guided-wave photonic network implementation assumes the use of lithium niobate couplers[8] as the switching modules of the network.

3.1 2x2 Basic Element

The lithium niobate coupler is inherently a 2x2 device. Thus, we assume the use of switching modules having no more than two inputs and two outputs. As with free-space photonics, such modules may or may not be viewed as conventional crossbar switches.

3.2 Switching Module Functionality

Crosstalk due to imperfect lithium niobate couplers can grow to an undesirable level in a large network. One solution to this problem is to allow no more than one active signal in any coupler[9]. This means that a coupler may be

unavailable for use even though the desired input and output of the coupler are both idle. EGS networks are able to deal directly with this constraint in network design.

3.3 Interstage Interconnection

To keep losses at a minimum, the waveguide bends between stages of couplers have relatively large radii of curvature. Additionally, the couplers themselves are relatively large in comparison to the substrate wafer used in the fabrication process. The result is that there is low coupler density and therefore limited switching functionality per substrate module. The challenge for EGS networks is to be able to utilize such low functionality modules in the design of efficient high functionality networks.

3.4 Switching Stage Size and Number of Stages

As with free-space networks, there are usually advantages in keeping both the switching stage size and the number of stages small. Overall crosstalk and loss are two items of consideration. EGS networks allow trade-offs between switching stage size and the number of stages. As one increases (decreases) the other decreases (increases). Furthermore, in the most efficient configurations, the number of stages increases slowly (log N) in comparison to N (the number of inlets and outlets).

4.0 EGS Network Attributes

The following subsections catalog a few of the EGS network attributes that are helpful in dealing with photonic switching constraints.

4.1 Global Generalized Conditions for Non-Blocking Operation

It is possible to establish conditons for non-blocking EGS networks in very general terms. These conditions do not impose any constraints on the number of inlets or outlets in a network or any relationship between these two values. There is no symmetry required in the network. There are no constraints on the number of stages in the network. There is no relationship required between the size of the switching modules in one stage and any other stage. Also, the size of the switching modules in any particular stage are not generally constrained.

The major impact here is that for the most part switching networks can be designed with arbitrarily sized modules and an arbitrary number of stages. Thus, 2x2 modules can be utilized easily and switching stage uniformity becomes a natural outgrowth.

4.2 Multiple Stage Modularity

Under certain easily met conditions EGS networks exhibit the following attribute. For specifc (not necessarily consecutive) stages i and j, there exist subsets of switches in both of these stages such that every switch in the stage-i subset has a path to every switch in the stage-j subset and paths to no other switches in stage j. This allows networks to be constructed via multi-stage modules, each of which is entirely unconnected from other modules in the corresponding stages.

4.3 Different Types of Switching Module Functionality

The analysis of EGS networks allows switching modules to have functionalities less than that of conventional crossbar switches. Such reduced functionality usually relates to the sizes of specified subsets of inlets and outlets on the module that can be individually connected to each other. For example, one type of module may only be able to connect all inlets to all outlets or no inlets to no outlets. Efficient EGS networks can be constructed from such modules.

4.4 Network Isomorphisms

Two networks may have the same connectivity, differing only in the way their switching modules and links are labeled or in the way they are drawn. Any two such networks are said to be isomorphic. This relationship divides the collection of all networks into isomorphic classes. It is the fortunate case that many isomorphic classes of EGS networks have members that are amenable to photonic implementation. Formal mapping functions provide the ability to similarly analyze and control many of the members of a given isomorphism class, thereby allowing technology consderations to dictate the particular member chosen for implementation.

4.5 Network Shape Trade-Offs

The generality inherent in EGS networks allows a network with a given number of inlet and outlets to have many dif-

ferent "shapes". More specifically, one can typically trade-off the number of modules per stage with the number of stages. Thus network designs can be tailored to accommodate the needs of various technologies.

4.6 Other Attributes

The theory of EGS networks encompasses other dimensions of switching applications such as routing and control. These items and others have also found value in the implementation of photonic networks. Unfortunately, the limited scope of this summary does not allow further elaboration of such topics.

5.0 References

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ATM Objectives and Requirements For Next-Generation Networks

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1. Introduction

Worldwide activities on ATM (Asynchronous Transfer Mode) have been intensifying with rapidly evolving standards (CCITT and ATM Forum) [1,2]. Applications include multimedia services, high-speed LAN's, central-office switches and high-speed digital crossconnects. Potential large-scale network conversion into ATM is being considered and debated within various research and development communities. The push for deploying ATM to upgrade the existing network infrastructure has sometimes been compared to the "analog-to-digital revolution". The primary incentive to do so stems almost entirely from its service flexibility. Here, we discuss various aspects of ATM networking, emphasizing the transport objectives and requirements for next-generation networks. We will begin with the basic notions of ATM networking and then shift to a specific example of a VP (Virtual Path) transport network using an integrated ATM Crossconnect as a key network element.

2. Basics of ATM Networking

In ATM networking, all user-generated information (voice, video and data) is converted into standard fixed-size packets called "cells" for switching and transport. This process of converting the original data into ATM cells is called "adaptation". An ATM cell has a fixed size of 53 octets consisting of a 5-octet header followed by a 48-octet payload (Fig. 1). The header contains primarily the routing information for the cell (VCI and VPI values). Unlike traditional synchronous TDM transmission systems where data are sent via preassigned time slots, ATM traffic is transported by cell multiplexing without dedicated slots, and cells from a given source would appear to the network as asynchronous traffic. A simplified depiction of an ATM network connecting two users, A and B, is illustrated in Fig. 2. In order to initiate a communication connection between A and B, a call set-up procedure has to be invoked, e.g., a call request from A to B via ATM Switch I (signaling and control not shown in Fig. 2). As part of the call set-up process, ATM Switch I needs to inform A's ATM adapter proper VCI and VPI values to use and also to assure that these header parameters are recognized by various network elements along the assigned route for routing. Let us focus on the routing function first.

An ATM end-to-end connection from A to B is designated as a Virtual Circuit and hence a VCI in the cell header. A specific path from ATM Switch I to ATM Switch II, however, is called a Virtual Path which may contain many Virtual Circuits between various source-destination pairs connected to ATM Switches I and II. Along a specific VP, there may be multiple ATM Crossconnects (XC's) which are VP switches. Therefore, a VP is essentially a specific routing path from an originating ATM Switch to a destinating ATM Switch through a series of ATM XC's. All cells from a given source in the same connection traverse the same Virtual Path, and

their original sequence is thus maintained. The VPI value in the header designates the VP, but its use requires a translation process explained later in the next section.

The transmission line standard between ATM network elements (Switches and XC's) is assumed to be SDH (or SDH), e.g., 155 Mb/s OC-3c, 622 Mb/s OC-12c or 1.4 Gb/s OC-48. As specified in the standards, ATM cells are mapped into the payload of the SDH envelope. Since the VPI value has 12 bits, each transmission link can carry up to 4096 unique VP's. The processing of the SDH overhead and ATM cells in the payload is an important part of the line interface at each ATM XC (often called "line cards"). The delivery of cells according their VP, namely VP transport, plays an important role in ATM networking because of its flexible service and fast restoration capabilities [3]. We will focus on the operation of VP transport by describing an overview of an integrated ATM XC.

3. ATM Crossconnect Functions and Requirements

When ATM cells are carried as payload in the SDH envelope for optical transmission, they have to be recovered before switching can take place at each ATM XC. The function of receiving the optical signal, terminating its SDH overhead and recovery of its payload (i.e., ATM cells) is usually called the LTE (lightwave terminal) function. The VP switching of cells is of course the main goal of the XC. VP switching here means the routing of the incoming cells to the appropriate output ports according to their VPI values on a cell-by-cell basis. Although not required, today's technology permits an integrated design whereby both the LTE and the VP switching functions are combined in a single machine. The LTE part is implemented mostly in the line cards, and the VP switching in the "XC fabric". For subsequent discussions, we only consider an integrated ATM XC.

Various essential functions required in an integrated ATM XC are summarized in Fig. 3. After optical detection, the received SDH signal is descrambled and frame synchronized so that the overhead bytes can be retrieved. Processing of these overhead bytes is required to provide several maintenance functions such as line integrity, line protection switching, inter-XC data communications, etc. Furthermore, pointer processing has be performed to establish synchronization for recovering the "floating" frames (called virtual containers) of ATM cells in the payload. The beginning of each cell has then to be identified within the virtual container. After the cells are extracted, they have to be properly processed before the actual switching, and this part may either be implemented in the line card or as part of the XC fabric.

In ATM cell processing, OA&M (operation, administration and maintenance) cells are separated from data cells. OA&M cells may be destined for the local system controller or for further transport. The data cells are first processed with HEC (header error correction). Cell headers with 1-bit errors can be corrected, and those with more than 1-bit errors are discarded immediately. The VPI value is then examined in a table look-up for validation and also to identify the output port for the routing of each cell. Cell routing is implemented in the XC fabric which is functionally identical to a conventional ATM switch fabric. As such, cell buffering is required because multiple cells may destine for the same output port at the same time. This aspect has been well understood in ATM switching. In addition to the routing, the most most important processing is perhaps the translation of the incoming VPI value in each cell to a new value (preassigned by network control). That is, for each cell transit through the ATM XC, there is a unique mapping of its incoming VPI value to its outgoing value. Consequently, a VP can be characterized by a unique series of VPI values along the various physical links in its route. Doing so allows for maximum utilization of the VPI values (limited to 12 bits) in each physical link.

At an output port of the XC fabric, cells from different inputs are multiplexed together to form a stream. They have to be individually checked for errors and to verify proper routing (plus internal diagnostics) before passed on as input to a SDH processor. In this SDH processor (output line card), the ATM cells are inserted into the payload envelopes, and new pointer and other overhead bytes are included in the final assembly of the whole SDH signal for optical transmission.

The capability of electronics is advancing rapidly to meet the requirements of high-performance ATM network elements. An integrated prototype ATM XC recently demonstrated includes an 8×8 ATM fabric operating at 2.5 Gb/s and with multiple-rate line cards (OC-3c to OC-48) [4]. This is equivalent to a total system capacity of 20 Gb/s, supporting up to 128 bidirectional OC-3c (155 Mb/s) interfaces or up to eight bidirectional OC-48 (2.4 Gb/s) interfaces. Expansion to much larger fabric sizes is possible and is being researched.

4. Conclusions

VP transport is a fundamental aspect of ATM networking. It provides flexible service and fast restoration capabilities in next-generation networks. An ATM XC capable of cell-by-cell routing is a key network element to support VP transport. In addition, extensive SDH and ATM cell processing is required in implementing the ATM XC, today's VLSI technology is adequate to meet these challenges efficiently and economically.

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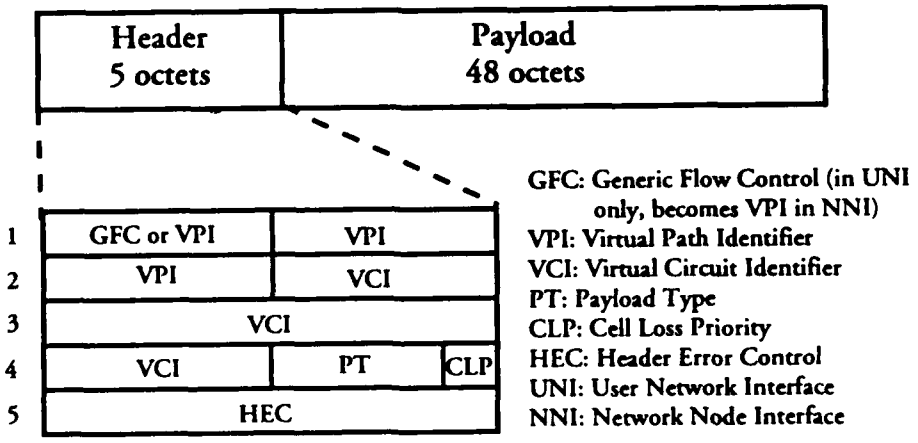


Fig. 1 ATM Cell

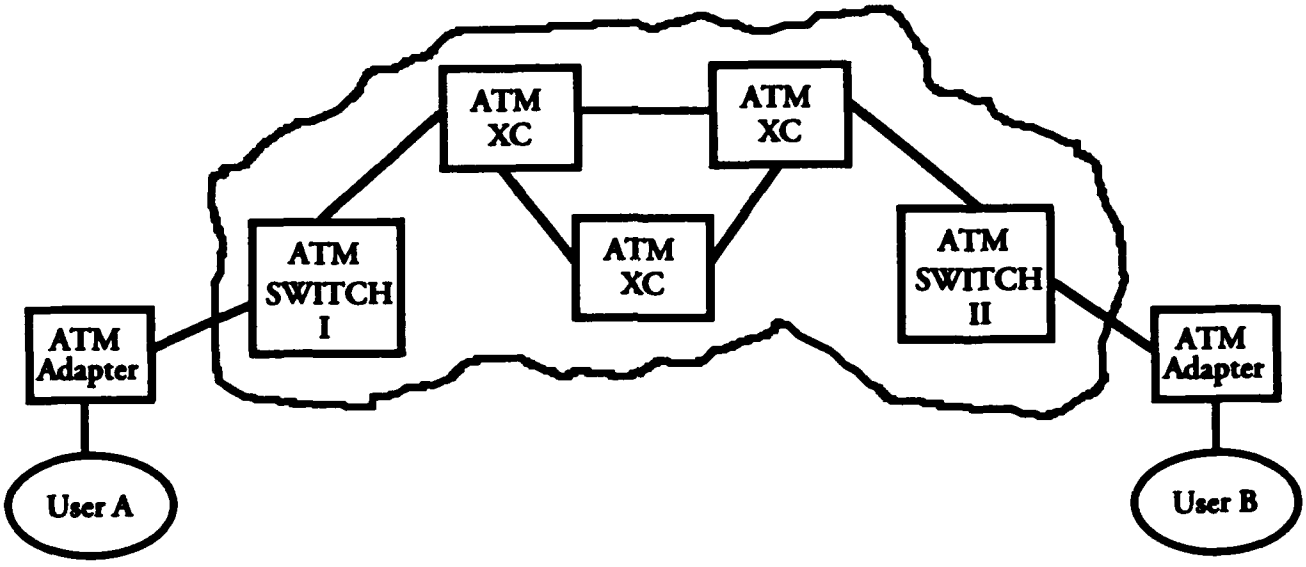
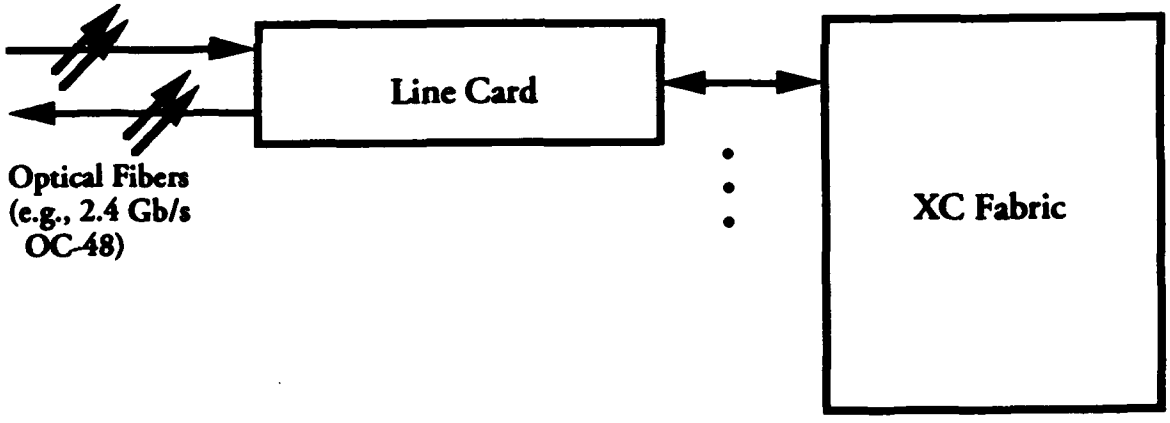


Fig. 2 An ATM Network Example



- SDH Overhead Termination
  - SDH framing
  - Timing recovery and synchronization
  - SDH overhead extraction
  - Pointer processing
  - Protection switching
  - Line and section parity check
  - Cell framing
- ATM Cell Processing
  - Cell synchronization
  - VPI validation
  - VPI table look-up
  - HEC
  - Internal diagnostics
  - OA&M
- XC
  - Physical routing
  - Cell buffering
  - Protection switching

Fig. 3 Essential Functions of An Integrated ATM XC

Photonics in switching: European systems demonstrators and the long term perspective

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ABSTRACT

Status in the area of photonics in switching in Europe, highlighted by systems demonstrators, is reviewed,and the long term perspective for photonics in switching is discussed.

1 INTRODUCTION

It is widely recognized that the progress and role of photonic switching have not paralleled that of fiber optics point to point communications, where new avenues for fiber optics keep opening, most recently in the shape of *fiber to the home* and the associated introduction of broadband services. The discussions concerning fiber to the home, and the corresponding systems issues, seem to have been only marginally influenced by the possibilities offered by photonic switching. Part of the explanation for this state of affairs is the competition from electronics, and the uncertainty of the actual bandwidths required by different services and subscriber categories, but mostly the lack of clear and verifiable systems solutions where photonic switching offers significant and unique advantages. In addition, we have the comparative immaturity of the device technology required as well as the lack of a practical and reasonably standardized way of assembling optical systems. This situation is reflected in the comparatively small number of systems demonstrators and the virtually nonexistent field trials to date. Ref [1], [2] are exceptions here, but they can not be described as fully fledged field trials.

This paper discusses development over the last few years concentrating on the European scene, where several European research programs (COST as well as RACE) have included projects (especially the RACE OSCAR R1033) more or less devoted to photonic switching. Some current representative systems demonstrators are described. Comments on the relationship between electronic and optical switching, based on switching energy, pertinent for ATM switching, are finally made.

This paper concentrates on *guided wave switching systems and devices* , there are strong proponents of *free space 3D systems and technology* , [3], [4]. However, the situation here is even less mature as far as technology is concerned, and systems proposals and technology demonstrated so far are no more convincing than the guided wave concepts. The rationale and motivation for *integrated photonics* in photonic switching is the same as those underlying the unparalleled success of *integrated electronics* .

2 DEVELOPMENTS IN PHOTONICS IN SWITCHING

The rationale for photonic switching is the uncontested bandwidth and loss of the optical guided wave transmission as well as the speed allowed by optical interactions. Different attempts have been made to

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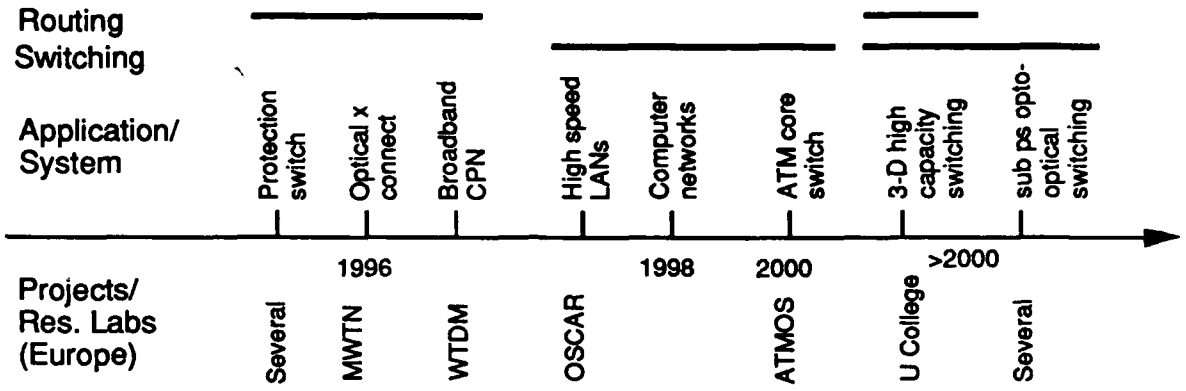

Figure 1: Evolution scenario of photonic switching. Years indicate possible time of field trial. MWTN, WTDM, ATMOS and OSCAR are RACE projects, mentioned in the text

shape this into new systems architectures, ("optical ether"). Broadly speaking, this has led to a number of schools:

A) Circuit type low speed switching, involving switching in space and wavelength

B) STM, ATM and PTM type switching, where optical temporal switching is involved,in some cases in conjunction with wavelength and space division switching.

C) 3D optical interconnects in combination with OEICs, where the processing is (mainly) electronic and the transmission optic.

D) Whereas the above approaches can in essence be classified as *optical interconnect under electronic control*, there also is the possibility for *opto-optical switching* , e g via soliton interactions [5]

Crucial in all attempts to apply temporal switching is the lack of an optical RAM type memory, comparable in integration and performance to electronic ones, since various degrees of synchronization and storage are required. It appears that only wavelength and space division switching make use of the bandwidth in a way commensurate with the bandwidth of the transmission medium, thus creating a novel fiber optic "network" that is to a degree bitrate and coding independent ("transparency"). It should be borne in mind that we are dealing with an *analog, nonlinear* network. However, time division switching type network structures have been suggested and partly demonstrated, where optical switching functions are simple and in some cases memoryless ([6], [7]), again taking advantages of the basic features of the optical transmission medium. See also [8]. One could attempt to structure the development in photonic switching according to Fig 1.

3 SYSTEMS DEMONSTRATORS

The systems demonstrators, which in some sense can be labeled as photonic switching ones, currently developed within the RACE program, are part of the following projects: Wavelength and time division multiplexing (WTDM) broadband CPN network, Multiwavelength transport network (MWTN) and ATM optical switch (ATMOS). The first two are essentially in category A) in section 2, the third in category B). All these projects are based on RACE I projects. In addition there is a German program, which addresses ATM type switching. The talk will discuss these projects, two of which are described below. Fig 2 shows the basic structure of the R2039 ATMOS demonstrator [9]. This utilizes synchronized ATM cells at the input (for all practical purposes of electronic origin). The cell encoder wavelength encodes the packets utilizing wavelength converters (eg in the shape of bistable DBR lasers). Contention is resolved by a cell buffer block with K fiber optic delay lines (K=16 in a suggested system; with no contention, this entire block can of course be deleted). Power splitters and optical gates (semiconductor laser amplifiers) route the packets to the pertinent delay line. The packets (still of course synchronized), enter a space switch in the shape of a star coupler, with optical filtering at the output. Four layers of this type, each comprising a Clos net with 3 stages of 16 × 16 switches will have a total throughput of 10 Tb/s, with a 10^{-9} cell loss rate for 16 cell buffers (fig 2), with $10\mu s$ delay. The line rate is 2.6 Gb/s. A rigorous comparison with an all electronic system still remains to be done and is a challenging research topic. It

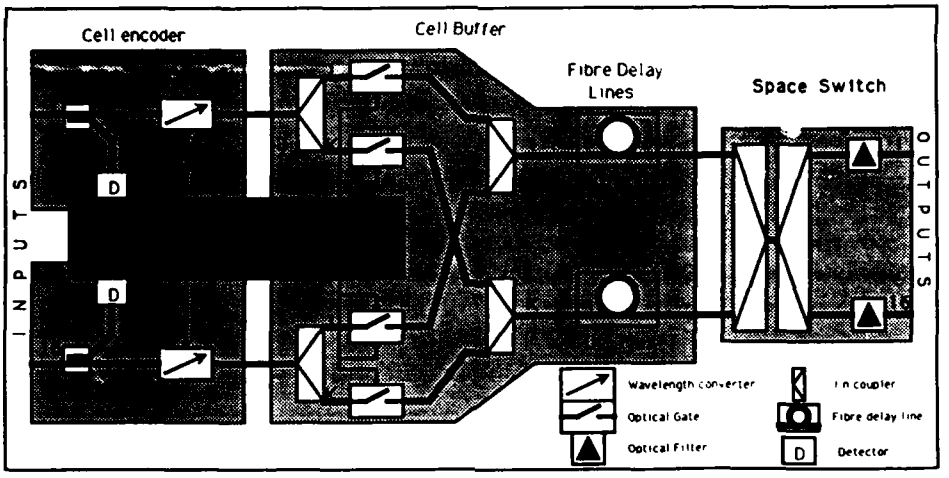

Figure 2: ATM optical switch (ATMOS) system demonstrator

should be noted that impressive results have been reported recently on fiber optic delay lines, applicable to this concept [10]. The ATMOS system presents a number of very challenging device requirements, notably wavelength converters and optical storage. Fig 3, on the other hand, represents an example of a *routing system* [11], see also [12]. The structure in fig 3 performs routing in the space and wavelength domains. Hence, we are not concerned with a reconfiguration of the network, more rapid than that called for by eg protection switching ($> \mu s$). The core of the network is formed by tunable lasers in the transmission system, tunable filters and space switches in the switching system and fiber amplifiers in a line system. Also important (but historically given little attention in systems like this) is the control system. Since the signals are not immediately available in electronic form (with a few exceptions, such as laser amplifiers [13]), the control system has to be structured accordingly, and the devices provided with control interfaces, the need of which is not superficially obvious. Two issues of prime importance are wavelength referencing and power equalization. The system in fig 3 constitutes a logical extension to the existing transport network concepts, adding flexibility, reliability as well as resilience, by performing routing in a frequency and code transparent way. The systems claims made here (the underlying systems rationale is about the same in WTDM) are maybe not as far reaching as for ATMOS, but the application appears reasonably near term. In fact, in view of the continued development of the transport network with electronic cross connects, the optical cross connect appears to be a good candidate for a fairly imminent application, being uncontested by electronics.

4 HIGH SPEED SWITCHING: PHOTONICS OR ELECTRONICS OR BOTH?

A view often advocated in the optics community is to justify photonic switching by extreme speed and superior bandwidth. However, MODFET transistors have been reported with speeds up to 500 GHz, and several roads into the THz realm exist: Superconductors, quantum interference, single electron transfer, and brute force scaling of dimensions. The last exercise has given uninterrupted *exponential* performance growth since the 40s! "Fundamental" limits appear to be no hindrance to continued development for the next few decades. This means that electronic integration levels, switch energy as well as speed will continue to improve. Concerning integration and switch energy, it appears that basic considerations prevents photonics from presenting a viable alternative to electronics [14]. Hence, the combination of photonics and electronics has to be given serious consideration. One example could be low level of photonic integration (where dissipation is less of a concern) for extremely high speed (sub ps) multiplexing and demultiplexing, with the slower and complex (more integration intensive) tasks carried out by electronics.

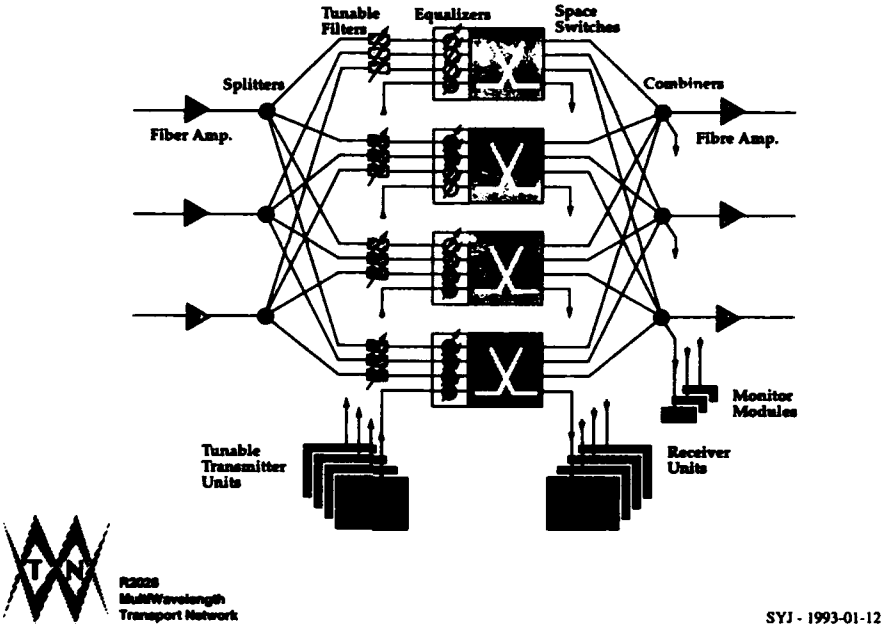

Figure 3: MWTN system demonstrator

5 CONCLUSIONS

This paper has described two representative examples of photonic switching demonstrators, showing different approaches, differing device requirements and addressing different time perspectives. It should be emphasized that photonic switching can not be seen in isolation but only from a total systems perspective. Some research items of photonic switching can be identified: Rigorous research on electronic vs photonic switching, including systems considerations; the potential of extremely high speed, low integration switching using nonlinear optical interactions, such as solitons; 3D reconfigurable interconnect, combined with OEICs. While these are certainly worthwhile to pursue, it appears that the span to the present needs to be bridged by more applied research; thus field trials are highly desired in the next few years, unless photonic switching is to share the fate of at least part of the field of optical computing.

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Transition from Optical Interconnections to Optical Computing

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Optical interconnections will be a foot in the door to the next generation of computer systems and provide an evolutionary path toward the use of optics at finer scales.

Poster Session

PTuD 6:30pm-8:00pm
Grand Ballroom Center

Holographic Perfect shuffle interconnections for planar optics

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I. Introduction

The perfect shuffle network is one of the regular multiple-stage interconnection networks with wide applications for telecommunications and parallel computing processors.[1] Optical implementation of the perfect shuffle interconnects has been mainly achieved by the use of free-space optical components, such as lenses, prisms, or holograms.[2,3] In order to implement the interconnects in a compact, robust, and alignment-free manner, technologies of planar integration of the free-space optical components[4] are required. In this summary, we propose a planar optical configuration which can carry out the perfect shuffle interconnects, and it is suitable to link areas of a wafer scale integrated circuit together by means of computer-generated holograms(CGH). Two double-imaging diffractive-reflective CGH's are used as key components acting as a set of four lenses in the free-space configuration of Ref.3. Interconnection capacity of the proposed planar system and the optimum number of internal reflections in an optical substrate are also derived by analyzing aberrations of the CGH's.

II. Perfect shuffle using a computer-generated hologram

In the folded perfect shuffle implementation[3] using a set of four conventional lenses or four holographic lenses, the input data are separated into four quadrants. Each quadrant is magnified to the original size and shifted for interlacing, and the quadrants are recombined into a single imaging pattern. The use of hololenses generated by computer is known as a more practical approach for integration to an optical substrate, since we can make them as surface relief holograms by lithographic techniques. Also It is possible to replace the four lenses with a multiple-imaging CGH. This CGH can be designed as an interferogram from the interference between diverging wavefronts from four point sources and a converging wavefront, so that it produces four images in the present of one input pattern[5].

Figure 1(a) shows the schematic diagrams to implement the folded perfect shuffle using the CGH. The input pattern consists of four quadrants, and each quadrant has the 2x2 pixels arranged to give an input format of the folded perfect shuffle. This would give the folded perfect shuffle in the center block of the output plane. The pixel arrays shaped with different patterns are interleaved, that is perfectly shuffled at the center. In the experiment, Fig.1(b) and Fig.1(c) show respectively an input with pixels of size $(50\mu m)^2$ and the experimental output obtained from the monitor screen. The 4x4 pixel array shown at the central region of Fig.1(c) is the result of the folded perfect shuffle interconnection.

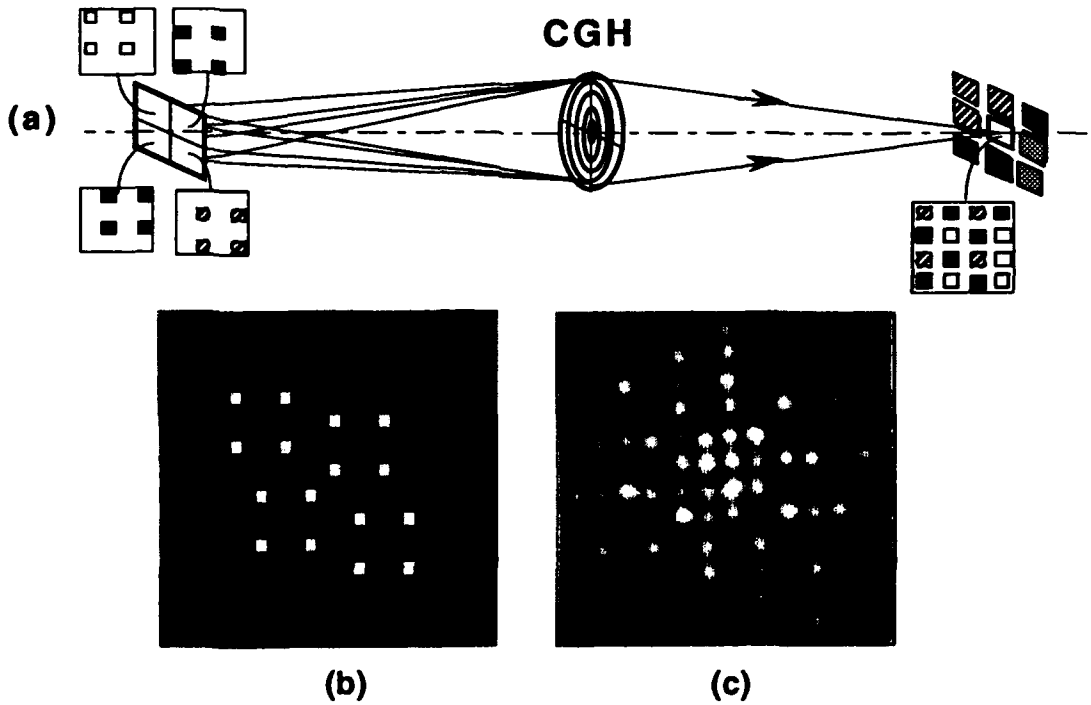

Figure 1. Folded perfect shuffle interconnection using a multiple-imaging CGH. (a); schematic diagram, (b); input with 4x4 pixel array (50μm^2 pixels), (c); experimental result of the perfect shuffled output shown at the center region of 4x4 pixel array.

III. Planar optics implementation

It is known that the planar integrated system which consists of an even number of diffraction gratings suffers less from wavelength dependence, since the diffraction angle relating to the different wavelength can be compensated exactly[6]. Therefore, when we implement a planar optical system based on the configuration shown in Fig.1(a), it is better to use two double-imaging CGH's, instead of the single multiple-imaging CGH of Fig.1(a). The planar configuration proposed here is depicted in Fig.2(a), and its equivalent diagram of an unfolded optical system is shown in Fig.2(b). The planar system of Fig.2(a) consists of two substrates, optical and optoelectronic integrated circuit(OEIC) embedded substrates, interfaced by the solder-bump bonding technique in order to achieve an alignment accuracy of less than 2μm[7]. The two double-imaging CGH's, CGH-Z and CGH-Y, are surface-relief phase holograms designed as an interferogram from interference between diverging wavefronts from two point sources and a converging wavefront with an angle, θ. They make, respectively, two images of the input object of laser diode array(LDA) onto the positions of P, and four images onto the photodiode array(PDA) as shown in Fig.2(b), via multiple internal reflections in the optical substrate. That is, the CGH-Z produces two identical patterns shifted with respect to each other in the direction of z-axis, and the patterns are again doubly imaged in the y-axis by the CGH-Y resulting in a 4x4 array format on the PDA.

IV. Interconnection capacity

The interconnection capacity, which is defined as the maximum number of input channels (laser diodes) to be connected by the planar optical system of Fig.2(a) to the same number of detectors, would be restricted by the aberrations of the double-imaging CGH's and by the choice of architecture. The third order coefficients of spherical aberration(S), coma(C), and astigmatism(A) of the Brandt-type hololens[8] are considered here to obtain the interconnection capacity.

When the Gaussian beams($\exp[-x^2/\omega_o^2]$) emitted from the LDA pass through the interface between air and the optical substrate, refraction occurs. Therefore, we can consider the effective optical path length from LDA to CGH-Z to be $R_O=n(Z_O+t)$ [9], where n and t are the refractive index

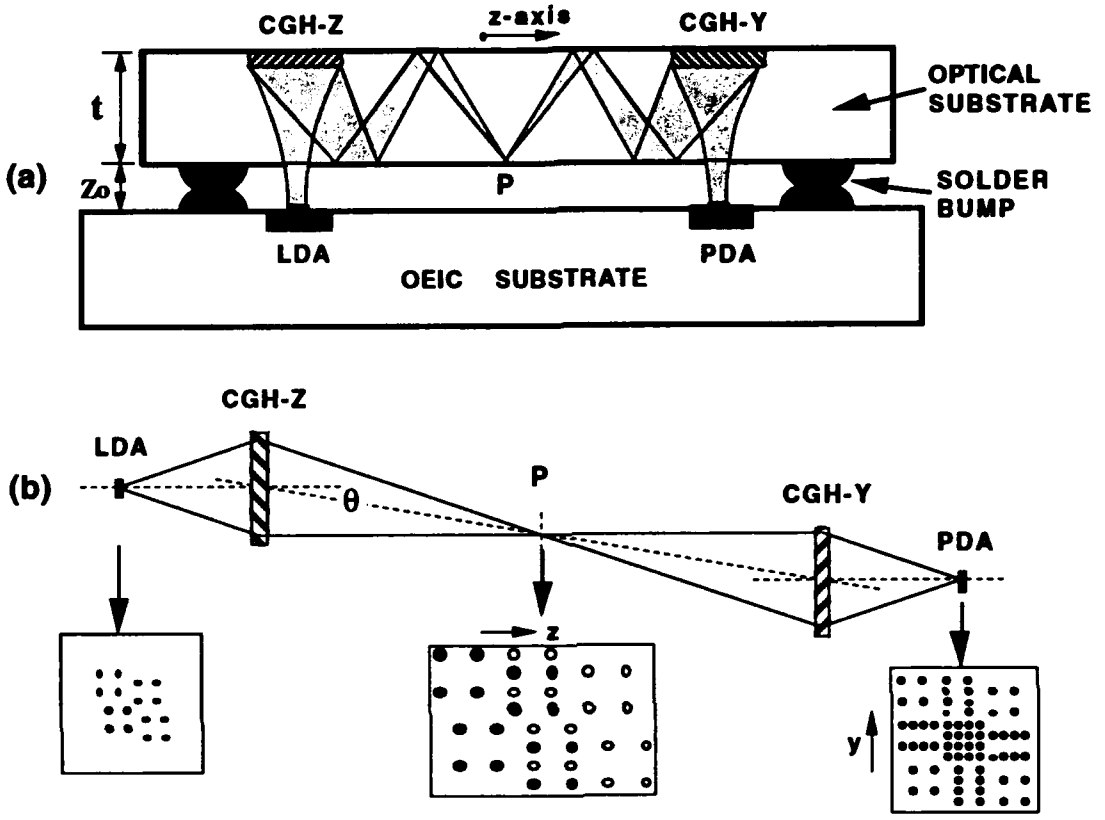

Figure 2. (a); planar optics configuration for the perfect shuffle interconnects using two double-imaging computer-generated holograms, CGH-Z and CGH-Y. (b); schematic diagram equivalent to the planar system of (a).

index and thickness respectively of the optical substrate. The air gap Z_O between the substrates is assume to be uniform and equal to 20μm, the height of the solder-bump[7]. The path length from the CGH-Z to point P is also given by $R_R=n(bt/\cos\theta)$, where b is the number of reflections when the beams propagate from LDA to P (b=3 in the Fig.2). The total aberration can be derived by[8]

$$|\Delta| = -\frac{D_c^4}{8\lambda} S + \frac{D_c^3}{2\lambda} C + \frac{D_c^2}{2\lambda} A, \quad \text{(in units of } \lambda) \qquad (1)$$

where, $S = 0$,

$$C = \left(\frac{1}{R_o^2} - \frac{1}{R_R^2}\right)\sin\alpha,$$

$$A = \left(\frac{1}{R_o} - \frac{1}{R_R}\right)\sin^2\alpha - \left(\frac{2\sin\theta}{R_R}\right)\sin\alpha,$$

$$\sin\alpha = \left(\frac{\delta x}{R_o}\right), \qquad D_c = 2k\sqrt{1+\left(\frac{\lambda R_o}{n\pi\omega_o^2}\right)^2}.$$

Dc is diameter of the CGH-Z, the constant k is the ratio of Dc/2 to the Gaussian beam waist at the CGH-Z plane, and δx is the half width of the input object(LDA). Figure 3(a) shows the total aberration (in units of λ) of Eq.(1) as a function of δx (in units of μm) for different beam waists, ω_o, at LDA, when λ =0.85μm, t=10mm, k=1.52, θ=15°, Z_o=20μm, n=1.5, and b=3. As ω_o increases from 5μm to 20μm, the aberration decreases from 0.5λ down to 0.1λ when δx=500μm. It is noted that the resolution limit of CGH-Z, which is defined by 1.2λf/Dc, is 4.7μm when ω_o=5μm, and 18.4μm when ω_o=20μm. Therefore the value of ω_o can be taken as a minimum pixel size of the input channels imaged by the CGH-Z. If we take $|\Delta|=\lambda/4$ as a maximum aberration to be tolerated in the planar system, and define R_x to be the smaller magnitude between positive and negative δx when $|\Delta|=\lambda/4$, then the maximum number of input channels (N) can be obtained by dividing $2R_x$ with the channel spacing (or center-to-center spacing of the laser diodes), $2x(2k\omega_o)$. As an example, when ω_o=5μm, R_x is given by 360μm, and so N=23. In the case of 2D array, the interconnection capacity (or the number of input channels) are $N^2=23^2$. For a larger ω_o than 5μm, N becomes smaller. Therefore at least 16x16 input channels are possible in the planar system of Fig.2(a), with the physical dimensions of the laser diode diameter; $2k\omega_o$=15.2μm, the glass thickness; t=10mm, and Z_o=20μm. Figure 3(b) shows the $|\Delta|$ according to the number of reflections, b, for the case of ω_o=5μm. When $|\Delta|=\lambda/4$, R_x=360μm for b=3, R_x=340μm for b=4, and R_x becomes much smaller for the other cases of b. Therefore, we can choose the b=3 as an optimum number of internal reflections in the optical substrate.

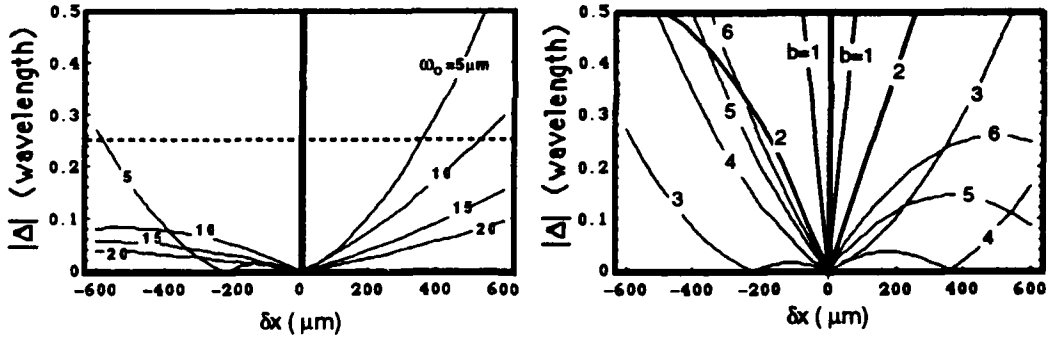

Figure 3. Total aberration, $|\Delta|$, as a function of δx for the different beam waists, ω_o, in (a), and for the different number of reflections, b, in (b).

In conclusion, by using two double-imaging CGH's we have proposed and analyzed a planar optics configuration for 2D perfect shuffle interconnections. It has been found that at least 16x16 2D input channels can be connected by the proposed planar system, when the beam waist, ω_o, at the LDA is 5μm and the number of internal reflections, b, is 3.

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An optoelectronic hybrid multi-stage interconnection network

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1. Introduction

Multi-stage interconnection networks (MINs) can be employed in switching systems and in interconnections of processors. The interconnection patterns in MINs, "perfect shuffle", "butterfly" or "crossover", are particularly appropriate for optical implementation [1]-[4].

Generally optics can be used for high speed data transmission nearly without cross-talk. This natural feature of optics is its strength but also its weakness, if optics must be used for switching. On the other hand electronics can switch signals quite well, but it is unsuitable to transmit data at high speed over long distances. Beyond a distance of about 1 mm optical interconnections can be more advantageous than electronic interconnections [5]. Therefore, we introduce a hybrid MIN with self-routing electronic switching elements (SEs) which are connected electrically for short distances and optically for long distances. In this way we combine the advantages of optics with the advantages of electronics.

Because additional laserdiodes (LDs), drivers for LDs, photodiodes (PDs), amplifiers for PDs and optical components like hologramms, lenses and beam splitters are still necessary for optoelectronic interconnections and cause more cost, we ought to realize the electronic switching module (SM) with many SEs as possible in order to save optoelectronic interconnections. An electronic SM is an electronic island with electrically interconnected SEs. This basic idea is well known and proposed in [6].

In the following, two new approaches to modularize the MIN for optoelectronic hybrid realization are introduced. A new design concept of a 3-dimensional optoelectronic MIN is described.

2. Architectural modification

In order to obtain suitable SMs the MINs must be modified architecturally. The optimal structure of the SMs is found if the SEs in a SM can be connected by short electronic interconnection paths up to 1 mm and the same kind of SMs can be deployed many times in a complete network.

2.1 Bitonic sorting network

First we consider a MIN based on the bitonic sorting algorithm [7]. This network was implemented as part of a self-routing switching network electrically [8] and also proposed for photonic implementation [9]. A bitonic sorting network can be implemented in the original form as shown by Batcher [7] (Fig. 1 (a)) or only with perfect shuffle as described by Stone [10] (Fig. 1 (b)). Unfortunately both implementations do not admit an optimal realization of the optoelectronic hybrid network described above if the number of the network inputs and outputs increases to several thousands. Both implementations show different structure from stage to stage.

In [7] Batcher shows the iterative rule for obtaining a bitonic sorter for SEs with 2 inputs and outputs (I/Os). To modify a bitonic sorting network in the sense described above, we extend Batcher's iterative rule from SEs to SMs. Instead of a SE with 2 I/Os we have a SM with 2^i I/Os. The perfect shuffle and the inverse shuffle in Batcher's iterative rule are substituted by two other shuffles. Considering here a bitonic sorter with $N = 2^n$ I/Os and using the matrix notation for the interconnection pattern introduced in [11], the perfect shuffle described by $S\left(2, 2^{n-1}\right)$ will be changed to $S\left(2^i, 2^{n-i}\right)$ $(i \le n)$ and the inverse shuffle $S\left(2^{n-1}, 2\right)$ will be changed to $S\left(2^{n-i}, 2^i\right)$. Batcher's iterative rule and the step to modularize a bitonic sorter are shown in Fig. 2 (a) and (b). The proof of the extended iterative rule is similar to the proof described in the appendix B in [7]. An example using this modularization approach on the fourth stage of the network in Fig. 1 is shown in Fig. 3 for $i=2$.

2.2 Modularization of other multi-stage interconnection networks

To modularize the third stage of the network in Fig. 1 (b) the approach described above cannot be applied, because this stage is not a bitonic sorter but a mixture of two bitonic sorters. There are three kinds of SEs with different switching functions: "higher address to upper output", "higher address to lower output" and "straight through". Modularizing an original MIN consisting of different SEs, we have to find out the switching function of the SEs in the modularized MIN. This can be done by obtaining an "address mapping algorithm of the SEs". Using this algorithm the corresponding SE in the original network can be found for each SE in the modularized MIN.

Because perfect shuffle, butterfly and crossover are isomorphic we only consider a MIN with $N = 2^n$ I/Os using perfect shuffle interconnection pattern. Each column of SEs is connected to the next column of SEs by perfect shuffle $S\left(2, 2^{n-1}\right)$. This perfect shuffle can also be described by a binary address of n address-bits a_1 to a_n which defines the position of the perfect shuffle input (left hand side of arrow) and the position of the perfect shuffle output (right hand side of arrow) [6]. Then the perfect shuffle is given by

$$a_1 a_2 a_3 \dots a_n \rightarrow a_2 a_3 \dots a_n a_1 \tag{2.1}$$

where a_1 to a_n can be 0 or 1. The most significant bit is here a_1.

The positions of SEs can also be defined by their binary addresses. They correspond to the binary addresses of the connections without the least significant bit. Now we want to obtain a MIN consisting of SMs with 2^i I/Os ($i \le n$) from the original MIN consisting of identical perfect shuffles and SEs. Assuming that the SEs in the SMs are interconnected by i identical perfect shuffle $S\left(2, 2^{n-1}\right)$, an address in the original MIN leads after i interconnections to

$$\begin{aligned} &a_1 a_2 a_3 \dots a_i a_{i+1} \dots a_n \rightarrow a_2 a_3 \dots a_i a_{i+1} \dots a_n a_1 \rightarrow a_3 \dots a_i a_{i+1} \dots a_n a_1 a_2 \rightarrow \dots \dots \\ &\rightarrow a_{i+1} \dots a_n a_1 a_2 a_3 \dots a_i \end{aligned} \tag{2.2}$$

The new modularized MIN with the first interconnection $S\left(2^i, 2^{n-i}\right)$ and i identical perfect shuffle $S\left(2, 2^{i-1}\right)$ leads after $i+1$ steps to the same result

$$\begin{aligned} &a_1 a_2 a_3 \dots a_i a_{i+1} \dots a_n \rightarrow a_{i+1} \dots a_n a_1 a_2 a_3 \dots a_i \rightarrow a_{i+1} \dots a_n a_2 a_3 \dots a_i a_1 \rightarrow \\ &a_{i+1} \dots a_n a_3 \dots a_i a_1 a_2 \rightarrow \dots \dots \rightarrow a_{i+1} \dots a_n a_1 a_2 a_3 \dots a_i \end{aligned} \tag{2.3}$$

The SE with the address $a_2 a_3 \dots a_i a_{i+1} \dots a_n$ in the first column of the original MIN corresponds to the SE with address $a_{i+1} \dots a_n a_2 a_3 \dots a_i$ in the new MIN and the SE with the address $a_3 \dots a_i a_{i+1} \dots a_n a_1$ in the second column of the original MIN to the SE with the address $a_{i+1} \dots a_n a_2 a_3 \dots a_i a_1$ in the new MIN and so on. In the ith column the SEs of both the original and the modularized MIN have the same address $a_{i+1} \dots a_n a_1 a_2 a_3 \dots a_{i-1}$. So the switching function of each SE in the modularized MIN can be found. A possible application of this approach on the third stage of the MIN in Fig. 1 (b) is shown in Fig. 4.

3. Design concept of a 3-dimensional optoelectronic MIN

The optical free-space interconnections introduced recently (see e. g. [1], [2]) show two essential disadvantages:

- requirements on mechanical tolerances are extremely high, especially for long slanted beams,
- it is difficult to obtain compact constructions.

These disadvantages can be avoided by using our new concept (Fig. 5). The complete network consists of a number of layered electronic chip carriers. Many electrically interconnected SMs (VLSI-dies) are mounted on the chip carrier, forming a multichip module.

Optical links are only used for the complex interconnections between layered chip carriers. The VLSI-dies are connected to 1-dimensional optical transmitter arrays (e. g. quantum-well laserdiode arrays) and 1-dimensional optical receiver arrays (e. g. photodiode arrays), which are mounted in direct neighbourhood of the VLSI-dies in order to avoid long electrical paths. Ideally, laser drivers and photodiode amplifiers are integrated on the VLSI-dies. In our first planned hardware realization separate driver and receiver arrays are considered.

The optical paths are folded twice, so a most compact construction is achieved. For beam folding reflective optical elements are prefered. For example, etched or molded 45°-mirrors utilizing total internal reflection are

adequate. Because free-space interconnections are difficult to obtain, we proposed the use of optical multimode waveguides. In this way even very long optical paths can be realized and the requirements on mechanical tolerances are widely uncrucial. The tolerable angle deviations must be less than about 0.1° if free-space interconnections are used. In contrast, the tolerable angle deviation is about 5° by application of waveguides with 1% difference in the index of refraction. In order to avoid undesirable crossing of waveguides and 45°-mirrors a multilayer construction as shown in Fig. 6 is possible.

4. Conclusion

With the two approaches introduced in this paper a MIN interconnected by "perfect shuffle", "butterfly" or "crossover" can be modified architecturally, so that SMs with appropriate number of I/Os are obtained. The modified network architecture combines the advantages of optics with the advantages of electronics. Also in electronic packaging and miniaturization several advances are expected in the next term. Based on the modified architecture a new design concept for a 3-D optoelectronic MIN is proposed which allows large mechanical tolerances and very compact constructions. The effort to produce the optical slabs can be reduced considerably by using the modularization approaches to obtain identical interconnection patterns from multi-chip-modul to multi-chip-modul.

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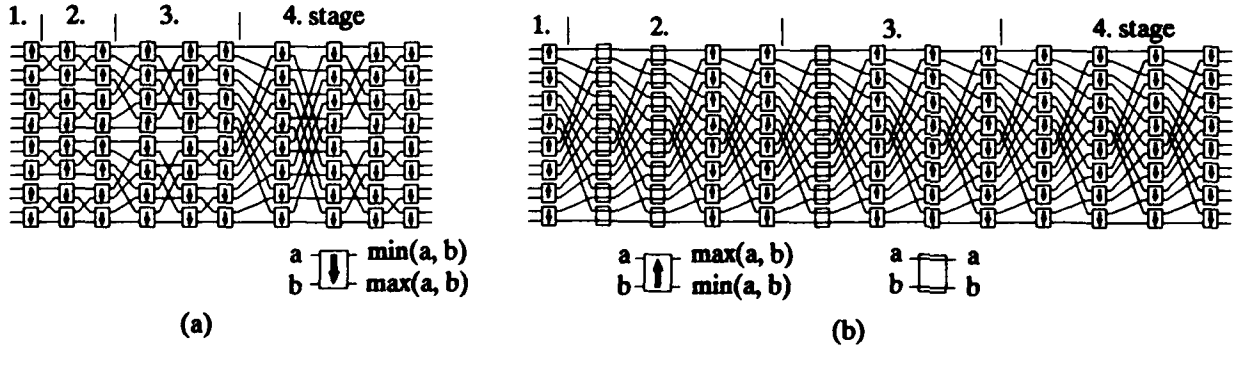

Fig.1 Bitonic sorting network proposed by
(a) Batcher [6]
(b) Stone [9]

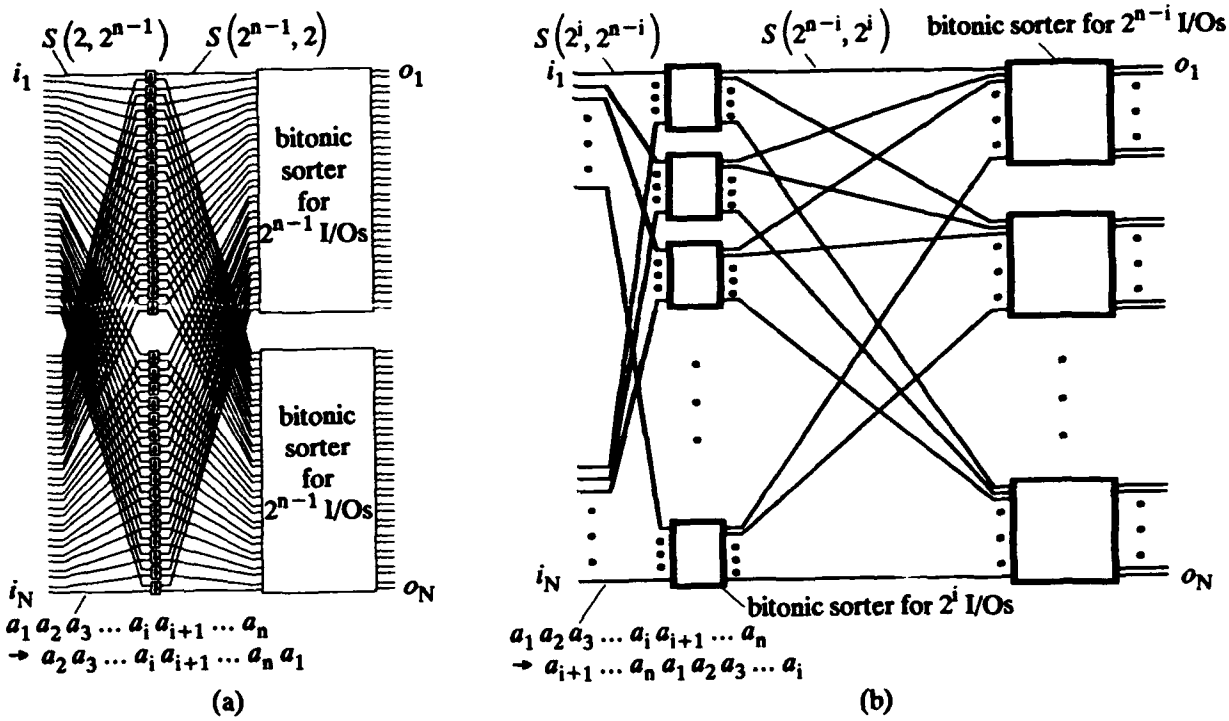

Fig. 2 (a) Batcher's iterative rule ($N = 2^n$)
(b) modified iterative rule for modularization of bitonic sorter

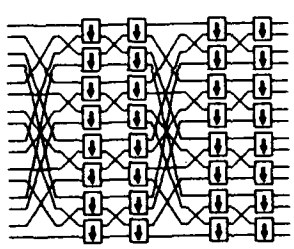

Fig. 3 Application of the modified iterative rule to the 4. stage of the bitonic sorting network in Fig. 1

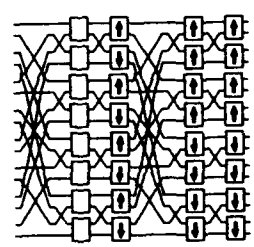

Fig. 4 Modularization to the 3. stage of the bitonic sorting network in Fig. 1 (b) using binary address moving

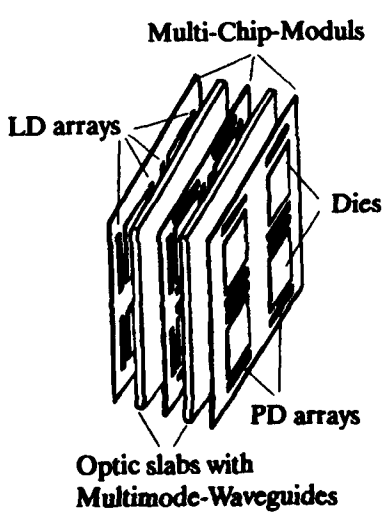

Fig. 5 Design concept of a 3-D optoelectronic MIN

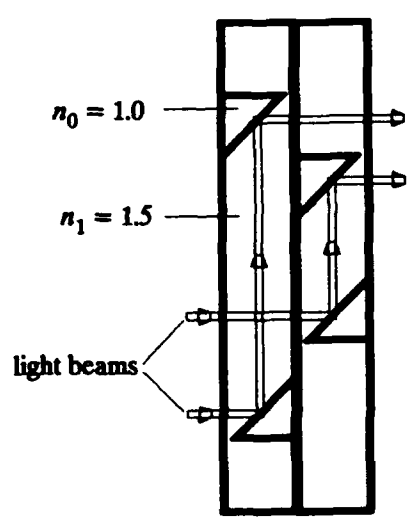

Fig. 6 A multilayer construction of the optic-slabs

Translation of laser tuning experiments into networks

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1. Introduction

Experiments on tunable lasers have been presented which show the high performance of devices as well as their capability to be integrated.[1] The aim of the present paper is to discuss some of the problems which arise if they are composed to an optical frequency division multiplexing (OFDM) system based on a multistage interconnection network with regular space-frequency interconnects. There the space interconnects (links) are deflected in a regular manner and at each link a fixed number of frequency channels is assumed which also are permuted according to a certain rule which is repeated at each stage. In this way, the least number of stages is needed for the nonblocking interconnection. The general concept presented may be extended to highly regular structures (nearest-neighbour interconnects).

2. Example

The way the laser is tuned to the frequencies (=ordered sequence of frequency channels) determines the permutation of the channels and in turn the topology of the frequency interconnects. First the laser is tuned to a channel, then this carrier is modulated according to the signal representing the data which then is transmitted and the data packets are stored at the destination array there waiting for being transmitted to subsequent stages (Fig. 1). The simplest experimental setup arises if the laser is tuned in one direction throughout the subsequently arranged and regularly spaced channels.[1] For convenience one may jump down from the highest frequency to the initial frequency and start the tuning within one cycle (16 channels in Fig. 2) but other strategies are also possible (Sections 3 and 4).

This sequential generation of frequency interconnects requires buffers at each stage (Fig. 1) and a balance may exist between the parallel generation of frequency interconnects (hardware costs) and the sequential generation (costs in terms of buffers and delay).

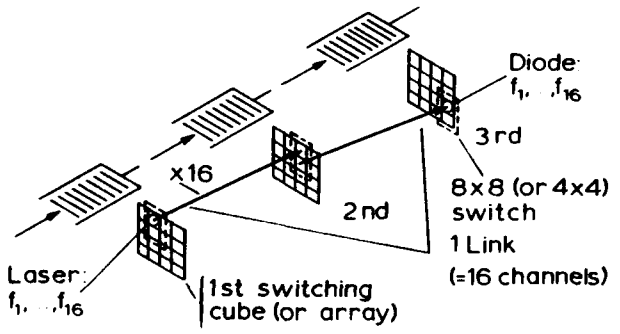

Fig. 1. Multistage space-frequency interconnects.

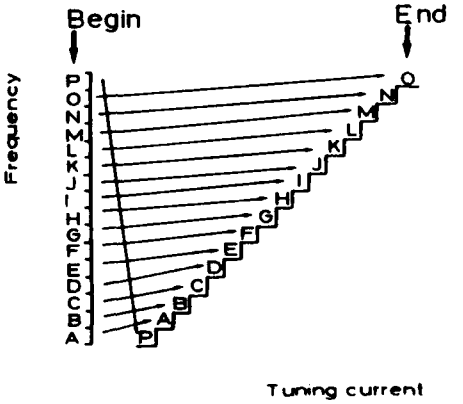

Fig. 2. Laser tuning experiment.

The simple experimental setup [Figs. 2 and 3 (a)] translates into local interconnects where data are only exchanged between nearest-neighbour channels [Fig. 3 (b)]. Thus the related OFDM system which is composed of several laser arrays whereby each link of an array operates according to the simple experimental setup may be evaluated by a MIN with local interconnects with regard to space and frequency.

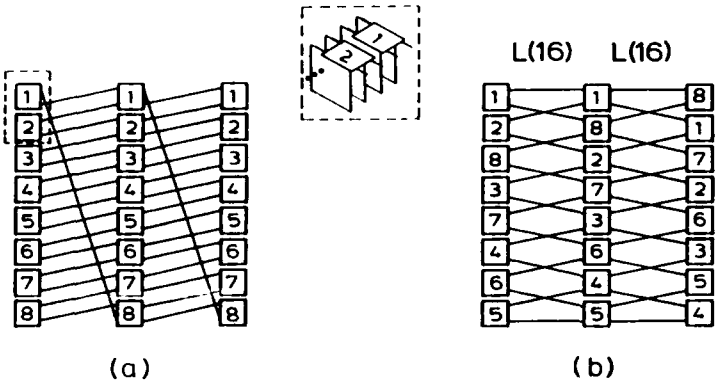

Fig. 3. Networks in the frequency domain.

Note a 2×2-module in Fig. 3 means the two ports of a switch (2 and 4 elements each for vectors and arrays, respectively) which is shown by the insert to Fig. 3. Switching within these modules describes frequency switching and the interstage pattern represents the frequency interconnects. Both, frequency switching and frequency pattern generation are characterized by the number of crossed channels ($d_{\sum}$).

3. Local interconnects

The permutation of a vector according to the local interconnection scheme and the assumption of frequency channels on each link which are permuted by the same rule [Fig. 4 (a)] causes MINs with 2-D local interconnects [Fig. 4 (b)]. Similar, the introduction of frequency channels on each link of an array and their permutation generates 3-D interconnects. Throughout the paper, assuming different organizations of laser tuning and different deflections of spatial interconnects, several topologies arise which all are aimed to be based on well-defined nets.

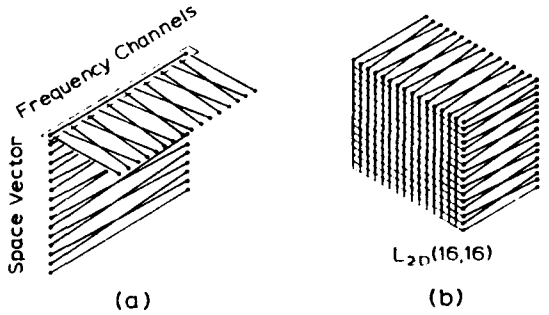

Fig. 4. Local interconnects for multiplexing on vectors.

The local MIN in Fig. 3 (b) is redrawn (Fig. 5) and the latter MIN is decomposed into a Spanke-Benes net[2] [Fig. 6 (a)] and into a modified Spanke-Benes net [Fig. 6 (b)].

Only one of these networks is active dependent on the state of the last switch in the middle stage of Fig. 5 (insert) and which depends on the control bit [0 for state (a) and 1 for state (b).] Thus we may implement the local MIN in Fig. 5 or its variants (Fig. 6) or combinations. For example, one may run the laser tuning experiment (Fig. 2) on a waveguide solution [Fig. 6 (a)].

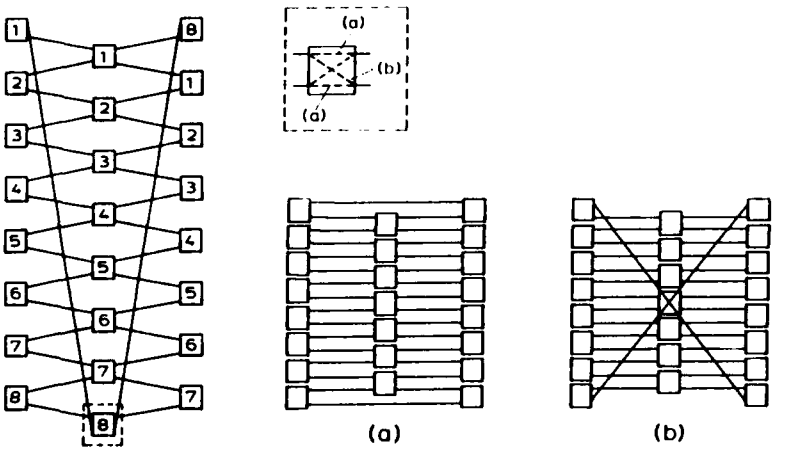

Fig. 5. Local MIN redrawn.

Fig. 6. Variants (a) and (b) of a local MIN.

The number of stages of the local MINs varies between N (Ref. 2) and the result for the local MIN in Fig. 6 (b).[3] These results are expected to be valid also for local 2-D MINs with N×N inputs/outputs iff 4×4-switches are applied. The number of crossed channels ($d_{\sum}$) for Fig. 3 (a) is N-1 and N-2 for Fig. 3 (b) whereas for Fig. 7 it is $3(N/2\text{-}1)$ with N=4,8,...

4. Shuffle interconnects

The most efficient control of MINs by selfrouting is based on shuffle-related interconnects (common shuffle, butterfly and crossover). One crucial problem is the high number of crossed channels during the generation of the frequency interconnects. Therefore, the application of shuffle interconnects via the final block structure (FBS) has been proposed.[4] This will simplify the experimental setup compared with the common shuffle and will reduce the number of crossed channels during the generation of frequency interconnects (Fig. 7). But the implementation of the FBS (readdressing) causes the resequencing of switches and in turn an increase of the number of crossed channels during frequency switching (Table 1). In Table 1 the interconnection of vectors is assumed and the switches are dimension-dependent. [For a pure space interconnection (1-D) the switch size is 2×2 and the same result for a pure frequency interconnection (OFDM on a single glas fiber), for a space-frequency interconnection (2-D) the switch size is 4×4 (see the two subsequently arranged 2×2-switches indicated by dots in Fig. 8). For example an 8×8-switch is distributed at four arrays existing on the frequency coordinate (Fig. 8). The number of channels crossed during switching is $d_{\sum}=12$, the weighted average is 2 thus the 8×8-switch is characterized by $\overline{d_{\sum}}=16$ crossings and approximately twice the results for the FBS (Table 1).

Table 1.

Switch	8×8	16×16	32×32	64×64
Shuffle: $\overline{d_{\sum}}$	16	150.8	1233.0	9616.5
FBS: $\overline{d_{\sum}}$	37.3	310.8	2432.2	19353.0

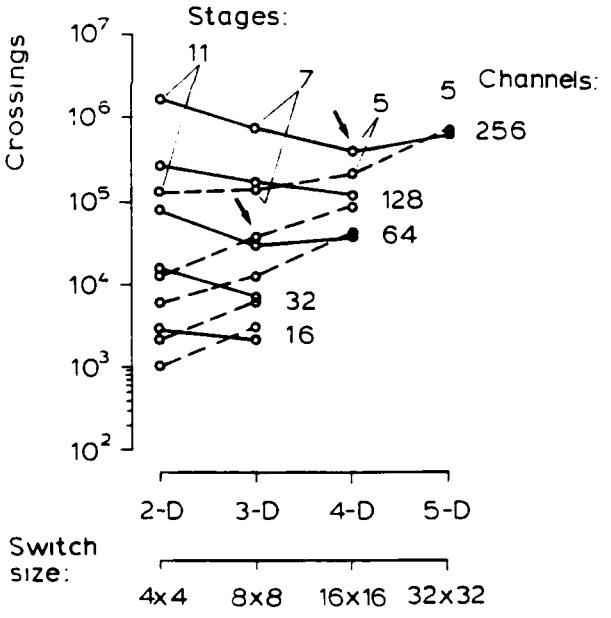

Fig. 9. Total number of crossings of shuffles (solid lines) and FBS (dashed lines) for the nonblocking interconnection of 8 OFDM links.

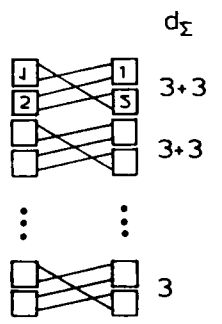

Fig. 7. FBS-implementation.

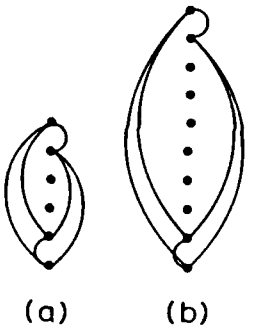

Fig. 8. 8×8-switch interconnects for shuffle (a) and FBS (b).

The results for the nonblocking interconnection (lower bound) of data by the shuffle, the Kronecker product (KP) of shuffles[4] and the FBS is presented in Fig. 9. By an appropriate organization of the frequency domain (increase of the dimension) the total number of crossings (pattern generation + switching) decreases with regard to the dimension or a balance exists (arrows). The least number of crossings occurs for the FBS and for 4×4-switches located at subsequently arranged arrays (dots in Fig. 8) where no crossing of channels occurs. But additional hardware costs (large number of stages) have to be considered in this case. The number of crossings increases with regard to the dimension (caused by additional switch interconnects).

5. Comparison

The interconnection schemes (KP of shuffles, FBS and local interconnects) have to be compa-

red with regard to the least number of crossed channels during pattern generation and switching. This is provided for the nonblocking interconnection of data arrays throughout Table 2 (2-D solution) and Fig. 10. For large arrays local interconnects are between shuffles (upper line) and FBS (lower line) though a large number of stages is required in the 1st case. For the shuffle the control may generate a block structure (BS in Table 2) but a homogeneous lay-out (1st number in the 1st column) is also possible ($\star$ in the 3rd column indicates the application of Fig. 7).

Table 2.

Data Set	Shuffle (BS)	Local	FBS*
4×4	16	24	24
8×8	384 (320)	560	288
16×16	5376 (4352)	4560	2016
32×32	61440 (50176)	34720	11520
64×64	634880 (528384)	262080	59520

The advantages of local interconnects are a small number of different deflection angles and a small amount of the angles, a homogeneous lay-out and a small number of crossings though the control seems to be more difficult.

6. Conclusions

Tunable laser experiments translate into networks which are tractable to be analysed with regard to the number of stages, blocking characteristics and queueing. The organization of the laser tuning prescribes the topology of the frequency interconnects and in turn the blocking and control characteristics of the net. Several possibilities have been shown which are represented by well defined nets.

Laser tuning may be organized in terms of shuffles, the final block structure (FBS) of shuffles and local interconnects. The results show that the FBS is superior (minor number of crossings and efficient shuffle-based control). The results for the Kronecker product (KP) of shuffles (dimension ≥ 3) and for local interconnects are between the common 2-D shuffle and the FBS.

Local interconnects are an interesting solution because of the small number of crossings (though they require a large number of stages), the simple organization of laser tuning and their implementation by simple and uniform components (nearest-neighbour interconnects for each frequency, for each link and for each stage).

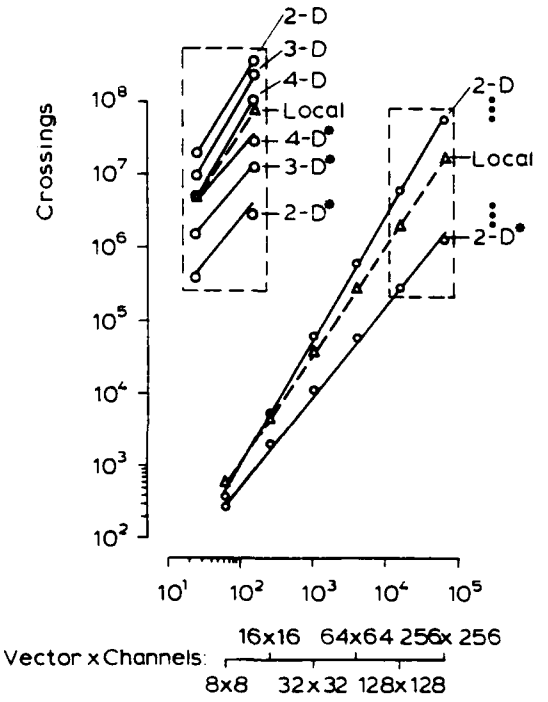

Fig. 10. Total number of crossings (pattern generation + frequency switching) for the nonblocking interconnection by shuffles (upper line), FBS (lower line and indicated by $\star$) and local interconnects (dashed line).

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Practical demonstration of a freespace optical crossbar switch

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1. Introduction

The use of free-space optics to perform high bandwidth connections for computing applications has been widely discussed in the literature. In this paper we present the practical results of a free-space optical crossbar switch which uses a ferroelectric liquid crystal spatial light modulator as the active switching element. This work has formed part of a collaborative project entitled OCPM which is concerned with developing optical free-space crossbar switching technology for use as the communications fabric for parallel computing systems. The OCPM project (Optically Connected Parallel Machines) is a collaboration between British Aerospace (Sowerby Research Centre), Meiko, BNR Europe, Heriot-Watt University, the University of Bath and Thorn EMI CRL. The project is coordinated by British Aerospace and is funded in part by the DTI and SERC.

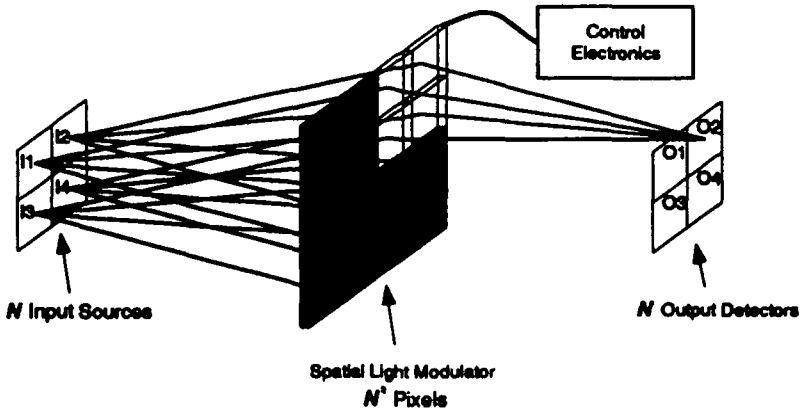

Figure 1: Matrix-Matrix Crossbar Switch

Figure 1 shows the principle of a matrix-matrix crossbar switch [1]. Each input is fanned-out and addresses N pixels on the SLM. Groups of N pixels (containing a channel from each input) are imaged onto one output channel. In this manner a fully non-blocking single stage switch, capable of full broadcast and multi-cast, is achieved. By choosing a matrix-matrix crossbar arrangement, instead of the more familiar vector-matrix geometry [2], the system is compact and thus the potential scalability is increased. In order to develop the optical components, a demonstration system was designed around a 16×16 electronically addressed spatial light modulator developed by BNR Europe Ltd. and Thorn EMI CRL Ltd. [3]. This is a binary reflective device with 100μm pixel mirrors on a 200μm pixel pitch and a reconfiguration speed of ~100μs.

2. Optical Design of the system

It is essential that future optical interconnections are compact and portable if they are to be fully integrated into computing systems. To this end the optical components of the crossbar were designed to be mounted on a single baseplate measuring 15cm×16cm. A novel channel-slot approach [4] is used to provide precise relative alignment. The layout of the optical system is shown in Figure 2, the lenses are custom-designed triplets (focal length of ~41.5mm) while the binary phase grating (BPG) is based on a non-separable two-dimensional design. Polarisation discrimination is provided by a polarising beam splitter between the triplet lenses, which reflects light along the output channel. L3 presents an aerial image of the SLM plane just in front of the fan-in optics LA1 and LA2. LA1 is a "micro-lens array" which collimates each beam, followed by a "macro-lens array", which focuses 4×4 groups of beams into the output fibres. Several pairs of lens arrays have been fabricated including (i) binary zone-plates; (ii) multi-level diffractive structures; and (iii) DCG holographic optical elements. In addition, the combining of LA1 and LA2 into a single binary element has been investigated.

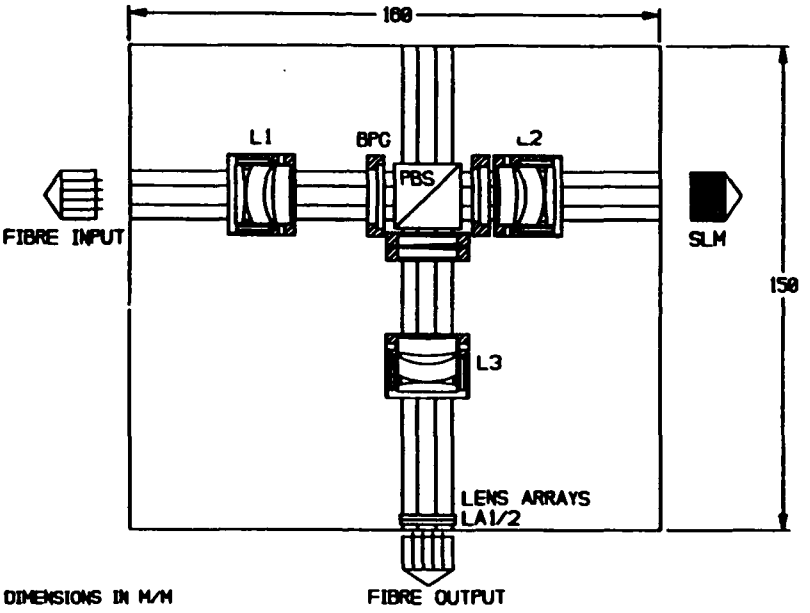

Figure 2: Layout of the 16×16 optical crossbar system

3. Pigtailed Sources and Detectors

Data is brought to and from the optical switch by means of optical fibres. This means that the high bandwidth sources and detectors can be incorporated into the processing boards, allowing all the off-board communications to be performed via fibres. As the SLM requires linearly polarised input light, the laser diodes for the system were purchased already pigtailed to polarisation maintaining fibres. These were PANDA fibres fabricated by Fujikura Ltd., which have a circular core of 4μm diameter and a cladding diameter of 125μm. The sources are Sharp LT024MD0 laser diodes operating at 793nm, in order to reduce costs, just three laser diodes were purchased, however, they could be connected to all of the fibres in the input array to test each of the possible links of the system.

The 16 input fibres were required to be accurately located in a 4×4 square array with a centre to centre spacing of 200μm. Thus, the one to one imaging of the lens system would match the input fibre array to the pixel spacing of the SLM. The technique employed to construct the 2-D array of input fibres was by means of excimer laser drilled holes in polyimide. Two sheets were used in an attempt to provide better angular alignment of the fibres. The holes drilled by the laser have tapers of about $\pm 1.5°$ and this can cause lateral errors in the core position when the fibres have been polished. By aligning the arrays in two pieces of polyimide, better angular alignment can be achieved. The fibres were sequentially fed though the holes and rotated so that the optical axis of the PANDA fibre was in line with that of the polarising beamsplitter. Once this was achieved the fibre was glued in place and the next fibre of the array was inserted.

If similar fibres were used for both the input and output arrays a $\frac{1}{N}$ intrinsic fan-in loss would be incurred according to Louiville's theorem [5]. To avoid this, multimode fibres of 100μm core diameter and a cladding diameter of 140μm were employed as the output fibres. These were constrained in the form of a 4×4 array with a 800μm pitch. Square holes wet etched in silicon were used to align the fibres and again two such arrays were used to avoid angular misalignment of the fibres. 16 photodiodes pigtailed to such multimode fibres have been incorporated with suitable amplifier electronics.

4. System Performance

The misalignment of the fibres in the input array was on average 5μm although an error of 15μm was noted for one fibre. Improvements in the alignment can be achieved by polishing the fibres right back to the substrate. The BPG used in the system has an efficiency of 74.5% ±0.5% and a uniformity of 3.0±0.5%. Used with the triplet lenses it produces 4×4 images of the input fibres on to the SLM with individual spots of ~9μm diameter showing that the system is near diffraction limited.

Figure 3 is a photograph of the system and Table 1 summarises initial results of the optical losses for a single channel of the crossbar switch. For a 2mW output from an input fibre end a detected intensity of 400nW was observered. Considerable scope exists for improving on this overall efficiency, as indicated in Table 1. Initial tests with three input channels operating have shown that this system is capable of performing with a BER of 10^{-12} at a data rate of 500MBits/s.

Component	Transmission %	Current Losses dB	Predicted Losses dB
Connector	85	-0.7	-0.2
Intrinsic Fan Out (1/16)	6.25	-12	-12
Excess Fan Out (BPG efficiency)	70	-1.55	-1.2
SLM	10	-10	-3
Beamsplitter (and other reflections)	76	-1.2	-0.5
Macrolens array	40	-4	-1.5
Microlens array	40	-4	-1.5
Fan-in to output fibre	74	-1.3	-1
Connector	85	-0.7	-0.2
Detector Coupling	70	-1.55	-1
TOTAL	0.02	-37.0	-22.1

Table 1: 16×16 crossbar losses

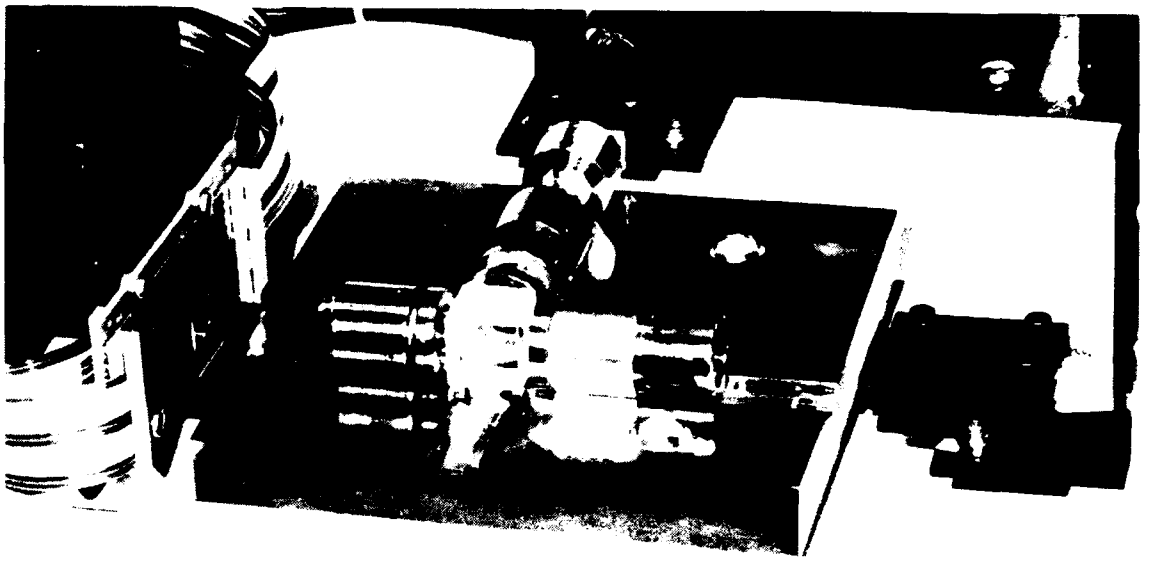

Figure 3: Hardware of the optical crossbar demonstrator

5. Conclusions

The construction of this 16×16 optical free-space crossbar switch has acted as a test bed for the components required for future systems. It has also demonstrated that such high bandwidth connections between large numbers of ports can be fabricated as compact and rugged systems. The OCPM consortium is currently involved in not only refining this system but also in the construction of a 64×64 crossbar switch based upon a similar design. This larger switch is to be constructively used as the communications mechanism between the high powered nodes of a parallel processing system with a data rate of 640MBits/s, a BER of 10^{-12} and a reconfiguration time of $<10\mu s$.

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An Efficient Implementation Methodology for 2-D Space-invariant Hypercube-based Free-space Optical Interconnection Networks

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Introduction

One of the most popular interconnection networks for parallel computers today is the binary n-cube, also called the hypercube, interconnection network. The attractiveness of the hypercube topology is its small diameter, simple and efficient message routing algorithms, strong connectivity, regularity, symmetry, and fault-tolerance. Unfortunately, conventional VLSI technology seems to be reaching its fundamental physical limits and is, therefore, unable to implement large-scale interconnection networks based on the hypercube topology (or any other topology for that matter) that provide high communication bandwidth, short latency, and reasonable power requirements[1].

Optics, owing to its inherent parallelism, high spectral and spatial bandwidth, and low signal crosstalk, possesses the potential for a permanent solution to the communication problem in parallel and distributed computing[2]. Several optical interconnection networks and techniques have been proposed and some of them demonstrated. However, the overall capability of these networks in terms of network size, speed, and cost does not yet present a major advantage over electronic ones because some of these network architectures are seriously failing to fully exploit optics' unique interconnect capabilities. Optics is inherently two dimensional (2-D), and an optical interconnect architecture which is designed to connect one-dimensional arrays of communicating nodes can evidently fail to exploit fully the parallelism available. A second design issue related to optical interconnects is the degree of *spatial invariance*: the degree of regularity of the connection patterns. While *space-variant* interconnects offer arbitrary connections, they require complex optical implementations, and are therefore less amenable to efficient optical implementations. On the other hand, *space-invariant* interconnects are highly desirable for optics because of their use of simple space-invariant optical elements. Such space-invariant networks would (1) better utilize the full space-bandwidth product of optical imaging systems, (2) take full advantage of the parallelism of free-space optics, and (3) would be better suited for the recent advances in compact, 2-D optical logic devices.

In this paper, we present a new methodology for embedding a hypercube into a 2-D plane. The proposed embedding scheme results in totally space-invariant connection patterns. The resulting layout is highly amenable to optical implementations. The optical hardware only needs to provide imaging and uniform spatial shifting without complicated dynamic beam-steering operations. In addition, such an embedding reduces greatly the space requirements on the 2-D plane as compared with previous embedding methods[3].

A New Design Methodology for Space-invariant 2-D Hypercube Networks

The optical implementation of the hypercube interconnects has been a driving force for several optics researchers. The most noticeable among the proposed schemes is the space-invariant scheme proposed by Sheng[3]. The embedding of nodes onto a plane is straightforward, meaning the address-node assignment is row-majoring indexing. In order to have totally space-invariant connections, empty rows and empty columns are inserted to mask off unwanted connections. Unfortunately, for hypercubes of higher dimensions, the number of empty rows and columns becomes very large. Consequently, Sheng's embedding scheme turns out to be very inefficient in terms of area utilization on the plane, and in terms of volume required by the free-space imaging optics.

The proposed embedding scheme, while realizing space-invariant implementation of the 2-D hypercube interconnection topology, greatly alleviates the space requirements. The basic idea is derived from an observation that a 4-cube can be embedded on a plane without empty rows or columns if Gray code is used for address-node assignment. Conceptual implementation of a 2-D 4-cube using a multiple imaging technique is shown in Fig. 1. A number in a node of the source plane represents the address of the node, and numbers in a node of the detector plane represent the addresses of nodes with which the given detector is supposed to be directly connected in the hypercube. For example, node 0 is connected to nodes 1,2,4, and 8. The dashed nodes on the detector plane represent falling-off images outside the detectors for the 4-cube implementation. The required connections for a 2-D 4-cube are then obtained by simultaneously superimposing 8 replicated and spatially shifted images of the source plane. The amount of shifts are $\pm 1d$ and $\pm 3d$ in both horizontal and vertical directions where d is the size of an input node and the origin is taken to be the center of the source plane.

The proposed embedding scheme can implement hypercubes with dimensions up to 4 using the space-invariant multiple imaging technique without inserting empty rows or columns. It should be noted that Sheng's scheme inserts 1 empty row and 1 empty column for 4-cube implementation. The proposed scheme inserts empty rows

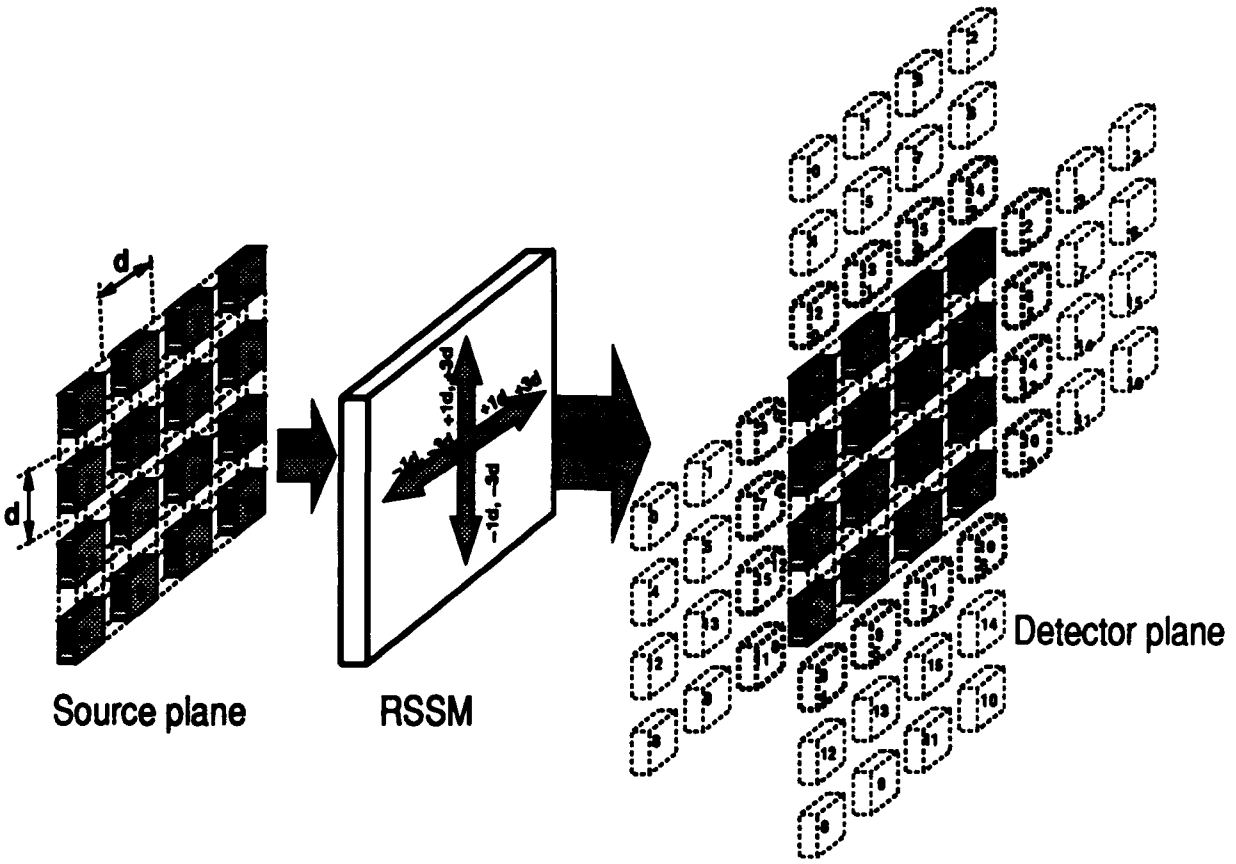

Figure 1: Conceptual optical implementation of a 4-cube: (Replication and Spatial Shift Module (RSSM) receives an image from the source array and generates 8 replicated images. These 8 images are spatially shifted horizontally and vertically as specified in the figure.)

or columns if the dimension of the hypercube becomes greater than 4. However, it requires approximately an order of magnitude less number of empty rows and columns than Sheng's scheme.

The construction of an arbitrary n-cube network is carried out incrementally by putting together a number of basic modules. Fig. 2 presents four types of basic modules corresponding to n-cube networks for $n = 1, \ldots, 4$. We denote by a *shift rule* the amount of spatial shift along the x-axis (left or right) and y-axis (upwards or downwards) required to achieve hypercube connections. Thus each shift rule contains two entities, *Row(n)* and *Col(n)*. For example, a shift rule such as *(Row(2)* $= \pm 1$, *Col(2)* $= \pm 1$*)* states that in order to implement a 2-cube network, the input plane is to be replicated into four images. Each replica is then shifted as follows. For a *Row(2)* $= +1$, the corresponding image is shifted upwards by an amount equal to the size of a single node on the plane along the y-axis. Similarly, a *Row(2)* $= -1$ indicates a shift by the size of one node downwards along the y-axis. A *Col(2)* $= +1$ means a shift to the right by one node, and *Col(2)* $= -1$ is a shift to the left by one node along the x-axis. There may be several shifts needed along a given direction, and that is indicated by a comma. For example, a shift rule such as *Row(4)* $= \pm 1, \pm 3$, *Col(4)* $= \pm 1, \pm 3$, would require eight images of the source plane. These images are then shifted according to the displacement indicated. The shifted images need to be simultaneously superimposed on the detector plane to achieve the required connections.

The basic modules of Fig. 2 are used to construct 2-D hypercubes with dimensions higher than four. To facilitate the description of the generalized embedding scheme, several functions are defined below:

$\mathcal{E}_r(n)$: the number of empty rows that are inserted between two layouts of $(n-1)$-cubes to construct an n-cube.
$\mathcal{E}_c(n)$: the number of empty columns that are inserted between two layouts of $(n-1)$-cubes to construct an n-cube.
$\mathcal{D}_r(n)$: the row dimension of the resulting 2-D n-cube.
$\mathcal{D}_c(n)$: the column dimension of the resulting 2-D n-cube.
$\mathcal{R}_r(n)$: the amount of upward rotation of an $(n-1)$-cube layout to construct an n-cube.

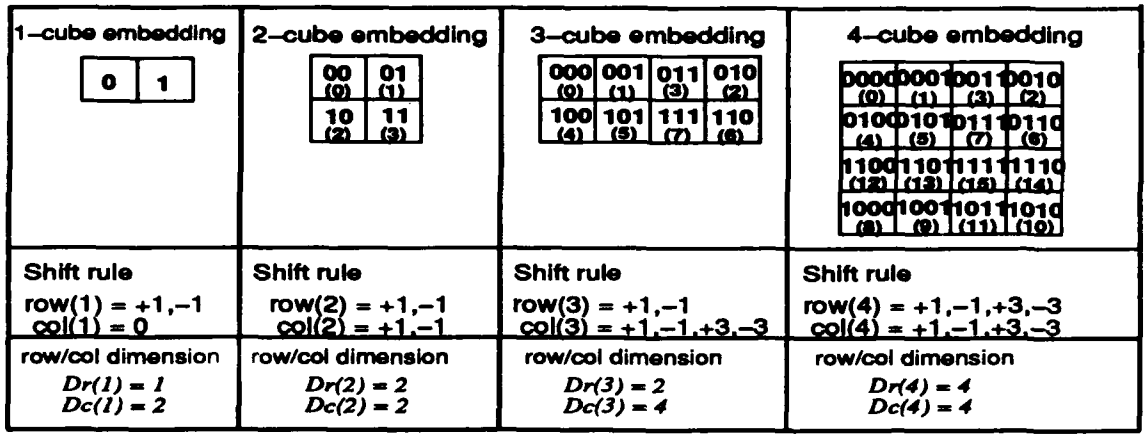

Figure 2: Embedding of hypercubes of dimensions 1 to 4 in a plane using the proposed scheme.

$\mathcal{R}_c(n)$: the amount of left rotation of an $(n-1)$-cube layout to construct an n-cube.
Row(n): the amount of shifts along x-axis for implementing an n-cube.
Col(n): the amount of shifts along y-axis for implementing an n-cube.

An Algorithm for Constructing a 2-D Space-Invariant n-cube from an $(n-1)$-cube

The following three-step algorithm constructs a 2-D space-invariant n-cube ($n > 4$) from a 2-D space-invariant $(n-1)$-cube network:

Step one: Given a 2-D space-invariant $(n-1)$-cube layout, and depending on whether n is odd or even, we rotate it to the left by $(\mathcal{R}_c(n) = 2^{[(n-1)/2-1]})$ columns if n is odd, or we rotate it upwards by $(\mathcal{R}_r(n) = 2^{[(n-2)/2-1]})$ rows if n is even. The rotated plane is then placed at the right side of the original $(n-1)$-cube layout if n is odd, or underneath it if n is even. During the rotation, no empty columns or rows that already exist in the $(n-1)$-cube layout are counted as the shift amount.

Step two: We insert between the two $(n-1)$-cube layouts, the original and the rotated one, $(\mathcal{E}_c(n) = 2^{[(n-1)/2-2]} + \sum_{i=1}^{[(n-1)/2-2]} \mathcal{E}_c(2i+3))$ empty columns if n is odd, or $(\mathcal{E}_r(n) = 2^{[(n-2)/2-2]} + \sum_{i=1}^{[(n-2)/2-2]} \mathcal{E}_r(2i+4))$ empty rows if n is even.

Step three: We prefix 0 as the most significant bit in all addresses of the original $(n-1)$-cube layout, and 1 as the most significant bit in all addresses of the rotated $(n-1)$-cube layout.

When n is odd, the resulting 2-D space-invariant n-cube has the same row dimension as that of the $(n-1)$-cube and its column dimension is 2× (column dimension of the $(n-1)$-cube) + (the number of empty columns inserted in step two). Thus, $\mathcal{D}_r(n) = \mathcal{D}_r(n-1)$ and $\mathcal{D}_c(n) = 2\mathcal{D}_c(n-1) + \mathcal{E}_c(n)$.

When n is even, the resulting n-cube has a total number of rows equal to 2× (row dimension of the $(n-1)$-cube) + (the number of empty rows inserted in step 2), and the same number of columns as that of the $(n-1)$-cube. Thus, $\mathcal{D}_r(n) = 2\mathcal{D}_r(n-1) + \mathcal{E}_r(n)$ and $\mathcal{D}_c(n) = \mathcal{D}_c(n-1)$.

If n is odd, the shift rule of the resulting n-cube is $(Row(n) = Row(n-1))$ and $(Col(n) = Col(n-1), \pm[\mathcal{D}_c(n) - \mathcal{D}_c(n-3)])$.

If n is even, the shift rule of the resulting n-cube is $(Row(n) = Row(n-1), \pm[\mathcal{D}_r(n) - \mathcal{D}_r(n-3)])$ and $(Col(n) = Col(n-1)))$.

Fig. 3 illustrates how the proposed scheme constructs a space-invariant 5-cube using two 4-cubes. A 4-cube embedding is shown in Fig. 3(a). It is rotated to left by 2 columns. The resulting plane is shown in Fig. 3(b). The rotated plane is then placed to the right of the original one as shown in Fig. 3(c). Next, 1 empty column are inserted. Finally, a 0 is prefixed as the most significant bit in every node address of the unrotated plane, and a 1 is prefixed as the most significant bit in every node address of the rotated plane. The resulting 2-D space-invariant 5-cube is shown in Fig 3(d). For the required hypercube connections, 10 replicated and spatially shifted images of the source plane are needed. The amount of shifts is $\pm 1d$ and $\pm 3d$ in row-wise direction, and $\pm 1d$, $\pm 3d$, and $\pm 7d$ in column-wise direction, where d is the size of a node.

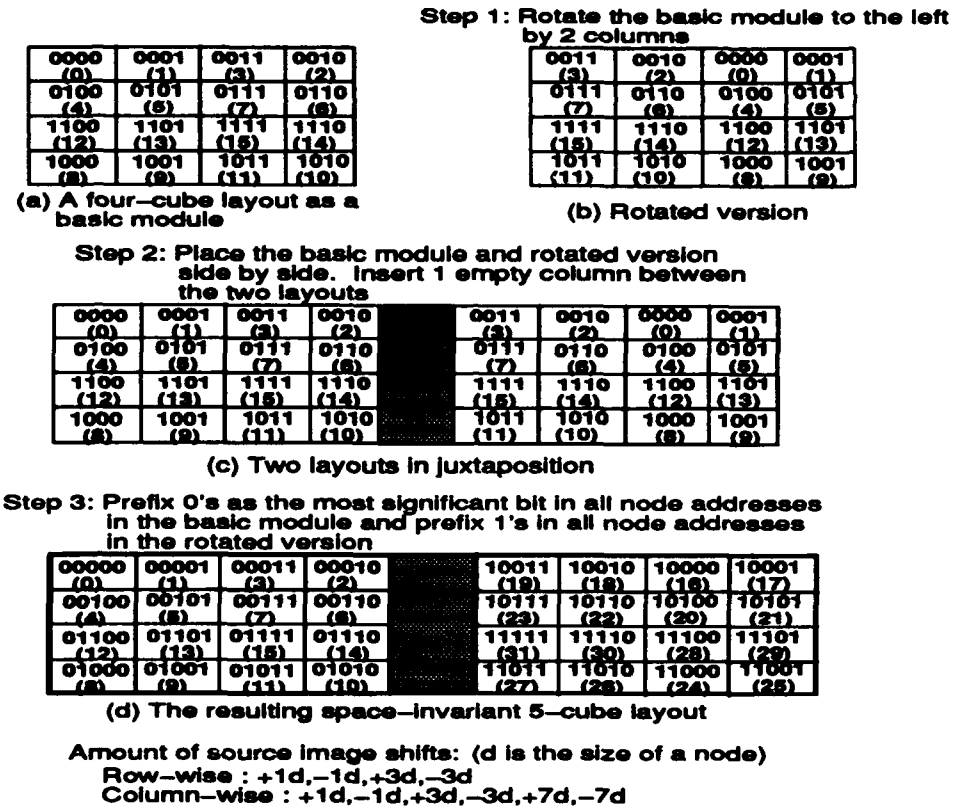

Figure 3: Construction of a 2-D space-invariant 5-cube from two 4-cubes.

It can be mathematically shown than the proposed scheme requires one order of magnitude less area than Sheng's scheme for hypercubes of dimensions equal to or greater than 3. In addition, for a given network size, the proposed scheme requires less amount of shifts to accomplish the desired connections. Since the volume is determined by the planar area and the maximum shift (the third dimension) required, the proposed scheme can implement the hypercube of a given size in a lesser volume. Thus, the proposed scheme is more amenable to optical implementations.

Concluding Remarks

In this paper, we introduced a new strategy for embedding a hypercube topology onto a plane for 2-D to 2-D interconnects. The proposed methodology results in totally space-invariant connection patterns for the hypercube when embedded into a plane. This not only simplifies the optical implementation of 2-D hypercube-based networks but also takes full advantage of the high space-bandwidth product of space-invariant optical elements. We can estimate the theoretical upper bound of the hypercube size that can be embedded into a given plane by calculating the smallest possible diffraction limited detector size. It can be shown that the hypercube of dimension 20 (about 1 million nodes) can be embedded by the proposed scheme using currently available space-invariant optical hardware such as lenses, prisms, mirrors, and holographic optical elements.

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The Role of Tunable-Transmitter Wavelength-Division-Multiplexing Star-Coupler Architecture in High-Performance Multigigabit Asynchronous-Transfer-Mode Switching.

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Many ongoing efforts to implement large-size, multi-gigabit ATM switches have been motivated by the fact that Asynchronous Transfer Mode (ATM) is becoming a standard for B-ISDN applications. The different approaches incorporate both electronic and photonic designs. We continue to investigate photonic designs in this area which are cost-effective compared to electronic designs and are feasible with present photonic technology. Our design goal is to implement a large ATM switch (in excess of 256 lines) with a data rate of 2.5 Gb/s per line. We concentrate on photonic implementations which use star-coupler based, WDM techniques. In this presentation we propose an architecture which, by incorporating the best features of some of the previous designs, offers the best possible switching performance in terms of delay-throughput characteristics but requires the smallest number of wavelengths and a simple control mechanism, independent of the switch size.

As described in [1] for the PAC configuration, a tunable-transmitter/fixed-receiver star-coupler based WDM approach offers the advantage of less stringent requirements in terms of tunability (i.e., there is no need to tune the lasers to a precise wavelength). The fixed-filter/direct-detection receiver can accommodate variations in laser wavelength due to either aging, temperature or current drifts. The technique, however, uses input queueing as the switch architecture. Input queueing has been shown [2] to offer poorer performance compared to output queueing.

An output queueing system has the best possible performance. A Growable Switch Architecture using output queueing was introduced in [3]. The architecture for an N:N switch is depicted in Fig. 1. It consists on a front-end N:M Photonic Cell Distribution Network and a column of m:n Electronic Output Packet Switch Modules. One important feature of this architecture is that the switch size N is independent of the output modlue size n. Therefore, the design can be extended to very large size N. However, as describe in [3], the star-coupler based WDM implementation of the cell distribution network requires a large number (M) of distinct wavelengths. This number grows proportionally with the switch size ($M = m \times \frac{N}{n}$). Furthermore, the architecture uses a tunable receiver approach, which requires precise tuning circuits.

The electronic approach introduced in [4] uses concentrators in order to grow modularly to a large switch from a small-size packet switch. Using concentrators, a 32:32 electronic switch module could be readily available (Fig. 2). However, larger electronic concentrators will faced the

present electronic bottlenecks, mainly: pin-out count, power consumption, and high-speed interconnects. We propose to implement the concentrator using a photonic technique. The concentrator approach is depicted in Fig. 3. It uses a 32:32 electronic output packet switch module. The photonic concentrator is depicted in Fig. 4. It uses a tunable-transmitter WDM technique. This is easier to implement as explained before compared to a tunable-receiver technique. Furthermore, the number of distinct wavelengths needed is 32, independent of the switch size N. The concentrator control function is simple; cells are accepted into the concentrator if they are destined to that output group (Fig. 3) and then served to the 32 outputs on a First-Come/First-Serve basis. The physical implementation employs cell buffering at the inputs lines but with scheduled cell transmissions to emulate an ideal N:32 FIFO operation and thus not to degrade the overall switch performance.

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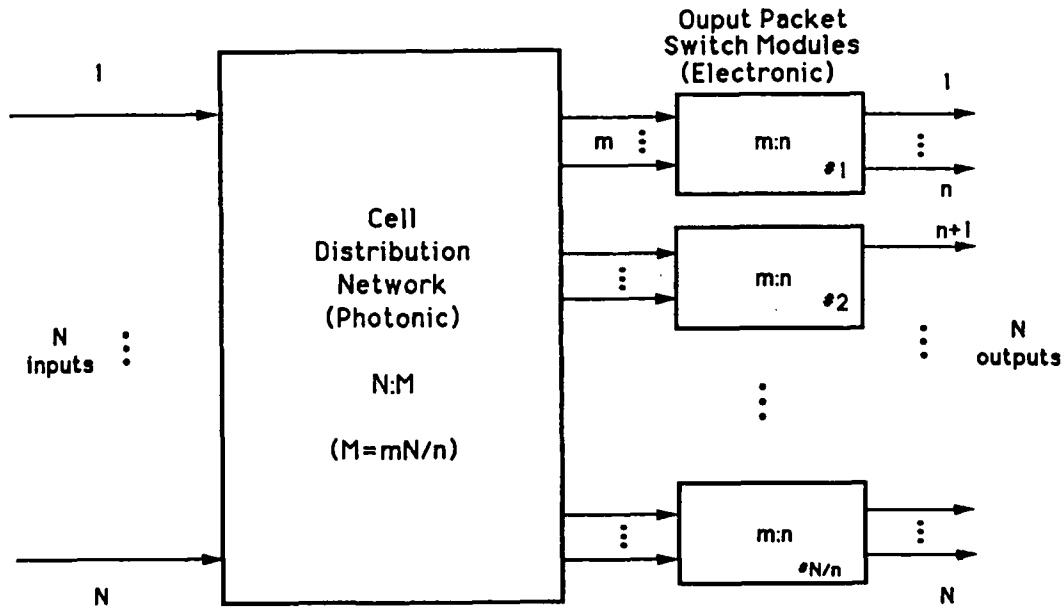

Figure 1: N:N Growable Packet Switch; Cell Distribution Network approach.

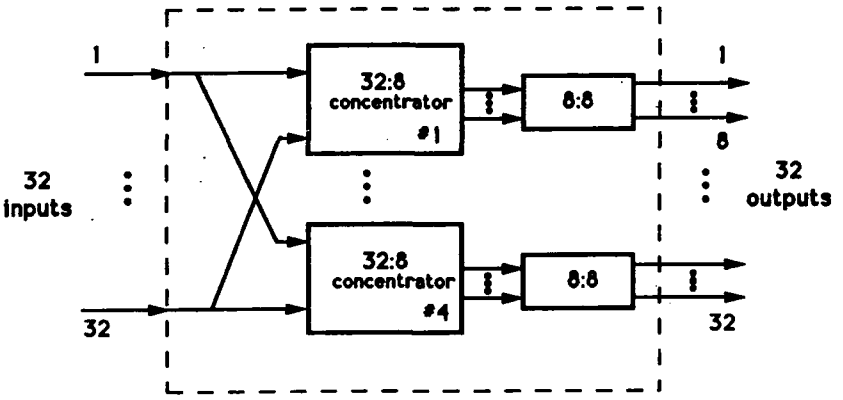

Figure 2: 32:32 electronic packet switch;concentrator approach.

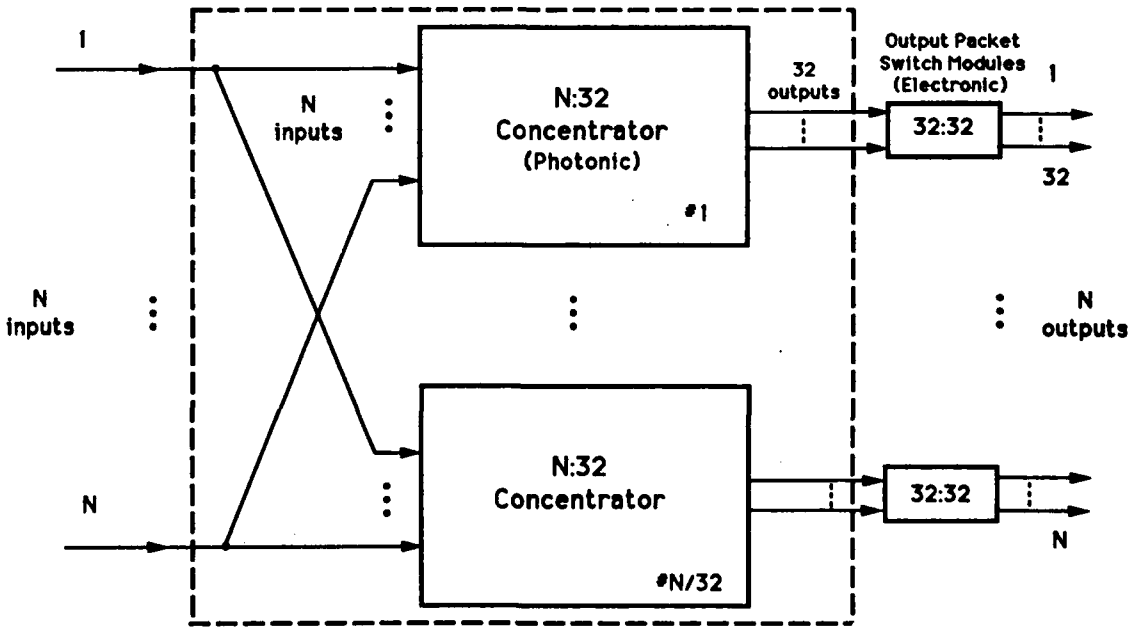

Figure 3: Growable Packet Switch Architecture; Concentrator approach.

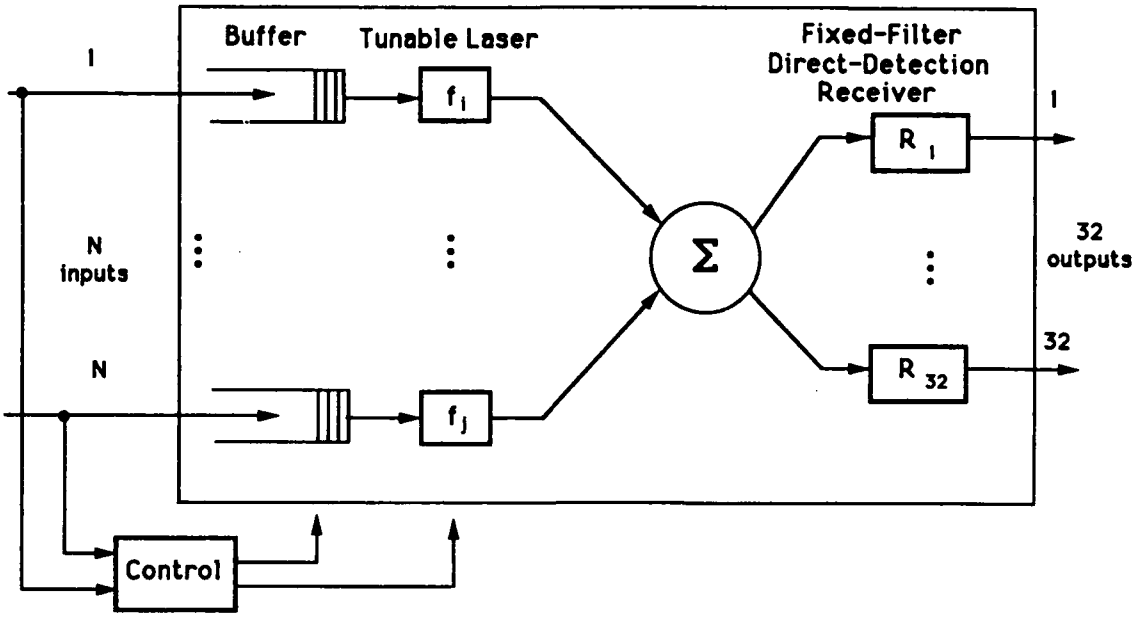

Figure 4: Tunable-transmitter WDM star-coupler based photonic concentrator.

A Time Domain Approach for Avoiding Crosstalk in MINs

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1. Introduction

Large photonic space switching networks can be built from 2×2 directional couplers (called *switches* hereafter) with Multistage Interconnection Network (MIN) architectures. These switches can cause problems such as crosstalk and optical path loss. Studies have shown that based on the current characteristics of these switches, crosstalk limits the size of a network more than path loss does [1,5].

Another factor that limits the size of a network is the hardware cost, which can be measured in terms of the number of switches used in the network. In this paper, we will focus on blocking MINs since they use fewer switches than nonblocking MINs of the same size. In addition, they have fewer stages, and thus shorter path delay and less path loss.

In blocking MINs, a permutation which cannot be realized due to switch setting conflicts can be *partitioned* into several subpermutations, such that each subpermutation can be realized at a time, or in one *pass*. The number of passes needed to realize the permutation is equal to the number of subpermutations resulted from the partition. To establish an arbitrary set of paths, we let a network go through a sequence of configurations such that a subset of paths is established in a configuration. A connection paradigm based on this idea, called *reconfiguration with time division multiplexing* (RTDM), was studied for multiprocessor communications in MINs and general optical interconnection networks [3,4]. In these studies, the topic of avoiding crosstalk has not been discussed.

First order crosstalk at switches can be avoided by ensuring that only one input of every switch is active at a time. To do so, one may take a space domain approach, called *network dilation* [2,6]. In this paper, a time domain approach for avoiding crosstalk without dilating networks is proposed. The approach is a simple application of the RTDM paradigm. The basic idea is that crosstalk can be avoided in a similar way switch setting conflicts are avoided when establishing a set of paths. More specifically, given a permutation P, P is partitioned into subsets such that paths in each subset can be established without crosstalk. Such a partition can be done, for example, by grouping paths in P that do not share switches with each other into the same subset. The time domain approach can also taken to avoid crosstalk when establishing an arbitrary set of paths in an undilated network.

The number of switches used in an undilated network is less than half of the number of switches used in a dilated network of the same size. On the other hand, using the time domain approach, the number of passes needed is usually more than what is needed using the space domain approach. In order to examine the tradeoffs between *Space* (in terms of the number of switches used) and *Time* (in terms of the number of passes needed), we define a cost function *coST* to be the product of these two numbers. We will study some properties of the time domain approach concerning the capability of realizing permutations and establishing arbitrary sets of paths in MINs. We will show that the proposed time domain approach, when compared to the space domain approach, results in nontrivial Space-Time tradeoffs and is advantageous in terms of the *coST* measure.

2. Realizing Permutations with the Time Domain Approach

We first discuss some properties of the time domain approach concerning the capability of realizing permutations. In an $N \times N$ network, at most $N/2$ paths can be established in one pass without crosstalk. Thus, using the time domain approach, at least two passed are needed to realize a permutation.

A blocking MIN with the topology of generalized cube (GC) networks is assumed. Figure 1 shows an 8×8 such network. The topology is chosen because large networks can be constructed recursively from smaller ones. It is worth noting, however, that the GC network is topologically equivalent to many blocking MINs such the Omega network [7]. For instance, the network in Figure 1 becomes an 8×8

Omega network after the positions of the two middle switches at the middle stage are interchanged.

Let Ω be the set of permutations realizable in an Omega network. It was shown that the set of permutations realizable in a dilated Omega network is equal to Ω [2]. Similarly, we can show that the set of permutations realizable in a dilated GC network is equal to Ω.

We are interested in the set of permutations realizable in two passes in an undilated GC network without crosstalk. Denote such set by Π. The following theorems state the relationship between the two sets Ω and Π.

Theorem 1. Not every permutation in Ω is in Π when $N \geq 8$.

We sketch the proof of the theorem by showing an example. Five paths, numbered from 1 to 5, are drawn in bold lines in Figure 1 as a part of a permutation in Ω in an 8×8 network. Figure 2 shows a graph in which a node corresponds to a path in Figure 1. There is an edge between two nodes if the two corresponding paths share a switch in the network. Accordingly, two paths corresponding to two adjacent nodes cannot be established in the same pass without crosstalk. Since the graph in Figure 2 is a ring of 5 nodes, it is impossible to establish the 5 corresponding paths in Figure 1 in just two passes without crosstalk. This proves that the example permutation is not in Π for $N = 8$. For $N > 8$, a permutation in Ω which includes the above 5 paths can be constructed. It can be shown similarly that this permutation is not in Π and therefore the theorem is proved. □

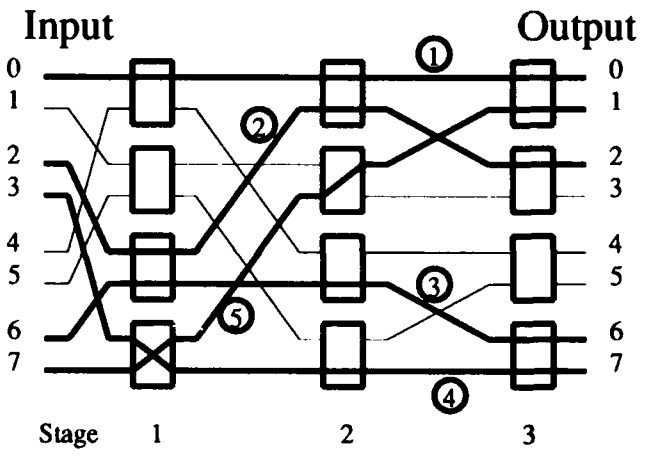


Figure 1

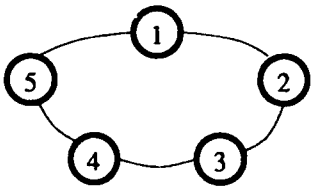


Figure 2

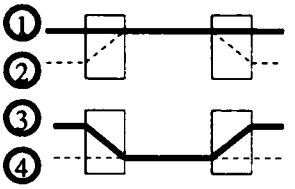


Figure 3

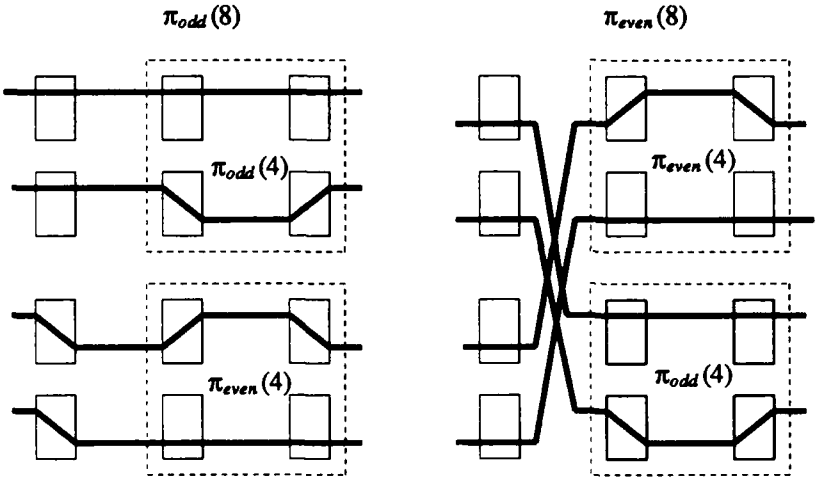
Theorem 2. Not every permutation in Π is in Ω.

We sketch the proof of the theorem by first showing an example. Figure 3 shows a 4×4 network and a permutation which is not in Ω due to switch setting conflicts. However, since paths 1 and 3 can be established in one pass and paths 2 and 4 can be established in another pass, the permutation is in Π.

It is easy to see that for $N > 4$, any permutation that includes the above 4 paths is not in Ω. The question is whether such a permutation can be constructed so that it is in Π. Let the inputs of an $N \times N$ network be numbered from 1 through N. Denote the set of paths originated from the odd and even numbered inputs by $\pi_{odd}(N)$ and $\pi_{even}(N)$, respectively. Figure 4(a) and 4(b) shows how $\pi_{odd}(8)$ and $\pi_{even}(8)$, respectively, can be constructed from $\pi_{odd}(4)$ and $\pi_{even}(4)$. It can be seen that the union of $\pi_{odd}(8)$ and $\pi_{even}(8)$ is a permutation in Π, but not in Ω. Similarly, a permutation in Π, but not in Ω can be constructed recursively for any $N > 8$. (the proof is omitted) □

Having found from the above two theorems that set Π and set Ω are not the same, we also observe that they have a common subset of permutations, as stated in the following theorem.

Theorem 3. Some permutations in Ω are also in Π (or vice versa).



4(a) 4(b)

Figure 4

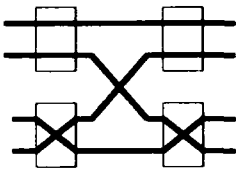


Figure 5

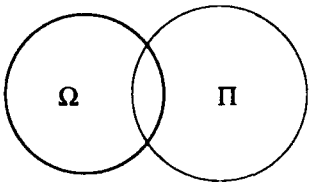


Figure 6

The proof of Theorem 3 is omitted. Instead, let us examine an example shown in Figure 5. Note that the permutation in this figure is in Ω, while the permutation in Figure 3 is not. It is easy to see that the permutation in Figure 5 is also in Π. Therefore, the theorem holds for a network with $N = 4$. For networks with $N > 4$, a permutation that is in both Ω and Π can be constructed recursively by following steps similar to the one shown in Figure 4. □

The relationship between the Ω set and the Π set is summarized in Figure 6. Unfortunately, neither the number of permutations in the Π set nor the number of permutations which are common in both sets is known at the moment.

3. Establishing Arbitrary Paths with the Time Domain Approach

We now consider applications that require the establishment of an arbitrary set of paths, which is not limited to permutations. One of the applications is to use a MIN as a centralized switching hub in which all possible paths between inputs and outputs need to be established. In [6], a *Dilated Slipped Banyan* (DSB) architecture was proposed. In a DSB network, N different permutations are realized, one in each pass. Every input is connected to a different output each time a different permutation is realized, and a completely-connected network is emulated within N passes. Crosstalk is avoided in the DSB through dilation. This method of emulating a completely-connected network can be used in dilated GC networks as well.

From the discussions in the previous section, it is not clear that an undilated GC network can emulate a completely-connected network within just $2N$ passes. However, the following theorem guarantees that $2N$ passes are enough.

Theorem 4. *An* $N \times N$ completely-connected network can be emulated in $2N$ passes without crosstalk using the time domain approach.

The theorem can be proved by induction. The proof is similar to those of Theorem 2 and Theorem 3 and thus is omitted.

In order to evaluate the space-time tradeoffs for applications that do not require all possible connections, simulation studies have been carried out. A set of random connection requests is generated from all possible N^2 connection requests. The number of passes needed for a dilated network as well as an undilated network (without crosstalk) is obtained. Figure 7(a) shows the number of passes as a function of the number of requests when $N = 32$. From Figure 7(a), it is clear that the number of passes needed in the undilated network is only about 1.5 times as many as that needed in the dilated network. This is also true in networks of other sizes according to our simulations. The above results indicate that, although the

domain approach will need at least twice as many passes as needed by the space domain approach when establishing a permutation, it is not the case when establishing an arbitrary set of paths. Intuitively, this is because the set of random requests may contain requests from identical inputs. In an undilated network, two paths from the same input may be realized without crosstalk in two passes. In a dilated network, two passes are still needed to avoid crosstalk when establishing these two paths.

Since the number of switches used in an undilated network is less than half of that used in a dilated network, the time domain approach will result in a smaller value of *coST*, (defined earlier to be the product of the number of switches and the number of passes), than the space domain approach. Figure 7(b) illustrates the *coST* values of the two approaches for different network sizes, with the *coST* value of the time domain approach normalized to 1. It can be seen from Figure 7(b) that the time domain approach improves the *coST* over the space domain approach by about 30% percent. In addition to that, we note that the time domain approach reduces path delay and optical path loss by using undilated networks. It is therefore an viable alternative to network dilation for avoiding crosstalk. We also note that the time domain approach is more flexible since the network can be used for applications with or without crosstalk budget problems. It can be combined with the space domain approach to avoid crosstalk in dilated networks in the presence of switch or link failures.

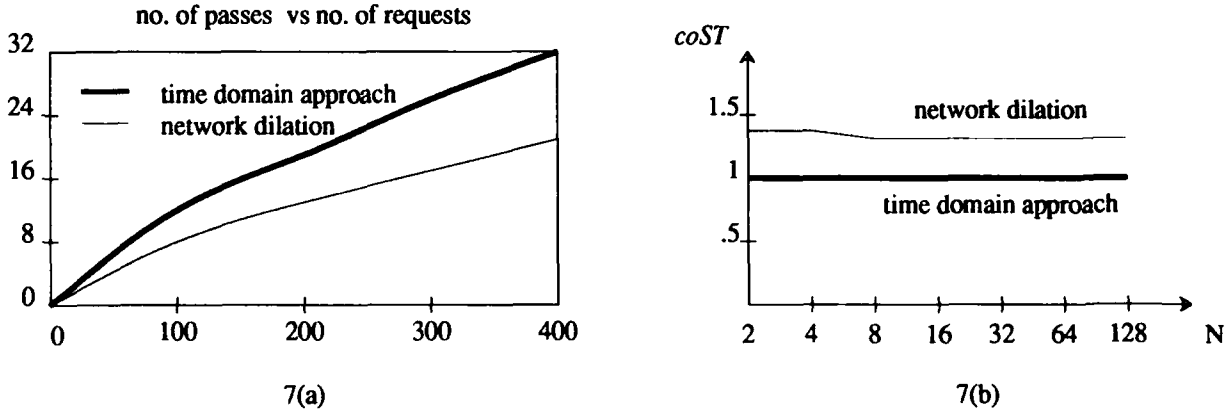


Figure 7

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Optoelectronic Logic Arrays Using the Light Amplifying Optical Switch (LAOS)

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Introduction

The massive parallelism and interconnectivity possible with optoelectronic systems requires the development of fast optoelectronic array processors. The arrays must be fast, with frame rates greater than 20 MHz, in order to effectively compete with electronics. The arrays must also have a large number of pixels ($>10^4$) and perform a logic or memory function. We have designed, fabricated and are in the process of testing an array that can meet these system requirements. This paper discusses our array design and presents some preliminary data.

Each pixel of the array is based upon a detector-emitter type of device which we call the light amplifying optical switch (LAOS)[1]. Previously, we have shown that this device can be used as an optical inverter [2], NOR [3], AND [4], and NAND [5] gate. The LED outputs of these gates have a high contrast ratio (6 to 50, depending on the type of gate) and have relatively fast response times considering that they were fabricated from square mesas, either 380μm or 260μm on a side.

Design and Fabrication

Figure 1 is a photograph of part of a 8x8 array of optoelectronic 2 input NOR gates fabricated with a four mesa pixel. One mesa of this pixel is a LAOS device, two mesas are heterojunction phototransistors and the fourth mesa is simply substrate area for a Cr-Ni thin film load resistor. Figure 2 shows the equivalent circuit for this pixel and Fig. 3 gives the topological layout details of the pixel. Note that each of the mesas has two side tabs which are used to electrically contact the power supply and ground buses and the intra pixel connections. This tab design leaves the main mesa area open for input and output windows and also allows the functionality of the pixel to be changed by only changing the metallization mask.

The NOR gate array was fabricated from layers of InGaAs and InP grown by gas-source molecular beam epitaxy using a layer structure similar to that use for the discrete NOR gate [3]. The mesas were wet chemically etched and were 75μm on a side. Polyimide was used to planarize the etched wafer, to form an insulating layer for the metal interconnects and to passivate the mesa sidewalls. The load resistors were formed by electron beam depositing a 300Å layer of 20/80 Cr-Ni alloy. For the present geometry, this gave a resistance value of $\approx$1300Ω.

Experimental Results

To date, a 16x16 array has been fabricated and preliminary tests on the individual devices and pixels have been performed. Figure 4 illustrates the transient response of one of the HPTs in

the array and the setup used for the measurement. The external 2N3565 transistor/1kΩ resistor formed a 10 ma current source which eliminated most of the problems associated with measuring the rise and fall time of the HPT. And while the noise on the HPT output signal prevents an accurate determination, the rise and fall times are estimated to be about equal and have a value of ≈25nS. Thus, operation up to 20 MHz is possible with the present geometry. Decreasing the mesa size to 20 μm should increase the cut off frequency to >100MHz.

The light output of the pixels has also been investigated. Unfortunately, for the array shown in Fig. 1, it has been found that a small misalignment of the metallization mask has caused many of LED's to be shorted and therefore full functional testing of this 16x16 array is not possible. However, the output of a 2x2 array using larger mesas is shown in Fig. 5. Uniform light output over the entire mesa area is observed, except in the metal contact areas. To focus this LED output we have formed photoresist microlenses on the top of the output mesas as shown in Fig. 6 (the lens have been deliberately misaligned in order to show the mesa underneath). The micro lenses have a measured focal length of 300 to 400μm and are non-absorbing in the wavelength range to be used for the arrays.

In summary, the array fabrication and testing has shown that the design and fabrication concepts are suitable for fast array processors, but that more care must be exercised in processing in order to produce a working array. We are presently processing new wafers in order to demonstrate a fully functional array. We will use these to measure the chip power, maximum frame rate and cascadability of this type of array processor. This data will be presented in this paper along with more details of the array design and analysis.

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Acknowledgements

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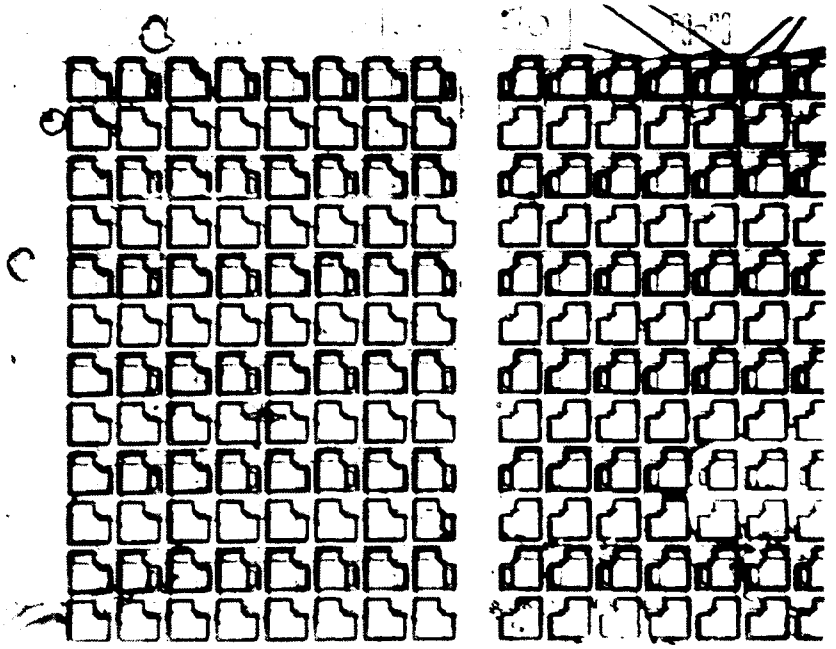

Fig. 1. Photograph of a section of the 8x8 optical NOR gate array.

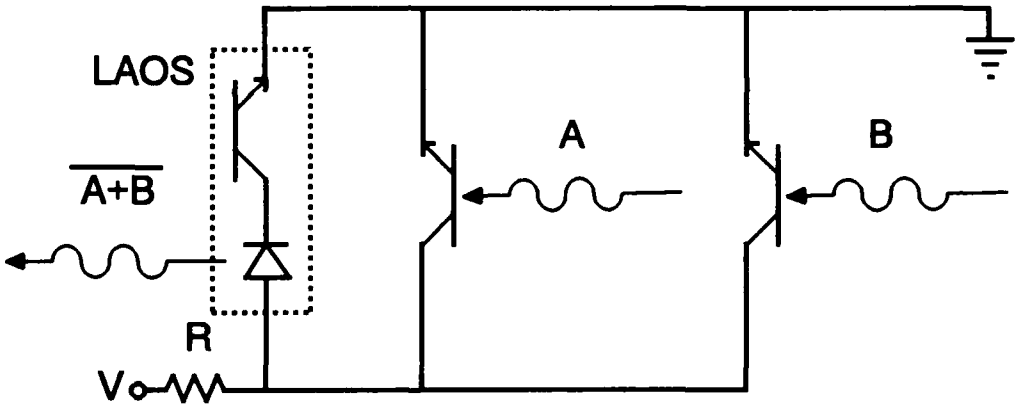

Fig. 2. Equivalent circuit diagram of one pixel of the optical NOR gate array.

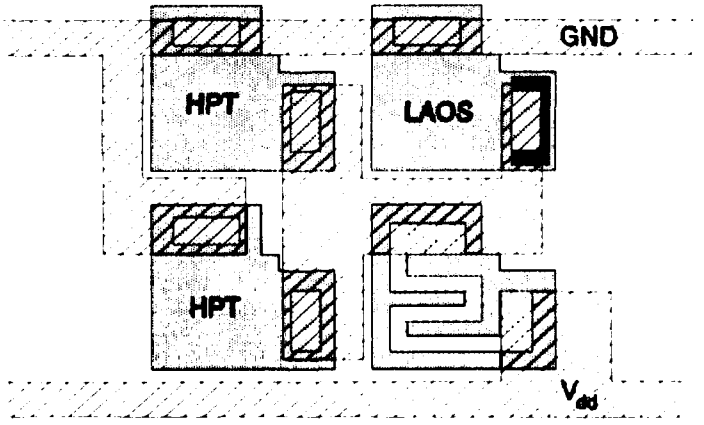

Fig. 3. Schematic diagram of one pixel of the optical NOR gate array.

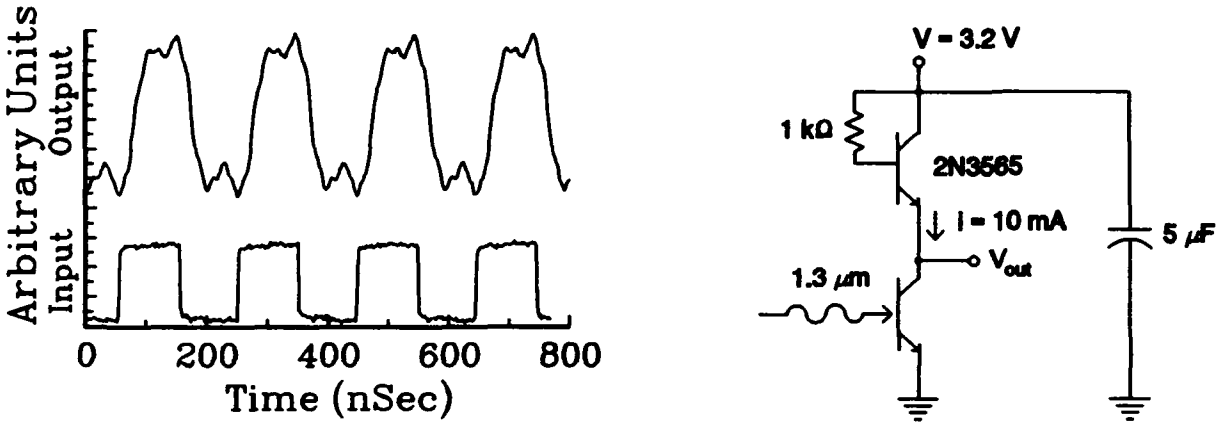

Fig. 4. Timing diagram and test circuit of integrated phototransistor.

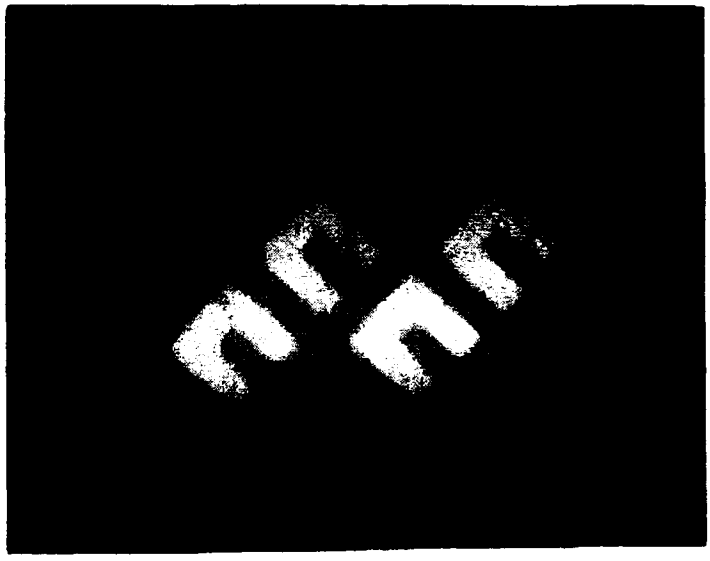

Fig. 5. Vidicon image of the infrared emission of a 2x2 LAOS device array.

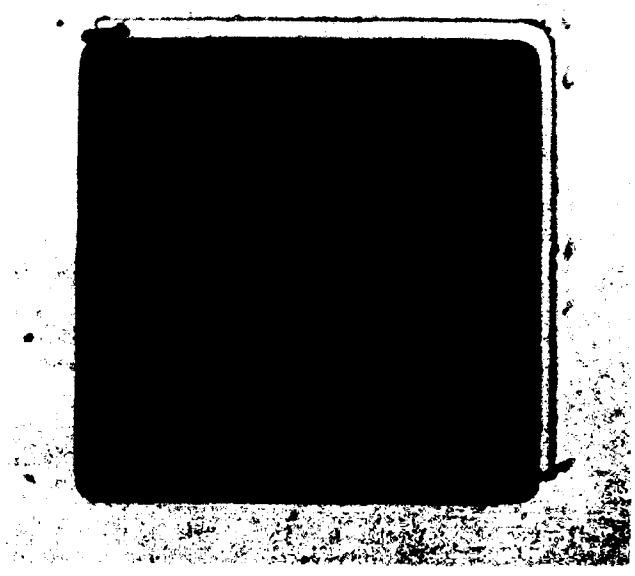

Fig. 6. Photograph of a microlens integrated over a mesa.

Complete All Optical Switching of Visible Picosecond Pulses in Birefringent Fiber

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Numerous approaches have been recently pursued in all optical switching in fiber devices.[1-4] A number of these efforts have demonstrated the principle of switching based upon cross-phase modulation (XPM) by a control pulse, but have failed to achieve high switching contrast ratios.[1-2] For anomalous dispersion, switching of soliton like pulses based upon XPM by a second wavelength has been accomplished.[2] Uniform XPM and high contrast switching of visible signal pulses was achieved using a long duration control pulse of a different color so that the control walks through the signal owing to group velocity dispersion.[4] In this paper the need for a second source is eliminated by using cross-phase modulation from a short, orthogonally polarized control pulse of the same frequency, in a birefringent fiber. It is found that 50:1 switching contrast is obtained and that the effects of broadening of the control pulse are significant and must be considered.

The arrangement used in this experiment is that of time division interferometry.[1] A synchronously pumped dye laser supplies 600nm, 2 ps pulses. After splitting off parts of the beam for use as a pump pulse and a probe, the remainder is directed into a simple Michelson interferometer which produces a signal and reference pulse of equal intensity and a selected (large) relative time delay. This pulse pair is focused into one polarization mode of a 10 m fiber of high birefringence (polarization dispersion of 1.6 ps/m), and the control (pump) pulse is directed into the orthogonal mode. The relative timing of the signal and pump pulses are adjusted so that the pump pulse walks through the signal during propagation (owing to the group velocity difference between

the fiber modes), such that the signal receives uniform XPM over its duration. The reference pulse, which has the same polarization as the signal, is delayed by a large duration so that it does not receive any XPM from the pump. During propagation the signal pulse undergoes XPM by the pump, while the reference serves to track mechanical variations in the linear phase of propagation through the fiber. At the fiber output the pump pulse is stripped by a polarizer and the signal and reference pulses are combined in a Michelson interferometer which compensates for their input delay and may be used to set their relative phase. The output of the interferometer thus contains three pulses: the desired interference between the reference and signal pulse, and a single pulse both before and after it separated by the reference delay (set much longer than the pulse width). A cross correlator using a compressed probe pulse (0.3 ps) is used to examine the intensity of only the interfered pulse.

With the pump absent the phase of the interferometer is adjusted for constructive interference (phase = 0), and the transmitted intensity, modulated owing to XPM by the pump, is measured. In Fig. 1, with the pump pulse energy of 120 pJ set to impart a π phase shift on the signal, the delay of the pump pulse with respect to the signal is varied. The maximum transmitted intensity observed in Fig. 1 is the same as that found with the pump absent (representing 0 phase), and thus for these delays there is negligible XPM of the signal pulse. For a window of $\sim$ 10 ps there is large extinction of the interfered pulse, with a maximum observed contrast ratio of $\sim$ 50:1. The duration of this window (which represents the duration over which XPM of π radians occurs) is set by a combination of the group velocity walkoff (1.6 ps/m $\times$ 10 m = 16 ps) and broadening of the pump and signal pulses during propagation. For the pump power used in Fig. 1 the pump broadens to 8.5 ps and the signal pulse (which has 5 pJ of energy) broadens to 4 ps. The center of the time window corresponds to the pump entering the fiber 8 ps after the signal and exiting 8 ps before it. As one goes away from the center of the time window the pump starts to overlap the signal either at the en-

trance or exit of the fiber, and thus leads to incomplete XPM of the signal pulse which reduces the contrast ratio. In general, by increasing (decreasing) the fiber length or birefringence one increases (decreases) the duration of the XPM time window, however, one must also consider the effects of the broadening of the pump pulse.

In Fig. 2, the pump delay is set for maximum extinction (t = 8 ps in Fig. 1) and the transmitted intensity is shown as the pump pulse energy is varied. The first minimum corresponds to π phase shift and the condition under which the data of Fig. 1 was taken. The succeeding extrema correspond to integer multiples of π phase shifts. The decrease in contrast ratio at higher powers is a result of the excessive pump pulse broadening from self-phase modulation. The pump, therefore, does not completely walk through the signal pulse, and incomplete XPM of the signal pulse then results in a loss of contrast. However, by using a sufficiently birefringent or long fiber, and thereby increasing the walkoff of the two polarization modes, one could insure complete XPM at higher powers.

Although the dual Michelson arrangement of the time division interferometry used here is cumbersome, an analogous all-fiber loop interferometer[2,3] could be used in an similar fashion and eliminate the need for both Michelsons and the time gating of the output.

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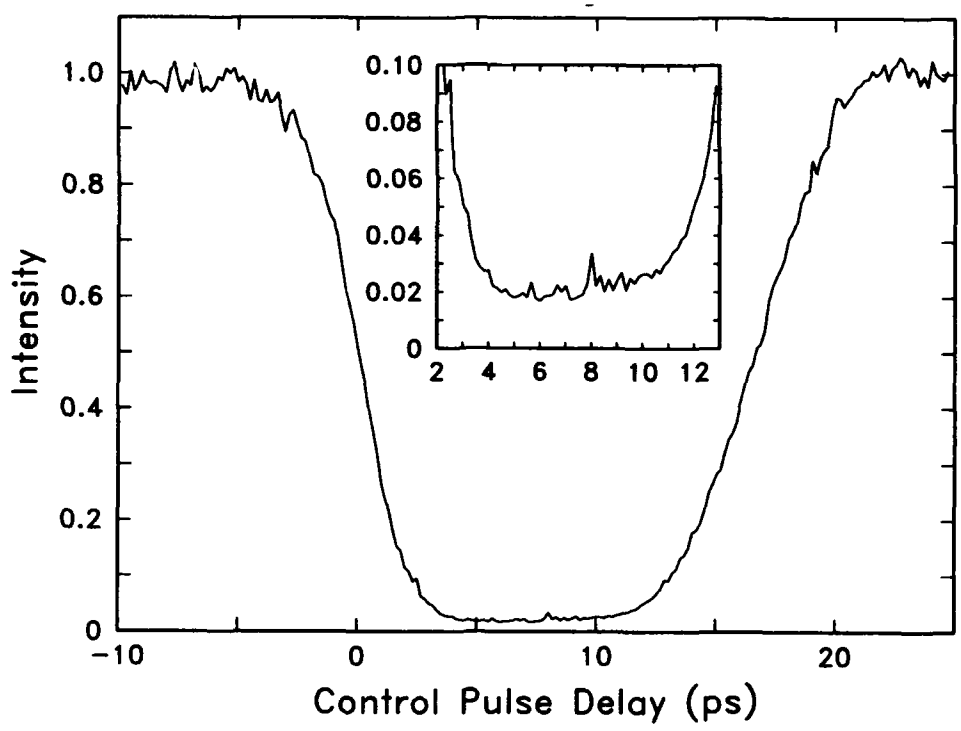

Figure 1: Transmitted intensity through the time division interferometer versus delay of 120 pJ control (pump) pulse.

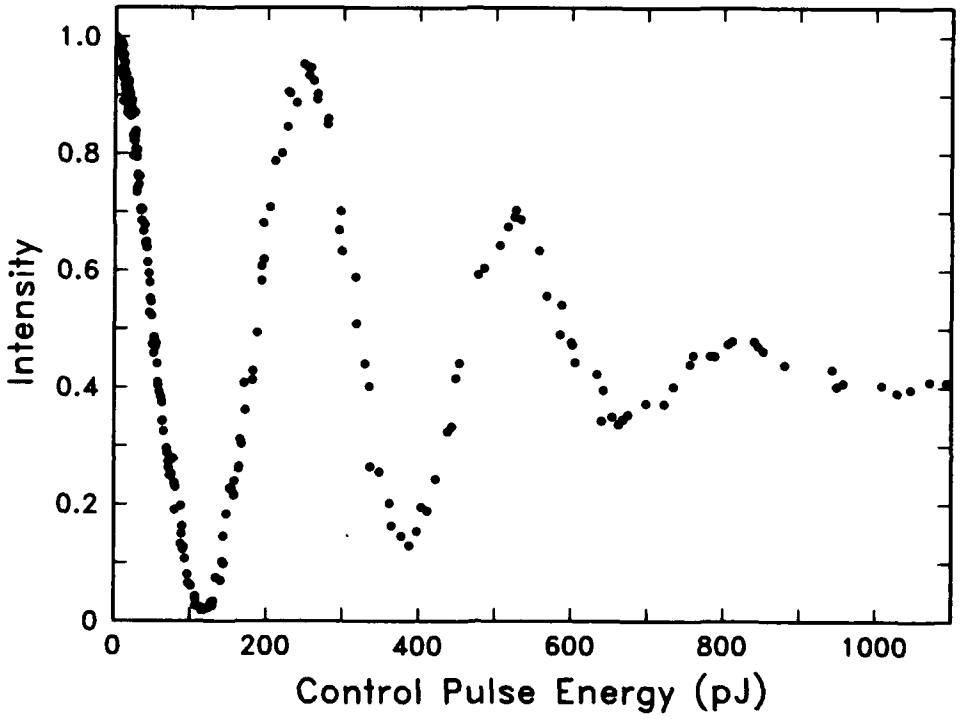

Figure 2: Transmitted interferometer intensity versus pump pulse energy at fixed delay corresponding to t = 8 ps in Fig. 1.

Electrically Actuated Nanomechanical Integrated Optical Switches

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We report on modulation, directional switching, and deflection of guided waves actuated by nanomechanically induced effective-refractive-index changes ΔN. The integrated optical (IO) devices are actuated electrically. No electrooptic materials are required; glass waveguides on silicon are used.

The IO nanomechanical effect

The IO nanomechanical effect works as follows: the width d of the small air gap (with $d \leq \lambda$, where λ is the wavelength) between a nonabsorbing dielectric plate, called "effective-refractive-index-shifting element" E, and a section of the planar or strip waveguide is varied. The evanescent field of the guided wave penetrates through the air gap into E. Therefore, the effective refractive index N depends on d. For suitably designed waveguides, gap-width variations Δd of only a few nanometers induce the ΔN changes required for IO device operation.[1,2] With an element E in the form of a bridge spanned over the waveguide (see Fig. 1), the gap-width variations Δd are realized by an elastic deflection of the bridge under electrostatic forces.

Fabrication of the waveguides and of the effective-refractive-index-shifting elements

For our experiments at the He-Ne-laser wavelength $\lambda = 633$ nm, we used planar SiO_2-TiO_2 waveguides on Si/SiO_2 substrates, i.e., on silicon wafers with thermally grown 3.5-µm-thick SiO_2 buffer layers. The waveguiding SiO_2-TiO_2 films F with refractive indices of $n_F \approx 1.88$ and thicknesses d_F of typically $d_F \approx 130$ - 200 nm were fabricated by dipcoating with the sol-gel process from Liquicoat® solutions (Merck, Darmstadt); firing temperatures of about 900° C were used. In the experiments, laser light was endfire-coupled into (and out of) the thin monomode waveguides. Waveguide endfaces of good optical quality were obtained by scribing and cleaving along the (100) crystal plane of the silicon.

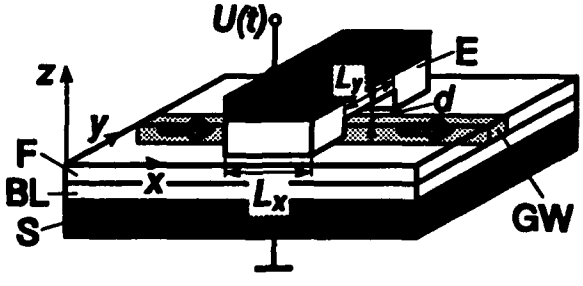

Fig. 1. Effective-refractive-index-shifting element E in the form of a bridge over a planar waveguide, both fabricated in silicon technology.
F, planar waveguiding film; BL, about 3.5-µm-thick oxidized SiO_2 buffer layer on silicon wafer S (substrate); E, oxidized silicon wafer (Si/SiO_2); GW, guided wave. L_x, width; L_y, length of bridge; d, width of (air) gap between element E and waveguide. $U(t)$, voltage between the upper part (Si) of element E and the waveguide substrate (Si).

The effective-refractive-index-shifting elements E were made of Si/SiO_2 platelets cut from oxidized silicon wafers (of thickness 500 μm) identical with the waveguide substrates. The evanescent field of the guided wave penetrates only into the nonabsorbing SiO_2 layer of refractive index $n_E \approx 1.46$, not into the silicon. The air gap was realized by chemically etching a channel into the SiO_2 layer; typically the channel was $\hat{d}_0 \approx 200$ nm deep, $L_x = 4$ mm long in the x direction, and $L_y = 4$ mm wide in the y direction. These bridges were optical-contact bonded to the planar waveguide. This bonding is useful in feasibility studies; the contact bond is quite stable, however reversible, i.e., the element E can be detached (by immersion in water) and after cleaning, bonded again.

Electrical actuation

The IO nanomechanical devices are actuated electrically. A voltage $U(t) = U_0 + \Delta U(t)$ is applied to the condenser formed by the upper conducting silicon part of the bridge and the waveguide substrate (Si). The resulting electrostatic pressure is $p(t) \propto [U(t)]^2 \approx U_0^2 + 2U_0\Delta U(t)$. The gap width is reduced from its initial value $\hat{d}_0$ to

$$d(t) = d_0 + \Delta d(t) \quad , \tag{1}$$

where d_0 is the median gap width which is adjusted with the d.c. voltage U_0. The gap-width variations

$$\Delta d(t) = C_p \Delta p(t) \propto C_p U_0 \, \Delta U(t) \quad , \tag{2}$$

where C_p is the frequency-dependent compliance of the bridge, are linearly proportional to the a.c. voltage $\Delta U(t)$.

Modulation and directional switching

Small gap-width variations Δd induce the effective-refractive-index changes

$$\Delta N = (\partial N/\partial d)\Delta d \quad . \tag{3}$$

The phase shift of a guided mode induced by an element E of length L_x is

$$\Delta\Phi = 2\pi(L_x/\lambda)\Delta N = 2\pi(L_x/\lambda)(\partial N/\partial d)\Delta d \quad ; \tag{4}$$

it is approximately linearly proportional to Δd.

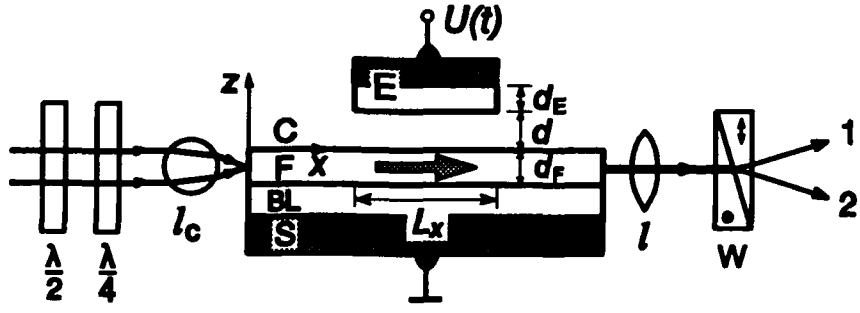

Fig. 2. Schematic of the polarimetric interferometer used as an intensity modulator or as a directional switch.
F, planar waveguiding film; BL, SiO_2 buffer layer on silicon wafer S (substrate); E, effective-refractive-index-shifting element of length L_x; C, medium (air) in gap; d, gap width; l_c, cylindrical incoupling lens; l, cylindrical or spherical outcoupling lens; W, Wollaston prism (oriented at 45°); 1 and 2, output ports; λ/2, λ/4, half- and quarter-wave plates for adjusting the point of operation of the modulator; $U(t)$, voltage.

In a Mach-Zehnder interferometer - with an element E in one leg - the phase modulation $\Delta\Phi$ can be transformed into an intensity modulation. A phase shift of $\Delta\Phi = \pi$ effects a directional switching of the output from one to the other output port of the interferometer. However, we used a polarimetric interferometer shown in Fig. 2 because it can be built without any microstructuring; only a planar waveguide is required. Incident linearly polarized laser light excites the TE_0 and TM_0 modes. Element E induces a phase difference between them:

$$\Delta\tilde{\Phi} \equiv \Delta\Phi_{TE_0} - \Delta\Phi_{TM_0} = 2\pi(L_x/\lambda)(\Delta N_{TE_0} - \Delta N_{TM_0}) = 2\pi(L_x/\lambda)[(\partial N_{TE_0}/\partial d) - (\partial N_{TM_0}/\partial d)]\Delta d \ . \qquad (5)$$

The output powers at ports 1 and 2 are proportional to $\{1 \pm \cos[\Delta\tilde{\Phi}(t) + \Delta\tilde{\Phi}_0]\}$, where $\Delta\tilde{\Phi}_0$ is an adjustable constant phase difference. If the latter is chosen to be $\Delta\tilde{\Phi}_0 = 0$, an induced phase shift of $\Delta\tilde{\Phi} = \pi$ switches the output signal from one to the other output port.

Some experimental results are shown in Fig. 3. We observed intensity modulation at frequencies up to $f = 1$ MHz. The temporal response of the IO nanomechanical device is determined by the dynamics of the mechanical system (bridge) with time constants of the order of microseconds and the time constant $\tau \equiv RC$ for charging and discharging the condenser C via a resistor R which can be made as short as a few nanoseconds; however, in the experiments reported here, we had $\tau \approx 10$ µs due to a high contact resistance R.

We expect that by a reduction of the thickness D of the bridge (from presently $D \approx 500$ µm) by one order of magnitude, the compliance C_p, which is proportional to $(L_y/D)^3$, can be increased by three orders, however at the expense of a tenfold increased response time. According to eq. (2), driving voltages U_0 and ΔU required to obtain the same gap-width variations Δd and thus the same phase shifts $\Delta\tilde{\Phi}$ can thus be reduced by 1.5 orders of magnitude.[3]

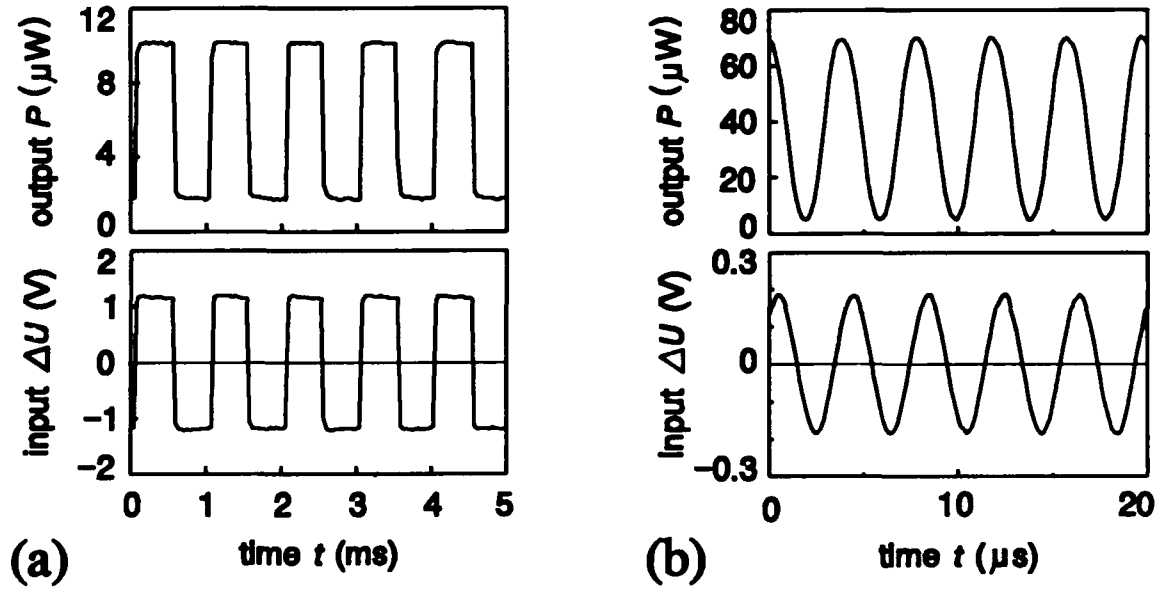

Fig. 3. Experimental results obtained with interferometer shown in Fig. 2.
Input voltage $\Delta U(t)$ and output power $P(t)$ at one output port vs time t. (a) Square-wave input of fundamental frequency $f = 1$ kHz; voltages $U_0 = 158$ V, $\Delta U = 2.3$ V; phase shift $\Delta\tilde{\Phi} \approx \pi$. (b) Sine-wave input of frequency $f = 250$ kHz; voltages $U_0 = 185$ V, $\Delta U = 0.37$ V; phase shift $\Delta\tilde{\Phi} \approx \pi$.

Deflection of guided waves

We also demonstrated the electrically actuated deflection of guided TE or TM modes using the same element E in the form of a bridge (see Fig. 4). It acts as an IO prism because the gap width $d(y)$, and consequently, the effective-refractive index $N(y) = N[d(y)]$ vary with coordinate y under the bridge. The deflection angle β is given by

$$\sin\beta = (L_x/N)(dN/dy) = (L_x/N)(\partial N/\partial d)(dd/dy) \quad . \qquad (6)$$

The deflection angle increases with voltage; with voltages of up to 350 V, maximum deflection angles of $\beta_{max} = \pm 5°$ were observed. This IO deflector could potentially be used to switch a guided wave to one of several output fibres.

Conclusions

In conclusion, we demonstrated that modulators, directional switches, and beam deflectors with response times of several microseconds based on the IO nanomechanical effect can be actuated electrically. We expect that by a further miniaturization of the devices (by micromachining techniques), the necessary driving voltages can be reduced to a few volts, possibly generated by IC's on the same silicon substrates.

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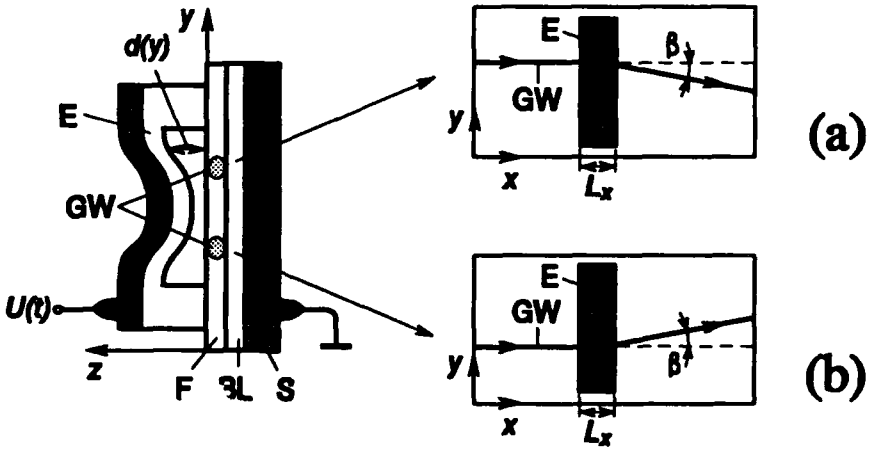

Fig. 4. Deflection of a guided wave by an effective-refractive-index-shifting element E in the form of a bridge with a spatially varying gap width $d = d(y)$.
Left, cross-sectional view through waveguide and element E. GW, guided wave under element E at positions (a) and (b). F, planar waveguide; S, substrate with buffer layer BL. $U(t)$, voltage between the upper part (Si) of element E and waveguide substrate (Si) causing bending of the bridge by electrostatic forces.

A resonant III-V semiconductor layer and a grating coupler integrated in a waveguide modulator for far-infrared light.

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Summary

Waveguide and grating structures offer a potential basis for novel far-infrared light (8-12 μm) integrated optics, as well as for replacing existing bulk infrared optical systems with guided-wave alternatives[1,2]. At these wavelengths residual waveguide losses are expected to be very small. Integration concepts can be applied with relaxed dimensional tolerances at these longer wavelengths. In this paper a new application of a resonant semiconductor layer integrated in a far-infrared waveguide modulator will be explained and experimental backing will be given.

By applying Drude's formula one can show that whenever the pulsation ω of the laser beam equals the plasma pulsation of the semiconductor layer ω_p ($\omega_p^2 = q^2 n_o/m^* \varepsilon\varepsilon_o$ with n_o, the electron density, m^* effective mass, q, the electron charge) the refractive index of the semiconductor layer almost vanishes. Realizing this resonant situation for a CO_2 laser needs semiconductors with small electron effective masses and sufficiently high doping concentrations (eg. 2 to 7 x 10^{18} cm^{-3} for n-InGaAs). However, the combination of high

doping concentrations and small electron effective masses is difficult to realise in III-V semiconductors due to the conduction band non-parabolicity.

In this resonant situation many interesting phenomena do exist. E.g., for TM-polarised plane waves this resonant plasma layer can act as a metallic mirror (whose reflectivity coefficient strongly depends on thickness variations in the range between 0 and 50 nm) due to photon-plasmon-photon transitions [3] or as an absorber due to surface plasmon polariton excitations [4]. Prototype depletion bulk modulators based on GaAs/AlGaAs technology were built to give experimental backing for these calculations. This design resulted in a device with low electrical power (300 mW) and low voltage (10 V) operation for 30% modulation depth. However, the maximum clocking frequency of these bulk modulators does not exceed 500 kHz due to the necessary large dimensions [5,6].

In order to increase this clocking frequency, waveguide structures have been considered. We showed that in waveguide mode regime the plasma layer can uncouple (couple) vertical parallel-coupled (uncoupled) waveguides [5]. The geometrical demands on this structure lead to inconvenient 10 μm thick structures. In order to decrease the total thickness a new application has been introduced: the uncoupling of a grating and a waveguide via the presence of a plasma layer.

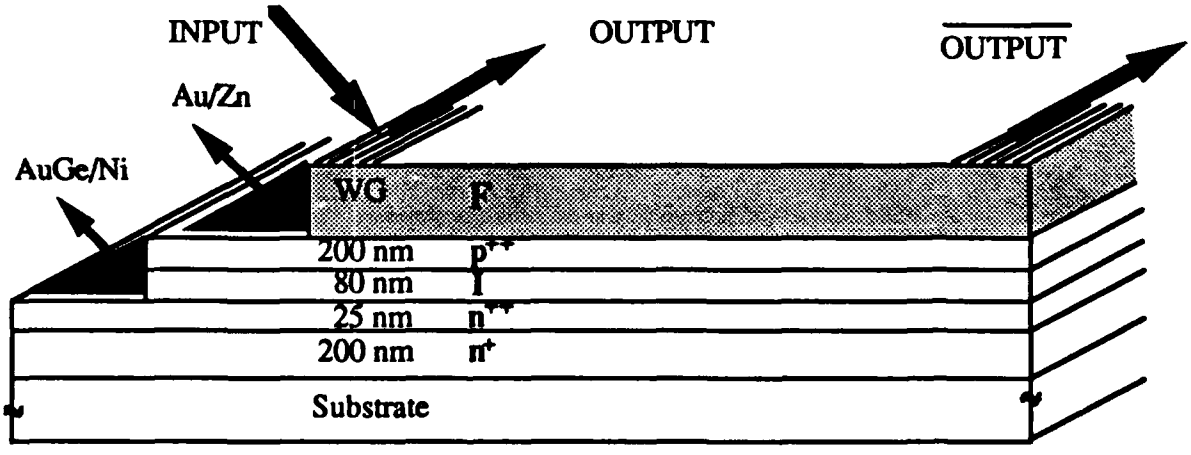

figure 1. Epitaxial layer structure for the grating-waveguide modulator where F is the waveguide film; p, I and n++/n+ form the electronic part of the modulator. The specific materials are indicated in tabel 1.

The grating-coupled waveguides studied in the present work, were designed using complex waveguide mode analysis and coupled-mode theory. The single mode waveguide structure is shown in figure 1. The material combinations we considered are indicated in table 1. These materials are grown by molecular beam epitaxy (MBE) and by metalorganic chemical vapour deposition (MOCVD). To minimize absorption as well as epilayer material, combinations of materials were preferred which don't need doped substrates or extra cladding layers between the waveguide film and the substrate, for establishing waveguide

regime. The effect of doping dependent material parameters were taken into account as well as the intrinsic and background doping in the waveguide layers.

cover	air	air
film	UN $In_{0.53}Ga_{0.47}As$	UN $In_{0.53}Ga_{0.47}As$
film thickness	3.6 μm	1.6 μm
p^{++}	p-GaAs (5.0×10^{18})	p-$In_{0.53}Ga_{0.47}As$ (5.0×10^{18})
I	UN $Al_{0.7}Ga_{0.3}As$	UN InP
n^{++}	n-GaAs (5.0×10^{18})	n-$In_{0.53}Ga_{0.47}As$ (3.0×10^{18})
n^{+}	n-GaAs (1.0×10^{17})	n-$In_{0.53}Ga_{0.47}As$ (1.0×10^{17})
substrate	UN GaAs	InP
technology	MBE	MOCVD

Tabel 1. Material combinations used for experimental grating waveguide modulators. Doping concentrations are expressed in cm^{-3}.

The real and imaginary part of the mode effective indices for the MBE structure are shown in figure 2. The differences between TE and TM polarised light and between resonant and no resonant layer are indicated. One can observe that the effect of the resonant layer is much larger for TM polarised light than for TE. For TM polarised light and for waveguide thicknesses between 3.3 and 3.7 μm the waveguides can be brought into cut off by the presence of the plasma layer. When the plasma layer is electronically depleted by the reversely biased pIn junction, coupling between the grating and the waveguide becomes possible for the correct coupling angle. Coupling between the grating and the waveguide results in a minimum for the reflection coefficient, yielding 100 % modulation depths for the complementary output.

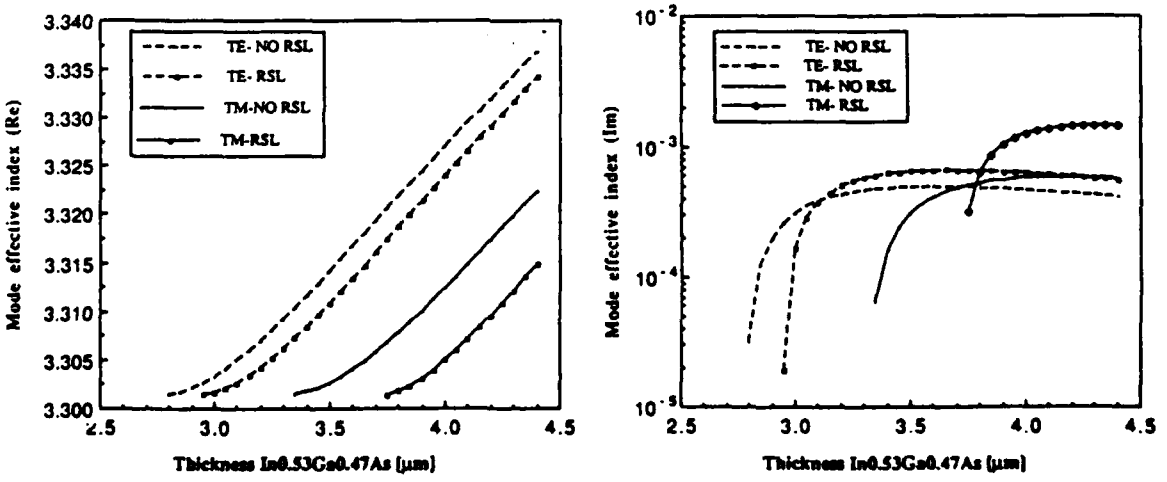

fig 2. Real and imaginary part of the mode effective index for the MBE waveguide structure. Thicknesses and doping concentrations of the different layers are indicated in fig. 1 and tabel 1.

Based on the coupled mode calculations, a grating period between 4 and 5 μm is necessary. This grating is chemically etched on top of the waveguide structure and is approximately 1μm deep. Input and output grating periods are chosen unidentically to distinguish the complementary output beams.

The maximum clocking frequency in this first prototype of 'cut-off' waveguide lay out is still determined by the RC time constants of the structure and has been limited by our own choice to 50 MHz (already 100 times faster than the previous prototype).

This coupling cut-off mechanism opens perspectives for very high modulation depths (theoretically 100 % at the complementary output). Theoretical calculations are performed for planar waveguide structures. This planar approach is valid as long as the experimental rib waveguides are wider than 50 μm. To finally push the switching speed into the GHz region, more compact, extremely low loss, structures are under consideration.

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2-D WDM OPTICAL INTERCONNECTS USING MULTIPLE-WAVELENGTH VCSEL's FOR SIMULTANEOUS AND RECONFIGURABLE COMMUNICATION BETWEEN MANY PLANES

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INTRODUCTION: The ability to connect efficiently many high-speed ports is of critical importance for large-capacity data processing. By taking advantage of the parallel nature of light, two-dimensional (2-D) optical planes can be employed to avoid the eventual electronic bottlenecks of reduced speed and increased power consumption.[1-3] However, a basic problem arises in the optical-plane solution when one plane wishes to communicate simultaneously or reconfigurably with many subsequent planes. Traditional optical systems solve this problem in two ways as shown in Fig. 1. The first method is for each plane to detect a data packet and then, if it was not intended for that plane, retransmit it to the next plane. The disadvantages include the possibility of an electronic high-speed bottleneck as well as the wasting of capacity, real estate, and optical hardware. The second method involves etching large via-holes in each plane's substrate as a window such that an unobstructed and permanent optical path is created between a transmitting pixel on plane i and a detecting pixel on plane j.[4] This second approach solves the electronic bottleneck but wastes real estate and allows only a given static configuration between any two planes.

We propose a novel solution using wavelength-division-multiplexing (WDM) [5,6] to facilitate simultaneous and reconfigurable communication of one-to-many 2-D optical planes. This advance would dramatically increase the system functionality of optical-plane interconnects. Such a system is realized by incorporating several multiple-wavelength vertical-cavity surface-emitting lasers (VCSEL) [7] into each transmitting pixel and incorporating wavelength-selectivity into each subsequent detecting plane which will absorb one wavelength and be transparent to the rest; these structures can be fabricated by slightly modifying existing technology. This system will allow for increased processing functionality of communicating both simultaneously and reconfigurably between many planes; broadcasting and dynamic independent interconnects are thus enabled. Our analysis shows that a high contrast-ratio with low power-penalty can be achieved for a $\Delta\lambda$>40nm. Furthermore, by implementing WDM, system capacity is enhanced and real-estate usage is more efficient.

SYSTEM CONFIGURATION: Figures 2a and 2b depict the basic concepts for this WDM 2-D optical interconnect system in which, for simplicity in this first example, only one plane is transmitting and several planes are receiving with a total of M planes. The transmitting plane is composed of an NXN pixel array with each pixel containing a miniature multiple-wavelength VCSEL array. Each laser in a pixel emits light at a different wavelength, λ, and these wavelengths are equally spaced apart. There are (M-1) lasers in each pixel corresponding to the (M-1) other planes which this pixel may wish to communicate with. This WDM pixel is repeated identically for the entire NXN plane array. Each of the (M-1) detector planes has N^2 pixels, each of which contains a p-i-n detector with its spectral response slightly offset from one plane to the next in its wavelength-dependent detectivity. The detector planes will be designed such that the cutoff wavelength increases for each subsequent plane. Each detecting plane will detect only the shortest-λ signal remaining in the beam and will be transparent to all the longer-wavelength signals. As an example, for (M-1)=3 and $\lambda_1<\lambda_2<\lambda_3$, detector plane 1 will absorb λ_1 only and be transparent to λ_2 and λ_3, detector plane 2 will absorb λ_2 only and be transparent to λ_3, and the final plane will absorb λ3. Thus, communication can be accomplished from one transmitting plane to many detecting planes in a dynamic and reconfigurable manner simply by switching "ON" the single appropriate laser in the VCSEL. Two other configurations exist. First, broadcasting simultaneously to many planes from this WDM pixel can be accomplished by turning "ON" many lasers simultaneously which can transmit the same bit stream to many planes. Second, if enough control electronics is included in each transmitting pixel, then each laser can be independently biased and one pixel can even communicate different, independent information to many planes simultaneously.

The fabrication of WDM pixels and λ-selective detectors can be achieved with slight alteration of existing technology.[7] By fabricating a thickness gradient in a few layers of the VCSEL structure, a series of lasers can be made to emit distinct, equally-spaced wavelengths. Such a gradient will be made periodic across the wafer to produce identical WDM pixels. Additionally, a potential problem from an arrangement in which all planes are transmitting and receiving is that some stray light from the lasers will be coupled into the laser cavities on other planes. We expect this stray light to change some of the laser characteristics but that the overall performance will not be significantly degraded since these VCSEL's will be spaced apart by several nm's and be operated well below their expected multi-GHz bandwidth.

PERFORMANCE ANALYSIS: Key parameters in evaluating the feasibility of WDM implementation include the contrast ratio and power penalty which can be achieved when a given plane absorbs one shorter-wavelength signal and rejects several other longer-wavelength signals. All the wavelengths are placed on the long-wavelength edge of a typical response curve of an InGaAs detector, as shown in Fig. 3;[8] such a detector can be tailored as follows: (i) its cutoff wavelength can be changed over a wide wavelength range by varying the In content, and (ii) the steepness of the responsivity roll-off can be varied by using bulk or multiple-quantum-well material. Figure 4a calculates the contrast ratio versus wavelength separation, $\Delta\lambda$, between a signal intended to be absorbed and a single rejected wavelength intended to be unaffected and passed. The contrast ratio is computed for different selected-signal wavelengths in comparison to the wavelength at which the responsivity curve is a maximum such that ($\lambda_{select}>\lambda_{max}$); this is depicted as the percent of the responsivity at the selected wavelength in comparison to the responsivity maximum. If the wavelength producing maximum responsivity (100%) is chosen for the selected signal, then more of the rejected wavelength will also be absorbed thus reducing the contrast ratio. It is determined that a $\Delta\lambda$>40nm for the 70%-of-maximum case will provide a contrast ratio >20dB; a $\Delta\lambda$<20nm can be used if the %-of-maximum is further decreased. Figure 4b shows the power penalty for a given $\Delta\lambda$ taking into account not only the rejected signal absorption but also the added penalty due to operating off the responsivity peak. A power penalty <3dB can thus be achieved with the operating conditions mentioned above. As an additional systems guideline, Fig. 5 shows the optimum responsivity level (and operating wavelength) of the selected signal in relation to the responsivity maximum. For a given $\Delta\lambda$, the curve has two distinct slopes, the right one representing the influence from the neighboring wavelength and the left slope arising from operating at a lower responsivity.

An analysis of the total system capacity can be performed when comparing the three systems of point-to-point (Fig. 1a), via (Fig. 1b), and WDM (Fig. 2) planes. We will address the following two basic scenarios, one in which one plane transmits and the rest receive or relay information, denoted as 1T-MR, and the other in which all intermediate planes can transmit their own data as well as receive, denoted as MT-MR; note that MT-MR would require each pixel to contain both a laser **and** a detector. Furthermore, we will examine three variations of the basic WDM pixel: (a) the (M-1) lasers can only be turned "ON" one at a time from the same driver (reconfigurably), (b) the (M-1) lasers can all be turned "ON" simultaneously but with the same data coming from the same driver, and (c) the (M-1) lasers can be turned "ON" simultaneously and independently, sending different data to many different planes and requiring (M-1) drivers. For simplicity, we have not included any fairness in the algorithm.

The total system capacity can be derived using analytical formulae (not shown) for all the above interconnect scenarios. We define system capacity as the total bandwidth of new information that can be transmitted for a given configuration. Also, if the same data is being broadcast from m lasers in a given pixel to m different planes, then this represents the establishment of m different signal channels. Figure 6a and 6b show the total system capacity as a function of the number of optical planes for the cases of 1T-MR and MT-MR, respectively. The plane-to-plane and via-hole interconnects have the same usable system capacity since the act of relaying information with a pixel or with a via-hole does not add any new information. The three WDM cases have different capacities. The case in which only one of the (M-1) lasers in a pixel can transmit represents the same capacity as the non-WDM solutions for 1T-MR, but it does provide the added feature of reconfigurability. An important and non-intuitive result is that this same WDM case for MT-MR is actually a significant enhancement over the traditional solutions. This is true because the WDM pixel can establish an **additional** communications channel between itself (i) and another plane (j) even if it is concurrently in the process of relaying data between another two planes (k,l) by being transparent to that other signal. The WDM cases in which all the lasers can be simultaneously broadcasting the same information or transmitting independent data represents the maximum capacity, even though the independent case is much more flexible than the broadcasting case. This capacity enhancement increases for increasing number of planes.

Even though WDM helps to achieve important capacity improvements, we wish to show the real-estate efficiency of the optoelectronic pixels. The calculation of the area required by each pixel for the cases of 1T-MR and MT-MR included the size of the lasers, detectors, laser-driver electronics, receiver electronics, and connecting wires on a 2-D plane.[9,10] It is determined that the pixel area is dominated by the laser electronics and receiver electronics and not by the size of the (M-1) VCSEL array in each pixel. The only WDM case in which the pixel area increases with M is when (M-1) laser drivers are needed to drive all the lasers simultaneously and independently.

SUMMARY: We have proposed and analyzed a novel optical interconnect configuration in which one 2-dimensional plane can communicate simultaneously and reconfigurably with many planes by using WDM. This advance would dramatically enhance the system functionality of optical-plane processing. Multiple-wavelength laser arrays and wavelength-selective detectors are used to provide high contrast ratio and low power penalty with a $\Delta\lambda$>40nm in addition to increased system capacity and more efficient real-estate usage.

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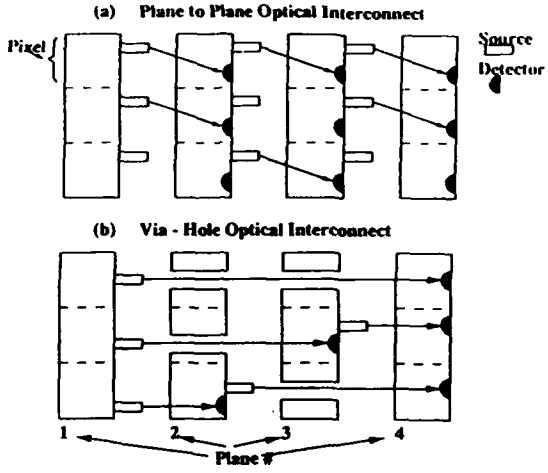

Fig. 1. Optical interconnections between several planes. (a) Plane-to-plane communication in which a given plane must relay data by receiving and then retransmitting it. (b) Via-hole windows which establish a permanent optical path.

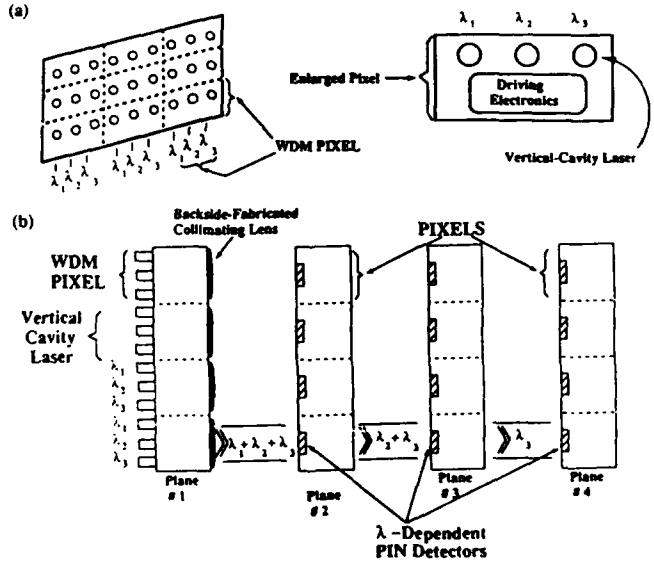

Fig. 2. (a) A multiple-λ VCSEL array in which (M-1) different-λ lasers are fabricated in each identical WDM pixel. (b) One-to-many optical plane interconnection configuration using a 3-λ VCSEL pixel array and three λ-selective detecting planes.

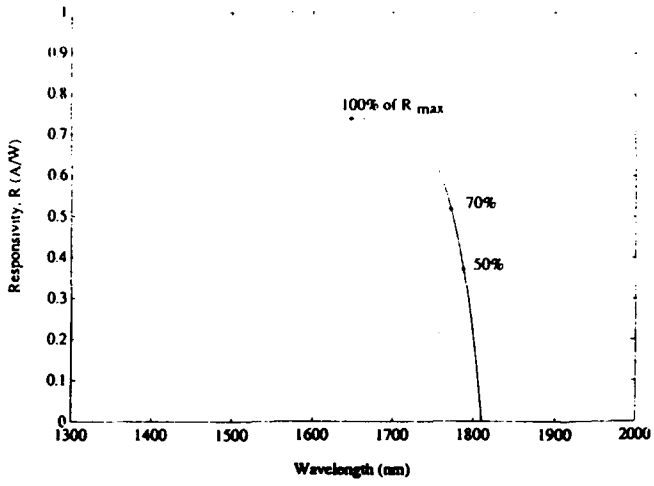

Fig. 3. Typical responsivity versus incident wavelength curve for an InGaAs detector.

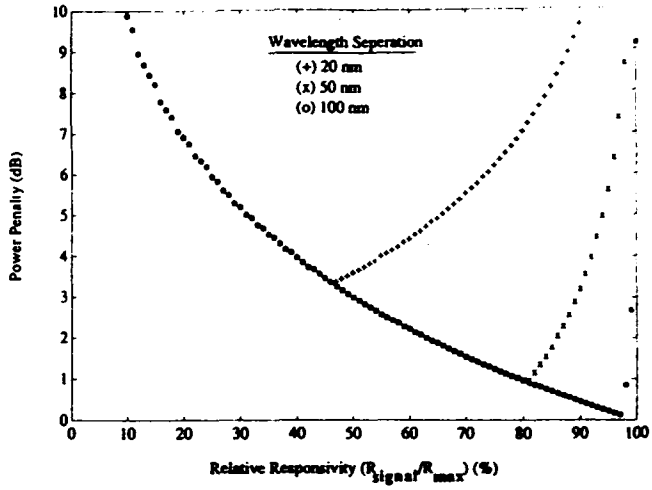

Fig. 5. Power penalty versus the percent of the responsivity of the selected channel in relation to the maximum responsivity, such that ($\lambda_{select}>\lambda_{max}$).

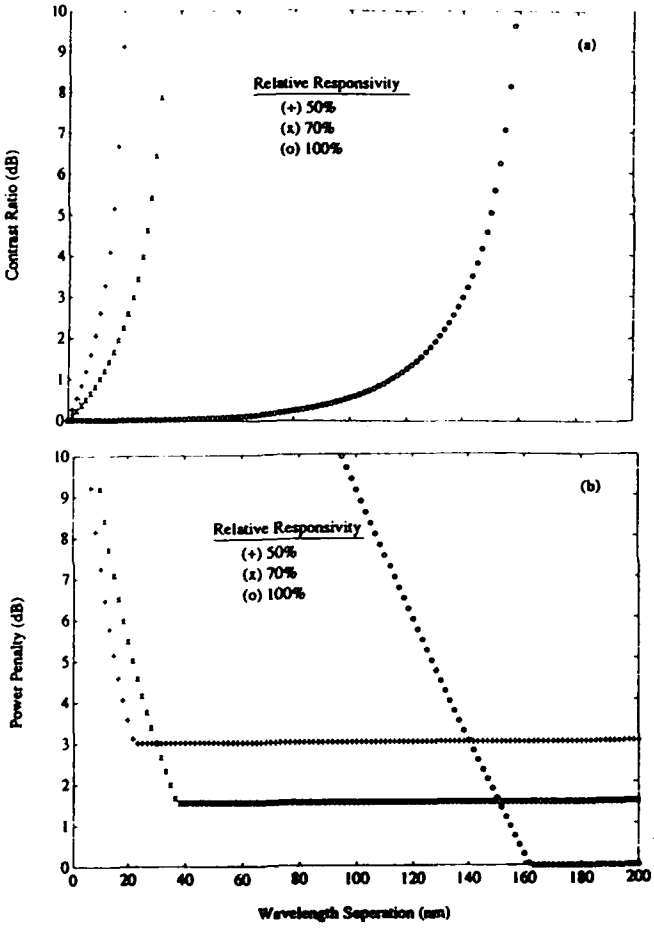

Fig. 4. (a) Contrast ratio between a selected and rejected wavelength versus their wavelength-separation. Curves represent different selected-channel responsivities in relation to the responsivity maximum, such that ($\lambda_{select}>\lambda_{max}$). (b) Power penalty versus $\Delta\lambda$.

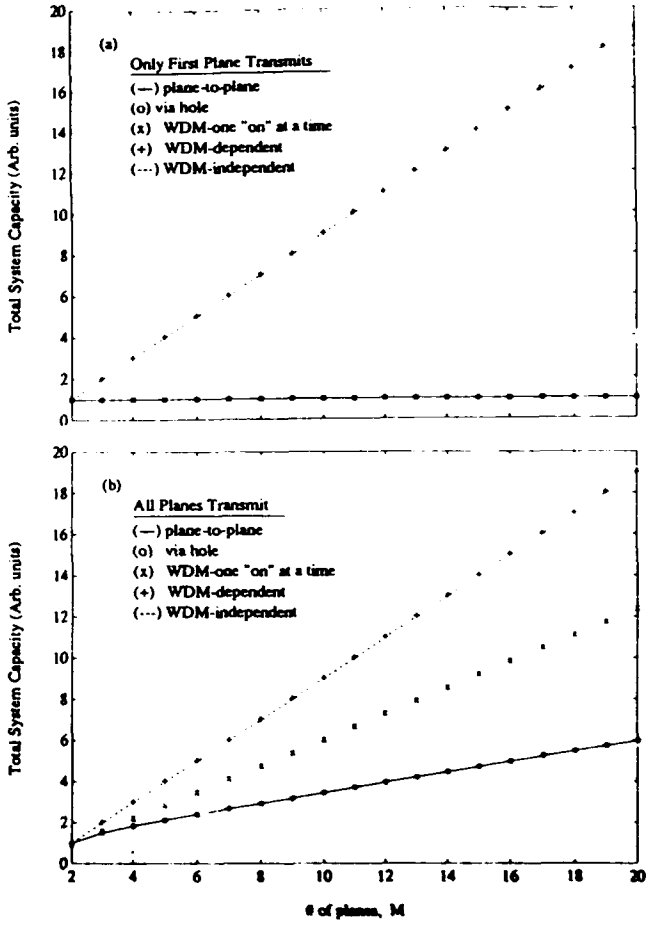

Fig. 6. Total system capacity versus number of optical planes for (a) only the first plane transmitting (1T-MR), or (b) all planes with the ability to transmit (MT-MR).

All-Optical Switching

PWA 8:30am-10:00am
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Kunio Tada, *Presider*
University of Tokyo, Japan

Nonlinear Loop Mirrors for All-Optical Switching

Keith J. Blow
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Ultrafast nonlinear refraction in an active MQW waveguide

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Introduction: Future practical ultrafast (>100 Gbit/s) all-optical switching and information processing systems will need nonlinear optical devices which combine high speed of operation with moderate optical power requirements. Recently a large above-bandgap ultrafast optical nonlinearity has been observed in active semiconductor waveguides driven at the material transparency current[1,2]. The origin of the new nonlinearity is not yet clear. Dynamic carrier effects may contribute, as may a resonantly enhanced optical Stark effect, not normally observable in passive waveguides because of high interband absorption. In the case of active waveguides at transparency this optical loss is balanced by gain from the electrical pumping.

In this paper we present the first assessment of the magnitude of the nonlinearity in a semiconductor multiple quantum well (MQW) waveguide, demonstrating a large nonlinear figure of merit. In a MQW waveguide at transparency a magnitude of n_2 of ~4×10^{-11} cm^2W^{-1} for TE polarisation was observed, resulting in peak nonlinear phase shifts in excess of 2π radians in a 1mm waveguide at sub-Watt peak guided powers and speeds faster than 20ps. MQW active waveguides have the additional benefit over the equivalent bulk devices of lower background loss which is a potentially limiting factor in photonic switching devices[3].

Experimental details: The device studied here is a 1mm long four quantum well (GaInAs/Q(1.29μm)) GRINSCH buried heterostructure waveguide, details of which have been given previously[4], with both facets anti-reflection coated. The nonlinearity was characterised by observing self phase modulation (SPM) of a short (~20-30ps), high power optical pulse on passing through a waveguide under conditions of carrier injection. The pulse source was a synchronously mode-locked KCl:Tl^0(1) colour-centre laser operating at a wavelength within the gain bandwidth of the active waveguide at a pulse repetition rate of 82MHz. It was configured to give stable, transform limited pulses which were monitored using an autocorrelator. Light was coupled into and out of the waveguides using microscope objectives and the launched polarisation controlled with a half-wave plate. A scanning Fabry-Perot interferometer was used to monitor the spectrum of the transmitted light. The

transparency current was identified by monitoring the voltage supplied to the waveguide by a constant current source in the presence of a modulated optical signal[5]. This technique may provide the basis for an automatic control scheme. The value of the transparency current may depend on the intensity of the optical input and in practice the value used will be chosen so as to minimise any long term effects on the carrier populations.

Results: Either above or below the transparency current, spectral broadening of the pulses was observed due to saturation of either the gain or the absorption respectively. This broadening was accompanied by a shift of the whole spectrum. At transparency (12.6mA at 15.0°C and a wavelength of 1526.8nm, for example), however, symmetrical broadening was observed with a change in the shape of the spectrum (Fig. 1).

The SPM behaviour was similar across the gain spectrum of the waveguide with appropriate setting of the transparency current. A single device should, therefore, be able to operate at any point across a broad wavelength range (10's of nm) with an appropriate current bias.

The behaviour illustrated in Fig.1 is similar to that observed by Grant and Sibbett[1] and is characteristic of SPM due to a nonlinear index change with a recovery time much faster than the incident pulse duration (21ps, assuming a Gaussian pulse shape). The particular shapes of the spectra allow the peak phase shift in the waveguide to be determined. The spectral data in Figs.1b and 1c imply peak phase shifts of $3\pi/2$ and $5\pi/2$ radians respectively. This allows us to deduce the magnitude of n_2, the nonlinear refractive index coefficient. The maximum peak guided power used was 820mW and the modal area was calculated using the weighted index method[6], modified for buried heterostructure waveguides, giving a value of $2\mu m^2$ for TE polarised light. Values for $|n_2|$ of $4\times10^{-11}cm^2W^{-1}$ for TE and $2.5\times10^{-11}cm^2W^{-1}$ for TM were obtained ($\pm\sim1\times10^{-11}cm^2W^{-1}$), similar to though somewhat larger than previously reported values[1,2]. These may be compared with values of $\sim1\times10^{-12}cm^2W^{-1}$ for below band-gap effects[7] such as would be expected from barrier and cladding material in the waveguide. The values quoted here are for the waveguide, not the nonlinear material, for which the optical confinement factor is approximately 0.04 in this particular waveguide structure. There is probably considerable scope for optimising the structure to give larger effective n_2 values if desired. Earlier work indicates that n_2 is defocussing (i.e. negative)[1,2]. As far as speed is concerned, these preliminary measurements indicate recovery

times considerably faster than 20ps but say no more than this. Grant and Sibbett[1] suggest a value of a few picoseconds but time resolved work[2] has demonstrated a large (negative) component faster than the 400fs pulses used in the experiments as well as a (positive) slower one (~1.7ps) associated with carrier heating. We may speculate that the spectral data of Ref.1 is affected by this slower component. The detailed mechanism of the nonlinearity is a question that needs to be addressed to allow optimisation of both its size and speed. Some calculations of nonlinear refraction in bulk material with current injection have recently been presented[8].

The spectrum in Fig.1c exhibits some deviation from the conventional three peaked structure resulting solely from a fast refractive nonlinearity. The abnormally high central peak is probably related to nonlinear absorption which will tend to flatten the temporal profile of the pulse. Some evidence of nonlinear absorption was detected in simple transmission measurements. This effect is most likely due to two photon absorption (TPA) in the barriers and confinement layers with some contribution from carrier heating in the wells[9].

We can evaluate the suitability of this ultrafast refractive nonlinearity for all-optical switching by considering a figure of merit for nonlinear materials[10], which makes clear some minimum requirements for all-optical switching device applications, independent of the waveguide length and the optical intensity:

$$\left|\frac{n_2}{\beta\lambda}\right| > c$$

where β is the nonlinear absorption coefficient, λ the operating wavelength and c a constant, depending on the device structure (2 for a nonlinear directional coupler and 1 for a Mach-Zehnder interferometer, for example). Assuming the dominant nonlinear absorption in this device is TPA in the confinement layers we follow the work of Sheik-Bahae et al.[11] on bulk material, and estimate β to be ~40cmGW^{-1}. This leads to a figure of merit of around 7 for the unoptimised waveguide structure in this device, comfortably above the minimum requirement for a range of potential devices. There is also scope for improvement in the waveguide design to increase the figure of merit and approach the goal of practical ultrafast switching devices.

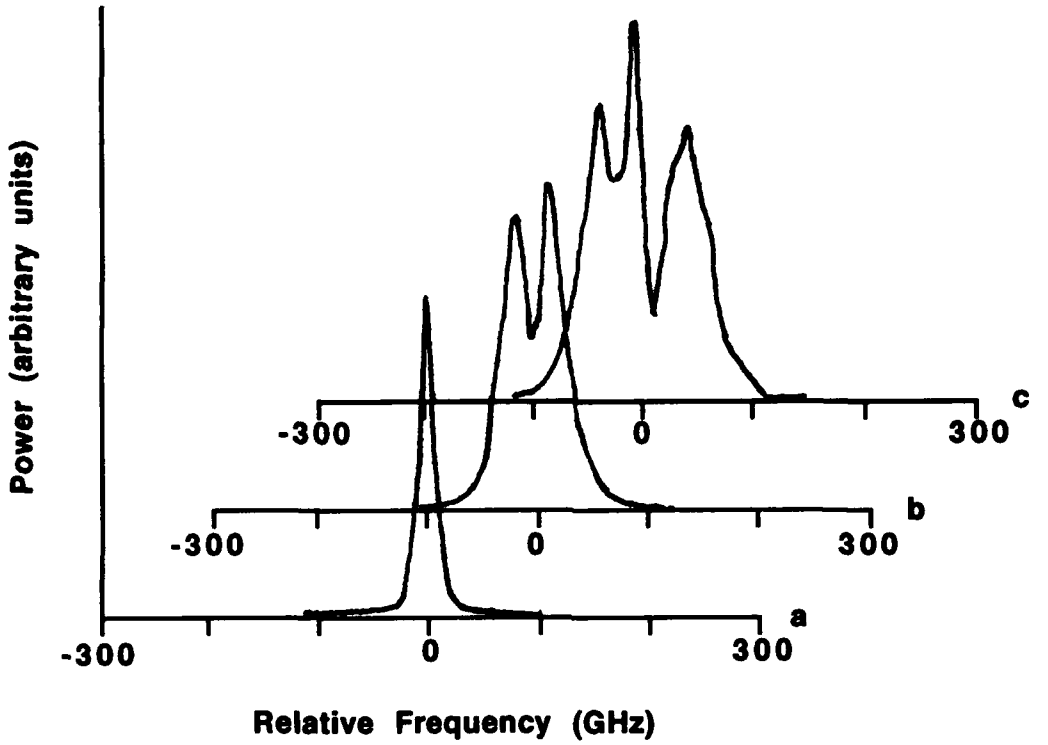

Fig.1: Spectra of 21ps pulses after passing through active ridge waveguides in TE polarisation.
a). Low power reference
b). 600 mW peak power, spectrum characteristic of a 3π/2 peak phase shift.
c). 800 mW peak power, spectrum characteristic of a 5π/2 peak phase shift.

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Demonstration of a Polarisation Rotation Gate in GaAs/AlGaAs Multiquantum Well Waveguides

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Introduction

Recent work on the development of integrated optical devices for nonlinear switching and processing has focused on the performance of Mach Zehnder[1] and directional coupler[2] switches. However previous research into optical fibres has identified the potential of the birefringent polarisation gate[3]which is known to have better stability against external fluctuation than interferometric gates based on independent optical paths.

This paper presents, to our knowledge, the first experimental demonstration of an integrated birefringent polarisation gate operating on femtosecond timescales in a GaAs/AlGaAs multiquantum well (MQW) waveguide. The gate demonstrated here employs, at photon energies near the half bandgap, the ultrafast third-order refractive nonlinearity which has only recently been quantitatively measured in semiconductors[4] and used for switching devices[1,2].

Fig. 1 shows a polarisation rotation gate using a rib waveguide as the nonlinear birefringent element. Light is launched into the birefringent waveguide at an angle,θ, to its principle axes. A phase delay, $\Delta\phi_B$, is induced between the modes propagating down the principle axes and elliptical light exits the waveguide. This is then linearised using a quarter wave plate and blocked with a polarising filter. If the power coupled into the waveguide is changed the refractive nonlinearity modifies the phase delay and hence the ellipticity of the light; the so called polarisation rotation. This rotation changes the net transmissivity of the quarter wave plate and polariser pair and provides the switching mechanism.

Experimental Details

The GaAs/AlGaAs single mode rib waveguide structure used in the polarisation rotation gate consisted of an MQW region composed of 64 GaAs quantum wells of nominal width 4nm separated by 63 4nm wide $Al_{0.45}Ga_{0.55}As$ barriers. Guiding was achieved through the formation of ribs of 8 micron width. Measurements of the linear absorption coefficient of the waveguides gave α~4.5cm^{-1} for both TE and TM polarisations, at a wavelength of 1.51 μm. The two photon absorption coefficients were measured to be 1.1cmGW^{-1} for TE and 0.1 cmGW^{-1} for TM polarised light, in agreement with previously measured values [5].

Fig. 2 shows the experimental arrangement used to observe polarisation rotation and gating. A coupled cavity mode-locked KCl:Tl colour centre laser was used to generate pulses of 90fs FWHM duration at a repetition rate of 82.3MHz and at a wavelength of 1.512μm. Longer pulses, of ~30ps duration, were obtained by blocking the external cavity of the colour centre laser. The pulse durations were measured using an SHG autocorrelator. The polarisation of the incident light was set to be 20° to the TM axis by a high extinction ratio polariser (#1). Light transmitted through the waveguide was collimated and passed through a linearising quarter-wave plate and another high extinction ratio polariser (#2) to enable observation of polarisation rotation. The modal quality of the waveguiding was continuously monitored on the IR camera.

Assessing the Nonlinear Rotation

Initial measurements of polarisation rotation were carried out on a 1.5mm long waveguide. A reference output polarisation was set using 90fs pulses of average incident power 9.7mW. The transmitted light was linearised and blocked at the output by the quarter wave plate and polariser, hereafter referred to as the ellipticity analyser. The incident power was then stepped down to 0.7mW and the power transmitted by the ellipticity analyser recorded against incident power. The upper trace in Fig. 3 shows the ratio of measured power, P_t, over incident power, P_o, plotted against the shift in incident power from the power at which the transmitted light was linearised, $P_{0,lin}$.

Polarisation Rotation Theory

The transmitted power, P_t, assuming lossless conditions and monomode operation, is given by the standard polarisation gating equation[3],

$$P_t = P_c \sin^2(2\theta) \sin^2\left(\frac{\Delta\phi_B}{2}\right) \tag{1}$$

where P_c is the power coupled into a lossless waveguide and $\Delta\phi_B$ is the phase difference between components of the light on the birefringent axes relative to the phase difference at which the light is blocked. $\Delta\phi_B$ Is given by

$$\Delta\phi_B = K_p \cos 2\theta (P_c - P_{lin}) \tag{2}$$

where K_p depends on the optical Kerr coefficient, n_2, the effective length of the waveguide, L_{eff}, the wavelength of the light, λ_p, and the effective area, A_{eff}, of the waveguide. The polarisation of the incident light is at an angle θ to the TM axis of the waveguide.

Taking into account the losses M, the lumped output coupling loss and the loss in the ellipticity analyser, and L', the lumped insertion loss and averaged absorption loss, it can be shown that for small $\Delta\phi_B$ the transmission varies as the square of the input power:

$$\frac{P_t}{P_o} = \frac{1}{16} M L'^3 K_p^2 \sin^2 4\theta (P_o - P_{lin})^2 + F \tag{3}$$

F represents the fraction of the incident power being detected due to non-ideal analysers in the system. This equation allows a parabolic curve to be fitted, with good accuracy for low $\Delta\phi_B$, to the data in figure 3.

Using this theoretical approach the experimental results have been replotted, Fig. 3, in terms of $\Delta\phi_B$. In agreement with theory where,

$$\Delta\phi_B = K_p L' \cos 2\theta (P_o - P_{o,lin}) \tag{4}$$

a linear response is found. Performing a linear regression on the data in Fig. 3 gives a straight line which correctly intercepts the y-axis at the origin and has a gradient of 6.7 °/mW. Using values of $\lambda_p = 1.512\mu m$, $A_{eff} = 3\text{x}10^{-12}\text{m}^2$, $L_{eff} = 1.1$mm, $\theta = 9°$ and $L' = 8.2$ dB, consistent with measured losses, a value of 1.2×10^{-17} m^2W^{-1} is found for the nonlinear refractive index. This is in good agreement with the recently measured value[4]. It should be noted that the value of θ used corresponds to the measured value at the output of the waveguide calculated from the linearisation position of the ellipticity analyser. This rotation is observed even in the absence of birefringent effects due to unequal nonlinear absorption losses for TE and TM light modes.

Polarisation Gate

To demonstrate the polarisation gate, measurements were performed on a longer, 7.9mm, waveguide. At low optical powers, the ellipticity analyser was set to block as much output light as possible. Switching of the gate was then achieved by increasing the peak optical power to induce nonlinear birefringence in the waveguide. The polarisation state of the light leaving the

waveguide therefore changed and thus the transmission through the ellipticity analyser was altered. Hence the device switched to a higher transmission state. 30ps pulses of 10mW average power (1W peak coupled power) were used as the low power pulses and 90fs pulses with the same average power but a higher, 330W, peak coupled power were used as the high power pulses. The transmission of the pulses increased by a factor of 44 from the low power to the high power input and thus a very strong nonlinear switching action was achieved. The transmission, expressed as a percentage of the maximum transmission taking account of losses, increased from 1.2% to 54% between "off" and "on" states. Thus, from equation 1, the phase shift $\Delta\phi_B$ between the TE and TM polarisations was at least 90°.

The Gaussian shape of the pulse meant that there was a differing amount of nonlinear transmission change for each part of the incident pulse. The increase in normalised transmission by the factor of 44 is an average over the pulse. At the peak of the pulse the increase was greater than the measured value. An advantage of the birefringent gate, therefore, is that high transmission changes and high total transmission may be achieved even with the non square pulses provided by femtosecond lasers.

Conclusion

We have demonstrated a polarisation rotation gate in a GaAs/AlGaAs MQW waveguide that transmits 54% of the maximum possible power output in the presence of a phase shift induced by nonlinear birefringence. The gate has been demonstrated to provide a very large 44:1 change in transmission between the "off" and "on" states.

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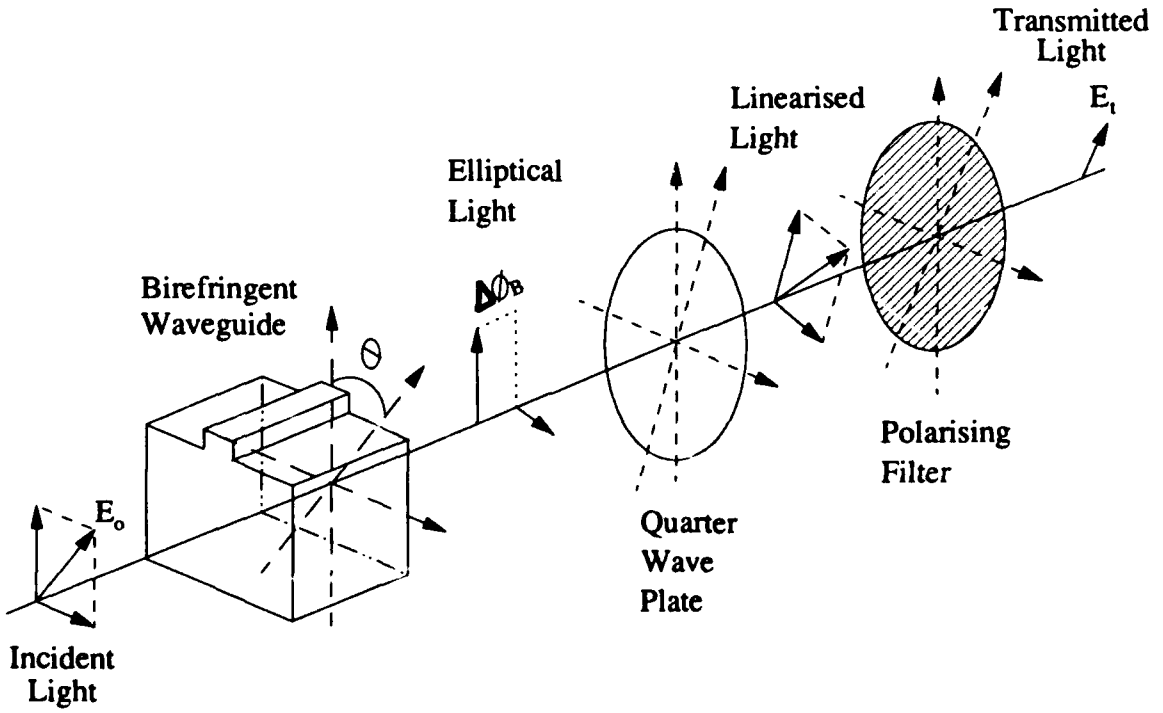

Figure 1 : Birefringent Polarisation Rotation Gate

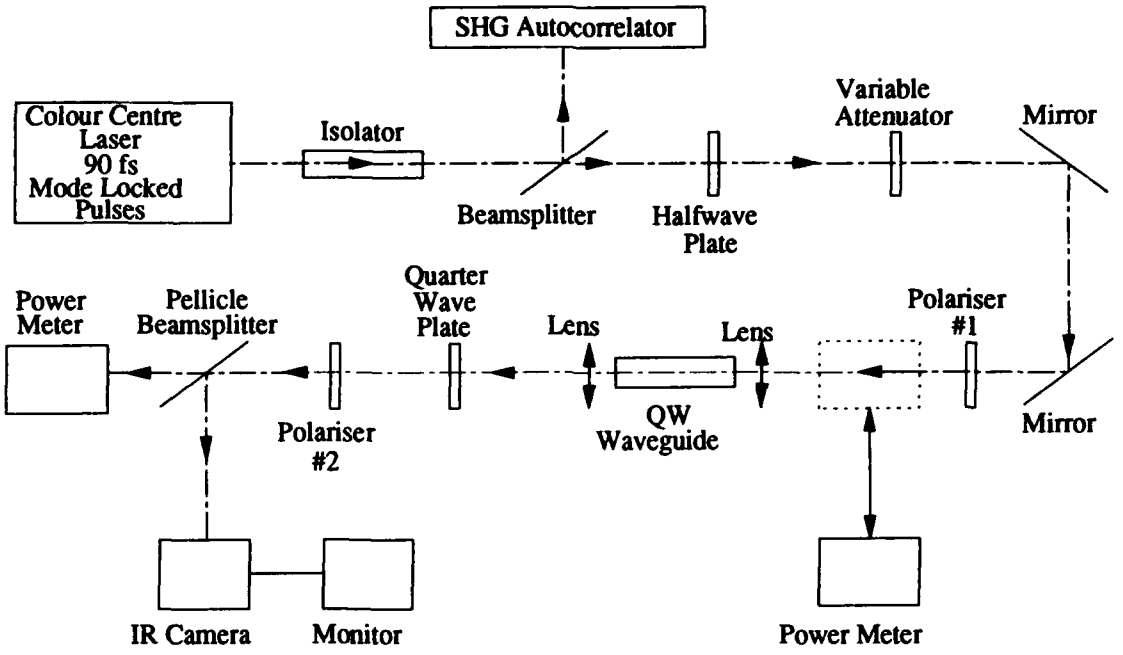

Figure 2 : Experimental Apparatus

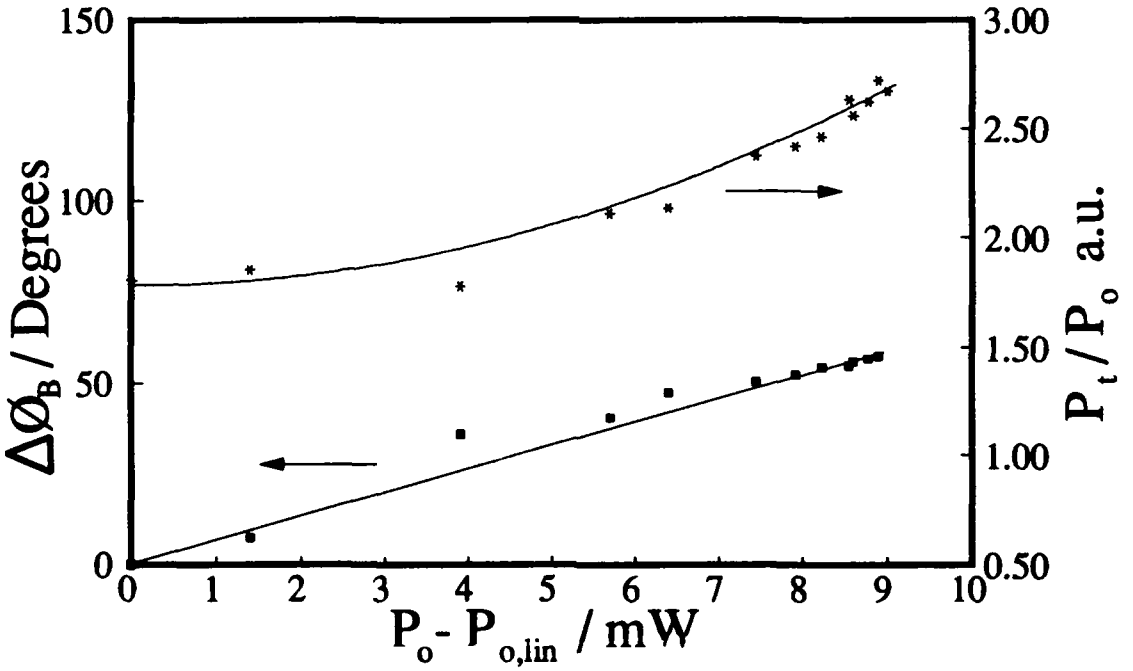

Figure 3 : Nonlinear Rotation Characterisation

All optical regenerator using a semiconductor laser amplifier in a loop mirror configuration

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All optical repeaters, which retime optical data signals, are essential components for photonic switching systems. In general these regenerators operate as follows. The optical data signal is combined with an optical clock signal (synchronized with the data signal) and both are coupled into a decision gate (AND gate). Decision gates based on a SEED (data rate 5 kbit/s [1]), on a bistable Fabry-Perot amplifier (data rate 140 Mbit/s [2]), on a bistable three electrode DFB laser diode (data rate 200 Mbit/s [3]) and on a nonlinear Sagnac interferometer switch (data rate 5 Gbit/s [4]) have been demonstrated. In this paper we report on a new kind of decision gate based on a semiconductor laser amplifier (SLA) in a loop mirror (SLALOM) configuration. This decision gate was operated at 1 Gbit/s. It exhibits a contrast ratio of better than 20 dB, no polarization dependence for the data signals, and it enables simultaneously all-optical wavelength conversion over a wavelength range of about 60 nm. As compared to the nonlinear Sagnac interferometer switch, it requires optical powers for switching, which are about three orders of magnitude lower. It is very compact and offers the advantage of a possible integration on a chip.

The SLALOM was introduced recently [5]. As depicted in Fig. 1, the SLALOM consists of a 3 dB-fiber coupler with two arms connected forming a loop (length a few cm). The loop contains a SLA and a delay line (length 6.2 cm) corresponding to a delay time T = 310 ps. In [5] the SLALOM was operated as an optical correlator for picosecond pulses. Two pulses were fed to the input and, at the output, an optical pulse was obtained if the pulses were separated by a time interval T. With a contrast ratio of 13 dB there was no output signal if the pulse separation differed from T by more than the gain recovery time of the SLA.

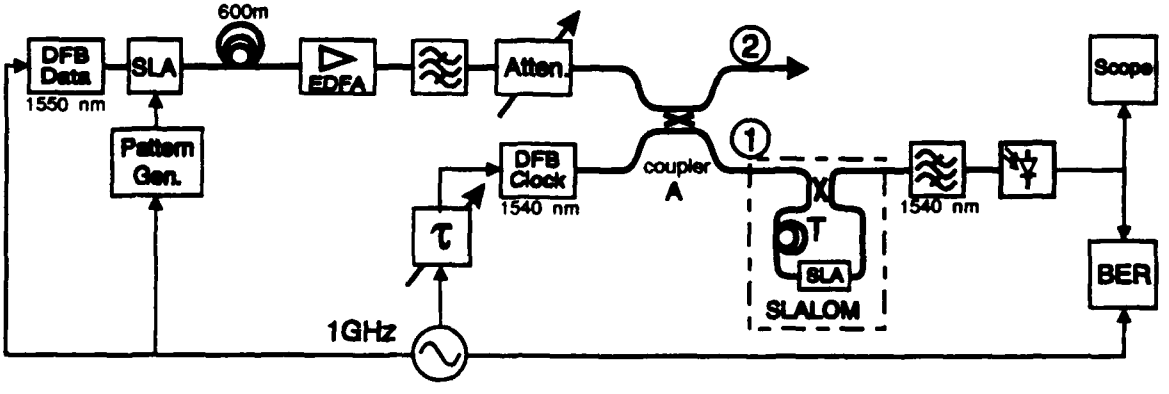

Fig.1: Experimental arrangement

In the present experiment the two pulses are a clock and a data pulse. Fig. 1 shows the experimental arrangement for investigations of the SLALOM based regenerator. (Strictly

speaking we investigate here only the operation of the decision gate and not the synchronization of the clock pulses.) At the coupler A, data pulses (λd = 1550 nm, peak power between -5 dBm and +10 dBm) and clock pulses (λc = 1540 nm, peak power -6.5 dBm) are combined. Both pulse sources (gain switched DFB lasers) are driven by the same master oscillator (1 GHz). The data pulses are modulated by a SLA gate, which is driven by a pattern generator (PRBS 2^{23}-1), and pass an Erbium doped fiber amplifier (EDFA, 26 dB gain), an optical filter and a variable attenuator to obtain the desired power at the coupler A. A tunable electrical delay line (time delay τ) between the master oscillator and the clock pulse source is used to change the time delay between clock and data pulses for testing the jitter tolerance of the optical regenerator. A dynamical relative jitter may also be provided by frequency modulation of the master oscillator in combination with the different fiber lengths in the clock and data paths. The filter at the output of the SLALOM is tuned to the clock pulses (λc = 1540 nm).

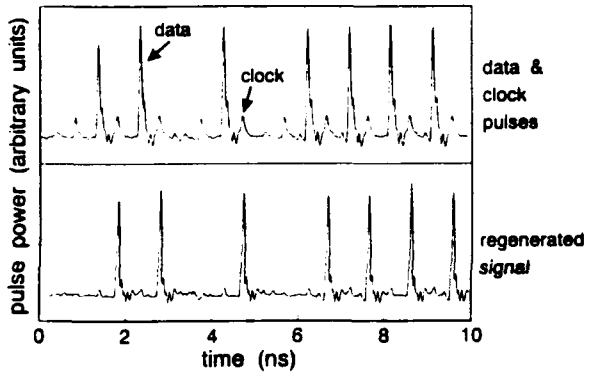

Fig. 2: Oscilloscope traces of the data and clock pulses at output 2 of coupler A and the regenerated signal

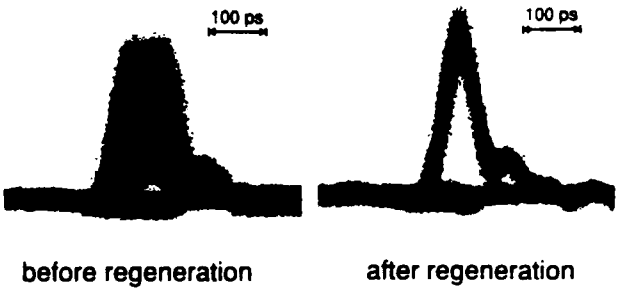

Fig. 3: Eye diagrams of the data signal before and after regeneration

Fig. 2 depicts, in the upper part, data and clock pulses at output 2 of the coupler A and, in the lower part, the regenerated signal, where the information of the data pulses has been transfered to the clock pulses. The regenerated signal is independent of the polarization of the data signal for $\lambda c \neq \lambda d$. In general the only requirement for λc and λd is, that both fit into the bandwidth (60 nm [6]) of the SLA. Fig. 3 depicts the eye diagrams of the data signals before and after regeneration, where the data pulses were jittered intentionally using frequency modulation of the master oscillator. To test the jitter tolerance of the SLALOM based regenerator, we performed BER measurements of the regenerated signal by electrically varying the relative delay between the input data pulses and the clock pulses for several values of the data pulse peak power (see Fig. 4). Fig. 5 shows measurements of the BER versus the input data pulse peak power for several values of relative delay between data and clock pulse. The results reveal that the SLALOM based regenerator provides retiming of data signals at BER $< 10^{-9}$, if these data signals remain within a $\pm$50 ps switching window and within a 10 dB dynamical range.

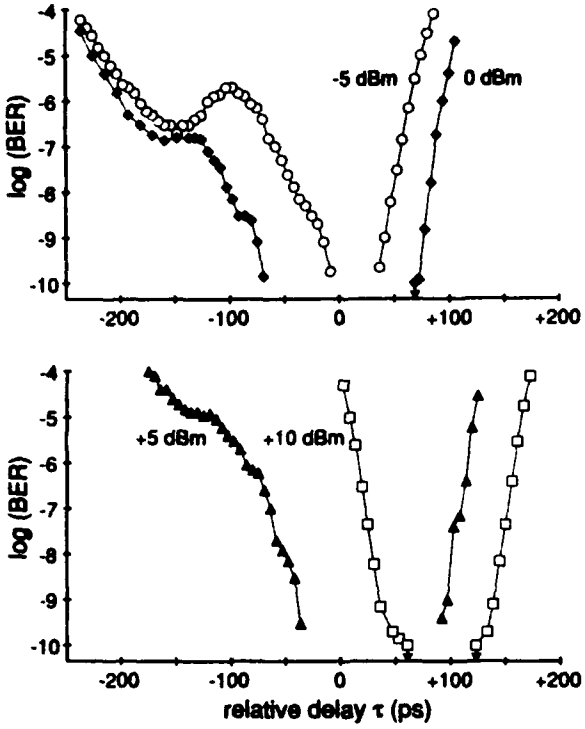

Fig. 4: Measured BER versus the relative delay τ between data pulse and clock pulse for the data pulse peak powers -5 dBm, 0 dBm, +5 dBm, +10 dBm

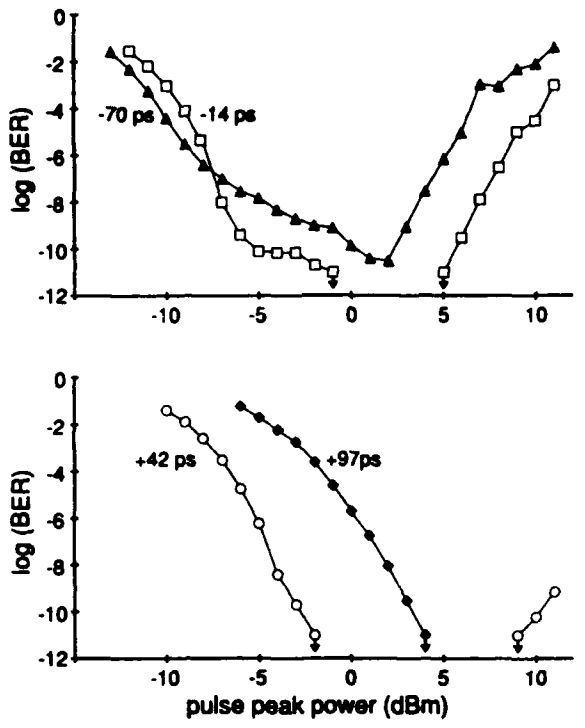

Fig. 5: Measured BER versus input data pulse peak power for the relative delays τ = -70 ps, -14 ps, +42 ps, +97 ps

In conclusion, a decision gate for all-optical regeneration based on a semiconductor laser amplifier in a loop mirror [SLALOM] configuration was operated at 1 Gbit/s. BER measurements revealed a retiming of data pulses at BER $< 10^{-9}$ within a 100 ps jitter range and within a 10 dB power range. The SLALOM based decision gate requires optical pulses having peak powers of about 1 mW corresponding to pulse energies of about 50 fJ. It is polarization independent for the data signal and enables simultaneously all-optical wavelength conversion over a wavelength range of about 60 nm.

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Photonic High-Speed Switching System

PWB 10:30am-12:00pm
Grand Ballroom East

Rodney S. Tucker, *Presider*
University of Melbourne, Australia

High-Speed Photonic Switching in Corporate Networks

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1. Introduction

The last decade has witnessed important advances in the area of optical communications. Unfortunately, technological progress has often outpaced system developments. Breakthroughs in wavelength conversion devices, high performance lasers, optical amplification, high-speed switching, and high-density optoelectronic integration have not always been matched by corresponding system applications [1-3]. As a result, optics remains mostly confined to the transport of information whereas switching and processing are still heavily dominated by electronics. Successful photonic switching applications will certainly for some time to come depend on both electronic and optical capabilities.

Traditionally, the development of photonic switching has been driven in large part by the requirements of the future broadband public network [4]. Optics aims there at handling extremely high throughputs in a centralized environment. The switching speed can be either relatively slow as in the case of cross-connects [5] or very fast as in the case of ATM switches [6].

In this paper, I want to show that interesting photonic switching applications exist in corporate networks as well. Indeed, first applications of modern multiplexing techniques such as ATM and optoelectronic technology may well take place in corporate networks. Such an evolution is supported by the rapid development of the corporate networking needs and the relatively high cost for the years to come of the transport bandwidth on the public network. Two application examples that have originated from our work in the European RACE program will illustrate the point.

2. High-Speed Corporate Networks

The term corporate network can be used to describe a wide range of private interconnection networks which can be very different in terms of capacity, number of users, and size. A commonly used description based on geographical coverage differentiates between local, metropolitan, and wide area networks (LANs, MANs, and WANs). Corporate networks support the exchange of information (data, voice, video, image) between business end-users. The goal of the network is to increase productivity and competitiveness. Cost as a consequence is a major design consideration.

To a large extent, voice and data still belong to different worlds. The two types of information often travel on separate networks, both within and outside corporations. The goal behind the evolution toward an integrated broadband communication network is precisely to integrate all services in a single network. This dichotomy has however not been resolved yet. For example data oriented networks like FDDI (fiber distributed data interface) and voice/transport oriented networks like SONET/SDH (synchronous optical network/synchronous digital hierarchy) do not share the same bitrate hierarchy. ATM holds the promise of integrating both worlds in an efficient fashion which would furthermore provide a seamless interface to the broadband public network [7-9]

The corporate networks' capacity requirements have steadily increased in the last few years. All indications show that this trend will continue over the years to cope with the development of applications, processing capabilities, and storage volumes [10,11]. Gbit/s type of networks will be needed in many instances. The success of a corporate networking strategy does not however solely depend on the sheer capacity. Aspects such as reliability, security, flexibility, maintenance, cabling, interfaces, equipment compatibility, and ultimately cost do play an important role as well. Various photonic network systems that can fulfil those needs have been devised. Interesting work, in particular, has been performed in the areas of wavelength-division multiplexing and spread-spectrum [12-15]. Technology complexity may however prevent an early implementation of such systems.

In the area of high-speed corporate networking, one can roughly identify two types of requirements. The first type of network interconnects a limited number of users (say 10) in a stable topology. The high capacity can be accessed almost in its entirety by one of the users. Transmission links are generally

dedicated to the network. Typical applications include distributed computing and medical image processing. The second type of network interconnects a large number of users (say 1000). The topology of the network changes often to adapt to the need of the users. Every user can only access a fraction, say 50Mbit/s, of the overall capacity. Transmission links can go through the public network. Typical applications include computer-aided design, multimedia applications, and work-at-home.

Below, I will briefly describe two TDM (time-division multiplexing) packet network concepts that address these requirements. The very high-speed optical loop (VHSOL) targets the first type whereas the corporate optical ATM transport (COAT) network targets the second type. In both cases, the optoelectronic interface lends itself well to integration which should facilitate near-term cost-effective implementations.

3. Very High-speed Optical Loop

The very high-speed optical loop concept [16] attempts to provide a solution to the best combined use of optics and electronics in an optical Gbit/s packet network. The ring shaped local area network connects broadband users through a single mode fiber (Fig. 1). The main originality of this network resides in the interconnection of users through passive access nodes (PANs). Each node, with the exception of one or several regenerators (REG), which share a lot of common features with the PANs, does not interrupt the optical flow on the ring; only a fraction of the available optical power is branched off at the PAN. The PAN is able to offer a full access as transmission is performed by a modulation by depletion scheme which writes information into "empty" packets containing cw (continuous wave) light. Information travels on the ring in fixed size packets. Headers contain synchronization, address, and access protocol information.

The VHSOL relies on optoelectronic integration (optical switches, waveguides, and detectors) [17] and brings advances in three areas. Firstly, a sharp reduction in the number of electrical-to-optical and optical-to-electrical conversions significantly reduces the weakness of conventional rings. In particular, jitter and electromagnetic interferences are decreased whereas reliability is increased. Secondly, a distributed power management on the loop allows an optimum use of the available optical energy. Less optical power is for example needed to interpret the header as to receive the data. Thirdly, optoelectronic processing at the access nodes allows synchronization and header interpretation with decision electronics operating at a speed which is roughly ten times slower than the loop bitrate. This is accomplished by using one or several optical switches as double-sided correlators [18].

Fig. 2 gives a typical PAN block diagram showing the access control and correlation switches as well as the synchronization and header interpretation paths. The optoelectronic correlation is performed on specially designed sequences for the synchronization and Hadamard code sequences for the address interpretation. A 1Gbit/s testbed has demonstrated the correlation process with specially designed optoelectronic devices. Custom designed GaAs circuits processed with a commercial foundry (Philips Microwave Limeil) onto specially prepared wafers have allowed the epitaxial lift-off implementation of fast front-end circuitry next to the integrated detectors [19].

4. Corporate Optical ATM Transport Network

The corporate optical ATM transport network concept answers the needs for broadband networking of end-users. We assume here two things. Firstly, that ATM will penetrate into corporate networks [8]. Secondly, that a large number of end-users will exist with individual bandwidth needs not exceeding a few tens of Mbit/s even if provision is made for paths up to 620Mbit/s. Corporate end-users located in a small geographical area like a building or a floor will be interconnected by a fully electronic ATM Hub switch through short (say up to 100m) copper lines. First versions of these ATM Hubs can already be found on the market. Twisted pairs provide an economical and perfectly adequate way of linking 150Mbit/s users to the Hub in a star topology [20]. Intense efforts in the ATM electronic switching area guarantee the future availability of relatively large Hubs operating at speeds ranging from 45Mbit/s to 620Mbit/s [21]. Target costs lie in the range of $1000 per terminal adapter card and $1500 per Hub port.

The ATM Hubs are in turn interconnected through a highly reliable high capacity fiber network as shown in Fig. 3. If a large portion of the traffic flows between users connected to the same Hub, an aggregate capacity in the order of a few Gbit/s will be needed to interconnect the Hubs. Access nodes (Fig.4) will interface the ATM Hub to the fiber network. Here, optical switching can make big contributions allowing enhanced reliability (for example by providing very high-speed fail-safe bypass switching), simplified

demultiplexing (for example with integrated optical demultiplexers requiring only the precise synchronization of the head switch), and efficient synchronization schemes (for example based on the optoelectronic correlation scheme developed for the VHSOL).

In all cases the goal is to combine high-speed integrated optics with low-speed parallel electronics. Unfortunately, the standard ATM cell format consisting of 53 octets is not very suitable for high-speed optoelectronic processing. The fiber network will transport bit-interleaved channels consisting of concatenated 64 octets cells encapsulating full ATM cells. ATM data rates are chosen so as to match the SDH hierarchy, which would mean a 3Gbit/s gross bitrate for STM-16 compatibility. Only a fraction of the Gbit/s capacity will be dropped or added at the access node. Typically 150Mbit/s to 620Mbit/s will be exchanged between the Hub and the fiber network at the access node. Single fiber attachments such as shown in Fig. 4 can be stacked to form multiple fiber access.

5. Conclusion

Economics dictates that electronics be used where it is cheaper. On the other hand optics should be used where it makes sense such as in the transport, access, and protection areas. At the present time, a market pull and a system (ATM) and technology push is being felt that should facilitate the introduction of photonic switching in the corporate networking world. First generation implementations will probably rely on TDM systems whereas second generation systems will complement the time dimension with wavelength dimension in order to increase the network capacity substantially.

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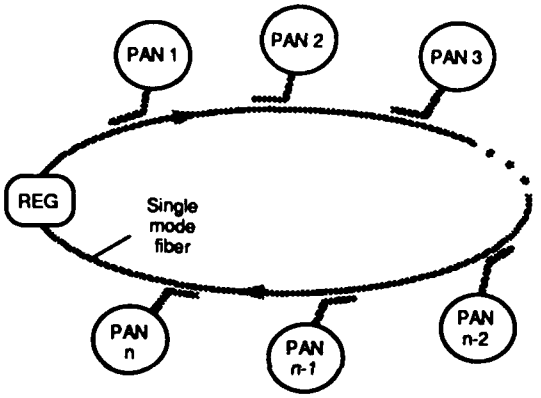

Fig. 1. VHSOL Ring.

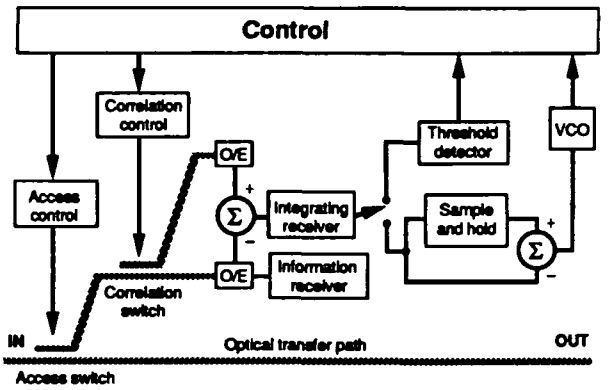

Fig. 2. Simplified PAN architecture.

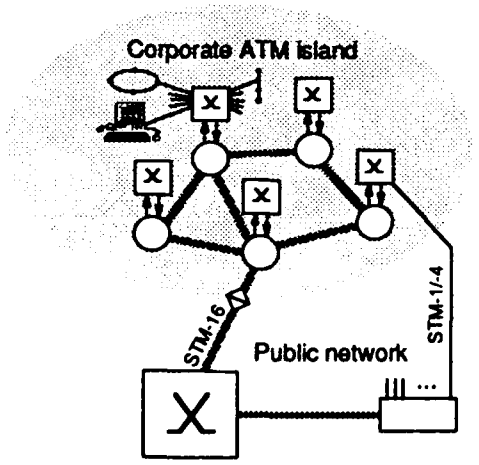

Fig. 3. Optical ATM corporate transport network.

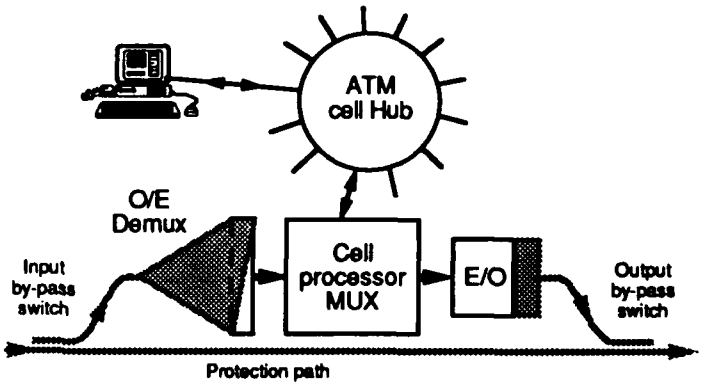

Fig. 4. Access node schematic diagram.

Optical Add/Drop Multiplexing for Cell Switched Networks

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Very high-speed optical networks with fixed-length cells at the physical layer, form the basis for a number of promising network architectures that have the potential to provide voice, data, and video services; asynchronous transfer mode (ATM) switching and the distributed queue dual bus (DQDB) are important examples of current fixed cell length network implementations. While these networks use the optical link to provide connectivity between nodes, with all switching being performed electronically, it is interesting to consider derivative networks that use optical switching (in conjunction with electronic switching) to improve performance. In this paper, we discuss the experimental and theoretical performance (bit error ratio, insertion loss, clock recovery, and jitter) of one such network in which fixed-length optical cells are inserted or removed from a ring or bus. Add/drop multiplexing in the optical domain [1-5] removes the requirement for optoelectronic regeneration, and store and forward of data, at every node in a network; it thus reduces latency, and is synergistic with the introduction of optical amplifiers into wide area and metropolitan area networks. Moreover, the physical layer protocol described in this paper avoids the electronic bottleneck associated with header processing at each node, and thus may lead to networks in which the data transfer rate approaches the (≈10 Gb/s) link transmission rates that can be obtained easily using conventional lightwave technology.

The physical layer protocol used for this work [3] uses a low bandwidth header which is placed on an electrical subcarrier above the baseband frequency content of the cell payload. The control header and the payload occupy the same time slot, and are transmitted simultaneously (Figure 1). Conventional nonreturn to zero amplitude shift keying is used to modulate the payload, while bipolar phase shift keying is used to modulate the header because of increased receiver sensitivity at very little expense in receiver complexity. At the input to the node (Figure 2), $(k\text{-}1)\%$ of the optical signal is tapped from the bus; the baseband portion of this tapped signal is used to recover the clock of the payload channel (the node must retain payload as well as header clock synchronization), while the cell address is decoded from the demultiplexed header. The untapped $k\%$ portion of the signal is delayed by a loop of fiber to insure that the cell header has been decoded and the switch state set prior to the arrival of the packet. As described below, the optimum modulation depth for the payload and header, and tapping ratio at the node input, depend upon the ratio of the bandwidth of the header (B_h) to the bandwidth of the payload (B_p), while the delay introduced by the fiber loop depends upon the sum of the cell length and the address decoding time. For the experimental demonstration of this node, cell payloads of 128 octets at 2.56 Gb/s were combined with headers of 2 octets at 40 Mb/s. Approximately 100 m of fiber was used to generate a 500 ns delay of which 400 ns was due to the cell length, and 100 ns was needed to decode the cell header using ordinary TTL logic. Header electronics for establishing node-to-node communications for a three-node system were fabricated based on a commercially available chipset for implementing FDDI; the header channel is placed on a 3 GHz subcarrier, which is sufficiently separated from the baseband channel in frequency to prevent crosstalk or distortion. The baseband payload generation was provided using a bit-error-rate (BER) transmitter.

A very high-speed optical network using optical add/drop multiplexing can be configured with multiple network access nodes as shown in Figure 3. A potential disadvantage of this network, compared with a conventional network (employing optoelectronic regeneration and electronic switching at all nodes), is the decrease in optical signal strength as a cell traverses many nodes. This optical loss is caused by two sources: tapping a portion of the signal prior to switching in order to read the header and maintain the payload clock, and an inherent penalty caused by dividing the optical power from the transmitting laser between the payload and header channels. Assuming that the acceptable BER for the packet header and payload are both 10^{-9}, and a total laser modulation depth of 1, the amount of signal tapping that gives the optimum (lowest) value for insertion loss occurs when $m = k$ (where m is the modulation depth devoted to the baseband payload), and is given by $m = k = \left\{1+\left(\frac{B_h}{2B_p}\right)^{1/4}\right\}^{-1}$. The effective insertion loss (again, compared with a conventional baseband system with regeneration at each node) can be calculated as -20 log(m) [dB]. Figure 4 shows a plot of the optimum insertion loss as a function of B_h/B_p. As the data rate of the header approaches the data rate of the payload, more light is needed to read the header. Consequently, both the modulation depth of the header and the amount of light tapped from the bus to read the header need to be increased, and the insertion loss becomes higher. Conversely, as the network overhead becomes smaller ($B_h << B_p$), the protocol becomes more efficient, and the insertion loss becomes smaller. For the parameters used in the experimental configuration discussed above (B_h = 40 Mb/s, B_p = 2.48 Gb/s) the measured and theoretical optimum insertion losses were 2 dB and 2.3 dB respectively, while the measured and theoretical optimum values for m and k were 80% and 77% respectively. For an ATM or DBDQ cell, B_h/B_p = 5/48, and the theoretical insertion loss equals 3.2 dB. For reasonable network overheads ($B_h/B_p < 0.1$), the insertion loss remains less than 3 dB, implying that semiconductor optical amplifiers monolithically integrated with 2 x 2 space division switches could be used to overcome protocol and component insertion loss, forming an optical add/drop multiplexer photonic integrated circuit. Figure 5 provides the experimental BER performance of the node for two different values of m and k, showing that the network performance is optimized when $m = k$. BER measurements with/without the presence of payload/header channels confirmed that there was no measurable penalty induced by crosstalk between header and payload channels.

In summary, the performance of a network that implements optical add/drop multiplexing of fixed-length, optical cells has been theoretically and experimentally investigated. This network show great promise for providing high speed services with data throughputs approaching the data transmission rate.

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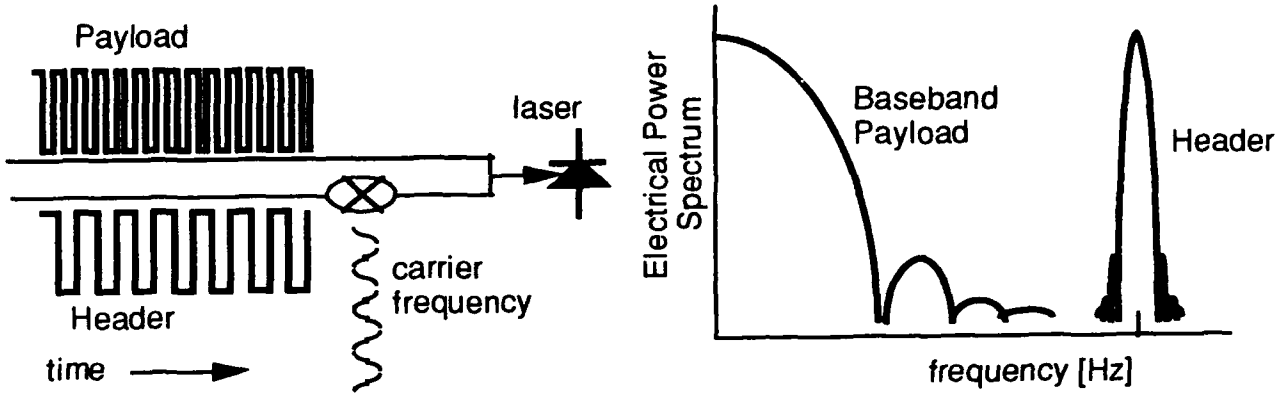

Figure 1 - Time domain and frequency domain pictures of cell with baseband payload and control header multiplexed on an electrical subcarrier.

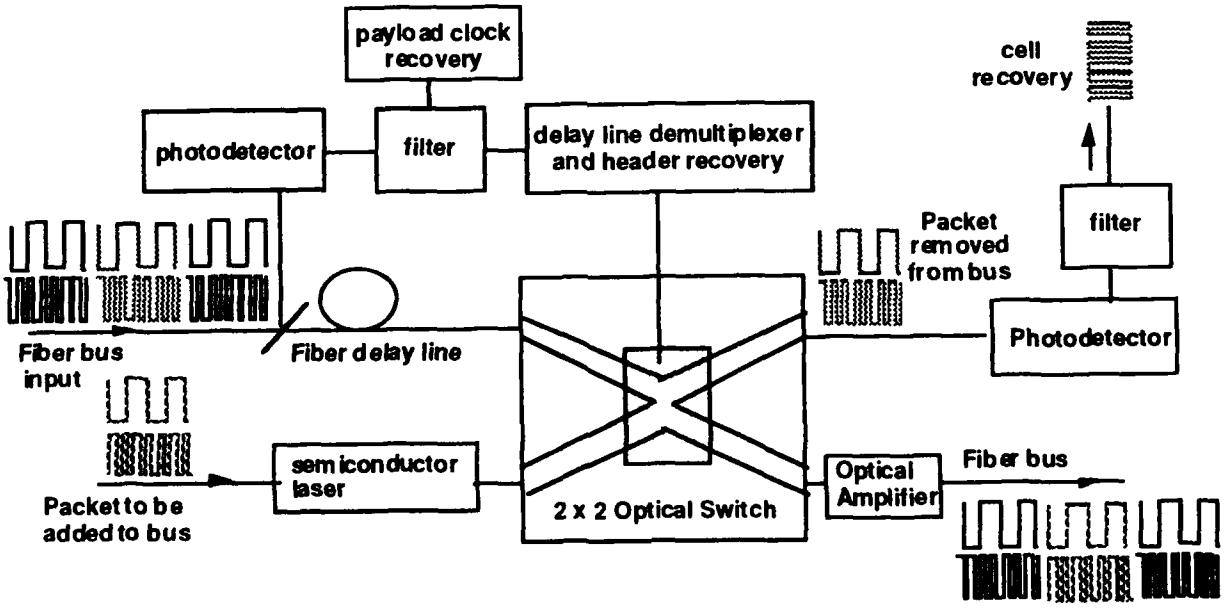

Figure 2 - Experimental configuration of optical add/drop multiplexer node showing a cell being optically switched from the fiber bus, and a replacement cell being inserted into the vacant slot.

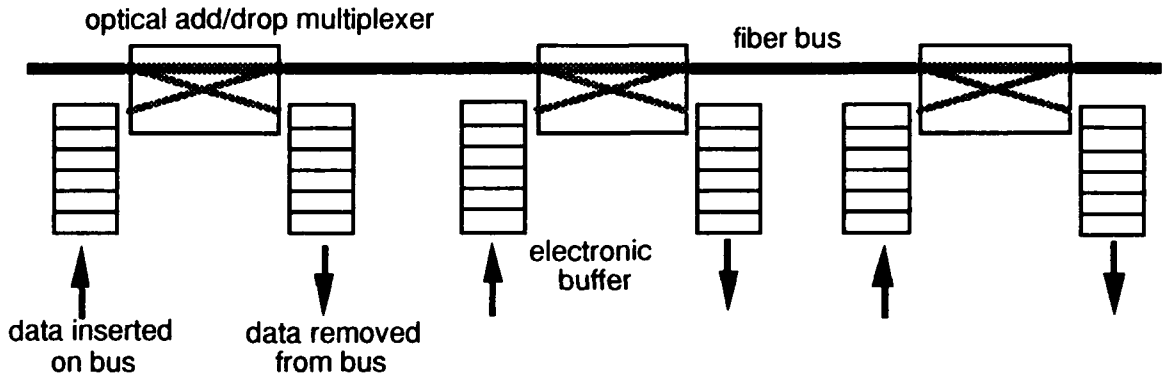

Figure 3 - Cell switched fiber bus using optical add/drop multiplexers

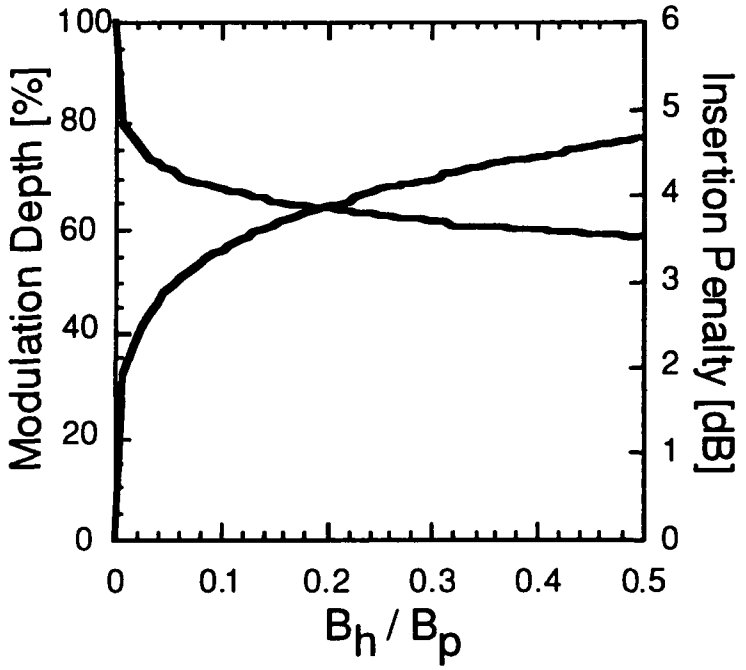

Figure 4 - Optimum modulation depth (m) and insertion loss as a function of header/payload bandwidth (or data rate).

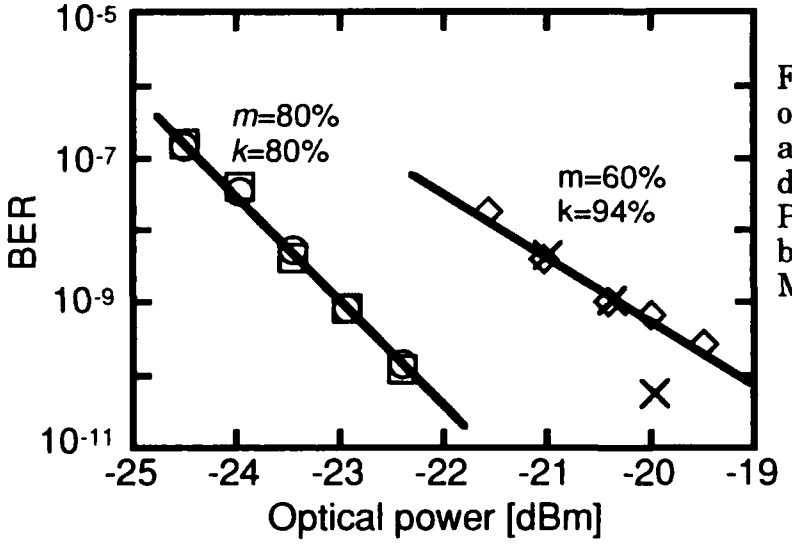

Figure 5 - BER vs. total received optical power (header+payload) at the input to the node for two different sets of values for m,k. Payload at 2.56 Gb/s represented by □ and ◇. Header at 40 Mb/s represented by ○, and ×.

A PHOTONIC TIME-DIVISION SWITCHING EXPERIMENT

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ABSTRACT

An experimental switching system is being designed and built for interconnecting broadband circuits through a photonic time-multiplexed switching network under DEFINITY® Communications System call control. The system is called DiSCO, for Distributed Switching with Centralized Optics. The DiSCO system is designed to switch broadband voice, data, and video calls over time multiplexed network paths through a guided-wave photonic network. The photonic network paths are transparent to data and are thus independent of transmitter and receiver bit rate. They are formed by linking together one or more Universal Time-Slots each capable of continuously transporting between 64 Kbps and 3 Mbps of voice, data or video signals. DiSCO's Time-Space-Time system architecture, the photonic broadband switching application, and its Cross-Talk Avoiding switching network topology are well matched with the emerging lithium niobate guided-wave directional coupler and digital optical switch technologies. The DEFINITY System architecture and technology platform is being used and extended in a natural way to implement this experimental system. While this gives the prototype a "production quality" appearance, this should not be taken as an indication that DiSCO will be offered as a commercial product.

SYSTEM ARCHITECTURE

The DiSCO prototype system features a modular Time-Space-Time architecture, distributed control, and transparent channels that extend earlier work.[1] DiSCO switches its inter-module control messages, data calls and video calls over transparent network paths in its photonic switching network.

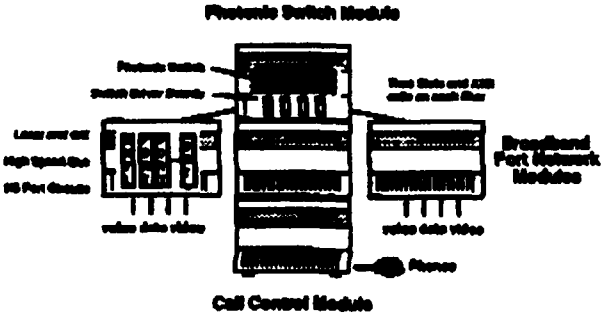

Figure 1. The DiSCO Prototype Architecture

In Figure 1, an 8-by-8 photonic switch module is shown interconnecting the three electronic broadband port network modules shown in the row directly below it. A standard DEFINITY System processor module is shown at the bottom, co-located with the middle broadband port network module. Each of the broadband port network modules is connected to the photonic switch module by a pair of one-way single-mode optical fibers. Data remain in serial optical form from the transmitting module's up-link to the receiving module's downlink.

The photonic switch module is a Time Multiplexed Space Switch (TMS) that is reconfigured for each 488 ns. time-slot in a pattern that completely cycles during each 125 µs. frame. At the front of the photonic switch module are the driver boards holding the electronic drivers that control the photonic crosspoints.

Each broadband port network module consists of an optical transmitter, an optical receiver, a parallel high speed transmitter bus, a parallel high speed receiver bus, a module controller board (MC), and a variety of high speed port circuit boards. Port boards are shown in Figure 1 that could interface with a variety of high bit-rate voice, data and video terminals. In the current program, video interface boards are being built that will use multiple time-slots to transmit and receive standard D1 digital RGB video signals at 216 Mbps. Other boards could be added later for transmitting and receiving 1.5 Mbps data or compressed video signals while using only one time-slot per two-way connection.

One broadband port network module is always co-located with the DEFINITY System call control module. The module-control board (MC) in this co-located broadband port network module is designated the "master" module-control board. It coordinates the actions of the other broadband port module controllers by exchanging data through the fibers when it is directed to set up a broadband call by the DEFINITY System call control module. The master module-control board also does the path hunt and controls the driver boards in the photonic switch module.

The DEFINITY System control module controls DiSCO by directing the master module-control board to set up and tear down broadband calls. The control module is also responsible for setting up conventional voice and data calls between its standard ISDN terminals, DCP terminals and analog voice telephones.

This style of photonic switching uses guided wave switches operating under electronic control. Guided wave optics has the advantage of relatively low optical loss. Therefore optical signals can traverse DISCO without needing regeneration. The throughput data rate can be much greater than the switching speed of each device. This gives rise to the concept of *Universal Time-Slots*.

TIME-MULTIPLEXED PHOTONIC SWITCHING

Universal Time-Slots

The digital electronic back-plane of each broadband port network module has two parallel 32-bit buses that transport asynchronously generated time multiplexed signals. With 8000 frames per second and 256 time-slots per frame, each time-slot lasts 488 ns. The hierarchy of this time structure is illustrated in the top two levels of Figure 2. In every time-slot, each bus can transfer as few as 8 bits for a traditional 64-kbps digital voice channel, or as many as 384 bits for part of a video or B-ISDN call.

In most electronic time multiplexed systems, all of the input and output signals are strictly synchronized at the bit level. In this photonic time multiplexed system, the signals in each time-slot are generated and received asynchronously at extremely high bit rates. Only one transmitter and one receiver will usually need to be concerned with coordinated bit level synchronization. This is possible because the photonic TMS switch fabric does not know nor care what is being transmitted within each time-slot. Time-slots created with this useful data transparency are called *Universal Time-Slots*.

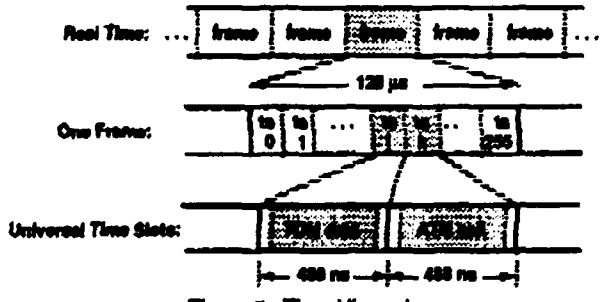

Figure 2. Time Hierarchy

Operation of this research model requires that frames and time-slots be synchronized in all 8 modules and in the TMS. Digital bursts of voice and video data are launched from each module to arrive within the *data* band of each time slot. The arrival of voice and video data is represented pictorially in the fourth line of Figure 2. A *guard* band is maintained at each time slot boundary to compensate for time slot misalignment.

Delay Synchronization

System operation requires that frames and time-slots received from up to 8 broadband port network modules be in synch at the photonic TMS. Digital bursts of voice and video data must be launched from each module to arrive within the *data* band of each time-slot. The arrival of voice and video data is represented pictorially in the fourth line of Figure 2. A *guard* band is provided at each time-slot boundary to provide for time-slot misalignment and switch reconfiguration time.

The frame and time-slot boundaries of each broadband port network module will be shifted in phase from the frame and time-slot boundaries of the photonic TMS. This phase shift must be monitored and dynamically adjusted by the system to compensate for the distance between each port network module and the switch module. This adjustment must continuously compensate for the transmission delay of each fiber link. This delay will vary noticeably with changes in fiber temperature, stress, etc. while the system is operating.

Time-Slot Synchronization

Since each kilometer of fiber corresponds to a delay of approximately 10 time-slots, the skewing of time-slot processing between different parts of the system can be substantial. A given frame in the high speed transmitter bus of a port network module will generally be several time-slots ahead of the corresponding time-slot at the photonic TMS. Likewise, each time-slot at the TMS will generally be several time-slots ahead of the corresponding time-slot on the high speed receiver bus of the port network module.

The bookkeeping and coordination required to keep port modules in synch can be complex, especially during multimodule multiparty calls.

Bit Synchronization

In standard fiber optic transmission systems, a transmitter is linked to the same receiver for a relatively long time. At the start of transmission a phase locked loop locks on to the transmitter data rate and creates a clock signal for reading out the data that follows. The lock-in time required by these circuits is short by message length standards, but relatively long by time-slot length standards. In this application these circuits must lock in within nanoseconds to keep the guardband short.

Switch Rearrangement Synchronization

In setting up new paths between broadband port networks, occasionally there is a need for rearranging existing calls to align free time-slots without creating any "break" in service. A simultaneous "cut" to a new system configuration during a designated time-slot is actually a staggered movement with

respect to real time. This requires the careful coordination of broadband port network modules

All of these time-slot, bit, delay and rearrangement synchronization issues are dealt with in the broadband port network modules. Each broadband port network module controller must be responsible for monitoring and adjusting delay and phase differences to insure that signals are synchronized at the photonic TMS. Programmable control chips are being designed that will gate signals in and out of every broadband port network circuit board. Frame memory shift registers are included to perform the required buffer and burst functions.

Adaptive Threshold Signal Detection

Each port network receiver expects to receive signals from different laser transmitters during different time-slots. Thus each receiver must be capable of adapting quickly to substantial jumps in phase and amplitude at time-slot boundaries. The signal detection threshold must be capable of being reset during each guardband and must quickly adapt to the optical power level of each new signal. Again, standard approaches would not respond quickly enough to insure proper system performance.

PHOTONIC SWITCH TECHNOLOGY

Lithium Niobate Guided Wave Directional Couplers

Lithium niobate directional couplers permit rapid switching of optical signals without reconversion into an electrical form. Single mode waveguides with high refractive indices are produced by diffusing strips of titanium into a $LiNbO_3$ crystal (see Figure 3). A refractive index change occurs when a voltage is applied across these guides due to the high electrooptic coefficient of $LiNbO_3$. This results in a change in the cross coupling between guides allowing optical power to be switched from one guide to the other.

Lithium niobate couplers can be switched in nanoseconds and can readily carry Gigabit data rates. In the DISCO prototype, up to 384 bits will be sent in each 488 ns time-slot at a burst rate of approximately 1 Gbps.

Most of the currently available Lithium Niobate guided wave couplers are inherently analog. Historically this resulted in drive and bias voltages that were individually tuned to prevent excessive crosstalk between network paths.

These devices also require that the input optical power appears at the substrate with TM polarization. Each stage of switching, when averaged over many stages, yields approximately 1.7 dB loss. Substrates fabricated on a 4 inch wafer can physically accommodate only 3 to 4 stages of switching (i.e. each path through the network can only pass through a sequence of 4 couplers on each substrate.)

While these problems continue to be dealt with individually, the approach being taken in the DiSCO prototype is to solve the crosstalk problem so completely using a crosstalk avoiding network topology that most of the other problems become easier to deal with at the device level. This architectural solution is called the Dilated Benes Network (DBN).

Having made this decision, the problem of drive voltage variation has been accommodated by building a fast analog driver circuit for each individual coupler. The substrate size limitation has been extended by butt-coupling two substrates within the same physical package. The optical loss through the couplers is accommodated by choosing a TDM switching application that readily exploits a relatively small network. The polarization issue is dealt with using a technique called Polarization Diversity.

Polarization Diversity

The second easiest way of dealing with the polarization constraint is to provide a brute force system architecture solution analogous to the brute force crosstalk solution of dilation. In the polarization diversity approach, the TE and TM polarizations are separated, switched separately, and then recombined. Using this approach, two 8-by-8 dilated Benes networks placed side by side on the same substrate could be used to emulate a truly polarization independent switch.

We expect this solution to be feasible for currently interesting transmission rates and to provide a robust vehicle for demonstrating the technical feasibility of photonic time division switching.

PHOTONIC NETWORK TOPOLOGIES

A number of different network topologies can all be implemented using either 2-by-2 guided wave couplers or 1-by-2 digital optical switches. Assuming 2-by-2 guided wave couplers are used, the total number of switching elements required for implementing each network topology is shown in Figure 6 below.

For a 4-by-4 switch built by using a lithium niobate substrate pair, it is relatively easy to implement a number of different network topologies. As one moves to 8-by-8 and 16-by-16, things become more difficult. At 32-by-32 one clearly moves to multiple packages for either of the non blocking network topologies.

In the time-multiplexed switching application, non blocking behavior can be achieved by using a rearrangeably non blocking network. Variants of the Benes network are appealing since the number of stages of 2-by-2 switching elements (beta elements) required is only $2Log_2N - 1$. The total number of switching elements is only $(N/2)(2Log_2N - 1)$.

The Dilated Benes Network (DBN) described below requires $2Log_2N$ stages of switching elements. Two of the stages are 1-by-2 switching elements and $2Log_2N - 2$ of the stages are 2-by-2 switching elements. The total number of switching elements is only $2NLog_2N$.

Dilated Benes Network

The 8-by-8 switching network depicted in Figure 3 is built from 48 guided wave couplers that operate as 2-by-2 switches. The *dilated Benes* topology consists of one column of 8, 1-by-2 switches on the left and right edges. Its 4 internal columns contain two separate 8-by-8 Benes networks with their middle column deleted. It is rearrangeably non blocking.[2]

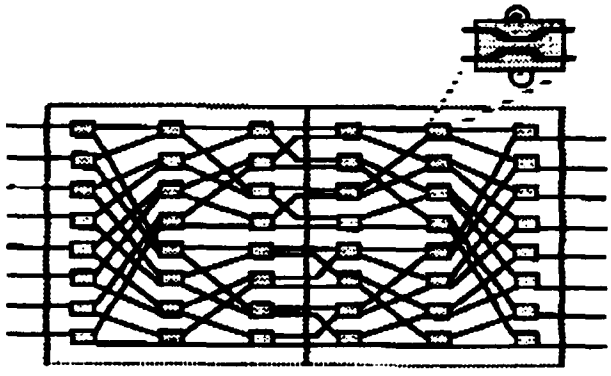

Figure 3. 8-by-8 Dilated Benes Network

This topology is both low loss and crosstalk avoidant. The optical path loss is low because there are only 6 columns of couplers. Crosstalk is avoided by expanding or *dilating* the network in the vertical direction to guarantee that only one active signal need appear in each coupler at a time.[3] With cross talk taken care of by a crosstalk avoiding architecture, problems of polarization and voltage drift were easier to address at the device level.

An array of 24 directional couplers was integrated onto each substrate of Lithium Niobate. Two identical chips were butt-coupled along the middle line to make the complete 8-by-8 dilated Benes network.

SUMMARY

Several interconnection networks will be evaluated for use in a photonic time multiplexed switching (TMS) application. The DiSCO with the DEFINITY System applications require circuit switching and packet switching but not large connectivity or ultra-fast switching speeds. These requirements match the characteristics of lithium niobate guided wave coupler and optical digital switch technology well. This program examines practical solutions to the previously reported problems of high loss, high crosstalk, and sensitivity to polarization and bias voltage drift. In this application network architectures are being chosen that reduce both optical loss and crosstalk at the system level to the point where problems with polarization and voltage drift can be successfully addressed at the device level.

Instead we have chosen to focus on the TMS application. We are evaluating three implementation options from the standpoint of technical feasibility, performance, system complexity and ultimate cost.

Research issues center around adapting the concept of Time Multiplexed Switching to the photonic domain, maintaining data transparency (and therefore flexibility) in the photonic switch module, and characterizing various near and long term solutions for exploiting the guided wave switch technology. All of these photonic switches are designed to be transparent to data rate below some maximum value. Thus adjacent time-slots can carry dramatically different signals. Voice, data and video synchronous and asynchronous signals can all be carried in one integrated photonic switching network.

ACKNOWLEDGEMENTS

The DiSCO experiment has come this far due to the tireless efforts and keen insights of many people. Special thanks are due to the current DiSCO team members: John Camlet, Jr., Don Shugard, Rich Thompson, Saul Einbinder, Amanda Kao, Walt Pitio, Bob Pritchard, Jitendra Sharma, and George Shevchuk. Special thanks for technical contributions are also due to; Rod Alferness, Jim Ferenc, Bill Fisher, Fred Heismann, Paul Henry, Keith Honea, Bill Minford, Ed Murphy, Tim Murphy, Arun Netravali, Kevin Oye, Yusuka Ota, and Mario Santoro. The strong management support of Kevin Oye, Jeff Iapicco, Pete Kusulas, Phil Anthony, Paul Henry, Rich Gitlin, Ilan Levi, Bob Lucky, and Arno Penzias has been essential.

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Experimental Results for Fast, High-Capacity Optical Switching Architectures

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K.S. Man & I.M. Burnett, BT Laboratories, Martlesham Heath, Ipswich, UK

Introduction

With the trends towards provision of broadband services, there will be an increasing requirement for high throughput and capacity in switch fabrics. Capacity gains can be achieved through exploiting the spectral bandwidth of optical switches. Additionally, the time and space domain can be exploited to give multidimensional switching[1]. Applications for such flexible switching lie in signal processing or fast-switching within the telecommunications network. Recently, interest has been growing in packet-based systems such as ATM. These systems require the header content of the cells to be interpreted, and used to route the cells. The control functions of such systems are best implemented using electronics, but optical switching can provide a high capacity and flexible interconnection medium.

This paper describes optical switching experiments carried out using a modular testbed developed under the European RACE OSCAR (R1033) programme. These experiments have explored the use of wavelength multiplexing in synchronous optical switching; firstly to increase capacity and secondly, to provide selective routing of a control channel. This selective routing was used to transmit the data and header content of cells separately.

Modular Testbed

The aim of the testbed was to provide a system capable of rapid reconfiguration for experiments. Lithium niobate and indium phosphide optical switches used in the testbed were packaged and mounted onto Eurocards. These cards could then be used interchangeably in the rack system, providing a technology-independent testbed. Standard SC optical connectors mounted on the front panel were used to access the switches. The testbed proved robust, and was successfully transported to exhibitions at the European Conference on Optical Communications (ECOC) in 1991 and 1992.

Wavelength Multiplexed Switching

These experiments demonstrated that the data throughput of an optical switching system can be expanded by using wavelength-multiplexed data. The key to such techniques lies in the wide spectral bandwidth of optical switches. The measured -3dB bandwidth of the 1x16 Lithium Niobate switch used in the experiments was of the order of 100nm. One way to exploit this bandwidth would be to use narrow linewidth sources such as DFB lasers; for example, over 50 switched channels could be provided with sources at a wavelength spacing of 2nm.

The basic switch fabric used for the experiments was an optical time multiplexed space switch architecture proposed [2]. Fast synchronous byte switching was demonstrated at 622 Mbit/s with no significant power penalty [3]. The capacity of this switch fabric was expanded by the use of wavelength multiplexed channels, closely spaced in the 1300nm window [4]. Each channel was modulated at 622Mbit/s for a distinct sequence of eight bytes, with switching taking place in the guard band. A BER of less than 10^{-9} was achieved, for a received optical power of less than -32dBm. There was no significant receiver power penalty (<0.2 dB) due to crosstalk for adding in a distributed optical clock at a wavelength of 1500nm.

Packet Switching

In addition to providing capacity expansion, wavelength can also be used for the intelligent routing of information channels. For example, a unique wavelength can be selected from a multi-wavelength data stream using wavelength demultiplexers or filters, and then routed to its required destination. This selective routing technique can be exploited in packet switching for separate transmission of the data and header content. In data packets, the header is usually smaller than the payload; therefore, the header information could be transmitted in parallel with the payload data and at a lower bit rate. By transmitting the header and data separately, the speed and complexity of the control electronics is reduced, permitting the use of standard header recognition circuitry. In this set of experiments, the feasibility of packet switching of signals in the Gbit/s domain was demonstrated by using a wavelength multiplexed control channel. In this way, the advantages of optical switching in terms of its high capacity and flexibility can be combined with the logic functionality of electronics.

The data and header content of ATM-size packets was transmitted on separate wavelength channels at two different data rates (Figure 1). These channels were multiplexed together over an optical link and then demultiplexed. The low data-rate control channel was transmitted on the 1550nm wavelength at a rate of 155 Mbit/s. (The effective data-rate, however, was 45 Mbit/s as only a portion of this data channel was needed to transmit the ATM format header). The routing address contained in the header was decoded by the ATM controller electronics into switch control instructions, and the appropriate TTL signals were output to the switch. The high data-rate packet information was transmitted on the 1300nm wavelength, and then routed through a 1xN optical switch fabric. Experiments were carried out at bit-rates of 622 Mbit/s and 933 Mbit/s; the upper bit-rate was determined by the availability of suitable test equipment, rather than any constraints of the switch fabric. Electronic and optical delays were incorporated into the system in order to synchronise the header and data information at the switch, and ensure that switching took place within the guard band.

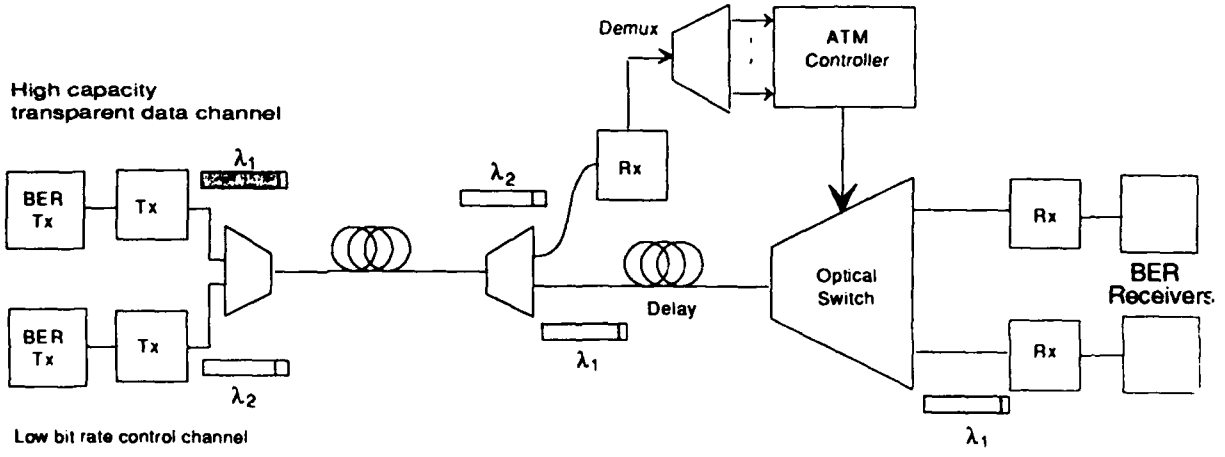

Figure 1: Experimental layout for packet switching

Packet switching was successfully demonstrated using a variety of technologies including a 1x4 Indium Phosphide switch (produced by ETH in Zurich) and a 1x16 Lithium Niobate switch [5]. Figure 2 shows two switched outputs using the 1x16 Lithium Niobate switch, using a switch control pattern of AAAB i.e. one packet of data is switched to output A and three packets are switched to output B, in a continuous sequence. Figure 3 shows the bit data within two switched data packets.

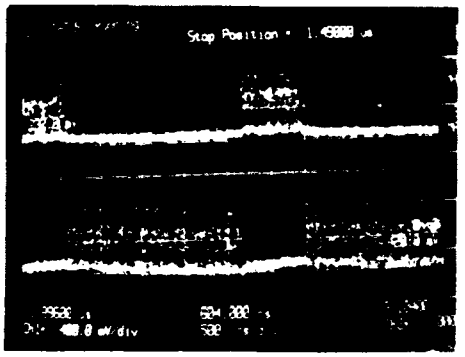

Figure 2: 622 Mbit/s data packets switched in a ABAA control sequence to two output ports of a 1x16 Lithium Niobate switch

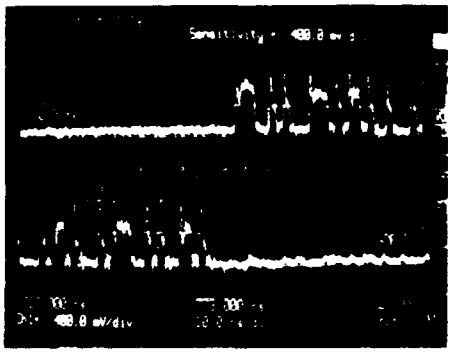

Figure 3: 622 Mbit/s data being switched using a 1x16 Lithium Niobate switch

BER measurements were made of the system by inserting an optical attenuator into the data path to the switch, and using a BT&D pinFET receiver. For the 1x16 Lithium Niobate switch, the receiver sensitivity was measured to be better than -28.5 dBm for a BER of less than 10^{-9} at bit-rates of 622 Mbit/s and 933 Mbit/s. For the 1x4 Indium Phosphide switch, the receiver sensitivity was measured as better than -30.5 dBm for a BER of less than 10^{-9} at a bit-rate of 622 Mbit/s (Figure 4). Using a 2x2 Lithium Niobate switch in a 1x2 configuration, the receiver sensitivity was found to be better than -28.5 dBm for a BER of less than 10^{-9} at bit-rates of 622 Mbit/s and 933 Mbit/s; this accords with the results measured for the 1x16 Lithium Niobate switch.

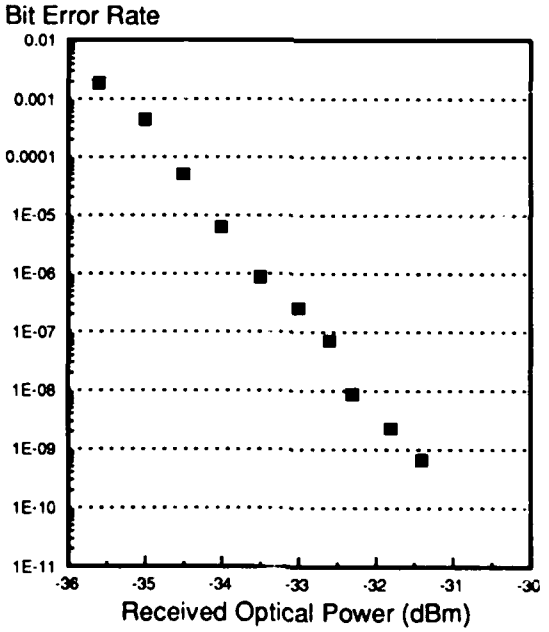

Figure 4: BER curve for packet switched data at 622 Mbit/s using a 1x4 Indium Phosphide switch

Discussion

These experiments have shown two ways in which wavelength can enhance switching performance within optical networks. Firstly, to increase capacity; secondly, to selectively route the header and payload content of cells in a packet-switching system. Cell-routing of data packets in the Gbit/s range has been demonstrated, but the potential exists for much greater capacity gains. This could be achieved by combining the enhanced data capacity offered by wavelength-multiplexing with the novel data/header separation technique. In this way, several wavelength-multiplexed streams of packet data could be switched simultaneously. This would give a packet network with a capacity well into the multi-Gbit/s regime. The rationale for such a system is that relatively low-speed control electronics could be used; therefore the costs per switched Gbit/s could be much lower than a comparable all-electronic system of the same capacity.

An application for such a high-capacity packet network would be for providing interconnection between users of very high bandwidth services (e.g. Image processing, supercomputing, video conferencing). The network could be upgraded in capacity by the addition of more wavelengths. Separate optical filters or wavelength multiplexers could be incorporated to route data channels based on wavelength-coded locations. This would provide a flexible, and easily reconfigurable network. Clearly, to exploit such a system fully requires careful consideration of the overall switch architecture, the way in which space and wavelength switches are integrated together and associated contention issues such as resolution.

Conclusions

This demonstration has proved the principle that the data and control paths can be decoupled for optical packet switching using a 1xN switch configuration. ATM length cells have been routed at 622 Mbit/s and 933 Mbit/s using a range of optical switch technologies. The use of such a technique minimises the speed and complexity of the control electronics whilst maintaining a high switched data throughput. Previous experiments have demonstrated the optical switching of wavelength-multiplexed data channels. Routes have been explored towards upgrading the packet switching system by using additional data channels multiplexed on closely spaced wavelengths. The combined use of electronics and optics in this way could lead to potential cost reductions, as well as providing a flexible switching system.

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Networks and Switching

PWC 1:30pm-3:10pm
Grand Ballroom East

David A. Smith, *Presider*
Bellcore

Sparsely-Filled Densely-Wavelength-Division-Multiplexed Networks

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INTRODUCTION

It has been clear for some time that optical fibre transmission systems have the potential to carry vastly greater amounts of traffic than they are currently used for. For example, in Fig.1, we show typical values for the insertion loss of a 50km fibre section in the 1500nm window and overlay it with an approximate representation of an Erbium Doped Fibre Amplifier (EDFA) gain spectrum. The combination promises transparency over a spectral window of about 35nm width, corresponding to a spectral bandwidth of approximately 4700 GHz. Dispersion in the fibre seems likely to limit the data rate transmitted over long distance circuits (say 1000km) to the region of 1Gbit/s unless optical equalisation techniques are employed or special low dispersion (dispersion shifted) fibres are employed. Moreover, it is clear that at the terminations of any long haul system, the signals will be reconverted to electrical form. Two questions have thus presented themselves to us. How can this awesome potential of the fibre be better used and, at the same time, how can such higher capacity signals be routed and distributed through a complex multinode network in a flexible manner without returning them to the electronic domain? This latter question raises key points about how the signals will be multiplexed in the optical domain.

PROPOSED NETWORK

We believe that many proposals to implement Photonic systems in switching suffer from the relatively fundamental problem that they involve breaking into time-multiplexed data streams at the switch, disassembling many such streams and reassembling them at the output prior to onward transmission. This arises but it has been traditional to time multiplex to the highest level possible electrically and in turn, this has led to blocks of data that frequently require partial disassembly at a node. This fundamentally involves having the optical switching element operate in time synchronism with the signal and generally implies complex electronic control. It also implies the use of buffers to time-align incoming data streams from different sources and fundamentally limits the capacity of the optical carrier to the data rate that can be conveniently accessed electronically, thus severely limiting the attraction of the optical medium.

If we arbitrarily assume that data will be electronically multiplexed to a level in the SDH heirarchy in the range STM-1 to STM-16 (150Mbit/s to 2.4Gbits), these being conveniently accessible electronic block sizes, then we can consider the implications of having many optical carriers per fibre, each carrying data at such a rate. For example, if we chose to space such optical carriers by 15 GHz, then we might be able to accomodate 300 such carriers within the EDFA gain window. This would correspond to a data capacity of 180 Gbit/s using STM-4 per carrier and in a multi-fibre cable, a great deal more. From a practical point of view, this may be rather greater than would

be desirable, both from the point of view of traffic demand and security. Accordingly, we have the potential of having many more wavelength slots than are needed for data transmission. Our proposal is to use such slots for routing purposes.

Let us define the number of possible wavelength slots as W (ie W = 300 in our example above) and let us assume that of these, we only need to use w. Typically, we believe w might lie in the range 30-100. In the UK, the core network comprises about 50 major switching nodes, so that for thinking purposes, it is convenient to envisage the network as an (nxm) array of nodes (n=5, m=10), with the longest possible (direct) path between any two nodes traversing (n + m - 2) arms. If we now wish to route a signal through such a network by choosing a suitable carrier wavelength slot and onward routing that same wavelength at each node without wavelength shifting, then we can easily establish the worst-case probability of doing so successfully assuming that wavelength slots are selected on a random basis. It will arise when w-1 wavelength slots are already allocated on each of (n+m-2) arms.

Starting at the chosen entrance point to the high speed core network, we select an unused wavelength slot on the first arm we wish to traverse. This we can do with certainty. We then poll the other entrance nodes to the arms of the network we wish to traverse to establish whether that same wavelength is free throughout the route. The probability that the wavelength is occupied on any single arm is simply ((w-1)/W) so that the probability of gaining a path is (1-(w-1)/W). Repeating this through the maximum number of arms in the network, we find the probability of gaining a path is $(1-(w-1)/W)^{(n+m-2)}$ so that the blocking probability is $P_{block} = [1- (1-(w-1)/W)^{(n+m-2)}]$.

In a more realistic situation, we recognise that along any one arm it is extremely unlikely that only one fibre will exist, so that more typically we might have p fibres in the cable. Since we could choose our wavelength in any one of the fibres along that arm, the blocking probability for that arm is reduced and the overall blocking probability takes the form $P_{block}(p) = [1- (1-((w-1)/W)^p)^{(n+m-2)}]$.

A further option exists that we have not exploited, namely that when setting up our circuit, we could identify not one unused wavelength in the first arm but q wavelengths and seek one that is available. Under these circumstances and with the same assumptions, the resultant blocking probability is given by :-

$P_{block}(p,q) = [1- (1-(w/W)^p)^{(n+m-2)}]^q$.

It is now a simple matter to evaluate this result for some realistic situations in order to establish how viable such a wavelength allocation scheme might be. For evaluation purposes, we will choose the following parameter values. n = 5; m = 10; p = 4, 6, 8; q =2, 4, 6, 8, 10; W = 300; w = 50,100,150, 200. The results of this are shown in Fig.2 below and show that very low blocking probabilities arise over such a multinode network even with filling factors (w/W) as large as 60%

provided that a reasonable number of wavelengths (q) are selected for testing and there are modest numbers of fibres available along any given route.

The funtional requirements for this wavelength switching node are illustrated in Fig.3 & 4. In many respects, it might closely resemble a grating spectrometer except that we envise the use of a reflective SLM to carry out the free-space selection of the connections to be made, perhaps located in the conventional position for the exit slit, and a fibre array to provide the I/O in place of the entrance slit. We envisage the input wavelength comb split into two interpenetratin combs of double spacing using a Mach-Zehnder interferometer to halve the resolution requirements and the power from each M-Z port then split between M fibres (for an MxM switch). A grating element is then used to form a 2M x W spot array on the SLM, of which only 2Mw spots will be illuminated. The selected channels are reflected back through the dispersive system to spatially recombine them at the output ports where a conventional cross connect of fibres makes the necessary connections to the chosen output port and power splitters re-assemble the wavelength multiplex entering each output fibre.

Commercial grating spectrometers offer 0.02nm resolution (eg 1.3 GHz) so that the separation of channels in a 10-50 GHz spacing comb spectrum does not seem impossible. Careful design is clearly necessary to achieve acceptable insertion losses but the performance of simple commercially available grating multiplexers for single mode fibres gives cause for some optimism. The need to suppress non-linear four-wave interactions between channels in the transmission arms of such a network appears to dictate of order 50 GHz spectral line spacing[1] implying a capability for W=100 rather than the 300 postulated. However, this still allows an impressively powerful network, having many of the characteristics of todays core networks with digital cross-connect,s and could meet our suggested design requirement of w=50 or more.

The component implications of the above proposal are difficult to meet but not beyonds the bounds of possibility. We envisage that the transmitter assemblies for such a network would include a comb wavelength reference source and tunable semiconductor lasers slaved to it for each of the w channels potentially launched at a given node.Commercial grating spectrometers offer perfromances close to those sought and SLM array shutters seem well placed provide the route selection. The major missing elements at present seem primarily to be those required for accurate control of the individual carrier power levels through such a complex network.

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FIGURES

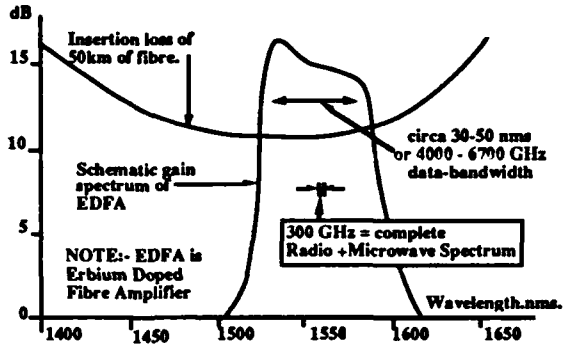

Fig.1 Schematic plot of insertion loss of 50km of fibre with an EDFA gain spectrum overlaid, showing potential transmission window.

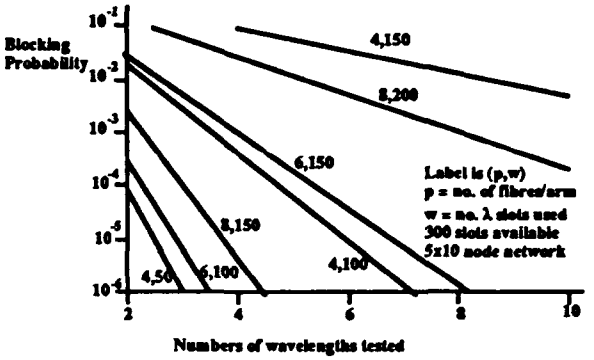

Fig.2. Plot of the blocking probability for a 5x10 multinode network using 300 wavelength slots and up to 60% occupancy.

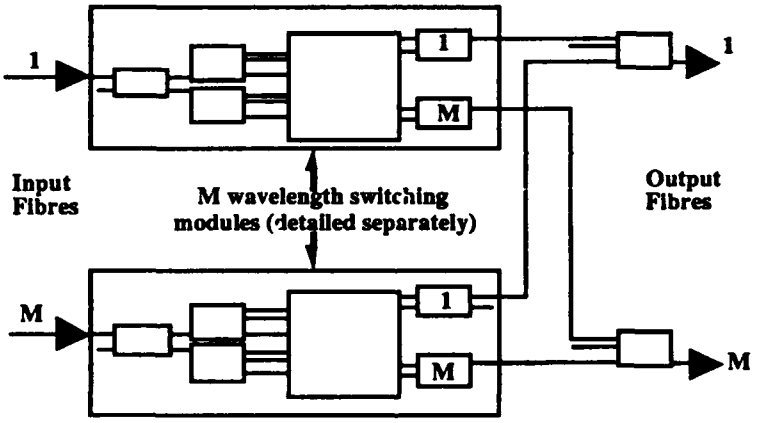

Fig.3. Functional schematic of the wavelength switching node proposed.

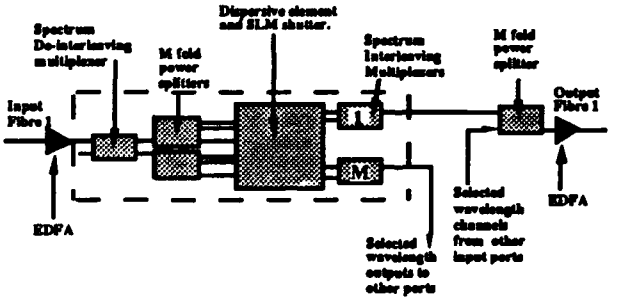

Fig.4. More detailed diagram of the wavelength selective stage.

"Broadcast and Switch" – A New Class of WDM Networks for High Switching-Speed, High Connectivity Applications

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Introduction

Optical networks can be categorized into two main types: "Broadcast and Select" and "Wavelength Routing" [1]. The main building blocks in these networks are: star couplers in the former and wavelength-selective switches (WSS) in the later. The WSS is a switch that can independently switch different wavelengths. In both networks, tunability of transmitters or receivers is usually needed to provide the desired connections. In current technologies optical networks experience a "tunability bottleneck": tunable lasers, although fast, are limited to a narrow region resulting in a relatively small number of wavelengths, and tunable filters are relatively slow for high speed applications.

We propose a strictly non-blocking architecture that makes use of both star couplers and WSSs. A specific realization of WSS is described where tunability of both transmitters and receivers is eliminated, thus, overcoming the "tunability bottleneck". This realization overcomes some possible drawbacks (e.g., limited connectivity, low switching speed and high complexity) of star-based networks. Both point-to-point and multi/broad-casting connections are possible in this architecture which can be implemented in existing technologies.

This paper describes a broadcast network which utilizes both the space and wavelength dimensions, however, the principle involved here is generic and true for any set of dimensions (e.g., space, wavelength and time, to name a few). Each user broadcasts via fixed multi-channels (one channel per dimension) to all users, and selects a specific user by selecting its corresponding channel in each one of the dimensions.

Architecture

In Figure 1 is shown the Star-Switch (STSW) architecture. The STSW has two stages, the first

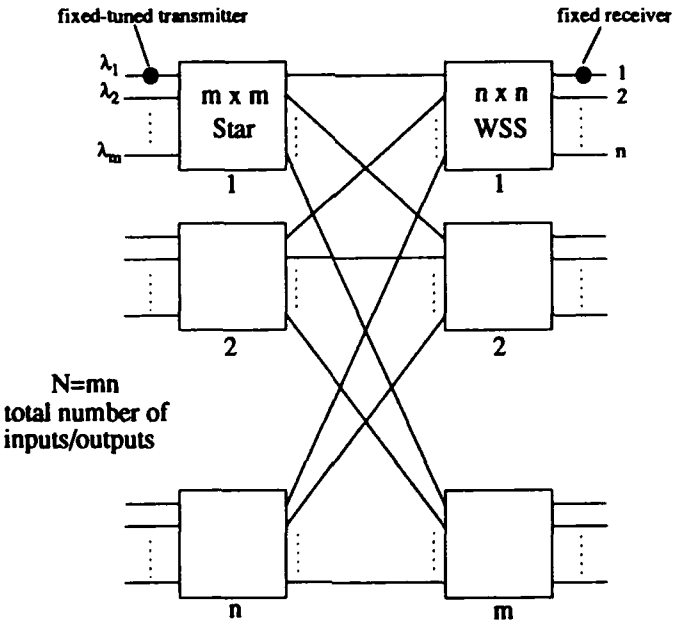

Figure 1: Star-Switch architecture using star couplers and Wavelength Selective Switches (WSSs).

stage is composed of n mxm star couplers and the second stage is composed of m nxn WSSs. The two stages are connected to each other by $N = mn$ links such that there is only one link between each star coupler and WSS. To each one of the n star couplers m fixed-tuned transmitters are connected, each with different wavelength (e.g., $\lambda_0, \lambda_1, \cdots \lambda_{m-1}$). The total number of wavelengths needed in the network is m. To each one of the m WSSs n identical fixed receivers are attached. Note that each WSS receives the entire information from all the N transmitters.

Several realizations of WSS are possible, in Figure 2 is shown a WSS composed of 1xn splitters, 1xm WDM-demultiplexers (WDMD) and single-output photonic switches (nx1 and mx1). The first part of the WSS is composed of splitters and photonic switches-I in an nxn tree configuration [2]. Each one of the tree's inputs is connected to a different star-coupler. The second part of the

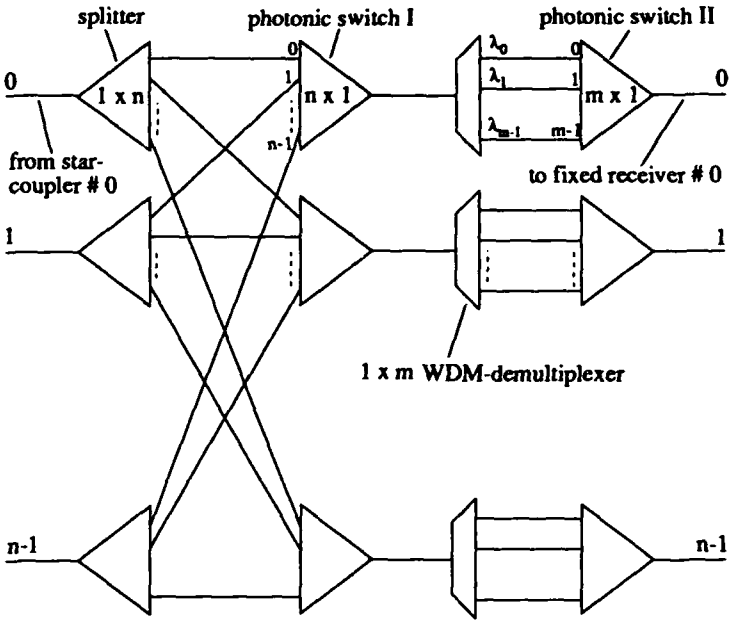

Figure 2: Wavelength Selective Switch (WSS) composed of splitters, WDM-demultiplexers and photonic switches.

WSS is composed of WDMDs and photonic switches-II to provide filtering of a specific wavelength out of a pool of m different wavelengths. The splitters, photonic switches and WDMDs (e.g., interference filters) are composed of their basic 1x2 elements arranged in a binary tree structure. To connect input i to output j in the STSW ($i, j = 0, 1, \cdots N-1$), only two switches have to be set in a unique way: in photonic switch-I of output j, input $\lfloor i/m \rfloor$ has to be switched; in photonic switch-II of output j, input $i \bmod m$ has to be switched. By setting these two switches of a specific output, any input can be selected. The total number of active switching stages (of 1x2 switching elements) is $log_2 N$. The switching elements are set easily since they are arranged in a binary tree structure. The switching-time of the STSW is of the order of nanoseconds since the only active elements in the network are the photonic switches.

Complexity and example

The complexity of the STSW in terms of basic spatial-elements count, is determined from the complexities of the star couplers and the WSSs. The n star couplers have complexity $O(N log_2 m)$. The WSS complexity is calculated as follows: the complexity due to the splitters and photonic switches-I, and the WDMDs and photonic switches-II is $O(n^2)$ and $O(N)$, respectively. Thus, the STSW complexity is $O((m+n)N)$, dominated by the WSSs. A minimum complexity of $O(N^{3/2})$

is achieved when $m = n = N^{1/2}$. In this case, the number of wavelengths needed is $N^{1/2}$. It can be shown [3] that when k dimensions are used, the STSW has a minimum complexity of $O(N^{1+1/k})$ using only $N^{1/k}$ wavelengths. Note that a pure space-division generalized switching network that is strictly non-blocking, must have a complexity of $O(N^2)$ [4] independently of the number of its stages. On the other extreme, a pure wavelength-division schemes (e.g., star-based networks) also have a complexity of $O(N^2)$, since N wavelengths are needed and the complexity of each tunable element is equivalent to $O(N)$. The fundamental power loss in the STSW is $1/N$.

	complexity	number of wavelengths	number of stages	power loss	type
Star	$O(N^2)$	N	$O(\log_2 N)$	1/N	point-to-point &multi/broad-casting
STSW 2-dimensions	$O(N^{3/2})$	$N^{1/2}$	$O(\log_2 N)$	1/N	point-to-point &multi/broad-casting
STSW k-dimensions	$O(N^{1+1/k})$	$N^{1/k}$	$O(\log_2 N)$	1/N	point-to-point &multi/broad-casting
Crossbar	$O(N^2)$	1	O(N)	1/N	point-to-point &multi/broad-casting
Tree	$O(N^2)$	1	$O(\log_2 N)$	1/N	point-to-point &multi/broad-casting
Clos 3-stage	$O(N^{3/2})$	1	$O(N^{1/2})$	—	point-to-point only

Figure 3: Comparison between strictly non-blocking photonic networks.

Consider a numerical example of a 1024x1024 STSW: only 32 wavelengths are needed together with 32 modules of 32x32 star couplers and 1024 modules of 1x32 splitters, WDMDs and switches. Modules of size 32 are feasible using existing technologies. The STSW has in this example only 10 active switching stages. Assuming each input transmits at 1 Gbps, the total throughput exceeds 1 Tbps. A comparison between the STSW, star-based networks and some classical strictly non-blocking networks appear in Figure 3. It turns out that the STSW outperforms some traditional networks. It has both low complexity, fewer wavelengths and a small number of stages (which results in low crosstalk), whereas, in other networks only part of the values are desirable.

Conclusions

We have described the "Broadcast and Switch" architecture making use of both star couplers and WSSs, where tunability of both transmitters and receivers is eliminated. This results in reduced complexity ($O(N^{3/2})$), much higher switching speed (nanoseconds) and fewer wavelengths ($N^{1/2}$) than in star-based networks. The architecture is strictly non-blocking supporting both point-to-point and multi/broad-casting connections, and can be implemented using existing technologies.

Acknowledgment

The author would like to thank K. W. Cheung and T. E. Stern for their comments and continued encouragement.

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Ultra-Fast Wavelength Switching and Wavelength Conversion with Strained-MQW-Y-Lasers

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Introduction:

To meet the demands of fast optical switching architectures we need photonic devices with short electronical as well as optical switching times. These requirements concern all degrees of freedom: frequency/wavelength, space and time. With Y-lasers we have already demonstrated fast electrical tuning in wavelength and space with 1 GHz /1/ and all optical wavelength conversion /2/.

In this paper we report (a) on new results obtained with an optimized Y-laser structure (fig.1) with respect to laser characteristics, (b) on asymmetrical Y-lasers fast electronic tunable with one single current and (c) on symmetric Y-laser tunable over more than 50 nm compatible for fast and ultra wide-band conversion in the THz regime.

Y-Laser Design and Characteristics:

The laser structure is given in fig. 1. The Y-laser is completely grown by low-pressure MOVPE. The vertical layers contain five compressively strained quarternary QWs, quaternary (Q1.2μm) barriers and a quaternary (Q1.2μm) waveguide layer at bottom and on top of the MQW stack. For the lateral laser structure we applied a semi-insulating buried heterostructure (SIBH) process. The light/current characteristics of MQW-SIBH-Y-laser is shown in fig. 2 with threshold currents of 4*20mA for a 1.5mm long device.

Fast Electrical Wavelength Tuning:

The Y-laser wavelength tuning is mainly performed by controlling the tuning currents of segments 3 and 4, see fig. 1. For asymmetrical Y-lasers /3/ the full tuning range for one single current (I_3 or I_4) is given by the Mach-Zehnder spacing $\Delta\lambda_{MZ}$, defined by the geometrical cavity length difference ΔL, see fig. 3.

To verify fast wavelength switching we performed spectral and time resolved measurements on the Y-laser light output. A tuning current modulation with 100 MHz pulse period was superimposed to the DC current I_3. The modulation amplitude for tuning across interferometric modes was derived from the tuning efficiency, which is typically 100 GHz/mA for small tuning currents. In fig. 4 we depict the time-average output spectrum under tuning between two adjacent modes with mode spacing of 0.5 nm. The signal rise and fall times (20/80%) of both wavelengths are about 500 psec, see fig.5. Applying higher modulation amplitudes the laser tunes across intermediate modes. The suppression of such intermediate modes is more than 10 dB, obtained from the time-average spectrum as well as from the spectral and time resolved measurement. This should be high enough for digital transmission where we have typically 10 dB extinction.

Wavelength Conversion:
The Y-laser has already been already demonstrated to operate as an optically triggerable wavelength converter /2/. For this function the Y-laser can be pre-adressed at any wavelength within the total tuning range of 50 nm.

The optical wavelength conversion device operates in the following manner: Intensity modulated light of a directly modulated DFB laser is injected into segment 1 of the Y-Laser. The gain of the pre-adressed Y-Laser wavelength is suppressed due to amplification of injected DFB (light in optical ON state). When injected light is in optical OFF state, the Y-laser mode recovers very fast. Consequenty we can use this effect for fast conversion of Gbit/s data from any injected wavelength to another Y-laser tuned wavelength. We need a wavelength filter at the Y-laser output at segments 3 or 4 to select the Y-laser wavelength from the injected wavelength. The conversion by the Y-laser results in an improvement of the extinction ratio (optical on/off state): We obtained up to 30 dB extinction at the output with in input signal having 3 dB extinction.

To demonstrate this ultra wide-band and fast conversion effect we injected a 2.5Gbit/s data stream at a wavelength of 1525 nm into segment 1 of the Y-laser. This results in an output 2.5 Gbit/s data stream at segment 3 (non-inverted) at 1525 nm and inverted at the pre-addressed Y-laser mode (1570 nm). In fig. 6 we show the wavelength filtered data traces for wavelength conversion of 2.5 Gbit/s across 45 nm.

From bit-error-rate (BER) measurement of 2.5 Gbit/s under wavelength conversion across 45 nm we received the following results: With 7 dB extinction of the DFB transmitter side we observed a receiver sensitivity at BER=10^{-9} of -24 dBm, corresponding to a power penalty of 3.5 dB, see fig. 7. However, with a transmitter extinction of only 3 dB we obtain a power gain of 1.5 dB which is a result of the increase of the extinction under wavelength conversion.

Summary:
Fast wavelength tuning with 500 psec speed and fast wavelength conversion of 2.5 Gbit/s across 45 nm (even with power gain) has been achieved. Thus the Y-laser has been demonstrated as an attractive device for wavelength switching applications for example in wavelength routing of e.g. 2.5 Gbit/s ATM cells.

Acknowledgements:
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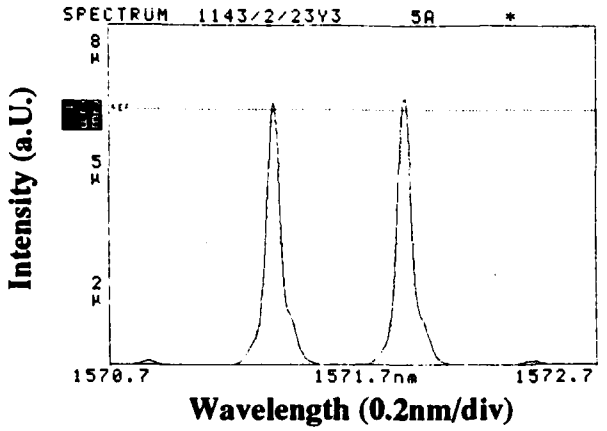

fig. 4:
Time-average spectrum under wavelength tuning between two adjacent interferometric modes

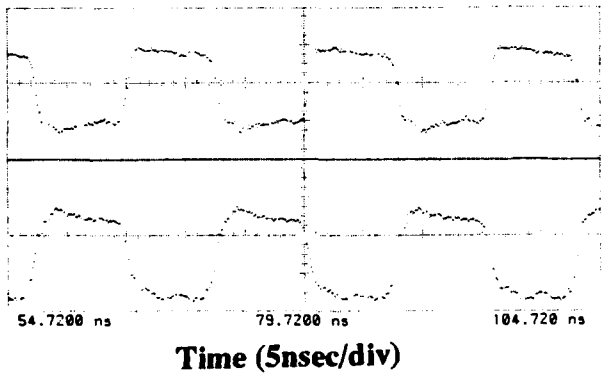

fig. 5:
Spectral- and time averaged measurement depicts the ON and OFF states:
11571.9 nm mode (upper trace)
1571.4 nm mode (lower trace)

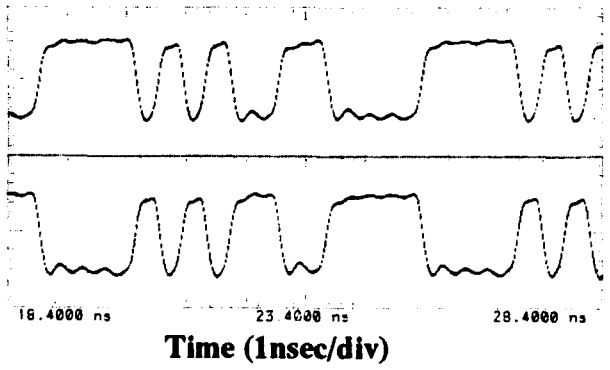

fig. 6:
2.5 Gbit/s
Wavelength Conversion
Output data of the Y-laser:
- upper trace at 1525 nm (= input wavelength)
- lower trace at 1570 nm (pre-adressed Y-laser wavelength)

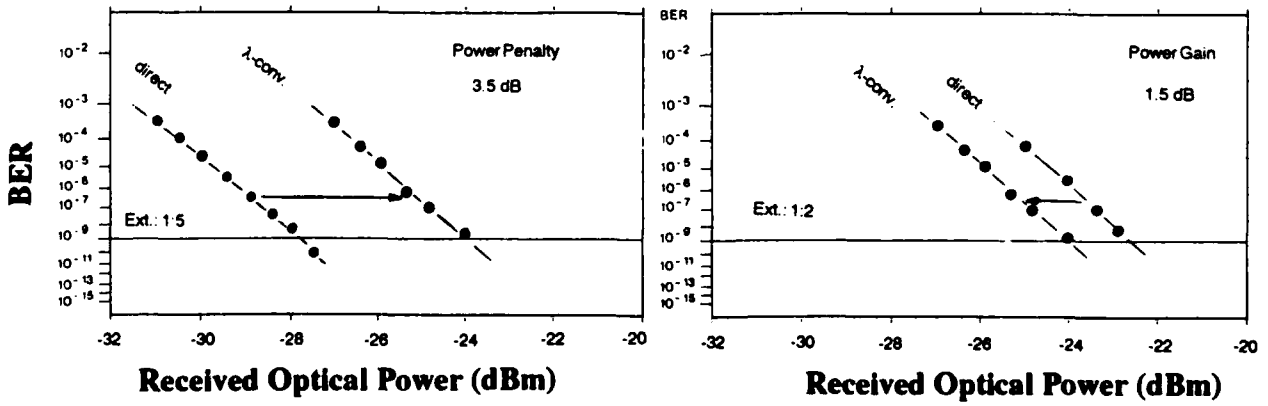

fig. 7: BER of 2.5 Gbit/s conversion across 45 nm with 7 dB and 3dB extinction at the transmitter side: Comparison direct and wavelength converted measurement.

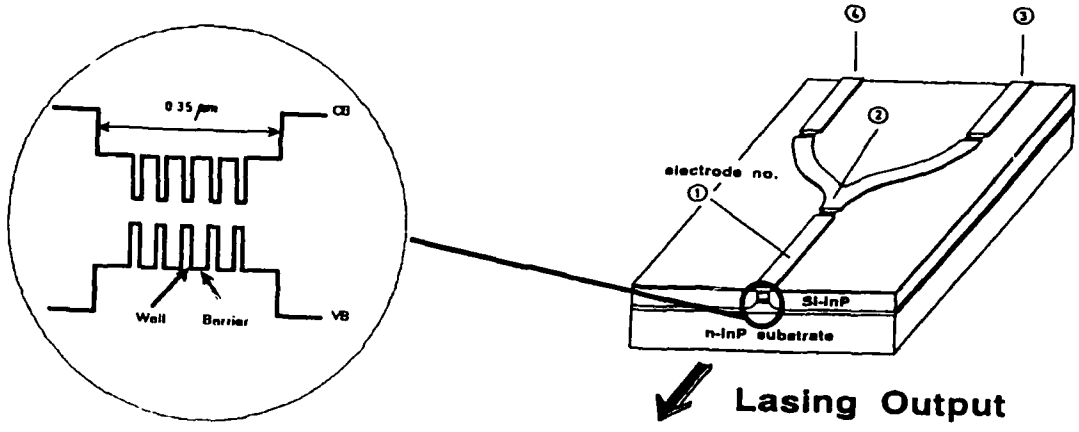

fig. 1: The basic Y-Laser structure as a 1:2 Y-junction with strained layer MQW active region

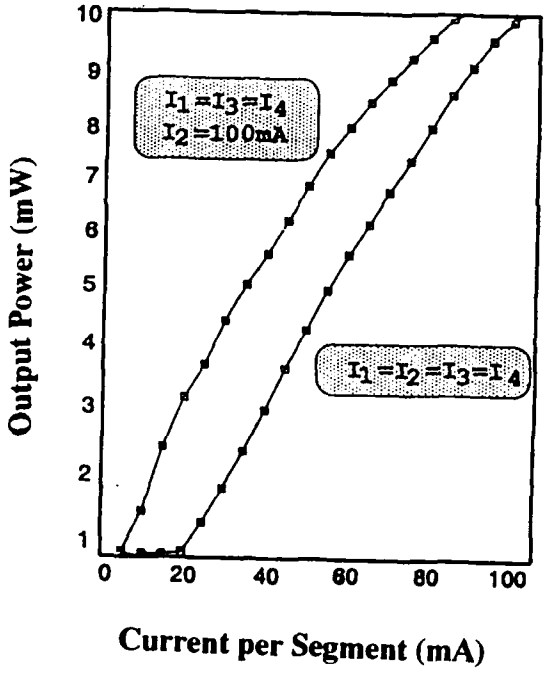

fig. 2:
Y-laser light/current characteristics

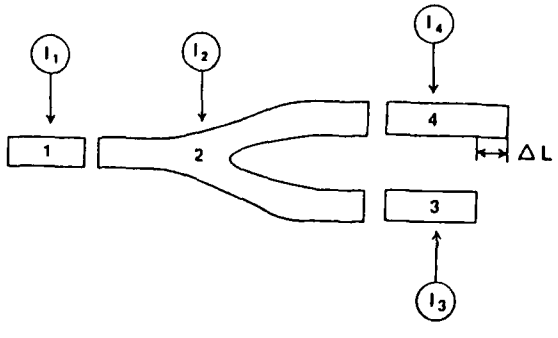

fig. 3:
Schematic of an asymmetrical Y-laser

Limits on Smart Pixel Granularity: Power Dissipation and Self-Inductance

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1 Introduction

Physical effects are present in high-performance systems that limit system packaging and architecture. For example, the finite capabilities of heat dissipation technology restrict the number of simultaneously switching elements, their density and switching speed for optoelectronic devices. In addition, the self-inductance of power and ground connectors between levels of packaging also limit the number of devices switching simultaneously. This paper examines the impact of these two effects for optoelectronic integrated circuits (OEIC). For high-speed optical I/O the power and ground pin-out can be comparable with the number of optical channels; hence, optical interconnects do not necessarily solve the package pin-out problem. Furthermore, these effects mandate large-grained smart pixels for high-bandwidth interchip communication.

2 Thermal Dissipation

Field effect optoelectronic devices like SEEDs can be modeled as capacitors for power dissipation analysis. The power dissipated by a capacitor is

$$P = CV^2B \tag{1}$$

where C is the device capacitance, V is the capacitor's charging voltage, and B is the operating bandwidth.

In an OEIC the capacitors are charged in parallel, and hence, the total chip capacitance is the sum of the device capacitances

$$C = \epsilon\epsilon_0\frac{A}{d} \tag{2}$$

where ϵ is the dielectric constant of the capacitor's dielectric, ϵ_0 is the permitivity of free-space, A is the sum of the device areas, and d is the dielectric thickness. Let the area of the chip (A_c) be equal to the sum of the device area (A) divided by a fill factor (F) between 1 and 0.

Assume that the thermal conductivity of the chip is large enough that there are no hot spots. If a fraction S of the devices can switch simultaneously, then the power per unit of chip area is

$$\frac{P}{A_c} = \frac{\epsilon\epsilon_0 FSV^2B}{d} \leq H \tag{3}$$

where H is the package power dissipation limit. For a given fill factor, switching fraction, operating voltage, dielectric constant and thickness, equation 3 places a limit on the bandwidth for a given power dissipation technology as shown in Figure 1.

Note that thermal dissipation severely limits the I/O bandwidth. The high-power dissipation methods are not a panacea because they are expensive and difficult to integrate into systems.

If the chip must operate at high speeds we have to either reduce the fill factor or the simultaneous switching

Method	H $[\frac{W}{cm^2}]$	B $[Hz]$
Air Convection	1	$4.6x10^4$
Forced Air	10	$4.6x10^5$
Liquid	100	$4.6x10^6$
Microchannel	1000	$4.6x10^7$

Figure 1: Bandwidth (B) vs heat flux (H) for fill factor of 0.9, switching fraction of 1, $\epsilon_{GaAs} = 10.9$, V = 5 V and dielectric thickness = 0.01 μm.

fraction of the device array. Large-grain smart pixels reduce both of these by devoting chip area to devices that do not switch simultaneously, e.g. memory and control logic. Moreover, the electronic capacitance is less than the optoelectronic capacitance because the process linewidth is less than the wavelength of light and the electronic dielectric thickness is smaller.

3 Self-Inductance

The inductance of the power and ground connectors to the package can also limit the density of high-speed optoelectronic devices. For inductance purposes, we can model optoelectronic devices as shown in figure 2.

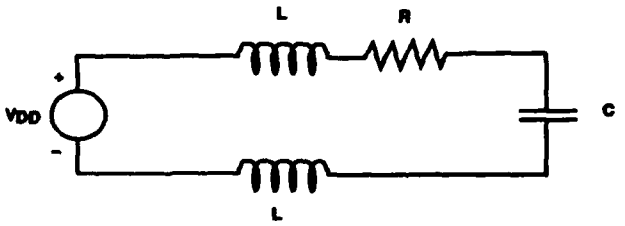

Figure 2: Equivalent circuit for power supply net.

The inductance of the package connectors will produce on the chip an increase in the ground potential and a decrease in the power potential for high-current and short-duration transients. To keep power and ground bounce voltages small we need the time constant of the inductive effects to be less than the RC time constant. This is equivalent to Faraday's Law [1]

$$\Delta V = L\frac{dI}{dt} \tag{4}$$

where L is the inductance of the power/ground connector, ΔV is the supply voltage bounce, and dI is the amount of current switched in time t.

Power supply voltage bounce can have several deleterious effects: [2] increased delay in the driver, spurious logical assignments by asynchronous receivers, increased delay in synchronous receivers, and increased delay and faulty logic states for gates on the same supply net.

If we add identical connectors in parallel to the power supply net, then the effective inductance decreases linearly. On the other hand, if we add more switching devices in parallel to the power net, the capacitance increases linearly. Let N be the number of simultaneously switching devices per package connector. If ΔV is the allowed voltage bounce on the power net then

Method	L $[nH]$	N	Pitch $[\mu m]$	A_B [%]
Wire Bond	1	103	150	95
TAB	0.7	148	75	75
Solder Bump	0.05	2072	100	28

Figure 3: Number of devices per pin (N) vs connector inductance (L) for conditions identical to those of Figure 1 with a 5% voltage bounce and a 25 μm^2 gate.

$$N \leq \frac{\Delta V T^2}{2LC_g V} \tag{5}$$

where T is the switching speed and C_g is the gate capacitance. Figure 3 shows the limit on the number of devices per pin (N) and total bond area as a percentage of chip area for inductances given in [3] and pitches given in [1].

Even for the most advanced packaging technology, solder bumps, a large fraction of the chip area is devoted to the power and ground connectors. Area devoted to connectors reduces the chip yield and reliability.

The large fraction of chip area devoted to connectors is another strong motivation to use large-grained smart pixels. Increasing the amount of circuitry in the pixel will increase the pixel size without dramatically increasing the current that must be switched in a small period of time. This reduces the fraction of the chip area devoted to power and ground connectors.

There are ways around some of the self-inductance problems, though none are perfect solutions. Using differential drivers and receivers will reduce the current by half. [1] Putting the optical receiver on the same chip as the source will greatly reduce the inductance of the supply loops. This implies that fine-grain smart pixels are compatible with intrachip optical interconnect architectures.

Optics provides a potentially significant advantage over electronics because one can electrically isolate the driver and receiver. To do this requires separate power systems for each pixel on the chip. Optical powering with photovoltaics can do this, [4] but it does not appear to be practical for large systems due to the power limitations of optical sources.

4 Conclusions

Thermal dissipation and self-inductance in OEIC's limit the I/O bandwidth and number of devices per power and ground connector. These limits favor large-grain smart pixel arrays because the bandwidth increases and the area penalty due to bond pads decreases with increasing granularity. On-chip current return loops favor intrachip optical interconnects and optical powering methods.

5 Acknowledgements

I would like to thank David Jared, Kelvin Wagner and Ted Weverka for helpful discussions. In addition, I would like to acknowledge support from a Department of Education fellowship and the NSF Optoelectronic Computing Systems Center.

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Turnover-type Free-space Multichannel Optical Switch

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1. Introduction:

Free-space optical switches are attractive candidates to replace conventional electrical switches in future supercomputers and telecommunication systems[1]. The switches have the potential to handle a large number of high speed signals without suffering from such problems as electromagnetic interference, signal delay, and clock skew. Liquid crystal light modulators which can control the polarization state of light are promising as the switching devices in such switches, because they make it easy to construct large arrays, and they are transparent to the lights being switched over a wide wavelength region. Several free-space multichannel optical switches based on these devices have been proposed for multistage optical switching networks [2],[3]. The optical switches are the one-way type in which optical signals enter one side of the switch body and are output from the other side. Input and output fiber arrays must, therefore, be situated on both sides of the switch. In applying such switches to intra-board chip-to-chip interconnects in a multiprocessor system, the input and output links of each processor have to be connected to the optical switch via input and output optical fibers, respectively[4]. This scheme causes wiring congestion and restricts the architecture of the system if the number of processors is increased.

This paper proposes the turnover-type switch which is a new type of free-space multichannel optical switch. The turnover-type optical switch inputs and outputs the optical signals from only one side of the switch. The features of the switch are, (1) the number of stages needed becomes about one half of that needed in the conventional one-way type switch, (2) the scheme is suitable for intra-board chip-to-chip interconnects.

2. Switch Configuration:

A turnover-type free-space multichannel optical switch is an optically implemented Benes network which is a rearrangeable multistage switching network. Fig.1 shows the configuration of a 16×16 turnover-type Benes network as an example. The network is composed of an I/O stage, four switching stages, five routing stages and a turning stage. The I/O stage and the switching stages are arrays of 2×2 switch elements. The switching state of all switch elements in the I/O stage is fixed to either 'bar' or 'cross' state. At each routing stage, switch elements in adjacent two switching stages are interconnected in a butterfly scheme as shown in the figure. The turning stage is an array of turning elements, each of which simply interconnects two lines. Routing stage 5 and the turning stage turn back the signals output from a switch element in switching stage 4 to another switch element in the same switching stage. If all switch elements in the I/O stage are fixed to 'bar' ('cross') state, a signal input to the network is always input to one of the upper (lower) half switch elements in switching stage 1. The signal is turned back at the turning stage and output from a lower (upper) half switch element in switching stage 1 in the reverse direction. The signal is finally output from one of the switch elements in the I/O stage. This operation allows the turnover-type network to locate all signal inputs and outputs on the same side of the network.

The network shown in Fig.1 can be implemented optically using the polarization multiplexing technique. Fig.2 shows the optical implementation of the turnover-type network proposed in this paper. Liquid crystal light modulator arrays (LCLMs), each element of which

acts as a 2×2 switch for the two orthogonally polarized optical beams, are used as the I/O stage and the switching stages. A routing element is formed by stacking polarization beam splitter (PBS) rods and glass rods as shown in Fig.2. Two orthogonally polarized (P- and S-polarization) optical beams are used as signal carriers. A P-polarized optical beam input to a routing element passes through the element, whereas an S-polarized beam is reflected a few times in the element and output from the shifted position. The turning stage is formed by cascading a λ/4 plate and a mirror. This structure exchanges the polarization state of the reflected beams. Therefore, each reflected beam takes a different path from its incident path. Fig.3 shows one possible configuration of the turnover-type free-space multichannel optical switch. The LCLM arrays and the routing elements are alternately layered. A λ/4 plate and a mirror form the turning stage.

In a turnover-type free-space multichannel optical switch, the input and output optical beams are multiplexed at the I/O stage. It is therefore possible to pass both input and output optical signals through a polarization maintaining fiber(PMF) by attaching a PMF collimator array at the I/O stage. This scheme permits a wide variety of architectures to install optical switches into electronic systems like multiprocessor and switching systems. When using an optical switch for board-to-board interconnects in an electrical system, for instance, each board has input and output links that can be connected to the optical switch through only one PMF. Moreover, the turnover-type switch can be easily implemented to realize intra-board chip-to-chip interconnects. Fig.4 shows the installation of a turnover-type optical switch as such interconnects. LSI chips, each of which has an optical source and a detector, are attached to the board. The turnover-type optical switch is placed above the board. A birefringent crystal is placed between the board and the optical switch as a directional coupler. Each optical source outputs a P-polarized collimated beam. The beam passes through the birefringent crystal and inputs the optical switch. The path of the optical beam as output from the switch is shifted within the birefringent crystal and falls on a detector. With the configuration shown in Fig.4, arbitrary interconnection among the LSI chips is possible.

To construct a $2^n \times 2^n$ turnover-type switch, n switching stages, (n+1) routing stages, an I/O stage and a turning stage are necessary, whereas 2n-1 switching stages and 2(n-1) routing stages are required for the conventional one-way-type switch of the same scale. The number of stages in a turnover-type switch, therefore, becomes about one half the number required by the one-way-type switch for large channel numbers. This means the turnover-type switch is compact and easy to construct. Although the number of elements in each stage in a turnover-type switch is twice that in the one-way-type switch, this doesn't matter since the optical array devices used are easy to extend as large arrays.

3. Experiment:

A 64×64 turnover-type free-space multichannel optical switch was fabricated. The specifications of the fabricated switch are summarized in Table 1. The LCLM array has 64 pixels arranged in an 8×8 pattern. Each pixel is 1.5mm square, and pixel spacing is 3mm. Routing elements of three different sizes were used. Seven LCLM arrays and seven routing elements were alternately layered to form the switch body. The turning stage is comprised of a quartz λ/4 plate and an aluminum-coated mirror, was placed at the far end of the switch body. The overall length of the switch body was 22cm. An 8×8 collimator array, consisting of polarization maintaining fibers(PMFs) and GRIN lenses was used to launch the polarized optical beams.

Output optical patterns were observed for six types of switching operations: (a) normal pattern, no switching, (b) reverse, (c) perfect shuffle, (d) transpose, (e) clockwise rotation, and (f) counterclockwise rotation. Fig.5 shows examples of the output optical patterns. The output optical beams are separated from the input beams using a PBS constructed from a 25mm cube. All switching operations were successfully performed by the fabricated optical switch. The optical insertion loss and crosstalk was measured on 32 input channels for the six switching

operations. The measured insertion loss histogram is shown in Fig.6. The average insertion loss and crosstalk of the fabricated optical switch were 9.2 dB and -15.2 dB, respectively. The average insertion loss predicted from the measured average insertion losses of LCLM arrays and routing elements[2] was 8.3dB. The residual loss is caused by the losses at the turning stage and the PBS, and residual misalignment of the optical components.

4. Summary:

A novel free-space multichannel optical switch structure, the turnover-type switch, was proposed. The structure makes it easy to integrate optical switches into processor networks as intra-board chip-to-chip interconnects. A 64×64 turnover-type optical switch was fabricated and its switching performance was confirmed.

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Table 1 Specifications of the fabricated optical switch.

Channel number	64 (8×8)
Wavelength	670nm
LCLM	Twisted nematic liquid crystal with AR.
Pixel size, spacing	1.5mm square, 3mm pitch
Number of LCLMs	7 (6 for switching and 1 for I/O stages)
Routing elements	stacked 3mm, 6mm and 12mm PBS rods with AR.
Number of the elements	7
Length of the switch body	22cm
Collimator array	
Optical fiber	polarization maintaining fiber(PMF)
Collimating lens	GRIN lens (2mm dia.)
Optical beam diameter	1mm

AR; antireflection coating

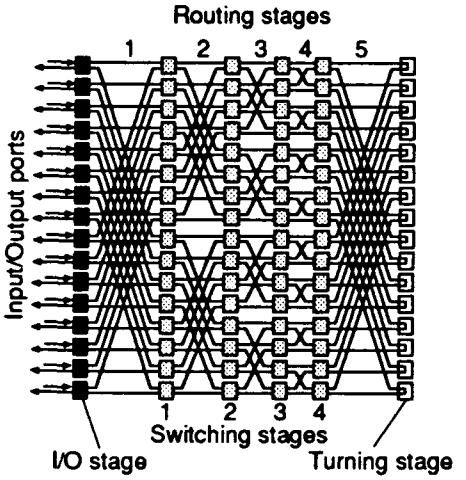

Fig.1 Network configuration of 16×16 turnover-type Benes network.

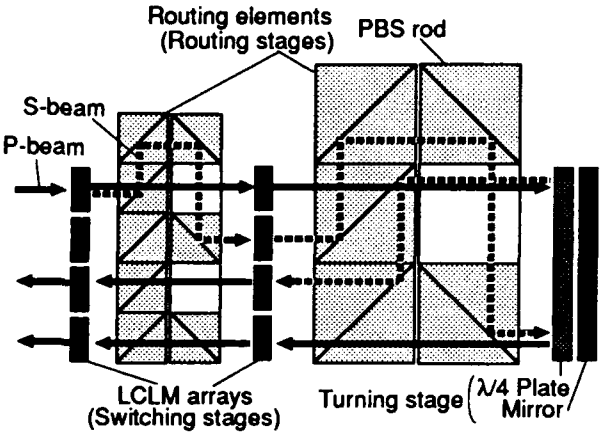

Fig.2 Optical implementation of the turnover-type switching network.

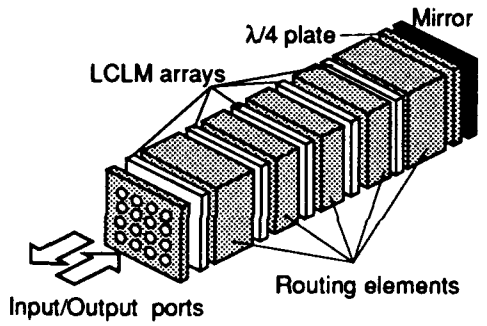

Fig.3 Configuration of the turnover-type free-space multichannel optical switch.

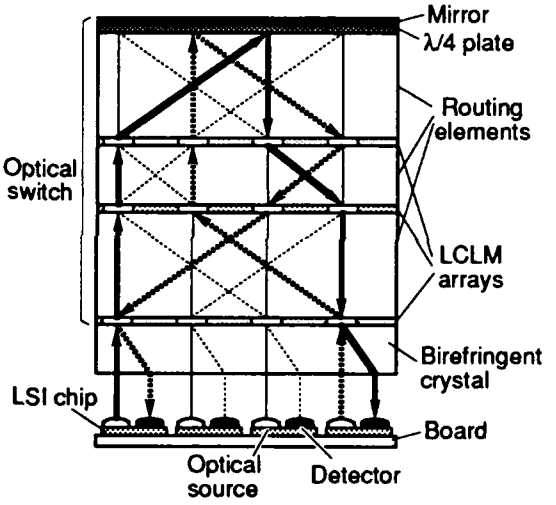

Fig.4 Installation of a turnover-type optical switch as chip-to-chip interconnects.

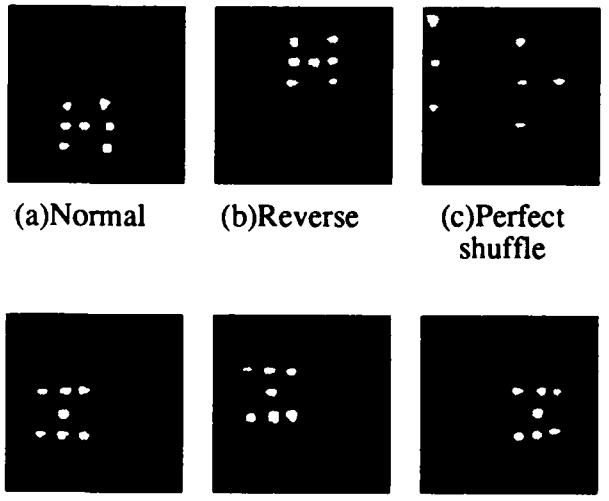

Fig.5 Examples of the output beam patterns.

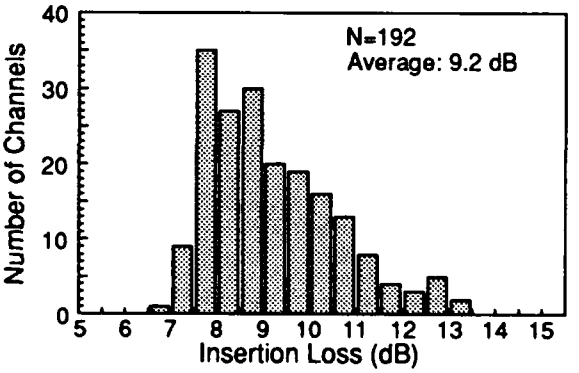

Fig.6 Optical insertion loss histogram for the fabricated 64×64 optical switch.