NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

Gallium Arsenide Dynamic Random Access Memory Support Circuitry

by

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March 1993

Thesis Advisor: Douglas J. Fouts

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release; distribution is unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION: Naval Postgraduate School; 6b. OFFICE SYMBOL (if applicable): EC	7a. NAME OF MONITORING ORGANIZATION: Naval Postgraduate School
6c. ADDRESS (City, State, and ZIP Code): Monterey, CA 93943-5000	7b. ADDRESS (City, State, and ZIP Code): Monterey, CA 93943-5000
8a. NAME OF FUNDING/SPONSORING ORGANIZATION; 8b. OFFICE SYMBOL (if applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State, and ZIP Code)	10. SOURCE OF FUNDING NUMBERS: PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)
GALLIUM ARSENIDE DYNAMIC RANDOM ACCESS MEMORY SUPPORT CIRCUITRY (U)

12. PERSONAL AUTHOR(S)
Morris, Michael Andrew

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Master's Thesis	FROM 01/92 TO 03/93	1993, March, 27	526

16. SUPPLEMENTARY NOTATION The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the United States Government.

17. COSATI CODES		
FIELD	GROUP	SUB-GROUP

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
RAM, DRAM, Gallium Arsenide DRAM, Support Circuitry DRAM
GaAs Logic Circuits, SBFL, DCFL, GaAs Layout, HSPICE, MAGIC

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This thesis presents the design and layout of a Gallium Arsenide (GaAs) Dynamic Random Access Memory (DRAM) array of eight four-bit words including refresh circuitry. In the last several years, there has been significant research investigating the possibilities of producing much faster, lower power and high density DRAM using GaAs. Thus far, this research has yielded success on a limited basis using special materials and fabrication techniques. This design, tested and simulated using HSPICE, supports a memory access time of approximately three nanoseconds, faster than present commercial Static Random Access Memory (SRAM). The logic circuits are designed using GaAs enhancement-mode and depletion-mode (E/D) metal semiconductor field-effect transistors (MESFETs). Charge storage is facilitated by a single GaAs MESFET connected to a parallel plate capacitor and the required minimum time between refresh is approximately three milli-seconds. Power consumption is acceptable and fabrication by Vitesse Semiconductor Corporation using the HGaAs3 process is in progress. The design techniques, power consumption and timing are discussed and demonstrated for the basic logic circuits and the memory array read, write and refresh cycles. A significant increase in DRAM memory bandwidth is gained narrowing the memory bandwidth differential between primary memory and the processor.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	UNCLASSIFIED
22a. NAME OF RESPONSIBLE INDIVIDUAL: Douglas J. Fouts	22b. TELEPHONE (Include Area Code): (408) 656-2852 — 22c. OFFICE SYMBOL: EC/Fs

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete.

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GALLIUM ARSENIDE
DYNAMIC RANDOM ACCESS MEMORY
SUPPORT CIRCUITRY

by

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Lieutenant, United States Navy
B.S.E.E, University of South Carolina, 1987

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 1993

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Abstract

This thesis presents the design and layout of a Gallium Arsenide (GaAs) Dynamic Random Access Memory (DRAM) array of eight four-bit words including refresh circuitry. In the last several years, there has been significant research investigating the possibilities of producing much faster, lower power and high density DRAM using GaAs. Thus far, this research has yielded success on a limited basis using special materials and fabrication techniques. This design, tested and simulated using HSPICE, supports a memory access time of approximately three nanoseconds, faster than present commercial Static Random Access Memory (SRAM). The logic circuits are designed using GaAs enhancement-mode and depletion-mode (E/D) metal semiconductor field-effect transistors (MESFETs). Charge storage is facilitated by a single GaAs MESFET connected to a parallel plate capacitor and the required minimum time between refresh is approximately three milliseconds. Power consumption is acceptable and fabrication by Vitesse Semiconductor Corporation using the HGaAs3 process is in progress. The design techniques, power consumption and timing are discussed and demonstrated for the basic logic circuits and the memory array read, write and refresh cycles. A significant increase in DRAM memory bandwidth is gained narrowing the memory bandwidth differential between primary memory and the processor.

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ACKNOWLEDGEMENTS

To Kathy, my wife: Your support, dedication and love throughout the last two and one half years has made this all possible. Thank you.

To my thesis advisor Dr. Douglas J. Fouts: Your vision, engineering expertise, unflagging confidence and perpetual enthusiasm served me well during my tenure. Thank you.

To my friend and associate Lieutenant Commander Christopher B. Vagts: Without your perseverance, expertise and previous work, this never would have happened. Thank you, and I wish for you "Fair Winds and Following Seas".

A special thanks to the Naval Postgraduate School ECE Department computer staff, especially Bob Limes, for their outstanding support service.

Out in the real world, a very special mention to the product support division of Framemaker (What a great product!) without whose help this thesis would not have made it, particularly when importing all these graphics.

Additionally, Meta Software, the HSPICE company deserves mega kudos for the product support provided to NPS.

Finally, thanks to my good friend, Lt. Charlie Victory, whose work ethic and enthusiasm made the thesis experience much more endurable.

I. INTRODUCTION

A. GALLIUM ARSENIDE (GaAs) DEVELOPMENT

Commercially, GaAs has been in use as a semiconductor since the 1960's, specifically in the fields of microwaves and optics. The speed offered by GaAs integrated circuits is its major drawing point. In the embryonic stages of GaAs integrated circuit (IC) development, low density devices such as microwave/ optical transmitters and receivers were considered breakthroughs. On the other hand, silicon (Si) ICs have been widely researched and tremendous density gains have been achieved. Examples of these gains are the 64 megabit DRAM chip and the Intel processor 80486. Conversely, GaAs IC research, development and fabrication processes are at least one generation behind. There are several reasons for this, the first and foremost is cost. Millions of dollars are required to "tool up" to fabricate ICs. While Si ICs are in tremendous worldwide demand with many large companies manufacturing a multitude of Si digital ICs, presently there is no such demand for GaAs. Until the demand increases, a limited number of smaller companies will continue research, development, testing and production of a small number of GaAs ICs using fabrication equipment from the last generation of Si processes. Additionally, as when Si development was in its early stages, there are several different GaAs fabrication processes being used, each has its own advantages, and some manufacturers may be "sitting out", waiting for a single process to become predominant.

B. SILICON -VS- GALLIUM ARSENIDE

Speed coupled with lower power consumption is the main issue when comparing Si to GaAs. Circuits that must operate at high-speeds use much less power when produced from GaAs than Si. The Power-Delay Product (power dissipated x propagation delay) when used to compare GaAs to Si, yields GaAs a 5:1 advantage. Additionally, circuits subject to radiation (such as in space satellites) suffer two results, Single Event Upsets (SEU's) and substrate degradation. GaAs ICs are subject to SEUs but do not suffer from substrate degradation. Logic gate propagation delays for GaAs digital ICs are on the order of 10-150 picoseconds, whereas Si offers gate delays in nanoseconds. [Ref. 1:p. 3].

However, there are disadvantages to GaAs digital IC fabrication. First, the present density of the commercially available GaAs ICs is much less than those produced in Si. Some of the reasons this is so were discussed above. Second, electrical signals traverse a glass epoxy circuit board at the rate of approximately

one foot per nanosecond, but the same electrical signal will traverse a GaAs logic gate in as few as 10 picoseconds yielding a large ratio of input/output delay-to-propagation delay. Because of the very high speeds offered by GaAs ICs, transmission line theory must be considered and utilized when designing in GaAs. Third, the layout of a Si CMOS gate (pull-up to pull-down) is very symmetric (this is because it is a complementary logic design using an *n*-type transistor and a *p*-type transistor. However, a GaAs MESFET inverter uses a much smaller pull-up than pull-down (both *n*-channel FETs, hence not a complementary logic design) and this yields very asymmetric geometries which complicate the layout and yield lower IC densities. Fourth, while the cost to produce GaAs ICs has fallen significantly in the last year such that GaAs ICs (in quantity) now cost less then comparable Emitter-Coupled Logic (ECL) or Bipolar Complementary Metal-Oxide Semiconductor (BiCMOS), fabrication of GaAs ICs is still expensive. However, should the trend towards lower costs continue, the cost of GaAs IC's will soon be comparable to Si for most circuits. Fifth, layout and circuit simulation tools for Si have evolved through several generations whereas the like tools for GaAs are sparse but improving steadily. Sixth, the voltage gain of GaAs MESFETs is small (this is imposed by the Schottky barrier junction gate of the MESFET which exhibits a forward voltage conduction limit of about 0.7 volts positive with respect to the source), consequently the noise margin for n-channel GaAs digital logic circuits is also small. The magnitude of the noise margin varies somewhat with which GaAs logic family is used. Finally, GaAs suffers from leakage currents not affecting Si. These GaAs leakage currents impact heavily on the design of GaAs circuits which use charge storage. [Ref. 1].

C. GALLIUM ARSENIDE MEMORIES

Considerable GaAs research within academe and, to a lesser extent within industry, has occurred and the results are encouraging. Within the field of GaAs memories, the late 1980's have yielded several low density GaAs static memories (SRAM's) [Ref. 2][Ref. 3] and at least four hybrid metal, dynamic memories [Ref. 4], [Ref. 5], [Ref. 6], and [Ref. 7]. To date, there have been no reports of a successful GaAs DRAM design which used standard GaAs materials and fabrication techniques.

Presently available commercial Si DRAMs offer access times on the order of 60 nanoseconds while commercial Si SRAMs have access times of approximately 10 nanoseconds. But static memory integrated circuits offer much lower densities by virtue of the fact that one data bit of static memory requires four to six transistors whereas one data bit of dynamic memory may be represented by a single transistor in a dynamic memory. This is because static memories use a flip-flop configuration of transistors as the basic storage element while dynamic memories use charge storing capacitors as the basic storage element. Additionally,

SRAMs, by virtue of their flip-flop design, use significantly more power per bit. For a thorough discussion of the charge storage aspects of this thesis, see the work by Vagts [Ref. 8].

This thesis will present some of the Gallium Arsenide logic families, basic designs of GaAs logic gates built into GaAs logic circuits, and then focus on the final product, a GaAs DRAM. The topics covered will include basic memory design, testing via HSPICE simulation, discussion of the layout using MAGIC (with GaAs technology files), overall timing diagrams, and finally, conclusions.

II. BASIC MEMORY DESIGN

A. TYPES OF MEMORY

Static memory retains its data anytime that power is applied because of the previously mentioned flip-flop. Dynamic memory, on the other hand, relies on the charge storage of a capacitor (generally) connected to a pass transistor. Both types of memories will lose their data once power is removed. However, maintaining the dynamic memory data, even with power on, requires periodic "recharging" of the capacitor in an operation called refresh. A discussion of the read-only memories (ROM) and its derivatives is beyond the scope of this thesis.

The type of memory being discussed here is referred to as "read-write" memory. It is incorrectly called "random access memory" in place of "read-write" memory" probably resulting from the "old" days when certain types of memories could not be accessed randomly (meaning the control logic could not obtain the contents of the desired address in memory without passing by other addresses before it or after it). As an example, magnetic tapes provide a type of memory that may only be accessed "sequentially". This label "random access memory" is the second part of the present commonly used abbreviation DRAM.

B. BASIC DYNAMIC MEMORY OPERATIONS

There are only three basic memory operations: read, write and refresh that will be discussed in this report. The discussion that follows generally relates to both the operation of "generic" memories and the operation of the topic memory.

Referring to Figure 2.1 on page 5, which is both a representation of a generic DRAM and the representation of the topic DRAM, one may see where the external inputs signals are applied and also the origin of the output signals.

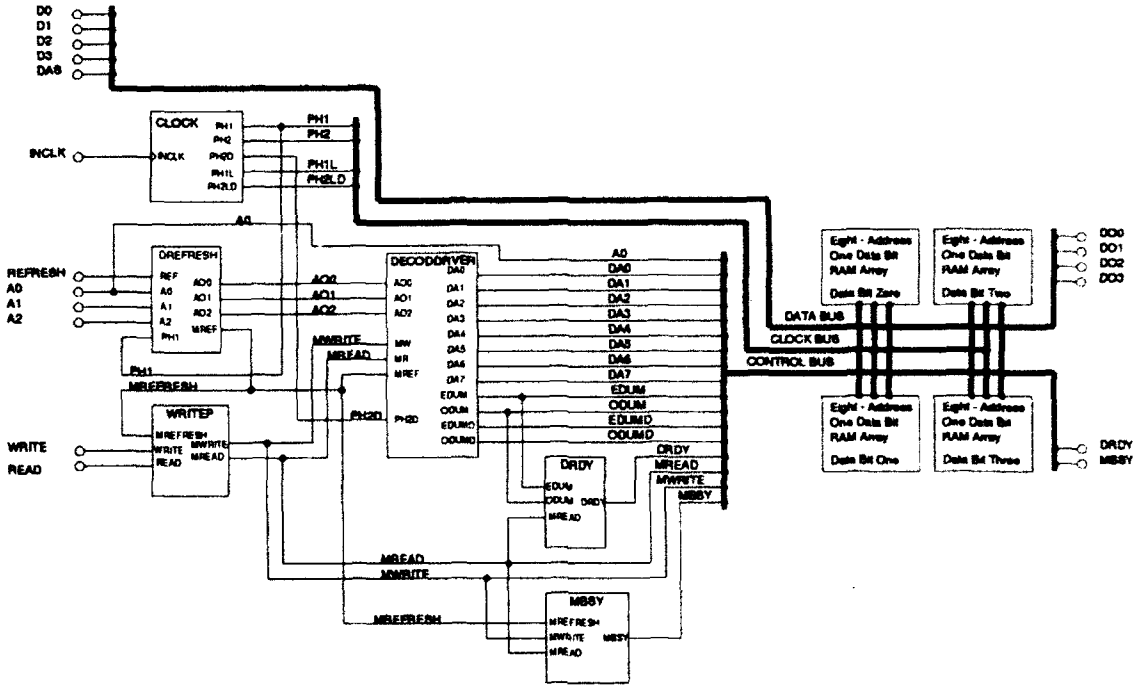


Figure 2.1 General Block Diagram of A Dynamic Memory

Reading the memory is accomplished by checking the status of the "memory busy" (MBSY) signal, presenting the memory control logic with the address of the desired location, pulsing the read line, latching the contents of the desired memory location, and setting the "data ready" (DRDY) signal. The memory busy signal tells the external users of the memory array that memory is presently unavailable and is asserted when the memory array is either busy accomplishing a read, write or a refresh operation. The strobe pulse on the read signal line instructs the control logic to commence the read operation and to assert the memory busy signal. Once the data is obtained from the desired memory location, it is latched into the output data latches, the data ready is asserted and memory busy signals is de-asserted. These signals indicates to the present external user that the requested data is ready and waiting on the memory output data lines. Additionally, the de-assertion of the memory busy signal indicate that the memory array is once again ready for further tasking.

Writing the memory is accomplished is a similar but slightly different manner. Writing requires data so the first step (given the correct status of the memory busy signal) is the present valid data and assert the "data strobe" (DAS) signal. This signal, asserted by the external user of the memory, indicates to the memory control logic that the data now present on the input data lines is stable, valid and ready to be latched. The

control logic then acts to latch the input data and will assert the memory busy signal. Once the input data is latched, this frees the external memory user to use the bus (or busses) for other business. Next (or simultaneous to the presentation of the input data), the external memory user presents the address of the target memory location and asserts the memory write signal. This signals directs the memory control logic to transfer the data (already latched or latched simultaneously) to the target memory location. Once the memory array control logic has completed the write operation, it will de-assert the memory busy signal.

As the subject memory is dynamic, the stored charge will eventually leak or diminish and requires that it be periodically recharged. This is accomplished by the third memory operation, refresh. The refresh operation is executed regularly on a schedule dictated by the physics of the particular DRAM. Commercial DRAMs accomplish the refresh operation approximately every three - five milliseconds and the refresh operation requires approximately 300 nanoseconds [Ref. 9:p. 648]. The topic GaAs DRAM requires refresh at a minimum interval of approximately 3 milliseconds. The refresh operation basically consists of sequential reading then writing of (all data bits) each address in the memory array. It is not required that it be sequential, it happens to be easier to design the refresh controller logic to operate sequentially. The topic GaAs DRAM, by virtue of its particular sense amplifier design, only requires that the addresses be read in order to be refreshed, not read then written. For a more thorough discussion of the sense amplifier and the topic GaAs DRAM refresh operation, see the work of Vagts [Ref. 8:pp. 10-21].

III. GALLIUM ARSENIDE LOGIC FAMILIES

This discussion of GaAs logic families will be restricted to *n*-channel GaAs MESFETs, both enhancement-mode (e-mode) and depletion-mode (d-mode). There exists a *p*-channel GaAs MESFET but it is not widely used because it requires a high electric field to obtain the necessary saturated velocity of holes in GaAs [Ref. 10:p. 195]. For an excellent discussion of the available GaAs logic families, see [Ref. 10:pp. 195-244].

A. GALLIUM ARSENIDE DEPLETION-MODE LOGIC FAMILIES

The Gallium Arsenide depletion-mode logic families use both depletion-mode (normally-on) MESFETs and level-shifters, usually formed of forward-biased Schottky diodes. The level-shifters are required because the logic circuits in these families are characterized by unequal input/output voltage levels. This arises because V_{GS} must be made negative in order to turn off the depletion-mode MESFET, but V_{DS} must remain positive at all times. Additionally, two power supplies are required in order to provide both positive and negative signals. These power supplies, positive V_{DD} (also referred to as V_{DS}) and negative V_{SS}, result in additional power dissipated in the circuit. However, in defense on the GaAs depletion-mode logic families, larger logic voltage swings may be obtained using depletion-mode GaAs MESFETs which results in better (larger) noise margins.

1. Unbuffered FET Logic (UBFL)

This form of GaAs logic circuit offers reasonably low power dissipation, high noise margins, fairly low propagation delays for low fanout only. However, UBFL requires excessive chip real estate as a single UBFL 2-input NOR gate requires five d-mode MESFETs and two Schottky diodes, see Figure 3.1 on page 8. For an example of a UBFL NAND gate, see Figure 3.2 on page 8.

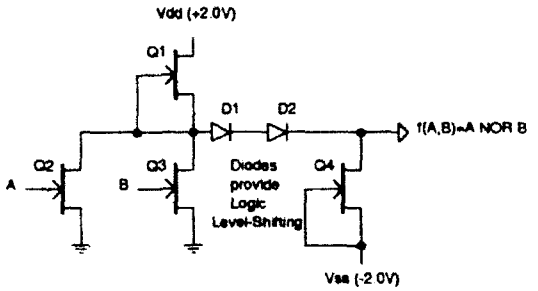


Figure 3.1 Gallium Arsenide UBFL NOR Gate [Ref. 1:p. 6]

The UBFL NAND gate structure is very similar to that of the UBFL NOR, the primary difference is the logic-determining d-mode MESFETs (Q2 & Q3) are in series vice parallel. This serves to limit the functionality in reality to a two input gate because anymore than two series MESFETs will prevent the individual MESFETs from acting upon their inputs. This is because the input pin action is relative to the source or drain voltage and for series transistors it varies. For the above reasons, one designs GaAs logic gates using almost exclusively NORs as the building blocks and applies the DeMorgan's theorems [Ref. 9:pp. 154-155] to yield the other desired logic elements. For an example of a true UBFL NAND gate, see Figure 3.2 on page 8.

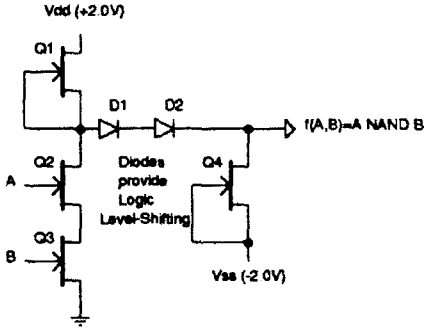


Figure 3.2 Gallium Arsenide UBFL NAND Gate [Ref. 1:p. 6]

2. Buffered FET Logic (BFL)

One possible solution to cure the poor fanout offered by UBFL is to couple a UBFL logic circuit with a source-follower stage. This works well to proportionally decrease the propagation delay as the fanout is increased but requires the use of two, active load, d-mode MESFETs which increases the amount of power

dissipated by the circuit. In addition, depending on the transistor sizes used, there is little savings in chip real estate. For an example of a BFL NOR gate, see Figure 3.3 on page 9.

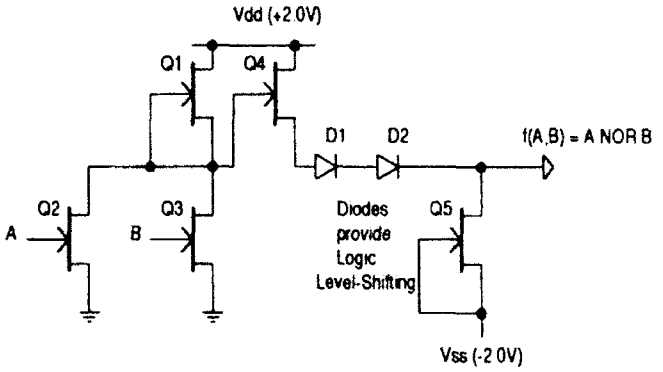


Figure 3.3 Gallium Arsenide BFL NOR Gate [Ref. 1:p. 7]

Examining Figure 3.3, the aforementioned source-follower stage is comprised of transistors Q4 and Q5. The diodes D1 and D2 again provide logic level-shifting. The additional power requirements of BFL arise from the addition of the source-follower stage direct current path from V_{DD} to V_{SS}. For an example of a true BFL NAND gate, see Figure 3.4 on page 9.

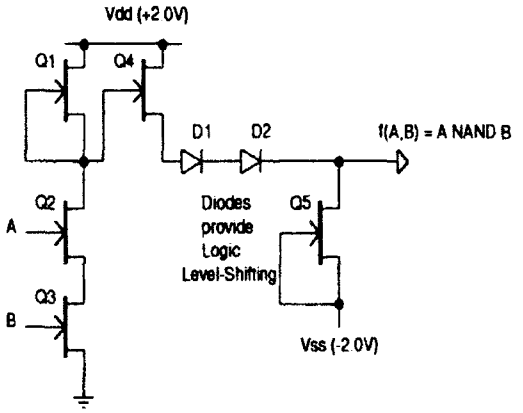


Figure 3.4 Gallium Arsenide BFL NAND Gate [Ref. 1:p. 7]

3. Schottky Diode FET Logic (SDFL)

Thus far in the discussion of GaAs logic families or circuits, the desired logic function has been performed by GaAs MESFETs. The NOR function is accomplished by MESFETs in parallel, the NAND function, series MESFETS, and more complex functions, a combination of both parallel and series MESFETs. Any use of Schottky diodes has been restricted to the level-shifting required by the circuit.

At this point, it is instructive to mention that Schottky diodes are well suited to directly accomplish the desired logic function. Some of the attractive features of the Schottky GaAs diodes: low capacitance, low series resistance, plus none of the problems associated with *pn* junction diodes. An additional advantage is realized in chip real estate in that Schottky diode can be made physically smaller than MESFETs. The disadvantage to SDFL lies in poor fanout which can be cured by the addition of a follow-on buffer circuit, but this brings the power consumption of the circuit up to that of BFL. Another disadvantage of SDFL is each gate may require individual crafting of the element sizes, which in turn may cascade into a whole series of requisite design changes. For an example of a DTL NOR gate, see Figure 3.5 on page 10.

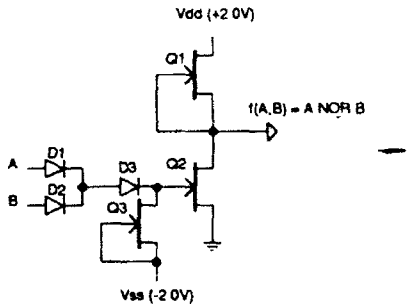


Figure 3.5 Gallium Arsenide DTL NOR gate [Ref. 1:p. 8]

The DTL NAND requires even more diodes and MESFETs than the DTL NOR. For an example of a DTL NAND gate, see Figure 3.6 on page 11.

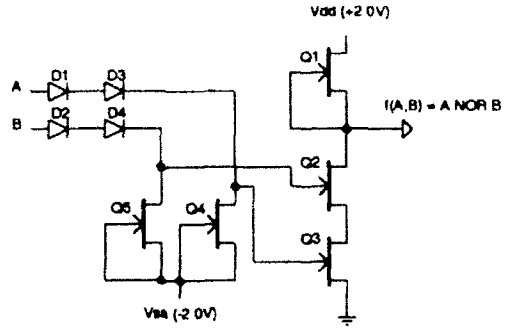


Figure 3.6 Gallium Arsenide DTL NAND gate [Ref. 1:p. 8]

B. GALLIUM ARSENIDE ENHANCEMENT-MODE LOGIC FAMILIES

Thus far, the discussion of GaAs logic families has been restricted to depletion-mode MESFETs. Enhancement-mode (normally off) GaAs MESFETs may also be used to implement logic functions and circuits. Because the e-mode MESFET may be turned off with a V_{GS} of 0 volts, now V_{DS} and V_{GS} are both positive, no level-shifting is required, and this allows the use (generally) of a single power supply, V_{DD}. Additionally, the saturation voltage $V_{D,sat}$ of an e-mode MESFET is less than that of a d-mode MESFET and this allows for lower power supply voltages which yields chip real estate savings and lower power consumption. The smaller logic voltage swing, 0.0V to a maximum of 0.7V (limited by forward conduction), may provide very high switching speeds.

Among the disadvantages of e-mode MESFETs are, first, the aforementioned smaller logic voltage swing requires careful uniformity of threshold voltages which places additional constraints on the fabrication process. A second disadvantage of e-mode MESFETs is that they are not particularly suited to being used as active loads because the charging current diminishes as the voltage across the load capacitor increases. This requires the use of d-mode MESFETs for the active load current sources of e-mode logic circuits.

1. Direct-Coupled FET Logic (DCFL)

DCFL provides the simplest and most widely used GaAs e-mode logic circuits. See Figure 3.7 on page 12 for an example of a DCFL 2-input NOR gate. Note the similarity between the mixed GaAs e-mode / d-mode MESFETs used there and those of E/D NMOS circuits. The active load, current source pull-up is accomplished using the aforementioned d-mode MESFET (Q1).

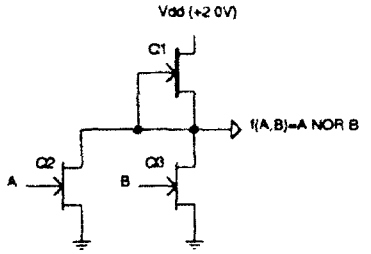


Figure 3.7 Gallium Arsenide DCFL NOR gate [Ref. 1:p. 10]

The DCFL NAND gate is very similar is structure to the NAND gates previously presented. The use of the active pull-up (Q1) precludes the previously used follow-on stages. See Figure 3.8 on page 12 for an example of DCFL NAND gate. It should been mentioned again that the use of so called "real" NAND gates is infrequent because of the series MESFETs, Q2 & Q3. These series MESFETs slow the operation of the circuit and therefore NAND gates constructed of NOR gates are almost exclusively used.

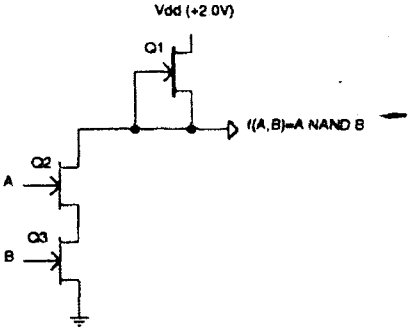


Figure 3.8 Gallium Arsenide DCFL NAND gate [Ref. 1:p. 10]

At this point it is illustrative to introduce the most basic logic gate, that of an inverter. See Figure 3.9 on page 13 for an example of a DCFL inverter logic gate. The symbol "/" preceding the "A" means "NOT A".

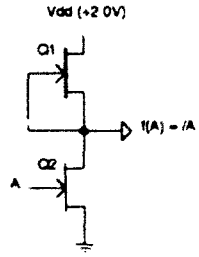


Figure 3.9 Gallium Arsenide DCFL INVERTER gate [Ref. 1:p. 11]

DCFL logic circuits offer fast switching speed but small noise margins (on the order of 200 millivolts, both high and low). These small noise margins require that the fabrication process pay particular attention to the material integrity and process parameters. Additionally, the fanout load for DCFL logic circuits is generally limited to two DCFL logic gates. The constraints placed on the logic designer by DCFL logic's low fanout and smaller noise margins lead to the incorporation of a buffer stage, this subfamily of DCFL is known as superbuffer FET logic. The topic GaAs DRAM integrated circuit chip was designed almost exclusively using DCFL and SBFL logic gates.

2. Superbuffer FET Logic (SBFL)

The peak load current - static current ratio of a DCFL inverter can be significantly improved through the addition of a quasi-complementary output driver (superbuffer). See Figure 3.10 on page 13 for the example schematic of a SBFL inverter.

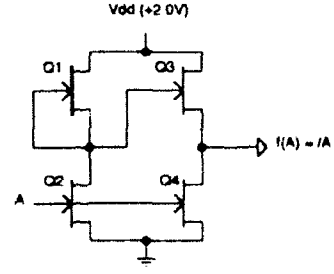


Figure 3.10 Gallium Arsenide SBFL INVERTER gate [Ref. 10:p. 215]

Note that the d-mode MESFET (Q1) acts again as an active load current source. Use of SBFL requires that the designer provide ample power bus width for the momentary voltage drop which occurs prior

to the HIGH to LOW transition. It is in instructive to note that once the DCFL inverter, transistors Q_1 and Q_2, passes its propagation delay, the load (connected between Q_3 and Q_4) will receive the full current capability of either Q_3 or Q_4. The addition of the superbuffer solves, to some extent, the poor fanout and smaller noise margin shortcomings of DCFL but adds propagation delay and requires more chip real estate in exchange. It should be mentioned that the static power of the SBFL driver (Q_3 and Q_4) is equal to the static power of the DCFL inverter (Q_1 and Q_2). A further illustration of SBFL gates, a SBFL NOR gate, may be seen in Figure 3.11 on page 14.

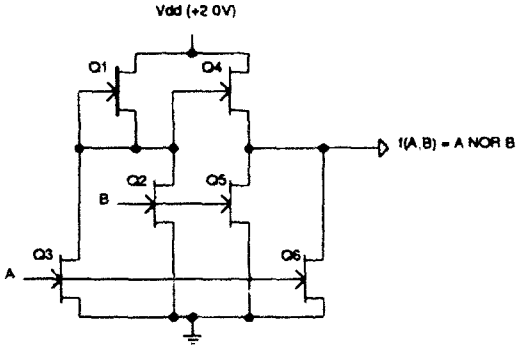


Figure 3.11 Gallium Arsenide SBFL NOR gate [Ref. 10:p. 215]

The extra chip real estate required and the increased power requirements of the superbuffer stage limit the use of the SBFL gates to those situations in which the fanout is unusually high and high speed is mandatory, such as clock drivers. This specific topic will be more thoroughly discussed in the succeeding chapters. One last note on SBFL, as noted on [Ref. 10:p. 216], a direct comparison between SBFL and DCFL ring oscillators yielded SBFL gate delays of 178 picoseconds and DCFL gates delays of 276 picoseconds.

3. Other GaAs E-mode Logic Families

Several other GaAs e-mode logic families exist: source-coupled FET logic (SCFL) which is very fast, E/D Buffered FET Logic (E/D BFL) which combines the best use of e-mode and d-mode GaAs MESFETs with BFL, pass transistor logic and complementary junction FET (JFET) logic. For a very thorough discussion of these additional GaAs e-mode logic families, the reader may peruse [Ref. 10:pp. 216-231].

The succeeding chapters will begin to discuss the actual logic elements used and the circuits which make up the GaAs DRAM.

IV. GALLIUM ARSENIDE DRAM LOW-LEVEL CIRCUITS

During the course of the design a multitude of different GaAs logic circuits were designed, tested and discarded for various reasons. Some of the reasons included poor noise margins and low fanout capabilities which did not become obvious until the target elements where placed into a larger circuit which then failed to function correctly. In addition, while no specific attempt was made at overall power consumption optimization, it was considered to be one of the factors while the design was in progress. The overriding factor that was used in judging the operation of the target GaAs logic element was a combination of speed and fanout. Early in the design cycle, little attention was paid to the mixing within a circuit of the various e-mode logic elements. After some time, it became obvious that DCFL will drive approximately two DCFL gates and perhaps as few as one SBFL gate, whereas SBFL could drive more than two DCFL gates, but usually at a slower speed. When germane, these issues will be mentioned in the discussion that follows.

A. GaAs DRAM DCFL Logic Circuits

The greatest majority of the GaAs DRAM circuits were designed using DCFL gates. This section will present the specific DCFL gates designed, tested, and used, presenting the schematic and logical equivalence for each. The following characteristics for each circuit will be demonstrated and presented: transient analysis under standard load, power consumption at nominal and high temperature, propagation delays and noise margins. These characteristics will be further summarized in TABLE 4.1 on page 158.

1. DCFL Inverter (DINV)

The basic and most widely used DCFL logic element was the inverter, hereafter called "DINV" for DCFL Inverter. As previously mentioned, true NAND gates were infrequently used, the more common ANDs, NANDs, and ORs were built using NORs with DINVs as per DeMorgan's theorems. See Figure 4.1 on page 16 for the DINV schematic and logical equivalence.

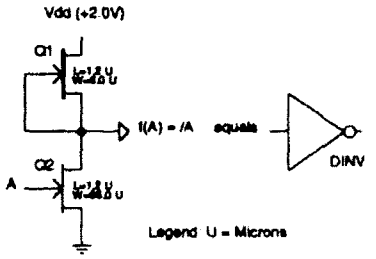


Figure 4.1 Schematic and Logical Equivalence for DINV

The following graph, Figure 4.2 on page 17, shows the output of the DINV for the input of a 50% duty cycle 4200 picosecond (ps) square wave with an input LOW (L) = 0.063V and HIGH (H) = 0.63V. The DINV was tested with two DINVs connected in parallel to the output as a standard DCFL load. Notice how the LOW to HIGH transition is somewhat slower than the HIGH to LOW transition. This is caused by the use of the active load pull-up Q1 (see Figure 4.1 on page 16). The pull-up transistor never turns completely off and this causes the delay in the LOW to HIGH transition. Similar LOW to HIGH transition characteristics are displayed by E/D NMOS logic circuits. The lower graph of Figure 4.2 on page 17 indicates the power dissipation of DINV operating at a temperature of 25.0C under a standard load of two DCFL Inverters (DINVs). See "Listing File for DINV Transient Analysis at 25.0C" of Appendix A on page 259.

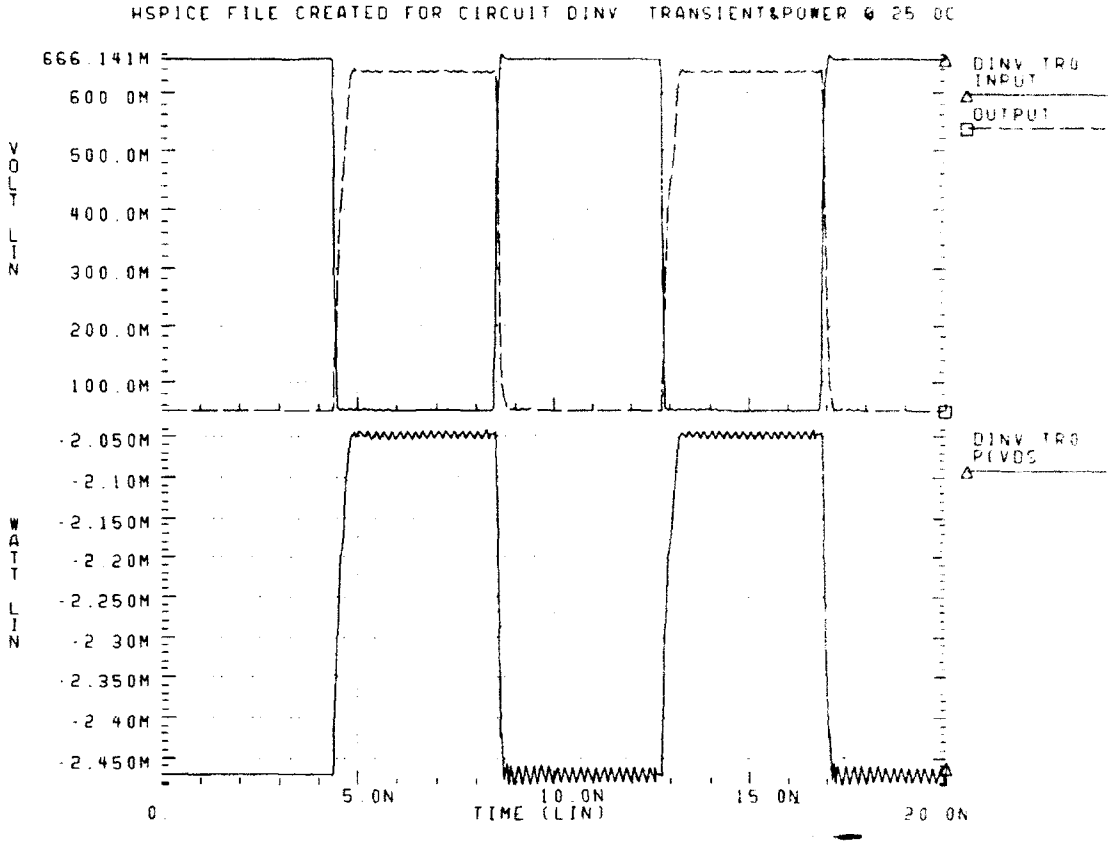


Figure 4.2 DINV HSPICE Transient Analysis and Power Dissipation at 25.0C

Temperature affects both the transient analysis and the DC transfer curve characteristics (from which the noise margins are calculated) for GaAs circuits. Whereas Figure 4.2 on page 17 (lower graph) shows the transient analysis of the DINV at room temperature (25.0C), Figure 4.3 on page 18 indicates the increased power consumption and slightly slower speed of the same circuit operating at 85.0C.

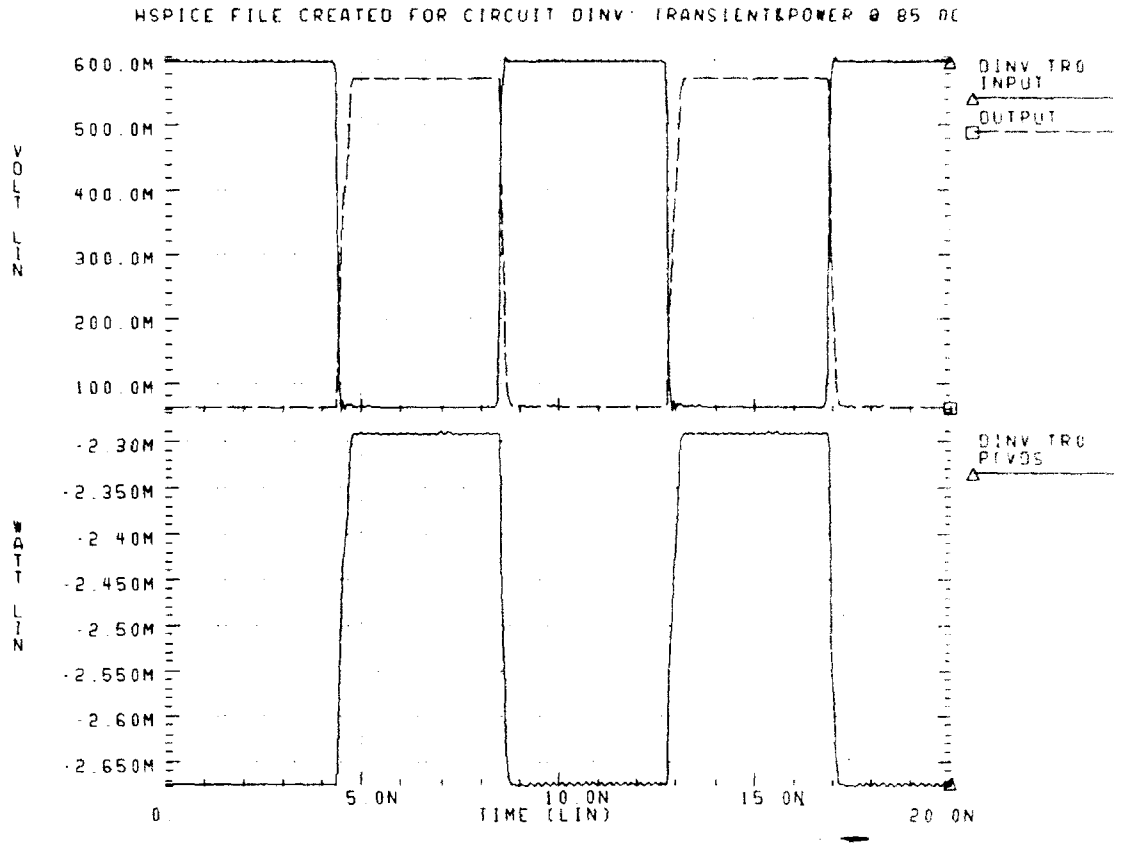


Figure 4.3 DINV HSPICE Transient Analysis and Power Dissipation at 85.0C

The noise margin calculations are calculated from the DC transfer curve for a DINV logic gate operating at 25.0C. See Figure 4.4 on page 19 for this graph. The noise margin calculation procedures are presented in this figure as used. This is the only example offered of noise margin calculation procedures though the noise margins for all the logic gates have been calculated and will be summarized in TABLE 4.1 on page 158. Reviewing Figure 4.4 on page 19, it is obvious that the noise margins are not as well balanced (NM_L versus NM_H) as may be desired. The cause of this shift of balance between NM_L and NM_H is the ratio of the physical size of the DINV pull-up MESFET relative to the size of the DINV pull-down MESFET. (See the DINV MESFET sizes in Figure 4.1 on page 16). One of the GaAs logic circuit design rules is maintenance of a sixteen-to-one of pull-down to pull-up size ratio. This rule allows for some variance as the DINV was designed with a 1-to-1 ratio on the "front end" and a sixteen-to-1 ratio on the "back end". Not splitting the Gallium Arsenide MESFET gate length versus gate width ratio into the idealized 2-to-1 for gate length and 8-to-1 for gate width is the cause of these skewed noise margins.

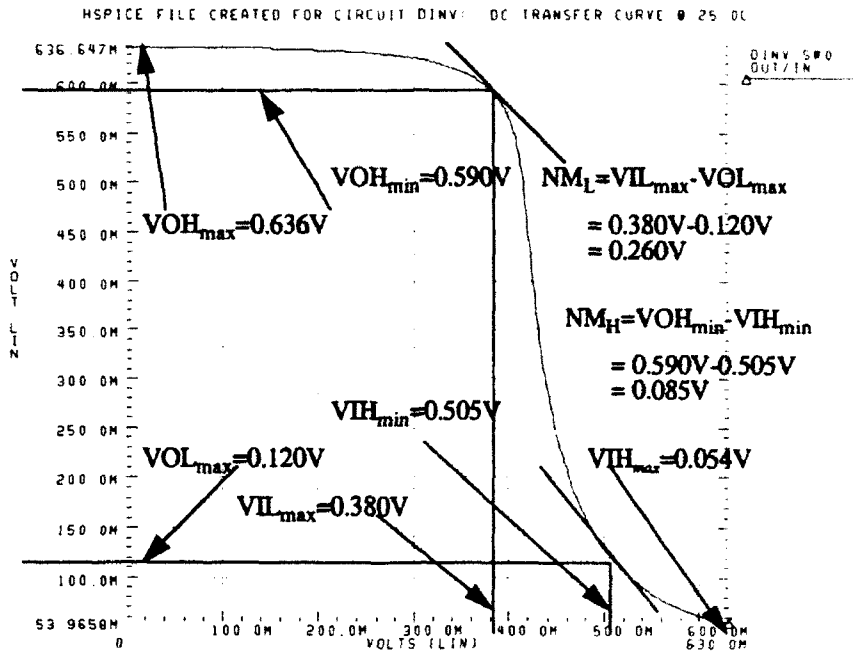


Figure 4.4 DINV DC Transfer Curve at 25.0C

The operating temperature of the circuit affects the noise margins as well as power dissipation and transient operating characteristics, see Figure 4.5 on page 20 for the DC transfer curve for a DINV logic gate operating at 85.0C. One can see that the relative position of the DC transfer curve has shifted somewhat, though the noise margins were not improved significantly. See TABLE 4.1 on page 158 for the specific noise margins for each logic gate.

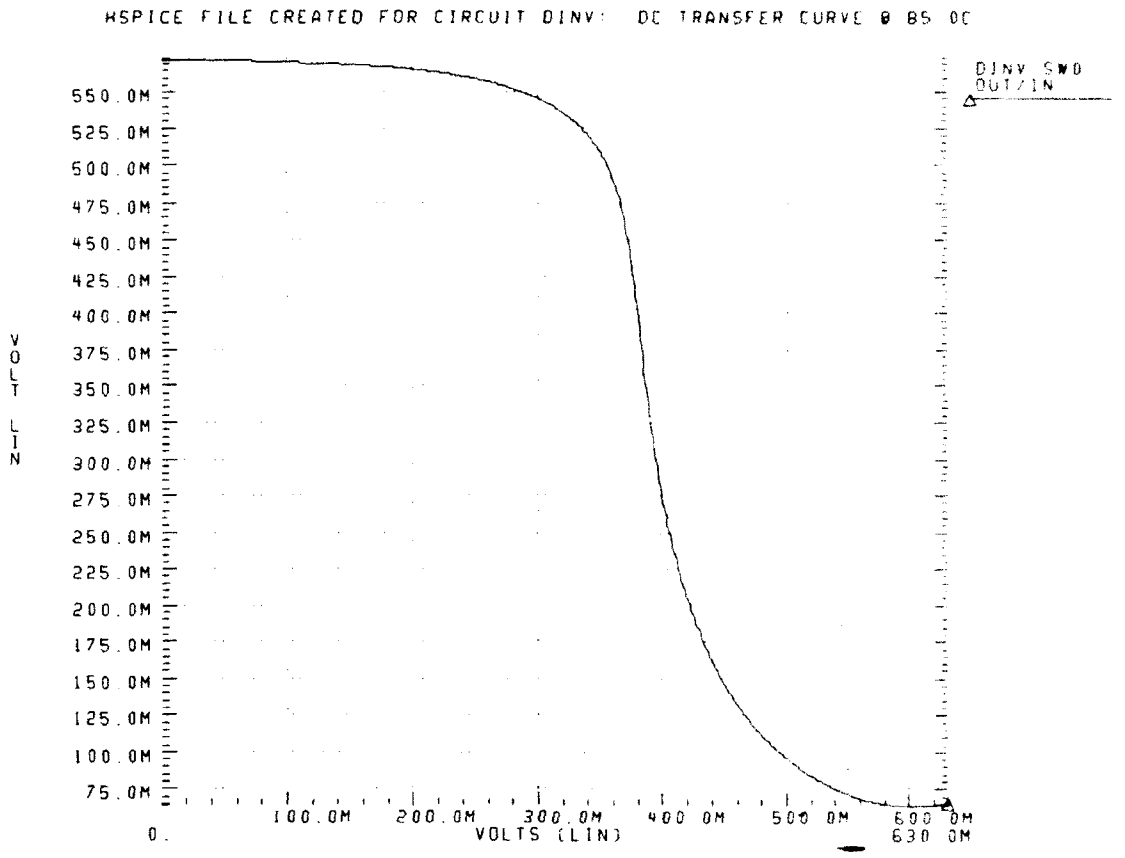


Figure 4.5 DINV DC Transfer Curve at 85.0C

2. DCFL 2-Input NOR (D2NOR)

The following graphs represent the operating characteristics of the D2NOR. The D2NOR schematic and logical representation are shown in Figure 4.6 on page 21. Figure 4.7 on page 21 indicates the transient analysis and power dissipation of the D2NOR logic gate at an operating temperature of 25.0C. The transient voltage spike shown in the output of Figure 4.7 (upper graph) (occurring at approximately 8.0 nanoseconds) is a result of non-overlapping input signals. That is to say, the first input signal goes LOW before the second input signal goes HIGH, consequently, the output begins to change from LOW to HIGH.

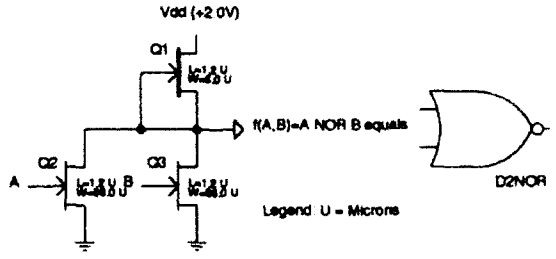


Figure 4.6 D2NOR Schematic and Logical Equivalence

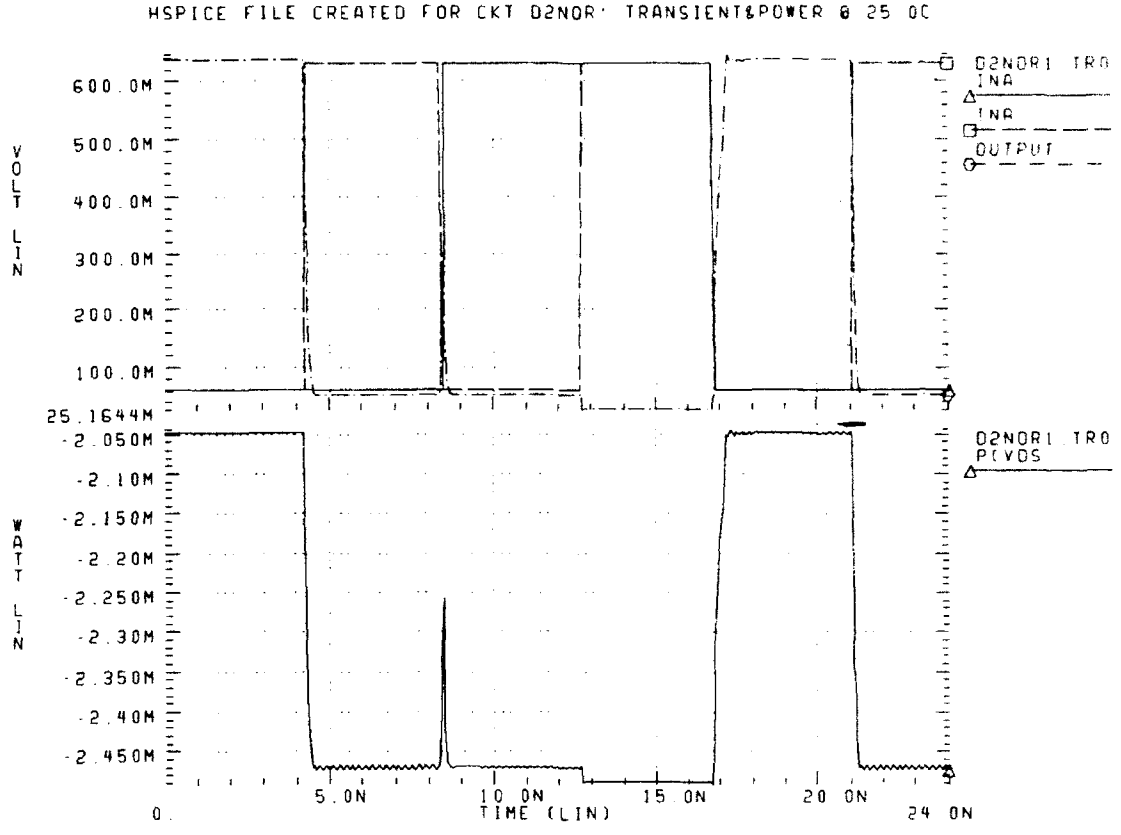


Figure 4.7 D2NOR HSPICE Transient Analysis and Power Dissipation at 25.0C.

Transient analysis and power dissipation for the D2NOR logic gate operating at 85.0C is displayed in Figure 4.8 on page 22. Notice the increased power dissipation caused by the higher operating temperature.

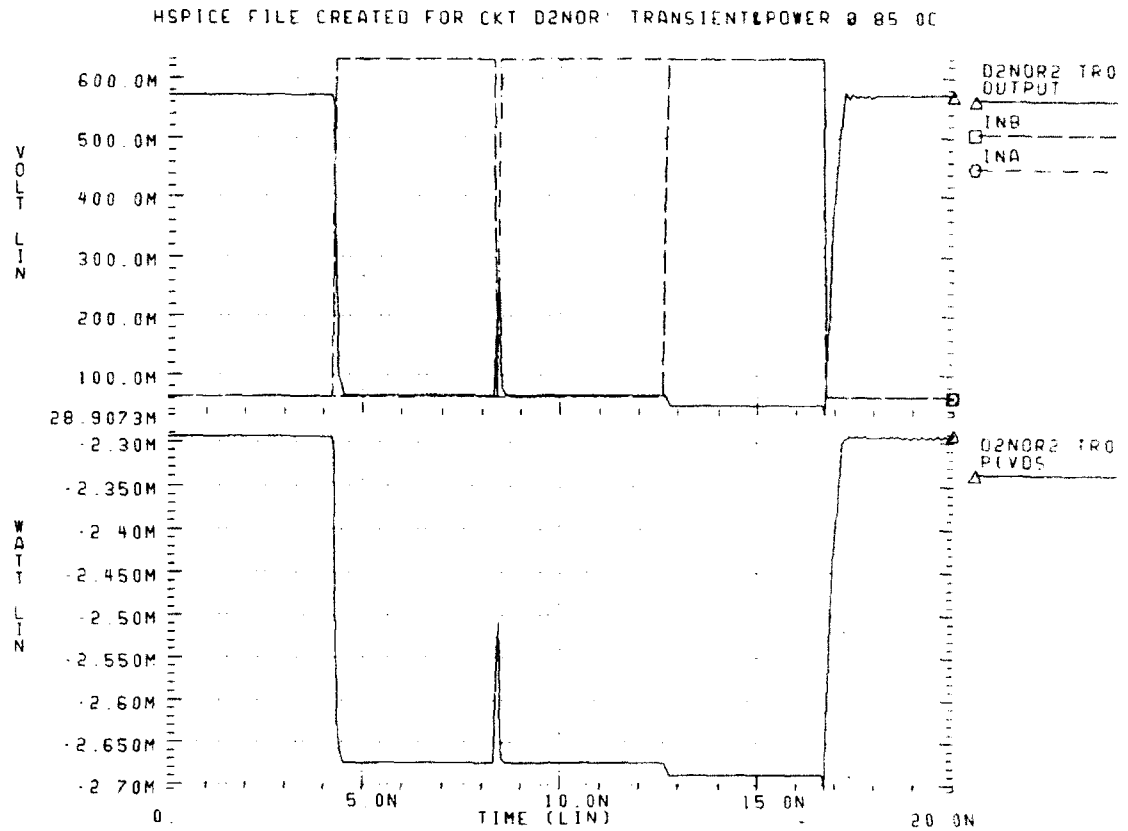


Figure 4.8 D2NOR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the D2NOR logic gate operating at a temperature of 25.0C is shown in Figure 4.9 on page 23. Notice that in Figure 4.9, the DC transfer curve is again "skewed" or shifted. The same conscious design decision is again the culprit. See the previous discussion on skewed noise margins.

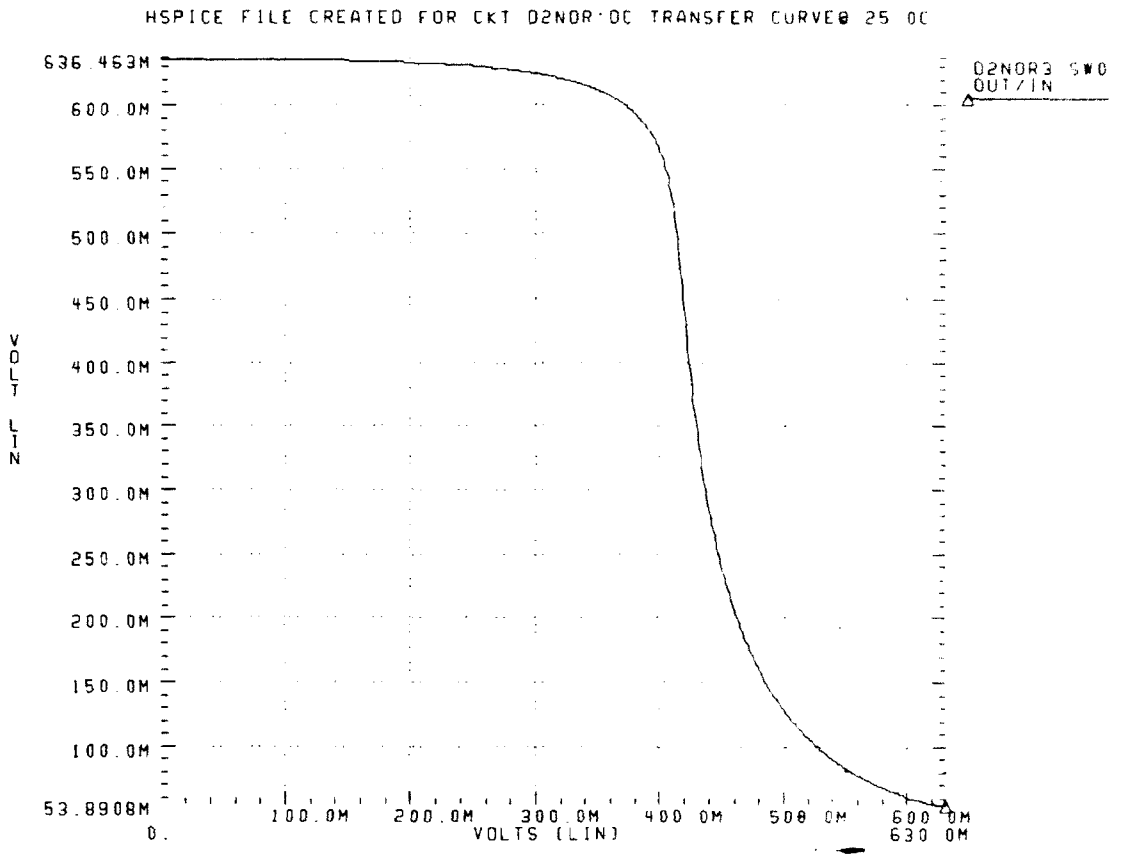


Figure 4.9 D2NOR DC Transfer Curve at 25.0C

The DC transfer characteristic of the D2NOR logic gate operating at a temperature of 85.0C is shown in Figure 4.10 on page 24.

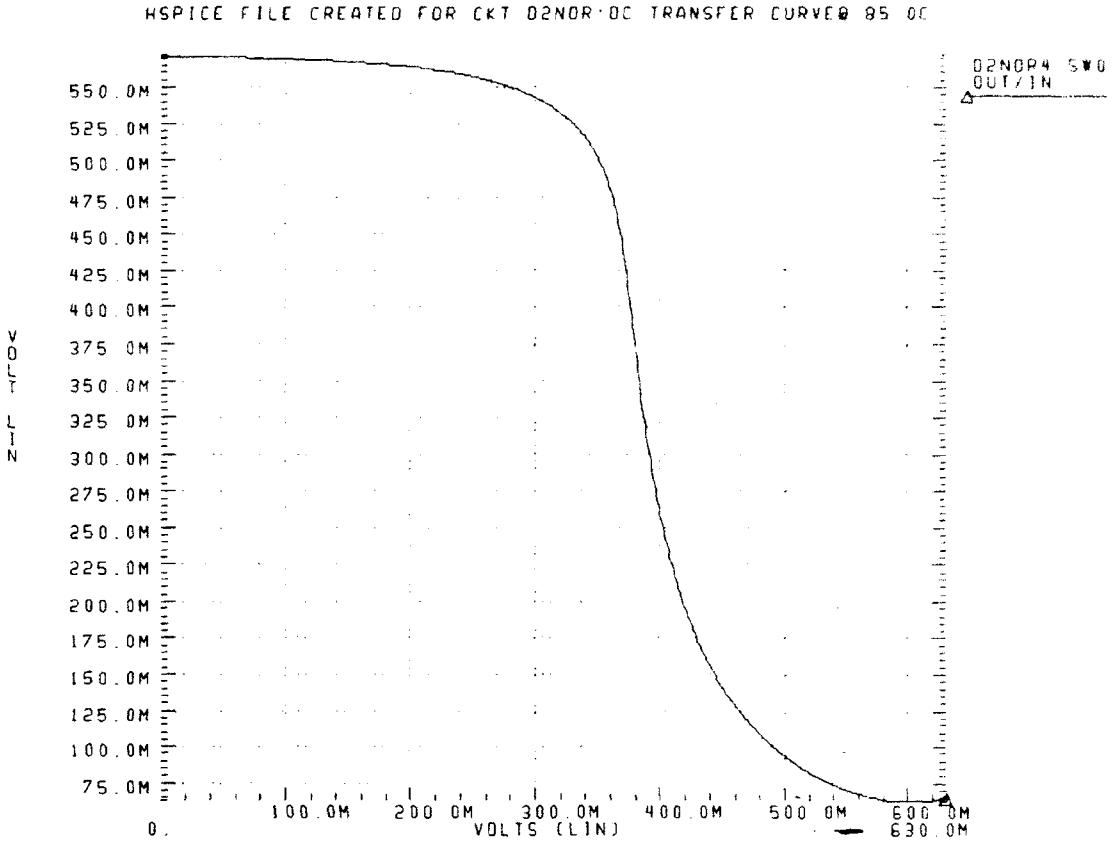


Figure 4.10 D2NOR DC Transfer Curve at 85.0C

3. DCFL 3-input NOR (D3NOR)

The following graphs represent the operating characteristics of the D3NOR. As previously mentioned, most GaAs DRAM logic gates were constructed of NORs, specifically DCFL NOR gates. The D3NOR schematic and logical representation are shown in Figure 4.11 on page 25. Notice again the sizing of the MESFETs and its associated effect on transient operation and noise margins.

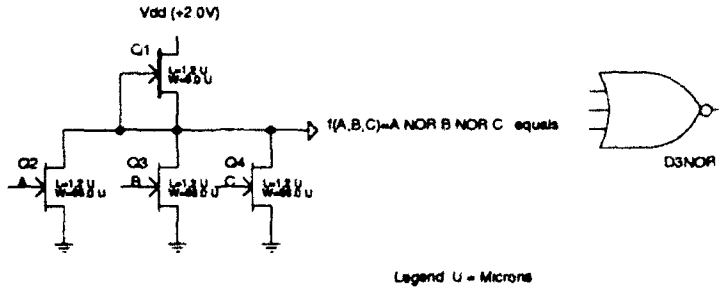


Figure 4.11 D3NOR Schematic and Logical Equivalence

Figure 4.12 on page 26 represents the transient analysis and power dissipation of the D3NOR logic gate at an operating temperature of 25.0C. The transient voltage spikes shown in the output of Figure 4.12 (upper graph) (occurring at approximately 9 nanoseconds and 17 nanoseconds) result from non-overlapping input signals as previously mentioned. It is interesting to note that the majority of the power dissipation occurs when the output is HIGH.

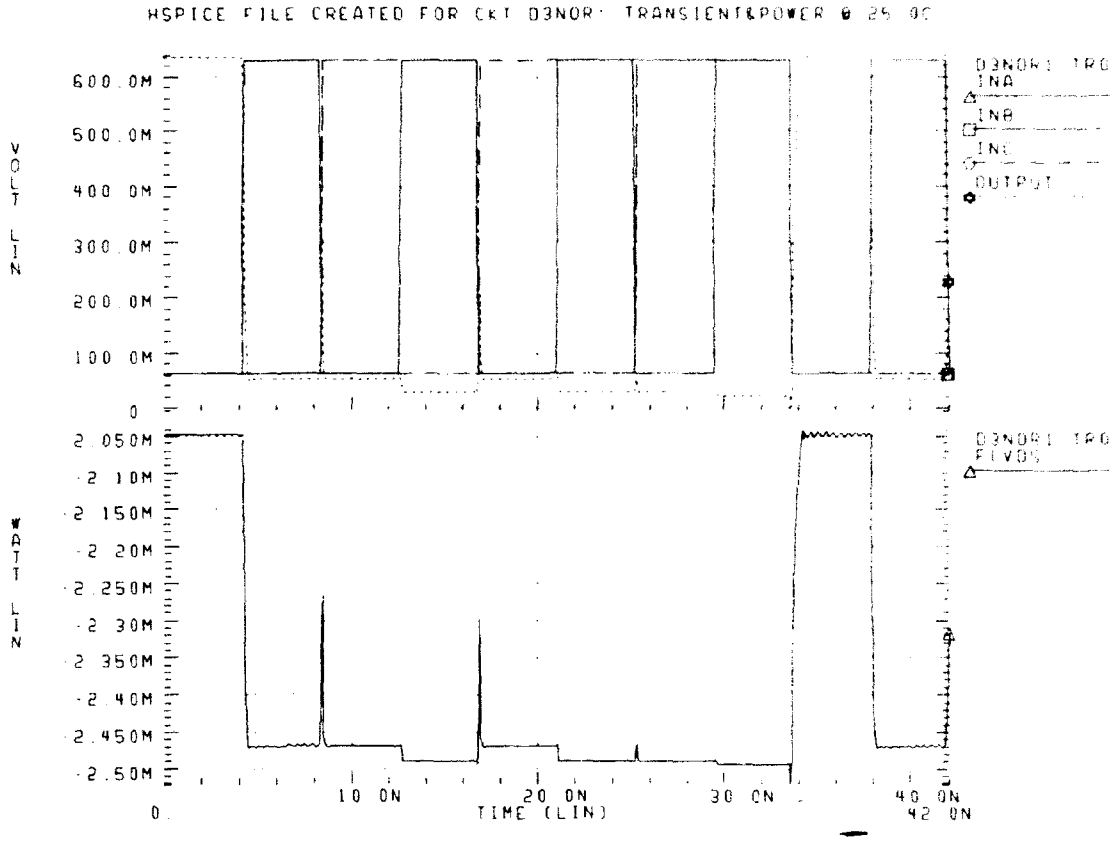


Figure 4.12 D3NOR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the D3NOR operating at a temperature of 85.0C is shown in Figure 4.13 on page 27.

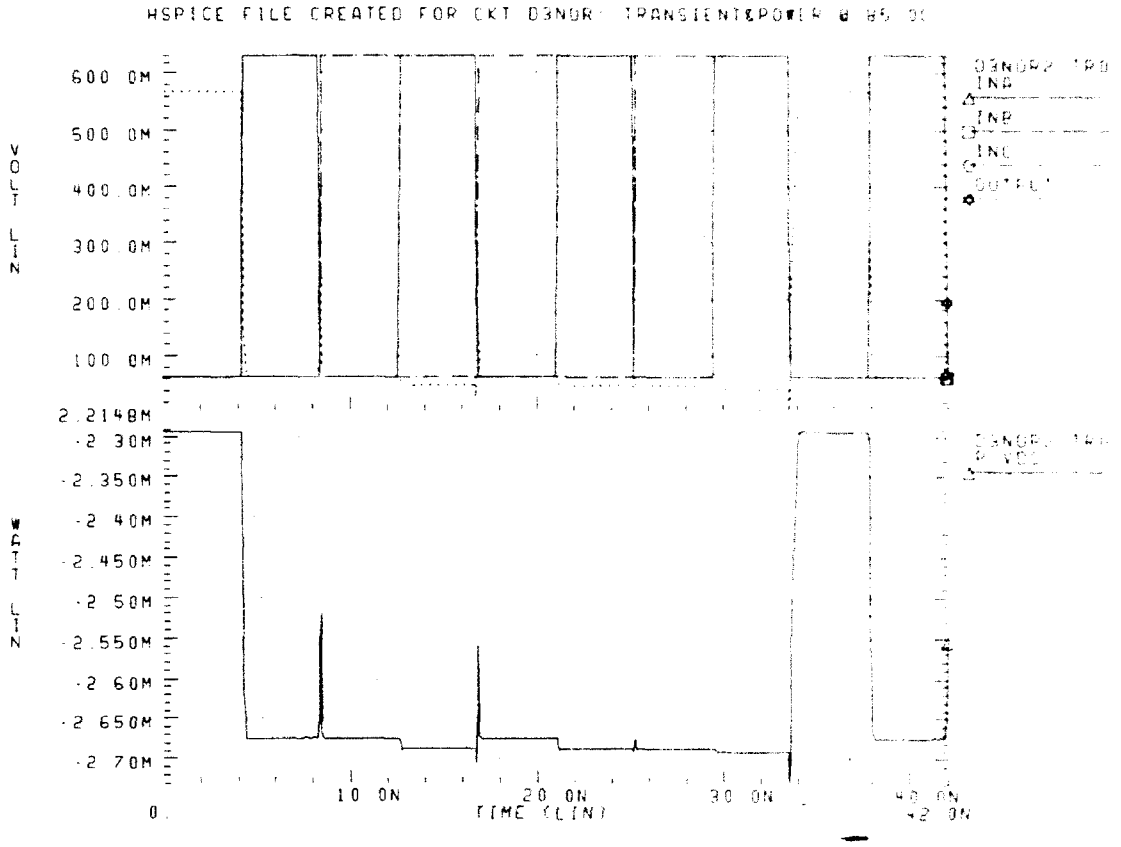


Figure 4.13 D3NOR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the D3NOR logic gate operating at a temperature of 25.0C is shown in Figure 4.14 on page 28.

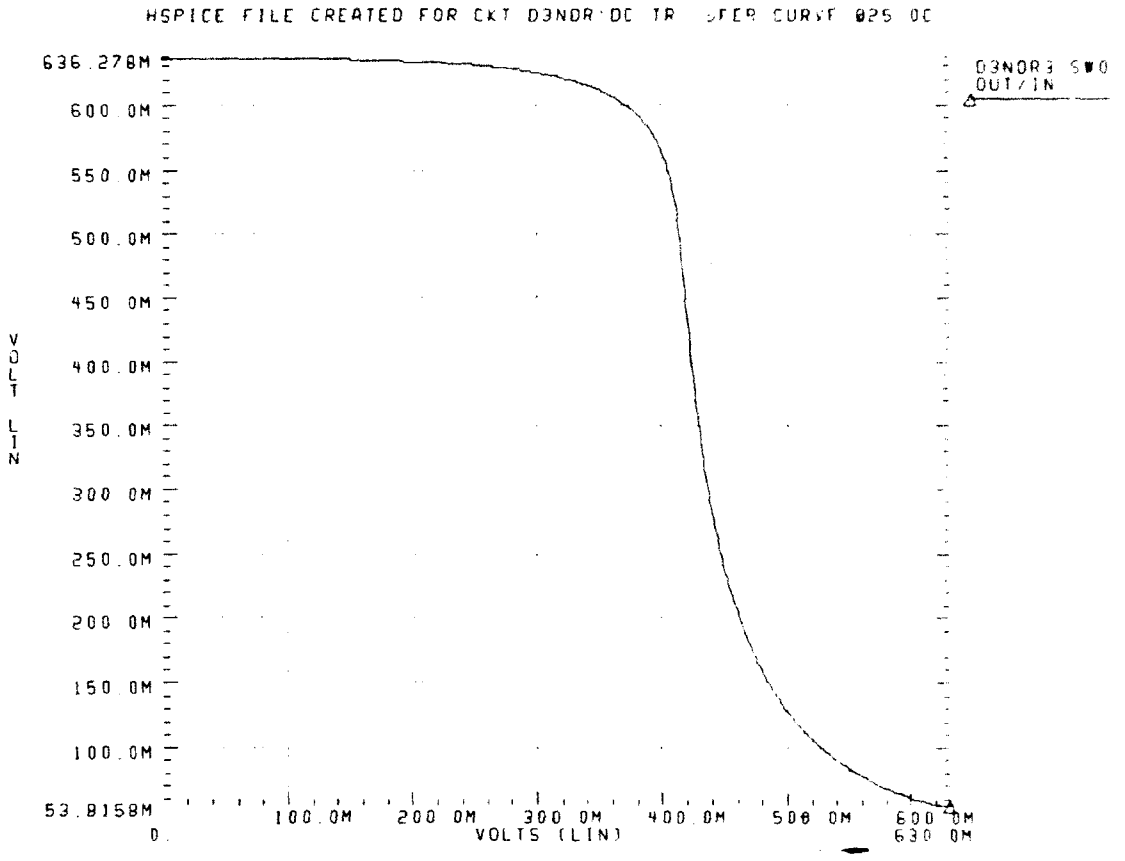


Figure 4.14 D3NOR DC Transfer Curve at 25.0C

The DC transfer characteristic of the D3NOR logic gate operating at a temperature of 85.0C is shown in Figure 4.15 on page 29.

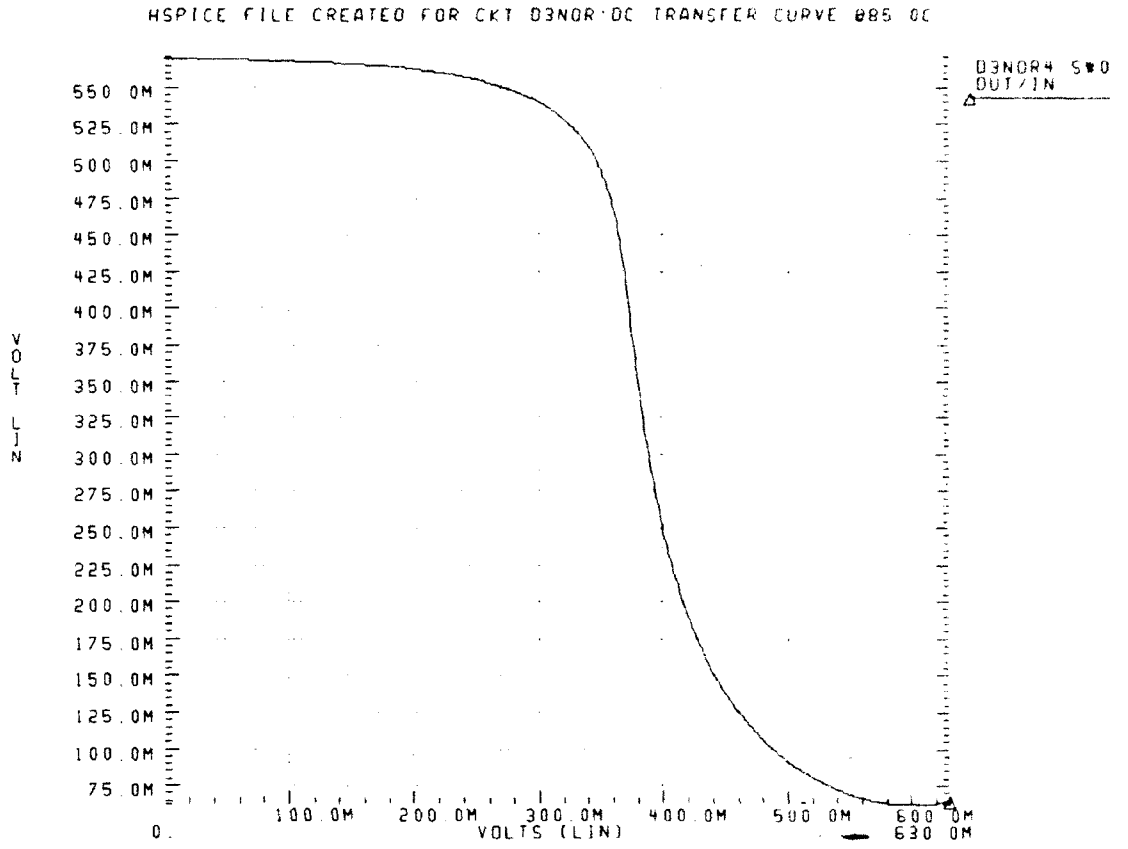


Figure 4.15 D3NOR DC Transfer Curve at 85.0C

4. DCFL 4-Input NOR Gate (D4NOR)

The following graphs represent the operating characteristics of the D4NOR. As previously mentioned, most GaAs DRAM logic gates were constructed of NOR's, specifically DCFL NOR gates. The D4NOR schematic and logical representation are shown in Figure 4.16 on page 30. Notice again the sizing of the MESFETs and its associated effect on transient operation and noise margins.

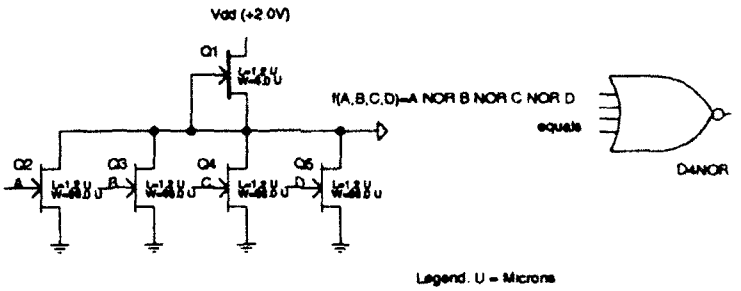


Figure 4.16 D4NOR Schematic and Logical Equivalence

The transient analysis and power dissipation of the D4NOR logic gate operating at a temperature of 25.0C is shown in Figure 4.17 on page 30. See "Listing File for D4NOR Transient Analysis @ 25.0C" of Appendix A on page 262.

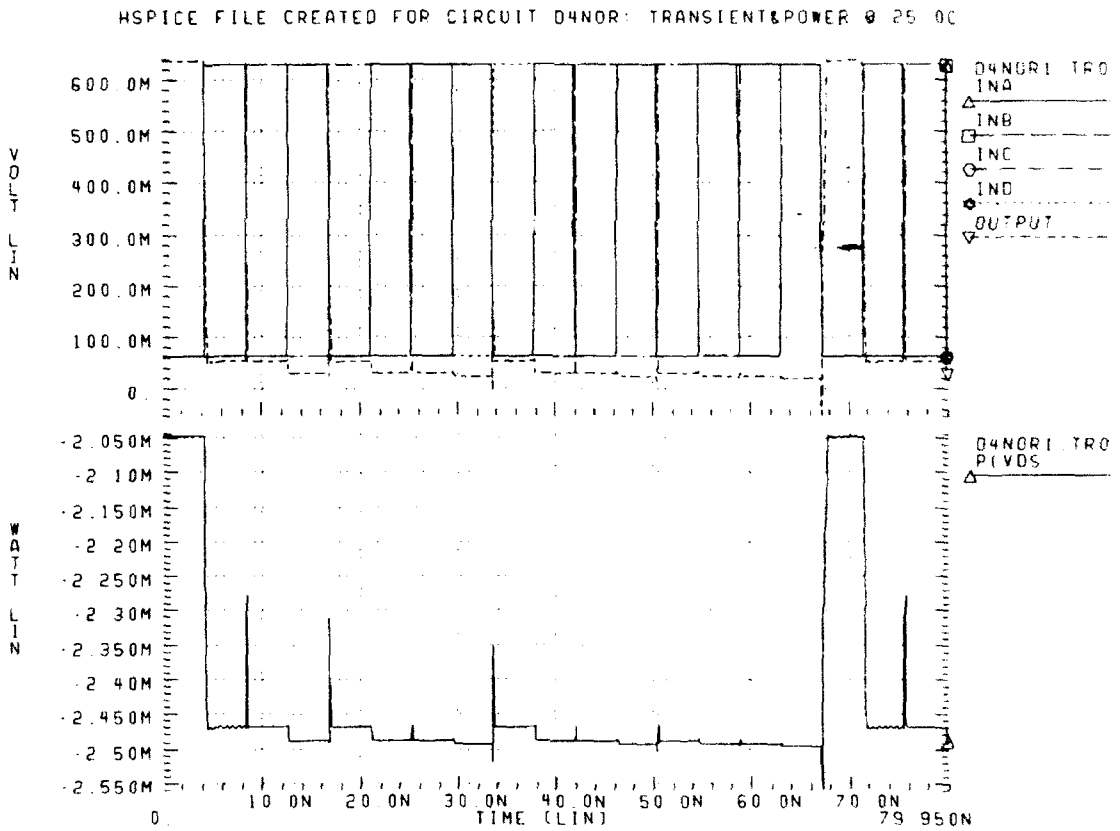


Figure 4.17 D4NOR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the D4NOR operating at a temperature of 85.0C is shown in Figure 4.18 on page 31.

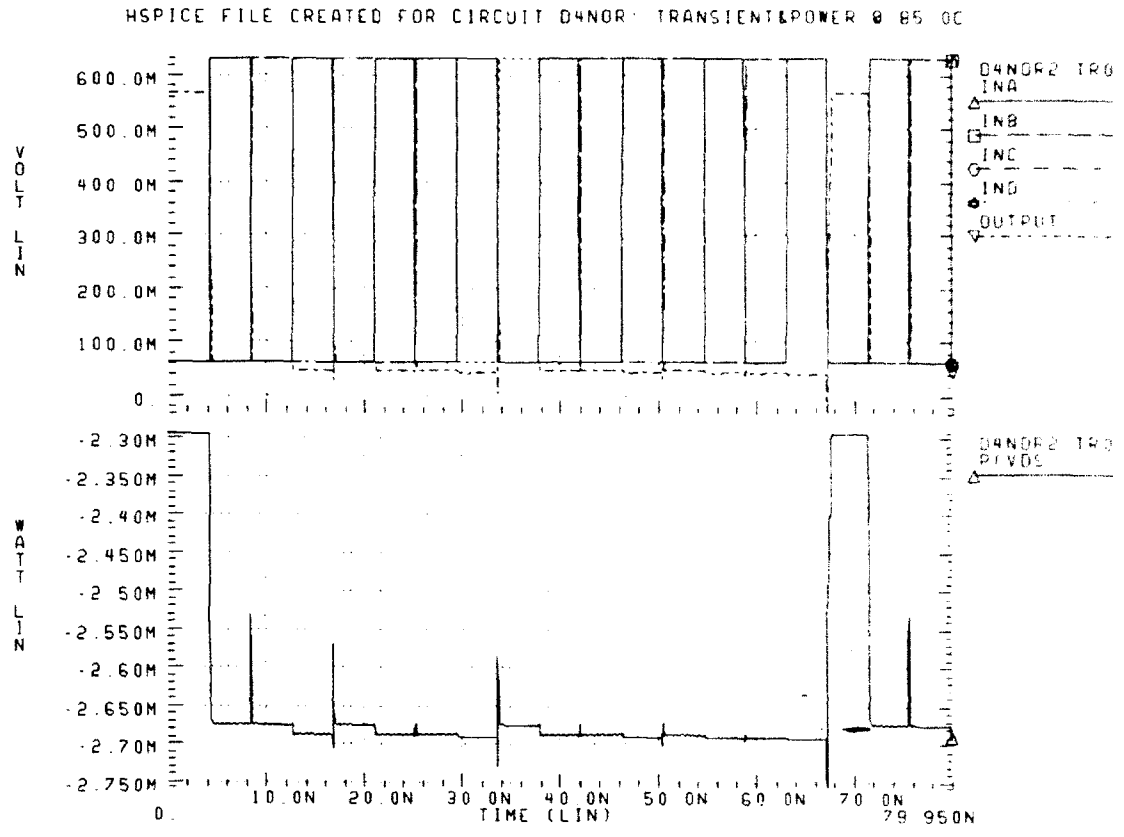


Figure 4.18 D4NOR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the D4NOR logic gate operating at a temperature of 25.0C is shown in Figure 4.19 on page 32.

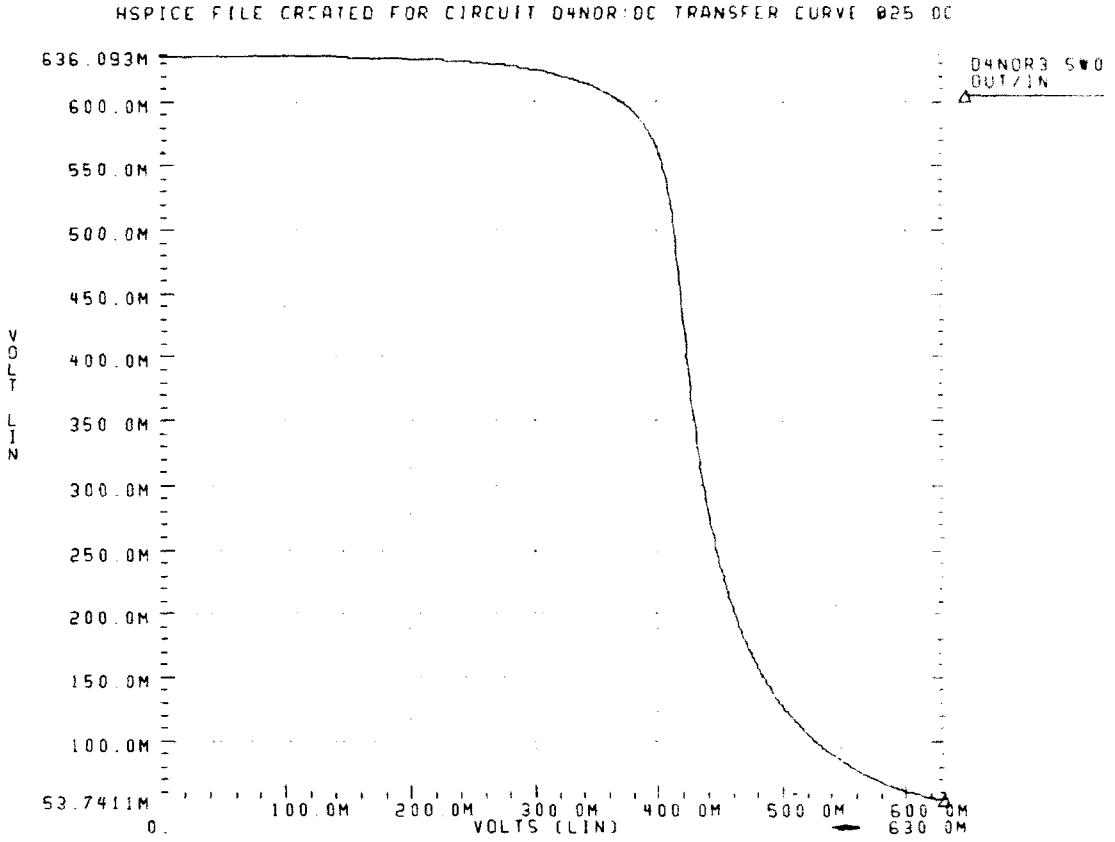


Figure 4.19 D4NOR DC Transfer Curve at 25.0C

The DC transfer characteristic of the D4NOR logic gate operating at a temperature of 85.0C is shown in Figure 4.20 on page 33.

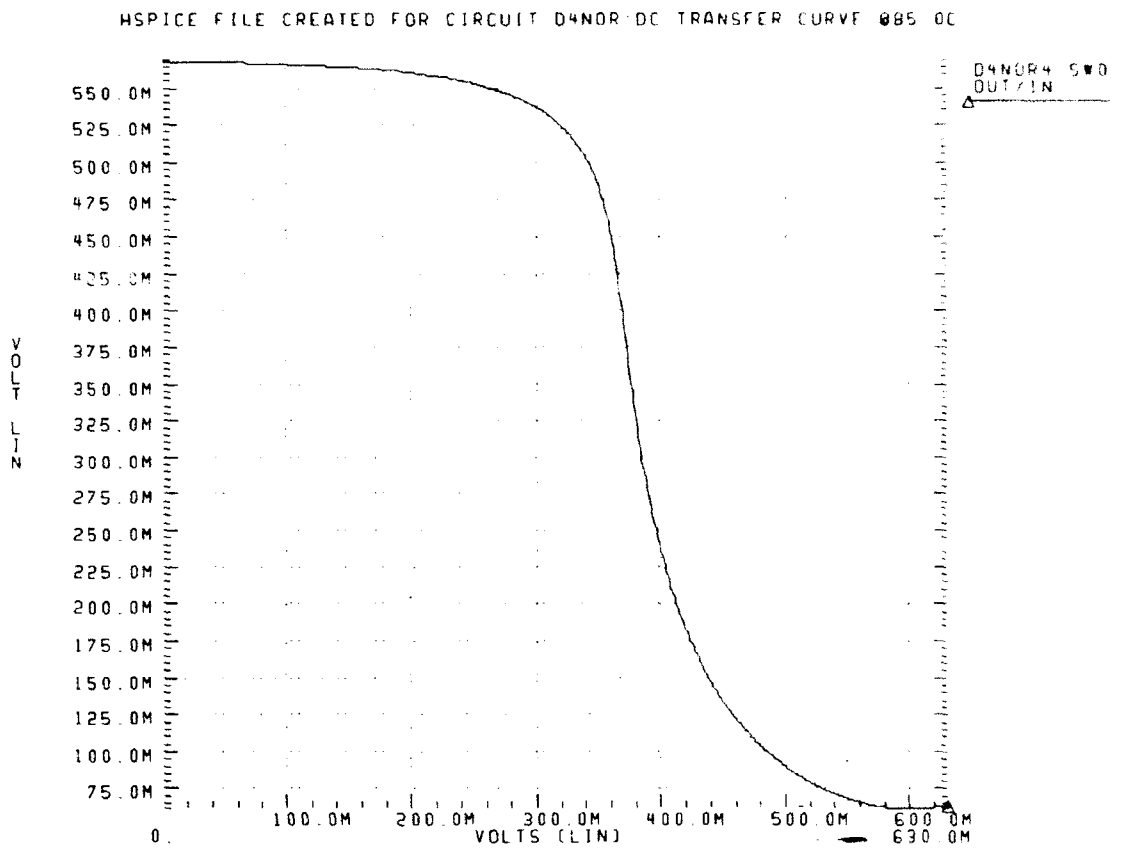


Figure 4.20 D4NOR DC Transfer Curve at 85.0C

5. DCFL 2-input True NAND Gate (D2NAND)

As previously mentioned, the largest majority of the DCFL GaAs DRAM logic gates are constructed from DCFL NOR gates. This gate, D2NAND, is an exception. It was necessary to use a true NAND gate in two fundamental circuits of the GaAs DRAM. These circuits are DLATCH and SDLATCH. The true NAND gate is very fast but as shown by its physical size in Figure 4.21 on page 34, it occupies considerable chip real estate. Figure 4.21 on page 34 presents the D2NAND schematic and logical equivalence.

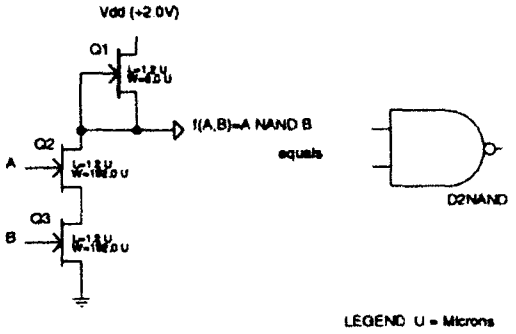


Figure 4.21 D2NAND Schematic and Logical Equivalence

The transient analysis and power dissipation of the D2NAND operating at a temperature of 25.0C is shown in Figure 4.22 on page 34.

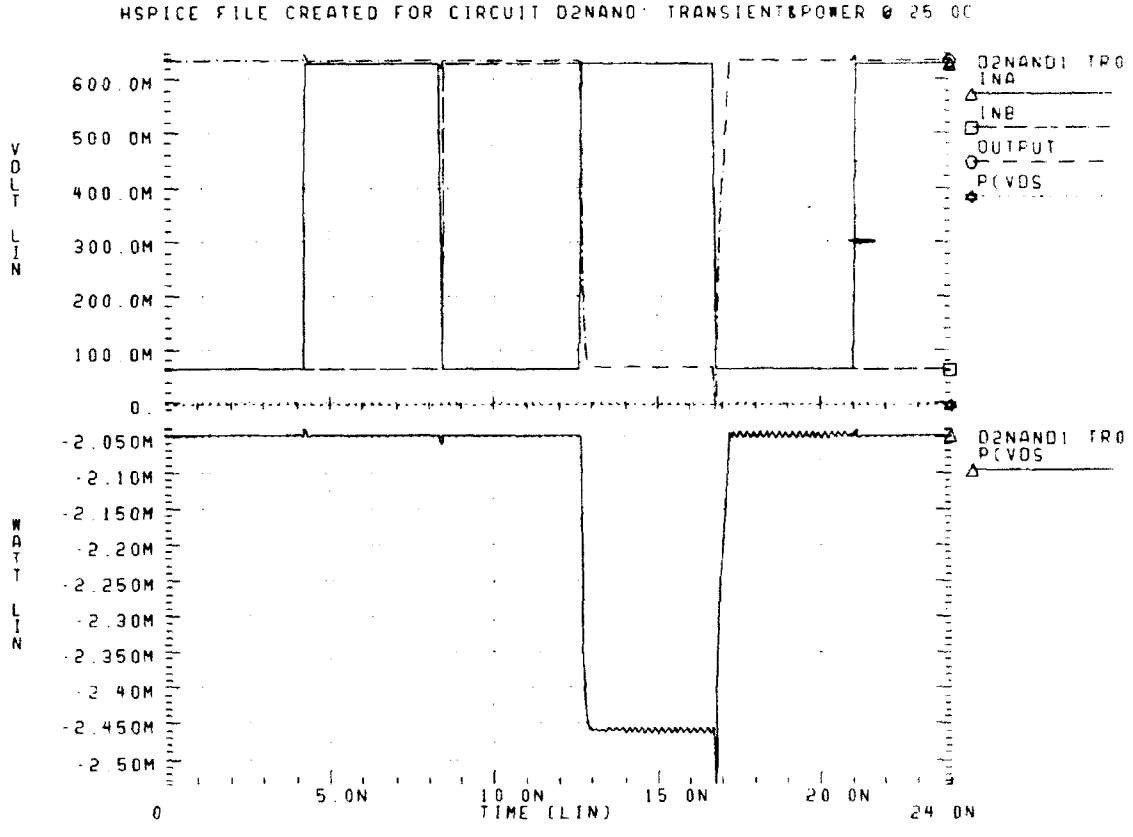


Figure 4.22 D2NAND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the D2NAND operating at a temperature of 85.0C is shown in Figure 4.23 on page 35.

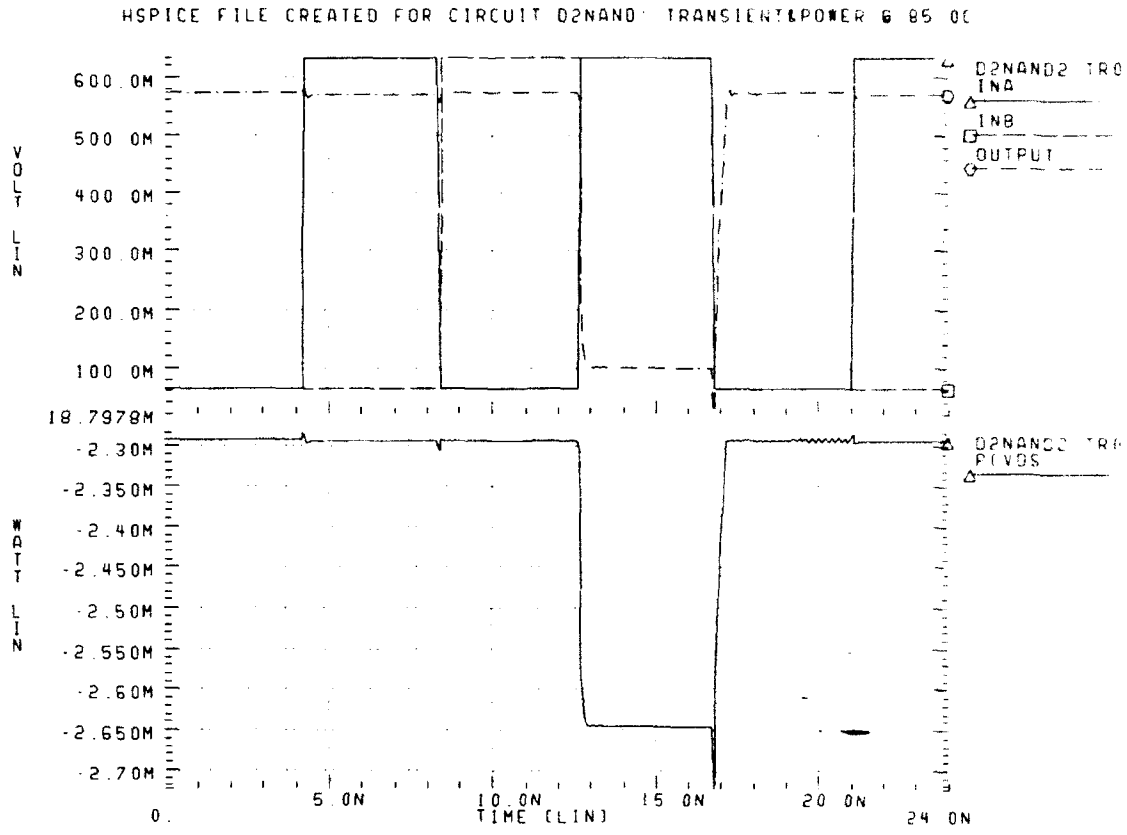


Figure 4.23 D2NAND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the D2NAND logic gate operating at a temperature of 25.0C is shown in Figure 4.24 on page 36.

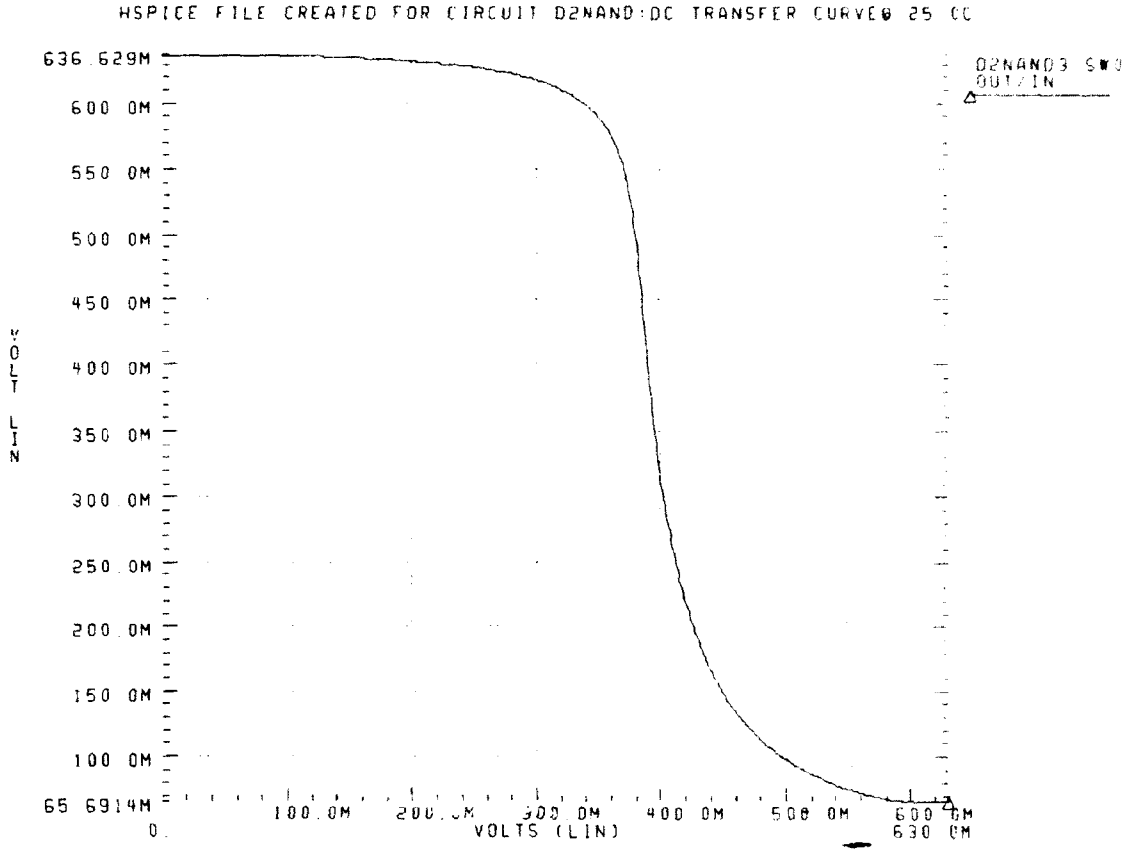


Figure 4.24 D2NAND DC Transfer Curve at 25.0C

The DC transfer characteristic of the D2NAND logic gate operating at a temperature of 85.0C is shown in Figure 4.25 on page 37.

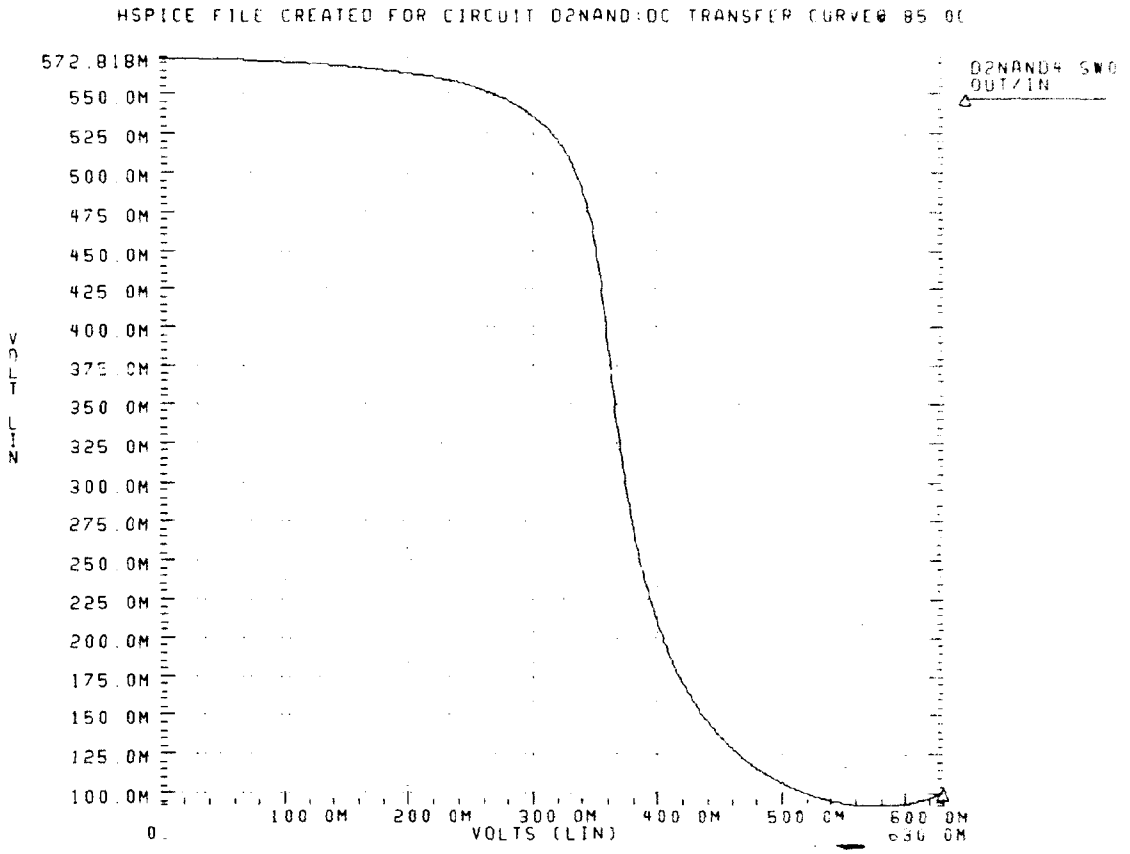


Figure 4.25 D2NAND DC Transfer Curve at 85.0C

6. DCFL 2-input NAND Gate (DD2NAND)

A DD2NAND logic gate is constructed using the DeMorgan equivalent of a D2NOR with two DINVs on its inputs and one DINV on its output. The end result is a DCFL 2-input NAND gate and Figure 4.26 on page 37 presents the DD2NAND schematic and logical equivalence.

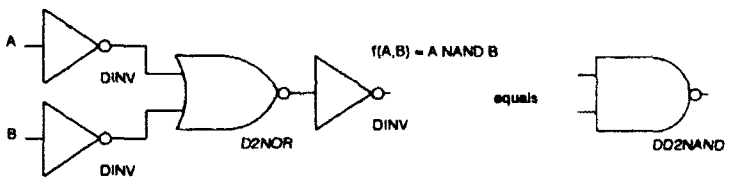


Figure 4.26 DD2NAND Schematic and Logical Equivalence

The transient analysis and power dissipation of the DD2NAND operating at a temperature of 25.0C is shown in Figure 4.27 on page 38.

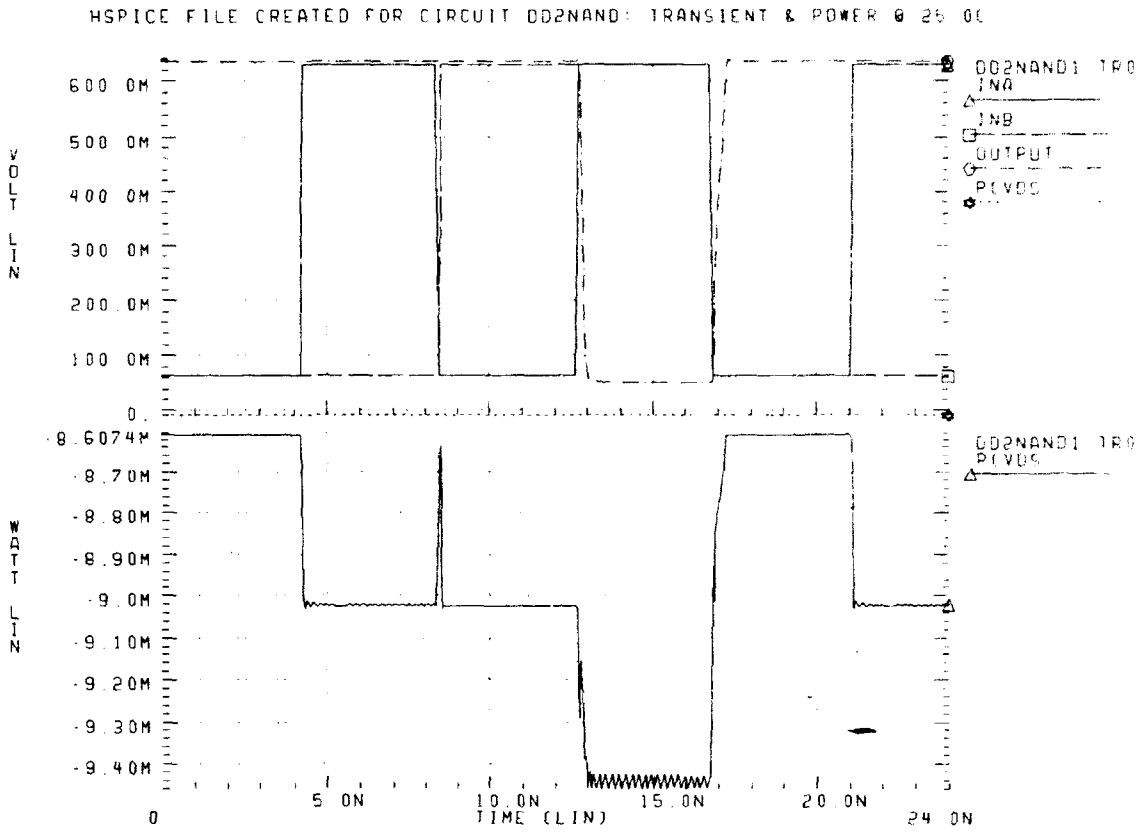


Figure 4.27 DD2NAND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DD2NAND operating at a temperature of 85.0C is shown in Figure 4.28 on page 39.

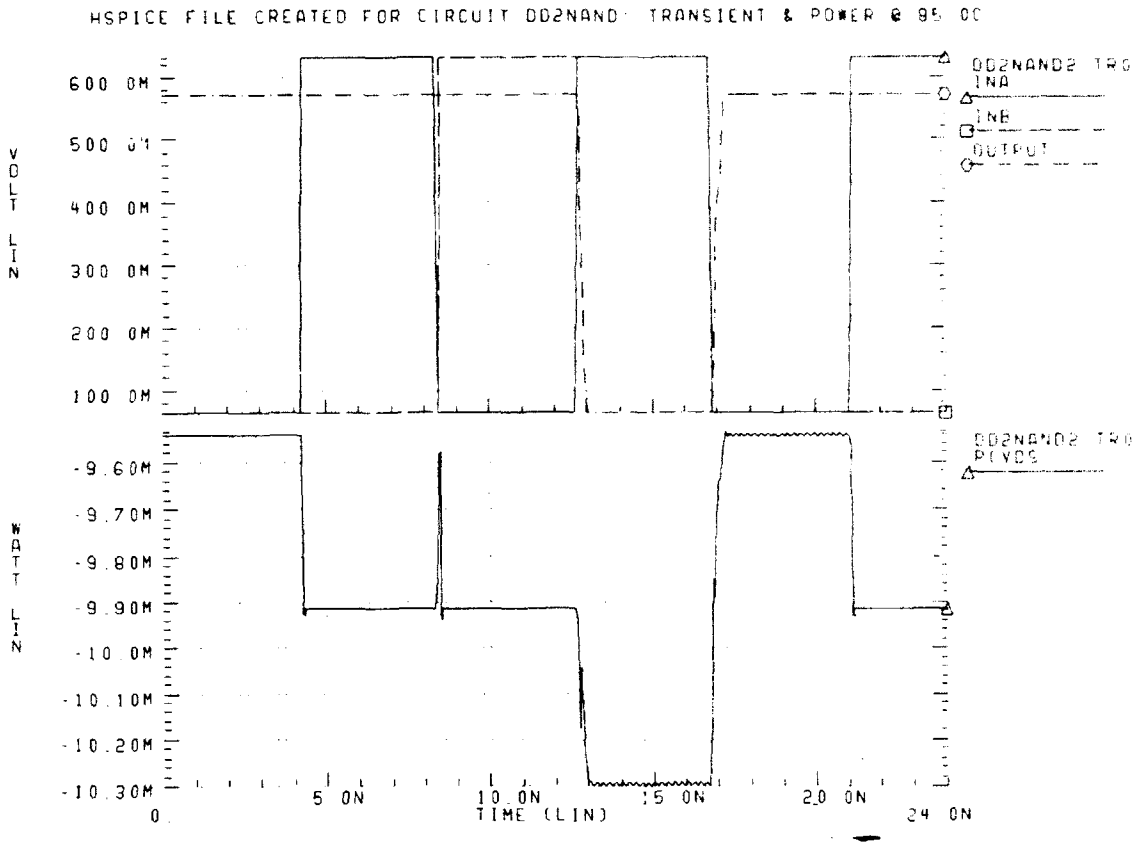


Figure 4.28 DD2NAND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DD2NAND logic gate operating at a temperature of 25.0C is shown in Figure 4.29 on page 40.

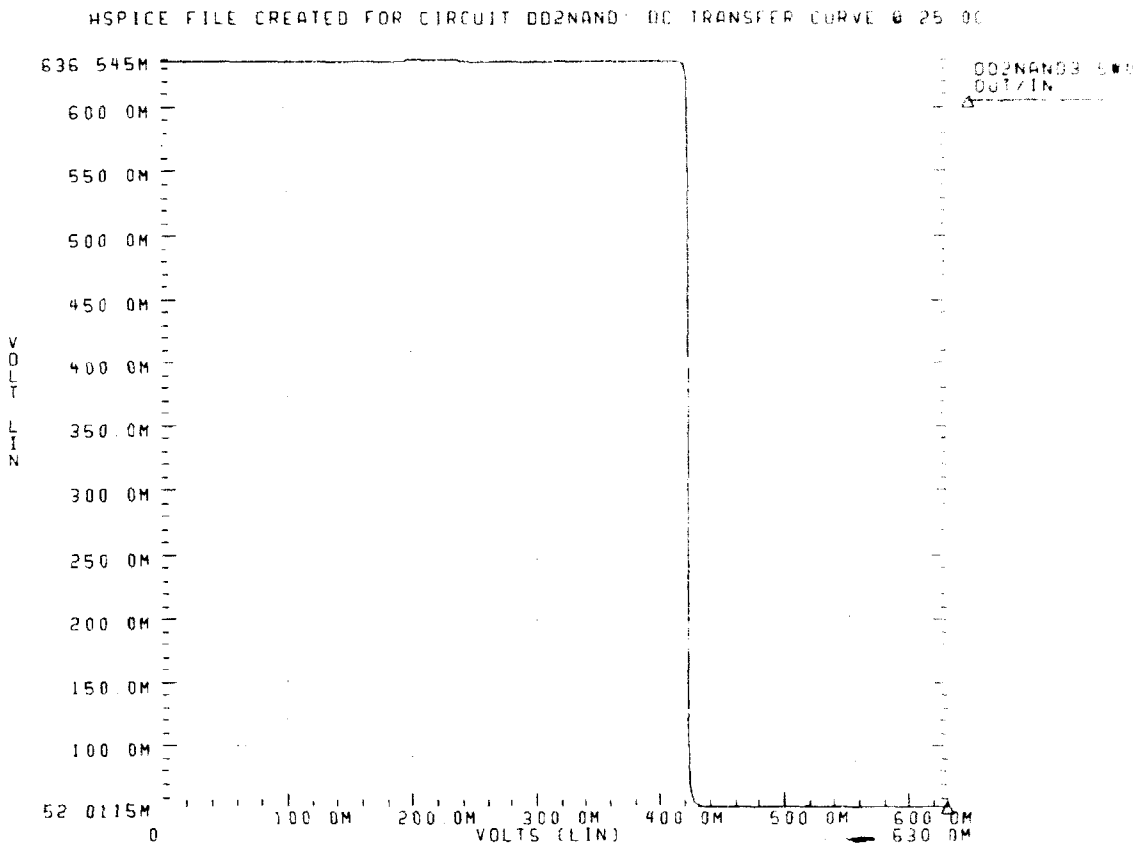


Figure 4.29 DD2NAND DC Transfer Curve at 25.0C

The DC transfer characteristic of the DD2NAND logic gate operating at a temperature of 85.0C is shown in Figure 4.30 on page 41.

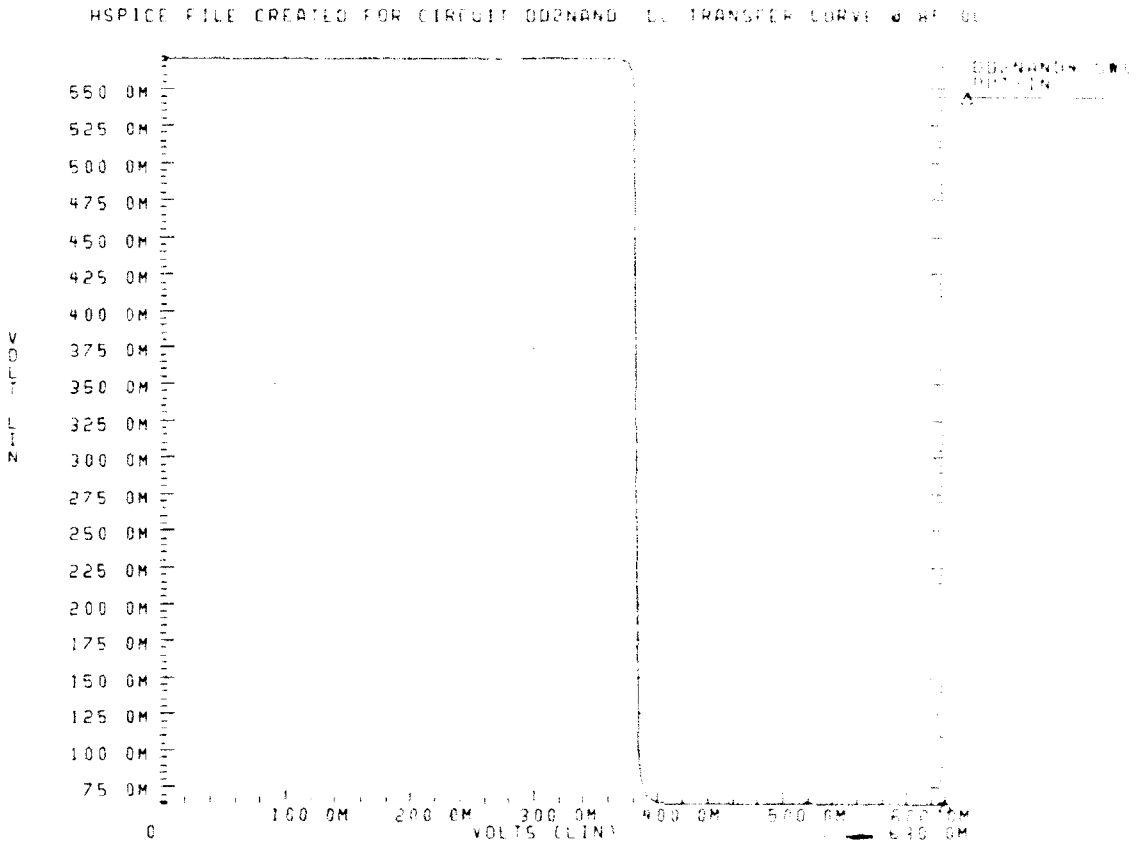


Figure 4.30 DD2NAND DC Transfer Curve at 85.0C

7. DCFL 3-input NAND Gate (DD3NAND)

A DD3NAND logic gate is constructed using the DeMorgan equivalent of a D3NOR with three DINVs on its inputs and one DINV on its output. The end result is a DCFL 3-input NAND gate and Figure 4.31 on page 41 presents the DD3AND schematic and logical equivalence.

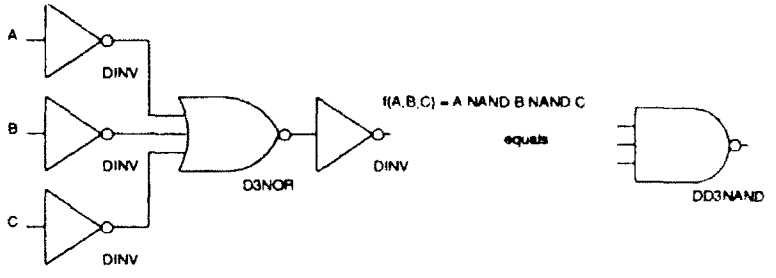


Figure 4.31 DD3NAND Schematic and Logical Equivalence

The transient analysis and power dissipation of the DD3NAND operating at a temperature of 25.0C is shown in Figure 4.32 on page 42. See "Listing File for DD3NAND Transient Analysis @ 25.0C" of Appendix A on page 265.

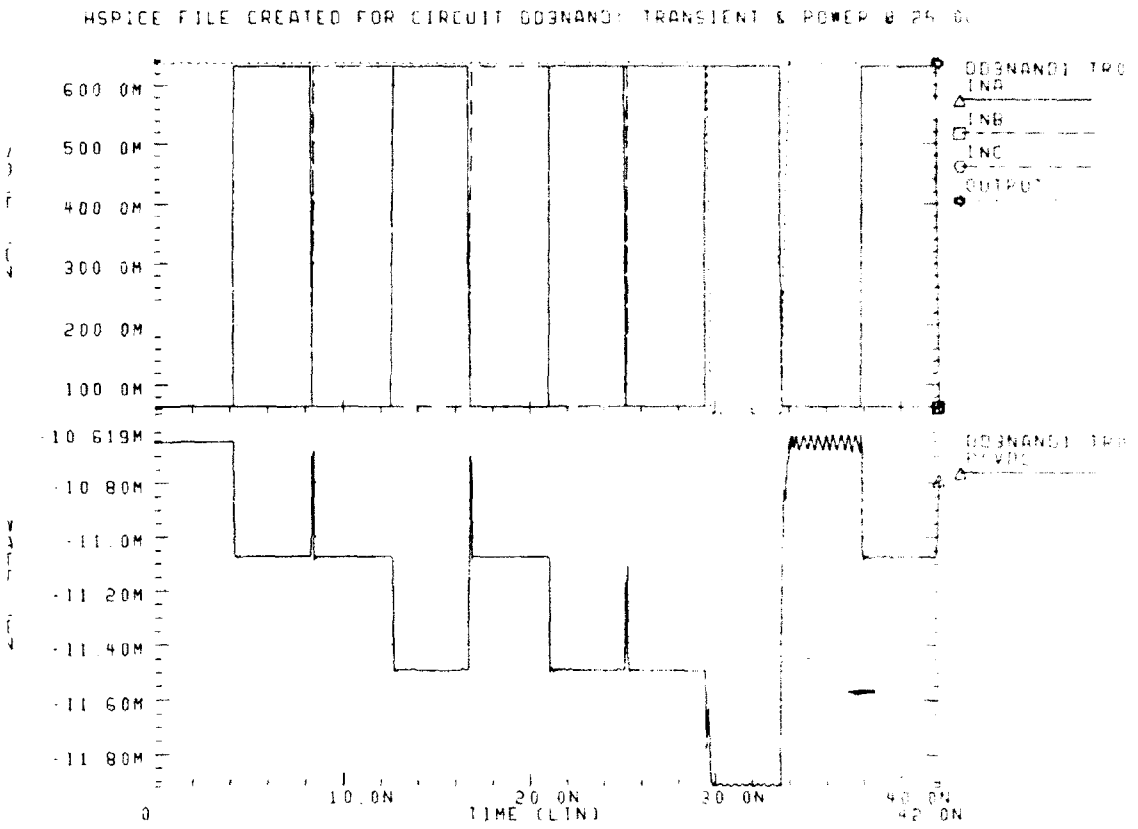


Figure 4.32 DD3NAND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DD3NAND operating at a temperature of 85.0C is shown in Figure 4.33 on page 43.

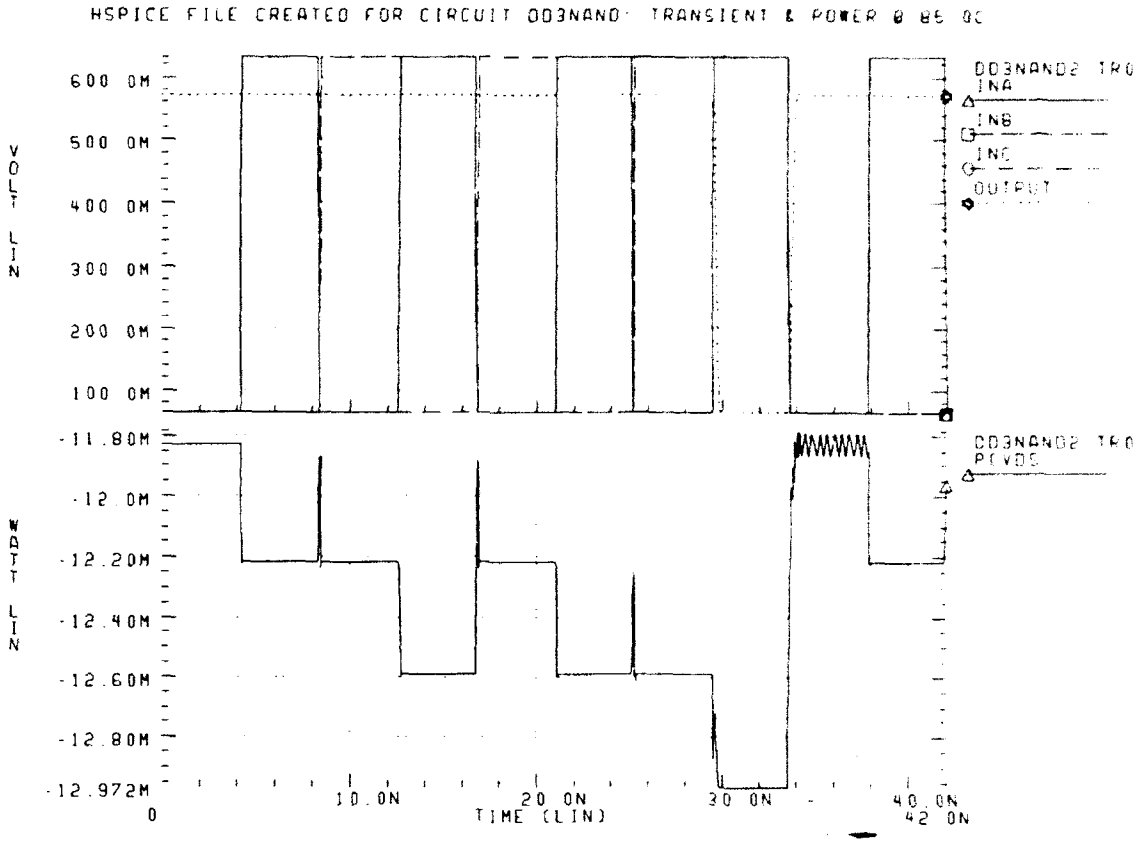


Figure 4.33 DD3NAND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DD3NAND logic gate operating at a temperature of 25.0C is shown in Figure 4.34 on page 44.

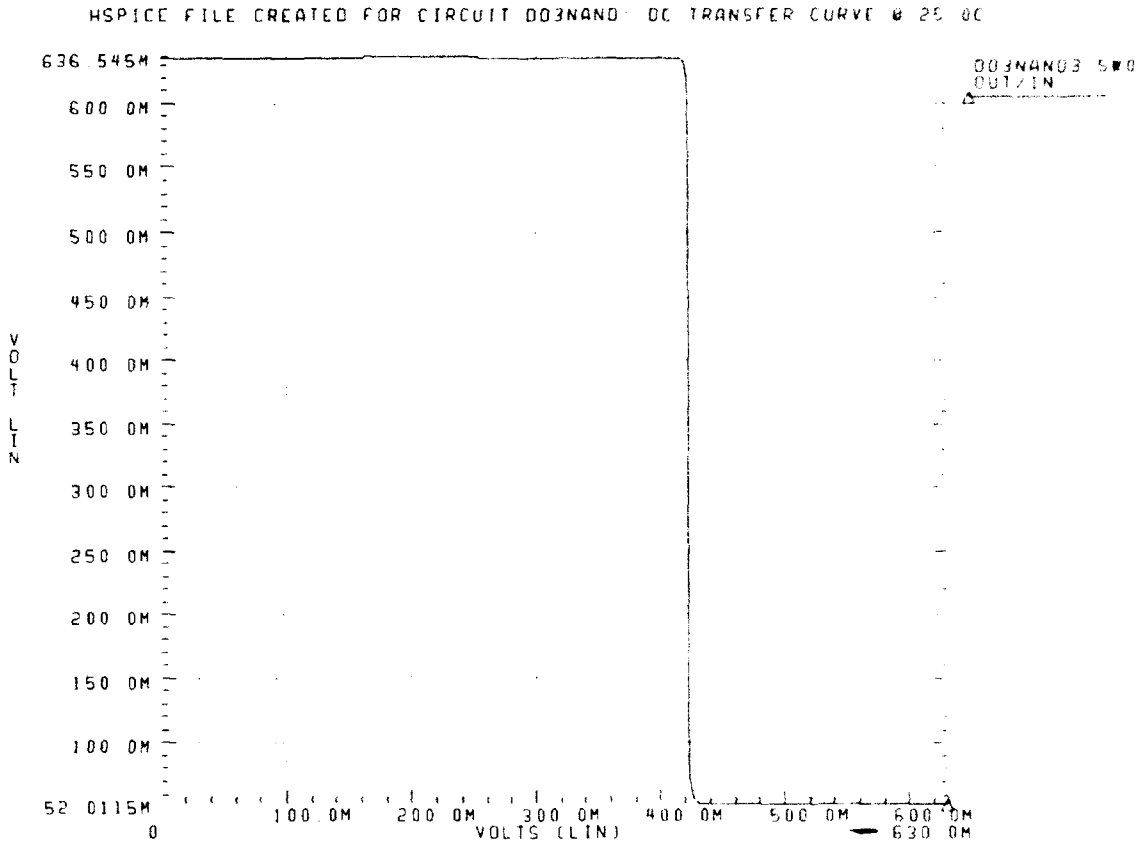


Figure 4.34 DD3NAND DC Transfer Curve at 25.0C

The DC transfer characteristic of the DD3NAND logic gate operating at a temperature of 85.0C is shown in Figure 4.35 on page 45.

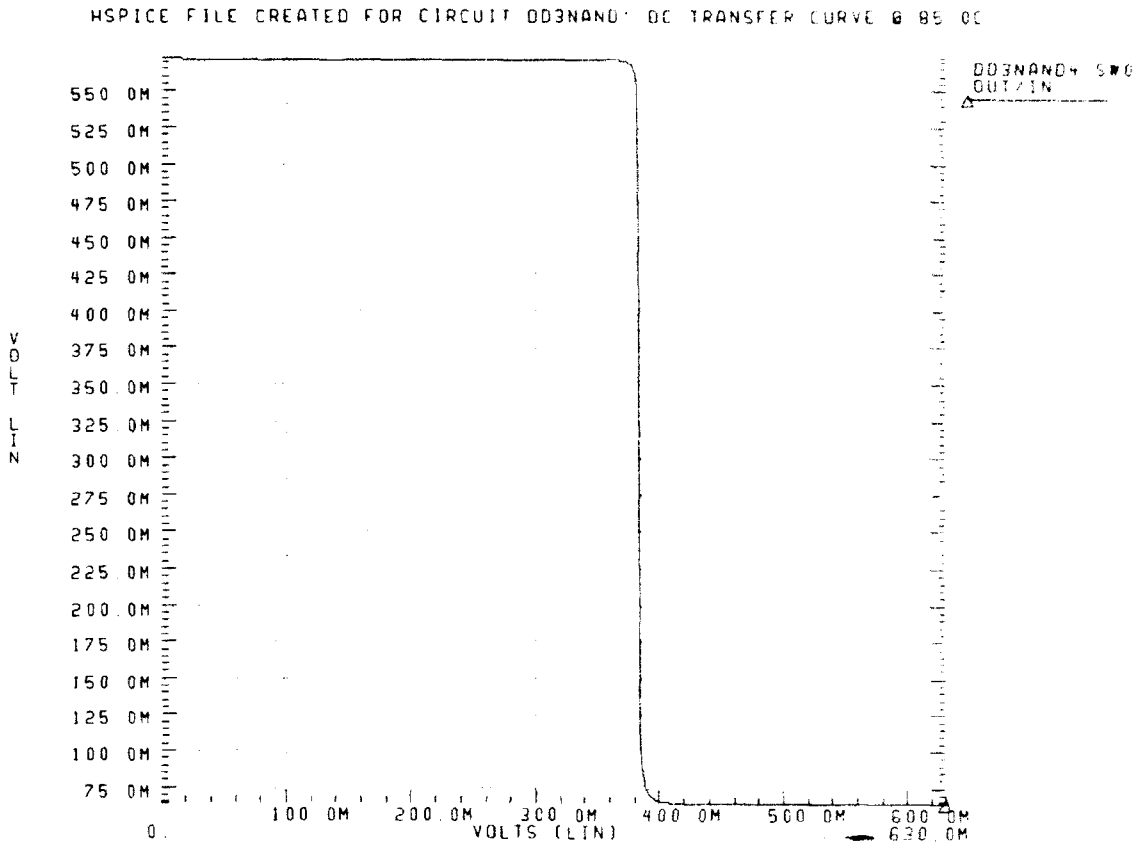


Figure 4.35 DD3NAND DC Transfer Curve at 85.0C

8. DCFL 2-input AND Gate (DD2AND)

A DD2AND logic gate is constructed using the DeMorgan equivalent of a D2NOR with two DINVs on its inputs. The end result is a DCFL 2-input AND gate and Figure 4.36 on page 45 presents the DD2AND schematic and logical equivalence.

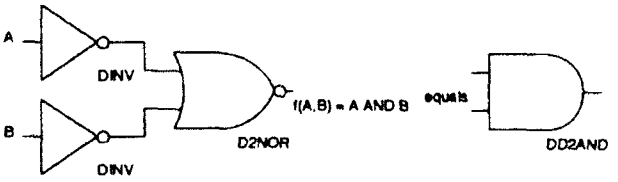


Figure 4.36 DD2AND Schematic and Logical Equivalence

The transient analysis and power dissipation of the DD2AND operating at a temperature of 25.0C is shown in Figure 4.37 on page 46.

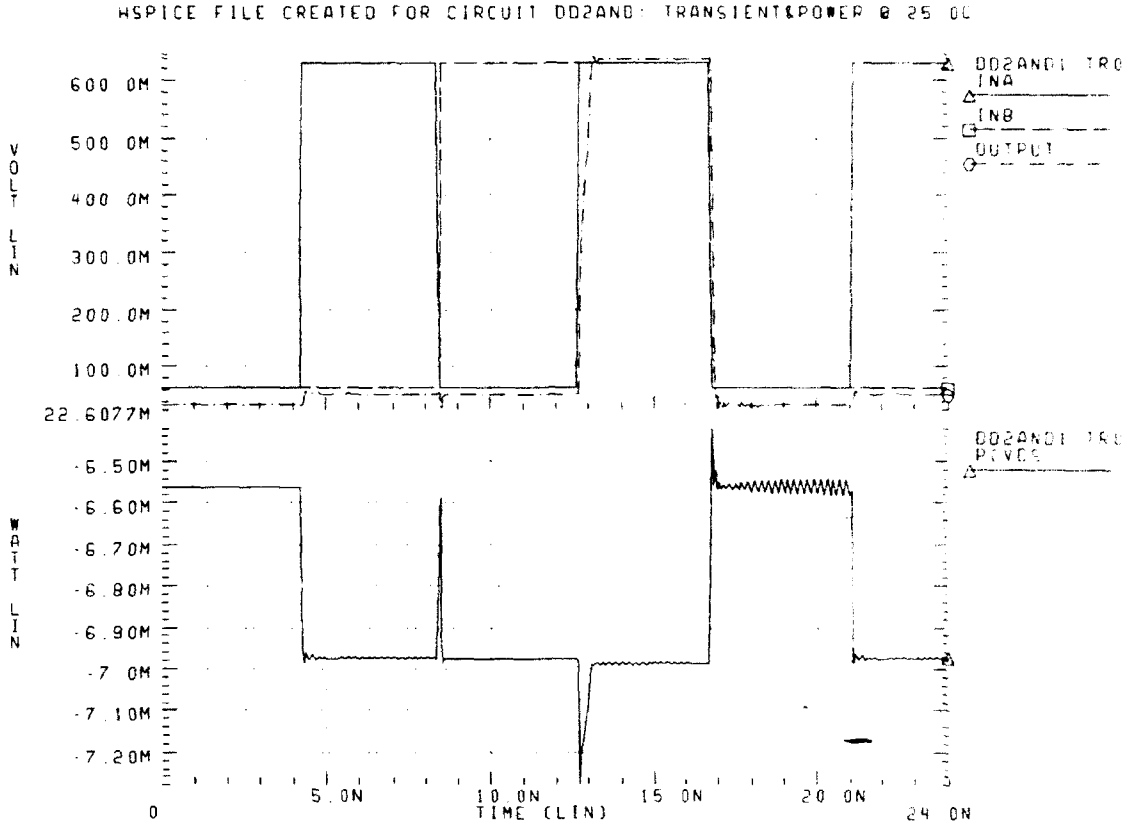


Figure 4.37 DD2AND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DD2AND operating at a temperature of 85.0C is shown in Figure 4.38 on page 47.

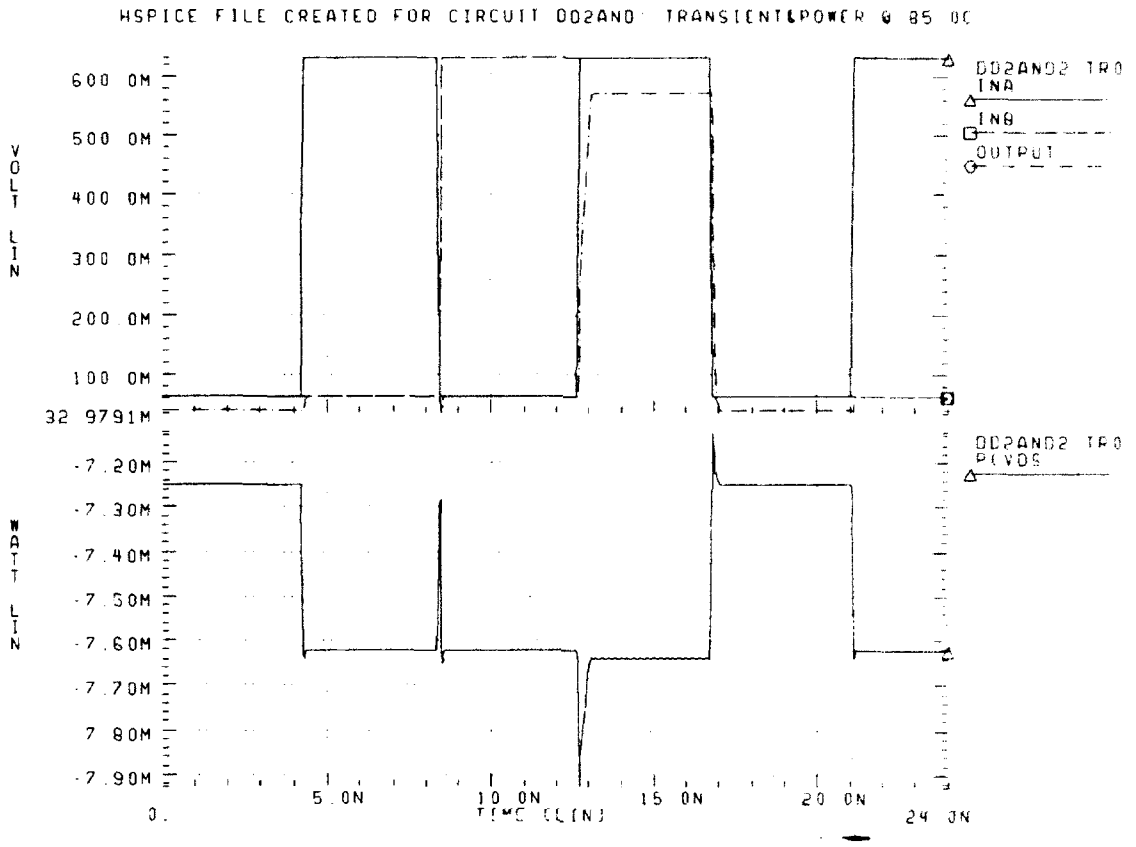


Figure 4.38 DD2AND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DD2AND logic gate operating at a temperature of 25.0C is shown in Figure 4.39 on page 48.

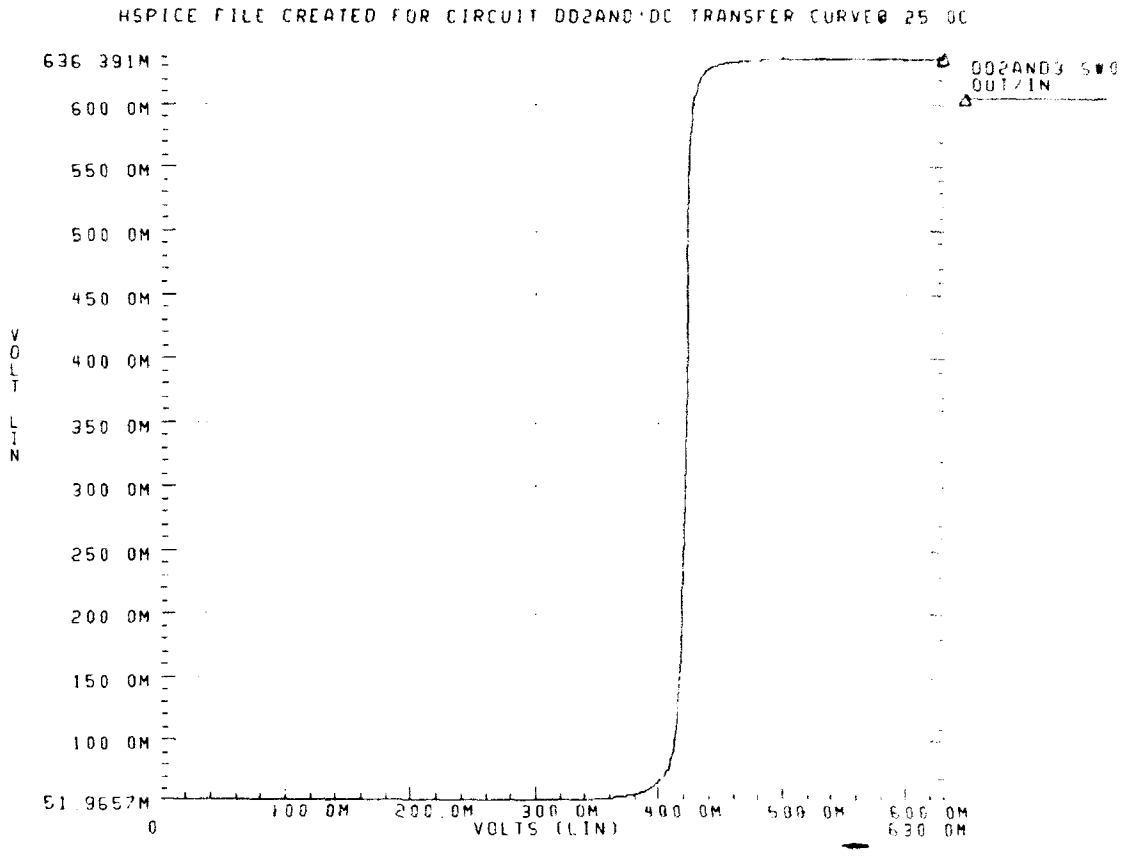


Figure 4.39 DD2AND DC Transfer Curve at 25.0C

The DC transfer characteristic of the DD2AND logic gate operating at a temperature of 85.0C is shown in Figure 4.40 on page 49.

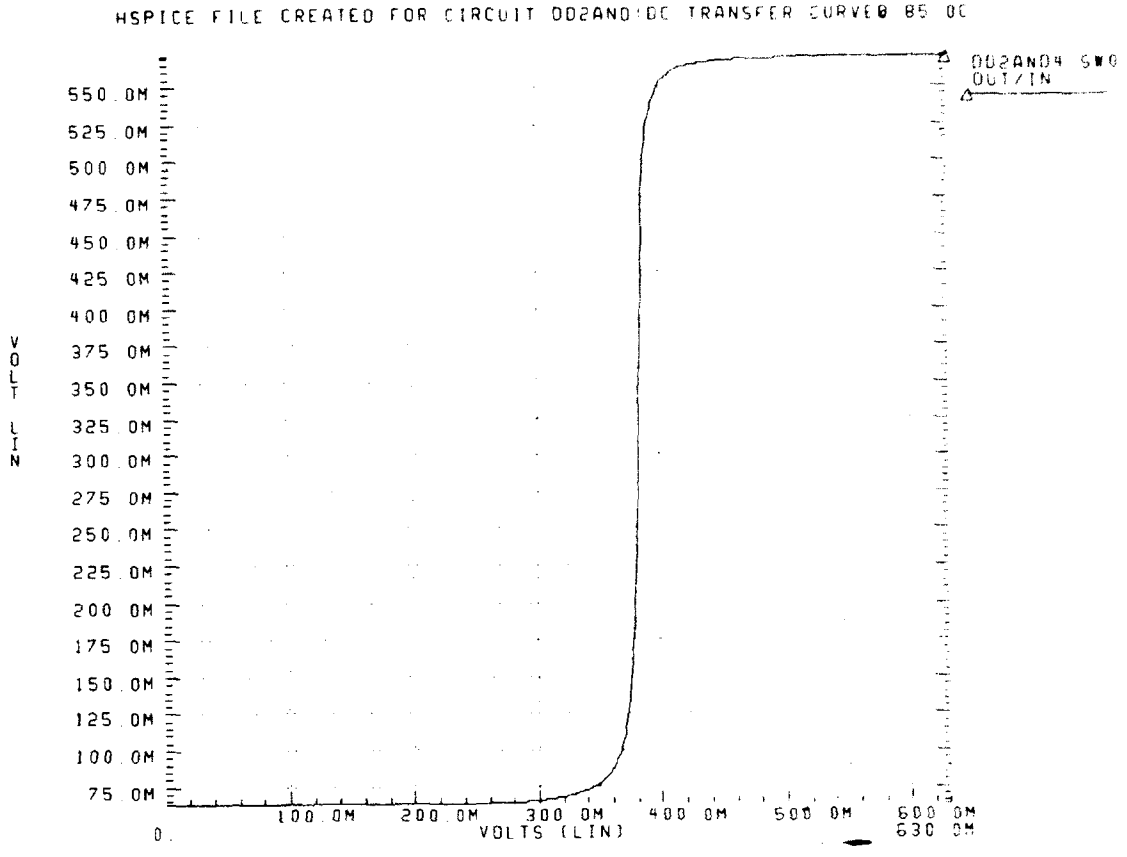


Figure 4.40 DD2AND DC Transfer Curve at 85.0C

9. DCFL 3-input AND Gate (DD3AND)

A DD3AND logic gate is constructed using the DeMorgan equivalent of a D3NOR with three DINVs on its inputs. The end result is a DCFL 3-input AND gate and Figure 4.41 on page 49 presents the DD3AND schematic and logical equivalence.

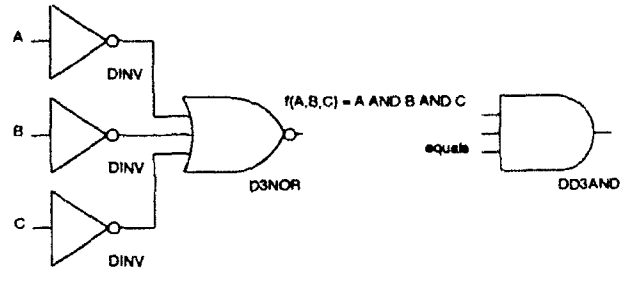


Figure 4.41 DD3AND Schematic and Logical Equivalence

The transient analysis and power dissipation of the DD3AND operating at a temperature of 25.0C is shown in Figure 4.42 on page 50.

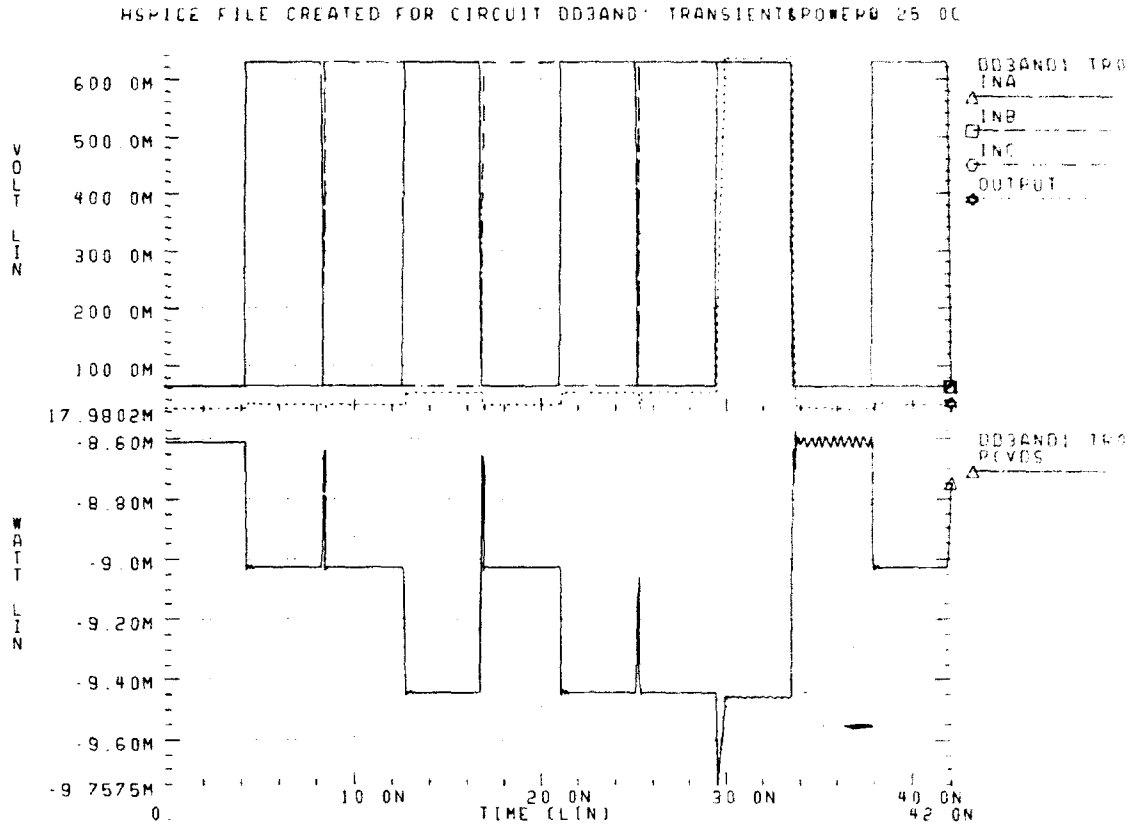


Figure 4.42 DD3AND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DD3AND operating at a temperature of 85.0C is shown in Figure 4.43 on page 51.

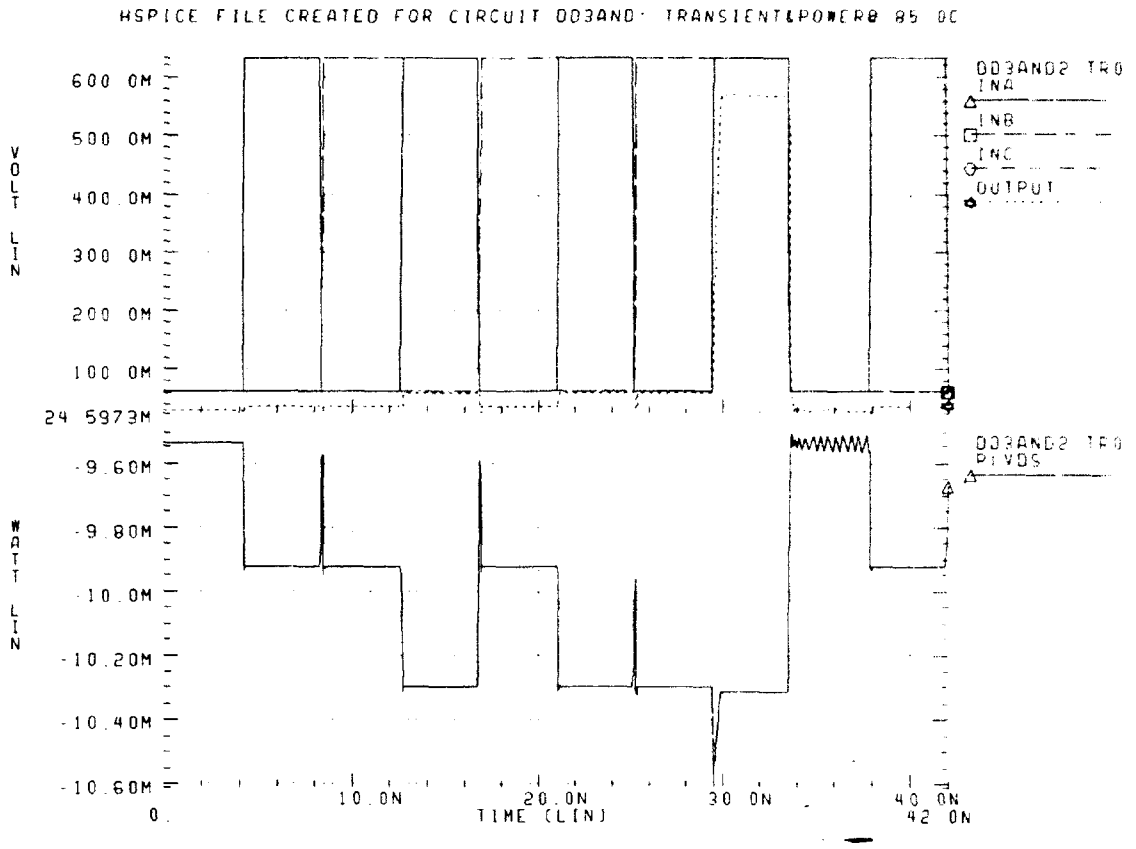


Figure 4.43 DD3AND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DD3AND logic gate operating at a temperature of 25.0C is shown in Figure 4.44 on page 52.

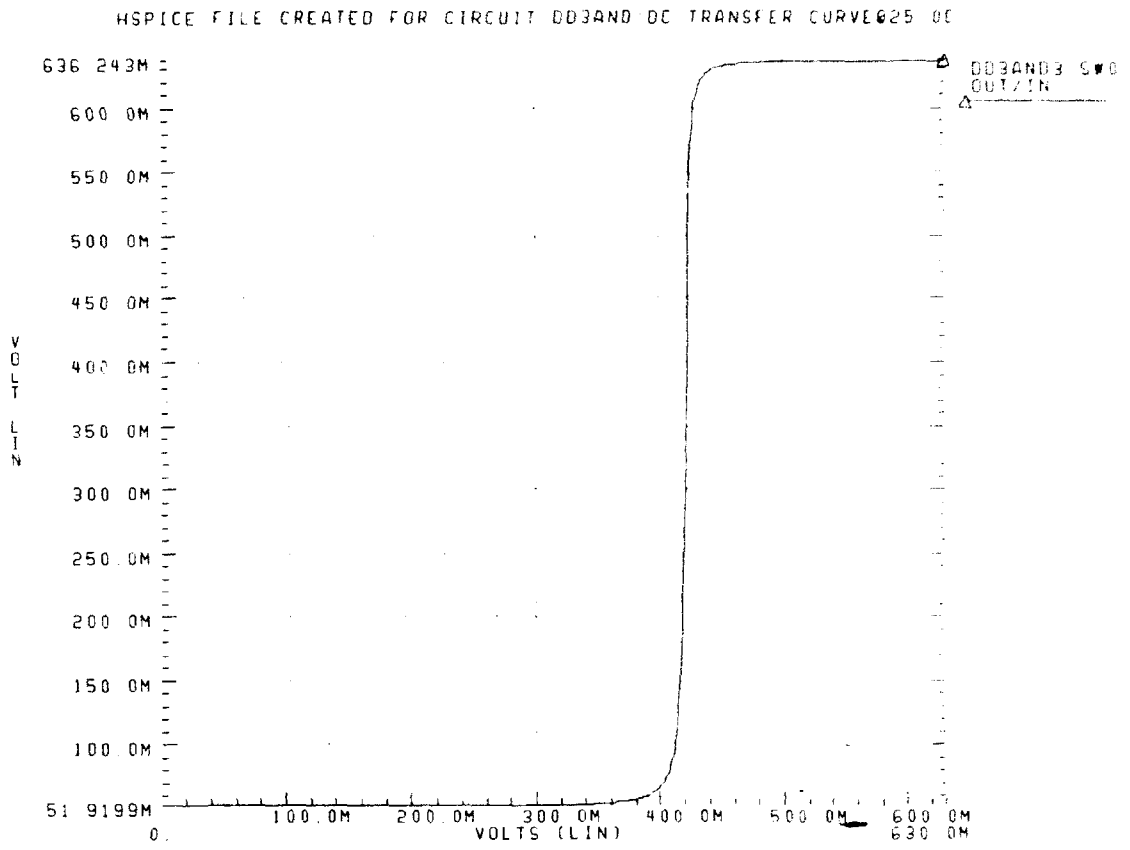


Figure 4.44 DD3AND DC Transfer Curve at 25.0C

The DC transfer characteristic of the DD3AND logic gate operating at a temperature of 85.0C is shown in Figure 4.45 on page 53.

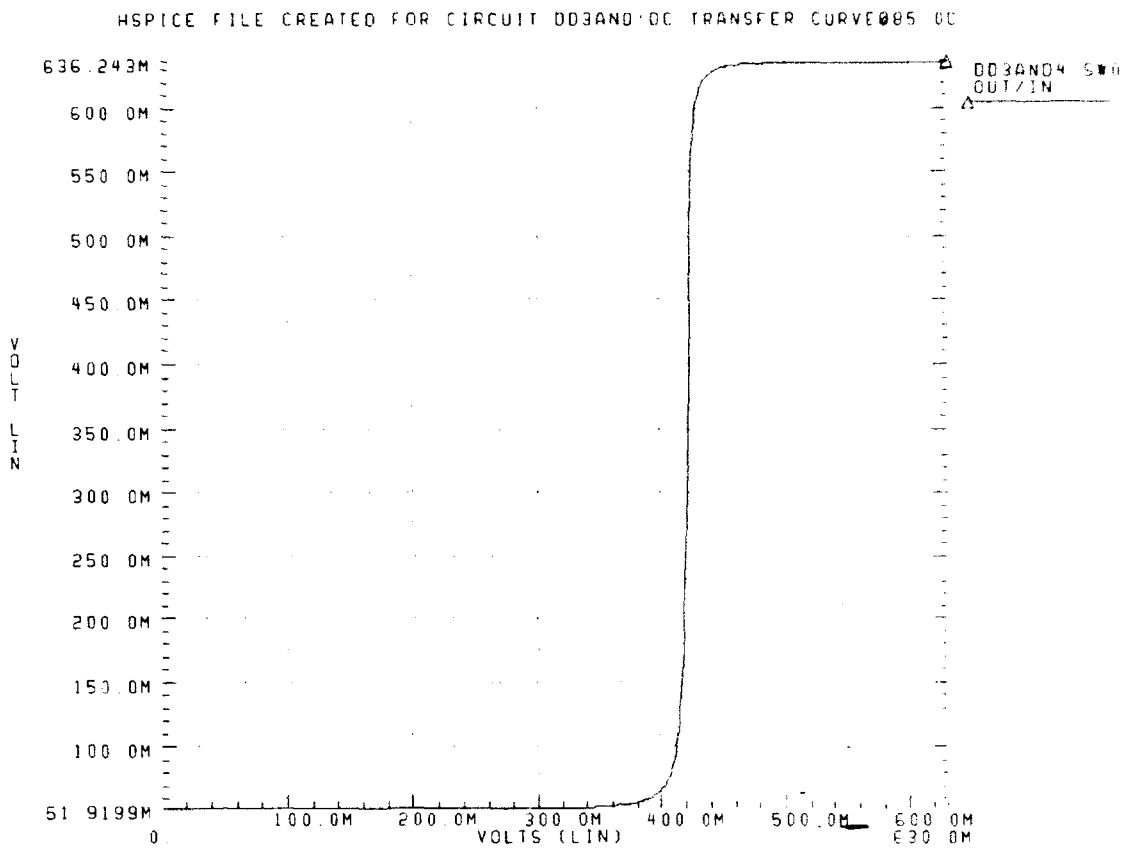


Figure 4.45 DD3AND DC Transfer Curve at 85.0C

10. DCFL 4-input AND Gate (DD4AND)

A DD4AND logic gate is constructed using the DeMorgan equivalent of a D4NOR with four DINVs on its inputs. The end result is a DCFL 4-input AND gate and Figure 4.46 on page 54 presents the DD4AND schematic and logical equivalence.

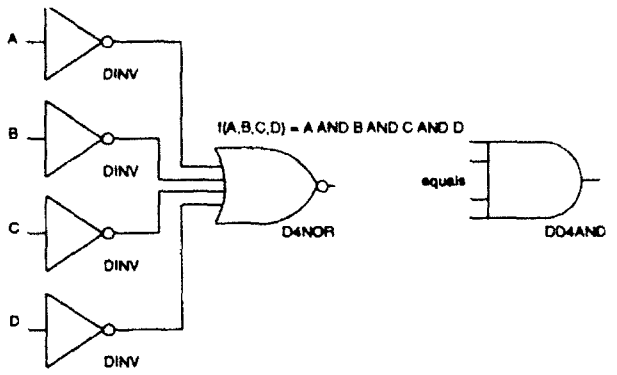


Figure 4.46 DD4AND Schematic and Logical Equivalence

The transient analysis and power dissipation of the DD4AND operating at a temperature of 25.0C is shown in Figure 4.47 on page 54. See "Listing File for DD4AND Transient Analysis @ 25.0C" of Appendix A on page 268.

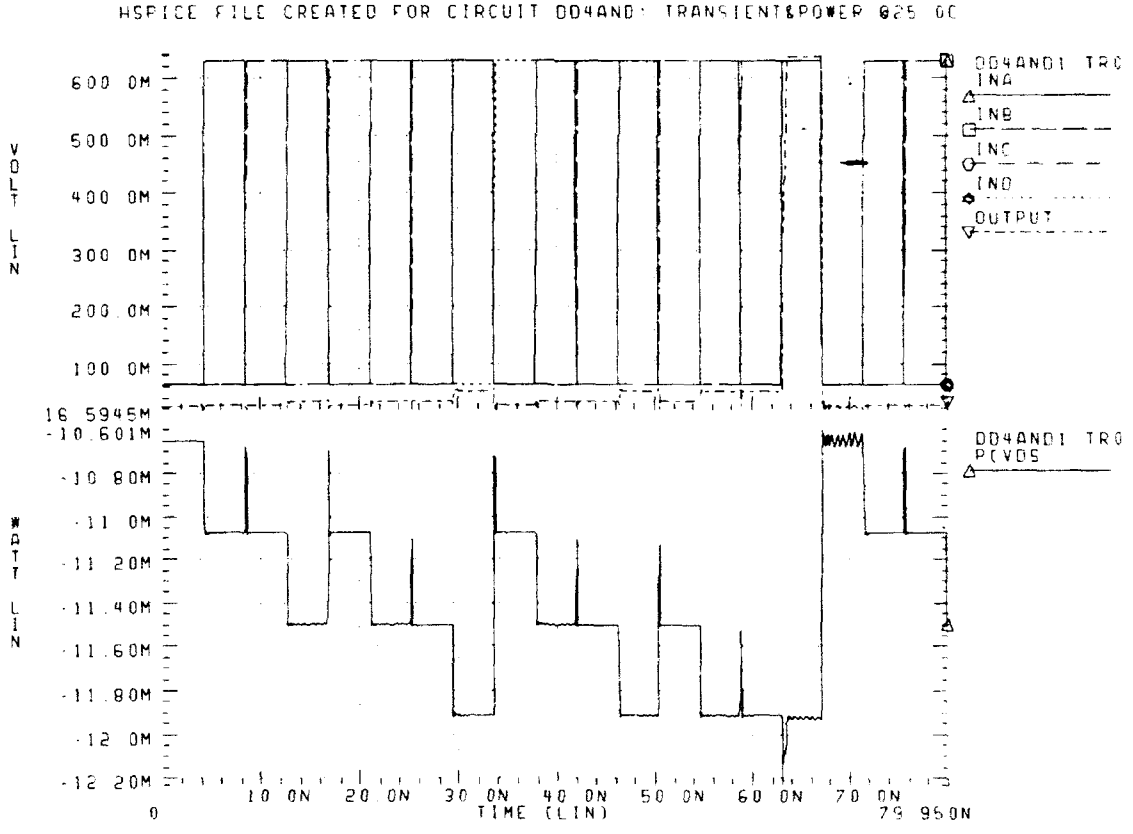


Figure 4.47 DD4AND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DD4AND operating at a temperature of 85.0C is shown in Figure 4.48 on page 55.

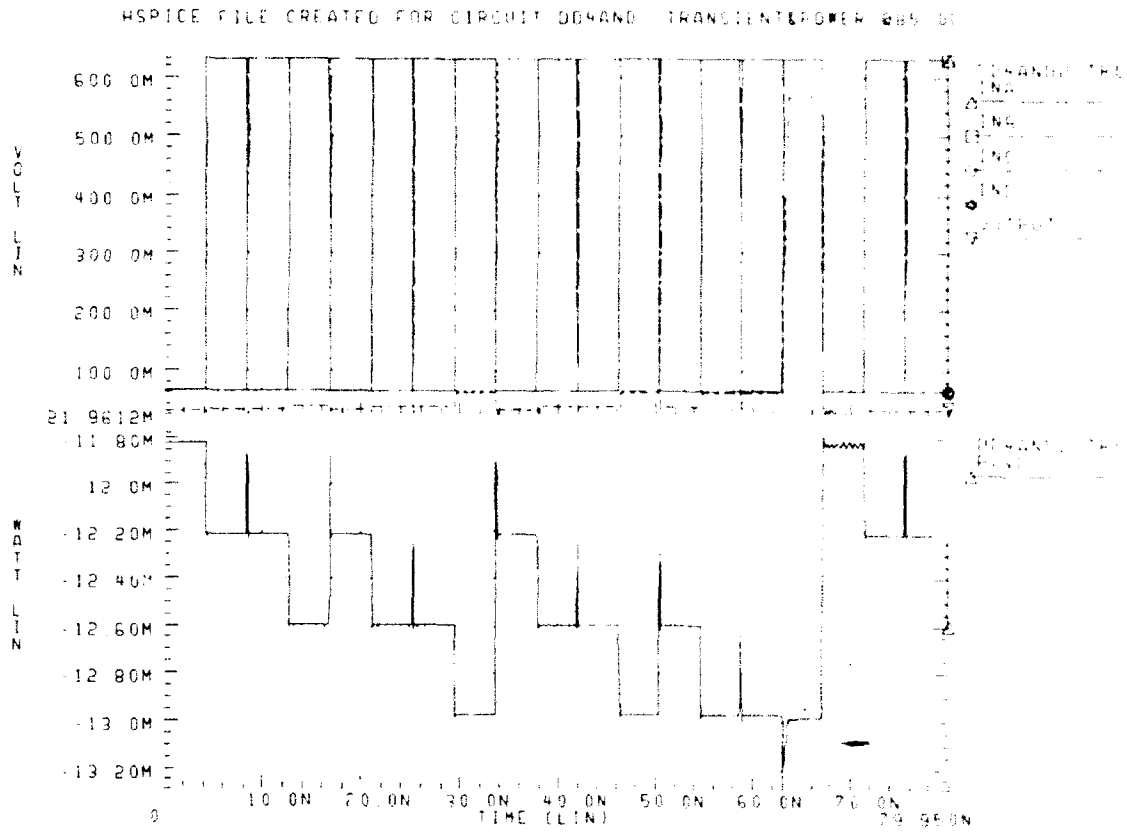


Figure 4.48 DD4AND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DD4AND logic gate operating at a temperature of 25.0C is shown in Figure 4.49 on page 56.

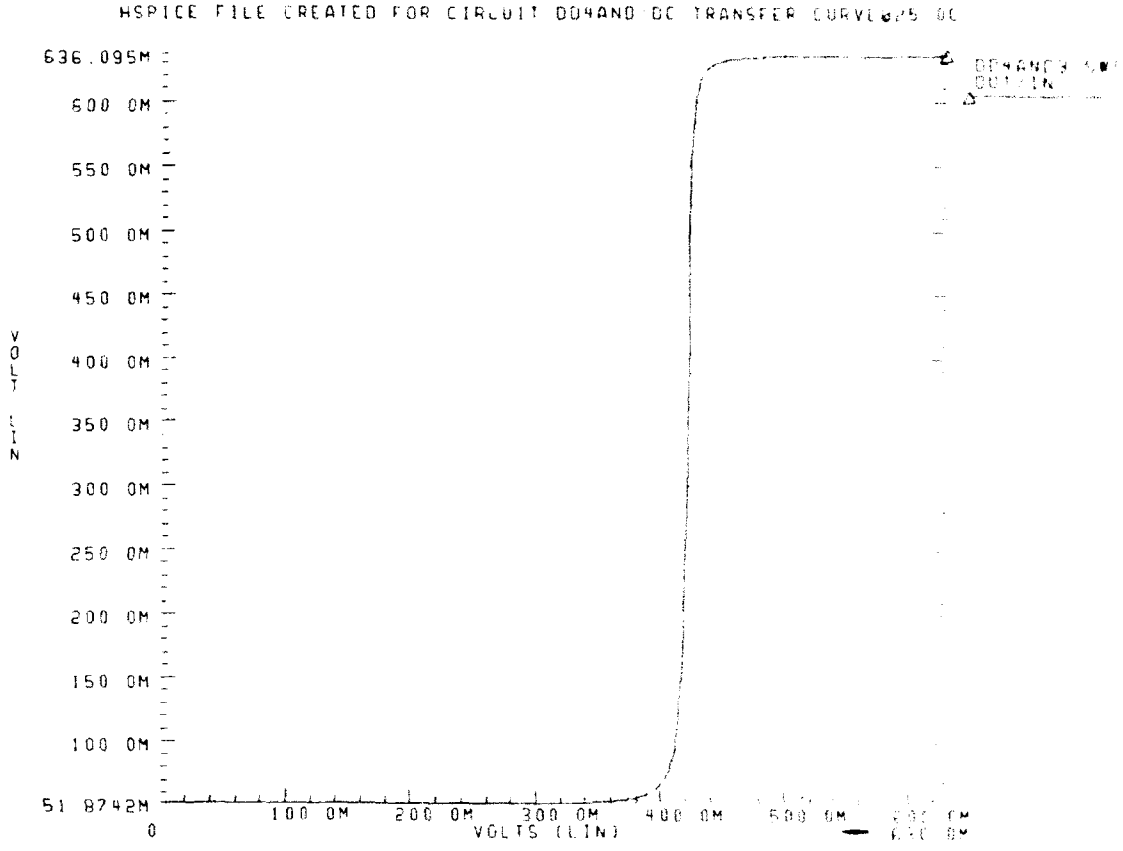


Figure 4.49 DD4AND DC Transfer Curve at 25.0C

The DC transfer characteristic of the DD4AND logic gate operating at a temperature of 85.0C is shown in Figure 4.50 on page 57.

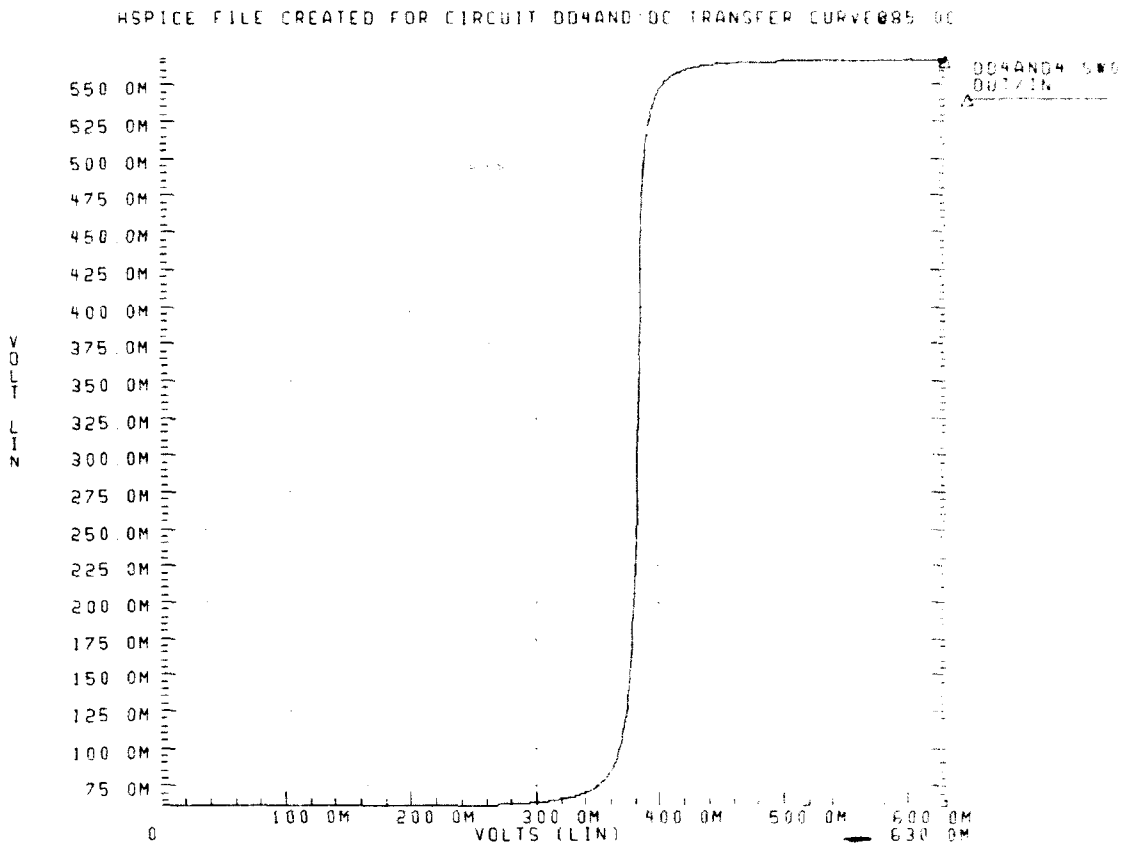


Figure 4.50 DD4AND DC Transfer Curve at 85.0C

11. DCFL 2-input OR Gate (DD2OR)

A DD2OR logic gate is constructed using the DeMorgan equivalent of a D2NOR with a single DINV on its input. The end result is a DCFL 2-input OR gate and Figure 4.51 on page 57 presents the DD2OR schematic and logical equivalence.

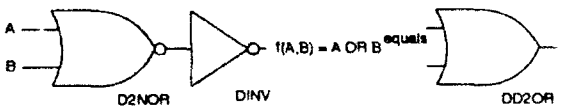


Figure 4.51 DD2OR Schematic And Logical Equivalence

The transient analysis and power dissipation of the DD2OR operating at a temperature of 25.0C is shown in Figure 4.52 on page 58.

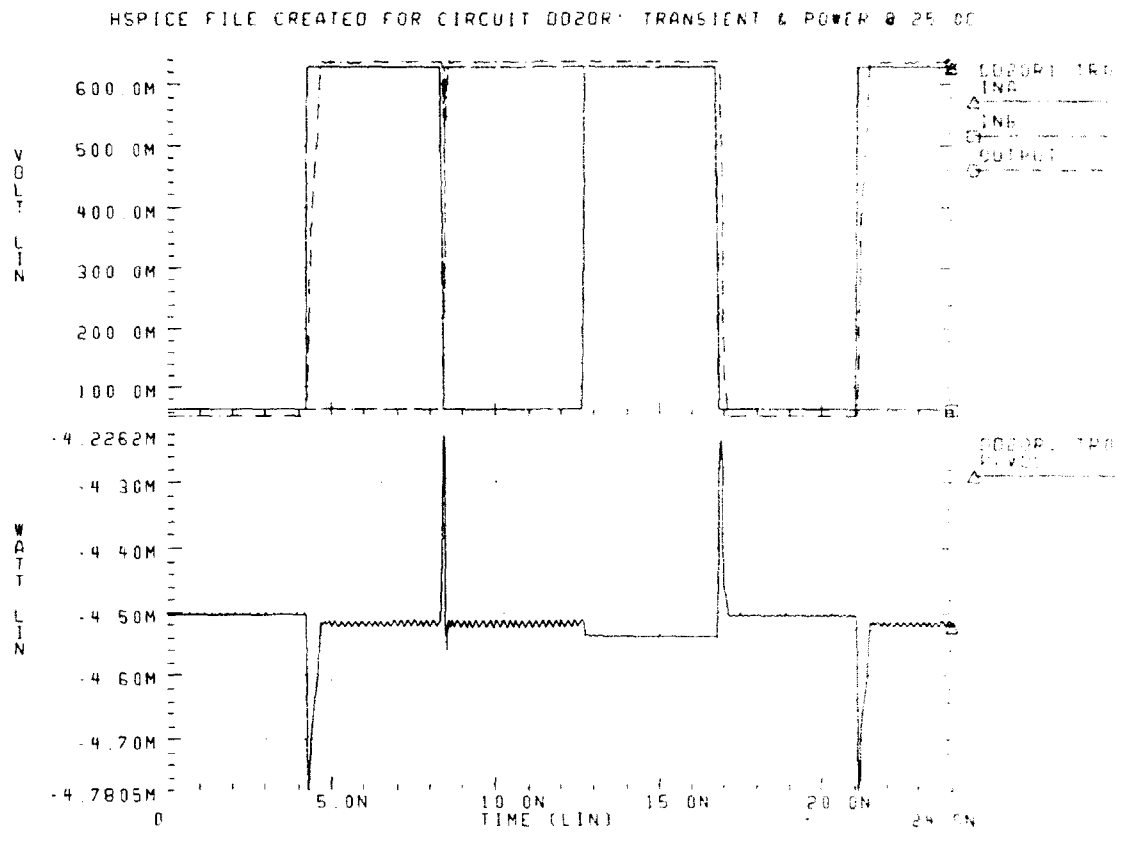


Figure 4.52 DD2OR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DD2OR operating at a temperature of 85.0C is shown in Figure 4.53 on page 59.

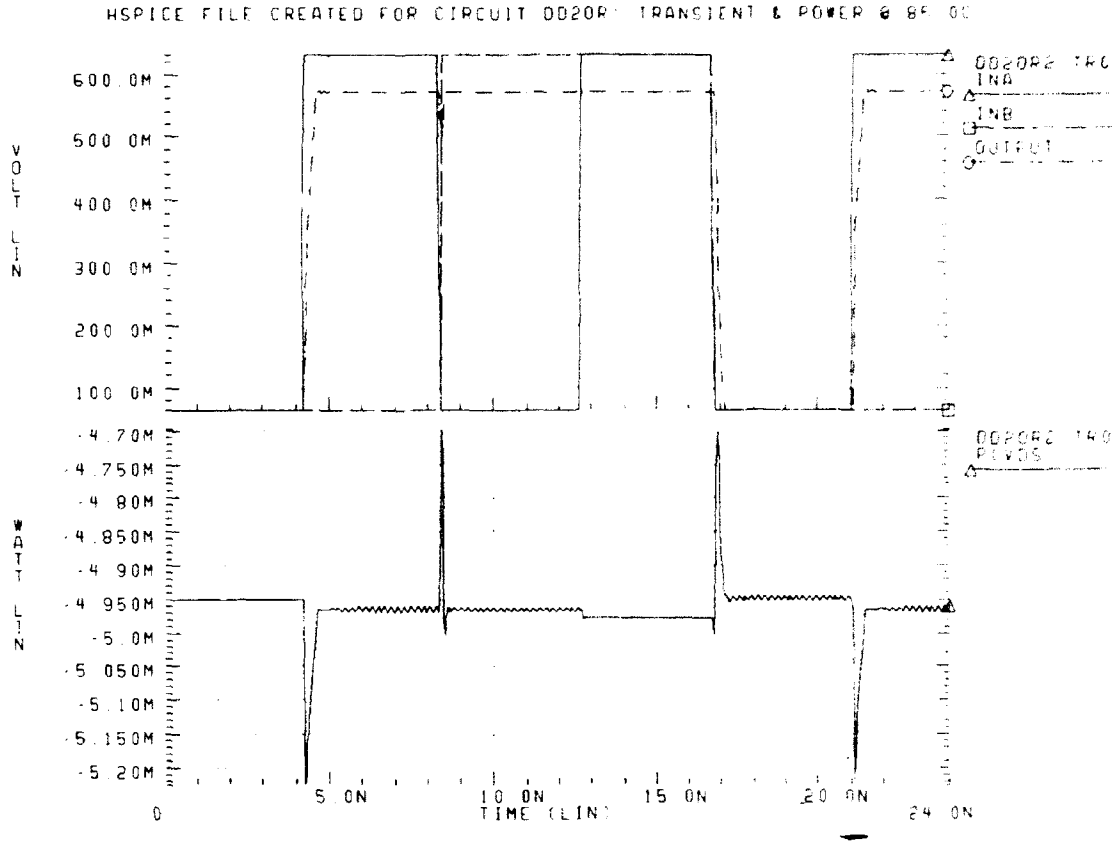


Figure 4.53 DD2OR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DD2OR logic gate operating at a temperature of 25.0C is shown in Figure 4.54 on page 60.

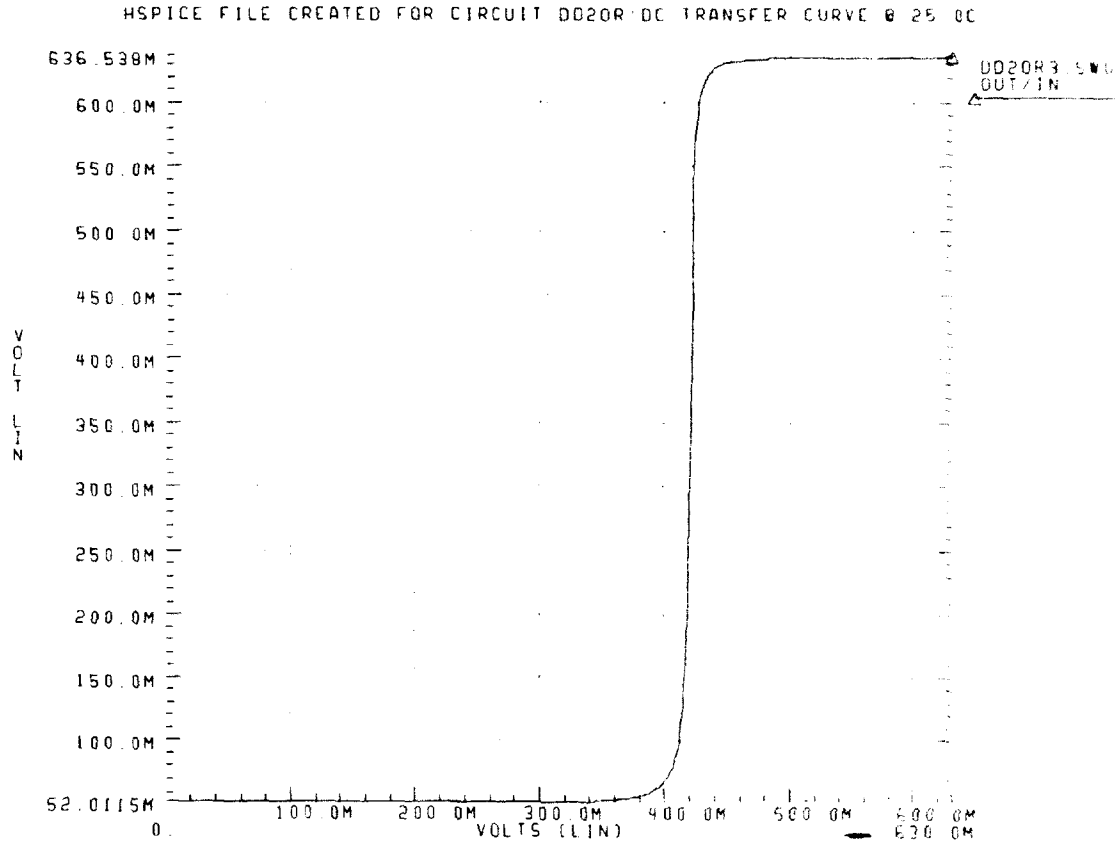


Figure 4.54 DD2OR DC Transfer Curve at 25.0C

The DC transfer characteristic of the DD2OR logic gate operating at a temperature of 85.0C is shown in Figure 4.55 on page 61.

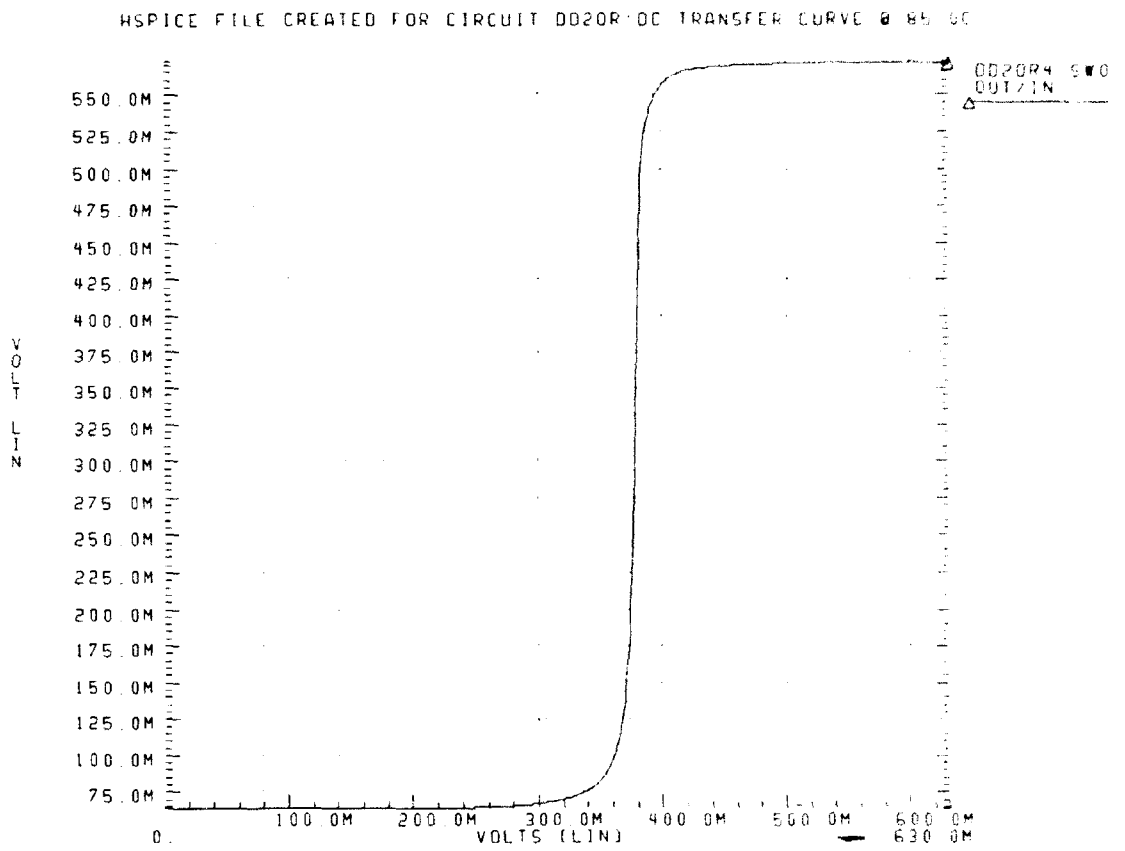


Figure 4.55 DD2OR DC Transfer Curve at 85.0C

12. DCFL 3-input OR Gate (DD3OR)

A DD3OR logic gate is constructed using the DeMorgan equivalent of a D3NOR with a single DINV on its input. The end result is a DCFL 3-input OR gate and Figure 4.56 on page 61 presents the DD3OR schematic and logical equivalence.

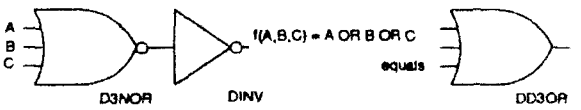


Figure 4.56 DD3OR Schematic And Logical Equivalence

The transient analysis and power dissipation of the DD3OR operating at a temperature of 25.0C is shown in Figure 4.57 on page 62.

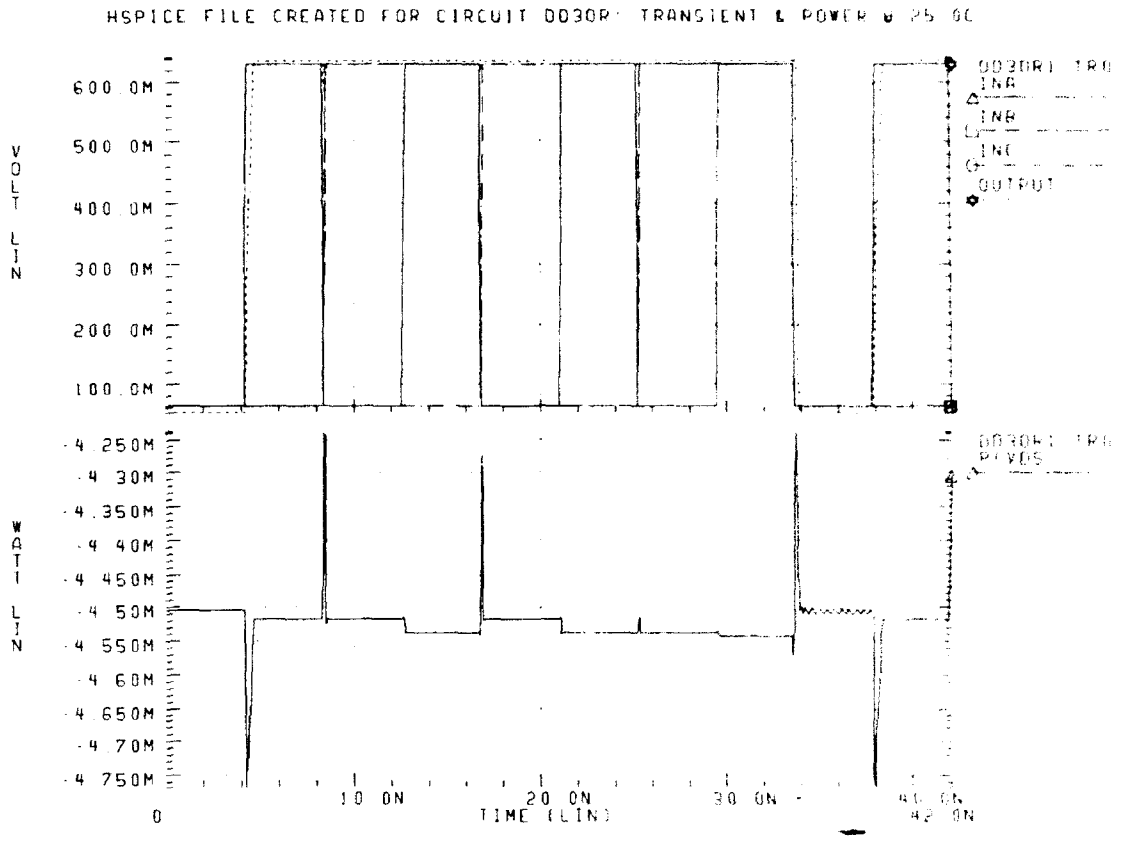


Figure 4.57 DD3OR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DD3OR operating at a temperature of 85.0C is shown in Figure 4.58 on page 63.

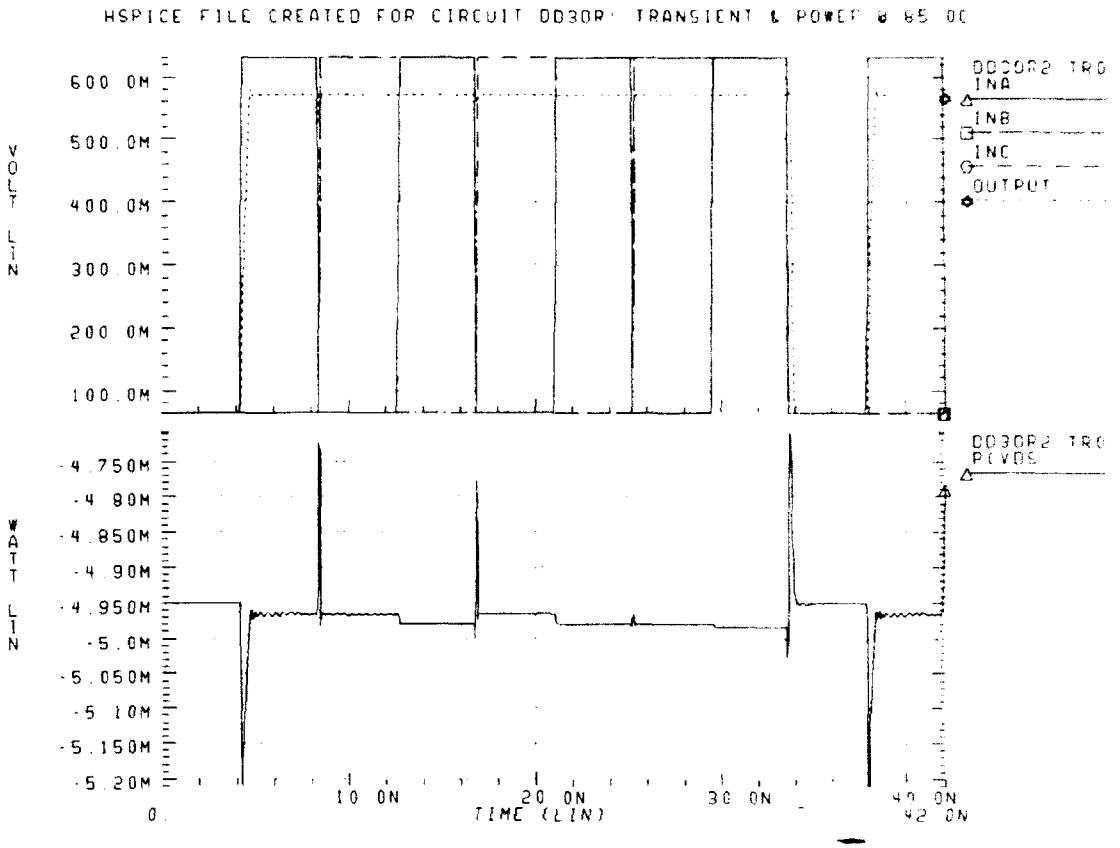


Figure 4.58 DD3OR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DD3OR logic gate operating at a temperature of 25.0C is shown in Figure 4.59 on page 64.

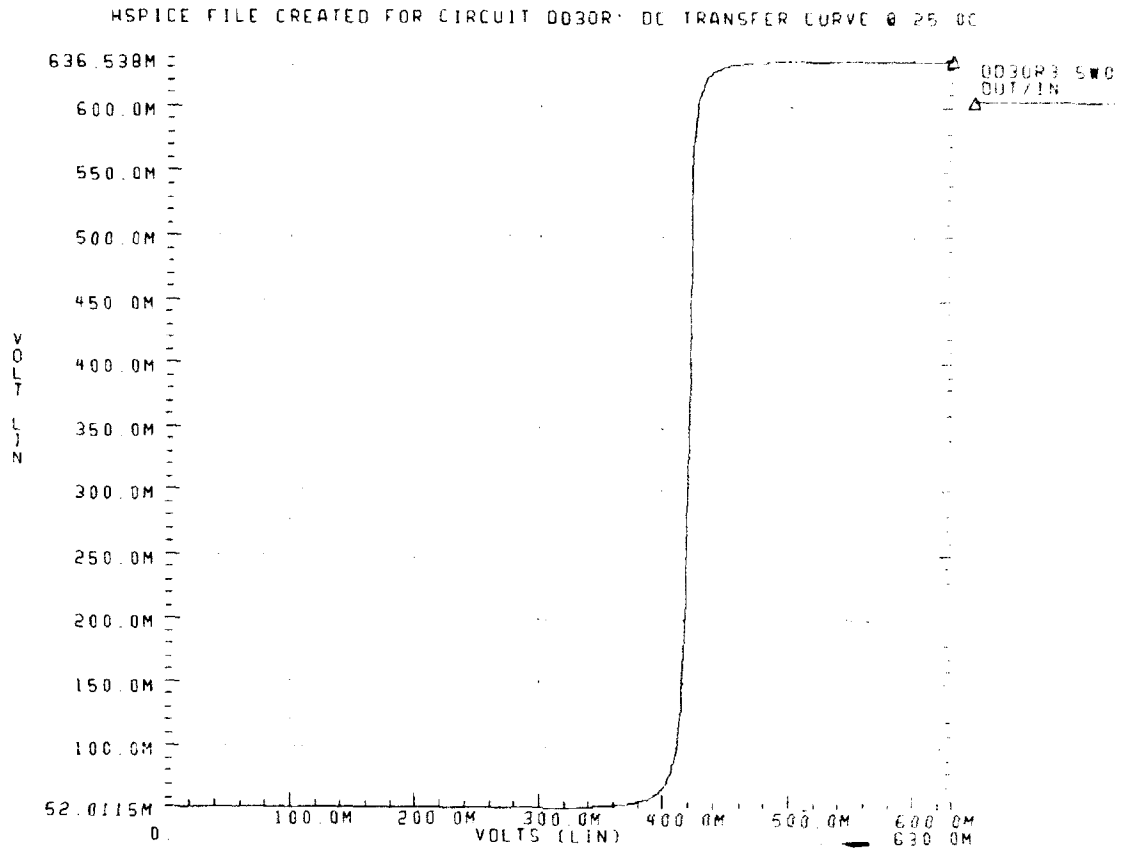


Figure 4.59 DD3OR DC Transfer Curve at 25.0C

The DC transfer characteristic of the DD3OR logic gate operating at a temperature of 85.0C is shown in Figure 4.60 on page 65.

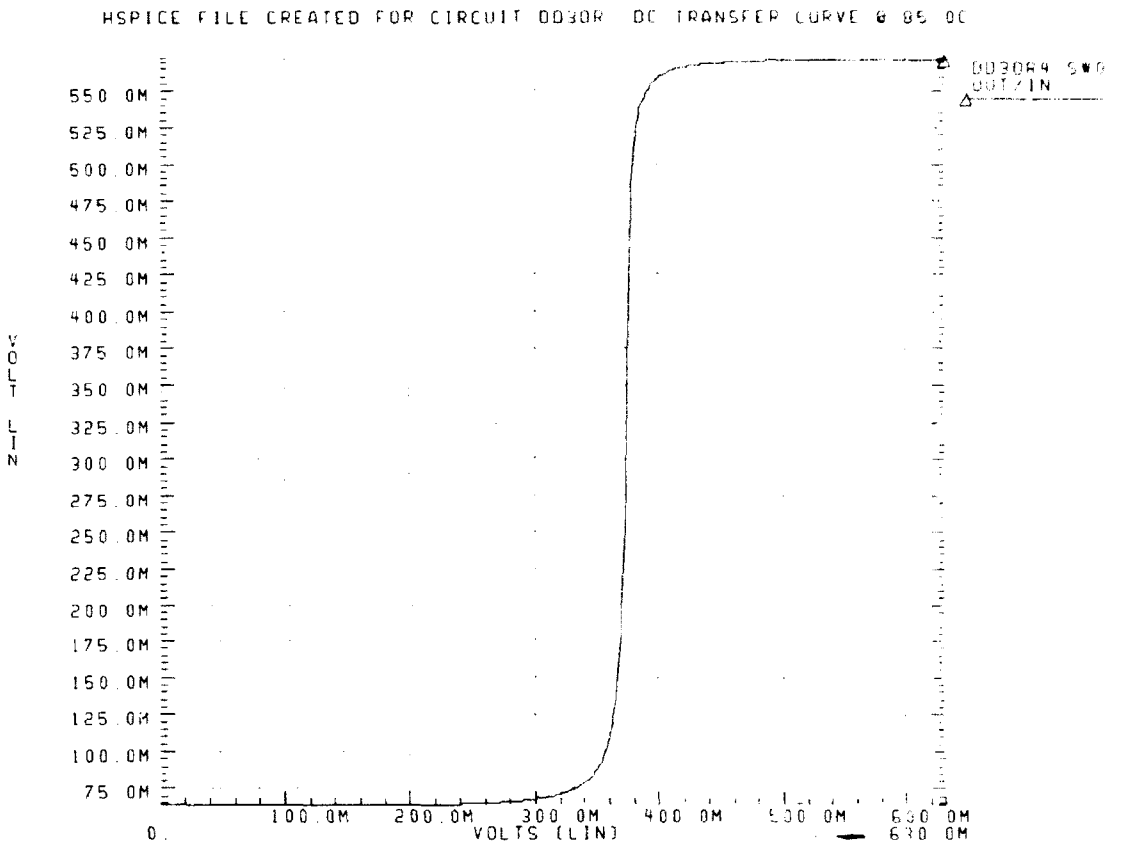


Figure 4.60 DD3OR DC Transfer Curve at 85.0C

13. DCFL 4-input OR Gate (DD4OR)

A DD4OR logic gate is constructed using the DeMorgan equivalent of a D4NOR with a single DINV on its input. The end result is a DCFL 4-input OR gate and Figure 4.61 on page 65 presents the DD4OR schematic and logical equivalence.

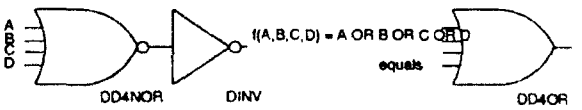


Figure 4.61 DD4OR Schematic And Logical Equivalence

The transient analysis and power dissipation of the DD4OR operating at a temperature of 25.0C is shown in Figure 4.62 on page 66. See "Listing File for DD4OR Transient Analysis @ 25.0C" of Appendix A on page 271.

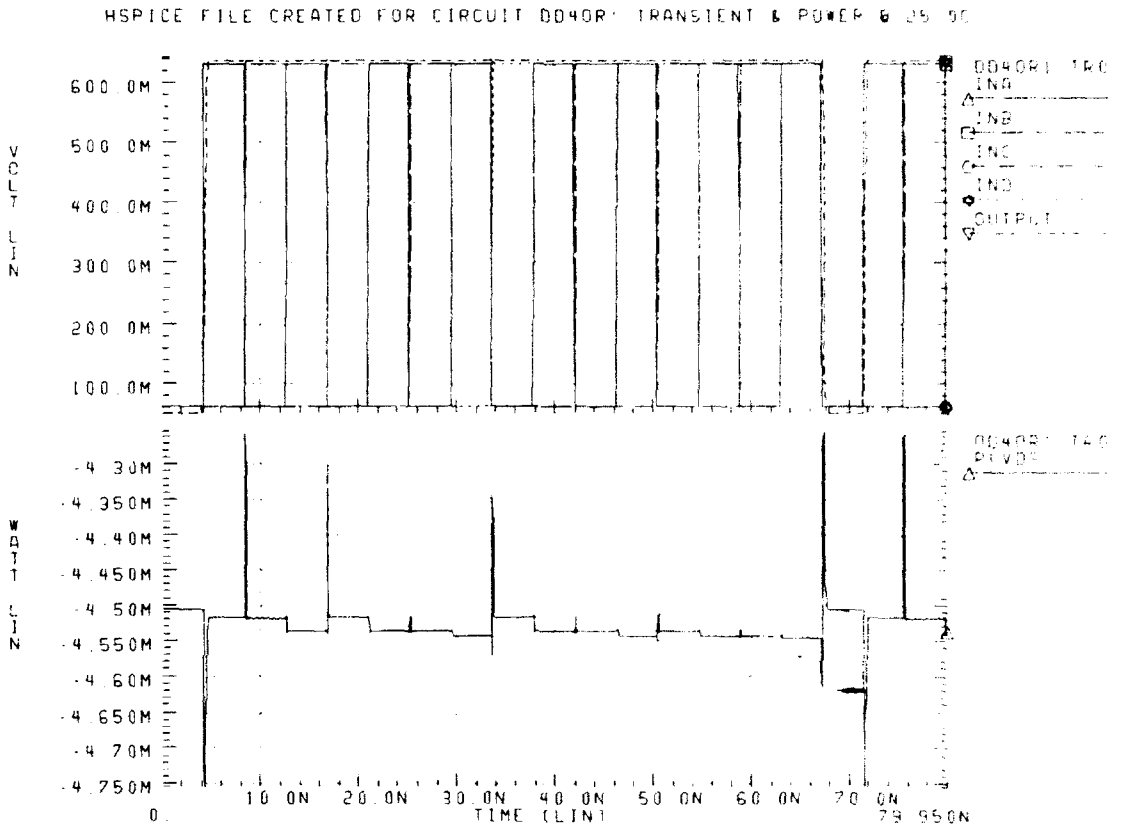


Figure 4.62 DD4OR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DD4OR operating at a temperature of 85.0C is shown in Figure 4.63 on page 67.

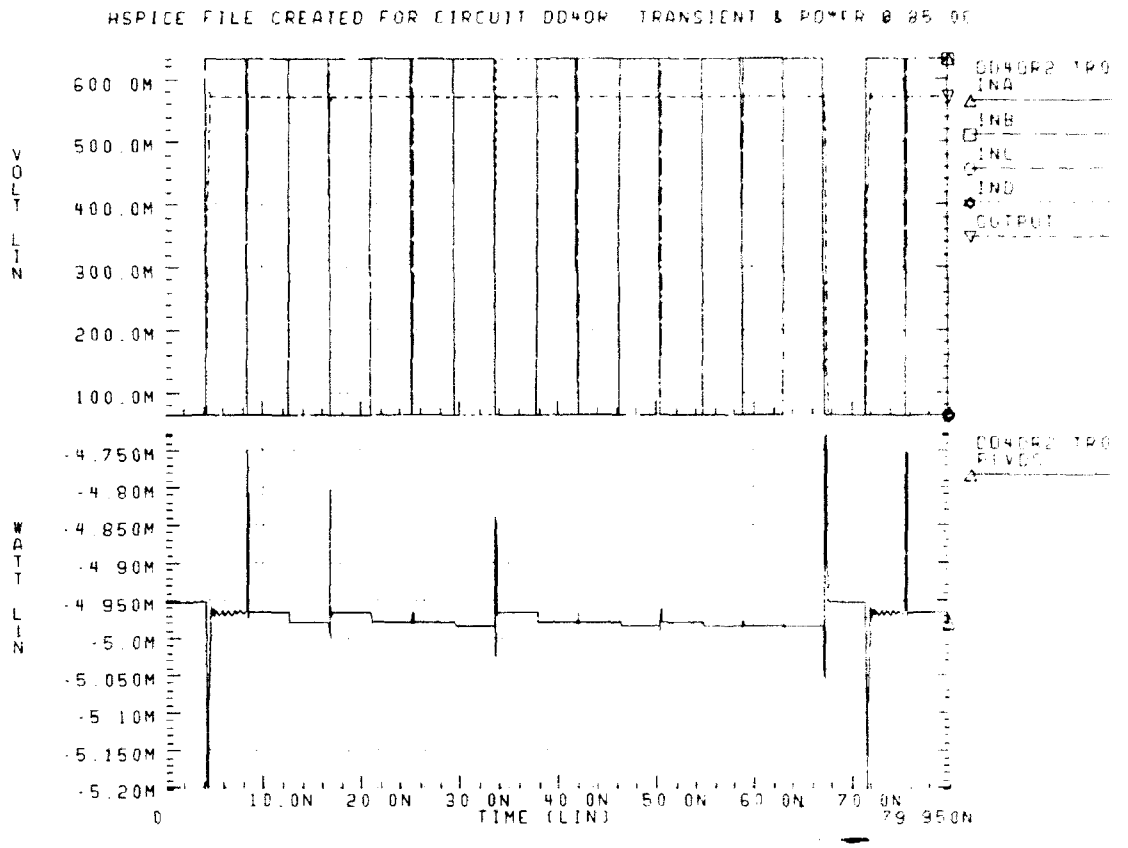


Figure 4.63 DD4OR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DD4OR logic gate operating at a temperature of 25.0C is shown in Figure 4.64 on page 68.

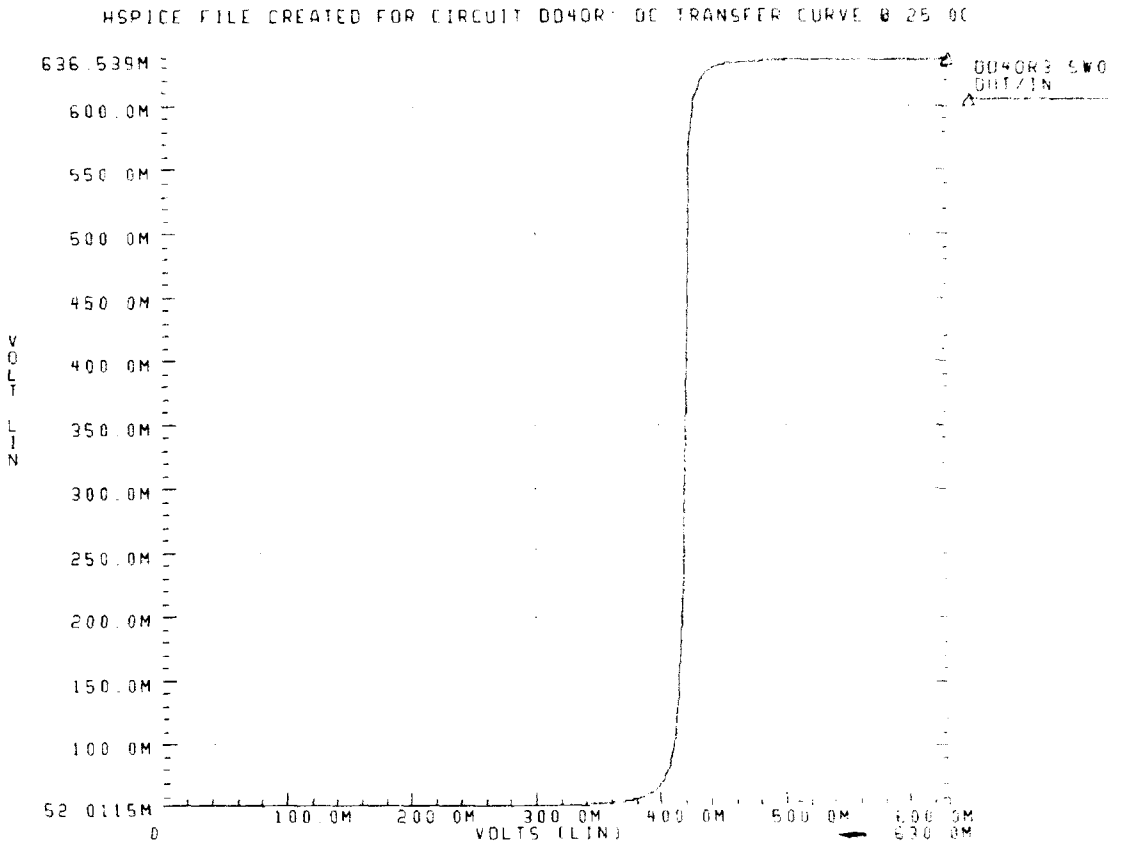


Figure 4.64 DD4OR DC Transfer Curve at 25.0C

The DC transfer characteristic of the DD4OR logic gate operating at a temperature of 85.0C is shown in Figure 4.65 on page 69.

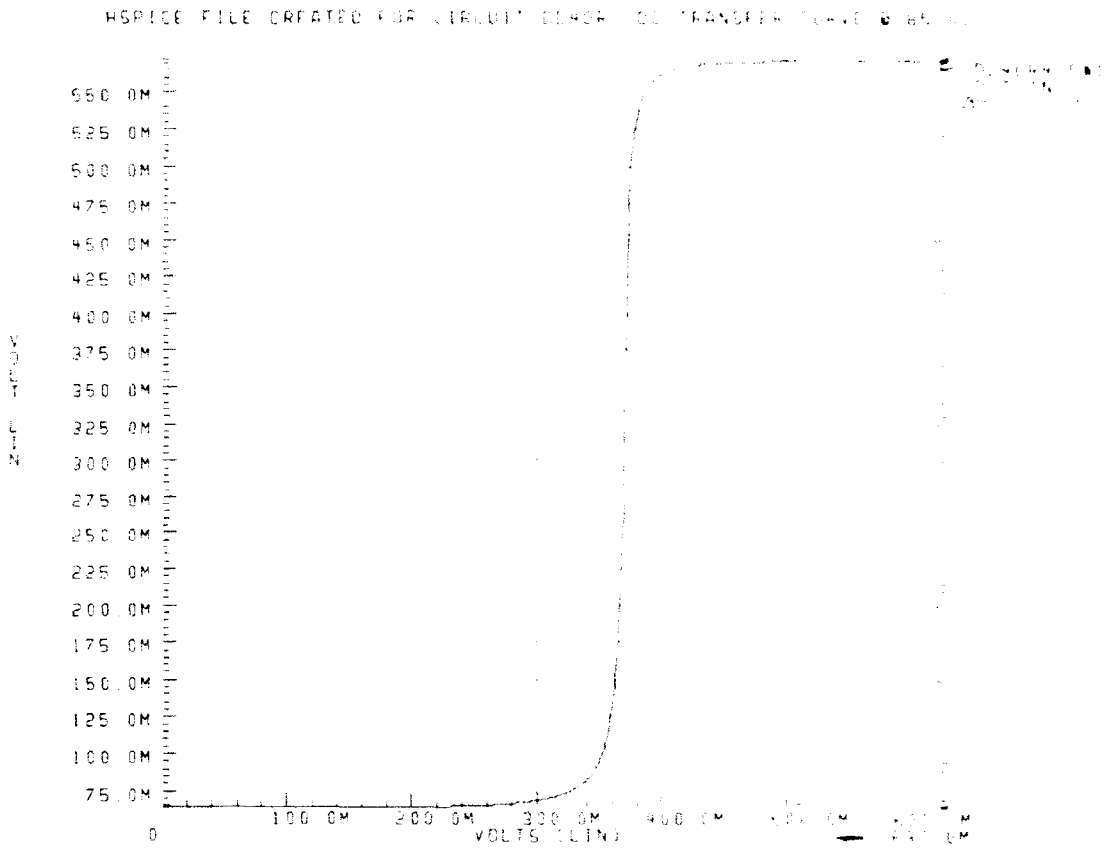


Figure 4.65 DD4OR DC Transfer Curve at 85.0C

14. "BIG" DCFL INVERTER (BDINV)

A very fast and powerful DCFL inverter was required for several circuits specifically, DELAY and BS2AND. The sizes of the MESFETs and its associated schematic and logical equivalence are shown in Figure 4.66 on page 69.

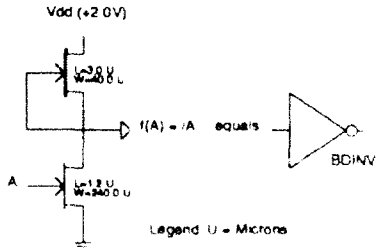


Figure 4.66 BDINV Schematic And Logical Equivalence

The transient analysis and power dissipation of the BDINV operating at a temperature of 25.0C is shown in Figure 4.67 on page 70. Examining Figure 4.67, the "ringing" in the lower (power) graph is believed to be caused by a current surge in the output node. When this logic circuit is used to drive larger circuits for which it was specifically designed, the output node shows no "ringing" because of the dampening factor of the increased load. For an excellent discussion of the device physics, see [Ref. 10:pp. 11-/8].

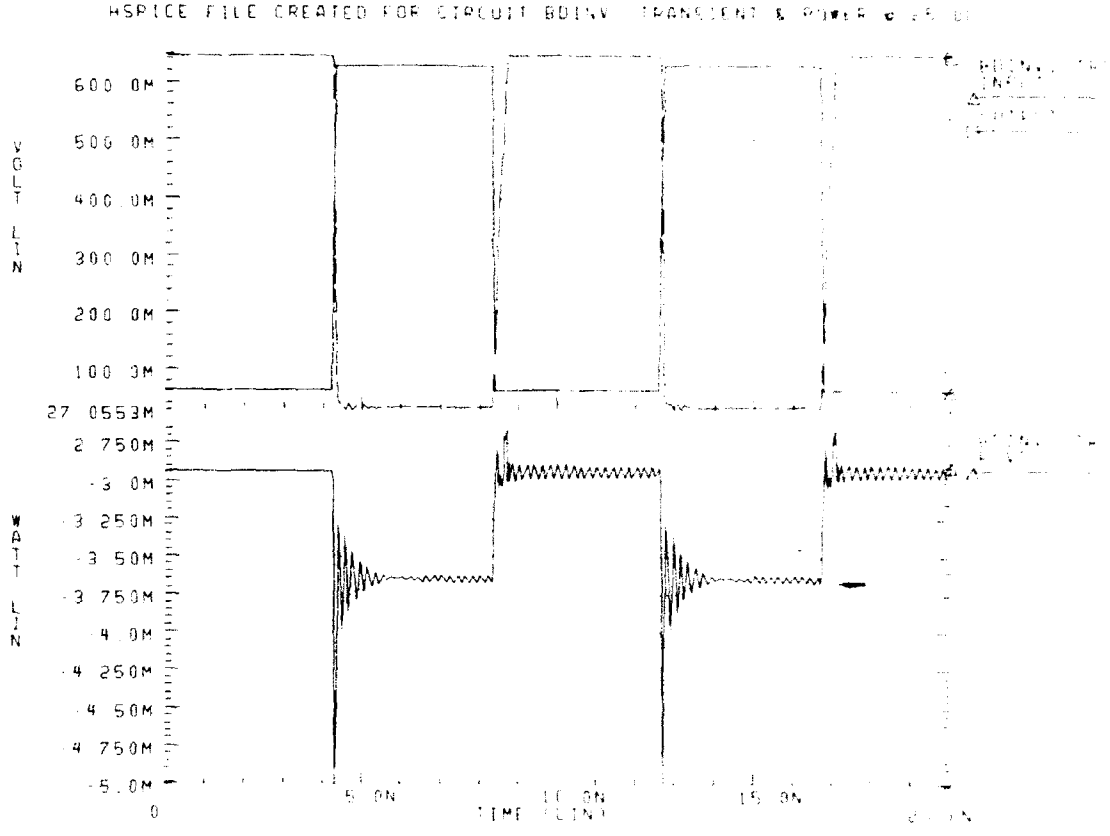


Figure 4.67 BDINV HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the BDINV operating at a temperature of 85.0C is shown in Figure 4.68 on page 71.

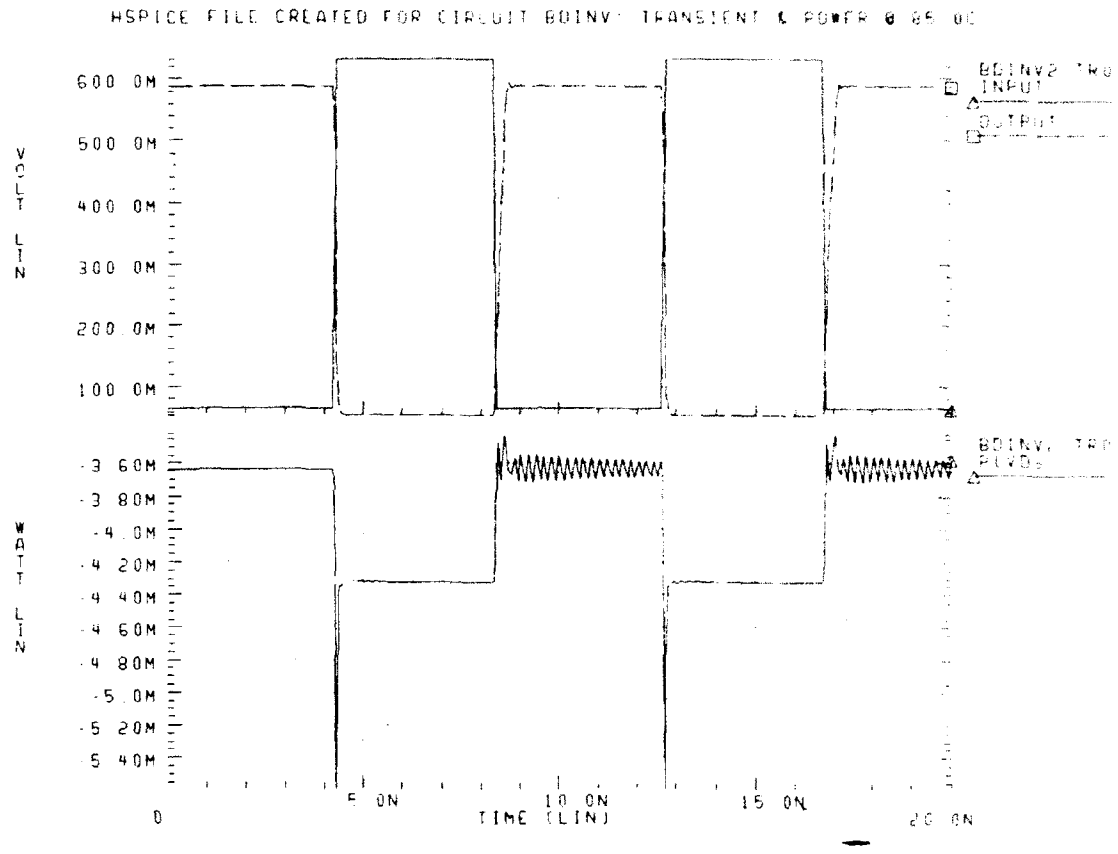


Figure 4.68 BDINV HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the BDINV logic gate operating at a temperature of 25.0C is shown in Figure 4.69 on page 72.

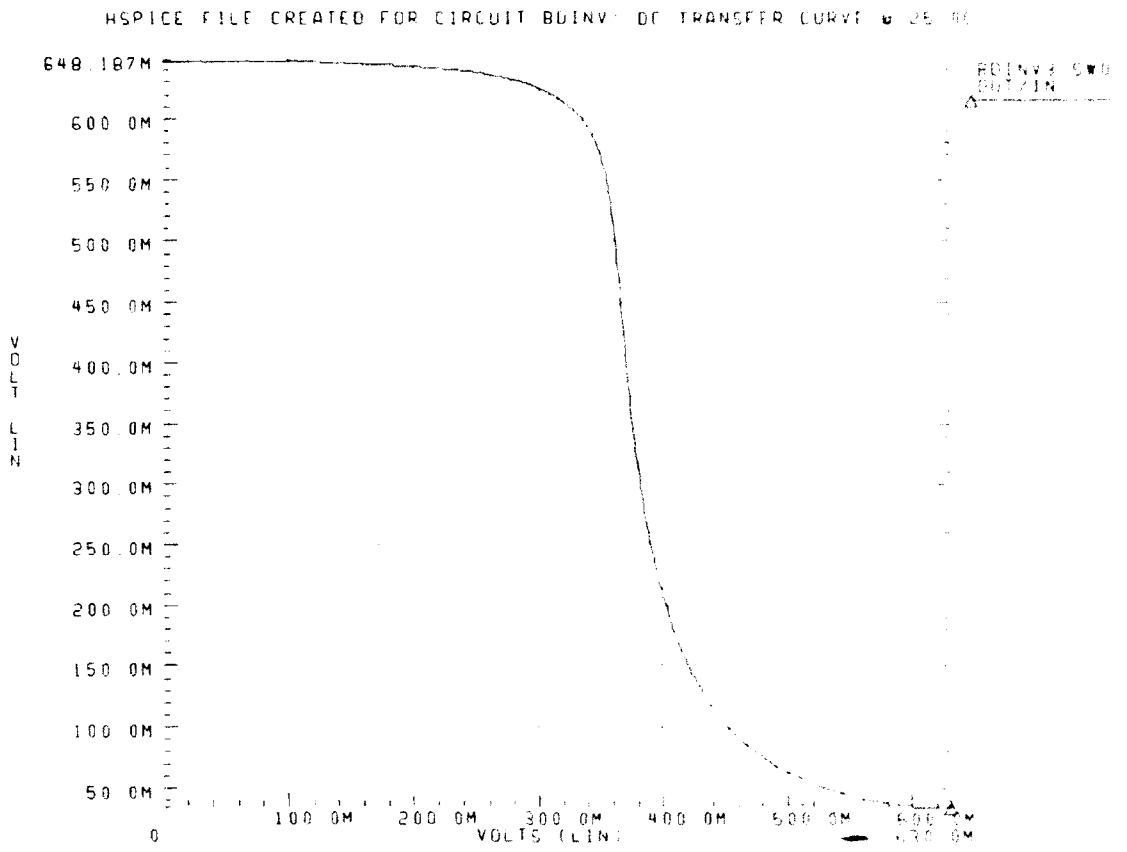


Figure 4.69 BDINV DC Transfer Curve at 25.0C

The DC transfer characteristic of the BDINV logic gate operating at a temperature of 85.0C is shown in Figure 4.70 on page 73.

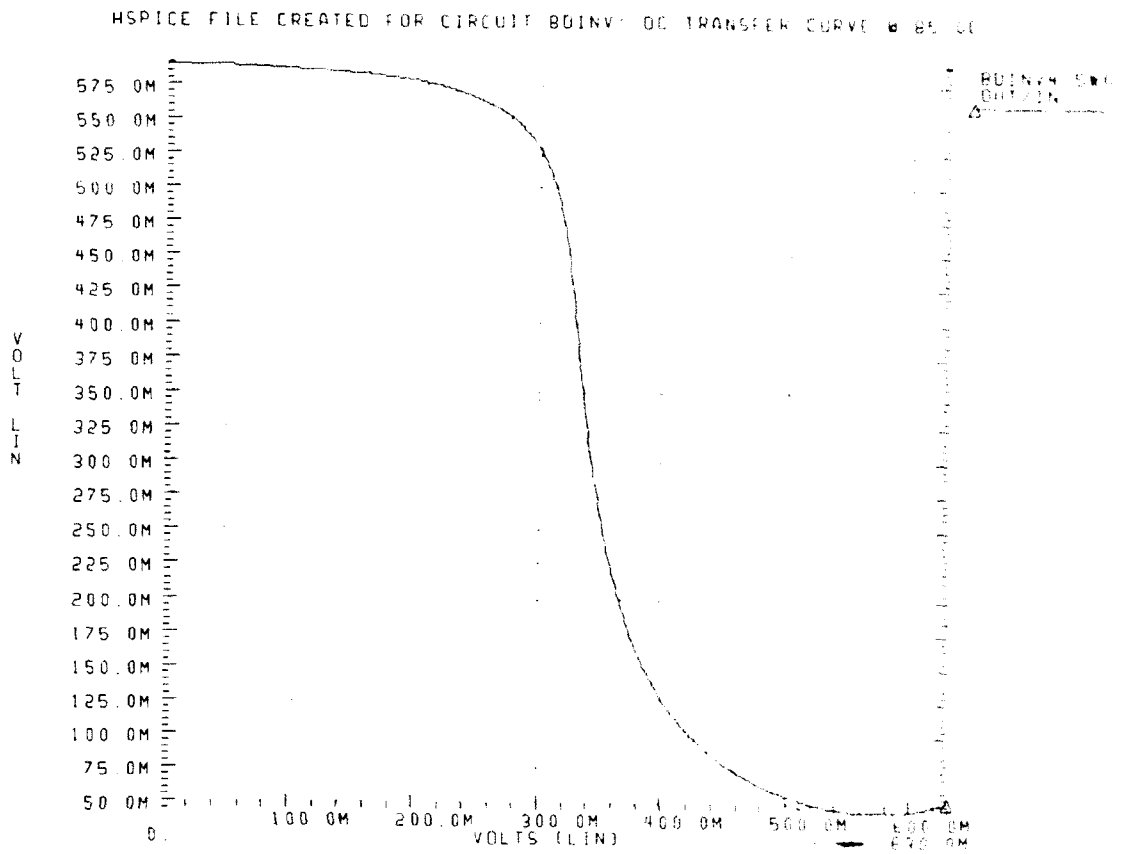


Figure 4.70 BDINV DC Transfer Curve at 85.0C

15. DCFL LATCH (DLATCH)

A data latch is constructed from DCFL logic gates. The DLATCH circuit schematic and logical equivalence are shown in Figure 4.71 on page 73.

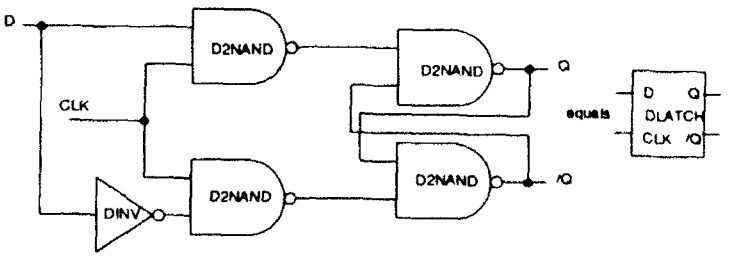


Figure 4.71 DLATCH Schematic And Logical Equivalence

The transient analysis and power dissipation of the DLATCH operating at a temperature of 25.0C is shown in Figure 4.72 on page 74. See "Listing File for DLATCH Transient Analysis @ 25.0C" of Appendix A on page 279.

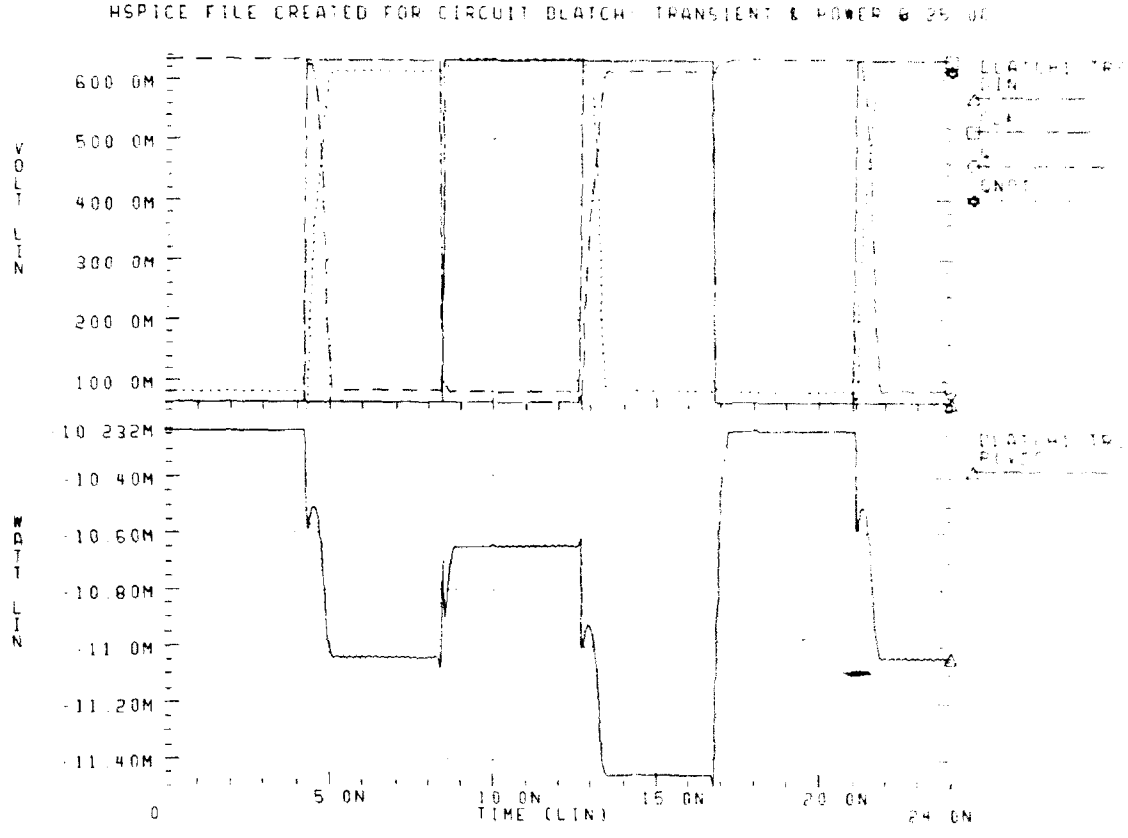


Figure 4.72 DLATCH HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DLATCH operating at a temperature of 85.0C is shown in Figure 4.73 on page 75.

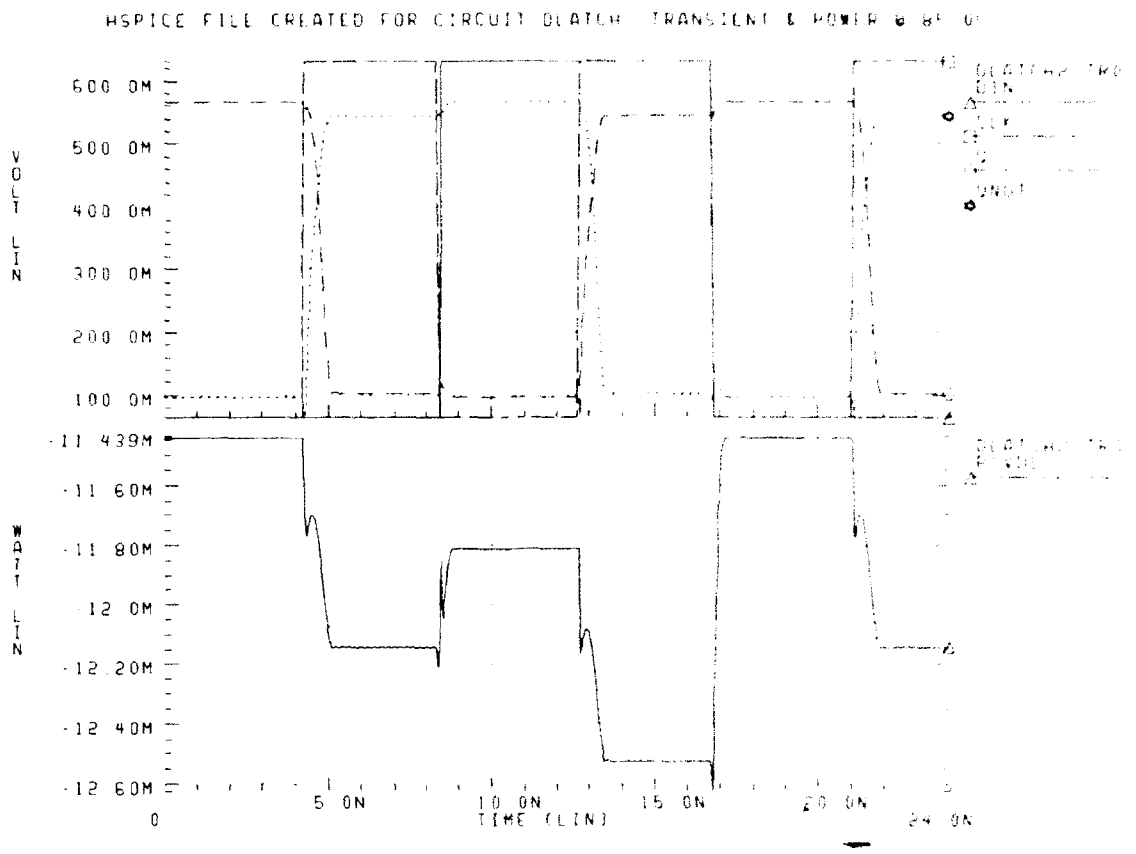


Figure 4.73 DLATCH HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DLATCH logic gate operating at a temperature of 25.0C is shown in Figure 4.74 on page 76.

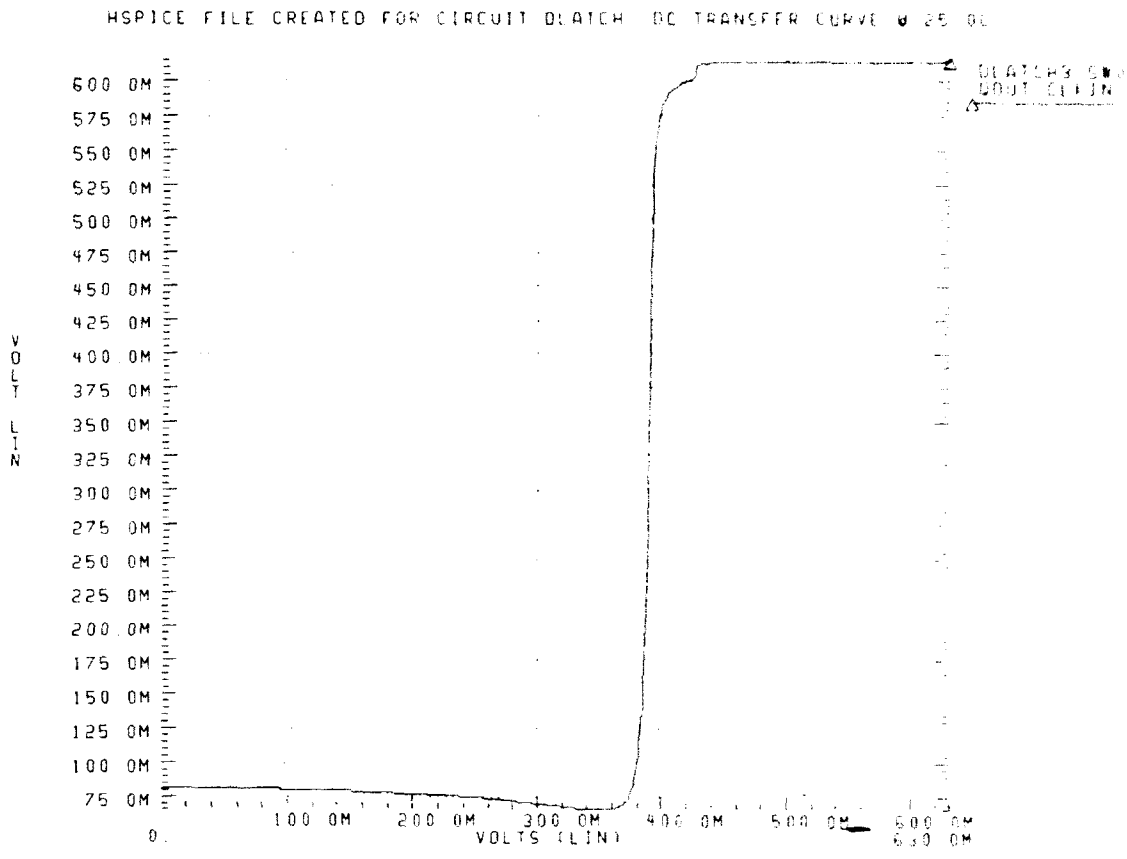


Figure 4.74 DLATCH DC Transfer Curve at 25.0C

The DC transfer characteristic of the DLATCH logic gate operating at a temperature of 85.0C is shown in Figure 4.75 on page 77.

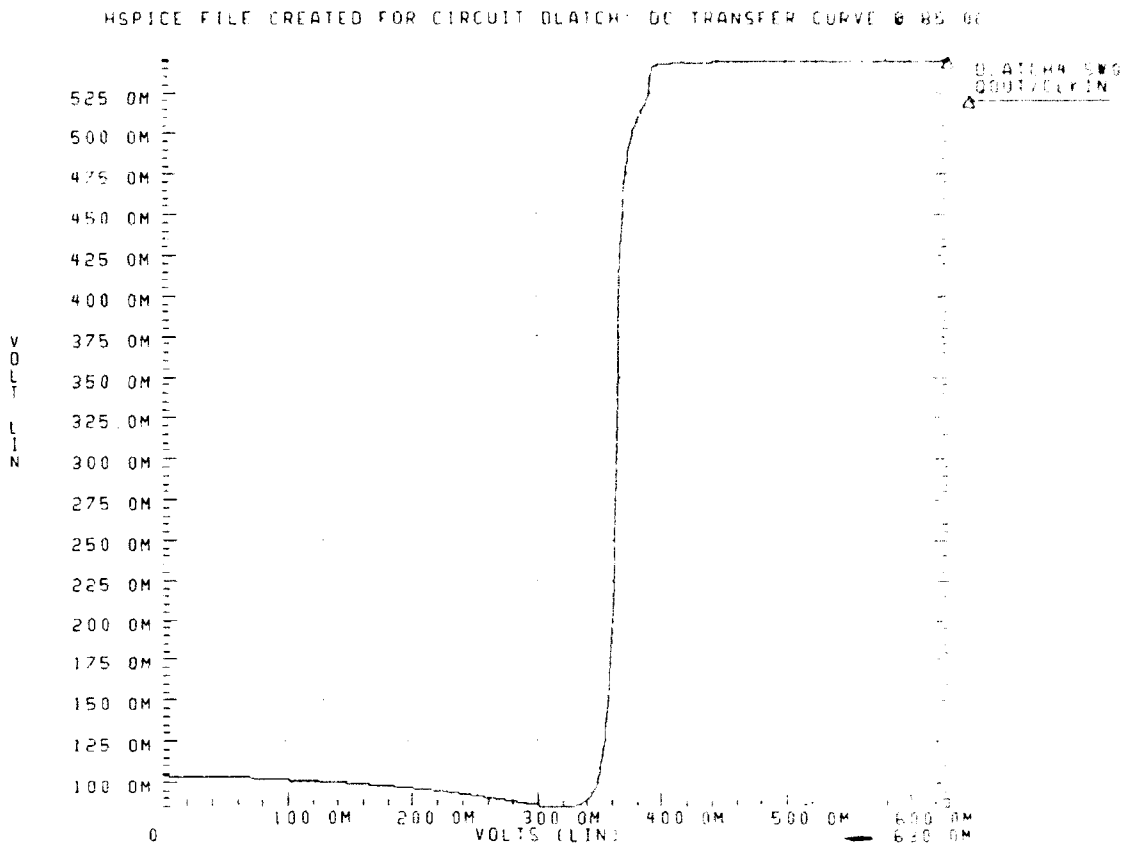


Figure 4.75 DLATCH DC Transfer Curve at 85.0C

16. DCFL /Clear Data Flip-Flop (CPDFF)

A data flip-flop with asynchronous active low CLEAR is constructed from DCFL logic gates. This logic element was constructed specifically for use in the COUNTER circuit. The CPDFF circuit schematic and logical equivalence are shown in Figure 4.76 on page 78.

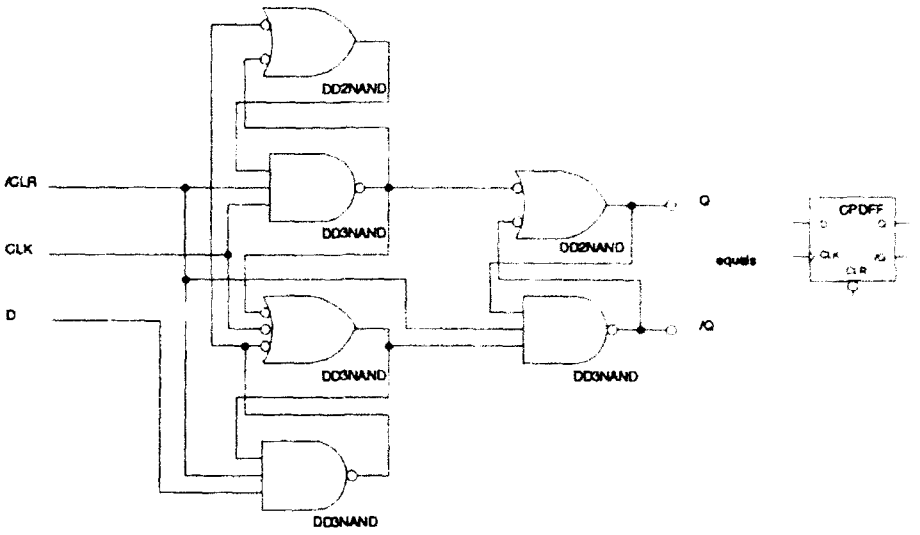


Figure 4.76 CPDFF Schematic And Logical Equivalence

The transient analysis and power dissipation of the CPDFF operating at a temperature of 25.0C is shown in Figure 4.77 on page 79. See "Listing File for CPDFF Transient Analysis @ 25.0C" of Appendix A on page 275.

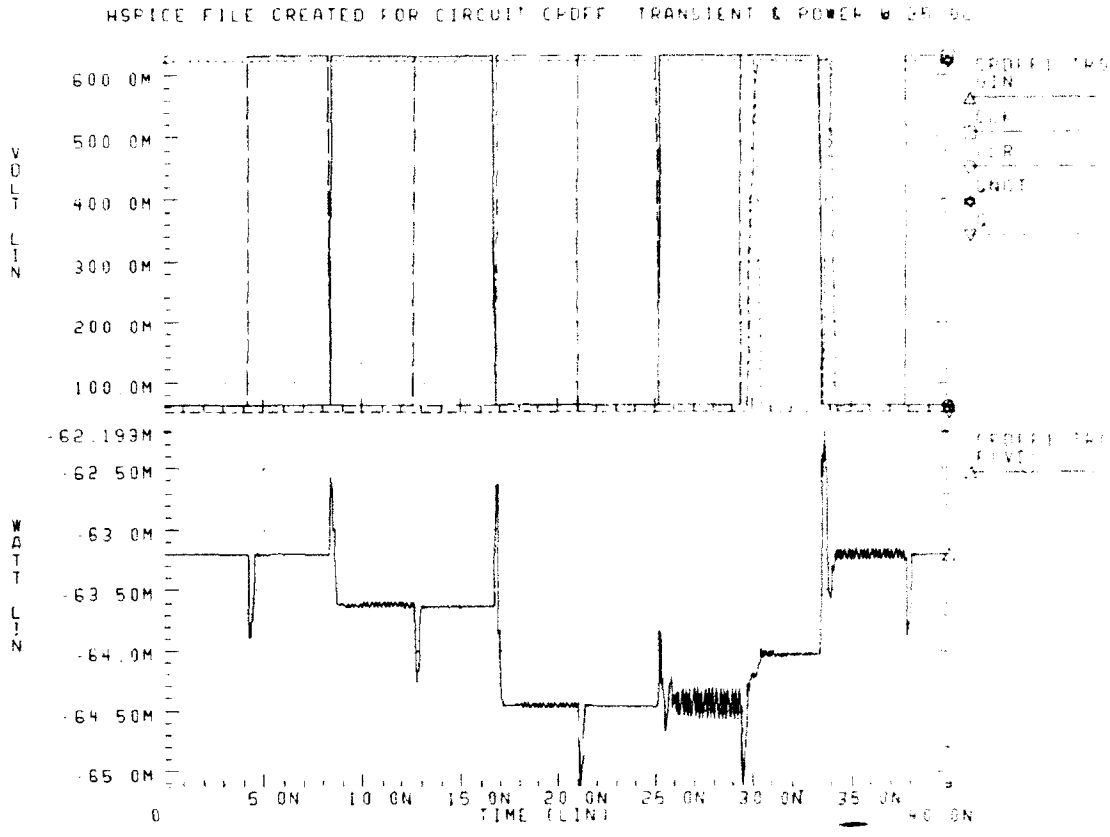


Figure 4.77 CPDFF HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the CPDFF operating at a temperature of 85.0C is shown in Figure 4.78 on page 80.

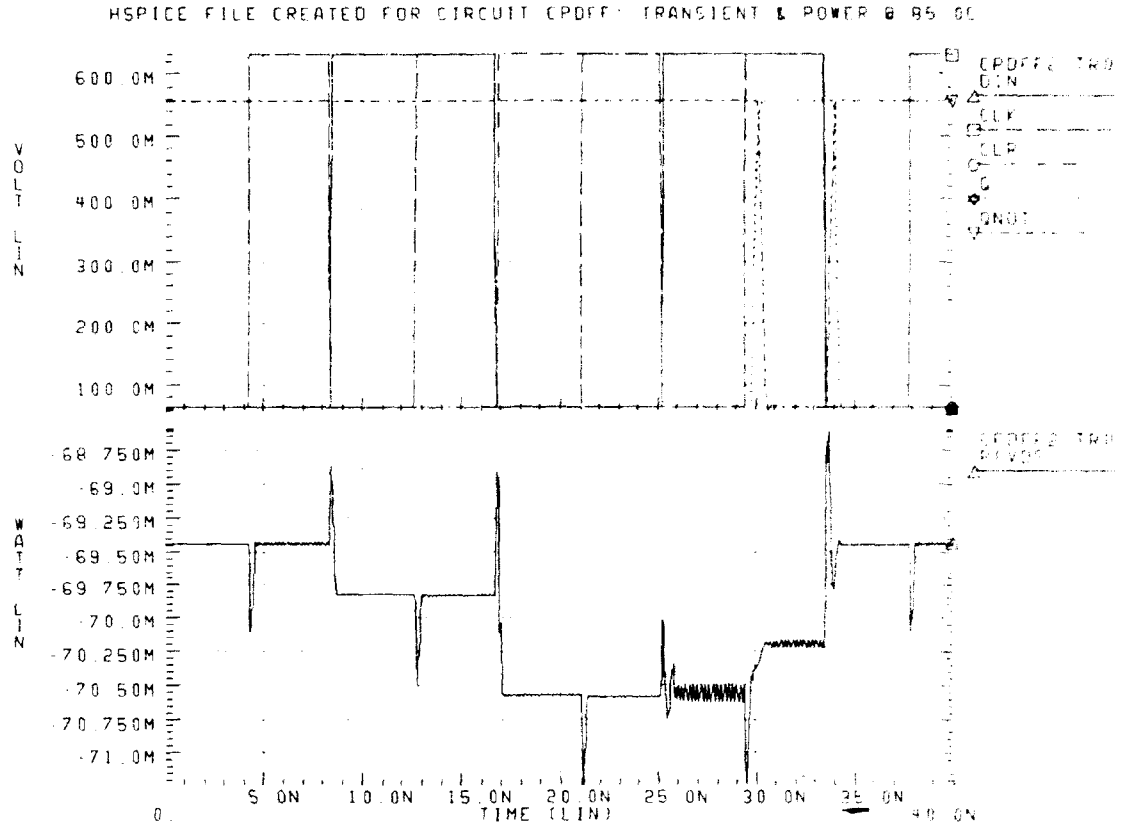


Figure 4.78 CPDFF HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the CPDFF logic gate operating at a temperature of 25.0C is shown in Figure 4.79 on page 81.

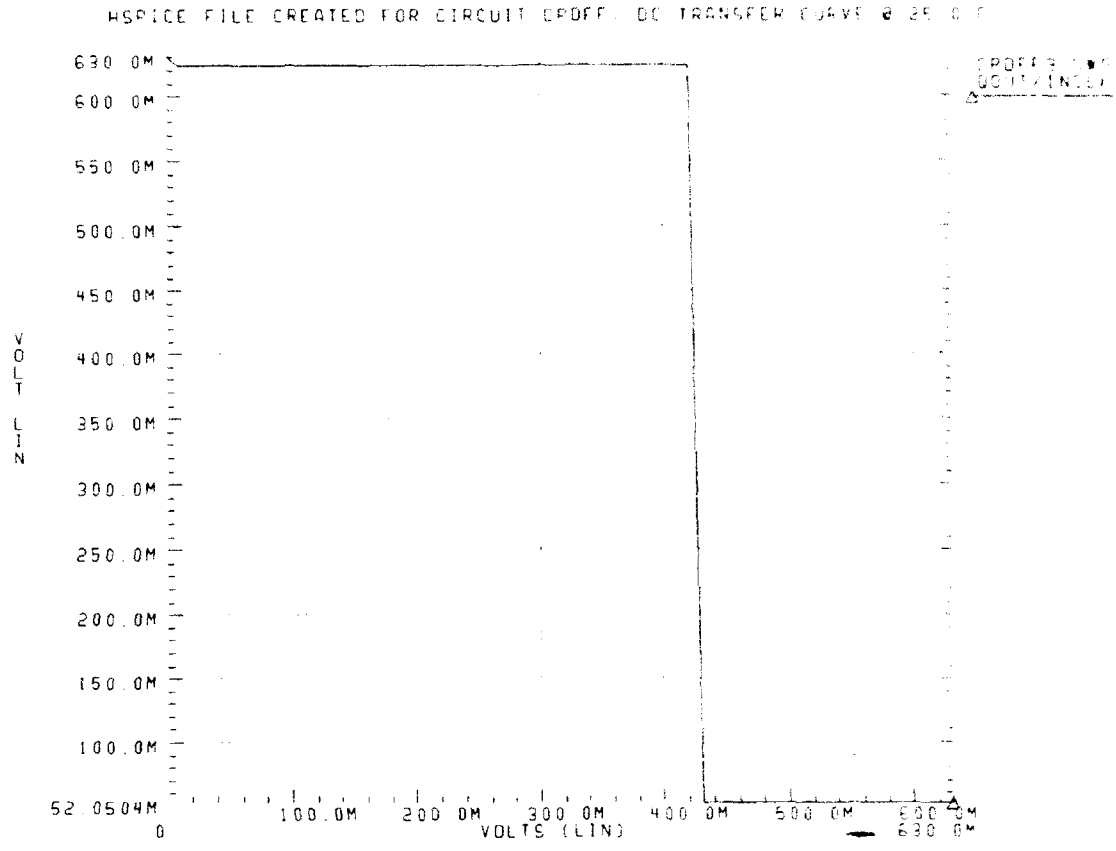


Figure 4.79 CPDFF DC Transfer Curve at 25.0C

The DC transfer characteristic of the CPDFF logic gate operating at a temperature of 85.0C is shown in Figure 4.80 on page 82.

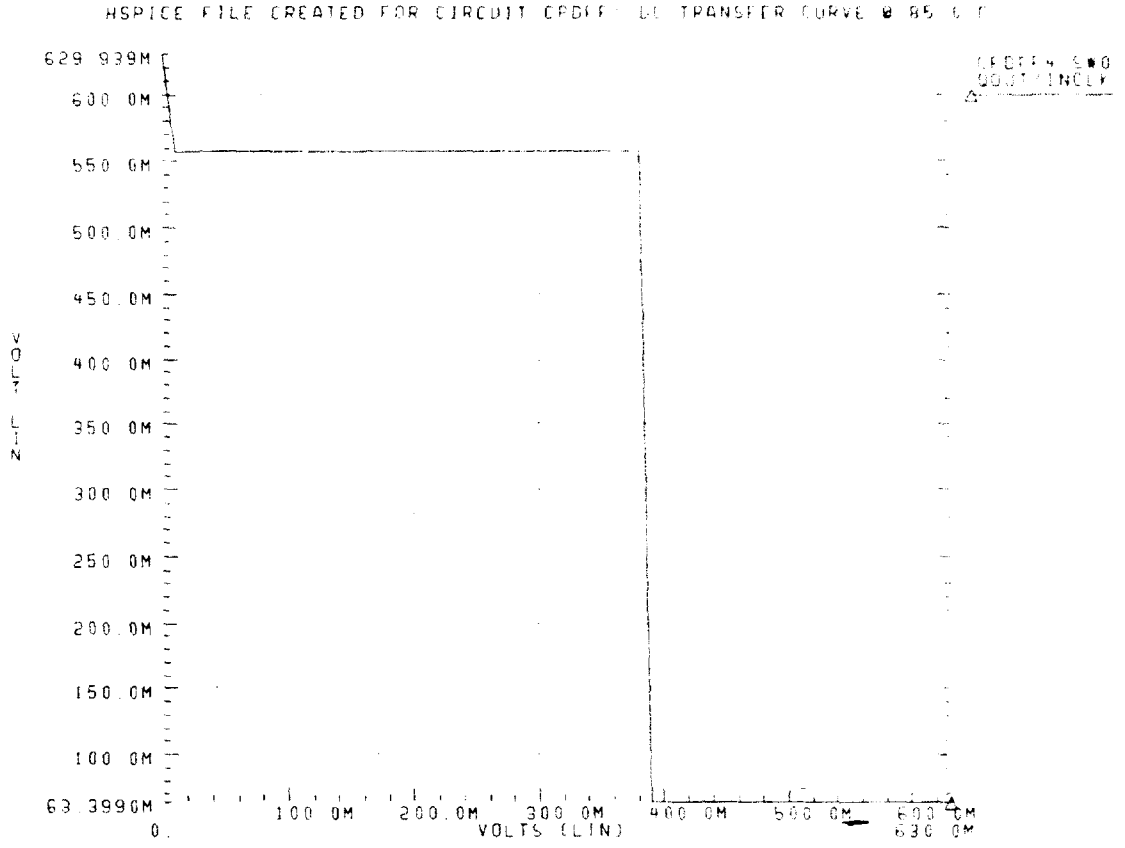


Figure 4.80 CPDFF DC Transfer Curve at 85.0C

B. GaAs DRAM SBFL Logic Circuits

This section will present the specific SBFL gates used, presenting the schematic and logical equivalence for each. The following characteristics for each circuit will be demonstrated and presented: transient analysis under standard load, power consumption at nominal and high temperature, propagation delays and noise margins. These characteristics will be further summarized in TABLE 4.1 on page 158.

1. SBFL Inverter (SINV)

The basic and most widely used SBFL logic element was the inverter, hereafter called "SINV" for SBFL Inverter. As previously mentioned, true NAND gates were infrequently used, the more common SBFL ANDs, NANDs, and ORs were built using NORs with SINVs as per DeMorgan's theorems. See Figure 4.81 on page 83 for the SINV schematic and logical equivalence.

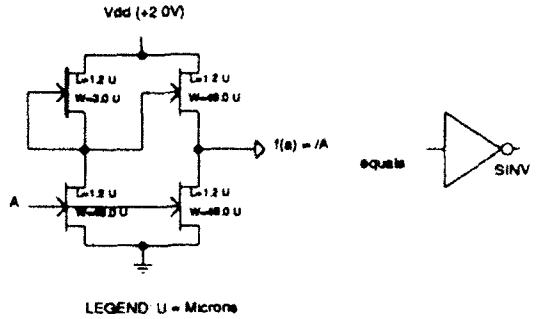


Figure 4.81 Schematic and Logical Equivalence for SINV

The transient analysis and power dissipation of the SINV operating at a temperature of 25.0C is shown in Figure 4.82 on page 83.

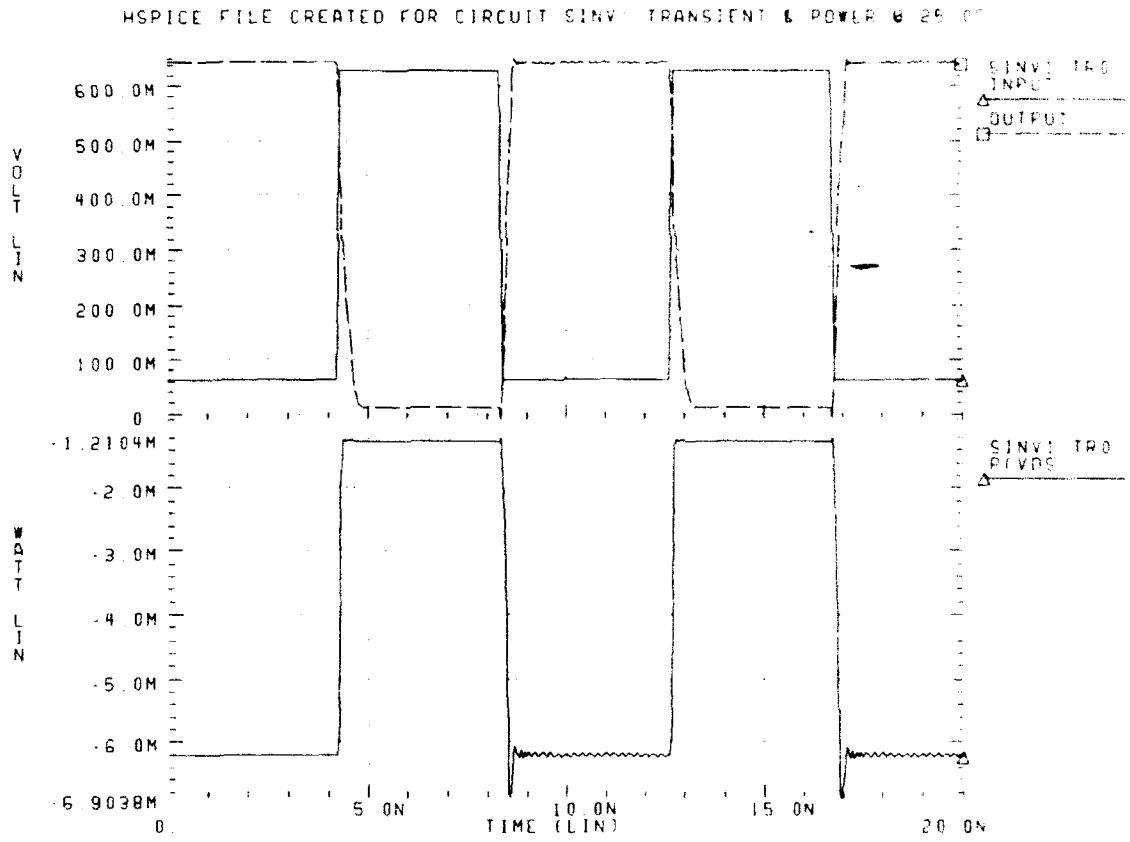


Figure 4.82 SINV HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the SINV operating at a temperature of 85.0C is shown in Figure 4.83 on page 84.

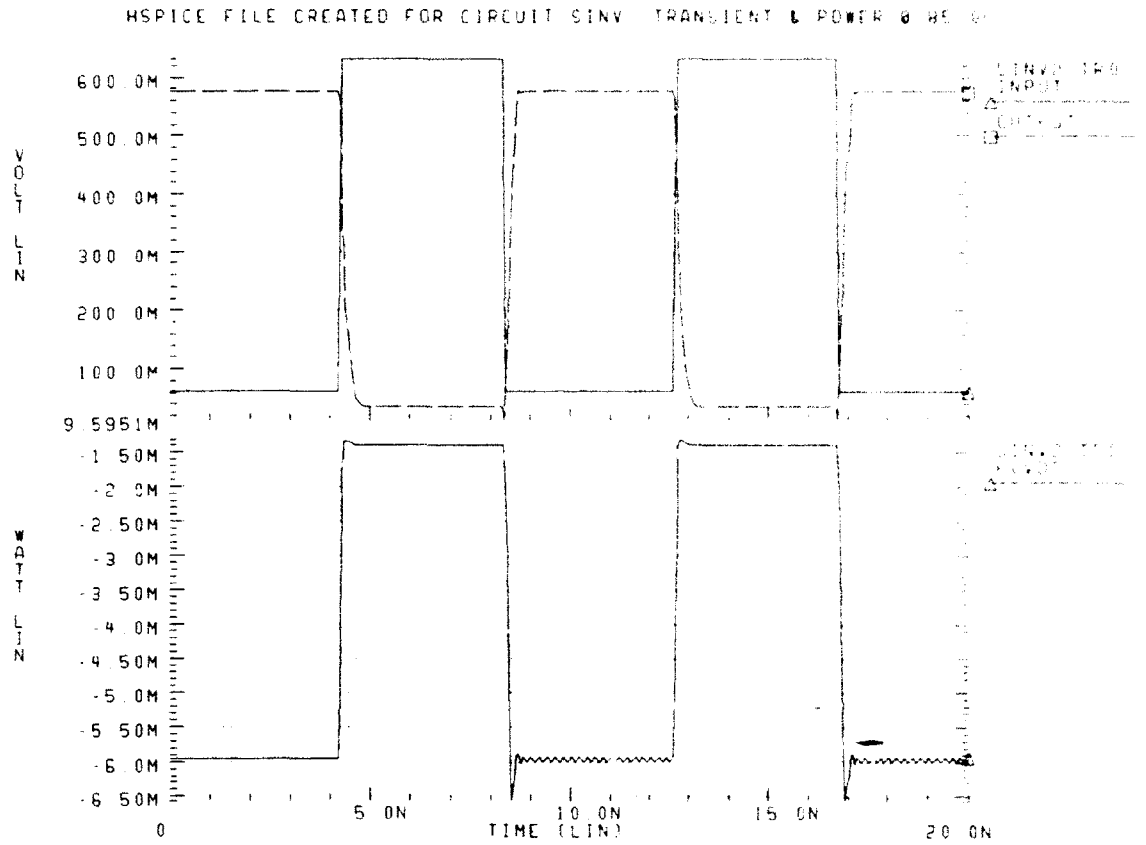


Figure 4.83 SINV HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the SINV logic gate operating at a temperature of 25.0C is shown in Figure 4.84 on page 85.

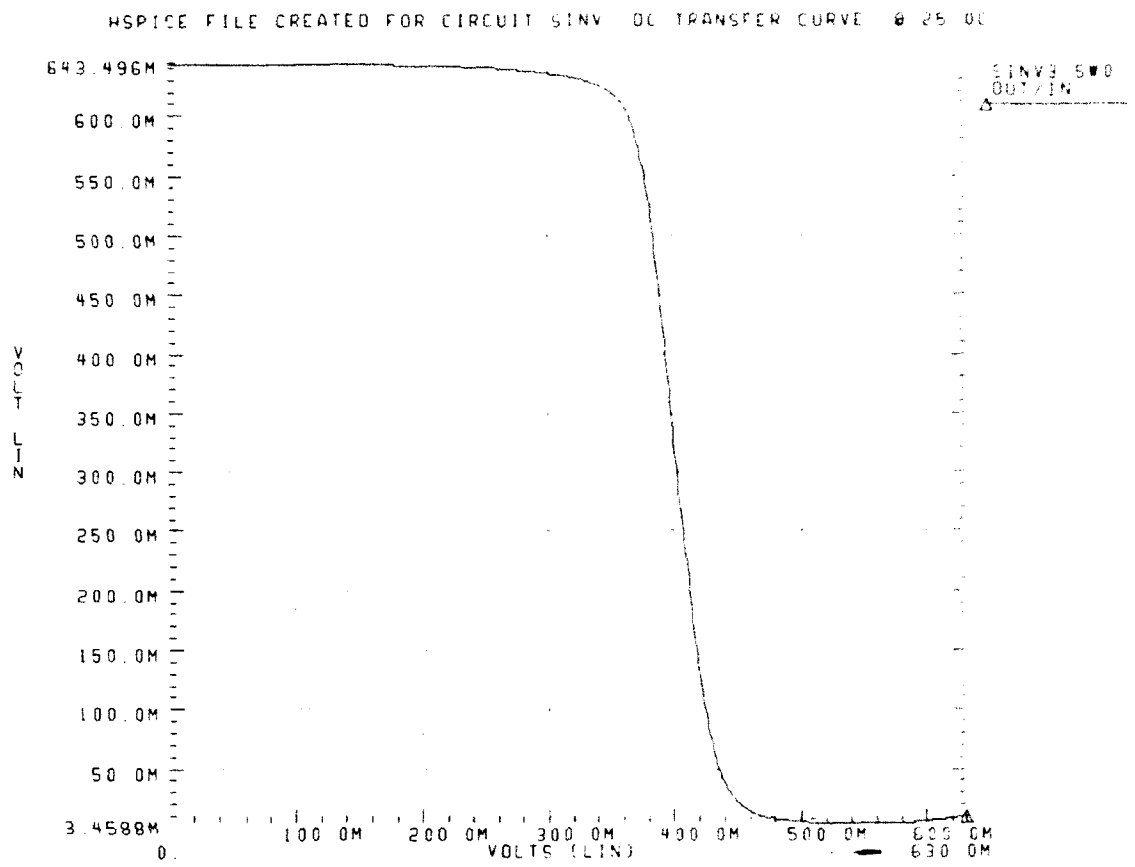


Figure 4.84 SINV DC Transfer Curve at 25.0C

The DC transfer characteristic of the SINV logic gate operating at a temperature of 85.0C is shown in Figure 4.85 on page 86.

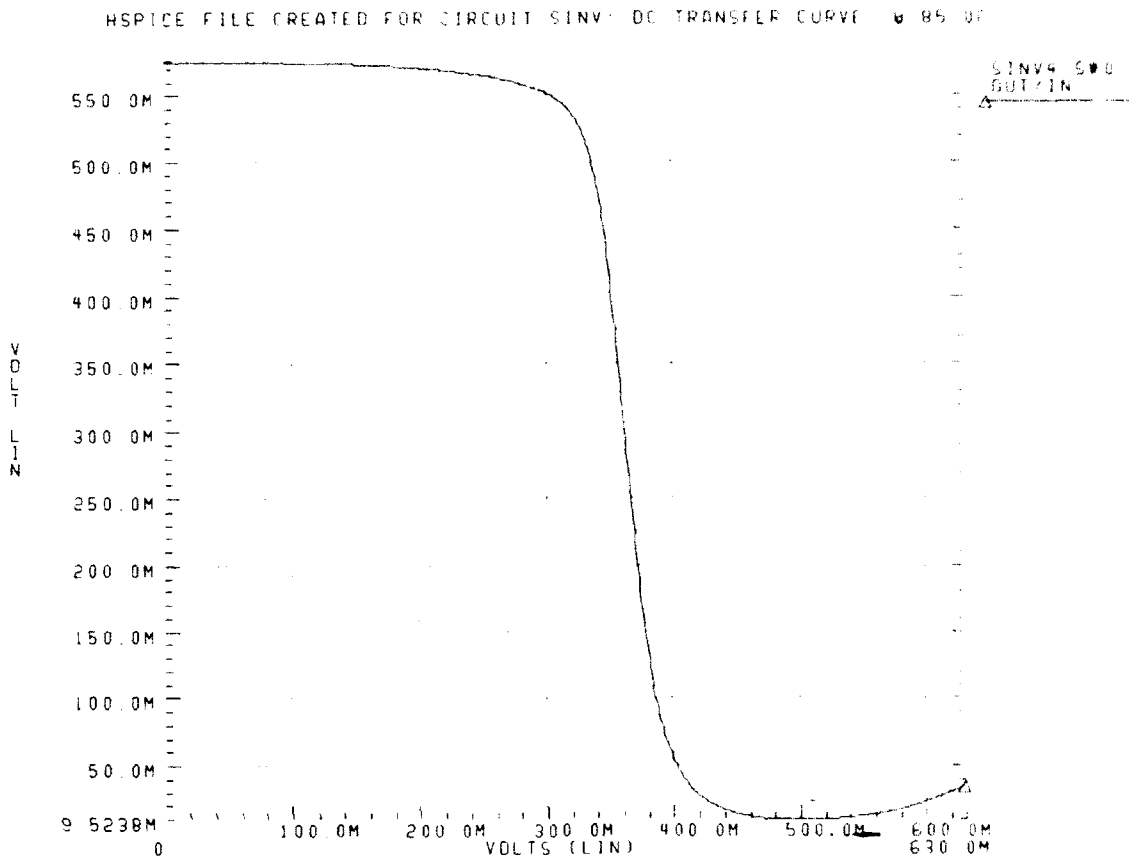


Figure 4.85 SINV DC Transfer Curve at 85.0C

2. Super SBFL Inverter (SSINV)

It was necessary to construct a very fast and powerful driver-inverter for use in the CLOCK circuit. Two reasons were the need to drive many gates and the need to minimize clock skew under heavy load. This SBFL logic element was the super SBFL inverter, hereafter called "SSINV". This very fast and powerful logic element extracts its cost in chip real estate. The sizes of the SSINV MESFETs are very large. See Figure 4.86 on page 87 for the SSINV schematic and logical equivalence.

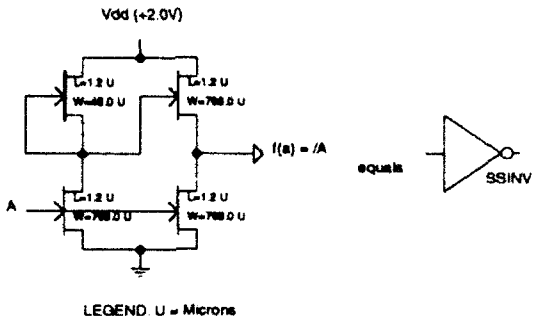


Figure 4.86 Schematic and Logical Equivalence for SSINV

The transient analysis and power dissipation of the SSINV operating at a temperature of 25.0C is shown in Figure 4.87 on page 87.

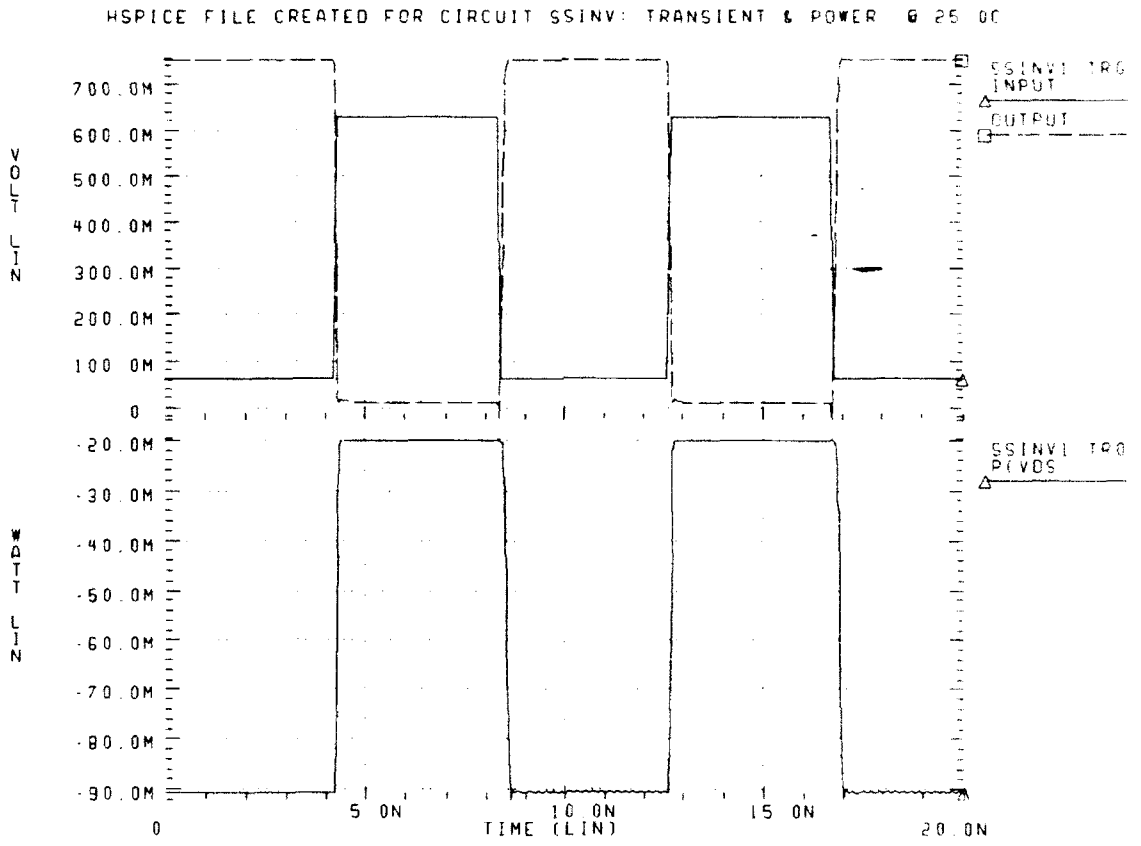


Figure 4.87 SSINV HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the SSINV operating at a temperature of 85.0C is shown in Figure 4.88 on page 88.

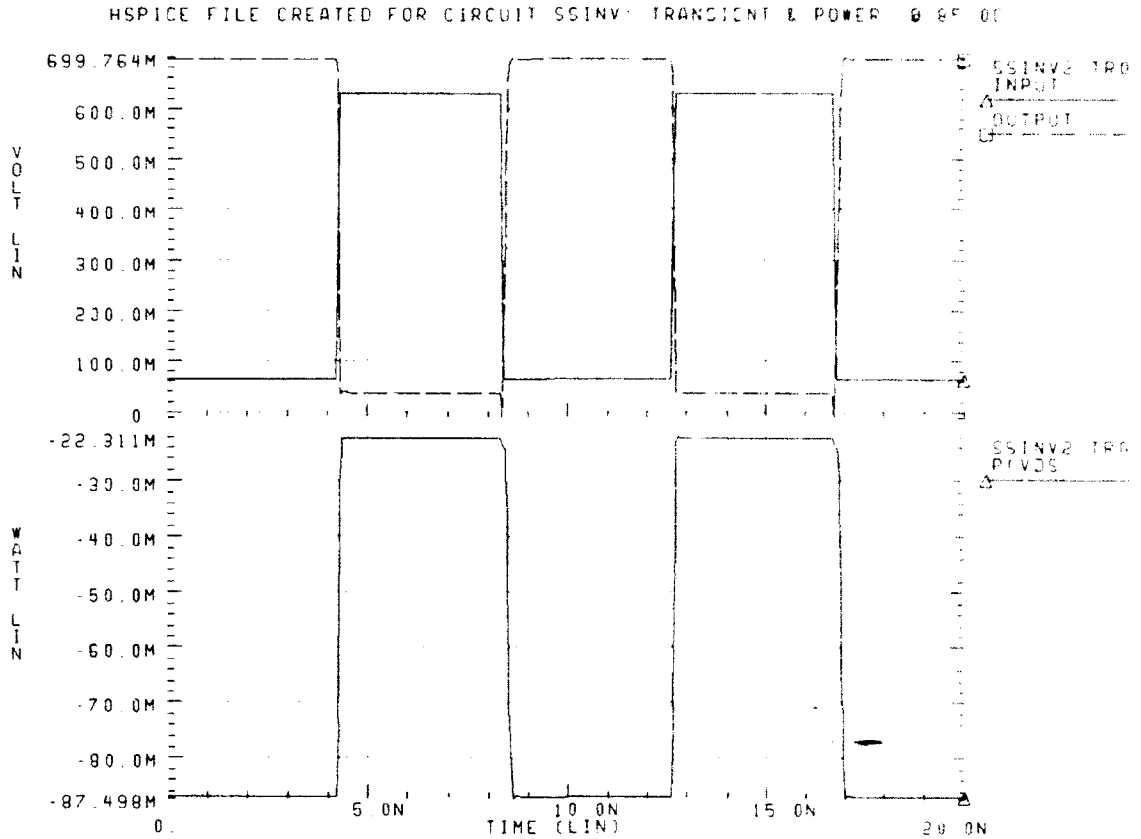


Figure 4.88 SSINV HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the SSINV logic gate operating at a temperature of 25.0C is shown in Figure 4.89 on page 89.

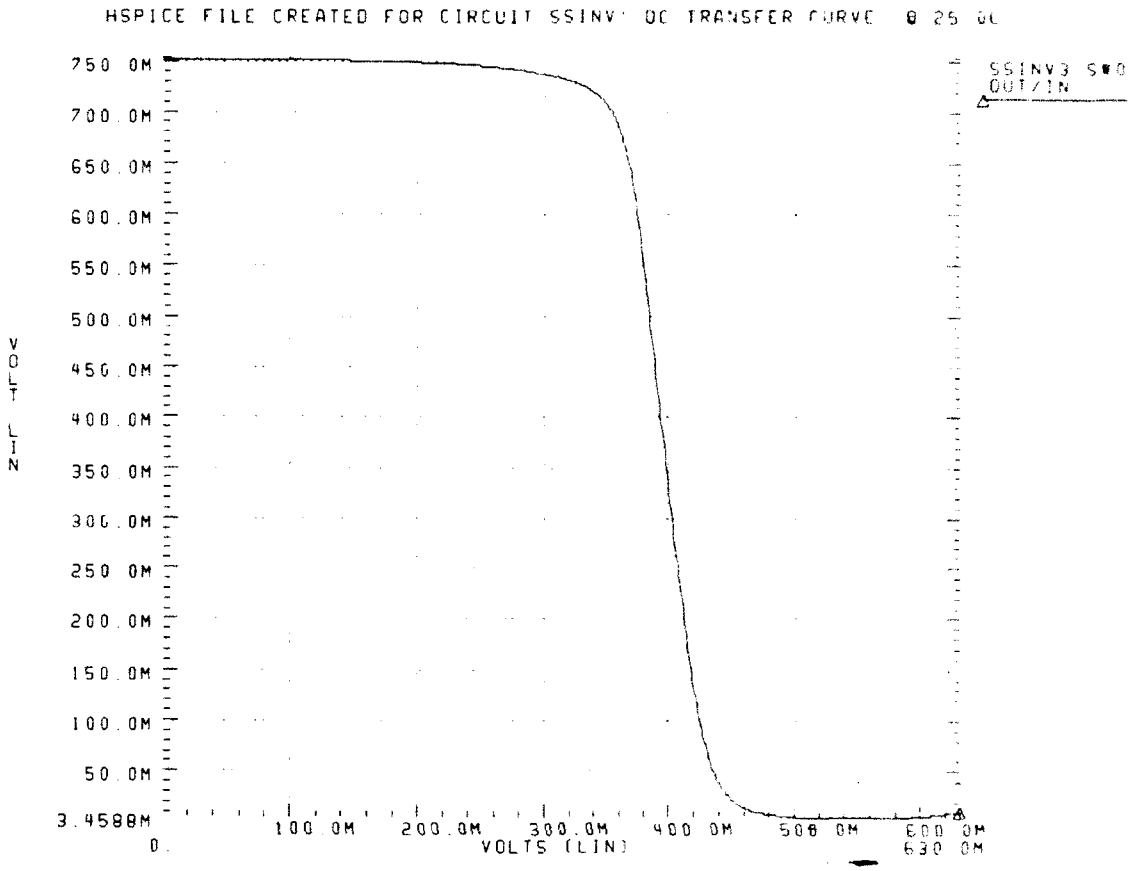


Figure 4.89 SSINV DC Transfer Curve at 25.0C

The DC transfer characteristic of the SSINV logic gate operating at a temperature of 85.0C is shown in Figure 4.85 on page 86.

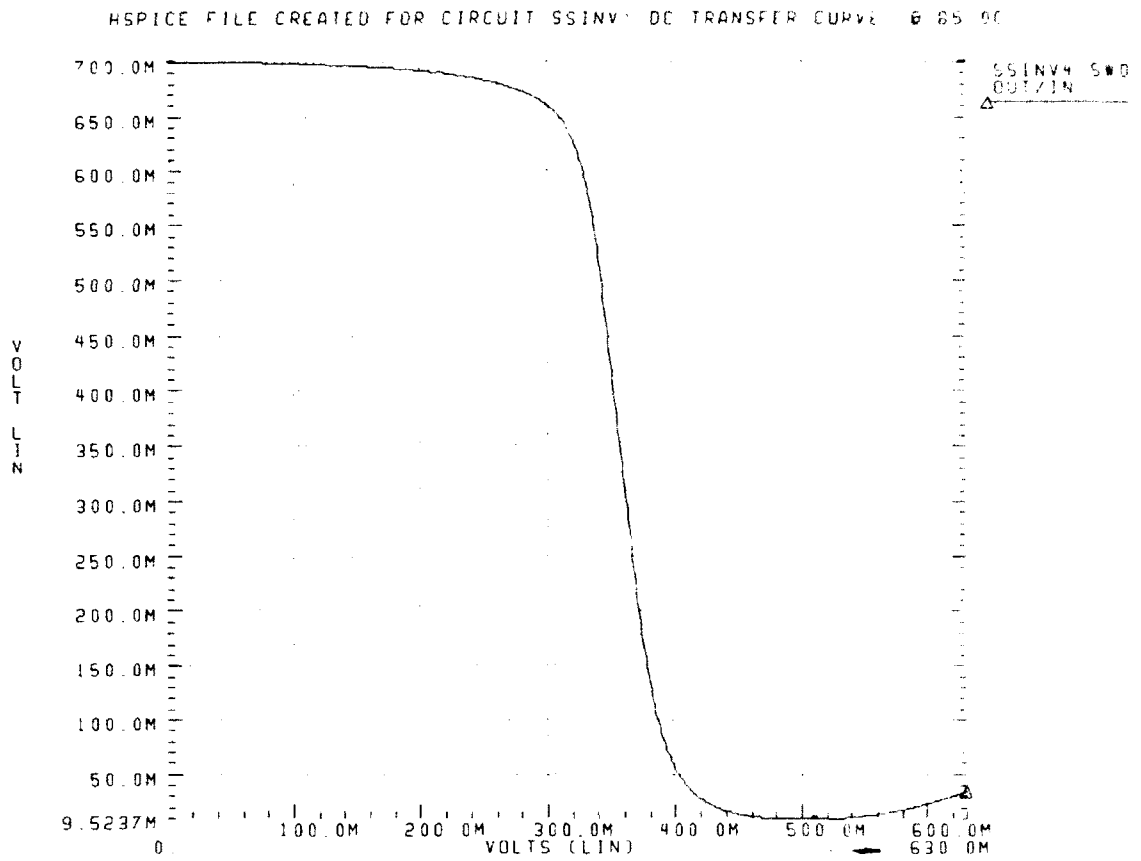


Figure 4.90 SSINV DC Transfer Curve at 85.0C

3. SBFL 2-input NOR Gate (S2NOR)

The following graphs represent the operating characteristics of the S2NOR. As previously mentioned, true NAND gates were infrequently used, the more common SBFL ANDs, NANDs, and ORs were built using NORs with SINVs as per DeMorgan's theorems. See Figure 4.91 on page 91 for the S2NOR schematic and logical equivalence.

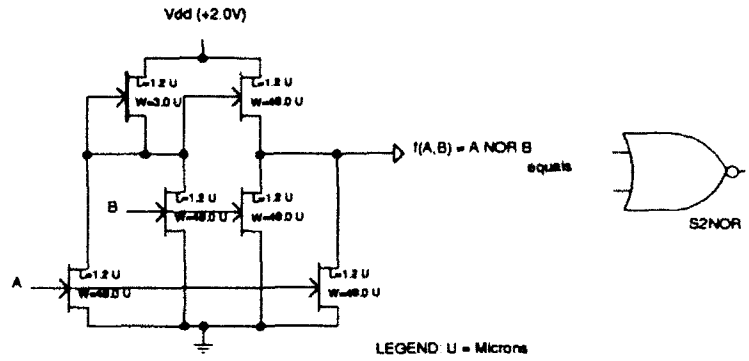


Figure 4.91 Schematic and Logical Equivalence for S2NOR

The transient analysis and power dissipation of the S2NOR operating at a temperature of 25.0C is shown in Figure 4.92 on page 91.

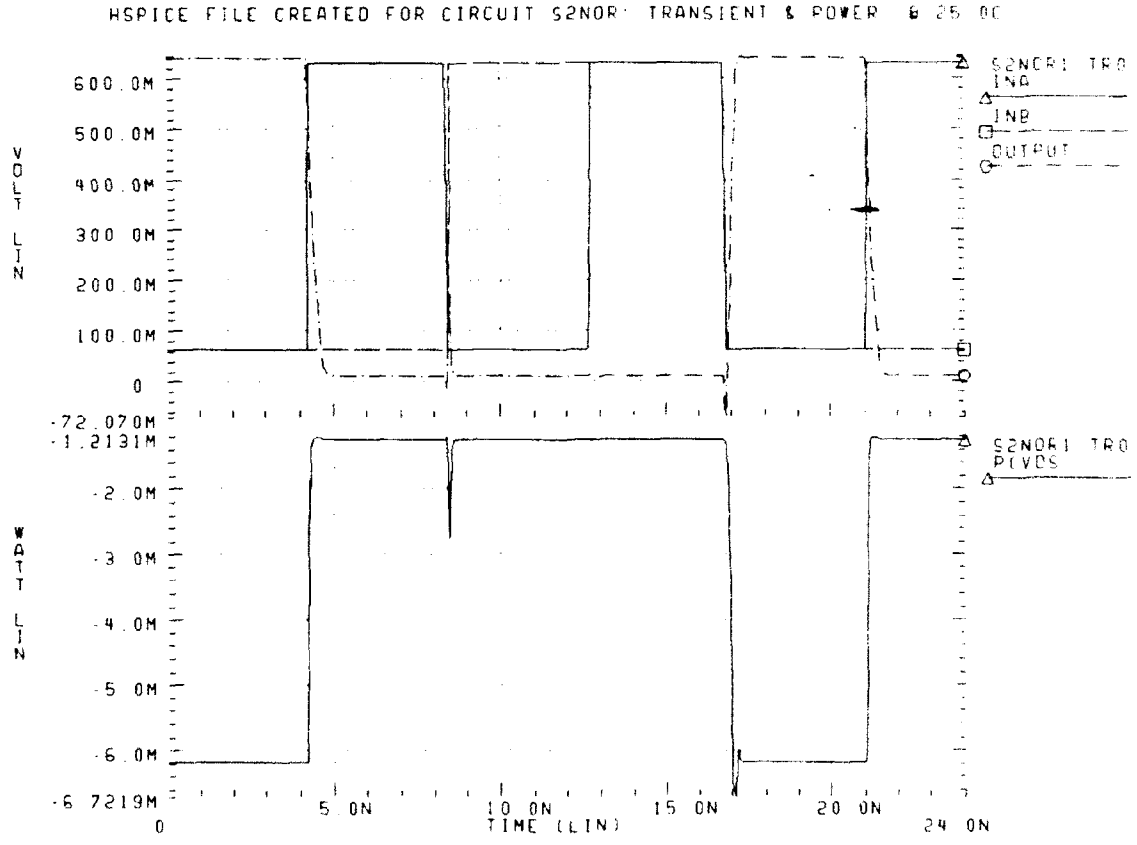


Figure 4.92 S2NOR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the S2NOR operating at a temperature of 85.0C is shown in Figure 4.93 on page 92.

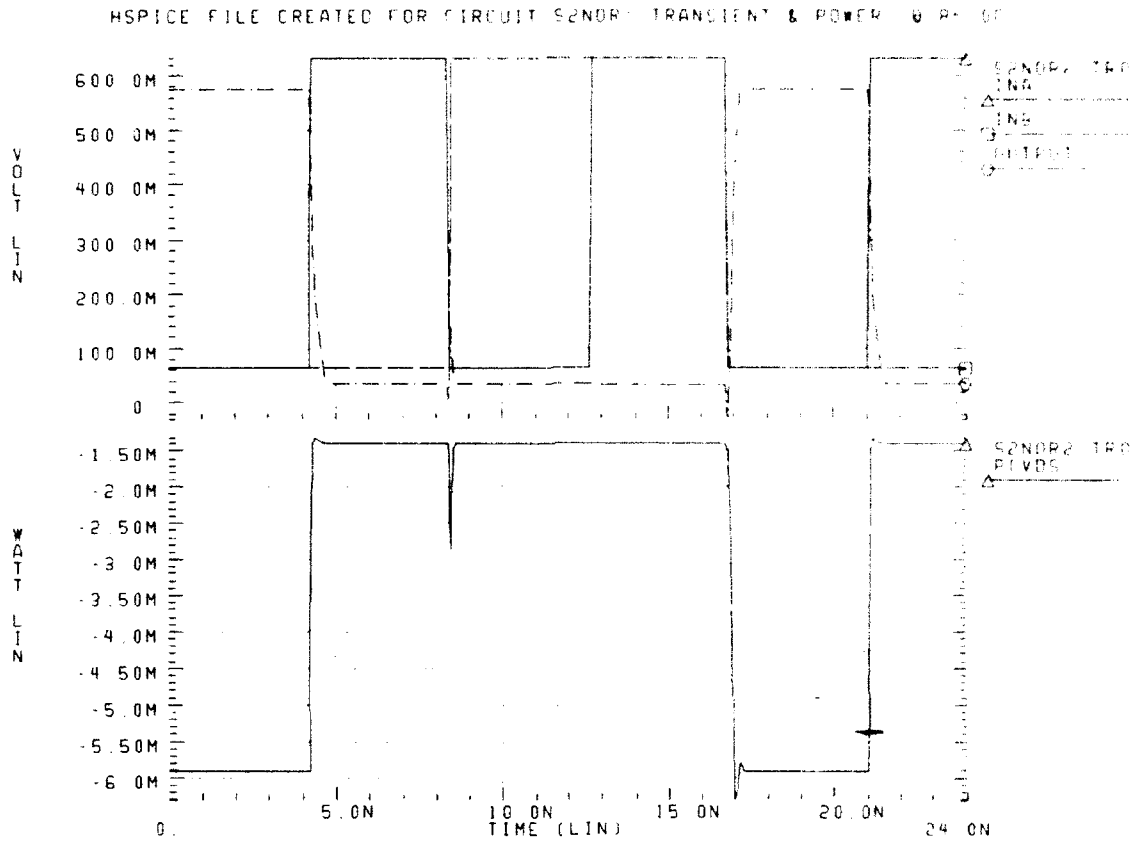


Figure 4.93 S2NOR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the S2NOR logic gate operating at a temperature of 25.0C is shown in Figure 4.94 on page 93.

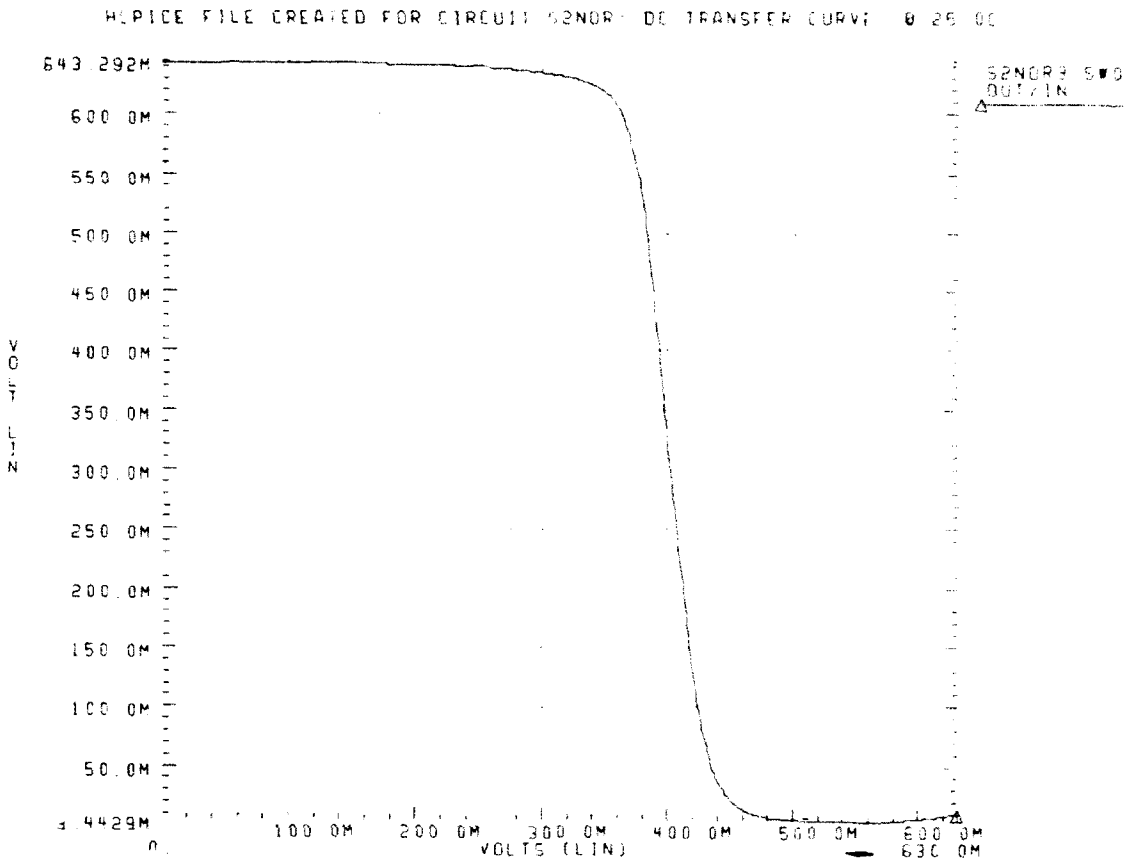


Figure 4.94 S2NOR DC Transfer Curve at 25.0C

The DC transfer characteristic of the S2NOR logic gate operating at a temperature of 85.0C is shown in Figure 4.95 on page 94.

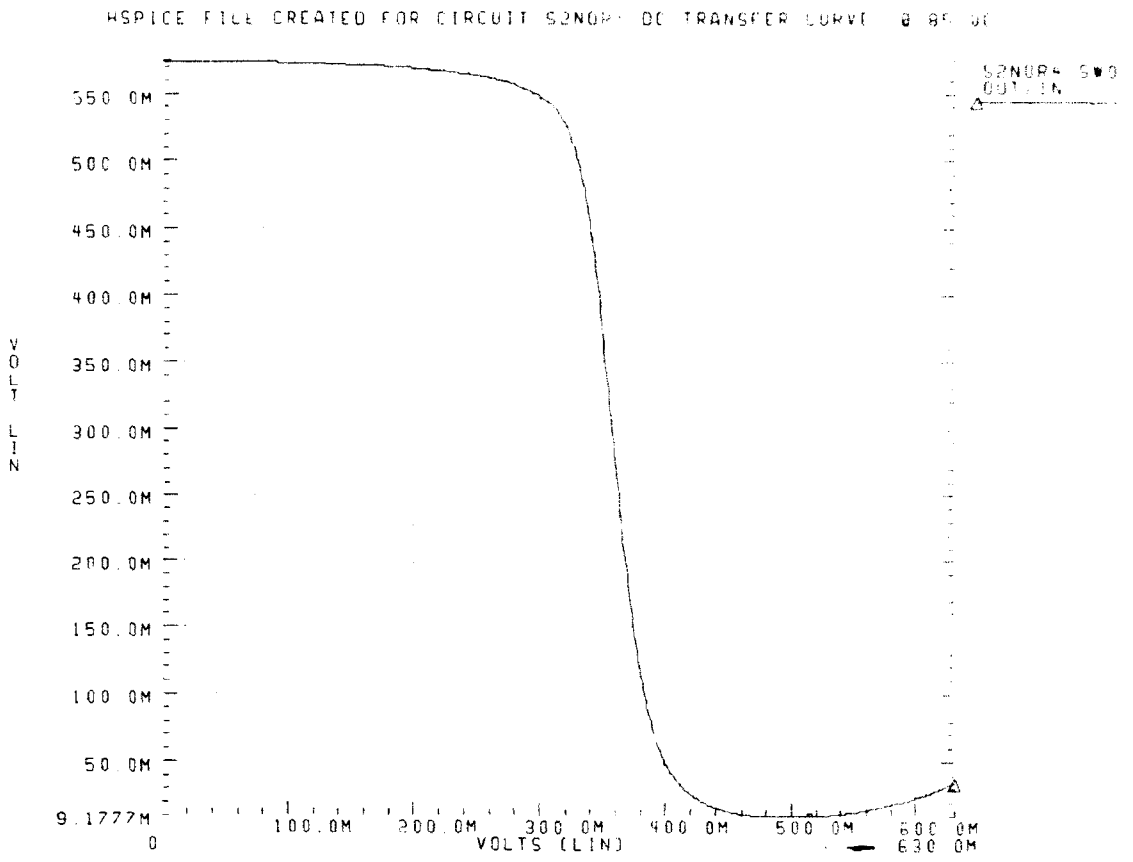


Figure 4.95 S2NOR DC Transfer Curve at 85.0C

4. SBFL 3-input NOR Gate (S3NOR)

The following graphs represent the operating characteristics of the S3NOR. See Figure 4.96 on page 95 for the S3NOR schematic and logical equivalence.

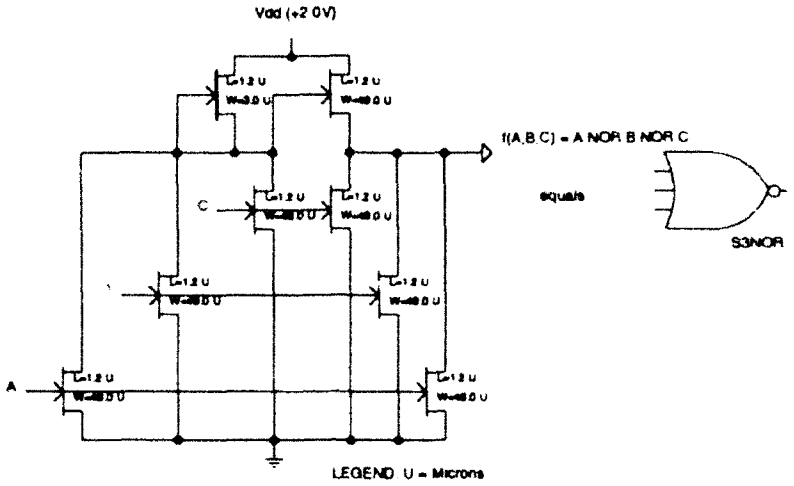


Figure 4.96 Schematic and Logical Equivalence for S3NOR

The transient analysis and power dissipation of the S3NOR operating at a temperature of 25.0C is shown in Figure 4.97 on page 96.

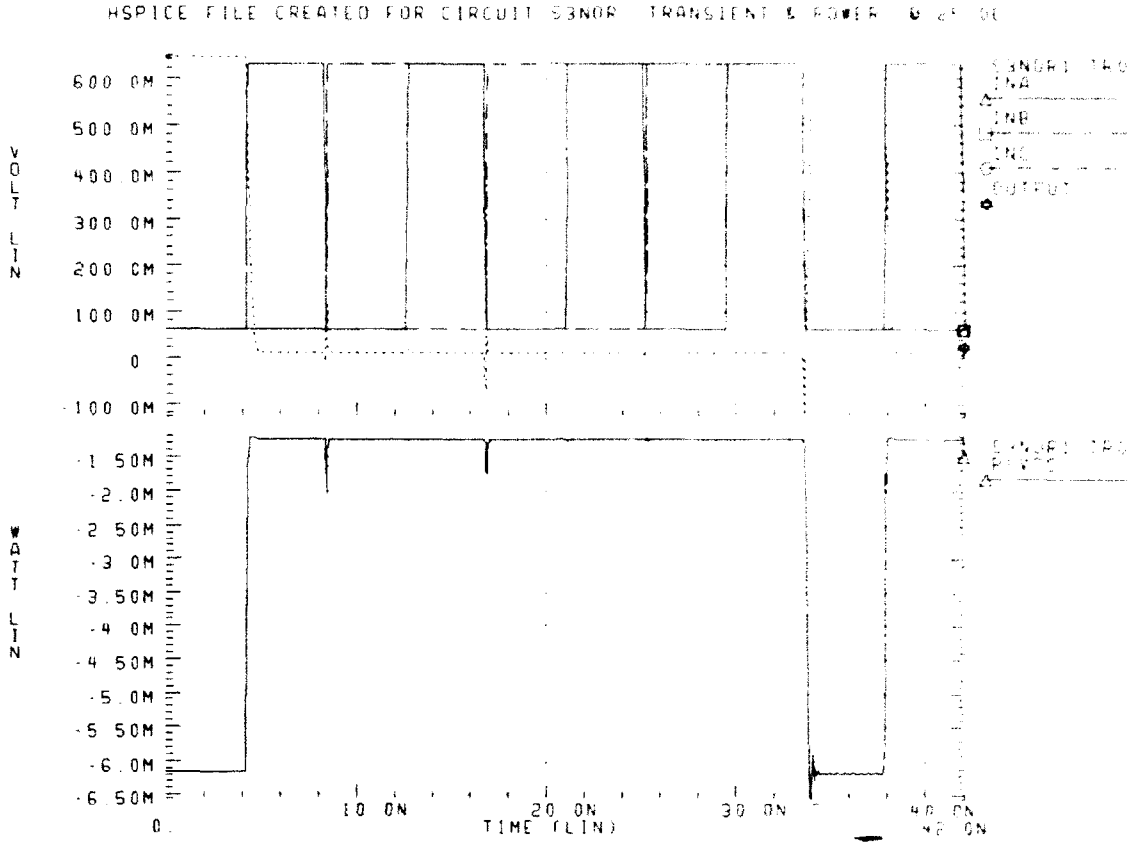


Figure 4.97 S3NOR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the S3NOR operating at a temperature of 85.0C is shown in Figure 4.98 on page 97.

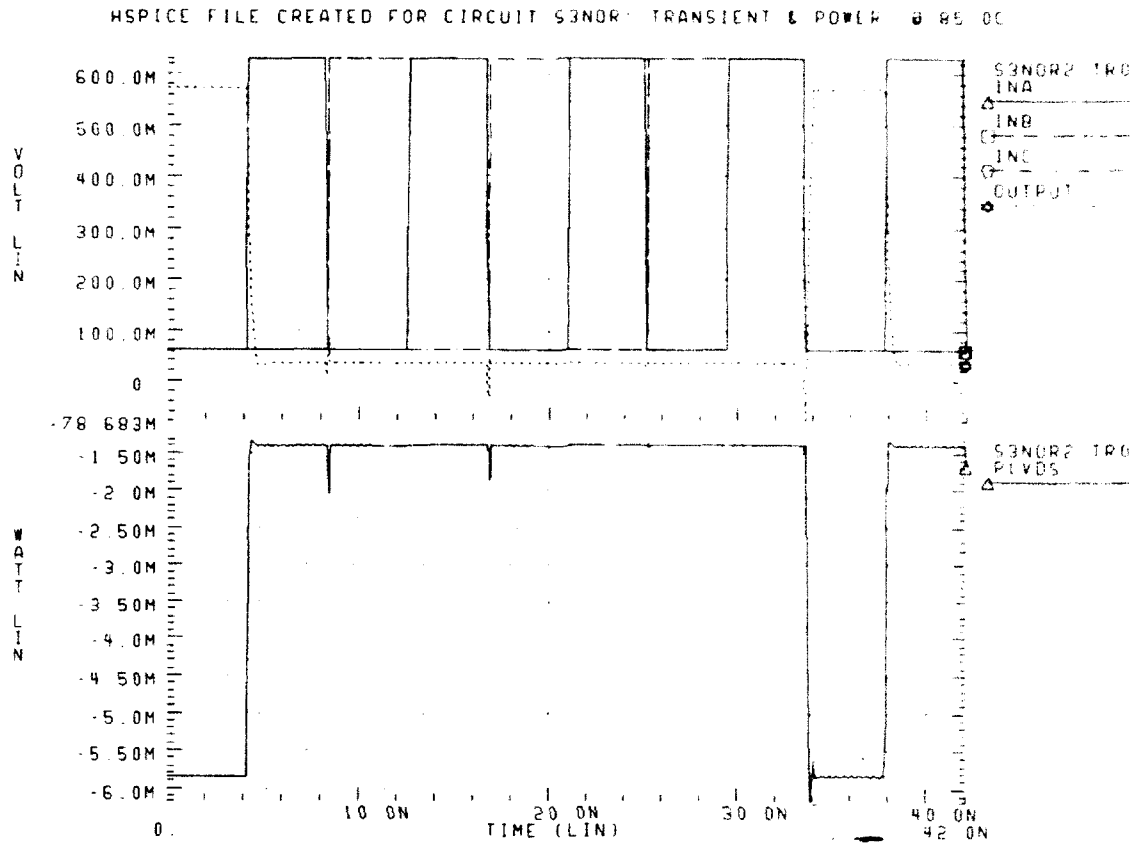


Figure 4.98 S3NOR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the S3NOR logic gate operating at a temperature of 25.0C is shown in Figure 4.99 on page 98.

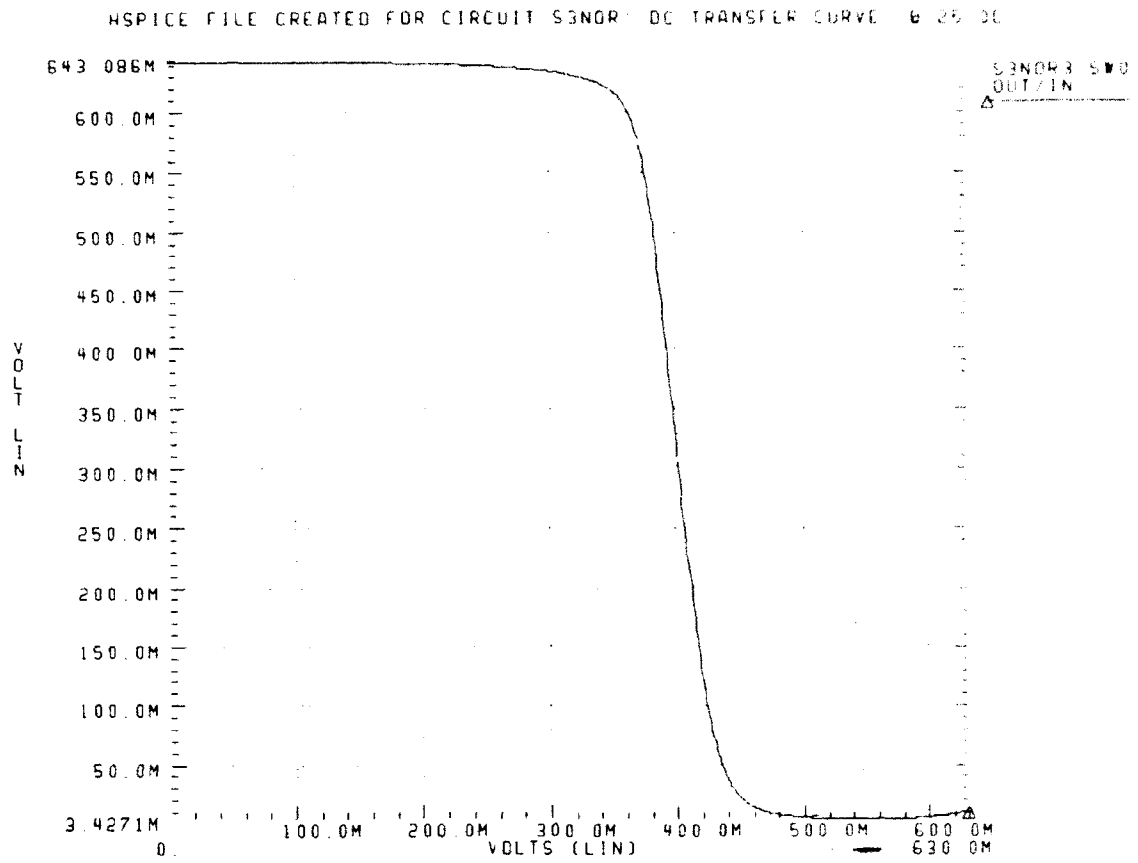


Figure 4.99 S3NOR DC Transfer Curve at 25.0C

The DC transfer characteristic of the S3NOR logic gate operating at a temperature of 85.0C is shown in Figure 4.100 on page 99.

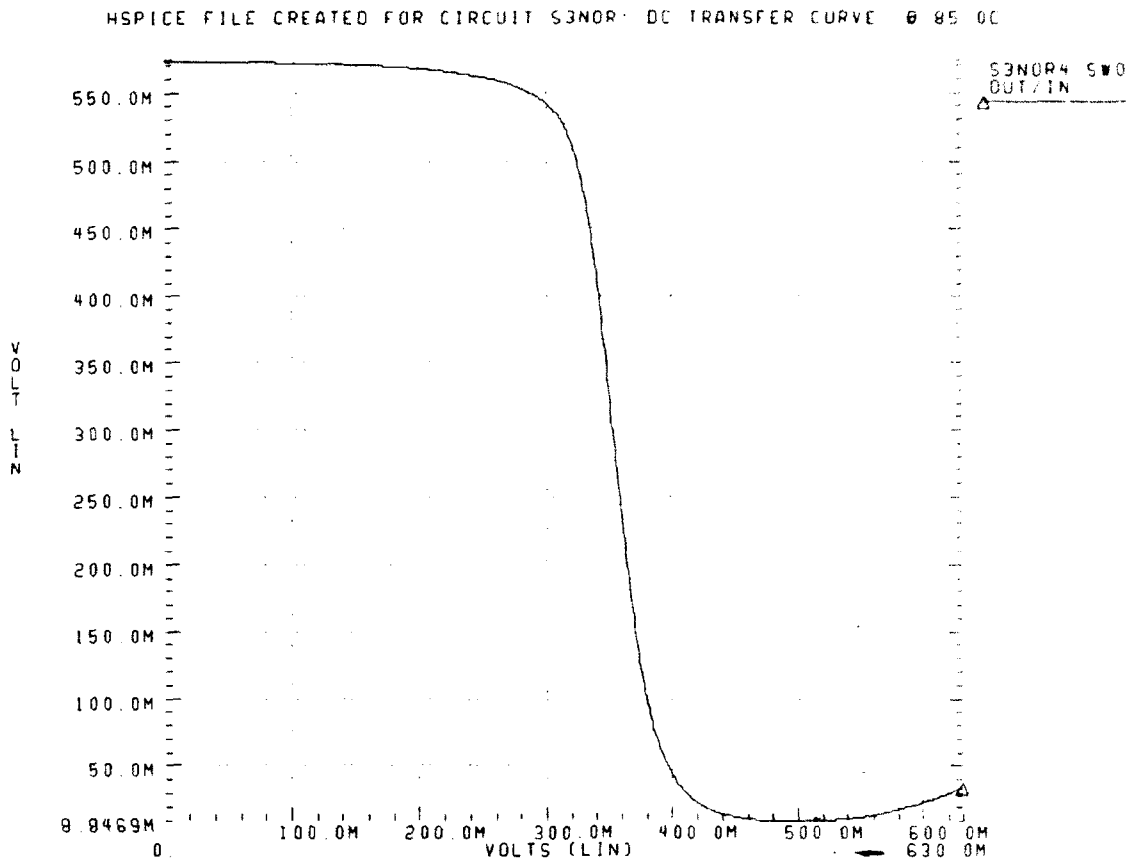


Figure 4.100 S3NOR DC Transfer Curve at 85.0C

5. SBFL 4-input NOR Gate (S4NOR)

The following graphs represent the operating characteristics of the S4NOR. As previously mentioned, true NAND gates were infrequently used, the more common SBFL ANDs, NANDs, and ORs were built using NORs with SINVs as per DeMorgan's theorems. See Figure 4.101 on page 100 for the S4NOR schematic and logical equivalence.

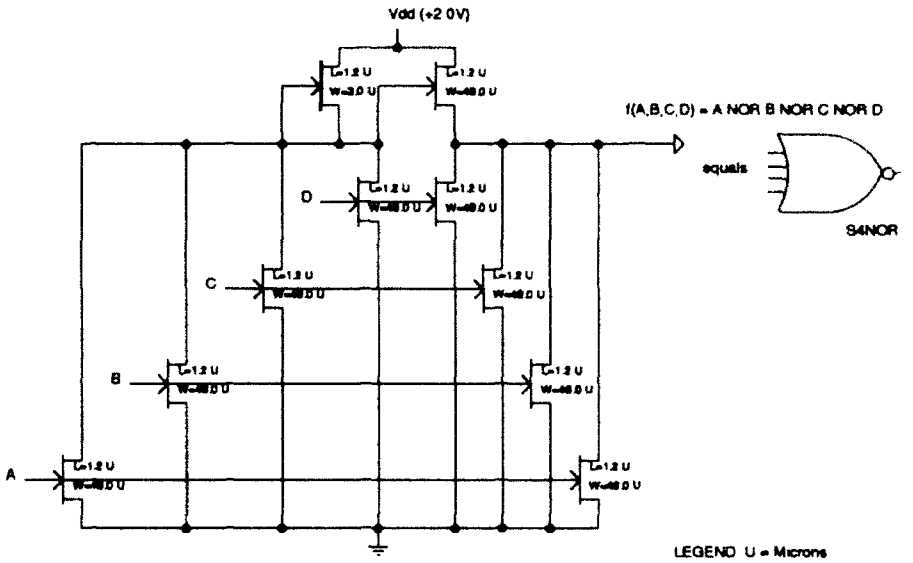


Figure 4.101 Schematic and Logical Equivalence for S4NOR

The transient analysis and power dissipation of the S4NOR operating at a temperature of 25.0C is shown in Figure 4.102 on page 101.

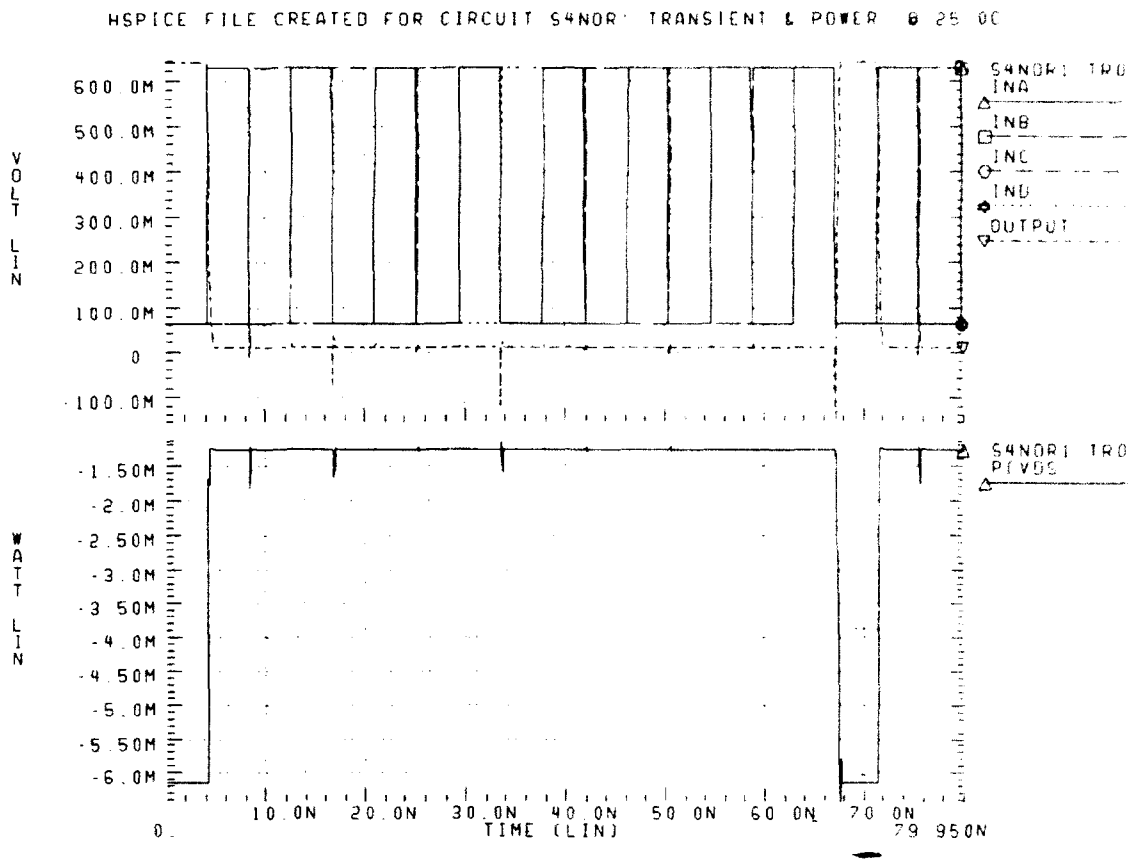


Figure 4.102 S4NOR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the S4NOR operating at a temperature of 85.0C is shown in Figure 4.103 on page 102.

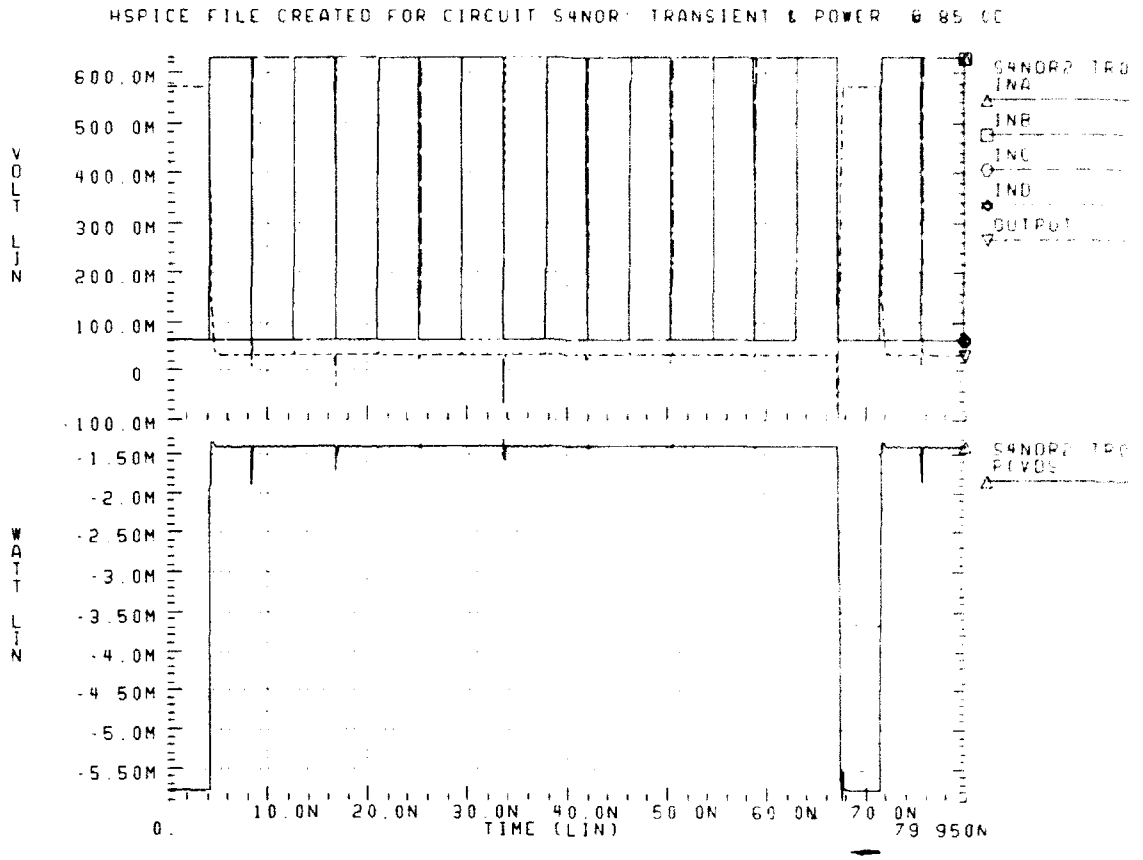


Figure 4.103 S4NOR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the S4NOR logic gate operating at a temperature of 25.0C is shown in Figure 4.104 on page 103.

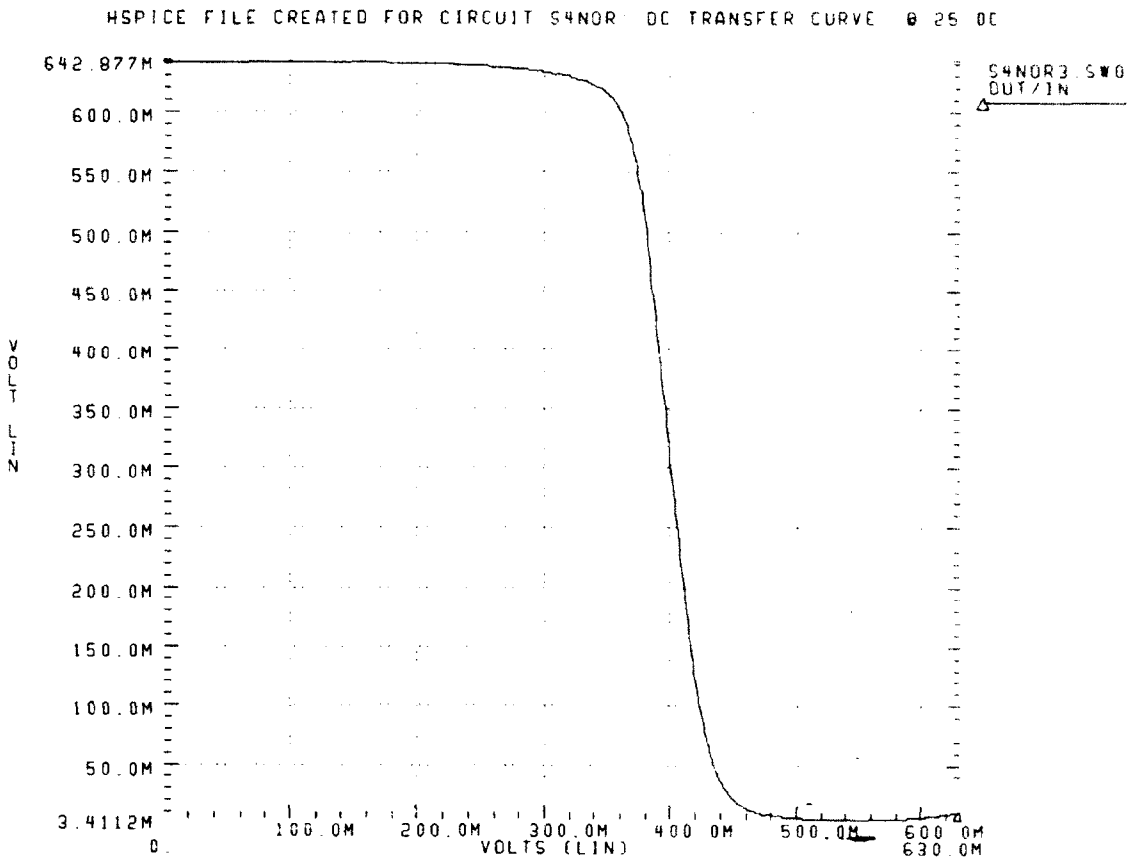


Figure 4.104 S4NOR DC Transfer Curve at 25.0C

The DC transfer characteristic of the S4NOR logic gate operating at a temperature of 85.0C is shown in Figure 4.105 on page 104.

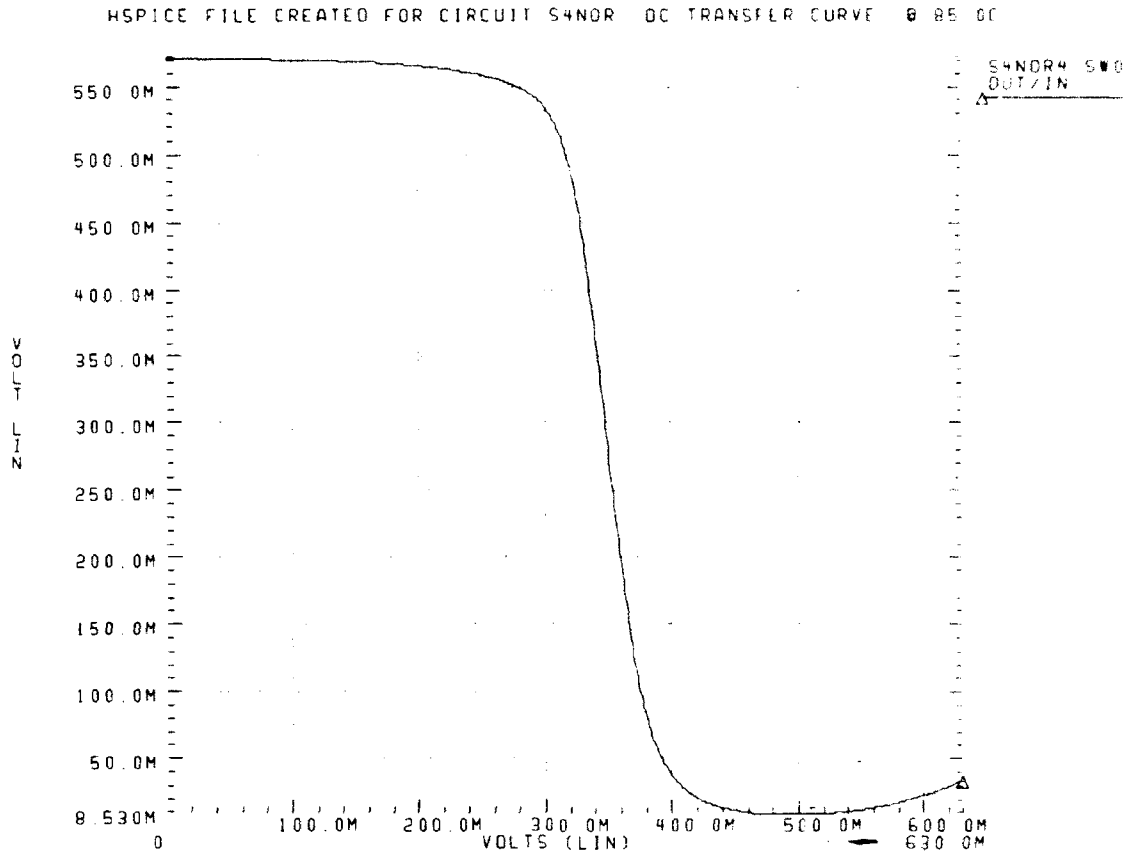


Figure 4.105 S4NOR DC Transfer Curve at 85.0C

6. *SBFL 3-input OR Gate (S3OR)*

The following graphs represent the operating characteristics of the S3OR. As previously mentioned, true NAND gates were infrequently used, the more common SBFL ANDs, NANDs, and ORs were built using NORs with SINVs as per DeMorgan's theorems. See Figure 4.106 on page 104 for the S3OR schematic and logical equivalence.

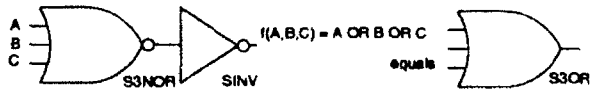


Figure 4.106 Schematic and Logical Equivalence for S3OR

The transient analysis and power dissipation of the S3OR operating at a temperature of 25.0C is shown in Figure 4.107 on page 105.

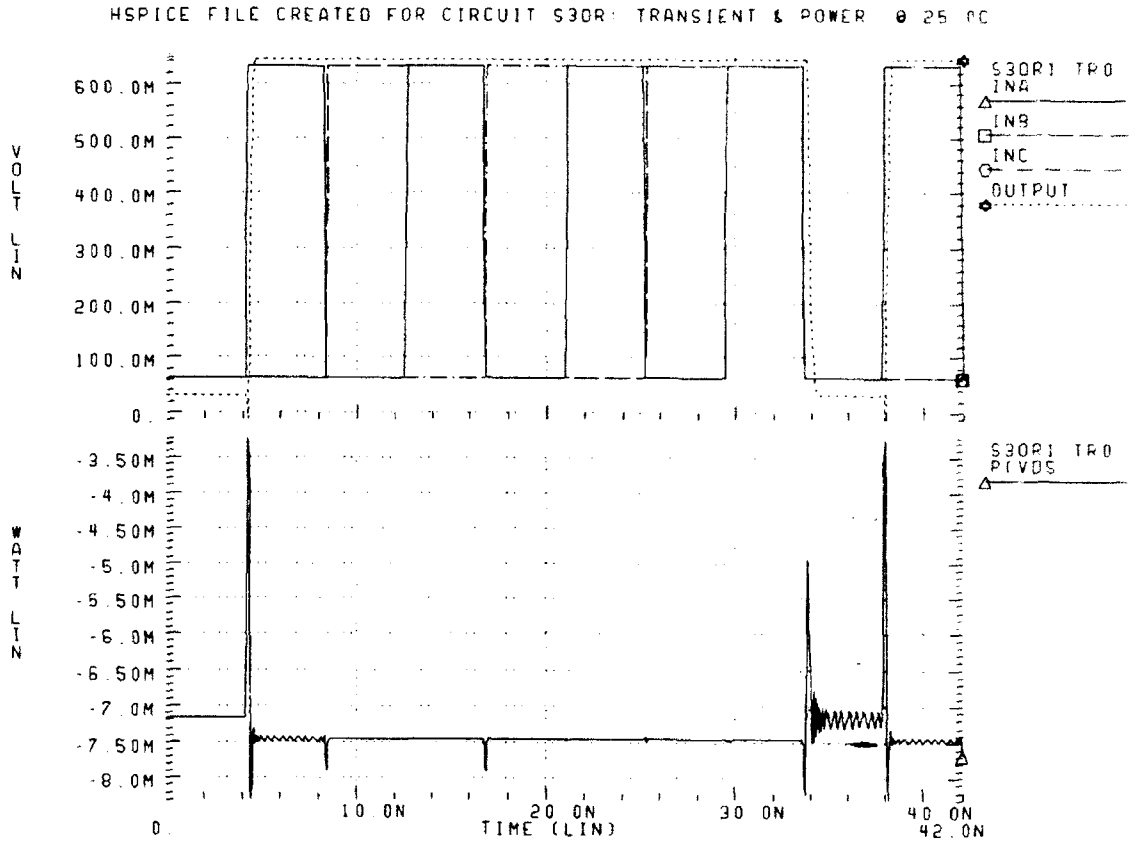


Figure 4.107 S3OR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the S3OR operating at a temperature of 85.0C is shown in Figure 4.108 on page 106.

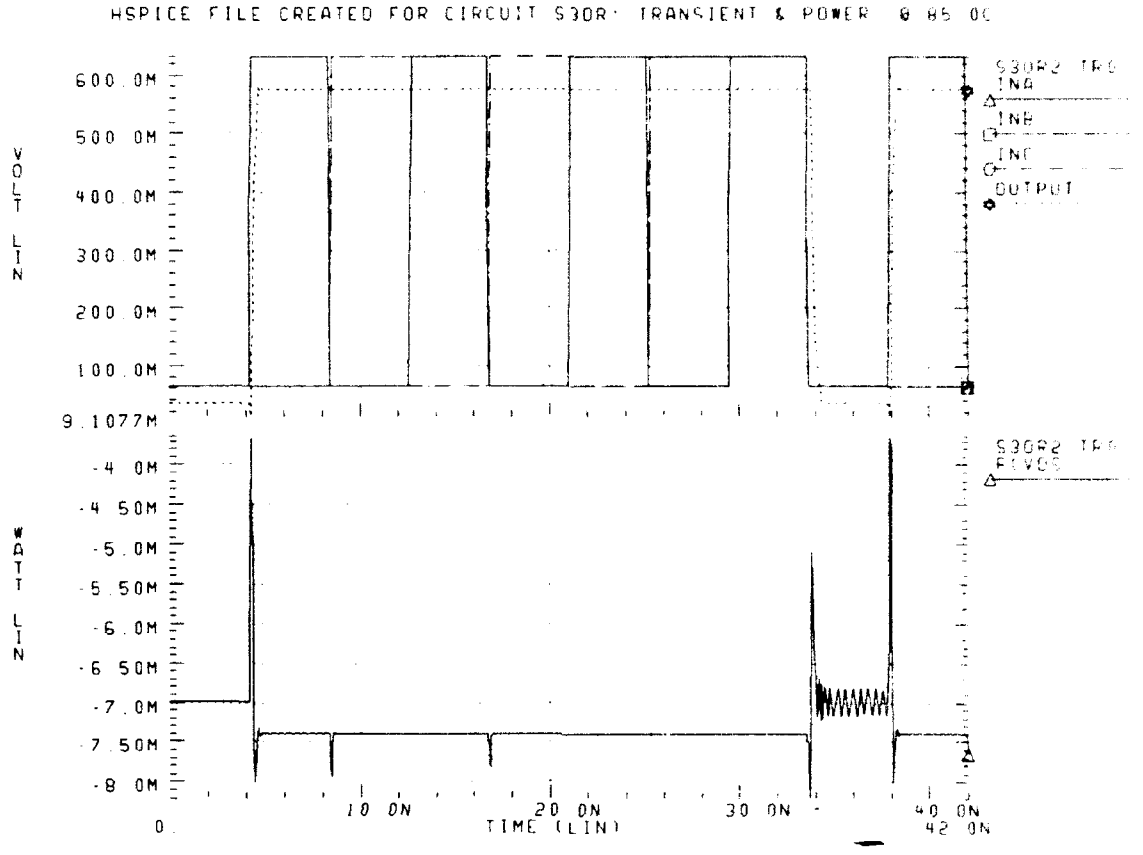


Figure 4.108 S3OR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the S3OR logic gate operating at a temperature of 25.0C is shown in Figure 4.109 on page 107.

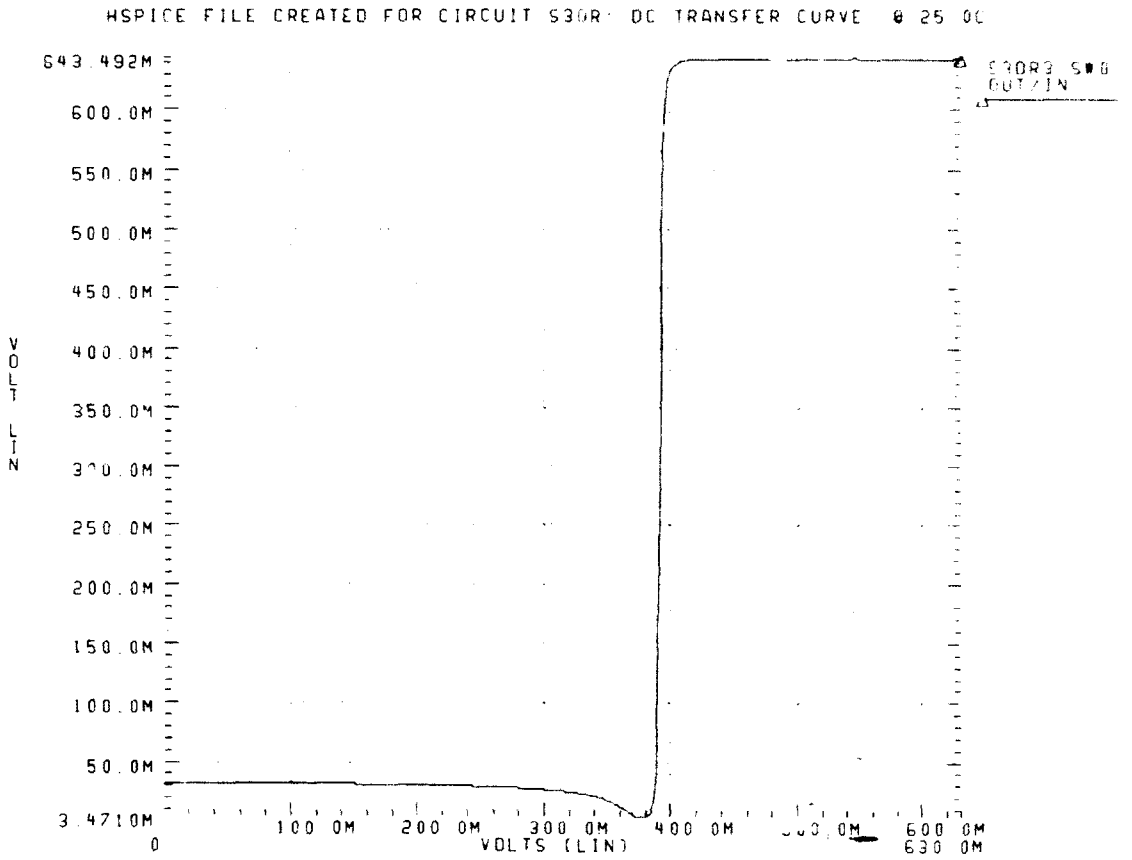


Figure 4.109 S3OR DC Transfer Curve at 25.0C

The DC transfer characteristic of the S3OR logic gate operating at a temperature of 85.0C is shown in Figure 4.110 on page 108.

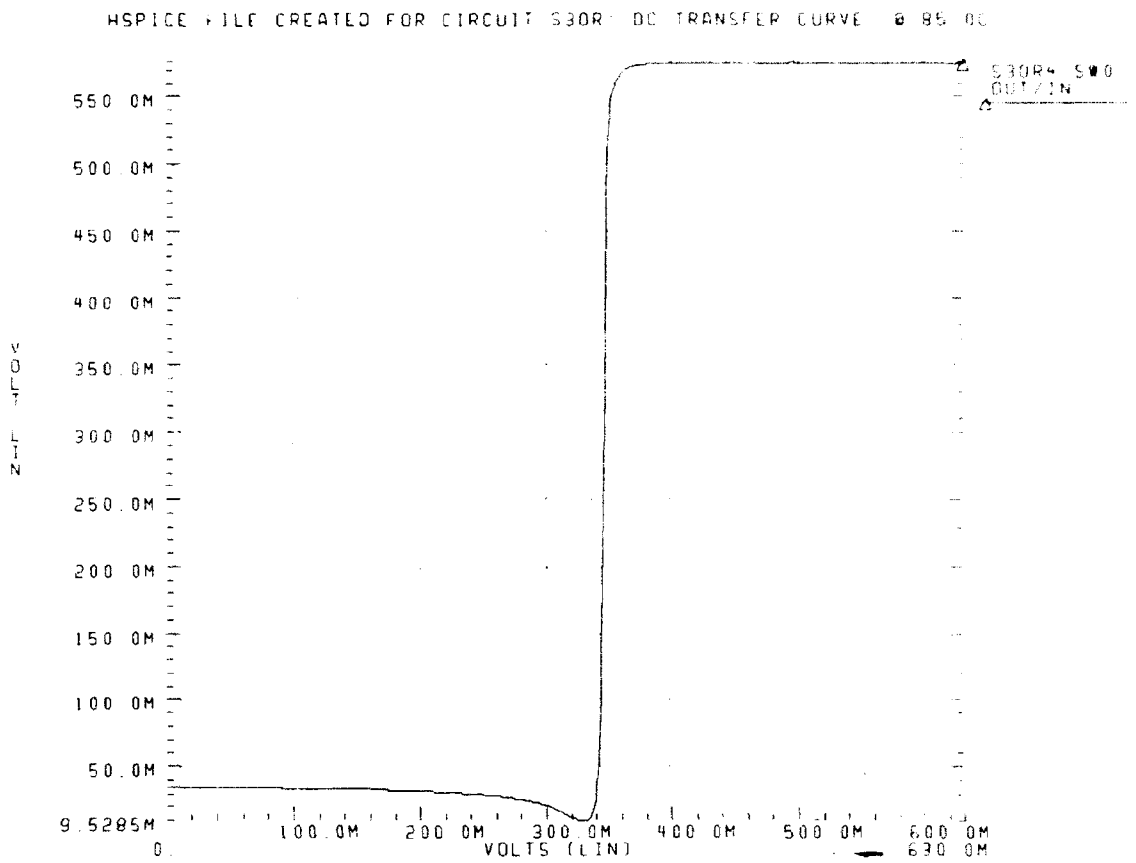


Figure 4.110 S3OR DC Transfer Curve at 85.0C

7. SBFL 2-input NAND Gate (SS2NAND)

The following graphs represent the operating characteristics of the SS2NAND. See Figure 4.111 on page 108 for the SS2NAND schematic and logical equivalence.

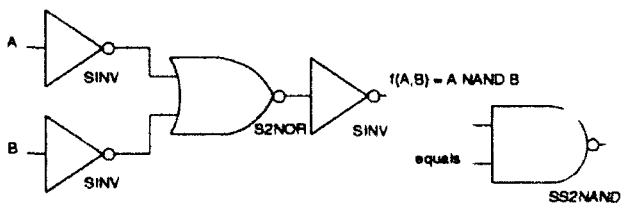


Figure 4.111 Schematic and Logical Equivalence for SS2NAND

The transient analysis and power dissipation of the SS2NAND operating at a temperature of 25.0C is shown in Figure 4.112 on page 109.

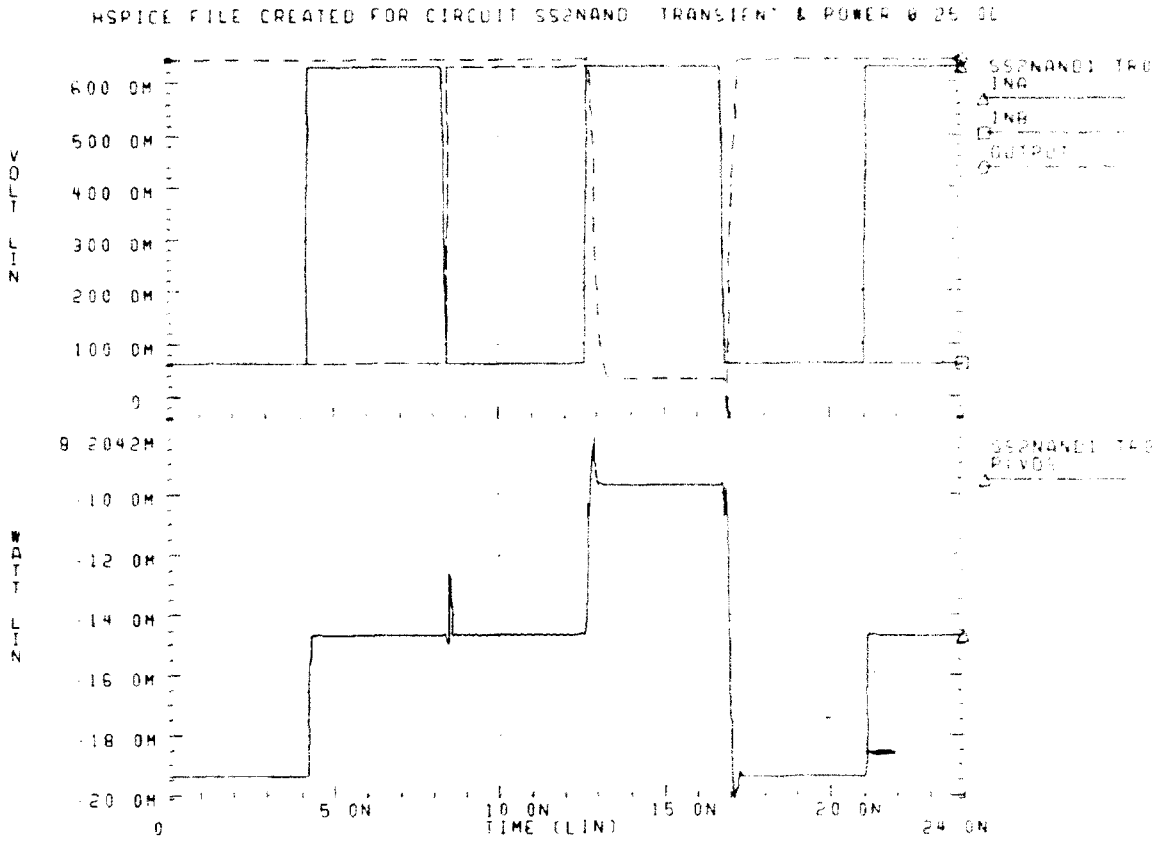


Figure 4.112 SS2NAND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the SS2NAND operating at a temperature of 85.0C is shown in Figure 4.113 on page 110.

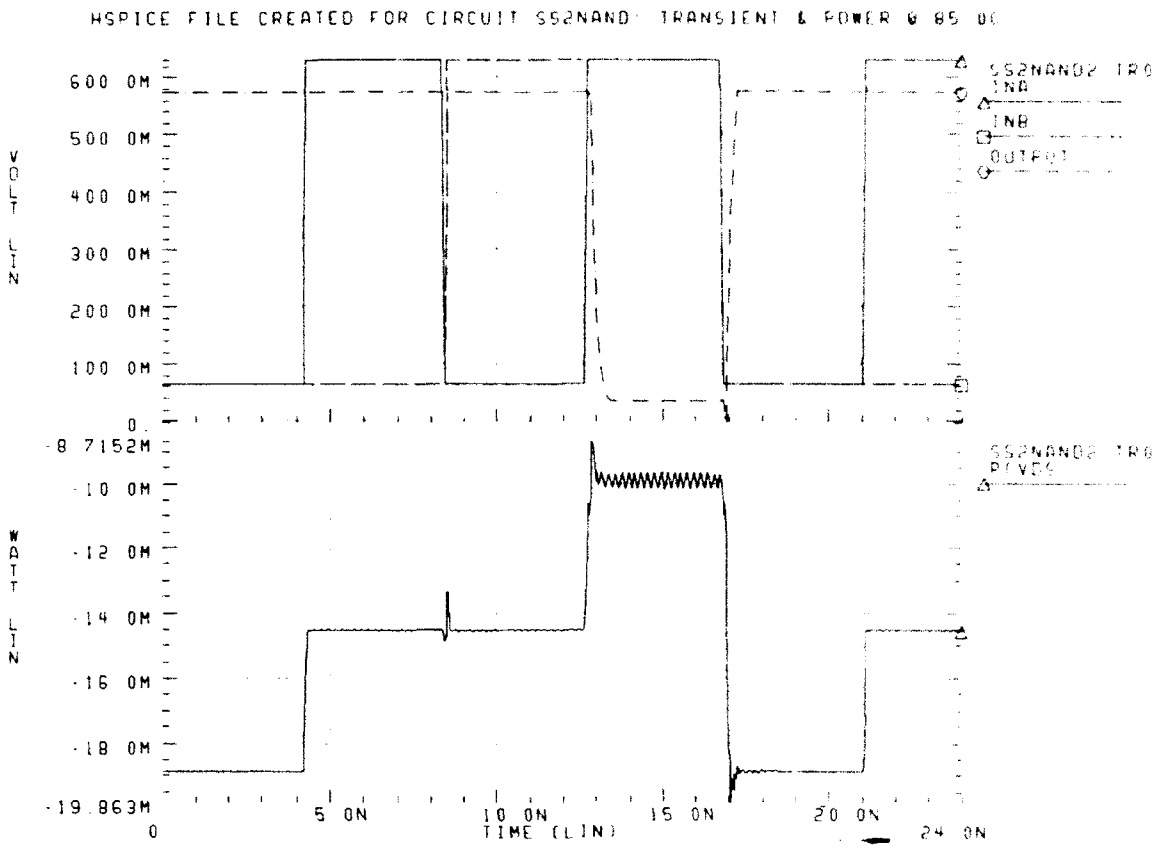


Figure 4.113 SS2NAND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the SS2NAND logic gate operating at a temperature of 25.0C is shown in Figure 4.114 on page 111.

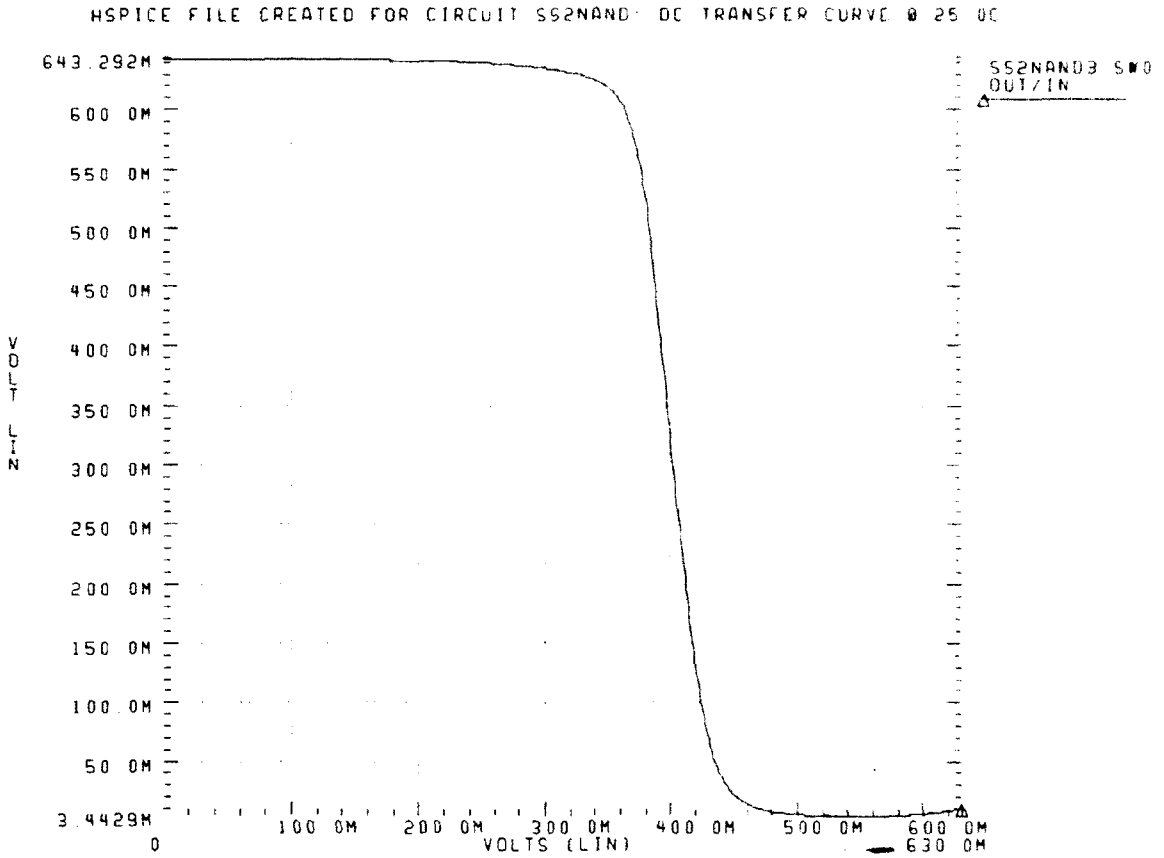


Figure 4.114 SS2NAND DC Transfer Curve at 25.0C

The DC transfer characteristic of the SS2NAND logic gate operating at a temperature of 85.0C is shown in Figure 4.115 on page 112.

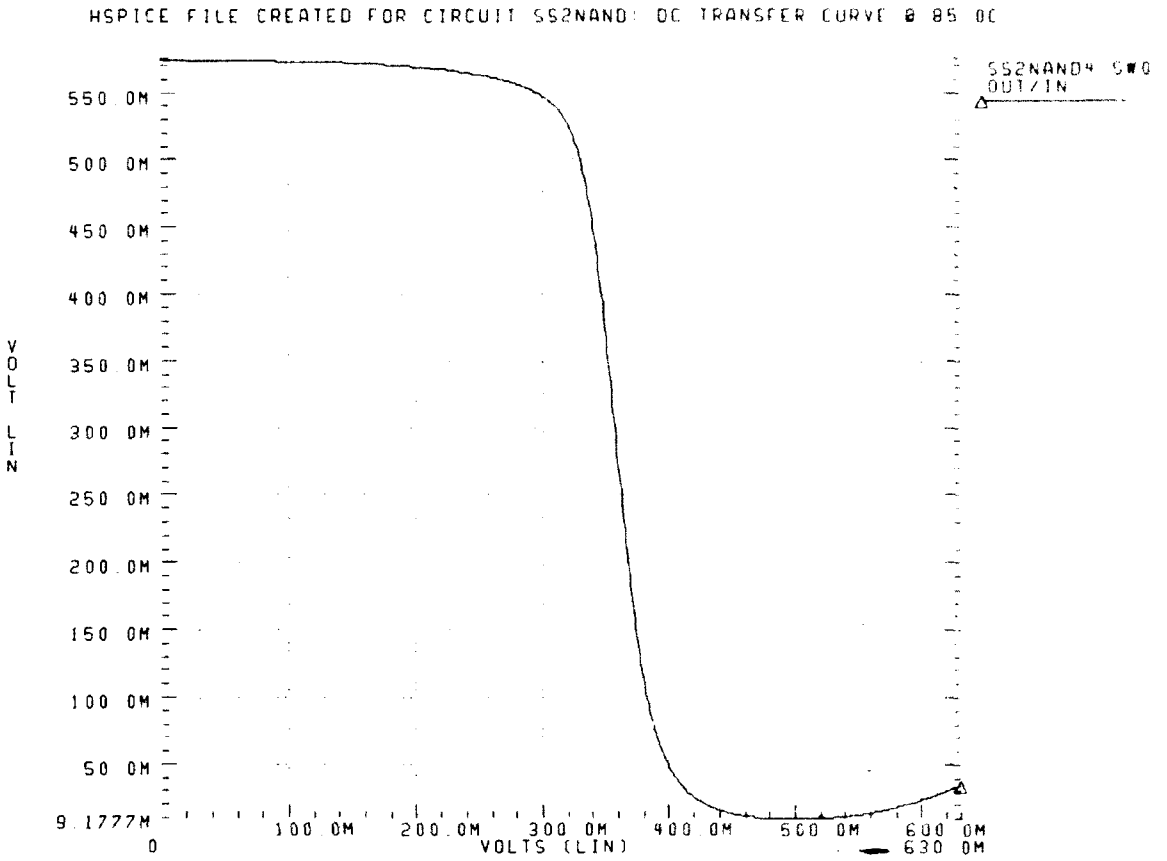


Figure 4.115 SS2NAND DC Transfer Curve at 85.0C

8. SBFL 4-input NAND Gate (SS4NAND)

The following graphs represent the operating characteristics of the SS4NAND. See Figure 4.116 on page 113 for the SS4NAND schematic and logical equivalence.

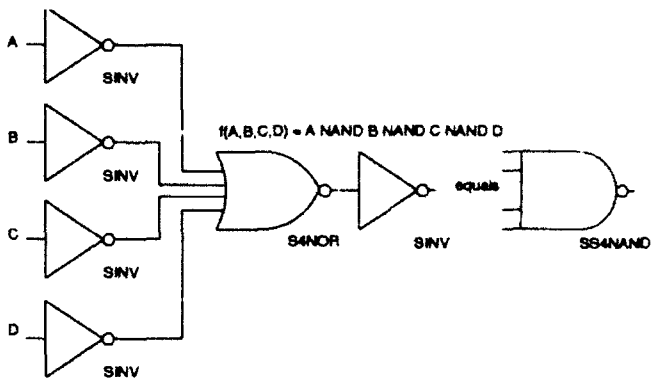


Figure 4.116 Schematic and Logical Equivalence for SS4NAND

The transient analysis and power dissipation of the SS4NAND operating at a temperature of 25.0C is shown in Figure 4.117 on page 113.

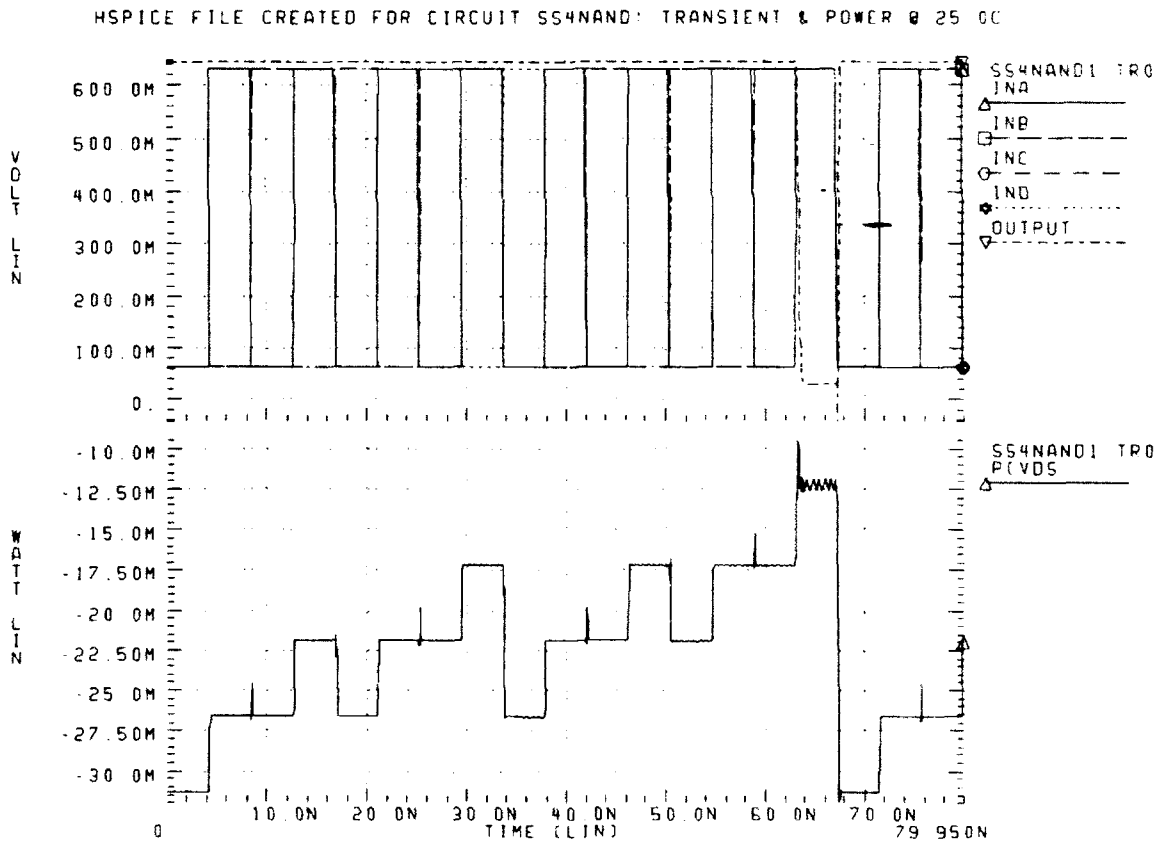


Figure 4.117 SS4NAND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the SS4NAND operating at a temperature of 85.0C is shown in Figure 4.118 on page 114.

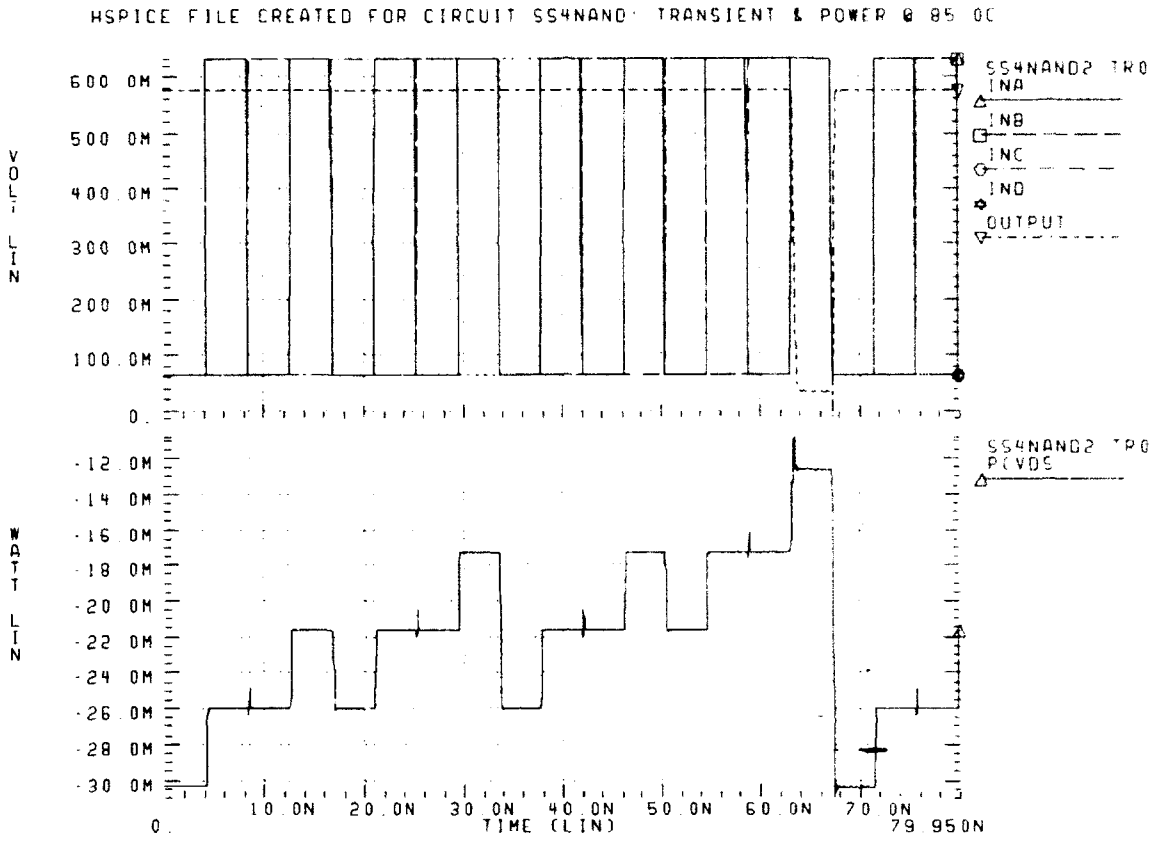


Figure 4.118 SS4NAND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the SS4NAND logic gate operating at a temperature of 25.0C is shown in Figure 4.119 on page 115.

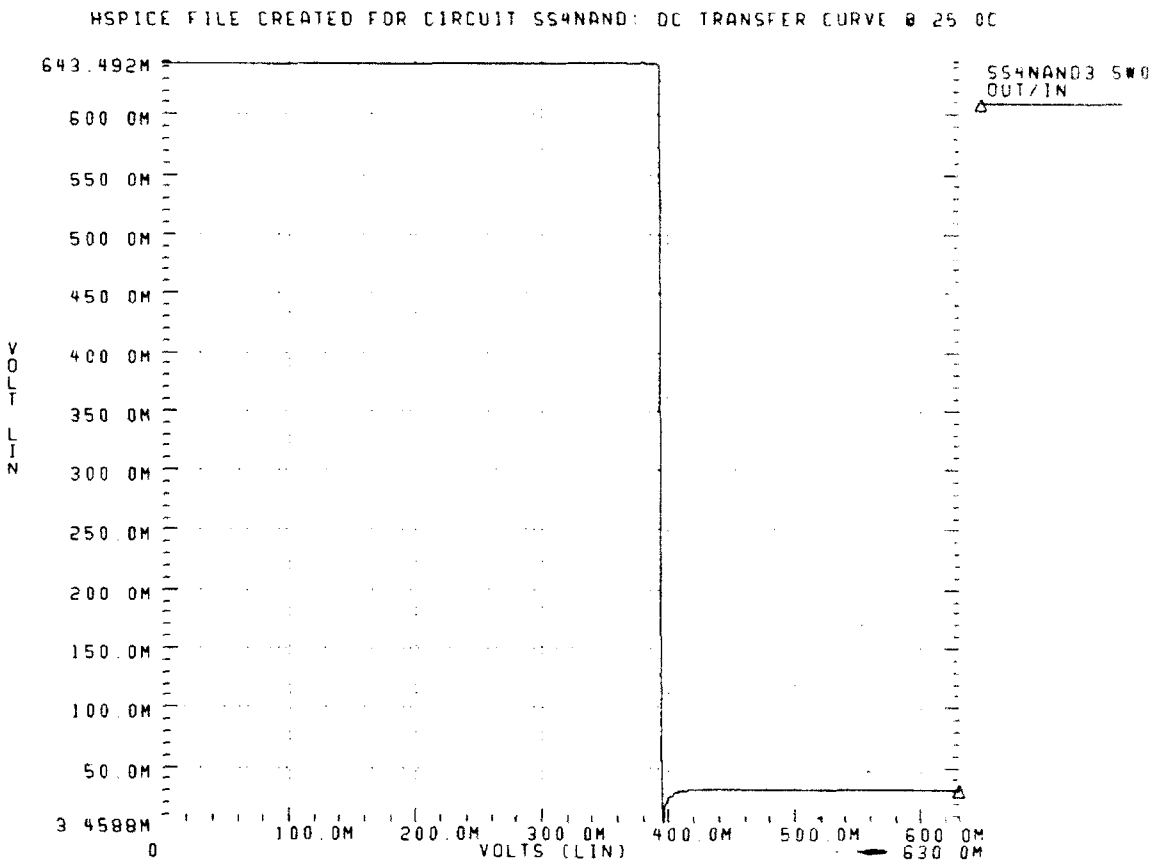


Figure 4.119 SS4NAND DC Transfer Curve at 25.0C

The DC transfer characteristic of the SS4NAND logic gate operating at a temperature of 85.0C is shown in Figure 4.120 on page 116.

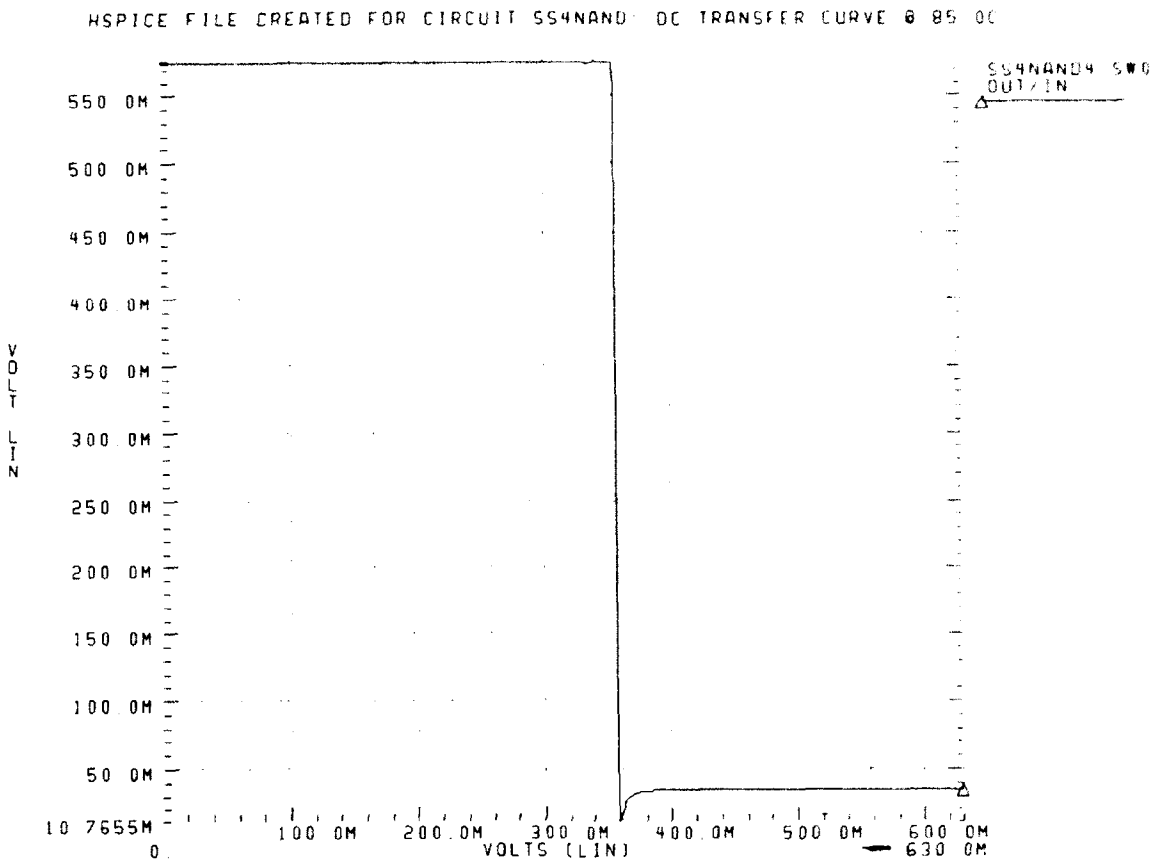


Figure 4.120 SS4NAND DC Transfer Curve at 85.0C

9. SBFL 3-input NAND Gate (SS3AND)

The following graphs represent the operating characteristics of the SS3AND. See Figure 4.121 on page 116 for the SS4NAND schematic and logical equivalence.

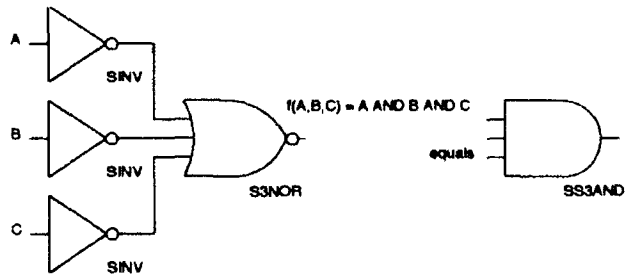


Figure 4.121 Schematic and Logical Equivalence for SS3AND

The transient analysis and power dissipation of the SS3AND operating at a temperature of 25.0C is shown in Figure 4.122 on page 117.

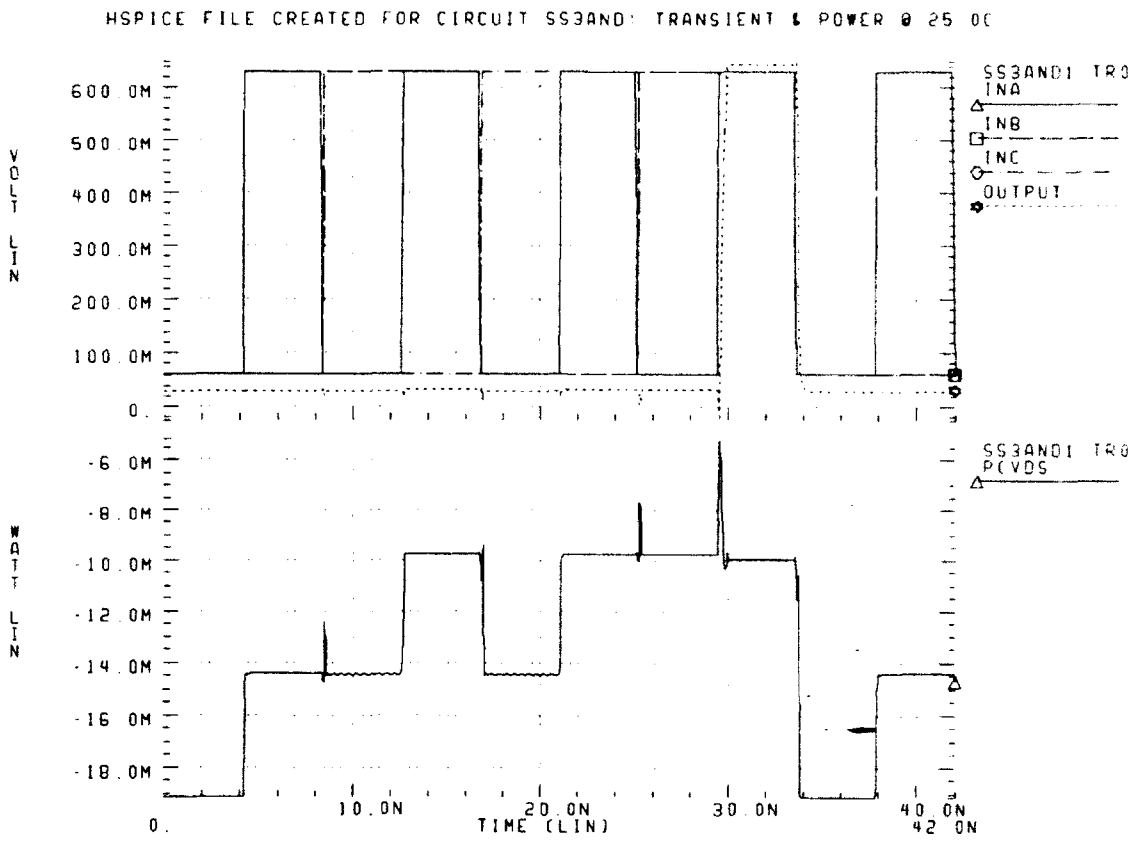


Figure 4.122 SS3AND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the SS3AND operating at a temperature of 85.0C is shown in Figure 4.123 on page 118.

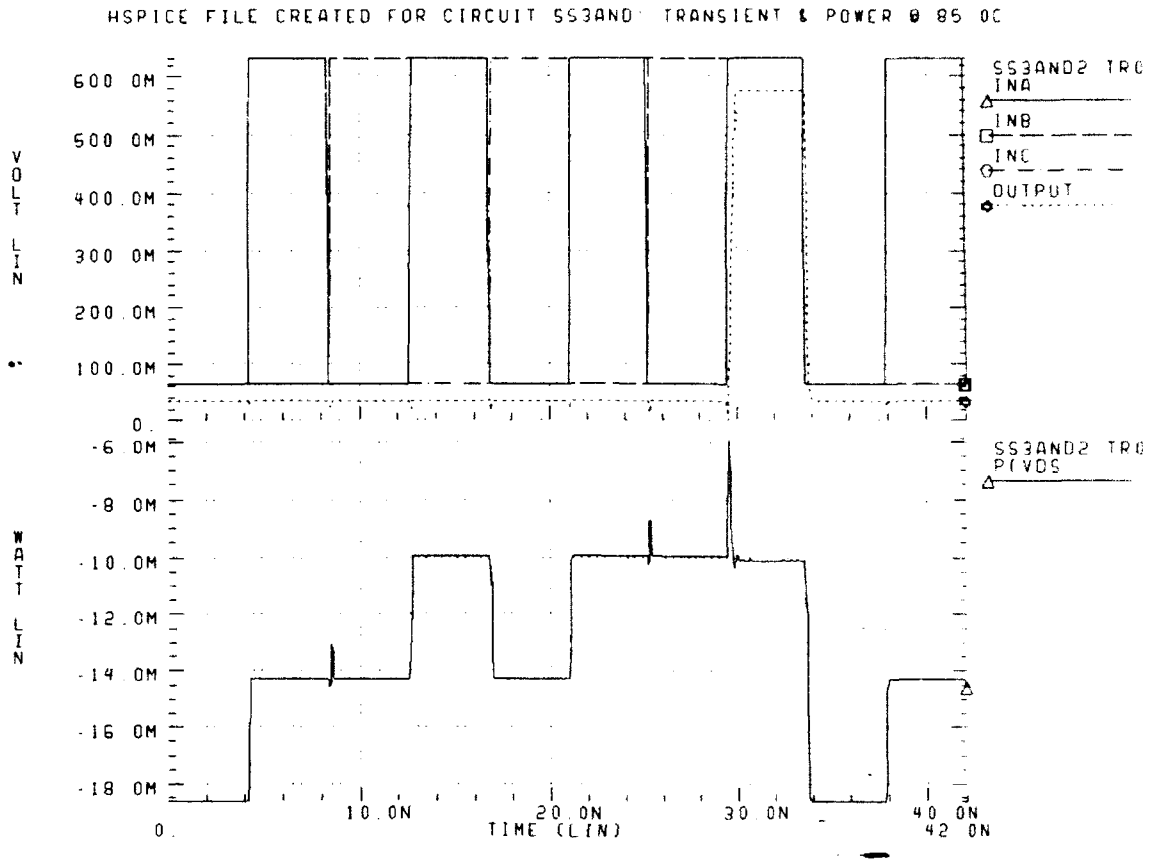


Figure 4.123 SS3AND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the SS3AND logic gate operating at a temperature of 25.0C is shown in Figure 4.124 on page 119.

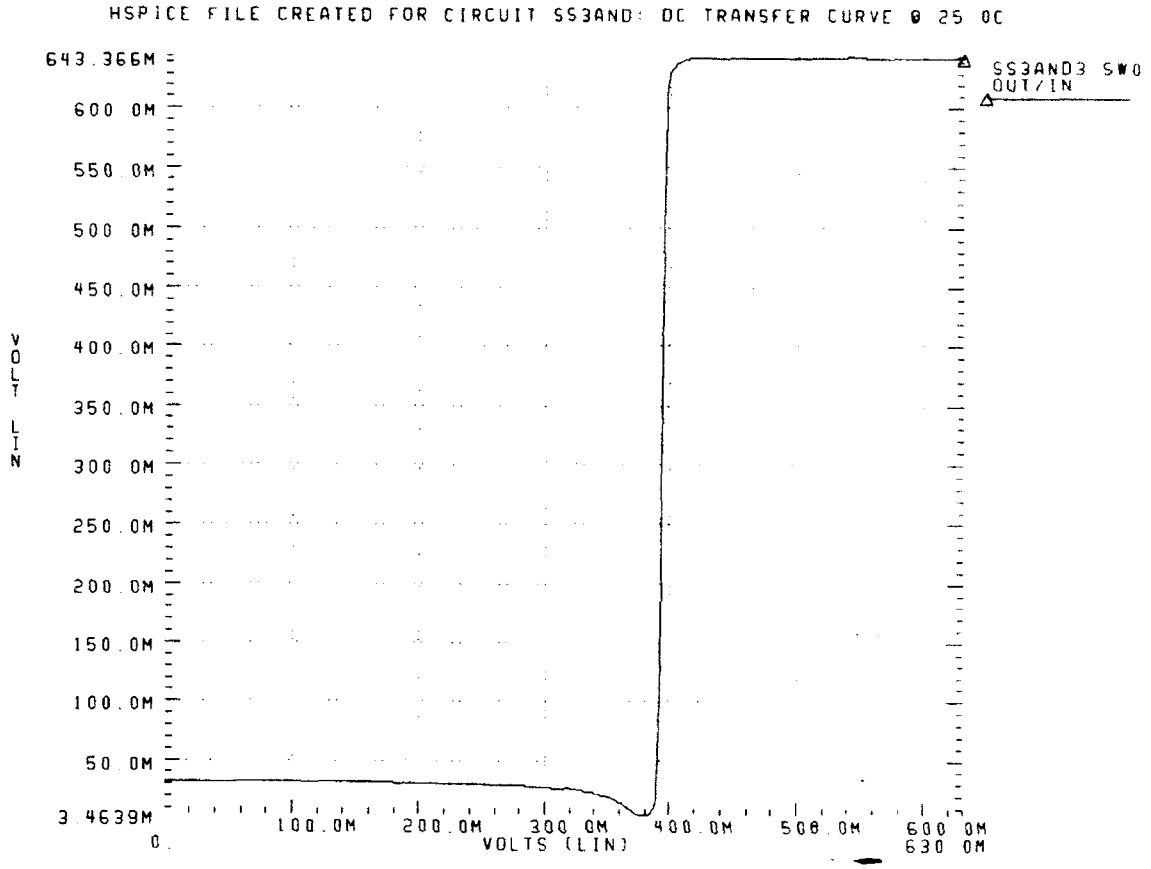


Figure 4.124 SS3AND DC Transfer Curve at 25.0C

The DC transfer characteristic of the SS3AND logic gate operating at a temperature of 85.0C is shown in Figure 4.125 on page 120.

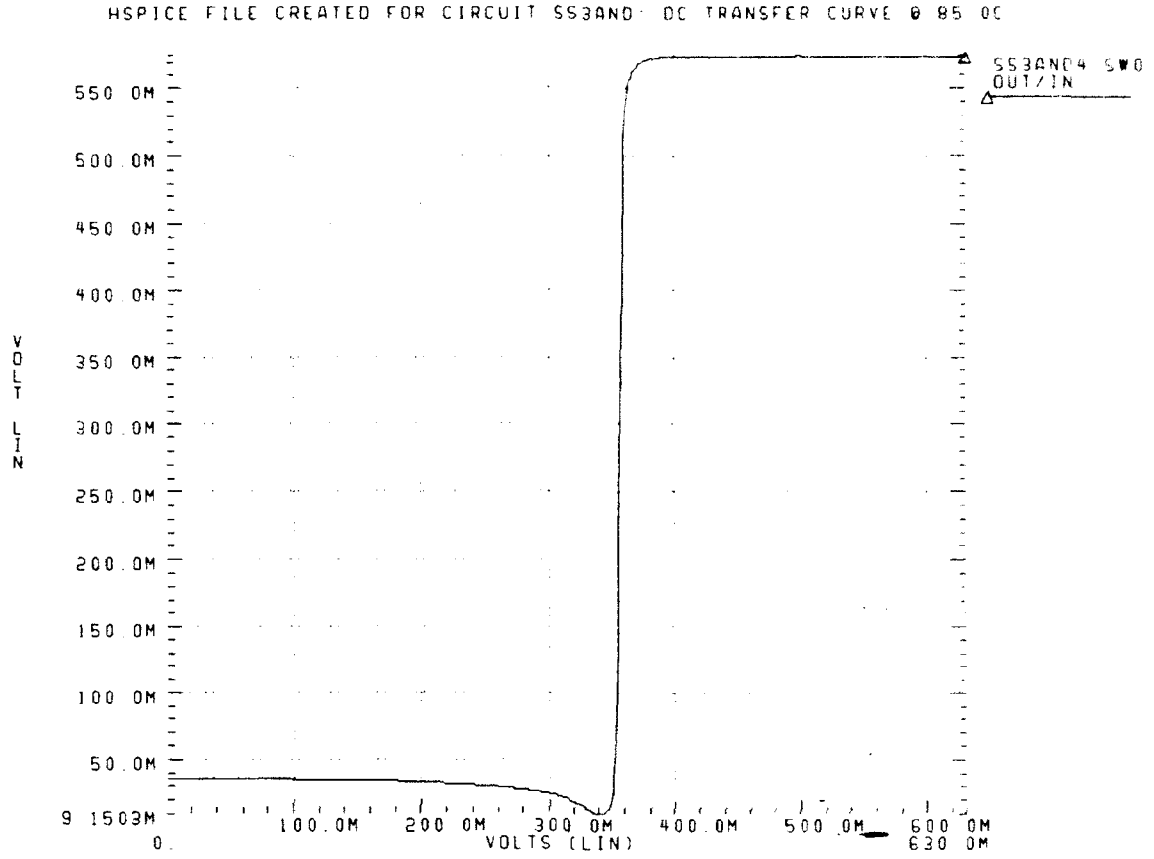


Figure 4.125 SS3AND DC Transfer Curve at 85.0C

10. SBFL 4-input NAND Gate (SS4AND)

The following graphs represent the operating characteristics of the SS4AND. See Figure 4.126 on page 121 for the SS4NAND schematic and logical equivalence.

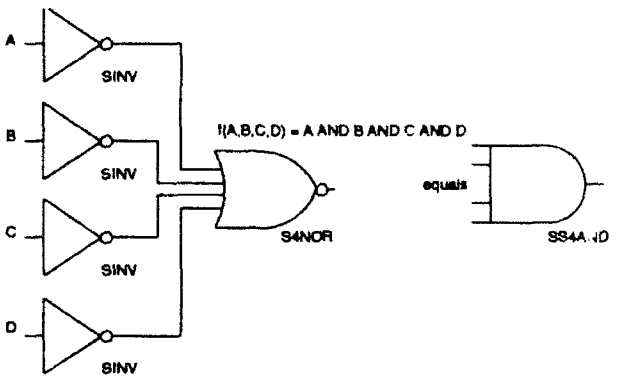


Figure 4.126 Schematic and Logical Equivalence for SS4AND

The transient analysis and power dissipation of the SS4AND operating at a temperature of 25.0C is shown in Figure 4.127 on page 121.

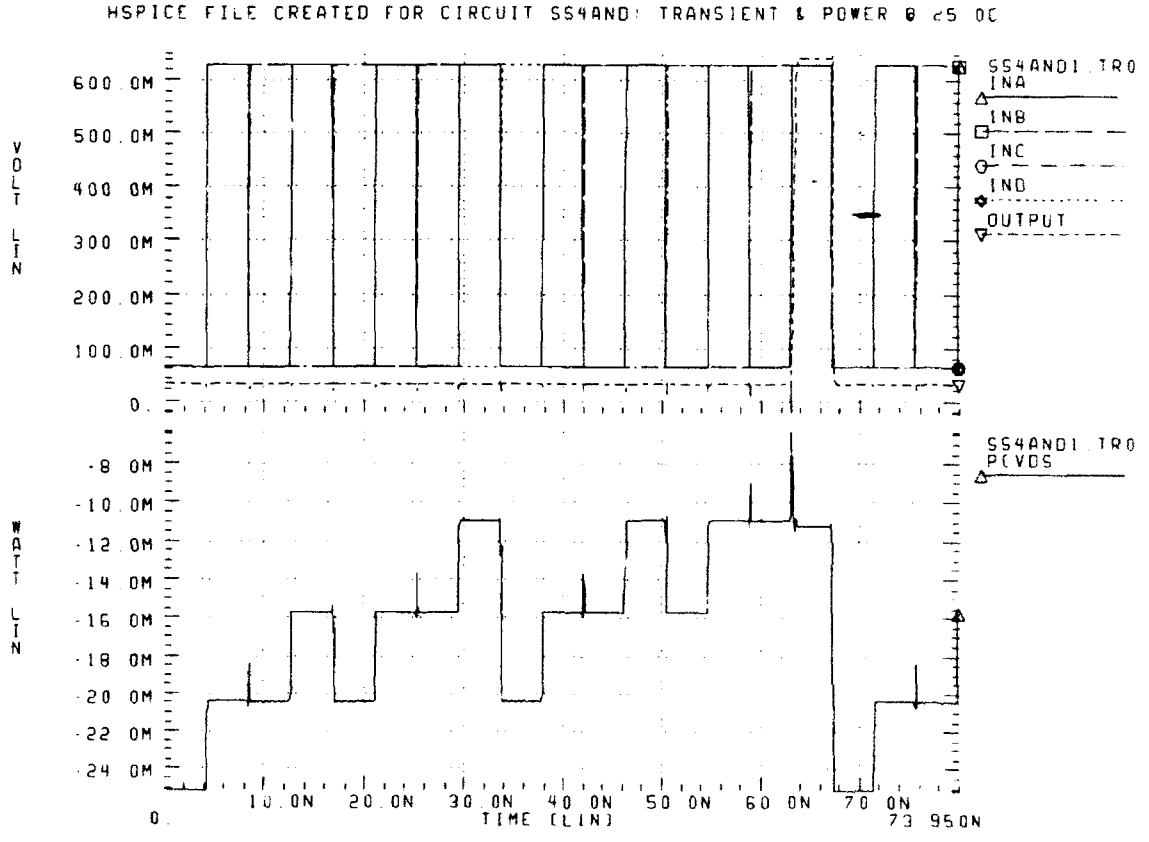


Figure 4.127 SS4AND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the SS4AND operating at a temperature of 85.0C is shown in Figure 4.128 on page 122.

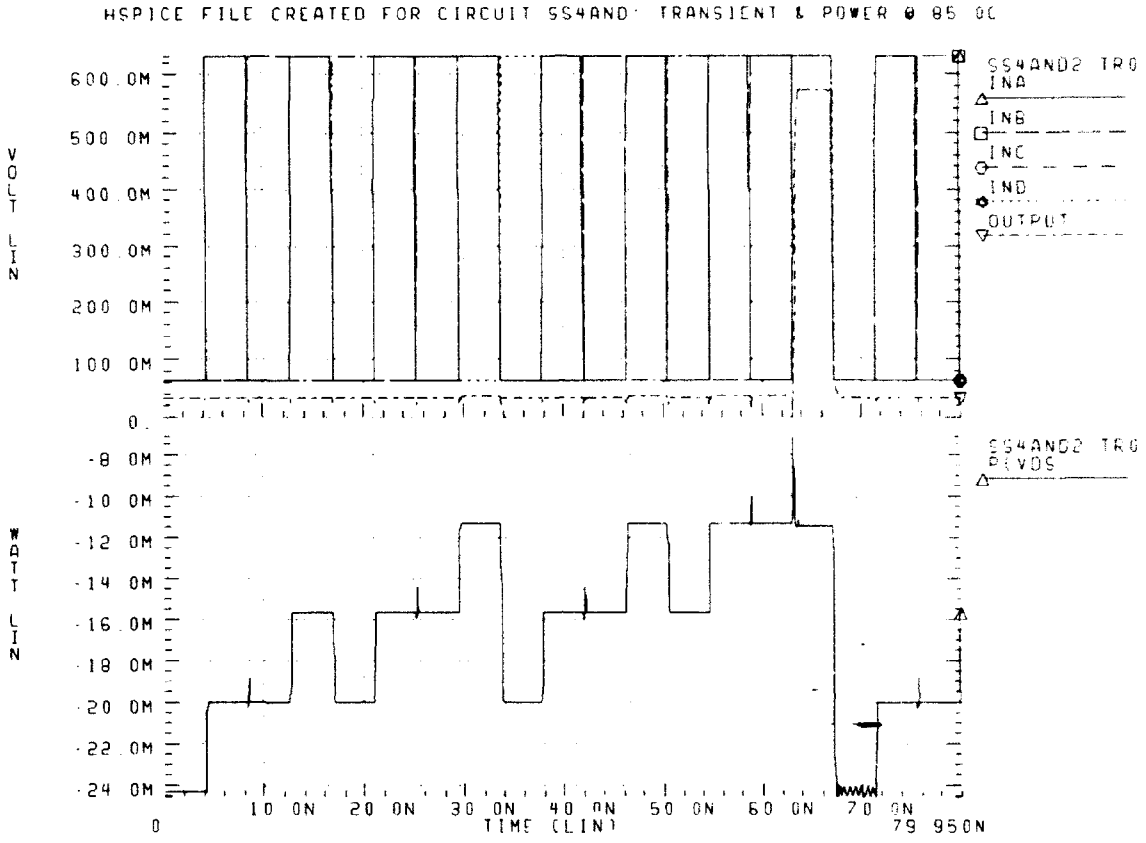


Figure 4.128 SS4AND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the SS4AND logic gate operating at a temperature of 25.0C is shown in Figure 4.129 on page 123.

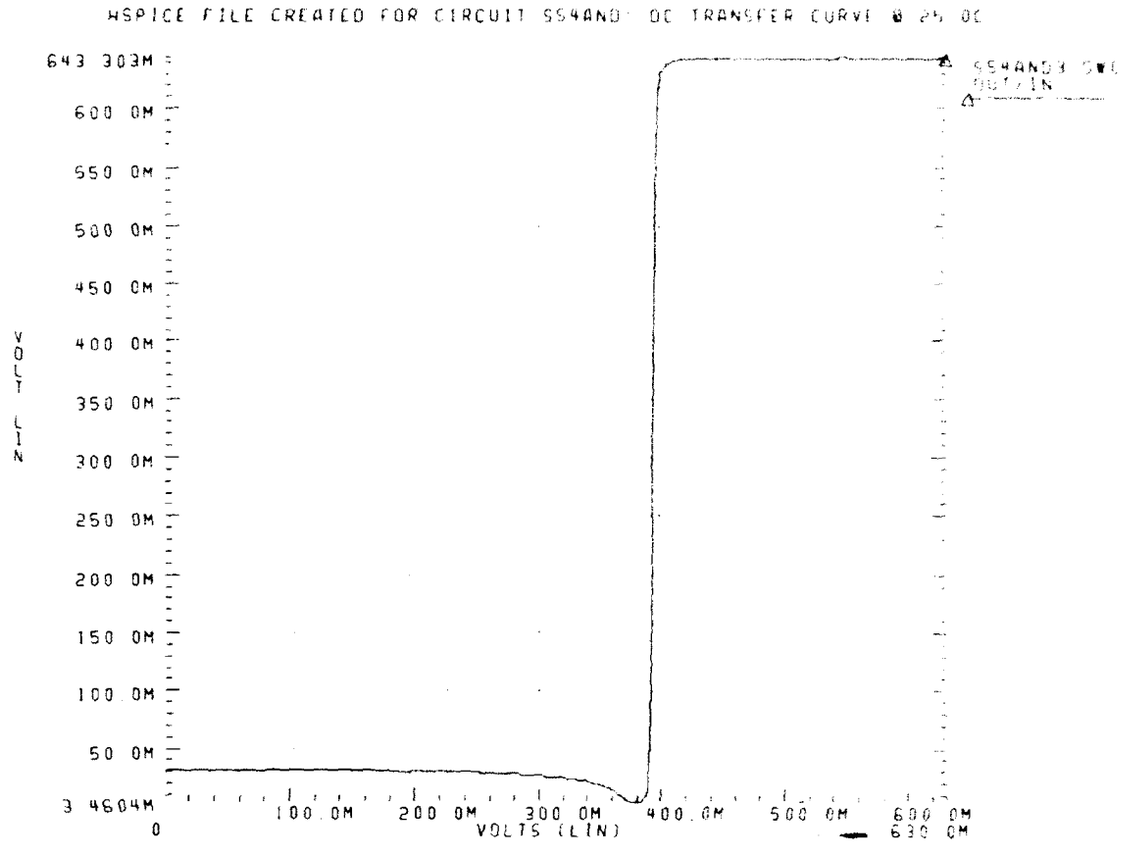


Figure 4.129 SS4AND DC Transfer Curve at 25.0C

The DC transfer characteristic of the SS4AND logic gate operating at a temperature of 85.0C is shown in Figure 4.130 on page 124.

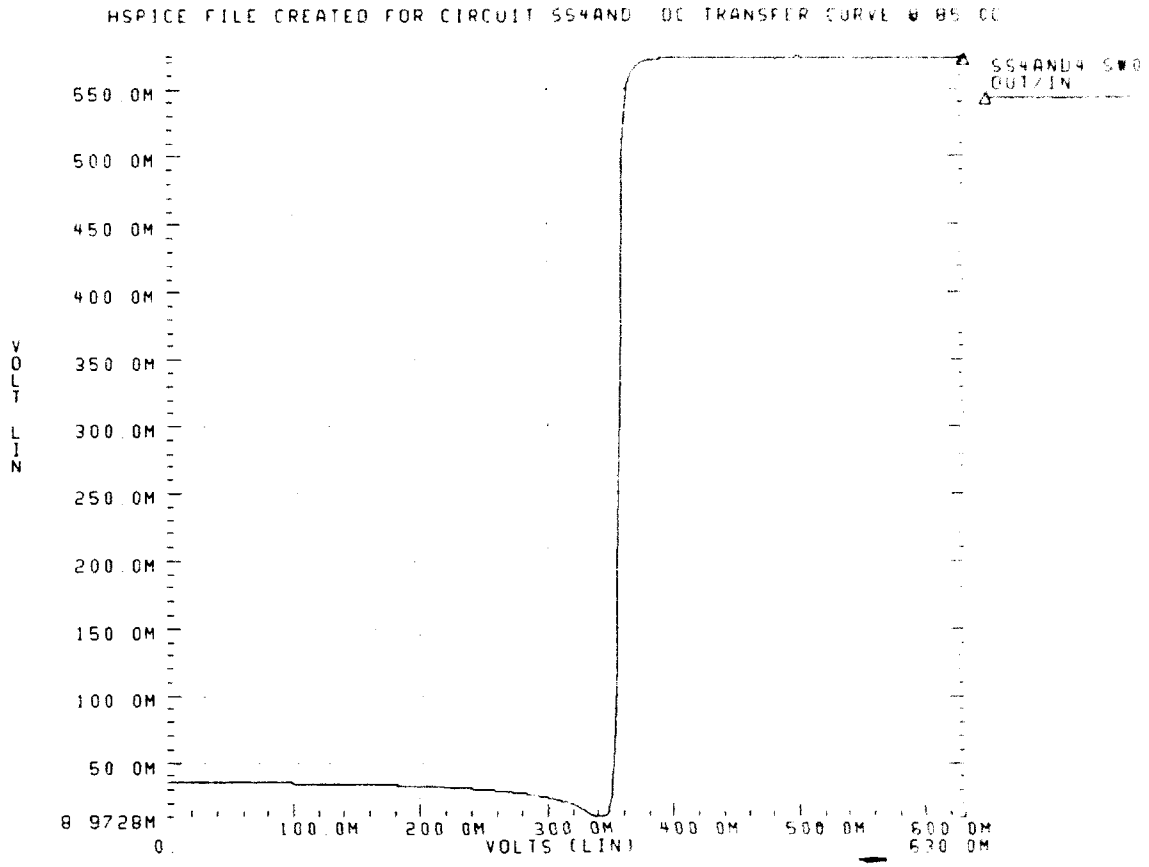


Figure 4.130 SS4AND DC Transfer Curve at 85.0C

11. SBFL 2-input NOR Gate (BS2NOR)

The following graphs represent the operating characteristics of the BS2NOR. This logic element was designed specifically for use in the BS2AND which is then used in the DELAY circuit. Notice the unusual MESFET size ratios. See Figure 4.131 on page 125 for the BS2NOR schematic and logical equivalence.

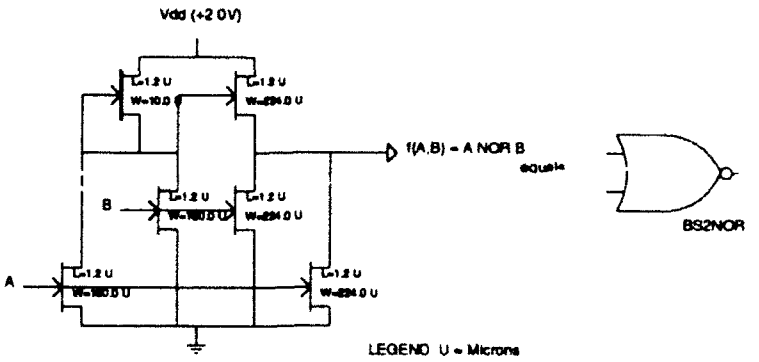


Figure 4.131 Schematic and Logical Equivalence for BS2NOR

The transient analysis and power dissipation of the BS2NOR operating at a temperature of 25.0C is shown in Figure 4.132 on page 125.

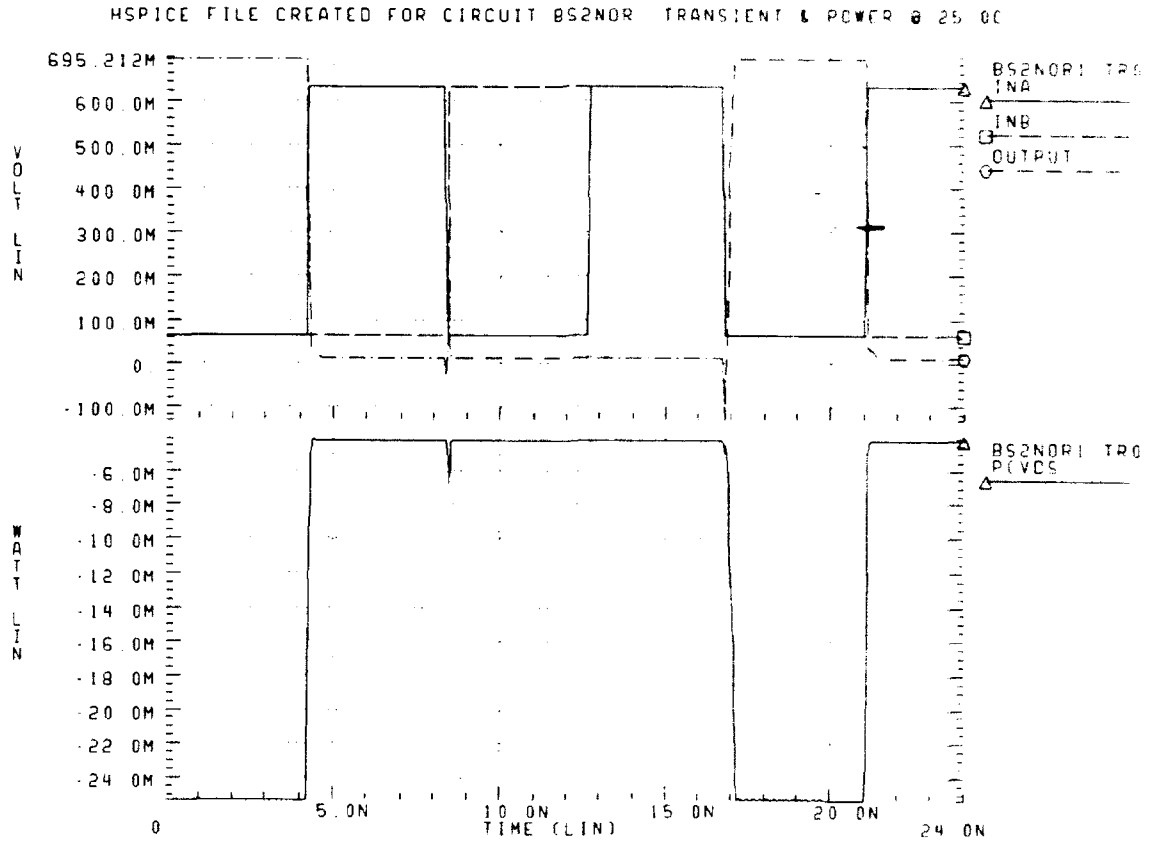


Figure 4.132 BS2NOR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the BS2NOR operating at a temperature of 85.0C is shown in Figure 4.133 on page 126.

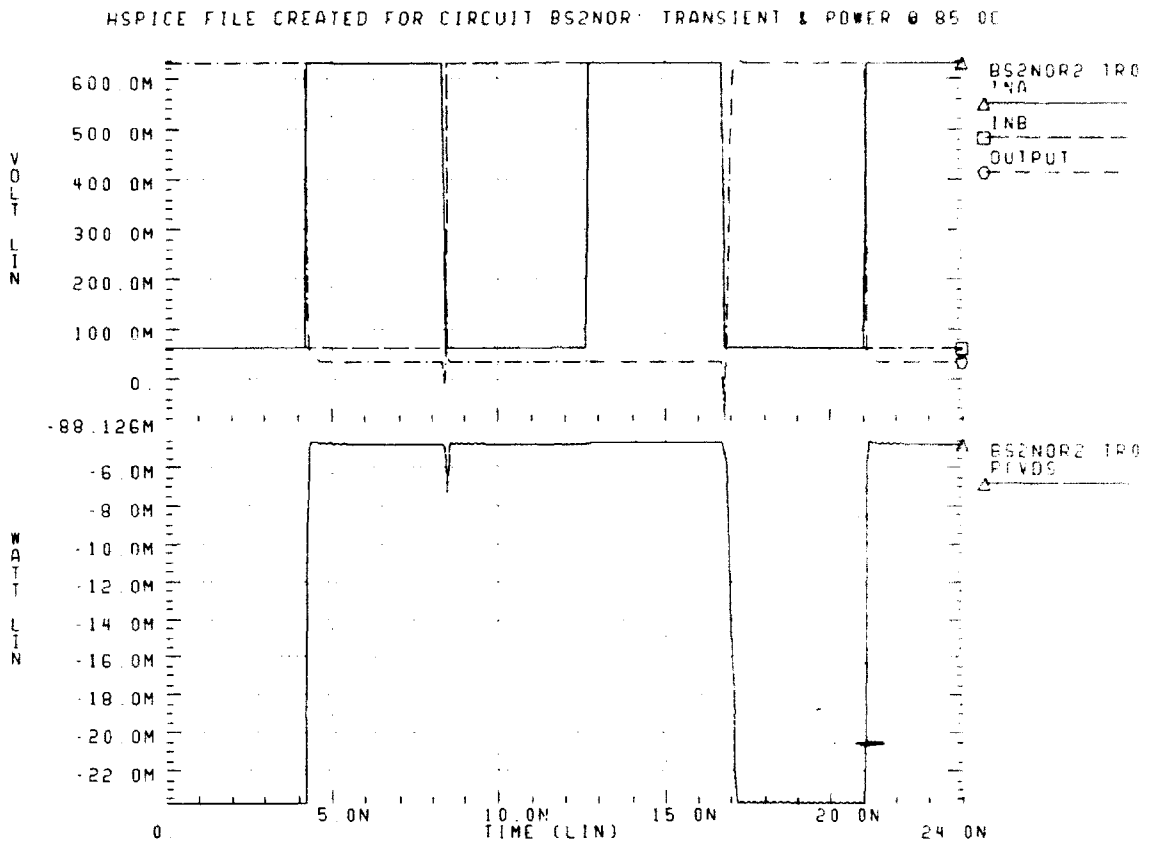


Figure 4.133 BS2NOR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the BS2NOR logic gate operating at a temperature of 25.0C is shown in Figure 4.134 on page 127.

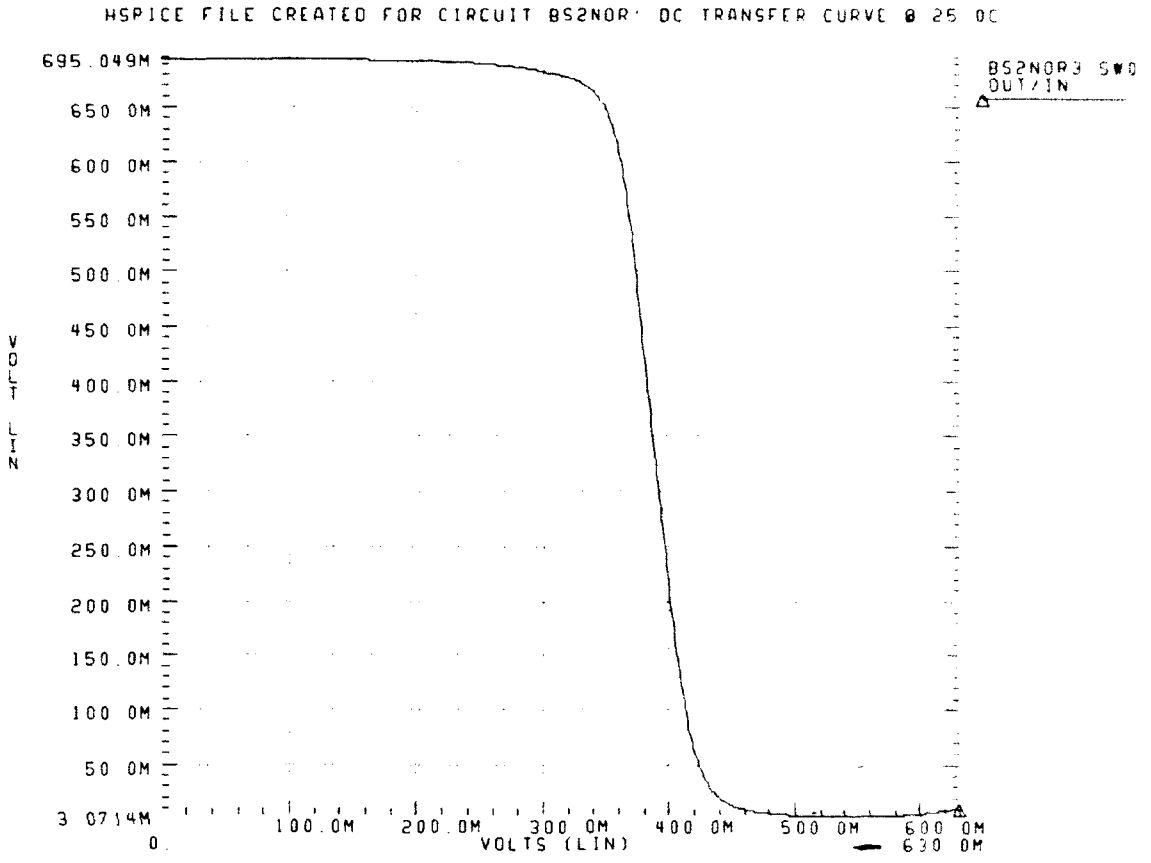


Figure 4.134 BS2NOR DC Transfer Curve at 25.0C

The DC transfer characteristic of the BS2NOR logic gate operating at a temperature of 85.0C is shown in Figure 4.135 on page 128.

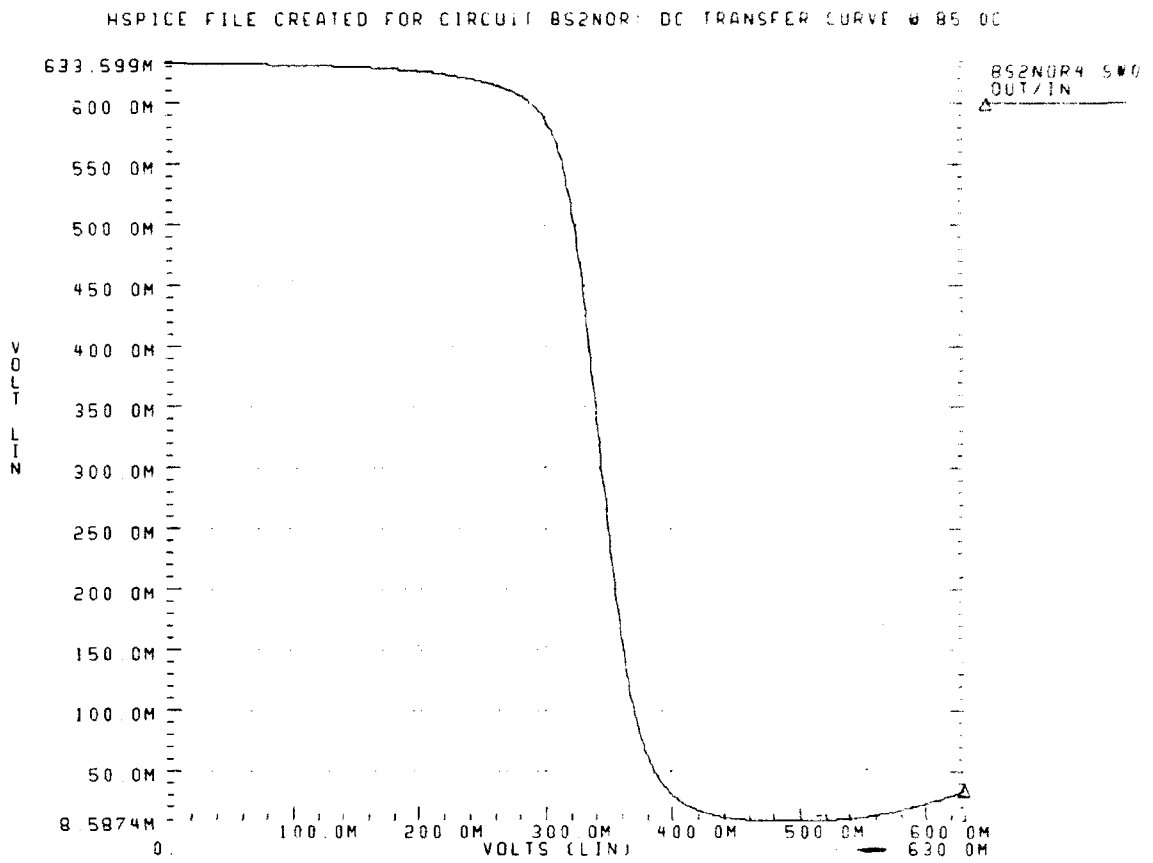


Figure 4.135 BS2NOR DC Transfer Curve at 85.0C

12. SBFL INVERTER (CSINV)

The following graphs represent the operating characteristics of the CSINV. This logic element was designed specifically for use in the CLOCK circuit. Notice the unusual MESFET size ratios. See Figure 4.136 on page 129 for the CSINV schematic and logical equivalence.

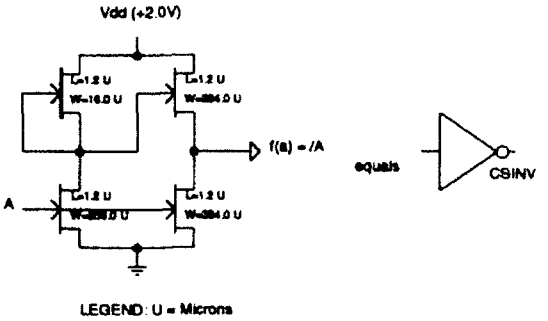


Figure 4.136 Schematic and Logical Equivalence for CSINV

The transient analysis and power dissipation of the CSINV operating at a temperature of 25.0C is shown in Figure 4.137 on page 129.

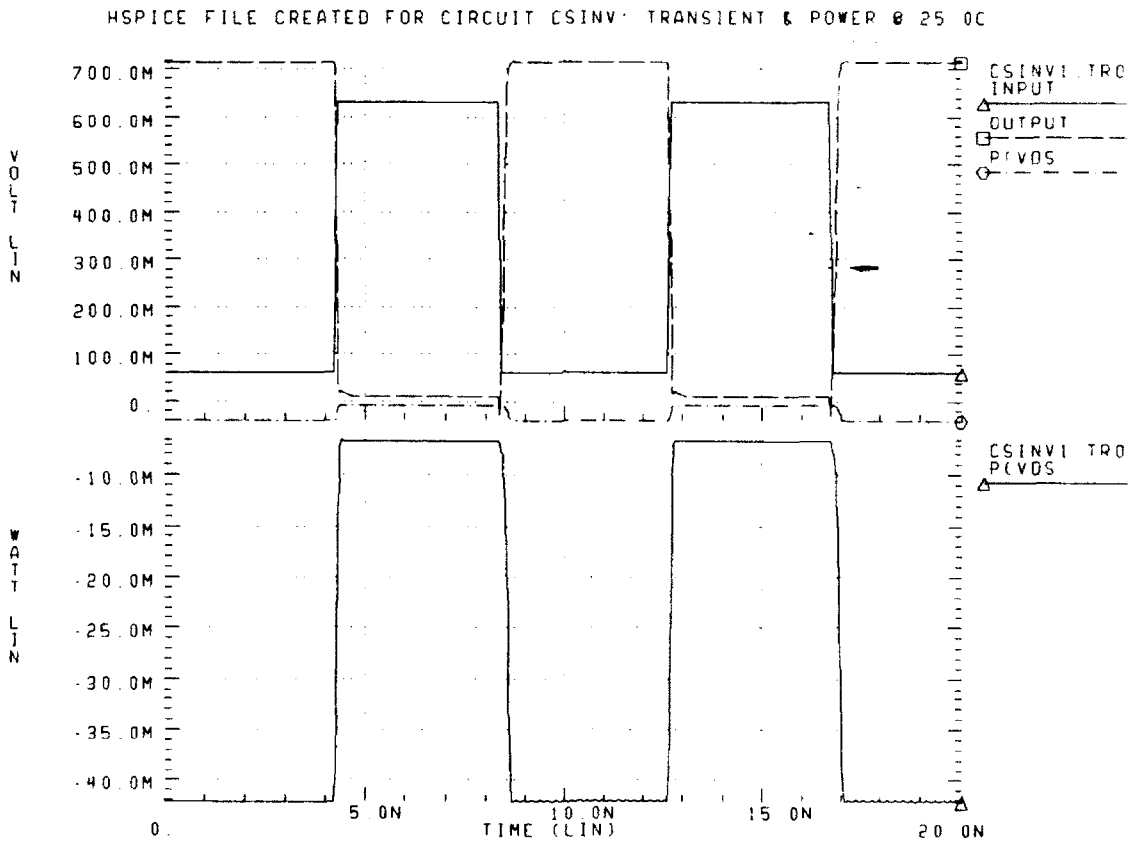


Figure 4.137 CSINV HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the CSINV operating at a temperature of 85.0C is shown in Figure 4.138 on page 130.

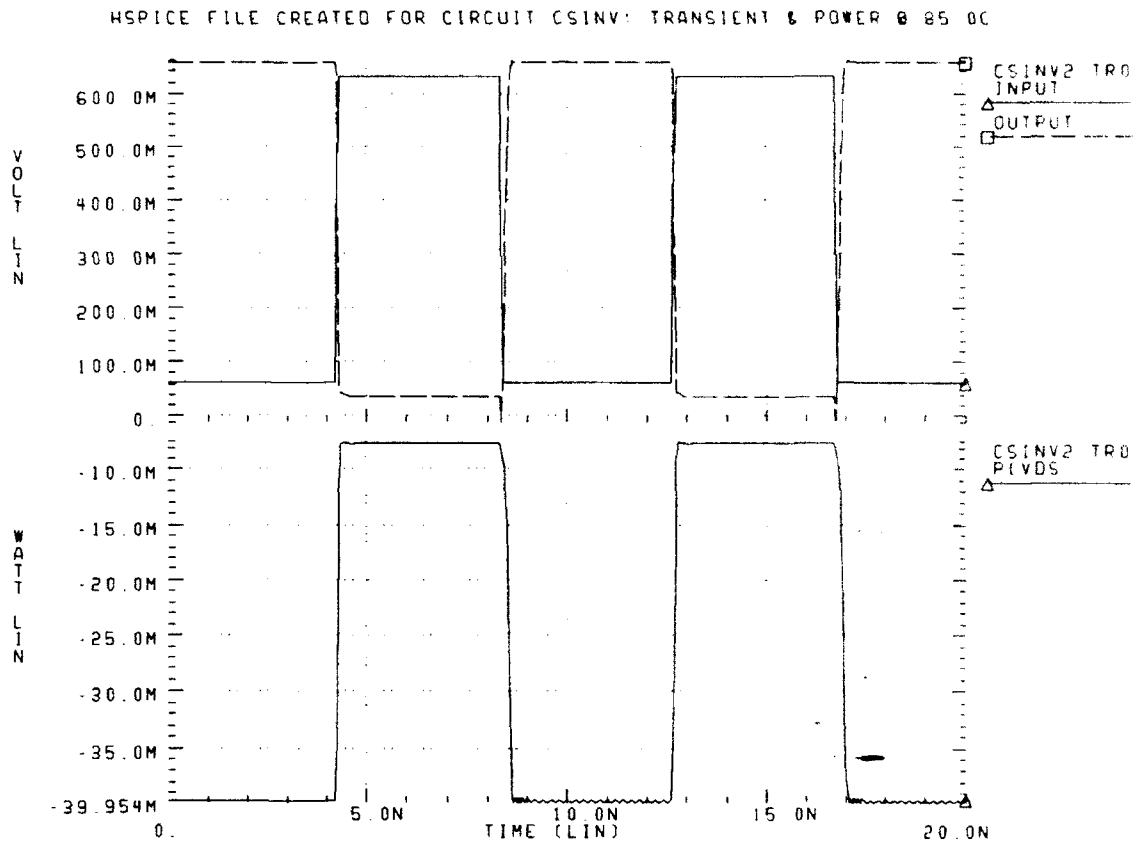


Figure 4.138 CSINV HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the CSINV logic gate operating at a temperature of 25.0C is shown in Figure 4.139 on page 131.

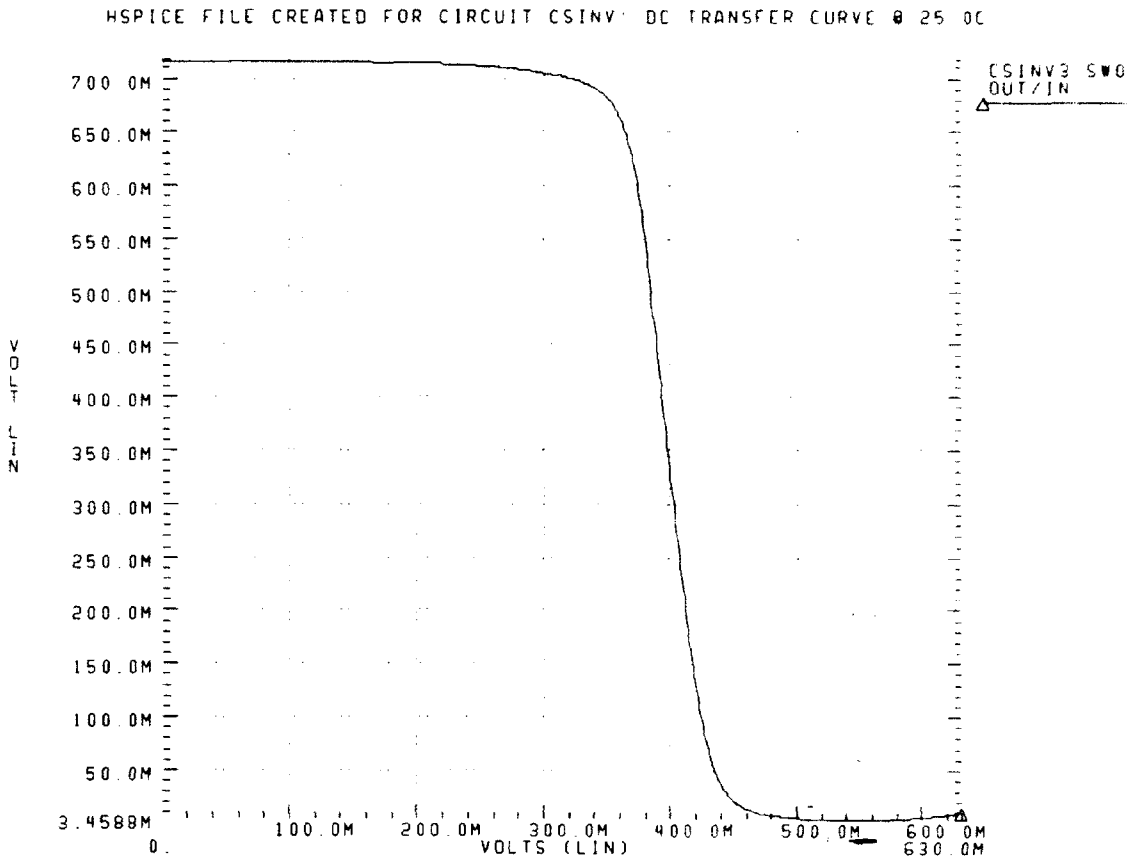


Figure 4.139 CSINV DC Transfer Curve at 25.0C

The DC transfer characteristic of the CSINV logic gate operating at a temperature of 85.0C is shown in Figure 4.140 on page 132.

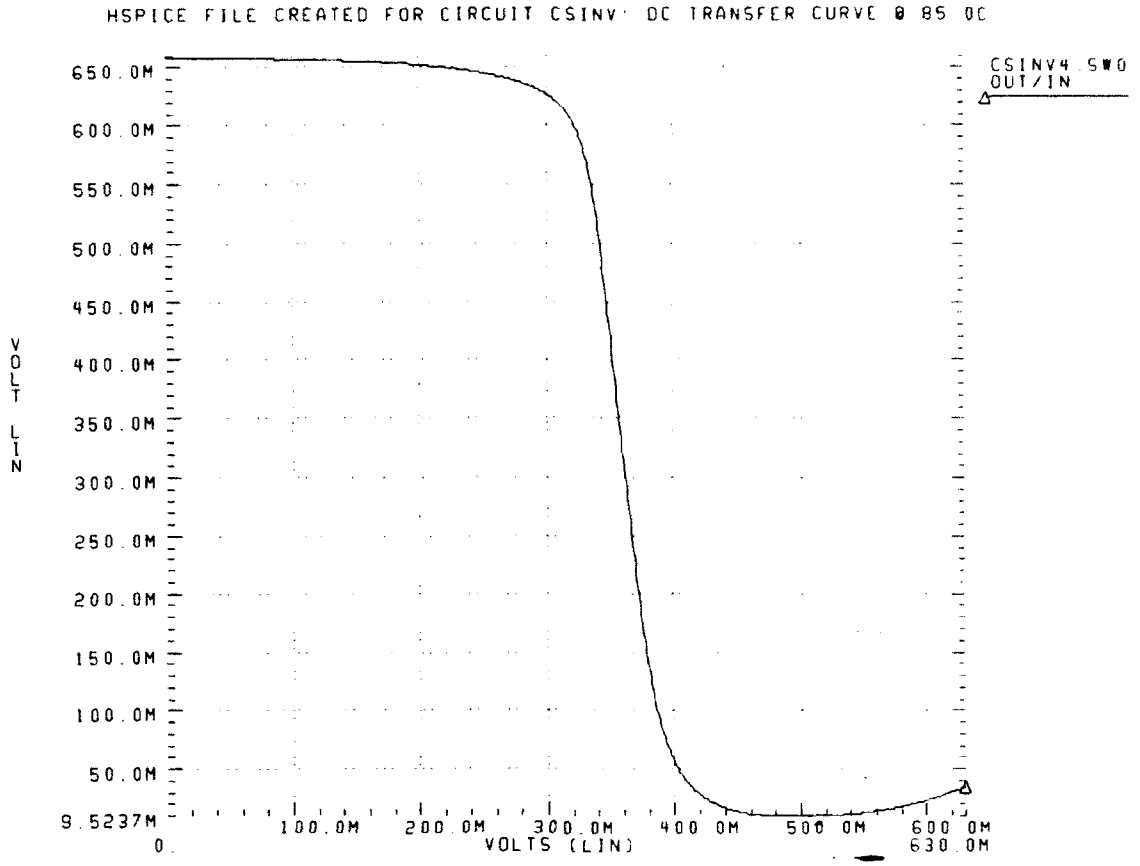


Figure 4.140 CSINV DC Transfer Curve at 85.0C

13. SBFL 2-input NOR Gate (CSNOR)

The following graphs represent the operating characteristics of the CSNOR. This logic element was designed specifically for use in the CLOCK circuit. Notice the unusual MESFET size ratios. See Figure 4.141 on page 133 for the BS2NOR schematic and logical equivalence.

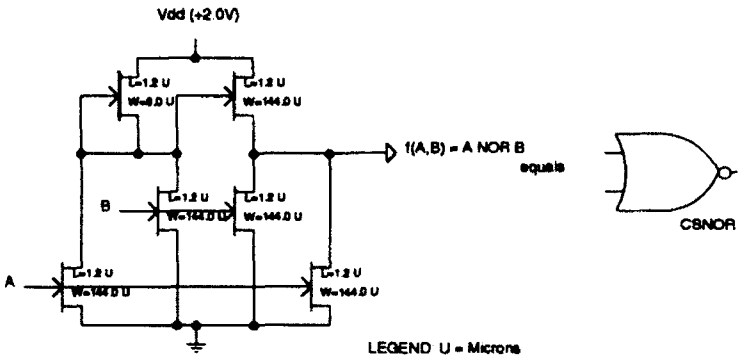


Figure 4.141 Schematic and Logical Equivalence for CSNOR

The transient analysis and power dissipation of the CSNOR operating at a temperature of 25.0C is shown in Figure 4.142 on page 133.

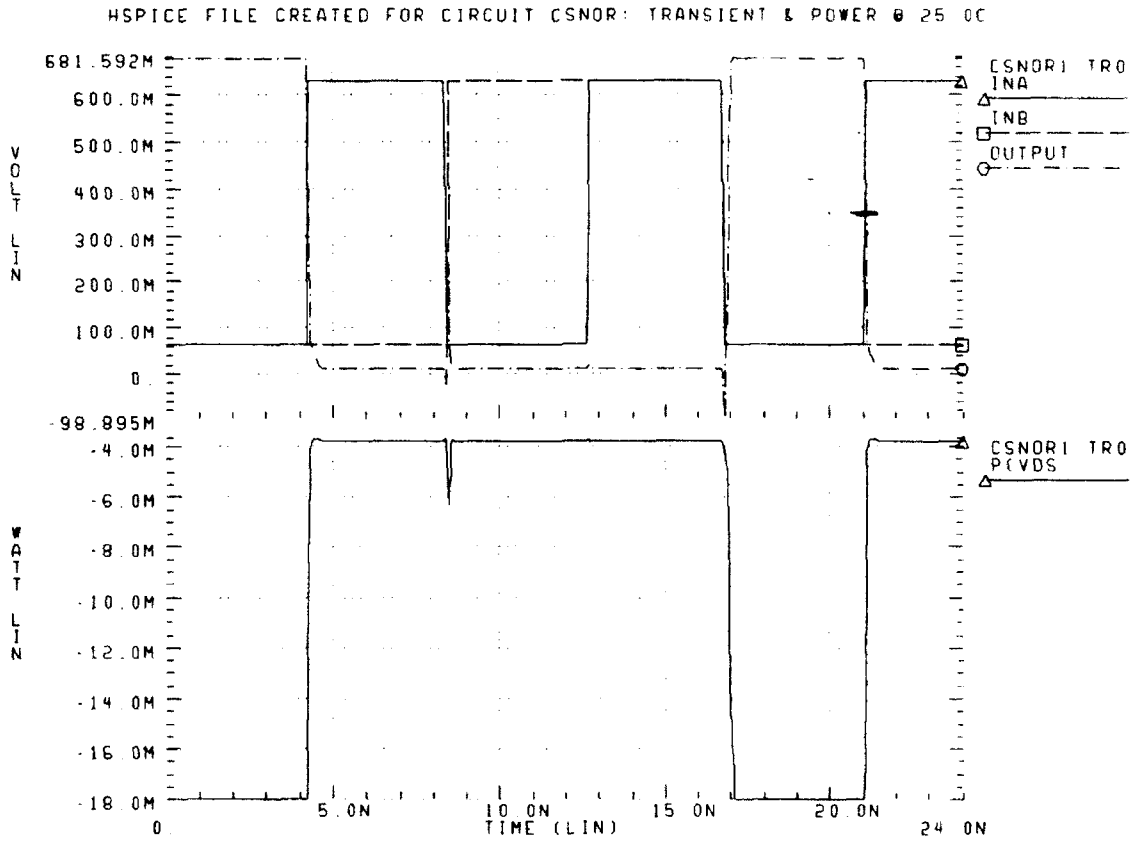


Figure 4.142 CSNOR HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the CSNOR operating at a temperature of 85.0C is shown in Figure 4.143 on page 134.

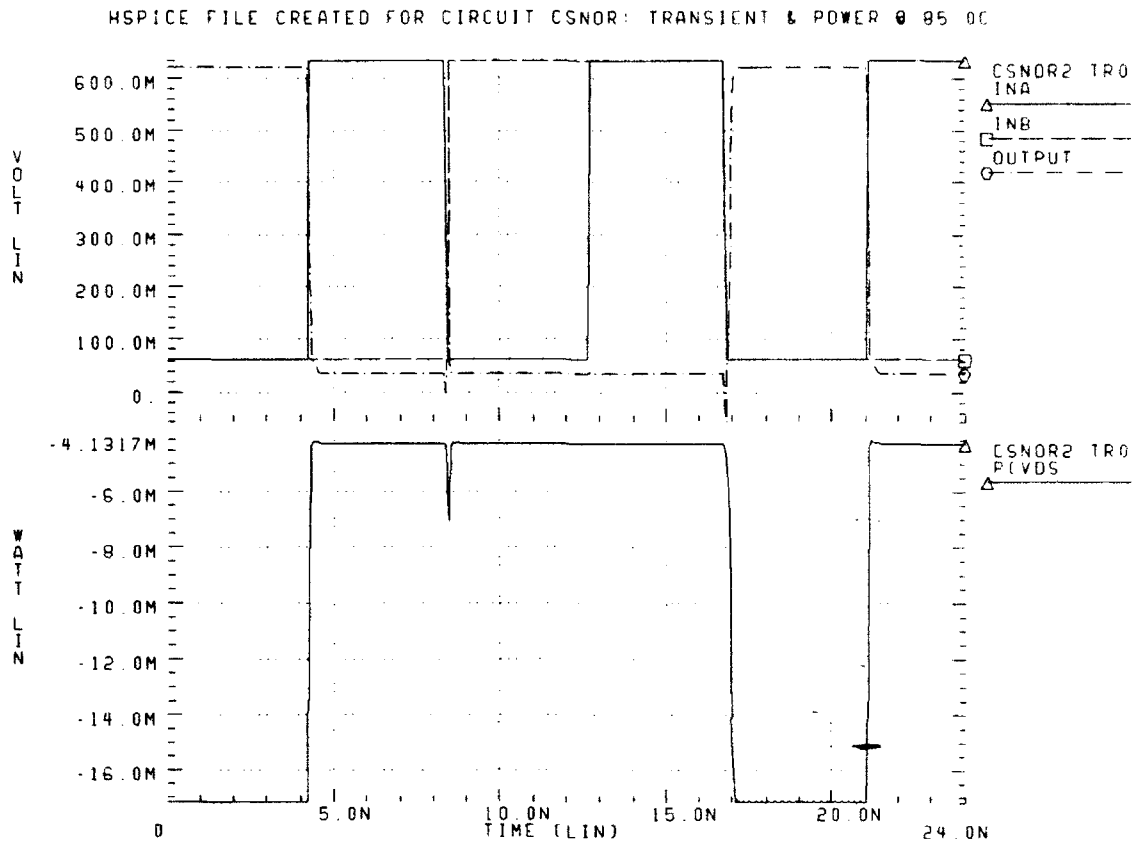


Figure 4.143 CSNOR HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the CSNOR logic gate operating at a temperature of 25.0C is shown in Figure 4.144 on page 135.

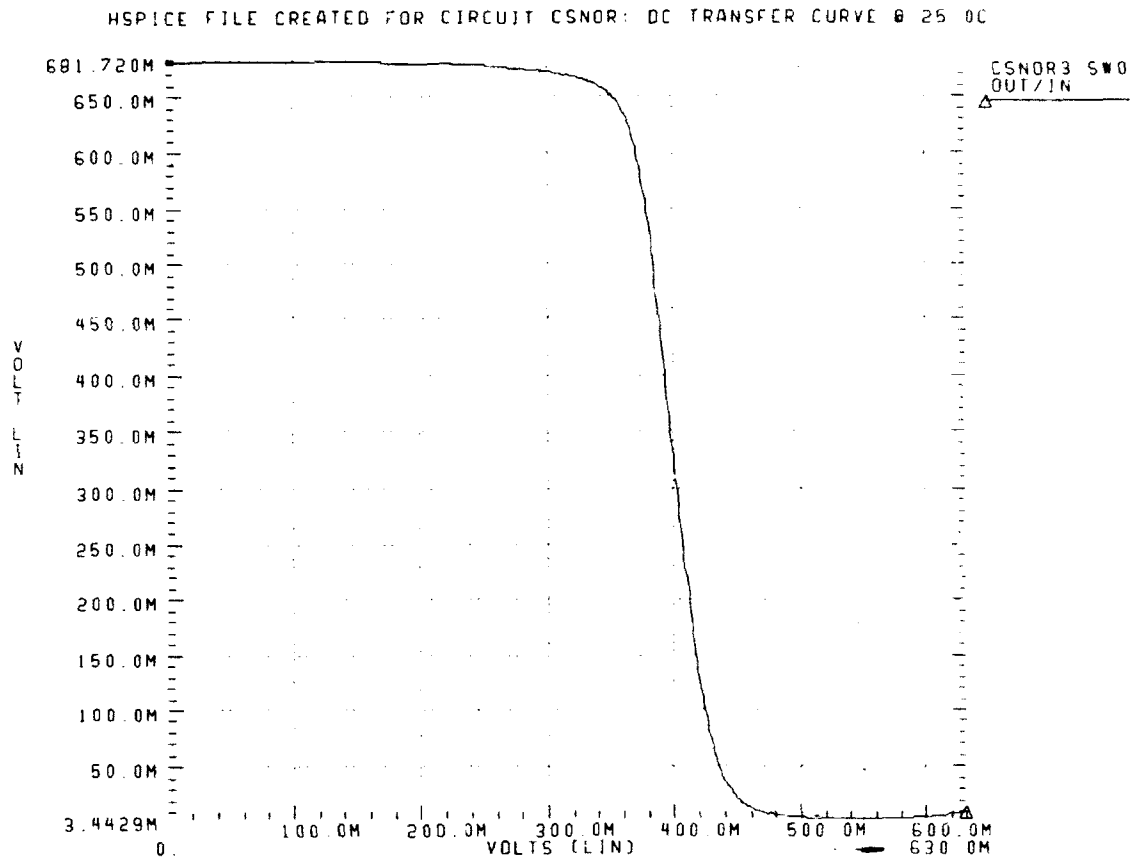


Figure 4.144 CSNOR DC Transfer Curve at 25.0C

The DC transfer characteristic of the CSNOR logic gate operating at a temperature of 85.0C is shown in Figure 4.145 on page 136.

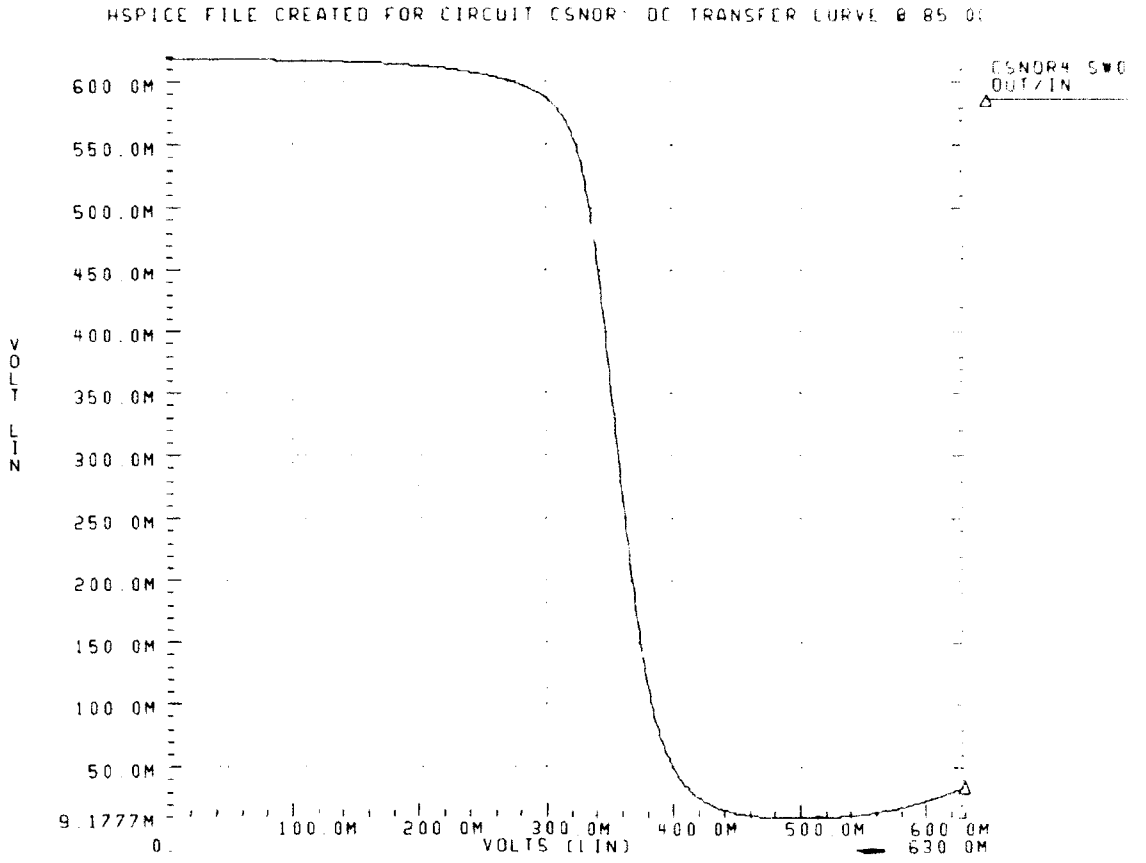


Figure 4.145 CSNOR DC Transfer Curve at 85.0C

C. GaAs DRAM Mixed DCFL-SBFL Logic Circuits

This section will present the specific mixed DCFL-SBFL gates used, presenting the schematic and logical equivalence for each. These gates are hybrids designed specifically for parameter requirements of particular circuits. The following characteristics for each circuit will be demonstrated and presented: transient analysis under standard load, power consumption at nominal and high temperature, propagation delays and noise margins. These characteristics will be further summarized in TABLE 4.1 on page 158. Germane comments will be made when appropriate.

1. DCFL-SBFL 2-input AND Gate (BS2AND)

The following graphs represent the operating characteristics of the BS2AND. This logic element was designed specifically for use in the DELAY circuit. See Figure 4.146 on page 137 for the BS2AND schematic and logical equivalence.

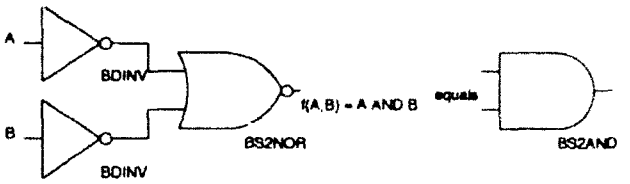


Figure 4.146 Schematic and Logical Equivalence for BS2AND

The transient analysis and power dissipation of the BS2AND operating at a temperature of 25.0C is shown in Figure 4.147 on page 137.

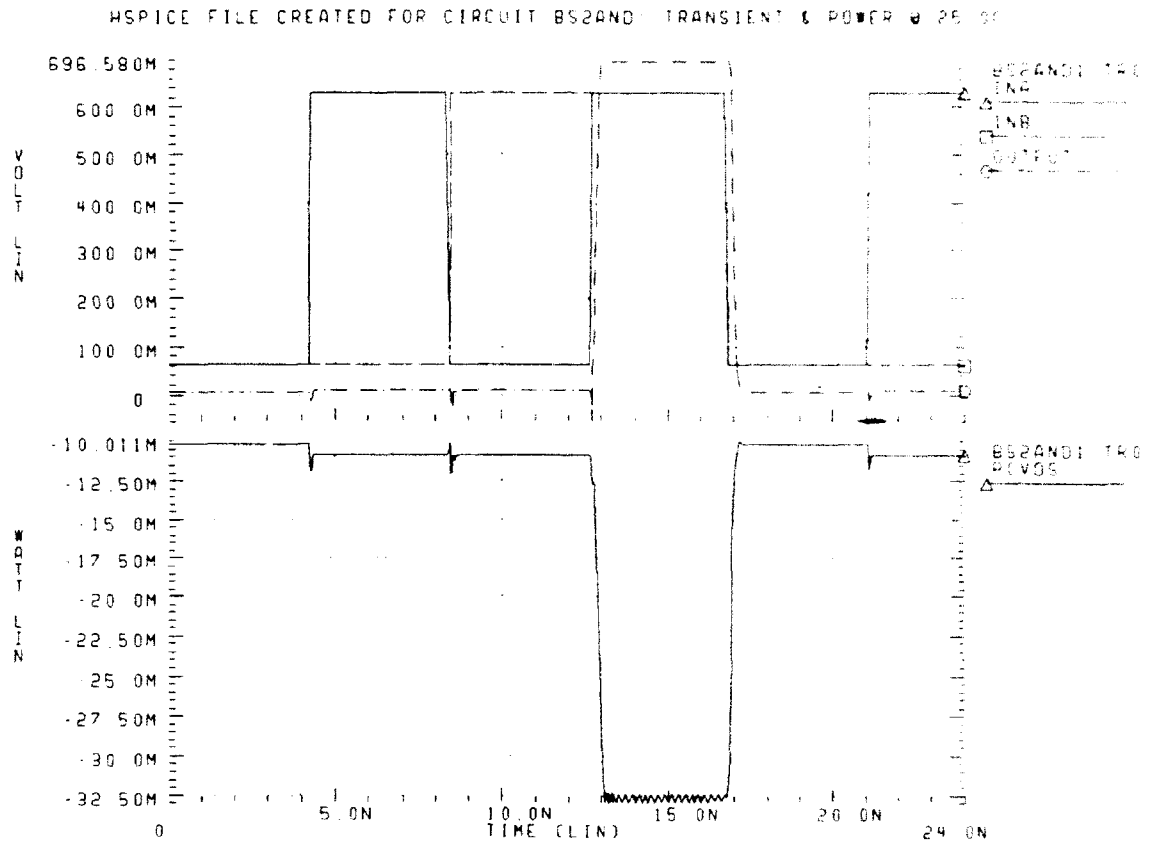


Figure 4.147 BS2AND HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the BS2AND operating at a temperature of 85.0C is shown in Figure 4.148 on page 138.

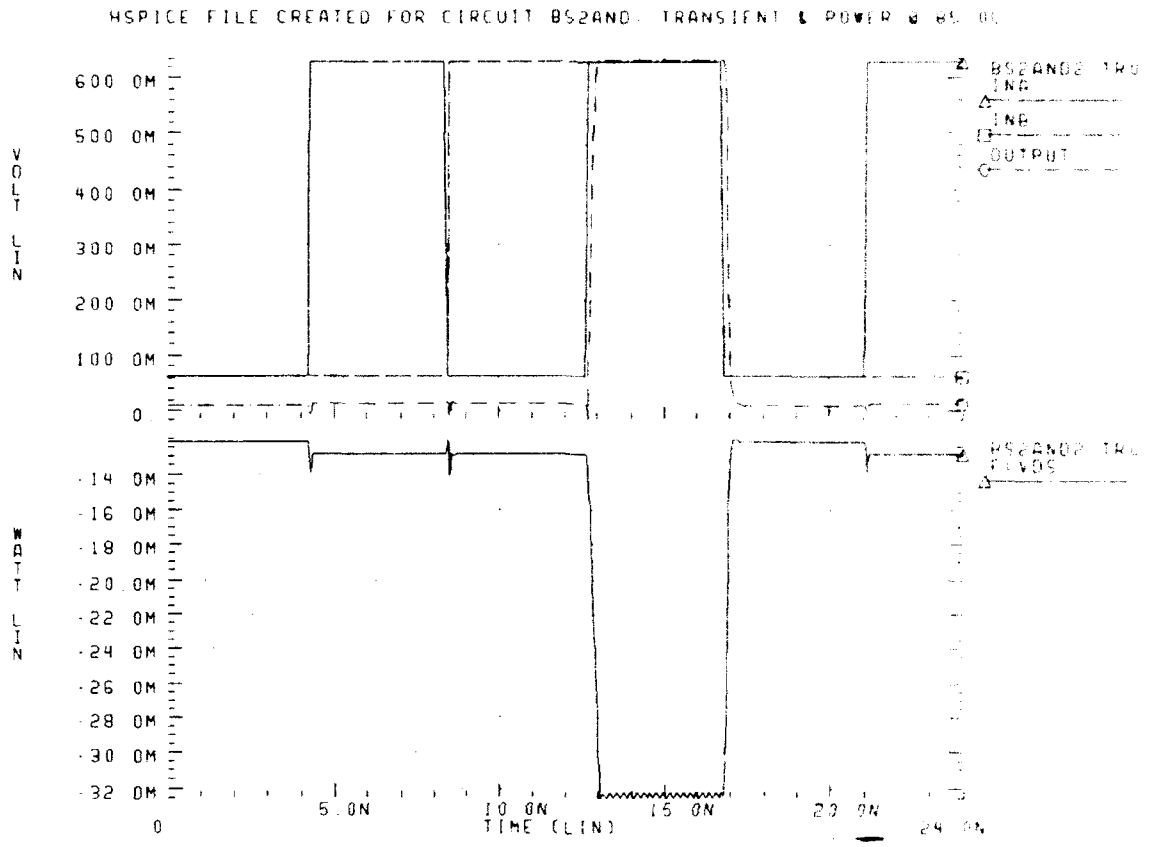


Figure 4.148 BS2AND HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the BS2AND logic gate operating at a temperature of 25.0C is shown in Figure 4.149 on page 139.

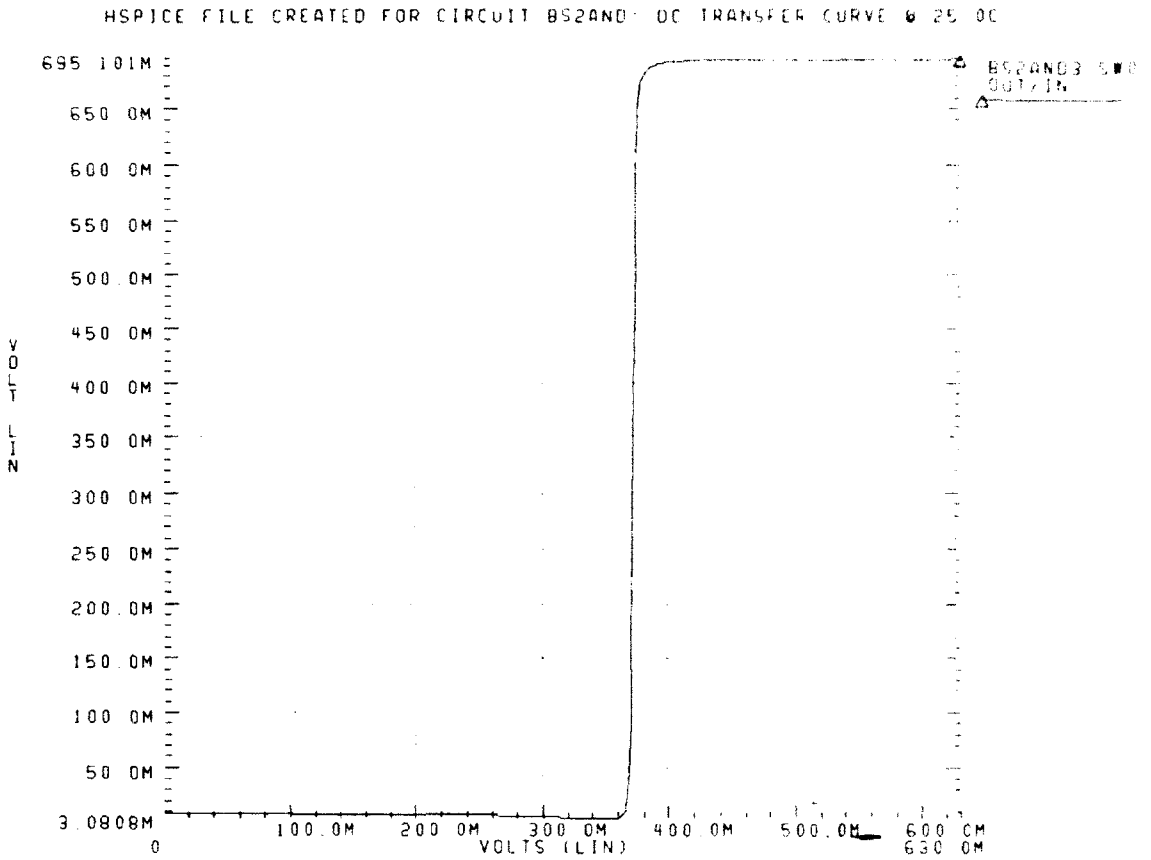


Figure 4.149 BS2AND DC Transfer Curve at 25.0C

The DC transfer characteristic of the BS2AND logic gate operating at a temperature of 85.0C is shown in Figure 4.150 on page 140.

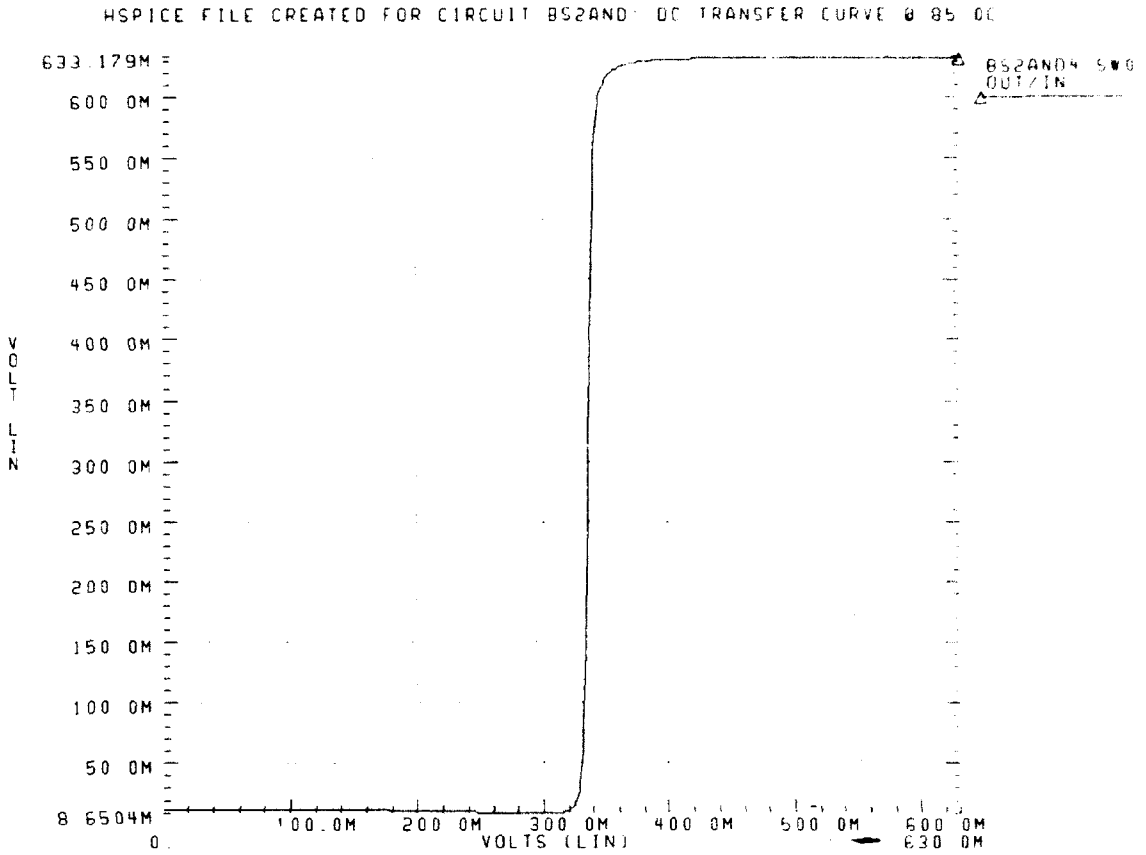


Figure 4.150 BS2AND DC Transfer Curve at 85.0C

2. SBFL-DCFL Data LATCH (SDLATCH)

The following graphs represent the operating characteristics of the SDLATCH. This logic element was designed specifically for use in the SDFF logic gate which is then used in the DREFRESH circuit. Notice that the structure of the logic element is such that it has a DCFL "front-end" with a SBFL "back-end" for use as drivers. See Figure 4.151 on page 141 for the SDLATCH schematic and logical equivalence.

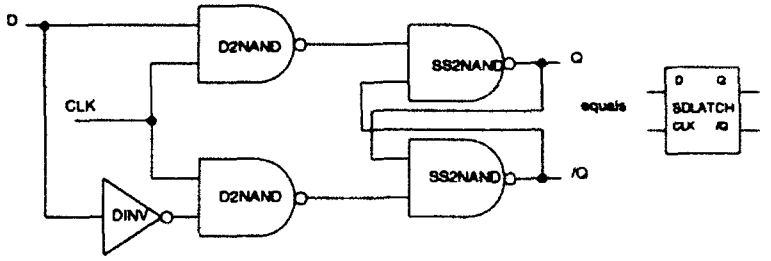


Figure 4.151 Schematic and Logical Equivalence for SDLATCH

The transient analysis and power dissipation of the SDLATCH operating at a temperature of 25.0C is shown in Figure 4.152 on page 142. Notice that in Figure 4.152 and Figure 4.153 on page 143, the lower (power) graph has several large power spikes. These spikes are caused by the surging of current when the Q output changes state which then in turn causes the /Q output to change state. Examining the schematic for the SDLATCH, as shown previously in Figure 4.151, one may see how this phenomenon occurs.

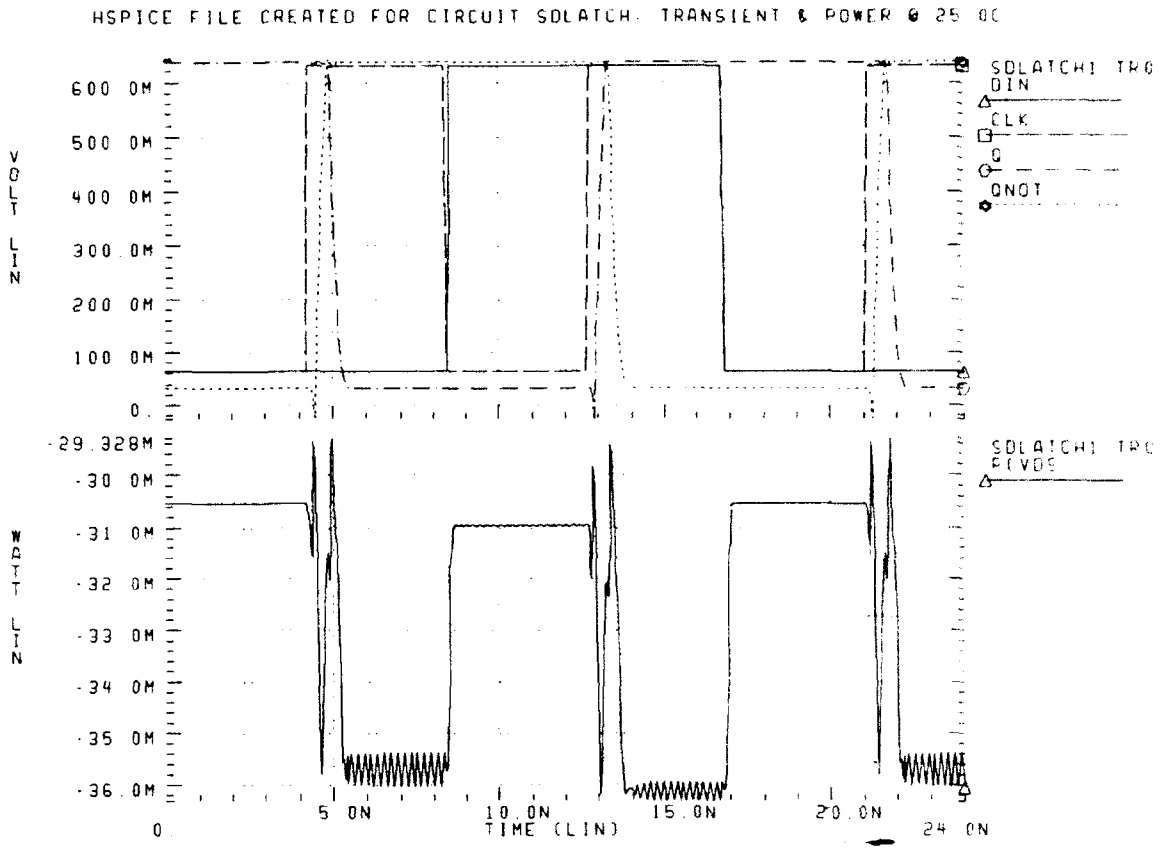


Figure 4.152 SDLATCH HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the SDLATCH operating at a temperature of 85.0C is shown in Figure 4.153 on page 143.

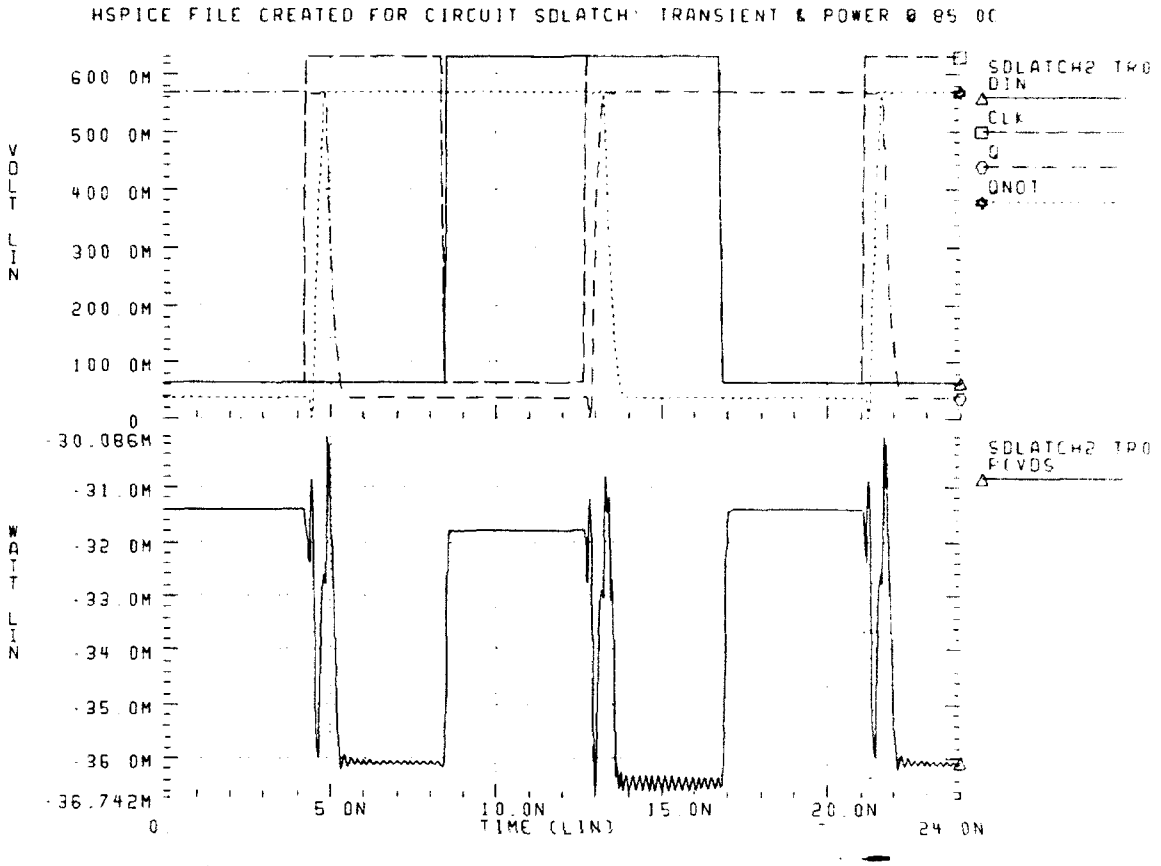


Figure 4.153 SDLATCH HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the SDLATCH logic gate operating at a temperature of 25.0C is shown in Figure 4.154 on page 144.

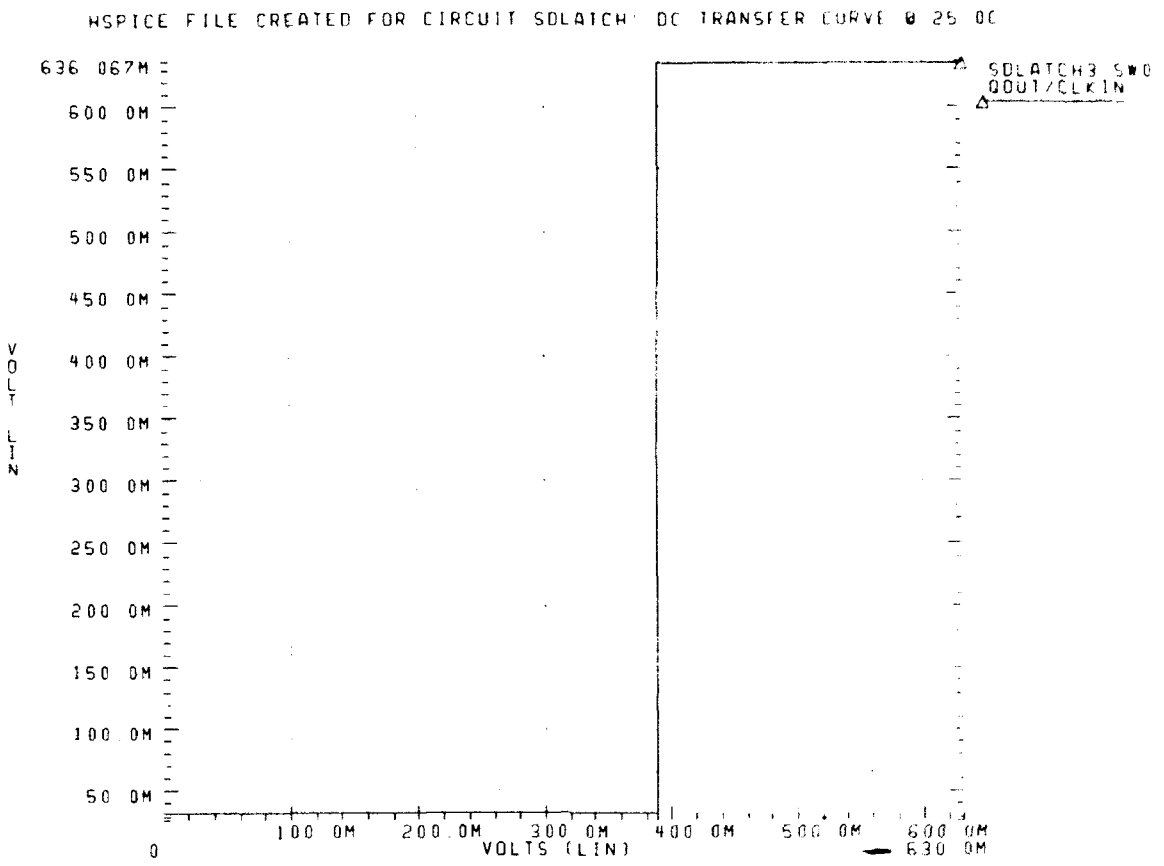


Figure 4.154 SDLATCH DC Transfer Curve at 25.0C

The DC transfer characteristic of the SDLATCH logic gate operating at a temperature of 85.0C is shown in Figure 4.150 on page 140.

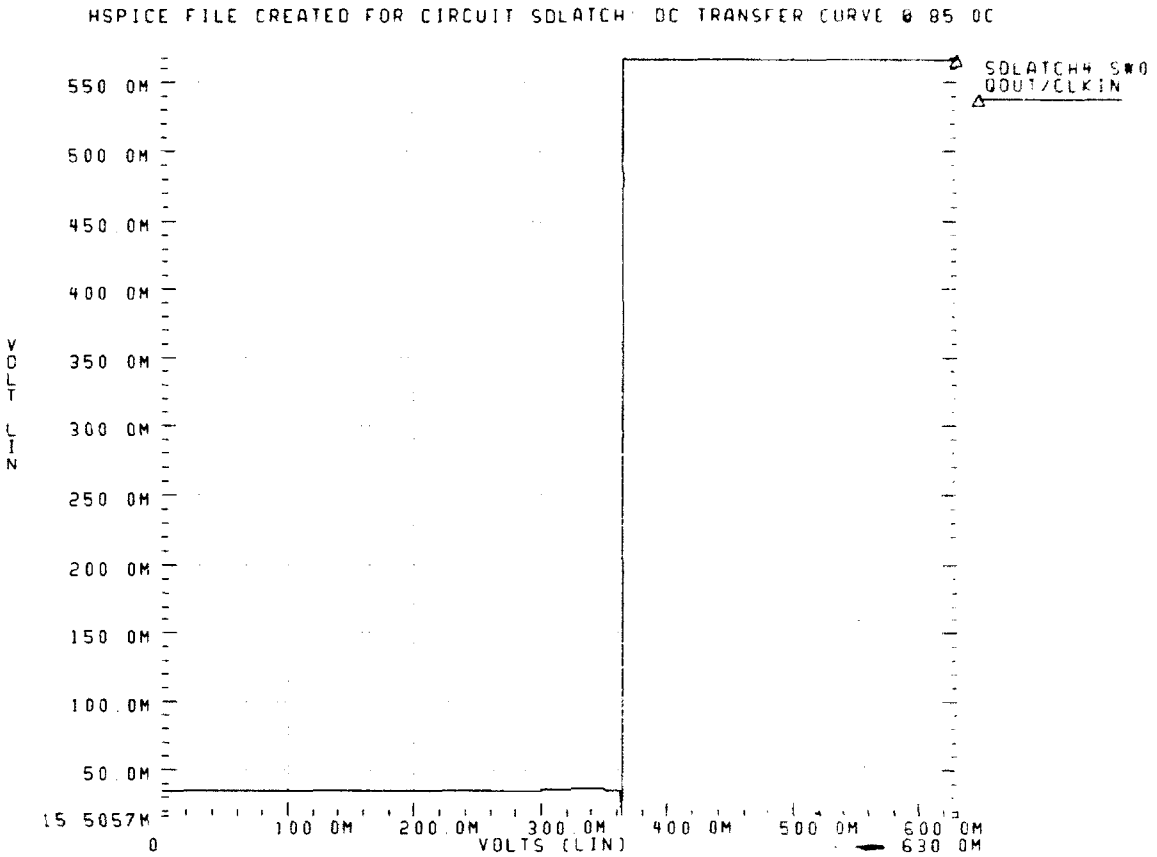


Figure 4.155 SDLATCH DC Transfer Curve at 85.0C

3. SBFL-DCFL Data Flip-Flop (SDFF)

The following graphs represent the operating characteristics of the SDFF. This logic element was designed specifically for use in the DREFRESH circuit. Notice that the structure of the logic element is such that it has a DCFL DLATCH "front-end" with a SBFL SDLATCH "back-end" for use as drivers. See Figure 4.156 on page 145 for the SDFF schematic and logical equivalence.

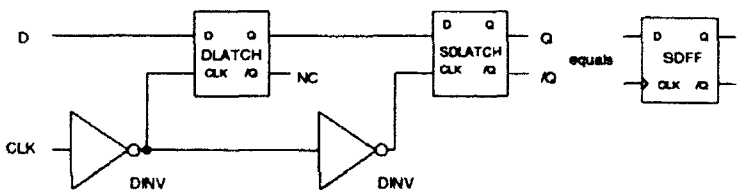


Figure 4.156 Schematic and Logical Equivalence for SDFF

The transient analysis and power dissipation of the SDFF operating at a temperature of 25.0C is shown in Figure 4.157 on page 146. The large power spikes, seen in Figure 4.157 and Figure 4.158 on page 147, arise from the use of the SDLATCH in the construction of the SDFF. Hence, the power spikes occur because of the current surges when the SDLATCH Q output changes state followed by the SDLATCH /Q output change of state.

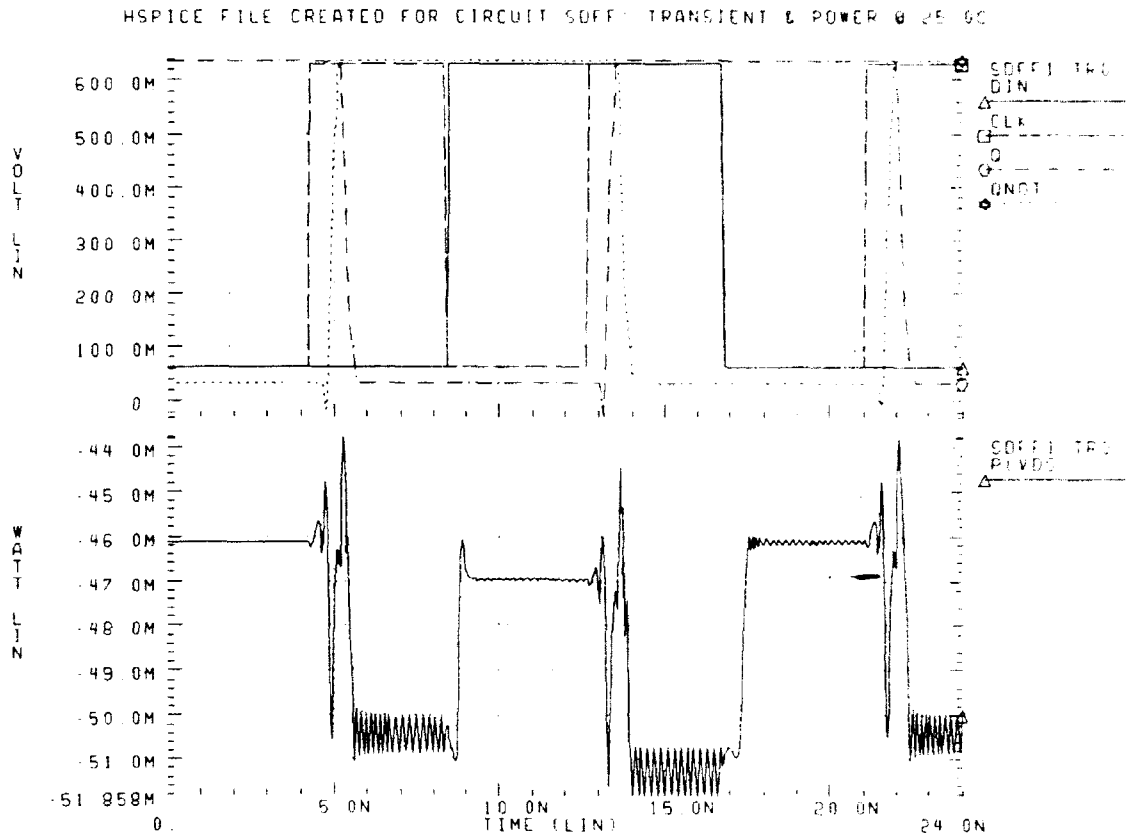


Figure 4.157 SDFF HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the SDFF operating at a temperature of 85.0C is shown in Figure 4.158 on page 147.

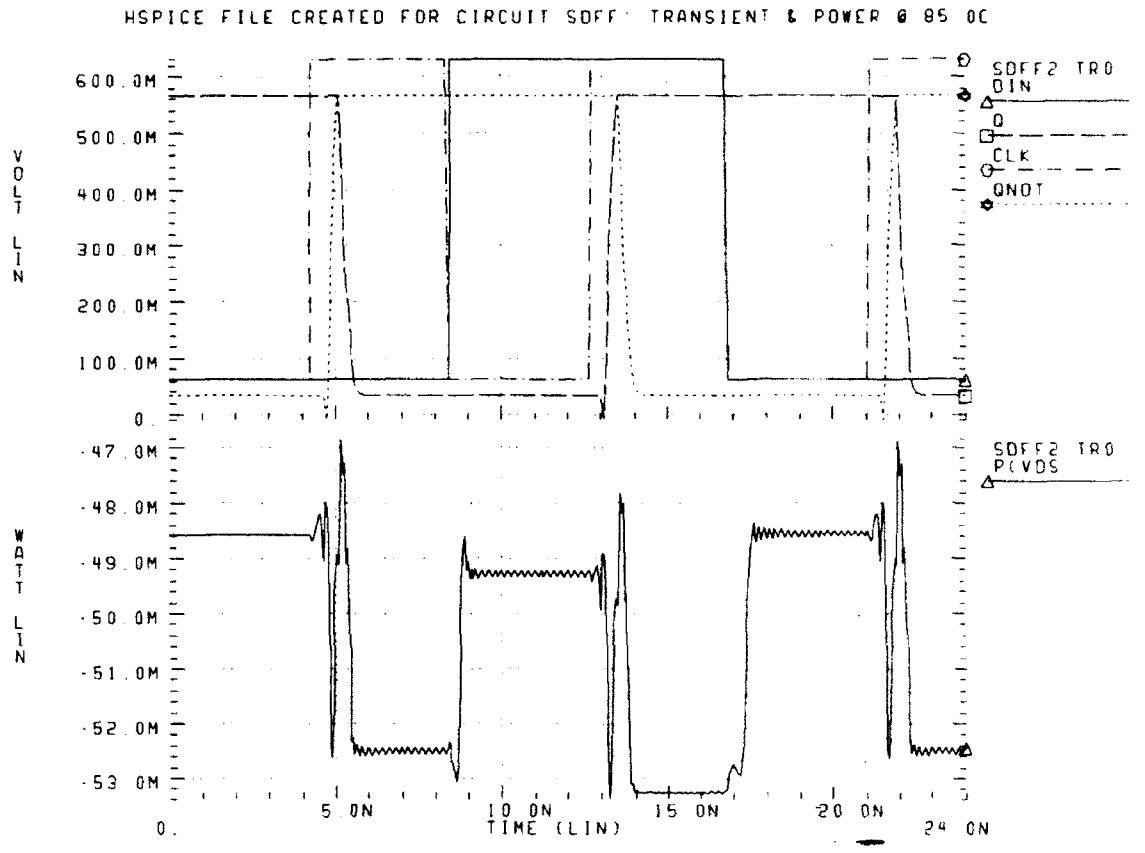


Figure 4.158 SDFF HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the SDFF logic gate operating at a temperature of 25.0C is shown in Figure 4.159 on page 148.

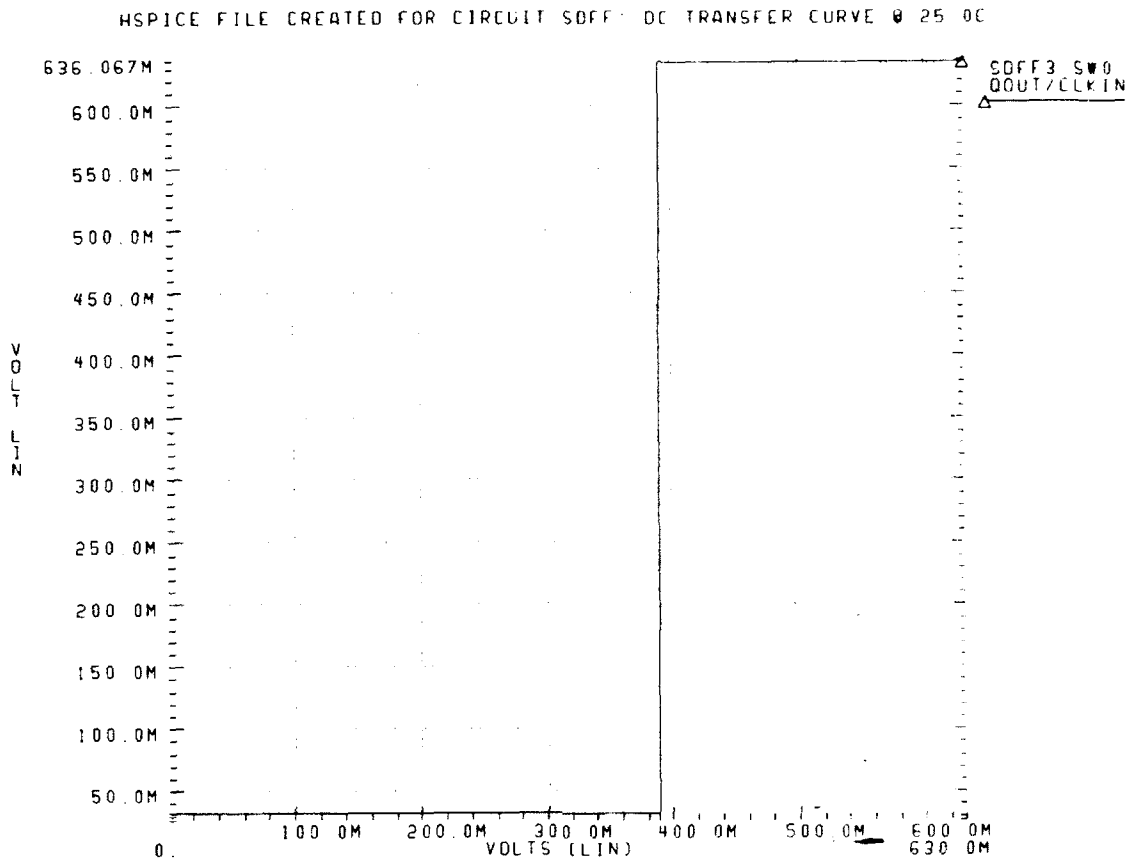


Figure 4.159 SDFF DC Transfer Curve at 25.0C

The DC transfer characteristic of the SDFF logic gate operating at a temperature of 85.0C is shown in Figure 4.160 on page 149.

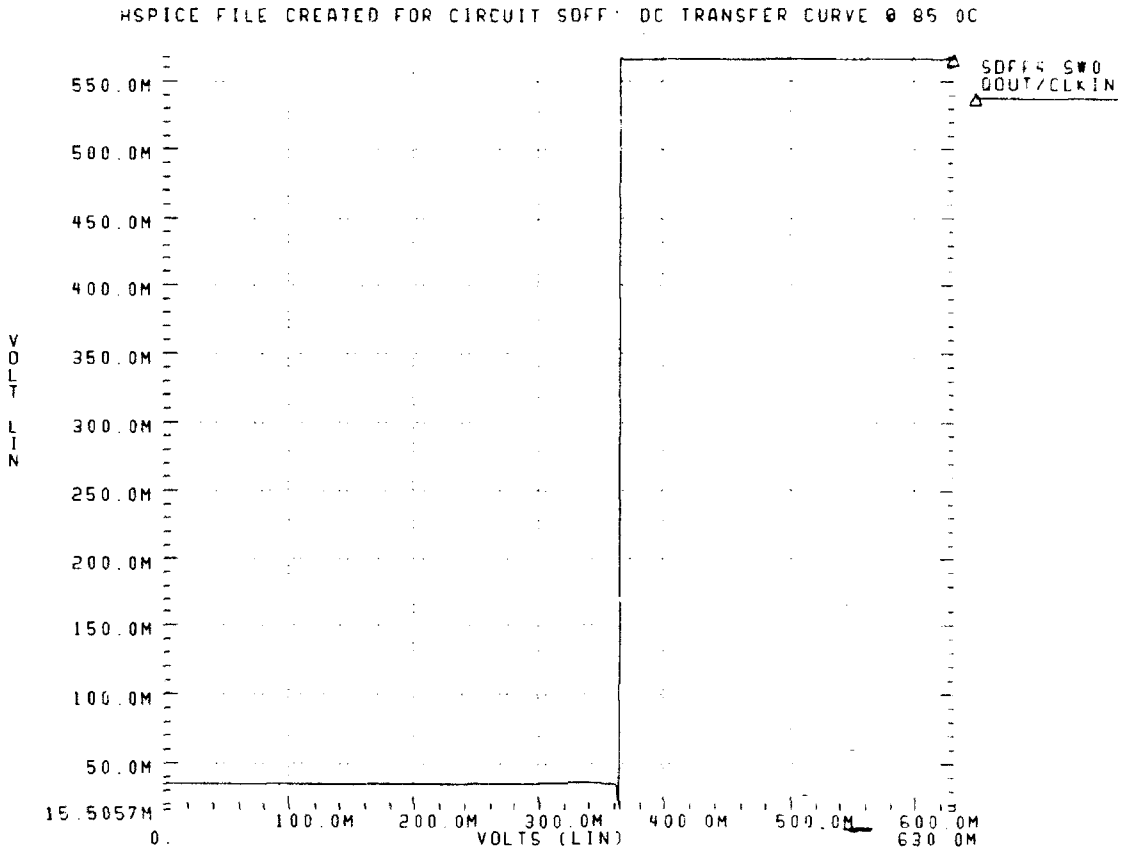


Figure 4.160 SDFF DC Transfer Curve at 85.0C

4. SBFL-DCFL DELAY Logic Element (DELAY)

The following graphs represent the operating characteristics of the DELAY. This logic element was designed specifically for use with the CLOCK circuit. The DELAY circuit will delay the input clock pulse by approximately 25% of a clock pulse width without applying logic inversion. See Table 4.1 for the specific details. See Figure 4.161 on page 149 for the DELAY schematic and logical equivalence.

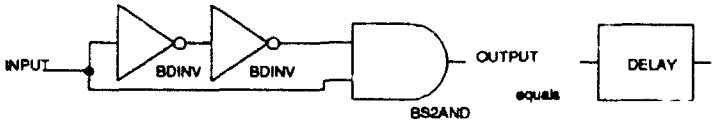


Figure 4.161 Schematic and Logical Equivalence for DELAY

The transient analysis and power dissipation of the DELAY operating at a temperature of 25.0C is shown in Figure 4.162 on page 150. It should be noted that this circuit was tested with a SBFL load of ten SINV's to better simulate real circuit loading conditions. See "Listing File for DELAY Transient Analysis @ 25.0C" of Appendix A on page 283.

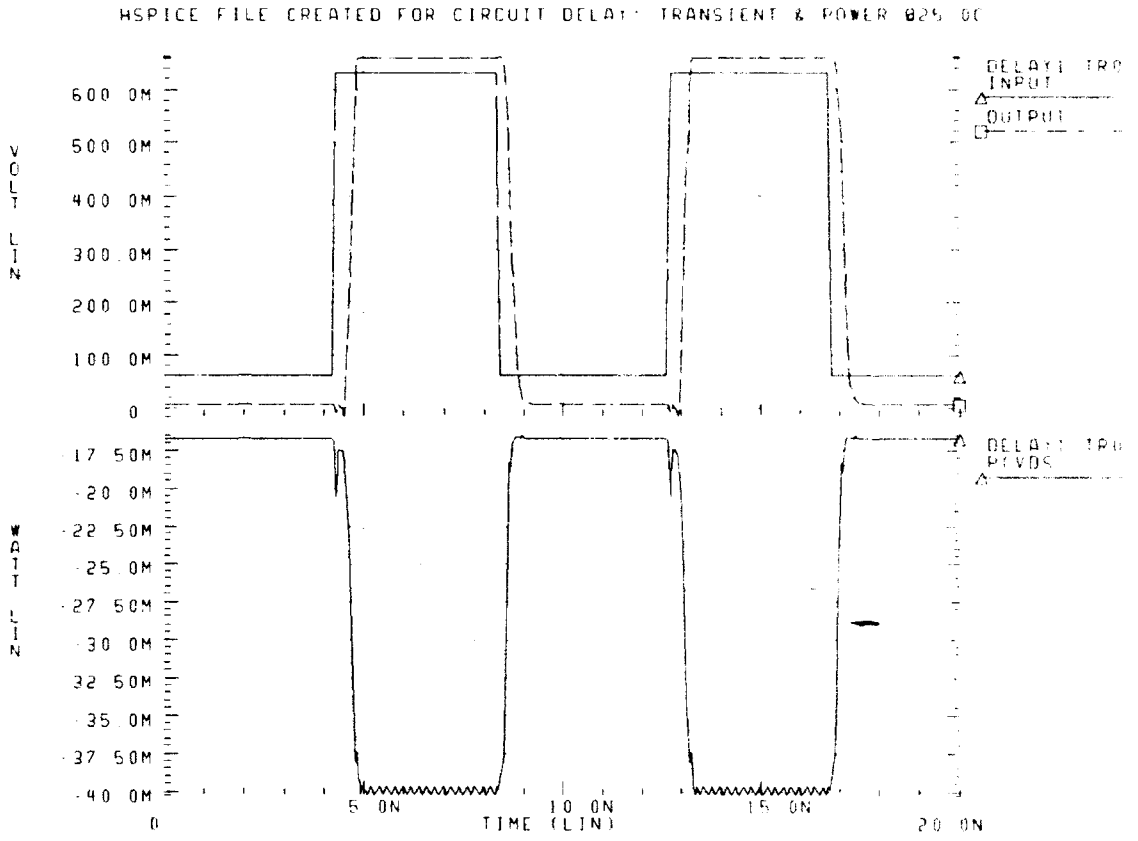


Figure 4.162 DELAY HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the DELAY operating at a temperature of 85.0C is shown in Figure 4.160 on page 149.

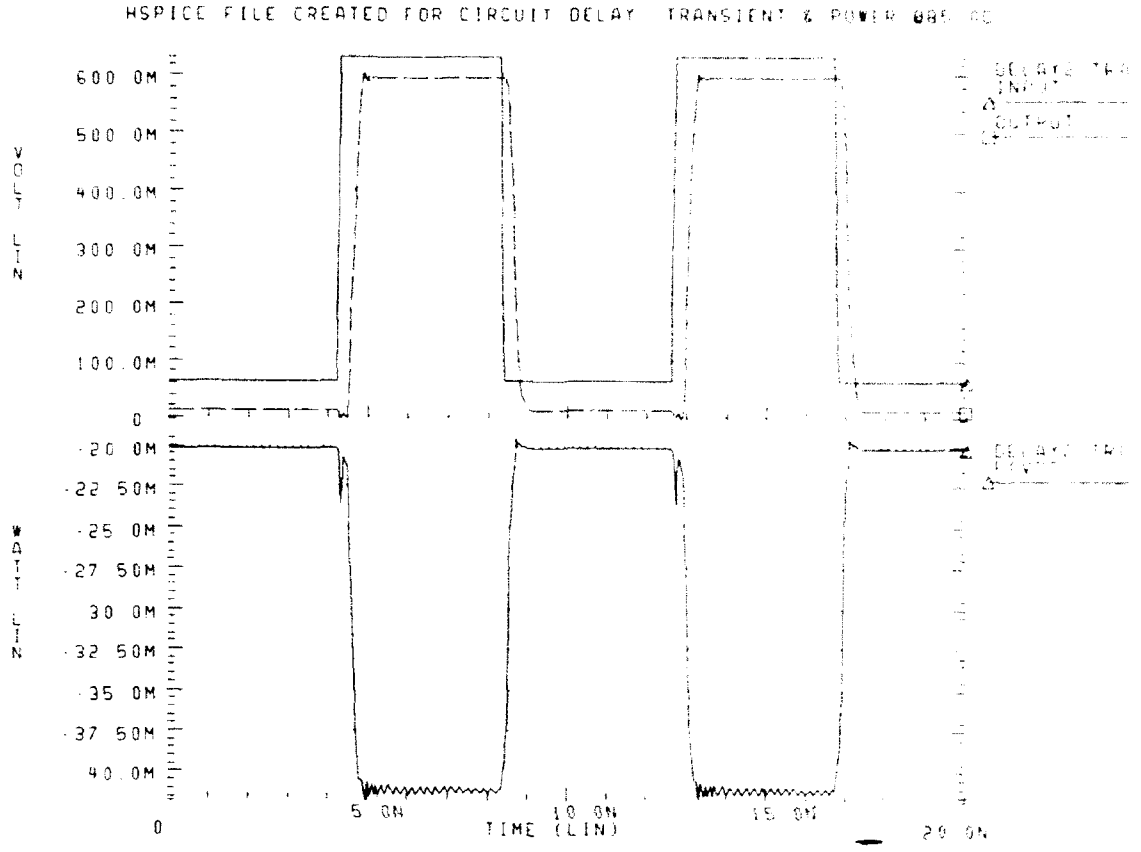


Figure 4.163 DELAY HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the DELAY logic gate operating at a temperature of 25.0C is shown in Figure 4.164 on page 152.

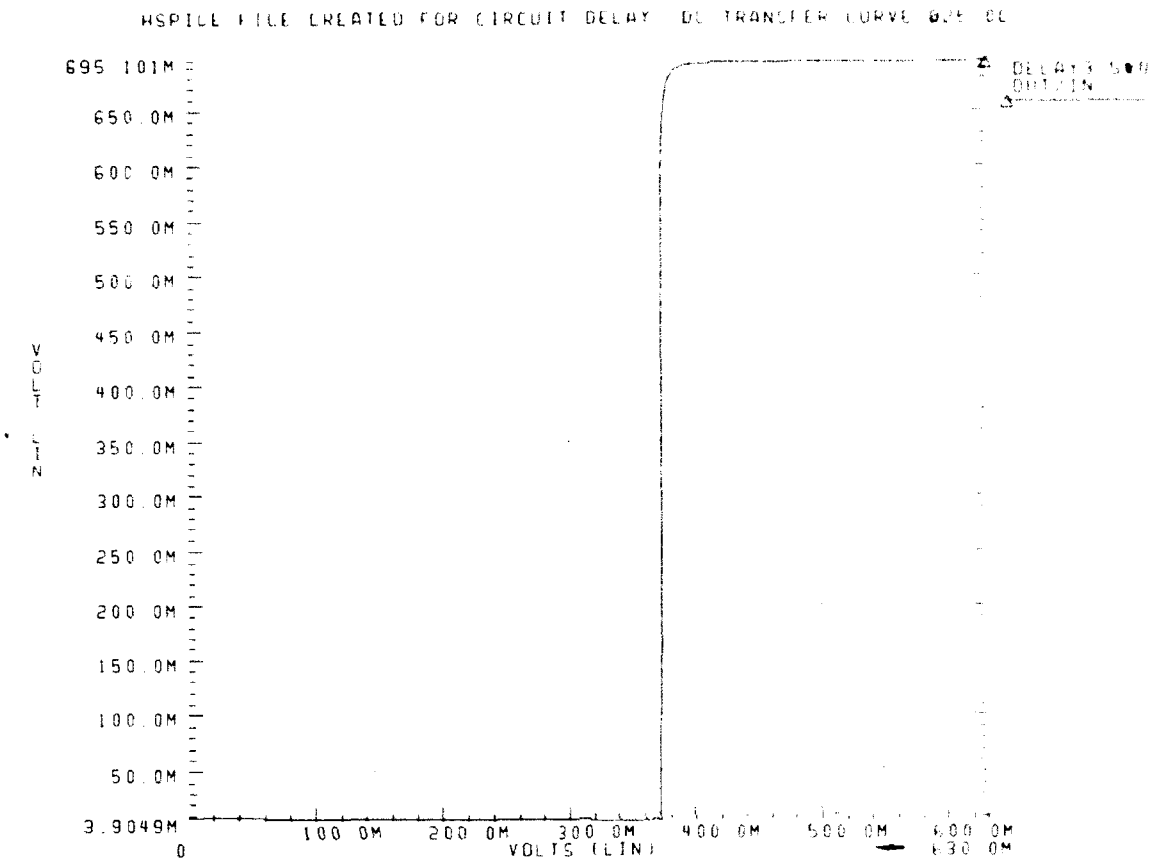


Figure 4.164 DELAY DC Transfer Curve at 25.0C

The DC transfer characteristic of the DELAY logic gate operating at a temperature of 85.0C is shown in Figure 4.165 on page 153.

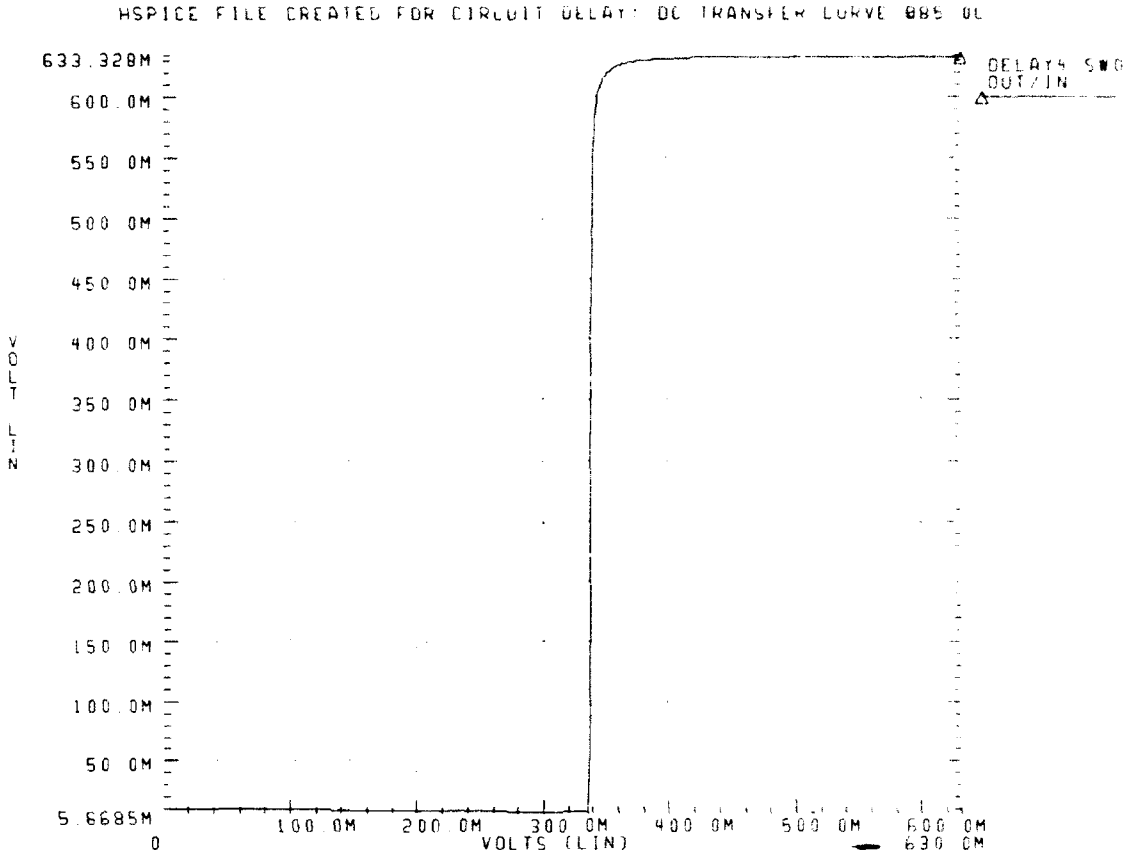


Figure 4.165 DELAY DC Transfer Curve at 85.0C

5. SBFL-DCFL Level Shifter Logic Element (LVL)

The following graphs represent the operating characteristics of the LVL. The GaAs DRAM memory array uses d-mode MESFETs as the access switches for the charge storage parallel plate capacitors. In order to directly control the d-mode MESFET transistors, a voltage level shifter is required to accept an input voltage of 0.00V to 0.63V and shifts it down to -1.20V to 0.00V. This level shifting circuit is by design an inverting circuit, thus, the DINV on its input. The diodes shown are actually GaAs e-mode MESFETs with the drain and source connected, which is referred to as "back-connected". See Figure 4.166 on page 154 for the LVL schematic and logical equivalence.

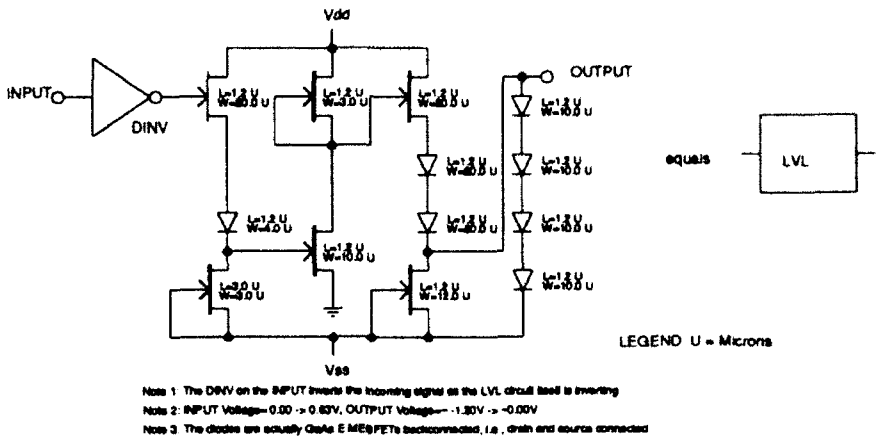


Figure 4.166 Schematic and Logical Equivalence for LVL

The transient analysis and power dissipation of the LVL operating at a temperature of 25.0C is shown in Figure 4.167 on page 155. This is the first circuit encountered that utilized a second power supply, V_{SS}. The power dissipation by both power supplies is shown in the lower graph of the indicated figure. It should be noted that this circuit was tested with a load of ten d-mode MESFETs to better simulate real circuit loading conditions. See "Listing File for LVL Transient Analysis @ 25.0C" of Appendix A on page 287.

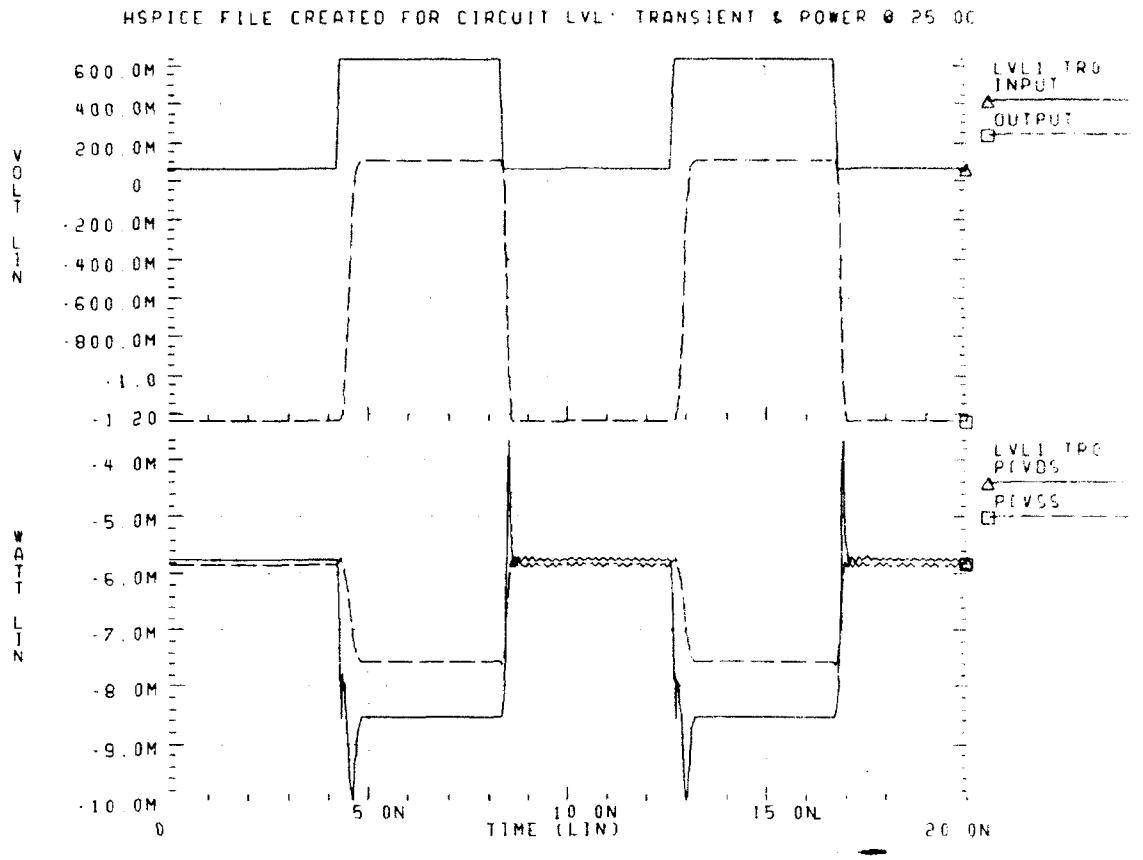


Figure 4.167 LVL HSPICE Transient Analysis and Power Dissipation at 25.0C

The transient analysis and power dissipation of the LVL operating at a temperature of 85.0C is shown in Figure 4.168 on page 156.

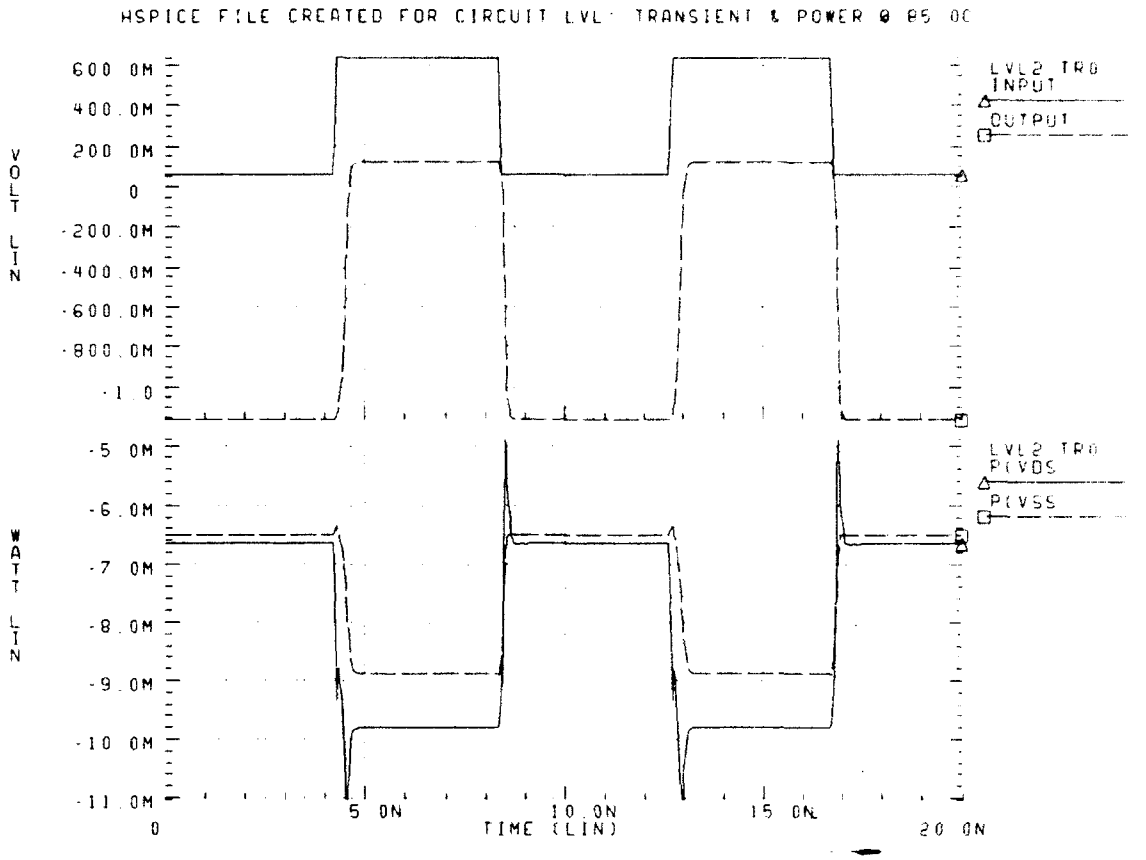


Figure 4.168 LVL HSPICE Transient Analysis and Power Dissipation at 85.0C

The DC transfer characteristic of the LVL logic gate operating at a temperature of 25.0C is shown in Figure 4.169 on page 157.

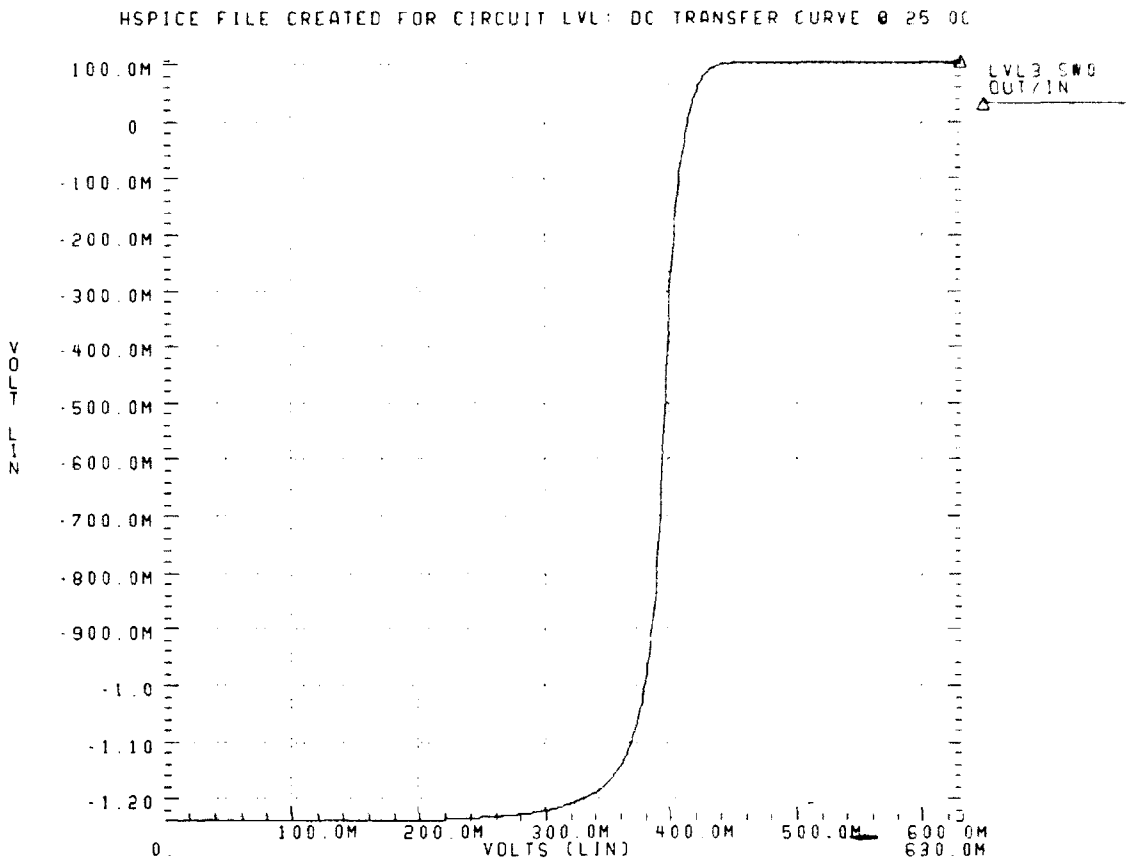


Figure 4.169 LVL DC Transfer Curve at 25.0C

The DC transfer characteristic of the LVL logic gate operating at a temperature of 85.0C is shown in Figure 4.170 on page 158.

Noise margins for the level shifter circuitry will not be discussed (or listed in TABLE 4.1) as level shifting circuitry provides no useful logic function and because level shifter circuitry usually has a linear transfer characteristic.

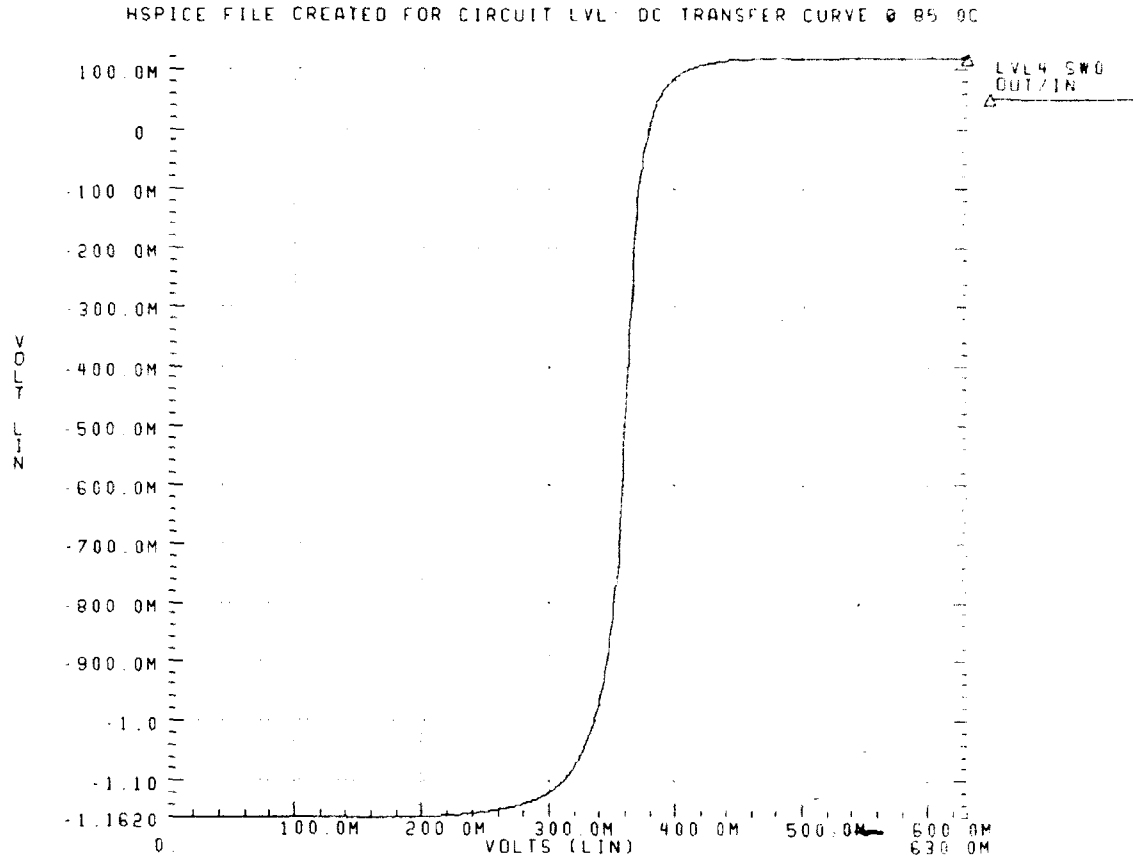


Figure 4.170 LVL DC Transfer Curve at 85.0C

D. SUMMARY

This concludes the detailed analysis of the GaAs DRAM fundamental logic elements and circuits. The characteristics of each of this circuits is found in TABLE 4.1. The next chapter will begin discussion of the major circuits of the GaAs DRAM.

TABLE 4.1 GaAs DRAM LOW-LEVEL CIRCUIT OPERATING CHARACTERISTICS

Circuit Name	tp_{HL} (ps)	tp_{LH} (ps)	t_{RISE} (ps)	t_{FALL} (ps)	t_{DELAY} (ps)	NM_L (V)	NM_H (V)
DINV @25.0C	108	71	352	130	63	0.260	0.085

TABLE 4.1 GaAs DRAM LOW-LEVEL CIRCUIT OPERATING CHARACTERISTICS

Circuit Name	t_{PHL} (ps)	t_{PLH} (ps)	t_{RISE} (ps)	t_{FALL} (ps)	t_{DELAY} (ps)	NM_L (V)	NM_H (V)
DINV @85.0C	112	58	312	146	77	0.205	0.040
D2NOR @25.0C	69	112	379	172	95	0.260	0.070
D2NOR @25.0C	65	108	347	157	117	0.205	0.065
D3NOR @25.0C	68	158	426	239	127	0.240	0.083
D3NOR @85.0C	64	148	366	240	148	0.220	0.045
D4NOR @25.0C	61	220	456	202	159	0.260	0.070
D4NOR @85.0C	58	204	399	148	187	0.210	0.060
D2NAND @25.0C	76	174	384	256	138	0.230	0.120
D2NAND @85.0C	78	146	355	402	148	0.175	0.095
DD2AND @25.0C	92	130	383	103	123	0.330	0.205
DD2NAND @25.0C	207	149	337	121	141	0.360	0.210
DD2NAND @85.0C	209	129	304	138	150	0.310	0.180
DD3NAND @25.0C	254	139	337	135	133	0.360	0.205
DD3NAND @85.0C	254	124	305	168	145	0.305	0.180
DD2AND @85.0C	84	126	350	98	133	0.275	0.160
DD3AND @25.0C	82	145	397	88	130	0.370	0.220
DD3AND @85.0C	73	140	394	103	146	0.365	0.225

TABLE 4.1 GaAs DRAM LOW-LEVEL CIRCUIT OPERATING CHARACTERISTICS

Circuit Name	t_{PHL} (ps)	t_{PLH} (ps)	t_{RISE} (ps)	t_{FALL} (ps)	t_{DELAY} (ps)	NM_L (V)	NM_H (V)
DD4AND @25.0C	76	159	418	101	139	0.360	0.225
DD4AND @85.0	66	153	416	102	160	0.325	0.190
DD2OR @25.0C	176	118	342	137	114	0.365	0.230
DD2OR @85.0C	176	111	325	156	122	0.315	0.220
DD3OR @25.0C	222	120	350	138	116	0.370	0.225
DD3OR @85.0C	221	112	369	166	123	0.300	0.210
DD4OR @25.0C	258	122	351	169	118	0.365	0.225
DD4OR @85.0C	262	132	370	203	124	0.300	0.220
BDINV @25.0C	42	95	290	68	78	0.240	0.150
BDINV @85.0C	48	71	247	64	78	0.190	0.115
DLATCH @25.0C	610	221	534	380	617	0.340	0.225
DLATCH @85.0C	631	209	512	456	595	0.295	0.190
CPDFF @25.0C	930	445	419	194	933	0.370	0.190
CPDFF @85.0C	900	425	379	216	875	0.320	0.150
SINV @25.0C	110	140	267	377	111	0.340	0.170
SINV @85.0C	103	122	261	349	122	0.290	0.130
SSINV @25.0C	18	93	123	51	56	0.320	0.270

TABLE 4.1 GaAs DRAM LOW-LEVEL CIRCUIT OPERATING CHARACTERISTICS

Circuit Name	tp_{HL} (ps)	tp_{LH} (ps)	t_{RISE} (ps)	t_{FALL} (ps)	t_{DELAY} (ps)	NM_L (V)	NM_H (V)
SSINV @85.0C	24	80	121	52	56	0.270	0.245
S2NOR @25.0C	95	231	303	632	180	0.330	0.170
S2NOR @85.0C	92	206	300	443	192	0.280	0.130
S3NOR @25.0C	79	309	367	366	228	0.325	0.165
S3NOR @85.0C	80	280	358	307	242	0.275	0.130
S4NOR @25.0C	75	371	407	383	276	0.320	0.175
S4NOR @85.0C	76	340	417	311	294	0.260	0.135
S3OR @25.0C	359	192	256	415	181	0.380	0.270
S3OR @85.0C	346	178	256	406	178	0.330	0.250
SS2NAND @25.0C	295	298	266	571	261	0.330	0.165
SS2NAND @85.0C	291	259	257	398	254	0.280	0.135
SS4NAND @25.0C	376	289	264	275	251	0.355	0.245
SS4NAND @85.0C	371	252	259	329	242	0.315	0.190
SS3AND @25.0C	153	258	323	305	235	0.375	0.245
SS3AND @85.0C	137	238	313	183	236	0.320	0.245
SS4AND @25.0C	145	286	353	255	262	0.375	0.260
SS4AND @85.0C	131	271	360	105	269	0.335	0.230

TABLE 4.1 GaAs DRAM LOW-LEVEL CIRCUIT OPERATING CHARACTERISTICS

Circuit Name	tp_{HL} (ps)	tp_{LH} (ps)	t_{RISE} (ps)	t_{FALL} (ps)	t_{DELAY} (ps)	NM_L (V)	NM_H (V)
BS2NOR @25.0C	17	229	229	65	157	0.320	0.230
BS2NOR @85.0C	25	202	214	58	159	0.260	0.195
CSINV @25.0C	24	119	160	59	79	0.330	0.240
CSINV @85.0C	30	101	154	60	78	0.280	0.210
CSNOR @25.0C	27	194	202	87	138	0.325	0.200
CSNOR @85.0C	35	170	194	73	140	0.275	0.175
BS2AND @25.0C	244	202	219	343	183	0.375	0.325
BS2AND @85.0C	199	181	198	188	172	0.340	0.300
SDLATCH @25.0C	797	370	289	490	828	0.360	0.245
SDLATCH @85.0C	773	348	281	419	774	0.330	0.205
SDFF @25.0C	1100	676	292	305	1132	0.360	0.240
SDFF @85.0C	1047	623	289	344	1051	0.325	0.210
DELAY @25.0C	431	346	255	301	415	0.375	0.320
DELAY @85.0C	387	286	259	287	381	0.355	0.285
LVL @25.0C	299	120	514	247	293	N/A	N/A
LVL @85.0C	266	115	435	294	249	N/A	N/A

V. GALLIUM ARSENIDE DRAM HIGH-LEVEL CIRCUITS

This chapter will discuss in some detail the major blocks of the highest level block diagram, see Figure 6.1 on page 218. The major circuits to be discussed in this chapter include CLOCK, DECODER, DECODDRVER, DREFRESH, WRITEP, COUNTER, OUTPUT, WLOGIC, and chip pad drivers/receivers. The GaAs DRAM memory array will be mentioned briefly and only in block diagram form (as it was the cornerstone of the work by Vagts [Ref. 8]). Each major block of the block diagram will have its own block diagram, transient analysis, power dissipation and general comments. A summary of the important circuit characteristics may be found in TABLE 5.1 on page 216.

A. Two-Phase Non-Overlapping Clock (CLOCK)

In order to operate any synchronous digital circuit, a clock of some sort is necessary. The GaAs DRAM circuit is no exception. The original form of the clock arose from the signals required to provide necessary timing for the GaAs DRAM memory array. This further lead to the creation and adaptation of the LVL and DELAY circuits. As utilized in the GaAs DRAM, this CLOCK circuit accepts a single input 50% duty cycle digital square wave of 0.06V to 0.63V and provides in outputs: phase one (PH1), phase one level shifted (PH1L), phase two (PH2), phase two delayed (PH2D), and phase two level shifted and delayed (PH2LD). The circuit requires two power supplies, V_{DD} and V_{SS}, where V_{SS} is used only for the level shifting circuitry. This circuit is one of the most tested and adjusted of all the circuits in the GaAs DRAM support circuitry as the fanout of the CLOCK is very large and clock skew under operational load was a serious concern. The power dissipation or consumption of this circuit is enormous, but, it was believed to be necessary to prevent other more serious timing anomalies. See Figure 5.1 on page 164 for a schematic and block diagram of the CLOCK circuit.

The CLOCK circuit was simulated using output loads of ten SBFL inverters and ten depletion mode MESFETs as loads for the level shifted clock outputs of PH1L and PH2LD. The simulation was executed twice, once at a nominal temperature of 25.0C and once at a nominal temperature of 85.0C. Power dissipation of these major circuits is certainly an issue and so the second (lower) (generally) graph on each will indicate the power dissipation of the circuit under test. The transient analysis and power dissipation of the CLOCK operating at a temperature of 25.0C is shown in Figure 5.2 on page 165. See "Listing File for CLOCK

Transient Analysis @ 25.0C" of Appendix A on page 290. The transient analysis and power dissipation of the CLOCK operating at a temperature of 85.0C is shown in Figure 5.3 on page 166. See TABLE 5.1 on page 216 for a summary of the CLOCK circuit operating characteristics.

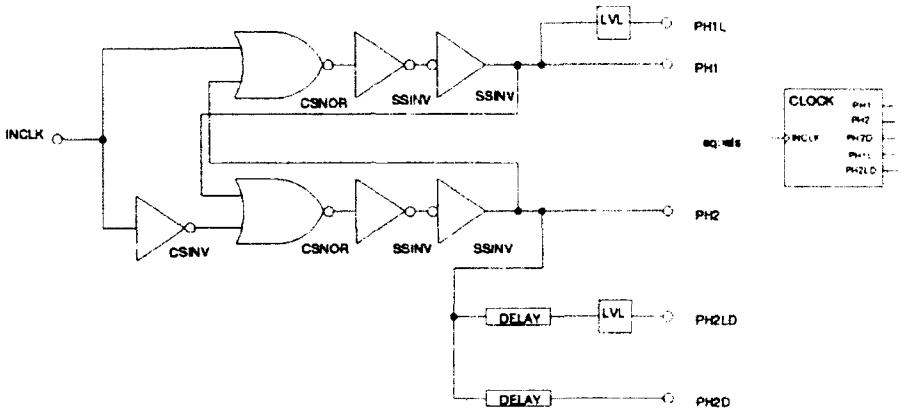


Figure 5.1 Schematic and Logical Equivalence for CLOCK

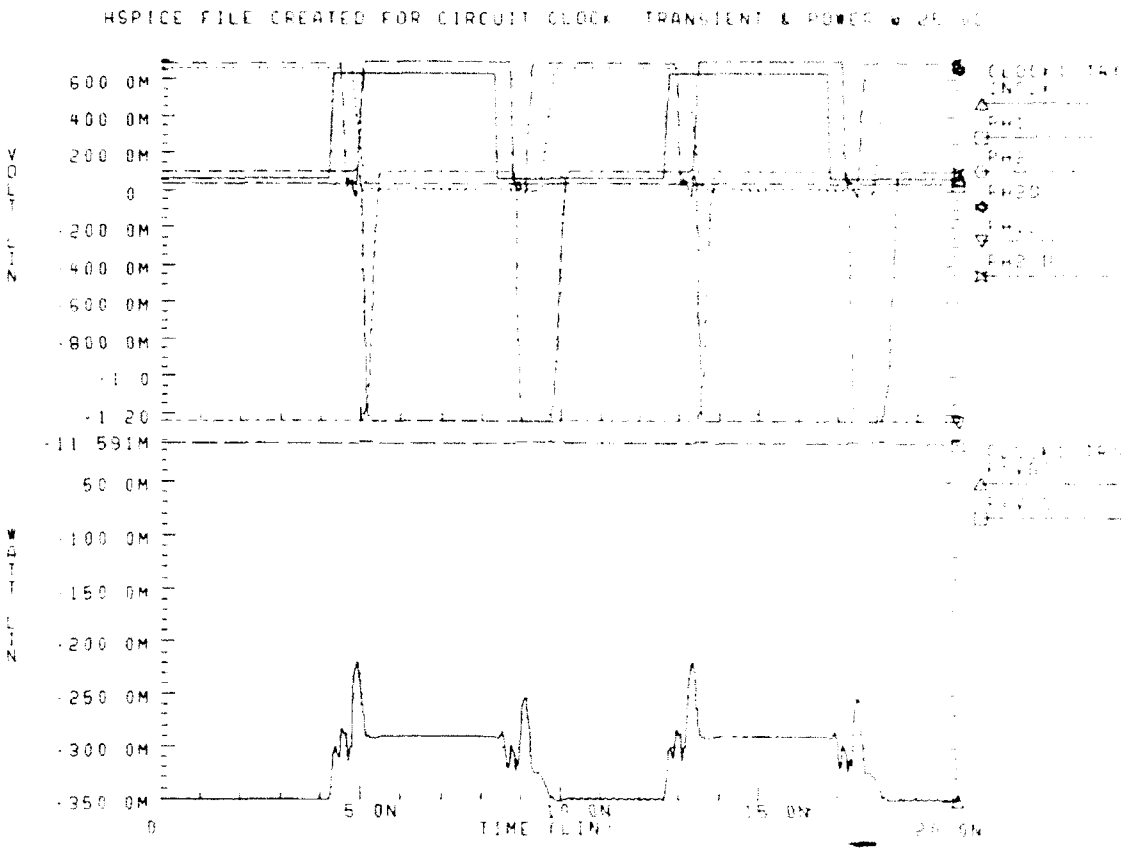


Figure 5.2 CLOCK HSPICE Transient Analysis and Power Dissipation at 25.0C

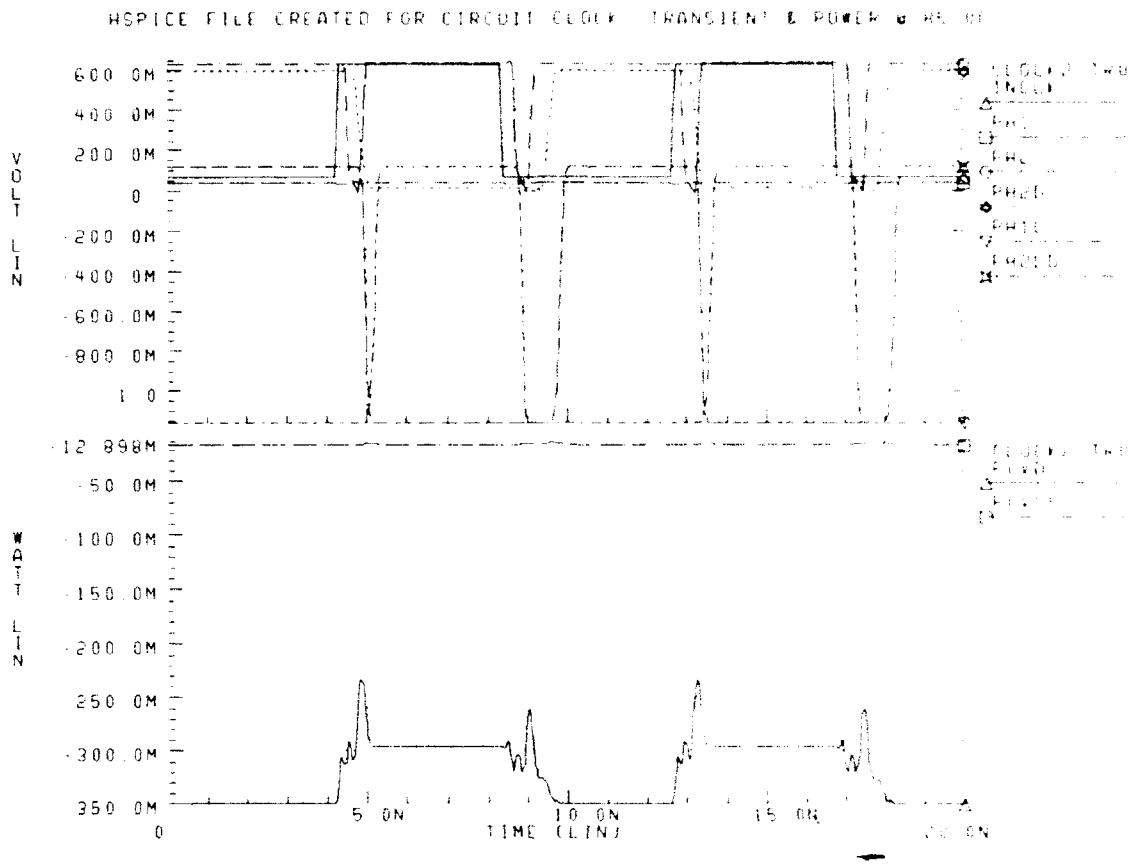


Figure 5.3 CLOCK HSPICE Transient Analysis and Power Dissipation at 85.0C

B. One-of-Eight Decoder (DECODER)

As this design is the support circuitry for an eight address by four data bit memory array, it was necessary to construct a decoder which would accept the three input address lines and decode these to one-of-eight memory array address line. The circuit DECODER is a non-clocked, non-latched glue logic decoder. It has six inputs (active HIGH), the three address lines and three enable lines, and nine outputs (active HIGH). The eight (one-of-eight) address lines and the enable line is carried through, being the OR of the three input enable lines. The DECODER circuit was constructed specially for use in a larger circuit, DECODDRVR, which will be discussed later.

As a ıe-bar, the initial DECODER design used data latches. The idea behind this was to latch the three input address lines while the decode operation occurred. It was found that the throughput of the circuit suffered to such an extent that the data latches were removed. The long data latch activation times were the reason for the degradation of the DECODER throughput, see TABLE 4.1 on page 158.

The DECODER schematic and logical representation are shown in Figure 5.4 on page 167. It can be seen in Figure 5.4 on page 167 that the ENBL signals are logically ORed such that any of the three will enable the outputs of the four-input AND gates. Notice also that the entire circuit operates using active HIGH logic, not the case in the standard transistor-transistor-logic (TTL) 74138. Ease of design dictated the use of active HIGH inputs and outputs.

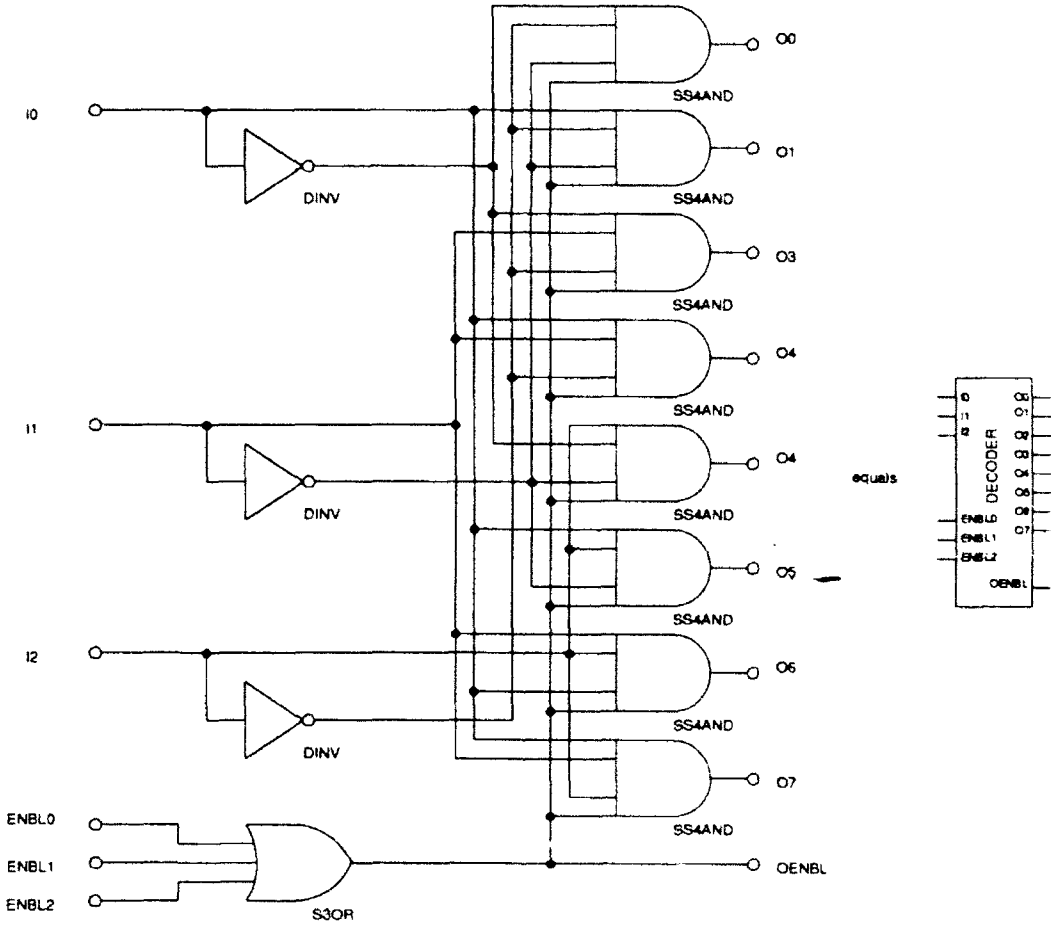


Figure 5.4 DECODER Schematic and Logical Equivalence

The transient analysis of the DECODER circuit is shown in two parts. (Additionally, the simulation was executed at the same two operating temperatures as before). Part One (upper graph), Figure 5 5 on page 168, shows the three input signals, I0, I1, and I2, and Part One (lower graph) shows the eight output signals, O0 through O7, in response to the changing input signals. The HSPICE transient analysis listing file is provided as before. See "Listing File for DECODER Transient Analysis @ 25.0C" of Appendix A on page 297.

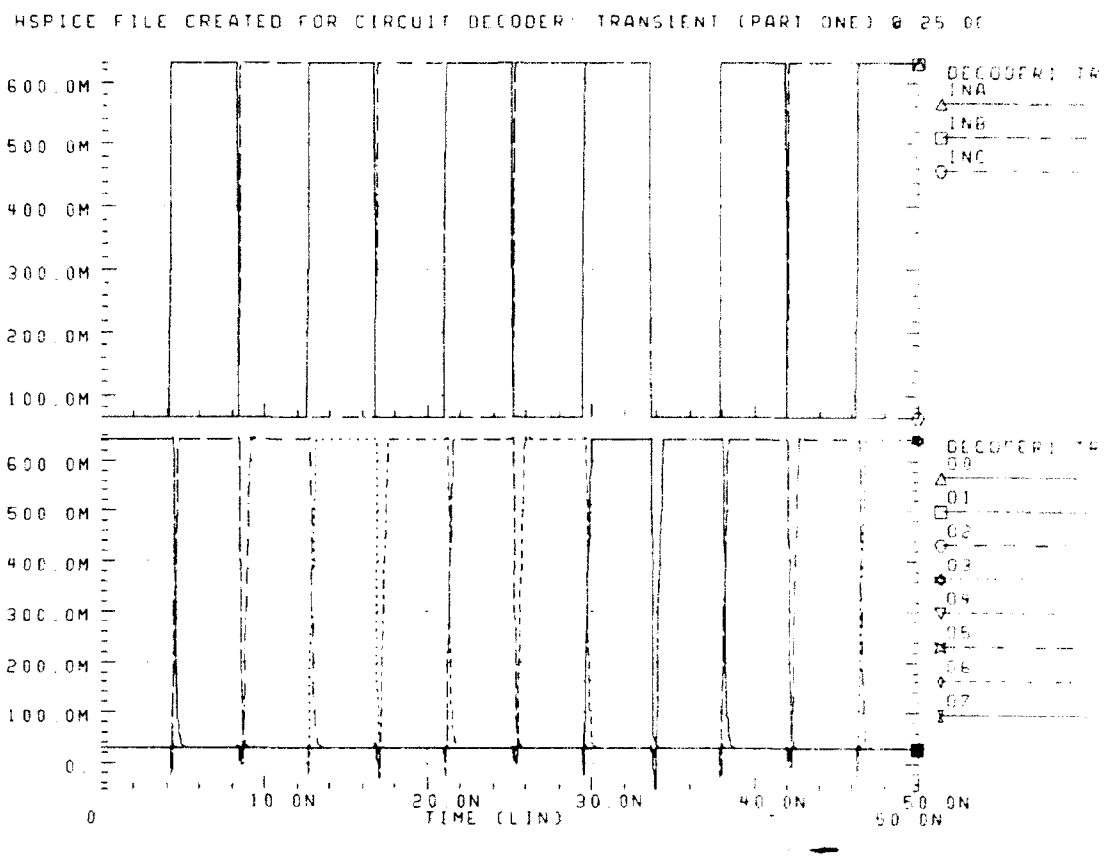


Figure 5.5 DECODER HSPICE Transient Analysis (Part One) at 25.0C

The second part of the DECODER transient analysis, Part Two, see Figure 5.6 on page 169, shows the activation and operation of the ENBL signal (upper graph) and the power dissipation of the DECODER circuit is displayed in the lower graph.

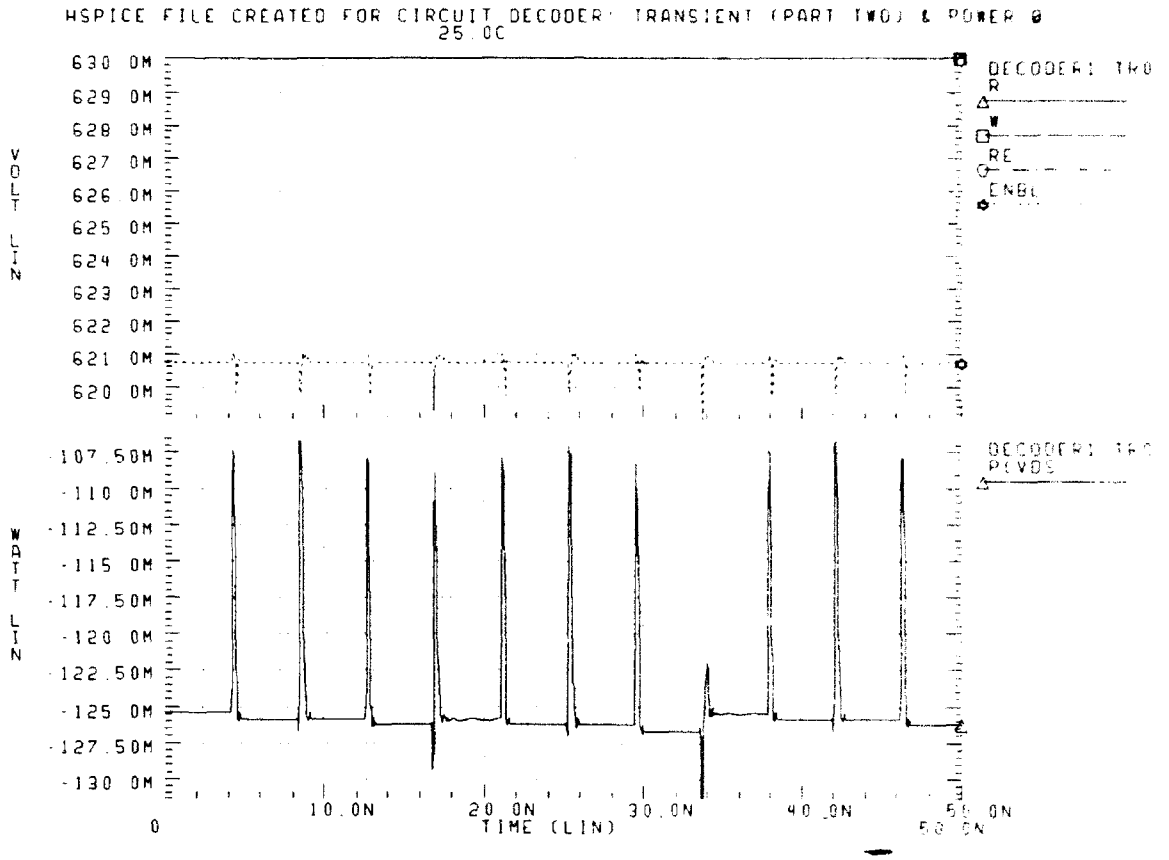


Figure 5.6 DECODER HSPICE Transient Analysis (Part Two) at 25.0C

The same signals as previously described as shown for the DECODER circuit operating at a temperature of 85.0C. See Figure 5.7 on page 170 and Figure 5.8 on page 171. The HSPICE transient analysis listing file is likewise provided.

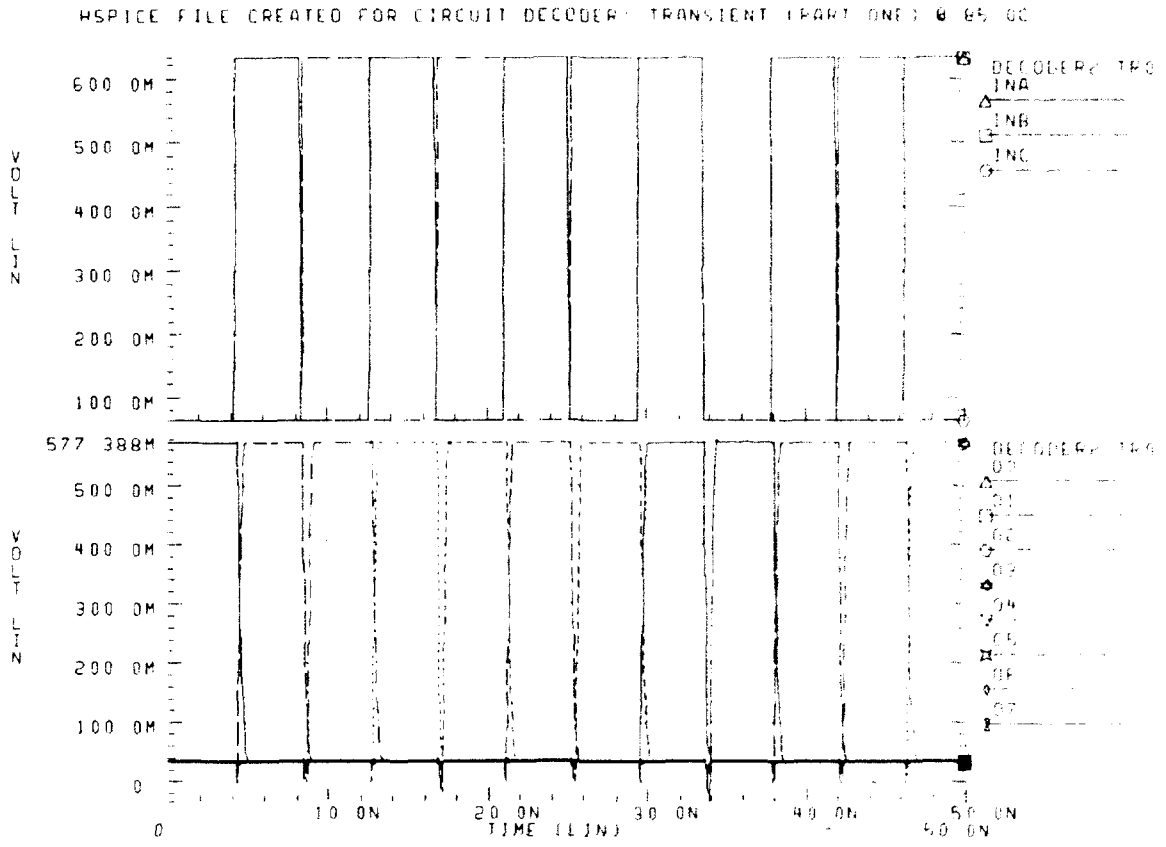


Figure 5.7 DECODER HSPICE Transient Analysis (Part One) at 85.0C

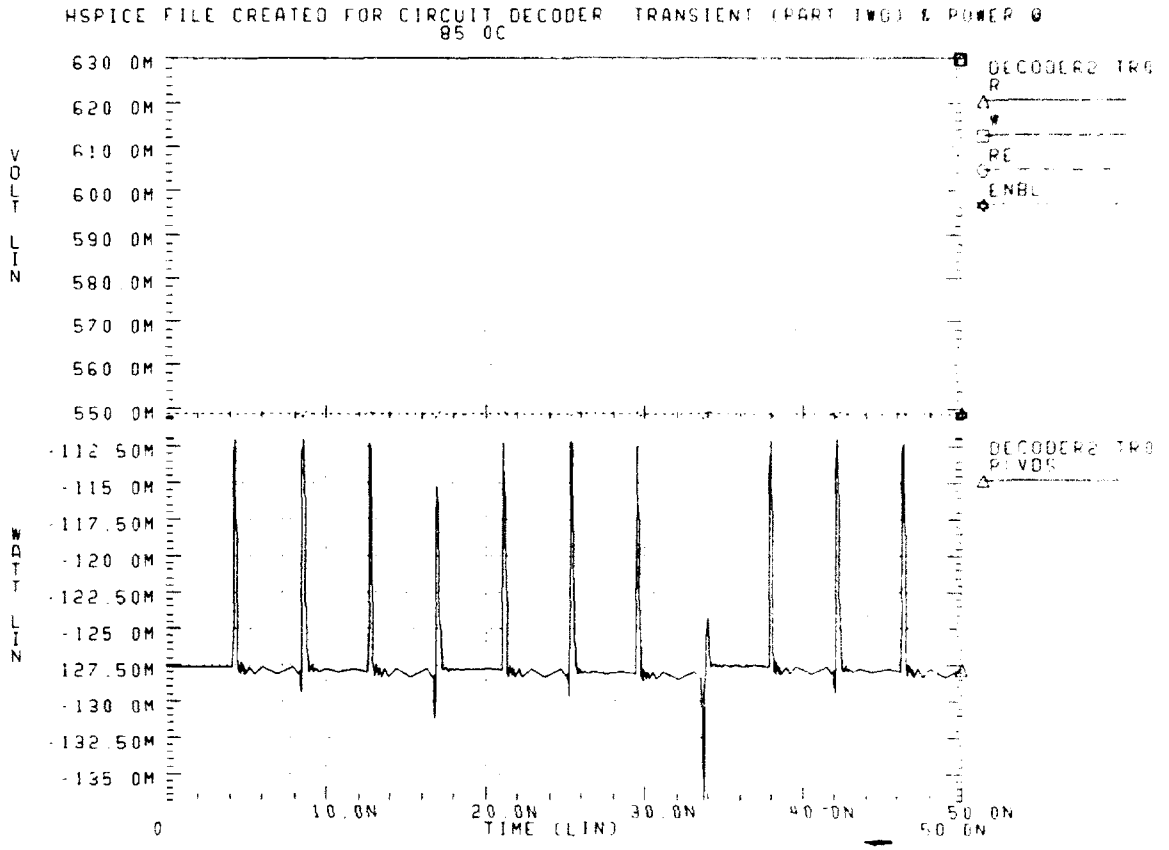


Figure 5.8 DECODER HSPICE Transient Analysis (Part Two) at 85.0C

C. Eight Stage Counter (COUNTER)

A DRAM design requires refresh operation circuitry. This COUNTER circuit is constructed in order to provide the eight counts necessary to access and refresh all eight GaAs DRAM memory array addresses. The COUNTER circuit is used inside a larger circuit entitled DREFRESH which will be covered later in this chapter. Three CPDFF flip-flops are used to maintain each of the eight states between ticks of the input clock signal. The reason for the use of the CPDFF flip-flop is its asynchronous /CLEAR signal which allows a larger circuit to force the COUNTER to a known state at any time. As a side-bar, the name "CPDFF" should really be "CDFF" as the "P" once represented an asynchronous "preset" signal which was later removed from the flip-flop design as it was not necessary to facilitate the requisite logic function.

The COUNTER circuit schematic and logical equivalence diagram is shown in Figure 5.9 on page 172.

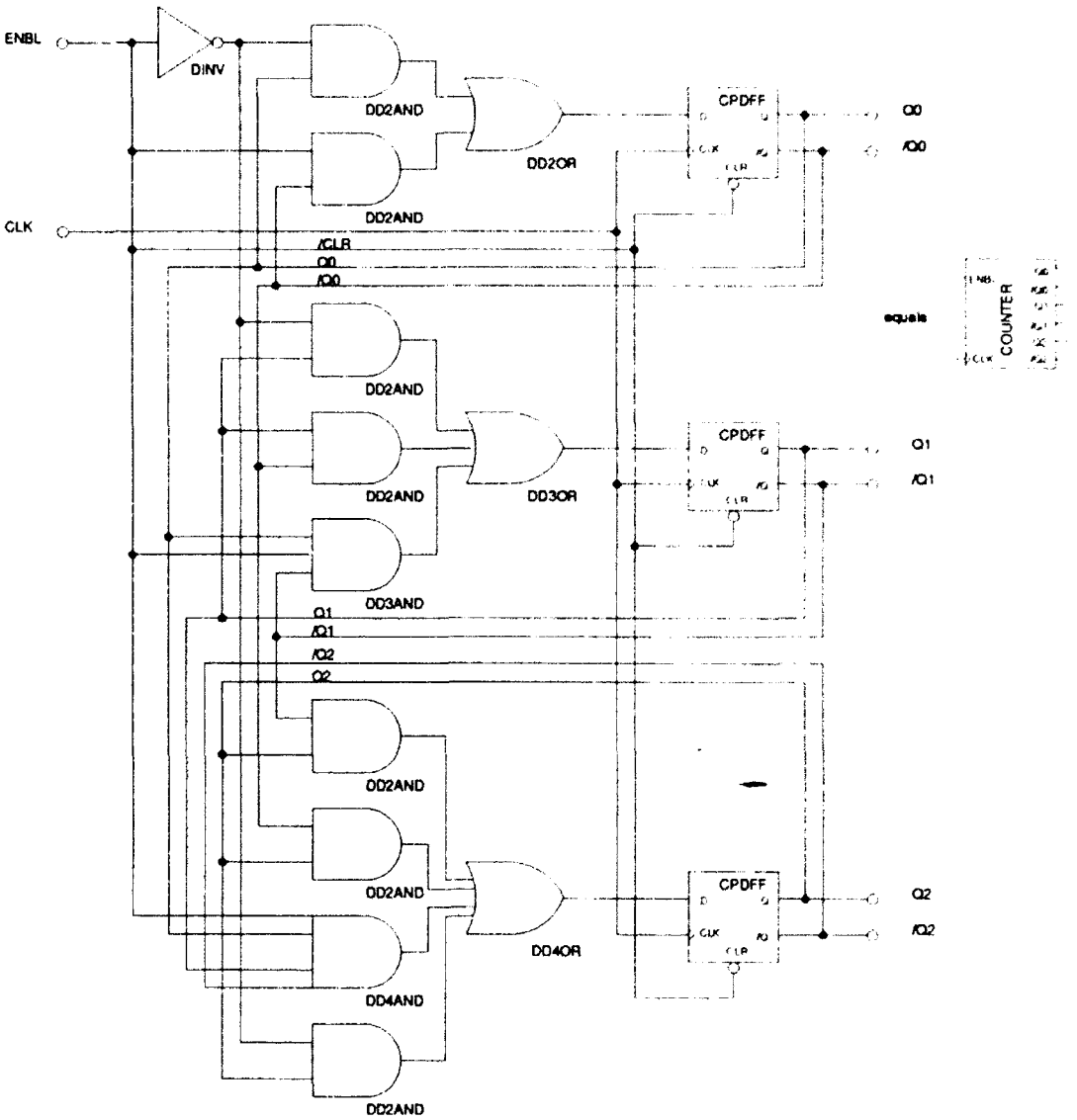


Figure 5.9 COUNTER Schematic and Logical Equivalence

It can be seen in Figure 5.9 on page 160 that the COUNTER circuit is constructed primarily from DCFL glue logic wired such to cause a count of 000 to 111. When the counter is disabled by de-assertion of the ENBL signal (or conversely, assertion of the /CLEAR signal), the COUNTER circuit will output assert /Q0, /Q1, and /Q2 or a positive logic equivalence of 000 for the count. It is interesting to note that because of the

initialization techniques of HSPICE, the COUNTER subcircuit will not begin counting at 000 as it is held in this state by use of the ".IC" statement. Hence, the first count out of the COUNTER is 001. One may see the use of this initial conditions card in the listing file for the transient analysis of the DREFRESH circuit.

The maximum operating frequency of this COUNTER is determined by the DCFL glue logic gate delays but especially, the switching speed of the three counting flip-flops. An interested reader may review the operating characteristics of the DCFL glue logic gates used in the COUNTER circuit by reviewing TABLE 4.1.

The HSPICE transient analysis of the COUNTER circuit may be seen in Figure 5.10 on page 173.

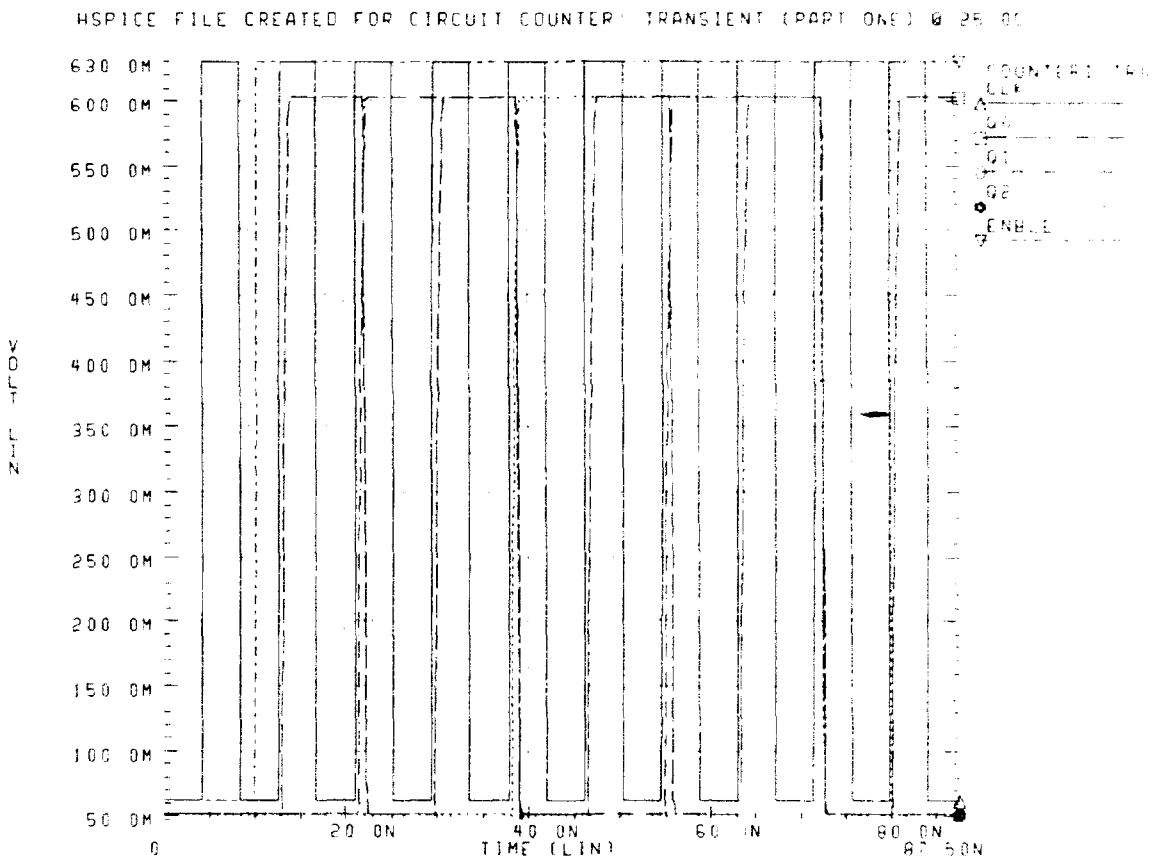


Figure 5.10 COUNTER HSPICE Transient Analysis (Part One) at 25.0C

Figure 5.10 on page 173 shows the first graph associated with the transient analysis of the COUNTER circuit. It contains the input clock signal (CLK), the input enable signal (ENBLE), and provides the "Q" outputs of the three aforementioned counting flip-flops. Standard DCFL loads of two DINVs were placed on

each "Q" output to represent realistic loading conditions. One can see from Figure 5.10 on page 173 that the counter begins counting at "001" which occurs for the HSPICE simulator initialization reasons mentioned earlier. The second part of the HSPICE transient analysis of the COUNTER circuit may be seen in Figure 5.11 on page 174.

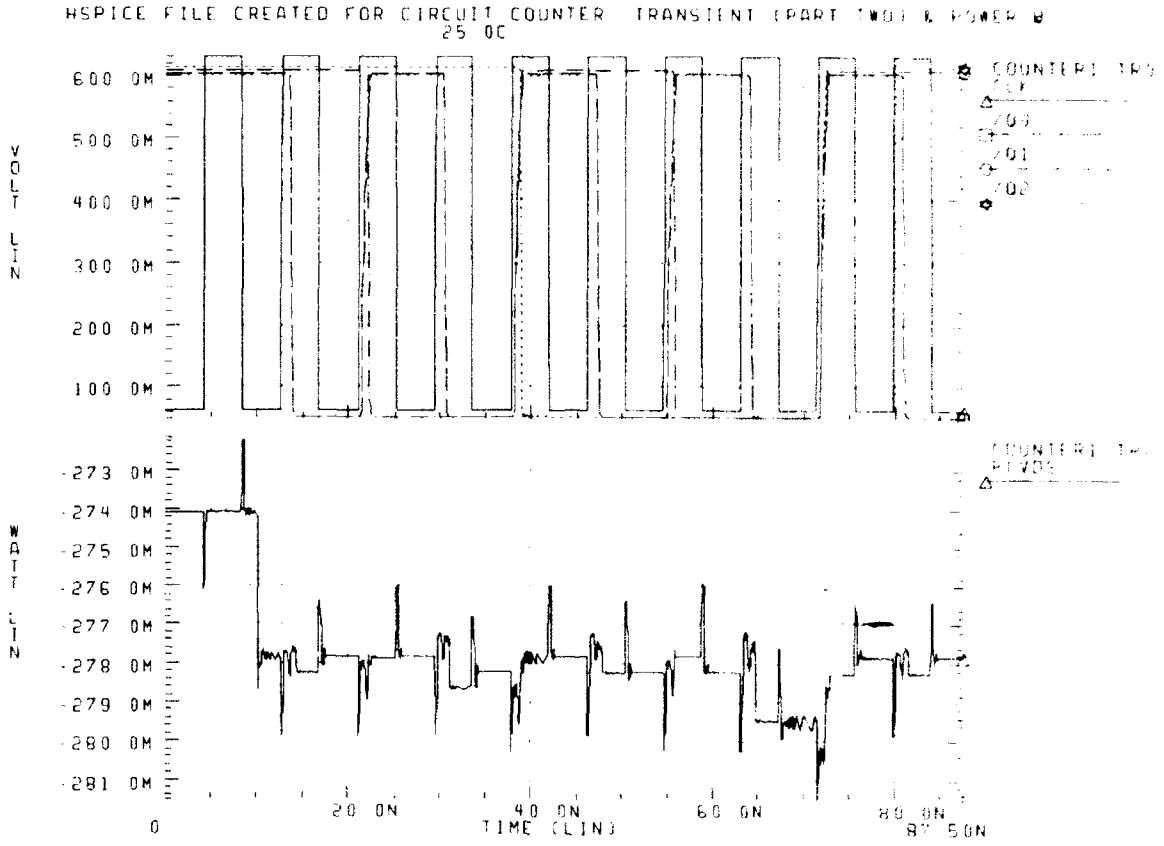


Figure 5.11 COUNTER HSPICE Transient Analysis (Part Two) & Power at 25.0C

Figure 5.11 on page 174 is derived from the same single simulator run as the previous graph. It was believed to be easier to see the results if the graph was not cluttered with too many plots. Figure 5.11 shows the "/Q" output signals in the upper graph superimposed with the exact same input clock signal (CLK). It may be seen in Figure 5.11 that the "/Q" output signals act as expected as logical inverse signals of the "Q" output signals seen in the first part of the transient analysis of the COUNTER circuit as shown in Figure 5.10 on page 173. The lower graph of Figure 5.11 indicates the power dissipation of the COUNTER circuit as it counts

through all possible states. See "Listing File for COUNTER Transient Analysis @ 25.0C" of Appendix A on page 305.

The COUNTER circuit was also simulated under the same operating conditions except the nominal temperature was increased from 25.0C to 85.0C. See Figure 5.12 on page 175 and Figure 5.13 on page 176.

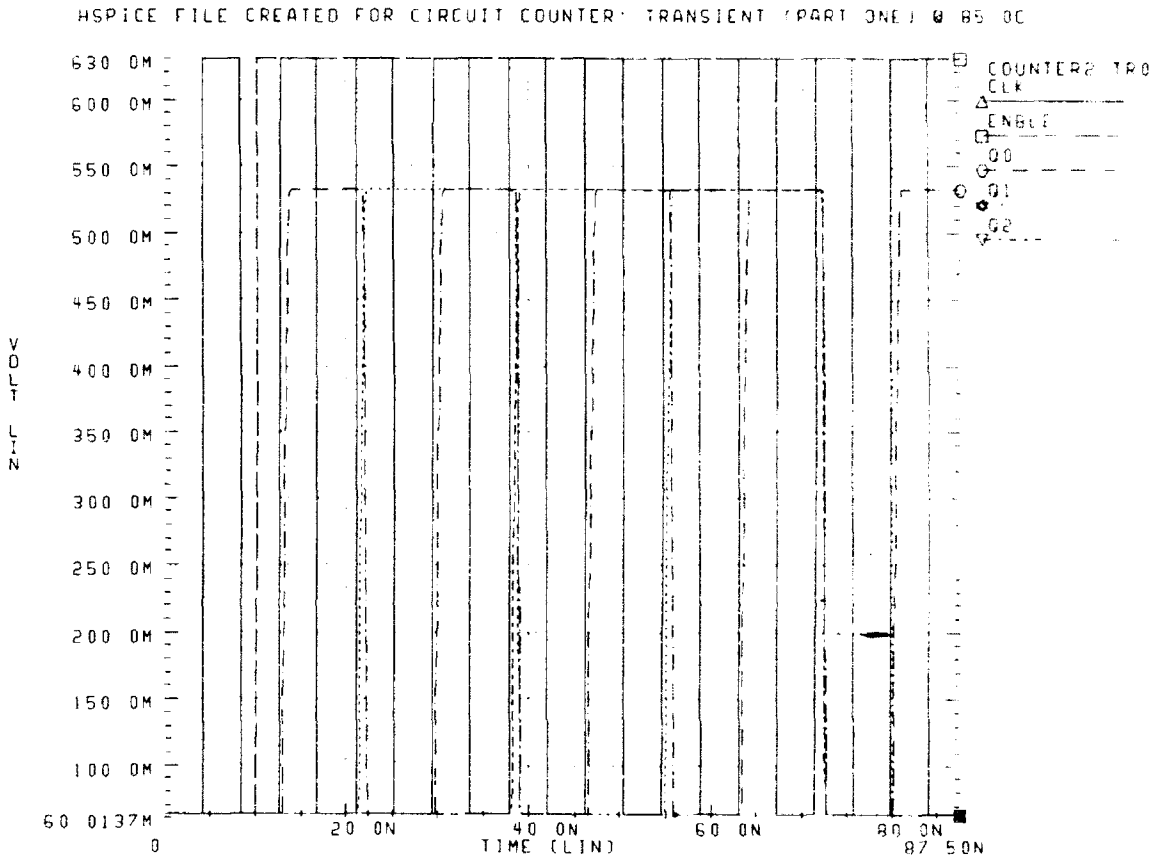


Figure 5.12 COUNTER HSPICE Transient Analysis (Part One) at 85.0C

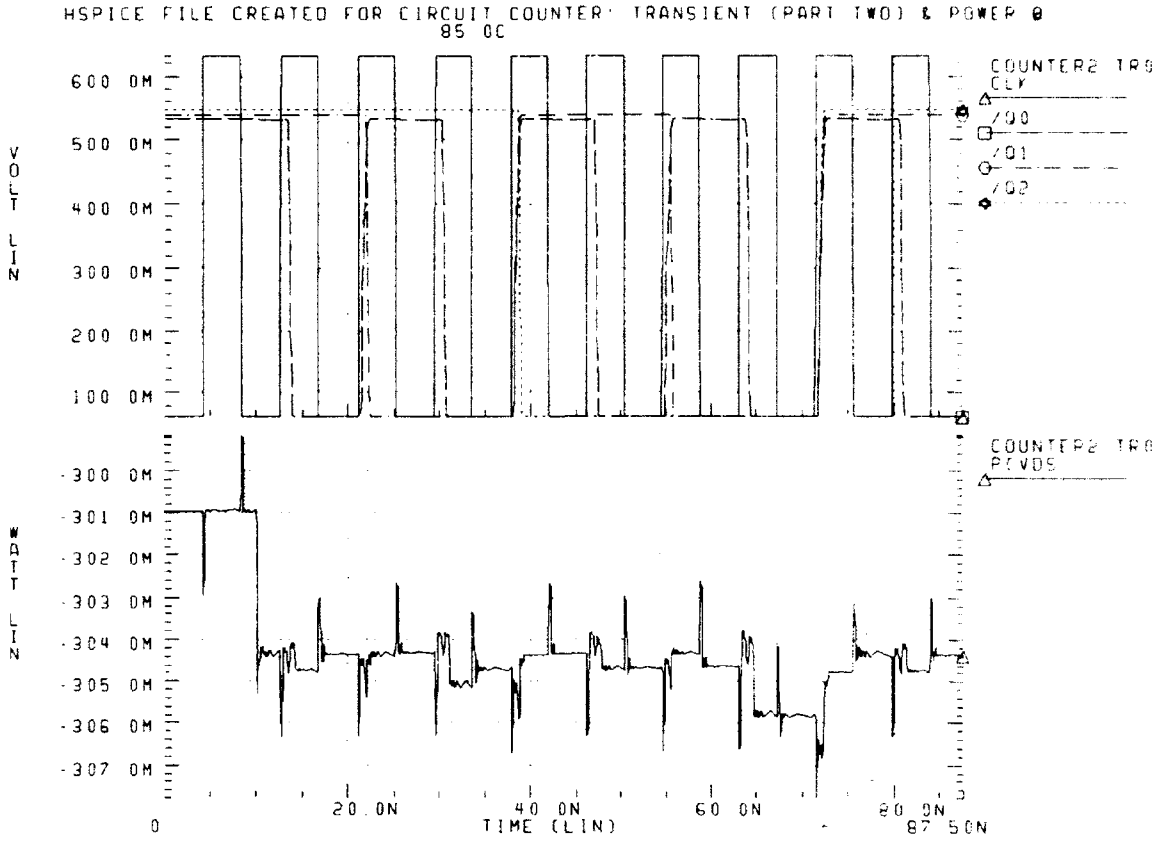


Figure 5.13 COUNTER HSPICE Transient Analysis (Part Two) & $\overline{\text{Power}}$ at 85.0C

D. DRAM Refresh Circuitry (DREFRESH)

A dynamic RAM requires periodic recharging of the storage element charges, else the charges leak away. The DREFRESH circuit provides the necessary logic function to control the refresh operation for the GaAs DRAM memory array. See Figure 5.14 on page 177 for the DREFRESH schematic and logical equivalence.

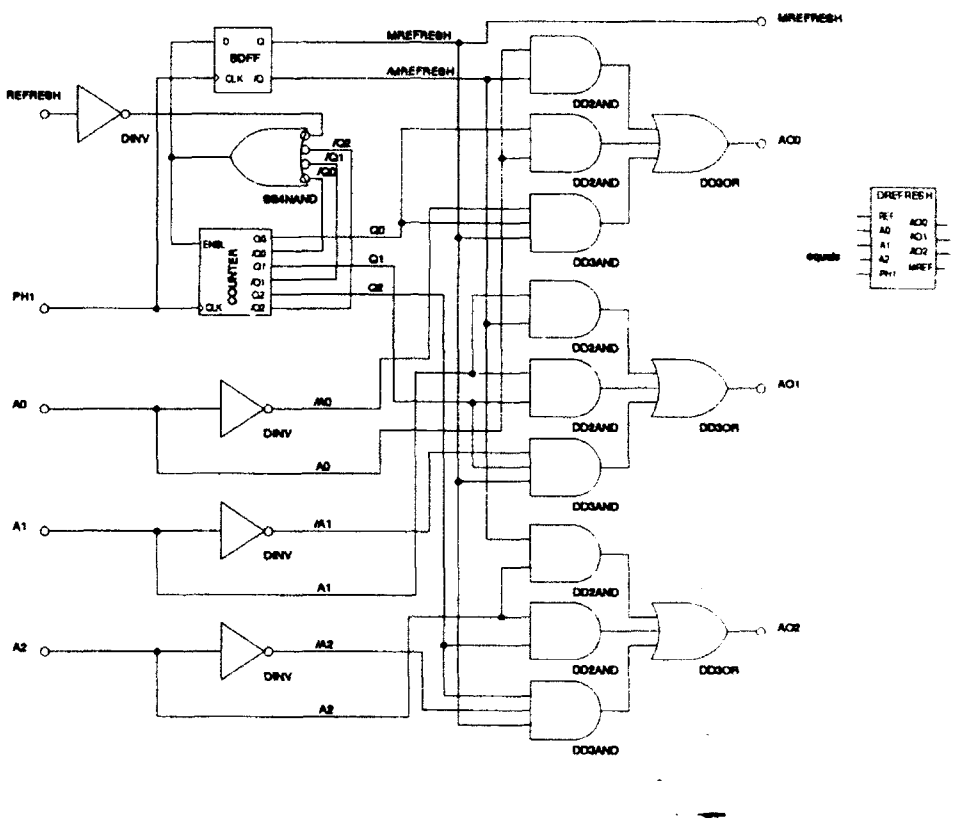


Figure 5.14 DREFRESH Schematic and Logical Equivalence

In words, the purpose of this circuit is to monitor the REFRESH signal and be prepared to act upon its assertion when ANDed with a PH1 clock pulse. When the DREFRESH circuit detects the assertion of the external REFRESH signal, it is designed to detect the "level" of the REFRESH signal and cause the SDFF to be set asserting MREFRESH to the rest of the GaAs DRAM memory array circuitry. This MREFRESH signal (occasionally abbreviated "MREF"), among other actions, asserts the memory busy signal, MBSY, to the rest of the GaAs DRAM memory array circuitry and off-chip and overrides the assertion of the READ or WRITE signal (the WRITEP circuit performs this function, it will be discussed later).

It was previously mentioned that the COUNTER circuit simulation required the use of the HSPICE ".IC" statement in order to force the circuit into a known state. One can see that if the circuit simulator HSPICE initializes the COUNTER to some arbitrary value (not 000, e.g., Q0=LOW, Q1=LOW, Q2=LOW, /Q0=HIGH, /Q1=HIGH, and /Q2=HIGH) then on the next PH1 clock pulse, the SDFF will see a HIGH on its D input and be set indicating MREFRESH by the next PH1 clock pulse falling edge. Additionally, the same

PH1 clock pulse will cause the COUNTER to count further into the REFRESH cycle. Now, this is an anomaly of the HSPICE simulation initialization routine, but, the first time, each time, this GaAs DRAM circuit is powered up, the COUNTER will come up in some unknown state and count through until the last refresh state and then the COUNTER and DREFRESH will enter a known state.

The second major function of this circuit is to choose between passing through the off-chip input address lines (A2 to A0) to the DREFRESH output address lines (AO2 to AO0) or passing through the addresses generated by the refresh sub-portion of the DREFRESH circuit.

As previously mentioned, the SDFF flip-flop will be set upon the assertion of the REFRESH signal ANDed with the COUNTER being at "000" and the next PH1 clock pulse, and the DREFRESH circuit will enter into a refresh operation. During the refresh operation, the external address signal inputs, A2 to A0, will be ignored and the address signals generated by the refresh circuitry will be passed through to the DREFRESH output address lines (AO2 to AO0) thereby causing the eight addresses of the GaAs DRAM memory array to be sequentially READ which is sufficient to refresh each storage element charge. For additional detailed information regarding the refresh of the individual charges, see the excellent and through work of Wagts [Ref. 8:pp. 20-22]. In the interest of brevity and by virtue of the DREFRESH circuit simplicity, the design state diagrams and Karnaugh mappings are not shown.

The DREFRESH transient analysis is demonstrated in the next eight graphs. As before, the graphs are kept to a few signals each to facilitate easier understanding. It is interesting to note that in order to better simulate DREFRESH reality, the GaAs DRAM memory array CLOCK circuit was included in the HSPICE file and used to generate the DREFRESH input clock signal, PH1. See "Listing File for DREFRESH Transient Analysis @ 25.0C" of Appendix A on page 315.

The first graph, see Figure 5.15 on page 179, shows the plot of the input clock signal, PH1, and the assertion of the external REFRESH signal and the resulting assertion of the MREFRESH signal upon the first edge of the PH1 signal.

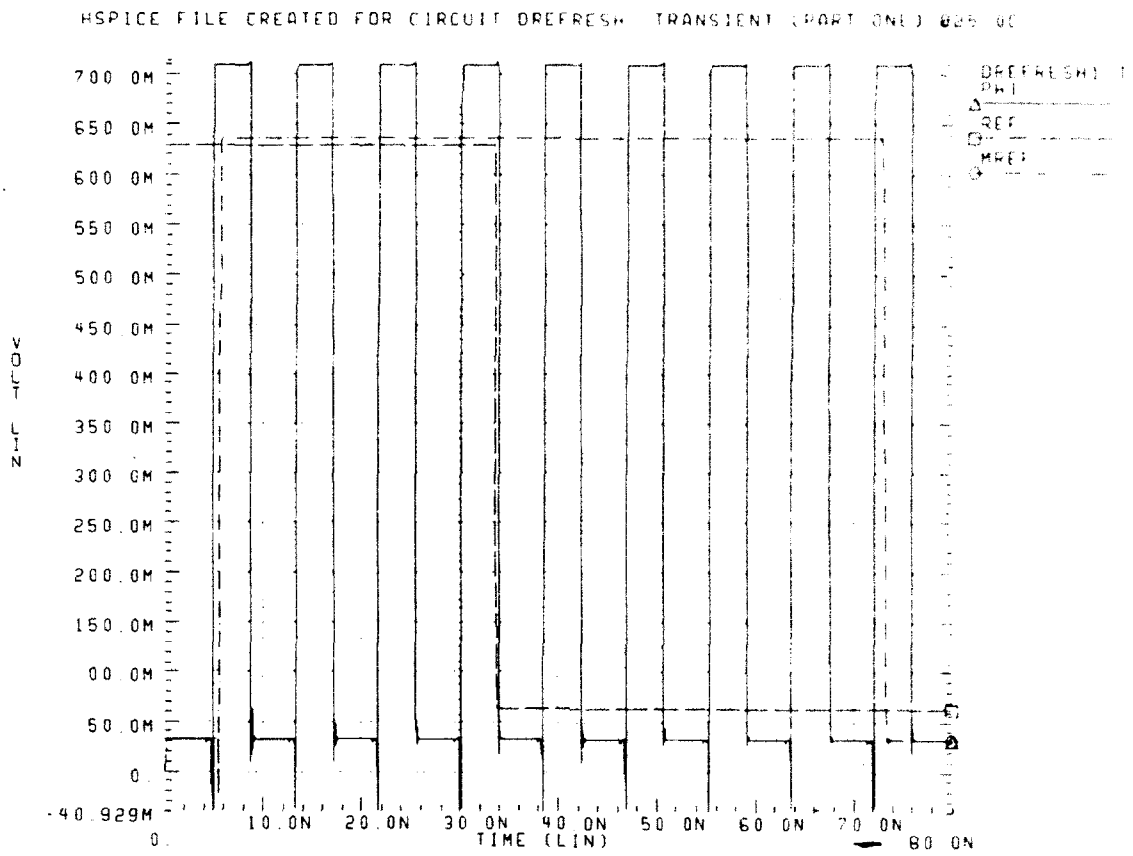


Figure 5.15 DREFRESH HSPICE Transient Analysis (Part One) at 25.0C

The next DREFRESH transient analysis graph, see Figure 5.16 on page 180, shows the CLOCK input signal, PH1, and the external input address lines, A2 to A0. It can be seen that the external input address lines are counting through the eight possible addresses.

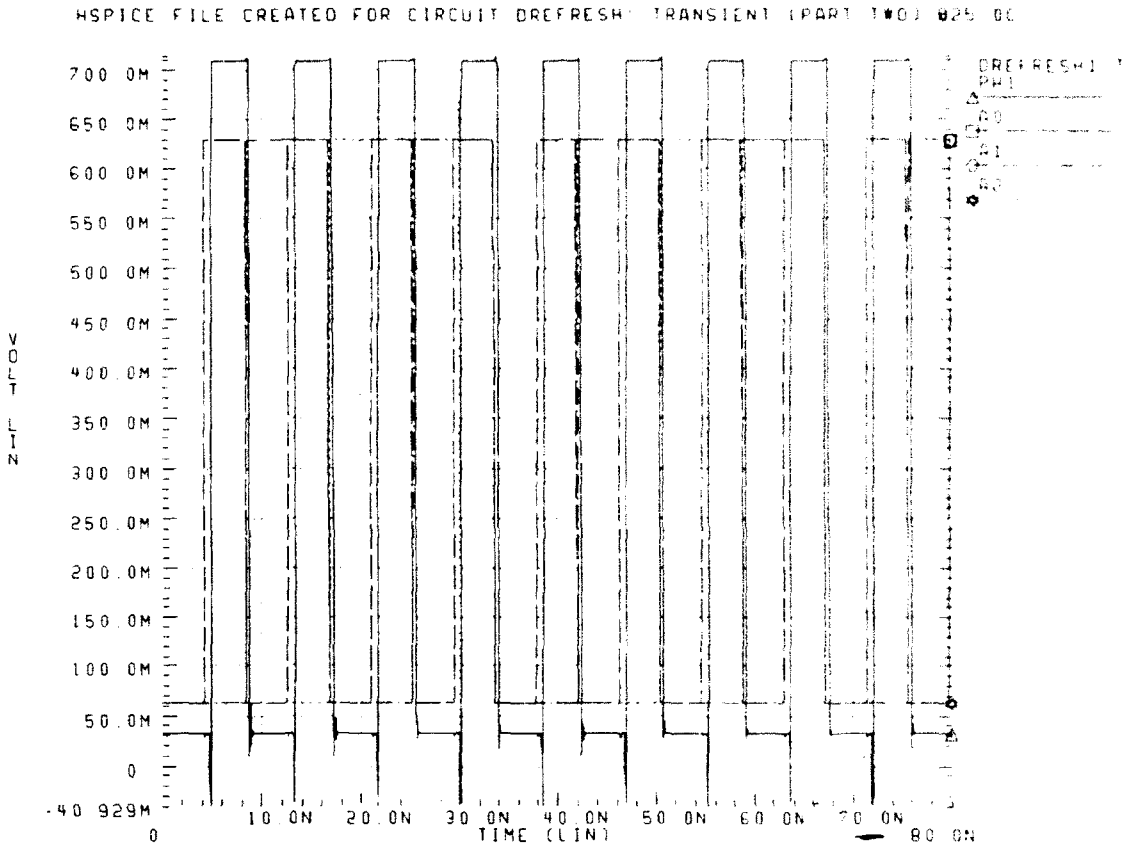


Figure 5.16 DREFRESH HSPICE Transient Analysis (Part Two) at 25.0C

The next DREFRESH transient analysis graph, see Figure 5.17 on page 181, shows the CLOCK input signal, PH1, the MREFRESH signal, and the DREFRESH output address lines, AO2 to AO0. It can be seen that the DREFRESH output address lines are counting through the eight possible addresses. Notice that the MREFRESH signal is de-asserted upon completion of the final GaAs DRAM memory array address refresh.

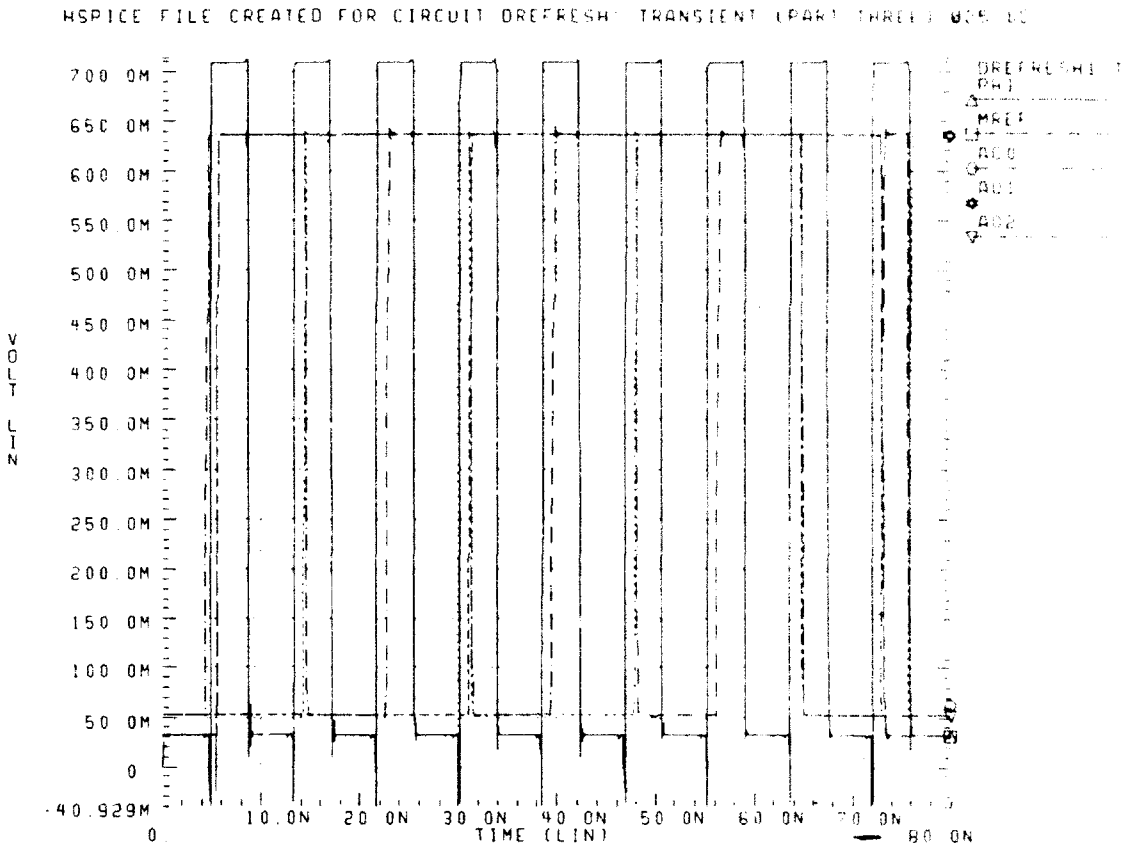


Figure 5.17 DREFRESH HSPICE Transient Analysis (Part Three) at 25.0C

The next DREFRESH transient analysis graph, see Figure 5.18 on page 182, shows the power dissipation.

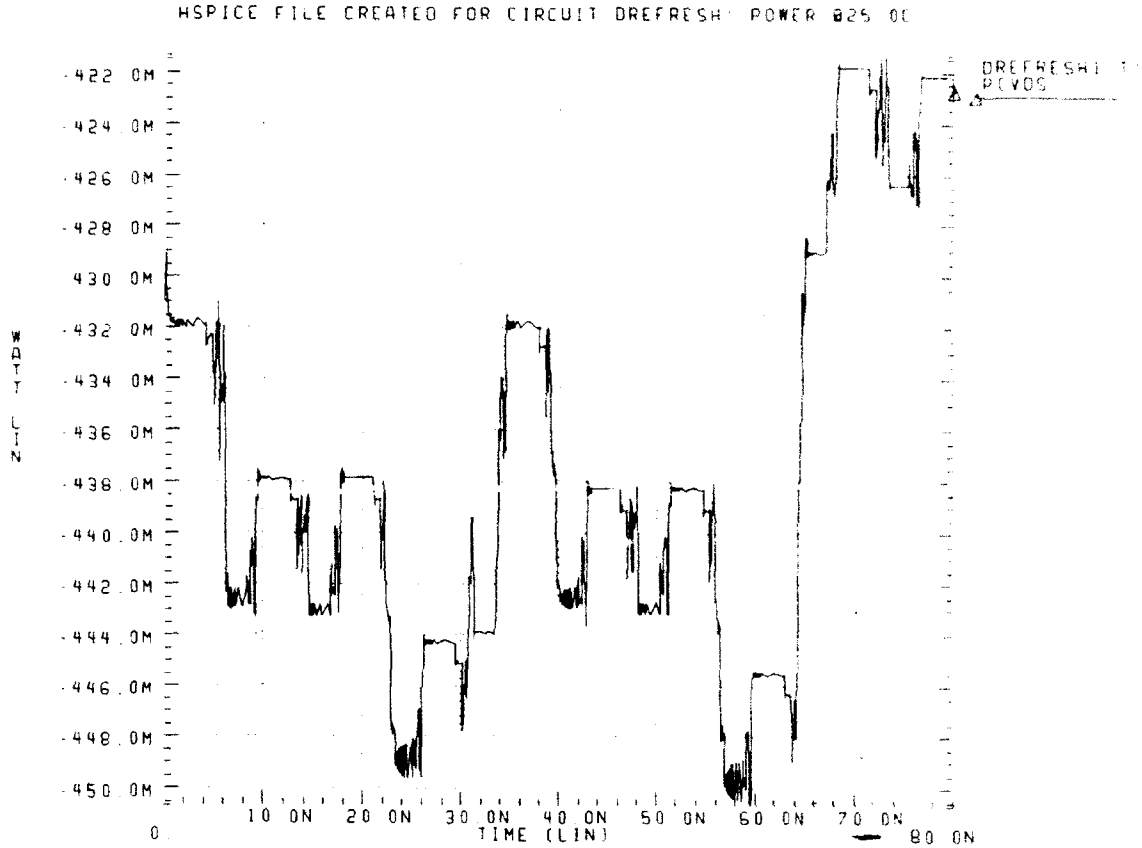


Figure 5.18 DREFRESH HSPICE POWER at 25.0C

The following four DREFRESH graphs show the same signals as discussed in the preceding paragraphs, but, using a simulation nominal temperature of 85.0C. See Figure 5.19 on page 183, Figure 5.20 on page 184, Figure 5.21 on page 185, and Figure 5.22 on page 186.

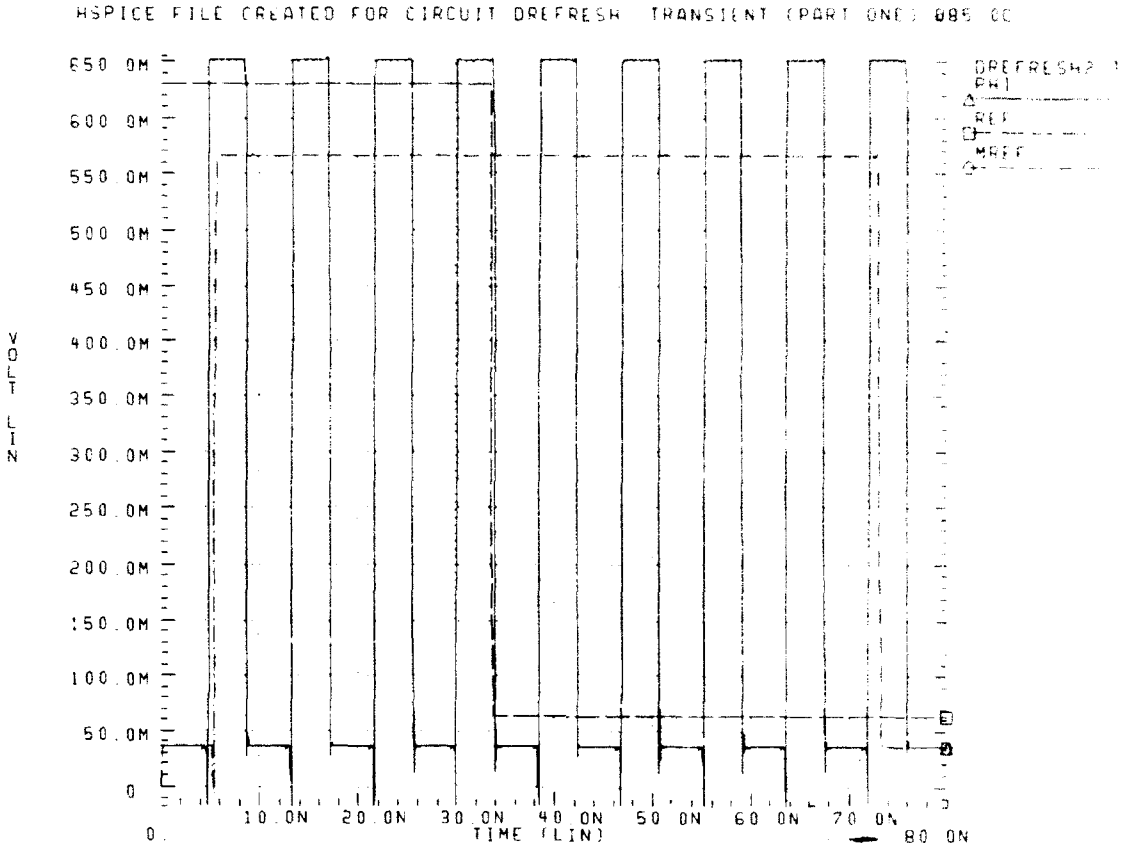


Figure 5.19 DREFRESH HSPICE Transient Analysis (Part One) at 85.0C

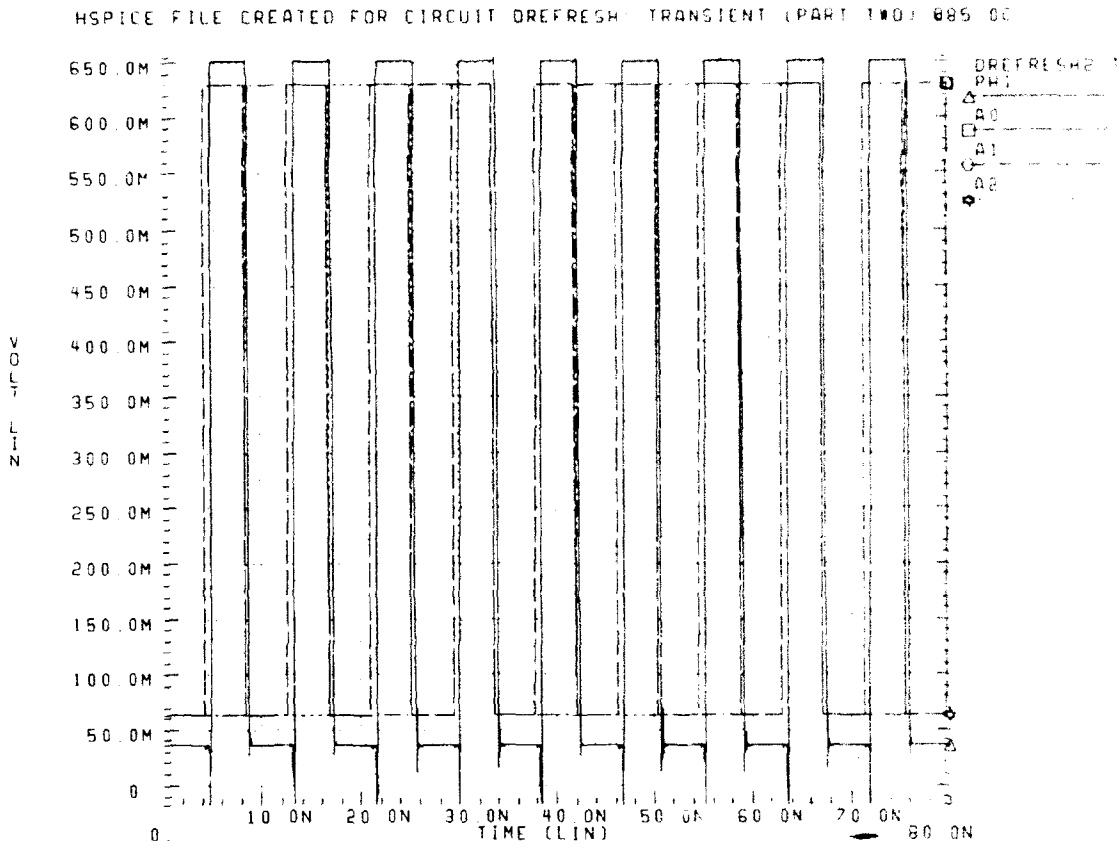


Figure 5.20 DREFRESH HSPICE Transient Analysis (Part Two) at 85.0C

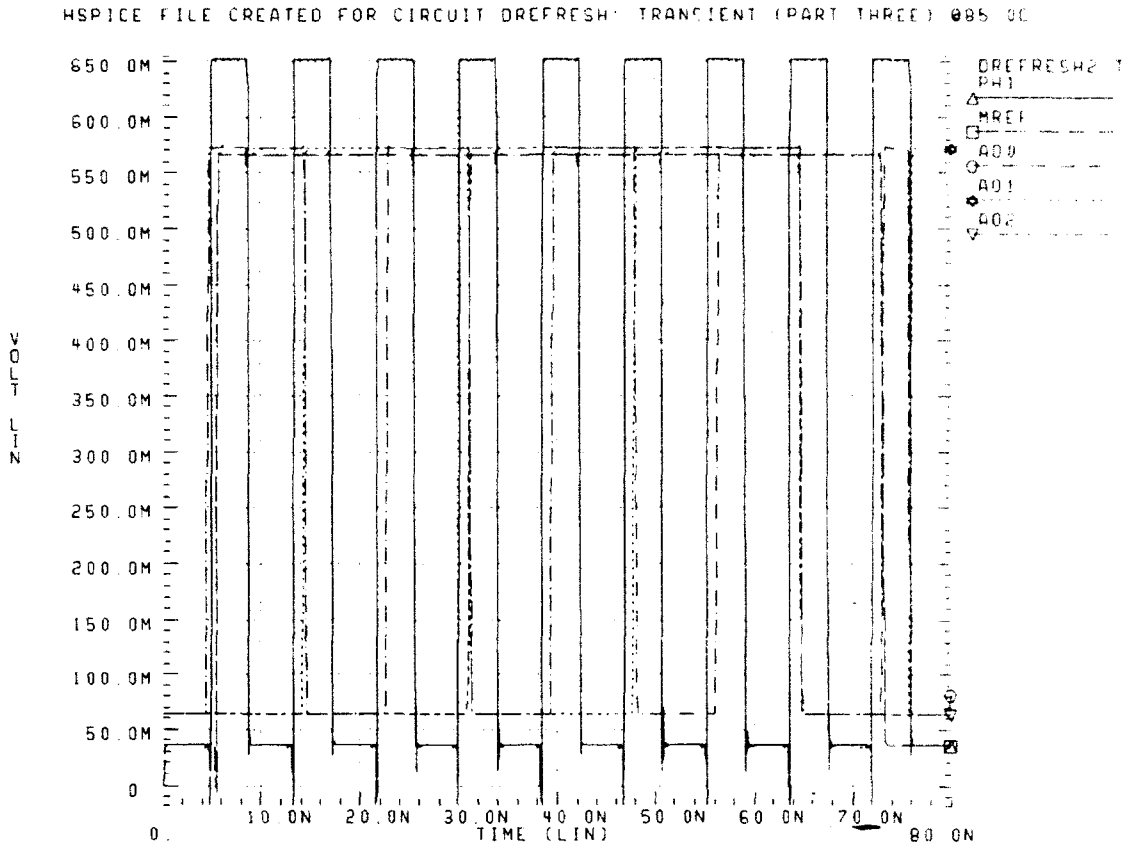


Figure 5.21 DREFRESH HSPICE Transient Analysis (Part Three) at 85.0C

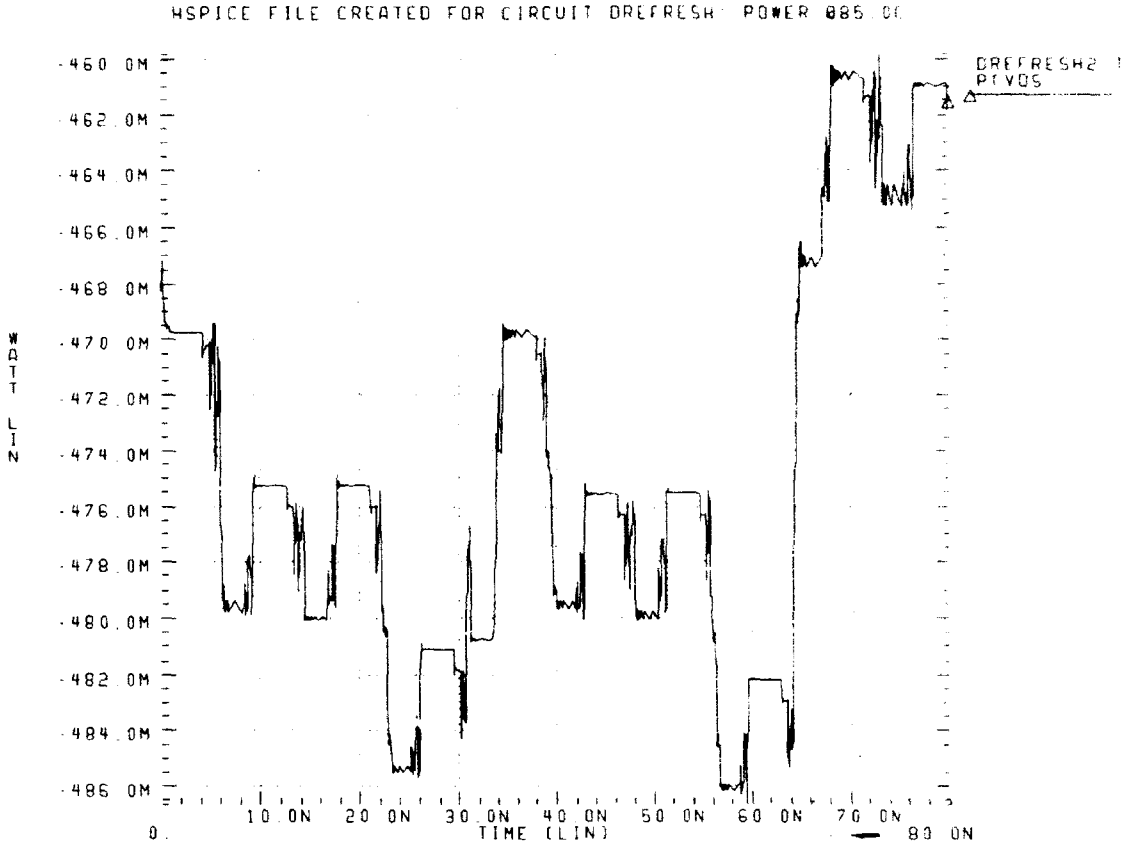


Figure 5.22 DREFRESH HSPICE POWER at 85.0C

E. Decoder Driver Circuit (DECODDRVER)

The purpose of the decoder driver circuit, DECODDRVER, is to synchronize the decoder generated address signals to the correct GaAs DRAM memory array CLOCK signal. Additionally, the DECODDRVER circuit generates the actual level-shifted pulses to actuate the GaAs MESFETs which are the access points to the fundamental charge storage elements, the parallel plate capacitors, of the GaAs DRAM memory array. Through experimentation, it was determined that the appropriate GaAs DRAM memory array CLOCK signal is the PH2D signal. For a thorough discussion of the reasons behind why this is so, see [Ref. 8:pp. 12-14]. In addition, the writing and reading operation requisite control signals, EDUM, ODUM, EDUMD, and ODUMD, are generated. This signals refer to the operations of the "dummy" cells, one on each side of the differential sense amplifier in the GaAs DRAM memory array. These signals are used by two other circuits, the OUTPUT circuit and the RAM_ARRAY circuit, both of which will be discussed later in this chapter.

See Figure 5.23 on page 187 for the DECODDRVER schematic and logical equivalence.

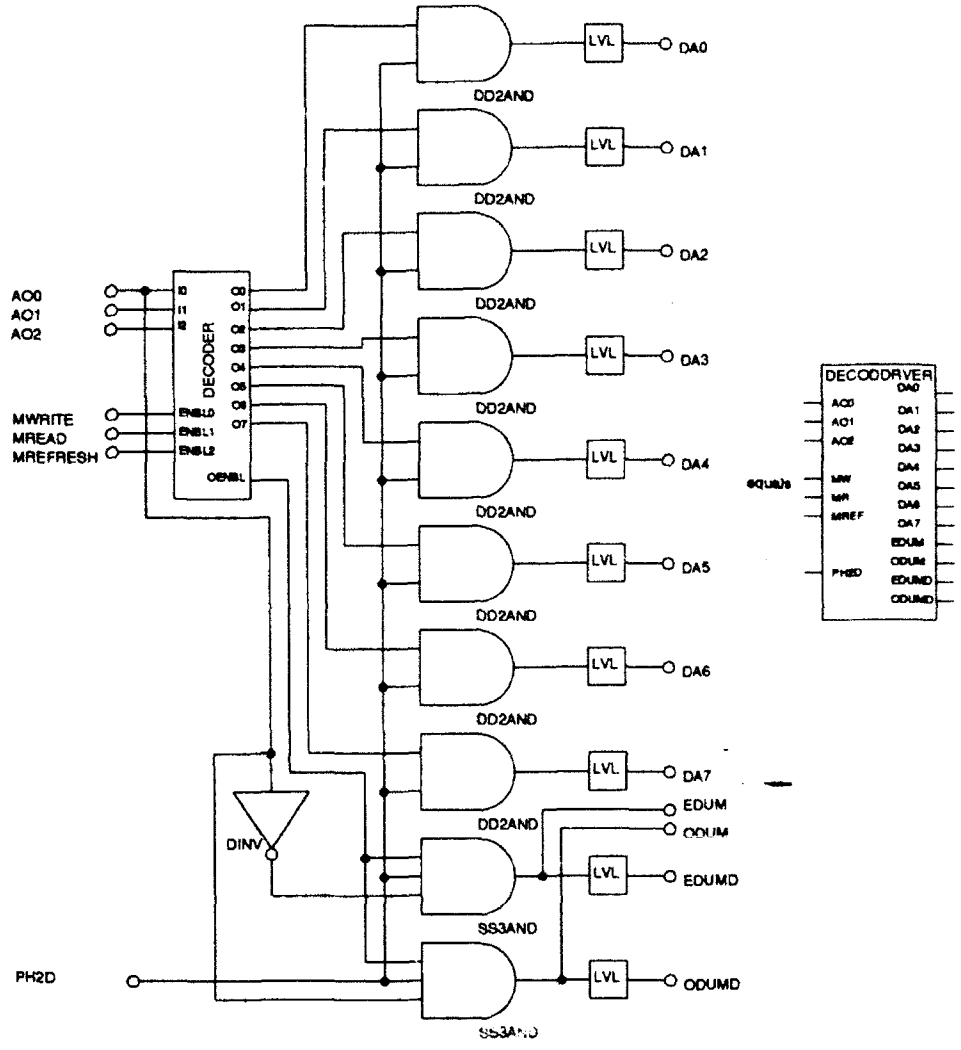


Figure 5.23 DECODDRVER Schematic and Logical Equivalence

The DECODDRVER circuit transient analysis is presented in the following eight figures. As before, the graphs are kept to a few signals each to facilitate easier understanding. It is interesting to note that in order to better simulate DECODDRVER reality, the GaAs DRAM memory array CLOCK and DREFRESH circuits were included in the HSPICE file and used to generate the following DECODDRVER input signals: PH1, AO0, AO1, AO2, and MREFRESH. See Figure 5.24 on page 188 for the DECODDRVER transient analysis (part one). See "Listing File for DECODDRVER Transient Analysis @ 25.0C" of Appendix A on page 333.

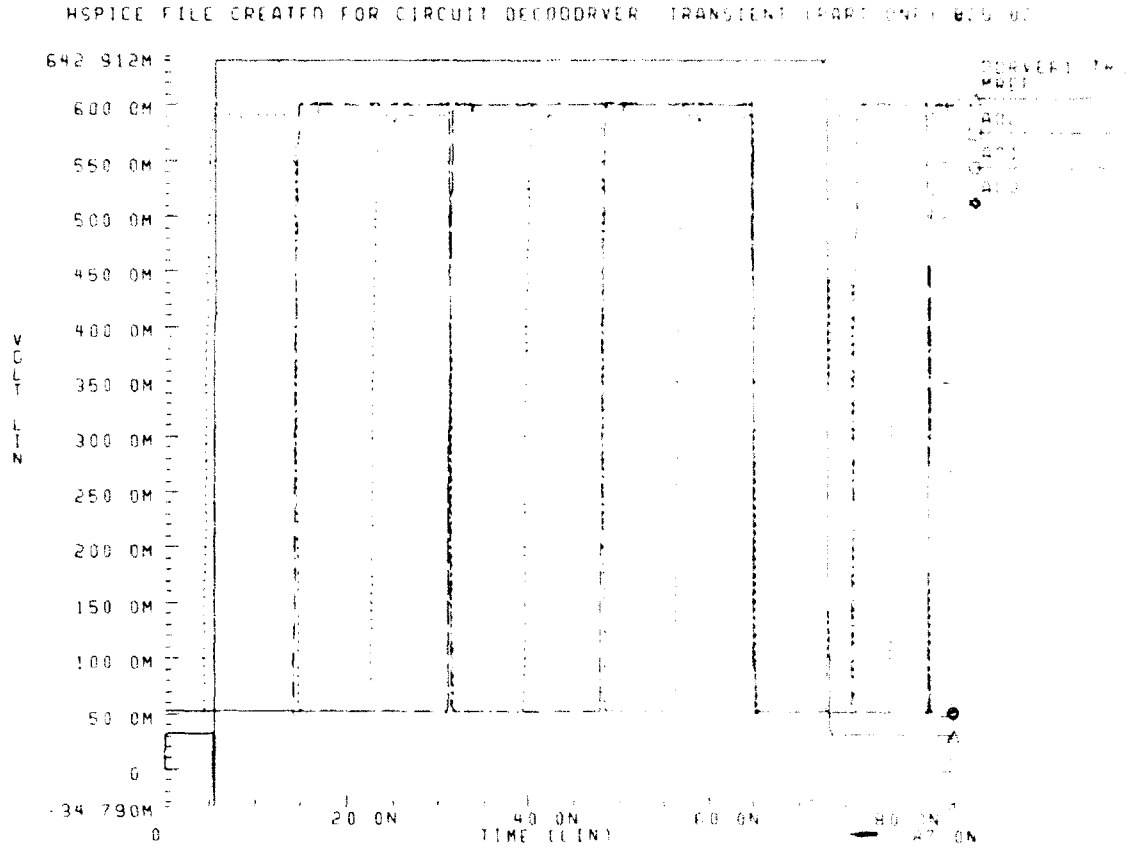


Figure 5.24 DECODDRVER HSPICE Transient Analysis (Part One) at 25.0C

Looking at Figure 5.24 on page 188, one may see the signals MREFRESH (MREF) and AO2 to AO0, as generated by the DREFRESH circuit and as inputs to the DECODDRVER circuit. The next figure, Figure 5.25 on page 189, shows the MREFRESH signal, the input CLOCK signal PH2D, and the eight "DA" signals, DA7 to DA0.

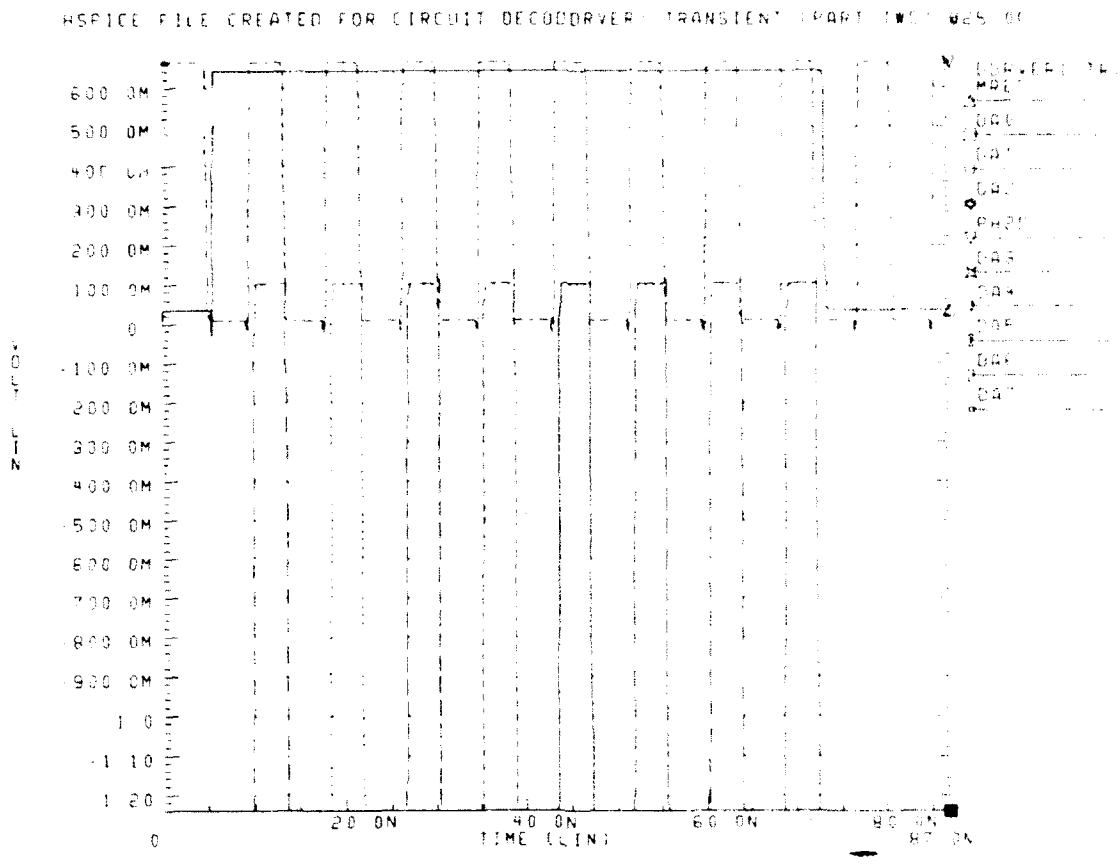


Figure 5.25 DECODDRVER HSPICE Transient Analysis (Part Two) at 25.0C

The third figure of the DECODDRVER transient analysis (part three), see Figure 5.26 on page 190, shows the aforementioned read and write control signals, EDUM, ODUM, EDUMD, and ODUMD.

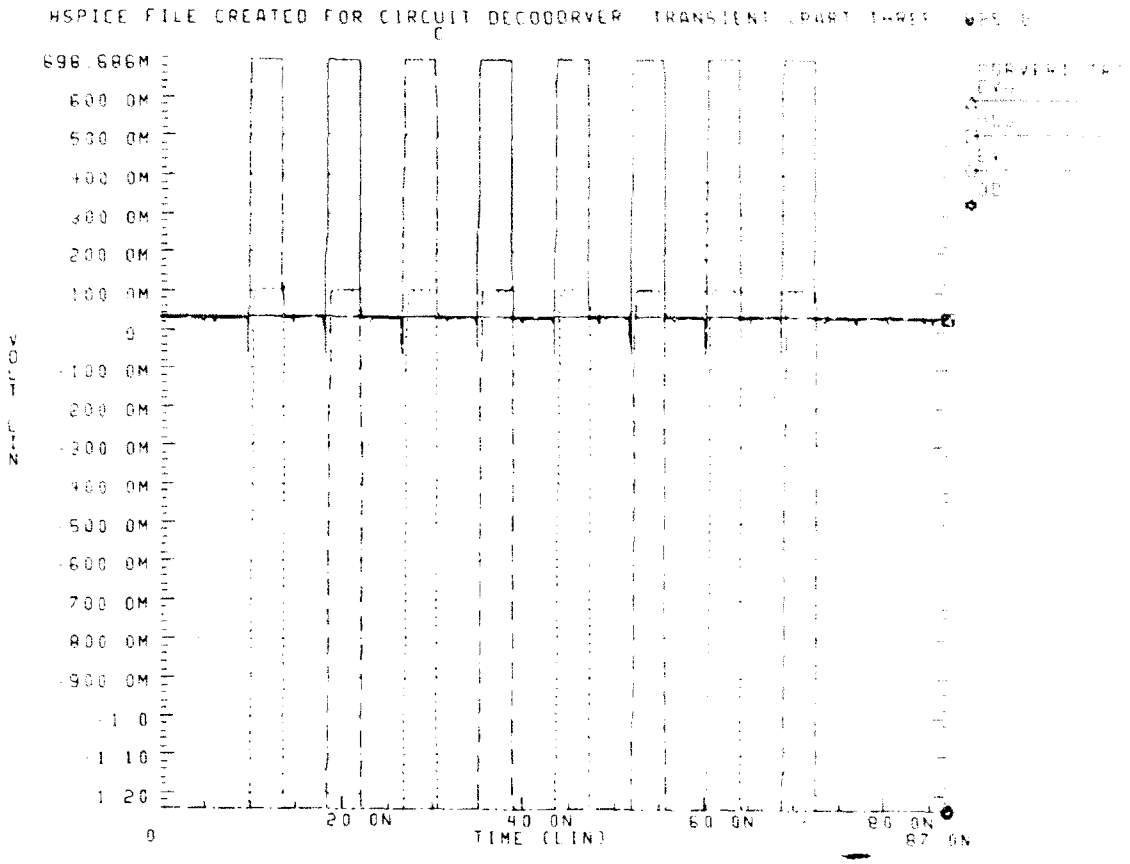


Figure 5.26 DECODDRVER HSPICE Transient Analysis (Part Three) at 25.0C

The fourth figure of the DECODDRVER transient analysis, see Figure 5.27 on page 191, presents the power dissipation of the circuit simulated at a nominal temperature of 25.0C.

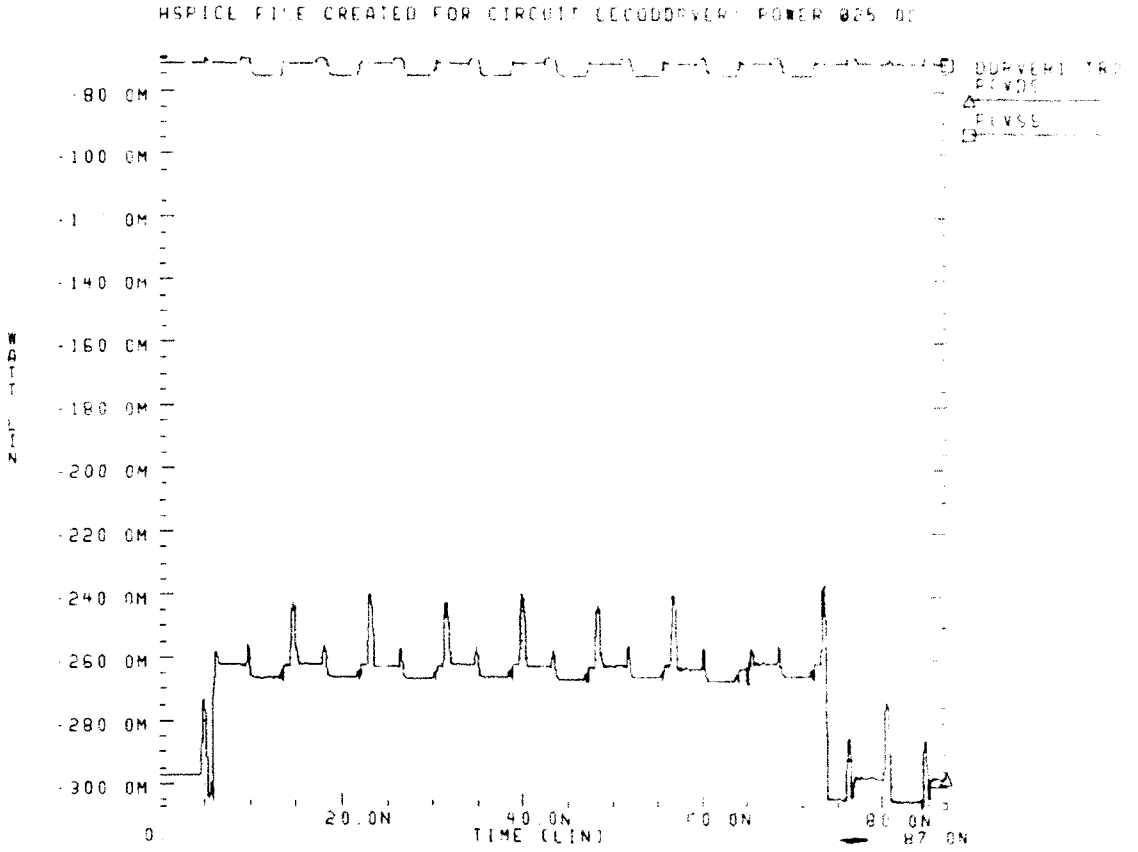


Figure 5.27 DECODDRVER HSPICE POWER at 25.0C

The following four DECODDRVER graphs show the same signals as discussed in the preceding paragraphs, but, a simulation nominal temperature of 85.0C. See Figure 5.28 on page 192, Figure 5.29 on page 193, Figure 5.30 on page 194, and Figure 5.31 on page 195.

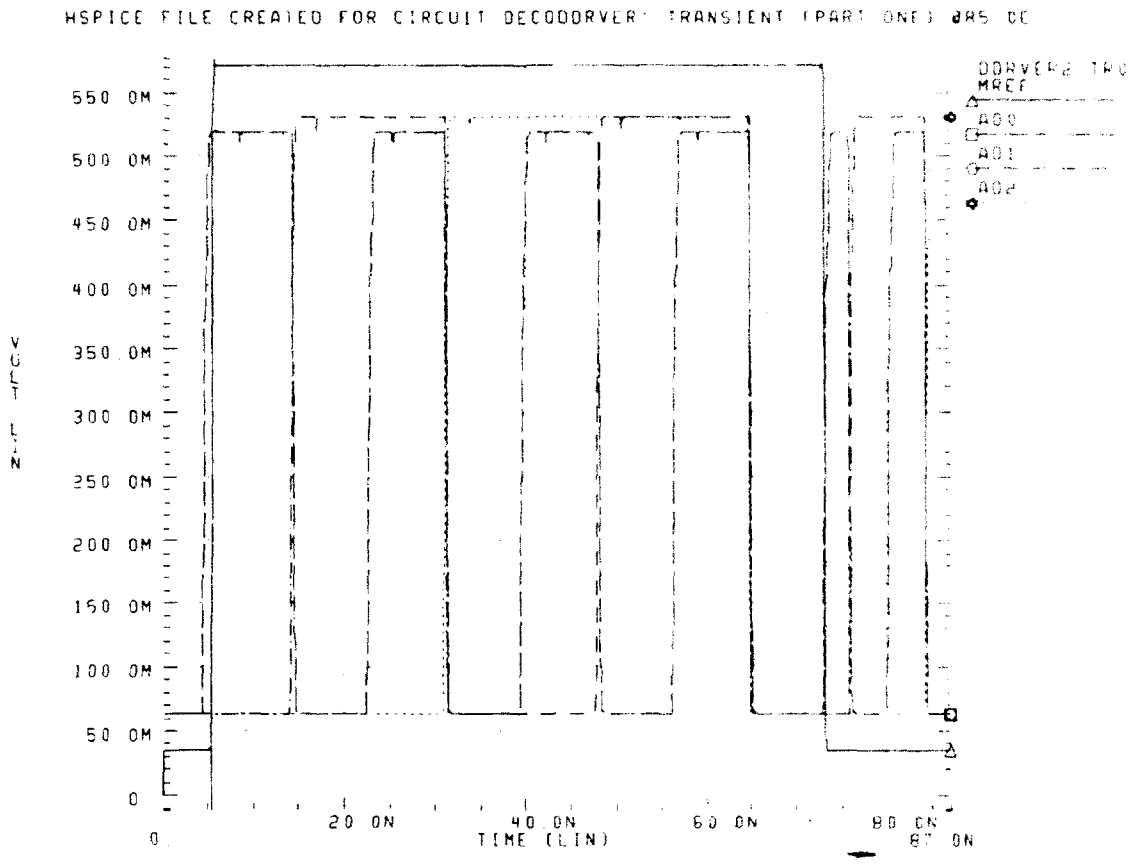


Figure 5.28 DECODDRVER HSPICE Transient Analysis (Part One) at 85.0C

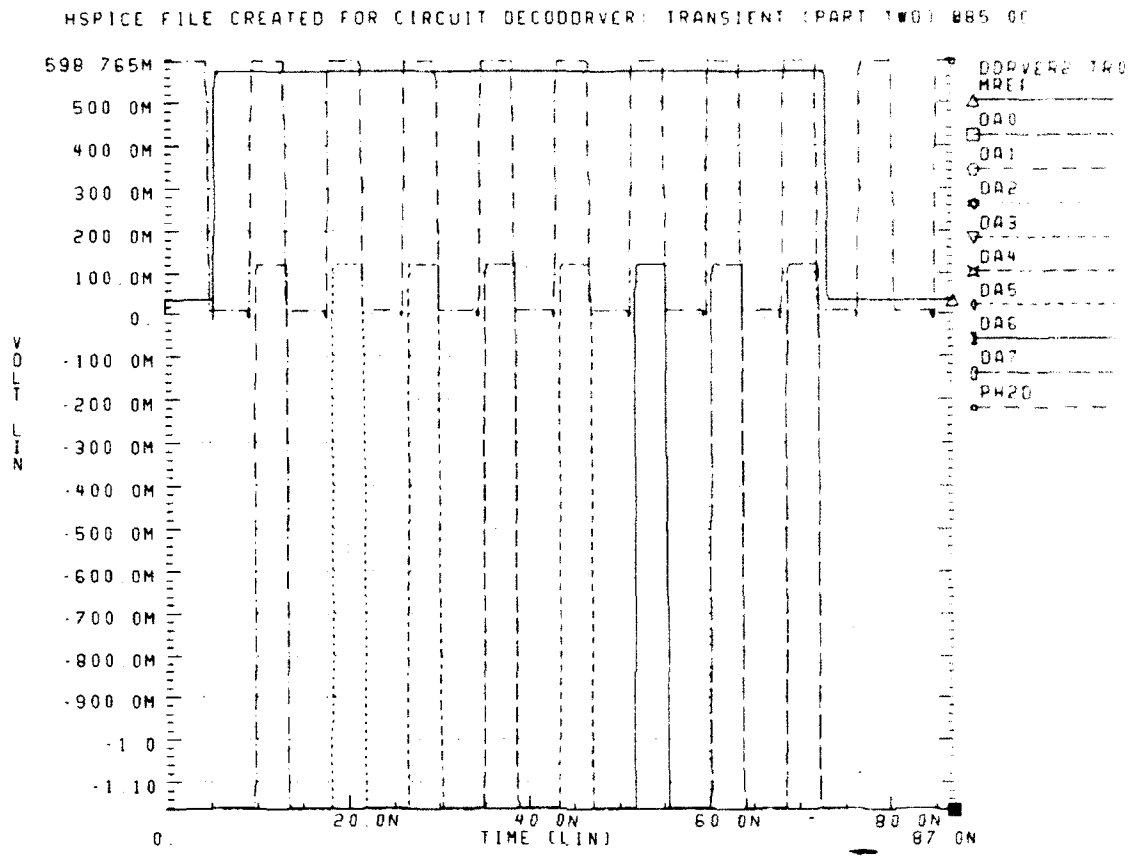


Figure 5.29 DECODDRVER HSPICE Transient Analysis (Part Two) at 85.0C

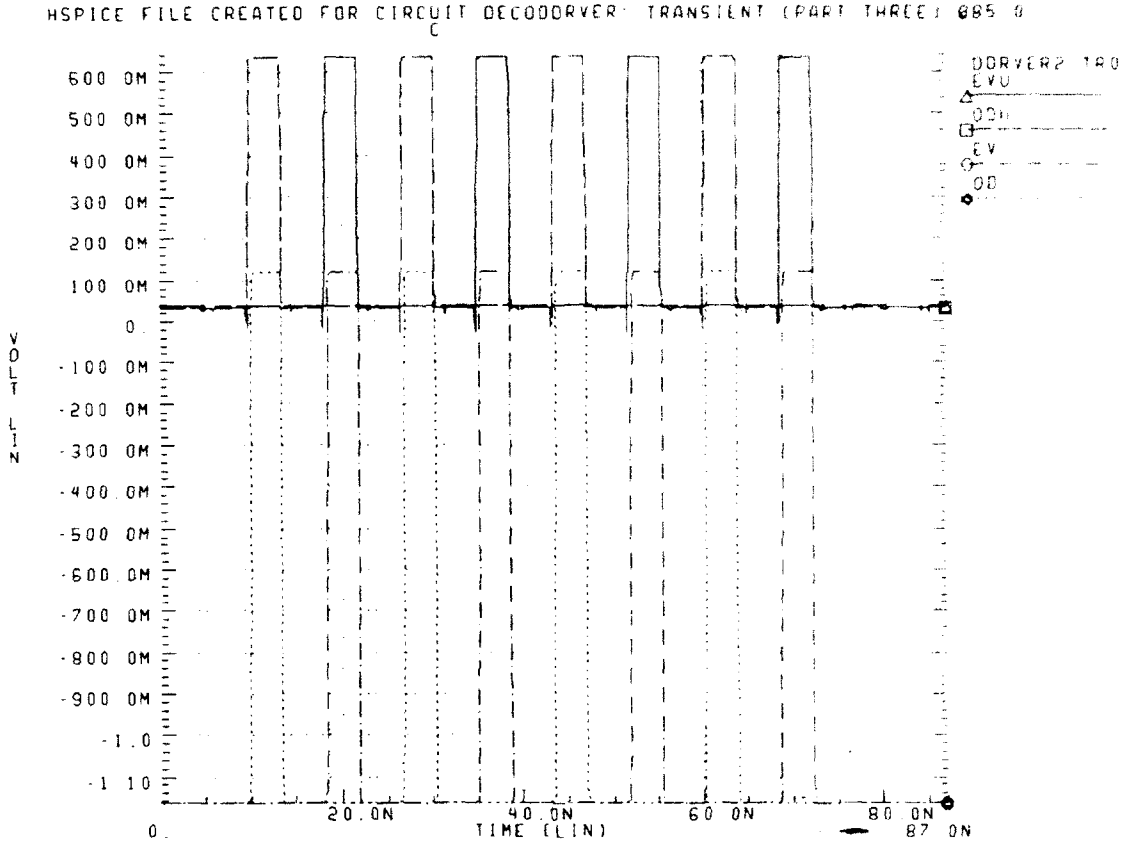


Figure 5.30 DECODDRVER HSPICE Transient Analysis (Part Three) at 85.0C

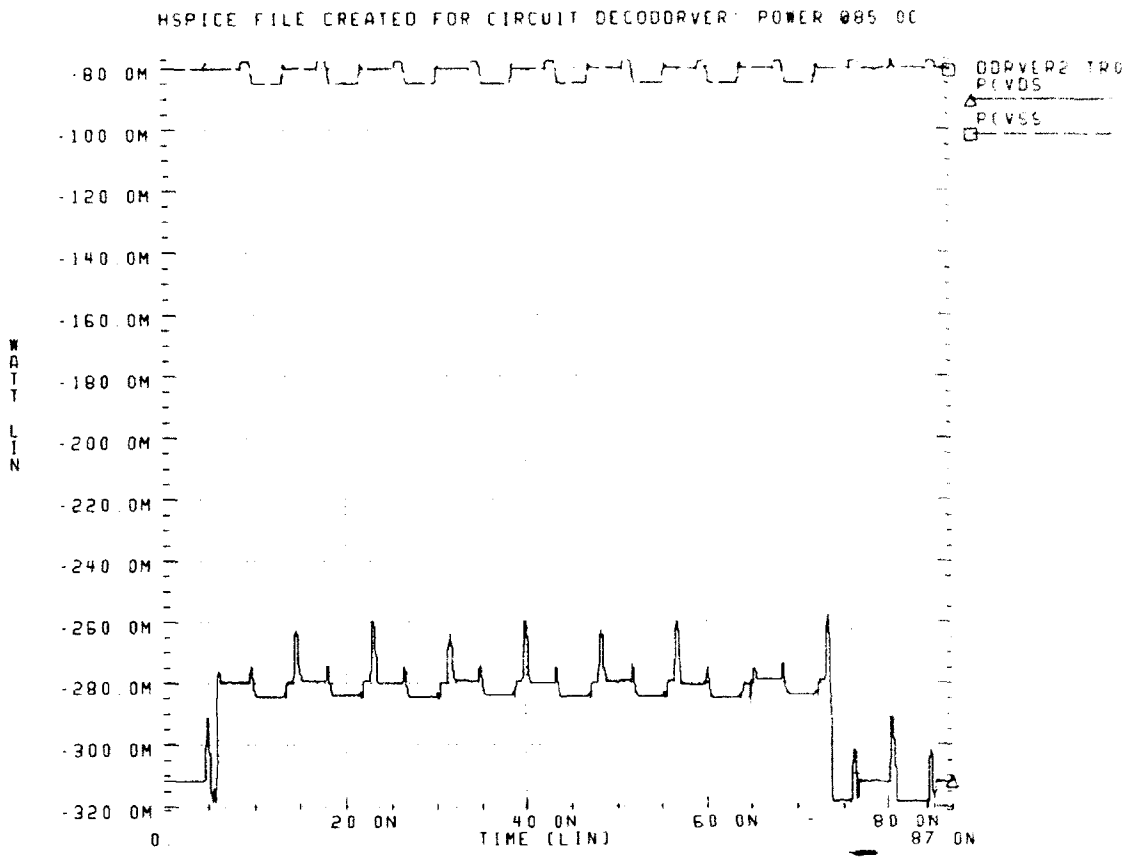


Figure 5.31 DECODDRVER HSPICE POWER at 85.0C

F. Output Logic Circuitry (OUTPUT)

The purpose of the OUTPUT circuit is to use the logical status of the GaAs DRAM memory array bit input-output (BIO) lines coupled with the assertion of either of the control signals, even dummy cell (EDUMMY) or odd dummy cell (ODUMMY), finally coupled with the presence of a READ operation to operate correctly the output data latch assigned to each data bit position. Using the design of the RAM array [Ref. 8], it may be seen that the BIO lines are on the two sides of the differential sense amplifier and are called "EVENBIO" (or EBIO) and "ODDBIO" (or OBIO). Additionally, each BIO line has a "dummy" cell attached to it, the EVENBIO side has a dummy cell, ODUMMY, and the ODDBIO side has a dummy cell, EVENDUMMY. The purpose of these dummy cells, as thoroughly discussed in [Ref. 8], is to provide a known reference voltage for use by the differential sense amplifier. Basically, the voltage placed on the "xBIO" line by the "yDUMMY" cell assists the differential sense amplifier in deciding which way to flip.

Notice also from the work of Vagts, [Ref. 8], the capacitance of the dummy cell is much smaller than the capacitance used by the main storage elements.

The control signals, EDUMMY and ODUMMY, are generated by the circuit DECODDRVER, see Figure 5.23 on page 187. The purpose of these signals is to provide to the OUTPUT circuit the knowledge of which dummy cell is being accessed, regardless of the chosen operation, READ, WRITE, or REFRESH. The knowledge of which dummy cell is being accessed (which indicates to the circuit which BIO line will contain the actual bit data read from the target memory cell), the voltaic status of the GaAs DRAM memory array BIO lines, and the assertion of a READ operation (as asserted through MREAD) are sufficient to easily discern the READ data bit value and cause it to be latched into the output data latch. It is interesting to note that a data latch, not a data flip-flop, was intentionally chosen so that the longest possible time within the target READ operation is allowed for the data lines to settle as the output data latch contents are not latched until the falling edge of the MREAD signal. See Figure 5.32 on page 196 for the OUTPUT schematic and logical equivalence.

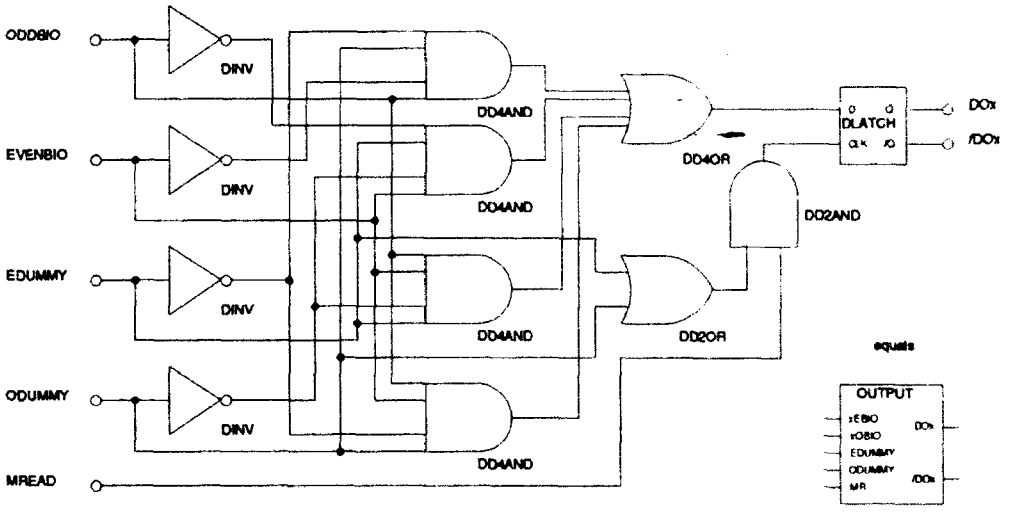


Figure 5.32 OUTPUT Schematic and Logical Equivalence

The OUTPUT circuit transient analysis was executed in much the same way as the previous major circuits. Two simulation runs were accomplished, one at the standard default nominal temperature of 25.0C and the other at the elevated nominal temperature of 85.0C. Additionally, as before, uncluttered figures

depicting the HSPICE simulation transient analysis are shown to facilitate easier understanding of the circuit under test. The first figure of the OUTPUT circuit transient analysis is Figure 5.33 on page 197.

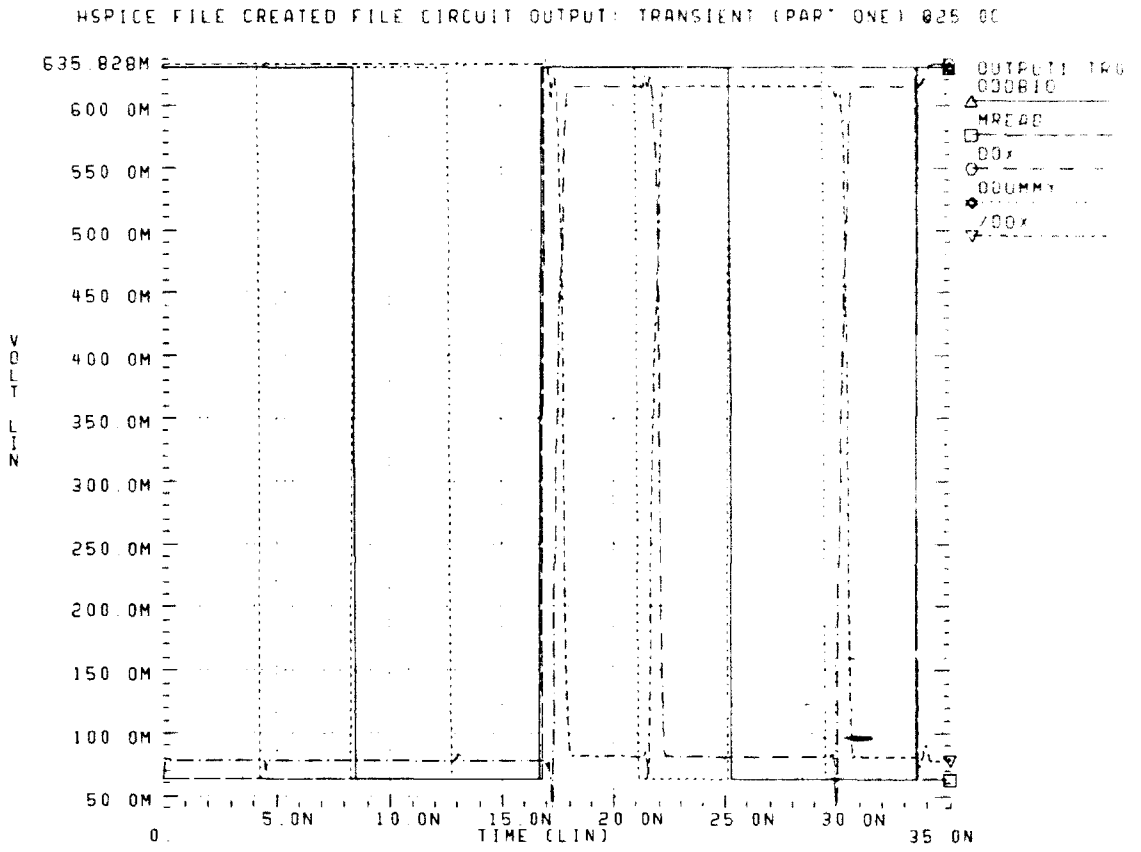


Figure 5.33 OUTPUT HSPICE Transient Analysis (Part One) at 25.0C

This figure, Figure 5.33 on page 197, shows the ODDBIO line from the GaAs DRAM memory array, the MREAD signal, the ODUMMY control signal, and the two output lines from the output data latch, DOx and /DOx (Data Out x & /{Data OUT x}). It may be seen in Figure 5.33 on page 197 that the output data latch output lines do not change until the enable signal to the output data latch (MREAD) is asserted, and continue to change until the enable signal to the output data latch (MREAD) is de-asserted. Additionally, it may be seen that once the output data latch is allowed to feel its Data input, the output DOx goes high because the ODDBIO signal is HIGH and the ODUMMY is high. The combination of the ODDBIO = HIGH and the ODUMMY = HIGH indicates to the OUTPUT logic that a bit data ONE has been read. This transition occurs from ~17 nanoseconds to ~22 nanoseconds. At time ~21 nanoseconds, the ODUMMY goes LOW causing the OUTPUT circuit logic to reconsider its position on the value of the "just read" bit data and the output data

latch goes to LOW at ~22 nanoseconds. The value of the output data latch is finally secured at ~34.5 nanoseconds, when the MREAD signal is de-asserted.

The second figure of the OUTPUT circuit transient analysis is Figure 5.34 on page 198. This figure shows the activities of the MREAD signal, the two output data latch signals, DOx and /DOx, and the EVENBIO and EDUMMY signals. An examination of the associated schematics for the GaAs DRAM memory array and the DECODDRVER will show that the EVENBIO and EDUMMY signals will always be the inverse of the ODDBIO and ODUMMY signals.

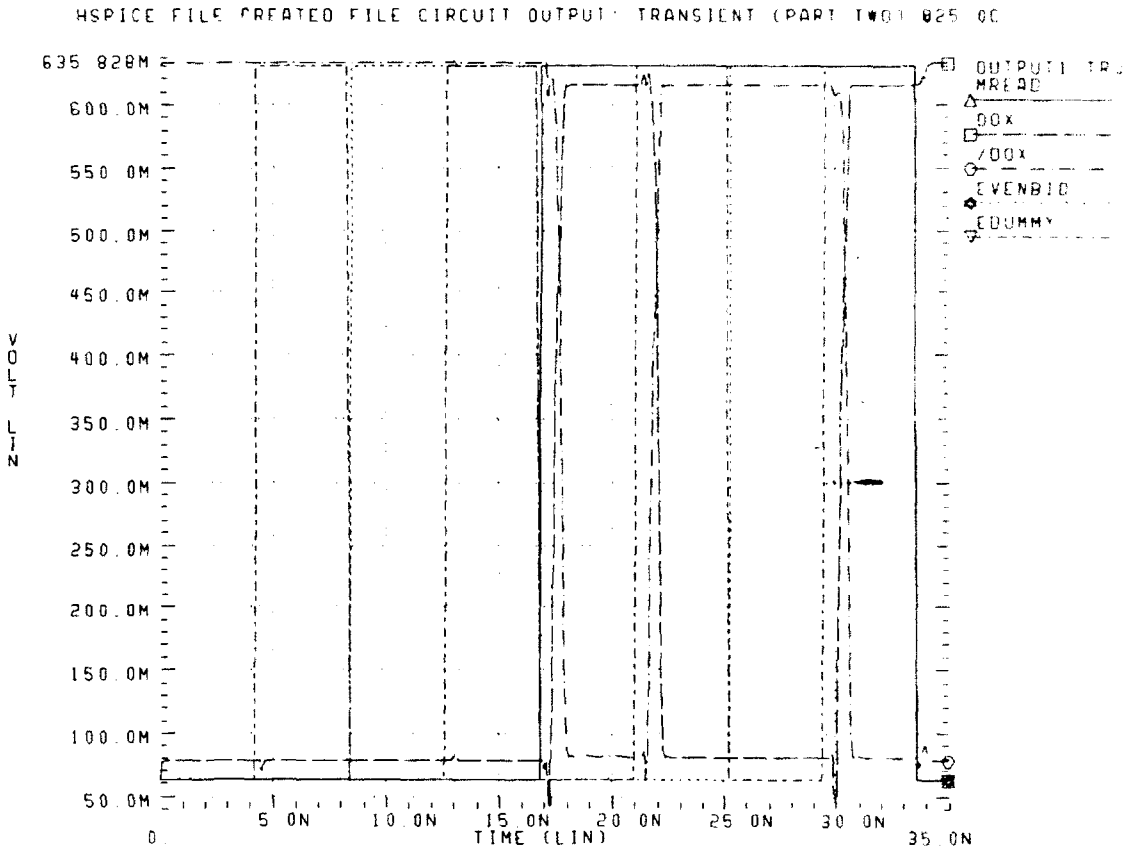


Figure 5.34 OUTPUT HSPICE Transient Analysis (Part Two) at 25.0C

The third and final figure for the nominal temperature HSPICE simulation of the OUTPUT circuit is the power dissipation, see Figure 5.35 on page 199. See "Listing File for OUTPUT Transient Analysis @ 25.0C" of Appendix A on page 357.

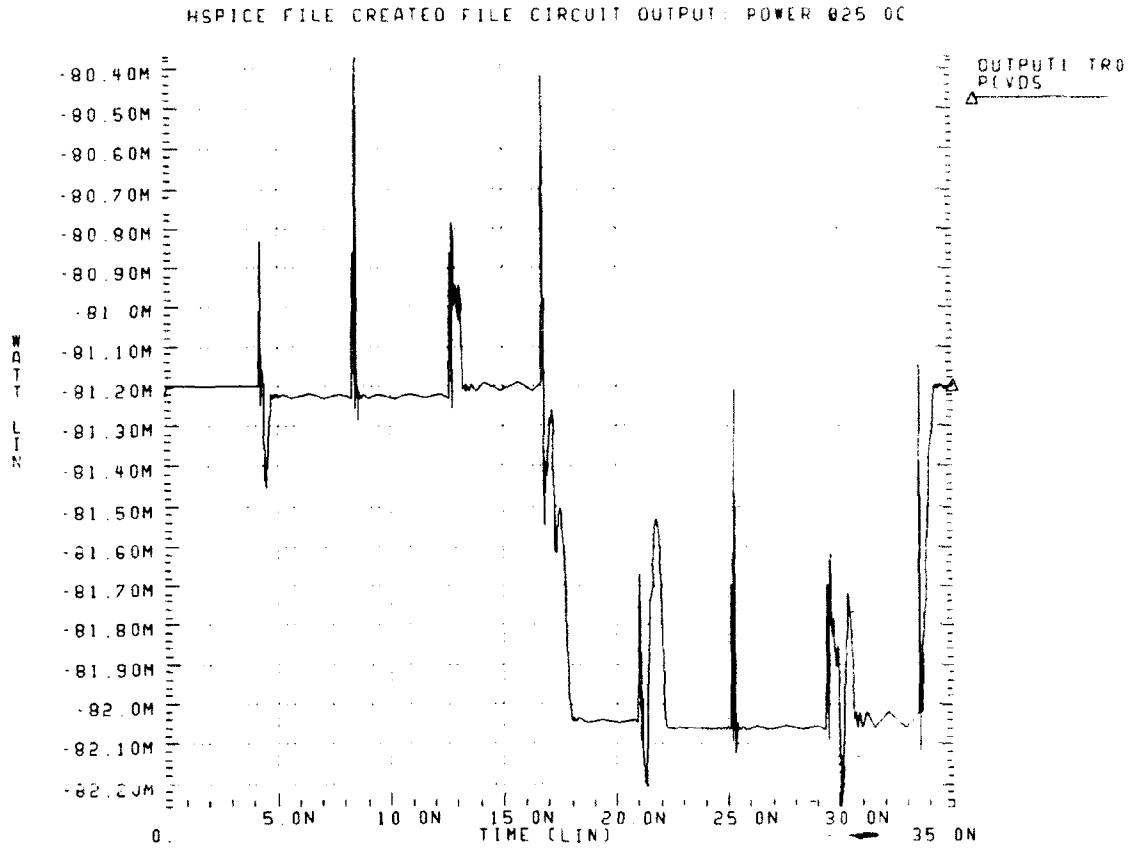


Figure 5.35 OUTPUT HSPICE POWER at 25.0C

The next three figures show the same signals as described previously for the HSPICE simulation of the OUTPUT circuit except the simulation was executed at a nominal temperature of 85.0C, see Figure 5.36 on page 200, Figure 5.37 on page 201, and Figure 5.38 on page 202.

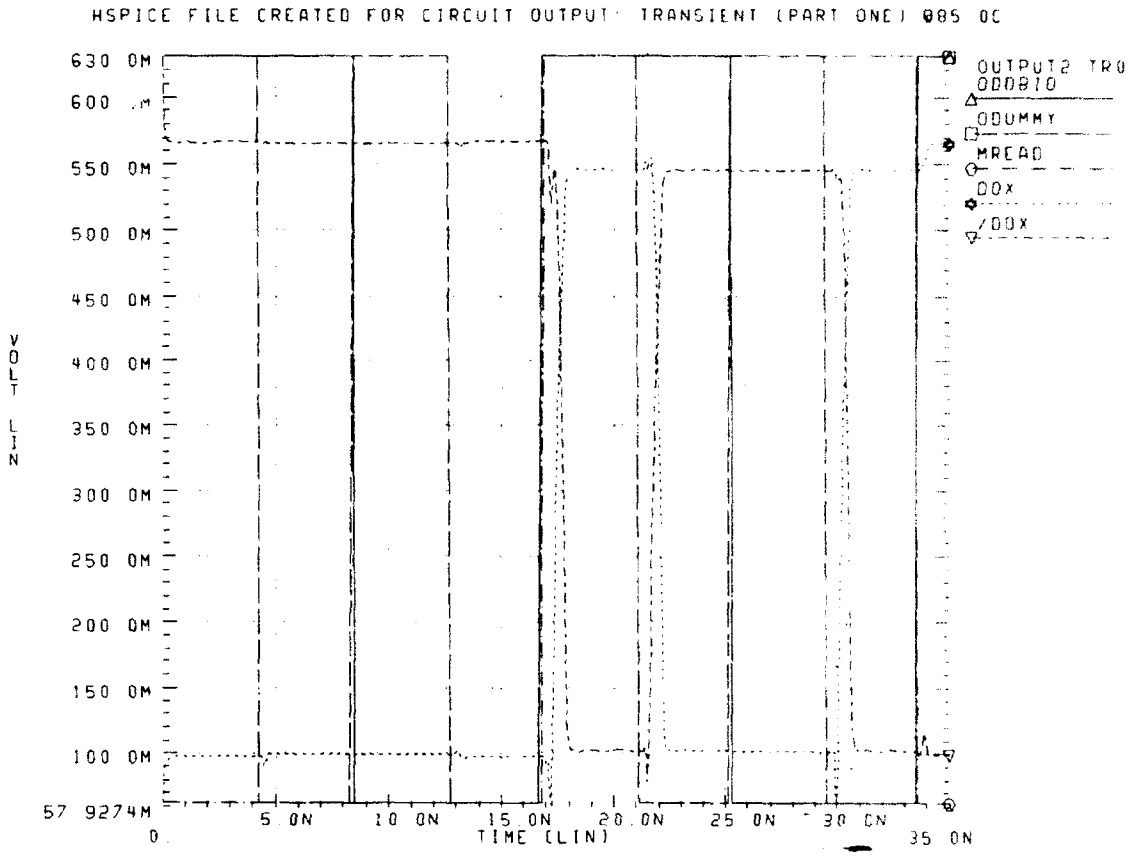


Figure 5.36 OUTPUT HSPICE Transient Analysis (Part One) at 85.0C

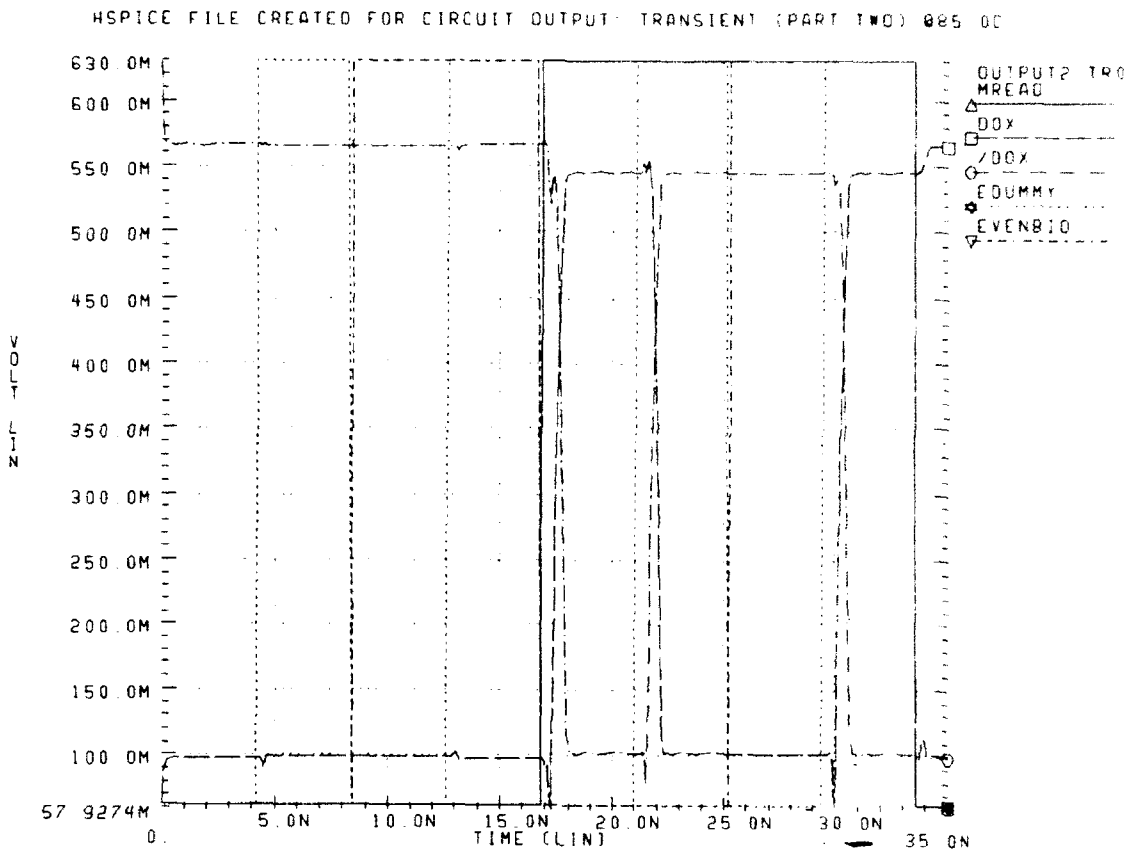


Figure 5.37 OUTPUT HSPICE Transient Analysis (Part Two) at 85.0C

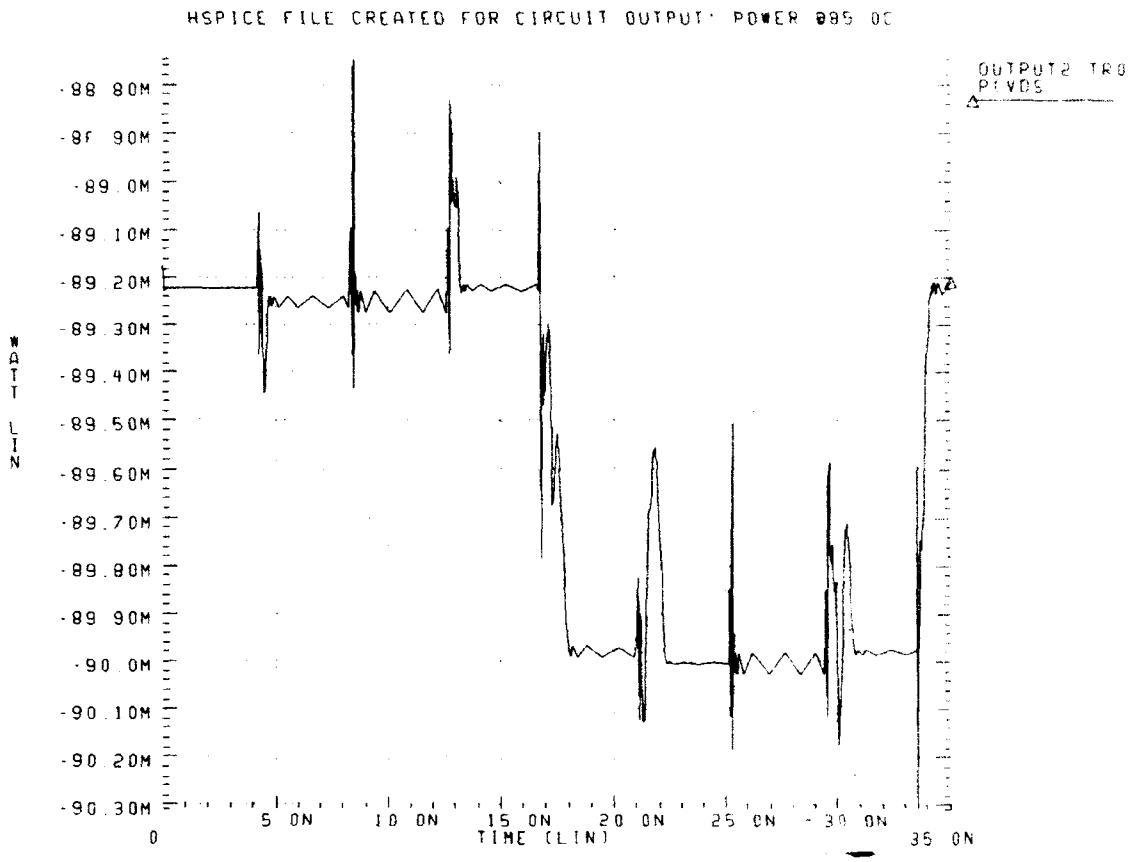


Figure 5.38 OUTPUT HSPICE POWER at 85.0C

G. Operation Priority Logic Circuitry (WRITEP)

The purpose of the operation priority circuit, WRITEP, is to establish the relative priorities amongst the three available GaAs DRAM memory operations, READ, WRITE and REFRESH.

The REFRESH operation was chosen to have the highest priority in order to prevent data spoilage due to refresh latency. The next operation in priority was the WRITE operation. This choice was made to allow the CPU to dump data into the memory using the WRITE operation. It was decided that the READ operation would have the lowest priority. The circuit design is simple and little else needs to be reported with regard to this circuit. See Figure 5.39 on page 203 for the WRITEP schematic and logical equivalence.

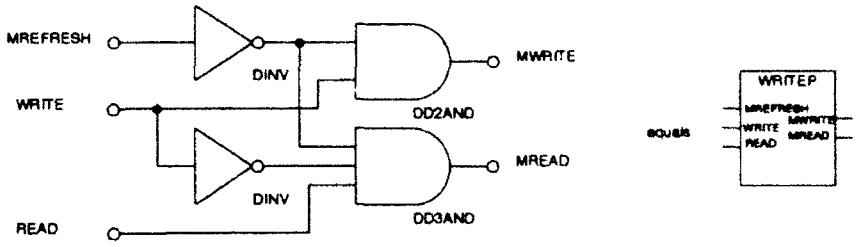


Figure 5.39 WRITEP Schematic and Logical Equivalence

The WRITEP HSPICE transient analysis is shown in Figure 5.40 on page 203. The upper graph of Figure 5.40 shows the three circuit inputs, READ, WRITE, and MREFRESH. The lower graph of Figure 5.40 shows the resultant output signals of MREAD and MWRITE. It may be seen in the lower graph of Figure 5.40 that the MREAD output is only asserted when both MWRITE and MREFRESH are de-asserted.

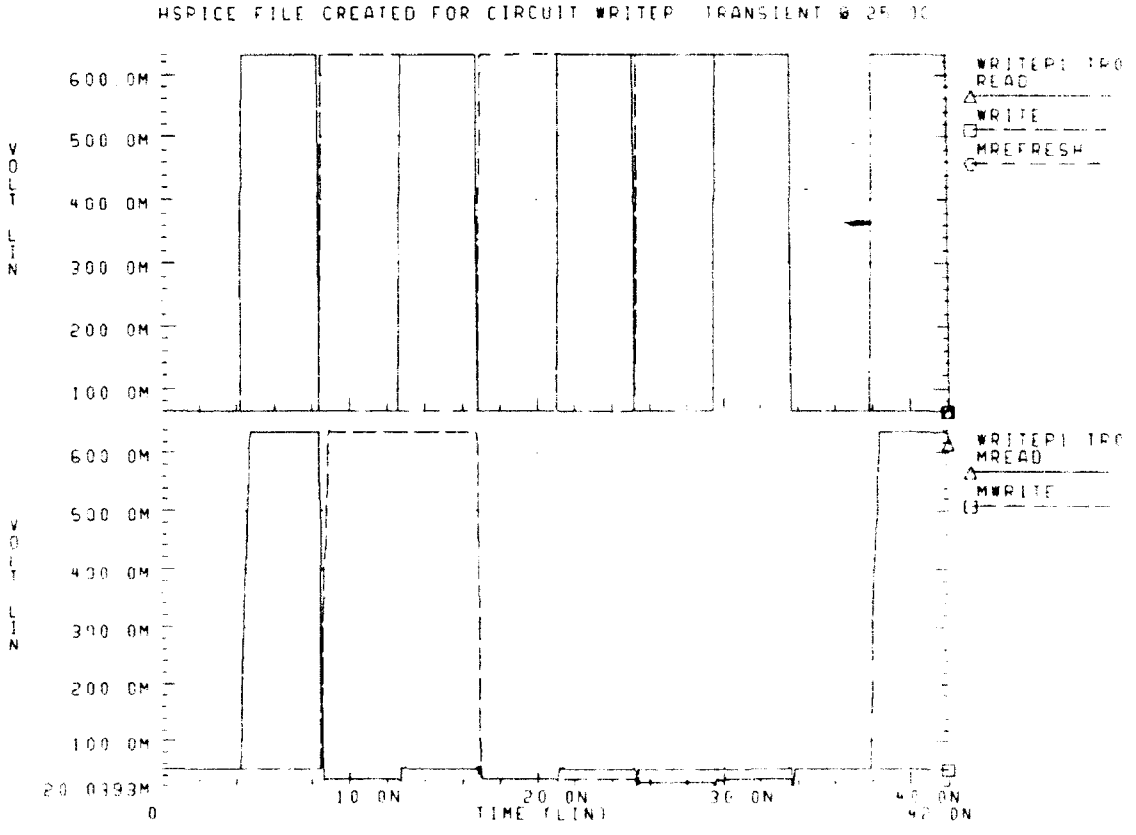


Figure 5.40 WRITEP HSPICE Transient Analysis at 25.0C

The next figure, Figure 5.41 on page 204, shows the power dissipation of the WRITEP circuit operating at a nominal temperature of 25.0C.

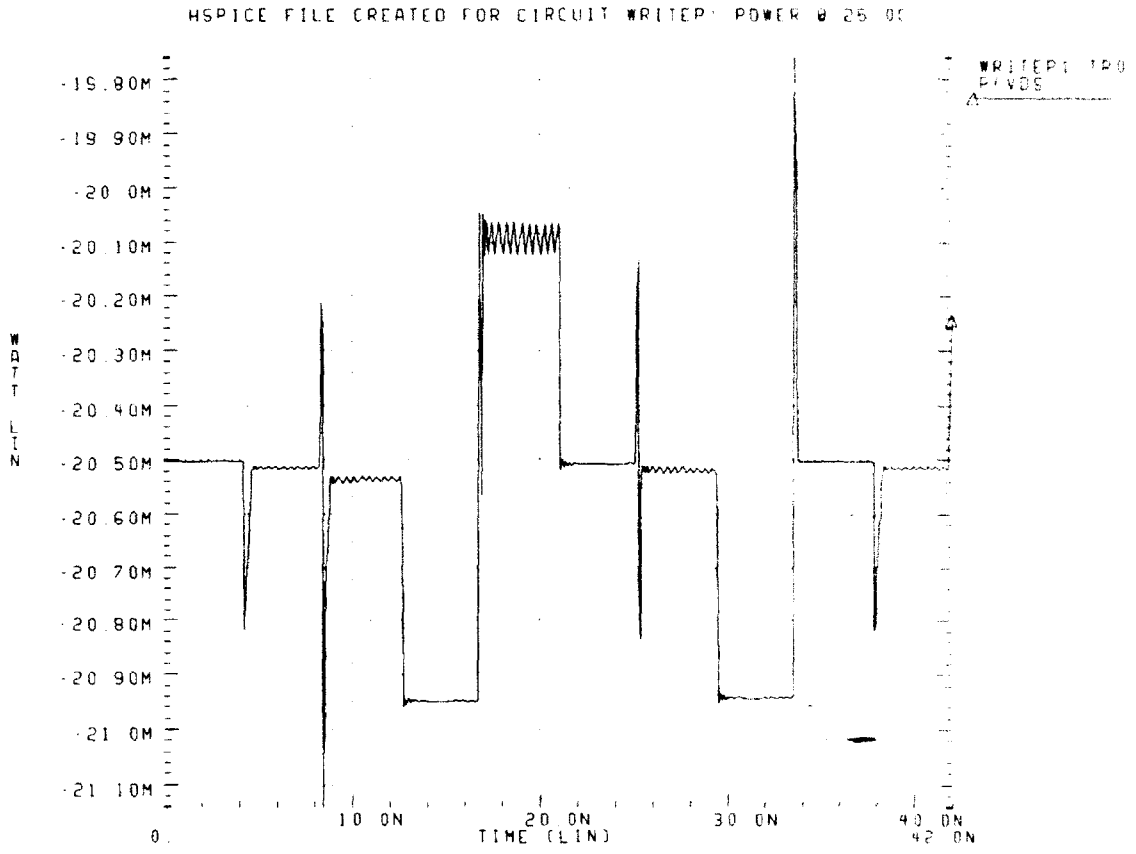


Figure 5.41 WRITEP HSPICE POWER at 25.0C

The final two figures concerning the WRITEP circuit demonstrates the same signals with the circuit operating at a nominal temperature of 85.0C. See Figure 5.42 on page 205 and Figure 5.43 on page 206.

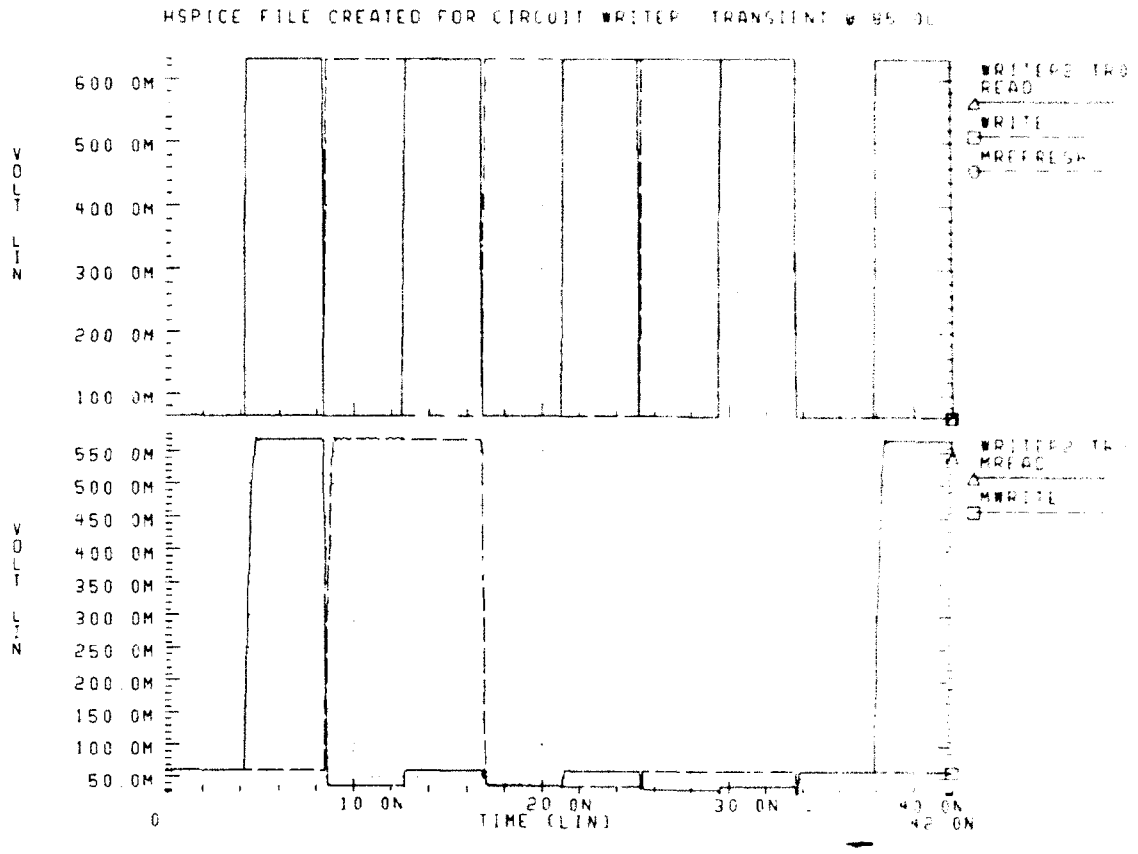


Figure 5.42 WRITEP HSPICE Transient Analysis at 85.0C

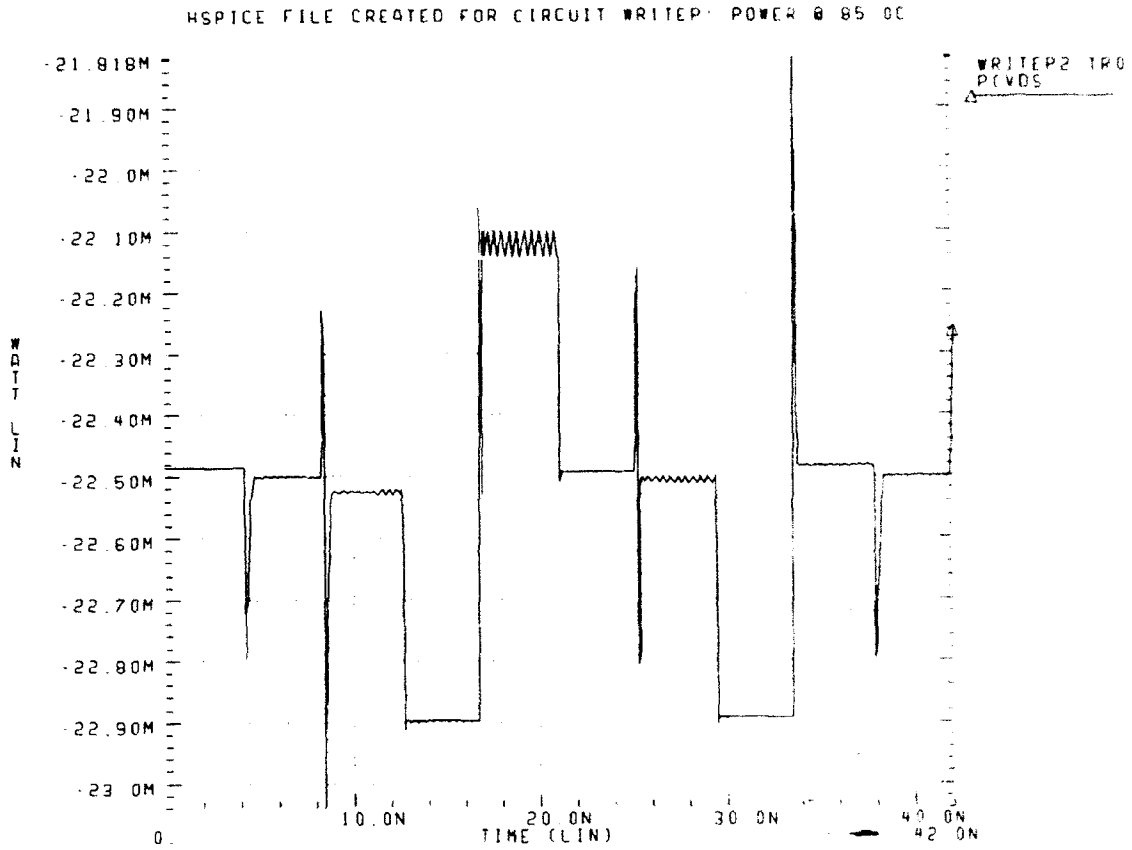


Figure 5.43 WRITEP HSPICE POWER at 85.0C

H. Memory Busy Circuitry (MBSY)

The only reason that this circuit (which consists entirely of one DD3OR gate) is in the major circuits portion of this report is because this circuit occupies a major block of the hierarchial block diagram, see Figure 6.1 on page 218.

The operation of this circuit is simple. If any of the three GaAs DRAM memory array operation signals (MREAD, MWRITE, and MREFRESH) are asserted then the memory busy signal (MBSY) is asserted. This control signal, MBSY, is one of the two external control signal outputs of the GaAs DRAM memory array. See Figure 5.44 on page 207 for the MBSY schematic and logical equivalence.

Figure 5.44 MBSY Schematic and Logical Equivalence

The MBSY HSPICE transient analysis and power dissipation graphs are shown in the following two figures. The first figure demonstrates the transient operation (upper graph) and power dissipation (lower graph) of the circuit operating at a nominal temperature of 25.0C. See Figure 5.45 on page 207. See "Listing File for MBSY Transient Analysis @ 25.0C" of Appendix A on page 366.

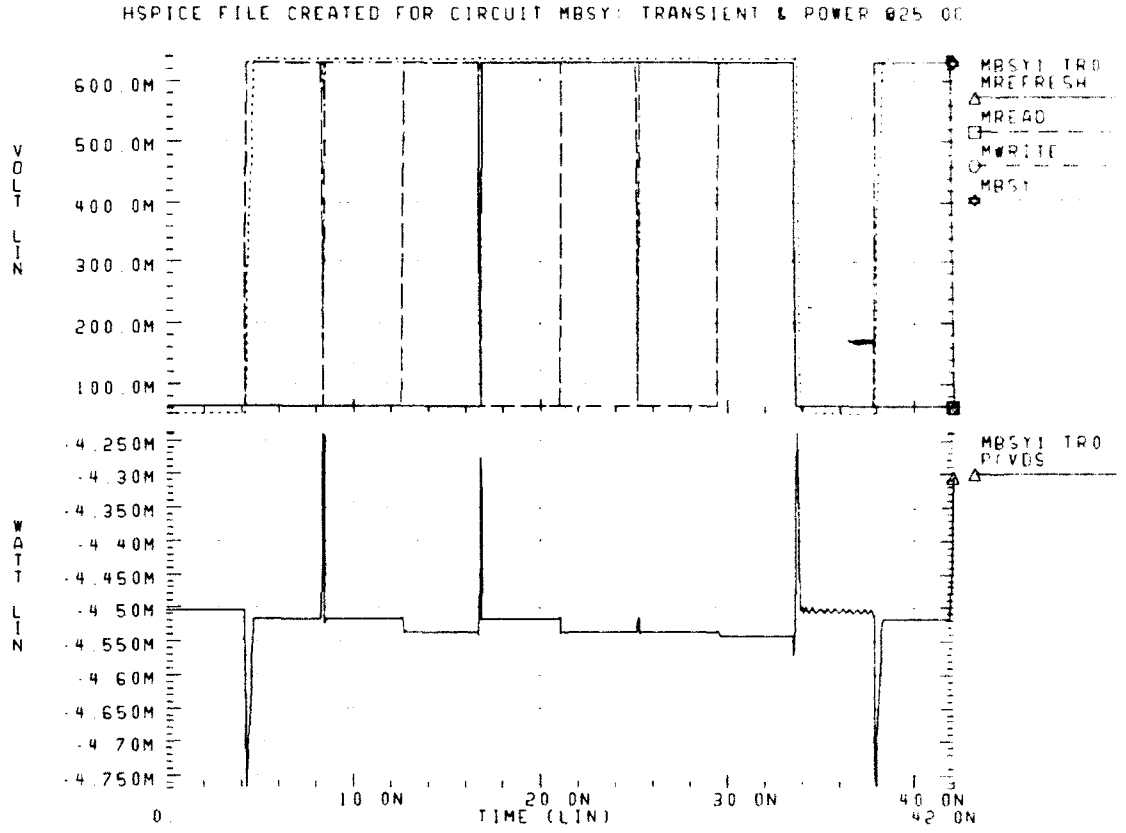


Figure 5.45 MBSY HSPICE Transient Analysis & Power at 25.0C

The next figure demonstrates the transient operation (upper graph) and power dissipation (lower graph) of the DRDY circuit operating at a nominal temperature of 85.0C. see Figure 5.46 on page 208.

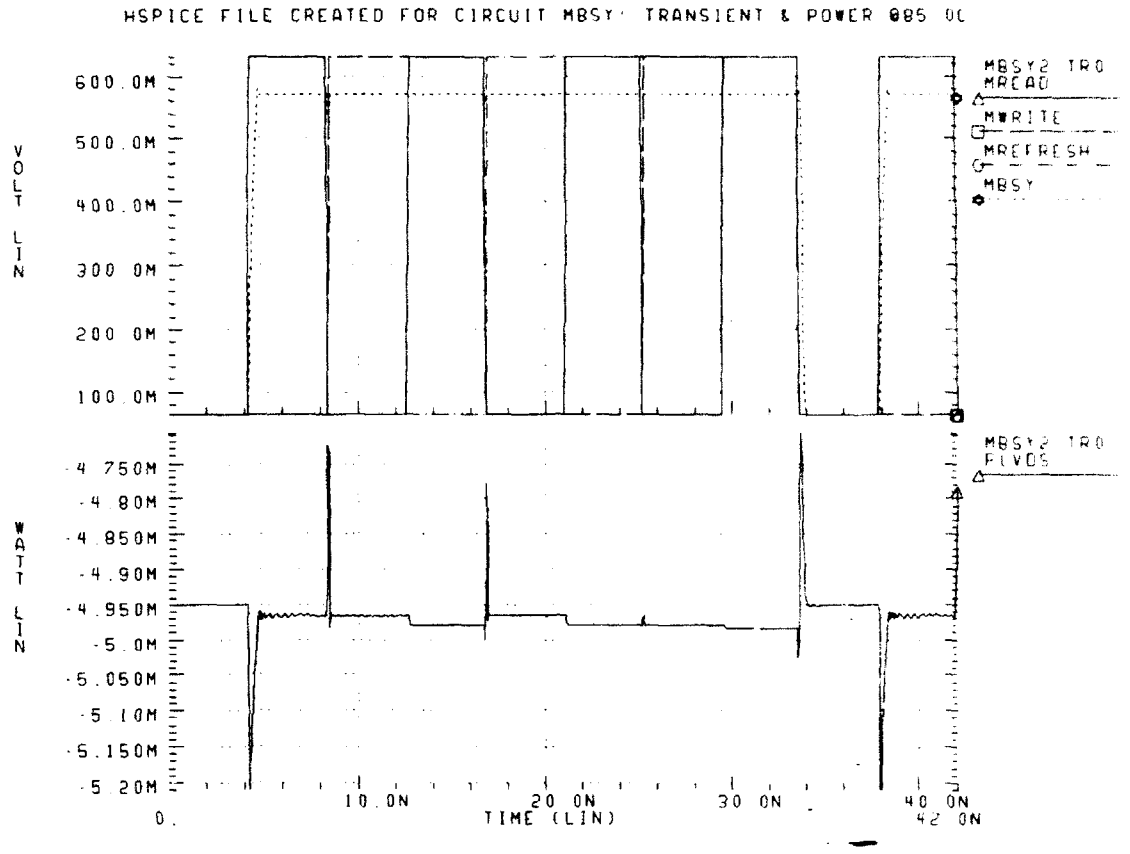


Figure 5.46 MBSY HSPICE Transient Analysis & Power at 85.0C

I. Data Ready Circuitry (DRDY)

This data ready (DRDY) circuit also occupies a major block of the hierarchial block diagram and this is its rationale for being included in the major circuits portion of this report.

The operation of this circuit is simple. The DRDY signal is de-asserted only during the actual operation of the READ cycle. Because of the output data latch, the data from the last READ operation is preserved. See "Output Logic Circuitry (OUTPUT)" on page 195. This control signal, DRDY, is the other external control signal output of the GaAs DRAM memory array. See Figure 5.47 on page 209 for the DRDY schematic and logical equivalence.

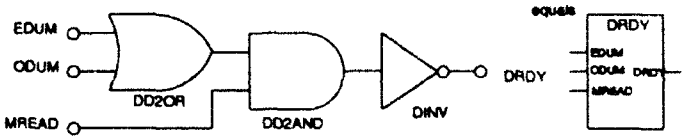


Figure 5.47 DRDY Schematic and Logical Equivalence

The DRDY HSPICE transient analysis and power dissipation graphs are shown in the following two figures. The first figure demonstrates the transient operation (upper graph) and power dissipation (lower graph) of the circuit operating at a nominal temperature of 25.0C, see Figure 5.48 on page 209. See "Listing File for DRDY Transient Analysis @ 25.0C" of Appendix A on page 370.

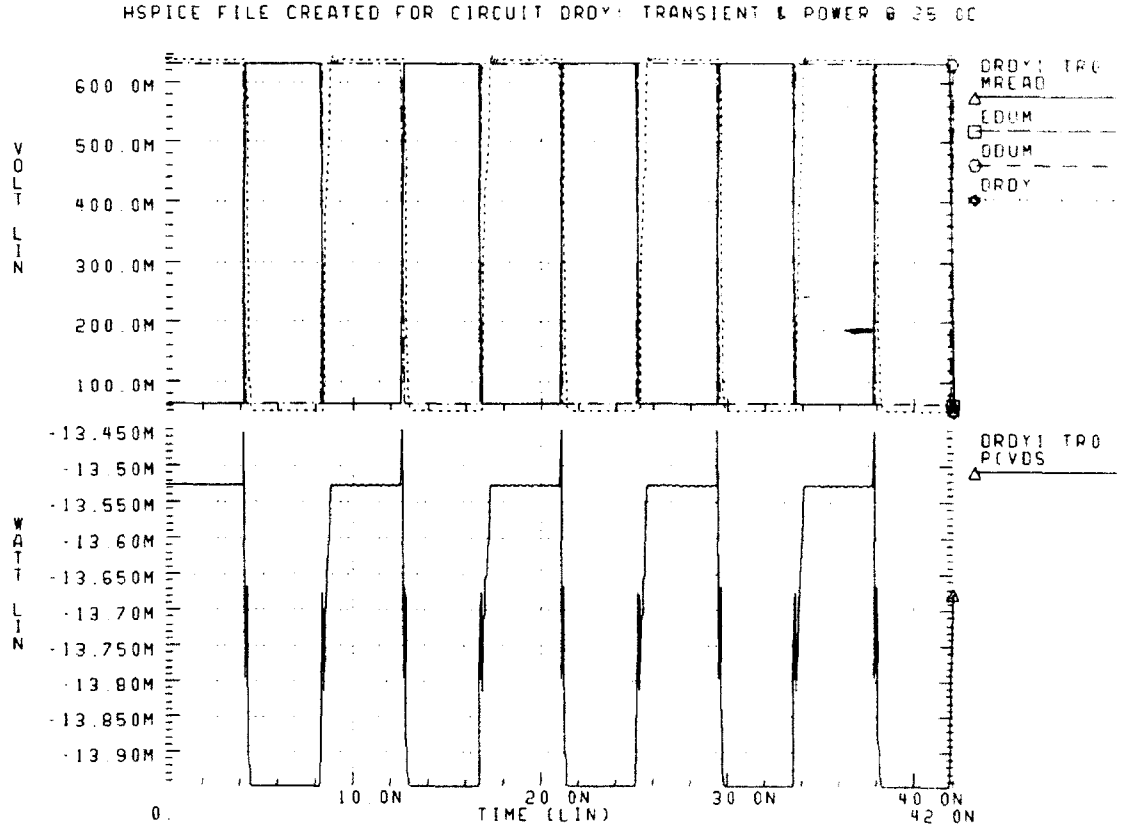


Figure 5.48 DRDY HSPICE Transient Analysis & Power at 25.0C

The next figure demonstrates the transient operation (upper graph) and power dissipation (lower graph) of the DRDY circuit operating at a nominal temperature of 85.0C, see Figure 5.49 on page 210.

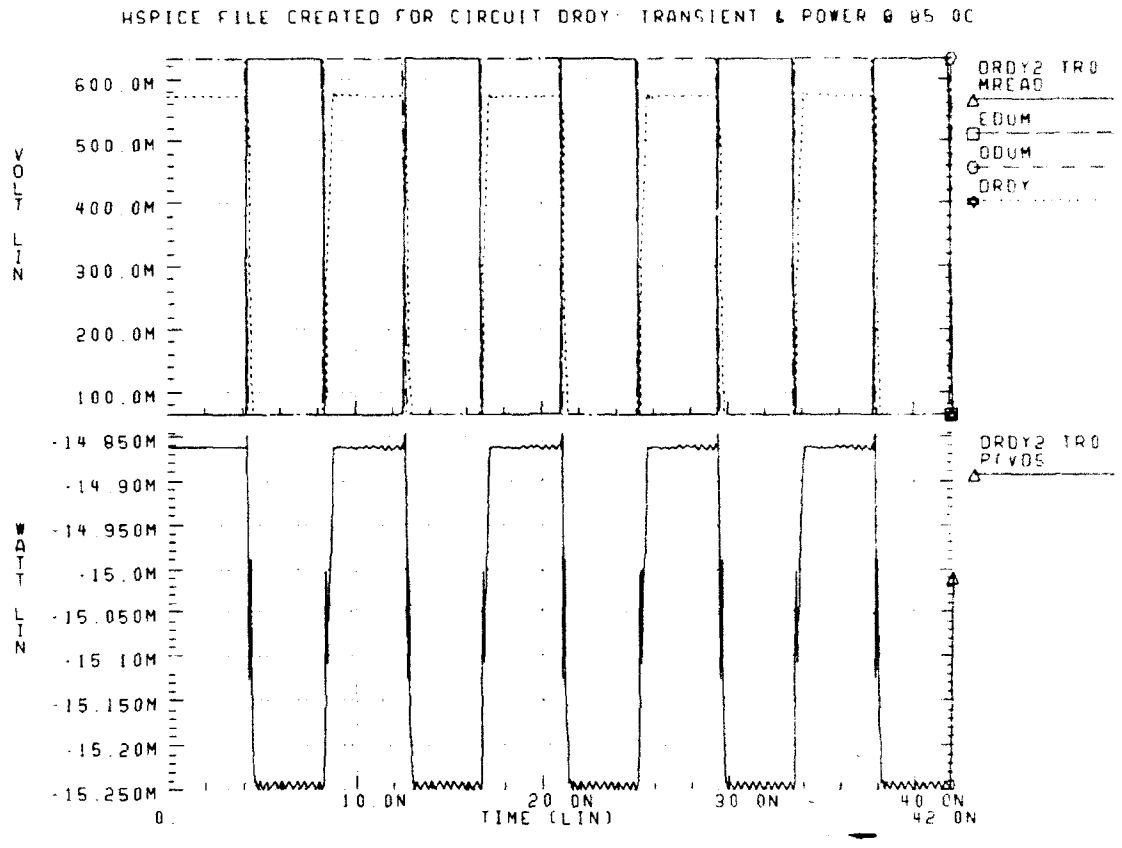


Figure 5.49 DRDY HSPICE Transient Analysis & Power at 85.0C

J. Write Logic Circuitry (WLOGIC)

The purpose of the write logic (WLOGIC) circuitry is to use the combination of input and control signals, Dx (data bit x), A0 (address bit zero), DAS (data strobe), MWRITE (master write), and PH2 (phase two of the GaAs DRAM clock) to control the actions of the pull-up and pull-down transistors attached to both BIO (bit I/O lines) to force the BIO lines to the correct voltage state at the WRITE (!) time. This is accomplished quite simply as seen in the following figure, see Figure 5.50 on page 211.

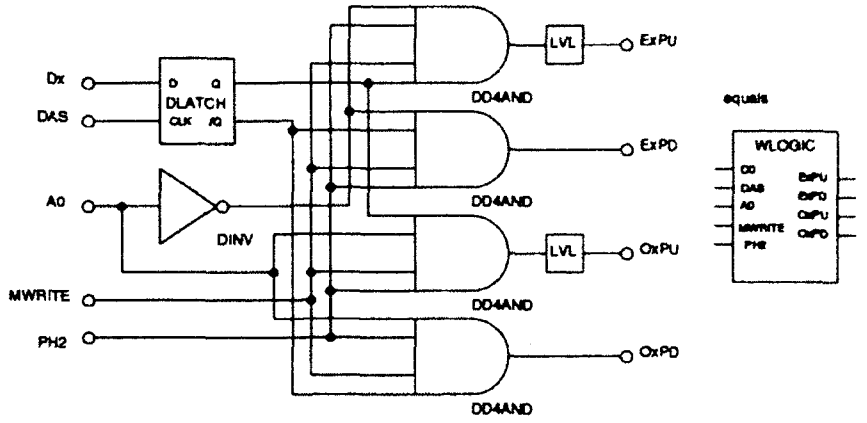


Figure 5.50 WLOGIC Schematic and Logical Equivalence

Examining Figure 5.50, it is seen that first the input data bit (Dx) is latched in the DLATCH by the de-assertion of the input control signal, data strobe (DAS). The master write signal (MWRITE) is then used along with the input address bit zero (A0) combined with the phase two signal of the CLOCK to enable one of the four DD4AND gates shown in Figure 5.50. Referring to [Ref. 8:p. 13], one may see that there are four GaAs MESFET driving transistors connected to the BIO lines of each memory array. These transistors, even side BIO bit x pull-up (ExPU), even side BIO bit x pull-down (ExPD), odd side BIO bit x pull-up (OxPU), and odd side BIO bit x pull-down (OxPD), serve to drive the appropriate BIO line to the correct data voltage level during a MWRITE cycle so that this appropriate data voltage level is then felt by the associated parallel plate capacitor through the associated access MESFET. Obviously, the circuit should only force the BIO line to the data value during a MWRITE cycle. Less obviously, this portion of the MWRITE cycle occurs during PH2 of the clock.

It is interesting to note that the input data bit may be latched at any time, that is falling edge DAS is the latching signal. Of course, if the input data bit is changed at an inappropriate time, it may cause the MWRITE operation to fail. The level shifters (LVL) associated with the ExPU and OxPU outputs are necessary because the associated driving MESFETs are depletion mode.

The WLOGIC HSPICE transient analysis and power dissipation graphs are shown in the following two figures. The first figure demonstrates the transient operation, input signals, (upper graph), transient operation, output signals (middle graph), and power dissipation (lower graph) of the circuit operating at a nominal temperature of 25.0C, see Figure 5.51 on page 212. See "Listing File for WLOGIC Transient Analysis @ 25.0C" of Appendix A on page 373.

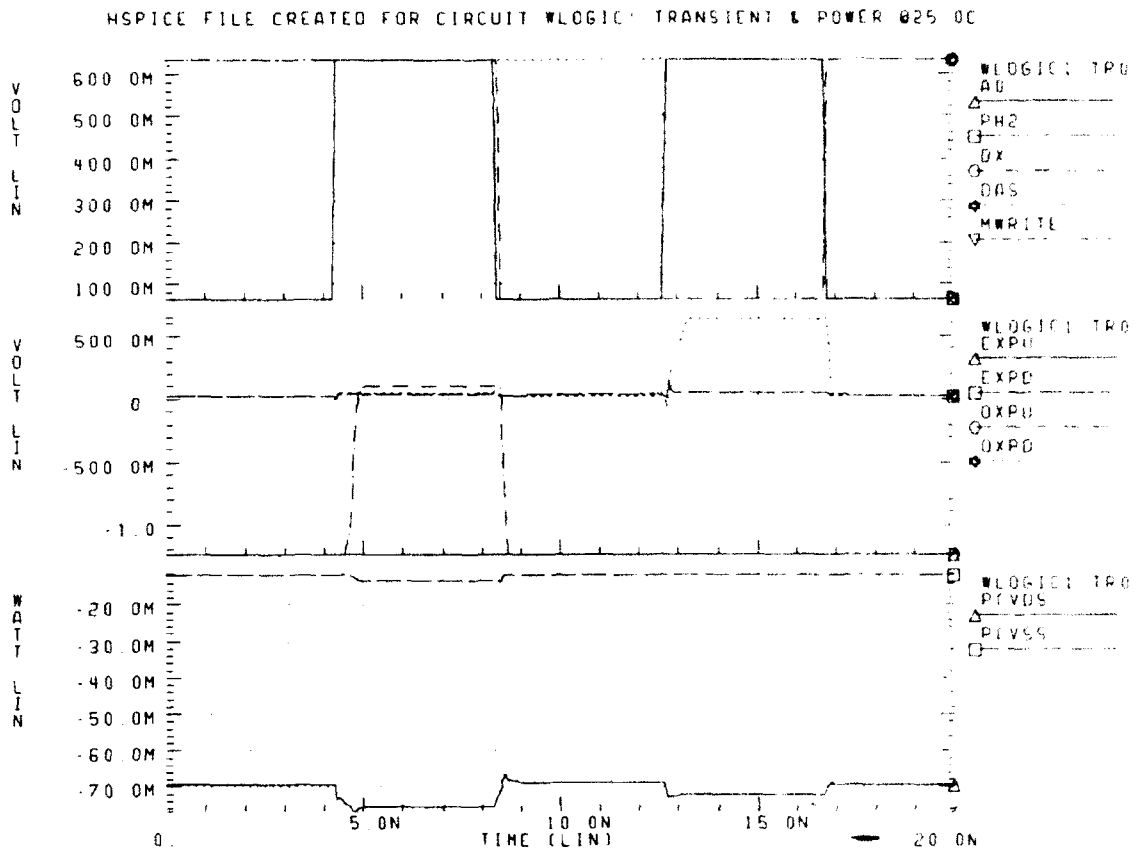


Figure 5.51 WLOGIC HSPICE Transient Analysis & Power at 25.0C

The second part of the WLOGIC HSPICE transient analysis and power dissipation graphs are shown in the following figure. This figure demonstrates the transient operation input signals, (upper graph), transient operation output signals (middle graph), and power dissipation (lower graph) of the circuit operating at a nominal temperature of 85.0C, see Figure 5.52 on page 213.

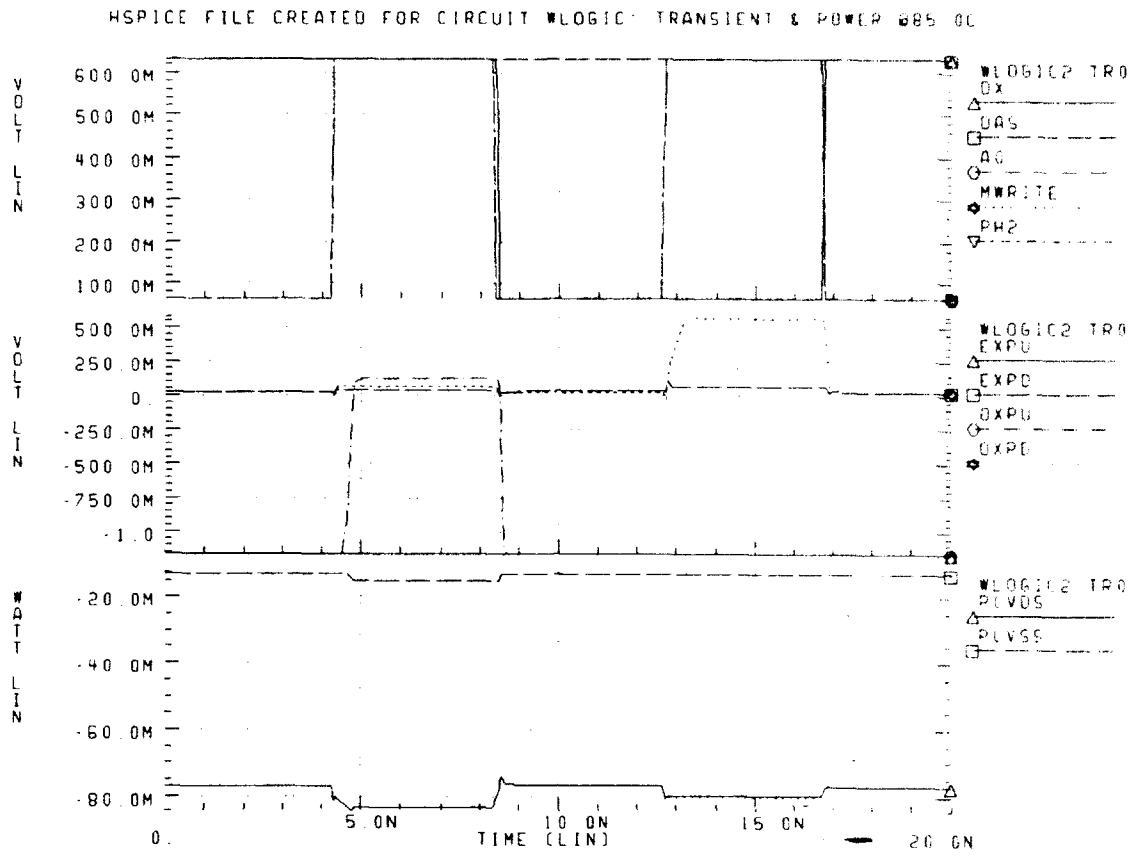
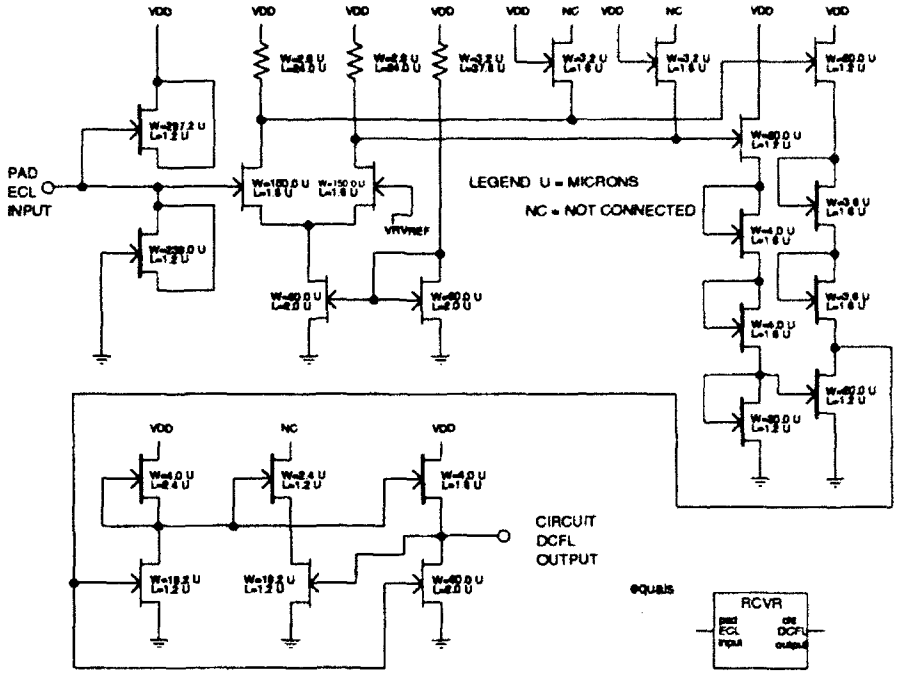


Figure 5.52 WLOGIC HSPICE Transient Analysis & Power at 85.0C

K. Pad Receiver Circuit (PADRCVR)

The pad receiver circuit was provided by Vitesse through MOSIS and further modified by S. Long of UCSB. The purpose of this circuit is to receive a ECL signal through the pad as input, convert it to DCFL and output to the main circuit. As this circuit is not original, the HSPICE transient analysis results are not provided and its correct operation will be validated by the demonstration of the GaAs DRAM in its pad-to-pad HSPICE simulation. For the purpose of completeness, the schematic and logical equivalence for the PADRCVR circuit is shown in Figure 5.53 on page 214.



NOTE 1: Resistors constructed of Active Area GaAs Material

Figure 5.53 PADRCVR Schematic and Logical Equivalence

L. Driver Pad Circuit (DRVRPAD)

The driver pad circuit was provided by Vitesse through MOSIS and further modified by S. Long of UCSB. The purpose of this circuit is to receive a DCFL signal from the main circuit as input, convert it to ECL and output it through the pad off-chip. As this circuit is not original, the HSPICE transient analysis results are not provided and its correct operation will be validated by the demonstration of the GaAs DRAM in its pad-to-pad HSPICE simulation. For the purpose of completeness, the schematic and logical equivalence for the DRVRPAD circuit is shown in Figure 5.54 on page 215.

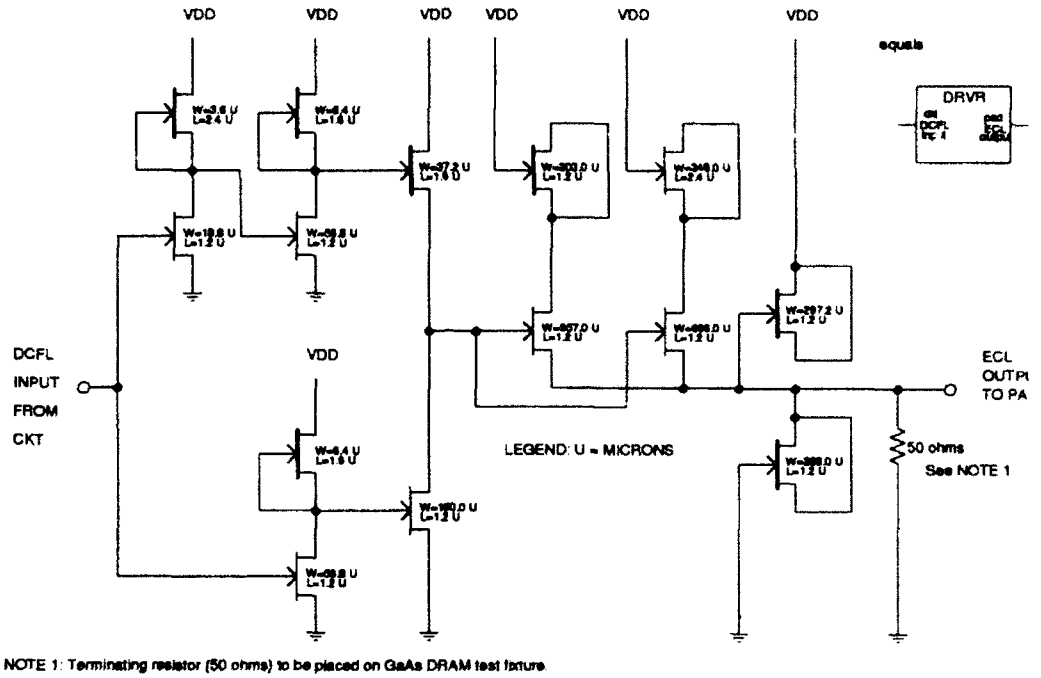


Figure 5.54 DRVRPAD Schematic and Logical Equivalence

M. GaAs DRAM Array (RAM_ARRAY)

The last major circuit to be mentioned in this chapter is the center point of the work by Vagts [Ref. 8]. This circuit is the GaAs DRAM array (RAM_ARRAY). This report will offer only a block diagram of this circuit and will demonstrate its transient analysis in the next chapter as part of the complete design. See Figure 5.55 on page 216 for the GaAs DRAM array as coupled with the circuits OUTPUT and WLOGIC.

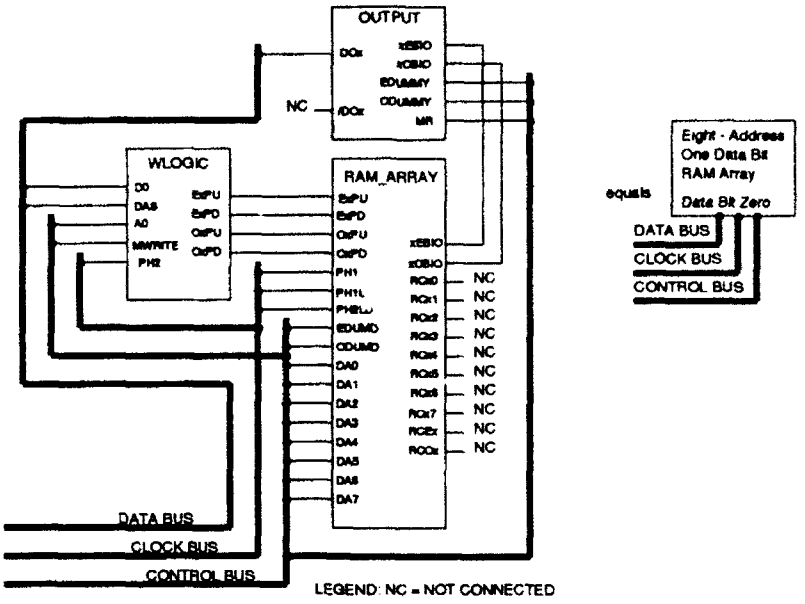


Figure 5.55 RAM_ARRAY Block Diagram

TABLE 5.1 GaAs DRAM HIGH-LEVEL CIRCUITS OPERATING CHARACTERISTICS

Circuit Name	t_{PHL} (ps)	t_{PLH} (ps)	t_{RISE} (ps)	t_{FALL} (ps)	$\overline{t_{DELAY}}$ (ps)	Avg pwr (watts)
CLOCK @25.0C	727	390	142	765	713	0.315
CLOCK @85.0C	663	353	128	845	656	0.320
DECODER @25.0C	326	555	286	204	555	0.125
DECODER @85.0C	287	542	373	287	542	0.127
COUNTER @25.0C	1117	500	655	254	1114	0.276
COUNTER @85.0C	1091	468	562	285	1049	0.302
DREFRESH @25.0C	1205	1044	355	132	1006	0.437

TABLE 5.1 GaAs DRAM HIGH-LEVEL CIRCUITS OPERATING CHARACTERISTICS

Circuit Name	t_{PHL} (ps)	t_{PLH} (ps)	t_{RISE} (ps)	t_{FALL} (ps)	t_{DELAY} (ps)	Avg pwr (watts)
DREFRESH @85.0C	1145	975	313	160	951	0.475
DECODDRVER @25.0C	1280	1018	505	236	1281	0.271
DECODDRVER @85.0C	1291	984	431	275	1275	0.288
OUTPUT @25.0C	1044	585	541	389	575	0.082
OUTPUT @85.0C	1029	571	510	454	592	0.090
WRITEP @25.0C	128	143	394	163	130	0.021
WRITEP @85.0C	127	139	393	173	146	0.023
MBSY @25.0C	222	120	350	138	116	0.005
MBSY @85.0C	221	112	368	166	123	0.005
DRDY @25.0C	201	179	356	139	171	0.014
DRDY @85.0C	208	153	324	157	173	0.015
WLOGIC @25.0C	85	242	426	89	483	0.071
WLOGIC @85.0C	75	228	417	93	444	0.079

VI. GALLIUM ARSENIDE DRAM

This chapter will present the operation and validation of the GaAs DRAM design. Such topics as the overall logic block diagram, layout block diagram, timing for each memory operation and pad to pad simulation results will be discussed and supporting figures will be provided. Additionally, at the end of this chapter, there is a section which summarizes the characteristics of these memory operations.

A. Overall Block Diagram

The following figure is the overall block diagram of the GaAs DRAM memory, see Figure 6.1 on page 218.

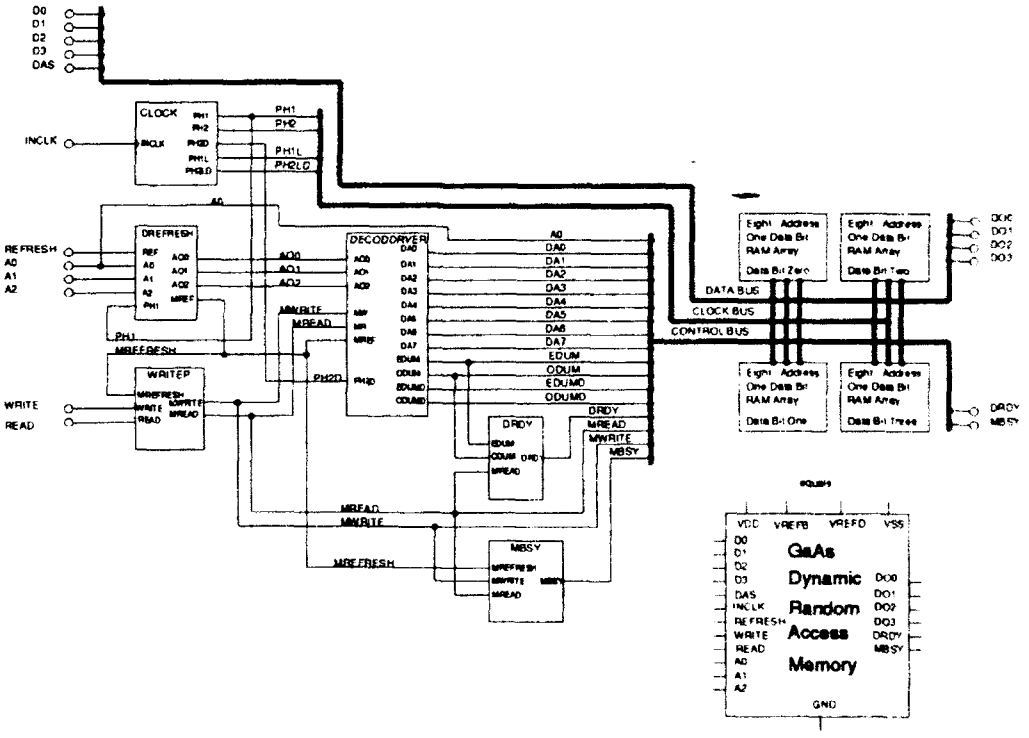


Figure 6.1 GaAs DRAM Overall Logic Block Diagram

This overall block diagram shows the 12 external inputs and the six external outputs. Each block of the block diagram was previously discussed in Chapter 5. The next figure shows the layout block diagram, see Figure 6.2 on page 219.

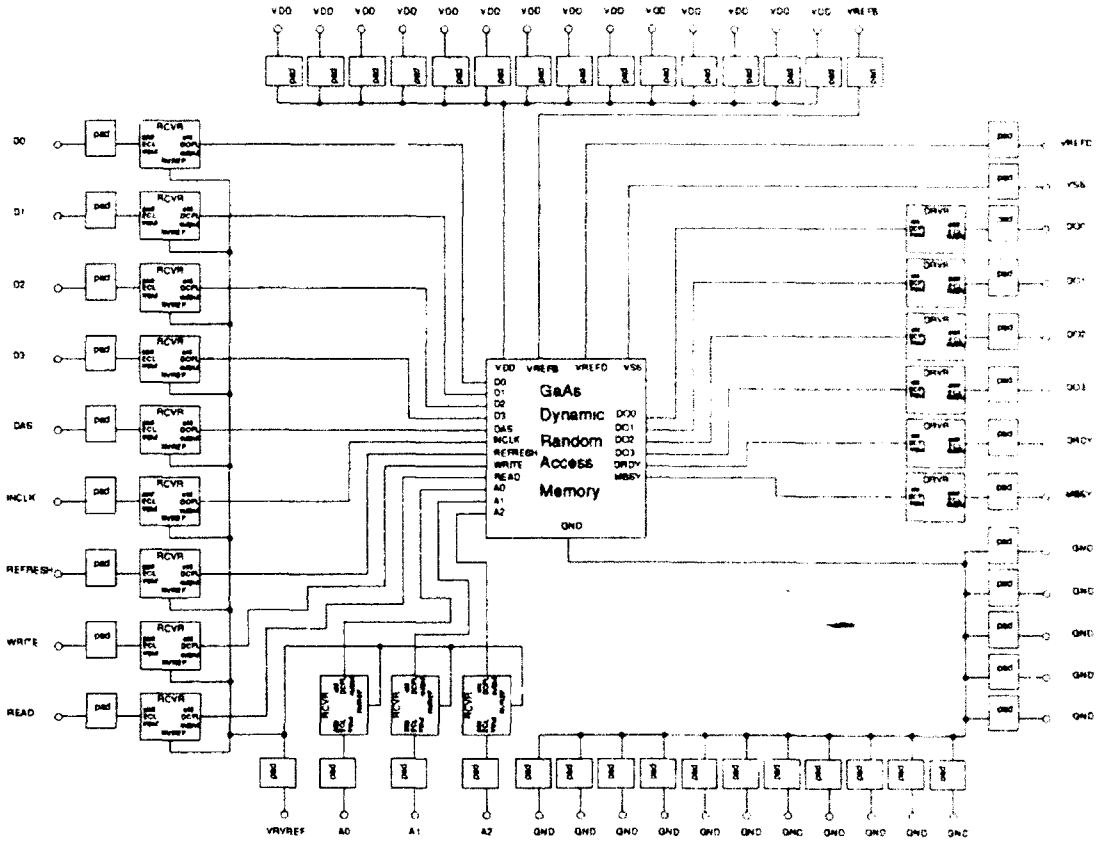


Figure 6.2 GaAs DRAM Layout Block Diagram

B. Layout Block Diagram

Figure 6.2 shows the layout block diagram with all 52 I/O pads. While the actual layout has the various power and ground pads (connections) distributed nearly evenly around the chip, this figure has these pads grouped to facilitate easier understanding. There are maximum current limitations per pad. For both the ground and the main power supply (V_{DD}), the current path and the return current path for the entire design must be distributed over a sufficient number of pads. The actual maximum current values per pad are provided

by the fabrication facility and this information is likely to be considered proprietary. The power consumption testing of the entire design yielded figures which dictated the assignment of 14 pads for V_{DD}, 16 pads for GND, one pad for each of the other various necessary power supplies: VREFB, VREFD, V_{SS}, and VRVREF. The power supply VRVREF is used only to provide a reference voltage for the pad receivers, see Figure 5.53 on page 214. The purpose of the reference voltages VREFB and VREFD are discussed in the work by Vagts [Ref. 8:p. 14], these two power supplies are used in the operation of the GaAs Dynamic RAM_ARRAY. The power supply, V_{SS}, is used by the level shifter (LVL) circuits, see Figure 4.166 on page 154.

One may also notice from both of the block diagrams, Figure 6.1and Figure 6.2, the inputs and outputs. The next two subsections will discuss each input and output. It should be mentioned again that the external signals, inputs and outputs, are at ECL levels, which equate to a positive logic LOW = 0.4 volts and a positive logic HIGH = 1.1 volts. These ECL levels are used because the vendor supplied pad drivers and pad receivers are designed specifically for ECL logic levels, see Figure 5.53 on page 214 and Figure 5.54 on page 215.

1. **INPUTS**

Data Bits (D3 - D0): These data inputs are level asserted signals, latched inside the WLOGIC circuitry.
Data Strobe (DAS): This level asserted control signal informs the input data latches (in the WLOGIC circuitry) that the input data bits are present and stable on the input data lines.
Address Bits (A2 - A0): These address data inputs are level asserted, non-latched signals applied to the DECODDRVR circuitry.
Clock (INCLK): This input control signal provides the basic timing reference to the two-phase, non-overlapping CLOCK circuitry.
Refresh (REFRESH): This pulse asserted input control signal, latched by the DREFRESH circuitry, dictates the start timing of the necessary GaAs DRAM refresh operation.
Write (WRITE): This level asserted, non latched, input control signal indicates the request for a GaAs DRAM write operation. It is applied to the operation priority (WRITEP) circuitry.
Read (READ): This level asserted, non-latched, input control signal indicates the request for a GaAs DRAM read operation. It is applied to the operation priority (WRITEP) circuitry.

2. **OUTPUTS**

Data Bits (DO3 - DO0): These data outputs are level asserted, latched signals which originate in the output logic (OUTPUT) circuitry.
Memory Busy (MBSY): This level asserted, non-latched, control signal originates in the memory busy (MBSY) circuitry. It indicates that the GaAs DRAM is busy with a read, write, or refresh operation.
Data Ready (DRDY): This level asserted, non-latched, control signal originates in the data ready (DRDY) circuitry. It indicates that the data fetched during the most recently requested read operation is available on the output data lines.

C. Timing and Pad->Pad Simulation

This section will discuss and demonstrate each of the three GaAs DRAM memory operations, WRITE, READ, and REFRESH. It should be mentioned that for the HSPICE execution of the GaAs DRAM pad to pad simulation, the ".options FAST" was used. This HSPICE option, FAST, results is a less stringent set of accuracy requirements for each HSPICE nodal iteration. Use of the FAST option causes a tremendous decrease in simulation time at the price of reduced accuracy for the results. It was decided that because a pad to pad simulation verifies overall design integrity, it was acceptable for use. As a side-bar, without the use of the FAST option, the required pad to pad simulation time (also using the ".option probe" which restricts the output data file to a maximum number of 32 nodes) executing on the SUN SPARCstation 2, was at least two weeks for a transient analysis of 60ns. Additionally, as a result of the less accurate FAST option, the graphs presented in this chapter in validation of the design of the GaAs DRAM are somewhat "choppy".

The HSPICE pad-pad simulation listing files are included in the listing files appendix for each execution. However, in order to reduce to overall size of the appendix, the second and further listing files for the HSPICE pad to pad simulation of the GaAs DRAM will have the multiple pages of identical HSPICE file data removed, leaving only the unique file data for each simulation run. See "GaAs DRAM HSPICE Pad->Pad Simulation" on page 379.

1. WRITE OPERATION

This section will discuss and demonstrate the execution of a GaAs DRAM WRITE operation. As a reminder, the external inputs and outputs are at ECL logic levels. The first graph, see Figure 6.3 on page 222, has two panels. The first (upper) panel shows the address input signals, A2 - A0, and the data strobe, DAS), signal. The input address bits are set to equal address five and the data strobe signal is set to a level logic HIGH. The second (lower) panel shows the data input signals, D3 - D0. These are set to equal 1101 in binary with MSB first, that is, D3=1, D2=1, D1=0, and D0=1.

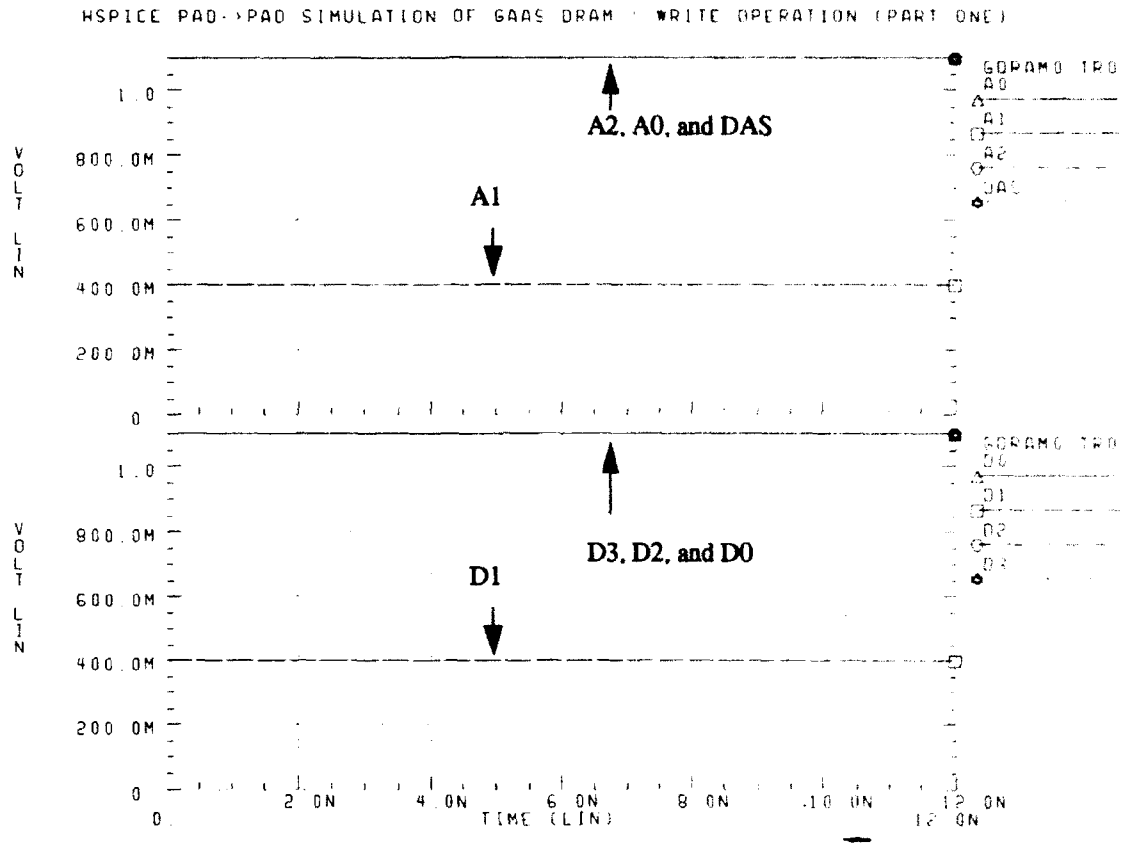


Figure 6.3 GaAs DRAM WRITE Operation at 25.0C (Part One)

The next figure, see Figure 6.4 on page 223, in the series presenting the WRITE operation shows the germane control signals, WRITE, MWRITE, READ, MREAD, PH1 and PH2. Notice that the x axis (time in nanoseconds) has been restricted to a zoom window of the period 2ns to 12ns. One may see the correct operation of the WRITEP circuitry, which establishes GaAs DRAM memory operation precedence, in this case, the WRITE has precedence over the READ. Notice also that as soon as the WRITE operation is completed (as signalled externally, albeit, somewhat artificially, by de-asserting the WRITE signal), the READ operation begins as indicated by the assertion of MREAD.

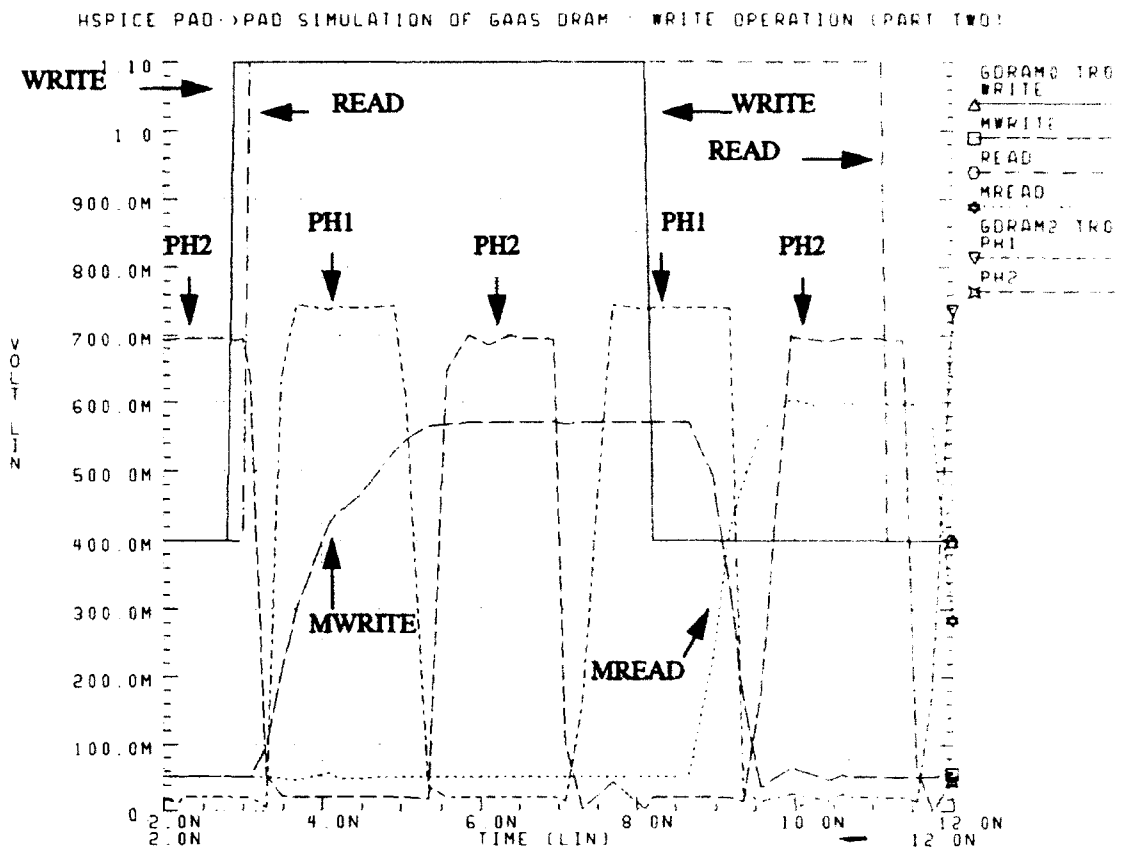


Figure 6.4 GaAs DRAM WRITE Operation at 25.0C (Part Two)

It should be noted at this point that, with regard to the timing of these memory operations, phase one (PH1) of the clock circuit exists almost entirely for the purposes of equalization and pre-charging operations within the RAM_ARRAY, see [Ref. 8:p. 12]. There is only one exception to this timing scheme and that is in the DREFRESH circuit. The exception will be fully discussed during the REFRESH operation of this chapter. Phase two of the GaAs DRAM clock timing scheme is the phase during which everything external to the RAM_ARRAY occurs (with the one exception noted). During the phase two (PH2) shown in Figure 6.4 the writing of the data occurs. In the next figure, see Figure 6.5 on page 224, the actual charge contents of the target memory addresses will be presented.

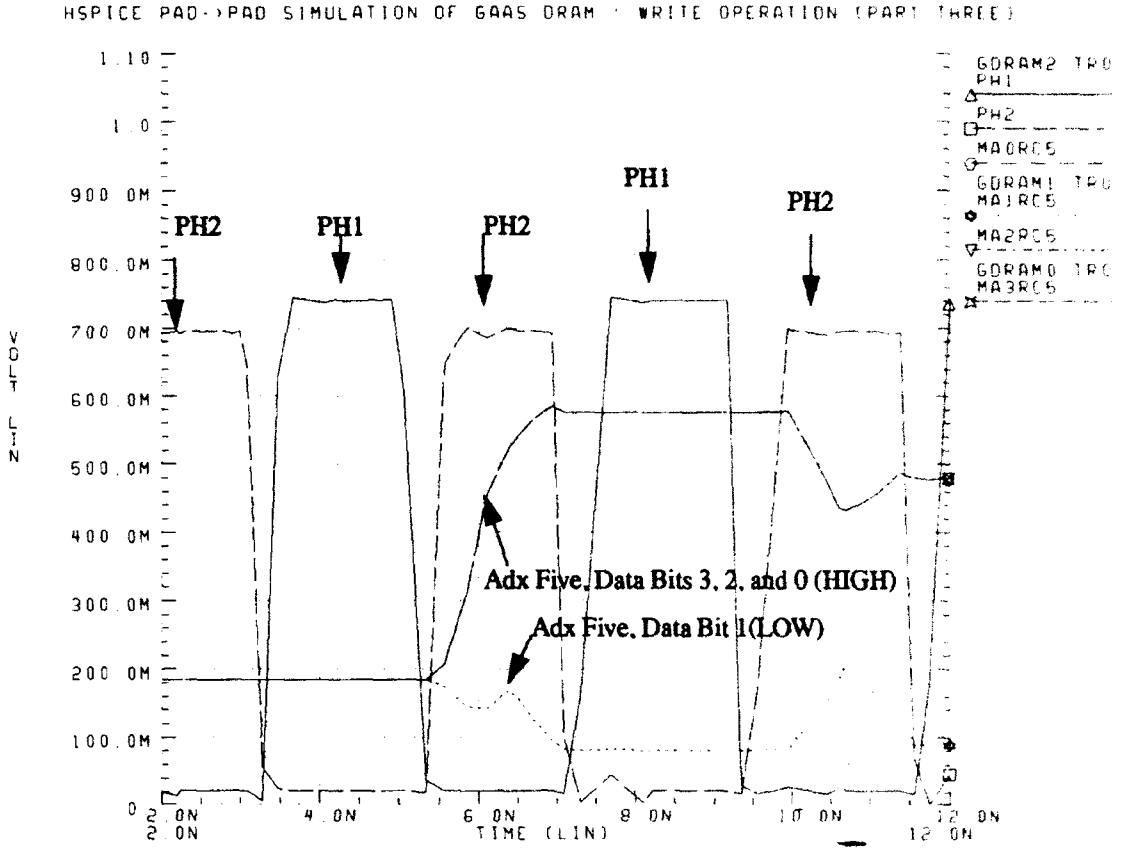


Figure 6.5 GaAs DRAM WRITE Operation at 25.0C (Part Three)

Looking at Figure 6.5, one sees, during the PH2 clock pulse at ~ 6.0 nanoseconds, the actual writing on the input data into the target address five. The activity shown during the PH2 clock pulse at ~11.0 nanoseconds, is a result of the READ operation which is the next topic to be discussed.

The next three figures demonstrate the same WRITE operation signals but at a simulation nominal temperature of 85.0C. See Figure 6.6 on page 225, Figure 6.7 on page 226, and Figure 6.8 on page 227.

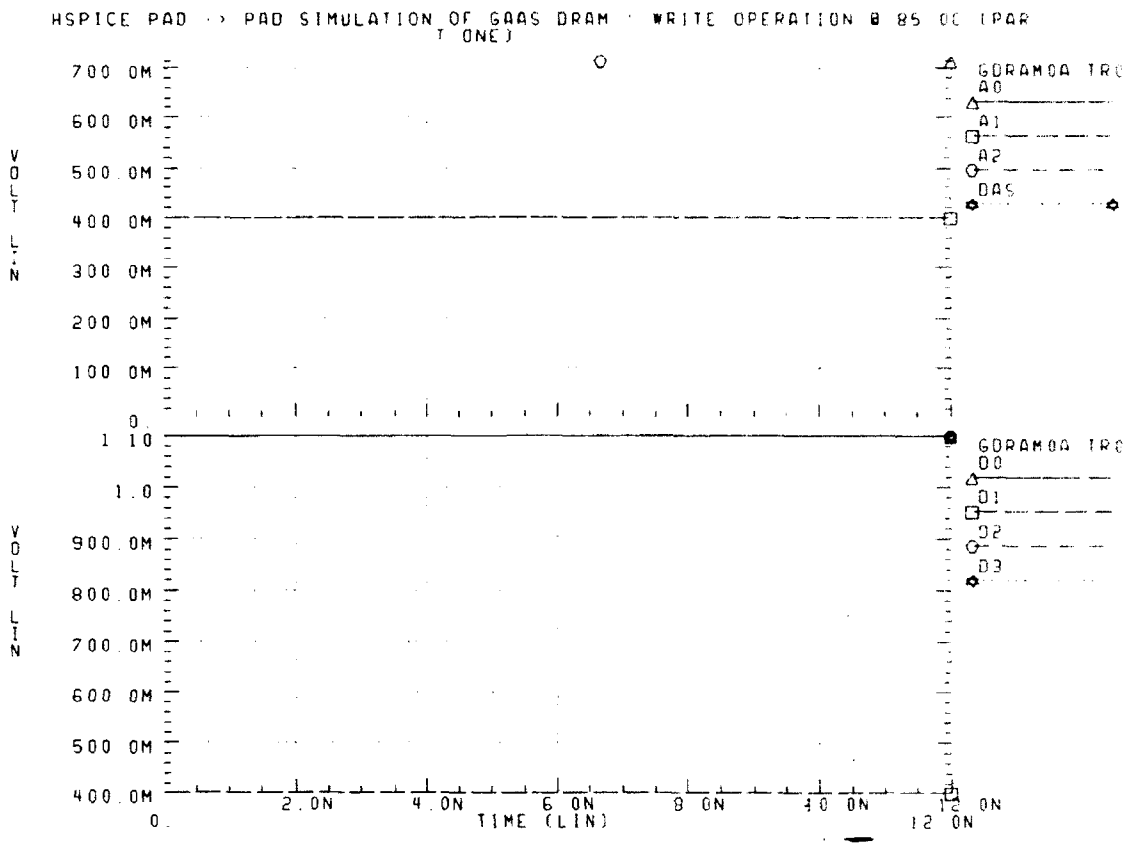


Figure 6.6 GaAs DRAM WRITE Operation at 85.0C (Part One)

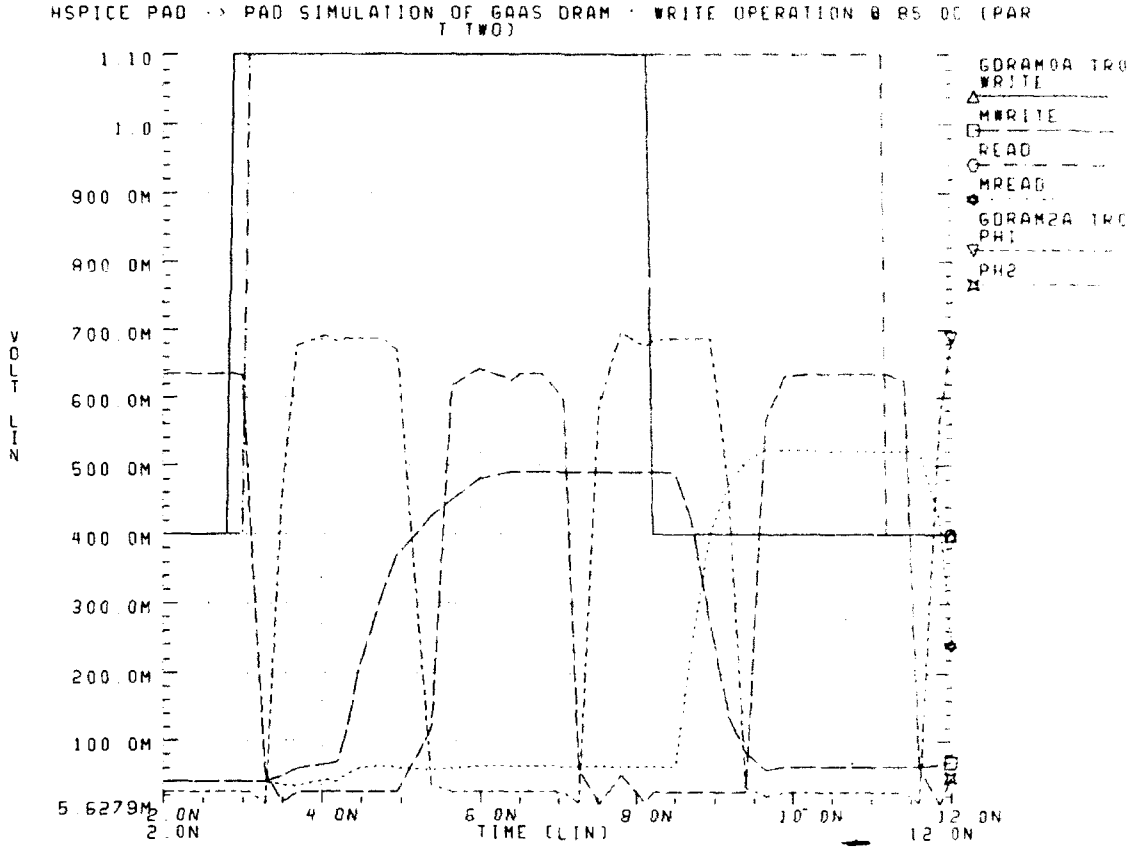


Figure 6.7 GaAs DRAM WRITE Operation at 85.0C (Part Two)

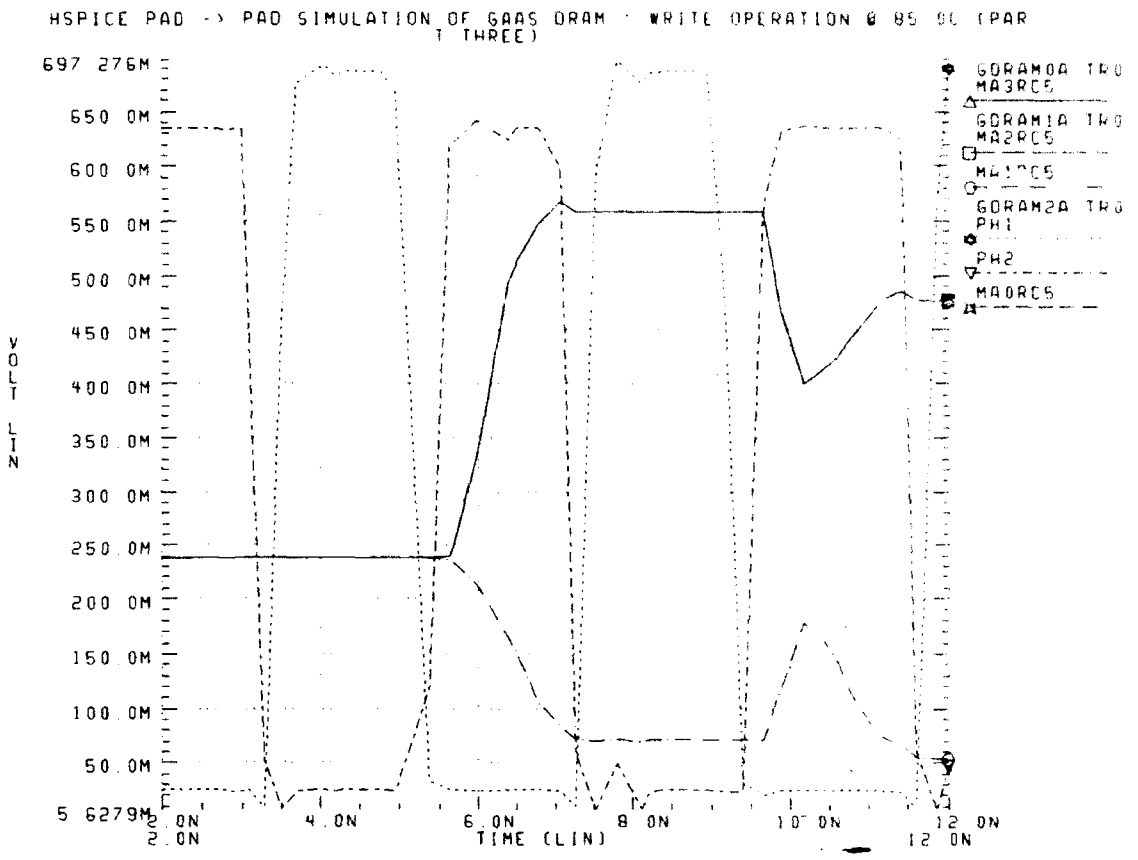


Figure 6.8 GaAs DRAM WRITE Operation at 85.0C (Part Three)

2. READ OPERATION

This section will discuss and demonstrate the execution of a GaAs DRAM READ operation. This READ operation occurs immediately after the previously mentioned WRITE operation so that the address and data parameters are the same. The first graph, see Figure 6.9 on page 228, shows the basic control signals of READ, MREAD, PH1, and PH2.

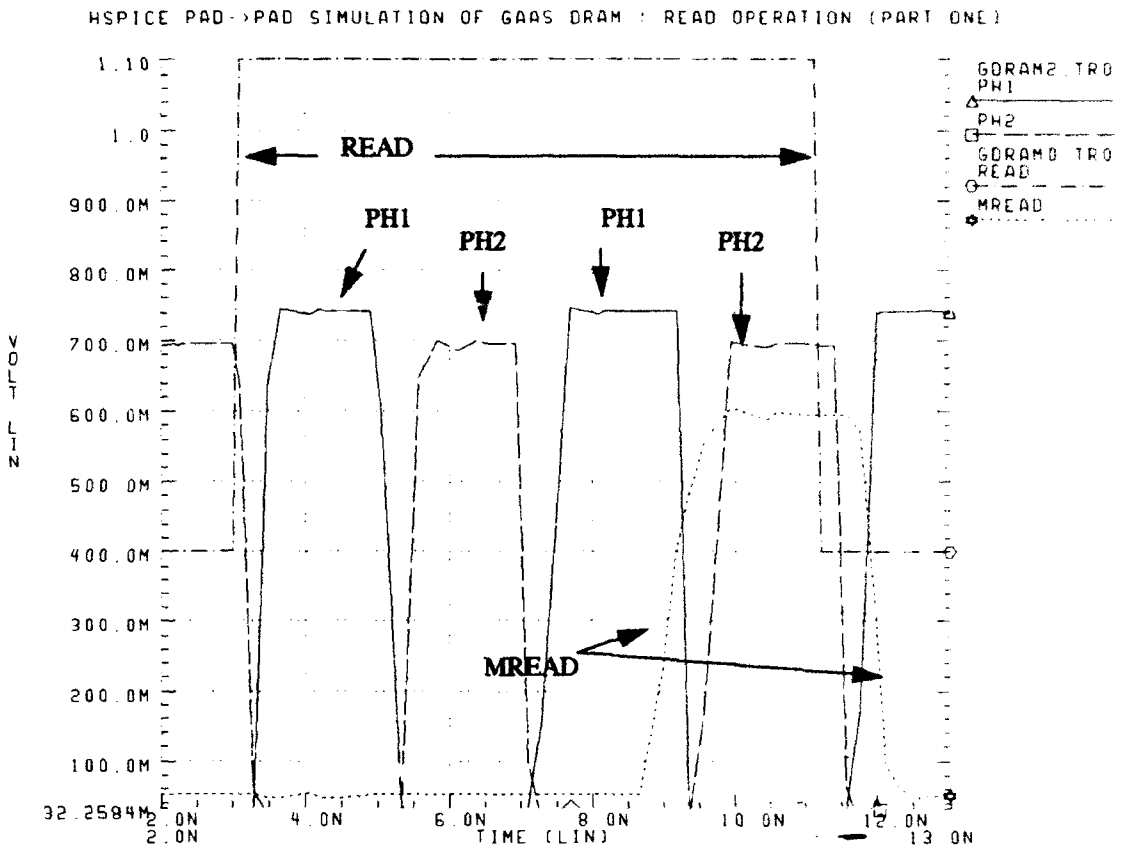


Figure 6.9 GaAs DRAM READ Operation at 25.0C (Part One)

Referring to Figure 6.9, the delay between the assertion of the external control signal READ and the assertion of the internal control signal MREAD occurs due to the preceding WRITE operation. In addition, notice that the x axis (time in nanoseconds) has again been restricted to a zoom window of the period 2 nanoseconds to 13 nanoseconds. The next figure, see Figure 6.10 on page 229, shows the basic internal control signals, MREAD and PH2, plus the actual charge contents of the target address, MA3RC5, MA2RC5, MA1RC5, and MA0RC5.

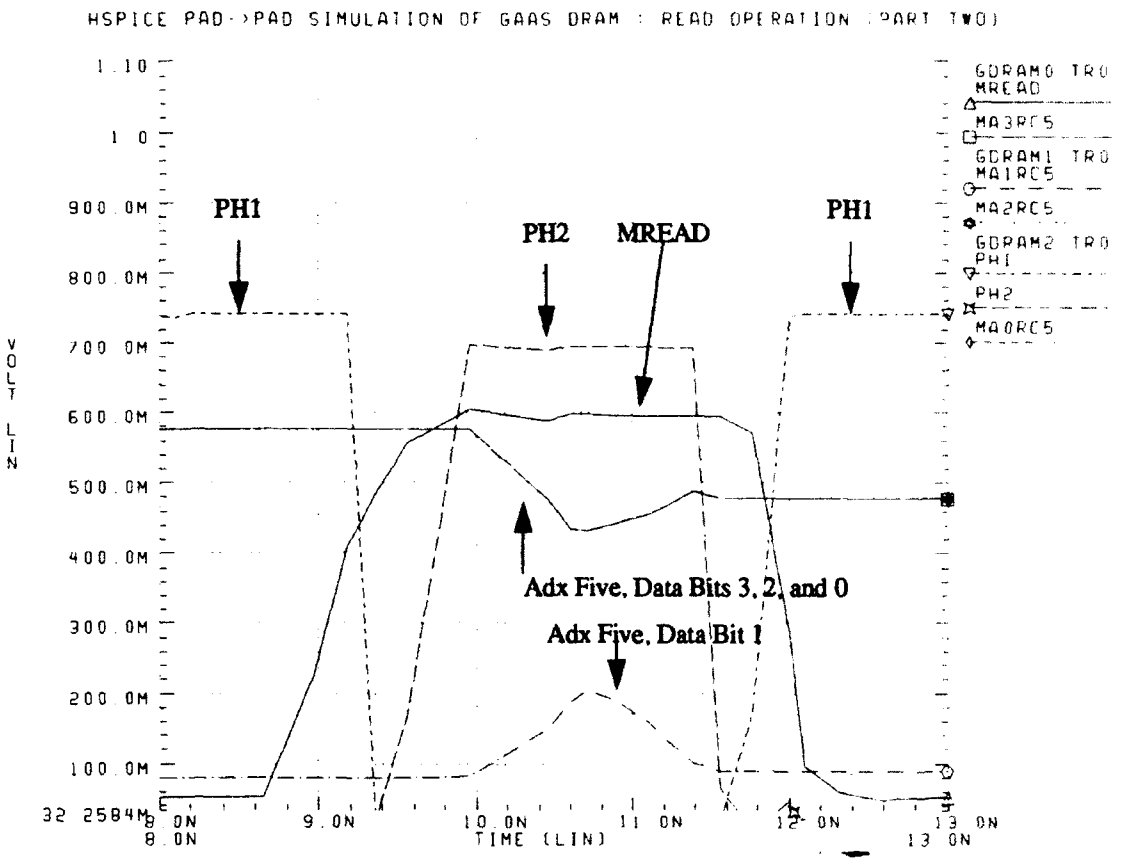


Figure 6.10 GaAs DRAM READ Operation at 25.0C (Part Two)

It may be seen in Figure 6.10, that the charge contents of the target address initially "dip" and recover to nearly their original charge levels during the READ operation. The reasons behind this phenomenon are thoroughly discussed in the works by Vagts [Ref 8:p. 14]. The next figure, see Figure 6.11 on page 230, demonstrates the operation of the two external control signals, memory busy (MBSY) and data ready (DRDY).

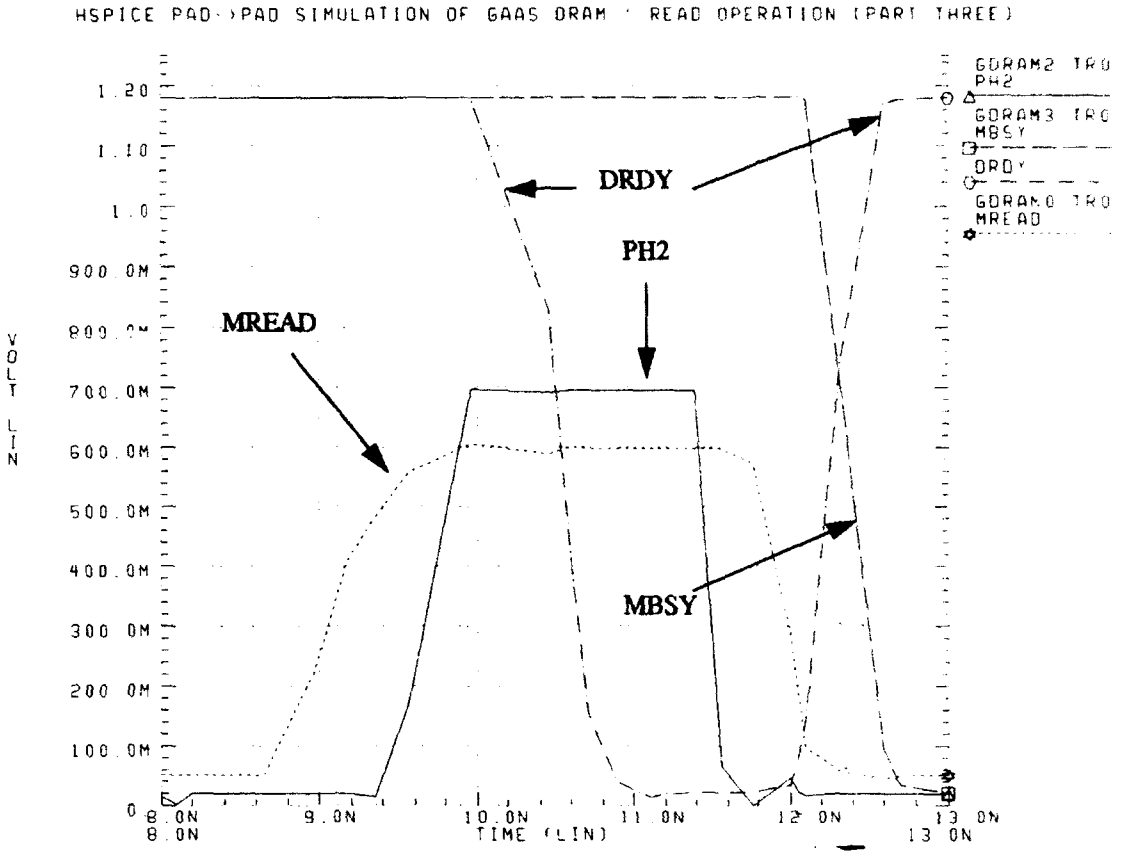


Figure 6.11 GaAs DRAM READ Operation at 25.0C (Part Three)

Examining Figure 6.11, it is seen that memory busy (MBY) is initially HIGH indicating that the GaAs DRAM memory is busy performing a requested operation and that upon completion of the READ operation, the MBSY signal is de-asserted. Also, the data ready (DRDY) signal is initially asserted which indicates off-chip that the data from the most recently requested READ operation is still valid on the output data lines. Once the READ operation commences as synchronized to the leading edge of the EDUM or ODUM signals (not shown), DRDY is momentarily de-asserted until the completion of the latching of the output data. The next figure, see Figure 6.12 on page 231, shows the output data lines and the output control signals, MBSY and DRDY.

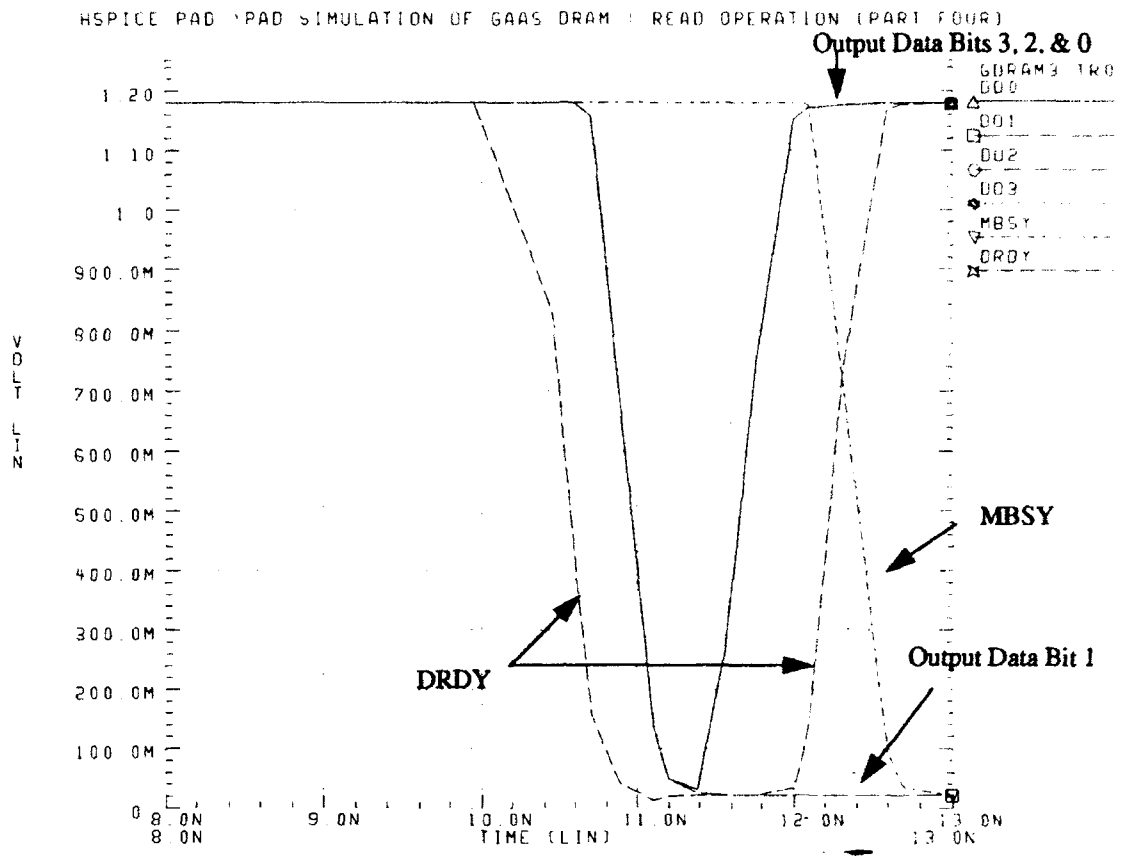


Figure 6.12 GaAs DRAM READ Operation at 25.0C (Part Four)

Referring to Figure 6.12, it may be seen that the output data lines indicate the last READ operation returned data values equal to D3 = 1, D2 = 1, D1 = 0, and D0 = 1. This is a correct result based on the input data previously written to the GaAs DRAM memory. Notice also that the DRDY signal is not asserted until the output data is latched and steady.

With regard to the overall operational precedence and in view of the fact that the input control signals WRITE and READ are not latched, it must be noted that if, in the midst of a READ or WRITE operation, a REFRESH is asserted then depending on the timing (and luck!), the READ or WRITE operation in progress may be "trounced" and become invalid. This control design shortcoming should be addressed in revisions to the design.

The next four figures demonstrate the same READ operation signals but at a simulation nominal temperature of 85.0C. See Figure 6.13 on page 232, Figure 6.14 on page 233, Figure 6.15 on page 234, and Figure 6.16 on page 235.

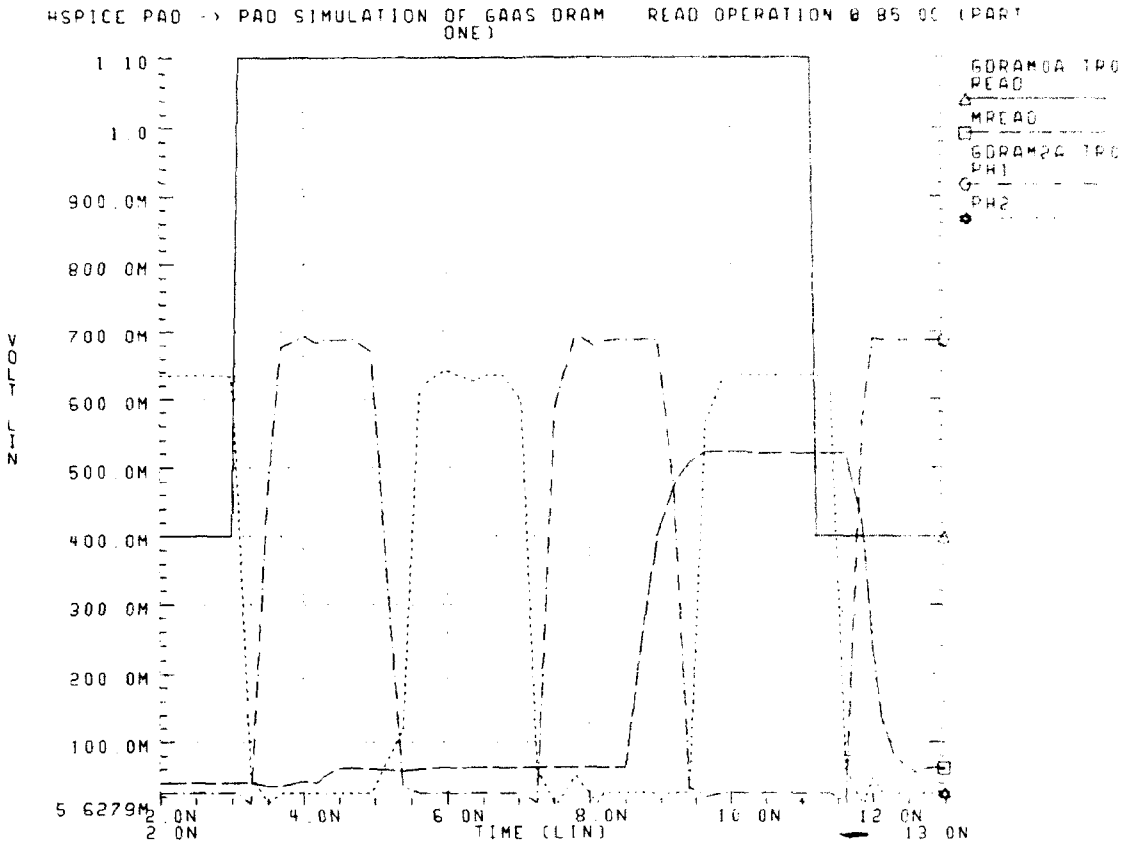


Figure 6.13 GaAs DRAM READ Operation at 85.0C (Part One)

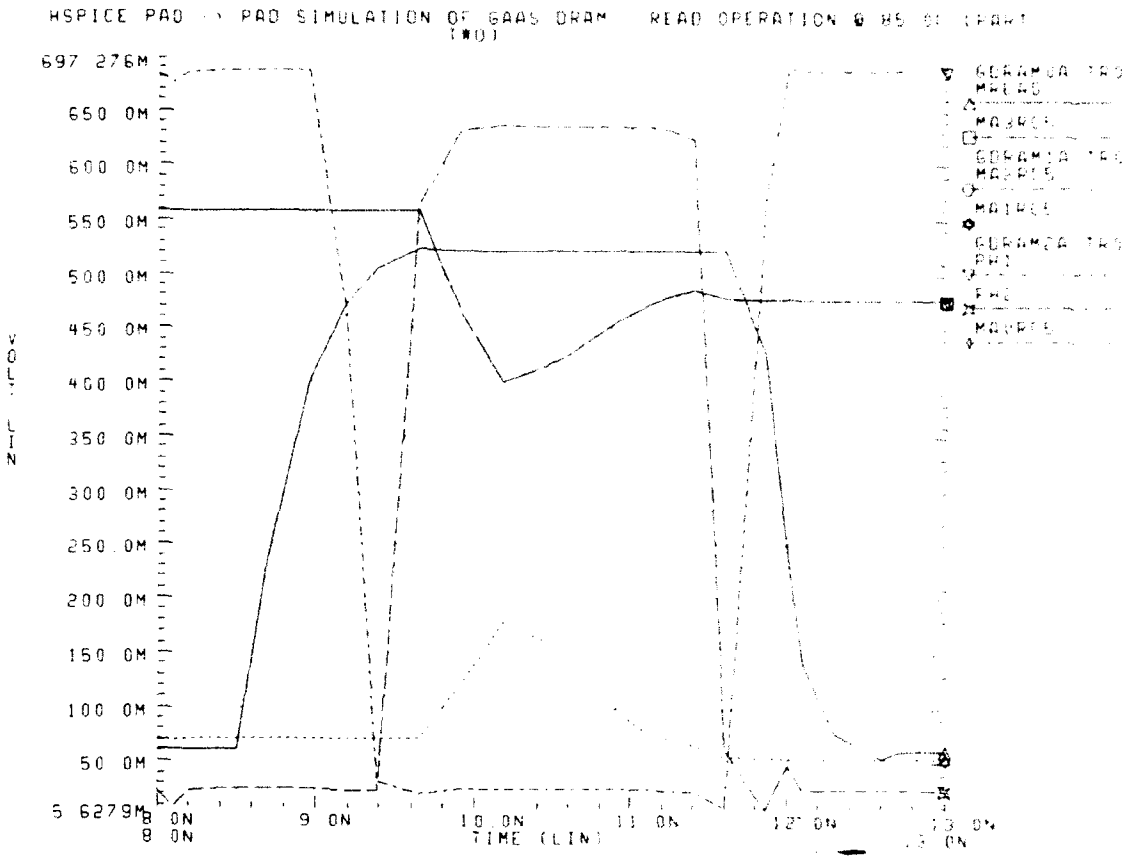


Figure 6.14 GaAs DRAM READ Operation at 85.0C (Part Two)

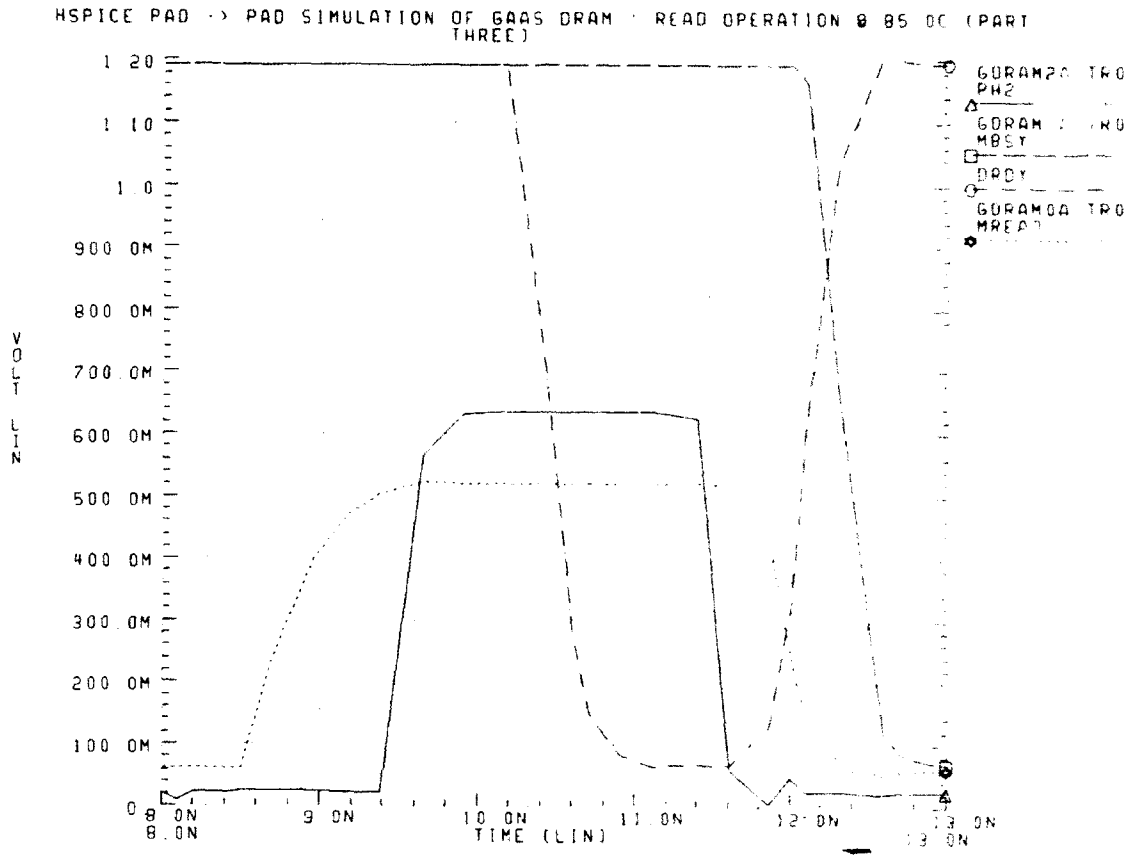


Figure 6.15 GaAs DRAM READ Operation at 85.0C (Part Three)

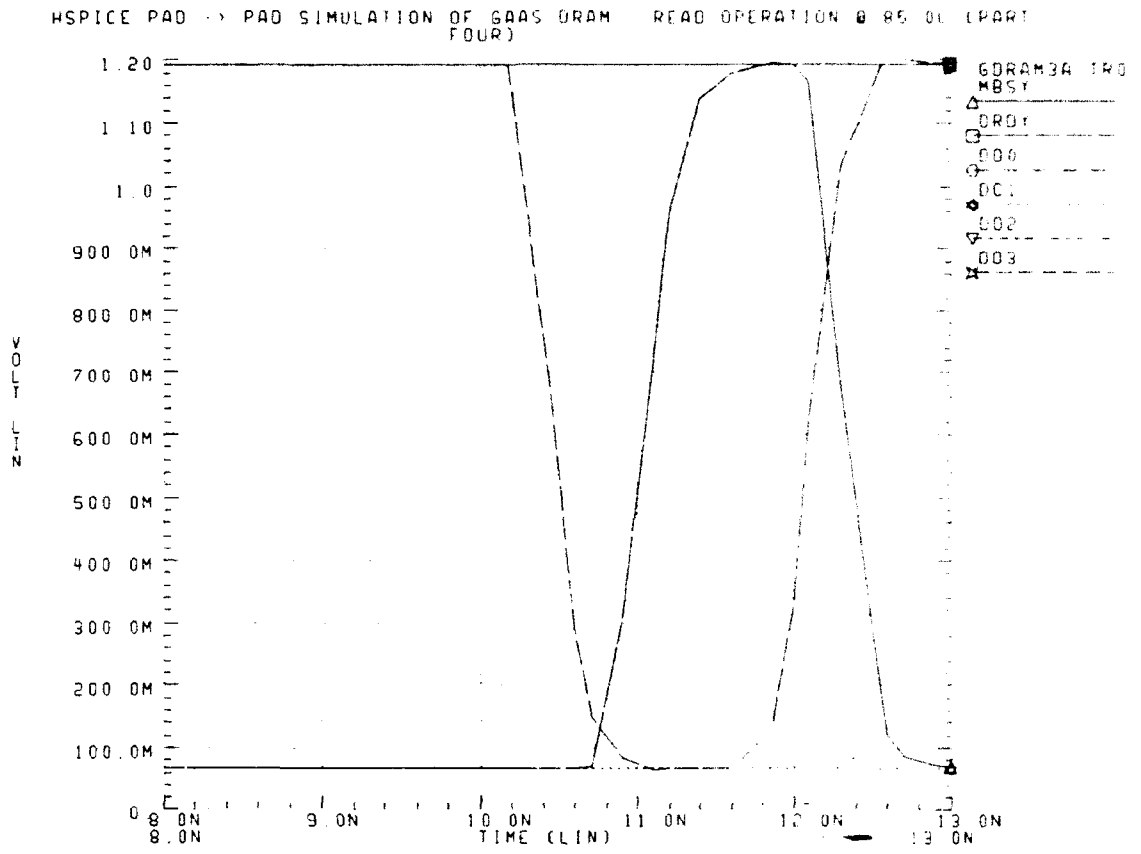


Figure 6.16 GaAs DRAM READ Operation at 85.0C (Part Four)

3. REFRESH OPERATION

This section will discuss and demonstrate the refresh operation which follows the WRITE and then READ in the same HSPICE GaAs DRAM pad to pad simulation execution. The REFRESH logic circuitry was the most difficult to design, as previously discussed in Chapter V. See "DRAM Refresh Circuitry (DREFRESH)" on page 176. The first figure in this discussion of the REFRESH operation, see Figure 6.17 on page 236, presents the control signals associated with REFRESH in the upper graph and the outputs of the DREFRESH circuitry in the lower graph. Notice also that in Figure 6.17, the upper and lower panels are time "zoomed", synchronized graphs such that the PH1 signals in the upper graph also reflect accurately the assertion times of the signals in the lower graph.

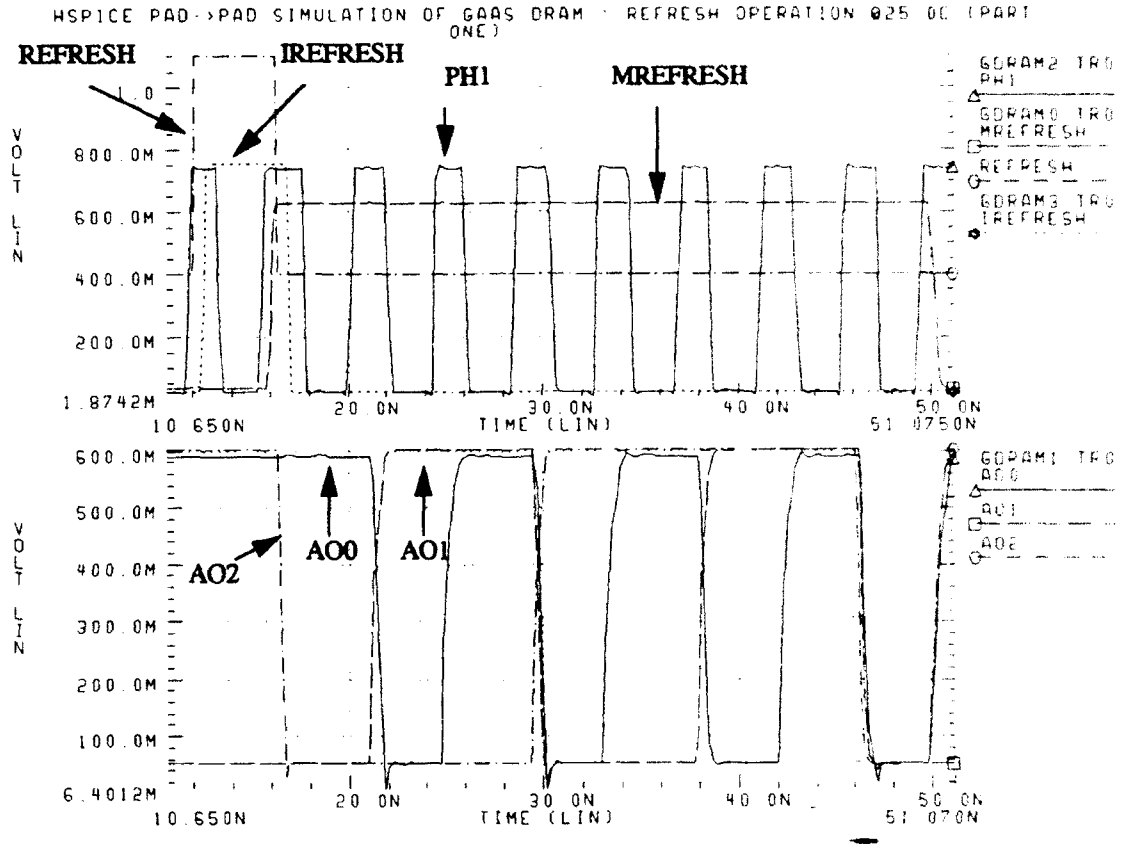


Figure 6.17 GaAs DRAM REFRESH Operation at 25.0C (Part One)

Referring to Figure 6.17 (upper graph), the external control signal REFRESH is asserted at approximately 10.65 nanoseconds and the refresh signal is passed through the pad receiver to become the IREFRESH (Intermediate) signal. The pad receiver propagation delay causes the IREFRESH to just miss the leading edge of the PH1 clock pulse and so MREFRESH does not occur until the next leading edge of the PH1 clock pulse. Those wishing to review the DREFRESH circuitry may see Figure 5.14 on page 177. This is the exception mentioned previously to the fact that almost all the activity that occurs with the GaAs DRAM design but external to the RAM_ARRAY, occurs during the PH2 clock pulse. Once the MREFRESH signal is asserted, the GaAs DRAM commences a refresh operation. The lower graph of Figure 6.17 demonstrates the output signals, AO2 - AO0, of the DREFRESH circuitry. These signals represent the counting sequence output by the DREFRESH circuitry to sequentially access all addresses in the GaAs DRAM memory array. It should be mentioned that the counting sequence does not begin with address zero as one might assume. Per

the previous discussion of HSPICE simulation initial conditions, viewing Figure 6.17, one may see that this is exactly what occurs.

In the DECODDRVR circuitry, the AO2 - AO0 signals coupled with the now asserted MREFRESH signal, causes the sequential assertion of the DRAM address driver signals, DA7 - DA0. Notice that the driver address signals are level shifted as these signals control the depletion mode GaAs MESFET DRAM access transistors. These signals are shown in Figure 6.18 on page 237.

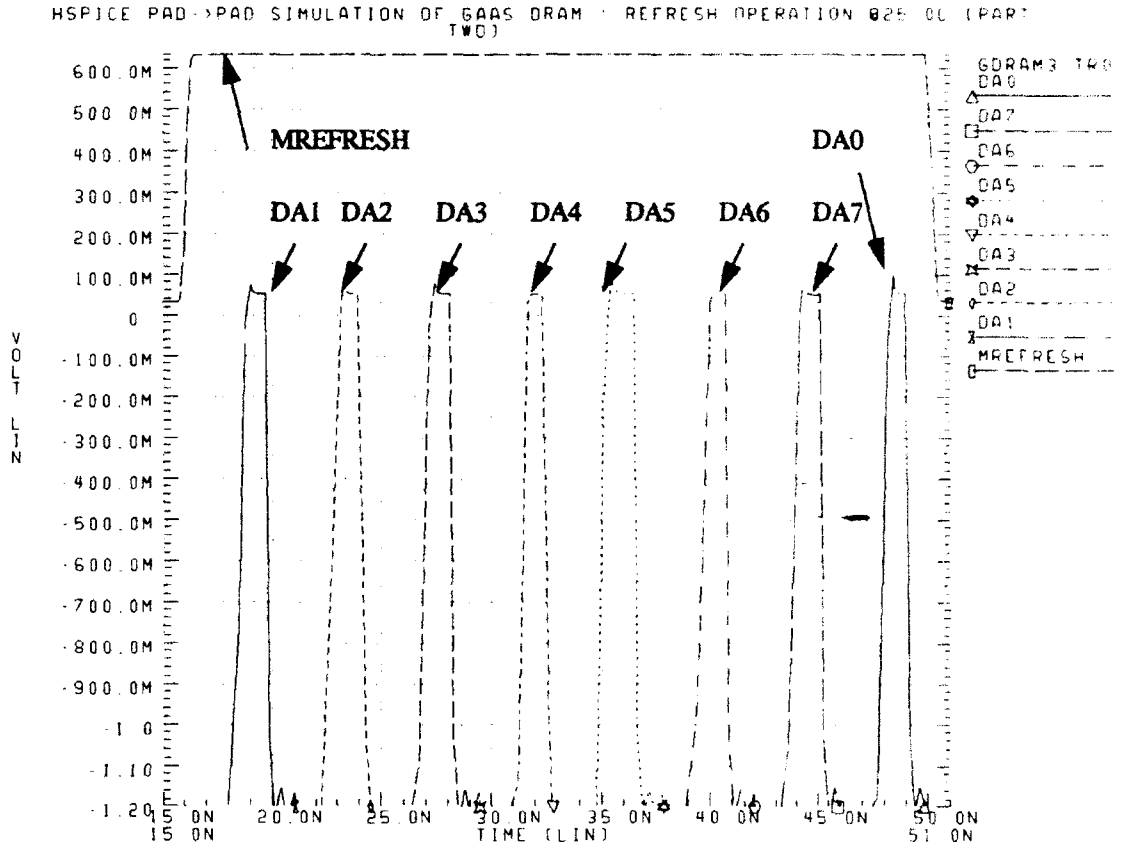


Figure 6.18 GaAs DRAM REFRESH Operation at 25.0C (Part Two)

Examining Figure 6.18, one sees the sequential assertion of the driver address signals, DA1 to DA7 to DA0. Notice again that this graph is x axis specified to display only the time frame of 15.0 nanoseconds to 51.0 nanoseconds. The final graph for the demonstration of the REFRESH operation includes the address five charge contents, the address three charge contents (for non-target comparison purposes), the output control signal MBSY, and several other germane signals, see Figure 6.19 on page 238.

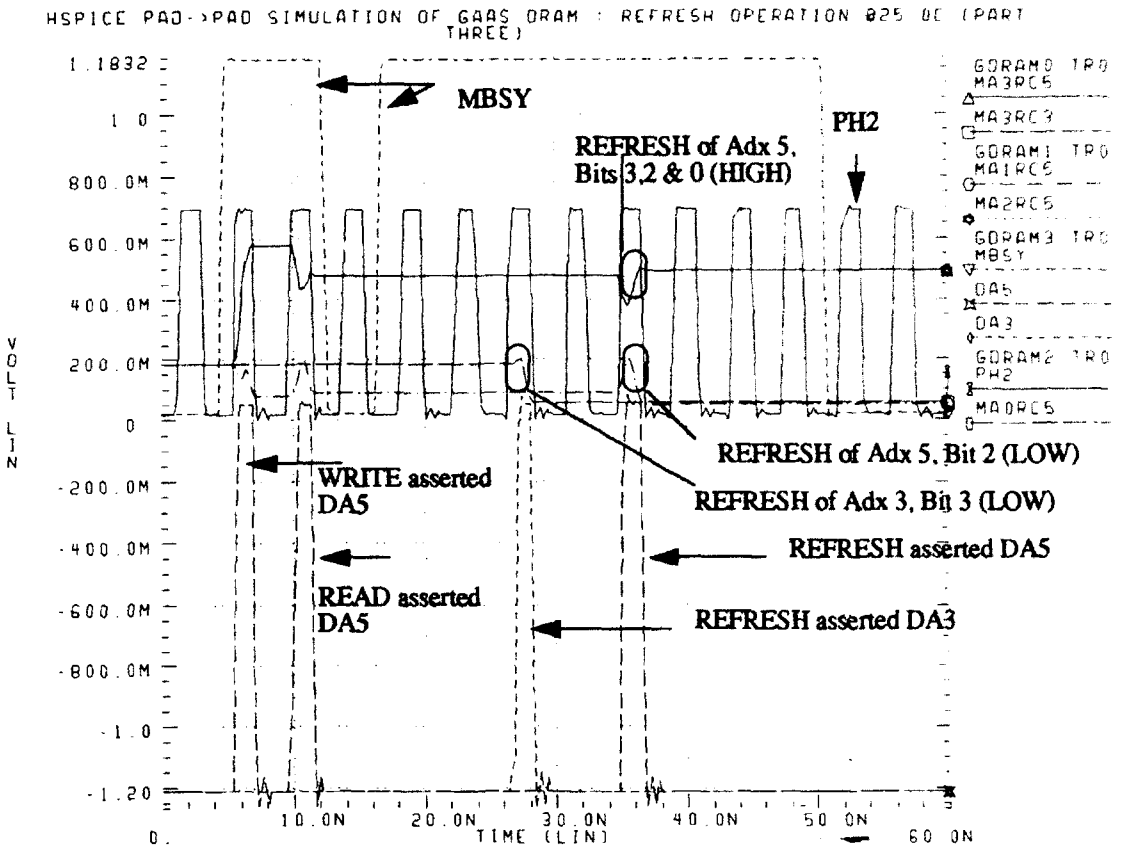


Figure 6.19 GaAs DRAM REFRESH Operation at 25.0C (Part Three)

Viewing Figure 6.19, one can immediately see quite a lot of information. First, the x axis (time in nanoseconds) is not zoom specified so that the entire HSPICE GaAs DRAM simulation interval may be seen. Secondly, the previously discussed WRITE and READ operation effects on address five (the target address) may be seen. Thirdly, the additional, non-target, memory address three charge contents are displayed for comparison purposes. Furthermore, the specific REFRESH effects are shown for address five, all four data bits. The effects of the REFRESH operation on the target address five are as expected. The data bits 3, 2, and 0 are refreshed to HIGH and the data bit 1 is refreshed to a LOW. Finally, the MBSY signal is demonstrated for the entire simulation interval to give a better idea of its operation.

The next three figures display the same REFRESH operation signals but at a simulation nominal temperature of 85.0C. See Figure 6.20 on page 239, Figure 6.21 on page 240, and Figure 6.22 on page 241.

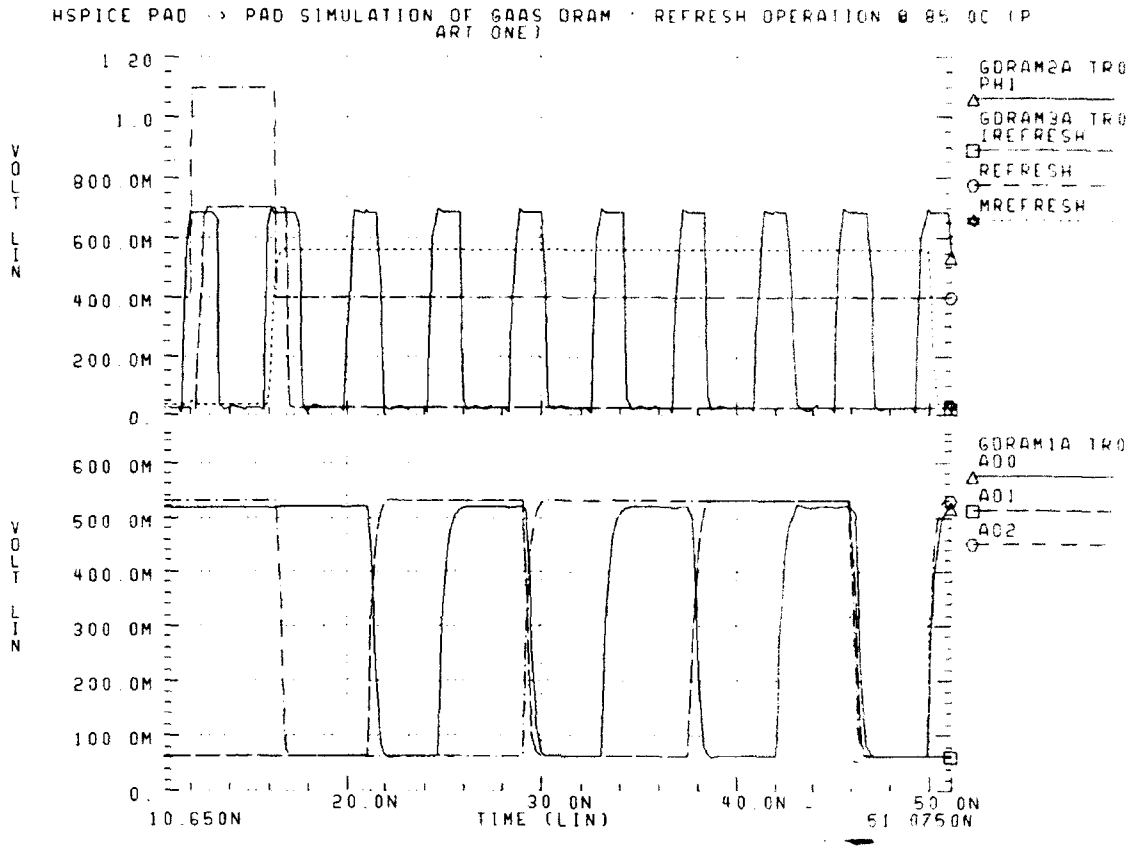


Figure 6.20 GaAs DRAM REFRESH Operation at 85.0C (Part One)

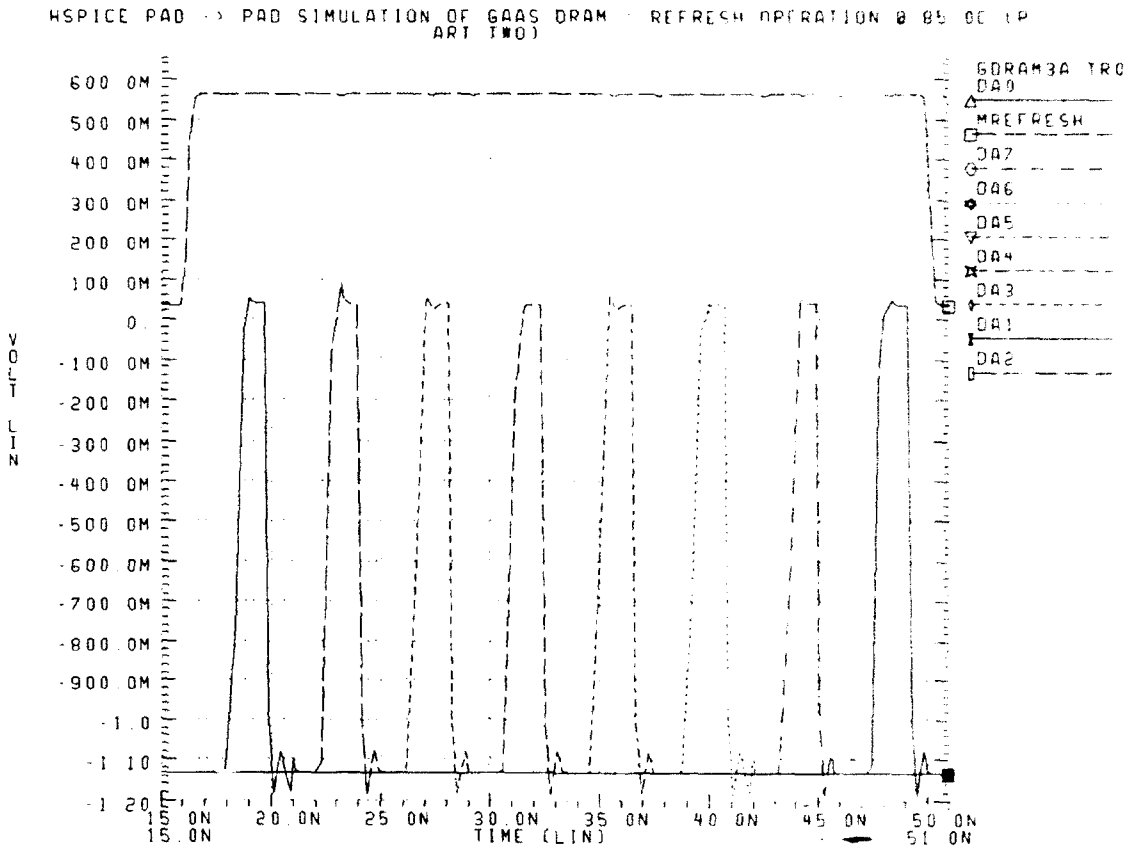


Figure 6.21 GaAs DRAM REFRESH Operation at 85.0C (Part Two)

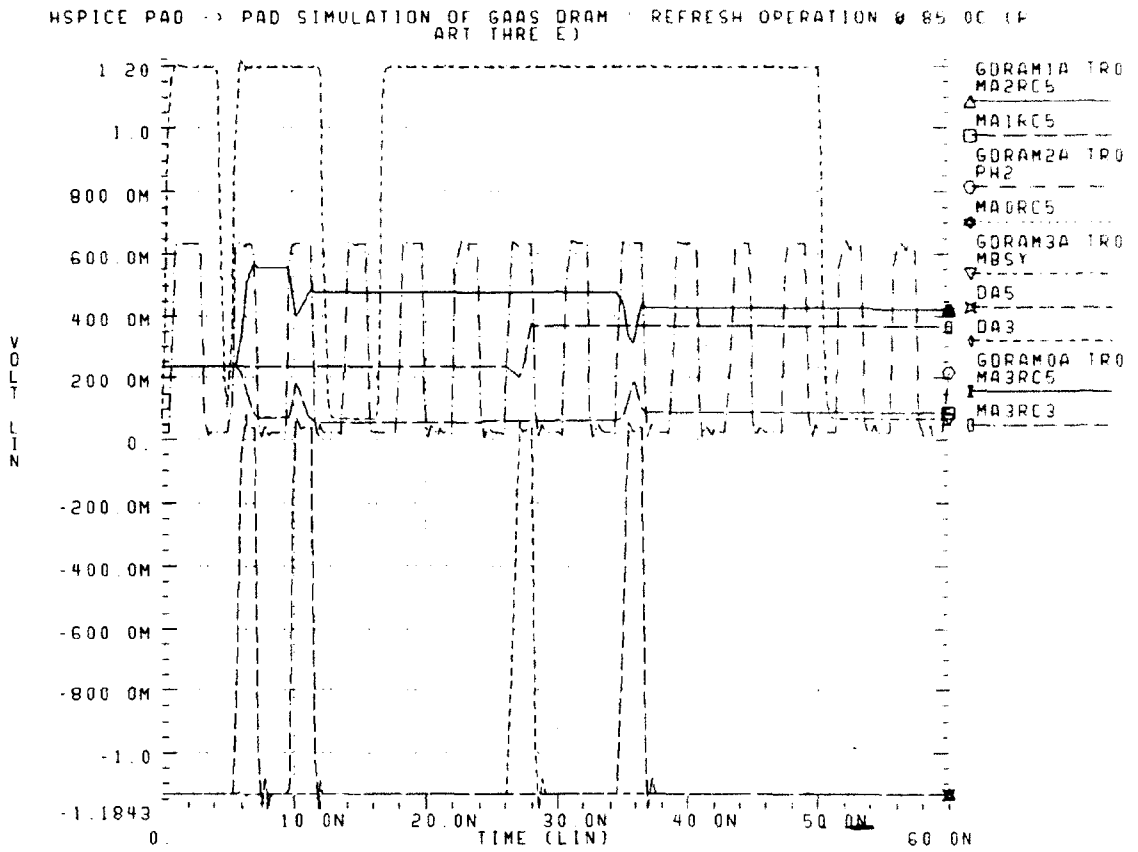


Figure 6.22 GaAs DRAM REFRESH Operation at 85.0C (Part Three)

D. GaAs DRAM POWER CONSUMPTION

The power consumption of the GaAs DRAM memory array circuit was certainly a concern. However, there were no power consumption optimization techniques employed. The absolute main thrust of the research was the design, validation, and fabrication of a functioning GaAs DRAM memory array constructed entirely using the industry standard GaAs fabrication process and materials. The next two figures provide power consumption for GaAs DRAM memory array, see Figure 6.23 on page 242 and Figure 6.24 on page 243.

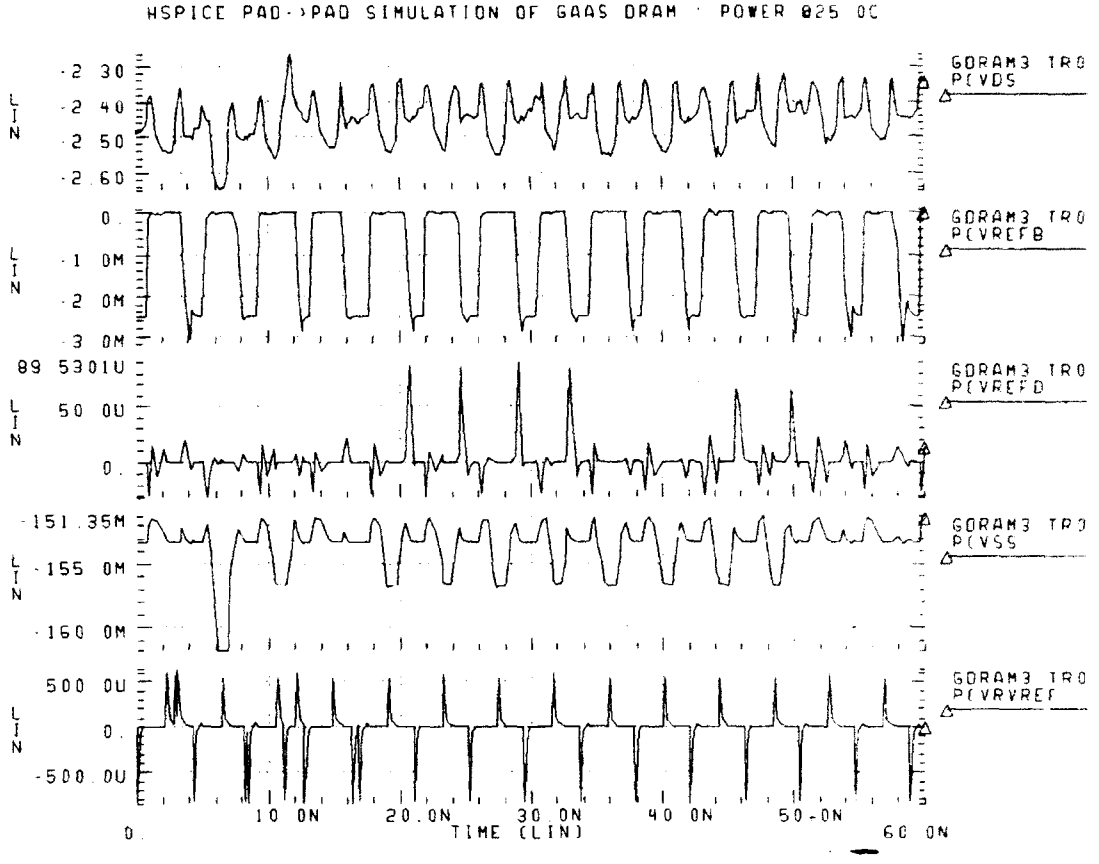


Figure 6.23 GaAs DRAM Memory Array Power Consumption @25.0C

Examining Figure 6.23, the power consumption graphs for all five of the external power supplies are provided. The uppermost graph displays the power consumption of the main power supply, V_{DS}. The HSPICE AVG function calculates the average power consumption of V_{DS} over the entire length of the simulation run (60 nanoseconds) to be 2.45 watts. The next graph of Figure 6.23 (second from top) displays the power consumption for the V_{REFB}. The HSPICE AVG function calculates the average power consumption of V_{REFB} over the entire length of the simulation run (60 nanoseconds) to be 9.15E-4 watts. The middle graph of Figure 6.23 presents the power consumption of V_{REFD}. The HSPICE AVG function calculates the average power consumption of V_{REFD} over the entire length of the simulation run (60 nanoseconds) to be 1.35E-6 watts. The fourth graph of Figure 6.23 demonstrates the power consumption of the V_{SS} power supply. The HSPICE AVG function calculates the average power consumption of V_{SS} over the entire length of the simulation run (60 nanoseconds) to be 1.54E-1 watts. The last graph of Figure 6.23 (fifth from top) displays the power

consumption of the V_{RVREF} power supply, which provides a reference voltage level to the 12 pad receiver circuits, as previously mentioned. The power consumption average values used here may be found in the HSPICE listing files. See "Run #1 LISTING FILE" on page 379.

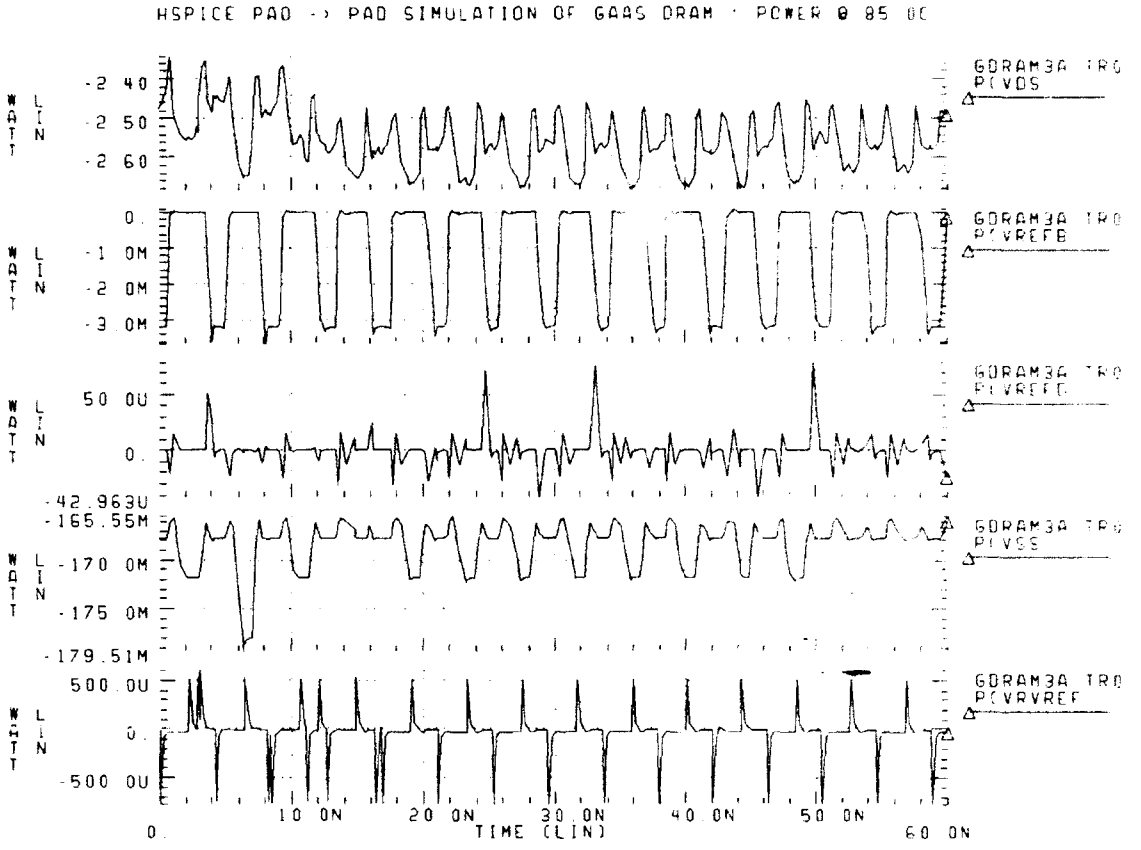


Figure 6.24 GaAs DRAM Memory Array Power Consumption @85.0C

E. SUMMARY OF GaAs DRAM MEMORY CHARACTERISTICS

The purpose of this summary is to collect some of the important characteristics of the GaAs DRAM memory design. Probably, the single most referenced DRAM characteristic is memory access time. Wakerly [REF 9:p. 642] defines the most commonly used access time to be t_{AA}, *access time from address* to be how long it takes (assuming the memory chip is already enabled) to achieve stable output data after the memory address is changed. For the GaAs DRAM, because the simulation used pre-set voltage levels for the input address lines, this report will define the memory access time to be from the time the external READ signal is asserted to the time that the output data is stable as reported by the assertion of the DRDY signal.

1. GaAs DRAM Minimum READ Operation

The following three figures will present a minimum access time READ operation at a simulation nominal temperature of 25.0 C. Address six was used as the target address for the minimum READ operation simulation. Additionally, the data contents of target address six were set to D3 = 0, D2 = 1, D1 = 0, and D0 = 1, using the HSPICE ".IC" option. The actual voltage values used were derived from the results of the previously discussed HSPICE pad-to-pad WRITE operation, a "1" = 0.437 volts and a "0" = 0.0728 volts. Examining Figure 6.25 on page 244, one may see the assertion of the external READ signal, the assertion of the MREAD signal, and the two fundamental clock pulses, PH1 and PH2.

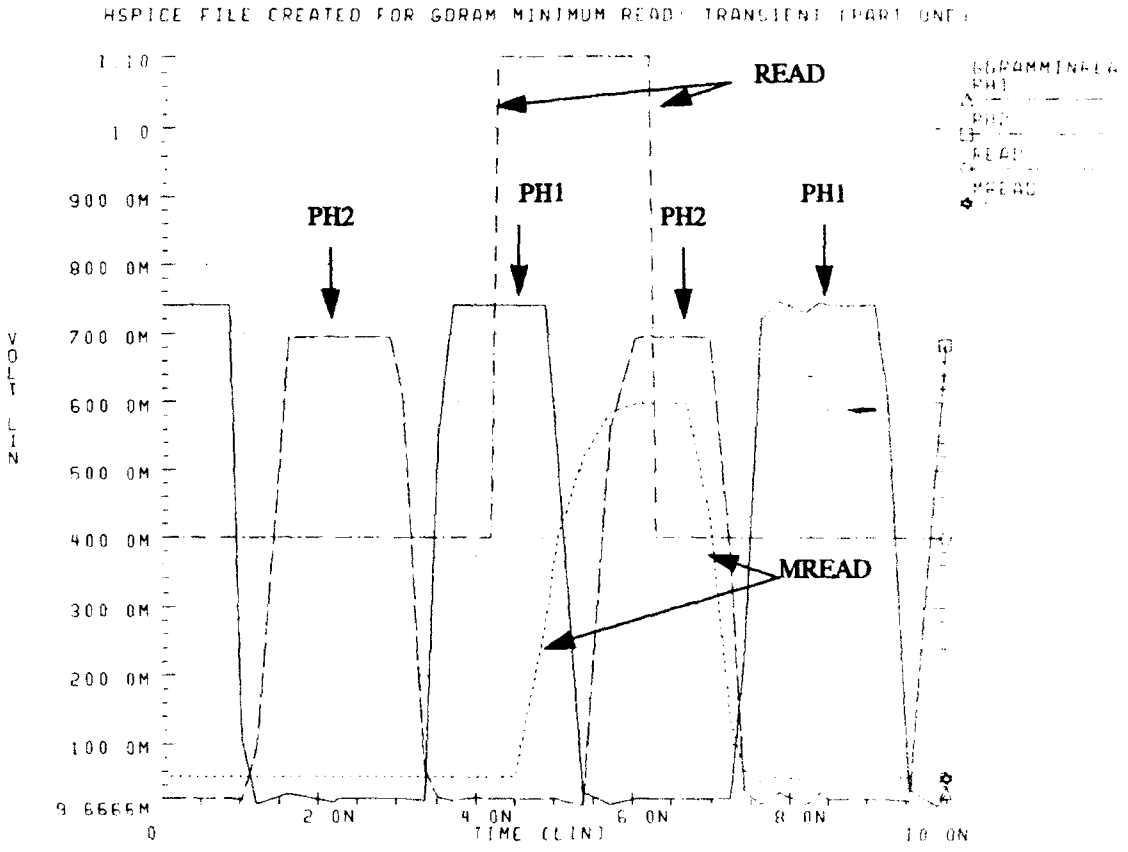


Figure 6.25 GaAs DRAM Minimum READ Operation: Transient Analysis (Part One)

Referring to Figure 6.25, as previously mentioned, it is not necessary to include the PH1 clock pulse in the minimum READ operation. This is because the PH1 clock pulse is only used internally in the RAM_ARRAY during a READ. The next figure of the minimum READ operation, Figure 6.26 on page 245,

presents the target address (address six) data outputs (DO3 - DO0), the charge contents of the target address (MA3RC6 - MA0RC6), and the two main clock pulses, PH1 and PH2.

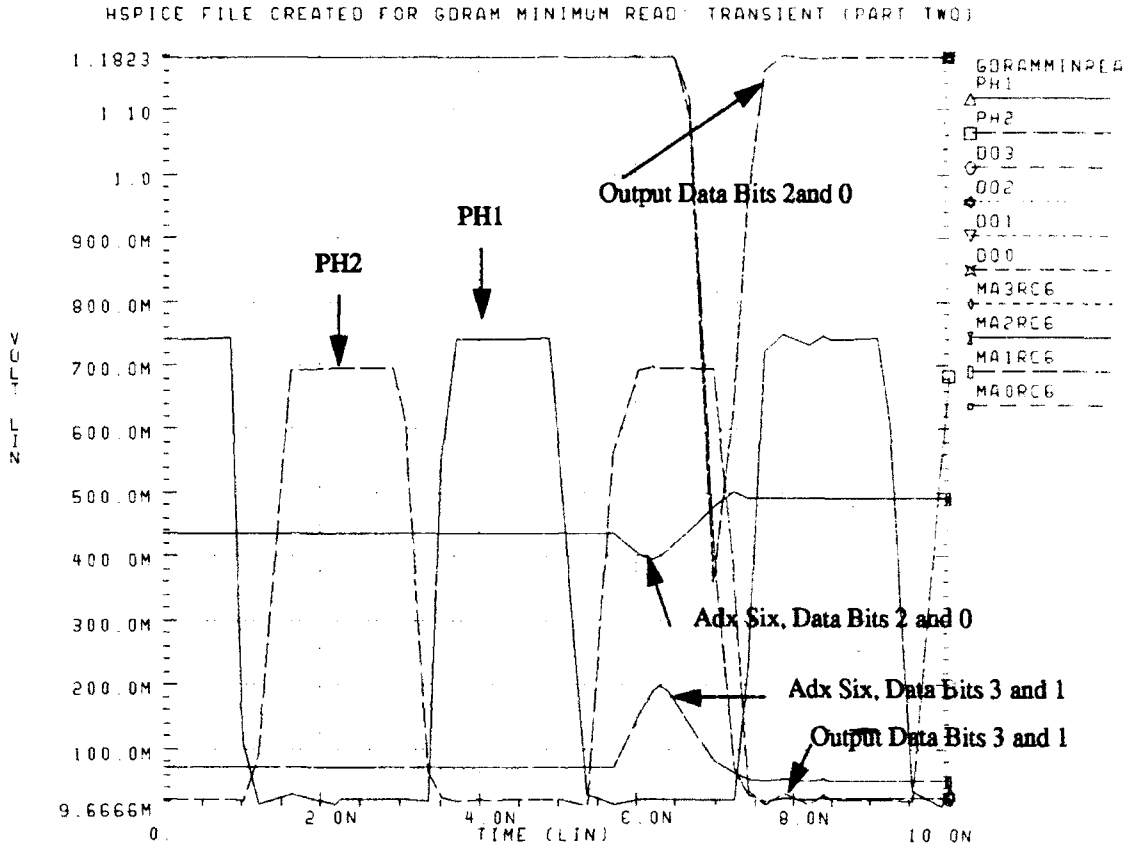


Figure 6.26 GaAs DRAM Minimum READ Operation: Transient Analysis (Part Two)

The final figure of the GaAs DRAM minimum READ operation, Figure 6.27 on page 246, demonstrates the assertion of the READ signal, the assertion of the MREAD signal, and the associated activity of the memory status control signals, MBSY and DRDY.

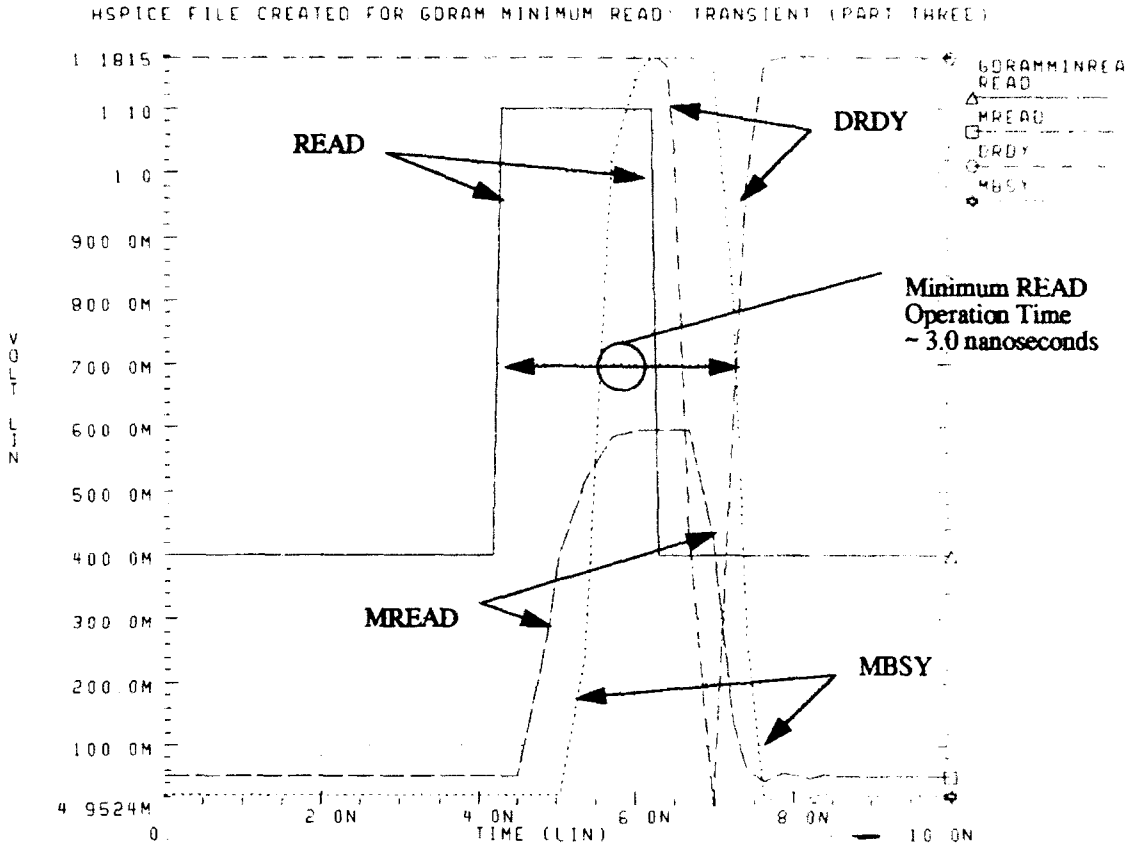


Figure 6.27 GaAs DRAM Minimum READ Operation: Transient Analysis (Part Three)

In Figure 6.27, one may see the defining interval for a GaAs DRAM minimum READ operation. This interval, as previously defined, is approximately 3.0 nanoseconds. The HSPICE AVG function calculated an average power, ($p(V_{DS})$), of 0.392 milliwatts over the minimum READ operation target interval.

2. GaAs DRAM Minimum WRITE Operation

The following three figures will present a minimum access time WRITE operation at a simulation nominal temperature of 25.0 C. Address seven was used as the target address for the minimum WRITE operation simulation. Additionally, the input data bits were set to D3 = 0, D2 = 1, D1 = 0, and D0 = 1. Examining Figure 6.28 on page 247, one may see the assertion of the external WRITE signal, the assertion of the MWRITE signal, and the two fundamental clock pulses, PH1 and PH2.

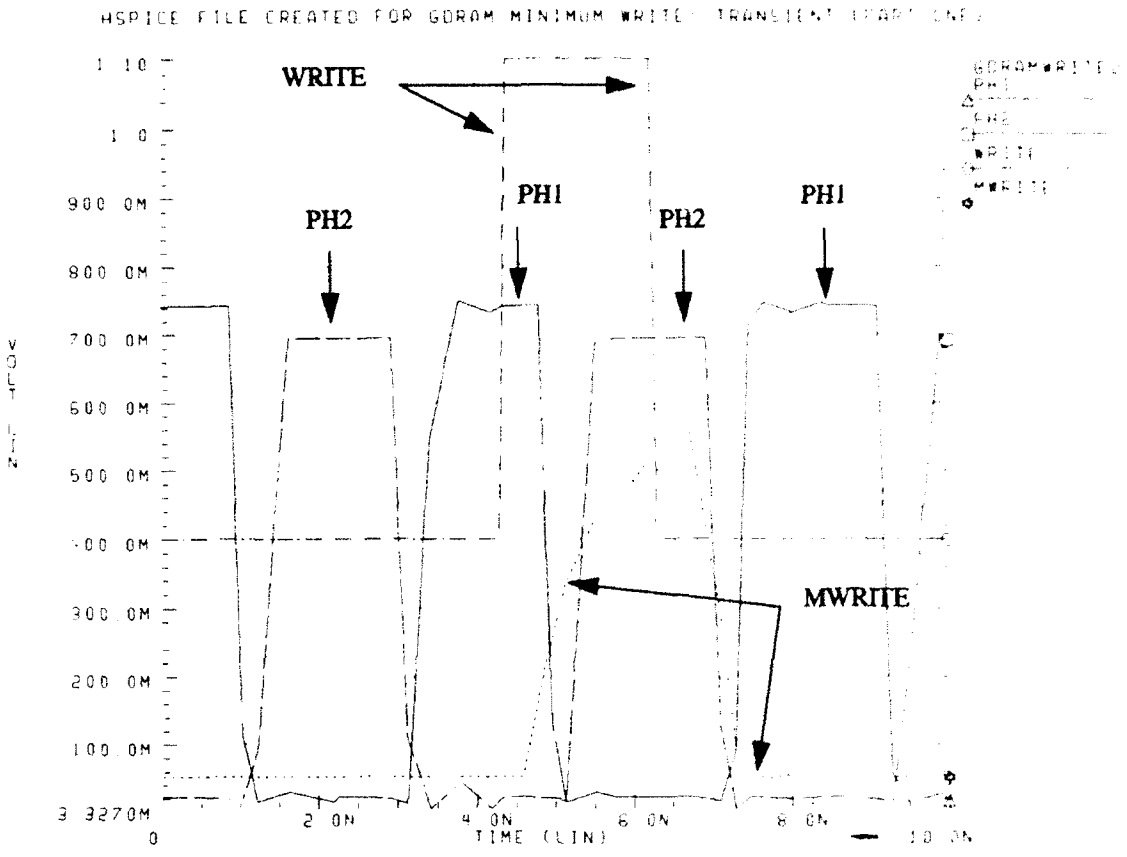


Figure 6.28 GaAs DRAM Minimum WRITE Operation: Transient Analysis (Part One)

For the reasons previously mentioned, the PH1 clock pulse is also not required for a GaAs DRAM minimum WRITE operation. Thus notice in Figure 6.28, the external WRITE is asserted such that the MWRITE signal becomes HIGH immediately prior to the rising edge of PH2. The next figure, Figure 6.29 on page 248, shows the writing of target address seven (MA3RC7 - MA0RC7) and the two fundamental clock pulses, PH1 and PH2.

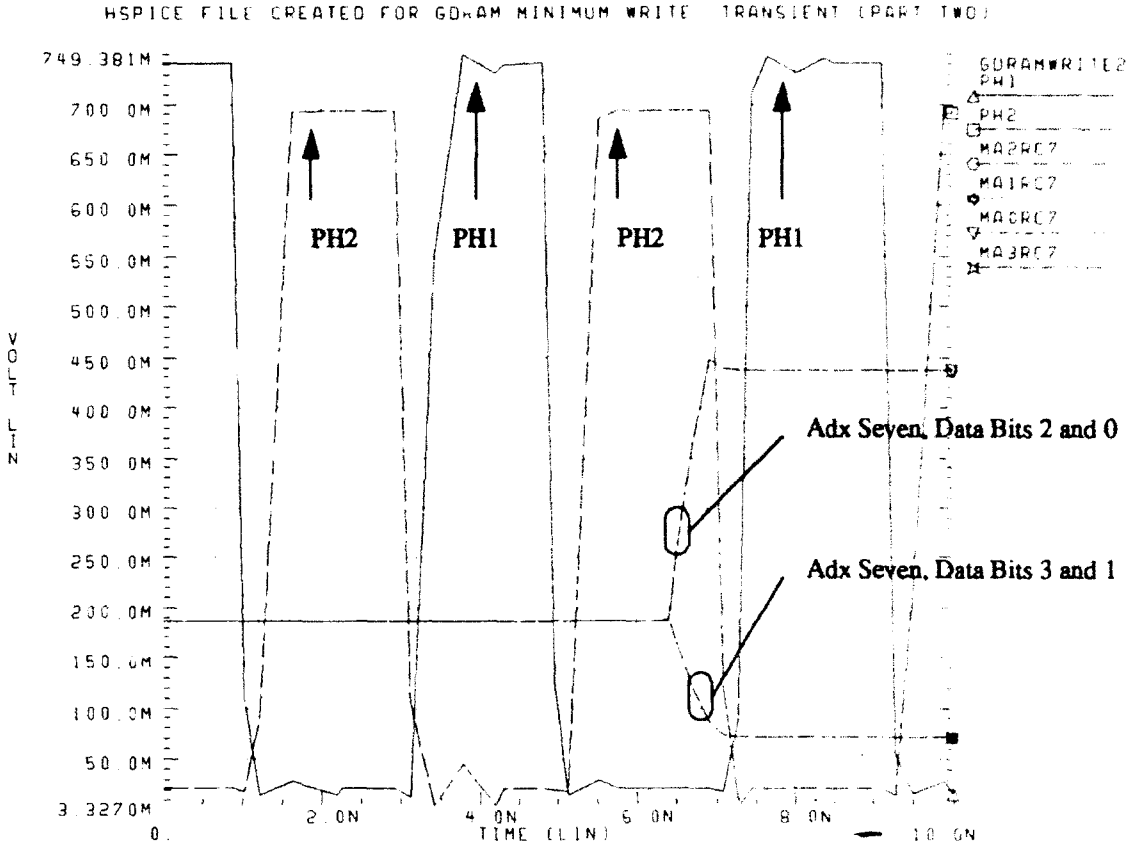


Figure 6.29 GaAs DRAM Minimum WRITE Operation: Transient Analysis (Part Two)

The final figure of the GaAs DRAM minimum WRITE operation, Figure 6.30 on page 249, demonstrates the assertion of the WRITE signal, the assertion of the MWRITE signal, and the associated activity of the memory status control signal, MBSY.

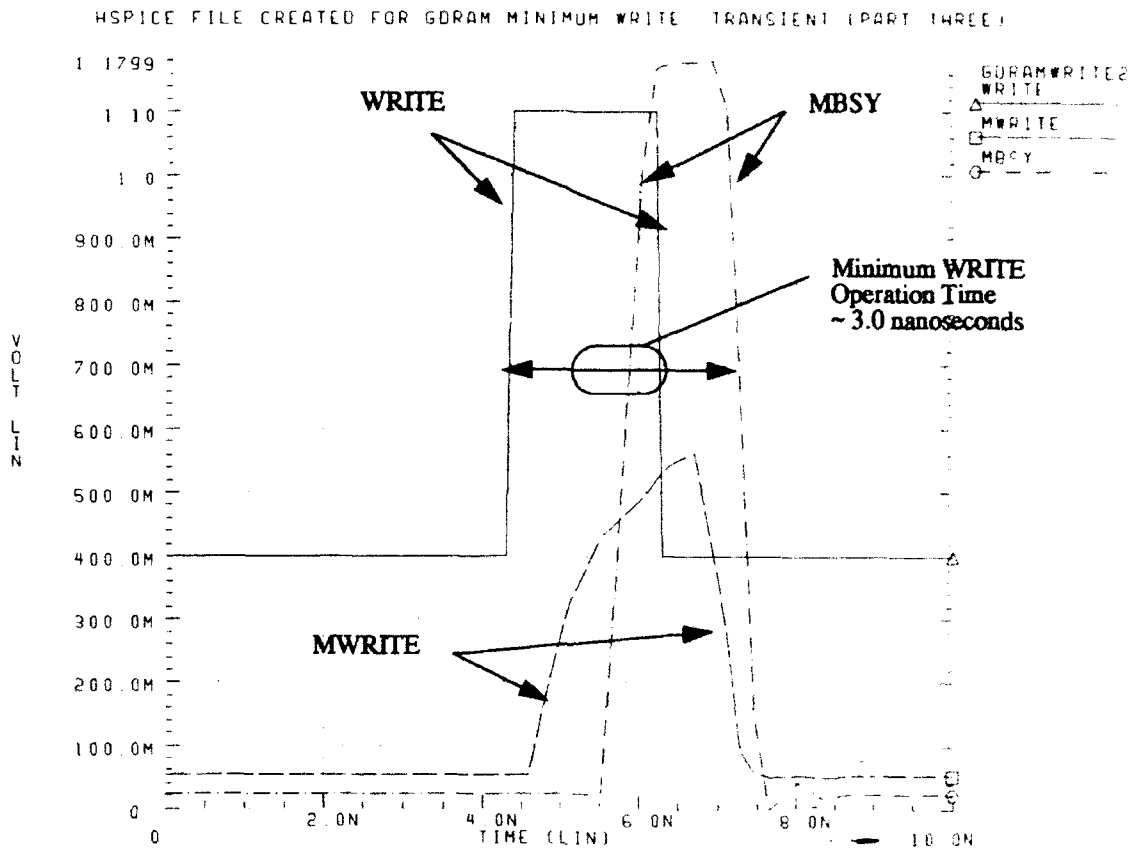


Figure 6.30 GaAs DRAM Minimum WRITE Operation: Transient Analysis (Part Three)

In Figure 6.30, one may see the defining interval for a GaAs DRAM minimum WRITE operation. This interval, defined to begin when the external control signal WRITE is asserted and to end when the external memory status control signal MBSY is de-asserted, is approximately 3.0 nanoseconds. The HSPICE AVG function calculated an average power, ($p(V_{DS})$), of 2.45 watts over the minimum WRITE operation target interval. For a through discussion of the RAM_ARRAY WRITE operation specifics, see the work of Vagts [Ref. 8:pp. 17-23].

3. GaAs DRAM Minimum REFRESH Operation

The following three figures will present a minimum time REFRESH operation at a simulation nominal temperature of 25.0 C. The data contents of address six were set to D3 = 0, D2 = 1, D1 = 0, and D0 = 1, using the HSPICE ".IC" option. The actual voltage values used were derived from the results of the previously discussed HSPICE pad-to-pad WRITE operation, a "1" = 0.437 volts and a "0" = 0.0728 volts.

Examining Figure 6.31 on page 250, one may see the assertion of the external REFRESH signal, the assertion of the MREFRESH signal, and the two fundamental clock pulses, PH1 and PH2.

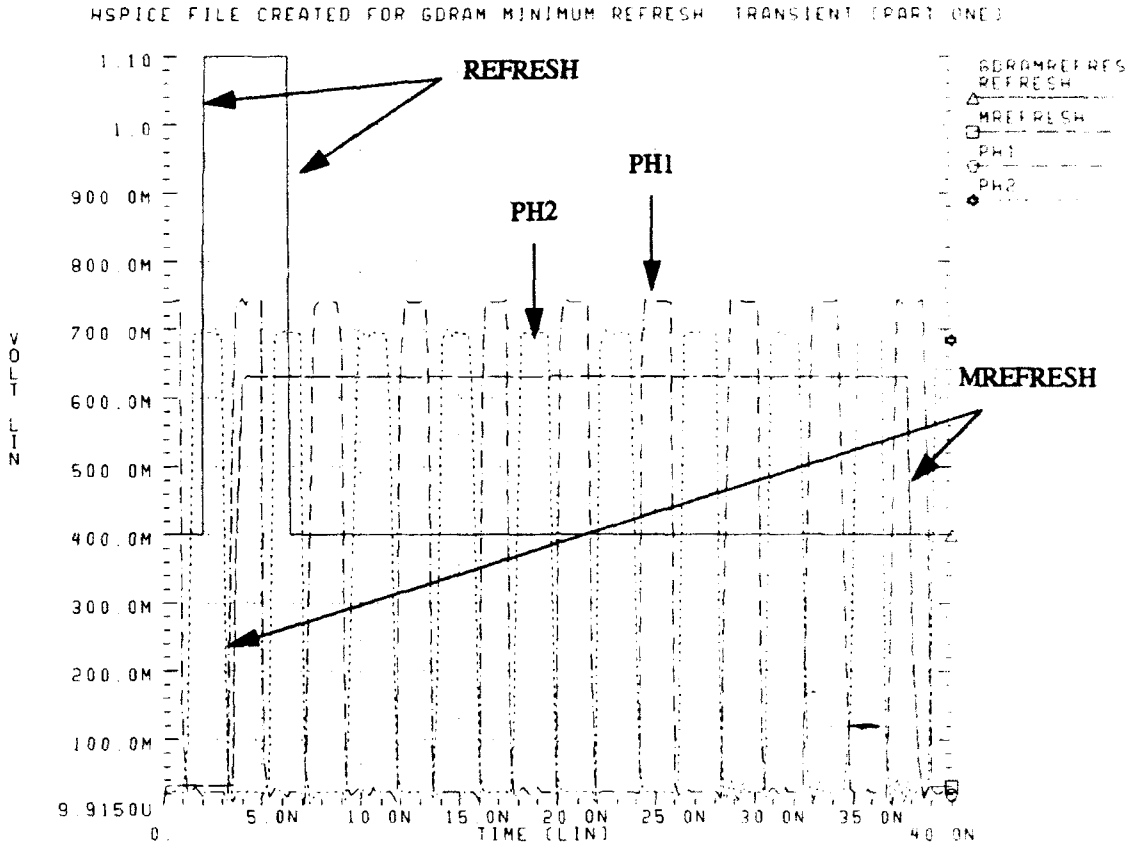


Figure 6.31 GaAs DRAM Minimum REFRESH Operation: Transient Analysis (Part One)

The next figure, Figure 6.32 on page 251, shows the REFRESH effects on the target address (six), the DRAM address driver signal DA6, and the two fundamental clock pulses, PH1 and PH2.

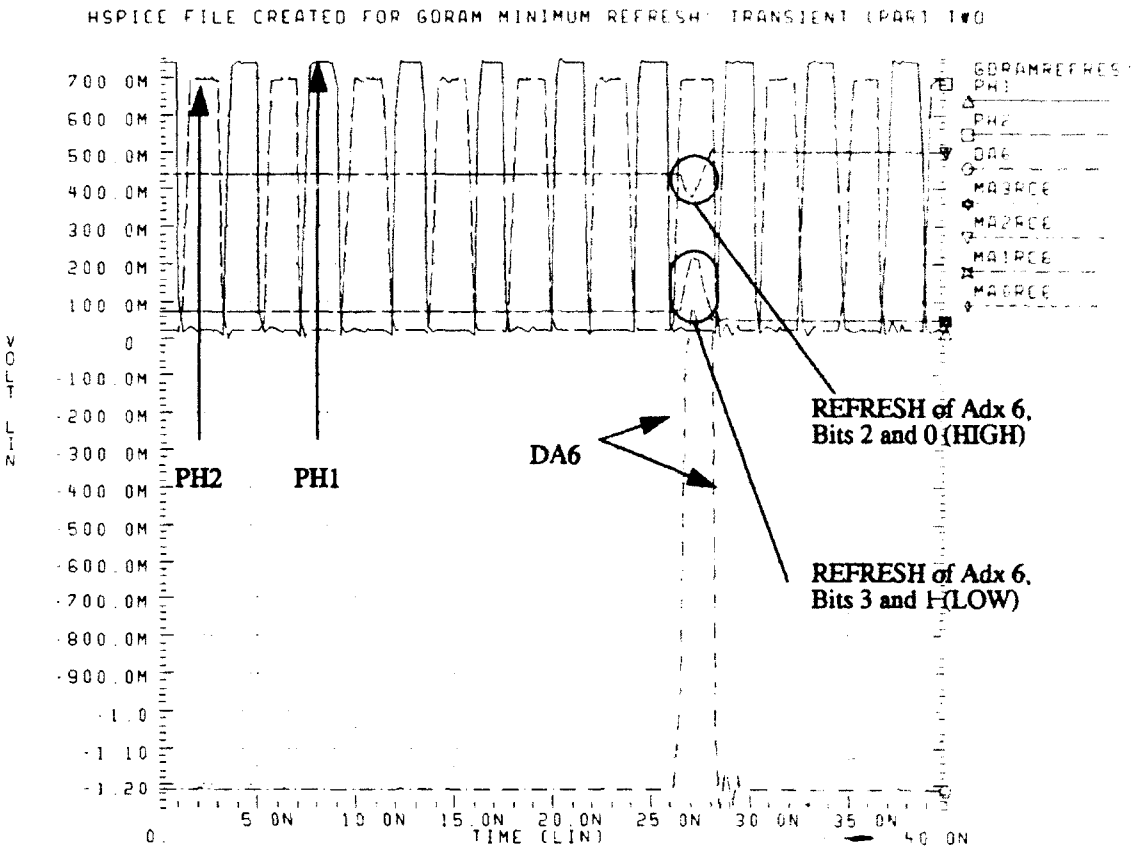


Figure 6.32 GaAs DRAM Minimum REFRESH Operation: Transient Analysis (Part Two)

The final figure of the GaAs DRAM minimum REFRESH operation, Figure 6.33 on page 252, demonstrates the assertion of the REFRESH signal, the assertion of the MREFRESH signal, and the associated activity of the memory status control signal, MBSY.

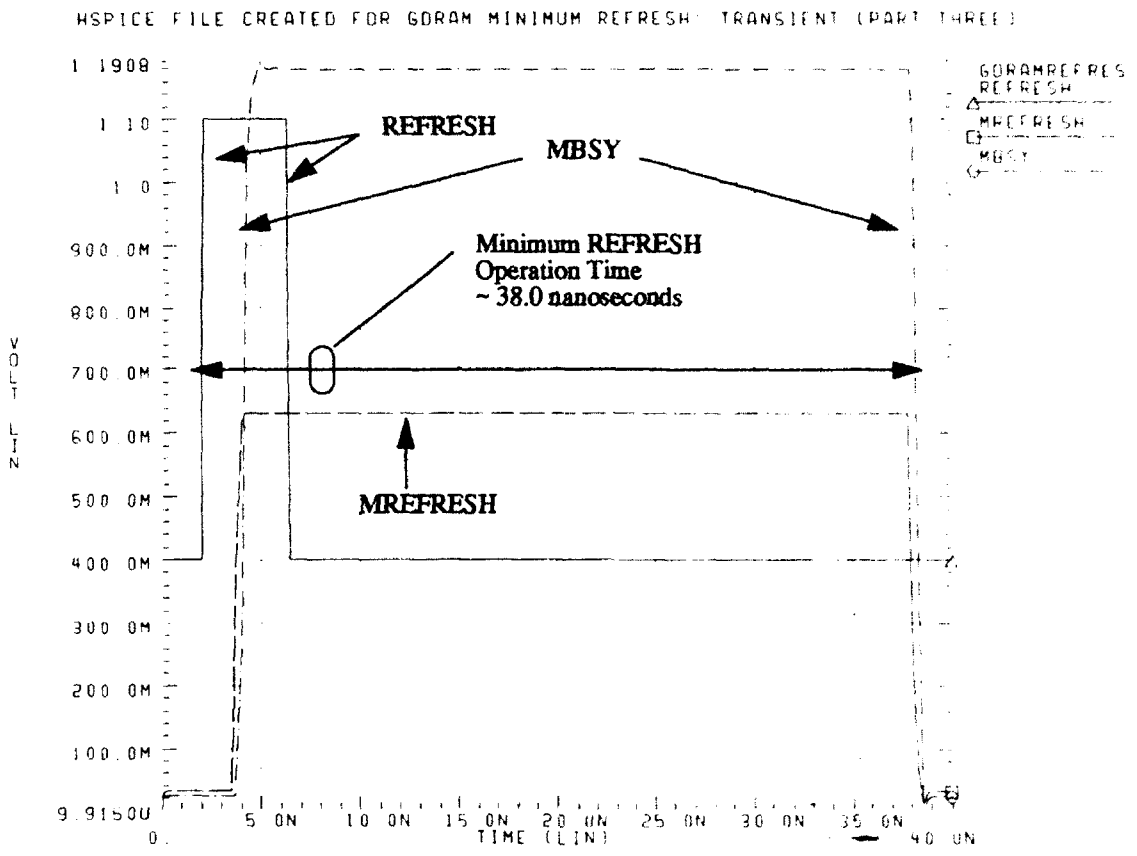


Figure 6.33 GaAs DRAM Minimum REFRESH Operation: Transient Analysis (Part Three)

In Figure 6.33, one may see the defining interval for a GaAs DRAM minimum REFRESH operation. This interval, defined to begin when the external control signal REFRESH is asserted and to end when the external memory status control signal MBSY is de-asserted, is approximately 38.0 nanoseconds. The HSPICE AVG function calculated an average power, ($p(V_{DS})$), of 2.45 watts over the minimum REFRESH operation target interval.

The final chapter of this report will present some observations on the design cycle followed by project conclusions.

VII. CONCLUSIONS

This final chapter will offer some observations on the design cycle followed by project conclusions.

A. THE DESIGN CYCLE

The design cycle for this project was rather long and full of twists and turns. The purpose of this chapter is to provide general information about the design paths chosen, traveled, discarded and re-traveled. Some mention of the Computer Aided Design (CAD) tools will be made and pitfalls will be disclosed.

1. Gallium Arsenide Circuit Design

Prior to commencing the research for the GaAs DRAM, a course in CMOS integrated circuit design and layout was completed. This course provided a useful background but in no way completely disclosed the necessary experience and procedures. Designing integrated circuits in CMOS is relatively "old news" these days, the leading edge of the CMOS technology is concentrated on greater and greater densities, such as the 64 megabit DRAM. Nevertheless, useful lessons may be learned and experience is gained.

The practical side of the design cycle included drawing out possible circuits and then testing these using the available simulator. After the circuits which operated correctly were integrated into the overall design, actual schematics were created for these circuits to facilitate both then present use and future reporting uses. A judicious choice of schematic editors, with an eye towards one day incorporating these same drawings directly into the future report was in order. However, the choices for the schematic editor were limited to the only one that was available. Much time along the path to the final design was invested in creating and updating schematic drawings and block diagrams. Unfortunately, as is sometimes the case, the only schematic editor which was available at the time did not have the facility to create postscript files that could then be later incorporated into the report. This lack of postscript capability was not noticed until much later and all the schematic drawings and block diagram drawings previously created and updated had to be redrawn.

The actual design of the GaAs DRAM occurred slowly because of the learning curve associated with designing in gallium arsenide. Whereas the design of CMOS logic elements is discussed in excruciating detail in any number of text books, the basic material necessary to design gallium arsenide logic elements is in short supply and what is available is frequently too advanced to be easily understood by students of GaAs. The main reference used to facilitate the GaAs DRAM design is the very comprehensive text written by

Messrs. Butner and Long of University of California, Santa Barbara campus [Ref. 10.]. Easily the best GaAs text found and used nearly exclusively as it covers, but is not limited to, such topics as device physics, use of circuit simulators, and layout procedures.

2. Gallium Arsenide Circuit Simulation and Testing

The first step in this design cycle was designing basic GaAs logic elements and then testing these using whichever circuit simulator one could find that incorporated GaAs device libraries. Some mention of these device libraries is in order. Designing in gallium arsenide requires a circuit simulator such as SPICE to test the target circuits. Initially SPICE version 3G (SPICE3G) was used as it was the only simulator available. The libraries for GaAs MESFETs in SPICE3G are adequate but suffer from having no GaAs second order effects modeled. The most important GaAs second order effects concerning the GaAs DRAM are subthreshold current and substrate leakage current. The reason that these two gallium arsenide second order effects are so important is that both have direct effects on using GaAs MESFETs for charge storage. See [Ref. 10:pp. 114 - 120] for a thorough discussion of both of these second order effects. Lacking the second order effects, SPICE3G yielded very optimistic results with regard to the amount of time that a charge was maintained on a capacitor.

The final goal of the GaAs DRAM design cycle was fabrication and to this end, it was determined that MOSIS would provide funding to fabricate through Vitesse. It was further discovered that Vitesse has configured or customized SPICE version 3G to incorporate more accurate GaAs models, this version of SPICE will be referred to as Vitesse SPICE (VSPICE). The design cycle graduated to using VSPICE hoping to achieve more realistic results using the improved VSPICE GaAs libraries. Results achieved through VSPICE still indicated very optimistic charge storage time. This is because VSPICE, like SPICE3G, does not model the GaAs second order effects of subthreshold current and substrate leakage current.

It was at this time in the GaAs DRAM design cycle that the modeling and selection of the charge storage element occurred. The candidates for the charge storage element were a parallel plate capacitor, the gate of a E/D MESFET, or an E/D MESFET back-connected as a diode. The eventual choice was the parallel plate capacitor based upon test results. For a thorough discussion of various results obtained for each of the aforementioned charge storage elements, see [Ref. 8:pp. 3 - 8]. The selection of the charge storage element for the GaAs DRAM was based upon test results obtained using circuit simulators that did not model the second order effects. Were HSPICE (from Meta Software) available at the Naval Postgraduate School at the time of the charge storage element selection, a different choice may have occurred. This is reported in [Ref.

8:pp. 3 - 8]. HSPICE is the next generation circuit simulator, it has extensive libraries including the most important GaAs second order effects, it has improved convergence algorithms and memory management, and finally, a vastly improved user interface.

All the work that occurred prior to the arrival of HSPICE was re-tested using HSPICE (with its associated Vitesse HGaAs3 models) and while this was fairly time consuming, it was believed that the results obtained would now be the closest possible to reality. VSPICE and SPICE3G were not used again. The charge storage results obtained from HSPICE were encouraging but vastly different from those obtained using SPICE3G and VSPICE. The point of the discussion is the incorrect tool will yield incorrect results every time.

3. Gallium Arsenide Layout and Testing

The next step in the design cycle was the tentative layout of these GaAs logic circuits. The only layout tool available was MAGIC using "edgaas" (1.2 micron) technology file. Layout is another example of the "you must know who before you do" syndrome. Prior to layout, it is necessary to know almost certainly which company will be fabricating the design as each fabrication facility operates with different sets of parameters. As the technology for GaAs fabrication improves, the parameters vary (e.g. generally the gate lengths of the MESFETs become shorter) and this information must be considered when actually laying out the chip. Vitesse had been selected as the fabrication facility so it was necessary to obtain the MAGIC technology file from Vitesse through MOSIS. The technology file contains fabrication process information such as minimum gate lengths, material routing and spacing, and material specifications.

After each GaAs logic circuit was laid out used MAGIC, it was extracted and tested using HSPICE with its associated Vitesse HGaAs3 models. It was during this time that attention should have been paid to power consumption and operating temperature, but alas, it was not. Nearly at the end of the layout procedure, it occurred that power consumption at the expected operating temperature needed to be considered for both the length and width of the power and ground busses. As expected, the power consumption of the circuits used required greater widths and lengths then the minimums which were routinely used in order to facilitate a dense layout. As previously mentioned, GaAs logic circuits are not physically symmetric (as CMOS circuits are generally) when laid out and this caused some difficulty during the process and optimization for density. Virtually the entire layout was re-worked to make room for the required sizes of the power and ground busses.

4. Gallium Arsenide Fabrication and Testing

The fabrication procedure as available to educational institutions such as the Naval Postgraduate School through MOSIS results in a sum of money being allocated by MOSIS to cover the entire costs of the

fabrication. Many factors are considered when planning the actual fabrication including type of package, number of pins, and size of actual chip real estate. Once the layout was complete, having adjusted it for the required power and ground busses, it was determined that the GaAs DRAM array of eight eight-bit words was too large for the amount of money allocated by MOSIS for fabrication by Vltesse. This required a further "down-sizing" of the GaAs DRAM array to eight four-bit words in order to make it fit on the chip real estate that could be purchased. Once the interior body of the chip was completely laid out, it was then necessary to place the emitter-coupled logic (ECL) input/output driver circuits on the signal pins and also apply the procedures for "bonding" the pads with metal four in accordance with the Vitesse fabrication process parameters.

The testing of the entire GaAs DRAM chip (pad to pad) was accomplished using HSPICE. It should be mentioned that although HSPICE was run on a SUN SPARCstation 2 with 32 megabytes of read/write memory, the simulation of the entire chip required many days to run and several hundred megabytes of disk storage. HSPICE has incorporated several improvements over SPICE3G and VSPICE to facilitate smaller output files by judiciously choosing a select number of nodes about which to record data but even using these techniques the simulation still required days to finish.

Once the final GaAs DRAM array size was determined and the chip was tested, a "cif" file was generated and sent over INTERNET to MOSIS which in turn sent it to Vitesse. The construction of a test platform and the testing of the fabricated GaAs DRAM array will be the subject of a follow-on thesis.

B. CONCLUSIONS

The design goals for the gallium arsenide DRAM were met. These goals included very short memory access times, the use of GaAs standard materials, standard GaAs fabrication techniques, simple control circuitry, and acceptable power consumption.

1. Access Times

The GaAs DRAM access times are remarkably short, even when compared to commercial SRAM. In the 1991 Vitesse Semiconductor Corporation GaAs device catalog, a typical GaAs 256X4 static RAM, constructed from E/D MESFET technology, has an access time of four nanoseconds while consuming 1.75 watts. The GaAs DRAM offers a minimum READ/WRITE access time of approximately 3.0 nanoseconds while consuming ~ 2.45 watts. Of course, the initial bit density of the GaAs DRAM is very low and the initial power consumption per bit is much higher. Also, the REFRESH operation requires approximately 38.0 nanoseconds and this is a very long time compared to the access time for a READ or WRITE. Additionally,

the required periodic interval for REFRESH is reported by Vagts [Ref. 8:p. 21] to be approximately three milliseconds. In a commercial DRAM, the refresh operation is typically accomplished approximately every four milliseconds using rows within two-dimensio' al arrays [Ref 9:p. 648]. This greatly reduces the amount of time required for commercial DRAM to refresh the contents of all its memory addresses. Were the commercial DRAM design and layout techniques applied to the GaAs DRAM, there is no reason why the results achieved would not be similar.

2. Power Consumption

The power values reported for the READ, WRITE, and REFRESH operations include power consumption of the entire chip for the target operation. The specific power consumption values for each of the major circuits are discussed in the previous chapter. The two largest consumers of V_{DS} power are the CLOCK and DREFRESH, as one might expect. Both of these circuits would be improved were power optimization techniques applied. Also, given that the topic design chip is only eight four-bit words, one could argue that the economies of scale would greatly diminish the power consumption per bit. Additionally, the support circuitry was designed with the intent to use eight data bits, however, as previously discussed, the data bit density was halved after control design was complete. Therefore, the physical size of the transistors could, in many cases, be reduced which would reduce the overall power consumption.

3. Control Circuitry

The simplicity utilized in the control design was intentional. Improvements may certainly be made to the control design and some could be considered mandatory. One such improvement would be a better design to handle the possible non-simultaneous assertion of two operation signals, such as READ then WRITE. Also, the incorporation of input data latches would simplify the design of the control circuitry.

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APPENDIX A - HSPICE FILES

The HSPICE files are provided for a representative sample of the GaAs DRAM logic circuits. Abbreviated in the interest of brevity (as providing all listing files will result in an appendix length over 600 pages), this collection of listing files provides both the structure of the "*.sp" file and the information not specifically contained in any graph but listed separately in TABLE 4.1, "GaAs DRAM LOW-LEVEL CIRCUIT OPERATING CHARACTERISTICS," on page 158. The listing files result from simulating the GaAs DRAM circuits with HSPICE.

A. Listing File for DINV Transient Analysis at 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        19:27:27  23-jan93   sun
** hspice file created for circuit 'dinv'
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
**********************************************************
**********************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1     2     3     4
*  d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
**********************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1      2     3      4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends   d2load
**********************************************************
* ******* hspice version *********
```

```
* include vitesse hgaas3 models and parameters for hspice.
*********************************************************
* power supplies
vds 1   0 dc  2.0v  $ element under test power supply
vload 888 0 dc 2.0v  $ test load power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next line is used to provide the test signal input for transient analysis
va0 101 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)

* main circuit
x0 101 102  888  0 dinv
x1 102 103  888  0 dinv
x2 103 106  888  0 dinv
x3 106 104  1    0 dinv     $ element under test
x4 104 107  888  0 d2load    $ test load

* measurement parameters

* next three lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe input=v(106) output=v(104)
.probe tran p(vds) p(va0) p(vload) power

* next 8 lines will calculate vmax vmin trise tfall and tdelay :transient analy
s
.meas tran vmax max v(104) from=2ns to=20ns
.meas tran vmin min v(104) from=2ns to=20ns
.meas tran tphl trig v(106) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(104) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(106) val='(vmax-vmin)*.5' td=2ns
+ fall=1 targ v(104) val='(vmax-vmin)*.5' td=2ns rise=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
.meas tran tfall trig v(104) val='0.9*vmax' td=2ns
+ fall=2 targ v(104) val='vmin+0.1*vmax' fall=2
.meas tran tdelay trig v(106) val=.2835 td=2ns fall=1
+       targ v(104) val=.2835 rise=1
.tran 50ps 20ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit 'dinv'
```

```
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                    dinv       1.00
   2 x1.                    dinv       1.00
   3 x2.                    dinv       1.00
   4 x3.                    dinv       1.00
   5 x4.                    d2load     1.00
   6 x4.x0.                  dinv      1.00
   7 x4.x1.                  dinv      1.00
 Opening plot unit= 15
file=dinv.pa0

** hspice file created for circuit 'dinv'
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is     0.
  node   =voltage     node   =voltage     node   =voltage


+0:1     =  2.0000  0:101    =  63.0000m 0:102    = 658.6414m
+0:103   =  52.0534m 0:104    =  52.0545m 0:106    = 658.6893m
+0:107   =  1.9872  0:888    =  2.0000  5:5      =  1.9872



 Opening plot unit= 16
file=dinv.tr0

** hspice file created for circuit 'dinv'
****** transient analysis            tnom= 25.000 temp= 25.000
******
 vmax         = 6.4062E-01   at= 4.8836E-09
        from= 2.0000E-09   to= 2.0000E-08
 vmin         = 5.0543E-02   at= 1.7275E-08
        from= 2.0000E-09   to= 2.0000E-08
 tphl         = 1.0795E-10 targ= 8.5989E-09  trig= 8.4910E-09
 tplh         = 7.0997E-11 targ= 4.4733E-09  trig= 4.4023E-09
 trise        = 3.5183E-10 targ= 4.7526E-09  trig= 4.4007E-09
 tfall        = 1.3037E-10 targ= 1.7061E-08  trig= 1.6931E-08
 tdelay       = 6.2566E-11 targ= 4.4672E-09  trig= 4.4046E-09

      ***** job concluded
      total cpu time       14.08 seconds
         job started at  19:27:27  23-jan93
         job ended   at  19:27:57  23-jan93


I am done with dinv.sp
```

Sat Jan 23 19:27:59 PST 1993

B. Listing File for D4NOR Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to  250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d         6:49: 1  25-jan93   sun
** hspice file created for circuit d4nor: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
**********************************************************
**********************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
*  d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
**********************************************************
**********************************************************
* hspice dcfl 4-input nor subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt d4nor    1  2   3   4    5     6    7
*  d g s b
j0 6 5 5 7 jfet16 l=1.2 w=6.0
j1 5 1 7 7 jfet04 l=1.2 w=96.0
j2 5 2 7 7 jfet04 l=1.2 w=96.0
j3 5 3 7 7 jfet04 l=1.2 w=96.0
j4 5 4 7 7 jfet04 l=1.2 w=96.0
.ends  d4nor
**********************************************************
**********************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2    3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
**********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
**********************************************************
```

```
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next three lines used to provide test signal inputs for transient analysis
va 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vb 101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
vc 102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)
vd 103 0 pulse(0.063 0.63 33600ps 100ps 100ps 33400ps 67200ps)


* main circuit
*  ina inb inc ind out pwr gnd subname
x3 100 101 102 103 104  1   0  d4nor    $ element under test
x4 104           107 888  0  d2load    $ test load

* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe ina=v(100) inb=v(101) inc=v(102) ind=v(103) output=v(104)
.probe tran p(vds) p(vload) power

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(104) from=2ns to=80ns
.meas tran vmin min v(104) from=2ns to=80ns
* next line is adjustment necessary to facilitate measuring tfall. if
* vmin is used in tfall calc, then the tfall calculation fails as the is a larg
e
* negative voltage spike when the four input mesfets switch from
* all on to all off and this skews the targ parameter. notice that
* vmin2 is used only in the tfall calculation line.
.meas tran vmin2 find v(104) at=64ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(104) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(103) val='(vmax-vmin)*.5' td=2ns
+ fall=1 targ v(104) val='(vmax-vmin)*.5' td=62ns rise=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=62ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
.meas tran tfall trig v(104) val='0.9*vmax' td=65ns
+ fall=1 targ v(104) val='vmin2+0.1*vmax' fall=1
```

```
.meas tran tdelay trig v(103) val=.2835 td=62ns fall=1
+      targ v(104) val=.2835 rise=1
.tran 150ps 80ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit d4nor: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x3.                    d4nor       1.00
   2 x4.                    d2load      1.00
   3 x4.x0.                  dinv       1.00
   4 x4.x1.                  dinv       1.00
 Opening plot unit= 15
file=d4nor1.pa0

** hspice file created for circuit d4nor: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
  node   =voltage     node   =voltage     node   =voltage


+0:1     =  2.0000  0:100    =  63.0000m 0:101    =  63.0000m
+0:102   =  63.0000m 0:103   =  63.0000m 0:104    =  635.9439m
+0:107   =  53.1628m 0:888   =  2.0000  2:5      =  53.1628m



 Opening plot unit= 16
file=d4nor1.tr0

** hspice file created for circuit d4nor: transient&power @ 25.0c
****** transient analysis            tnom= 25.000 temp= 25.000
******
 vmax        =  6.3802E-01   at=  6.7826E-08
        from=  2.0000E-09   to=  8.0000E-08
 vmin        = -5.3923E-02   at=  6.7200E-08
        from=  2.0000E-09   to=  8.0000E-08
 vmin2       =  1.9445E-02
 tpll        =  6.1325E-11 targ=  4.3112E-09  trig=  4.2499E-09
 tplh        =  2.1956E-10 targ=  6.7370E-08  trig=  6.7150E-08
 trise       =  4.5618E-10 targ=  6.7673E-08  trig=  6.7217E-08
 tfall       =  2.0223E-10 targ=  7.1664E-08  trig=  7.1461E-08
 tdelay      =  1.5877E-10 targ=  6.7320E-08  trig=  6.7161E-08

      ***** job concluded
      total cpu time       16.01 seconds
        job started at  6:49: 1  25-jan93
```

```
        job ended   at   6:49:36  25-jan93


I am done with d4nor1.sp
Mon Jan 25 06:49:38 PST 1993
```

C. Listing File for DD3NAND Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to  250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        6:26:19  2-feb93  sun
** hspice file created for circuit dd3nand: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
**********************************************************
**********************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
*  d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
**********************************************************
**********************************************************
* hspice dcfl 3-input demorgan nand subcircuit
*            ina, inb, inc,  output, power, ground
.subckt dd3nand   1  2   3     4     5     6
x0 1       10 5 6 dinv
x1 2       11 5 6 dinv
x2 3       12 5 6 dinv
x3 10 11 12 13 5 6 d3nor
x4 13      4  5 6 dinv
.ends   dd3nand
**********************************************************
**********************************************************
* hspice dcfl 3-input nor subcircuit
*            ina, inb, inc,  output, power, ground
.subckt d3nor     1  2   3     4     5     6
*  d g s b
j0 5 4 4 6 jfet16 l=1.2 w=6.0
j1 4 1 6 6 jfet04 l=1.2 w=96.0
j2 4 2 6 6 jfet04 l=1.2 w=96.0
```

```
j3 4 3 6 6 jfet04 l=1.2 w=96.0
.ends  d3nor
************************************************************
************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2     3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
************************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next three lines used to provide test signal inputs for transient analysis
va 101 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vb 102 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
vc 103 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)



* main circuit
*  ina inb inc out pwr gnd subname
x3 101 102 103 104  1   0  dd3nand   $ element under test
x4 104        107 888  0  d2load    $ test load

* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe ina=v(101) inb=v(102) inc=v(103) output=v(104)
.probe tran p(vds) p(vload) power

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(104) from=2ns to=42ns
.meas tran vmin min v(104) from=2ns to=42ns
.meas tran tphl trig v(101) val='(vmax-vmin)*.5' td=2ns
```

```
+ rise=1 targ v(104) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(103) val='(vmax-vmin)*.5' td=2ns
+ fall=1 targ v(104) val='(vmax-vmin)*.5' td=32ns rise=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=32ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
.meas tran tfall trig v(104) val='0.9*vmax' td=25ns
+ fall=1 targ v(104) val='vmin+0.1*vmax' fall=1
.meas tran tdelay trig v(103) val=.2835 td=32ns fall=1
+      targ v(104) val=.2835 rise=1
.tran 100ps 42ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit dd3nand: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x3.                    dd3nand     1.00
   2 x4.                    d2load      1.00
   3 x3.x0.                  dinv       1.00
   4 x3.x1.                  dinv       1.00
   5 x3.x2.                  dinv       1.00
   6 x3.x3.                  d3nor      1.00
   7 x3.x4.                  dinv       1.00
   8 x4.x0.                  dinv       1.00
   9 x4.x1.                  dinv       1.00
 Opening plot unit= 15
file=dd3nand1.pa0

** hspice file created for circuit dd3nand: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
  node   =voltage     node   =voltage     node   =voltage


+0:1     =  2.0000  0:101    =  63.0000m 0:102    =  63.0000m
+0:103    =  63.0000m 0:104    = 636.6116m 0:107    =  53.0853m
+0:888    =  2.0000  1:10     = 651.4791m 1:11     = 651.4791m
+1:12     = 651.4791m 1:13     =  26.2297m 2:5      =  53.0853m



 Opening plot unit= 16
file=dd3nand1.tr0

** hspice file created for circuit dd3nand: transient&power @ 25.0c
****** transient analysis             tnom= 25.000 temp= 25.000
******
 vmax         =  6.4002E-01   at=  3.4050E-08
```

```
        from= 2.0000E-09   to= 4.2000E-08
 vmin       = 5.1063E-02   at= 2.9925E-08
        from= 2.0000E-09   to= 4.2000E-08
 tphl       = 2.5424E-08 targ= 2.9665E-08  trig= 4.2408E-09
 tplh       = 1.3913E-10 targ= 3.3698E-08  trig= 3.3559E-08
 trise      = 3.3657E-10 targ= 3.3969E-08  trig= 3.3633E-08
 tfall      = 1.3463E-10 targ= 2.9722E-08  trig= 2.9588E-08
 tdelay     = 1.3311E-10 targ= 3.3694E-08  trig= 3.3561E-08

      ***** job concluded
      total cpu time       18.28 seconds
        job started at  6:26:19  2-feb93
        job ended  at  6:27:15  2-feb93


I am done with dd3nand1.sp
Tue Feb  2 06:27:16 PST 1993
```

D. Listing File for DD4AND Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to  250000 words. (  2000000 bytes)

******    h s p i c e   9007d        7: 4:18  26-jan93   sun
** hspice file created for circuit dd4and: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
************************************************************
************************************************************
* hspice dcfl 4-input nor subcircuit
*           ina, inb, inc, ind, output, power, ground
.subckt d4nor    1  2   3   4    5     6    7
* d g s b
j0 6 5 5 7 jfet16 l=1.2 w=6.0
j1 5 1 7 7 jfet04 l=1.2 w=96.0
```

```
j2 5 2 7 7 jfet04 l=1.2 w=96.0
j3 5 3 7 7 jfet04 l=1.2 w=96.0
j4 5 4 7 7 jfet04 l=1.2 w=96.0
.ends  d4nor
************************************************************
************************************************************
* hspice dcfl 4-input demorgan  and subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt dd4and  1   2   3   4    5     6   7
x0 1          10 6 7 dinv
x1 2          11 6 7 dinv
x2 3          12 6 7 dinv
x3 4          13 6 7 dinv
x4 10 11 12 13  5  6 7 d4nor
.ends  dd4and
************************************************************
************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2    3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
************************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next three lines used to provide test signal inputs for transient analysis
va 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vb 101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
vc 102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)
vd 103 0 pulse(0.063 0.63 33600ps 100ps 100ps 33400ps 67200ps)


* main circuit
*  ina inb inc ind out pwr gnd subname
x3 100 101 102 103 104  1   0  dd4and    $ element under test
x4 104           107 888  0  d2load    $ test load

* measurement parameters
```

```
* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104.0)

* next two lines are used for transient analysis
.probe ina=v(100) inb=v(101) inc=v(102) ind=v(103) output=v(104)
.probe tran p(vds) p(vload) power

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(104) from=2ns to=80ns
.meas tran vmin min v(104) from=2ns to=80ns
* next line is adjustment necessary to facilitate measuring tfall. if
* vmin is used in tfall calc, then the tfall calculation fails as the is a larg
e
* negative voltage spike when the four input mesfets switch from
* all on to all off and this skews the targ parameter. notice that
* vmin2 is used only in the tfall calculation line.
.meas tran vmin2 find v(104) at=64ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=62ns
+ fall=1 targ v(104) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=60ns
+ rise=1 targ v(104) val='(vmax-vmin)*.5' td=60ns rise=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
.meas tran tfall trig v(104) val='0.9*vmax' td=2ns
+ fall=1 targ v(104) val='vmin+0.1*vmax' fall=1
.meas tran tdelay trig v(100) val=.2835 td=60ns rise=1
+       targ v(104) val=.2835 rise=1
.tran 150ps 80ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit dd4and: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x3.                    dd4and      1.00
   2 x4.                    d2load      1.00
   3 x3.x0.                  dinv       1.00
   4 x3.x1.                  dinv       1.00
   5 x3.x2.                  dinv       1.00
   6 x3.x3.                  dinv       1.00
   7 x3.x4.                  d4nor      1.00
   8 x4.x0.                  dinv       1.00
   9 x4.x1.                  dinv       1.00
 Opening plot unit= 15
file=dd4and1.pa0

** hspice file created for circuit dd4and: transient&power @ 25.0c
```

```
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
  node   =voltage     node   =voltage     node   =voltage


+0:1     =  2.0000  0:100    =  63.0000m 0:101    =  63.0000m
+0:102   =  63.0000m 0:103   =  63.0000m 0:104    =  23.1758m
+0:107   =  1.9925  0:888    =  2.0000  1:10     = 650.4087m
+1:11    = 650.4087m 1:12    = 650.4087m 1:13     = 650.4087m
+2:5     =  1.9925



 Opening plot unit= 16
file=dd4and1.tr0

** hspice file created for circuit dd4and: transient&power @ 25.0c
****** transient analysis            tnom= 25.000 temp= 25.000
******
 vmax        = 6.4077E-01   at= 6.7150E-08
        from= 2.0000E-09   to= 8.0000E-08
 vmin        = 1.6595E-02   at= 7.5700E-08
        from= 2.0000E-09   to= 8.0000E-08
 vmin2       = 6.3620E-01
 tphl        = 7.5761E-11 targ= 6.7232E-08  trig= 6.7156E-08
 tplh        = 1.5859E-10 targ= 6.3203E-08  trig= 6.3044E-08
 trise       = 4.1758E-10 targ= 6.3491E-08  trig= 6.3074E-08
 tfall       = 1.0060E-10 targ= 6.7281E-08  trig= 6.7181E-08
 tdelay      = 1.3853E-10 targ= 6.3177E-08  trig= 6.3039E-08

      ***** job concluded
       total cpu time       24.41 seconds
         job started at   7: 4:18  26-jan93
         job ended  at    7: 5:11  26-jan93


I am done with dd4and1.sp
Tue Jan 26 07:05:12 PST 1993
```

E. Listing File for DD4OR Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        21: 2:42  26-jan93   sun
** hspice file created for circuit dd4or: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
```

```
****** input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
**********************************************************
**********************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
**********************************************************
**********************************************************
* hspice dcfl 4-input nor subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt d4nor    1  2   3   4    5     6    7
* d g s b
j0 6 5 5 7 jfet16 l=1.2 w=6.0
j1 5 1 7 7 jfet04 l=1.2 w=96.0
j2 5 2 7 7 jfet04 l=1.2 w=96.0
j3 5 3 7 7 jfet04 l=1.2 w=96.0
j4 5 4 7 7 jfet04 l=1.2 w=96.0
.ends  d4nor
**********************************************************
**********************************************************
* subcircuit dcfl 4-input or
*          ina inb inc ind output power ground
.subckt dd4or  1  2  3  4   5    6    7
*  ina inb inc ind out pwr gnd subname
x0  1  2  3  4  8  6  7  d4nor
x1  8           5  6  7  dinv
.ends  dd4or
**********************************************************
**********************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2    3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
**********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
**********************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply
```

```
* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next three lines used to provide test signal inputs for transient analysis
va 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vb 101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
vc 102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)
vd 103 0 pulse(0.063 0.63 33600ps 100ps 100ps 33400ps 67200ps)


* main circuit
*  ina inb inc ind out pwr gnd subname
x3 100 101 102 103 104  1   0  dd4or    $ element under test
x4 104           107 888  0  d2load    $ test load

* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe ina=v(100) inb=v(101) inc=v(102) ind=v(103) output=v(104)
.probe tran p(vds) p(vload) power

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(104) from=2ns to=80ns
.meas tran vmin min v(104) from=2ns to=80ns
* next line is adjustment necessary to facilitate measuring tfall. if
* vmin is used in tfall calc, then the tfall calculation fails as the is a larg
e
* negative voltage spike when the four input mesfets switch from
* all on to all off and this skews the targ parameter. notice that
* vmin2 is used only in the tfall calculation line.
.meas tran vmin2 find v(104) at=64ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=62ns
+ fall=1 targ v(104) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=70ns
+ rise=1 targ v(104) val='(vmax-vmin)*.5' td=70ns rise=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
.meas tran tfall trig v(104) val='0.9*vmax' td=2ns
+ fall=1 targ v(104) val='vmin+0.1*vmax' fall=1
.meas tran tdelay trig v(100) val=.2835 td=70ns rise=1
+       targ v(104) val=.2835 td=70ns rise=1
.tran 150ps 80ns
.options scale=1e-06 brief=0 nopage measout post probe
```

```
.end
** hspice file created for circuit dd4or: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x3.                    dd4or      1.00
   2 x4.                    d2load     1.00
   3 x3.x0.                  d4nor      1.00
   4 x3.x1.                  dinv       1.00
   5 x4.x0.                  dinv       1.00
   6 x4.x1.                  dinv       1.00
 Opening plot unit= 15
file=dd4or1.pa0

** hspice file created for circuit dd4or: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
  node   =voltage     node   =voltage     node   =voltage


+0:1     =  2.0000  0:100    =  63.0000m 0:101    =  63.0000m
+0:102   =  63.0000m 0:103   =  63.0000m 0:104    =  52.0403m
+0:107   =  1.9872  0:888    =  2.0000  1:8      =658.0337m
+2:5     =  1.9872


 Opening plot unit= 16
file=dd4or1.tr0

** hspice file created for circuit dd4or: transient&power @ 25.0c
****** transient analysis              tnom= 25.000 temp= 25.000
******
 vmax        = 6.4095E-01   at= 3.3625E-08
         from= 2.0000E-09   to= 8.0000E-08
 vmin        = 5.1203E-02   at= 6.7750E-08
         from= 2.0000E-09   to= 8.0000E-08
 vmin2       = 6.3663E-01
 tphl        = 2.5787E-10 targ= 6.7417E-08  trig= 6.7159E-08
 tplh        = 1.2195E-10 targ= 7.1563E-08  trig= 7.1441E-08
 trise       = 3.5080E-10 targ= 4.6374E-09  trig= 4.2866E-09
 tfall       = 1.6879E-10 targ= 6.7496E-08  trig= 6.7328E-08
 tdelay      = 1.1768E-10 targ= 7.1557E-08  trig= 7.1439E-08

      ***** job concluded
      total cpu time       17.67 seconds
         job started at  21: 2:42  26-jan93
         job ended   at  21: 3:18  26-jan93
```

```
I am done with dd4or1.sp
Tue Jan 26 21:03:20 PST 1993
```

F. Listing File for CPDFF Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to  250000 words. (  2000000 bytes)

******    h s p i c e   9007d        8:43: 4  2-feb93  sun
** hspice file created for circuit cpdff: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* subcircuit hspice dcfl /clear d flip flop
* wakerly pg 363 - 31july 1992
***         d clk /clr  q  /q  power  ground
.subckt cpdff  1  2  3   4 5    6     7
x0    12  10        9  6  7  dd2nand
x1  9 3  2         10 6  7  dd3nand
x2  10 2  12        11 6  7  dd3nand
x3  11 3  1         12 6  7  dd3nand
x4    10  5        4  6  7  dd2nand
x5  4  3  11        5  6  7  dd3nand
.ends  cpdff
************************************************************
************************************************************
* hspice dcfl 3-input nor subcircuit
*           ina, inb, inc,  output, power, ground
.subckt d3nor     1  2   3     4     5      6
* d g s b
j0 5 4 4 6 jfet16 l=1.2 w=6.0
j1 4 1 6 6 jfet04 l=1.2 w=96.0
j2 4 2 6 6 jfet04 l=1.2 w=96.0
j3 4 3 6 6 jfet04 l=1.2 w=96.0
.ends  d3nor
************************************************************
* hspice dcfl 3-input demorgan nand subcircuit
*           ina, inb, inc,  output, power, ground
.subckt dd3nand  1  2   3     4     5      6
x0 1       10 5 6 dinv
x1 2       11 5 6 dinv
```

```
x2 3      12 5 6 dinv
x3 10 11 12 13 5 6 d3nor
x4 13     4  5 6 dinv
.ends  dd3nand
*************************************************************
*************************************************************
* hspice dcfl 2-input nor subcircuit
*           ina, inb, output, power, ground
.subckt d2nor    1   2   3    4    5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 5 5 jfet04 l=1.2 w=96.0
j2 3 2 5 5 jfet04 l=1.2 w=96.0
.ends  d2nor
*************************************************************
* hspice dcfl 2-input demorgan nand subcircuit
*           ina, inb, output, power, ground
.subckt dd2nand   1   2   3    4    5
x0 1    10 4 5 dinv
x1 2    11 4 5 dinv
x2 10 11 12 4 5 d2nor
x3 12   3  4 5 dinv
.ends  dd2nand
*************************************************************
*************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
*************************************************************
*************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2    3    4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
*************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*************************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc  2.0v  $ test load power supply

* temperature card
*.temp 85.0
```

```
* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next three lines used to provide test signal inputs for transient analysis
va 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vb 101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
vc 102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)



* main circuit
*  d  clk  clr  q   /q power ground
x0 101 100  102 104 105  1     0   cpdff    $ element under test
x1 104     107     888     0   d2load   $ test load
x2 105     108     888     0   d2load   $ test load
* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe din=v(101) clk=v(100) clr=v(102) q=v(104) qnot=v(105)
.probe tran p(vds) p(vload) power

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(104) from=2ns to=40ns
.meas tran vmin min v(104) from=2ns to=40ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=27ns
+ rise=1 targ v(105) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=27ns
+ rise=1 targ v(104) val='(vmax-vmin)*.5' td=2ns rise=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
.meas tran tfall trig v(105) val='0.9*vmax' td=2ns
+ fall=1 targ v(105) val='vmin+0.1*vmax' fall=1
.meas tran tdelay trig v(100) val=.2835 td=27ns rise=1
+       targ v(105) val=.2835 td=20ns fall=1
.tran 50ps 40ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit cpdff: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                  cpdff       1.00
   2 x1.                  d2load      1.00
   3 x2.                  d2load      1.00
```

```
  4 x0.x0.                dd2nand    1.00
  5 x0.x1.                dd3nand    1.00
  6 x0.x2.                dd3nand    1.00
  7 x0.x3.                dd3nand    1.00
  8 x0.x4.                dd2nand    1.00
  9 x0.x5.                dd3nand    1.00
 10 x1.x0.                 dinv      1.00
 11 x1.x1.                 dinv      1.00
 12 x2.x0.                 dinv      1.00
 13 x2.x1.                 dinv      1.00
 14 x0.x0.x0.               dinv      1.00
 15 x0.x0.x1.               dinv      1.00
 16 x0.x0.x2.               d2nor     1.00
 17 x0.x0.x3.               dinv      1.00
 18 x0.x1.x0.               dinv      1.00
 19 x0.x1.x1.               dinv      1.00
 20 x0.x1.x2.               dinv      1.00
 21 x0.x1.x3.               d3nor     1.00
 22 x0.x1.x4.               dinv      1.00
 23 x0.x2.x0.               dinv      1.00
 24 x0.x2.x1.               dinv      1.00
 25 x0.x2.x2.               dinv      1.00
 26 x0.x2.x3.               d3nor     1.00
 27 x0.x2.x4.               dinv      1.00
 28 x0.x3.x0.               dinv      1.00
 29 x0.x3.x1.               dinv      1.00
 30 x0.x3.x2.               dinv      1.00
 31 x0.x3.x3.               d3nor     1.00
 32 x0.x3.x4.               dinv      1.00
 33 x0.x4.x0.               dinv      1.00
 34 x0.x4.x1.               dinv      1.00
 35 x0.x4.x2.               d2nor     1.00
 36 x0.x4.x3.               dinv      1.00
 37 x0.x5.x0.               dinv      1.00
 38 x0.x5.x1.               dinv      1.00
 39 x0.x5.x2.               dinv      1.00
 40 x0.x5.x3.               d3nor     1.00
 41 x0.x5.x4.               dinv      1.00
 Opening plot unit= 15
file=cpdff1.pa0

** hspice file created for circuit cpdff: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage      node   =voltage      node   =voltage


+ 0:1     =  2.0000  0:100   = 63.0000m 0:101   = 63.0000m
+ 0:102   = 63.0000m 0:104   = 52.0504m 0:105   = 624.0322m
+ 0:107   =  1.9872  0:108   = 54.9711m 0:888   =  2.0000
```

```
+ 1:9    = 52.0506m 1:10    = 624.0441m 1:11    = 636.5449m
+ 1:12   = 636.5992m 2:5    =  1.9872  3:5     = 54.9711m
+ 4:10   = 53.0867m 4:11    = 54.9689m 4:12     = 658.5204m
+ 5:10   = 651.5268m 5:11   = 651.4803m 5:12    = 651.4803m
+ 5:13   = 26.2332m 6:10    = 54.9689m 6:11     = 658.6219m
+ 6:12   = 53.0867m 6:13    = 51.9641m 7:10     = 53.0929m
+ 7:11   = 653.4945m 7:12   = 653.4945m 7:13    = 32.4207m
+ 8:10   = 54.9689m 8:11    = 54.9711m 8:12     = 658.5128m
+ 9:10   = 653.5426m 9:11   = 653.4958m 9:12    = 53.0929m
+ 9:13   = 32.4248m


 Opening plot unit= 16
file=cpdff1.tr0

** hspice file created for circuit cpdff: transient&power @ 25.0c
****** transient analysis          tnom= 25.000 temp= 25.000
******
 vmax       = 6.2537E-01   at= 3.4000E-08
        from= 2.0000E-09   to= 4.0000E-08
 vmin       = 5.0705E-02   at= 3.4475E-08
        from= 2.0000E-09   to= 4.0000E-08
 tphl       = 9.3060E-10 targ= 3.0370E-08  trig= 2.9440E-08
 tplh       = 4.4528E-10 targ= 2.9885E-08  trig= 2.9440E-08
 trise      = 4.1904E-10 targ= 3.0219E-08  trig= 2.9800E-08
 tfall      = 1.9364E-10 targ= 3.0445E-08  trig= 3.0251E-08
 tdelay     = 9.3260E-10 targ= 3.0371E-08  trig= 2.9439E-08

      ***** job concluded
      total cpu time       68.01 seconds
         job started at  8:43: 4  2-feb93
         job ended  at  8:46:37  2-feb93


I am done with cpdff1.sp
Tue Feb  2 08:46:39 PST 1993
```

G. Listing File for DLATCH Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to  250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        7:17:20 27-jan93  sun
** hspice file created for circuit dlatch: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
```

```
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
************************************************************
************************************************************
* subcircuit dcfl d-latch using generic gates
*           d  clk q  /q power ground
.subckt dlatch  1  2 3 4   5    6
*   ina  inb output  power ground subname
x0   1   2   8     5    6  d2nand
x1   1       7     5    6  dinv
x2   2   7   9     5    6  d2nand
x3   8   4   3     5    6  d2nand
x4   9   3   4     5    6  d2nand
.ends dlatch
************************************************************
************************************************************
* hspice dcfl 2-input real nand subcircuit
*            ina, inb, output, power, ground
.subckt d2nand   1   2    3     4    5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 6 5 jfet04 l=1.2 w=192.0
j2 6 2 5 5 jfet04 l=1.2 w=192.0
.ends d2nand
************************************************************
************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2     3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends   d2load
************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
************************************************************
* power supplies
vds    1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
```

```
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next three lines used to provide test signal inputs for transient analysis
va 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vb 101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)



* main circuit
*  d clk  q  /q power ground
x3 101 100  104 105  1    0   dlatch   $ element under test
x4 104    107    888   0   d2load   $ test load
x5 105    108    888   0   d2load   $ test load
* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe din=v(101) clk=v(100) q=v(104) qnot=v(105)
.probe tran p(vds) p(vload) power

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(104) from=2ns to=24ns
.meas tran vmin min v(104) from=2ns to=24ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(104) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(105) val='(vmax-vmin)*.5' td=2ns rise=1
.meas tran trise trig v(105) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(105) val='0.9*vmax' rise=1
.meas tran tfall trig v(104) val='0.9*vmax' td=2ns
+ fall=1 targ v(104) val='vmin+0.1*vmax' fall=1
.meas tran tdelay trig v(100) val=.2835 td=20ns rise=1
+      targ v(104) val=.2835 td=20ns fall=1
.tran 50ps 24ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit dlatch: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x3.                    dlatch      1.00
   2 x4.                    d2load      1.00
```

```
  3 x5.                 d2load     1.00
  4 x3.x0.              d2nand     1.00
  5 x3.x1.              dinv       1.00
  6 x3.x2.              d2nand     1.00
  7 x3.x3.              d2nand     1.00
  8 x3.x4.              d2nand     1.00
  9 x4.x0.              dinv       1.00
 10 x4.x1.              dinv       1.00
 11 x5.x0.              dinv       1.00
 12 x5.x1.              dinv       1.00
 Opening plot unit= 15
file=dlatch1.pa0

** hspice file created for circuit dlatch: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage     node   =voltage     node   =voltage


+ 0:1     =  2.0000  0:100   =  63.0000m  0:101   =  63.0000m
+ 0:104   = 632.6195m  0:105   =  78.6713m  0:107   =  53.5871m
+ 0:108   =  1.9798  0:888   =  2.0000  1:7     = 622.5037m
+ 1:8     =  1.2482  1:9     = 678.4738m  2:5     =  53.5871m
+ 3:5     =  1.9798  4:6     =  73.6471m  6:6     =  8.6084m
+ 7:6     = 641.3001m  8:6     =  48.5086m


 Opening plot unit= 16
file=dlatch1.tr0

** hspice file created for circuit dlatch: transient&power @ 25.0c
****** transient analysis           tnom= 25.000 temp= 25.000
******
 vmax        =  6.3262E-01   at=  2.0175E-08
        from=  2.0000E-09   to=  2.4000E-08
 vmin        =  4.9117E-02   at=  1.2700E-08
        from=  2.0000E-09   to=  2.4000E-08
 tphl        =  6.1047E-10 targ=  4.8508E-09  trig=  4.2403E-09
 tplh        =  2.2097E-10 targ=  4.4613E-09  trig=  4.2403E-09
 trise       =  5.3429E-10 targ=  4.8861E-09  trig=  4.3518E-09
 tfall       =  3.7997E-10 targ=  4.9966E-09  trig=  4.6166E-09
 tdelay      =  6.1734E-10 targ=  2.1656E-08  trig=  2.1039E-08

      ***** job concluded
      total cpu time       19.75 seconds
        job started at   7:17:20  27-jan93
        job ended  at    7:18: 2  27-jan93
```

```
I am done with dlatch1.sp
Wed Jan 27 07:18:04 PST 1993
```

H. Listing File for DELAY Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        11: 1:31  30-jan93   sun
** hspice file created for circuit delay: transient&power @ 25.0c
****** copyright 1990 meta-software.inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
**********************************************************
**********************************************************
* subcircuit delay generates  delayed clock pulse
*          input  output  power  ground
.subckt delay   1    2     3     4
*   ina inb       out   power  ground  subname
x0   1            9     3     4    bdinv
x1   9            6     3     4    bdinv
x2   1  6         2     3     4    bs2and
.ends delay
**********************************************************
**********************************************************
* subcircuit sbfl 2-input nor
*          ina   inb  output power ground
.subckt bs2nor  1    2    3    4    5
* d g s
j0 8 1 5 0 jfet04 l=1.2 w=180.0
j1 8 2 5 0 jfet04 l=1.2 w=180.0
j2 4 8 8 0 jfet16 l=1.2 w=10.0
j3 4 8 3 0 jfet04 l=1.2 w=224.0
j4 3 2 5 0 jfet04 l=1.2 w=224.0
j5 3 1 5 0 jfet04 l=1.2 w=224.0
.ends  bs2nor
**********************************************************
**********************************************************
* subcircuit dcfl-sbfl 2- input and
*           ina   inb  output power ground
.subckt bs2and  1    2    3    4    5
*  ina inb out pwr gnd subname
x0 1      9  4  5  bdinv  $dcfl gate
x1 2      6  4  5  bdinv  $dcfl gate
x2 9   6  3  4  5  bs2nor  $sbfl gate
```

```
.ends  bs2and
*************************************************************
*************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt bdinv   1    2    3    4
*  d g s b
j0 3 2 2 4 jfet20 l=3.0 w=40.0
j1 2 1 4 4 jfet04 l=1.2 w=240.0
.ends  bdinv
*******************************************************
*******************************************************
* subcircuit sbfl inverter
*          input, output, power, ground
.subckt sinv   1    2    3    4
*  d g s
j0 9 1 4 0 jfet04 l=1.2 w=48.0
j1 3 9 9 0 jfet16 l=1.2 w=3.0
j2 3 9 2 0 jfet04 l=1.2 w=48.0
j3 2 1 4 0 jfet04 l=1.2 w=48.0
.ends sinv
*******************************************************
*************************************************************
* hspice sbfl standard load subcircuit
*          input, output, power, ground
.subckt s10load  1     2    3     4
x0 1 5  3 4 sinv
x1 1 2  3 4 sinv
x2 1 6  3 4 sinv
x3 1 7  3 4 sinv
x4 1 8  3 4 sinv
x5 1 9  3 4 sinv
x6 1 10 3 4 sinv
x7 1 11 3 4 sinv
x8 1 12 3 4 sinv
x9 1 13 3 4 sinv
.ends  s10load
*************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*******************************************************
* power supplies
vds   1   0 dc  2.0v  $ elemert under test power supply
vload 888  0 dc  2.0v  $ test load power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0
```

```
* next line is used to provide the test signal input for transient analysis
va0 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)

* main circuit
x3 100 104  1    0 delay      $ element under test
x4 104 107  888  0 s10load    $ test load

* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe input=v(100) output=v(104)
.probe tran p(vds) p(vload) power

* next 8 lines will calculate vmax vmin trise .fall and tdelay :transient analy
s
.meas tran vmax max v(104) from=2ns to=20ns
.meas tran vmin min v(104) from=2ns to=20ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(104) val='(vmax-vmin)*.5' td=2ns rise=1
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=2ns
+ fall=1 targ v(104) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
.meas tran tfall trig v(104) val='0.9*vmax' td=2ns
+ fall=2 targ v(104) val='vmin+0.1*vmax' fall=2
.meas tran tdelay trig v(100) val=.2835 td=2ns rise=1
+       targ v(104) val=.2835 rise=1
.tran 50ps 20ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit delay: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x3.                    delay       1.00
   2 x4.                    s10load     1.00
   3 x3.x0.                 bdinv       1.00
   4 x3.x1.                 bdinv       1.00
   5 x3.x2.                 bs2and      1.00
   6 x4.x0.                 sinv        1.00
   7 x4.x1.                 sinv        1.00
   8 x4.x2.                 sinv        1.00
   9 x4.x3.                 sinv        1.00
  10 x4.x4.                 sinv        1.00
```

```
 11 x4.x5.                sinv      1.00
 12 x4.x6.                sinv      1.00
 13 x4.x7.                sinv      1.00
 14 x4.x8.                sinv      1.00
 15 x4.x9.                sinv      1.00
 16 x3.x2.x0.             bdinv     1.00
 17 x3.x2.x1.             bdinv     1.00
 18 x3.x2.x2.             bs2nor    1.00
Opening plot unit= 15
file=delay1.pa0

** hspice file created for circuit delay: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage  simulation time is    0.
   node   =voltage     node   =voltage     node   =voltage


+ 0:1     =  2.0000  0:100   =  63.0000m 0:104   =  7.0515m
+ 0:107   =  1.7620  0:888   =  2.0000  1:6     =  33.9777m
+ 1:9     = 636.1803m 2:5     =  1.7620  2:6     =  1.7620
+ 2:7     =  1.7620  2:8     =  1.7620  2:9     =  1.7620
+ 2:10    =  1.7620  2:11    =  1.7620  2:12    =  1.7620
+ 2:13    =  1.7620  5:6     = 613.1155m 5:9     = 612.9554m
+ 6:9     =  1.9945  7:9     =  1.9945  8:9     =  1.9945
+ 9:9     =  1.9945  10:9    =  1.9945  11:9    =  1.9945
+12:9     =  1.9945  13:9    =  1.9945  14:9    =  1.9945
+15:9     =  1.9945  18:8    =  26.8679m


 Opening plot unit= 16
file=delay1.tr0

** hspice file created for circuit delay: transient&power @ 25.0c
****** transient analysis          tnom= 25.000 temp= 25.000
******
  vmax        = 6.6232E-01   at= 1.6800E-08
        from= 2.0000E-09   to= 2.0000E-08
  vmin        = -1.8424E-02   at= 4.5000E-09
        from= 2.0000E-09   to= 2.0000E-08
  tphl        = 4.3145E-10 targ= 4.6804E-09  trig= 4.2489E-09
  tplh        = 3.4595E-10 targ= 8.6970E-09  trig= 8.3511E-09
  trise       = 2.5538E-10 targ= 4.8088E-09  trig= 4.5535E-09
  tfall       = 3.0072E-10 targ= 1.7273E-08  trig= 1.6972E-08
  tdelay      = 4.1530E-10 targ= 4.6542E-09  trig= 4.2389E-09

      ***** job concluded
      total cpu time       30.94 seconds
         job started at  11: 1:31  30-jan93
         job ended   at  11: 2:37  30-jan93
```

```
I am done with delay1.sp
Sat Jan 30 11:02:38 PST 1993

I.      Listing File for LVL Transient Analysis @ 25.0C

Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install config.. ation file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        22:40:59  30-jan93   sun
** hspice file created for circuit lvl: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* subcircuit level-shifter to drive dfets
* use hspice diode models for backconnected mesfets
*          input output vds vss
.subckt lvl   1    2    3  4
*    d  g    s   b
x0   1  25   3   0   dinv
j1   3  25   6   4   jfet04 l=1.2 w=20.0
j2   7  6    7   4   dio16  l=1.2 w=4.0
j3   7  4    4   4   jfet20 l=3.0 w=3.0
j4   3  9    9   4   jfet16 l=1.2 w=3.0
j5   9  7    0   4   jfet16 l=1.2 w=10.0
j6   3  9    10  4   jfet16 l=1.2 w=20.0
j7   11 10   11  4   dio16  l=1.2 w=20.0
j8   2  11   2   4   dio16  l=1.2 w=20.0
j9   2  4    4   4   jfet16 l=1.2 w=12.0
j10  12 2    12  4   dio16  l=1.2 w=10.0
j11  13 12   13  4   dio16  l=1.2 w=10.0
j12  14 13   14  4   dio16  l=1.2 w=10.0
j13  4  14   4   4   dio16  l=1.2 w=10.0
.ends lvl
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   '    2    3    4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
```

```
.ends dinv
*************************************************************
* hspice d mesfet load subcircuit
*          input,  power, ground
.subckt dm10load  1   3     4
j0 3 1 4 4 jfet16 l=1.2 w= 10.0
j1 3 1 4 4 jfet16 l=1.2 w= 10.0
j2 3 1 4 4 jfet16 l=1.2 w= 10.0
j3 3 1 4 4 jfet16 l=1.2 w= 10.0
j4 3 1 4 4 jfet16 l=1.2 w= 10.0
j5 3 1 4 4 jfet16 l=1.2 w= 10.0
j6 3 1 4 4 jfet16 l=1.2 w= 10.0
j7 3 1 4 4 jfet16 l=1.2 w= 10.0
j8 3 1 4 4 jfet16 l=1.2 w= 10.0
j9 3 1 4 4 jfet16 l=1.2 w= 10.0
.ends   dm10load
*************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*************************************************************
* power supplies
vds   1  0 dc  2.0v  $ element under test power supply
vss   777 0 dc -2.5v $ test load negative power supply
vload 888 0 dc  2.0v  $ test load positive power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next line is used to provide the test signal input for transient analysis
va0 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)

* main circuit
x0 100 104  1   777 lvl       $ element under test
x1 104    888  0  dm10load    $ test load

* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe input=v(100) output=v(104)
.probe tran p(vds) p(vss) p(vload) power

* next 8 lines will calculate vmax vmin trise tfall and tdelay :transient analy
s
```

```
.meas tran vimax max v(100) from=2ns to=20ns $ vmax input
.meas tran vimin min v(100) from=2ns to=20ns $ vmin input
.meas tran vmax max v(104) from=2ns to=20ns
.meas tran vmin min v(104) from=2ns to=20ns
.meas tran tphl trig v(100) val='(vimax-vimin)*.5' td=2ns
+ rise=1 targ v(104) val='(vmax+vmin)*.5' td=2ns rise=1
.meas tran tplh trig v(100) val='(vimax-vimin)*.5' td=2ns
+ fall=1 targ v(104) val='(vmax+vmin)*.5' td=2ns fall=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
.meas tran tfall trig v(104) val='0.9*vmax' td=2ns
+ fall=2 targ v(104) val='vmin+0.1*vmax' fall=2
.meas tran tdelay trig v(100) val=.2835 td=2ns rise=1
+       targ v(104) val=-.6000 rise=1
.tran 50ps 20ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit lvl: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                    lvl        1.00
   2 x1.                    dm10load    1.00
   3 x0.x0.                  dinv       1.00
 Opening plot unit= 15
file=lvl1.pa0

** hspice file created for circuit lvl: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
  node   =voltage     node   =voltage     node   =voltage


+0:1     =  2.0000  0:100    =  63.0000m 0:104    =  -1.2402
+0:777   =  -2.5000  0:888   =  2.0000  1:6      =  1.3537
+1:7     = 649.2362m 1:9     =  74.9851m 1:10     = 230.9228m
+1:11    =-504.6211m 1:12    =  -1.5551  1:13    =  -1.8701
+1:14    =  -2.1850  1:25    =  1.9636



 Opening plot unit= 16
file=lvl1.tr0

** hspice file created for circuit lvl: transient&power @ 25.0c
****** transient analysis            tnom= 25.000 temp= 25.000
******
 vimax         =  6.3000E-01   at=  4.3000E-09
```

```
          from= 2.0000E-09   to= 2.0000E-08
 vimin       = 6.3000E-02   at= 2.0000E-09
          from= 2.0000E-09   to= 2.0000E-08
 vmax        = 1.0646E-01   at= 8.3500E-09
          from= 2.0000E-09   to= 2.0000E-08
 vmin        = -1.2403E+00  at= 1.7199E-08
          from= 2.0000E-09   to= 2.0000E-08
 tphl        = 2.9870E-10 targ= 4.5376E-09  trig= 4.2389E-09
 tplh        = 1.2030E-10 targ= 8.4814E-09  trig= 8.3611E-09
 trise       = 5.1389E-10 targ= 4.7920E-09  trig= 4.2781E-09
 tfall       = 2.4363E-10 targ= 1.7003E-08  trig= 1.6760E-08
 tdelay      = 2.9262E-10 targ= 4.5315E-09  trig= 4.2389E-09

      ***** job concluded
      total cpu time       18.46 seconds
         job started at  22:40:59  30-jan93
         job ended   at  22:41:40  30-jan93


I am done with lv11.sp
Sat Jan 30 22:41:41 PST 1993
```

J. Listing File for CLOCK Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        19:53:59  2-feb93  sun
** hspice file created for circuit clock: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt bdinv   1    2    3    4
*  d g s b
j0 3 2 2 4 jfet20 l=3.0 w=40.0
j1 2 1 4 4 jfet04 l=1.2 w=240.0
.ends   bdinv
************************************************************
* subcircuit sbfl 2-input nor
*          ina   inb  output power ground
.subckt bs2nor  1    2    3    4    5
```

```
* d g s
j0 8 1 5 0 jfet04 l=1.2 w=180.0
j1 8 2 5 0 jfet04 l=1.2 w=180.0
j2 4 8 8 0 jfet16 l=1.2 w=10.0
j3 4 8 3 0 jfet04 l=1.2 w=224.0
j4 3 2 5 0 jfet04 l=1.2 w=224.0
j5 3 1 5 0 jfet04 l=1.2 w=224.0
.ends  bs2nor
*************************************************************
* subcircuit sbfl 2- input and
*          ina   inb  output power ground
.subckt bs2and  1    2    3    4    5
*  ina inb out pwr gnd subname
x0 1      9  4  5  bdinv
x1 2      6  4  5  bdinv
x2 9   6  3  4  5  bs2nor
.ends  bs2and
*************************************************************
*************************************************************
* subckt hspice sbfl large 2-input nor
*          ina   inb  output power ground
.subckt csnor   1    2    3    4    5
* d g s b
j0 8 1 5 0 jfet04 l=1.2 w=144.0
j1 8 2 5 0 jfet04 l=1.2 w=144.0
j2 4 8 8 0 jfet16 l=1.2 w= 9.0
j3 4 8 3 0 jfet04 l=1.2 w=144.0
j4 3 2 5 0 jfet04 l=1.2 w=144.0
j5 3 1 5 0 jfet04 l=1.2 w=144.0
.ends csnor
*************************************************************
* hspice sbfl extra-large driver-inverter subcircuit
*          input, output, power, ground
.subckt ssinv   1    2    3    4
* d g s b
j0 9 1 4 0 jfet04 l=1.2 w=768.0
j1 3 9 9 0 jfet16 l=1.2 w= 48.0
j2 3 9 2 0 jfet04 l=1.2 w=768.0
j3 2 1 4 0 jfet04 l=1.2 w=768.0
.ends ssinv
*************************************************************
* hspice sbfl large driver-inverter subcircuit
*          input, output, power, ground
.subckt csinv   1    2    3    4
* d g s b
j0 9 1 4 0 jfet04 l=1.2 w=256.0
j1 3 9 9 0 jfet16 l=1.2 w= 16.0
j2 3 9 2 0 jfet04 l=1.2 w=384.0
j3 2 1 4 0 jfet04 l=1.2 w=384.0
.ends csinv
*************************************************************
```

```
* subcircuit delay generates fee d
*          input  output  power  ground
.subckt delay   1    2     3     4
*   ina inb       out   power  ground  subname
x0   1           9     3     4   bdinv
x1   9           6     3     4   bdinv
x2   1  6        2     3     4   bs2and
.ends delay
*********************************************************
* subcircuit for hspice two-phase sbfl clock
*          inclk ph1 ph2 ph2d ph1l ph2ld power1 power2  ground
.subckt clock  1  2  3   4   5    6    7    8      9
*  ina inb out pwr gnd subname
x0 1  2  10 7  9  csnor
x1 10    11 7  9  ssinv
x2 11    3  7  9  ssinv
x3 12 3  13 7  9  csnor
x4 13    14 7  9  ssinv
x5 14    2  7  9  ssinv
x6 1     12 7  9  csinv
x7 3     4  7  9  delay
x8 2     5  7  8  lvl
x9 4     6  7  8  lvl
.ends clock
*********************************************************
*********************************************************
* subcircuit level-shifter to drive dfets
* use hspice diode models for backconnected mesfets
*         input output vds vss
.subckt lvl  1    2    3  4
*    d  g    s    b
x0   1  25   3    0   dinv
j1   3  25   6    4   jfet04 l=1.2 w=20.0
j2   7  6    7    4   dio16  l=1.2 w=4.0
j3   7  4    4    4   jfet20 l=3.0 w=3.0
j4   3  9    9    4   jfet16 l=1.2 w=3.0
j5   9  7    0    4   jfet16 l=1.2 w=10.0
j6   3  9    10   4   jfet16 l=1.2 w=20.0
j7   11 10   11   4   dio16  l=1.2 w=20.0
j8   2  11   2    4   dio16  l=1.2 w=20.0
j9   2  4    4    4   jfet16 l=1.2 w=12.0
j10  12 2    12   4   dio16  l=1.2 w=10.0
j11  13 12   13   4   dio16  l=1.2 w=10.0
j12  14 13   14   4   dio16  l=1.2 w=10.0
j13  4  14   4    4   dio16  l=1.2 w=10.0
.ends lvl
*********************************************************
*********************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
```

```
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
*********************************************************
* hspice d mesfet load subcircuit
*          input, power, ground
.subckt dm10load  1   3     4
j0 3 1 4 4 jfet16 l=1.2 w= 10.0
j1 3 1 4 4 jfet16 l=1.2 w= 10.0
j2 3 1 4 4 jfet16 l=1.2 w= 10.0
j3 3 1 4 4 jfet16 l=1.2 w= 10.0
j4 3 1 4 4 jfet16 l=1.2 w= 10.0
j5 3 1 4 4 jfet16 l=1.2 w= 10.0
j6 3 1 4 4 jfet16 l=1.2 w= 10.0
j7 3 1 4 4 jfet16 l=1.2 w= 10.0
j8 3 1 4 4 jfet16 l=1.2 w= 10.0
j9 3 1 4 4 jfet16 l=1.2 w= 10.0
.ends   dm10load
*********************************************************
*********************************************************
* subcircuit sbfl inverter
*          input, output, power, ground
.subckt sinv   1    2    3    4
* d g s
j0 9 1 4 0 jfet04 l=1.2 w=48.0
j1 3 9 9 0 jfet16 l=1.2 w=3.0
j2 3 9 2 0 jfet04 l=1.2 w=48.0
j3 2 1 4 0 jfet04 l=1.2 w=48.0
.ends sinv
*********************************************************
*********************************************************
* hspice sbfl standard load subcircuit
*          input, output, power, ground
.subckt s10load  1     2    3     4
x0 1 5  3 4 sinv
x1 1 2  3 4 sinv
x2 1 6  3 4 sinv
x3 1 7  3 4 sinv
x4 1 8  3 4 sinv
x5 1 9  3 4 sinv
x6 1 10 3 4 sinv
x7 1 11 3 4 sinv
x8 1 12 3 4 sinv
x9 1 13 3 4 sinv
.ends   s10load
*********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*********************************************************
* power supplies
```

```
vds   1  0 dc  2.0v  $ element under test power supply
vss   777 0 dc -2.5v  $ test load negative power supply
vload 888 0 dc  2.0v  $ test load positive power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next line is used to provide the test signal input for transient analysis
va0 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)

* main circuit
x0 100 104 105 106 107 108 1   777  0 clock     $ element under test
x1 104 120            888     0 s10load    $ test load
x2 105 121            888     0 s10load    $ test load
x3 106 122            888     0 s10load    $ test load
x4 107              888     0 dm10load   $ test load
x5 108              888     0 dm10load   $ test load

* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
.probe inclk=v(100) ph1=v(104) ph2=v(105) ph2d=v(106) ph1l=v(107)
+ ph2ld=v(108)
.probe tran p(vds) p(vss) p(vload) power
.measure tran avgpwr avg p(vds) from 0.0ns to 20ns
* next 8 lines will calculate vmax vmin trise tfall and tdelay :transient analy
s
.meas tran vimax max v(100) from=2ns to=20ns $ vmax input
.meas tran vimin min v(100) from=2ns to=20ns $ vmin input
.meas tran vmax max v(104) from=2ns to=20ns
.meas tran vmin min v(104) from=2ns to=20ns
* next line is adjustment necessary to facilitate measuring tfall. if
* vmin is used in tfall calc, then the tfall calculation fails as the is a larg
e
* all on to all off and this skews the targ parameter. notice that
* vmin2 is used only in the tfall calculation line.
.meas tran vmin2 find v(104) at=11ns
.meas tran tphl trig v(100) val='(vimax-vimin)*.5' td=2ns
+ rise=1 targ v(104) val='(vmax+vmin)*.5' td=2ns rise=1
.meas tran tplh trig v(100) val='(vimax-vimin)*.5' td=2ns
+ fall=1 targ v(104) val='(vmax+vmin)*.5' td=2ns fall=1
.meas tran trise trig v(104) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(104) val='0.9*vmax' rise=1
```

```
.meas tran tfall trig v(104) val='0.9*vmax' td=16ns
+ fall=1 targ v(104) val='vmin2+0.1*vmax' fall=1
.meas tran tdelay trig v(100) val=0.2835 td=2ns rise=1
+      targ v(104) val=0.2835    rise=1
.tran 550ps 20ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit clock: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname             definition  multiplier
   0 main circuit
   1 x0.                  clock       1.00
   2 x1.                  s10load     1.00
   3 x2.                  s10load     1.00
   4 x3.                  s10load     1.00
   5 x4.                  dm10load    1.00
   6 x5.                  dm10load    1.00
   7 x0.x0.                csnor      1.00
   8 x0.x1.                ssinv      1.00
   9 x0.x2.                ssinv      1.00
  10 x0.x3.                csnor      1.00
  11 x0.x4.                ssinv      1.00
  12 x0.x5.                ssinv      1.00
  13 x0.x6.                csinv      1.00
  14 x0.x7.                delay      1.00
  15 x0.x8.                lvl        1.00
  16 x0.x9.                lvl        1.00
  17 x1.x0.                sinv       1.00
  18 x1.x1.                sinv       1.00
  19 x1.x2.                sinv       1.00
  20 x1.x3.                sinv       1.00
  21 x1.x4.                sinv       1.00
  22 x1.x5.                sinv       1.00
  23 x1.x6.                sinv       1.00
  24 x1.x7.                sinv       1.00
  25 x1.x8.                sinv       1.00
  26 x1.x9.                sinv       1.00
  27 x2.x0.                sinv       1.00
  28 x2.x1.                sinv       1.00
  29 x2.x2.                sinv       1.00
  30 x2.x3.                sinv       1.00
  31 x2.x4.                sinv       1.00
  32 x2.x5.                sinv       1.00
  33 x2.x6.                sinv       1.00
  34 x2.x7.                sinv       1.00
  35 x2.x8.                sinv       1.00
  36 x2.x9.                sinv       1.00
  37 x3.x0.                sinv       1.00
  38 x3.x1.                sinv       1.00
```

```
 39 x3.x2.              sinv      1.00
 40 x3.x3.              sinv      1.00
 41 x3.x4.              sinv      1.00
 42 x3.x5.              sinv      1.00
 43 x3.x6.              sinv      1.00
 44 x3.x7.              sinv      1.00
 45 x3.x8.              sinv      1.00
 46 x3.x9.              sinv      1.00
 47 x0.x7.x0.           bdinv     1.00
 48 x0.x7.x1.           bdinv     1.00
 49 x0.x7.x2.           bs2and    1.00
 50 x0.x8.x0.           dinv      1.00
 51 x0.x9.x0.           dinv      1.00
 52 x0.x7.x2.x0.        bdinv     1.00
 53 x0.x7.x2.x1.        bdinv     1.00
 54 x0.x7.x2.x2.        bs2nor    1.00
 Opening plot unit= 15
file=clock1.pa0

** hspice file created for circuit clock: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage      node   =voltage      node   =voltage


+ 0:1     =  2.0000  0:100   =  63.0000m 0:104   =  31.9774m
+ 0:105   = 688.8112m 0:106   = 658.8150m 0:107   =  -1.2402
+ 0:108   = 104.5431m 0:120   =  1.7422  0:121   =  30.1523m
+ 0:122   =  18.2371m 0:777   =  -2.5000  0:888   =  2.0000
+ 1:10    = 633.6943m  1:11    =  11.3673m  1:12    = 724.8418m
+ 1:13    =  41.8449m  1:14    = 692.6584m  2:5     =  1.7422
+ 2:6     =  1.7422  2:7     =  1.7422  2:8     =  1.7422
+ 2:9     =  1.7422  2:10    =  1.7422  2:11    =  1.7422
+ 2:12    =  1.7422  2:13    =  1.7422  3:5     =  30.1523m
+ 3:6     =  30.1523m  3:7     =  30.1523m  3:8     =  30.1523m
+ 3:9     =  30.1523m  3:10    =  30.1523m  3:11    =  30.1523m
+ 3:12    =  30.1523m  3:13    =  30.1523m  4:5     =  18.2371m
+ 4:6     =  18.2371m  4:7     =  18.2371m  4:8     =  18.2371m
+ 4:9     =  18.2371m  4:10    =  18.2371m  4:11    =  18.2371m
+ 4:12    =  18.2371m  4:13    =  18.2371m  7:8     =  1.2978
+ 8:9     =  53.4430m  9:9     =  1.3520  10:8    =  51.8795m
+11:9     =  1.3555  12:9    =  56.8574m 13:9    =  1.3729
+14:6     = 636.3051m 14:9    =  44.0977m 15:6    =  1.3578
+15:7     = 652.5225m 15:9    =  74.9274m 15:10   = 230.8765m
+15:11    =-504.6670m 15:12   =  -1.5552  15:13   =  -1.8701
+15:14    =  -2.1851  15:25   =  1.9694  16:6    =-379.7082m
+16:7     =  -1.0722  16:9    =  1.9993  16:10   =  1.5989
+16:11    = 851.7082m 16:12   =-546.5927m 16:13   =  -1.1977
+16:14    =  -1.8489  16:25   =  52.0530m 17:9    =  1.9911
+18:9     =  1.9911  19:9    =  1.9911  20:9    =  1.9911
```

```
+21:9    =  1.9911  22:9    =  1.9911  23:9    =  1.9911
+24:9    =  1.9911  25:9    =  1.9911  26:9    =  1.9911
+27:9    =  55.9050m 28:9    =  55.9050m 29:9    =  55.9050m
+30:9    =  55.9050m 31:9    =  55.9050m 32:9    =  55.9050m
+33:9    =  55.9050m 34:9    =  55.9050m 35:9    =  55.9050m
+36:9    =  55.9050m 37:9    =  52.0576m 38:9    =  52.0576m
+39:9    =  52.0576m 40:9    =  52.0576m 41:9    =  52.0576m
+42:9    =  52.0576m 43:9    =  52.0576m 44:9    =  52.0576m
+45:9    =  52.0576m 46:9    =  52.0576m 49:6    =  33.9838m
+49:9    =  44.0977m 54:8    =  1.3110


 Opening plot unit= 16
file=clock1.tr0

** hspice file created for circuit clock: transient&power @ 25.0c
****** transient analysis           tnom=  25.000 temp=  25.000
******
 avgpwr       = -3.1516E-01 from=  0.0000E+00   to=  2.0000E-08
 vimax        =  6.3000E-01  at=  4.3000E-09
        from=  2.0000E-09  to=  2.0000E-08
 vimin        =  6.3000E-02  at=  2.0000E-09
        from=  2.0000E-09  to=  2.0000E-08
 vmax         =  7.0077E-01  at=  8.6476E-09
        from=  2.0000E-09  to=  2.0000E-08
 vmin         = -4.1470E-02  at=  4.8753E-09
        from=  2.0000E-09  to=  2.0000E-08
 vmin2        =  3.1978E-02
 tphl         =  7.2371E-10 targ=  4.9626E-09  trig=  4.2389E-09
 tplh         =  3.8966E-10 targ=  8.7508E-09  trig=  8.3611E-09
 trise        =  1.4221E-10 targ=  5.0374E-09  trig=  4.8952E-09
 tfall        =  7.6519E-11 targ=  1.7178E-08  trig=  1.7102E-08
 tdelay       =  7.1342E-10 targ=  4.9523E-09  trig=  4.2389E-09

      ***** job concluded
      total cpu time      138.48 seconds
         job started at  19:53:59  2-feb93
         job ended  at  20: 1:17  2-feb93


I am done with clock1.sp
Tue Feb  2 20:01:18 PST 1993
```

K. Listing File for DECODER Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)
```

```
******    h s p i c e   9007d        20: 9:10  2-feb93  sun
** hspice file created for: circuit decoder: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
**********************************************************
**********************************************************
* subcircuit sbfl 3-input or
*          ina   inb   inc  output power ground
.subckt s3or   1    2    3    4    5    6
*  ina inb inc out pwr gnd subname
x0  1  2  3  7  5  6  s3nor
x1  7        4  5  6  sinv
.ends  s3or
**********************************************************
**********************************************************
* subcircuit sbfl 4-input and
*          ina inb inc ind output power ground
.subckt ss4and  1  2  3  4   5    6    7
*  ina inb inc ind out pwr gnd subname
x0 1            9  6  7  sinv
x1 2            10  6  7  sinv
x2 3            11  6  7  sinv
x3 4            12  6  7  sinv
x4 9  10 11  12  5  6  7  s4nor
.ends ss4and
**********************************************************
**********************************************************
* subcircuit sbfl 4-input nor
*          ina inb inc ind output power ground
.subckt s4nor  1  2  3  4   5    6    7
*  d g s
j0  8 1 7 0 jfet04 l=1.2 w=48.0
j1  8 2 7 0 jfet04 l=1.2 w=48.0
j2  8 3 7 0 jfet04 l=1.2 w=48.0
j3  8 4 7 0 jfet04 l=1.2 w=48.0
j4  6 8 8 0 jfet16 l=1.2 w=3.0
j5  6 8 5 0 jfet04 l=1.2 w=48.0
j6  5 1 7 0 jfet04 l=1.2 w=48.0
j7  5 2 7 0 jfet04 l=1.2 w=48.0
j8  5 3 7 0 jfet04 l=1.2 w=48.0
j9  5 4 7 0 jfet04 l=1.2 w=48.0
.ends s4nor
**********************************************************
**********************************************************
* subcircuit sbfl 3-input nor
*          ina   inb   inc  output power ground
```

```
.subckt s3nor  1    2    3    4    5    6
* d g s
j0 8 1 6 0 jfet04 l=1.2 w=48.0
j1 8 2 6 0 jfet04 l=1.2 w=48.0
j2 8 3 6 0 jfet04 l=1.2 w=48.0
j3 5 8 8 0 jfet16 l=1.2 w=3.0
j4 5 8 4 0 jfet04 l=1.2 w=48.0
j5 4 1 6 0 jfet04 l=1.2 w=48.0
j6 4 2 6 0 jfet04 l=1.2 w=48.0
j7 4 3 6 0 jfet04 l=1.2 w=48.0
.ends s3nor
*********************************************************
*********************************************************
* subcircuit sbfl inverter
*          input, output, power, ground
.subckt sinv   1    2    3    4
* d g s
j0 9 1 4 0 jfet04 l=1.2 w=48.0
j1 3 9 9 0 jfet16 l=1.2 w=3.0
j2 3 9 2 0 jfet04 l=1.2 w=48.0
j3 2 1 4 0 jfet04 l=1.2 w=48.0
.ends sinv
*********************************************************
*********************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
*********************************************************
*********************************************************
* hspice sbfl standard load subcircuit
*          input, output, power, ground
.subckt s4load  1    2    3    4
x0 1 5 3 4 sinv
x1 1 2 3 4 sinv
x2 1 6 3 4 sinv
x3 1 7 3 4 sinv
.ends  s4load
*********************************************************
*********************************************************
* subcircuit non-latched sbfl/dcfl combination decoder
****          a0 a1 a2 w  r  re o0 o1 o2 o3 o4 o5 o6 o7 enbl pwr grnd
.subckt decoder 1  2  3  4  5  6  7  8  9  10 11 12 13 14  15   16  17
*   ina inb inc ind      output  power ground subname
x1   1                  20     16   17  dinv
x2   2                  18     16   17  dinv
x3   3                  19     16   17  dinv
x4    4  5  6           15     16   17  s3or
```

```
x5    20  18  19  15     7     16   17  ss4and
x6    1   18  19  15     8     16   17  ss4and
x7    20  2   19  15     9     16   17  ss4and
x8    1   2   19  15     10    16   17  ss4and
x9    20  18  3   15     11    16   17  ss4and
x10   1   18  3   15     12    16   17  ss4and
x11   20  2   3   15     13    16   17  ss4and
x12   1   2   3   15     14    16   17  ss4and
.ends decoder
*********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*********************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next three lines used to provide test signal inputs for transient analysis
va  100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vb  101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
vc  102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)
vr  103 0 0.63v
vw  104 0 0.63v
vre 105 0 0.63v

* main circuit
*   a0 a1 a2 w  r re  o0 o1 o2 o3 o4 o5 o6 o7 enbl pwr grnd
x0 100 101 102 104 103 105 110 111 112 113 114 115 116 117 120  1   0 decoder
x1 110                                    210  888  0 s4load
x2 111                                    211  888  0 s4load
x3 112                                    212  888  0 s4load
x4 113                                    213  888  0 s4load
x5 114                                    214  888  0 s4load
x6 115                                    215  888  0 s4load
x7 116                                    216  888  0 s4load
x8 117                                    217  888  0 s4load

* measurement parameters

* next two lines are used for dc transfer analysis
*.dc vin 0.00  0.63 0.001
*.probe dc out/in=v(104,0)

* next two lines are used for transient analysis
```

```
.probe ina=v(100) inb=v(101) inc=v(102) r=v(103) w=v(104) re=v(105)
+ o0=v(110) o1=v(111) o2=v(112) o3=v(113) o4=v(114) o5=v(115) o6=v(116)
+ o7=v(117) enbl=v(120)
.probe tran p(vds) p(vload) power
.measure tran avgpwr avg p(vds)

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(100) from=2ns to=50ns
.meas tran vmin min v(100) from=2ns to=50ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=35ns
+ rise=1 targ v(110) val='(vmax-vmin)*.5' td=35ns fall=1
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=32ns
+ fall=1 targ v(110) val='(vmax-vmin)*.5' td=32ns rise=1
.meas tran trise trig v(110) val='vmin+0.1*vmax' td=32ns
+ rise=1 targ v(110) val='0.9*vmax' rise=1
.meas tran tfall trig v(110) val='0.9*vmax' td=32ns
+ fall=1 targ v(110) val='vmin+0.1*vmax' td=32ns fall=1
.meas tran tdelay trig v(100) val=.2835 td=32ns fall=1
+       targ v(110) val=.2835 td=32ns rise=1
.tran 500ps 50ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit decoder: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname             definition  multiplier
   0 main circuit
   1 x0.                    decoder     1.00
   2 x1.                    s4load      1.00
   3 x2.                    s4load      1.00
   4 x3.                    s4load      1.00
   5 x4.                    s4load      1.00
   6 x5.                    s4load      1.00
   7 x6.                    s4load      1.00
   8 x7.                    s4load      1.00
   9 x8.                    s4load      1.00
  10 x0.x1.                   dinv       1.00
  11 x0.x2.                   dinv       1.00
  12 x0.x3.                   dinv       1.00
  13 x0.x4.                   s3or       1.00
  14 x0.x5.                   ss4and      1.00
  15 x0.x6.                   ss4and      1.00
  16 x0.x7.                   ss4and      1.00
  17 x0.x8.                   ss4and      1.00
  18 x0.x9.                   ss4and      1.00
  19 x0.x10.                   ss4and      1.00
  20 x0.x11.                   ss4and      1.00
  21 x0.x12.                   ss4and      1.00
  22 x1.x0.                   sinv       1.00
  23 x1.x1.                   sinv       1.00
```

24 x1.x2.	sinv	1.00
25 x1.x3.	sinv	1.00
26 x2.x0.	sinv	1.00
27 x2.x1.	sinv	1.00
28 x2.x2.	sinv	1.00
29 x2.x3.	sinv	1.00
30 x3.x0.	sinv	1.00
31 x3.x1.	sinv	1.00
32 x3.x2.	sinv	1.00
33 x3.x3.	sinv	1.00
34 x4.x0.	sinv	1.00
35 x4.x1.	sinv	1.00
36 x4.x2.	sinv	1.00
37 x4.x3.	sinv	1.00
38 x5.x0.	sinv	1.00
39 x5.x1.	sinv	1.00
40 x5.x2.	sinv	1.00
41 x5.x3.	sinv	1.00
42 x6.x0.	sinv	1.00
43 x6.x1.	sinv	1.00
44 x6.x2.	sinv	1.00
45 x6.x3.	sinv	1.00
46 x7.x0.	sinv	1.00
47 x7.x1.	sinv	1.00
48 x7.x2.	sinv	1.00
49 x7.x3.	sinv	1.00
50 x8.x0.	sinv	1.00
51 x8.x1.	sinv	1.00
52 x8.x2.	sinv	1.00
53 x8.x3.	sinv	1.00
54 x0.x4.x0.	s3nor	1.00
55 x0.x4.x1.	sinv	1.00
56 x0.x5.x0.	sinv	1.00
57 x0.x5.x1.	sinv	1.00
58 x0.x5.x2.	sinv	1.00
59 x0.x5.x3.	sinv	1.00
60 x0.x5.x4.	s4nor	1.00
61 x0.x6.x0.	sinv	1.00
62 x0.x6.x1.	sinv	1.00
63 x0.x6.x2.	sinv	1.00
64 x0.x6.x3.	sinv	1.00
65 x0.x6.x4.	s4nor	1.00
66 x0.x7.x0.	sinv	1.00
67 x0.x7.x1.	sinv	1.00
68 x0.x7.x2.	sinv	1.00
69 x0.x7.x3.	sinv	1.00
70 x0.x7.x4.	s4nor	1.00
71 x0.x8.x0.	sinv	1.00
72 x0.x8.x1.	sinv	1.00
73 x0.x8.x2.	sinv	1.00
74 x0.x8.x3.	sinv	1.00

```
 75 x0.x8.x4.              s4nor     1.00
 76 x0.x9.x0.              sinv      1.00
 77 x0.x9.x1.              sinv      1.00
 78 x0.x9.x2.              sinv      1.00
 79 x0.x9.x3.              sinv      1.00
 80 x0.x9.x4.              s4nor     1.00
 81 x0.x10.x0.             sinv      1.00
 82 x0.x10.x1.             sinv      1.00
 83 x0.x10.x2.             sinv      1.00
 84 x0.x10.x3.             sinv      1.00
 85 x0.x10.x4.             s4nor     1.00
 86 x0.x11.x0.             sinv      1.00
 87 x0.x11.x1.             sinv      1.00
 88 x0.x11.x2.             sinv      1.00
 89 x0.x11.x3.             sinv      1.00
 90 x0.x11.x4.             s4nor     1.00
 91 x0.x12.x0.             sinv      1.00
 92 x0.x12.x1.             sinv      1.00
 93 x0.x12.x2.             sinv      1.00
 94 x0.x12.x3.             sinv      1.00
 95 x0.x12.x4.             s4nor     1.00
 Opening plot unit= 15
file=decoder1.pa0

** hspice file created for circuit decoder: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage     node   =voltage     node   =voltage


+ 0:1     =  2.0000  0:100   =  63.0000m 0:101   =  63.0000m
+ 0:102   =  63.0000m 0:103   =  630.0000m 0:104   =  630.0000m
+ 0:105   =  630.0000m 0:110   =  643.3119m 0:111   =  31.9148m
+ 0:112   =  31.9148m 0:113   =  30.9112m 0:114   =  31.9148m
+ 0:115   =  30.9112m 0:116   =  30.9112m 0:117   =  30.5639m
+ 0:120   =  620.7250m 0:210   =  13.6773m 0:211   =  1.7422
+ 0:212   =  1.7422  0:213   =  1.7430  0:214   =  1.7422
+ 0:215   =  1.7430  0:216   =  1.7430  0:217   =  1.7433
+ 0:888   =  2.0000  1:18    =  606.6802m 1:19    =  606.6802m
+ 1:20    =  606.6802m 2:5     =  13.6773m 2:6     =  13.6773m
+ 2:7     =  13.6773m 3:5     =  1.7422  3:6     =  1.7422
+ 3:7     =  1.7422  4:5     =  1.7422  4:6     =  1.7422
+ 4:7     =  1.7422  5:5     =  1.7430  5:6     =  1.7430
+ 5:7     =  1.7430  6:5     =  1.7422  6:6     =  1.7422
+ 6:7     =  1.7422  7:5     =  1.7430  7:6     =  1.7430
+ 7:7     =  1.7430  8:5     =  1.7430  8:6     =  1.7430
+ 8:7     =  1.7430  9:5     =  1.7433  9:6     =  1.7433
+ 9:7     =  1.7433  13:7    =  10.0800m 14:9    =  6.7572m
+14:10    =  6.7572m 14:11    =  6.7572m 14:12    =  8.8318m
+15:9     =  692.5577m 15:10    =  6.7572m 15:11    =  6.7572m
```

```
+15:12   =  8.8318m 16:9    =  6.7572m 16:10   = 692.5577m
+16:11   =  6.7572m 16:12   =  8.8318m 17:9    = 690.7612m
+17:10   = 690.7612m 17:11  =  6.7572m 17:12   =  8.8318m
+18:9    =  6.7572m 18:10   =  6.7572m 18:11   = 692.5577m
+18:12   =  8.8318m 19:9    = 690.7612m 19:10  =  6.7572m
+19:11   = 690.7612m 19:12  =  8.8318m 20:9    =  6.7572m
+20:10   = 690.7612m 20:11  = 690.7612m 20:12  =  8.8318m
+21:9    = 690.1019m 21:10  = 690.1019m 21:11  = 690.1019m
+21:12   =  8.8318m 22:9    = 52.4532m 23:9    = 52.4532m
+24:9    = 52.4532m 25:9    = 52.4532m 26:9    =  1.9911
+27:9    =  1.9911 28:9     =  1.9911 29:9     =  1.9911
+30:9    =  1.9911 31:9     =  1.9911 32:9     =  1.9911
+33:9    =  1.9911 34:9     =  1.9913 35:9     =  1.9913
+36:9    =  1.9913 37:9     =  1.9913 38:9     =  1.9911
+39:9    =  1.9911 40:9     =  1.9911 41:9     =  1.9911
+42:9    =  1.9913 43:9     =  1.9913 44:9     =  1.9913
+45:9    =  1.9913 46:9     =  1.9913 47:9     =  1.9913
+48:9    =  1.9913 49:9     =  1.9913 50:9     =  1.9914
+51:9    =  1.9914 52:9     =  1.9914 53:9     =  1.9914
+54:8    = 22.8197m 55:9    =  1.2859 56:9     = 58.9751m
+57:9    = 58.9751m 58:9    = 58.9751m 59:9    = 55.6117m
+60:8    =  1.3073 61:9     =  1.3552 62:9     = 58.9751m
+63:9    = 58.9751m 64:9    = 55.6117m 65:8    = 56.8042m
+66:9    = 58.9751m 67:9    =  1.3552 68:9     = 58.9751m
+69:9    = 55.6117m 70:8    = 56.8042m 71:9    =  1.3534
+72:9    =  1.3534 73:9     = 58.9751m 74:9    = 55.6117m
+75:8    = 42.5420m 76:9    = 58.9751m 77:9    = 58.9751m
+78:9    =  1.3552 79:9     = 55.6117m 80:8    = 56.8042m
+81:9    =  1.3534 82:9     = 58.9751m 83:9    =  1.3534
+84:9    = 55.6117m 85:8    = 42.5420m 86:9    = 58.9751m
+87:9    =  1.3534 88:9     =  1.3534 89:9     = 55.6117m
+90:8    = 42.5420m 91:9    =  1.3528 92:9     =  1.3528
+93:9    =  1.3528 94:9     = 55.6117m 95:8    = 38.1558m


 Opening plot unit= 16
file=decoder1.tr0

** hspice file created for circuit decoder: transient&power @ 25.0c
****** transient analysis          tnom= 25.000 temp= 25.000
******
 avgpwr       = -1.2518E-01 from= 0.0000E+00   to= 5.0000E-08
 vmax          = 6.3000E-01   at= 4.3000E-09
         from= 2.0000E-09   to= 5.0000E-08
 vmin          = 6.3000E-02   at= 2.0000E-09
         from= 2.0000E-09   to= 5.0000E-08
 tphl         = 3.2624E-10 targ= 3.8165E-08  trig= 3.7839E-08
 tplh         = 5.5513E-10 targ= 3.4116E-08  trig= 3.3561E-08
 trise        = 2.8580E-10 targ= 3.4318E-08  trig= 3.4032E-08
 tfall        = 2.0350E-10 targ= 3.8268E-08  trig= 3.8064E-08
```

```
tdelay      = 5.5513E-10 targ= 3.4116E-08  trig= 3.3561E-08

     ***** job concluded
     total cpu time      306.61 seconds
        job started at  20: 9:10  2-feb93
        job ended   at  20:25:19  2-feb93


I am done with decoder1.sp
Tue Feb  2 20:25:20 PST 1993
```

L. Listing File for COUNTER Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        11:42: 2  3-feb93  sun
** hspice file created for circuit counter: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* hspice dcfl 2-input nor subcircuit
*            ina, inb, output, power, ground
.subckt d2nor     1   2    3      4     5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 5 5 jfet04 l=1.2 w=96.0
j2 3 2 5 5 jfet04 l=1.2 w=96.0
.ends   d2nor
************************************************************
************************************************************
* hspice dcfl 2-input demorgan and subcircuit
*            ina, inb, output, power, ground
.subckt dd2and   1   2    3      4     5
x0 1     10 4 5 dinv
x1 2     11 4 5 dinv
x2 10 11  3 4 5 d2nor
.ends   dd2and
******************************************************
******************************************************
* subcircuit dcfl 2-input or
*           ina   inb  output power ground
.subckt dd2or   1     2    3     4    5
```

```
*  ina inb out pwr gnd subname
x0  1  2  6  4  5  d2nor
x1  6     3  4  5  dinv
.ends  dd2or
*************************************************************
*************************************************************
* hspice dcfl 3-input nor subcircuit
*            ina, inb, inc,  output, power, ground
.subckt d3nor     1  2  3     4     5     6
* d g s b
j0 5 4 4 6 jfet16 l=1.2 w=6.0
j1 4 1 6 6 jfet04 l=1.2 w=96.0
j2 4 2 6 6 jfet04 l=1.2 w=96.0
j3 4 3 6 6 jfet04 l=1.2 w=96.0
.ends  d3nor
*************************************************************
* hspice dcfl 3-input demorgan and subcircuit
*            ina, inb, inc,  output, power, ground
.subckt dd3and   1  2  3     4     5     6
x0 1       10 5 6 dinv
x1 2       11 5 6 dinv
x2 3       12 5 6 dinv
x3 10 11 12  4 5 6 d3nor
.ends  dd3and
*************************************************************
*************************************************************
* subcircuit dcfl 3-input or
*          ina   inb   inc  output power ground
.subckt dd3or   1     2     3    4     5     6
*  ina inb inc out pwr gnd subname
x0  1  2  3  7  5  6  d3nor
x1  7        4  5  6  dinv
.ends  dd3or

*************************************************************
*************************************************************
* hspice dcfl 4-input nor subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt d4nor     1  2  3  4     5     6    7
* d g s b
j0 6 5 5 7 jfet16 l=1.2 w=6.0
j1 5 1 7 7 jfet04 l=1.2 w=96.0
j2 5 2 7 7 jfet04 l=1.2 w=96.0
j3 5 3 7 7 jfet04 l=1.2 w=96.0
j4 5 4 7 7 jfet04 l=1.2 w=96.0
.ends  d4nor
*************************************************************
*************************************************************
* subcircuit dcfl 4-input or
*          ina inb inc ind output power ground
.subckt dd4or  1  2  3  4  5     6    7
```

```
*  ina inb inc ind out pwr gnd subname
x0  1  2  3  4  8  6  7  d4nor
x1  8          5  6  7  dinv
.ends  dd4or
*************************************************************
*************************************************************
* hspice dcfl 4-input demorgan  and subcircuit
*           ina, inb, inc, ind, output, power, ground
.subckt dd4and  1   2   3   4    5     6    7
x0 1          10 6 7 dinv
x1 2          11 6 7 dinv
x2 3          12 6 7 dinv
x3 4          13 6 7 dinv
x4 10 11 12 13  5  6 7 d4nor
.ends  dd4and
*************************************************************
*************************************************************
* subcircuit hspice dcfl clear d flip flop
* wakerly pg 363 - 31july 1992
***         d clk clr  q  /q  power  ground
.subckt cpdff  1  2  3 4 5    6     7
x0    12  10        9  6  7  dd2nand
x1  9  3  2         10  6  7  dd3nand
x2  10  2  12        11  6  7  dd3nand
x3  11  3  1         12  6  7  dd3nand
x4    10  5         4  6  7  dd2nand
x5  4  3  11         5  6  7  dd3nand
.ends  cpdff
*************************************************************
*************************************************************
* hspice dcfl 2-input demorgan nand subcircuit
*           ina, inb, output, power, ground
.subckt dd2nand   1   2    3     4     5
x0 1     10 4 5 dinv
x1 2     11 4 5 dinv
x2 10 11 12 4 5 d2nor
x3 12    3  4 5 dinv
.ends  dd2nand
*************************************************************
*************************************************************
* hspice dcfl 3-input demorgan nand subcircuit
*           ina, inb, inc,  output, power, ground
.subckt dd3nand  1  2   3     4     5     6
x0 1        10 5 6 dinv
x1 2        11 5 6 dinv
x2 3        12 5 6 dinv
x3 10 11 12 13 5 6 d3nor
x4 13       4  5 6 dinv
.ends  dd3nand
*************************************************************
*************************************************************
```

```
* subcircuit sbfl inverter
*          input, output, power, ground
.subckt sinv   1    2    3    4
* d g s
j0 9 1 4 0 jfet04 l=1.2 w=48.0
j1 3 9 9 0 jfet16 l=1.2 w=3.0
j2 3 9 2 0 jfet04 l=1.2 w=48.0
j3 2 1 4 0 jfet04 l=1.2 w=48.0
.ends sinv
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
************************************************************
************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1    2    3    4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
************************************************************
************************************************************
* hspice sbfl standard load subcircuit
*          input, output, power, ground
.subckt s4load  1    2    3    4
x0 1 5 3 4 sinv
x1 1 2 3 4 sinv
x2 1 6 3 4 sinv
x3 1 7 3 4 sinv
.ends  s4load
************************************************************
************************************************************
* subcircuit dcfl counter using clear/preset d fps - cpdff
***          enble clk q0 q1 q2 /q0 /q1 /q2 power ground
.subckt counter  1   2  3 4 5 6  7  8   9    10
*** ina inb inc ind d clk q  /q out power ground subname
x0  1                    11  9   10    dinv
x1  3   11               12  9   10    dd2and
x2  1   6                13  9   10    dd2and
x3  12  13               20  9   10    dd2or
x4  4   11               14  9   10    dd2and
x5  4   6                15  9   10    dd2and
x6  3   7   1            16  9   10    dd3and
x7  14  15  16             21  9   10    dd3or
x8  5   7                17  9   10    dd2and
```

```
x9  5  6              18  9   10   dd2and
x10 1  3  4  8          19  9   10   dd4and
x11 11 5              23  9   10   dd2and
x12 17 18 19 23         22  9   10   dd4or
x13 20 2  1        3 6    9   10   cpdff
x14 21 2  1        4 7    9   10   cpdff
x15 22 2  1        5 8    9   10   cpdff
.ends  counter
*********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*********************************************************
* power supplies
vds   1 0 dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs
* next line is for dc transfer analysis
*vin 999 0

* next three lines used to provide test signal inputs for transient analysis
vclk   100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
venble 101 0 pulse(0.063 0.63 10000ps 100ps 100ps 88400ps 98200ps)

* main circuit
* enble clk  q0  q1  q2 /q0 /q1 /q2 power ground subname
x0 101  100 110 111 112 120 121 122  1     0   counter
x1 110                  210  888   0   d2load
x2 111                  211  888   0   d2load
x3 112                  212  888   0   d2load
x4 120                  220  888   0   d2load
x5 121                  221  888   0   d2load
x6 122                  222  888   0   d2load

* measurement parameters


* next two lines are used for transient analysis
.probe clk=v(100) enble=v(101) q0=v(110) q1=v(111) q2=v(112)
+                       /q0=v(120) /q1=v(121) /q2=v(122)
.probe tran p(vds) p(vload) power
.measure tran avgpwr avg p(vds) from 0.0ns to 88ns

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(110) from=2ns to=88ns
.meas tran vmin min v(110) from=2ns to=88ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=20ns
+ rise=1 targ v(110) val='(vmax-vmin)*.5' td=20ns fall=1
```

```
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=10ns
+ rise=1 targ v(110) val='(vmax-vmin)*.5' td=10ns rise=1
.meas tran trise trig v(110) val='vmin+0.1*vmax' td=10ns
+ rise=1 targ v(110) val='0.9*vmax' rise=1
.meas tran tfall trig v(110) val='0.9*vmax' td=20ns
+ fall=1 targ v(110) val='vmin+0.1*vmax' td=20ns fall=1
.meas tran tdelay trig v(100) val=.2835 td=20ns rise=1
+       targ v(110) val=.2835 td=20ns fall=1
.tran 2500ps 88ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit counter: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                  counter     1.00
   2 x1.                  d2load      1.00
   3 x2.                  d2load      1.00
   4 x3.                  d2load      1.00
   5 x4.                  d2load      1.00
   6 x5.                  d2load      1.00
   7 x6.                  d2load      1.00
   8 x0.x0.                dinv       1.00
   9 x0.x1.                dd2and      1.00
  10 x0.x2.                 dd2and      1.00
  11 x0.x3.                 dd2or      1.00
  12 x0.x4.                 dd2and      1.00
  13 x0.x5.                 dd2and      1.00
  14 x0.x6.                 dd3and      1.00
  15 x0.x7.                 dd3or      1.00
  16 x0.x8.                 dd2and      1.00
  17 x0.x9.                 dd2and      1.00
  18 x0.x10.                 dd4and      1.00
  19 x0.x11.                 dd2and      1.00
  20 x0.x12.                 dd4or      1.00
  21 x0.x13.                 cpdff      1.00
  22 x0.x14.                 cpdff      1.00
  23 x0.x15.                 cpdff      1.00
  24 x1.x0.                 dinv       1.00
  25 x1.x1.                 dinv       1.00
  26 x2.x0.                 dinv       1.00
  27 x2.x1.                 dinv       1.00
  28 x3.x0.                 dinv       1.00
  29 x3.x1.                 dinv       1.00
  30 x4.x0.                 dinv       1.00
  31 x4.x1.                 dinv       1.00
  32 x5.x0.                 dinv       1.00
  33 x5.x1.                 dinv       1.00
  34 x6.x0.                 dinv       1.00
```

35 x6.x1.	dinv	1.00
36 x0.x1.x0.	dinv	1.00
37 x0.x1.x1.	dinv	1.00
38 x0.x1.x2.	d2nor	1.00
39 x0.x2.x0.	dinv	1.00
40 x0.x2.x1.	dinv	1.00
41 x0.x2.x2.	d2nor	1.00
42 x0.x3.x0.	d2nor	1.00
43 x0.x3.x1.	dinv	1.00
44 x0.x4.x0.	dinv	1.00
45 x0.x4.x1.	dinv	1.00
46 x0.x4.x2.	d2nor	1.00
47 x0.x5.x0.	dinv	1.00
48 x0.x5.x1.	dinv	1.00
49 x0.x5.x2.	d2nor	1.00
50 x0.x6.x0.	dinv	1.00
51 x0.x6.x1.	dinv	1.00
52 x0.x6.x2.	dinv	1.00
53 x0.x6.x3.	d3nor	1.00
54 x0.x7.x0.	d3nor	1.00
55 x0.x7.x1.	dinv	1.00
56 x0.x8.x0.	dinv	1.00
57 x0.x8.x1.	dinv	1.00
58 x0.x8.x2.	d2nor	1.00
59 x0.x9.x0.	dinv	1.00
60 x0.x9.x1.	dinv	1.00
61 x0.x9.x2.	d2nor	1.00
62 x0.x10.x0.	dinv	1.00
63 x0.x10.x1.	dinv	1.00
64 x0.x10.x2.	dinv	1.00
65 x0.x10.x3.	dinv	1.00
66 x0.x10.x4.	d4nor	1.00
67 x0.x11.x0.	dinv	1.00
68 x0.x11.x1.	dinv	1.00
69 x0.x11.x2.	d2nor	1.00
70 x0.x12.x0.	d4nor	1.00
71 x0.x12.x1.	dinv	1.00
72 x0.x13.x0.	dd2nand	1.00
73 x0.x13.x1.	dd3nand	1.00
74 x0.x13.x2.	dd3nand	1.00
75 x0.x13.x3.	dd3nand	1.00
76 x0.x13.x4.	dd2nand	1.00
77 x0.x13.x5.	dd3nand	1.00
78 x0.x14.x0.	dd2nand	1.00
79 x0.x14.x1.	dd3nand	1.00
80 x0.x14.x2.	dd3nand	1.00
81 x0.x14.x3.	dd3nand	1.00
82 x0.x14.x4.	dd2nand	1.00
83 x0.x14.x5.	dd3nand	1.00
84 x0.x15.x0.	dd2nand	1.00
85 x0.x15.x1.	dd3nand	1.00

86 x0.x15.x2.	dd3nand	1.00
87 x0.x15.x3.	dd3nand	1.00
88 x0.x15.x4.	dd2nand	1.00
89 x0.x15.x5.	dd3nand	1.00
90 x0.x13.x0.x0.	dinv	1.00
91 x0.x13.x0.x1.	dinv	1.00
92 x0.x13.x0.x2.	d2nor	1.00
93 x0.x13.x0.x3.	dinv	1.00
94 x0.x13.x1.x0.	dinv	1.00
95 x0.x13.x1.x1.	dinv	1.00
96 x0.x13.x1.x2.	dinv	1.00
97 x0.x13.x1.x3.	d3nor	1.00
98 x0.x13.x1.x4.	dinv	1.00
99 x0.x13.x2.x0.	dinv	1.00
100 x0.x13.x2.x1.	dinv	1.00
101 x0.x13.x2.x2.	dinv	1.00
102 x0.x13.x2.x3.	d3nor	1.00
103 x0.x13.x2.x4.	dinv	1.00
104 x0.x13.x3.x0.	dinv	1.00
105 x0.x13.x3.x1.	dinv	1.00
106 x0.x13.x3.x2.	dinv	1.00
107 x0.x13.x3.x3.	d3nor	1.00
108 x0.x13.x3.x4.	dinv	1.00
109 x0.x13.x4.x0.	dinv	1.00
110 x0.x13.x4.x1.	dinv	1.00
111 x0.x13.x4.x2.	d2nor	1.00
112 x0.x13.x4.x3.	dinv	1.00
113 x0.x13.x5.x0.	dinv	1.00
114 x0.x13.x5.x1.	dinv	1.00
115 x0.x13.x5.x2.	dinv	1.00
116 x0.x13.x5.x3.	d3nor	1.00
117 x0.x13.x5.x4.	dinv	1.00
118 x0.x14.x0.x0.	dinv	1.00
119 x0.x14.x0.x1.	dinv	1.00
120 x0.x14.x0.x2.	d2nor	1.00
121 x0.x14.x0.x3.	dinv	1.00
122 x0.x14.x1.x0.	dinv	1.00
123 x0.x14.x1.x1.	dinv	1.00
124 x0.x14.x1.x2.	dinv	1.00
125 x0.x14.x1.x3.	d3nor	1.00
126 x0.x14.x1.x4.	dinv	1.00
127 x0.x14.x2.x0.	dinv	1.00
128 x0.x14.x2.x1.	dinv	1.00
129 x0.x14.x2.x2.	dinv	1.00
130 x0.x14.x2.x3.	d3nor	1.00
131 x0.x14.x2.x4.	dinv	1.00
132 x0.x14.x3.x0.	dinv	1.00
133 x0.x14.x3.x1.	dinv	1.00
134 x0.x14.x3.x2.	dinv	1.00
135 x0.x14.x3.x3.	d3nor	1.00
136 x0.x14.x3.x4.	dinv	1.00

```
 137 x0.x14.x4.x0.          dinv      1.00
 138 x0.x14.x4.x1.          dinv      1.00
 139 x0.x14.x4.x2.          d2nor     1.00
 140 x0.x14.x4.x3.          dinv      1.00
 141 x0.x14.x5.x0.          dinv      1.00
 142 x0.x14.x5.x1.          dinv      1.00
 143 x0.x14.x5.x2.          dinv      1.00
 144 x0.x14.x5.x3.          d3nor     1.00
 145 x0.x14.x5.x4.          dinv      1.00
 146 x0.x15.x0.x0.          dinv      1.00
 147 x0.x15.x0.x1.          dinv      1.00
 148 x0.x15.x0.x2.          d2nor     1.00
 149 x0.x15.x0.x3.          dinv      1.00
 150 x0.x15.x1.x0.          dinv      1.00
 151 x0.x15.x1.x1.          dinv      1.00
 152 x0.x15.x1.x2.          dinv      1.00
 153 x0.x15.x1.x3.          d3nor     1.00
 154 x0.x15.x1.x4.          dinv      1.00
 155 x0.x15.x2.x0.          dinv      1.00
 156 x0.x15.x2.x1.          dinv      1.00
 157 x0.x15.x2.x2.          dinv      1.00
 158 x0.x15.x2.x3.          d3nor     1.00
 159 x0.x15.x2.x4.          dinv      1.00
 160 x0.x15.x3 x0.          dinv      1.00
 161 x0.x15.x3.x1.          dinv      1.00
 162 x0.x15.x3.x2.          dinv      1.00
 163 x0.x15.x3.x3.          d3nor     1.00
 164 x0.x15.x3.x4.          dinv      1.00
 165 x0.x15.x4.x0.          dinv      1.00
 166 x0.x15.x4.x1.          dinv      1.00
 167 x0.x15.x4.x2.          d2nor     1.00
 168 x0.x15.x4.x3.          dinv      1.00
 169 x0.x15.x5.x0.          dinv      1.00
 170 x0.x15.x5.x1.          dinv      1.00
 171 x0.x15.x5.x2.          dinv      1.00
 172 x0.x15.x5.x3.          d3nor     1.00
 173 x0.x15.x5.x4.          dinv      1.00
 Opening plot unit= 15
file=counter1.pa0

** hspice file created for circuit counter: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is     0.
    node   =voltage       node   =voltage       node   =voltage


+ 0:1     =  2.0000   0:100   =  63.0000m  0:101   =  63.0000m
+ 0:110   =  52.0499m  0:111   =  52.0501m  0:112   =  52.0502m
+ 0:120   = 602.9491m  0:121   = 608.4583m  0:122   = 615.2330m
+ 0:210   =  1.9872   0:211   =  1.9872   0:212   =  1.9872
```

```
+ 0:220   = 60.0405m  0:221   = 58.4926m  0:222   = 56.8042m
+ 0:888   = 2.0000   1:11    = 623.9374m  1:12    = 52.0087m
+ 1:13    = 52.0005m  1:14    = 52.0087m  1:15    = 52.0017m
+ 1:16    = 32.4223m  1:17    = 52.0039m  1:18    = 52.0017m
+ 1:19    = 26.2272m  1:20    = 52.0509m  1:21    = 52.0488m
+ 1:22    = 52.0458m  1:23    = 52.0087m  2:5     = 1.9872
+ 3:5     = 1.9872   4:5     = 1.9872   5:5     = 60.0405m
+ 6:5     = 58.4926m  7:5     = 56.8042m  9:10    = 658.6792m
+ 9:11    = 54.9887m  10:10   = 658.6298m  10:11   = 60.0405m
+ 11:6    = 658.5363m  12:10   = 658.6792m  12:11   = 54.9887m
+ 13:10   = 658.6777m  13:11   = 60.0405m  14:10   = 653.5418m
+ 14:11   = 58.4926m  14:12   = 653.4950m  15:7    = 658.4424m
+ 16:10   = 658.6782m  16:11   = 58.4926m  17:10   = 658.6777m
+ 17:11   = 60.0405m  18:10   = 651.4782m  18:11   = 651.5247m
+ 18:12   = 651.5247m  18:13   = 56.8042m  19:10   = 54.9887m
+ 19:11   = 658.6792m  20:8    = 658.3021m  21:9    = 52.0506m
+ 21:10   = 624.0441m  21:11   = 636.5449m  21:12   = 636.5992m
+ 22:9    = 52.0506m  22:10   = 624.0441m  22:11   = 636.5449m
+ 22:12   = 636.5992m  23:9    = 52.0506m  23:10   = 624.0441m
+ 23:11   = 636.5449m  23:12   = 636.5992m  72:10   = 53.0867m
+ 72:11   = 54.9689m  72:12   = 658.5204m  73:10   = 651.5268m
+ 73:11   = 651.4803m  73:12   = 651.4803m  73:13   = 26.2332m
+ 74:10   = 54.9689m  74:11   = 658.6219m  74:12   = 53.0867m
+ 74:13   = 51.9641m  75:10   = 53.0929m  75:11   = 653.4958m
+ 75:12   = 653.5426m  75:13   = 32.4248m  76:10   = 54.9689m
+ 76:11   = 60.0405m  76:12   = 658.4906m  77:10   = 653.5426m
+ 77:11   = 653.4958m  77:12   = 53.0929m  77:13   = 32.4248m
+ 78:10   = 53.0867m  78:11   = 54.9689m  78:12   = 658.5204m
+ 79:10   = 651.5268m  79:11   = 651.4803m  79:12   = 651.4803m
+ 79:13   = 26.2332m  80:10   = 54.9689m  80:11   = 658.6219m
+ 80:12   = 53.0867m  80:13   = 51.9641m  81:10   = 53.0929m
+ 81:11   = 653.4958m  81:12   = 653.5426m  81:13   = 32.4248m
+ 82:10   = 54.9689m  82:11   = 58.4926m  82:12   = 658.4976m
+ 83:10   = 653.5426m  83:11   = 653.4958m  83:12   = 53.0929m
+ 83:13   = 32.4248m  84:10   = 53.0867m  84:11   = 54.9689m
+ 84:12   = 658.5204m  85:10   = 651.5268m  85:11   = 651.4803m
+ 85:12   = 651.4803m  85:13   = 26.2332m  86:10   = 54.9689m
+ 86:11   = 658.6219m  86:12   = 53.0867m  86:13   = 51.9641m
+ 87:10   = 53.0929m  87:11   = 653.4958m  87:12   = 653.5426m
+ 87:13   = 32.4248m  88:10   = 54.9689m  88:11   = 56.8042m
+ 88:12   = 658.5051m  89:10   = 653.5426m  89:11   = 653.4958m
+ 89:12   = 53.0929m  89:13   = 32.4248m


 Opening plot unit= 16
file=counter1.tr0

** hspice file created for circuit counter: transient&power @ 25.0c
****** transient analysis            tnom= 25.000 temp= 25.000
******
```

```
avgpwr       = -2.7612E-01 from= 0.0000E+00   to= 8.8000E-08
vmax         = 6.0395E-01  at= 7.2275E-08
       from= 2.0000E-09  to= 8.8000E-08
vmin         = 4.7781E-02  at= 3.9181E-08
       from= 2.0000E-09  to= 8.8000E-08
tphl         = 1.1171E-09 targ= 2.2155E-08  trig= 2.1038E-08
tplh         = 5.0023E-10 targ= 1.3138E-08  trig= 1.2638E-08
trise        = 6.5525E-10 targ= 1.3671E-08  trig= 1.3016E-08
tfall        = 2.5412E-10 targ= 2.2265E-08  trig= 2.2011E-08
tdelay       = 1.1138E-09 targ= 2.2153E-08  trig= 2.1039E-08

     ***** job concluded
     total cpu time      569.23 seconds
        job started at  11:42: 2  3-feb93
        job ended   at  12:11:26  3-feb93


I am done with counter1.sp
Wed Feb  3 12:11:27 PST 1993
```

M. Listing File for DREFRESH Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
 reading design configuration file: drefresh1.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        20:28:46  3-feb93  sun
** hspice file created for circuit drefresh: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2     3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends   d2load
************************************************************
************************************************************
* subcircuit sbfl 2-input nor
*          ina   inb  output power ground
.subckt s2nor  1     2     3     4     5
* d g s
```

```
j0 8 1 5 0 jfet04 l=1.2 w=48.0
j1 8 2 5 0 jfet04 l=1.2 w=48.0
j2 4 8 8 0 jfet16 l=1.2 w=3.0
j3 4 8 3 0 jfet04 l=1.2 w=48.0
j4 3 2 5 0 jfet04 l=1.2 w=48.0
j5 3 1 5 0 jfet04 l=1.2 w=48.0
.ends s2nor
*********************************************************
*********************************************************
* subcircuit sbfl 2-input nand
*            ina   inb  output power ground
.subckt ss2nand  1    2    3    4    5
*  ina inb out pwr gnd subname
x0 1      9  4  5  sinv
x1 2      6  4  5  sinv
x2 9   6  7  4  5  s2nor
x3 7      3  4  5  sinv
.ends ss2nand
*********************************************************
*********************************************************
* subcircuit dcfl sd-latch using generic gates
*           d  clk q  /q power ground
.subckt sdlatch  1   2 3 4   5    6
** sbfl d latch **
*   ina  inb output  power ground subname
x0   1   2   8     5    6  d2nand
x1   1       7     5    6  dinv
x2   2   7   9     5    6  d2nand
x3   8   4   3     5    6  ss2nand
x4   9   3   4     5    6  ss2nand
.ends sdlatch
*********************************************************
*********************************************************
* subcircuit dcfl d-latch using generic gates
*           d  clk q  /q power ground
.subckt dlatch  1   2 3 4   5    6
*   ina  inb output  power ground subname
x0   1   2   8     5    6  d2nand
x1   1       7     5    6  dinv
x2   2   7   9     5    6  d2nand
x3   8   4   3     5    6  d2nand
x4   9   3   4     5    6  d2nand
.ends dlatch
*********************************************************
*********************************************************
* hspice dcfl 2-input real nand subcircuit
*            ina, inb, output, power, ground
.subckt d2nand   1   2    3     4     5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 6 5 jfet04 l=1.2 w=192.0
```

```
j2 6 2 5 5 jfet04 l=1.2 w=192.0
.ends d2nand
*********************************************************
*********************************************************
* subcircuit sbfl 4-input nor
*          ina inb inc ind output power ground
.subckt s4nor  1  2  3  4  5    6   7
*  d g s
j0  8 1 7 0 jfet04 l=1.2 w=48.0
j1  8 2 7 0 jfet04 l=1.2 w=48.0
j2  8 3 7 0 jfet04 l=1.2 w=48.0
j3  8 4 7 0 jfet04 l=1.2 w=48.0
j4  6 8 8 0 jfet16 l=1.2 w=3.0
j5  6 8 5 0 jfet04 l=1.2 w=48.0
j6  5 1 7 0 jfet04 l=1.2 w=48.0
j7  5 2 7 0 jfet04 l=1.2 w=48.0
j8  5 3 7 0 jfet04 l=1.2 w=48.0
j9  5 4 7 0 jfet04 l=1.2 w=48.0
.ends s4nor
*********************************************************
*********************************************************
* hspice dcfl 2-input nor subcircuit
*           ina, inb, output, power, ground
.subckt d2nor    1   2   3    4    5
*  d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 5 5 jfet04 l=1.2 w=96.0
j2 3 2 5 5 jfet04 l=1.2 w=96.0
.ends   d2nor
*********************************************************
*********************************************************
* hspice dcfl 2-input demorgan and subcircuit
*           ina, inb, output, power, ground
.subckt dd2and   1   2   3    4    5
x0 1    10 4 5 dinv
x1 2    11 4 5 dinv
x2 10 11  3 4 5 d2nor
.ends   dd2and
*********************************************************
*********************************************************
* subcircuit dcfl 2-input or
*          ina   inb  output power ground
.subckt dd2or   1    2   3    4   5
*  ina inb out pwr gnd subname
x0  1  2  6  4  5  d2nor
x1  6     3  4  5  dinv
.ends   dd2or
*********************************************************
*********************************************************
* hspice dcfl 3-input nor subcircuit
*           ina, inb, inc,  output, power, ground
```

```
.subckt d3nor    1  2  3    4    5    6
* d g s b
j0 5 4 4 6 jfet16 l=1.2 w=6.0
j1 4 1 6 6 jfet04 l=1.2 w=96.0
j2 4 2 6 6 jfet04 l=1.2 w=96.0
j3 4 3 6 6 jfet04 l=1.2 w=96.0
.ends  d3nor
************************************************************
* hspice dcfl 3-input demorgan and subcircuit
*           ina, inb, inc,  output, power, ground
.subckt dd3and   1  2  3    4    5    6
x0 1      10 5 6 dinv
x1 2      11 5 6 dinv
x2 3      12 5 6 dinv
x3 10 11 12  4 5 6 d3nor
.ends  dd3and
************************************************************
************************************************************
* subcircuit dcfl 3-input or
*          ina   inb   inc  output power ground
.subckt dd3or   1    2    3    4    5    6
*  ina inb inc out pwr gnd subname
x0  1  2  3  7  5  6  d3nor
x1  7        4  5  6  dinv
.ends  dd3or

************************************************************
************************************************************
* hspice dcfl 4-input nor subcircuit
*           ina, inb, inc, ind, output, power, ground
.subckt d4nor    1  2  3  4    5    6   7
* d g s b
j0 6 5 5 7 jfet16 l=1.2 w=6.0
j1 5 1 7 7 jfet04 l=1.2 w=96.0
j2 5 2 7 7 jfet04 l=1.2 w=96.0
j3 5 3 7 7 jfet04 l=1.2 w=96.0
j4 5 4 7 7 jfet04 l=1.2 w=96.0
.ends  d4nor
************************************************************
************************************************************
* subcircuit dcfl 4-input or
*          ina inb inc ind output power ground
.subckt dd4or  1  2  3  4  5    6   7
*  ina inb inc ind out pwr gnd subname
x0  1  2  3  4  8  6  7  d4nor
x1  8           5  6  7  dinv
.ends  dd4or
************************************************************
************************************************************
* hspice dcfl 4-input demorgan  and subcircuit
*           ina, inb, inc, ind, output, power, ground
```

```
.subckt dd4and  1   2   3   4    5     6   7
x0 1          10 6 7 dinv
x1 2          11 6 7 dinv
x2 3          12 6 7 dinv
x3 4          13 6 7 dinv
x4 10 11 12 13  5  6 7 d4nor
.ends  dd4and
*********************************************************
*********************************************************
* subcircuit hspice dcfl clear d flip flop
* wakerly pg 363 - 31july 1992
***          d clk clr  q  /q  power  ground
.subckt cpdff  1  2  3 4 5    6     7
x0    12  10        9   6   7   dd2nand
x1   9  3   2        10  6   7   dd3nand
x2  10  2  12         11  6   7   dd3nand
x3  11  3   1        12  6   7   dd3nand
x4    10   5        4   6   7   dd2nand
x5   4  3  11        5   6   7   dd3nand
.ends  cpdff
*********************************************************
*********************************************************
* hspice dcfl 2-input demorgan nand subcircuit
*            ina, inb, output, power, ground
.subckt dd2nand   1   2    3      4     5
x0 1     10 4 5 dinv
x1 2     11 4 5 dinv
x2 10 11 12 4 5 d2nor
x3 12    3  4 5 dinv
.ends  dd2nand
*********************************************************
*********************************************************
* hspice dcfl 3-input demorgan nand subcircuit
*            ina, inb, inc,  output, power, ground
.subckt dd3nand  1  2   3      4     5      6
x0 1       10 5 6 dinv
x1 2       11 5 6 dinv
x2 3       12 5 6 dinv
x3 10 11 12 13 5 6 d3nor
x4 13      4  5 6 dinv
.ends  dd3nand
*********************************************************
*********************************************************
* subcircuit dcfl counter using clear/preset d fps - cpdff
***          enble clk q0 q1 q2 /q0 /q1 /q2 power ground
.subckt counter  1    2  3 4 5 6  7  8   9     10
*** ina inb inc ind d clk q  /q out power ground subname
x0  1                    11  9   10    dinv
x1  3   11               12  9   10    dd2and
x2  1   6                13  9   10    dd2and
x3  12  13               20  9   10    dd2or
```

```
x4  4  11              14  9   10   dd2and
x5  4  6               15  9   10   dd2and
x6  3  7  1            16  9   10   dd3and
x7  14 15 16             21  9   10   dd3or
x8  5  7               17  9   10   dd2and
x9  5  6               18  9   10   dd2and
x10 1  3  4  8           19  9   10   dd4and
x11 11 5               23  9   10   dd2and
x12 17 18 19 23          22  9   10   dd4or
x13 20 2  1        3 6     9   10   cpdff
x14 21 2  1        4 7     9   10   cpdff
x15 22 2  1        5 8     9   10   cpdff
.ends  counter
*************************************************************
*************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt bdinv   1    2    3    4
* d g s b
j0 3 2 2 4 jfet20 l=3.0 w=40.0
j1 2 1 4 4 jfet04 l=1.2 w=240.0
.ends  bdinv
*************************************************************
* subcircuit sbfl 2-input nor
*          ina   inb  output power ground
.subckt bs2nor  1    2    3    4    5
* d g s
j0 8 1 5 0 jfet04 l=1.2 w=180.0
j1 8 2 5 0 jfet04 l=1.2 w=180.0
j2 4 8 8 0 jfet16 l=1.2 w=10.0
j3 4 8 3 0 jfet04 l=1.2 w=224.0
j4 3 2 5 0 jfet04 l=1.2 w=224.0
j5 3 1 5 0 jfet04 l=1.2 w=224.0
.ends  bs2nor
*************************************************************
* subcircuit sbfl 2- input and
*          ina   inb  output power ground
.subckt bs2and  1    2    3    4    5
*  ina inb out pwr gnd subname
x0 1      9  4  5  bdinv
x1 2      6  4  5  bdinv
x2 9   6  3  4  5  bs2nor
.ends  bs2and
*************************************************************
*************************************************************
* subckt hspice sbfl large 2-input nor
*          ina   inb  output power ground
.subckt csnor   1    2    3    4    5
* d g s b
j0 8 1 5 0 jfet04 l=1.2 w=144.0
j1 8 2 5 0 jfet04 l=1.2 w=144.0
```

```
j2 4 8 8 0 jfet16 l=1.2 w= 9.0
j3 4 8 3 0 jfet04 l=1.2 w=144.0
j4 3 2 5 0 jfet04 l=1.2 w=144.0
j5 3 1 5 0 jfet04 l=1.2 w=144.0
.ends csnor
*********************************************************
* hspice sbfl extra-large driver-inverter subcircuit
*          input, output, power, ground
.subckt ssinv   1    2    3    4
*  d g s b
j0 9 1 4 0 jfet04 l=1.2 w=768.0
j1 3 9 9 0 jfet16 l=1.2 w= 48.0
j2 3 9 2 0 jfet04 l=1.2 w=768.0
j3 2 1 4 0 jfet04 l=1.2 w=768.0
.ends ssinv
*********************************************************
* hspice sbfl large driver-inverter subcircuit
*          input, output, power, ground
.subckt csinv   1    2    3    4
*  d g s b
j0 9 1 4 0 jfet04 l=1.2 w=256.0
j1 3 9 9 0 jfet16 l=1.2 w= 16.0
j2 3 9 2 0 jfet04 l=1.2 w=384.0
j3 2 1 4 0 jfet04 l=1.2 w=384.0
.ends csinv
*********************************************************
* subcircuit sbfl 4-input nand
*           ina inb inc ind output power ground
.subckt ss4nand  1  2  3  4   5    6    7
*   ina inb inc ind out pwr gnd subname
x0  1            9   6   7  sinv
x1  2            10  6   7  sinv
x2  3            11  6   7  sinv
x3  4            12  6   7  sinv
x4  9   10  11   12  8   6   7  s4nor
x5  8            5   6   7  sinv
.ends ss4nand
*********************************************************
*********************************************************
* subcircuit delay generates fee d
*          input  output  power  ground
.subckt delay   1    2     3     4
*   ina inb        out    power  ground  subname
x0   1             9      3      4    bdinv
x1   9             6      3      4    bdinv
x2   1   6         2      3      4    bs2and
.ends delay
*********************************************************
* subcircuit for hspice two-phase sbfl clock
*          inclk ph1 ph2 ph2d ph1l ph2ld power1 power2  ground
.subckt clock  1  2  3   4   5    6    7    8      9
```

```
* ina inb out pwr gnd subname
x0 1  2  10 7  9  csnor
x1 10    11 7  9  ssinv
x2 11    3  7  9  ssinv
x3 12 3  13 7  9  csnor
x4 13    14 7  9  ssinv
x5 14    2  7  9  ssinv
x6 1     12 7  9  csinv
x7 3     4  7  9  delay
x8 2     5  7  8  lvl
x9 4     6  7  8  lvl
.ends clock
************************************************************
************************************************
* subcircuit level-shifter to drive dfets
* use hspice diode models for backconnected mesfets
*        input output vds vss
.subckt lvl  1    2    3  4
*   d  g    s   b
x0   1  25   3   0   dinv
j1   3  25   6   4   jfet04 l=1.2 w=20.0
j2   7  6    7   4   dio16  l=1.2 w=4.0
j3   7  4    4   4   jfet20 l=3.0 w=3.0
j4   3  9    9   4   jfet16 l=1.2 w=3.0
j5   9  7    0   4   jfet16 l=1.2 w=10.0
j6   3  9    10  4   jfet16 l=1.2 w=20.0
j7   11 10   11  4   dio16  l=1.2 w=20.0
j8   2  11   2   4   dio16  l=1.2 w=20.0
j9   2  4    4   4   jfet16 l=1.2 w=12.0
j10  12 2    12  4   dio16  l=1.2 w=10.0
j11  13 12   13  4   dio16  l=1.2 w=10.0
j12  14 13   14  4   dio16  l=1.2 w=10.0
j13  4  14   4   4   dio16  l=1.2 w=10.0
.ends lvl
************************************************************
************************************************
* subcircuit dcfl with sbfl outputs d flip-flop
***        d clk q /q power ground
.subckt sdff 1  2 3 4  5    6
** sbfl d flip flop
*  ina inb d  clk q  /q out power ground subname
x0       1  9 7 8     5     6   dlatch
x1 2                9  5     6   dinv
x2 9                10 5     6   dinv
x3       7  10 3 4     5     6   sdlatch
.ends sdff
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1     2     3     4
```

```
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
*********************************************************
* hspice d mesfet load subcircuit
*          input,  power, ground
.subckt dm10load  1    3      4
j0 3 1 4 4 jfet16 l=1.2 w= 10.0
j1 3 1 4 4 jfet16 l=1.2 w= 10.0
j2 3 1 4 4 jfet16 l=1.2 w= 10.0
j3 3 1 4 4 jfet16 l=1.2 w= 10.0
j4 3 1 4 4 jfet16 l=1.2 w= 10.0
j5 3 1 4 4 jfet16 l=1.2 w= 10.0
j6 3 1 4 4 jfet16 l=1.2 w= 10.0
j7 3 1 4 4 jfet16 l=1.2 w= 10.0
j8 3 1 4 4 jfet16 l=1.2 w= 10.0
j9 3 1 4 4 jfet16 l=1.2 w= 10.0
.ends   dm10load
*********************************************************
*********************************************************
* subcircuit sbfl inverter
*          input, output, power, ground
.subckt sinv    1     2     3     4
* d g s
j0 9 1 4 0 jfet04 l=1.2 w=48.0
j1 3 9 9 0 jfet16 l=1.2 w=3.0
j2 3 9 2 0 jfet04 l=1.2 w=48.0
j3 2 1 4 0 jfet04 l=1.2 w=48.0
.ends sinv
*********************************************************
*********************************************************
* hspice sbfl standard load subcircuit
*          input, output, power, ground
.subckt s10load  1      2     3      4
x0 1 5  3 4 sinv
x1 1 2  3 4 sinv
x2 1 6  3 4 sinv
x3 1 7  3 4 sinv
x4 1 8  3 4 sinv
x5 1 9  3 4 sinv
x6 1 10 3 4 sinv
x7 1 11 3 4 sinv
x8 1 12 3 4 sinv
x9 1 13 3 4 sinv
.ends   s10load
*********************************************************
*********************************************************
* subcircuit dcfl/sbfl combination refresh circuit
*           refresh ph 1 clock a0 a1 a2 ao0 ao1 ao2 mrefresh power ground
.subckt drefresh  1      2      3 4 5  6  7  8    9     10    11
```

```
*** ina inb inc ind d clk q  /q out power ground subname
x0  15 28 29 30          31  10  11   ss4nand
x1  31 2          9  33     10  11   sdff
x2  31 2  25 26 27 28 29 30  10  11   counter
x3  3                12  10  11   dinv
x4  4                13  10  11   dinv
x5  5                14  10  11   dinv
x6  1                15  10  11   dinv
x7  3  33             16  10  11   dd2and
x8  3  25             17  10  11   dd2and
x9  12 25 9            18  10  11   dd3and
x10 4  33             19  10  11   dd2and
x11 4  26             20  10  11   dd2and
x12 13 26 9            21  10  11   dd3and
x13 5  33             22  10  11   dd2and
x14 5  27             23  10  11   dd2and
x15 14 27 9            24  10  11   dd3and
x16 16 17 18           6  10  11   dd3or
x17 19 20 21           7  10  11   dd3or
x18 22 23 24           8  10  11   dd3or
.ic v(25)=0.0 v(26)=0.0 v(27)=0.0 v(31)=0.0 v(9)=0.0
+ v(28)=0.63 v(29)=0.63 v(30)=0.63 v(33)=0.63
.ends drefresh
*********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*********************************************************
* power supplies
vds   1  0 dc  2.0v  $ element under test power supply
vss   777 0 dc -2.5v  $ test load negative power supply
vload 888 0 dc  2.0v  $ test load positive power supply

* temperature card
*.temp 85.0

* signal inputs

* next line is used to provide the test signal input for transient analysis
va0  100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
va1  101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
va2  102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)
vref 200 0 pulse(0.63 0.063 33600ps 100ps 100ps 63400ps 87200ps)

* main circuit

*inclk ph1 ph2 ph2d ph11 ph2ld power1 power2  ground
x0 100 104 105 106  107  108   888   777    0  clock
*  ref ph1 a0 a1 a2 ao0 ao1 ao2 mrefresh pwr gnd
x1 200 104 100 101 102 120 121 122 130   1   0  drefresh
*  standard dcfl loads on the outputs of the circuit under test
x2 120                    220   888 0 d2load
```

```
x3 121                221   888 0 d2load
x4 122                222   888 0 d2load
x5 130                230   888 0 d2load

* measurement parameters

* next lines are used for transient analysis
.probe ph1=v(104) ref=v(200) a0=v(100) a1=v(101) a2=v(102)
+ ao0=v(120) ao1=v(121) ao2=v(122) mref=v(130)

.probe tran p(vds) p(vss) power
.measure tran avgpwr avg p(vds) from 0.0ns to 80ns
* next 8 lines will calculate vmax vmin trise tfall and tdelay :transient analy
s
.meas tran vimax max v(100) from=2ns to=20ns $ vmax input
.meas tran vimin min v(100) from=2ns to=20ns $ vmin input
.meas tran vmax max v(120) from=2ns to=20ns
.meas tran vmin min v(120) from=2ns to=20ns
* next line is adjustment necessary to facilitate measuring tfall. if
* vmin is used in tfall calc, then the tfall calculation fails as the is a larg
e
* all on to all off and this skews the targ parameter. notice that
* vmin2 is used only in the tfall calculation line.
*.meas tran vmin2 find v(104) at=11ns
.meas tran tphl trig v(104) val='(vimax-vimin)*.5' td=28ns
+ rise=1 targ v(120) val='(vmax+vmin)*.5' td=30ns fall=1
.meas tran tplh trig v(104) val='(vimax-vimin)*.5' td=20ns
+ rise=1 targ v(120) val='(vmax+vmin)*.5' td=20ns rise=1
.meas tran trise trig v(120) val='vmin+0.1*vmax' td=20ns
+ rise=1 targ v(120) val='0.9*vmax' rise=1
.meas tran tfall trig v(120) val='0.9*vmax' td=30ns
+ fall=1 targ v(120) val='vmin+0.1*vmax' td=30ns fall=1
.meas tran tdelay trig v(104) val=0.2835 td=20ns rise=1
+       targ v(120) val=0.2835    rise=1
.tran 1000ps 80ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit drefresh: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                  clock      1.00
   2 x1.                  drefresh   1.00
   3 x2.                  d2load     1.00
   4 x3.                  d2load     1.00
   5 x4.                  d2load     1.00
   6 x5.                  d2load     1.00
   7 x0.x0.                csnor     1.00
   8 x0.x1.                ssinv     1.00
```

9 x0.x2.	ssinv	1.00
10 x0.x3.	csnor	1.00
11 x0.x4.	ssinv	1.00
12 x0.x5.	ssinv	1.00
13 x0.x6.	csinv	1.00
14 x0.x7.	delay	1.00
15 x0.x8.	lvl	1.00
16 x0.x9.	lvl	1.00
17 x1.x0.	ss4nand	1.00
18 x1.x1.	sdff	1.00
19 x1.x2.	counter	1.00
20 x1.x3.	dinv	1.00
21 x1.x4.	dinv	1.00
22 x1.x5.	dinv	1.00
23 x1.x6.	dinv	1.00
24 x1.x7.	dd2and	1.00
25 x1.x8.	dd2and	1.00
26 x1.x9.	dd3and	1.00
27 x1.x10.	dd2and	1.00
28 x1.x11.	dd2and	1.00
29 x1.x12.	dd3and	1.00
30 x1.x13.	dd2and	1.00
31 x1.x14.	dd2and	1.00
32 x1.x15.	dd3and	1.00
33 x1.x16.	dd3or	1.00
34 x1.x17.	dd3or	1.00
35 x1.x18.	dd3or	1.00
36 x2.x0.	dinv	1.00
37 x2.x1.	dinv	1.00
38 x3.x0.	dinv	1.00
39 x3.x1.	dinv	1.00
40 x4.x0.	dinv	1.00
41 x4.x1.	dinv	1.00
42 x5.x0.	dinv	1.00
43 x5.x1.	dinv	1.00
44 x0.x7.x0.	bdinv	1.00
45 x0.x7.x1.	bdinv	1.00
46 x0.x7.x2.	bs2and	1.00
47 x0.x8.x0.	dinv	1.00
48 x0.x9.x0.	dinv	1.00
49 x1.x0.x0.	sinv	1.00
50 x1.x0.x1.	sinv	1.00
51 x1.x0.x2.	sinv	1.00
52 x1.x0.x3.	sinv	1.00
53 x1.x0.x4.	s4nor	1.00
54 x1.x0.x5.	sinv	1.00
55 x1.x1.x0.	dlatch	1.00
56 x1.x1.x1.	dinv	1.00
57 x1.x1.x2.	dinv	1.00
58 x1.x1.x3.	sdlatch	1.00
59 x1.x2.x0.	dinv	1.00

60 x1.x2.x1.	dd2and	1.00
61 x1.x2.x2.	dd2and	1.00
62 x1.x2.x3.	dd2or	1.00
63 x1.x2.x4.	dd2and	1.00
64 x1.x2.x5.	dd2and	1.00
65 x1.x2.x6.	dd3and	1.00
66 x1.x2.x7.	dd3or	1.00
67 x1.x2.x8.	dd2and	1.00
68 x1.x2.x9.	dd2and	1.00
69 x1.x2.x10.	dd4and	1.00
70 x1.x2.x11.	dd2and	1.00
71 x1.x2.x12.	dd4or	1.00
72 x1.x2.x13.	cpdff	1.00
73 x1.x2.x14.	cpdff	1.00
74 x1.x2.x15.	cpdff	1.00
75 x1.x7.x0.	dinv	1.00
76 x1.x7.x1.	dinv	1.00
77 x1.x7.x2.	d2nor	1.00
78 x1.x8.x0.	dinv	1.00
79 x1.x8.x1.	dinv	1.00
80 x1.x8.x2.	d2nor	1.00
81 x1.x9.x0.	dinv	1.00
82 x1.x9.x1.	dinv	1.00
83 x1.x9.x2.	dinv	1.00
84 x1.x9.x3.	d3nor	1.00
85 x1.x10.x0.	dinv	1.00
86 x1.x10.x1.	dinv	1.00
87 x1.x10.x2.	d2nor	1.00
88 x1.x11.x0.	dinv	1.00
89 x1.x11.x1.	dinv	1.00
90 x1.x11.x2.	d2nor	1.00
91 x1.x12.x0.	dinv	1.00
92 x1.x12.x1.	dinv	1.00
93 x1.x12.x2.	dinv	1.00
94 x1.x12.x3.	d3nor	1.00
95 x1.x13.x0.	dinv	1.00
96 x1.x13.x1.	dinv	1.00
97 x1.x13.x2.	d2nor	1.00
98 x1.x14.x0.	dinv	1.00
99 x1.x14.x1.	dinv	1.00
100 x1.x14.x2.	d2nor	1.00
101 x1.x15.x0.	dinv	1.00
102 x1.x15.x1.	dinv	1.00
103 x1.x15.x2.	dinv	1.00
104 x1.x15.x3.	d3nor	1.00
105 x1.x16.x0.	d3nor	1.00
106 x1.x16.x1.	dinv	1.00
107 x1.x17.x0.	d3nor	1.00
108 x1.x17.x1.	dinv	1.00
109 x1.x18.x0.	d3nor	1.00
110 x1.x18.x1.	dinv	1.00

111 x0.x7.x2.x0.	bdinv	1.00
112 x0.x7.x2.x1.	bdinv	1.00
113 x0.x7.x2.x2.	bs2nor	1.00
114 x1.x1.x0.x0.	d2nand	1.00
115 x1.x1.x0.x1.	dinv	1.00
116 x1.x1.x0.x2.	d2nand	1.00
117 x1.x1.x0.x3.	d2nand	1.00
118 x1.x1.x0.x4.	d2nand	1.00
119 x1.x1.x3.x0.	d2nand	1.00
120 x1.x1.x3.x1.	dinv	1.00
121 x1.x1.x3.x2.	d2nand	1.00
122 x1.x1.x3.x3.	ss2nand	1.00
123 x1.x1.x3.x4.	ss2nand	1.00
124 x1.x2.x1.x0.	dinv	1.00
125 x1.x2.x1.x1.	dinv	1.00
126 x1.x2.x1.x2.	d2nor	1.00
127 x1.x2.x2.x0.	dinv	1.00
128 x1.x2.x2.x1.	dinv	1.00
129 x1.x2.x2.x2.	d2nor	1.00
130 x1.x2.x3.x0.	d2nor	1.00
131 x1.x2.x3.x1.	dinv	1.00
132 x1.x2.x4.x0.	dinv	1.00
133 x1.x2.x4.x1.	dinv	1.00
134 x1.x2.x4.x2.	d2nor	1.00
135 x1.x2.x5.x0.	dinv	1.00
136 x1.x2.x5.x1.	dinv	1.00
137 x1.x2.x5.x2.	d2nor	1.00
138 x1.x2.x6.x0.	dinv	1.00
139 x1.x2.x6.x1.	dinv	1.00
140 x1.x2.x6.x2.	dinv	1.00
141 x1.x2.x6.x3.	d3nor	1.00
142 x1.x2.x7.x0.	d3nor	1.00
143 x1.x2.x7.x1.	dinv	1.00
144 x1.x2.x8.x0.	dinv	1.00
145 x1.x2.x8.x1.	dinv	1.00
146 x1.x2.x8.x2.	d2nor	1.00
147 x1.x2.x9.x0.	dinv	1.00
148 x1.x2.x9.x1.	dinv	1.00
149 x1.x2.x9.x2.	d2nor	1.00
150 x1.x2.x10.x0.	dinv	1.00
151 x1.x2.x10.x1.	dinv	1.00
152 x1.x2.x10.x2.	dinv	1.00
153 x1.x2.x10.x3.	dinv	1.00
154 x1.x2.x10.x4.	d4nor	1.00
155 x1.x2.x11.x0.	dinv	1.00
156 x1.x2.x11.x1.	dinv	1.00
157 x1.x2.x11.x2.	d2nor	1.00
158 x1.x2.x12.x0.	d4nor	1.00
159 x1.x2.x12.x1.	dinv	1.00
160 x1.x2.x13.x0.	dd2nand	1.00
161 x1.x2.x13.x1.	dd3nand	1.00

162 x1.x2.x13.x2.	dd3nand	1.00
163 x1.x2.x13.x3.	dd3nand	1.00
164 x1.x2.x13.x4.	dd2nand	1.00
165 x1.x2.x13.x5.	dd3nand	1.00
166 x1.x2.x14.x0.	dd2nand	1.00
167 x1.x2.x14.x1.	dd3nand	1.00
168 x1.x2.x14.x2.	dd3nand	1.00
169 x1.x2.x14.x3.	dd3nand	1.00
170 x1.x2.x14.x4.	dd2nand	1.00
171 x1.x2.x14.x5.	dd3nand	1.00
172 x1.x2.x15.x0.	dd2nand	1.00
173 x1.x2.x15.x1.	dd3nand	1.00
174 x1.x2.x15.x2.	dd3nand	1.00
175 x1.x2.x15.x3.	dd3nand	1.00
176 x1.x2.x15.x4.	dd2nand	1.00
177 x1.x2.x15.x5.	dd3nand	1.00
178 x1.x1.x3.x3.x0.	sinv	1.00
179 x1.x1.x3.x3.x1.	sinv	1.00
180 x1.x1.x3.x3.x2.	s2nor	1.00
181 x1.x1.x3.x3.x3.	sinv	1.00
182 x1.x1.x3.x4.x0.	sinv	1.00
183 x1.x1.x3.x4.x1.	sinv	1.00
184 x1.x1.x3.x4.x2.	s2nor	1.00
185 x1.x1.x3.x4.x3.	sinv	1.00
186 x1.x2.x13.x0.x0.	dinv	1.00
187 x1.x2.x13.x0.x1.	dinv	1.00
188 x1.x2.x13.x0.x2.	d2nor	1.00
189 x1.x2.x13.x0.x3.	dinv	1.00
190 x1.x2.x13.x1.x0.	dinv	1.00
191 x1.x2.x13.x1.x1.	dinv	1.00
192 x1.x2.x13.x1.x2.	dinv	1.00
193 x1.x2.x13.x1.x3.	d3nor	1.00
194 x1.x2.x13.x1.x4.	dinv	1.00
195 x1.x2.x13.x2.x0.	dinv	1.00
196 x1.x2.x13.x2.x1.	dinv	1.00
197 x1.x2.x13.x2.x2.	dinv	1.00
198 x1.x2.x13.x2.x3.	d3nor	1.00
199 x1.x2.x13.x2.x4.	dinv	1.00
200 x1.x2.x13.x3.x0.	dinv	1.00
201 x1.x2.x13.x3.x1.	dinv	1.00
202 x1.x2.x13.x3.x2.	dinv	1.00
203 x1.x2.x13.x3.x3.	d3nor	1.00
204 x1.x2.x13.x3.x4.	dinv	1.00
205 x1.x2.x13.x4.x0.	dinv	1.00
206 x1.x2.x13.x4.x1.	dinv	1.00
207 x1.x2.x13.x4.x2.	d2nor	1.00
208 x1.x2.x13.x4.x3.	dinv	1.00
209 x1.x2.x13.x5.x0.	dinv	1.00
210 x1.x2.x13.x5.x1.	dinv	1.00
211 x1.x2.x13.x5.x2.	dinv	1.00
212 x1.x2.x13.x5.x3.	d3nor	1.00

213 x1.x2.x13.x5.x4.	dinv	1.00
214 x1.x2.x14.x0.x0.	dinv	1.00
215 x1.x2.x14.x0.x1.	dinv	1.00
216 x1.x2.x14.x0.x2.	d2nor	1.00
217 x1.x2.x14.x0.x3.	dinv	1.00
218 x1.x2.x14.x1.x0.	dinv	1.00
219 x1.x2.x14.x1.x1.	dinv	1.00
220 x1.x2.x14.x1.x2.	dinv	1.00
221 x1.x2.x14.x1.x3.	d3nor	1.00
222 x1.x2.x14.x1.x4.	dinv	1.00
223 x1.x2.x14.x2.x0.	dinv	1.00
224 x1.x2.x14.x2.x1.	dinv	1.00
225 x1.x2.x14.x2.x2.	dinv	1.00
226 x1.x2.x14.x2.x3.	d3nor	1.00
227 x1.x2.x14.x2.x4.	dinv	1.00
228 x1.x2.x14.x3.x0.	dinv	1.00
229 x1.x2.x14.x3.x1.	dinv	1.00
230 x1.x2.x14.x3.x2.	dinv	1.00
231 x1.x2.x14.x3.x3.	d3nor	1.00
232 x1.x2.x14.x3.x4.	dinv	1.00
233 x1.x2.x14.x4.x0.	dinv	1.00
234 x1.x2.x14.x4.x1.	dinv	1.00
235 x1.x2.x14.x4.x2.	d2nor	1.00
236 x1.x2.x14.x4.x3.	dinv	1.00
237 x1.x2.x14.x5.x0.	dinv	1.00
238 x1.x2.x14.x5.x1.	dinv	1.00
239 x1.x2.x14.x5.x2.	dinv	1.00
240 x1.x2.x14.x5.x3.	d3nor	1.00
241 x1.x2.x14.x5.x4.	dinv	1.00
242 x1.x2.x15.x0.x0.	dinv	1.00
243 x1.x2.x15.x0.x1.	dinv	1.00
244 x1.x2.x15.x0.x2.	d2nor	1.00
245 x1.x2.x15.x0.x3.	dinv	1.00
246 x1.x2.x15.x1.x0.	dinv	1.00
247 x1.x2.x15.x1.x1.	dinv	1.00
248 x1.x2.x15.x1.x2.	dinv	1.00
249 x1.x2.x15.x1.x3.	d3nor	1.00
250 x1.x2.x15.x1.x4.	dinv	1.00
251 x1.x2.x15.x2.x0.	dinv	1.00
252 x1.x2.x15.x2.x1.	dinv	1.00
253 x1.x2.x15.x2.x2.	dinv	1.00
254 x1.x2.x15.x2.x3.	d3nor	1.00
255 x1.x2.x15.x2.x4.	dinv	1.00
256 x1.x2.x15.x3.x0.	dinv	1.00
257 x1.x2.x15.x3.x1.	dinv	1.00
258 x1.x2.x15.x3.x2.	dinv	1.00
259 x1.x2.x15.x3.x3.	d3nor	1.00
260 x1.x2.x15.x3.x4.	dinv	1.00
261 x1.x2.x15.x4.x0.	dinv	1.00
262 x1.x2.x15.x4.x1.	dinv	1.00
263 x1.x2.x15.x4.x2.	d2nor	1.00

```
 264 x1.x2.x15.x4.x3.          dinv      1.00
 265 x1.x2.x15.x5.x0.          dinv      1.00
 266 x1.x2.x15.x5.x1.          dinv      1.00
 267 x1.x2.x15.x5.x2.          dinv      1.00
 268 x1.x2.x15.x5.x3.          d3nor     1.00
 269 x1.x2.x15.x5.x4.          dinv      1.00
 Opening plot unit= 15
file=drefresh1.pa0

** hspice file created for circuit drefresh: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage      node   =voltage      node   =voltage


+ 0:1     =  2.0000   0:100   =  63.0000m  0:101   =  63.0000m
+ 0:102   =  63.0000m  0:104   =  31.9639m  0:105   = 720.7624m
+ 0:106   = 758.0773m  0:107   =  -1.2402   0:108   = 104.3442m
+ 0:120   =  52.0502m  0:121   =  52.0502m  0:122   =  52.0502m
+ 0:130   =  9.6973u   0:200   = 630.0000m  0:220   =  1.9872
+ 0:221   =  1.9872   0:222   =  1.9872   0:230   =  1.9952
+ 0:777   =  -2.5000   0:888   =  2.0000   1:10    = 633.6943m
+ 1:11    =  11.3673m  1:12    = 726.7178m  1:13    =  49.0605m
+ 1:14    = 692.6305m  2:12    = 658.6414m  2:13    = 658.6414m
+ 2:14    = 658.6414m  2:15    =  53.9658m  2:16    =  52.0088m
+ 2:17    =  32.4497m  2:18    =  32.4488m  2:19    =  52.0088m
+ 2:20    =  32.4497m  2:21    =  32.4488m  2:22    =  52.0088m
+ 2:23    =  32.4497m  2:24    =  32.4488m  2:25    =  17.6214u
+ 2:26    =  17.6214u  2:27    =  17.6214u  2:28    = 629.9885m
+ 2:29    = 629.9926m  2:30    = 629.9967m  2:31    =  48.9071u
+ 2:33    = 630.0137m  3:5     =  1.9872   4:5     =  1.9872
+ 5:5     =  1.9872   6:5     =  1.9952   7:8     =  1.2978
+ 8:9     =  53.4430m  9:9     =  1.3829   10:8    =  57.9851m
+ 11:9    =  1.3554   12:9    =  56.8501m  13:9    =  1.3747
+ 14:6    = 636.2190m  14:9    =  58.0085m  15:6    =  1.3578
+ 15:7    = 652.5236m  15:9    =  74.9274m  15:10   = 230.8765m
+ 15:11   =-504.6670m  15:12   =  -1.5552   15:13   =  -1.8701
+ 15:14   =  -2.1851   15:25   =  1.9694   16:6    =-347.6985m
+ 16:7    =  -1.0403   16:9    =  1.9988   16:10   =  1.5987
+ 16:11   = 851.5057m  16:12   =-546.7419m  16:13   =  -1.1978
+ 16:14   =  -1.8489   16:25   =  87.5051m  17:8    =  31.9352m
+ 17:9    = 692.6027m  17:10   =  10.5772m  17:11   =  10.5781m
+ 17:12   =  10.5790m  18:7    =  78.5842m  18:8    = 635.5417m
+ 18:9    = 607.4009m  18:10   =  58.7776m  19:11   = 624.0781m
+ 19:12   =  52.0115m  19:13   =  52.0127m  19:14   =  52.0115m
+ 19:15   =  52.0127m  19:16   =  32.4480m  19:17   =  52.0127m
+ 19:18   =  52.0127m  19:19   =  26.2560m  19:20   =  52.0509m
+ 19:21   =  52.0488m  19:22   =  52.0458m  19:23   =  52.0115m
+ 24:10   = 658.6317m  24:11   =  53.9637m  25:10   = 653.5035m
+ 25:11   = 653.6595m  26:10   =  52.0534m  26:11   = 653.6593m
```

+26:12 = 653.6593m 27:10 = 658.6317m 27:11 = 53.9637m
+28:10 = 653.5035m 28:11 = 653.6595m 29:10 = 52.0534m
+29:11 = 653.6593m 29:12 = 653.6593m 30:10 = 658.6317m
+30:11 = 53.9637m 31:10 = 653.5035m 31:11 = 653.6595m
+32:10 = 52.0534m 32:11 = 653.6593m 32:12 = 653.6593m
+33:7 = 658.5020m 34:7 = 658.5020m 35:7 = 658.5020m
+46:6 = 33.9796m 46:9 = 58.0085m 49:9 = 1.3553
+50:9 = 53.9676m 51:9 = 53.9669m 52:9 = 53.9663m
+53:8 = 56.8134m 54:9 = 678.3717m 55:7 = 631.5538m
+55:8 = 678.6259m 55:9 = 65.8780m 58:7 = 622.4007m
+58:8 = 652.8533m 58:9 = 652.6687m 60:10 = 658.7911m
+60:11 = 54.9626m 61:10 = 658.7914m 61:11 = 53.9676m
+62:6 = 658.5363m 63:10 = 658.7911m 63:11 = 54.9626m
+64:10 = 658.7914m 64:11 = 53.9676m 65:10 = 653.6590m
+65:11 = 53.9669m 65:12 = 653.6590m 66:7 = 658.4423m
+67:10 = 658.7914m 67:11 = 53.9669m 68:10 = 658.7914m
+68:11 = 53.9676m 69:10 = 651.6432m 69:11 = 651.6432m
+69:12 = 651.6432m 69:13 = 53.9663m 70:10 = 54.9626m
+70:11 = 658.7911m 71:8 = 658.3019m 72:9 = 52.0506m
+72:10 = 624.0440m 72:11 = 636.5449m 72:12 = 636.5992m
+73:9 = 52.0506m 73:10 = 624.0440m 73:11 = 636.5449m
+73:12 = 636.5992m 74:9 = 52.0506m 74:10 = 624.0440m
+74:11 = 636.5449m 74:12 = 636.5992m 113:8 = 1.4067
+114:6 = 6.0274m 116:6 = 32.7632m 117:6 = 48.4090m
+118:6 = 36.3487m 119:6 = 58.4402m 121:6 = 8.5683m
+122:6 = 10.5824m 122:7 = 684.7784m 122:9 = 16.3579m
+123:6 = 692.7547m 123:7 = 32.0179m 123:9 = 16.3022m
+160:10 = 53.0867m 160:11 = 54.9689m 160:12 = 658.5204m
+161:10 = 651.5335m 161:11 = 651.6421m 161:12 = 651.5924m
+161:13 = 26.2529m 162:10 = 54.9689m 162:11 = 658.7304m
+162:12 = 53.0867m 162:13 = 51.9668m 163:10 = 53.0929m
+163:11 = 653.6561m 163:12 = 653.5469m 163:13 = 32.4387m
+164:10 = 54.9689m 164:11 = 53.9676m 164:12 = 640.4275m
+165:10 = 653.6591m 165:11 = 653.6591m 165:12 = 53.0929m
+165:13 = 32.4484m 166:10 = 53.0867m 166:11 = 54.9689m
+166:12 = 658.5204m 167:10 = 651.5335m 167:11 = 651.6421m
+167:12 = 651.5924m 167:13 = 26.2529m 168:10 = 54.9689m
+168:11 = 658.7304m 168:12 = 53.0867m 168:13 = 51.9668m
+169:10 = 53.0929m 169:11 = 653.6561m 169:12 = 653.5469m
+169:13 = 32.4387m 170:10 = 54.9689m 170:11 = 53.9663m
+170:12 = 640.4275m 171:10 = 653.6591m 171:11 = 653.6591m
+171:12 = 53.0929m 171:13 = 32.4484m 172:10 = 53.0867m
+172:11 = 54.9689m 172:12 = 658.5204m 173:10 = 651.5335m
+173:11 = 651.6421m 173:12 = 651.5924m 173:13 = 26.2529m
+174:10 = 54.9689m 174:11 = 658.7304m 174:12 = 53.0867m
+174:13 = 51.9668m 175:10 = 53.0929m 175:11 = 653.6561m
+175:12 = 653.5469m 175:13 = 32.4387m 176:10 = 54.9689m
+176:11 = 53.9663m 176:12 = 640.4275m 177:10 = 653.6591m
+177:11 = 653.6591m 177:12 = 53.0929m 177:13 = 32.4484m
+178:9 = 52.0275m 179:9 = 53.9637m 180:8 = 1.3479
+181:9 = 55.0192m 182:9 = 52.0302m 183:9 = 1.3559

```
+184:8     =  56.8710m 185:9     =  1.2949


 Opening plot unit= 16
file=drefresh1.tr0

** hspice file created for circuit drefresh: transient&power @ 25.0c
****** transient analysis           tnom=  25.000 temp=  25.000
******
 avgpwr       = -4.3741E-01  from=  0.0000E+00    to=  8.0000E-08
 vimax        =  6.3000E-01   at=  4.3000E-09
        from=  2.0000E-09   to=  2.0000E-08
 vimin        =  6.3000E-02   at=  2.0000E-09
        from=  2.0000E-09   to=  2.0000E-08
 vmax         =  6.4008E-01   at=  1.4419E-08
        from=  2.0000E-09   to=  2.0000E-08
 vmin         =  5.0554E-02   at=  4.3589E-09
        from=  2.0000E-09   to=  2.0000E-08
 tphl         =  1.2046E-09  targ=  3.1349E-08  trig=  3.0145E-08
 tplh         =  1.0436E-09  targ=  2.2781E-08  trig=  2.1737E-08
 trise        =  3.5483E-10  targ=  2.3016E-08  trig=  2.2661E-08
 tfall        =  1.3193E-10  targ=  3.1419E-08  trig=  3.1287E-08
 tdelay       =  1.0060E-09  targ=  2.2743E-08  trig=  2.1737E-08

      ***** job concluded
       total cpu time      1930.53 seconds
          job started at  20:28:46  3-feb93
          job ended   at  21:35:50  3-feb93


I am done with drefresh1.sp
Wed Feb  3 21:35:51 PST 1993
```

N. Listing File for DECODDRVER Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
 reading design configuration file: ddrver1.cfg
setting user memory from  config file     to  1000000 words. (  8000000 bytes)

 ******    h s p i c e   9007d        18:44:12  4-feb93  sun
** hspice file created for circuit decoddrver: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
```

```
*********************************************************
*********************************************************
* subcircuit sbfl 2-input nor
*          ina   inb  output power ground
.subckt s2nor  1    2   3    4   5
* d g s
j0 8 1 5 0 jfet04 l=1.2 w=48.0
j1 8 2 5 0 jfet04 l=1.2 w=48.0
j2 4 8 8 0 jfet16 l=1.2 w=3.0
j3 4 8 3 0 jfet04 l=1.2 w=48.0
j4 3 2 5 0 jfet04 l=1.2 w=48.0
j5 3 1 5 0 jfet04 l=1.2 w=48.0
.ends s2nor
*********************************************************
*********************************************************
* subcircuit dcfl with sbfl outputs d flip-flop
***        d clk q /q power ground
.subckt sdff 1  2 3 4  5    6
** sbfl d flip flop
*  ina inb d  clk q  /q out power ground subname
x0       1  9 7 8     5     6   dlatch
x1 2                9  5     6   dinv
x2 9                10 5     6   dinv
x3       7  10 3 4      5     6   sdlatch
.ends sdff
*********************************************************
*********************************************************
* subcircuit sbfl 4-input nand
*          ina inb inc ind output power ground
.subckt ss4nand  1  2  3  4   5    6    7
*  ina inb inc ind out pwr gnd subname
x0 1             9  6  7  sinv
x1 2             10  6  7  sinv
x2 3             11  6  7  sinv
x3 4             12  6  7  sinv
x4 9   10  11  12  8  6  7  s4nor
x5 8             5  6  7  sinv
.ends ss4nand
*********************************************************
*********************************************************
* subcircuit sbfl 2-input nand
*          ina   inb  output power ground
.subckt ss2nand  1    2   3    4   5
*  ina inb out pwr gnd subname
x0 1       9  4  5  sinv
x1 2       6  4  5  sinv
x2 9   6  7  4  5  s2nor
x3 7       3  4  5  sinv
.ends ss2nand
*********************************************************
*********************************************************
```

```
* subcircuit dcfl sd-latch using generic gates
*          d  clk q  /q power ground
.subckt sdlatch  1  2 3 4   5    6
** sbfl d latch **
*   ina  inb output  power ground subname
x0   1   2   8     5    6  d2nand
x1   1       7     5    6  dinv
x2   2   7   9     5    6  d2nand
x3   8   4   3     5    6  ss2nand
x4   9   3   4     5    6  ss2nand
.ends sdlatch
*********************************************************
*********************************************************
* subcircuit dcfl d-latch using generic gates
*          d  clk q  /q power ground
.subckt dlatch  1  2 3 4   5    6
*   ina  inb output  power ground subname
x0   1   2   8     5    6  d2nand
x1   1       7     5    6  dinv
x2   2   7   9     5    6  d2nand
x3   8   4   3     5    6  d2nand
x4   9   3   4     5    6  d2nand
.ends dlatch
*********************************************************
*********************************************************
* hspice dcfl 2-input real nand subcircuit
*           ina, inb, output, power, ground
.subckt d2nand   1   2    3     4     5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 6 5 jfet04 l=1.2 w=192.0
j2 6 2 5 5 jfet04 l=1.2 w=192.0
.ends d2nand
*********************************************************
*********************************************************
* subcircuit sbfl 3-input or
*          ina   inb   inc  output power ground
.subckt s3or   1     2    3    4     5    6
*   ina inb inc out pwr gnd subname
x0   1   2   3   7   5   6  s3nor
x1   7         4   5   6  sinv
.ends   s3or
*********************************************************
*********************************************************
* subcircuit sbfl 4-input and
*          ina inb inc ind output power ground
.subckt ss4and   1   2   3   4   5    6     7
*   ina inb inc ind out pwr gnd subname
x0  1            9   6   7  sinv
x1  2            10  6   7  sinv
x2  3            11  6   7  sinv
```

```
x3 4          12  6  7 sinv
x4 9  10 11 12  5  6  7 s4nor
.ends ss4and
*********************************************************
*********************************************************
* subcircuit sbfl 4-input nor
*         ina inb inc ind output power ground
.subckt s4nor  1  2  3  4   5    6   7
*  d g s
j0  8 1 7 0 jfet04 l=1.2 w=48.0
j1  8 2 7 0 jfet04 l=1.2 w=48.0
j2  8 3 7 0 jfet04 l=1.2 w=48.0
j3  8 4 7 0 jfet04 l=1.2 w=48.0
j4  6 8 8 0 jfet16 l=1.2 w=3.0
j5  6 8 5 0 jfet04 l=1.2 w=48.0
j6  5 1 7 0 jfet04 l=1.2 w=48.0
j7  5 2 7 0 jfet04 l=1.2 w=48.0
j8  5 3 7 0 jfet04 l=1.2 w=48.0
j9  5 4 7 0 jfet04 l=1.2 w=48.0
.ends s4nor
*********************************************************
*********************************************************
* subcircuit sbfl 3-input nor
*         ina   inb   inc  output power ground
.subckt s3nor  1    2    3   4    5   6
*  d g s
j0 8 1 6 0 jfet04 l=1.2 w=48.0
j1 8 2 6 0 jfet04 l=1.2 w=48.0
j2 8 3 6 0 jfet04 l=1.2 w=48.0
j3 5 8 8 0 jfet16 l=1.2 w=3.0
j4 5 8 4 0 jfet04 l=1.2 w=48.0
j5 4 1 6 0 jfet04 l=1.2 w=48.0
j6 4 2 6 0 jfet04 l=1.2 w=48.0
j7 4 3 6 0 jfet04 l=1.2 w=48.0
.ends s3nor
*********************************************************
*********************************************************
* subcircuit sbfl 3-input and
*         ina  inb  inc  output power ground
.subckt ss3and  1   2   3   4    5   6
*  ina inb inc out pwr gnd subname
x0  1        9  5  6  sinv
x1  2        10 5  6  sinv
x2  3        11 5  6  sinv
x3  9  10 11  4  5  6  s3nor
.ends ss3and
*********************************************************
*********************************************************
* subcircuit dcfl 2-input or
*         ina   inb  output power ground
.subckt dd2or   1    2   3    4   5
```

```
*  ina inb out pwr gnd subname
x0  1  2  6  4  5  d2nor
x1  6     3  4  5  dinv
.ends  dd2or
*********************************************************
*********************************************************
* hspice dcfl 3-input nor subcircuit
*            ina, inb, inc,  output, power, ground
.subckt d3nor     1  2  3     4     5     6
* d g s b
j0 5 4 4 6 jfet16 l=1.2 w=6.0
j1 4 1 6 6 jfet04 l=1.2 w=96.0
j2 4 2 6 6 jfet04 l=1.2 w=96.0
j3 4 3 6 6 jfet04 l=1.2 w=96.0
.ends  d3nor
*********************************************************
* hspice dcfl 3-input demorgan and subcircuit
*            ina, inb, inc,  output, power, ground
.subckt dd3and   1  2  3     4     5     6
x0 1       10 5 6 dinv
x1 2       11 5 6 dinv
x2 3       12 5 6 dinv
x3 10 11 12  4 5 6 d3nor
.ends  dd3and
*********************************************************
*********************************************************
* subcircuit dcfl 3-input or
*          ina   inb   inc  output power ground
.subckt dd3or   1     2     3    4     5    6
*  ina inb inc out pwr gnd subname
x0  1  2  3  7  5  6  d3nor
x1  7        4  5  6  dinv
.ends  dd3or

*********************************************************
*********************************************************
* hspice dcfl 4-input nor subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt d4nor     1  2  3  4     5     6    7
* d g s b
j0 6 5 5 7 jfet16 l=1.2 w=6.0
j1 5 1 7 7 jfet04 l=1.2 w=96.0
j2 5 2 7 7 jfet04 l=1.2 w=96.0
j3 5 3 7 7 jfet04 l=1.2 w=96.0
j4 5 4 7 7 jfet04 l=1.2 w=96.0
.ends  d4nor
*********************************************************
*********************************************************
* subcircuit dcfl 4-input or
*          ina inb inc ind output power ground
.subckt dd4or  1  2  3  4  5     6    7
```

```
*  ina inb inc ind out pwr gnd subname
x0  1  2  3  4  8  6  7  d4nor
x1  8          5  6  7  dinv
.ends  dd4or
*********************************************************
*********************************************************
* hspice dcfl 4-input demorgan  and subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt dd4and  1   2   3   4     5      6    7
x0 1          10 6 7 dinv
x1 2          11 6 7 dinv
x2 3          12 6 7 dinv
x3 4          13 6 7 dinv
x4 10 11 12 13  5  6 7 d4nor
.ends  dd4and
*********************************************************
*********************************************************
* subcircuit hspice dcfl clear d flip flop
* wakerly pg 363 - 31july 1992
***          d clk clr  q  /q  power  ground
.subckt cpdff  1  2   3 4 5    6     7
x0    12  10        9   6   7   dd2nand
x1   9  3   2        10  6   7   dd3nand
x2  10  2  12         11  6   7   dd3nand
x3  11  3   1         12  6   7   dd3nand
x4    10   5         4   6   7   dd2nand
x5   4  3  11         5   6   7   dd3nand
.ends  cpdff
*********************************************************
*********************************************************
* hspice dcfl 2-input demorgan nand subcircuit
*            ina, inb, output, power, ground
.subckt dd2nand   1   2    3      4     5
x0 1     10 4 5 dinv
x1 2     11 4 5 dinv
x2 10 11 12 4 5 d2nor
x3 12    3  4 5 dinv
.ends  dd2nand
*********************************************************
*********************************************************
*********************************************************
* hspice dcfl 3-input demorgan nand subcircuit
*            ina, inb, inc,  output, power, ground
.subckt dd3nand  1   2   3      4     5      6
x0 1        10 5 6 dinv
x1 2        11 5 6 dinv
x2 3        12 5 6 dinv
x3 10 11 12 13 5 6 d3nor
x4 13       4  5 6 dinv
.ends  dd3nand
*********************************************************
```

```
*************************************************************
* hspice dcfl 2-input nor subcircuit
*            ina, inb, output, power, ground
.subckt d2nor    1   2   3    4    5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 5 5 jfet04 l=1.2 w=96.0
j2 3 2 5 5 jfet04 l=1.2 w=96.0
.ends  d2nor
*************************************************************
* hspice dcfl 2-input demorgan and subcircuit
*            ina, inb, output, power, ground
.subckt dd2and   1   2   3    4    5
x0 1    10 4 5 dinv
x1 2    11 4 5 dinv
x2 10 11  3 4 5 d2nor
.ends  dd2and
*************************************************************
*************************************************************
* subcircuit level-shifter to drive dfets
* use hspice diode models for backconnected mesfets
*         input output vds vss
.subckt lvl  1    2    3  4
*    d  g    s   b
x0   1  25   3   0   dinv
j1   3  25   6   4   jfet04 l=1.2 w=20.0
j2   7  6    7   4   dio16  l=1.2 w=4.0
j3   7  4    4   4   jfet20 l=3.0 w=3.0
j4   3  9    9   4   jfet16 l=1.2 w=3.0
j5   9  7    0   4   jfet16 l=1.2 w=10.0
j6   3  9    10  4   jfet16 l=1.2 w=20.0
j7   11 10   11  4   dio16  l=1.2 w=20.0
j8   2  11   2   4   dio16  l=1.2 w=20.0
j9   2  4    4   4   jfet16 l=1.2 w=12.0
j10  12 2    12  4   dio16  l=1.2 w=10.0
j11  13 12   13  4   dio16  l=1.2 w=10.0
j12  14 13   14  4   dio16  l=1.2 w=10.0
j13  4  14   4   4   dio16  l=1.2 w=10.0
.ends lvl
*************************************************************
*************************************************************
* hspice dcfl inverter subcircuit
*           input, output, power, ground
.subckt bdinv   1    2    3    4
* d g s b
j0 3 2 2 4 jfet20 l=3.0 w=40.0
j1 2 1 4 4 jfet04 l=1.2 w=240.0
.ends  bdinv
*************************************************************
* subcircuit sbfl 2-input nor
*           ina   inb  output power ground
```

```
.subckt bs2nor  1    2    3    4    5
* d g s
j0 8 1 5 0 jfet04 l=1.2 w=180.0
j1 8 2 5 0 jfet04 l=1.2 w=180.0
j2 4 8 8 0 jfet16 l=1.2 w=10.0
j3 4 8 3 0 jfet04 l=1.2 w=224.0
j4 3 2 5 0 jfet04 l=1.2 w=224.0
j5 3 1 5 0 jfet04 l=1.2 w=224.0
.ends  bs2nor
*********************************************************
* subcircuit sbfl 2- input and
*          ina   inb  output power ground
.subckt bs2and  1    2    3    4    5
*  ina inb out pwr gnd subname
x0 1      9  4  5  bdinv
x1 2      6  4  5  bdinv
x2 9   6  3  4  5  bs2nor
.ends  bs2and
*********************************************************
*********************************************************
* subckt hspice sbfl large 2-input nor
*          ina   inb  output power ground
.subckt csnor   1    2    3    4    5
* d g s b
j0 8 1 5 0 jfet04 l=1.2 w=144.0
j1 8 2 5 0 jfet04 l=1.2 w=144.0
j2 4 8 8 0 jfet16 l=1.2 w= 9.0
j3 4 8 3 0 jfet04 l=1.2 w=144.0
j4 3 2 5 0 jfet04 l=1.2 w=144.0
j5 3 1 5 0 jfet04 l=1.2 w=144.0
.ends csnor
*********************************************************
* hspice sbfl extra-large driver-inverter subcircuit
*          input, output, power, ground
.subckt ssinv   1    2    3    4
* d g s b
j0 9 1 4 0 jfet04 l=1.2 w=768.0
j1 3 9 9 0 jfet16 l=1.2 w= 48.0
j2 3 9 2 0 jfet04 l=1.2 w=768.0
j3 2 1 4 0 jfet04 l=1.2 w=768.0
.ends ssinv
*********************************************************
*********************************************************
* hspice sbfl large driver-inverter subcircuit
*          input, output, power, ground
.subckt csinv   1    2    3    4
* d g s b
j0 9 1 4 0 jfet04 l=1.2 w=256.0
j1 3 9 9 0 jfet16 l=1.2 w= 16.0
j2 3 9 2 0 jfet04 l=1.2 w=384.0
j3 2 1 4 0 jfet04 l=1.2 w=384.0
```

```
.ends csinv
*****************************************************
* subcircuit delay generates fee d
*          input  output  power  ground
.subckt delay   1    2     3     4
*   ina inb       out   power  ground  subname
x0   1            9     3     4    bdinv
x1   9            6     3     4    bdinv
x2   1  6         2     3     4    bs2and
.ends delay
*****************************************************
* subcircuit for hspice two-phase sbfl clock
*          inclk ph1 ph2 ph2d ph1l ph2ld power1 power2  ground
.subckt clock  1  2  3   4   5    6    7    8      9
*  ina inb out pwr gnd subname
x0  1   2   10 7   9   csnor
x1  10      11 7   9   ssinv
x2  11      3  7   9   ssinv
x3  12 3    13 7   9   csnor
x4  13      14 7   9   ssinv
x5  14      2  7   9   ssinv
x6  1       12 7   9   csinv
x7  3       4  7   9   delay
x8  2       5  7   8   lvl
x9  4       6  7   8   lvl
.ends clock
*****************************************************
*****************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1     2     3     4
*  d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
*****************************************************
* hspice d mesfet load subcircuit
*          input,  power, ground
.subckt dm10load  1    3      4
j0 3 1 4 4 jfet16 l=1.2 w= 10.0
j1 3 1 4 4 jfet16 l=1.2 w= 10.0
j2 3 1 4 4 jfet16 l=1.2 w= 10.0
j3 3 1 4 4 jfet16 l=1.2 w= 10.0
j4 3 1 4 4 jfet16 l=1.2 w= 10.0
j5 3 1 4 4 jfet16 l=1.2 w= 10.0
j6 3 1 4 4 jfet16 l=1.2 w= 10.0
j7 3 1 4 4 jfet16 l=1.2 w= 10.0
j8 3 1 4 4 jfet16 l=1.2 w= 10.0
j9 3 1 4 4 jfet16 l=1.2 w= 10.0
.ends  dm10load
*****************************************************
```

```
*********************************************************
* subcircuit sbfl inverter
*          input, output, power, ground
.subckt sinv   1    2    3    4
* d g s
j0 9 1 4 0 jfet04 l=1.2 w=48.0
j1 3 9 9 0 jfet16 l=1.2 w=3.0
j2 3 9 2 0 jfet04 l=1.2 w=48.0
j3 2 1 4 0 jfet04 l=1.2 w=48.0
.ends sinv
*********************************************************
*************************************************************
* hspice sbfl standard load subcircuit
*          input, output, power, ground
.subckt s10load  1     2    3     4
x0 1 5  3 4 sinv
x1 1 2  3 4 sinv
x2 1 6  3 4 sinv
x3 1 7  3 4 sinv
x4 1 8  3 4 sinv
x5 1 9  3 4 sinv
x6 1 10 3 4 sinv
x7 1 11 3 4 sinv
x8 1 12 3 4 sinv
x9 1 13 3 4 sinv
.ends  s10load
*************************************************************
*********************************************************
* subcircuit dcfl counter using clear/preset d fps - cpdff
***          enble clk q0 q1 q2 /q0 /q1 /q2 power ground
.subckt counter  1   2  3 4 5 6  7  8   9    10
*** ina inb inc ind d clk q  /q out power ground subname
x0  1                    11  9   10    dinv
x1  3  11                 12  9   10    dd2and
x2  1  6                  13  9   10    dd2and
x3  12 13                  20  9   10    dd2or
x4  4  11                 14  9   10    dd2and
x5  4  6                  15  9   10    dd2and
x6  3  7  1                16  9   10    dd3and
x7  14 15 16                21  9   10    dd3or
x8  5  7                  17  9   10    dd2and
x9  5  6                  18  9   10    dd2and
x10 1  3  4  8              19  9   10    dd4and
x11 11 5                  23  9   10    dd2and
x12 17 18 19 23             22  9   10    dd4or
x13 20 2  1         3 6      9   10    cpdff
x14 21 2  1         4 7      9   10    cpdff
x15 22 2  1         5 8      9   10    cpdff
.ends  counter
*********************************************************
*********************************************************
```

```
* subcircuit non-latched sbfl/dcfl combination decoder
****          a0 a1 a2 w  r  re o0 o1 o2 o3 o4 o5 o6 o7 enbl pwr grnd
.subckt decoder 1  2  3  4  5  6  7  8  9  10 11 12 13 14  15   16  17
*   ina inb inc ind      output  power ground subname
x1   1               20    16   17   dinv
x2   2               18    16   17   dinv
x3   3               19    16   17   dinv
x4    4  5  6         15    16   17   s3or
x5    20 18 19 15     7     16   17   ss4and
x6    1  18 19 15     8     16   17   ss4and
x7    20 2  19 15     9     16   17   ss4and
x8    1  2  19 15     10    16   17   ss4and
x9    20 18 3  15     11    16   17   ss4and
x10   1  18 3  15     12    16   17   ss4and
x11   20 2  3  15     13    16   17   ss4and
x12   1  2  3  15     14    16   17   ss4and
.ends decoder
************************************************************
************************************************************
* subcircuit dcfl/sbfl combination refresh circuit
*           refresh ph 1 clock a0 a1 a2 ao0 ao1 ao2 mrefresh power g: ound
.subckt drefresh  1     2     3 4 5  6  7  8    9     10    11
*** ina inb inc ind d clk q  /q out power ground subname
x0  15 28 29 30          31  10  11   ss4nand
x1  31 2           9  33     10  11   sdff
x2  31 2  25 26 27 28 29 30  10  11   counter
x3  3                12  10  11   dinv
x4  4                13  10  11   dinv
x5  5                14  10  11   dinv
x6  1                15  10  11   dinv
x7  3  33             16  10  11   dd2and
x8  3  25             17  10  11   dd2and
x9  12 25 9            18  10  11   dd3and
x10 4  33             19  10  11   dd2and
x11 4  26             20  10  11   dd2and
x12 13 26 9            21  10  11   dd3and
x13 5  33             22  10  11   dd2and
x14 5  27             23  10  11   dd2and
x15 14 27 9            24  10  11   dd3and
x16 16 17 18           6   10  11   dd3or
x17 19 20 21           7   10  11   dd3or
x18 22 23 24           8   10  11   dd3or
.ic v(25)=0.0 v(26)=0.0 v(27)=0.0 v(31)=0.0 v(9)=0.0
+ v(28)=0.63 v(29)=0.63 v(30)=0.63 v(33)=0.63
.ends drefresh
************************************************************
************************************************************
* subcircuit decoder/driver 'decoddrver'
** 1   2  3  4  5  6 7  8  9 10 11 12 13 14 15 16 17 18 19 20
** ph2d ao0 ao1 ao2 mref mr mw da0 da1 da2 da3 da4 da5 da6 da7 evu odu ev od pw
r
```

```
.subckt decoddrver 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
*** ina inb inc ind d clk q  /q out       enbl pwr  bulk  subname
x0  2  3 4 7 6 5  30 31 32 33 34 35 36 37 50  20    22   decoder
x1  2                  48          20    22  dinv
x2  2  1 50             17          20    22  ss3and
x3  48  1 50            16          20    22  ss3and
x4  30  1          40               20    22  dd2and
x5  31  1          41               20    22  dd2and
x6  32  1          42               20    22  dd2and
x7  33  1          43               20    22  dd2and
x8  34  1          44               20    22  dd2and
x9  35  1          45               20    22  dd2and
x10 36  1          46               20    22  dd2and
x11 37  1          47               20    22  dd2and
x12 40             8                20    21  lvl
x13 41             9                20    21  lvl
x14 42             10               20    21  lvl
x15 43             11               20    21  lvl
x16 44             12               20    21  lvl
x17 45             13               20    21  lvl
x18 46             14               20    21  lvl
x19 47             15               20    21  lvl
x20 16             18               20    21  lvl
x21 17             19               20    21  lvl
.ends decoddrver
*********************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*******************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vss   777 0  dc -2.5v  $ test load negative power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs

* next three lines used to provide test signal inputs for transient analysis
va0   100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
va1   101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
va2   102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)
vref  200 0 pulse(0.63 0.063 63600ps 100ps 100ps 63400ps 87200ps)
vmr   201 0 0.063v
vmw   202 0 0.063v

*inclk ph1 ph2 ph2d ph1l ph2ld power1 power2  ground
x0 100 104 105 106  107  108    888   777     0  clock
*******************************************************
*  ref ph1 a0 a1 a2 ao0 ao1 ao2 mrefresh pwr gnd
```

```
x1 200 104 100 101 102 120 121 122 130  888   0  drefresh
**********************************************************
** ph2d ao0 ao1 ao2 mref mr mw  da0 da1 da2 da3 da4 da5 da6 da7 evu odu ev  od
x2 106  120 121 122 130 201 202 150 151 152 153 154 155 156 157 160 161 170 171
*  pwr1 pwr2 gnd subname
+  1  777  0 decoddrver

* measurement parameters


* next lines are used for transient analysis
.probe ao0=v(120) ao1=v(121) ao2=v(122) mref=v(130)
+ ph2d=v(106) da0=v(150) da1=v(151) da2=v(152) da3=v(153) da4=v(154) da5=v(155)
+ da6=v(156) da7=v(157) evu=v(160) odu=v(161) ev=v(170) od=v(171)
.probe tran p(vds) p(vss) power
.measure tran avgpwr avg p(vds)

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(120) from=2ns to=88ns
.meas tran vmin min v(120) from=2ns to=88ns
.meas tran tphl trig v(106) val='(vmax-vmin)*.5' td=12ns
+ fall=1 targ v(120) val='(vmax-vmin)*.5' td=12ns fall=1
.meas tran tplh trig v(106) val='(vmax-vmin)*.5' td=12ns
+ fall=1 targ v(121) val='(vmax-vmin)*.5' td=12ns rise=1
.meas tran trise trig v(121) val='vmin+0.1*vmax' td=12ns
+ rise=1 targ v(121) val='0.9*vmax' rise=1
.meas tran tfall trig v(120) val='0.9*vmax' td=12ns
+ fall=1 targ v(120) val='vmin+0.1*vmax' td=12ns fall=1
.meas tran tdelay trig v(106) val=.2835 td=12ns fall=1
+      targ v(120) val=.2835 td=12ns fall=1
.tran 1500ps 88ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit decoddrver: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                  clock       1.00
   2 x1.                  drefresh    1.00
   3 x2.                  decoddrver  1.00
   4 x0.x0.                csnor       1.00
   5 x0.x1.                ssinv       1.00
   6 x0.x2.                ssinv       1.00
   7 x0.x3.                csnor       1.00
   8 x0.x4.                ssinv       1.00
   9 x0.x5.                ssinv       1.00
  10 x0.x6.                csinv       1.00
  11 x0.x7.                delay       1.00
  12 x0.x8.                lvl         1.00
```

13 x0.x9.	lvl	1.00
14 x1.x0.	ss4nand	1.00
15 x1.x1.	sdff	1.00
16 x1.x2.	counter	1.00
17 x1.x3.	dinv	1.00
18 x1.x4.	dinv	1.00
19 x1.x5.	dinv	1.00
20 x1.x6.	dinv	1.00
21 x1.x7.	dd2and	1.00
22 x1.x8.	dd2and	1.00
23 x1.x9.	dd3and	1.00
24 x1.x10.	dd2and	1.00
25 x1.x11.	dd2and	1.00
26 x1.x12.	dd3and	1.00
27 x1.x13.	dd2and	1.00
28 x1.x14.	dd2and	1.00
29 x1.x15.	dd3and	1.00
30 x1.x16.	dd3or	1.00
31 x1.x17.	dd3or	1.00
32 x1.x18.	dd3or	1.00
33 x2.x0.	decoder	1.00
34 x2.x1.	dinv	1.00
35 x2.x2.	ss3and	1.00
36 x2.x3.	ss3and	1.00
37 x2.x4.	dd2and	1.00
38 x2.x5.	dd2and	1.00
39 x2.x6.	dd2and	1.00
40 x2.x7.	dd2and	1.00
41 x2.x8.	dd2and	1.00
42 x2.x9.	dd2and	1.00
43 x2.x10.	dd2and	1.00
44 x2.x11.	dd2and	1.00
45 x2.x12.	lvl	1.00
46 x2.x13.	lvl	1.00
47 x2.x14.	lvl	1.00
48 x2.x15.	lvl	1.00
49 x2.x16.	lvl	1.00
50 x2.x17.	lvl	1.00
51 x2.x18.	lvl	1.00
52 x2.x19.	lvl	1.00
53 x2.x20.	lvl	1.00
54 x2.x21.	lvl	1.00
55 x0.x7.x0.	bdinv	1.00
56 x0.x7.x1.	bdinv	1.00
57 x0.x7.x2.	bs2and	1.00
58 x0.x8.x0.	dinv	1.00
59 x0.x9.x0.	dinv	1.00
60 x1.x0.x0.	sinv	1.00
61 x1.x0.x1.	sinv	1.00
62 x1.x0.x2.	sinv	1.00
63 x1.x0.x3.	sinv	1.00

64 x1.x0.x4.	s4nor	1.00
65 x1.x0.x5.	sinv	1.00
66 x1.x1.x0.	dlatch	1.00
67 x1.x1.x1.	dinv	1.00
68 x1.x1.x2.	dinv	1.00
69 x1.x1.x3.	sdlatch	1.00
70 x1.x2.x0.	dinv	1.00
71 x1.x2.x1.	dd2and	1.00
72 x1.x2.x2.	dd2and	1.00
73 x1.x2.x3.	dd2or	1.00
74 x1.x2.x4.	dd2and	1.00
75 x1.x2.x5.	dd2and	1.00
76 x1.x2.x6.	dd3and	1.00
77 x1.x2.x7.	dd3or	1.00
78 x1.x2.x8.	dd2and	1.00
79 x1.x2.x9.	dd2and	1.00
80 x1.x2.x10.	dd4and	1.00
81 x1.x2.x11.	dd2and	1.00
82 x1.x2.x12.	dd4or	1.00
83 x1.x2.x13.	cpdff	1.00
84 x1.x2.x14.	cpdff	1.00
85 x1.x2.x15.	cpdff	1.00
86 x1.x7.x0.	dinv	1.00
87 x1.x7.x1.	dinv	1.00
88 x1.x7.x2.	d2nor	1.00
89 x1.x8.x0.	dinv	1.00
90 x1.x8.x1.	dinv	1.00
91 x1.x8.x2.	d2nor	1.00
92 x1.x9.x0.	dinv	1.00
93 x1.x9.x1.	dinv	1.00
94 x1.x9.x2.	dinv	1.00
95 x1.x9.x3.	d3nor	1.00
96 x1.x10.x0.	dinv	1.00
97 x1.x10.x1.	dinv	1.00
98 x1.x10.x2.	d2nor	1.00
99 x1.x11.x0.	dinv	1.00
100 x1.x11.x1.	dinv	1.00
101 x1.x11.x2.	d2nor	1.00
102 x1.x12.x0.	dinv	1.00
103 x1.x12.x1.	dinv	1.00
104 x1.x12.x2.	dinv	1.00
105 x1.x12.x3.	d3nor	1.00
106 x1.x13.x0.	dinv	1.00
107 x1.x13.x1.	dinv	1.00
108 x1.x13.x2.	d2nor	1.00
109 x1.x14.x0.	dinv	1.00
110 x1.x14.x1.	dinv	1.00
111 x1.x14.x2.	d2nor	1.00
112 x1.x15.x0.	dinv	1.00
113 x1.x15.x1.	dinv	1.00
114 x1.x15.x2.	dinv	1.00

115 x1.x15.x3.	d3nor	1.00
116 x1.x16.x0.	d3nor	1.00
117 x1.x16.x1.	dinv	1.00
118 x1.x17.x0.	d3nor	1.00
119 x1.x17.x1.	dinv	1.00
120 x1.x18.x0.	d3nor	1.00
121 x1.x18.x1.	dinv	1.00
122 x2.x0.x1.	dinv	1.00
123 x2.x0.x2.	dinv	1.00
124 x2.x0.x3.	dinv	1.00
125 x2.x0.x4.	s3or	1.00
126 x2.x0.x5.	ss4and	1.00
127 x2.x0.x6.	ss4and	1.00
128 x2.x0.x7.	ss4and	1.00
129 x2.x0.x8.	ss4and	1.00
130 x2.x0.x9.	ss4and	1.00
131 x2.x0.x10.	ss4and	1.00
132 x2.x0.x11.	ss4and	1.00
133 x2.x0.x12.	ss4and	1.00
134 x2.x2.x0.	sinv	1.00
135 x2.x2.x1.	sinv	1.00
136 x2.x2.x2.	sinv	1.00
137 x2.x2.x3.	s3nor	1.00
138 x2.x3.x0.	sinv	1.00
139 x2.x3.x1.	sinv	1.00
140 x2.x3.x2.	sinv	1.00
141 x2.x3.x3.	s3nor	1.00
142 x2.x4.x0.	dinv	1.00
143 x2.x4.x1.	dinv	1.00
144 x2.x4.x2.	d2nor	1.00
145 x2.x5.x0.	dinv	1.00
146 x2.x5.x1.	dinv	1.00
147 x2.x5.x2.	d2nor	1.00
148 x2.x6.x0.	dinv	1.00
149 x2.x6.x1.	dinv	1.00
150 x2.x6.x2.	d2nor	1.00
151 x2.x7.x0.	dinv	1.00
152 x2.x7.x1.	dinv	1.00
153 x2.x7.x2.	d2nor	1.00
154 x2.x8.x0.	dinv	1.00
155 x2.x8.x1.	dinv	1.00
156 x2.x8.x2.	d2nor	1.00
157 x2.x9.x0.	dinv	1.00
158 x2.x9.x1.	dinv	1.00
159 x2.x9.x2.	d2nor	1.00
160 x2.x10.x0.	dinv	1.00
161 x2.x10.x1.	dinv	1.00
162 x2.x10.x2.	d2nor	1.00
163 x2.x11.x0.	dinv	1.00
164 x2.x11.x1.	dinv	1.00
165 x2.x11.x2.	d2nor	1.00

166 x2.x12.x0. dinv 1.00
167 x2.x13.x0. dinv 1.00
168 x2.x14.x0. dinv 1.00
169 x2.x15.x0. dinv 1.00
170 x2.x16.x0. dinv 1.00
171 x2.x17.x0. dinv 1.00
172 x2.x18.x0. dinv 1.00
173 x2.x19.x0. dinv 1.00
174 x2.x20.x0. dinv 1.00
175 x2.x21.x0. dinv 1.00
176 x0.x7.x2.x0. bdinv 1.00
177 x0.x7.x2.x1. bdinv 1.00
178 x0.x7.x2.x2. bs2nor 1.00
179 x1.x1.x0.x0. d2nand 1.00
180 x1.x1.x0.x1. dinv 1.00
181 x1.x1.x0.x2. d2nand 1.00
182 x1.x1.x0.x3. d2nand 1.00
183 x1.x1.x0.x4. d2nand 1.00
184 x1.x1.x3.x0. d2nand 1.00
185 x1.x1.x3.x1. dinv 1.00
186 x1.x1.x3.x2. d2nand 1.00
187 x1.x1.x3.x3. ss2nand 1.00
188 x1.x1.x3.x4. ss2nand 1.00
189 x1.x2.x1.x0. dinv 1.00
190 x1.x2.x1.x1. dinv 1.00
191 x1.x2.x1.x2. d2nor 1.00
192 x1.x2.x2.x0. dinv 1.00
193 x1.x2.x2.x1. dinv 1.00
194 x1.x2.x2.x2. d2nor 1.00
195 x1.x2.x3.x0. d2nor 1.00
196 x1.x2.x3.x1. dinv 1.00
197 x1.x2.x4.x0. dinv 1.00
198 x1.x2.x4.x1. dinv 1.00
199 x1.x2.x4.x2. d2nor 1.00
200 x1.x2.x5.x0. dinv 1.00
201 x1.x2.x5.x1. dinv 1.00
202 x1.x2.x5.x2. d2nor 1.00
203 x1.x2.x6.x0. dinv 1.00
204 x1.x2.x6.x1. dinv 1.00
205 x1.x2.x6.x2. dinv 1.00
206 x1.x2.x6.x3. d3nor 1.00
207 x1.x2.x7.x0. d3nor 1.00
208 x1.x2.x7.x1. dinv 1.00
209 x1.x2.x8.x0. dinv 1.00
210 x1.x2.x8.x1. dinv 1.00
211 x1.x2.x8.x2. d2nor 1.00
212 x1.x2.x9.x0. dinv 1.00
213 x1.x2.x9.x1. dinv 1.00
214 x1.x2.x9.x2. d2nor 1.00
215 x1.x2.x10.x0. dinv 1.00
216 x1.x2.x10.x1. dinv 1.00

217 x1.x2.x10.x2.	dinv	1.00
218 x1.x2.x10.x3.	dinv	1.00
219 x1.x2.x10.x4.	d4nor	1.00
220 x1.x2.x11.x0.	dinv	1.00
221 x1.x2.x11.x1.	dinv	1.00
222 x1.x2.x11.x2.	d2nor	1.00
223 x1.x2.x12.x0.	d4nor	1.00
224 x1.x2.x12.x1.	dinv	1.00
225 x1.x2.x13.x0.	dd2nand	1.00
226 x1.x2.x13.x1.	dd3nand	1.00
227 x1.x2.x13.x2.	dd3nand	1.00
228 x1.x2.x13.x3.	dd3nand	1.00
229 x1.x2.x13.x4.	dd2nand	1.00
230 x1.x2.x13.x5.	dd3nand	1.00
231 x1.x2.x14.x0.	dd2nand	1.00
232 x1.x2.x14.x1.	dd3nand	1.00
233 x1.x2.x14.x2.	dd3nand	1.00
234 x1.x2.x14.x3.	dd3nand	1.00
235 x1.x2.x14.x4.	dd2nand	1.00
236 x1.x2.x14.x5.	dd3nand	1.00
237 x1.x2.x15.x0.	dd2nand	1.00
238 x1.x2.x15.x1.	dd3nand	1.00
239 x1.x2.x15.x2.	dd3nand	1.00
240 x1.x2.x15.x3.	dd3nand	1.00
241 x1.x2.x15.x4.	dd2nand	1.00
242 x1.x2.x15.x5.	dd3nand	1.00
243 x2.x0.x4.x0.	s3nor	1.00
244 x2.x0.x4.x1.	sinv	1.00
245 x2.x0.x5.x0.	sinv	1.00
246 x2.x0.x5.x1.	sinv	1.00
247 x2.x0.x5.x2.	sinv	1.00
248 x2.x0.x5.x3.	sinv	1.00
249 x2.x0.x5.x4.	s4nor	1.00
250 x2.x0.x6.x0.	sinv	1.00
251 x2.x0.x6.x1.	sinv	1.00
252 x2.x0.x6.x2.	sinv	1.00
253 x2.x0.x6.x3.	sinv	1.00
254 x2.x0.x6.x4.	s4nor	1.00
255 x2.x0.x7.x0.	sinv	1.00
256 x2.x0.x7.x1.	sinv	1.00
257 x2.x0.x7.x2.	sinv	1.00
258 x2.x0.x7.x3.	sinv	1.00
259 x2.x0.x7.x4.	s4nor	1.00
260 x2.x0.x8.x0.	sinv	1.00
261 x2.x0.x8.x1.	sinv	1.00
262 x2.x0.x8.x2.	sinv	1.00
263 x2.x0.x8.x3.	sinv	1.00
264 x2.x0.x8.x4.	s4nor	1.00
265 x2.x0.x9.x0.	sinv	1.00
266 x2.x0.x9.x1.	sinv	1.00
267 x2.x0.x9.x2.	sinv	1.00

268 x2.x0.x9.x3.	sinv	1.00
269 x2.x0.x9.x4.	s4nor	1.00
270 x2.x0.x10.x0.	sinv	1.00
271 x2.x0.x10.x1.	sinv	1.00
272 x2.x0.x10.x2.	sinv	1.00
273 x2.x0.x10.x3.	sinv	1.00
274 x2.x0.x10.x4.	s4nor	1.00
275 x2.x0.x11.x0.	sinv	1.00
276 x2.x0.x11.x1.	sinv	1.00
277 x2.x0.x11.x2.	sinv	1.00
278 x2.x0.x11.x3.	sinv	1.00
279 x2.x0.x11.x4.	s4nor	1.00
280 x2.x0.x12.x0.	sinv	1.00
281 x2.x0.x12.x1.	sinv	1.00
282 x2.x0.x12.x2.	sinv	1.00
283 x2.x0.x12.x3.	sinv	1.00
284 x2.x0.x12.x4.	s4nor	1.00
285 x1.x1.x3.x3.x0.	sinv	1.00
286 x1.x1.x3.x3.x1.	sinv	1.00
287 x1.x1.x3.x3.x2.	s2nor	1.00
288 x1.x1.x3.x3.x3.	sinv	1.00
289 x1.x1.x3.x4.x0.	sinv	1.00
290 x1.x1.x3.x4.x1.	sinv	1.00
291 x1.x1.x3.x4.x2.	s2nor	1.00
292 x1.x1.x3.x4.x3.	sinv	1.00
293 x1.x2.x13.x0.x0.	dinv	1.00
294 x1.x2.x13.x0.x1.	dinv	1.00
295 x1.x2.x13.x0.x2.	d2nor	1.00
296 x1.x2.x13.x0.x3.	dinv	1.00
297 x1.x2.x13.x1.x0.	dinv	1.00
298 x1.x2.x13.x1.x1.	dinv	1.00
299 x1.x2.x13.x1.x2.	dinv	1.00
300 x1.x2.x13.x1.x3.	d3nor	1.00
301 x1.x2.x13.x1.x4.	dinv	1.00
302 x1.x2.x13.x2.x0.	dinv	1.00
303 x1.x2.x13.x2.x1.	dinv	1.00
304 x1.x2.x13.x2.x2.	dinv	1.00
305 x1.x2.x13.x2.x3.	d3nor	1.00
306 x1.x2.x13.x2.x4.	dinv	1.00
307 x1.x2.x13.x3.x0.	dinv	1.00
308 x1.x2.x13.x3.x1.	dinv	1.00
309 x1.x2.x13.x3.x2.	dinv	1.00
310 x1.x2.x13.x3.x3.	d3nor	1.00
311 x1.x2.x13.x3.x4.	dinv	1.00
312 x1.x2.x13.x4.x0.	dinv	1.00
313 x1.x2.x13.x4.x1.	dinv	1.00
314 x1.x2.x13.x4.x2.	d2nor	1.00
315 x1.x2.x13.x4.x3.	dinv	1.00
316 x1.x2.x13.x5.x0.	dinv	1.00
317 x1.x2.x13.x5.x1.	dinv	1.00
318 x1.x2.x13.x5.x2.	dinv	1.00

319 x1.x2.x13.x5.x3.	d3nor	1.00
320 x1.x2.x13.x5.x4.	dinv	1.00
321 x1.x2.x14.x0.x0.	dinv	1.00
322 x1.x2.x14.x0.x1.	dinv	1.00
323 x1.x2.x14.x0.x2.	d2nor	1.00
324 x1.x2.x14.x0.x3.	dinv	1.00
325 x1.x2.x14.x1.x0.	dinv	1.00
326 x1.x2.x14.x1.x1.	dinv	1.00
327 x1.x2.x14.x1.x2.	dinv	1.00
328 x1.x2.x14.x1.x3.	d3nor	1.00
329 x1.x2.x14.x1.x4.	dinv	1.00
330 x1.x2.x14.x2.x0.	dinv	1.00
331 x1.x2.x14.x2.x1.	dinv	1.00
332 x1.x2.x14.x2.x2.	dinv	1.00
333 x1.x2.x14.x2.x3.	d3nor	1.00
334 x1.x2.x14.x2.x4.	dinv	1.00
335 x1.x2.x14.x3.x0.	dinv	1.00
336 x1.x2.x14.x3.x1.	dinv	1.00
337 x1.x2.x14.x3.x2.	dinv	1.00
338 x1.x2.x14.x3.x3.	d3nor	1.00
339 x1.x2.x14.x3.x4.	dinv	1.00
340 x1.x2.x14.x4.x0.	dinv	1.00
341 x1.x2.x14.x4.x1.	dinv	1.00
342 x1.x2.x14.x4.x2.	d2nor	1.00
343 x1.x2.x14.x4.x3.	dinv	1.00
344 x1.x2.x14.x5.x0.	dinv	1.00
345 x1.x2.x14.x5.x1.	dinv	1.00
346 x1.x2.x14.x5.x2.	dinv	1.00
347 x1.x2.x14.x5.x3.	d3nor	1.00
348 x1.x2.x14.x5.x4.	dinv	1.00
349 x1.x2.x15.x0.x0.	dinv	1.00
350 x1.x2.x15.x0.x1.	dinv	1.00
351 x1.x2.x15.x0.x2.	d2nor	1.00
352 x1.x2.x15.x0.x3.	dinv	1.00
353 x1.x2.x15.x1.x0.	dinv	1.00
354 x1.x2.x15.x1.x1.	dinv	1.00
355 x1.x2.x15.x1.x2.	dinv	1.00
356 x1.x2.x15.x1.x3.	d3nor	1.00
357 x1.x2.x15.x1.x4.	dinv	1.00
358 x1.x2.x15.x2.x0.	dinv	1.00
359 x1.x2.x15.x2.x1.	dinv	1.00
360 x1.x2.x15.x2.x2.	dinv	1.00
361 x1.x2.x15.x2.x3.	d3nor	1.00
362 x1.x2.x15.x2.x4.	dinv	1.00
363 x1.x2.x15.x3.x0.	dinv	1.00
364 x1.x2.x15.x3.x1.	dinv	1.00
365 x1.x2.x15.x3.x2.	dinv	1.00
366 x1.x2.x15.x3.x3.	d3nor	1.00
367 x1.x2.x15.x3.x4.	dinv	1.00
368 x1.x2.x15.x4.x0.	dinv	1.00
369 x1.x2.x15.x4.x1.	dinv	1.00

```
 370 x1.x2.x15.x4.x2.          d2nor     1.00
 371 x1.x2.x15.x4.x3.          dinv      1.00
 372 x1.x2.x15.x5.x0.          dinv      1.00
 373 x1.x2.x15.x5.x1.          dinv      1.00
 374 x1.x2.x15.x5.x2.          dinv      1.00
 375 x1.x2.x15.x5.x3.          d3nor     1.00
 376 x1.x2.x15.x5.x4.          dinv      1.00
 Opening plot unit= 15
file=ddrver1.pa0

** hspice file created for circuit decoddrver: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage      node   =voltage      node   =voltage


+ 0:1     =  2.0000   0:100   =  63.0000m  0:101   =  63.0000m
+ 0:102   =  63.0000m  0:104   =  31.9639m  0:105   = 720.7624m
+ 0:106   = 662.7461m  0:107   =  -1.2402   0:108   = 104.5425m
+ 0:120   =  52.0502m  0:121   =  52.0502m  0:122   =  52.0502m
+ 0:130   =   9.6973u  0:150   =  -1.2402   0:151   =  -1.2402
+ 0:152   =  -1.2402   0:153   =  -1.2402   0:154   =  -1.2402
+ 0:155   =  -1.2402   0:156   =  -1.2402   0:157   =  -1.2402
+ 0:160   =  31.9780m  0:161   =  30.9568m  0:170   =  -1.2402
+ 0:171   =  -1.2402   0:200   = 630.0000m  0:201   =  63.0000m
+ 0:202   =  63.0000m  0:777   =  -2.5000   0:888   =   2.0000
+ 1:10    = 633.6943m  1:11    =  11.3673m  1:12    = 726.7178m
+ 1:13    =  49.0605m  1:14    = 692.6305m  2:12    = 658.6414m
+ 2:13    = 658.6414m  2:14    = 658.6414m  2:15    =  53.9658m
+ 2:16    =  52.0088m  2:17    =  32.4497m  2:18    =  32.4488m
+ 2:19    =  52.0088m  2:20    =  32.4497m  2:21    =  32.4488m
+ 2:22    =  52.0088m  2:23    =  32.4497m  2:24    =  32.4488m
+ 2:25    =  17.6214u  2:26    =  17.6214u  2:27    =  17.6214u
+ 2:28    = 629.9885m  2:29    = 629.9926m  2:30    = 629.9967m
+ 2:31    =  48.9071u  2:33    = 630.0137m  3:30    =  31.9766m
+ 3:31    =  30.9553m  3:32    =  30.9553m  3:33    =  30.6021m
+ 3:34    =  30.9553m  3:35    =  30.6021m  3:36    =  30.6021m
+ 3:37    =  30.4227m  3:40    =  52.0136m  3:41    =  52.0137m
+ 3:42    =  52.0137m  3:43    =  52.0137m  3:44    =  52.0137m
+ 3:45    =  52.0137m  3:46    =  52.0137m  3:47    =  52.0137m
+ 3:48    = 652.8042m  3:50    =  31.7757m  4:8     =   1.2978
+ 5:9     =  53.4430m  6:9     =   1.3829   7:8     =  57.9851m
+ 8:9     =   1.3554   9:9     =  56.8501m  10:9    =   1.3747
+ 11:6    = 636.2190m  11:9    =  58.0085m  12:6    =   1.3578
+ 12:7    = 652.5236m  12:9    =  74.9274m  12:10   = 230.8765m
+ 12:11   =-504.6670m  12:12   =  -1.5552   12:13   =  -1.8701
+ 12:14   =  -2.1851   12:25   =   1.9694   13:6    =-379.5736m
+ 13:7    =  -1.0721   13:9    =   1.9993   13:10   =   1.5989
+ 13:11   = 851.7076m  13:12   =-546.5932m  13:13   =  -1.1977
+ 13:14   =  -1.8489   13:25   =  52.2021m  14:8    =  31.9352m
```

+ 14:9 = 692.6027m 14:10 = 10.5772m 14:11 = 10.5781m
+ 14:12 = 10.5790m 15:7 = 78.5842m 15:8 = 635.5417m
+ 15:9 = 607.4009m 15:10 = 58.7776m 16:11 = 624.0781m
+ 16:12 = 52.0115m 16:13 = 52.0127m 16:14 = 52.0115m
+ 16:15 = 52.0127m 16:16 = 32.4480m 16:17 = 52.0127m
+ 16:18 = 52.0127m 16:19 = 26.2560m 16:20 = 52.0509m
+ 16:21 = 52.0488m 16:22 = 52.0458m 16:23 = 52.0115m
+ 21:10 = 658.6317m 21:11 = 53.9637m 22:10 = 653.5035m
+ 22:11 = 653.6595m 23:10 = 52.0534m 23:11 = 653.6593m
+ 23:12 = 653.6593m 24:10 = 658.6317m 24:11 = 53.9637m
+ 25:10 = 653.5035m 25:11 = 653.6595m 26:10 = 52.0534m
+ 26:11 = 653.6593m 26:12 = 653.6593m 27:10 = 658.6317m
+ 27:11 = 53.9637m 28:10 = 653.5035m 28:11 = 653.6595m
+ 29:10 = 52.0534m 29:11 = 653.6593m 29:12 = 653.6593m
+ 30:7 = 658.5020m 31:7 = 658.5020m 32:7 = 658.5020m
+ 33:18 = 606.7231m 33:19 = 606.7231m 33:20 = 606.7231m
+ 35:9 = 690.8217m 35:10 = 19.5641m 35:11 = 690.8861m
+ 36:9 = 16.3431m 36:10 = 19.5641m 36:11 = 692.6857m
+ 37:10 = 658.7406m 37:11 = 52.2065m 38:10 = 658.7429m
+ 38:11 = 52.2065m 39:10 = 658.7429m 39:11 = 52.2065m
+ 40:10 = 658.7437m 40:11 = 52.2065m 41:10 = 658.7429m
+ 41:11 = 52.2065m 42:10 = 658.7437m 42:11 = 52.2065m
+ 43:10 = 658.7437m 43:11 = 52.2065m 44:10 = 658.7441m
+ 44:11 = 52.2065m 45:6 = 1.3554 45:7 = 650.5943m
+ 45:9 = 74.9593m 45:10 = 230.9021m 45:11 =-504.6416m
+ 45:12 = -1.5551 45:13 = -1.8701 45:14 = -2.1850
+ 45:25 = 1.9660 46:6 = 1.3554 46:7 = 650.5943m
+ 46:9 = 74.9593m 46:10 = 230.9021m 46:11 =-504.6416m
+ 46:12 = -1.5551 46:13 = -1.8701 46:14 = -2.1850
+ 46:25 = 1.9660 47:6 = 1.3554 47:7 = 650.5943m
+ 47:9 = 74.9593m 47:10 = 230.9021m 47:11 =-504.6416m
+ 47:12 = -1.5551 47:13 = -1.8701 47:14 = -2.1850
+ 47:25 = 1.9660 48:6 = 1.3554 48:7 = 650.5943m
+ 48:9 = 74.9593m 48:10 = 230.9021m 48:11 =-504.6416m
+ 48:12 = -1.5551 48:13 = -1.8701 48:14 = -2.1850
+ 48:25 = 1.9660 49:6 = 1.3554 49:7 = 650.5943m
+ 49:9 = 74.9593m 49:10 = 230.9021m 49:11 =-504.6416m
+ 49:12 = -1.5551 49:13 = -1.8701 49:14 = -2.1850
+ 49:25 = 1.9660 50:6 = 1.3554 50:7 = 650.5943m
+ 50:9 = 74.9593m 50:10 = 230.9021m 50:11 =-504.6416m
+ 50:12 = -1.5551 50:13 = -1.8701 50:14 = -2.1850
+ 50:25 = 1.9660 51:6 = 1.3554 51:7 = 650.5943m
+ 51:9 = 74.9593m 51:10 = 230.9021m 51:11 =-504.6416m
+ 51:12 = -1.5551 51:13 = -1.8701 51:14 = -2.1850
+ 51:25 = 1.9660 52:6 = 1.3554 52:7 = 650.5943m
+ 52:9 = 74.9593m 52:10 = 230.9021m 52:11 =-504.6416m
+ 52:12 = -1.5551 52:13 = -1.8701 52:14 = -2.1850
+ 52:25 = 1.9660 53:6 = 1.3578 53:7 = 652.5225m
+ 53:9 = 74.9274m 53:10 = 230.8765m 53:11 =-504.6670m
+ 53:12 = -1.5552 53:13 = -1.8701 53:14 = -2.1851
+ 53:25 = 1.9694 54:6 = 1.3579 54:7 = 652.6040m

+54:9 = 74.9262m 54:10 = 230.8755m 54:11 =-504.6679m
+54:12 = -1.5552 54:13 = -1.8701 54:14 = -2.1851
+54:25 = 1.9695 57:6 = 33.9796m 57:9 = 58.0085m
+60:9 = 1.3553 61:9 = 53.9676m 62:9 = 53.9669m
+63:9 = 53.9663m 64:8 = 56.8134m 65:9 = 678.3717m
+66:7 = 631.5538m 66:8 = 678.6259m 66:9 = 65.8780m
+69:7 = 622.4007m 69:8 = 652.8533m 69:9 = 652.6687m
+71:10 = 658.7911m 71:11 = 54.9626m 72:10 = 658.7914m
+72:11 = 53.9676m 73:6 = 658.5363m 74:10 = 658.7911m
+74:11 = 54.9626m 75:10 = 658.7914m 75:11 = 53.9676m
+76:10 = 653.6590m 76:11 = 53.9669m 76:12 = 653.6590m
+77:7 = 658.4423m 78:10 = 658.7914m 78:11 = 53.9669m
+79:10 = 658.7914m 79:11 = 53.9676m 80:10 = 651.6432m
+80:11 = 651.6432m 80:12 = 651.6432m 80:13 = 53.9663m
+81:10 = 54.9626m 81:11 = 658.7911m 82:8 = 658.3019m
+83:9 = 52.0506m 83:10 = 624.0440m 83:11 = 636.5449m
+83:12 = 636.5992m 84:9 = 52.0506m 84:10 = 624.0440m
+84:11 = 636.5449m 84:12 = 636.5992m 85:9 = 52.0506m
+85:10 = 624.0440m 85:11 = 636.5449m 85:12 = 636.5992m
+125:7 = 692.2401m 126:9 = 6.7626m 126:10 = 6.7626m
+126:11 = 6.7626m 126:12 = 692.6852m 127:9 = 690.8211m
+127:10 = 6.7626m 127:11 = 6.7626m 127:12 = 690.8856m
+128:9 = 6.7626m 128:10 = 690.8211m 128:11 = 6.7626m
+128:12 = 690.8856m 129:9 = 690.1607m 129:10 = 690.1607m
+129:11 = 6.7626m 129:12 = 690.2249m 130:9 = 6.7626m
+130:10 = 6.7626m 130:11 = 690.8211m 130:12 = 690.8856m
+131:9 = 690.1607m 131:10 = 6.7626m 131:11 = 690.1607m
+131:12 = 690.2249m 132:9 = 6.7626m 132:10 = 690.1607m
+132:11 = 690.1607m 132:12 = 690.2249m 133:9 = 689.8191m
+133:10 = 689.8191m 133:11 = 689.8191m 133:12 = 689.8833m
+134:9 = 1.3536 135:9 = 52.2065m 136:9 = 1.3539
+137:8 = 42.5789m 138:9 = 52.0282m 139:9 = 52.2065m
+140:9 = 1.3556 141:8 = 56.8403m 178:8 = 1.3147
+179:6 = 6.0274m 181:6 = 32.7632m 182:6 = 48.4090m
+183:6 = 36.3487m 184:6 = 58.4402m 186:6 = 8.5683m
+187:6 = 10.5824m 187:7 = 684.7784m 187:9 = 16.3579m
+188:6 = 692.7547m 188:7 = 32.0179m 188:9 = 16.3022m
+225:10 = 53.0867m 225:11 = 54.9689m 225:12 = 658.5204m
+226:10 = 651.5335m 226:11 = 651.6421m 226:12 = 651.5924m
+226:13 = 26.2529m 227:10 = 54.9689m 227:11 = 658.7304m
+227:12 = 53.0867m 227:13 = 51.9668m 228:10 = 53.0929m
+228:11 = 653.6561m 228:12 = 653.5469m 228:13 = 32.4387m
+229:10 = 54.9689m 229:11 = 53.9676m 229:12 = 640.4275m
+230:10 = 653.6591m 230:11 = 653.6591m 230:12 = 53.0929m
+230:13 = 32.4484m 231:10 = 53.0867m 231:11 = 54.9689m
+231:12 = 658.5204m 232:10 = 651.5335m 232:11 = 651.6421m
+232:12 = 651.5924m 232:13 = 26.2529m 233:10 = 54.9689m
+233:11 = 658.7304m 233:12 = 53.0867m 233:13 = 51.9668m
+234:10 = 53.0929m 234:11 = 653.6561m 234:12 = 653.5469m
+234:13 = 32.4387m 235:10 = 54.9689m 235:11 = 53.9669m
+235:12 = 640.4275m 236:10 = 653.6591m 236:11 = 653.6591m

```
+236:12    = 53.0929m 236:13    = 32.4484m 237:10    = 53.0867m
+237:11    = 54.9689m 237:12    = 658.5204m 238:10   = 651.5335m
+238:11    = 651.6421m 238:12   = 651.5924m 238:13   = 26.2529m
+239:10    = 54.9689m 239:11    = 658.7304m 239:12   = 53.0867m
+239:13    = 51.9668m 240:10    = 53.0929m 240:11    = 653.6561m
+240:12    = 653.5469m 240:13   = 32.4387m 241:10    = 54.9689m
+241:11    = 53.9663m 241:12    = 640.4275m 242:10   = 653.6591m
+242:11    = 653.6591m 242:12   = 53.0929m 242:13    = 32.4484m
+243:8     = 1.3540 244:9       = 56.7487m 245:9     = 58.9632m
+246:9     = 58.9632m 247:9     = 58.9632m 248:9     = 1.3556
+249:8     = 56.8380m 250:9     = 1.3536 251:9       = 58.9632m
+252:9     = 58.9632m 253:9     = 1.3539 254:8       = 42.5769m
+255:9     = 58.9632m 256:9     = 1.3536 257:9       = 58.9632m
+258:9     = 1.3539 259:8       = 42.5769m 260:9     = 1.3530
+261:9     = 1.3530 262:9       = 58.9632m 263:9     = 1.3532
+264:8     = 38.1889m 265:9     = 58.9632m 266:9     = 58.9632m
+267:9     = 1.3536 268:9       = 1.3539 269:8       = 42.5769m
+270:9     = 1.3530 271:9       = 58.9632m 272:9     = 1.3530
+273:9     = 1.3532 274:8       = 38.1889m 275:9     = 58.9632m
+276:9     = 1.3530 277:9       = 1.3530 278:9       = 1.3532
+279:8     = 38.1889m 280:9     = 1.3527 281:9       = 1.3527
+282:9     = 1.3527 283:9       = 1.3529 284:8       = 36.0549m
+285:9     = 52.0275m 286:9     = 53.9637m 287:8     = 1.3479
+288:9     = 55.0192m 289:9     = 52.0302m 290:9     = 1.3559
+291:8     = 56.8710m 292:9     = 1.2949


 Opening plot unit= 16
file=ddrver1.tr0

** hspice file created for circuit decoddrver: transient&power @ 25.0c
****** transient analysis          tnom= 25.000 temp= 25.000
******
 avgpwr       = -2.7061E-01  from= 0.0000E+00   to= 8.7000E-08
 vmax         = 5.9400E-01   at= 6.4802E-08
        from= 2.0000E-09   to= 8.8000E-08
 vmin         = 5.0752E-02   at= 7.2991E-08
        from= 2.0000E-09   to= 8.8000E-08
 tphl         = 1.2805E-09 targ= 1.4637E-08  trig= 1.3357E-08
 tplh         = 1.0183E-09 targ= 1.4375E-08  trig= 1.3357E-08
 trise        = 5.0463E-10 targ= 1.4790E-08  trig= 1.4286E-08
 tfall        = 2.3630E-10 targ= 1.4761E-08  trig= 1.4525E-08
 tdelay       = 1.2808E-09 targ= 1.4632E-08  trig= 1.3352E-08

      ***** job concluded
      total cpu time      4629.20 seconds
         job started at  18:44:12  4-feb93
         job ended  at  21:25:37  4-feb93
```

```
I am done with ddrver1.sp
Thu Feb  4 21:25:39 PST 1993
```

O. Listing File for OUTPUT Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        12:44:56  5-feb93  sun
** hspice file created for circuit output: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
*  d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
************************************************************
************************************************************
* hspice dcfl 2-input nor subcircuit
*           ina, inb, output, power, ground
.subckt d2nor    1   2    3     4     5
*  d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 5 5 jfet04 l=1.2 w=96.0
j2 3 2 5 5 jfet04 l=1.2 w=96.0
.ends  d2nor
************************************************************
************************************************************
* hspice dcfl 2-input demorgan and subcircuit
*           ina, inb, output, power, ground
.subckt dd2and   1   2    3     4     5
x0 1    10 4 5 dinv
x1 2    11 4 5 dinv
x2 10 11  3 4 5 d2nor
.ends  dd2and
************************************************************
************************************************************
* subcircuit dcfl 2-input or
*          ina   inb  output power ground
```

```
.subckt dd2or   1    2   3    4   5
*  ina inb out pwr gnd subname
x0  1  2  6  4  5  d2nor
x1  6     3  4  5  dinv
.ends  dd2or
*********************************************************
***********************************************************
* hspice dcfl 2-input real nand subcircuit
*            ina, inb, output, power, ground
.subckt d2nand   1   2   3     4    5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 6 5 jfet04 l=1.2 w=192.0
j2 6 2 5 5 jfet04 l=1.2 w=192.0
.ends d2nand
***********************************************************
***********************************************************
* subcircuit dcfl 4-input or
*          ina inb inc ind output power ground
.subckt dd4or  1  2  3  4   5    6   7
*  ina inb inc ind out pwr gnd subname
x0  1  2  3  4  8  6  7  d4nor
x1  8           5  6  7  dinv
.ends  dd4or
***********************************************************
***********************************************************
* hspice dcfl 4-input nor subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt d4nor    1  2  3  4    5     6   7
* d g s b
j0 6 5 5 7 jfet16 l=1.2 w=6.0
j1 5 1 7 7 jfet04 l=1.2 w=96.0
j2 5 2 7 7 jfet04 l=1.2 w=96.0
j3 5 3 7 7 jfet04 l=1.2 w=96.0
j4 5 4 7 7 jfet04 l=1.2 w=96.0
.ends  d4nor
***********************************************************
***********************************************************
* hspice dcfl 4-input demorgan  and subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt dd4and  1   2   3   4    5     6   7
x0 1          10 6 7 dinv
x1 2          11 6 7 dinv
x2 3          12 6 7 dinv
x3 4          13 6 7 dinv
x4 10 11 12 13  5  6 7 d4nor
.ends  dd4and
***********************************************************
***********************************************************
* subcircuit dcfl d-latch using generic gates
*            d  clk q  /q power ground
```

```
.subckt dlatch  1  2 3 4  5   6
*   ina  inb output  power ground subname
x0   1   2   8     5    6  d2nand
x1   1       7     5    6  dinv
x2   2   7   9     5    6  d2nand
x3   8   4   3     5    6  d2nand
x4   9   3   4     5    6  d2nand
.ends dlatch
*****************************************************
**********************************************************************
* subcircuit output
*           oddbio evenbio edummy odummy  rd  q  /q  pwr gnd
.subckt output   1     2     3     4   5  6 7   8  9
*  ina  inb  inc  ind  ine  inf
x0  1                   12  8   9    dinv
x1  2                   13  8   9    dinv
x2  3                   14  8   9    dinv
x3  4                   15  8   9    dinv
x4  1  4   13  14         17  8   9    dd4and
x5  12 15  2   3          30  8   9    dd4and
x6  1  15  2   3          31  8   9    dd4and
x7  1  4   2   14         20  8   9    dd4and
x8  17 30  31  20          21  8   9    dd4or
x9  3  4                 22  8   9    dd2or
x10 5  22                16  8   9    dd2and
x11 21 16              6 7    8   9    dlatch
.ends output
*****************************************************
*********************************************************
* hspice dcfl standard load subcircuit
*           input, output, power, ground
.subckt d2load  1     2     3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends   d2load
*********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*****************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc  2.0v  $ test load power supply

* temperature card
*.temp 85.0

* signal inputs

* next three lines used to provide test signal inputs for transient analysis
voddbio  100 0 pulse(0.63 0.063 8400ps 100ps 100ps 8200ps 16800ps)
vevenbio 101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
```

```
vedummy  102 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vodummy  103 0 pulse(0.63 0.063 4200ps 100ps 100ps 4000ps 8400ps)
vread    104 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)

* main circuit
x0 100 101 102 103 104 110 111  1   0  output   $ element under test
x1 110     120 888  0  d2load   $ test load
x2 111     121 888  0  d2load   $ test load

.ic v(110)=0.063 v(111)=0.63
* measurement parameters


* next two lines are used for transient analysis
.probe oddbio=v(100) evenbio=v(101) edummy=v(102)
+ odummy=v(103) mread=v(104) dox=v(110) /dox=v(111)
.probe tran p(vds) p(vload) power
.measure tran avgpwr avg p(vds)
* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(110) from=2ns to=35ns
.meas tran vmin min v(110) from=2ns to=35ns
.meas tran tphl trig v(103) val='(vmax-vmin)*.5' td=20ns
+ fall=1 targ v(110) val='(vmax-vmin)*.5' td=20ns fall=1
.meas tran tplh trig v(104) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(110) val='(vmax-vmin)*.5' td=15ns rise=1
.meas tran trise trig v(110) val='vmin+0.1*vmax' td=15ns
+ rise=1 targ v(110) val='0.9*vmax' rise=1
.meas tran tfall trig v(110) val='0.9*vmax' td=20ns
+ fall=1 targ v(110) val='vmin+0.1*vmax' fall=1
.meas tran tdelay trig v(104) val=.2835 td=15ns rise=1
+       targ v(110) val=.2835 td=15ns rise=1
.tran 500ps 35ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit output: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                    output      1.00
   2 x1.                    d2load      1.00
   3 x2.                    d2load      1.00
   4 x0.x0.                  dinv       1.00
   5 x0.x1.                  dinv       1.00
   6 x0.x2.                  dinv       1.00
   7 x0.x3.                  dinv       1.00
   8 x0.x4.                  dd4and      1.00
   9 x0.x5.                  dd4and      1.00
  10 x0.x6.                   dd4and     1.00
  11 x0.x7.                   dd4and     1.00
```

```
  12 x0.x8.              dd4or     1.00
  13 x0.x9.              dd2or     1.00
  14 x0.x10.             dd2and    1.00
  15 x0.x11.             dlatch    1.00
  16 x1.x0.              dinv      1.00
  17 x1.x1.              dinv      1.00
  18 x2.x0.              dinv      1.00
  19 x2.x1.              dinv      1.00
  20 x0.x4.x0.           dinv      1.00
  21 x0.x4.x1.           dinv      1.00
  22 x0.x4.x2.           dinv      1.00
  23 x0.x4.x3.           dinv      1.00
  24 x0.x4.x4.           d4nor     1.00
  25 x0.x5.x0.           dinv      1.00
  26 x0.x5.x1.           dinv      1.00
  27 x0.x5.x2.           dinv      1.00
  28 x0.x5.x3.           dinv      1.00
  29 x0.x5.x4.           d4nor     1.00
  30 x0.x6.x0.           dinv      1.00
  31 x0.x6.x1.           dinv      1.00
  32 x0.x6.x2.           dinv      1.00
  33 x0.x6.x3.           dinv      1.00
  34 x0.x6.x4.           d4nor     1.00
  35 x0.x7.x0.           dinv      1.00
  36 x0.x7.x1.           dinv      1.00
  37 x0.x7.x2.           dinv      1.00
  38 x0.x7.x3.           dinv      1.00
  39 x0.x7.x4.           d4nor     1.00
  40 x0.x8.x0.           d4nor     1.00
  41 x0.x8.x1.           dinv      1.00
  42 x0.x9.x0.           d2nor     1.00
  43 x0.x9.x1.           dinv      1.00
  44 x0.x10.x0.          dinv      1.00
  45 x0.x10.x1.          dinv      1.00
  46 x0.x10.x2.          d2nor     1.00
  47 x0.x11.x0.          d2nand    1.00
  48 x0.x11.x1.          dinv      1.00
  49 x0.x11.x2.          d2nand    1.00
  50 x0.x11.x3.          d2nand    1.00
  51 x0.x11.x4.          d2nand    1.00
 Opening plot unit= 15
file=output1.pa0

** hspice file created for circuit output: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage      node   =voltage      node   =voltage


+ 0:1      =  2.0000  0:100    = 630.0000m  0:101    =  63.0000m
```

```
+ 0:102   = 63.0000m 0:103   = 630.0000m 0:104   = 63.0000m
+ 0:110   = 63.0042m 0:111   = 630.0010m 0:120   = 1.9844
+ 0:121   = 53.9657m 0:888   = 2.0000  1:12    = 53.9658m
+ 1:13    = 658.6414m 1:14   = 636.5005m 1:15   = 53.9658m
+ 1:16    = 52.0112m 1:17    = 658.1907m 1:20   = 51.9209m
+ 1:21    = 658.6896m 1:22   = 658.6821m 1:30   = 23.1807m
+ 1:31    = 26.2239m 2:5     = 1.9844  3:5     = 53.9657m
+ 8:10    = 53.9658m 8:11    = 53.9658m 8:12   = 52.0534m
+ 8:13    = 53.0980m 9:10    = 650.4496m 9:11   = 650.4496m
+ 9:12    = 650.4105m 9:13   = 650.4105m 10:10   = 53.9658m
+10:11    = 651.5163m 10:12   = 651.4771m 10:13   = 651.4771m
+11:10    = 53.9658m 11:11   = 53.9658m 11:12   = 658.6124m
+11:13    = 53.0980m 12:8    = 51.9626m 13:6    = 53.8908m
+14:10    = 658.6322m 14:11   = 52.0544m 15:7    = 52.0545m
+15:8     = 668.0491m 15:9    = 1.2457  47:6    = 532.3943m
+49:6     = 75.0262m 50:6     = 40.4805m 51:6    = 638.8192m


 Opening plot unit= 16
file=output1.tr0

** hspice file created for circuit output: transient&power @ 25.0c
****** transient analysis          tnom= 25.000 temp= 25.000
******
 avgpwr       = -8.1584E-02 from= 0.0000E+00   to= 3.5000E-08
 vmax         = 6.3253E-01   at= 3.5000E-08
        from= 2.0000E-09   to= 3.5000E-08
 vmin         = 3.9594E-02   at= 1.7238E-08
        from= 2.0000E-09   to= 3.5000E-08
 tphl         = 1.0443E-09 targ= 2.2103E-08  trig= 2.1059E-08
 tplh         = 5.8453E-10 targ= 1.7426E-08  trig= 1.6841E-08
 trise        = 5.4070E-10 targ= 1.7847E-08  trig= 1.7307E-08
 tfall        = 3.8850E-10 targ= 2.2263E-08  trig= 2.1875E-08
 tdelay       = 5.7533E-10 targ= 1.7414E-08  trig= 1.6839E-08

      ***** job concluded
      total cpu time       66.75 seconds
         job started at  12:44:56  5-feb93
         job ended   at  12:48:21  5-feb93


I am done with output1.sp
Fri Feb  5 12:48:23 PST 1993
```

P. Listing File for WRITEP Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
```

```
setting user memory from environment var  to  250000 words. (  2000000 bytes)

******    h s p i c e   9007d        14: 6:57  7-feb93  sun
** hspice file created for circuit writep: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
**********************************************************
**********************************************************
* subcircuit operation priority circuit
*the call      14   60 61   17   18   1     0 writep
******        mref write read mwrite mread power ground
.subckt  writep 1   2   3    4    5    6     7
* write priority logic 04 august 1992
x0 1        8 6 7 dinv
x1 2        9 6 7 dinv
x2 2  8     4 6 7 dd2and
x3 3  9  8   5 6 7 dd3and
.ends   writep
**********************************************************
**********************************************************
* hspice dcfl 2-input demorgan and subcircuit
*             ina, inb, output, power, ground
.subckt dd2and   1   2    3     4     5
x0 1     10 4 5 dinv
x1 2     11 4 5 dinv
x2 10 11  3 4 5 d2nor
.ends   dd2and
**********************************************************
**********************************************************
* hspice dcfl 2-input nor subcircuit
*             ina, inb, output, power, ground
.subckt d2nor     1   2    3     4     5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 5 5 jfet04 l=1.2 w=96.0
j2 3 2 5 5 jfet04 l=1.2 w=96.0
.ends   d2nor
**********************************************************
**********************************************************
* hspice dcfl inverter subcircuit
*           input, output, power, ground
.subckt dinv   1     2     3     4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
**********************************************************
```

```
*************************************************************
* hspice dcfl 3-input nor subcircuit
*            ina, inb, inc,  output, power, ground
.subckt d3nor     1  2  3     4    5     6
* d g s b
j0 5 4 4 6 jfet16 l=1.2 w=6.0
j1 4 1 6 6 jfet04 l=1.2 w=96.0
j2 4 2 6 6 jfet04 l=1.2 w=96.0
j3 4 3 6 6 jfet04 l=1.2 w=96.0
.ends  d3nor
*************************************************************
*************************************************************
* hspice dcfl 3-input demorgan and subcircuit
*            ina, inb, inc,  output, power, ground
.subckt dd3and   1  2  3     4    5     6
x0 1       10 5 6 dinv
x1 2       11 5 6 dinv
x2 3       12 5 6 dinv
x3 10 11 12  4 5 6 d3nor
.ends  dd3and
*************************************************************
*************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2    3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
*************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*************************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs

* next three lines used to provide test signal inputs for transient analysis
vread 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vwrite 101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
vmrefresh 102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)


* main circuit
x0 102 101 100 104 103  1   0  writep    $ element under test
x1 103        107 888  0  d2load    $ test load
x2 104        108 888  0  d2load    $ test load
```

```
* measurement parameters


* next two lines are used for transient analysis
.probe read=v(100) write=v(101) mrefresh=v(102) mread=v(103)
+ mwrite=v(104)
.probe tran p(vds) p(vload) power

.measure tran avgpwr avg p(vds)
* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(103) from=2ns to=42ns
.meas tran vmin min v(103) from=2ns to=42ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=2ns
+ fall=1 targ v(103) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(103) val='(vmax-vmin)*.5' td=2ns rise=1
.meas tran trise trig v(103) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(103) val='0.9*vmax' rise=1
.meas tran tfall trig v(103) val='0.9*vmax' td=2ns
+ fall=1 targ v(103) val='vmin+0.1*vmax' fall=1
.meas tran tdelay trig v(100) val=.2835 td=2ns rise=1
+       targ v(103) val=.2835 rise=1
.tran 100ps 42ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit writep: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname             definition  multiplier
   0 main circuit
   1 x0.                    writep      1.00
   2 x1.                    d2load      1.00
   3 x2.                    d2load      1.00
   4 x0.x0.                  dinv       1.00
   5 x0.x1.                  dinv       1.00
   6 x0.x2.                  dd2and      1.00
   7 x0.x3.                  dd3and      1.00
   8 x1.x0.                  dinv       1.00
   9 x1.x1.                  dinv       1.00
  10 x2.x0.                   dinv      1.00
  11 x2.x1.                   dinv      1.00
  12 x0.x2.x0.                 dinv      1.00
  13 x0.x2.x1.                 dinv      1.00
  14 x0.x2.x2.                 d2nor      1.00
  15 x0.x3.x0.                 dinv      1.00
  16 x0.x3.x1.                 dinv      1.00
  17 x0.x3.x2.                 dinv      1.00
  18 x0.x3.x3.                 d3nor      1.00
 Opening plot unit= 15
```

```
file=writep1.pa0

** hspice file created for circuit writep: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage     node   =voltage     node   =voltage


+ 0:1     =  2.0000  0:100    =  63.0000m 0:101    =  63.0000m
+ 0:102    =  63.0000m 0:103    =  51.9677m 0:104    =  52.0099m
+ 0:107    =  1.9872  0:108    =  1.9872  0:888    =  2.0000
+ 1:8      = 636.5005m 1:9      = 658.6414m 2:5      =  1.9872
+ 3:5      =  1.9872  6:10     = 658.6319m 6:11     =  53.0980m
+ 7:10     = 658.6227m 7:11     =  52.0534m 7:12     =  53.0980m



 Opening plot unit= 16
file=writep1.tr0

** hspice file created for circuit writep: transient&power @ 25.0c
****** transient analysis           tnom= 25.000 temp= 25.000
******
 avgpwr       = -2.0557E-02 from= 0.0000E+00    to= 4.2000E-08
 vmax         =  6.3760E-01   at= 3.8350E-08
        from= 2.0000E-09   to= 4.2000E-08
 vmin         =  2.0039E-02   at= 3.3675E-08
        from= 2.0000E-09   to= 4.2000E-08
 tphl         =  1.2793E-10 targ= 8.4846E-09  trig= 8.3567E-09
 tplh         =  1.4321E-10 targ= 4.3866E-09  trig= 4.2433E-09
 trise        =  3.9394E-10 targ= 4.6674E-09  trig= 4.2735E-09
 tfall        =  1.6279E-10 targ= 8.5831E-09  trig= 8.4203E-09
 tdelay       =  1.3022E-10 targ= 4.3691E-09  trig= 4.2389E-09

      ***** job concluded
      total cpu time       25.91 seconds
         job started at  14: 6:57   7-feb93
         job ended   at  14: 8:23   7-feb93


I am done with writep1.sp
Sun Feb  7 14:08:24 PST 1993
```

Q. Listing File for MBSY Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)
```

```
******    h s p i c e   9007d        20:45:58  7-feb93  sun
** hspice file created for circuit mbsy: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
*  d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
************************************************************
************************************************************
* hspice dcfl 3-input nor subcircuit
*             ina, inb, inc,  output, power, ground
.subckt d3nor    1  2   3    4    5    6
*  d g s b
j0 5 4 4 6 jfet16 l=1.2 w=6.0
j1 4 1 6 6 jfet04 l=1.2 w=96.0
j2 4 2 6 6 jfet04 l=1.2 w=96.0
j3 4 3 6 6 jfet04 l=1.2 w=96.0
.ends  d3nor
************************************************************
************************************************************
* subcircuit dcfl 3-input or
*           ina   inb   inc  output power ground
.subckt dd3or   1    2    3    4    5    6
*  ina inb inc out pwr gnd subname
x0  1  2  3  7  5  6  d3nor
x1  7        4  5  6  dinv
.ends  dd3or
************************************************************
************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2    3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
************************************************************
* power supplies
```

```
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs

* next three lines used to provide test signal inputs for transient analysis
vmread 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vmwrite 101 0 pulse(0.063 0.63 8400ps 100ps 100ps 8200ps 16800ps)
vmrefresh 102 0 pulse(0.063 0.63 16800ps 100ps 100ps 16600ps 33600ps)


* main circuit
x0 100 101 102 103  1   0  dd3or    $ element under test
x1 103        107 888  0  d2load    $ test load
x2 104        108 888  0  d2load    $ test load

* measurement parameters


* next two lines are used for transient analysis
.probe mread=v(100) mwrite=v(101) mrefresh=v(102) mbsy=v(103)
.probe tran p(vds) p(vload) power

.measure tran avgpwr avg p(vds)
* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(103) from=2ns to=42ns
.meas tran vmin min v(103) from=2ns to=42ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=32ns
+ fall=1 targ v(103) val='(vmax-vmin)*.5' td=32ns fall=1
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(103) val='(vmax-vmin)*.5' td=2ns rise=1
.meas tran trise trig v(103) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(103) val='0.9*vmax' rise=1
.meas tran tfall trig v(103) val='0.9*vmax' td=32ns
+ fall=1 targ v(103) val='vmin+0.1*vmax' fall=1
.meas tran tdelay trig v(100) val=.2835 td=2ns rise=1
+       targ v(103) val=.2835 rise=1
.tran 100ps 42ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit mbsy: transient&power @ 25.0c
******  circuit name directory
******
circuit number to circuit name directory
number  circuitname             definition  multiplier
   0 main circuit
   1 x0.                    dd3or       1.00
   2 x1.                    d2load      1.00
```

```
  3 x2.                  d2load     1.00
  4 x0.x0.               d3nor      1.00
  5 x0.x1.               dinv       1.00
  6 x1.x0.               dinv       1.00
  7 x1.x1.               dinv       1.00
  8 x2.x0.               dinv       1.00
  9 x2.x1.               dinv       1.00
 Opening plot unit= 15
file=mbsy1.pa0

** hspice file created for circuit mbsy: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
  node   =voltage     node   =voltage     node   =voltage


+0:1     =  2.0000  0:100    =  63.0000m 0:101    =  63.0000m
+0:102   =  63.0000m 0:103   =  52.0444m 0:104    =  46.8784m
+0:107   =  1.9872  0:108    =  1.9883  0:888    =  2.0000
+1:7     = 658.2372m 2:5     =  1.9872  3:5      =  1.9883



 Opening plot unit= 16
file=mbsy1.tr0

** hspice file created for circuit mbsy: transient&power @ 25.0c
****** transient analysis            tnom= 25.000 temp= 25.000
******
 avgpwr       = -4.5233E-03  from= 0.0000E+00    to= 4.2000E-08
 vmax         = 6.4100E-01   at= 3.3625E-08
        from= 2.0000E-09   to= 4.2000E-08
 vmin         = 5.1475E-02   at= 3.4125E-08
        from= 2.0000E-09   to= 4.2000E-08
 tphl         = 2.2152E-10  targ= 3.3781E-08  trig= 3.3559E-08
 tplh         = 1.1997E-10  targ= 4.3608E-09  trig= 4.2409E-09
 trise        = 3.4966E-10  targ= 4.6355E-09  trig= 4.2859E-09
 tfall        = 1.3832E-10  targ= 3.3841E-08  trig= 3.3703E-08
 tdelay       = 1.1568E-10  targ= 4.3546E-09  trig= 4.2389E-09

      ***** job concluded
      total cpu time       16.16 seconds
         job started at  20:45:58  7-feb93
         job ended   at  20:46:48  7-feb93


I am done with mbsy1.sp
Sun Feb  7 20:46:50 PST 1993
```

R. Listing File for DRDY Transient Analysis @ 25.0C

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to   250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        5:51:54  8-feb93  sun
** hspice file created for circuit drdy: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
**********************************************************
**********************************************************
* hspice dcfl 2-input demorgan and subcircuit
*            ina, inb, output, power, ground
.subckt dd2and   1   2    3     4     5
x0 1    10 4 5 dinv
x1 2    11 4 5 dinv
x2 10 11  3 4 5 d2nor
.ends   dd2and
**********************************************************
**********************************************************
* hspice dcfl 2-input nor subcircuit
*            ina, inb, output, power, ground
.subckt d2nor     1   2    3     4     5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 5 5 jfet04 l=1.2 w=96.0
j2 3 2 5 5 jfet04 l=1.2 w=96.0
.ends   d2nor
**********************************************************
**********************************************************
* subcircuit dcfl 2-input or
*           ina   inb  output power ground
.subckt dd2or   1     2    3     4     5
*   ina inb out pwr gnd subname
x0   1   2   6   4   5  d2nor
x1   6      3   4   5  dinv
.ends   dd2or
**********************************************************
**********************************************************
* hspice dcfl inverter subcircuit
*           input, output, power, ground
.subckt dinv    1     2    3     4
* d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
```

```
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
*************************************************************
*************************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load 1     2    3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
*************************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*************************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs

* next three lines used to provide test signal inputs for transient analysis
vread 100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vedum 101 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vodum 102 0 pulse(0.63 0.063 4200ps 100ps 100ps 4000ps 8400ps)


* main circuit
**********************
*  data ready (drdy) circuit
x0 101 102 104 1 0 dd2or       $ element under test
x1 104 100 105 1 0 dd2and      $ element under test
x2 105    103 1 0 dinv         $ element under test
*************************************************
x3 103    107 888  0  d2load    $ test load

* measurement parameters


* next two lines are used for transient analysis
.probe mread=v(100) edum=v(101) odum=v(102) drdy=v(103)
.probe tran p(vds) p(vload) power

.measure tran avgpwr avg p(vds)
* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(103) from=2ns to=42ns
.meas tran vmin min v(103) from=2ns to=42ns
.meas tran tphl trig v(100) val='(vmax-vmin)*.5' td=2ns
+ rise=1 targ v(103) val='(vmax-vmin)*.5' td=2ns fall=1
```

```
.meas tran tplh trig v(100) val='(vmax-vmin)*.5' td=2ns
+ fall=1 targ v(103) val='(vmax-vmin)*.5' td=2ns rise=1
.meas tran trise trig v(103) val='vmin+0.1*vmax' td=2ns
+ rise=1 targ v(103) val='0.9*vmax' rise=1
.meas tran tfall trig v(103) val='0.9*vmax' td=2ns
+ fall=2 targ v(103) val='vmin+0.1*vmax' fall=2
.meas tran tdelay trig v(100) val=.2835 td=2ns fall=1
+       targ v(103) val=.2835 rise=1
.tran 100ps 42ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit drdy: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                    dd2or       1.00
   2 x1.                    dd2and      1.00
   3 x2.                    dinv        1.00
   4 x3.                    d2load      1.00
   5 x0.x0.                  d2nor       1.00
   6 x0.x1.                  dinv        1.00
   7 x1.x0.                  dinv        1.00
   8 x1.x1.                  dinv        1.00
   9 x1.x2.                  d2nor       1.00
  10 x3.x0.                   dinv        1.00
  11 x3.x1.                   dinv        1.00
 Opening plot unit= 15
file=drdy1.pa0

** hspice file created for circuit drdy: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is     0.
   node   =voltage      node   =voltage      node   =voltage


+ 0:1     =  2.0000  0:100    =  63.0000m  0:101    =  63.0000m
+ 0:102    = 630.0000m  0:103    = 636.5447m  0:104    = 658.6821m
+ 0:105    =  52.0112m  0:107    =  53.0930m  0:888    =  2.0000
+ 1:6      =  53.8908m  2:10     =  52.0544m  2:11     = 658.6322m
+ 4:5      =  53.0930m



 Opening plot unit= 16
file=drdy1.tr0

** hspice file created for circuit drdy: transient&power @ 25.0c
****** transient analysis             tnom= 25.000 temp= 25.000
```

```
******
 avgpwr       = -1.3732E-02 from= 0.0000E+00   to= 4.2000E-08
 vmax         = 6.4321E-01   at= 1.7342E-08
        from= 2.0000E-09   to= 4.2000E-08
 vmin         = 5.0553E-02   at= 4.7000E-09
        from= 2.0000E-09   to= 4.2000E-08
 tphl         = 2.0124E-10 targ= 4.4424E-09  trig= 4.2412E-09
 tplh         = 1.7905E-10 targ= 8.5379E-09  trig= 8.3588E-09
 trise        = 3.5592E-10 targ= 8.8165E-09  trig= 8.4606E-09
 tfall        = 1.3901E-10 targ= 1.2913E-08  trig= 1.2774E-08
 tdelay       = 1.7104E-10 targ= 8.5321E-09  trig= 8.3611E-09

      ***** job concluded
      total cpu time       20.37 seconds
         job started at  5:51:54  8-feb93
         job ended  at  5:52:57  8-feb93


I am done with drdy1.sp
Mon Feb  8 05:52:59 PST 1993
```

S. **Listing File for WLOGIC Transient Analysis @ 25.0C**

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
setting user memory from environment var  to  250000 words. (  2000000 bytes)

 ******    h s p i c e   9007d        9:45:34  8-feb93  sun
** hspice file created for circuit wlogic: transient&power @ 25.0c
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
** standard 16-to-1 ratio of pull-down-to-pullup is used
************************************************************
************************************************************
* hspice dcfl inverter subcircuit
*          input, output, power, ground
.subckt dinv   1    2    3    4
*  d g s b
j0 3 2 2 4 jfet16 l=1.2 w=6.0
j1 2 1 4 4 jfet04 l=1.2 w=96.0
.ends dinv
************************************************************
************************************************************
* hspice dcfl 4-input nor subcircuit
*            ina, inb, inc, ind, output, power, ground
.subckt d4nor    1  2  3  4    5    6   7
```

```
* d g s b
j0 6 5 5 7 jfet16 l=1.2 w=6.0
j1 5 1 7 7 jfet04 l=1.2 w=96.0
j2 5 2 7 7 jfet04 l=1.2 w=96.0
j3 5 3 7 7 jfet04 l=1.2 w=96.0
j4 5 4 7 7 jfet04 l=1.2 w=96.0
.ends  d4nor
*************************************************************
*************************************************************
* hspice dcfl 4-input demorgan  and subcircuit
*           ina, inb, inc, ind, output, power, ground
.subckt dd4and  1   2   3   4    5     6    7
x0 1         10 6 7 dinv
x1 2         11 6 7 dinv
x2 3         12 6 7 dinv
x3 4         13 6 7 dinv
x4 10 11 12 13  5  6 7 d4nor
.ends  dd4and
*************************************************************
*************************************************************
* hspice dcfl 2-input real nand subcircuit
*           ina, inb, output, power, ground
.subckt d2nand   1   2   3    4    5
* d g s b
j0 4 3 3 5 jfet16 l=1.2 w=6.0
j1 3 1 6 5 jfet04 l=1.2 w=192.0
j2 6 2 5 5 jfet04 l=1.2 w=192.0
.ends d2nand
*************************************************************
*************************************************************
* subcircuit dcfl d-latch using generic gates
*           d  clk q  /q power ground
.subckt dlatch  1  2 3 4   5    6
*   ina  inb output  power ground subname
x0   1   2   8    5    6  d2nand
x1   1       7    5    6  dinv
x2   2   7   9    5    6  d2nand
x3   8   4   3    5    6  d2nand
x4   9   3   4    5    6  d2nand
.ends dlatch
*************************************************************
*************************************************************
* hspice d mesfet load subcircuit
*           input,  power, ground
.subckt dm10load  1   3    4
j0 3 1 4 4 jfet16 l=1.2 w= 10.0
j1 3 1 4 4 jfet16 l=1.2 w= 10.0
j2 3 1 4 4 jfet16 l=1.2 w= 10.0
j3 3 1 4 4 jfet16 l=1.2 w= 10.0
j4 3 1 4 4 jfet16 l=1.2 w= 10.0
j5 3 1 4 4 jfet16 l=1.2 w= 10.0
```

```
j6 3 1 4 4 jfet16 l=1.2 w= 10.0
j7 3 1 4 4 jfet16 l=1.2 w= 10.0
j8 3 1 4 4 jfet16 l=1.2 w= 10.0
j9 3 1 4 4 jfet16 l=1.2 w= 10.0
.ends  dm10load
*********************************************************
*********************************************************
* hspice d mesfet load subcircuit
*          input, power, ground
.subckt dm4load  1   3     4
j0 3 1 4 4 jfet16 l=1.2 w= 10.0
j1 3 1 4 4 jfet16 l=1.2 w= 10.0
j2 3 1 4 4 jfet16 l=1.2 w= 10.0
j3 3 1 4 4 jfet16 l=1.2 w= 10.0
.ends  dm4load
*********************************************************
*********************************************************
* subcircuit level-shifter to drive dfets
* use hspice diode models for backconnected mesfets
*         input output vds vss
.subckt lvl  1    2    3  4
*   d  g    s   b
x0   1  25   3   0   dinv
j1   3  25   6   4   jfet04 l=1.2 w=20.0
j2   7  6    7   4   dio16  l=1.2 w=4.0
j3   7  4    4   4   jfet20 l=3.0 w=3.0
j4   3  9    9   4   jfet16 l=1.2 w=3.0
j5   9  7    0   4   jfet16 l=1.2 w=10.0
j6   3  9    10  4   jfet16 l=1.2 w=20.0
j7   11 10   11  4   dio16  l=1.2 w=20.0
j8   2  11   2   4   dio16  l=1.2 w=20.0
j9   2  4    4   4   jfet16 l=1.2 w=12.0
j10  12 2    12  4   dio16  l=1.2 w=10.0
j11  13 12   13  4   dio16  l=1.2 w=10.0
j12  14 13   14  4   dio16  l=1.2 w=10.0
j13  4  14   4   4   dio16  l=1.2 w=10.0
.ends lvl
*********************************************************
*********************************************************
* subcircuit write logic in hspice
* epu=even pull up -- bring in a0 for even/odd & writing
*          data das a0 w clk epu epd opu opd power grnd vss
.subckt wlogic  1  2 3 4 5  6  7  8  9 10    11  12
x0  1  2        14  15   10 11 dlatch
x1  3           13       10 11 dinv
x2  13 14 4  5 16        10 11 dd4and
x3  13 15 4  5 7         10 11 dd4and
x4  4  3  14 5 17        10 11 dd4and
x5  3  15 4  5 9         10 11 dd4and
x6  16          6        10 12 lvl
x7  17          8        10 12 lvl
```

```
.ends  wlogic
*********************************************************
*********************************************************
* hspice dcfl standard load subcircuit
*          input, output, power, ground
.subckt d2load  1     2    3     4
x0 1 5 3 4 dinv
x1 1 2 3 4 dinv
.ends  d2load
*********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
*********************************************************
* power supplies
vds   1  0  dc  2.0v  $ element under test power supply
vss   777 0  dc -2.5v  $ test load negative power supply
vload 888 0  dc 2.0v   $ test load power supply

* temperature card
*.temp 85.0

* signal inputs

* next three lines used to provide test signal inputs for transient analysis
va0    100 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vmwrite 101 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vph2   102 0 pulse(0.063 0.63 4200ps 100ps 100ps 4000ps 8400ps)
vdx    103 0 pulse(0.63 0.063 8400ps 100ps 100ps 8200ps 16800ps)
vdas   104 0 0.63v

* main circuit
*  dx   das a0  mw  ph2 expu expd oxpu oxpd power grnd vss
x0 103  104 100 101 102 110  111  112  113   1   0    777 wlogic
x1 110                              888  0  dm10load
x2 111                         121    888  0  d2load
x3 112                              888  0  dm10load
x4 113                         123    888  0  d2load

* measurement parameters


* next two lines are used for transient analysis
.probe dx=v(103) das=v(104) a0=v(100) mwrite=v(101) ph2=v(102)
+ expu=v(110)  expd=v(111) oxpu=v(112) oxpd=v(113)
.probe tran p(vds) p(vss) power
.measure tran avgpwr avg p(vds)

* next 8 lines calculate vmax vmin trise tfall and tdelay :transient analysis
.meas tran vmax max v(113) from=2ns to=20ns
.meas tran vmin min v(113) from=2ns to=20ns
.meas tran vmin2 find v(113) at=10ns
```

```
.meas tran tphl trig v(102) val='(vmax-vmin)*.5' td=16ns
+ fall=1 targ v(113) val='(vmax-vmin)*.5' td=2ns fall=1
.meas tran tplh trig v(102) val='(vmax-vmin)*.5' td=12ns
+ rise=1 targ v(113) val='(vmax-vmin)*.5' td=2ns rise=1
.meas tran trise trig v(113) val='vmin+0.1*vmax' td=12ns
+ rise=1 targ v(113) val='0.9*vmax' td=12ns rise=1
.meas tran tfall trig v(113) val='0.9*vmax' td=2ns
+ fall=1 targ v(113) val='vmin2+0.1*vmax' fall=1
.meas tran tdelay trig v(102) val=.2835 td=2ns rise=1
+      targ v(112) val=-0.600 rise=1
.tran 250ps 20ns
.options scale=1e-06 brief=0 nopage measout post probe
.end
** hspice file created for circuit wlogic: transient&power @ 25.0c
****** circuit name directory
******
circuit number to circuit name directory
number  circuitname              definition  multiplier
   0 main circuit
   1 x0.                    wlogic      1.00
   2 x1.                    dm10load    1.00
   3 x2.                    d2load      1.00
   4 x3.                    dm10load    1.00
   5 x4.                    d2load      1.00
   6 x0.x0.                  dlatch      1.00
   7 x0.x1.                  dinv        1.00
   8 x0.x2.                  dd4and      1.00
   9 x0.x3.                  dd4and      1.00
  10 x0.x4.                   dd4and      1.00
  11 x0.x5.                   dd4and      1.00
  12 x0.x6.                   lvl         1.00
  13 x0.x7.                   lvl         1.00
  14 x2.x0.                   dinv        1.00
  15 x2.x1.                   dinv        1.00
  16 x4.x0.                   dinv        1.00
  17 x4.x1.                   dinv        1.00
  18 x0.x0.x0.                 d2nand      1.00
  19 x0.x0.x1.                 dinv        1.00
  20 x0.x0.x2.                 d2nand      1.00
  21 x0.x0.x3.                 d2nand      1.00
  22 x0.x0.x4.                 d2nand      1.00
  23 x0.x2.x0.                 dinv        1.00
  24 x0.x2.x1.                 dinv        1.00
  25 x0.x2.x2.                 dinv        1.00
  26 x0.x2.x3.                 dinv        1.00
  27 x0.x2.x4.                 d4nor       1.00
  28 x0.x3.x0.                 dinv        1.00
  29 x0.x3.x1.                 dinv        1.00
  30 x0.x3.x2.                 dinv        1.00
  31 x0.x3.x3.                 dinv        1.00
  32 x0.x3.x4.                 d4nor       1.00
```

```
  33 x0.x4.x0.              dinv      1.00
  34 x0.x4.x1.              dinv      1.00
  35 x0.x4.x2.              dinv      1.00
  36 x0.x4.x3.              dinv      1.00
  37 x0.x4.x4.              d4nor     1.00
  38 x0.x5.x0.              dinv      1.00
  39 x0.x5.x1.              dinv      1.00
  40 x0.x5.x2.              dinv      1.00
  41 x0.x5.x3.              dinv      1.00
  42 x0.x5.x4.              d4nor     1.00
  43 x0.x6.x0.              dinv      1.00
  44 x0.x7.x0.              dinv      1.00
 Opening plot unit= 15
file=wlogic1.pa0

** hspice file created for circuit wlogic: transient&power @ 25.0c
****** operating point information     tnom= 25.000 temp= 25.000
******
***** operating point status is voltage   simulation time is    0.
   node   =voltage     node   =voltage     node   =voltage


+ 0:1     =  2.0000  0:100    = 63.0000m 0:101    = 63.0000m
+ 0:102   = 63.0000m 0:103    = 630.0000m 0:104   = 630.0000m
+ 0:110   = -1.2402  0:111    = 26.2129m 0:112    = -1.2402
+ 0:113   = 23.1689m 0:121    =  1.9920  0:123    =  1.9925
+ 0:777   = -2.5000  0:888    =  2.0000  1:13     = 636.5005m
+ 1:14    = 614.6238m 1:15    = 81.2740m 1:16     = 32.4038m
+ 1:17    = 26.2202m 3:5      =  1.9920  5:5      =  1.9925
+ 6:7     = 53.9658m 6:8      = 66.4030m 6:9      = 681.1090m
+ 8:10    = 53.0980m 8:11     = 56.9463m 8:12     = 653.4893m
+ 8:13    = 653.4893m 9:10    = 53.0980m 9:11     = 651.3630m
+ 9:12    = 651.4733m 9:13    = 651.4733m 10:10   = 651.4758m
+10:11    = 651.4758m 10:12   = 56.9463m 10:13    = 651.4758m
+11:10    = 650.4062m 11:11   = 650.2962m 11:12   = 650.4062m
+11:13    = 650.4062m 12:6    =  1.3577  12:7     = 652.4880m
+12:9     =  74.9279m 12:10   = 230.8769m 12:11   =-504.6665m
+12:12    = -1.5552  12:13    = -1.8701  12:14    = -2.1851
+12:25    =  1.9693  13:6     =  1.3583  13:7     = 652.9635m
+13:9     =  74.9209m 13:10   = 230.8713m 13:11   =-504.6721m
+13:12    = -1.5552  13:13    = -1.8701  13:14    = -2.1851
+13:25    =  1.9702  18:6     = 35.5694m 20:6     = 508.1467m
+21:6     = 34.2476m 22:6     = 51.0945m



 Opening plot unit= 16
file=wlogic1.tr0

** hspice file created for circuit wlogic: transient&power @ 25.0c
****** transient analysis          tnom= 25.000 temp= 25.000
```

```
******
 avgpwr       = -7.1033E-02 from= 0.0000E+00   to= 2.0000E-08
 vmax         = 6.3964E-01   at= 1.6750E-08
        from= 2.0000E-09   to= 2.0000E-08
 vmin         = -6.6850E-02   at= 1.2700E-08
        from= 2.0000E-09   to= 2.0000E-08
 vmin2        = 2.6230E-02
 tphl         = 8.5134E-11 targ= 1.6834E-08  trig= 1.6749E-08
 tplh         = 2.4188E-10 targ= 1.2893E-08  trig= 1.2651E-08
 trise        = 4.2605E-10 targ= 1.3156E-08  trig= 1.2730E-08
 tfall        = 8.8808E-11 targ= 1.6880E-08  trig= 1.6791E-08
 tdelay       = 4.8307E-10 targ= 4.7220E-09  trig= 4.2389E-09

     ***** job concluded
     total cpu time       46.47 seconds
        job started at  9:45:34  8-feb93
        job ended  at  9:48: 2  8-feb93


I am done with wlogic1.sp
Mon Feb  8 09:48:03 PST 1993
```

T. GaAs DRAM HSPICE Pad->Pad Simulation

The GaAs DRAM design was simulated multiple times per temperature setting using HSPICE for the transient analysis. The reason for the multiple runs arises from the use the HSPICE ".option probe" which restrictes the output data file to a maximum of 32 target nodes. Additionally, the replicated GaAs DRAM data from the second and further HSPICE pad->pad simulation runs will be deleted leaving only the data unique to each.

1. Run #1 LISTING FILE

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
 reading design configuration file: gdram0.cfg
setting user memory from  config file     to  1000000 words. (  8000000 bytes)

 ******    h s p i c e   9007d        10:47:32  6-feb93   sun
** spice file created for circuit gaasdram0   1/10/93 mike morris
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
**
```

```
** node: 0 = gnd
** node: 1 = vdd
j0 100 101 0 0 jfet04 l=1.2 w=28.4
j1 102 103 0 0 jfet04 l=1.2 w=28.4
j2 0 101 100 0 jfet04 l=1.2 w=28.4
j3 0 101 103 0 jfet04 l=1.2 w=18.8
j4 0 103 102 0 jfet04 l=1.2 w=28.4
j5 100 100 1 0 jfet16 l=1.6 w=6.4
j6 103 103 1 0 jfet16 l=2.4 w=3.6
j7 102 102 1 0 jfet16 l=1.6 w=6.4
j8 1 102 104 0 jfet16 l=1.6 w=34.8
j9 104 100 0 0 jfet04 l=1.2 w=47.6
j10 104 100 0 0 jfet04 l=1.2 w=47.6
j11 0 100 104 0 jfet04 l=1.2 w=42.4
j12 0 100 104 0 jfet04 l=1.2 w=42.4
j13 105 1 105 248 dio16 l=2.4 w=36.4
j14 106 1 106 248 dio16 l=1.2 w=30.4
j15 105 1 105 248 dio16 l=2.4 w=52.0
j16 106 1 106 248 dio16 l=1.2 w=30.4
j17 105 1 105 248 dio16 l=2.4 w=52.0
j18 106 1 106 248 dio16 l=1.2 w=30.4
j19 106 1 106 248 dio16 l=1.2 w=30.4
j20 105 1 105 248 dio16 l=2.4 w=52.0
j21 106 1 106 248 dio16 l=1.2 w=30.4
j22 105 1 105 248 dio16 l=2.4 w=52.0
j23 106 1 106 248 dio16 l=1.2 w=30.4
j24 105 1 105 248 dio16 l=2.4 w=52.0
j25 106 1 106 248 dio16 l=1.2 w=30.4
j26 105 1 105 248 dio16 l=2.4 w=52.0
j27 106 1 106 248 dio16 l=1.2 w=30.4
j28 106 1 106 248 dio16 l=1.2 w=30.4
j29 106 1 106 248 dio16 l=1.2 w=29.2
j30 106 104 107 0 jfet04 l=1.2 w=47.6
j31 107 104 105 0 jfet04 l=1.2 w=34.8
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r23 1 1159 2350
r24 1 1139 1714.29
r25 1 1283 1714.29
r26 1 1074 2350
r27 1117 1 2350
r28 1 1138 2350
r29 1 1199 1714.29
r30 1 1223 1714.29
r31 1 1304 1714.29
r32 1 1072 1714.29
r33 1118 1 1714.29
r34 1 1222 2350
r35 1 1157 1714.29
** node: 1313 = a1!
** node: 1292 = inclk!
** node: 1271 = d0!
** node: 1250 = d1!
** node: 1229 = d2!
** node: 1208 = d3!
** node: 1187 = a0!
** node: 1166 = das!
** node: 1145 = a2!
** node: 1124 = refresh!
** node: 1103 = read!
** node: 1082 = write!
** node: 1081 = rvref!
** node: 1014 = cm1_0/o7
** node: 993 = cm1_0/read
** node: 992 = cm1_0/write
** node: 965 = cm1_0/d3
** node: 929 = cm1_0/3cdo
** node: 927 = cm1_0/3rc6
** node: 926 = cm1_0/3rc4
** node: 916 = cm1_0/3rc2
** node: 907 = cm1_0/3ep
** node: 906 = cm1_0/3rc0
** node: 901 = cm1_0/a2

** node: 857 = cm1_0/3epd
** node: 853 = cm1_0/3opd
** node: 822 = cm1_0/a1
** node: 816 = cm1_0/q2
** node: 789 = cm1_0/3opu
** node: 786 = cm1_0/3cde
** node: 788 = cm1_0/3rc7
** node: 787 = cm1_0/3rc5
** node: 790 = cm1_0/3rc3
** node: 849 = cm1_0/3rc1
** node: 784 = cm1_0/3ebio
** node: 779 = cm1_0/3obio
** node: 651 = cm1_0/q1
** node: 600 = cm1_0/ao1
** node: 599 = cm1_0/ao2
** node: 604 = cm1_0/d2
** node: 548 = cm1_0/2cdo
** node: 546 = cm1_0/2rc6
** node: 545 = cm1_0/2rc4
** node: 523 = cm1_0/2rc2
** node: 507 = cm1_0/2epu
** node: 512 = cm1_0/q0
** node: 506 = cm1_0/2rc0
** node: 483 = cm1_0/2epd
** node: 482 = cm1_0/2opd
** node: 472 = cm1_0/q0n
** node: 473 = cm1_0/q1n
** node: 467 = cm1_0/q2n
** node: 466 = cm1_0/refresh
** node: 598 = cm1_0/mref
** node: 462 = cm1_0/2opu
** node: 459 = cm1_0/2cde
** node: 461 = cm1_0/2rc7
** node: 460 = cm1_0/2rc5
** node: 463 = cm1_0/2rc3
** node: 464 = cm1_0/2rc1
** node: 439 = cm1_0/ao0
** node: 455 = cm1_0/2ebio
** node: 450 = cm1_0/2obio
** node: 372 = cm1_0/d1
** node: 360 = cm1_0/1cdo
** node: 359 = cm1_0/1rc6
** node: 358 = cm1_0/1rc4
** node: 347 = cm1_0/1rc2
** node: 338 = cm1_0/1epu
** node: 337 = cm1_0/1rc0
** node: 329 = cm1_0/1epd
** node: 318 = cm1_0/1opd
** node: 315 = cm1_0/1opu
** node: 312 = cm1_0/1cde
** node: 314 = cm1_0/1rc7

** node: 313 = cm1_0/1rc5
** node: 316 = cm1_0/1rc3
** node: 317 = cm1_0/1rc1
** node: 297 = cm1_0/ph1
** node: 296 = cm1_0/inclk
** node: 311 = cm1_0/1ebio
** node: 306 = cm1_0/1obio
** node: 253 = cm1_0/a0
** node: 244 = cm1_0/mw
** node: 243 = cm1_0/ph2
** node: 227 = cm1_0/das
** node: 225 = cm1_0/d0
** node: 218 = cm1_0/0cdo
** node: 219 = cm1_0/od
** node: 216 = cm1_0/0rc6
** node: 215 = cm1_0/0rc4
** node: 217 = cm1_0/da6
** node: 214 = cm1_0/da4
** node: 206 = cm1_0/0rc2
** node: 205 = cm1_0/da2
** node: 195 = cm1_0/0epu
** node: 194 = cm1_0/da0
** node: 193 = cm1_0/0rc0
** node: 192 = cm1_0/0epd
** node: 202 = cm1_0/mr
** node: 191 = cm1_0/ph2ld
** node: 190 = cm1_0/0opd
** node: 188 = cm1_0/da1
** node: 187 = cm1_0/da3
** node: 184 = cm1_0/0op
** node: 183 = cm1_0/ev
** node: 182 = cm1_0/da7
** node: 179 = cm1_0/da5
** node: 177 = cm1_0/ph1l
** node: 178 = cm1_0/0cde
** node: 181 = cm1_0/0rc7
** node: 180 = cm1_0/0rc5
** node: 186 = cm1_0/0rc3
** node: 189 = cm1_0/0rc1
** node: 175 = cm1_0/ev
** node: 174 = cm1_0/0ebio
** node: 169 = cm1_0/od
** node: 168 = cm1_0/0obio
** node: 141 = cm1_0/o0
** node: 147 = do0!
** node: 133 = cm1_0/o1
** node: 139 = do1!
** node: 125 = cm1_0/o2
** node: 131 = do2!
** node: 117 = cm1_0/o3
** node: 123 = do3!

```
** node: 109 = cm1_0/mbsy
** node: 115 = mbsy!
** node: 0 = gnd!
** node: 1 = vdd!
** node: 101 = cm1_0/drdy
** node: 107 = drdy!
** node: 176 = vrefd!
** node: 185 = vrefb!
** node: 248 = vss!
c0 178 0 70ff
c1 218 0 70ff
c2 312 0 70ff
c3 360 0 70ff
c4 459 0 70ff
c5 548 0 70ff
c6 786 0 70ff
c7 929 0 70ff

c100 189 0 620ff
c101 186 0 620ff
c102 180 0 620ff
c103 181 0 620ff
c104 193 0 620ff
c105 206 0 620ff
c106 215 0 620ff
c107 216 0 620ff

c110 317 0 620ff
c111 316 0 620ff
c112 313 0 620ff
c113 314 0 620ff
c114 337 0 620ff
c115 347 0 620ff
c116 359 0 620ff
c117 358 0 620ff

c120 464 0 620ff
c121 463 0 620ff
c122 460 0 620ff
c123 461 0 620ff
c124 506 0 620ff
c125 523 0 620ff
c126 545 0 620ff
c127 546 0 620ff

c130 849 0 620ff
c131 790 0 620ff
c132 787 0 620ff
c133 788 0 620ff
c134 906 0 620ff
c135 916 0 620ff
```

```
c136 926 0 620ff
c137 927 0 620ff

* don't forget the terminating resistors on each output pad
r100 147 0 50
r101 139 0 50
r102 131 0 50
r103 123 0 50
r104 107 0 50
r105 115 0 50
**********************************************************
* ******* hspice version *********
* include vitesse hgaas3 models and parameters for hspice.
**********************************************************
**********************************************************
**********************************************************
* power supply
vds   1  0 dc  2.0v
vrefb 185 0 dc 0.7v
vrefd 176  0 dc 0.26v
vrvref 1081 0 dc 0.70v
vss  248  0 dc -2.5v
* signal input
*******************************************************************************
*
*remember that the inputs are ecl re: l=0.4v h=1.1v
*remember that outputs are ecl too!:
*******************************************************************************
*


vinclk  1292 0 pulse(1.1  0.4   0ps 100ps 100ps 2100ps 4200ps)



va0  1187    0 1.1v $ memory address bit 0
va1  1313    0 0.4v $ memory address bit 1
va2  1145    0 1.1v $ memory address bit 2

vd0  1271 0 1.1v $ memory data bit 0
vd1  1250 0 0.4v $ memory data bit 1
vd2  1229 0 1.1v $ memory data bit 2
vd3  1208 0 1.1v $ memory data bit 3
vdas  1166 0 1.1v $ memory data strobe

vwrite   1082  0  pulse(0.4 1.1 2.8ns 100ps 100ps 5200ps 1000ms) $ memory writ
e
vread    1103  0  pulse(0.4 1.1 3ns 100ps 100ps 8000ps 1000ms)   $ memory read
*vrefresh 1124 0 0.4v
vrefresh 1124 0 pulse(0.4 1.1 12ns 100ps 100ps 4200ps 1000ms)    $ test eol co
m
```

```
* following .ic line initializes the refresh control counter to 3 zeroes
* simulation purposes only
*    q0        q1        q2        q0n       q1n       q2n
.ic v(512)=0.0 v(651)=0.0 v(816)=0.0 v(472)=0.63 v(473)=0.63 v(467)=0.63
*    mref
+  v(598)=0.0
*.temp 85.0
.tran 500ps 60ns


.measure tran vds_avgpwr avg p(vds) from 0.0ns to 60ns
.measure tran vrefb_avgpwr avg p(vrefb) from 0.0ns to 60ns
.measure tran vrefd_avgpwr avg p(vrefd) from 0.0ns to 60ns
.measure tran vrvref_avgpwr avg p(vrvrf) from 0.0ns to 60ns
.measure tran vss_avgpwr avg p(vss) from 0.0ns to 60ns

*                                                    80 columns->>*
.probe inclk=v(1292) a0=v(1187) a1=v(1313) a2=v(1145) d0=v(1271) d1=v(1250)
+ d2=v(1229) d3=v(1208) das=v(1166) write=v(1082) read=v(1103) refresh=v(1124)
+ mrefresh=v(598) mwrite=v(244) mread=v(202)
+ ma3cdo=v(929) ma3cde=v(786) ma3rc6=v(927) ma3rc4=v(926)
+ ma3rc2=v(916) ma3rc0=v(906) ma3rc7=v(788) ma3rc5=v(787) ma3rc3=v(790)
+ ma3rc1=v(849) ma3ebio=v(784) ma3obio=v(779) ma3epu=v(907) ma3epd=v(857)
+ ma3opu=v(789) ma3opd=v(853) q0=v(512)

.options fast ft=0.95 fs=.95 imin=16.0 imax=16.0 delmax=1.0s  rmax=8.0
+ scale=1e-06 brief=0 nopage measout post probe gmindc=1e-11 captab acct
*.options scale=1e-06 probe post gmindc=1e-11 acct captab
.end


**warning**  the fast option decreases  the cpu time but results may be
          less accurate.
***fast option sets default value of the options:
 dvdt= 1       rmax=  8.00     fs= 950.00m     ft= 950.00m
relvar= 400.00m absvar=  1.00  relmos= 100.00m absmos=  10.00u
**warning** could not find branch element     0:vrvrf
    branch - output ignored
** spice file created for circuit gaasdram0  1/10/93 mike morris
******  operating point information     tnom=  25.000 temp=  25.000
******
***** operating point status is voltage   simulation time is    0.
  node   =voltage     node   =voltage     node   =voltage


+0:1     =  2.0000  0:100    =  61.5008m 0:101    =  668.5881m
+0:102   =  1.9874  0:103    =  63.4356m 0:104    =  1.7750
+0:105   =  1.3406  0:106    =  1.3028  0:107    =  1.1799
+0:108   =  635.3582m 0:109    =  52.0500m 0:110    =  65.6886m
+0:111   =  633.3473m 0:112    =  110.9801m 0:113    =  1.4638
```

+0:114 = 1.4226 0:115 = 23.0831m 0:116 = 63.1546m
+0:117 = 646.3142m 0:118 = 1.9870 0:119 = 65.5267m
+0:120 = 1.7749 0:121 = 1.3406 0:122 = 1.3028
+0:123 = 1.1799 0:124 = 63.1546m 0:125 = 646.3142m
+0:126 = 1.9870 0:127 = 65.5267m 0:128 = 1.7749
+0:129 = 1.3406 0:130 = 1.3028 0:131 = 1.1799
+0:132 = 63.1546m 0:133 = 646.3142m 0:134 = 1.9870
+0:135 = 65.5267m 0:136 = 1.7749 0:137 = 1.3406
+0:138 = 1.3028 0:139 = 1.1799 0:140 = 63.1546m
+0:141 = 646.3142m 0:142 = 1.9870 0:143 = 65.5267m
+0:144 = 1.7749 0:145 = 1.3406 0:146 = 1.3028
+0:147 = 1.1799 0:148 = 644.3156m 0:149 = 653.4293m
+0:150 = 52.1099m 0:151 = 53.0832m 0:152 = 31.7692m
+0:153 = 53.0833m 0:154 = 52.1099m 0:155 = 644.3155m
+0:156 = 653.4296m 0:157 = 31.7693m 0:158 = 642.1434m
+0:159 = 642.1432m 0:160 = 651.2168m 0:161 = 53.0833m
+0:162 = 25.0740m 0:163 = 642.1434m 0:164 = 642.1432m
+0:165 = 651.2166m 0:166 = 53.0832m 0:167 = 25.0740m
+0:168 = 283.3468m 0:169 = 15.0105m 0:170 = 649.5537m
+0:171 = 636.6299m 0:172 = 636.6297m 0:173 = 649.5538m
+0:174 = 283.3478m 0:175 = 14.8309m 0:176 = 260.0000m
+0:177 = 47.0991m 0:178 = 260.0000m 0:179 = -1.2102
+0:180 = 185.3334m 0:181 = 185.3334m 0:182 = -1.2102
+0:183 = -1.2102 0:184 = -1.2102 0:185 = 700.0000m
+0:186 = 185.3334m 0:187 = -1.2102 0:188 = -1.2102
+0:189 = 185.3334m 0:190 = 26.2262m 0:191 = -1.2102
+0:192 = 23.1826m 0:193 = 185.3336m 0:194 = -1.2102
+0:195 = -1.2102 0:196 = 658.5029m 0:197 = 52.0502m
+0:198 = 658.7224m 0:199 = 52.0553m 0:200 = 653.5485m
+0:201 = 653.5488m 0:202 = 51.9710m 0:203 = 32.4441m
+0:204 = 1.3252 0:205 = -1.2102 0:206 = 185.3336m
+0:207 = 62.1464m 0:208 = 1.2617 0:209 = 654.8023m
+0:210 = 94.4918m 0:211 = 720.2099m 0:212 = 711.4147m
+0:213 = 62.4027m 0:214 = -1.2102 0:215 = 185.3336m
+0:216 = 185.3336m 0:217 = -1.2102 0:218 = 260.0000m
+0:219 = -1.2102 0:220 = 83.7791m 0:221 = 614.6034m
+0:222 = 681.1434m 0:223 = 81.2916m 0:224 = 61.2124m
+0:225 = 706.7093m 0:226 = 53.6483m 0:227 = 660.6934m
+0:228 = 44.1940m 0:229 = 18.5576m 0:230 = 51.1112m
+0:231 = 650.4577m 0:232 = 650.3010m 0:233 = 650.5376m
+0:234 = 650.4577m 0:235 = 651.5281m 0:236 = 56.9511m
+0:237 = 651.5281m 0:238 = 651.6083m 0:239 = 26.2368m
+0:240 = 1.9864 0:241 = 91.2977m 0:242 = 52.0122m
+0:243 = 21.1598m 0:244 = 52.0131m 0:245 = 1.4151
+0:246 = 687.7530m 0:247 = 281.0546m 0:248 = -2.5000
+0:249 = -2.1776 0:250 = -464.5912m 0:251 = -1.8551
+0:252 = -1.5327 0:253 = 654.6080m 0:254 = 52.0122m
+0:255 = 651.3674m 0:256 = 651.6047m 0:257 = 651.5245m
+0:258 = 52.0122m 0:259 = 56.9511m 0:260 = 653.5411m
+0:261 = 653.6218m 0:262 = 32.4197m 0:263 = 1.9855
+0:264 = -464.6009m 0:265 = -1.5327 0:266 = 687.4029m

+0:267 = 1.4146 0:268 = 281.0448m 0:269 = -1.8551
+0:270 = 91.2850m 0:271 = -2.1776 0:272 = 644.3159m
+0:273 = 653.4293m 0:274 = 52.1099m 0:275 = 53.0832m
+0:276 = 31.7693m 0:277 = 53.0833m 0:278 = 52.1099m
+0:279 = 644.3156m 0:280 = 653.4296m 0:281 = 31.7693m
+0:282 = 642.1437m 0:283 = 642.1433m 0:284 = 651.2168m
+0:285 = 53.0833m 0:286 = 25.0740m 0:287 = 642.1437m
+0:288 = 642.1433m 0:289 = 651.2166m 0:290 = 53.0832m
+0:291 = 25.0740m 0:292 = 1.4024 0:293 = 52.5036m
+0:294 = 1.3308 0:295 = 61.1855m 0:296 = 664.3093m
+0:297 = 741.0191m 0:298 = 48.0693m 0:299 = 667.2192m
+0:300 = 54.1981m 0:301 = 52.2948m 0:302 = 20.1113m
+0:303 = 1.3020 0:304 = 628.5119m 0:305 = 10.2774m
+0:306 = 283.3449m 0:307 = 649.5538m 0:308 = 636.6299m
+0:309 = 636.6297m 0:310 = 649.5541m 0:311 = 283.3472m
+0:312 = 260.0000m 0:313 = 185.3330m 0:314 = 185.3330m
+0:315 = -1.2102 0:316 = 185.3330m 0:317 = 185.3330m
+0:318 = 32.4197m 0:319 = 52.5036m 0:320 = 633.5094m
+0:321 = 32.0844m 0:322 = 610.7009m 0:323 = 610.6642m
+0:324 = 26.7721m 0:325 = 6.6963m 0:326 = 1.9887
+0:327 = -464.5655m 0:328 = 1.4024 0:329 = 26.2368m
+0:330 = 77.1805m 0:331 = 1.9341 0:332 = -1.5327
+0:333 = -230.1995m 0:334 = -939.2934m 0:335 = 1.5584
+0:336 = -1.8632 0:337 = 185.3334m 0:338 = -1.2102
+0:339 = 658.5029m 0:340 = 52.0502m 0:341 = 658.7224m
+0:342 = 52.0553m 0:343 = 653.5485m 0:344 = 653.5488m
+0:345 = 32.4441m 0:346 = 1.3252 0:347 = 185.3334m
+0:348 = 802.7575m 0:349 = -1.2265 0:350 = 62.1464m
+0:351 = 1.2617 0:352 = 654.8023m 0:353 = 94.4918m
+0:354 = 720.2099m 0:355 = 711.4147m 0:356 = 62.4027m
+0:357 = -589.6757m 0:358 = 185.3334m 0:359 = 185.3334m
+0:360 = 260.0000m 0:361 = 681.3352m 0:362 = 81.3768m
+0:363 = 78.4572m 0:364 = 614.6178m 0:365 = 678.4986m
+0:366 = 688.6339m 0:367 = 1.4163 0:368 = 281.0805m
+0:369 = -1.8551 0:370 = 91.3312m 0:371 = -2.1776
+0:372 = 21.4729m 0:373 = 558.0589m 0:374 = 51.1900m
+0:375 = 48.2828m 0:376 = 40.9551m 0:377 = 651.5281m
+0:378 = 56.9477m 0:379 = 651.6083m 0:380 = 651.5281m
+0:381 = 650.4577m 0:382 = 650.3003m 0:383 = 650.4577m
+0:384 = 650.5376m 0:385 = 23.1826m 0:386 = 1.9868
+0:387 = 91.3036m 0:388 = 52.0122m 0:389 = 1.4153
+0:390 = 687.9123m 0:391 = 281.0592m 0:392 = -2.1776
+0:393 = -464.5867m 0:394 = -1.8551 0:395 = -1.5327
+0:396 = 52.0122m 0:397 = 56.9477m 0:398 = 653.6218m
+0:399 = 653.5411m 0:400 = 52.0122m 0:401 = 651.3667m
+0:402 = 651.5245m 0:403 = 651.6047m 0:404 = 26.2262m
+0:405 = 1.9864 0:406 = -464.5912m 0:407 = -1.5327
+0:408 = 687.7536m 0:409 = 1.4151 0:410 = 281.0546m
+0:411 = -1.8551 0:412 = 91.2978m 0:413 = -2.1776
+0:414 = 644.3156m 0:415 = 653.4293m 0:416 = 52.1099m
+0:417 = 53.0832m 0:418 = 31.7692m 0:419 = 53.0833m

+0:420 = 52.1099m 0:421 = 644.3155m 0:422 = 653.4296m
+0:423 = 31.7693m 0:424 = 642.1434m 0:425 = 642.1432m
+0:426 = 651.2168m 0:427 = 53.0833m 0:428 = 25.0740m
+0:429 = 642.1434m 0:430 = 642.1432m 0:431 = 651.2166m
+0:432 = 53.0832m 0:433 = 25.0740m 0:434 = 63.7170m
+0:435 = 26.4851m 0:436 = 1.3150 0:437 = 1.3154
+0:438 = 1.3155 0:439 = 591.6209m 0:440 = 648.8233m
+0:441 = 32.2745m 0:442 = 648.9187m 0:443 = 1.9879
+0:444 = 91.3185m 0:445 = 648.9397m 0:446 = 1.4158
+0:447 = 688.3053m 0:448 = 281.0706m 0:449 = -2.1776
+0:450 = 283.3468m 0:451 = 649.5537m 0:452 = 636.6299m
+0:453 = 636.6297m 0:454 = 649.5538m 0:455 = 283.3478m
+0:456 = -464.5753m 0:457 = -1.8551 0:458 = -1.5327
+0:459 = 260.0000m 0:460 = 185.3334m 0:461 = 185.3334m
+0:462 = -1.2102 0:463 = 185.3334m 0:464 = 185.3334m
+0:465 = 653.1676m 0:466 = 21.4729m 0:467 = 629.9968m
+0:468 = 57.5154m 0:469 = 10.6195m 0:470 = 10.6178m
+0:471 = 57.5170m 0:472 = 629.9885m 0:473 = 629.9927m
+0:474 = 57.5162m 0:475 = 10.6186m 0:476 = 16.4768m
+0:477 = 54.9190m 0:478 = 1.3579 0:479 = 693.3843m
+0:480 = 59.0264m 0:481 = 32.3384m 0:482 = 26.2262m
+0:483 = 23.1826m 0:484 = 53.9676m 0:485 = 658.7393m
+0:486 = 52.0114m 0:487 = 658.7911m 0:488 = 54.9711m
+0:489 = 52.0114m 0:490 = 658.5363m 0:491 = 52.0509m
+0:492 = 651.5307m 0:493 = 651.5887m 0:494 = 651.5307m
+0:495 = 26.2446m 0:496 = 636.6116m 0:497 = 653.5993m
+0:498 = 653.5409m 0:499 = 77.1806m 0:500 = 32.4194m
+0:501 = 624.0322m 0:502 = 54.9711m 0:503 = 53.0853m
+0:504 = 658.5204m 0:505 = 52.0506m 0:506 = 185.3336m
+0:507 = -1.2102 0:508 = 678.3256m 0:509 = 78.2660m
+0:510 = 1.2803 0:511 = 657.5160m 0:512 = 17.6214u
+0:513 = 624.0324m 0:514 = 52.0443m 0:515 = 658.5029m
+0:516 = 52.0502m 0:517 = 658.7224m 0:518 = 52.0553m
+0:519 = 653.5485m 0:520 = 653.5488m 0:521 = 32.4441m
+0:522 = 1.3252 0:523 = 185.3336m 0:524 = 77.1806m
+0:525 = 1.8535 0:526 = 79.2828m 0:527 = 48.0917m
+0:528 = 1.2832 0:529 = 667.7719m 0:530 = 62.1464m
+0:531 = 1.2617 0:532 = 654.8023m 0:533 = 94.4918m
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+0:1293 = 1.3336 0:1294 = 1.3336 0:1295 = 55.0936m
+0:1296 = 55.0936m 0:1297 = 55.0936m 0:1298 = 55.0936m
+0:1299 = 66.1073m 0:1300 = 668.0228m 0:1301 = 616.9350m
+0:1302 = 268.2792n 0:1303 = 80.8626m 0:1304 = 1.9044
+0:1305 = 1.3296 0:1306 = 620.9308m 0:1307 = 1.2422
+0:1308 = 794.3590m 0:1309 = 968.6015m 0:1310 = 604.6550m
+0:1311 = 418.2974m 0:1312 = 274.2922m 0:1313 = 400.0000m

maximum nodal capacitance= 4.291E-11 on node 0:1

nodal capacitance table

node	= cap	node	= cap	node	= cap
+0:1	= 42.9105p	0:100	= 325.7088f	0:101	= 197.9760f
+0:102	= 170.9088f	0:103	= 123.8339f	0:104	= 2.5773p
+0:105	= 2.2431p	0:106	= 1.2935p	0:107	= 2.3619p
+0:108	= 325.7088f	0:109	= 193.9920f	0:110	= 170.9088f
+0:111	= 123.8339f	0:112	= 2.5773p	0:113	= 2.2431p
+0:114	= 1.2935p	0:115	= 2.3619p	0:116	= 325.7088f
+0:117	= 554.8905f	0:118	= . 0.9088f	0:119	= 123.8339f
+0:120	= 2.5773p	0:121	= 2.2431p	0:122	= 1.2935p
+0:123	= 2.3619p	0:124	= 325.7088f	0:125	= 554.8905f
+0:126	= 170.9088f	0:127	= 123.8339f	0:128	= 2.5773p
+0:129	= 2.2431p	0:130	= 1.2935p	0:131	= 2.3619p
+0:132	= 325.7088f	0:133	= 554.8905f	0:134	= 170.9088f
+0:135	= 123.8339f	0:136	= 2.5773p	0:137	= 2.2431p
+0:138	= 1.2935p	0:139	= 2.3619p	0:140	= 325.7088f
+0:141	= 554.8905f	0:142	= 170.9088f	0:143	= 123.8339f
+0:144	= 2.5773p	0:145	= 2.2431p	0:146	= 1.2935p
+0:147	= 2.3619p	0:148	= 227.3520f	0:149	= 223.3680f
+0:150	= 227.3520f	0:151	= 223.3680f	0:152	= 434.7120f
+0:153	= 227.3520f	0:154	= 223.3680f	0:155	= 227.3520f
+0:156	= 223.3680f	0:157	= 434.7120f	0:158	= 227.3520f
+0:159	= 223.3680f	0:160	= 227.3520f	0:161	= 223.3680f
+0:162	= 434.7120f	0:163	= 227.3520f	0:164	= 223.3680f
+0:165	= 227.3520f	0:166	= 223.3680f	0:167	= 434.7120f
+0:168	= 1.2737p	0:169	= 3.1795p	0:170	= 223.3680f
+0:171	= 365.5920f	0:172	= 361.6080f	0:173	= 227.3520f
+0:174	= 1.2803p	0:175	= 3.1795p	0:176	= 17.1008f
+0:177	= 360.7840f	0:178	= 79.6064f	0:179	= 139.9840f
+0:180	= 630.6560f	0:181	= 625.3440f	0:182	= 139.9840f
+0:183	= 139.9840f	0:184	= 447.9840f	0:185	= 32.0640f
+0:186	= 625.3440f	0:187	= 139.9840f	0:188	= 139.9840f
+0:189	= 630.6560f	0:190	= 301.1280f	0:191	= 223.1840f
+0:192	= 305.1120f	0:193	= 625.3440f	0:194	= 139.9840f
+0:195	= 447.9840f	0:196	= 434.7120f	0:197	= 499.8480f
+0:198	= 296.4720f	0:199	= 223.3680f	0:200	= 227.3520f
+0:201	= 223.3680f	0:202	= 1.1910p	0:203	= 711.1920f
+0:204	= 361.6080f	0:205	= 139.9840f	0:206	= 630.6560f
+0:207	= 276.4800f	0:208	= 415.4294f	0:209	= 276.4800f
+0:210	= 446.0266f	0:211	= 276.4800f	0:212	= 415.4294f
+0:213	= 276.4800f	0:214	= 139.9840f	0:215	= 630.6560f
+0:216	= 625.3440f	0:217	= 139.9840f	0:218	= 79.6064f
+0:219	= 139.9840f	0:220	= 419.4134f	0:221	= 726.4905f
+0:222	= 419.4134f	0:223	= 726.4905f	0:224	= 361.6080f
+0:225	= 691.2000f	0:226	= 276.4800f	0:227	= 2.4883p
+0:228	= 276.4800f	0:229	= 276.4800f	0:230	= 276.4800f
+0:231	= 227.3520f	0:232	= 223.3680f	0:233	= 227.3520f
+0:234	= 223.3680f	0:235	= 227.3520f	0:236	= 223.3680f
+0:237	= 227.3520f	0:238	= 223.3680f	0:239	= 434.7120f
+0:240	= 113.9280f	0:241	= 61.8576f	0:242	= 361.6080f

+0:243 = 6.8256p 0:244 = 2.6466p 0:245 = 17.6192f
+0:246 = 35.4816f 0:247 = 53.3600f 0:248 = 1.7123p
+0:249 = 40.0000f 0:250 = 80.0000f 0:251 = 40.0000f
+0:252 = 40.0000f 0:253 = 2.2118p 0:254 = 227.3520f
+0:255 = 223.3680f 0:256 = 227.3520f 0:257 = 223.3680f
+0:258 = 227.3520f 0:259 = 223.3680f 0:260 = 227.3520f
+0:261 = 223.3680f 0:262 = 430.7280f 0:263 = 113.9280f
+0:264 = 80.0000f 0:265 = 40.0000f 0:266 = 42.9184f
+0:267 = 17.6192f 0:268 = 53.3600f 0:269 = 40.0000f
+0:270 = 61.8576f 0:271 = 40.0000f 0:272 = 227.3520f
+0:273 = 223.3680f 0:274 = 227.3520f 0:275 = 223.3680f
+0:276 = 434.7120f 0:277 = 227.3520f 0:278 = 223.3680f
+0:279 = 227.3520f 0:280 = 223.3680f 0:281 = 434.7120f
+0:282 = 227.3520f 0:283 = 223.3680f 0:284 = 227.3520f
+0:285 = 223.3680f 0:286 = 434.7120f 0:287 = 227.3520f
+0:288 = 223.3680f 0:289 = 227.3520f 0:290 = 223.3680f
+0:291 = 434.7120f 0:292 = 1.8188p 0:293 = 1.8188p
+0:294 = 1.8188p 0:295 = 358.9744f 0:296 = 1.5264p
+0:297 = 3.6461p 0:298 = 2.4490p 0:299 = 5.5296p
+0:300 = 1.8188p 0:301 = 790.5920f 0:302 = 881.2800f
+0:303 = 358.9744f 0:304 = 2.4490p 0:305 = 5.5296p
+0:306 = 1.2737p 0:307 = 223.3680f 0:308 = 365.5920f
+0:309 = 361.6080f 0:310 = 227.3520f 0:311 = 1.2803p
+0:312 = 79.6064f 0:313 = 630.6560f 0:314 = 625.3440f
+0:315 = 447.9840f 0:316 = 625.3440f 0:317 = 630.6560f
+0:318 = 301.1280f 0:319 = 1.7869p 0:320 = 891.9200f
+0:321 = 891.9200f 0:322 = 1.1292p 0:323 = 1.1292p
+0:324 = 609.5920f 0:325 = 622.0800f 0:326 = 113.9280f
+0:327 = 80.0000f 0:328 = 1.7869p 0:329 = 305.1120f
+0:330 = 113.9280f 0:331 = 61.8576f 0:332 = 40.0000f
+0:333 = 17.6192f 0:334 = 35.4816f 0:335 = 53.3600f
+0:336 = 40.0000f 0:337 = 625.3440f 0:338 = 447.9840f
+0:339 = 434.7120f 0:340 = 499.8480f 0:341 = 296.4720f
+0:342 = 223.3680f 0:343 = 227.3520f 0:344 = 223.3680f
+0:345 = 711.1920f 0:346 = 361.6080f 0:347 = 630.6560f
+0:348 = 80.0000f 0:349 = 40.0000f 0:350 = 276.4800f
+0:351 = 415.4294f 0:352 = 276.4800f 0:353 = 446.0266f
+0:354 = 276.4800f 0:355 = 415.4294f 0:356 = 276.4800f
+0:357 = 40.0000f 0:358 = 630.6560f 0:359 = 625.3440f
+0:360 = 79.6064f 0:361 = 419.4134f 0:362 = 726.4905f
+0:363 = 419.4134f 0:364 = 726.4905f 0:365 = 361.6080f
+0:366 = 42.9184f 0:367 = 17.6192f 0:368 = 53.3600f
+0:369 = 40.0000f 0:370 = 61.8576f 0:371 = 40.0000f
+0:372 = 691.2000f 0:373 = 276.4800f 0:374 = 276.4800f
+0:375 = 276.4800f 0:376 = 276.4800f 0:377 = 227.3520f
+0:378 = 223.3680f 0:379 = 227.3520f 0:380 = 223.3680f
+0:381 = 227.3520f 0:382 = 223.3680f 0:383 = 227.3520f
+0:384 = 223.3680f 0:385 = 434.7120f 0:386 = 113.9280f
+0:387 = 61.8576f 0:388 = 361.6080f 0:389 = 17.6192f
+0:390 = 35.4816f 0:391 = 53.3600f 0:392 = 40.0000f
+0:393 = 80.0000f 0:394 = 40.0000f 0:395 = 40.0000f

+0:396 = 227.3520f 0:397 = 223.3680f 0:398 = 227.3520f
+0:399 = 223.3680f 0:400 = 227.3520f 0:401 = 223.3680f
+0:402 = 227.3520f 0:403 = 223.3680f 0:404 = 430.7280f
+0:405 = 113.9280f 0:406 = 80.0000f 0:407 = 40.0000f
+0:408 = 42.9184f 0:409 = 17.6192f 0:410 = 53.3600f
+0:411 = 40.0000f 0:412 = 61.8576f 0:413 = 40.0000f
+0:414 = 227.3520f 0:415 = 223.3680f 0:416 = 227.3520f
+0:417 = 223.3680f 0:418 = 434.7120f 0:419 = 227.3520f
+0:420 = 223.3680f 0:421 = 227.3520f 0:422 = 223.3680f
+0:423 = 434.7120f 0:424 = 227.3520f 0:425 = 223.3680f
+0:426 = 227.3520f 0:427 = 223.3680f 0:428 = 434.7120f
+0:429 = 227.3520f 0:430 = 223.3680f 0:431 = 227.3520f
+0:432 = 223.3680f 0:433 = 434.7120f 0:434 = 227.3520f
+0:435 = 448.4685f 0:436 = 125.8163f 0:437 = 125.8163f
+0:438 = 100.7437f 0:439 = 1.0528p 0:440 = 483.8400f
+0:441 = 1.4515p 0:442 = 483.8400f 0:443 = 113.9280f
+0:444 = 61.8576f 0:445 = 483.8400f 0:446 = 17.6192f
+0:447 = 35.4816f 0:448 = 53.3600f 0:449 = 40.0000f
+0:450 = 1.2737p 0:451 = 223.3680f 0:452 = 365.5920f
+0:453 = 361.6080f 0:454 = 227.3520f 0:455 = 1.2803p
+0:456 = 80.0000f 0:457 = 40.0000f 0:458 = 40.0000f
+0:459 = 79.6064f 0:460 = 630.6560f 0:461 = 625.3440f
+0:462 = 447.9840f 0:463 = 625.3440f 0:464 = 630.6560f
+0:465 = 223.3680f 0:466 = 414.7200f 0:467 = 499.8480f
+0:468 = 125.8163f 0:469 = 207.3600f 0:470 = 207.3600f
+0:471 = 100.7437f 0:472 = 776.3280f 0:473 = 638.0880f
+0:474 = 125.8163f 0:475 = 207.3600f 0:476 = 207.3600f
+0:477 = 100.7437f 0:478 = 215.8976f 0:479 = 299.5661f
+0:480 = 125.8163f 0:481 = 2.2810p 0:482 = 301.1280f
+0:483 = 305.1120f 0:484 = 227.3520f 0:485 = 223.3680f
+0:486 = 296.4720f 0:487 = 227.3520f 0:488 = 223.3680f
+0:489 = 296.4720f 0:490 = 296.4720f 0:491 = 223.3680f
+0:492 = 223.3680f 0:493 = 223.3680f 0:494 = 223.3680f
+0:495 = 365.5920f 0:496 = 361.6080f 0:497 = 223.3680f
+0:498 = 223.3680f 0:499 = 223.3680f 0:500 = 365.5920f
+0:501 = 499.8480f 0:502 = 223.3680f 0:503 = 223.3680f
+0:504 = 296.4720f 0:505 = 223.3680f 0:506 = 625.3440f
+0:507 = 447.9840f 0:508 = 419.4134f 0:509 = 864.7305f
+0:510 = 419.4134f 0:511 = 450.0106f 0:512 = 914.5680f
+0:513 = 503.8320f 0:514 = 361.6080f 0:515 = 434.7120f
+0:516 = 499.8480f 0:517 = 296.4720f 0:518 = 223.3680f
+0:519 = 227.3520f 0:520 = 223.3680f 0:521 = 711.1920f
+0:522 = 361.6080f 0:523 = 630.6560f 0:524 = 776.3280f
+0:525 = 361.6080f 0:526 = 276.4800f 0:527 = 276.4800f
+0:528 = 276.4800f 0:529 = 276.4800f 0:530 = 276.4800f
+0:531 = 415.4294f 0:532 = 276.4800f 0:533 = 446.0266f
+0:534 = 276.4800f 0:535 = 415.4294f 0:536 = 276.4800f
+0:537 = 125.8163f 0:538 = 483.8400f 0:539 = 125.8163f
+0:540 = 483.8400f 0:541 = 483.8400f 0:542 = 100.7437f
+0:543 = 446.3437f 0:544 = 113.9280f 0:545 = 630.6560f
+0:546 = 625.3440f 0:547 = 80.0000f 0:548 = 79.6064f

+0:549 = 419.4134f 0:550 = 726.4905f 0:551 = 40.0000f
+0:552 = 419.4134f 0:553 = 726.4905f 0:554 = 42.9184f
+0:555 = 17.6192f 0:556 = 53.3600f 0:557 = 361.6080f
+0:558 = 40.0000f 0:559 = 61.8576f 0:560 = 40.0000f
+0:561 = 642.0720f 0:562 = 638.0880f 0:563 = 638.0880f
+0:564 = 125.8163f 0:565 = 100.7437f 0:566 = 125.8163f
+0:567 = 100.7437f 0:568 = 218.0224f 0:569 = 281.1734f
+0:570 = 125.8163f 0:571 = 100.7437f 0:572 = 148.9024f
+0:573 = 223.3680f 0:574 = 223.3680f 0:575 = 223.3680f
+0:576 = 361.6080f 0:577 = 223.3680f 0:578 = 223.3680f
+0:579 = 223.3680f 0:580 = 361.6080f 0:581 = 223.3680f
+0:582 = 223.3680f 0:583 = 292.4880f 0:584 = 638.0880f
+0:585 = 361.6080f 0:586 = 227.3520f 0:587 = 223.3680f
+0:588 = 296.4720f 0:589 = 227.3520f 0:590 = 223.3680f
+0:591 = 158.2320f 0:592 = 276.4800f 0:593 = 207.3600f
+0:594 = 207.3600f 0:595 = 622.0800f 0:596 = 125.8163f
+0:597 = 230.4461f 0:598 = 1.0368p 0:599 = 776.3280f
+0:600 = 776.3280f 0:601 = 207.3600f 0:602 = 207.3600f
+0:603 = 207.3600f 0:604 = 691.2000f 0:605 = 276.4800f
+0:606 = 276.4800f 0:607 = 276.4800f 0:608 = 276.4800f
+0:609 = 227.3520f 0:610 = 223.3680f 0:611 = 227.3520f
+0:612 = 223.3680f 0:613 = 227.3520f 0:614 = 223.3680f
+0:615 = 227.3520f 0:616 = 223.3680f 0:617 = 434.7120f
+0:618 = 113.9280f 0:619 = 61.8576f 0:620 = 361.6080f
+0:621 = 17.6192f 0:622 = 35.4816f 0:623 = 53.3600f
+0:624 = 40.0000f 0:625 = 80.0000f 0:626 = 40.0000f
+0:627 = 40.0000f 0:628 = 207.3600f 0:629 = 299.5661f
+0:630 = 227.3520f 0:631 = 223.3680f 0:632 = 296.4720f
+0:633 = 113.9280f 0:634 = 61.8576f 0:635 = 365.5920f
+0:636 = 223.3680f 0:637 = 223.3680f 0:638 = 223.3680f
+0:639 = 223.3680f 0:640 = 365.5920f 0:641 = 361.6080f
+0:642 = 223.3680f 0:643 = 223.3680f 0:644 = 223.3680f
+0:645 = 365.5920f 0:646 = 499.8480f 0:647 = 223.3680f
+0:648 = 223.3680f 0:649 = 296.4720f 0:650 = 223.3680f
+0:651 = 914.5680f 0:652 = 138.2400f 0:653 = 361.6080f
+0:654 = 361.6080f 0:655 = 100.7437f 0:656 = 253.3939f
+0:657 = 207.3600f 0:658 = 207.3600f 0:659 = 146.7776f
+0:660 = 125.8163f 0:661 = 100.7437f 0:662 = 307.7866f
+0:663 = 276.4800f 0:664 = 125.8163f 0:665 = 207.3600f
+0:666 = 207.3600f 0:667 = 100.7437f 0:668 = 125.8163f
+0:669 = 207.3600f 0:670 = 207.3600f 0:671 = 100.7437f
+0:672 = 215.8976f 0:673 = 299.5661f 0:674 = 17.6192f
+0:675 = 35.4816f 0:676 = 53.3600f 0:677 = 40.0000f
+0:678 = 80.0000f 0:679 = 40.0000f 0:680 = 40.0000f
+0:681 = 125.8163f 0:682 = 100.7437f 0:683 = 125.8163f
+0:684 = 100.7437f 0:685 = 218.0224f 0:686 = 227.3520f
+0:687 = 223.3680f 0:688 = 296.4720f 0:689 = 113.9280f
+0:690 = 80.0000f 0:691 = 40.0000f 0:692 = 227.3520f
+0:693 = 223.3680f 0:694 = 227.3520f 0:695 = 223.3680f
+0:696 = 227.3520f 0:697 = 223.3680f 0:698 = 227.3520f
+0:699 = 223.3680f 0:700 = 430.7280f 0:701 = 113.9280f

+0:702 = 80.0000f 0:703 = 40.0000f 0:704 = 42.9184f
+0:705 = 17.6192f 0:706 = 42.9184f 0:707 = 17.6192f
+0:708 = 227.3520f 0:709 = 227.3520f 0:710 = 223.3680f
+0:711 = 296.4720f 0:712 = 227.3520f 0:713 = 223.3680f
+0:714 = 296.4720f 0:715 = 227.3520f 0:716 = 223.3680f
+0:717 = 223.3680f 0:718 = 361.6080f 0:719 = 365.5920f
+0:720 = 227.3520f 0:721 = 223.3680f 0:722 = 223.3680f
+0:723 = 223.3680f 0:724 = 223.3680f 0:725 = 223.3680f
+0:726 = 361.6080f 0:727 = 223.3680f 0:728 = 223.3680f
+0:729 = 223.3680f 0:730 = 361.6080f 0:731 = 223.3680f
+0:732 = 223.3680f 0:733 = 292.4880f 0:734 = 138.2400f
+0:735 = 207.3600f 0:736 = 207.3600f 0:737 = 207.3600f
+0:738 = 207.3600f 0:739 = 299.5661f 0:740 = 53.3600f
+0:741 = 53.3600f 0:742 = 40.0000f 0:743 = 61.8576f
+0:744 = 40.0000f 0:745 = 40.0000f 0:746 = 227.3520f
+0:747 = 223.3680f 0:748 = 227.3520f 0:749 = 223.3680f
+0:750 = 61.8576f 0:751 = 40.0000f 0:752 = 434.7120f
+0:753 = 227.3520f 0:754 = 223.3680f 0:755 = 227.3520f
+0:756 = 223.3680f 0:757 = 434.7120f 0:758 = 227.3520f
+0:759 = 223.3680f 0:760 = 227.3520f 0:761 = 223.3680f
+0:762 = 434.7120f 0:763 = 227.3520f 0:764 = 223.3680f
+0:765 = 227.3520f 0:766 = 223.3680f 0:767 = 434.7120f
+0:768 = 227.3520f 0:769 = 223.3680f 0:770 = 296.4720f
+0:771 = 113.9280f 0:772 = 61.8576f 0:773 = 17.6192f
+0:774 = 35.4816f 0:775 = 53.3600f 0:776 = 40.0000f
+0:777 = 80.0000f 0:778 = 40.0000f 0:779 = 1.2737p
+0:780 = 223.3680f 0:781 = 365.5920f 0:782 = 361.6080f
+0:783 = 227.3520f 0:784 = 1.2803p 0:785 = 40.0000f
+0:786 = 79.6064f 0:787 = 630.6560f 0:788 = 625.3440f
+0:789 = 447.9840f 0:790 = 625.3440f 0:791 = 227.3520f
+0:792 = 223.3680f 0:793 = 296.4720f 0:794 = 227.3520f
+0:795 = 223.3680f 0:796 = 296.4720f 0:797 = 227.3520f
+0:798 = 223.3680f 0:799 = 296.4720f 0:800 = 434.7120f
+0:801 = 223.3680f 0:802 = 223.3680f 0:803 = 223.3680f
+0:804 = 223.3680f 0:805 = 365.5920f 0:806 = 361.6080f
+0:807 = 223.3680f 0:808 = 223.3680f 0:809 = 223.3680f
+0:810 = 365.5920f 0:811 = 499.8480f 0:812 = 223.3680f
+0:813 = 223.3680f 0:814 = 296.4720f 0:815 = 223.3680f
+0:816 = 914.5680f 0:817 = 430.7280f 0:818 = 361.6080f
+0:819 = 223.3680f 0:820 = 138.2400f 0:821 = 227.3520f
+0:822 = 552.9600f 0:823 = 223.3680f 0:824 = 296.4720f
+0:825 = 227.3520f 0:826 = 223.3680f 0:827 = 296.4720f
+0:828 = 227.3520f 0:829 = 223.3680f 0:830 = 223.3680f
+0:831 = 361.6080f 0:832 = 365.5920f 0:833 = 125.8163f
+0:834 = 207.3600f 0:835 = 207.3600f 0:836 = 100.7437f
+0:837 = 125.8163f 0:838 = 207.3600f 0:839 = 207.3600f
+0:840 = 100.7437f 0:841 = 215.8976f 0:842 = 299.5661f
+0:843 = 227.3520f 0:844 = 223.3680f 0:845 = 296.4720f
+0:846 = 113.9280f 0:847 = 80.0000f 0:848 = 40.0000f
+0:849 = 630.6560f 0:850 = 42.9184f 0:851 = 17.6192f
+0:852 = 53.3600f 0:853 = 301.1280f 0:854 = 40.0000f

+0:855 = 61.8576f 0:856 = 40.0000f 0:857 = 305.1120f
+0:858 = 125.8163f 0:859 = 100.7437f 0:860 = 125.8163f
+0:861 = 100.7437f 0:862 = 218.0224f 0:863 = 227.3520f
+0:864 = 227.3520f 0:865 = 223.3680f 0:866 = 296.4720f
+0:867 = 227.3520f 0:868 = 223.3680f 0:869 = 296.4720f
+0:870 = 227.3520f 0:871 = 223.3680f 0:872 = 227.3520f
+0:873 = 223.3680f 0:874 = 223.3680f 0:875 = 223.3680f
+0:876 = 223.3680f 0:877 = 361.6080f 0:878 = 223.3680f
+0:879 = 223.3680f 0:880 = 223.3680f 0:881 = 361.6080f
+0:882 = 223.3680f 0:883 = 223.3680f 0:884 = 292.4880f
+0:885 = 227.3520f 0:886 = 223.3680f 0:887 = 223.3680f
+0:888 = 361.6080f 0:889 = 365.5920f 0:890 = 207.3600f
+0:891 = 207.3600f 0:892 = 207.3600f 0:893 = 227.3520f
+0:894 = 223.3680f 0:895 = 207.3600f 0:896 = 299.5661f
+0:897 = 296.4720f 0:898 = 113.9280f 0:899 = 61.8576f
+0:900 = 138.2400f 0:901 = 552.9600f 0:902 = 17.6192f
+0:903 = 35.4816f 0:904 = 53.3600f 0:905 = 40.0000f
+0:906 = 625.3440f 0:907 = 447.9840f 0:908 = 434.7120f
+0:909 = 499.8480f 0:910 = 296.4720f 0:911 = 223.3680f
+0:912 = 227.3520f 0:913 = 223.3680f 0:914 = 711.1920f
+0:915 = 361.6080f 0:916 = 630.6560f 0:917 = 80.0000f
+0:918 = 40.0000f 0:919 = 276.4800f 0:920 = 415.4294f
+0:921 = 276.4800f 0:922 = 446.0266f 0:923 = 276.4800f
+0:924 = 415.4294f 0:925 = 276.4800f 0:926 = 630.6560f
+0:927 = 625.3440f 0:928 = 40.0000f 0:929 = 79.6064f
+0:930 = 419.4134f 0:931 = 726.4905f 0:932 = 419.4134f
+0:933 = 726.4905f 0:934 = 361.6080f 0:935 = 365.5920f
+0:936 = 365.5920f 0:937 = 223.3680f 0:938 = 227.3520f
+0:939 = 223.3680f 0:940 = 227.3520f 0:941 = 223.3680f
+0:942 = 223.3680f 0:943 = 125.8163f 0:944 = 207.3600f
+0:945 = 207.3600f 0:946 = 100.7437f 0:947 = 125.8163f
+0:948 = 207.3600f 0:949 = 207.3600f 0:950 = 100.7437f
+0:951 = 215.8976f 0:952 = 299.5661f 0:953 = 227.3520f
+0:954 = 223.3680f 0:955 = 296.4720f 0:956 = 113.9280f
+0:957 = 80.0000f 0:958 = 40.0000f 0:959 = 42.9184f
+0:960 = 17.6192f 0:961 = 53.3600f 0:962 = 40.0000f
+0:963 = 61.8576f 0:964 = 40.0000f 0:965 = 691.2000f
+0:966 = 276.4800f 0:967 = 276.4800f 0:968 = 276.4800f
+0:969 = 276.4800f 0:970 = 227.3520f 0:971 = 223.3680f
+0:972 = 227.3520f 0:973 = 223.3680f 0:974 = 227.3520f
+0:975 = 223.3680f 0:976 = 227.3520f 0:977 = 223.3680f
+0:978 = 434.7120f 0:979 = 113.9280f 0:980 = 61.8576f
+0:981 = 361.6080f 0:982 = 17.6192f 0:983 = 35.4816f
+0:984 = 53.3600f 0:985 = 40.0000f 0:986 = 80.0000f
+0:987 = 40.0000f 0:988 = 40.0000f 0:989 = 227.3520f
+0:990 = 223.3680f 0:991 = 296.4720f 0:992 = 552.9600f
+0:993 = 414.7200f 0:994 = 113.9280f 0:995 = 61.8576f
+0:996 = 125.8163f 0:997 = 100.7437f 0:998 = 125.8163f
+0:999 = 100.7437f 0:1000 = 218.0224f 0:1001 = 207.3600f
+0:1002 = 207.3600f 0:1003 = 207.3600f 0:1004 = 207.3600f
+0:1005 = 299.5661f 0:1006 = 17.6192f 0:1007 = 35.4816f

+0:1008 = 53.3600f 0:1009 = 40.0000f 0:1010 = 80.0000f
+0:1011 = 40.0000f 0:1012 = 40.0000f 0:1013 = 227.3520f
+0:1014 = 299.5661f 0:1015 = 223.3680f 0:1016 = 296.4720f
+0:1017 = 113.9280f 0:1018 = 80.0000f 0:1019 = 40.0000f
+0:1020 = 292.4880f 0:1021 = 227.3520f 0:1022 = 223.3680f
+0:1023 = 227.3520f 0:1024 = 292.4880f 0:1025 = 227.3520f
+0:1026 = 223.3680f 0:1027 = 227.3520f 0:1028 = 223.3680f
+0:1029 = 227.3520f 0:1030 = 223.3680f 0:1031 = 227.3520f
+0:1032 = 223.3680f 0:1033 = 430.7280f 0:1034 = 113.9280f
+0:1035 = 80.0000f 0:1036 = 40.0000f 0:1037 = 42.9184f
+0:1038 = 17.6192f 0:1039 = 42.9184f 0:1040 = 17.6192f
+0:1041 = 169.8637f 0:1042 = 276.4800f 0:1043 = 125.8163f
+0:1044 = 125.8163f 0:1045 = 207.3600f 0:1046 = 207.3600f
+0:1047 = 100.7437f 0:1048 = 125.8163f 0:1049 = 207.3600f
+0:1050 = 207.3600f 0:1051 = 100.7437f 0:1052 = 215.8976f
+0:1053 = 53.3600f 0:1054 = 40.0000f 0:1055 = 53.3600f
+0:1056 = 40.0000f 0:1057 = 61.8576f 0:1058 = 40.0000f
+0:1059 = 61.8576f 0:1060 = 40.0000f 0:1061 = 125.8163f
+0:1062 = 100.7437f 0:1063 = 125.8163f 0:1064 = 100.7437f
+0:1065 = 125.8163f 0:1066 = 100.7437f 0:1067 = 344.9631f
+0:1068 = 691.2000f 0:1069 = 99.7560f 0:1070 = 23.2136f
+0:1071 = 61.8936f 0:1072 = 218.3280f 0:1073 = 33.5880f
+0:1074 = 345.6000f 0:1075 = 218.3280f 0:1076 = 35.1888f
+0:1077 = 21.6000f 0:1078 = 24.0000f 0:1079 = 75.2112f
+0:1080 = 384.1056f 0:1081 = 3.8880p 0:1082 = 1.4944p
+0:1083 = 125.8163f 0:1084 = 100.7437f 0:1085 = 125.8163f
+0:1086 = 100.7437f 0:1087 = 125.8163f 0:1088 = 100.7437f
+0:1089 = 344.9631f 0:1090 = 691.2000f 0:1091 = 99.7560f
+0:1092 = 23.2136f 0:1093 = 61.8936f 0:1094 = 218.3280f
+0:1095 = 33.5880f 0:1096 = 345.6000f 0:1097 = 218.3280f
+0:1098 = 35.1888f 0:1099 = 21.6000f 0:1100 = 24.0000f
+0:1101 = 75.2112f 0:1102 = 384.1056f 0:1103 = 1.4944p
+0:1104 = 125.8163f 0:1105 = 100.7437f 0:1106 = 125.8163f
+0:1107 = 100.7437f 0:1108 = 125.8163f 0:1109 = 100.7437f
+0:1110 = 344.9631f 0:1111 = 691.2000f 0:1112 = 99.7560f
+0:1113 = 23.2136f 0:1114 = 61.8936f 0:1115 = 218.3280f
+0:1116 = 33.5880f 0:1117 = 345.6000f 0:1118 = 218.3280f
+0:1119 = 35.1888f 0:1120 = 21.6000f 0:1121 = 24.0000f
+0:1122 = 75.2112f 0:1123 = 384.1056f 0:1124 = 1.4944p
+0:1125 = 125.8163f 0:1126 = 100.7437f 0:1127 = 125.8163f
+0:1128 = 100.7437f 0:1129 = 125.8163f 0:1130 = 100.7437f
+0:1131 = 344.9631f 0:1132 = 691.2000f 0:1133 = 99.7560f
+0:1134 = 23.2136f 0:1135 = 61.8936f 0:1136 = 218.3280f
+0:1137 = 33.5880f 0:1138 = 345.6000f 0:1139 = 218.3280f
+0:1140 = 35.1888f 0:1141 = 21.6000f 0:1142 = 24.0000f
+0:1143 = 75.2112f 0:1144 = 384.1056f 0:1145 = 1.4944p
+0:1146 = 125.8163f 0:1147 = 100.7437f 0:1148 = 125.8163f
+0:1149 = 100.7437f 0:1150 = 125.8163f 0:1151 = 100.7437f
+0:1152 = 344.9631f 0:1153 = 691.2000f 0:1154 = 99.7560f
+0:1155 = 23.2136f 0:1156 = 61.8936f 0:1157 = 218.3280f
+0:1158 = 33.5880f 0:1159 = 345.6000f 0:1160 = 218.3280f

+0:1161 = 35.1888f 0:1162 = 21.6000f 0:1163 = 24.0000f
+0:1164 = 75.2112f 0:1165 = 384.1056f 0:1166 = 1.4944p
+0:1167 = 125.8163f 0:1168 = 100.7437f 0:1169 = 125.8163f
+0:1170 = 100.7437f 0:1171 = 125.8163f 0:1172 = 100.7437f
+0:1173 = 344.9631f 0:1174 = 691.2000f 0:1175 = 99.7560f
+0:1176 = 23.2136f 0:1177 = 61.8936f 0:1178 = 218.3280f
+0:1179 = 33.5880f 0:1180 = 345.6000f 0:1181 = 218.3280f
+0:1182 = 35.1888f 0:1183 = 21.6000f 0:1184 = 24.0000f
+0:1185 = 75.2112f 0:1186 = 384.1056f 0:1187 = 1.4944p
+0:1188 = 125.8163f 0:1189 = 100.7437f 0:1190 = 125.8163f
+0:1191 = 100.7437f 0:1192 = 125.8163f 0:1193 = 100.7437f
+0:1194 = 344.9631f 0:1195 = 691.2000f 0:1196 = 99.7560f
+0:1197 = 23.2136f 0:1198 = 61.8936f 0:1199 = 218.3280f
+0:1200 = 33.5880f 0:1201 = 345.6000f 0:1202 = 218.3280f
+0:1203 = 35.1888f 0:1204 = 21.6000f 0:1205 = 24.0000f
+0:1206 = 75.2112f 0:1207 = 384.1056f 0:1208 = 1.4944p
+0:1209 = 125.8163f 0:1210 = 100.7437f 0:1211 = 125.8163f
+0:1212 = 100.7437f 0:1213 = 125.8163f 0:1214 = 100.7437f
+0:1215 = 344.9631f 0:1216 = 691.2000f 0:1217 = 99.7560f
+0:1218 = 23.2136f 0:1219 = 61.8936f 0:1220 = 218.3280f
+0:1221 = 33.5880f 0:1222 = 345.6000f 0:1223 = 218.3280f
+0:1224 = 35.1888f 0:1225 = 21.6000f 0:1226 = 24.0000f
+0:1227 = 75.2112f 0:1228 = 384.1056f 0:1229 = 1.4944p
+0:1230 = 125.8163f 0:1231 = 100.7437f 0:1232 = 125.8163f
+0:1233 = 100.7437f 0:1234 = 125.8163f 0:1235 = 100.7437f
+0:1236 = 344.9631f 0:1237 = 691.2000f 0:1238 = 99.7560f
+0:1239 = 23.2136f 0:1240 = 61.8936f 0:1241 = 218.3280f
+0:1242 = 33.5880f 0:1243 = 345.6000f 0:1244 = 218.3280f
+0:1245 = 35.1888f 0:1246 = 21.6000f 0:1247 = 24.0000f
+0:1248 = 75.2112f 0:1249 = 384.1056f 0:1250 = 1.4944p
+0:1251 = 125.8163f 0:1252 = 100.7437f 0:1253 = 125.8163f
+0:1254 = 100.7437f 0:1255 = 125.8163f 0:1256 = 100.7437f
+0:1257 = 344.9631f 0:1258 = 691.2000f 0:1259 = 99.7560f
+0:1260 = 23.2136f 0:1261 = 61.8936f 0:1262 = 218.3280f
+0:1263 = 33.5880f 0:1264 = 345.6000f 0:1265 = 218.3280f
+0:1266 = 35.1888f 0:1267 = 21.6000f 0:1268 = 24.0000f
+0:1269 = 75.2112f 0:1270 = 384.1056f 0:1271 = 1.4944p
+0:1272 = 125.8163f 0:1273 = 100.7437f 0:1274 = 125.8163f
+0:1275 = 100.7437f 0:1276 = 125.8163f 0:1277 = 100.7437f
+0:1278 = 344.9631f 0:1279 = 691.2000f 0:1280 = 99.7560f
+0:1281 = 23.2136f 0:1282 = 61.8936f 0:1283 = 218.3280f
+0:1284 = 33.5880f 0:1285 = 345.6000f 0:1286 = 218.3280f
+0:1287 = 35.1888f 0:1288 = 21.6000f 0:1289 = 24.0000f
+0:1290 = 75.2112f 0:1291 = 384.1056f 0:1292 = 1.4944p
+0:1293 = 125.8163f 0:1294 = 100.7437f 0:1295 = 125.8163f
+0:1296 = 100.7437f 0:1297 = 125.8163f 0:1298 = 100.7437f
+0:1299 = 344.9631f 0:1300 = 691.2000f 0:1301 = 99.7560f
+0:1302 = 23.2136f 0:1303 = 61.8936f 0:1304 = 218.3280f
+0:1305 = 33.5880f 0:1306 = 345.6000f 0:1307 = 218.3280f
+0:1308 = 35.1888f 0:1309 = 21.6000f 0:1310 = 24.0000f
+0:1311 = 75.2112f 0:1312 = 384.1056f 0:1313 = 1.4944p

```
 Opening plot unit= 15
file=gdram0.tr0

** spice file created for circuit gaasdram0  1/10/93 mike morris
****** transient analysis           tnom= 25.000 temp= 25.000
******
 vds_avgpwr    = -2.4510E+00 from= 0.0000E+00   to= 6.0000E-08
 vrefb_avgpwr  = -9.1525E-04 from= 0.0000E+00   to= 6.0000E-08
 vrefd_avgpwr  =  1.3509E-06 from= 0.0000E+00   to= 6.0000E-08
 vss_avgpwr    = -1.5365E-01 from= 0.0000E+00   to= 6.0000E-08

      ***** job concluded
** spice file created for circuit gaasdram0  1/10/93 mike morris
****** job statistics summary        tnom= 25.000 temp= 25.000
******

# nodes =  9864 # elements=  4423 # real*8 mem avail/used= 1000000/  945198
# diodes=    0 # bjts   =    0 # jfets  =  4324 # mosfets =    0

  analysis    time    # points  tot. iter  conv.iter

  op point      119.45       1       74
  transient   41472.89     121    20785     1348 rev= 1086
  input+setup  1050.62
  pass1          13.91
  readin         95.55
  errchk        268.71
  setup         672.45
  output          0.13
     total cpu time     42642.29 seconds
       job started at  10:47:32  6-feb93
       job ended  at  11:24: 7  7-feb93


I am done with gdram0.sp
Sun Feb  7 11:24:09 PST 1993
```

2. Run #2 LISTING FILE (Abbreviated)

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
 reading design configuration file: gdram1.cfg
**warning** illegal config file syntax on line=21
 of file=gdram1.cfg
=>plotsetup pr12 pscript<=
```

```
**warning** illegal config file syntax on line=21
 of file=gdram1.cfg
=>plotsetup pr12 pscript<=
setting user memory from  config file    to  1000000 words. (  8000000 bytes)

 ******    h s p i c e   9007d         10:41:55  6-feb93  sun
** spice file created for circuit gaasdram1.sp 1/10/93 mike morris
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
**

** node: 0 = gnd
** node: 1 = vdd
probe q1=v(651) q2=v(816) q0n=v(472) q1n=v(473) q2n=v(467)
+ ao0=v(439) ao1=v(600) ao2=v(599)
+ ma2cdo=v(548) ma2cde=v(459) ma2rc6=v(546) ma2rc4=v(545) ma2rc2=v(523)
+ ma2rc0=v(506) ma2rc7=v(461) ma2rc5=v(460) ma2rc3=v(463) ma2rc1=v(464)
+ ma2epu=v(507) ma2epd=v(483) ma2opu=v(462) ma2opd=v(482)
+ ma2ebio=v(455) ma2obio=v(450)
+ ma1cdo=v(360) ma1cde=v(312) ma1rc6=v(359) ma1rc4=v(358) ma1rc2=v(347)
+ ma1rc0=v(337) ma1rc7=v(314) ma1rc5=v(313)

.options fast ft=0.95 fs=.95 imin=16.0 imax=16.0 delmax=1.0s  rmax=8.0
+ scale=1e-06 brief=0 nopage measout post probe gmindc=1e-11 captab acct

*.options scale=1e-06 probe post gmindc=1e-11 acct captab
.end


**warning**  the fast option decreases  the cpu time but results may be
          less accurate.
***fast option sets default value of the options:
 dvdt= 1       rmax=  8.00     fs= 950.00m     ft= 950.00m
relvar= 400.00m absvar=  1.00  relmos= 100.00m absmos=  10.00u
**warning** could not find branch element    0:vrvrf
   branch - output ignored
** spice file created for circuit gaasdram1.sp 1/10/93 mike morris
 Opening plot unit= 15
file=gdram1.tr0

** spice file created for circuit gaasdram1.sp 1/10/93 mike morris
******  transient analysis            tnom=  25.000 temp=  25.000
******
 vds_avgpwr     = -2.4510E+00  from=  0.0000E+00    to=  6.0000E-08
 vrefb_avgpwr   = -9.1525E-04  from=  0.0000E+00    to=  6.0000E-08
 vrefd_avgpwr   =  1.3509E-06  from=  0.0000E+00    to=  6.0000E-08
 vss_avgpwr     = -1.5365E-01  from=  0.0000E+00    to=  6.0000E-08
```

```
      ***** job concluded
** spice file created for circuit gaasdram1.sp 1/10/93 mike morris
****** job statistics summary          tnom= 25.000 temp= 25.000
******

# nodes = 9864 # elements= 4423 # real*8 mem avail/used= 1000000/ 945198
# diodes=    0 # bjts   =    0 # jfets  = 4324 # mosfets =    0

  analysis     time     # points  tot. iter  conv.iter

  op point      119.34        1       74
  transient   41435.61      121    20785     1348 rev= 1086
  input+setup  1049.63
  pass1          13.93
  readin         95.62
  errchk        267.69
  setup         672.39
  output          0.11
      total cpu time     42603.93 seconds
        job started at  10:41:55  6-feb93
        job ended  at  11:19:20  7-feb93


I am done with gdram1.sp
Sun Feb  7 11:19:22 PST 1993
```

3. Run #3 LISTING FILE (Abbreviated)

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
 reading design configuration file: gdram2.cfg
setting user memory from  config file    to  1000000 words. (  8000000 bytes)

******    h s p i c e   9007d        13:26:15  7-feb93   sun
** spice file created for circuit gdram2.sp  1/7/93
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
**

** node: 0 = gnd
** node: 1 = vdd
.probe ma1rc3=v(316) ma1rc1=v(317) ma1epu=v(338) ma1epd=v(329) ma1opu=v(315)
+ ma1opd=v(318) ma1ebio=v(311) ma1obio=v(306)
+ ph1=v(297) ph1l=v(177) ph2=v(243) ph2ld=v(191)
+ ma0cdo=v(218) ma0cde=v(178) ma0rc6=v(216) ma0rc4=v(215) ma0rc2=v(206)
```

```
+ ma0rc0=v(193) ma0rc7=v(181) ma0rc5=v(180) ma0rc3=v(186) ma0rc1=v(189)
+ ma0epu=v(195) ma0epd=v(192) ma0opu=v(184) ma0opd=v(190)
+ ma0ebio=v(174) ma0obio=v(168)
+ ev=v(183) evu=v(175) od=v(219) odu=v(169)

.options fast ft=0.95 fs=.95 imin=16.0 imax=16.0 delmax=1.0s  rmax=8.0
+ scale=1e-06 brief=0 nopage measout post probe gmindc=1e-11 captab acct
*.options scale=1e-06 probe post gmindc=1e-11 acct captab
.end
**warning** the fast option decreases the cpu time but results may be
          less accurate.
***fast option sets default value of the options:
 dvdt= 1       rmax=  8.00     fs= 950.00m     ft= 950.00m
relvar= 400.00m absvar=  1.00  relmos= 100.00m absmos=  10.00u
**warning** could not find branch element     0:vrvrf
   branch - output ignored
** spice file created for circuit gdram2.sp  1/7/93
 Opening plot unit= 15
file=gdram2.tr0

** spice file created for circuit gdram2.sp  1/7/93
****** transient analysis            tnom=  25.000 temp=  25.000
******
 vds_avgpwr    = -2.4510E+00 from=  0.0000E+00    to=  6.0000E-08
 vrefb_avgpwr  = -9.1525E-04 from=  0.0000E+00    to=  6.0000E-08
 vrefd_avgpwr  =  1.3509E-06 from=  0.0000E+00    to=  6.0000E-08
 vss_avgpwr    = -1.5365E-01 from=  0.0000E+00    to=  6.0000E-08

     ***** job concluded
** spice file created for circuit gdram2.sp  1/7/93
****** job statistics summary          tnom=  25.000 temp=  25.000
******

# nodes =  9864 # elements=  4423 # real*8 mem avail/used= 1000000/ 945318
# diodes=    0 # bjts   =    0 # jfets  =  4324 # mosfets =    0

  analysis     time     # points  tot. iter  conv.iter

  op point       120.28        1       74
  transient    41639.32      241    20785      1348 rev= 1086
  input+setup   1052.76
  pass1           14.15
  readin          95.82
  errchk         268.98
  setup          673.81
  output           0.12
      total cpu time     42811.84 seconds
         job started at  13:26:15  7-feb93
         job ended  at  14:35: 2  8-feb93
```

I am done with gdram2.sp
Mon Feb 8 14:35:06 PST 1993

4. Run #4 LISTING FILE (Abbreviated)

```
Using: /tools3/cad/meta/h9007/sun4.1/hspice
lic: license granted by the license server for hspice
lic: from permit file: /tools3/cad/meta/h9007/permit.hsp
 reading install configuration file: /tools3/cad/meta/h9007/meta.cfg
 reading design configuration file: gdram3.cfg
setting user memory from  config file     to  1000000 words. (  8000000 bytes)

 ******    h s p i c e   9007d         13:26:27  7-feb93   sun
** spice file created for circuit gdram3.sp  2/7/93
****** copyright 1990 meta-software,inc. *****site:
******  input listing
******
* hspice.ini
** technology: edgaas
**

** node: 0 = gnd
** node: 1 = vdd
tran  250ps 60ns


.measure tran vds_avgpwr avg p(vds) from 0.0ns to 60ns
.measure tran vrefb_avgpwr avg p(vrefb) from 0.0ns to 60ns
.measure tran vrefd_avgpwr avg p(vrefd) from 0.0ns to 60ns
.measure tran vrvref_avgpwr avg p(vrvrf) from 0.0ns to 60ns
.measure tran vss_avgpwr avg p(vss) from 0.0ns to 60ns




.probe tran p(vds) p(vss) p(vrefb) p(vrefd) p(vrvref) power
*                                          80 columns->>*
.probe da7=v(182) da6=v(217) da5=v(179) da4=v(214) da3=v(187) da2=v(205)
+ da1=v(188) da0=v(194)
+ do0=v(147) do1=v(139) do2=v(131) do3=v(123)
+ drdy=v(107) mbsy=v(115) refresh=v(1124) irefresh=v(466) mrefresh=v(598)

.options fast ft=0.95 fs=.95 imin=16.0 imax=16.0 delmax=1.0s  rmax=8.0
+ scale=1e-06 brief=0 nopage measout post probe gmindc=1e-11 captab acct
.end


**warning** the fast option decreases  the cpu time but results may be
            less accurate.
```

```
***fast option sets default value of the options:
 dvdt= 1       rmax=  8.00     fs= 950.00m    ft= 950.00m
relvar= 400.00m absvar=  1.00  relmos= 100.00m absmos=  10.00u
**warning** could not find branch element    0:vrvrf
   branch - output ignored
** spice file created for circuit gdram3.sp  2/7/93
Opening plot unit= 15
file=gdram3.tr0

** spice file created for circuit gdram3.sp  2/7/93
******  transient analysis            tnom=  25.000 temp=  25.000
******
 vds_avgpwr    = -2.4510E+00 from=  0.0000E+00    to=  6.0000E-08
 vrefb_avgpwr  = -9.1525E-04 from=  0.0000E+00    to=  6.0000E-08
 vrefd_avgpwr  =  1.3509E-06 from=  0.0000E+00    to=  6.0000E-08
 vss_avgpwr    = -1.5365E-01 from=  0.0000E+00    to=  6.0000E-08

     ***** job concluded
** spice file created for circuit gdram3.sp  2/7/93
******  job statistics summary        tnom=  25.000 temp=  25.000
******

# nodes =  9864 # elements=  4423 # real*8 mem avail/used= 1000000/  945278
# diodes=    0 # bjts   =    0 # jfets  =  4324 # mosfets =    0

  analysis    time    # points  tot. iter  conv.iter

  op point      121.01       1       74
  transient   41769.61     241    20785     1348 rev= 1086
  input+setup   1051.88
  pass1          13.80
  readin         95.87
  errchk        268.04
  setup         674.17
  output          0.11
     total cpu time     42941.87 seconds
        job started at  13:26:27  7-feb93
        job ended  at  14:37:30  8-feb93


I am done with gdram3.sp
Mon Feb  8 14:37:33 PST 1993
```

U. Original HSPICE GaAs DRAM Source File

```
HSPICE -- gaasdram.sp  -- 06 August 1992
* ************************ HSPICE VERSION **********************************
* include Vitesse HGaAs3 models and parameters for hspice.
.pro`ect
.include '/tools3/cad/meta/h9007/lib/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h9007/lib/vitesse/hgaas3.corners' tt
```

```
.unprotect
*****************************************************************************
* Total pull-down/pull-up ratio is 16 to 1.
*****************************************************************************
* Subcircuit SBFL 2-input NOR
*                    INA   INB  OUTPUT POWER GROUND
.SUBCKT S2NOR  1      2       3         4         5
* D G S B
J0 8 1 5 0  JFET04 L=1.2 W=48.0
J1 8 2 5 0  JFET04 L=1.2 W=48.0
J2 4 8 8 0  JFET16 L=1.2 W=3.0
J3 4 8 3 0  JFET04 L=1.2 W=48.0
J4 3 2 5 0  JFET04 L=1.2 W=48.0
J5 3 1 5 0  JFET04 L=1.2 W=48.0
.ENDS   S2NOR
*****************************************************************************
* Subcircuit SBFL 3-input NOR
*                    INA   INB   INC  OUTPUT POWER GROUND
.SUBCKT S3NOR  1      2     3       4         5         6
* D G S B
J0 8 1 6 0  JFET04 L=1.2 W=48.0
J1 8 2 6 0  JFET04 L=1.2 W=48.0
J2 8 3 6 0  JFET04 L=1.2 W=48.0
J3 5 8 8 0  JFET16 L=1.2 W=3.0
J4 5 8 4 0  JFET04 L=1.2 W=48.0
J5 4 1 6 0  JFET04 L=1.2 W=48.0
J6 4 2 6 0  JFET04 L=1.2 W=48.0
J7 4 3 6 0  JFET04 L=1.2 W=48.0
.ENDS   S3NOR
*****************************************************************************
* Subcircuit SBFL 4-input NOR
*                    INA INB INC IND OUTPUT POWER GROUND
.SUBCKT S4NOR  1    2    3   4       5         6         7
* D G S B
J0  8 1 7 0  JFET04 L=1.2 W=48.0
J1  8 2 7 0  JFET04 L=1.2 W=48.0
J2  8 3 7 0  JFET04 L=1.2 W=48.0
J3  8 4 7 0  JFET04 L=1.2 W=48.0
J4  6 8 8 0  JFET16 L=1.2 W=3.0
J5  6 8 5 0  JFET04 L=1.2 W=48.0
J6  5 1 7 0  JFET04 L=1.2 W=48.0
J7  5 2 7 0  JFET04 L=1.2 W=48.0
J8  5 3 7 0  JFET04 L=1.2 W=48.0
J9  5 4 7 0  JFET04 L=1.2 W=48.0
.ENDS     S4NOR
*****************************************************************************
* Subcircuit SBFL 3-input OR
*                    INA   INB   INC  OUTPUT POWER GROUND
.SUBCKT S3OR   1      2     3       4         5         6
*  INA INB INC OUT PWR GND SUBNAME
X0  1   2   3    7    5    6    S3NOR
```

```
X1 7          4   5   6   SINV
.ENDS   S3OR
*******************************************************************************
* Subcircuit SBFL 2-input NAND
*                    INA   INB  OUTPUT POWER GROUND
.SUBCKT SS2NAND  1     2      3        4        5
*  INA INB OUT PWR GND SUBNAME
X0 1         9    4    5   SINV
X1 2         6    4    5   SINV
X2 9   6     7    4    5   S2NOR
X3 7         3    4    5   SINV
.ENDS   SS2NAND
*******************************************************************************
* Subcircuit SBFL 4-input NAND
*                    INA INB INC IND OUTPUT POWER GROUND
.SUBCKT SS4NAND 1    2   3   4       5        6        7
*  INA INB INC IND OUT PWR GND SUBNAME
X0 1                 9    6    7   SINV
X1 2                 10   6    7   SINV
X2 3                 11   6    7   SINV
X3 4                 12   6    7   SINV
X4 9   10  11  12    8    6    7    S4NOR
X5 8                 5    6    7   SINV
.ENDS   SS4NAND
*******************************************************************************
* Subcircuit SBFL 3-input AND
*                    INA  INB  INC  OUTPUT POWER GROUND
.SUBCKT SS3AND  1    2    3       4        5        6
*  INA INB INC OUT PWR GND SUBNAME
X0 1              9    5    6   SINV
X1 2              10   5    6   SINV
X2 3              11   5    6   SINV
X3 9   10  11     4    5    6   S3NOR
.ENDS   SS3AND
*******************************************************************************
* Subcircuit SBFL 4-input AND
*                    INA INB INC IND OUTPUT POWER GROUND
.SUBCKT SS4AND  1    2   3   4       5        6        7
*  INA INB INC IND OUT PWR GND SUBNAME
X0 1                 9    6    7   SINV
X1 2                 10   6    7   SINV
X2 3                 11   6    7   SINV
X3 4                 12   6    7   SINV
X4 9   10  11  12    5    6    7    S4NOR
.ENDS   SS4AND
*******************************************************************************
* Subcircuit SBFL INVERTER
*              INPUT OUTPUT POWER GROUND
.SUBCKT SINV   1       2        3        4
* D G S B
J0 9 1 4 0  JFET04 L=1.2 W=48.0
```

```
J1 3 9 9 0  JFET16 L=1.2 W=3.0
J2 3 9 2 0  JFET04 L=1.2 W=48.0
J3 2 1 4 0  JFET04 L=1.2 W=48.0
.ENDS    SINV
*********************************************************************************
* Subckt HSPICE SBFL LARGE 2-input NOR - Used in CLOCK
*                    INA INB OUTPUT POWER GROUND
.SUBCKT CSNOR   1    2       3        4        5
* D G S B
J0 8 1 5 0  JFET04 L=1.2 W=144.0
J1 8 2 5 0  JFET04 L=1.2 W=144.0
J2 4 8 8 0  JFET16 L=1.2 W= 9.0
J3 4 8 3 0  JFET04 L=1.2 W=144.0
J4 3 2 5 0  JFET04 L=1.2 W=144.0
J5 3 1 5 0  JFET04 L=1.2 W=144.0
.ENDS    CSNOR
*********************************************************************************
* HSPICE SBFL EXTRA-LARGE DRIVER-INVERTER SUBCIRCUIT - Used in CLOCK
*                  INPUT OUTPUT POWER GROUND
.SUBCKT SSINV   1        2        3        4
* D G S B
J0 9 1 4 0  JFET04 L=1.2 W=768.0
J1 3 9 9 0  JFET16 L=1.2 W= 48.0
J2 3 9 2 0  JFET04 L=1.2 W=768.0
J3 2 1 4 0  JFET04 L=1.2 W=768.0
.ENDS    SSINV
*********************************************************************************
* HSPICE SBFL LARGE  DRIVER-INVERTER SUBCIRCUIT - Used in CLOCK
*                  INPUT OUTPUT POWER GROUND
.SUBCKT CSINV   1        2        3        4
* D G S B
J0 9 1 4 0  JFET04 L=1.2 W=256.0
J1 3 9 9 0  JFET16 L=1.2 W= 16.0
J2 3 9 2 0  JFET04 L=1.2 W=384.0
J3 2 1 4 0  JFET04 L=1.2 W=384.0
.ENDS     CSINV
*********************************************************************************
* Subcircuit LVL Level-Shifter to Drive D-mode MESFETs
* USE HSPICE Diode Models for Backconnected MESFETS
*               INPUT OUTPUT VDS VSS
.SUBCKT LVL  1         2       3    4
* LVL is logically inverting, hence pre-invert using DINV
*  INPUT  OUTPUT  POWER  GROUND SUBNAME
X0   1         25        3         0      DINV
*    D  G    S   B
J1   3  25   6   4   JFET04 L=1.2 W=20.0
J2   7   6   7   4   DIO16  L=1.2 W=4.0
J3   7   4   4   4   JFET20 L=3.0 W=3.0
J4   3   9   9   4   JFET16 L=1.2 W=3.0
J5   9   7   0   4   JFET16 L=1.2 W=10.0
J6   3   9   10  4   JFET16 L=1.2 W=20.0
```

```
J7  11 10  11  4   DIO16 L=1.2 W=20.0
J8   2 11   2  4   DIO16 L=1.2 W=20.0
J9   2  4   4  4   JFET16 L=1.2 W=12.0
J10 12  2  12  4   DIO16 L=1.2 W=10.0
J11 13 12  13  4   DIO16 L=1.2 W=10.0
J12 14 13  14  4   DIO16 L=1.2 W=10.0
J13 4  14   4  4   DIO16 L=1.2 W=10.0
.ENDS     LVL
********************************************************************************
* Subcircuit DELAY - generates Clock Pulse Delay
*                INPUT  OUTPUT  POWER  GROUND
.SUBCKT DELAY   1        2        3        4
*   INA INB OUT POWER  GROUND  SUBNAME
X0   1        9      3        4      BDINV
X1   9        6      3        4      BDINV
X2   1    6   2      3        4      BS2AND
.ENDS    DELAY
********************************************************************************
* Subcircuit CLOCK - two-phase SBFL clock
*                INCLK PH1 PH2 PH2D PH1L PH2LD POWER1 POWER2  GROUND
.SUBCKT CLOCK  1      2   3   4     5     6       7        8          9
* INA INB OUT PWR GND SUBNAME
X0 1    2    10   7    9   CSNOR
X1 10        11   7    9   SSINV
X2 11         3   7    9   SSINV
X3 12   3    13   7    9   CSNOR
X4 13        14   7    9   SSINV
X5 14         2   7    9   SSINV
X6 1         12   7    9   CSINV
X7 3          4   7    9   DELAY
X8 2          5   7    8   LVL
X9 4          6   7    8   LVL
.ENDS    CLOCK
********************************************************************************
* Subcircuit DCFL INVERTER
*                INPUT OUTPUT POWER GROUND
.SUBCKT DINV   1        2        3        4
* D G S B
J0 3 2 2 4   JFET16 L=1.2 W=6.0
J1 2 1 4 4   JFET04 L=1.2 W=96.0
.ENDS    DINV
********************************************************************************
* Subcircuit DCFL LARGE INVERTER
*                INPUT OUTPUT POWER GROUND
.SUBCKT BDINV   1        2        3        4
* D G S B
j0 3 2 2 4   JFET20 L=3.0 W=40.0
J1 2 1 4 4   JFET04 L=1.2 W=240.0
.ENDS    BDINV
********************************************************************************
* Subcircuit SBFL LARGE 2-input NOR
```

```
*                    INA INB  OUTPUT POWER GROUND
.SUBCKT BS2NOR  1    2        3        4        5
* D G S B
J0 8 1 5 0  JFET04 L=1.2 W=180.0
J1 8 2 5 0  JFET04 L=1.2 W=180.0
J2 4 8 8 0  JFET16 L=1.2 W=10.0
J3 4 8 3 0  JFET04 L=1.2 W=224.0
J4 3 2 5 0  JFET04 L=1.2 W=224.0
J5 3 1 5 0  JFET04 L=1.2 W=224.0
.ENDS    BS2NOR
*****************************************************************************
* Subcircuit SBFL LARGE 2- input AND
*                    INA INB  OUTPUT POWER GROUND
.SUBCKT BS2AND  1    2        3        4        5
*  INA INB OUT PWR GND SUBNAME
X0 1         9    4    5   BDINV
X1 2         6    4    5   BDINV
X2 9    6    3    4    5   BS2NOR
.ENDS    BS2AND
*****************************************************************************
*Subcircuit  DCFL 2-INPUT NON-DeMORGAN NAND
*                     INA INB OUTPUT POWER GROUND
.SUBCKT D2NAND   1    2        3        4        5
* D G S B
J0 4 3 3 5  JFET16 L=1.2 W=6.0
J1 3 1 6 5  JFET04 L=1.2 W=192.0
J2 6 2 5 5  JFET04 L=1.2 W=192.0
.ENDS    D2NAND
*****************************************************************************
*Subcircuit  DCFL 2-INPUT NON-DeMORGAN AND
*                    INA INB OUTPUT POWER GROUND
.SUBCKT D2AND   1    2        3        4        5
*  INA INB OUT PWR GND SUBNAME
X0 1    2    6    4    5   D2NAND
X1 6         3    4    5   DINV
.ENDS    D2AND
*****************************************************************************
*Subcircuit DCFL 2-INPUT NOR
*                    INA INB OUTPUT POWER GROUND
.SUBCKT D2NOR    1    2        3        4        5
* D G S B
J0 4 3 3 5  JFET16 L=1.2 W=6.0
J1 3 1 5 5  JFET04 L=1.2 W=96.0
J2 3 2 5 5  JFET04 L=1.2 W=96.0
.ENDS    D2NOR
*****************************************************************************
*Subcircuit DCFL 2-INPUT DeMORGAN AND
*                     INA INB  OUTPUT POWER GROUND
.SUBCKT DD2AND   1    2        3        4        5
*  INA INB OUT PWR GND SUBNAME
X0 1         10   4    5   DINV
```

```
X1 2        11   4    5  DINV
X2 10  11    3 4 5 D2NOR
.ENDS   DD2AND
*********************************************************************************
*Subcircuit DCFL 2-INPUT DeMORGAN NAND
*                    INA INB  OUTPUT POWER GROUND
.SUBCKT DD2NAND  1    2       3        4        5
*  INA INB OUT PWR GND SUBNAME
X0 1        10   4    5  DINV
X1 2        11   4    5  DINV
X2 10  11   12   4    5  D2NOR
X3 12        3   4    5  DINV
.ENDS   DD2NAND
*********************************************************************************
* Subcircuit DCFL 2-INPUT DeMORGAN OR
*                   INA INB  OUTPUT POWER GROUND
.SUBCKT DD2OR   1    2       3        4        5
*  INA INB OUT PWR GND SUBNAME
X0  1   2    6    4    5  D2NOR
X1  6        3    4    5  DINV
.ENDS   DD2OR
*********************************************************************************
* Subcircuit DCFL 3-INPUT DeMORGAN OR
*                   INA INB INC  OUTPUT POWER GROUND
.SUBCKT DD3OR   1    2    3       4        5        6
*  INA INB INC OUT PWR GND SUBNAME
X0  1   2    3    7    5    6  D3NOR
X1  7             4    5    6  DINV
.ENDS   DD3OR
*********************************************************************************
* Subcircuit DCFL 4-INPUT DeMORGAN OR
*                   INA INB INC IND OUTPUT POWER GROUND
.SUBCKT DD4OR   1    2    3   4       5        6        7
*  INA INB INC IND OUT PWR GND SUBNAME
X0  1   2    3   4    8    6    7  D4NOR
X1  8             5    6    7  DINV
.ENDS   DD4OR
*********************************************************************************
* Subcircuit DCFL 3-INPUT NOR
*                    INA INB INC OUTPUT POWER GROUND
.SUBCKT D3NOR    1    2    3       4        5        6
* D G S B
J0 5 4 4 6  JFET16 L=1.2 W=6.0
J1 4 1 6 6  JFET04 L=1.2 W=96.0
J2 4 2 6 6  JFET04 L=1.2 W=96.0
J3 4 3 6 6  JFET04 L=1.2 W=96.0
.ENDS   D3NOR
*********************************************************************************
*Subcircuit  DCFL 3-INPUT DeMORGAN AND
*                    INA INB INC OUTPUT POWER GROUND
.SUBCKT DD3AND   1    2    3       4        5        6
```

```
*  INA INB INC OUT PWR GND SUBNAME
X0 1              10   5    6  DINV
X1 2              11   5    6  DINV
X2 3              12   5    6  DINV
X3 10  11   12    4    5    6  D3NOR
.ENDS    DD3AND
*******************************************************************************
*Subcircuit  DCFL 3-INPUT DeMORGAN NAND
*                    INA INB INC OUTPUT POWER GROUND
.SUBCKT DD3NAND  1    2    3       4       5       6
*  INA INB INC OUT PWR GND SUBNAME
X0 1              10   5    6  DINV
X1 2              11   5    6  DINV
X2 3              12   5    6  DINV
X3 10  11  12     13   5    6  D3NOR
X4 13             4    5    6  DINV
.ENDS    DD3NAND
*******************************************************************************
*Subcircuit  DCFL 4-INPUT NOR
*                    INA INB INC IND OUTPUT POWER GROUND
.SUBCKT D4NOR    1    2    3    4       5       6       7
* D G S B
J0 6 5 5 7  JFET16 L=1.2 W=6.0
J1 5 1 7 7  JFET04 L=1.2 W=96.0
J2 5 2 7 7  JFET04 L=1.2 W=96.0
J3 5 3 7 7  JFET04 L=1.2 W=96.0
J4 5 4 7 7  JFET04 L=1.2 W=96.0
.ENDS    D4NOR
*******************************************************************************
*Subcircuit  DCFL 4-INPUT DeMORGAN NAND
*                    INA INB INC IND OUTPUT POWER GROUND
.SUBCKT DD4NAND  1    2    3    4       5       6       7
*  INA INB INC IND OUT PWR GND SUBNAME
X0 1                10   6    7   DINV
X1 2                11   6    7   DINV
X2 3                12   6    7   DINV
X3 4                13   6    7   DINV
X4 10  11   12   13   14   6    7   D4NOR
X5 14               5    6    7   DINV
.ENDS    DD4NAND
*******************************************************************************
*Subcircuit  DCFL 4-INPUT DeMORGAN AND
*                    INA INB INC IND OUTPUT POWER GROUND
.SUBCKT DD4AND  1    2    3    4       5       6       7
*  INA INB INC IND OUT PWR GND SUBNAME
X0 1                10   6    7   DINV
X1 2                11   6    7   DINV
X2 3                12   6    7   DINV
X3 4                13   6    7   DINV
X4 10  11   12   13   5    6    7   D4NOR
.ENDS    DD4AND
```

```
*******************************************************************************
* Subcircuit DCFL D-LATCH Using Generic Gates
*                    D  CLK Q  /Q POWER GROUND
.SUBCKT DLATCH 1    2    3 4     5        6
*   INA  INB OUTPUT  POWER GROUND SUBNAME
X0   1    2      8        5        6     D2NAND
X1   1           7        5        6     DINV
X2   2    7      9        5        6     D2NAND
X3   8    4      3        5        6     D2NAND
X4   9    3      4        5        6     D2NAND
.ENDS   DLATCH
*******************************************************************************
* Subcircuit SBFL/DCFL SD-LATCH Using Generic Gates First Stage
*                    D  CLK Q  /Q POWER GROUND
.SUBCKT SDLATCH 1    2    3 4     5        6
*   INA  INB OUTPUT  POWER GROUND SUBNAME
X0   1    2      8        5        6     D2NAND
X1   1           7        5        6     DINV
X2   2    7      9        5        6     D2NAND
X3   8    4      3        5        6     SS2NAND
X4   9    3      4        5        6     SS2NAND
.ENDS   SDLATCH
*******************************************************************************
* Subcircuit SBFL DFF D Flip-Flop
***             D CLK Q /Q POWER GROUND
.SUBCKT DFF 1    2    3 4     5        6
*   INA INB D  CLK Q  /Q OUT POWER GROUND SUBNAME
X0          1    9    7  8         5        6     DLATCH
X1  2                      9       5        6     DINV
X2  9                      10      5        6     DINV
X3          7    10   3  4         5        6     DLATCH
.ENDS   DFF
*******************************************************************************
* Subcircuit DCFL CPDFF Clear D Flip Flop
* Wakerly pg 363 - 31July 1992
***                D CLK CLR  Q  /Q  POWER  GROUND
.SUBCKT CPDFF 1    2    3    4  5     6        7
*   INA INB INC OUT PWR GND SUBNAME
X0   12   10        9     6    7   DD2NAND
X1   9    3    2    10    6    7   DD3NAND
X2   10   2    12   11    6    7   DD3NAND
X3   11   3    1    12    6    7   DD3NAND
X4   10   5         4     6    7   DD2NAND
X5   4    3    11   5     6    7   DD3NAND
.ENDS   CPDFF
*******************************************************************************
* Subcircuit DCFL (with SBFL Outputs) D Flip-Flop
***             D CLK Q /Q POWER GROUND
.SUBCKT SDFF 1    2    3 4     5        6
*   INA INB D  CLK Q  /Q OUT POWER GROUND SUBNAME
X0          1    9    7  8         5        6     DLATCH
```

```
X1 2                    9     5     6     DINV
X2 9                    10    5     6     DINV
X3        7  10  3  4          5     6     SDLATCH
.ENDS   SDFF
*******************************************************************************
* Subcircuit SBFL/DCFL (Combination) 3-to-8 Non-Latched Decoder
****                A0 A1 A2 W  R  RE O0 O1 O2 O3 O4 O5 O6 O7 ENBL PWR GRND
.SUBCKT DECODER 1   2  3  4  5  6  7  8   9 10  11 12 13 14  15   16   17
*   INA INB INC IND    OUTPUT  POWER GROUND SUBNAME
X0  1                  20      16    17    DINV
X1  2                  18      16    17    DINV
X2  3                  19      16    17    DINV
X3  4   5   6          15      16    17    S3OR
X4  20  18  19  15      7       16    17    SS4AND
X5  1   18  19  15      8       16    17    SS4AND
X6  20  2   19  15      9       16    17    SS4AND
X7  1   2   19  15      10      16    17    SS4AND
X8  20  18  3   15      11      16    17    SS4AND
X9  1   18  3   15      12      16    17    SS4AND
X10 20  2   3   15      13      16    17    SS4AND
X11 1   2   3   15      14      16    17    SS4AND
.ENDS   DECODER
*******************************************************************************
* Subcircuit DCFL 3-bit COUNTER using clear D FFs (CPDFF)
***                 ENBLE CLK Q0 Q1 Q2 /Q0 /Q1 /Q2 POWER GROUND
.SUBCKT COUNTER 1     2   3  4  5  6   7   8    9      10
*** INA INB INC IND D CLK CLR Q  /Q OUT POWER GROUND SUBNAME
X0  1                          11     9      10    DINV
X1  3   11                     12     9      10    DD2AND
X2  1   6                      13     9      10    DD2AND
X3  12  13                     20     9      10    DD2OR
X4  4   11                     14     9      10    DD2AND
X5  4   6                      15     9      10    DD2AND
X6  3   7   1                  16     9      10    DD3AND
X7  14  15  16                 21     9      10    DD3OR
X8  5   7                      17     9      10    DD2AND
X9  5   6                      18     9      10    DD2AND
X10 1   3   4   8              19     9      10    DD4AND
X11 11  5                      23     9      10    DD2AND
X12 17  18  19  23             22     9      10    DD4OR
*** INA INB INC IND D CLK CLR Q  /Q OUT POWER GROUND SUBNAME
X13                20  2   1  3  6      9      10    CPDFF
X14                21  2   1  4  7      9      10    CPDFF
X15                22  2   1  5  8      9      10    CPDFF
.ENDS   COUNTER
*******************************************************************************
* Subcircuit DCFL/SBFL Combination REFRESH Circuit
*                       REF PH1 A0 A1 A2 AO0 AO1 AO2 MREF PWR GND
.SUBCKT DREFRESH  1     2   3  4  5  6   7   8    9     10   11
*** INA INB INC IND D CLK Q  /Q OUT POWER GROUND SUBNAME
X0  15  28  29  30             31     10     11    SS4NAND
```

```
X1                    31  2   9  33        10        11   SDFF
*** ENBLE  CLK Q0 Q1 Q2 /Q0 /Q1 /Q2 POWER GROUND
X2     31      2   25 26 27 28 29   30     10        11    COUNTER
X3   3                                12     10        11    DINV
X4   4                                13     10        11    DINV
X5   5                                14     10        11    DINV
X6   1                                15     10        11    DINV
X7   3  33                            16     10        11    DD2AND
X8   3  25                            17     10        11    DD2AND
X9  12  25   9                        18     10        11    DD3AND
X10  4  33                            19     10        11    DD2AND
X11  4  26                            20     10        11    DD2AND
X12 13 26   9                        21     10        11    DD3AND
X13  5  33                            22     10        11    DD2AND
X14  5  27                            23     10        11    DD2AND
X15 14 27   9                        24     10        11    DD3AND
X16 16  17  18                        6     10        11    DD3OR
X17 19  20  21                        7     10        11    DD3OR
X18 22  23  24                        8     10        11    DD3OR
* Following are initial conditions via HSPICE (Simulation only)
.IC v(25)=0.0 v(26)=0.0 v(27)=0.0 v(31)=0.0 v(9)=0.0
+ v(28)=0.63 v(29)=0.63 v(30)=0.63 v(33)=0.63
.ENDS    DREFRESH
********************************************************************************
* Subcircuit SBFL/DCFL Decoder/Driver "DECODDRVER"
**   1     2     3   4      5    6    7     8     9   10  11   12   13   14   15   16
** PH2D AO0 AO1 AO2 MREF MR MW DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7 EVU
    17   18 19    20    21      22
**ODU EV OD PWR1 PWR2 GND
.SUBCKT DECODDRVER 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
***A0 A1 A2 W  R  RE O0 O1 O2 O3 O4 O5 O6 O7 ENBL PWR GND SUBNAME
X0  2  3  4   7  6   5  30 31 32 33 34 35 36 37  50     20    22   DECODER
*** INA INB INC IND D CLK Q  /Q OUT  ENBL PWR GND  BULK   SUBNAME
X1  2                              48          20   22           DINV
X2  2     1   50                   17          20   22           SS3AND
X3  48    1   50                   16          20   22           SS3AND
X4  30    1                        40          20   22           DD2AND
X5  31    1                        41          20   22           DD2AND
X6  32    1                        42          20   22           DD2AND
X7  33    1                        43          20   22           DD2AND
X8  34    1                        44          20   22           DD2AND
X9  35    1                        45          20   22           DD2AND
X10 36    1                        46          20   22           DD2AND
X11 37    1                        47          20   22           DD2AND
X12 40                             8           20        21      LVL
X13 41                             9           20        21      LVL
X14 42                             10          20        21      LVL
X15 43                             11          20        21      LVL
X16 44                             12          20        21      LVL
X17 45                             13          20        21      LVL
X18 46                             14          20        21      LVL
```

```
X19 47                          15      20      21      LVL
X20 16                          18      20      21      LVL
X21 17                          19      20      21      LVL
.ENDS     DECODDRVER
*$
* Subcircuit OUTPUT
*                    ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND
.SUBCKT OUTPUT   1       2       3       4       5   6  7    8    9
*  INA  INB  INC  IND  OUT POWER GROUND SUBNAME
X0  1                   12      8       9       DINV
X1  2                   13      8       9       DINV
X2  3                   14      8       9       DINV
X3  4                   15      8       9       DINV
X4  1    4    13   14   17      8       9       DD4AND
X5  12   15   2    3    30      8       9       DD4AND
X6  1    15   2    3    31      8       9       DD4AND
X7  1    4    2    14   20      8       9       DD4AND
X8  17   30   31   20   21      8       9       DD4OR
X9  3    4              22      8       9       DD2OR
X10 5    22             16      8       9       DD2AND
*    D   CLK    Q   /Q          POWER  GROUND SUBNAME
X11 21   16     6   7               8       9       DLATCH
.ENDS   OUTPUT
*$
* Subcircuit WLOGIC - Write Logic
* EPU=Even Pull UP -- Bring in A0 for Even/Odd & Writing
*                    DATA DAS A0 MW CLK EPU EPD OPU OPD POWER GND VSS
.SUBCKT WLOGIC  1     2   3   4   5    6   7   8   9     10     11   12
*    D   CLK    Q   /Q          POWER  GROUND SUBNAME
X0  1    2      14  15              10      11      DLATCH
*  INA  INB  INC  IND  OUT POWER  GROUND SUBNAME
X1  3                   13   10         11      DINV
X2  13   14   4    5     16   10         11      DD4AND
X3  13   15   4    5     7    10         11      DD4AND
X4  4    3    14   5     17   10         11      DD4AND

X5  3    15   4    5     9    10         11      DD4AND
*   IN                  OUT  VDS   VSS          SUBNAME
X6 16                    6    10    12          LVL
X7 17                    8    10    12          LVL
.ENDS     WLOGIC
*$
* Subcircuit RAM Cell -- One Bit Position by Eight Addresses
* PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5 DA6 *DA7
EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx Pwr Gnd     *Vrefb Vrefd
.SUBCKT  RAM 1  2  3  4  5  6  7  8  9  10 11 12 13 14 15 16 17 18 19
+ 20 21 22 23 24 25 26 27 28 29 30 31 32 33
*    D   G   S   B
J0   30  3   18  31  JFET16 L=1.2 W=9.0
J1   30  3   19  31  JFET16 L=1.2 W=9.0
J2   18  10  20  31  JFET16 L=1.2 W=8.0
```

```
J3   18  9  29 31  JFET16 L=1.2 W=8.0
J4   18  19  31 31 JFET04 L=1.2 W=210.0
J5   19  18  31 31 JFET04 L=1.2 W=210.0
J6   19  8  28 31  JFET16 L=1.2 W=8.0
J7   19  11  21 31 JFET16 L=1.2 W=8.0
J8   33  1  28 31  JFET16 L=1.2 W=3.0
J10  30  6  18 31  JFET16 L=1.2 W=185.0
J11  30  4  19 31  JFET16 L=1.2 W=185.0
J12  18  7  31 31  JFET04 L=1.2 W=6.0
J13  19  5  31 31  JFET04 L=1.2 W=6.0
J14  19  1  18 31  JFET16 L=1.2 W=20.0
J15  18  12  22 31 JFET16 L=1.2 W=8.0
J16  18  14  24 31 JFET16 L=1.2 W=8.0
J17  18  16  26 31 JFET16 L=1.2 W=8.0
J18  19  13  23 31 JFET16 L=1.2 W=8.0
J19  19  15  25 31 JFET16 L=1.2 W=8.0
J20  19  17  27 31 JFET16 L=1.2 W=8.0
J21  33  1  29 31  JFET16 L=1.2 W=3.0
J23  32  1  19 31  JFET16 L=1.2 W=6.0
J25  32  1  18 31  JFET16 L=1.2 W=6.0
C0   20  31  620FF
C1   21  31  620FF
C2   29  31  70FF
C3   28  31  70FF
C4   22  31  620FF
C5   23  31  620FF
C6   24  31  620FF
C7   25  31  620FF
C8   26  31  620FF
C9   27  31  620FF
.ENDS    RAM
********************************************************************************
* Subcircuit WRITEP - Operation Priority Circuit
*The Call     14   60 61   17   18   1    0 WRITEP
******              MREF W R MW MR POWER GROUND
.SUBCKT  WRITEP 1    2 3  4   5      6        7
   INA INB INC OUT PWR GND SUBNAME
X0 1              8    6    7   DINV
X1 2              9    6    7   DINV
X2 2    8         4    6    7   DD2AND
X3 3    9   8     5    6    7   DD3AND
.ENDS    WRITEP
********************************************************************************

* POWER SUPPLIES
VDS          1   0    DC   2.0V
VREFB      777 0     DC    0.7V
VREFD      888 0     DC    0.26V
VSS        999 0     DC   -2.5V
* SIGNAL INPUTS
```

```
VCLOCKIN  8  0     PULSE(0.63 0.06  0PS 100PS 100PS 2100PS 4200PS)

*The next 3 lines will count 000 -> 111  with XXX PS up/down times
* Count through all eight addresses for testing purposes
*VA0        2  0     PULSE(0.06 0.63 4200PS 100PS 100PS 4000PS 8400PS)
*VA1        3  0     PULSE(0.06 0.63 8400PS 100PS 100PS 8200PS 16800PS)
*VA2        4  0     PULSE(0.06 0.63 16800PS 100PS 100PS 16600PS 33600PS)
*VA0        2  0     PULSE(0.06 0.63 4.5NS 100PS 100PS 4.3NS 9.0NS)
*VA1        3  0     PULSE(0.06 0.63 9.0NS 100PS 100PS 8.8NS 18.0NS)
*VA2        4  0     PULSE(0.06 0.63 18.0NS 100PS 100PS 17.8NS 36.0NS)
* Address Inputs - Following three lines are steady state DC voltages for testing purposes
VA0        2  0     DC  0.063V
VA1        3  0     DC  0.63V
VA2        4  0     DC  0.63V
* Data Inputs - Following eight lines are steady state DC voltages for testing purposes
VD0       100 0     DC  0.63V
VD1       101 0     DC  0.06V
VD2       102 0     DC  0.63V
VD3       103 0     DC  0.63V
VD4       104 0     DC  0.06V
VD5       105 0     DC  0.06V
VD6       106 0     DC  0.63V
VD7       107 0     DC  0.06V

* Data Strobe - Following  line is steady state DC voltage for testing purposes
VDAS      108 0     DC  0.63V
* Write Signal -
VW         60 0     PULSE(0.06 0.63 3NS 100PS 100PS 5000PS 1000MS)
* Read Signals -
*VR        61 0     PULSE(0.06 0.63 0PS 100PS 100PS 8000PS 1000NS)
VR         61 0     0.06V
* Refresh Signals -
*VREF      70 0     0.06V
VREF       70 0     PULSE(0.06 0.63 8000PS 100PS 100PS 4200PS 1000MS)

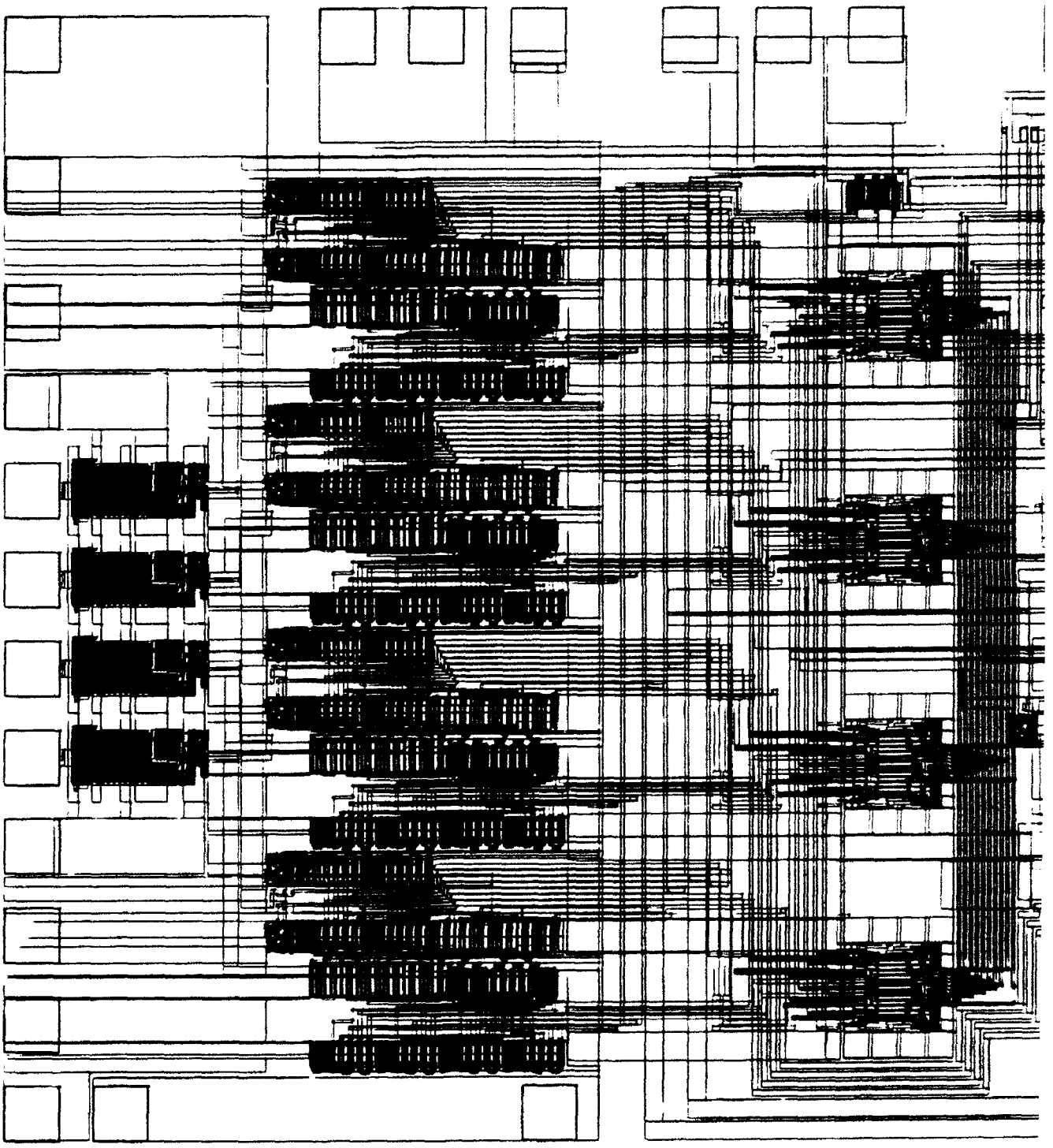
** Main Circuit **
*******************************************************************************
* Commence Subcircuit Calls
*******************************************************************************
*  INCLK PH1 PH2 PH2D PH1L PH2LD POWER1 POWER2  GROUND SUBNAME
X0  8     9   10   89    88    189       1        999        0     CLOCK
*******************************************************************************
** REF PH1 A0 A1 A2 AO0 AO1 AO2 MREF  POWER GROUND  SUBNAME
X1 70   9   2  3  4   11   12   13   14       1        0     DREFRESH
*******************************************************************************
**  MREF W  R   MW  MR  POWER GROUND SUBNAME
X2   14   60 61   17   18      1        0     WRITEP
*******************************************************************************
** PH2D AO0 AO1 AO2 MREF MR MW DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7 EVU
X3 10    11  12   13   14   18 17   20   21   22  23  24   25   26  27   30
**  ODU EV OD PWR1 PWR2 GND SUBNAME
```

```
+   31   40 41   1      999    0  DECODDRVER
*********************************************************************************
* This circuitry generates the output control signal Data Ready(DRDY) PIN 34
*   INA INB OUT PWR GND SUBNAME
X4  30  31   32    1    0   DD2OR
X5  32  18   33    1    0   DD2AND
X6  33       34    1    0   DINV
*********************************************************************************
* This circuitry generates the output control signal Memory Busy (MBSY)PIN 35
*   INA INB INC OUT PWR GND SUBNAME
X7  14   17   18   35    1    0   DD3OR
*********************************************************************************
* Commence Subcircuit Calls to RAM, each with its associated OUTPUT & WLOGIC
*********************************************************************************
* SUBCKT RAM -- Call for Data Bit Position ZERO
* PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5
X8 88   9     189    84     85     82     83    40    41    20   21    22   23    24    25
* DA6 DA7 EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx
+ 26   27    98    99     50    51    54    55    56    57     58    59     53    52
* PWR GND VREFB VREFD SUBNAME
+ 1      0      777     888    RAM
*  ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND SUBNAME
X9    99         98          30          31        18 300 310   1     0    OUTPUT
*      DATA DAS A0 MW PH2  EPU EPD OPU OPD POWER GND VSS SUBNAME
X10    100   108  2   17   10    82   83    84    85      1       0     999 WLOGIC
*********************************************************************************
*********************************************************************************
* SUBCKT RAM -- Call for Data Bit Position ONE
*   PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5
X20 88    9     189    184    185    182   183   40    41    20   21    22   23    24   25
* DA6 DA7 EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx
+ 26   27    198   199    150   151   154   155   156   157   158   159  153   152
* PWR GND VREFB VREFD SUBNAME
+  1     0      777     888    RAM
*  ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND SUBNAME
X21  199        198         30          31        18  301 311   1     0    OUTPUT
*      DATA DAS A0 MW PH2  EPU EPD OPU OPD POWER GND VSS SUBNAME
X22     101   108  2   17   10    182  183  184  185     1       0     999 WLOGIC
*********************************************************************************
*********************************************************************************
* SUBCKT RAM -- Call for Data Bit Position TWO
*   PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5
X23 88    9     189    284    285    282   283   40    41    20   21    22   23    24   25
* DA6 DA7 EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx
+ 26   27    298   299    250   251   254   255   256   257   258   259  253   252
* PWR GND VREFB VREFD SUBNAME
+  1     0      777     888    RAM
*  ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND SUBNAME
X24  299        298         30          31        18  302 312   1     0    OUTPUT
*    DATA DAS A0 MW PH2  EPU EPD OPU OPD POWER GND VSS  SUBNAME
X25 102   108   2   17   10    282  283 284  285     1       0     999  WLOGIC
```

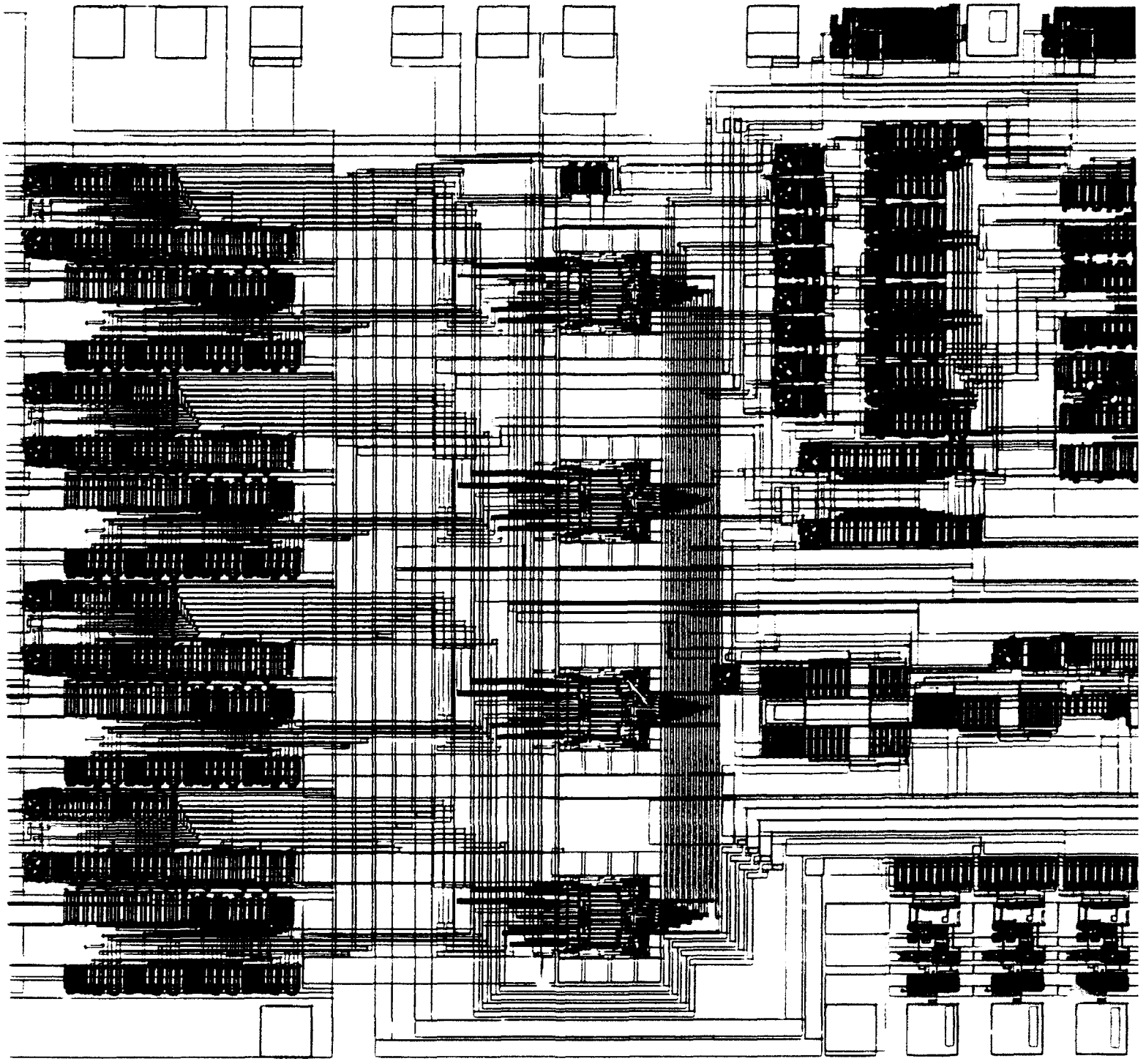
```
*******************************************************************************
*******************************************************************************
* SUBCKT RAM -- Call for Data Bit Position THREE
*   PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5
X26 88    9    189    384  385   382   383  40   41    20   21   22   23   24   25
* DA6 DA7 EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx
+ 26   27   398  399  350   351   354   355   356  357   358   359   353   352
* PWR GND VREFB VREFD SUBNAME
+  1    0     777     888   RAM
*  ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND SUBNAME
X27 399        398         30          31        18 303 313    1     0   OUTPUT
*    DATA DAS A0 MW PH2  EPU EPD OPU OPD POWER GND VSS   SUBNAME
X28 103    108  2   17   10    382 383  384  385     1       0   999  WLOGIC
*******************************************************************************
*******************************************************************************
* SUBCKT RAM -- Call for Data Bit Position FOUR
*   PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5
X29 88    9    189    484  485   482   483  40   41    20   21   22   23   24   25
* DA6 DA7 EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx
+ 26   27   498  499  450   451   454   455   456  457   458   459   453   452
* PWR GND VREFB VREFD SUBNAME
+  1    0     777     888   RAM
*  ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND SUBNAME
X30 499        498         30          31        18 304 314    1     0   OUTPUT
*    DATA DAS A0 MW PH2  EPU EPD OPU OPD POWER GND VSS   SUBNAME
X31 104    108  2   17   10    482 483  484  485     1       0   999  WLOGIC
*******************************************************************************
*******************************************************************************
* SUBCKT RAM -- Call for Data Bit Position FIVE
*   PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5
X32 88    9    189    584  585   582   583  40   41    20   21   22   23   24   25
* DA6 DA7 EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx
+ 26   27   598  599  550   551   554   555   556  557   558   559   553   552
* PWR GND VREFB VREFD SUBNAME
+  1    0     777     888   RAM
*  ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND SUBNAME
X33 599        598         30          31        18 305 315    1     0   OUTPUT
*    DATA DAS A0 MW PH2  EPU EPD OPU OPD POWER GND VSS   SUBNAME
X34 105    108   2  17   10   582   583 584  585     1       0   999  WLOGIC
*******************************************************************************
*******************************************************************************
* SUBCKT RAM -- Call for Data Bit Position SIX
*   PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5
X35 88    9    189    684  685   682   683  40   41    20   21   22   23   24   25
* DA6 DA7 EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx
+ 26   27   698  699  650   651   654   655   656  657   658   659   653   652
* PWR GND VREFB VREFD SUBNAME
+  1    0     777     888   RAM
*  ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND SUBNAME
X36 699        698         30          31        18 306 316    1     0   OUTPUT
*    DATA DAS A0 MW PH2  EPU EPD OPU OPD POWER GND VSS   SUBNAME
```

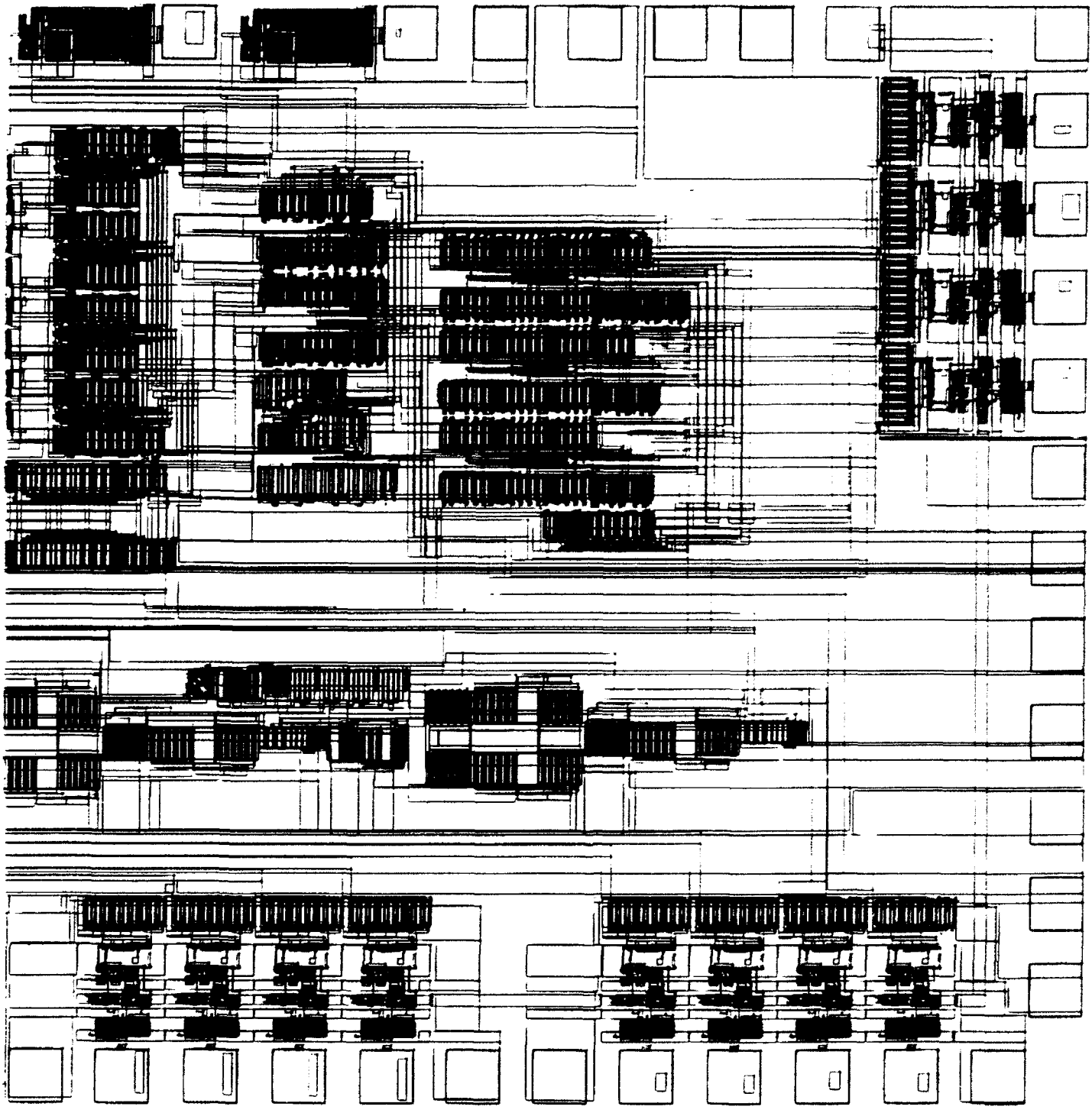
```
X37  106  108  2  17  10  682  683  684  685    1      0   999   WLOGIC
*******************************************************************************
*******************************************************************************
* SUBCKT RAM -- Call for Data Bit Position SEVEN
*   PH1L PH1 PH2LD OxPU OxPD ExPU ExPD EDC ODC DA0 DA1 DA2 DA3 DA4 DA5
X38 88   9    189   784  785  782  783  40   41   20  21   22   23   24   25
* DA6 DA7 EBIO OBIO RCx0 RCx1 RCx2 RCx3 RCx4 RCx5 RCx6 RCx7 RCEx RCOx
+ 26   27   798  799  750  751  754  755  756  757  758  759  753  752
* PWR GND VREFB VREFD SUBNAME
+  1     0    777     888   RAM
*  ODDBIO EVENBIO EDUMMY ODUMMY  MR  Q  /Q  PWR GND SUBNAME
X39  799       798        30         31      18  307 317  1     0  OUTPUT
*    DATA DAS A0 MW PH2  EPU EPD OPU OPD POWER GND VSS   SUBNAME
X40 107    108  2  17  10   782  783  784 785    1      0   999   WLOGIC
*******************************************************************************
*******************************************************************************
* Following Lines are operating directions for HSPICE
.TRAN 250PS 40.0ns
.options scale=1E-06 post acct captab
.END
```

APPENDIX B - LAYOUT PLOT OF GaAs DRAM



APPENDIX B - LAYOUT PLOT OF GaAs DRAM





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