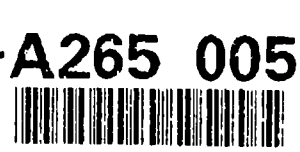

NSWCDD/MP-92/547

DEINTERLEAVER TECHNOLOGY FOR FUTURE ELECTRONIC SUPPORT MEASURES (ESM) SYSTEMS

BY J. DARREN PARKER
SHIP DEFENSE SYSTEMS DEPARTMENT

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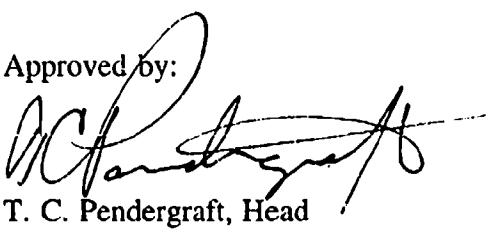
FOREWORD

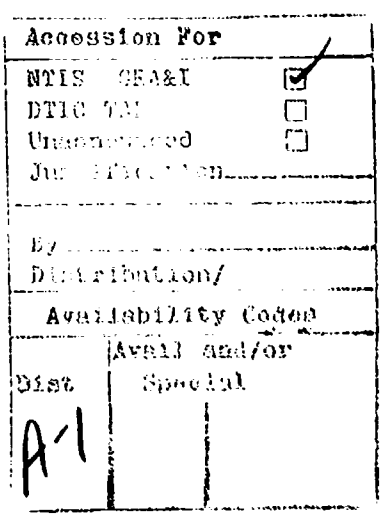
This report documents concepts and ongoing research related to the processing functions that future electronic support measures (ESM) systems will perform. Specifically, the focus of the report is on pre-filtering, sorting, and deinterleaving the pulse data generated by the ESM receivers. The identification function is not discussed. The author acknowledges the significant contributions of Mike Garner (F23) and John Miniuk (F21) to this work.

This report was reviewed by Sam Stello, Electronic Warfare Systems Integration Branch, Tom W. Kimbrell, Head, Electronic Warfare Systems Integration Branch, and Richard Lee, Head, Electronic Warfare Systems Division.

Approved by:



T. C. Pendergraft, Head
Ship Defense Systems Department



ABSTRACT

The precision electronic support measures (ESM) systems of the future must operate in dense environments of emitters that have agility in several parameters. A deinterleaving system that would be capable of processing the pulse data generated by a future precision ESM receiver is described at the block diagram level. To be effective in a dense environment of agile emitters, the deinterleaving system will need adaptable pulse data filters to eliminate the data from friendly emitters, a processor dedicated to sorting the pulse data from new and high-priority emitters by angle-of-arrival and frequency, and sophisticated, multiparameter deinterleaving algorithms. A summary of research related to ESM processing is given.

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ILLUSTRATIONS

INTRODUCTION

The precision electronic support measures (ESM) systems of the future must operate in a dense environment of agile emitters. Current emitters can stagger or jitter pulse repetition intervals (PRIs). They can be agile in radio frequency (RF) on a pulse-to-pulse basis and agile in pulse amplitude (PA) and pulse width (PW) on a dwell-to-dwell basis. They can also use pulse compression techniques. Future emitters may extend their capabilities to include agility in PA and PW on a pulse-to-pulse basis. Consequently, the deinterleavers of the future must be able to reconstruct the pulse trains from emitters that can have random PRIs and can be agile in RF, PW, and PA on a pulse-to-pulse basis. This will require future deinterleavers to use intrapulse measurements and robust multiparameter deinterleaving algorithms.

The ESM system's receivers generate a packet of digital data, which is called a pulse descriptor word (PDW), for every pulse detected. A PDW contains all of the measurements made on a pulse, which includes azimuth (AZ), elevation (EL), RF, PW, PA, time-of-arrival (TOA), and possibly intrapulse modulations. In a dense environment, the ESM system's processors (deinterleavers, emitter identification, emitter trackers, etc.) would be overloaded if every PDW were processed. Therefore, the ESM system will need an adaptable PDW filter that can block the PDWs from friendly and low priority emitters (many of which will be agile in several parameters), so that the PDWs from new emitters and threats can be processed quickly.

A block diagram for a deinterleaver that could provide the performance required by a future ESM system is presented. Also, a summary of research related to ESM processing is given.

PROPOSED DEINTERLEAVER STRUCTURE

One approach to achieving the required ESM deinterleaver performance is to combine an adaptable PDW filter bank, an angle-of-arrival (AOA) clustering device, an RF histogramming device, and robust multiparameter deinterleaving algorithms. A block diagram of this type of deinterleaving system is shown in Figure 1. The inputs to the deinterleaving system are the PDWs generated by the ESM sensor. The outputs are the re-constructed pulse trains from every emitter in the environment that are sent to the identification (ID) processor.

The first stage of the deinterleaving system (Figure 1) is the PDW filter bank. The purpose of this bank is to block PDWs from friendly and low-priority emitters, so PDWs from high-priority emitters can be closely tracked and new emitters can be identified quickly. Each

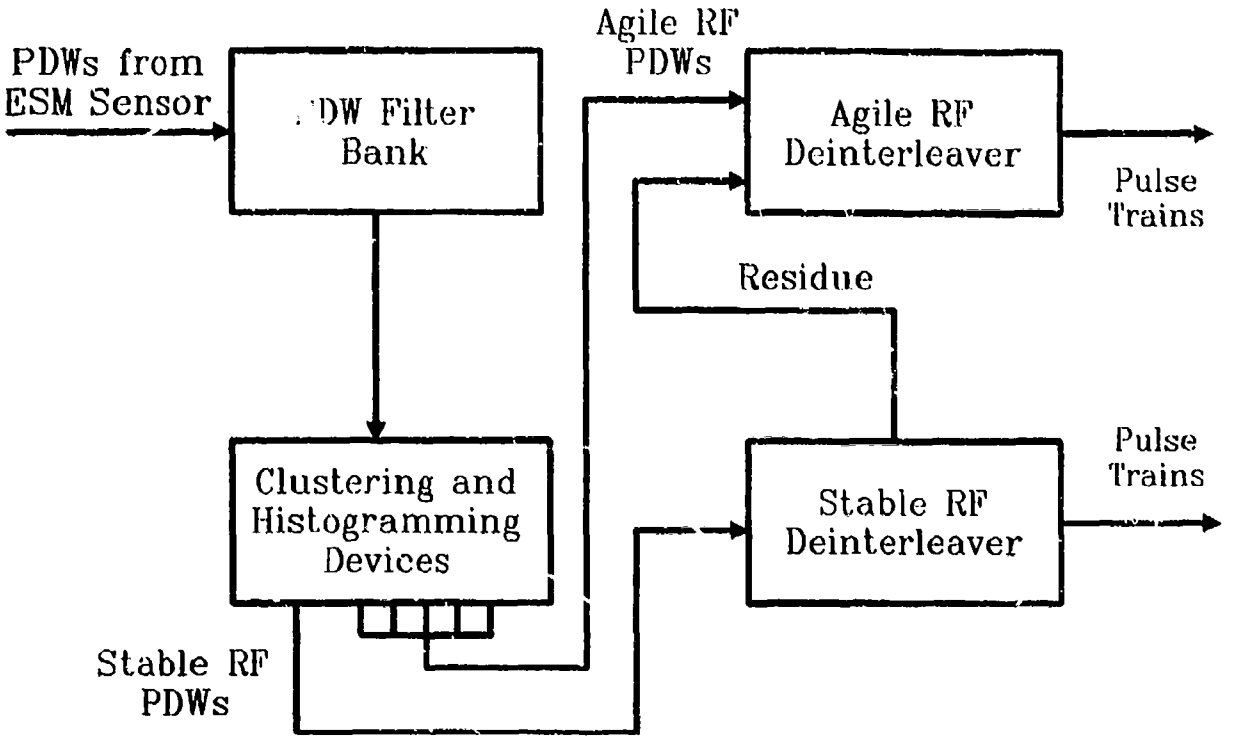

FIGURE 1. DEINTERLEAVER FOR PRECISION ESM SYSTEM

filter will have the capability to automatically allow a group of PDWs to pass periodically, so that tracks on all emitters can be maintained. The period and the number of PDWs passed can be controlled for each filter independently. When PDWs are passed, an emitter number tag can be appended to the PDWs to eliminate redundant sorting. The filter bank can configure each of its filters to block PDWs according to a combination of stable parameters. For instance, precision AOA alone could be used to block all of the PDWs from all of the emitters on a given ship. Similarly, a combination of AOA and RF could be used to block the PDWs from an emitter with a stable RF or one with agility in RF over a band (i.e., bandwidths up to 500 MHz). Combinations of other parameters (including PW and PA) may also be used to filter PDWs from agile emitters. When using AOA as a PDW filter parameter, both AZ and EL are considered. Therefore, a filter that is designated to block PDWs from a particular AZ and EL will allow PDWs from emitters at that AZ but with different ELs to pass. Each filter's AOA window can be adjusted as the emitter moves in angle by using information from the emitter's track file that is maintained outside the deinterleaving system.

The optimal implementation of the PDW filter will depend on the type of receivers used in the ESM system. Most of the PDW filters that have been implemented were designed for use with Instantaneous Frequency Measurement (IFM) receivers that typically have PDW output rates slow enough for the PDW filter to process the PDWs one at a time. For a future ESM system that uses a channelized receiver, the PDW output rates will probably be so fast that the PDW filter will not be able to process the data if it is input along a single path.

The receiver type that has traditionally been used in ESM systems is the IFM. A single IFM can measure the frequency of signals over a wideband (i.e., 2 GHz) by measuring the difference between the input signal and a delayed version of the input signal. Its simplicity is its major advantage, but it has great difficulty detecting simultaneous signals. The IFM receiver will typically either ignore the weaker of the two simultaneous signals or provide a corrupted frequency measurement. The channelized receiver is much more complex and, consequently, expensive than the IFM receiver. It uses many narrow-band receivers that give the channelized receiver a high probability of intercept (POI) for simultaneous signals. The optimal implementation of the PDW filter for a channelized ESM system would be Application Specific Integrated Circuit (ASIC) chips that are small and simple enough to be incorporated into each channel, so the inherent parallel structure of the channelizer can be exploited. A single processor would require that all of the PDWs generated in all channels be combined and sent down a single path to the processor performing the PDW filter function. Therefore, if the PDW filter were implemented as a single processor, the throughput of the system would be lower than the same system with PDW filters in each channel.

A simplified block diagram of a channelized ESM system that uses the proposed deinterleaving system is given in Figure 2, which shows the receiver having N channels. The RF, PW, PA, and TOA are measured in the receiver channels labeled "RECV CHAN" in the figure. The AOA is measured in the phase interferometer channels labeled "AOA CHAN" in the figure. In Figure 2, the label "K" over the line leaving the phase interferometer antenna array is intended to illustrate that the outputs of each of the K antennae are inputs to each AOA channel. The AOA is measured in each AOA channel from the phase differences between the antenna outputs. For this figure, AOA refers to AZ only. If the ESM system measures EL as well, another phase interferometer must be included in the system. A PDW assembler circuit to combine all the measurements made on each pulse is labeled "PDW Assm" in the figure. A PDW filter chip follows each PDW assembler, so the PDWs from friendly emitters can be removed immediately. This will require each PDW filter chip to have enough memory cells for the maximum number of emitters to be filtered, but each must be simple enough to be placed in each channel. Two pulses arriving simultaneously within the same channel will cause a corrupted frequency measurement. Special frequency measurement techniques, which are beyond the scope of this report, will be required to handle this case.

A block diagram of a PDW filter chip is shown in Figure 3. At the top of the figure, the PDW from the PDW assembler is shifted into a buffer . The parameters that are needed for comparison with the cells in memory are extracted and sent to each cell. Each cell is represented in this figure by a column of windows (a window being a range of acceptable values for a parameter), each of which is denoted with the label "WIN." Cells are formed for emitters that have been identified by the ESM system as low priority emitters. Each cell will have windows for each parameter that can be used to characterize that particular emitter. The control logic block, shown at the bottom of the figure, performs logic operations on the results of the comparisons, so each cell can be configured to sort on any combination of parameters. Note that the vertically aligned dots in the figure are intended to indicate that each cell can be configured with windows for any number of parameters; however, only windows for AZ, EL, and PW are shown in Figure 3. The horizontally aligned dots in the figure indicate that the total number of

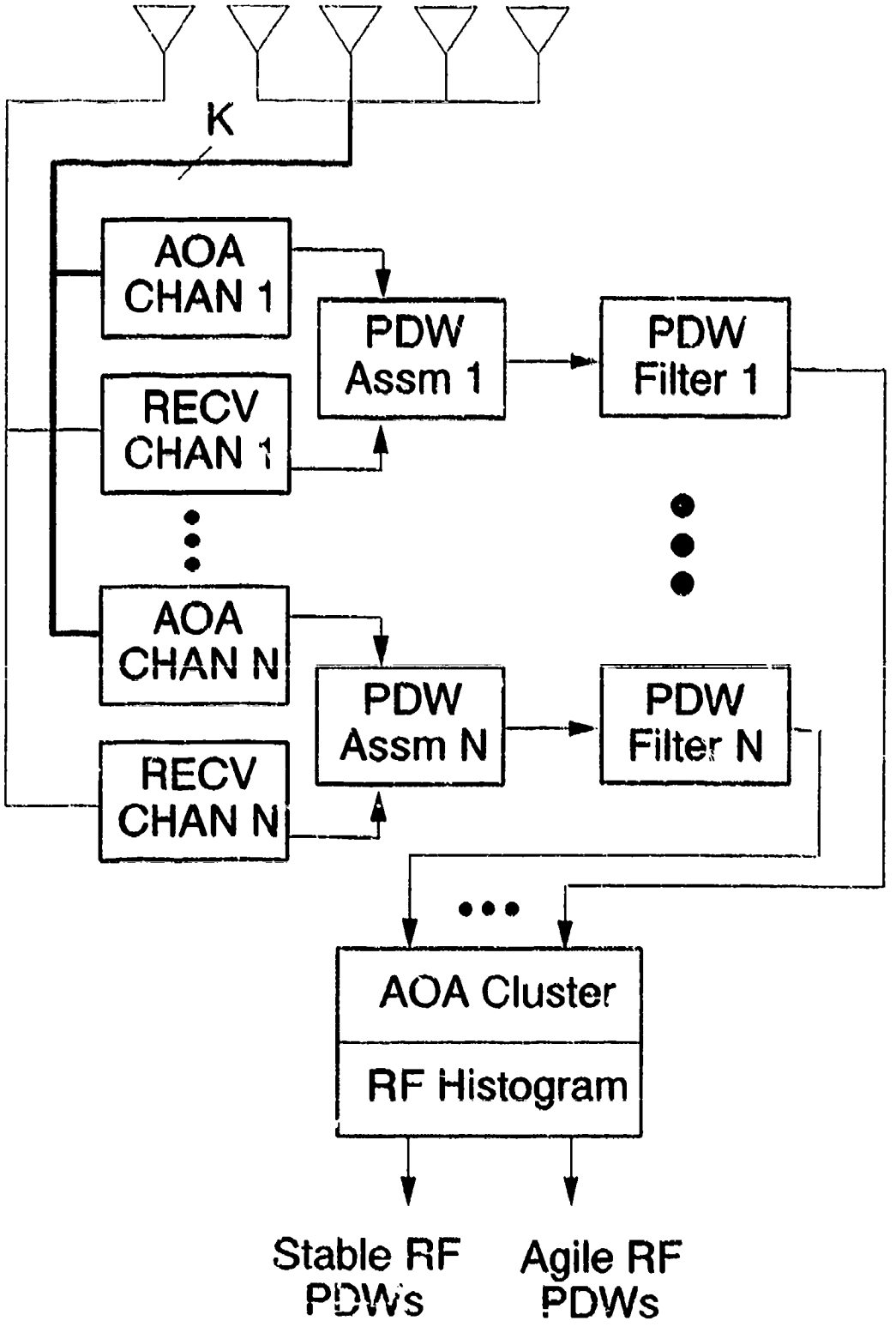

FIGURE 2. PROPOSED DEINTERLEAVING SYSTEM FOR A CHANNELIZED ESM RECEIVER

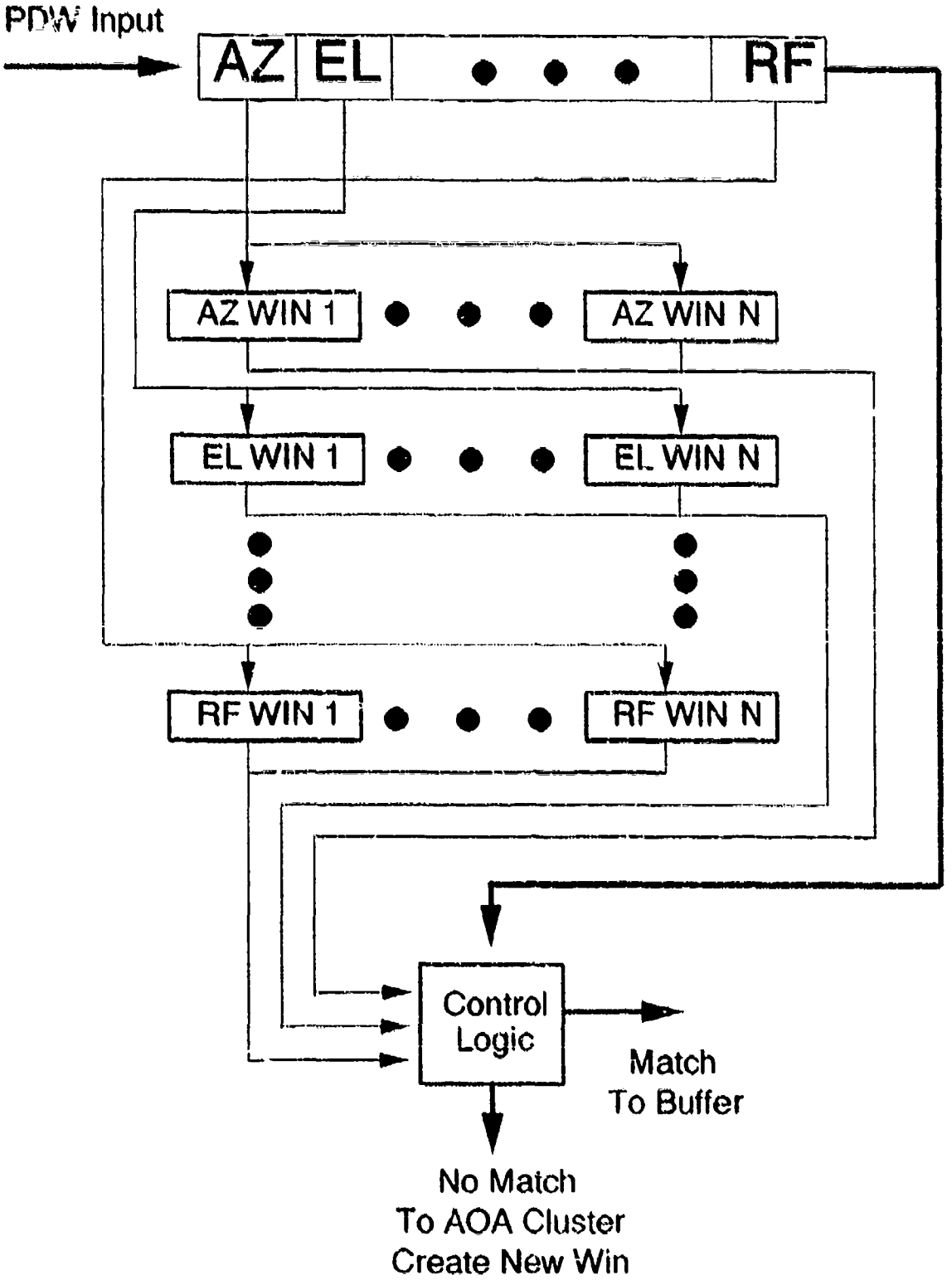

FIGURE 3. BLOCK DIAGRAM OF A PDW FILTER CHIP

cells used at any given time will depend on the total number of emitters the system desires to filter. For example, a cell that filters PDWs from an RF stable emitter could use AZ, EL, RF, and PW and a cell that filters PDWs from an RF agile emitter could use just AZ and EL or perhaps AZ, EL, and PW. It is noted that PW is not a good sorting parameter when used alone because multipath can cause corrupted PW measurements. However, PW may provide better sorting when used in conjunction with other parameters. If there are emitters in the environment with stable PRIs, expected TOA could be used along with the other sorting parameters. The control logic block, at the bottom of Figure 3, determines if the input PDW matches any of the cells. If a match occurs, the PDW is sent to a buffer since it corresponds to a low-priority emitter. If no match occurs, the PDW is sent directly to the AOA clustering device. The emitter identification function of the ESM system will cue the PDW filter to create a new cell if an emitter is identified as a low-priority emitter. The emitter tracking function of the ESM system will initialize timers that are included in the control logic block (Figure 3). A timer for each cell will be set to allow PDWs to be passed to the emitter tracking function of the ESM system at a sufficient rate to maintain an accurate track of the emitter.

The windows shown in Figure 3 can be implemented in two ways. One implementation, which is illustrated in Figure 4, requires storing both a maximum and a minimum value to define the acceptable region for the parameter. Then, the measured parameter must be compared to both the maximum and minimum values and logic operations must be performed to determine if the measured value is less than the maximum and greater than the minimum. The other implementation, which is illustrated in Figure 5, requires storing only the median value between the maximum and minimum. Then, the measured value is compared to the median value to the required number of most significant bits to obtain the desired resolution.[1]

The second and third stages of the deinterleaving system (Figure 1) consist of an AOA clustering device and an RF histogramming device, respectively. The AOA clustering device clusters all PDWs by AOA. This is the logical first step in the pulse sorting process since this parameter is the only one that will be stable on a pulse-to-pulse basis for all emitters in the environment. A state-of-the-art ESM sensor can measure AZ and EL to accuracies on the order of tenths of a degree which will enable the AOA clustering device to separate most platforms. After the PDWs have been clustered by AOA, the RF histogramming device clusters the PDWs from stable RF emitters. These stable RF PDWs are then sent to a stable RF deinterleaving algorithm. The PDWs from agile RF emitters will be scattered by the histogramming device, and these PDWs will be sent directly to an agile RF deinterleaving algorithm.

The optimal implementation for both the AOA clustering device and the RF histogramming device is probably a Content Addressable Memory (CAM), which is a memory that simultaneously compares the input to all memory cells and generates pointers to all matching cells. A CAM that is commercially available is the Coherent Processor (CP),[1] which has 4096 cells of 32-bit CAM. Each cell also has a processing element that could be used to count the number of PDWs falling into each cell. Programs that can completely simulate the CP are available, so bench-marks can be run to determine if implementing one's processing algorithms on the CP will be practical. The Associative Processor, which was developed by IBM, performs the same function as a CAM and was developed specifically for ESM pulse data sorting.[2] This

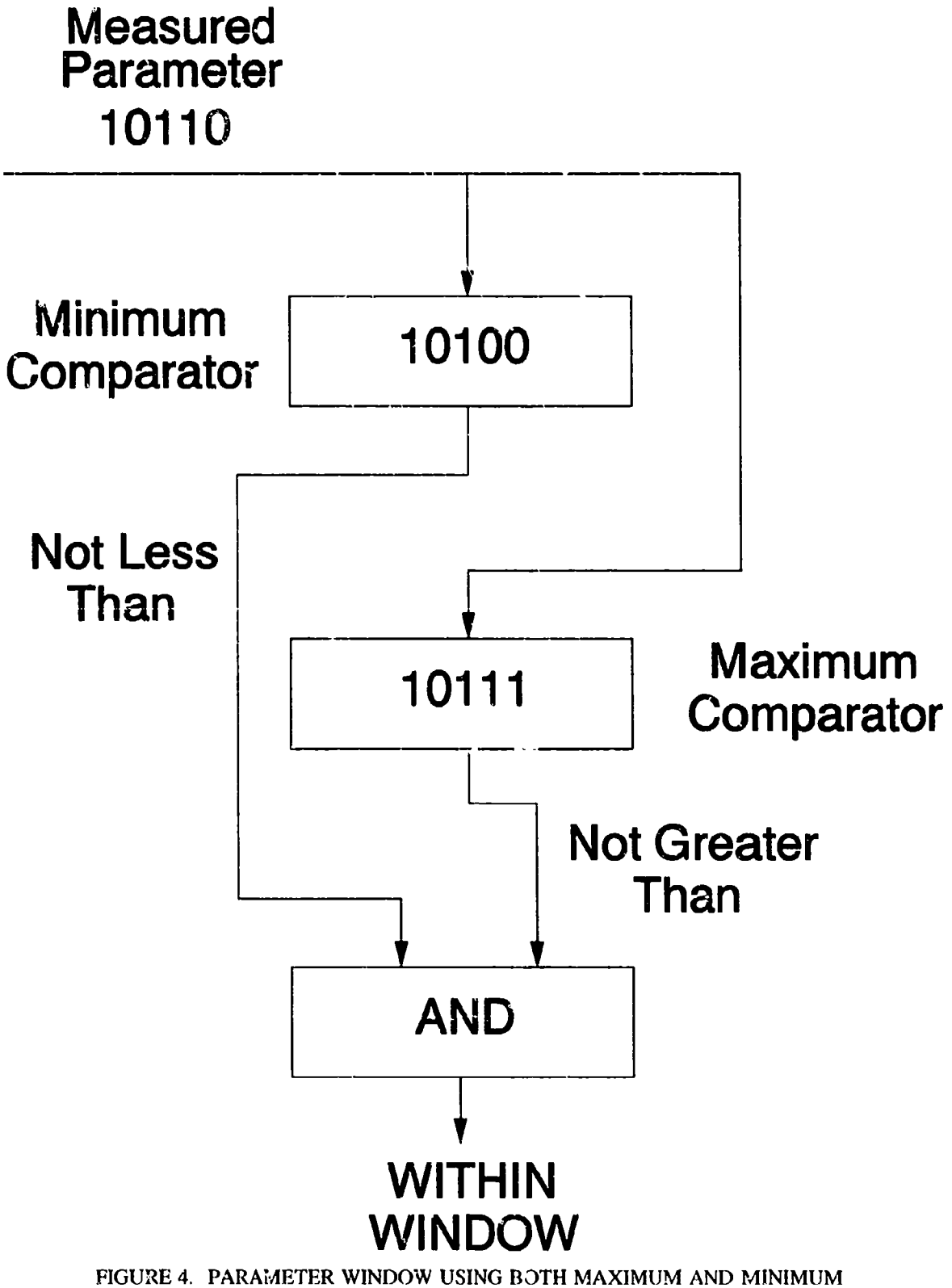

FIGURE 4. PARAMETER WINDOW USING BOTH MAXIMUM AND MINIMUM

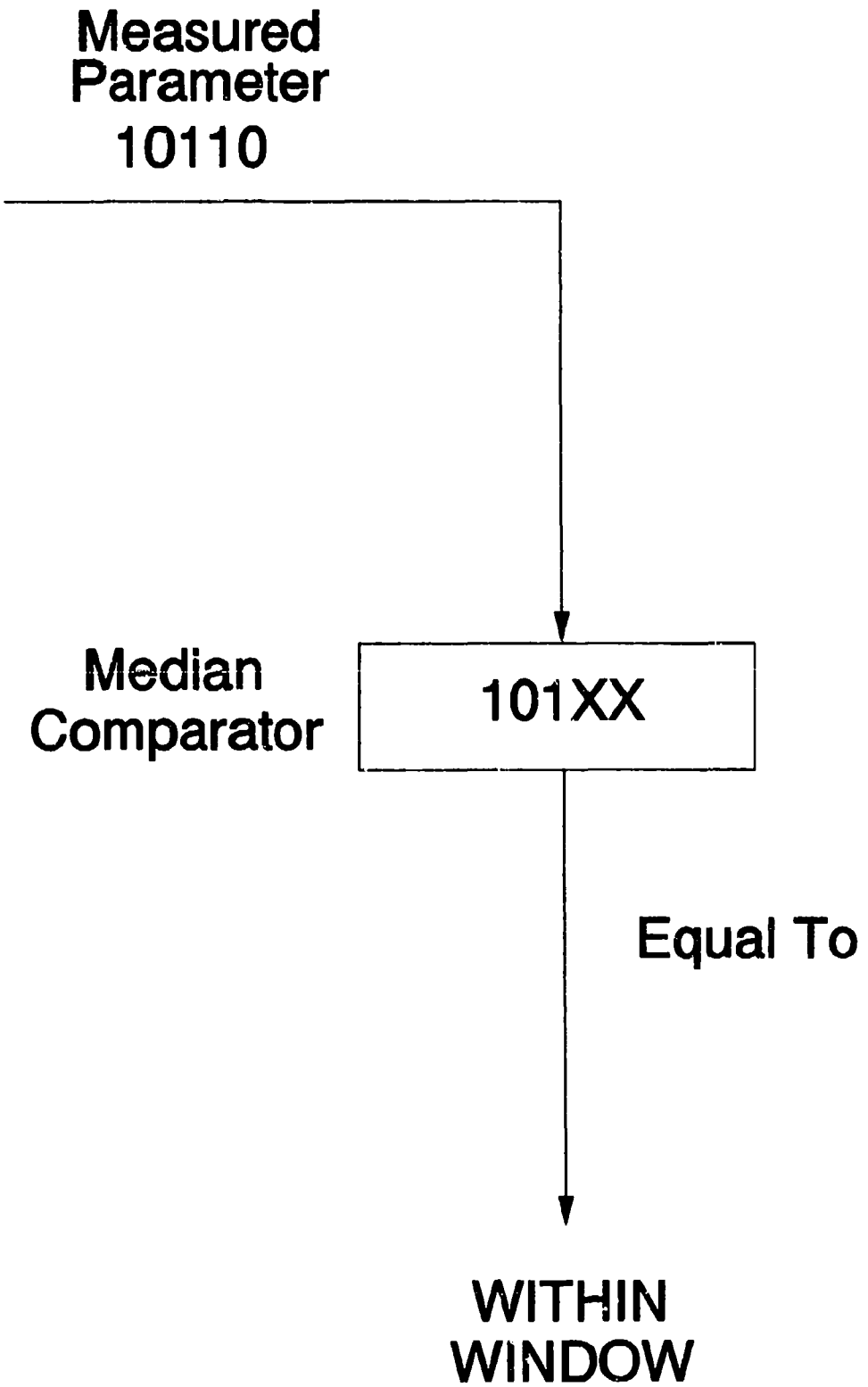

FIGURE 5. PARAMETER WINDOW USING ONLY MEDIAN

processor is discussed in greater detail in the next section (SUMMARY OF RELATED RESEARCH).

The deinterleaving function of the system, as shown in Figure 1, is performed in two separate algorithms operating in parallel; one deinterleaver operates on stable RF PDWs only, and the other operates on agile RF PDWs. This arrangement makes it possible to deinterleave the PDWs from simple emitters quickly. The stable RF deinterleaver forms a two-dimensional array from the stable RF PDWs and uses all of the available parameters to deinterleave them. The array will contain a one-dimensional array of vectors; each vector will contain all the measured parameters for a received pulse at a particular TOA. Intrapulse parameters will be used only if necessary due to their pulse train complexity. Any residue will be sent to the agile RF deinterleaver. The agile RF deinterleaver forms a three-dimensional array from the agile RF PDWs and the residue from the stable RF deinterleaver. The array will contain a two-dimensional array of vectors; one vector for each discrete TOA and each RF, as illustrated in Figure 6. Like the stable RF deinterleaver, the agile RF deinterleaver will use all of the available parameters to deinterleave the PDWs, and it will use the intrapulse parameters only if necessary. In Figure 6, the intrapulse measurements, which are shown as secondary sort parameters, are frequency modulation (FM), phase modulation (PM), and unintentional modulation (UM). The residue from the agile RF deinterleaver will be maintained in memory for several seconds, so emitters with very slow PRIs can be detected. The performance of both deinterleaving algorithms (especially the agile RF deinterleaving algorithm) will depend on the ESM system's ability to maintain accurate TOA tags over a span of several seconds.

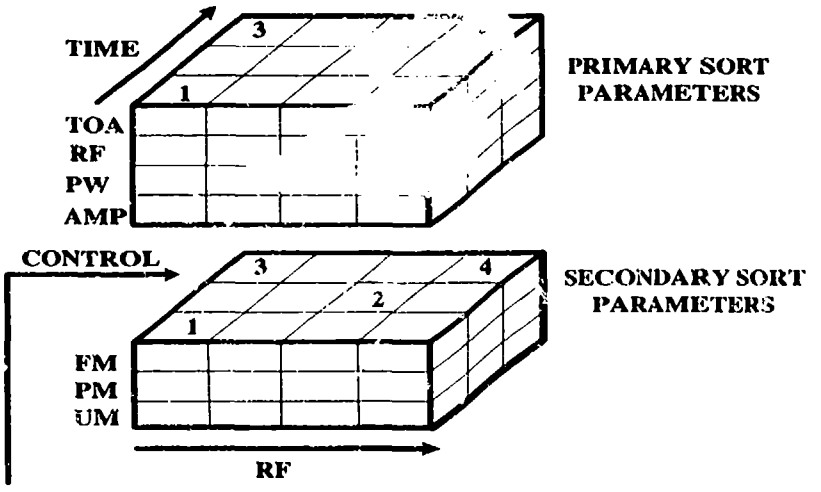

FIGURE 6. AGILE RF DEINTERLEAVER STRUCTURE

SUMMARY OF RELATED RESEARCH

A summary of research published in the open literature concerned with improving the performance of ESM processors is given. This summary is provided because much of this research may be practical for future ESM deinterleaving systems.

SPECIFIC ESM PROCESSORS

Four ESM processors are described:

SADIE ESM Signal Processor---Kellet describes the ESM signal processor developed by Racal Defence called SADIE.[3] This processor was designed based on the assumption that most of received pulses have been previously characterized, so extensive processing should be reserved for complex emitters. The SADIE consists of a segregator, an analyzer, a monitor, and a control processor; it has already been used in ship, air, and ground ESM systems.

The segregator is the most important part of the system. It can use all of the measured pulse parameters; e.g., RF, PW, AOA, Modulation Flags, TOA, and PA. The key component of the segregator is the extended WAM (EWAM), which is implemented on ASIC chips. It stores mean and tolerance for comparisons. Many EWAMs operate in parallel on each parameter. Control logic determines the combinations of matches that are acceptable. The EWAM chip is based on 2.5-micron CMOS technology and performs several billion bit comparisons per second. The segregator can also use expected TOA in the matching process. It allows for 0,1, or 2 missing pulses and accounts for scan bursts as well. Each EWAM can operate on its own after being initialized.

The analyzer is the deinterleaver and operates on pulses that do not match the parameters stored in the segregator. The monitor detects changes in the pulse environment. The control processor takes outputs from the analyzer and the monitor to update an emitter track file. It configures the segregator so that a scan analysis can be performed.

IBM's Associative Comparator (AC) Chip---Hanna describes the AC chip developed by IBM Federal Systems Division.[2] Each AC chip has 32 comparison cells; each cell consists of a pair of upper and lower limits. It can perform 32 two-parameter comparisons in 1.6 microseconds, 16 two-parameter comparisons in 1 microsecond, and 8 two-parameter comparisons in 0.5 microseconds where each parameter is 16 bits. This gives the AC chip a minimum throughput of 625,000 pulses per second. Hanna states that this throughput is adequate for IFM type ESM receivers, but channelized, micro-scan, or acoustic-optical type ESM receivers will require compare times less than 100

nanoseconds. Any cell can be independently enabled/disabled, or all cells can be globally enabled/disabled. Multiple AC chips can be cascaded to compare more parameters and/or to have more cells.

IBM developed an ESM processor that uses AC chips to sort and filter incoming pulses.[4] It uses three AC chips, which gives the processor a total of 96 comparison cells. Each comparison cell can either accept or reject matching pulses. The pulses that are accepted are sent to the main memory of the ESM processor along with a number that identifies the matching cell. New cells are created for pulses that do not match any of the current cells.

IBM made improvements to the ESM processor by improving the AC chip.[5] The next generation chip was called the Advanced Associative Comparator (AAC), and it was incorporated on a module called the Pulse Sort Module (PSM). The AAC chip can compare an input to 128 cells in 2 microseconds. The input can be two 16-bit, one 16-bit and two 8-bit, or four 8-bit parameters. The PSM consists of a pulse processor and a cell processor. The pulse processor uses four AACs to compare incoming pulse data to 512 cells in memory. When a match occurs, the data and an ID number are passed to the cell processor. If no match occurs, a new ID number is formed, and the data, the new ID number, and a new pulse flag are sent to the cell processor. When the cell processor receives a new ID flag, it performs a 2D histogram in AOA and RF on the data. The cell processor maintains a 16 pulse history for each of the 512 compare cells. The cell processor has 8 analysis channels to perform PRI analysis and parameter averaging. Each analysis channel has enough memory for 256 pulses.

Anaren's ESM Processor---Anaren developed an ESM system capable of operating in signal densities of one million pulses per second without any frequency, amplitude, or spacial filtering.[6] The receiver generates 55-bit PDWs that are sent to a Pulse Controller (PC). The PC forms a 2D histogram using bearing and frequency and has 4 Mbytes of memory. It takes less than one microsecond to map a pulse's bearing and frequency to a cell on the histogram. The Emitter Processor (EP) is linked to the PC through a bidirectional bus. The EP searches the memory map of the PC looking for clusters and performs PRI and scan analysis on the clusters it finds. If the EP obtains poor results, it retrieves more pulse data from the memory map and repeats the analysis. The algorithms used by the EP are written in Fortran 77, but the author states that plans for future improvements include converting the algorithms to Ada. This ESM processor was simulated during development using the techniques developed by Hollands.[7]

AN/SLQ-32(v) Inner Processor (IP)---The IP of the AN/SLQ-32(v) performs the initial deinterleaving functions of sorting the incoming PDWs into pulse trains.[8] This document is the only one referenced that is not published in the open literature. It uses AOA (bearing only) and RF as sorting parameters. When a PDW is received, the IP tries to match its AOA and RF with cells stored in memory. If it finds a match, the IP increments the counter for that cell. When the count reaches a threshold, the IP informs the CPU of a new emitter so the PDWs corresponding to this cell can be analyzed for identification

of the emitter. However, before reporting this new cell as a new emitter, the IP first checks the adjacent AOA bins. If the same RF bin is found in an adjacent AOA bin, the IP assumes it is the same emitter and removes the older cell from memory. The IP attempts this same correlation using the next two adjacent bins if the amplitude of the pulse is below a threshold or if the AOA bin is at the bow or stern of the ship.When the IP receives a PDW that does not match any cells in memory, it forms a new cell. No received PDW is reported to the CPU until the count threshold for that cell is reached. Also, a timer is used to remove cells for which no PDWs have been received in a given amount of time.

DISTRIBUTED ARRAY PROCESSORS

Parallel processors have been applied to a variety of fields, and they will be required or future ESM systems that will operate in very dense environments. Transputers are a Single Instruction Multiple Data (SIMD) type of parallel processor architecture, and they seem to be particularly well suited to ESM processing. The research of Roberts, Merrifield, and Beton in applying transputers to ESM processing is discussed.

Roberts discusses the use of the Mil-DAP as a processor for an airborne radar and describes the next-generation processor called the MSI DAP.[9] Both consist of many 1-bit Processing Elements (PEs) with each PE connected to its 4 neighbors. MSI DAP has 4096 PEs in 64 by 64 lattice with each PE containing 16 Kbytes of memory. Mil-DAP has an array of 32 by 32 PEs with each having 8 or 16 Kbytes of memory. Each PE has a 1-bit adder and 3 registers. Any word length can be used because all operations are built up bit wise. The Mil-DAP was used as the processor on an airborne radar with several operating modes. The measures of performance were the data input time, the times to compute FFTs and CFARs, and time to resolve ambiguities in range and doppler. It was determined that the Mil-DAP processed data fast enough to have 20- to 25-percent dead time between data inputs.

Merrifield investigated the use of the Mil-DAP for ESM applications.[10] He reports that ESM-related benchmarks demonstrate that the Mil-DAP can perform real-time processing. The Mil-DAP can be programmed either at the bit level with an assembler language or by using an extended version of Fortran developed for this processor. The Mil-DAP was programmed to sort ESM pulse data into chains and to compare the chains. The processing functions were divided into association and recognition functions. The association process forms pulse chains and maintains a database of received pulses. The recognition process performs the ID and maintains a database of active emitters. The parameters used by the association function include RF, PW, AOA, and TOA. The recognition function uses all of these to compute PRI; the researchers plan to add scan analysis at a later time. The rate of change of the number of emitters in the environment affects the performance because reformatting of the databases contained in each PE is time consuming. Merrifield states that special-purpose hardware is needed to perform

associations of simple emitters before the input to the Mil-DAP associator. He also states that performing PRI analysis using histograms of TOA differences is slow on this type of SIMD machine.

Beton discusses the performance achieved by ESM processing algorithms implemented on an array of transputers.[11] The ESM processing algorithms were originally written in PASCAL on a Vax computer and then, were translated to OCCAM, which is a language designed for implementing parallelized algorithms. The ESM processor functions were broken into three parts: a deinterleaver, a merger, and an emitter identification. Beton did not implement a pulse filter prior to the deinterleaver, but stated that the deinterleaver would have a maximum input rate of 10^5 pulses per second after front-end filtering. The deinterleaver function required the highest throughput and was implemented on 40 processors. Beton stated that the transputer implementation of the deinterleaver performed 350 times faster than the Vax version. He did not determine if the transputer implemented ESM processor could achieve real-time performance.

KNOWLEDGE-BASED ESM PROCESSING

A area of research that seems to promise major improvements over current ESM processors is the application of knowledge-based (also called expert systems) algorithms to deinterleaving. The work of Cussons, Feltman, and Self is discussed.

Cussons is researching knowledge-based processing for deinterleaving, merging, and ID.[12] Admiralty Research Establishment (ARE) contributed to the SEAVIEW knowledge-based emitter ID processor. Its most important characteristic is its ability to reverse a hypothesis that is proven false. The information released by the reversed hypothesis is available for the creation of new hypotheses. Cussons plans to use this same knowledge-based architecture for deinterleaving and pulse chain merging. Also, he plans to develop real-time implementations of all three processors. Initial research indicates that a transputer implementation is most likely one for real-time applications.

Feltman is researching transputer implementations of knowledge-based deinterleaving and merging.[13] He states that conventional, algorithmic type deinterleavers can already be implemented on transputers for real-time applications, but knowledge-based deinterleavers implemented on transputers are a little slow for real-time. However, he expects the next-generation transputers to be fast enough for real-time applications of knowledge-based deinterleavers. Feltman predicts that the processors of ESM systems developed in the near future will consist of a prefilter implemented in hardware, an algorithmic deinterleaver implemented on a Multiple Instruction Multiple Data (MIMD)-type parallel processor, and a knowledge-based merger and ID implemented on an MIMD-type parallel processor. Then, in the future, replacing the algorithmic deinterleaver with a knowledge-based deinterleaver will be practical.

The work of Self has resulted in an ESM processor implemented in ADA.[14] Self is continuing research to incorporate expert system techniques, to develop a multiprocessor implementation, and to develop an ASIC implementation of the preprocessor.

USING INTRAPULSE MEASUREMENTS AS A SORTING PARAMETER

Another area of research that holds promise for ESM processor improvements is the use of intrapulse measurement data for deinterleaving pulse trains. Danielsen has investigated a deinterleaver that operates on a pulse-by-pulse basis and relies exclusively on intrapulse measurements [15] He reports that using this technique alone does not provide adequate deinterleaver performance. Agg continued this research by adding TOA analysis after the intrapulse measurement sorter.[16] Agg reported a significant improvement in performance, but this deinterleaver could not handle the case of two identical emitters along the same line of bearing. He speculates that a deinterleaver using intrapulse measurements as a sorting parameter will be easier to implement in real-time than a knowledge-based approach.

MISCELLANEOUS TOPICS

A general discussion of microprocessor applications to electronic warfare (EW) and methods to evaluate the performance of a particular processor are given by Lemley.[17] Hollands discussed a software package he developed in Fortran 77 that can simulate and evaluate the performance of an ESM processor.[7] It models the interfaces between hardware and software components of the processor to evaluate the real-time performance.

CONCLUSIONS

Future ESM systems will need highly sensitive receivers in order to maintain a high probability of detection for threat emitters. This will make these ESM systems vulnerable to processor overload due to the large number of nonthreatening emitters in the environment. A block diagram of an deinterleaver that would allow a sensitive ESM system to operate in a dense environment was presented. Also, a summary of recent research that has potential applications to ESM data processing was given.

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REPORT DOCUMENTATION PAGE

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1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	December 1992	

4. TITLE AND SUBTITLE
Deinterleaver Technology for Future Electronic Support Measures (ESM) Systems

5. FUNDING NUMBERS

6. AUTHOR(S)
J. Darren Parker

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Surface Warfare Center
Dahlgren Division (F21)
Dahlgren, VA 22448-5000

8. PERFORMING ORGANIZATION REPORT NUMBER
NSWCDD/MP-92/547

9. SPONSORING/MONITORING AGENCY NAME(S) AND

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

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The precision electronic support measures (ESM) systems of the future must operate in dense environments of emitters that have agility in several parameters. A deinterleaving system that would be capable of processing the pulse data generated by a future precision ESM receiver is described at the block diagram level. To be effective in a dense environment of agile emitters, the deinterleaving system will need adaptable pulse data filters to eliminate the data from friendly emitters, a processor dedicated to sorting the pulse data from new and high-priority emitters by angle-of-arrival and frequency, and sophisticated, multiparameter deinterleaving algorithms. A summary of research related to ESM processing is given.

14. SUBJECT TERMS		15. NUMBER OF PAGES
Electronic Warfare (EW) Deinterleaving	Radar Signal Processing	27 16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
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