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DARPA Contract MDA972-92-C-0075

OETC Optical Backplane Bus Testbed

IBM Tasks: Receiver OEIC and Link Simulation Tools and Analysis

Quarterly Technical Report
Period ___3Q92_____

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Task Objectives

The general objective of this first contract period was to establish people interactions between researchers at the OETC companies, and establish a methodology for co-ordinating the development of the components in the Testbed. Specifically, we were to:

- Establish contacts between researchers/engineers from each company.
- Define a framework for interface specifications between components.
- Obtain preliminary component specifications
- Identify experiments needed or test vehicles needed to determine initial specifications.
- Establish reporting and interaction procedures within IBM.

Technical Problems

The main challenge to setting up this framework is getting the right people interacting, and understanding the main features and limitations of each component.

For the link modeling, we needed to understand the maturity of the components. We needed to know how well the mean values of the specification parameters could be maintained; and how these parameters varied over environment and manufacturing. We needed this information to determine the level of sophistication for the model.

For the receiver design, we needed to determine the design trade-offs which were necessary in order to meet module performance objectives. We needed to understand the limits of the package, and the bus performance objectives.

General Methodology

Meetings were held between workers to establish contacts, and an e-mail communication network was established. AT&T and IBM interactions with one of the University support schools were co-ordinated.

Experiments were conducted both at AT&T and IBM to establish link and component specifications.

Test vehicles were designed and sent to the receiver chip foundries.

Technical Results

This is a summary of technical results. The appendix explains in more detail the technical results of each IBM contributor to the project.

Receiver Tasks Completed

- Initial physical layout of 32 channel receiver chip made. Review held with AT&T on 9/23/92 (packaging compatibility).
- A low frequency noise model of the receiver preamp and MSM-PD was made, and successfully correlated against receiver front ends fabricated at a MESFET foundry.
- MSM Photodiode test macro was designed and sent to a MESFET foundry. This test vehicle is to test the PD characteristics for devices made in the MESFET line, specifically looking for low frequency peaking, DC leakage characteristics, responsivity and capacitance. Design review held on 9/1/92.
- Initial on-wafer chip testing strategy developed. An on-wafer MUX circuit, and an array of optical fibers are to be employed to accelerate the testing of 32-channel chips across the entire wafer.
- Review of receiver packaging options were conducted with AT&T, 8/20/92, 9/23/92.
- Draft of receiver functional description and interface specifications was prepared, and items to resolve identified.

Link Simulation Tasks Completed

- Review of VSEL device AC performance made with AT&T, 8/20/92, 9/23-24/92. Lab characterization was done at IBM for bandwidth, modal characteristics, and laser noise. A preliminary VSEL functional specification was made.
- A quasi-analytical approach to link modeling was adopted, based on an OLAP framework. Commercial spreadsheet programs were reviewed for suitability of interactive interface, and availability of statistical programs for bus analysis. APL2 was selected as the programming language for the simulator, with an interface based on APE,vers.2.
- Maximum link wavelength of 850 nm was established as optimum for both PD and LD performance and yield (identical to ANSI FCS standard). 5 GaAs MSM-PD chips (made at foundry C) were characterized by AT&T for relative responsivity. Response was found adequate to $\lambda \geq 850$ nm.
- Review of techniques for link interface specifications was made. A decision was made to describe components by an eye diagram template was made; similar to the specification techniques of the ANSI Fiber Channel and CCITT SONET Standards. A decision was made to specify receiver and transmitter modules at the 32 input and output lines of the modules, for link simulation purposes. Review of these definitions was made on 9/3/92.

Administrative Tasks Completed

- Kick-off presentation to DARPA was prepared and delivered - 7/ 29/92
- Draft of Functional Specifications for Receiver was prepared- see appendix.
- Lists of outstanding issues between IBM and AT&T, GE, and Honeywell were prepared, and updated as questions were resolved, and new questions arose.
- Presentation prepared for GOMAC, OFC'92 on OETC Overview.
- Final Contract prepared and submitted 8/20/92. Effective start date: 7/1/92.
- Program co-ordination with UCSB, a participating OETC University, was made. UCSB will assist in VSEL device modeling and characterization under AT&T support, and assist in VSEL transmitter modeling and characterization under IBM support. UCSB may provide alternate designs to test VSEL limitations.

Important Findings and Conclusions

Anticipated progress was made in both receiver and link design objectives. Working contacts with GE and AT&T were established. Honeywell contacts are yet to be established.

Some exposures are:

1. More detailed Testbed definition is necessary to determine the link and chip interfaces to the Testbed. Testbed support chips and second level packages need functional and electrical definition in order to provide design objectives for the receiver chip, and link models.

2. More resource needs to be devoted to O-E module package definition in order to determine the overall module performance.

3. Significantly more characterization of the VSEL is needed in order to establish an initial design point, and determine the variability of the array properties.

The development of models and prediction of link/bus performance is predicated on good component definition; which, in turn, is predicated on device and package models and experimental characterization. At all levels there is significant work to be done, both in conceptualization and experimentation.

It is important that a manufacturability assessment be done on the device and packaging directions chosen, even at this early stage. This will prevent the development of approaches which might have been anticipated early on to be low yielding or expensive. A user group meeting has been set-up for Oct. 26 to help in this assessment.

Optical Receiver Array OEIC
for
OETC Optical Bus Project

Description and Specifications
32 Channels/chip

by

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Note: This is an appendix to the DARPA Contract MDA972-92-C-0075 Quarterly Technical Report. It is an engineering working document, and it meant to indicate the status of development for a specification for an optical link receiver. There are many uncompleted sections of this document, and it is expected to evolve as the project continues.

8/23/92 Preliminary	9/25/92					

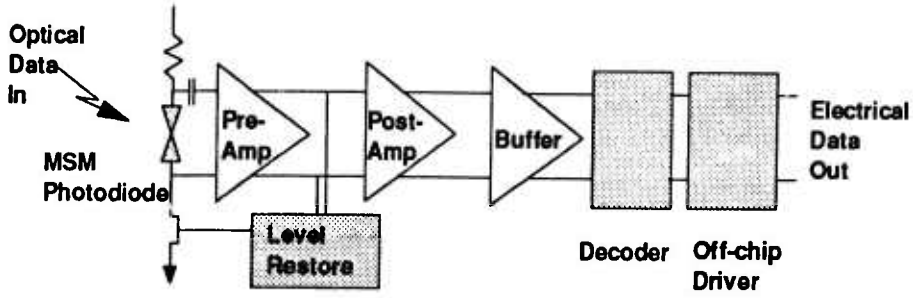
Engineering Changes and Dates

Functional Description

General

This OEIC is an experimental test vehicle to evaluate different candidate structures that will eventually culminate in a 32 channel receiver chip fabricated in GaAs MESFET technology. One receiver channel contains a photodiode, a preamp, a postamp, an optional level restoring circuit, and a decision/decoder circuit. This chip is to be packaged on a module provided by ATT, along with multipler chip(s) provided by GE to form a receiver bus module.

Schematic of Single Channel:



The chip accepts modulated light from 32 multimode fibers, and provides hi- level differential electrical output to wirebond pads. The 32 channels (in the final configuration) are to operate independently, and have low crosstalk so that low BER can be achieved on all channels. The main application of the chip is to provide an O-E conversion for 4 bytes wide of data in an optical bus. Therefore, a main objective is to maintain bit alignment between the data flow through each receiver.

This chip is expected to push the limits of dense receiver array integration . In order to realize density with performance, its design stresses low power consumption, achieved by using a hierarchy of supplies that may include 5, 3.3, and 2.0 volt power supplies, and minimal signal levels to drive off chip. The skew, jitter, and noise implications of this design are to be investigated.

Early test vehicle chips will have accomodation for higher power supplies (+5V) higher drive power (ECL logic levels), and lower density of channels (280 μm pitch) for evaluation and fallback.

Photodiode

An MSM photodiode (PD) is used because it has been shown to be easily integrated into a MESFET IC process.

Also these detectors have low capacitance per unit area, so that fast detectors can be designed compatible with multimode fibers.

The aspect ratio of the detector area can be tailored to match the anticipated shape of the incident optical spot once this has been determined.

Preamplifier

The preamplifier is AC coupled to the PD to make it insensitive to DC link offsets. It may include a level restoring circuit to give the receiver enough optical dynamic range to support input signal levels from adjacent transmitters up to transmitters on other boards (in other equipment) up to 100 meters away.

Amplifier

The amplifier is of differential design to reject common mode noise. It will boost the preamplifier signal to a sufficient level to drive the decoder.

Decoder

The decoder assumes a differential Manchester Coded data pattern. It assumes that bit and byte synchronism has already been established by the link and network. This assumption is made based on the desire for low latency through the network and the presumption that the switched network would have to run synchronously to meet this low latency criteria. The decoder is therefore synchronized with respect to bit boundaries, and will make its decision based on sampling during the first half of the bit interval (the first 1 nsec). The second half of the bit interval can be used to verify the logical decision (if desired). The first half is chosen to minimize the latency through the receiver.

Off-Chip Driver

The off-chip driver circuit is expected to drive hi level signals off the chip, chip carrier, and card to a line receiver on a logic chip. To keep power dissipation low, the design approach will be to use as low a signal level as possible, consistent with low error rate.

Physical Description

- Photodetectors on 140 μ m centers
- Photodiode diameter: 100 μm (subject to change; ellipital shape may be adopted)
- Nominal Chip Outer Dimension: 5.5 mm by 3.5 mm, 0.625 mm thick. 3.5 mm dimension may increase as circuit designs are developed. Wafer thickness tolerance is nominally ± 25 microns, with tighter control possible through wafer screening- at added cost!
- Bonding Pads are 80 μm square, with (Al/Si) top surface metal (thicknesses ??). The TSM is subject to chip foundry eventually chosen, with Au the other candidate.
- The back surface of the chip is not metallized. It will be lapped flat and polished. The current plan is to have it metallized at AT&T with registration features to align the chip to the carrier.

- Alignment marks will be located on the front surface of the chip for (1) aligning the front surface with back surface metallurgy; (2) exploring alternate front surface alignment techniques in the packaging.

- The physical pad layout and functional partitioning of the first test vehicle (TV1) is shown on the attached footprint drawing. The TV1 chip is divided into 16 channels on 140 μm centers and 8 channels (of double width) on 280 μm centers.

- The requirements for EMI shielding of this chip, and wirebond dressing are TBD.

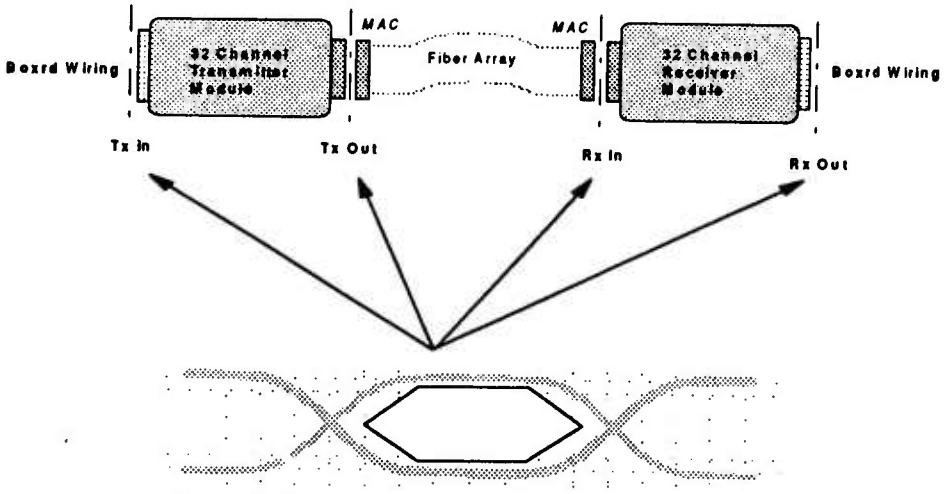
Physical Description- Outstanding Questions and Issues

- What is the max chip size available for the vendor's litho? Is 5 x 4 too large or awkward? Will it severly limit the number of variations that can be tried as test vehicles?
- Is thickness of TSM needed for ATT packaging spec.?
- The I/O pad layout, and wiring will be difficult. Do we need two layers of bonding pads, or staggered bonding pads? Can ATT package this? Do we need more than three layers of wiring on the chip carrier?
- Can AT&T support the necessary pitch/pin count for fully differential outputs?
- Can AT&T support the desired decoupling capacitor network with the anticipated package metallurgy and cavity dimensions?

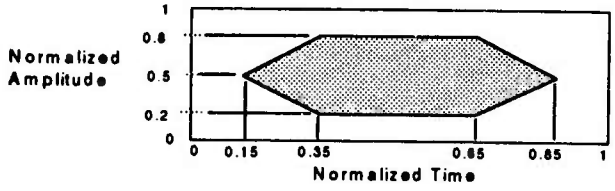
8/23/92 Preliminary	9/25/92					

Engineering Changes and Dates

- **Receiver Latency:** The delay through the receiver and decoder is targeted to be ≤ 1 nsec.
- **Receiver Output Jitter:** < **TBD** psec will be added to the input optical jitter. It is expected that this will be specified in terms of an optical eye template on the photodiode and an electrical eye template off the chip I/O. The diagram below describes this eye template.



Measured Eye Diagram



Eye Mask Specification

- **AC Crosstalk Between Receivers** (adjacent channels): < **TBD** dB will be added to the optical input crosstalk.
- **Skew between receiver outputs:** < **TBD** will be added to the optical input skew.
- **Power Supplies:** The power supplies must provide the following characteristics to the chip. Measurements are to be made at the chip I/O pad.
  - 2.0 volts (off-chip drivers)
  - 3.3 volts
  - 5.0 volts (may be needed for PD+preamp, target is to use 3.3 volts also)

  The three power distribution networks shall be seperately decoupled and brought out to different package pins. It may be desireable in the final configuration to segment each power supply network into smaller clusters, each supporting some fraction of the final 32 channel population.

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Engineering Changes and Dates

Power For:	Max DC Current (32 ch)	Max. AC Current	DC noise	AC noise	Comments
+ mp + ostamp (V_{dd1})	360 mA	30 mA	240 mV	5 mV (p-p)	Noise measured @30 mA ac, 1 GHz BW, all channels operationing
Postamp + Decode (V_{dd2})	390 mA	35mA	270 mV	50 mV	
Off-chip Drivers (V_{dd3})	1000 mA	800 mA	150 mV	200 mV	
	1750 mA				Total chip power <5W worst case

A 5 volt power supply for the PD will also be considered as a backup.

- **Decoupling Capacitors:** The following numbers and values of decoupling capicators are to be provided for the chip. Placement and size of the CAPs are to be described in the physical specifications, as well as any critical placement requirements.

  12 decoupling capacitors, distributed along the 4 mm sides of the chip, adjacent to the power pads:
  0.002 µfd on power supply net to preamp/decisions ckts.
  0.1 µfd for off-chip crivers (total on each net)
  ESR for each - **TBD**

- **Power Dissipation:** 5 watts per chip. Thisis subject to modification once thermal management of the modules is better understood.
- **Signal Levels: TBD**

Electrical Description- Questions and Issues

- Skew is power dependent- how should we specify?
- How do we scale noise in going from 5 to 3.3 volts? I scaled by keeping % the same 7% for preamp, 8 % for logic. I did not scale ac noise-OK?
- Young comments that distributed coupling is required for 32 channels. We need to define distribution.

Electrical Interface (Output from the Receiver Chip)

- **Wiring list:** A wiring list describing the function of each pad will be made here. **TBD**

2 signal I/O per channel = 64 signal I/O
(option) 1 signal I/O per channel = 32 signal I/O

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Engineering Changes and Dates

4 V_{dd1},Gnd @ 2 pads each
4 V_{dd2}, Gnd @ 2 pads each
4 V_{dd3}, Gnd @ 4 pads each = 32 power I/O
10-40 test points - **TBD** ≤ 20 I/O
Clock I/O from decoders @3-5 pads (for optional differential clook output and assoc. grounds)

Approximate I/O count = 77-141

- Identification of all pads, signal levels and power supply values and tolerances. Identify test points and I/O. **TBD**

  Output signal driver current: (specify the load)

- Skew on output signal lines : **TBD**
  The output jitter and noise will be described in terms of an eye mask, as per specified in the link specifications. See above diagram.
- Jitter on output signal lines: **TBD**

Questions and Issues on Electrical Interface

- Need to establish logic levels and drive conditions for DEMUX chip input.
- Need to establish test conditions for wafer level. What is testing approach? Can we mux I/O for testing?

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Engineering Changes and Dates

Optical Interface (Input to the Receiver Chip)

Target Specification
(measured at the chip surface)

Parameter	Minimum Value	Nominal Value	Maximum Value
Wavelength	-	-	850 nm
Optical Spot Size (90% power down)	-	-	70 μm
Spot spacing		140 μm	± 1 μ m
Optical power/spot	-15 dBm	-	-5 dBm
Optical beam overlap (@ PD to PD pitch)		-20 dB	
Extinction Ratio		8:1	
Optical Noise on Hi level			TBD
Optical Noise on Lo level			TBD
Jitter in leading and trailing edge			TBD
Skew between Channels			TBD
Jitter Between Channels			TBD

The input optical conditions are to be described in terms of an eye mask specification, as described in the link specifications. This noise will be specified as a percentage of optical zero/one level; and jitter will be described as a % of bit interval. See the above eye mask description.

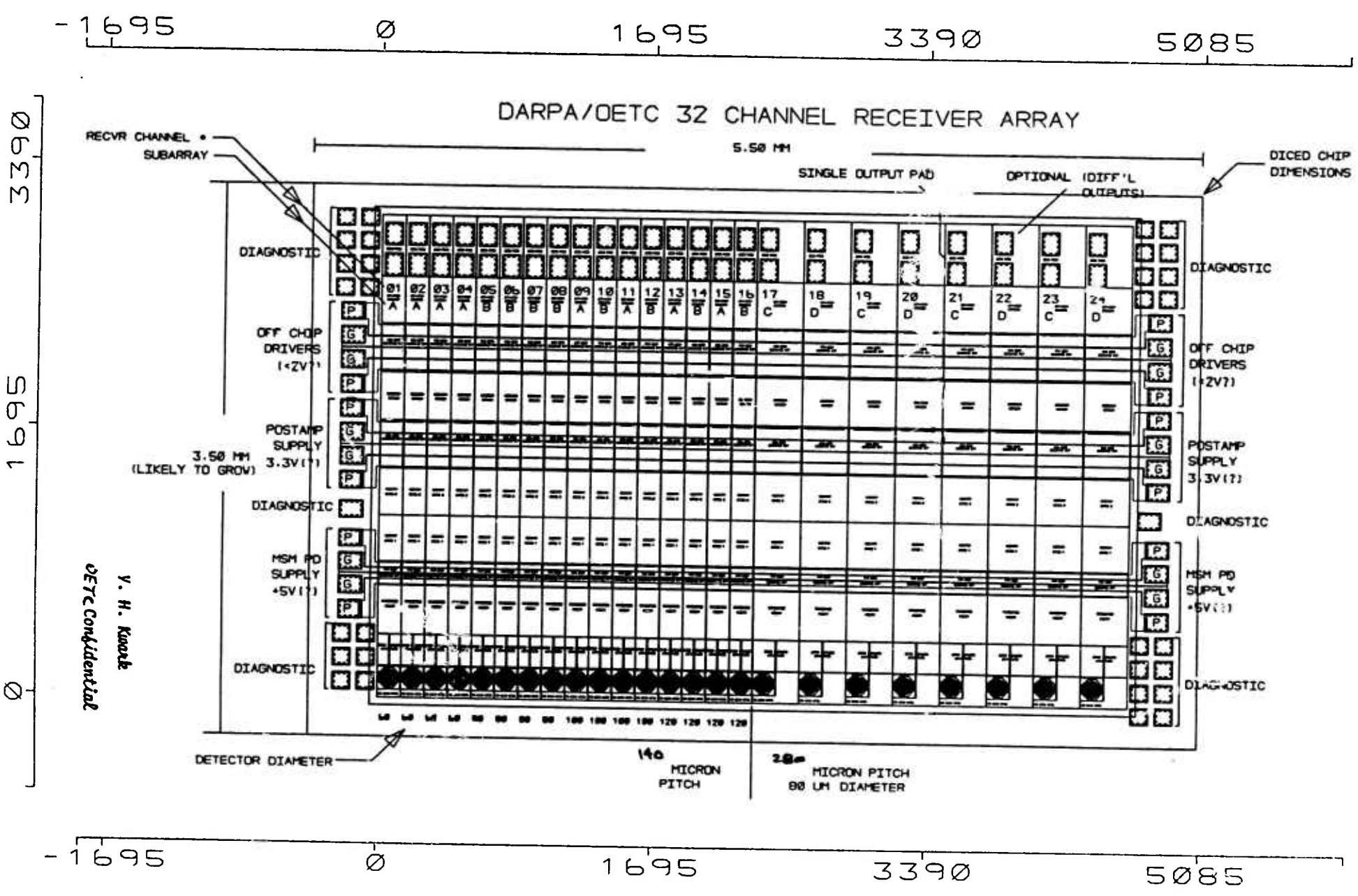
For the decoder to provide valid data at the output of the receiver channel, there must not be phase jumps or excessive jitter on the optical input to the PDs.

Questions and Issues on Optical Interface

- How to specify input distortion and noise? How to test consistently.
-
-
-

8/23/92 Preliminary	9/25/92					

Engineering Changes and Dates


-1695
0
1695
3390
5085
3390
1695
0
DARPA/OETC 32 CHANNEL RECEIVER ARRAY
RECVR CHANNEL
SUBARRAY
5.50 MM
SINGLE OUTPUT PAD
OPTIONAL (DIFF'L OUTPUTS)
DICED CHIP DIMENSIONS
DIAGNOSTIC
OFF CHIP DRIVERS (+2V?)
POSTAMP SUPPLY 3.3V(?)
3.50 MM (LIKELY TO GROW)
MSM PD SUPPLY +5V(?)
DETECTOR DIAMETER
140 MICRON PITCH
280 MICRON PITCH
80 UM DIAMETER
V. H. Kwok
OETC Confidential

DARPA TECHNICAL ACCOMPLISHMENTS PROGRESS REPORT

Reporting Period: July 1992 - September 1992

Author: Young H Kwark

ACCOMPLISHMENTS:

Summary:

Initial sizing of the receiver design was completed during the months of August and September. Most of the issues relating to the optical packaging of the receiver have been identified, and those that impact initial floorplanning of the receiver chip have been closed. Still unresolved are issues relating to design of the off-chip drivers as the protocal for signal levels and signal architecture have not yet been addressed with GE.

DETAILS:

Floorplan:

The initial strategy of two separate receiver array floorplans has been discarded in favor a single geometry that maintains full packaging compatibility with the final fully populated 32 channel layout. The risks associated with the layout of such a dense array on a tight 140 μm pitch will be reduced by incorporating both an aggressive design on the 140 μm pitch as well as a more conservative layout based on a 280 μm pitch as shown on the attached receiver floorplan. The use of a single chip layout will obviate the need for AT&T to develop a multiple sub-connector strategy, albeit at the cost of greater risk for the receiver array design. The single chip array was seen to be the most viable approach to a low cost packaging solution.

Examination of the receiver floorplan will reveal that the array is comprised of 4 subarrays. These subarrays have independent power planes so that in the eventuality that receiver array yield is low, or if the package power dissipation inadequate, subarrays can be independently powered and tested. The power planes have also been segmented into three power supplies each independently decoupled, with one for the noise sensitive preamp/photodetector, one for the postamp/decision circuit, and a high current plane for the off-chip drivers. In order to reduce high frequency L di/dt noise, it is desirable to use fully differential low signal amplitude outputs. This would however place severe requirements on package signal density and pin count as well as wire bond capability. In the eventuality that only one signal output can be allocated per

channel, the power plane feeding the off-chip drivers may need further segmentation. Space has been reserved for on-chip decoupling capacitors, although their inclusion in the final layout await simulations to determine their efficacy. It remains to be seen if the currently envisioned AT&T package can support the distributed decoupling requirements of the receiver array.
The overall dimensions of the chip are approx 5.5 x 3.5 x 0.625 mm. The 0.625 mm thickness dimension currently has a tolerance specification of +/- 25 microns, 2X larger than the tolerance that will be required for optical packaging. This spread can be reduced by mechanically prescreening wafers prior to processing. It may be necessary to allocate funds up-front in order for the semiconductor vendor to have an assured supply of wafers that meet the thickness tolerance requirements.

On-Chip Test Strategy

On wafer screening of receiver arrays prior to dicing will be mandatory due to the high anticipated device count for a fully populated 32 channel array (eg over 10K equivalent devices). Screening will consist of a sequential test of DC parametrics (eg. power dissipation, DC output levels), and time domain functionality testing (rise/fall times, amplitudes, jitter). Full speed time domain testing will be attempted with a fall-back position of reduced data rate (eg. half-speed) if technical obstacles prove too expensive to overcome. The major difficulties with testing involve the large number (32) of high speed signal lines that must be accomodated and the difficulty of coupling the large number of optical inputs to the small area MSM detectors.
The chip testing plan is currently to design and place a MUX array on the chip reticle with wiring traversing the dicing channel that separates it from the receiver array. This will simplify high speed on-wafer screening of the arrays by fanning in 32 channels to a single high speed output. Subsequent to chip testing, the auxiliary MUX array will be discarded automatically by the action of the saw kerf. Samples of polished/connectorized fiber ribbons will be be directly imaged onto the array of MSM detectors, thereby permitting testing of all channels without complicated mechanical stepping fixtures.

Preliminary Test Sites Sent to Vendor:

A mask set that includes several test sites dedicated to the DARPA receiver array has been sent to a GaAs vendor for fabrication. Included are MSM arrays on 140 μm centers with diameters of 60 and 80 μm. These small arrays can be used to evaluate coupling efficiency and optical cross-talk of the optical package. A large diameter (200 μm) MSM detector was also included to facilitate total power measurements. An existing IBM receiver design was modified and laid out on 280 μm centers to form a three channel array. This array can be used for preliminary studies of electrical cross-talk as well as some rudimentary

packaging studies to determine the amount of power supply decoupling that will be needed.

MSM Detectors Sent to AT&T:

A sample of MSM detectors was sent to AT&T to characterize their spectral response. It was determined that a maximum wavelength specification of 850 nm for the SEL array provides an adequate gaurdband. AT&T has been asked to remeasure these detectors at 100 C to verify that the intrinsic bandgap change and gate metal/dielectric stress effects do not change this conclusion when the chips are close to the anticipated operating temperature.

DARPA
Technical Accomplishments
Progress Report

Dennis L. Rogers
IBM T.J. Watson Research Center

September 30, 1992

1 Detector Test Sites

Work has begun to evaluated the capacity of the prospective MESFET foundries to fabricate the integrated MSM detectors. Preliminary MSM detector data has been obtained from test sites on vendor A's mask set. A spread of process conditions were explored to determine the optimum design point. For certain of these conditions detectors with sufficiently high bandwidth, low dark current, and low low frequency gain were measured indicating suitability for receiver OEIC fabrication.

2 MSM model

One of the differences between the MSM detector and more conventional PIN detectors is the presence of low frequency gain. This gain can lead to eye closure and result in a reduction of signal to noise ratio and thus sensitivity. A model of the MSM detector that accurately take this effect into account is needed.

A preliminary circuit model for the MSM detector which is compatible with our candidate vendor foundries has been developed. This model includes the effects of low frequency gain and can be expressed in terms of simple

SPICE circuit models allowing simulation with existing vendor models for their MESFETs.

The model is based on a trap induced tunneling mechanism for the low frequency gain in MSMs. In this model the gain is assumed due to electrons and holes tunneling from the metal contactes into the semiconductor with the tunneling barrier being modulated by the amount of trapped charge near the electrode edges.

The model has four parameters that can be fitted to experimental frequency response data. The figure below shows a fitting of the model to frequency response data taken from detectors fabricated at vendor B. A detector with a particularly large low frequency gain was chosen to illustrate the model's ability to model this gain. As can seen from the figure the response can be modeled to within .3 db of the measured results.

3 Meetings Attended

July: At AT&T Murray Hill, initial meeting with packaging group.
Sept 23: AT IBM Yorktown Heights, meeting with AT&T

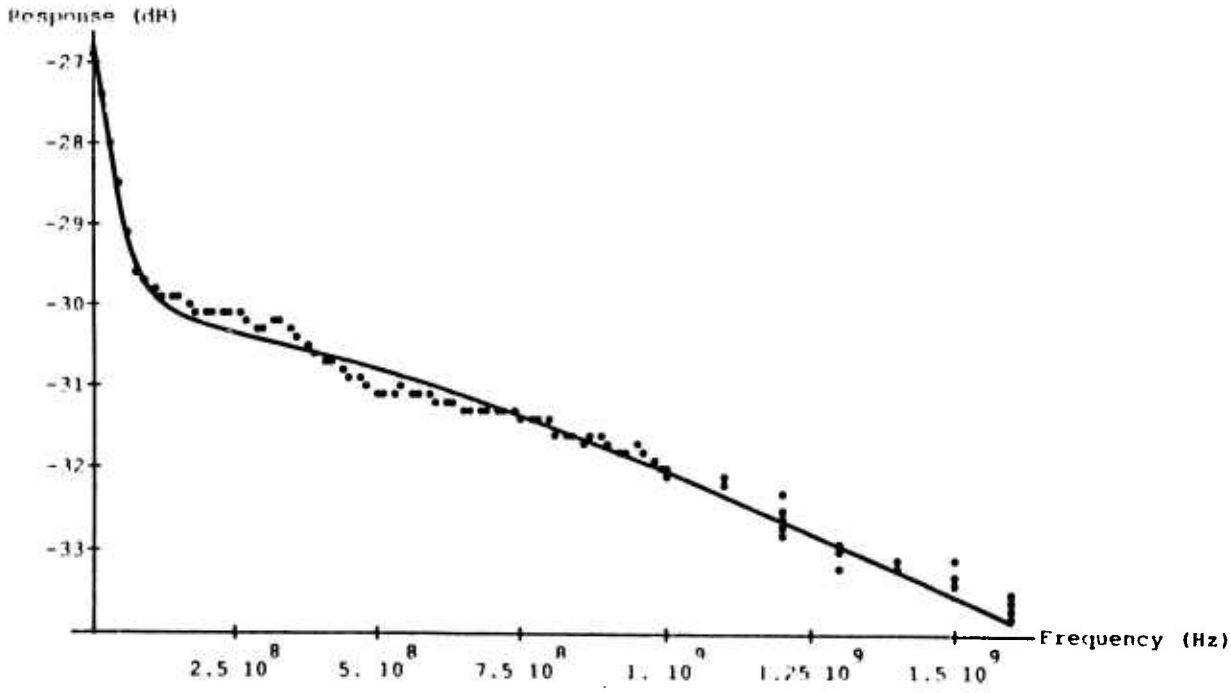


Figure 1: MSM Frequency Response. Model is solid line

OETC: Link Simulation - Report 1
July 1, 1992 - September 30, 1992

R. J. S. Bates
IBM Research Division, Yorktown NY 10598

September 30, 1992

Abstract

This report summarizes the work accomplished during this quarter; it comprises a review of link simulation requirements and potential software tools, a format for link interface specifications, some details of the optical loss budget concerned with noise and some preliminary experimental link results using a prototype AT&T surface-emitting laser and an IBM integrated receiver.

1 Review of Link Simulation Requirements and Potential Software Tools

The OETC link simulator should have the capabilities to model the operation of the whole multi-channel link with sufficient detail so as to be able to investigate the trade-offs in the performance of the different components and to ensure that together they operate successfully to meet the overall system specifications. Thus, it would not be appropriate for the link simulator to includes the sort of device details required by a circuit simulator; nor at the other extreme, should the simulator abstract the individual components to such a level so as to loose the ability the accurately model their interaction. The former approach would necessitate inordinate computation time to model events occurring at rates of 10^{-15}; the latter approach would not provide the sufficient detail.

In 1991 a single-channel optical link simulator (OLAP) [1] was developed with these objectives in mind. It was written to run on an IBM VM/XA 'main-frame' operating system, using ALP2 1.3.00 Release 3 (GDDM V2.3) and required a 3279-type 'graphics' terminal. It employed a technique described recently by Jeruchim *et al* [2] as the 'quasi-analytical' (QA) approach:

- The noise-free signal is propagated through the different components in the link simulator, in the time and/or frequency domain as appropriate, encountering the various band-limiting functions, non-linearities, etc.
- The various sources of noise and interference are evaluated and combined to give the amplitude probability density function at the decision point
- The link bit error ratio (BER) is calculated as the average BER over all the bits in the signal, each at the appropriate signal to noise ratio (S/N)

According to Jeruchim *et al*, the QA approach " should be implemented in any simulation, for several reasons"; these include its speed, that permits it to be used for parametric studies that would otherwise take prohibitively long.

Based on the experience gained developing and using OLAP, and the recommendations by Jeruchum *et al*, it was decided that the OETC multi-channel link simulator should be based on the QA approach; this will allow statistical details of components to be included and give the required level of insight into the whole system.

There are a variety of software tools that could in principle be used to develop the OETC multi-channel link simulator. For example, SYSTID [3] is a very sophisticated QA system simulator with very extensive libraries of communication components; this could be used. Alternatively, a common PC-based spread-sheet programs, like Lotus 1-2-3 or Microsoft Excel, could be configured, with the appropriate 'functions', as a simulator. However, these examples really serve to highlight the important requirements for the simulator:

- It should be powerful enough to allow whatever detailed modeling of the components is required

- It should be flexible, to allow for future extensions
- It should have an easy user interface for input and output
- It should run on common hardware platforms

Based on these requirements, it was decided that the OETC multi-channel link simulator should be written in APL2, with a user interface based on the Application Prototype Environment (APE) Version 2 program; these are programs licensed and supported by IBM. For the normal user, the simulator will be an executable program that will be run on hardware platforms using a DOS, OS/2 AIX or VM/XA operating system. Users interested in extending the program may purchase APL2 and APE and add additional features.

2 Format for Link Interface Specifications

Recent CCITT SONET [4] and Fiber Channel Standards (FCS) [5] have adopted the use of eye diagram masks to specify the optical signals in their systems. Figure 1 shows an example specification from reference [4] of an eye mask; the specification requires that the measured signal is bounded by the parameters $\{x_{1-4}, y_{1,2}\}$. Figure 2 shows a measured eye at $1\,Gb/s$, where an oscilloscope has been configured to count the signal incursion within the 'template'; in this illustration, there have been no 'hits'

The eye diagram mask approach conveniently encompasses the characteristics of rise time, fall time, pulse overshoot, pulse undershoot, ringing, etc. and is compatible with modern test equipment; for example, compliance with the standards can readily be determined using a high-speed photodetector, broad-band amplifier electrical filter and digital storage oscilloscope. The mask approach represents a 'broad-brush' approach to specifying components in an optical communication system, recognizing the need for inter-operability between components from different vendors and a relatively un-sophisticated user community.

It was decided that the eye diagram mask approach should be adopted for the external interfaces of the OETC multi-channel link. These masks will *not* be the only specifications - some of these are discussed in the next section - but they will be the *only* specifications, except for BER, tested at the link level.

Like its application for CCITT and FCS systems, the mask approach will simplify testing the overall compliance of the link components. However, the most important reason for its adoption here is that it approaches the necessary simplistic specification that will be demanded by the user community, in order that they may design systems using 'optical bus' technology; the user will not be skilled in optical communications - it would, for example, be quite inappropriate to specify arcane noise penalties.

It is proposed that there be 4 external interfaces of the OETC multichannel link; these interfaces are illustrated in Figure 3. The 2 electrical specifications have yet to be determined, but may be ECL-like. The 2 optical specifications have not yet been determined, but will be based on some of the considerations discussed in the following section.

3 Some Details of Optical Loss Budget

The following details are proposed for the external parameters of the surface-emitting laser (SEL); all figures are for 1mW output CW, over range 10-50 C except where noted.

Voltage drop	$< 3.0v$
Drive current, including bias	$< 10mA$
Center wavelength	$< 850nm$
Relative Intensity Noise at 1GHz	$< -125dB/Hz$
Turn-on delay, without pre-bias	$< 50ps$
Fiber coupling noise penalty (1)	$< 0.5dB$
Receiver coupling noise penalty (2)	$< 0.5dB$

1. Penalty measured at 10^{-9} bit error ratio (BER) at $1Gb/s$, coupling into a $50/125\mu m$ multimode fiber placed $100\mu m$ above emitting area, with a $3dB$ coupling loss

2. Penalty measured at 10^{-9} BER, coupled into a $75\mu m$ diameter detector with a $3dB$ coupling loss

4 Preliminary Experimental Link Results

A single-channel channel link has been constructed using a prototype AT&T SEL and an IBM integrated pre-amplifier receiver, to study some of the noise mechanisms associated with these devices. Measurements so far have concentrated on a SEL that is relatively single-mode at low power levels. The components have been operated error-free at $1\,Gb/s$, transmitting a $2^7 - 1$ pseudo-random data sequence over $10\,m$ of multimode fiber. Figure 4 shows an example of an eye diagram, measured at the receiver output.

Measurements have been taken to investigate the sensitivity of the link to changes in the laser bias. For the one device studied, it was observed that the relative intensity noise (RIN) of the laser was high near threshold; this may be due to the proportionally higher levels of spontaneous noise in SEL, compared to standard stripe lasers. Figure 5 shows the effects of operating the laser with the optical 'zero' level first $2\,mA$ above threshold and then at threshold; in the first case, the link BER decreases as expected with increased receiver optical modulated power; in the second case there is evident signs of an 'error floor'.

Measurements have also been taken to investigate the sensitivity of transmitter fiber misalignment, above the SEL. In the experiment the SEL was biased so that the optical 'zero' level was $2\,mA$ above threshold, to avoid a RIN penalty. A $50/125\,\mu m$ multimode fiber was placed $100\,\mu m$ above the SEL and aligned to maximize the coupling (90%). The link BER was measured. The transmitter fiber was then misaligned to give an additional $3\,dB$ coupling penalty and the BER re-measured. Figure 6 shows that for this arrangement of laser bias and coupling height, there was no sign of coupling noise penalty.

References

[1] R. J. S. Bates, "Optical link analysis program: general description and user's manual," *IBM Research Report*, September 1991.

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[4] Study Group XV, *Draft Recommendation G. 957 - Optical Interfaces for equipments and systems relating to the synchronous digital hierarchy.* Geneva: International Telegraph and Telephone Consultative Committee (CCITT), August 1990.

[5] I. D. Allan, ed., *Fibre Channel: Physical and Signaling Interface, Rev. 3.0.* New York: American National Standards Institute, 1992. section 5.6.5.

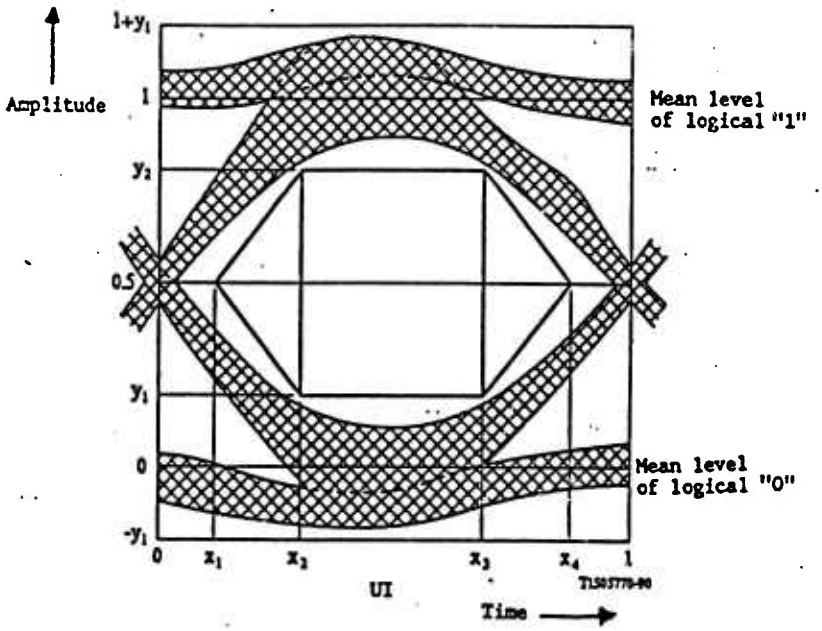

Figure 1: Example: Eye mask specification from reference 4

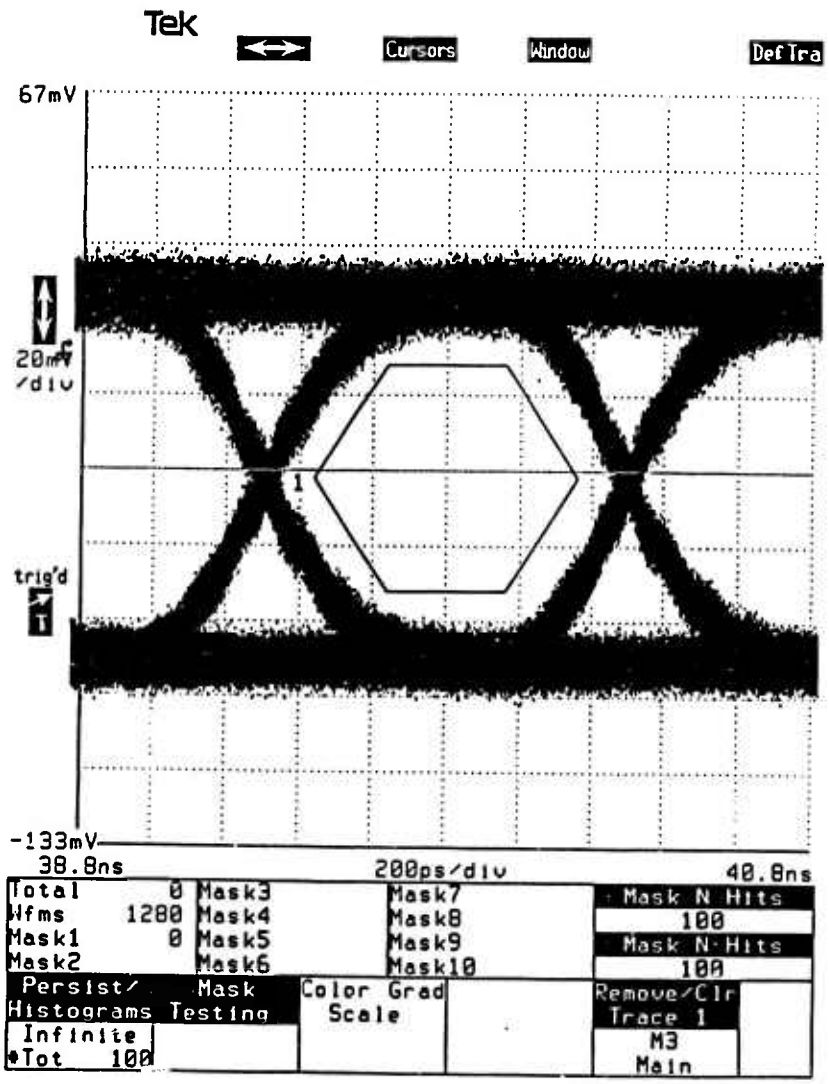

Figure 2: Example: Eye mask measurement

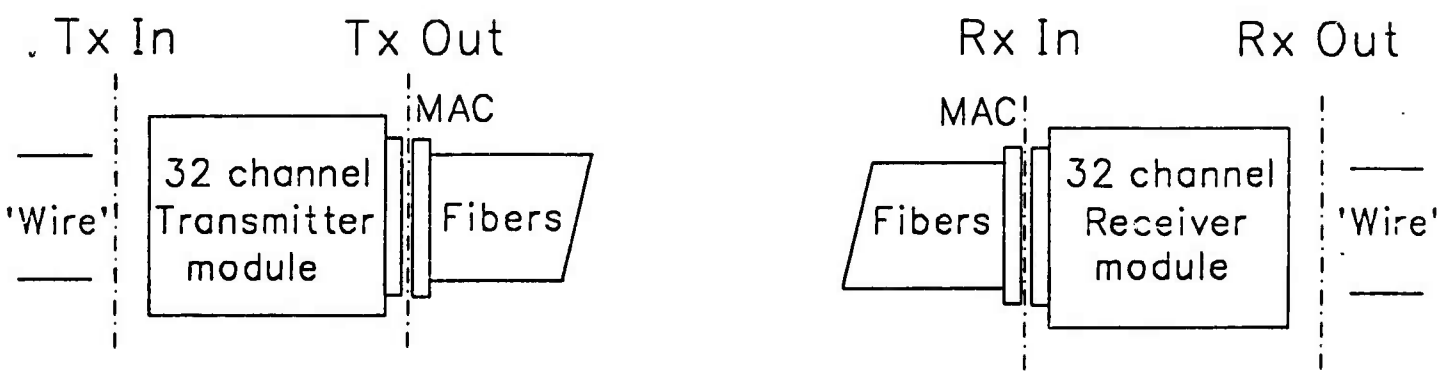

Figure 3: External Interfaces in OETC Multi-channel Link

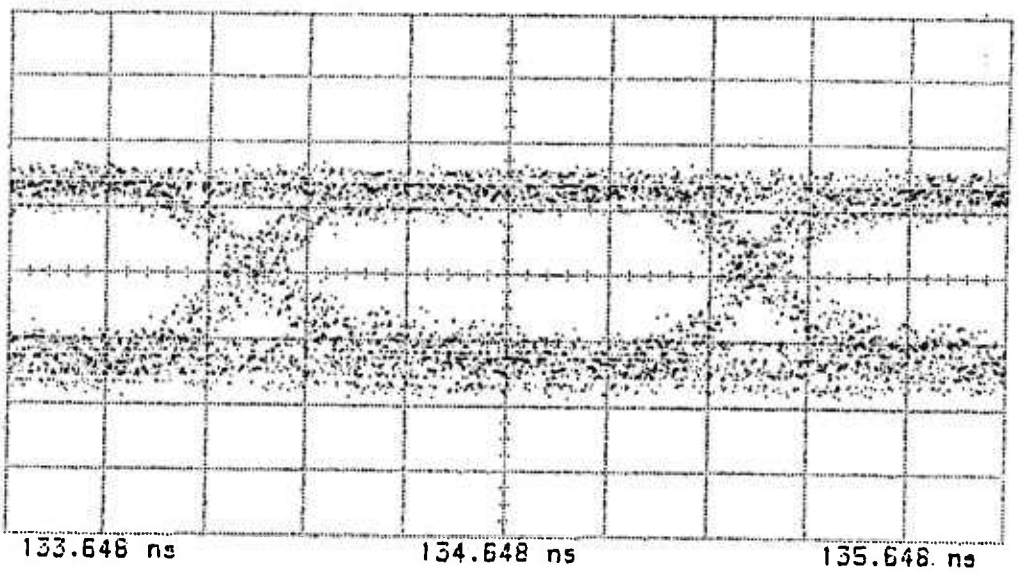

Figure 4: Measured Eye Diagram of Prototype Single-Channel Link at 1 Gb/s

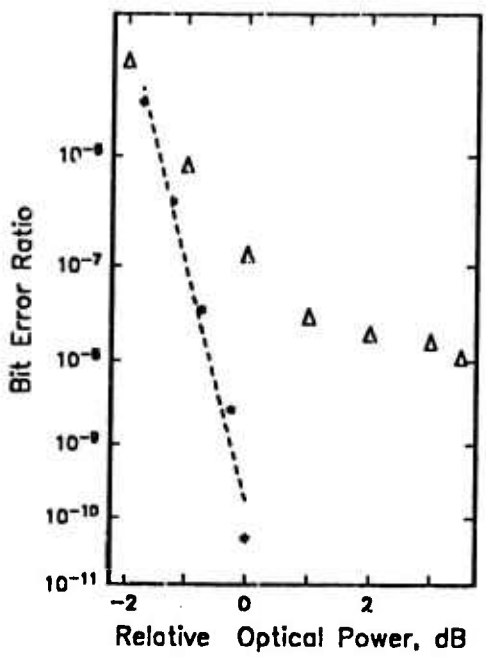

Figure 5: Measured BER: laser biased with optical 'zero' level $2\,mA$ above and at threshold

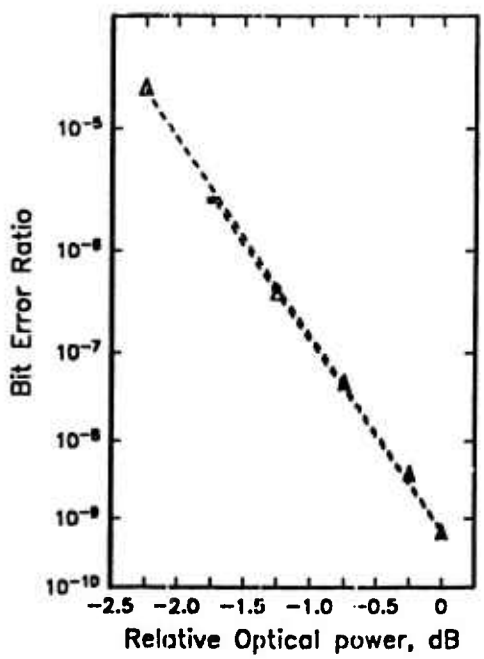

Figure 6: Measured BER: effect of 3 dB coupling loss due to transmitter fiber misalignment