IMPROVED FIELD EMITTER CURRENT DENSITIES AND STABILITY THROUGH THE APPLICATION OF A PROPRIETARY PROCESS

CONTRACT MDA972-92-C-0033
QUARTERLY REPORT #4 December '92 - February '93

1. INTRODUCTION

As detailed in the previous reports, the necessary current densities (60 A/cm^2), linear current densities (3 mA/mm) and stability (> 2 days) to meet the contract goals (at least theoretically) have been achieved. The next step is to fabricate three terminal devices to demonstrate the remaining contract goal - a one GHz current gain cutoff frequency (f_t).

During this period the design of the three terminal devices was completed and the mask set was received at the end of the period.

RF modulation at one GHz was also demonstrated using the old two-terminal designs described in the past reports. Modulation was demonstrated as high as 2 GHz with an incremental gain in s_{21} of 0.5 dB.

2. RF MODULATION AT ONE GHz

In an effort to measure rf modulation at one GHz in time for the on-site DARPA Vacuum Microelectronics Review held February 22 at GRC, chips using the anode-less old design were used. The mask set for the new device designs with monolithic anodes were not due to be in until early March (see Section 3). Fig. 1 shows the microwave fixturing used for the rf measurements, with the anode spaced ~ 0.6 mm above the emitter-gate chip. As discussed in the previous report, only a small percent (~ 1% or so) of the emitted electrons can be collected from an anode spaced such a long distance away.

Fig. 2 shows the rf test setup used to obtain the following measurements. Many devices were tested, out only the best of the results are presented for the sake of clarity and brevity.

Initially the TEK495P spectrum analyzer was used, with the thicking being that the narrow detection bandwidth would keep the noise floor lower. The data in Fig. 3 was obtained at 100 MHz. With the anode voltage fixed at 200V (the highest the bias tees will permit), the lower plot is for no gate bias and the upper curve is for 200V on the gate, resulting in about ~1μA of anode current.

With the input and output impedances of the devices negligible compared to 50Ω, the simple model of Fig. 4 applies for no matching. Thus, the output power is

$$(1) \quad P_{out} = \frac{|v_1|^2 (g_m^2 + \omega^2 C_f^2)}{R_0 \left(\left[\frac{1}{R_0} \right]^2 + \omega^2 C_f^2 \right)}$$

The lower curve of Fig. 3 is for $g_m = 0$ in the above expression and the upper curve gives the data from which g_m can be solved. Doing this give $g_m \cong 0.08\ \mu S$, and with

$$(2) \qquad g_m = 12.44\frac{I}{V}$$

then $I = 1.28\mu A$, which is about right. The feedback capacitance can also be solved for giving $C_f = 0.00034pF$. The resulting small-signal model is shown in Fig. 5.

At one GHz, the noise ($g_m=0$) floor rises to around - 31 dBm, making it impossible to detect emission modulation. A rise of 20 dB would be expected from the term, but the 47dB rise observed probably reflects the noise floor characteristics of the spectrum analyzer. To get around this problem, the network analyzer was used. Its noise floor at one GHz was around -60 dB, more than sufficient to see rf modulation. After zeroing out the noise floor, the data in Fig. 6 was obtained. About 0.5 dB incremental increase in s_{21} was obtained at 2 GHz. $|s_{21}|^2$ is the actual power gain in an unmatched microwave circuit. The frequency dependence in Fig. 6 suggests some matching, possibly due to the long bond wires used.

Ignoring C_f in Fig. 4,

$$(3) \qquad s_{21} = -2g_m R_0$$

If matching is used to provide an effective transformer turns ratio of n_1 at the input and n_2 at the output, s_{21} improves to

$$(4) \qquad s_{21} = -2n_1 n_2 g_m R_0$$

at the matching frequency. Away from this frequency, the matching and hence s_{21} degrades, giving the response in Fig. 6. Eq. (4) applied to the Fig. 6 data gives a matching coefficient of $n_1 n_2 \cong 20$.

Summarizing, rf modulation was observed at one GHz. Applying the data to theory resulted in emission currents consistent with those actually used. A simple small-signal model was derived from the data.

3. NEW DEVICE DESIGN

The problem of the trajectory simulations mentioned in the last report was resolved. The grid resolution at the emitter tip was continually increased until the trajectory parameters 1000Å away from the tip converged to fixed values. The electrons were then started with these parameter values for the low resolution grid pattern, giving 10-12 microns of trajectory length independent of the grid resolution (2, 4, or 6 grids per 0.5 micron).

Fig. 7 gives the device layout for the new mask set. Layout A is as in Fig. 8 (b), layout B is similar, but with no ohmic metallization under the air bridge (to avoid electrons hitting any grain boundaries). Layout C is as in Fig. 8 (a) with an air bridge to act as a focusing electrode. This extra electrode is needed to prevent the electrons from landing on the gate before reaching the anode in the Fig. 8 (a) planar scheme. Although the simulations show that the electrons can span a

10 micron wide gate, the actual devices emit at a 30° trajectory (vs the 45° angle of the simulation), so the fourth electrode was inserted as a precautionary measure. Layout C2 if the same as C except there is no metallization in the gate stripes to avoid contact with emitted electrons. Layout D is the self-aligned version of Layout A. The self-aligned technique is used in place of E-beam exposure to define the emitter-gate gap, and can usually result in smaller gap distances and threshold voltages. Layout E is a self-aligned structure with a planar emitter and anode with the air bridge gate directly above the emitter.

The mask set for the Fig. 7 designs was fabricated by Hewlett Packard and received at the end of this reporting period. Device fabrication will commence immediately.

4. DEVICE WIDTH

The device layouts in Fig. 7 are all 200 microns wide. This width is typically double that for GaAs FET devices. Larger values would reduce significantly the number of devices available to test all the concepts mentioned in Section 3 (single crystal vs air bridge anodes, metallized vs unmetallized gates, and self-aligned for lower thresholds).

In carrying out the task of Section 2, it became very apparent that the power gain was taking a large beating due to the severe impedance mismatches occurring at both the input and the output when tested in the standard 50-ohm system. For example, Fig. 9 shows a frequency independent equivalent circuit having a maximum available gain (MAG) of 8 dB when fully matched. This gain value is independent of width. However, the gain s_{21} in a 50-ohm system without matching is given by Eq. (3) as -40 dB, a 48 dB drop! Matching circuits can help, but they themselves become too lossy if trying to overcome impedance mismatches of more than 10:1. A better solution is to make the device wider and then fine-tune with matching circuits.

If Z is the device width, r_i and C_i the input resistance and capacitance, and r_0 the output shunt resistance, then the optimum device width is given by

$$(5) \quad Z^3(125{,}000\omega^2C_i^2) + Z^2(2{,}500r_i\omega^2C_i^2) - 50Z(r_ir_0\omega^2C_i^2) = r_0(1+\omega^2C_i^2r_i^2)$$

For the expected parameter values for the Varian design, Z values of around 10 mm are expected to be optimum.

5. CONTRACT SUMMARY

This is the last quarterly report of the contract. The final report will be written and include in it preliminary measurements of the device runs made with the new mask set.

Fig. 1 Microwave fixturing for the rf measurements

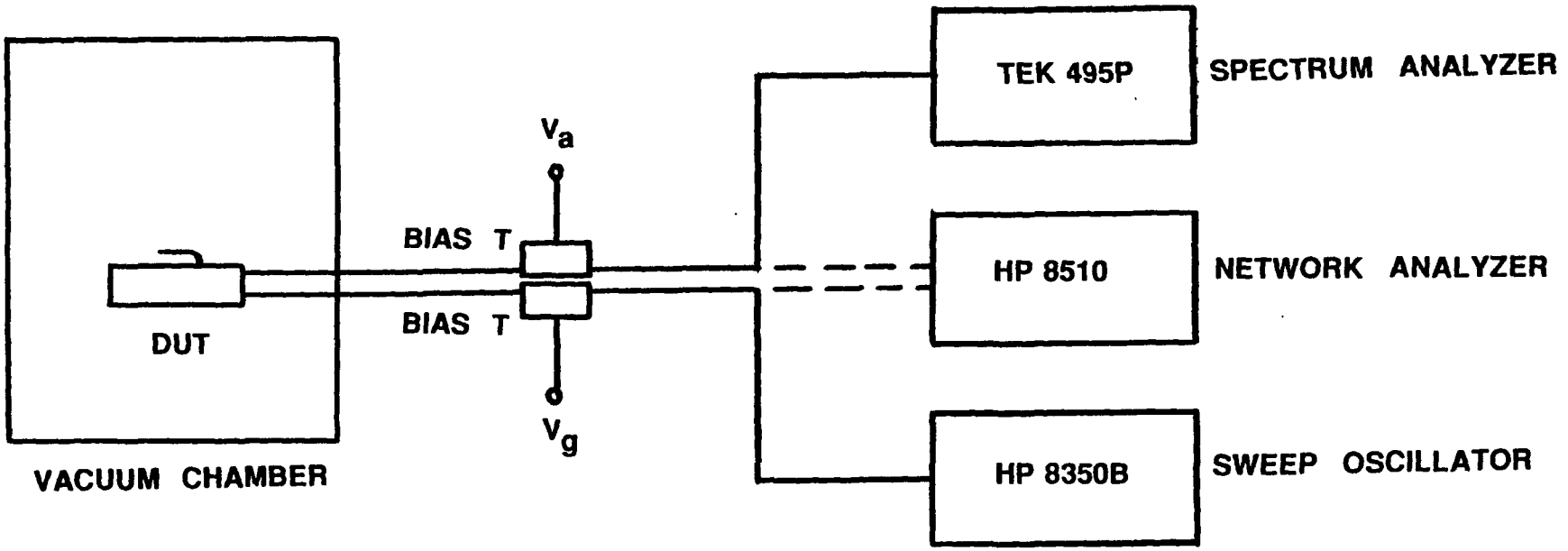


Fig. 2 RF test setup

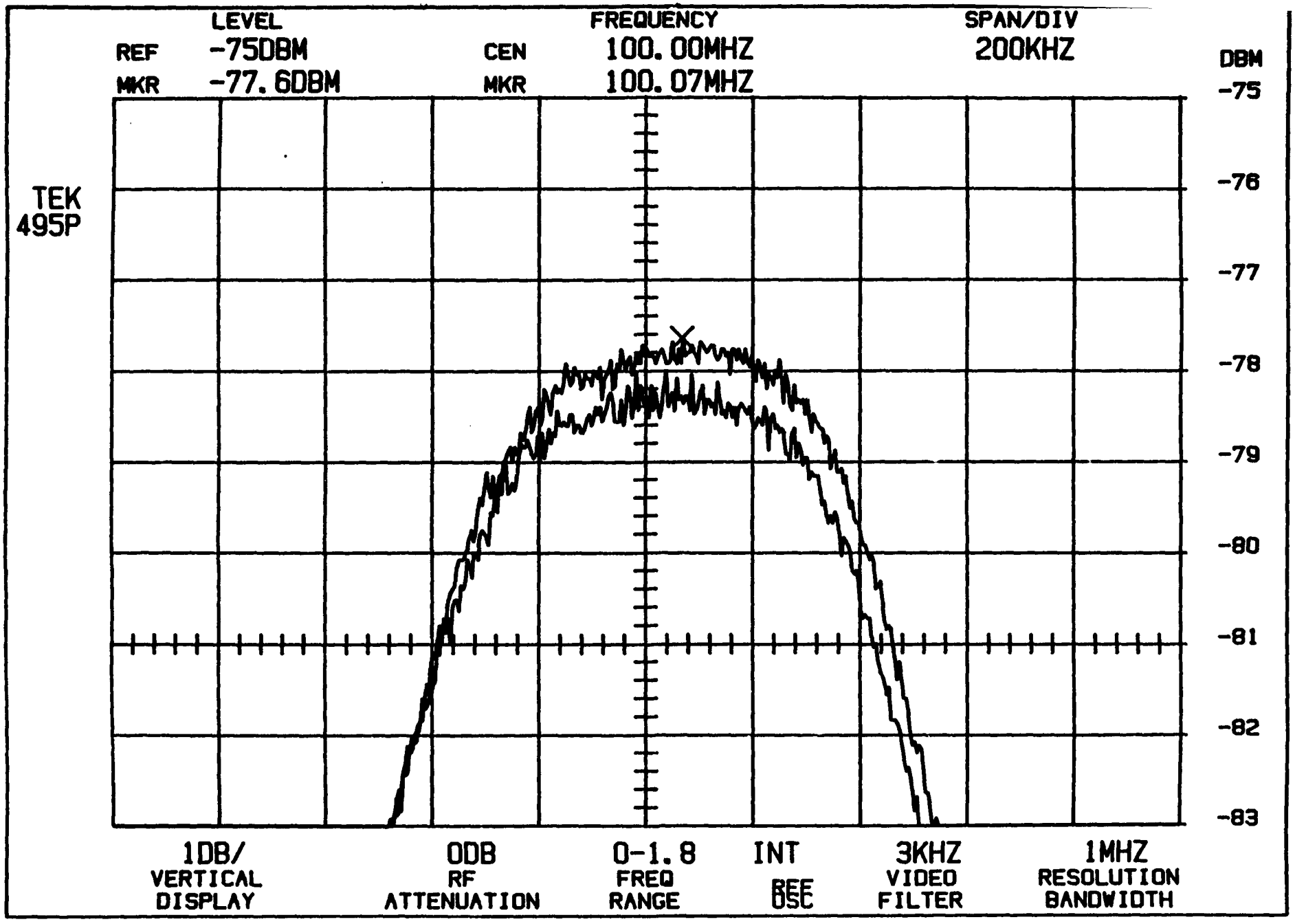


Fig. 3 Spectrum analyzer data

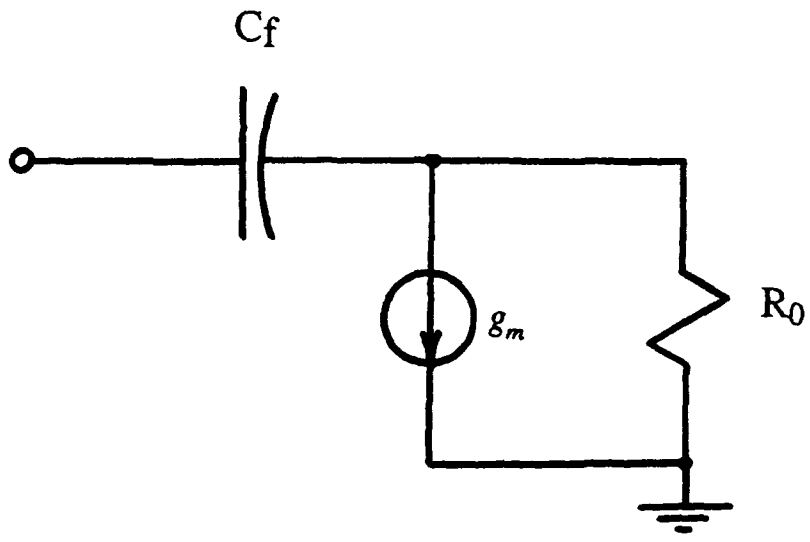


Fig. 4 Simple small-signal model

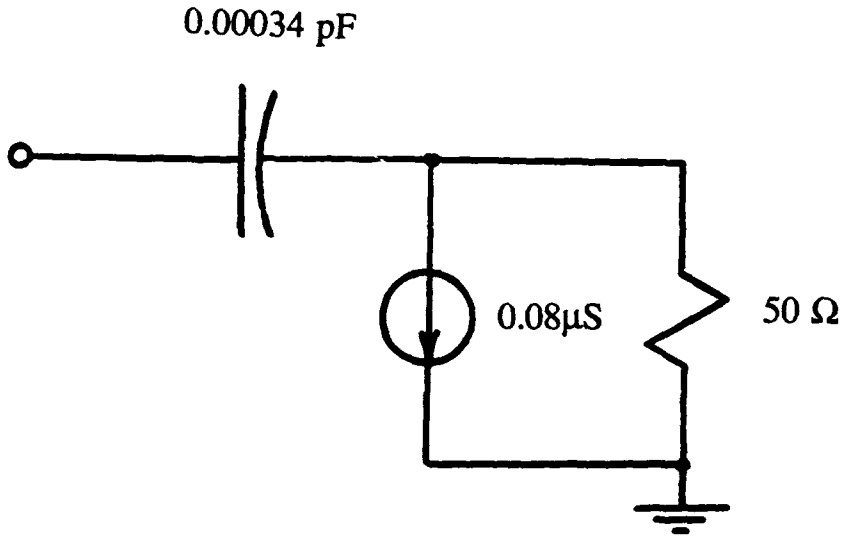


Fig. 5 Model values from the data

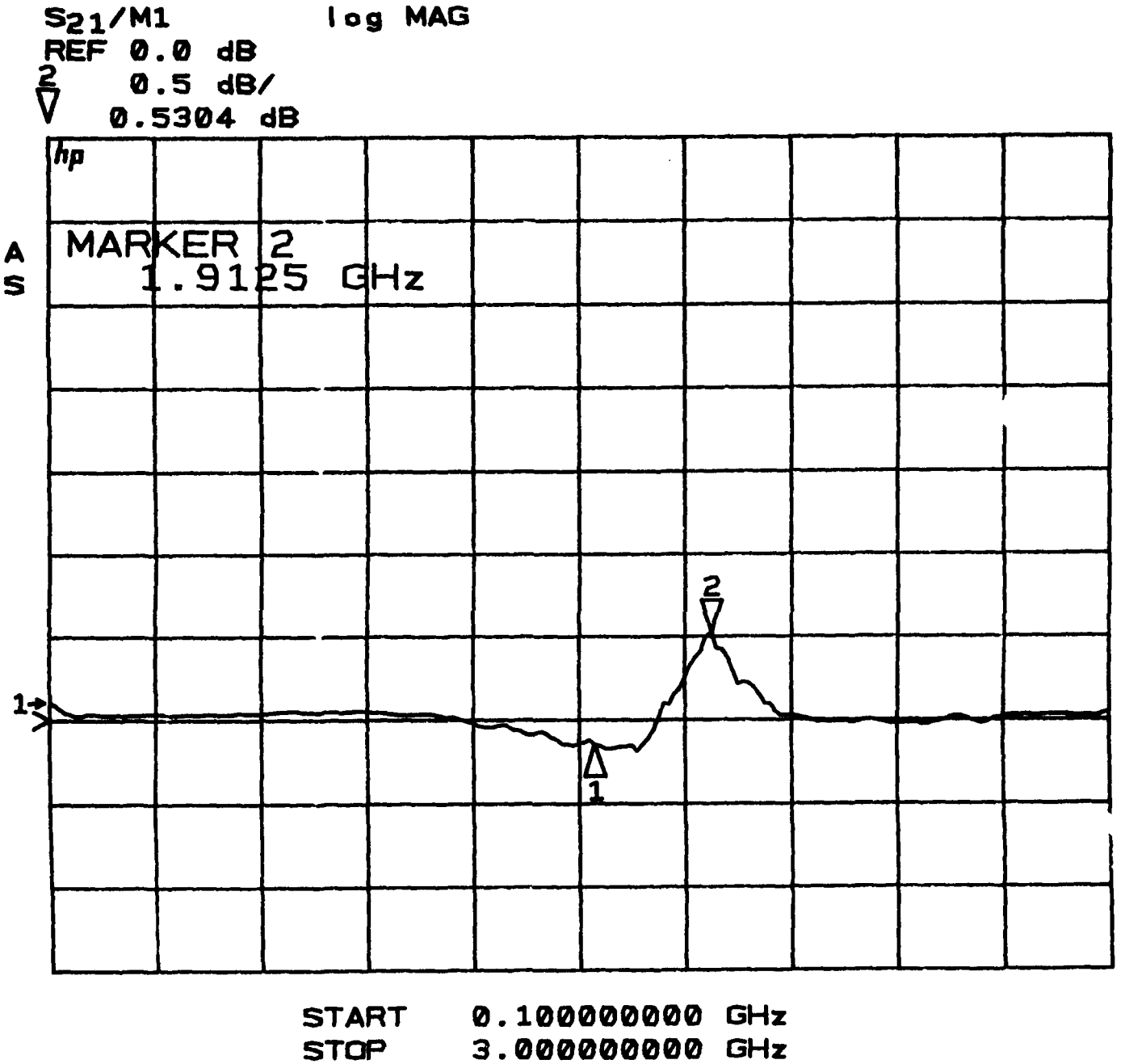


Fig. 6 Network analyzer data

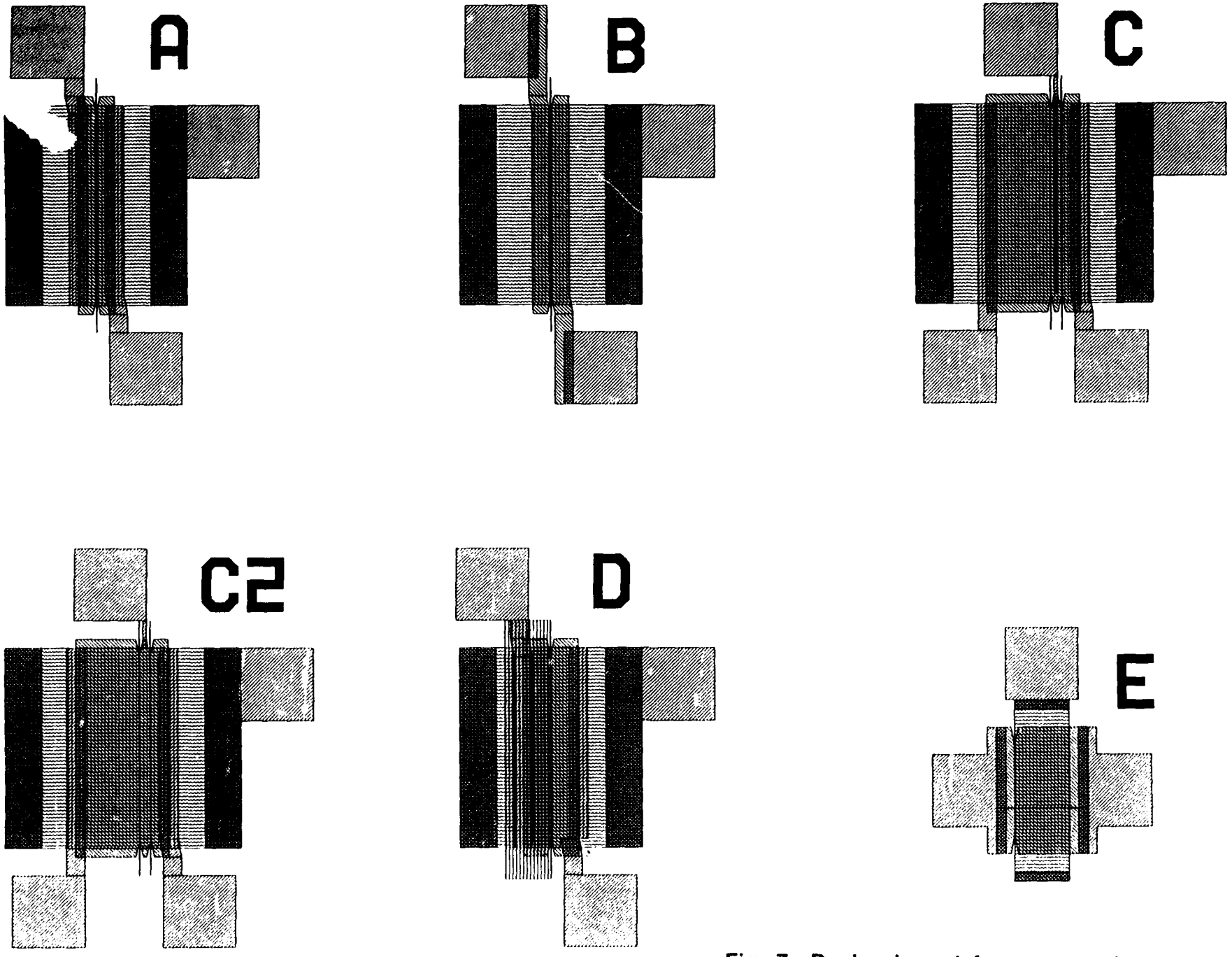


Fig. 7 Device layout for new mask set

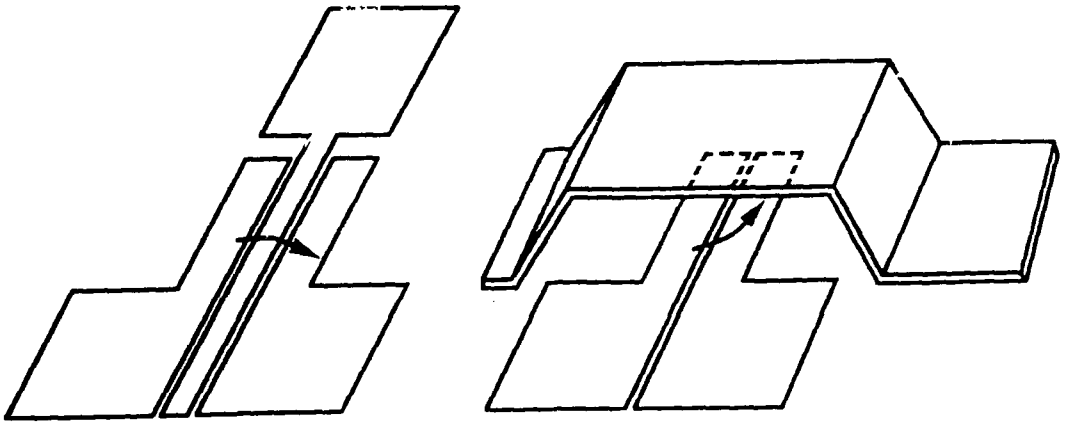


Fig. 8 Anode placement schemes

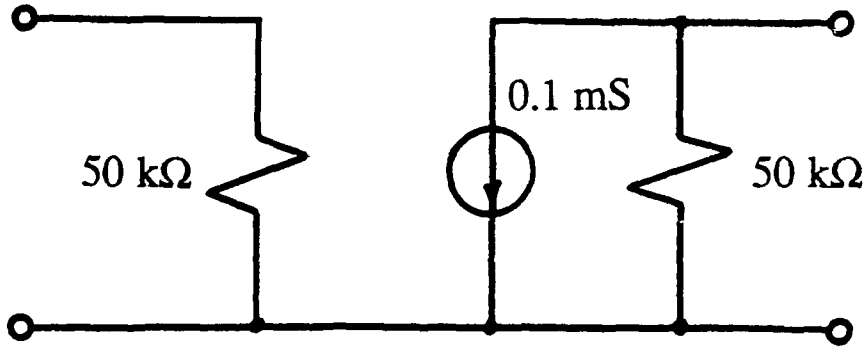
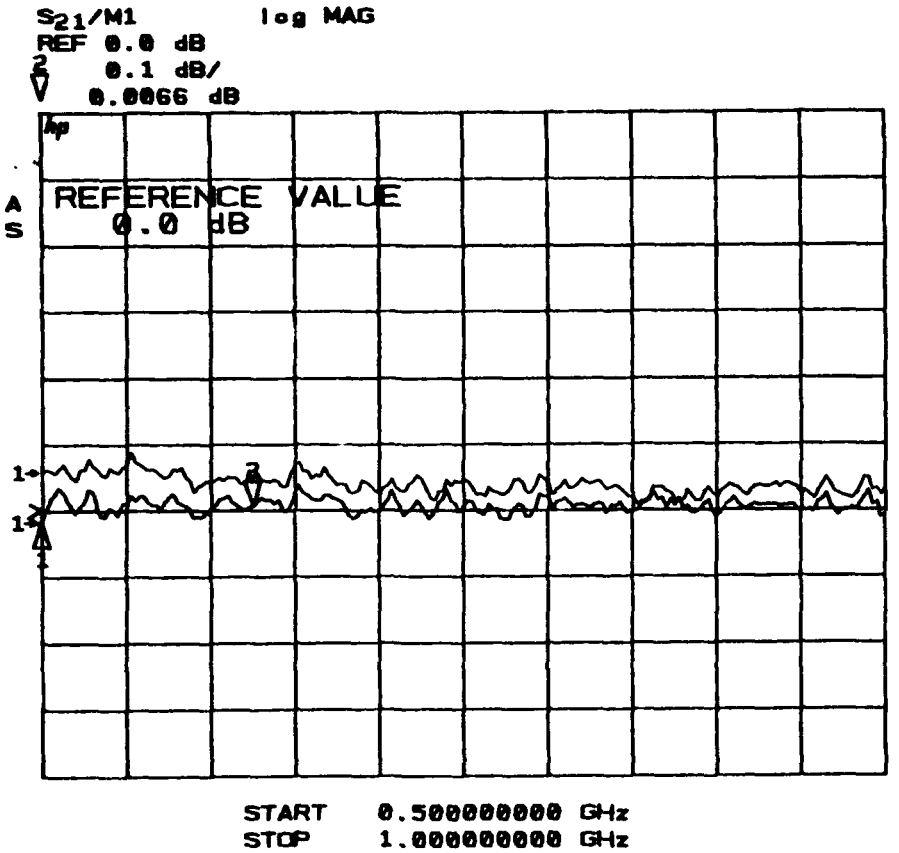


Fig. 9 Equivalent circuit illustrating poor impedance match

Latest Results

The following page shows a photo of one of the devices recently obtained form the new mask set, along with the rf results obtained from 0.5 to 1.0 GHz. The device has an air bridge anode ~2 microns above the emitter-gate structure. The lower plot is for zero anode current and the upper plot is the increase in s_{21} due to 0.15 mA of anode current. s_{21} is the power gain in a 50 ohm system with no matching either at the input or the output. The device width is 200 microns. We believe these rf results are the first for a field emission transistor with all three terminals fabricated monolithically on the same wafer.


S21/M1
log MAG
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0.1 dB/
0.0066 dB
REFERENCE VALUE
0.0 dB
START 0.500000000 GHz
STOP 1.000000000 GHz

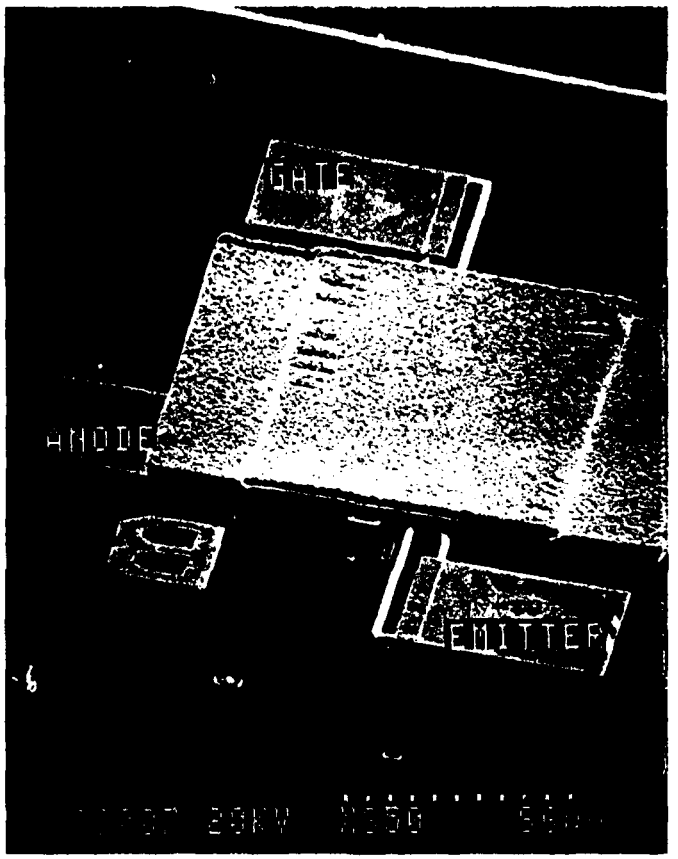
GATE
ANODE
EMITTER

Fig. 1.10