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A SINGLE-TRANSISTOR MEMORY CELL AND SENSE AMPLIFIER FOR A GALLIUM ARSENIDE DYNAMIC RANDOM ACCESS MEMORY

by

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A Single-Transistor
Memory Cell and Sense Amplifier
for a Gallium Arsenide Dynamic Random Access Memory

by

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I. INTRODUCTION

A. BACKGROUND

Gallium Arsenide (GaAs) has been used commercially since the 1960's in the microwave/optics field. Many advances in GaAs technology have occurred since then. It has been in the last ten or so years that GaAs has started to play a more important role in digital integrated circuits. In applications where speed is required and power consumption is not a big concern, GaAs is now a strong contender with Emitter-Coupled Logic (ECL).

GaAs is a compound semiconductor with properties that in many respects are much better than those of silicon (Si). These properties also pose different problems than the properties of Si. For this application, some of the worst properties are the leakage currents. Digital integrated circuits utilizing GaAs are still part of a young field with many different and varied topics in which to do research.

The main advantages [Ref. 1] of GaAs are:

Short logic gate propagation delays-- Typically around 10-150 picoseconds compared to nanoseconds for Si.

Low power consumption-- GaAs typically dissipates more power than Si, but for Si circuits operating at the speed of GaAs, GaAs is far superior. The Power-Delay Product (power dissipated x propagation delay) is a good measure for comparison and it gives GaAs a 5:1 advantage in favor of GaAs.

Radiation hard-- There are two problems that circuits have with radiation. The first of these is single event upsets where a nuclear particle collides with a transistor and causes an incorrect voltage level to appear in the circuit. Both Si and GaAs suffer from this problem. The second problem, substrate degradation from bombardment, is a 'Si only' problem and means that after a period of time the Si circuit will eventually stop working.

Optical properties-- GaAs has been widely used in optics.

The disadvantages [Ref. 1] of GaAs as claimed by Si:

Lower logic density--The technology for GaAs fabrication is approximately a generation behind that of Si. This greatly reduces the density of the circuits as does the odd layout shape of the GaAs logic gates.

High Input/Output delay to propagation delay ratio-- The delay of a signal on a glass epoxy circuit board is approximately one nanosecond per foot. This, compared to picosecond logic propagation delays is a big problem. Due to the

very small delays and high operating speed. GaAs suffers from all the problems and effects of transmission lines. Therefore, GaAs design and layout must take transmission line theory into consideration.

High power dissipation for high speed logic-- This is true, but as technology improves the power dissipation is decreasing. Si has an even higher power dissipation for very high speed logic.

Some other disadvantages that may have been true a year ago are that GaAs is more costly and difficult to design. The costly part is no longer an issue. As more GaAs chips are fabricated, the cost continues to drop, and it is now comparable to Si. The difficulty in the design stems from the lack of design tools available to design GaAs circuits. Spice and MAGIC are now available. Other difficulties arise from the few small manufacturers that fabricate GaAs chips -- the design specifications vary from manufacturer to manufacturer.

B. GaAs DYNAMIC RANDOM ACCESS MEMORY

With the continual improvements in processing power and speed of Central Processing Units (CPUs), the mismatch between CPU and memory is getting larger and larger and the CPU is 'waiting' for memory more and more. The need is ever increasing for a Dynamic Random Access Memory (DRAM) that can better cater to the speed requirements of the CPU. Dynamic memory is being sold with a 50 nanosecond access time while static memory can be found with approximately a 10 nanosecond access time. With GaAs, it is possible to reduce this access time to much less than one nanosecond. The access times would be much less than this if power and space requirements were not an issue.

This thesis will present some basic designs of GaAs DRAM cells and then focus on a One-Transistor DRAM cell. It will cover charge storage and maintenance, sensitivity, refresh, timing, simulation, layout and final testing.

II. DYNAMIC RANDOM ACCESS MEMORY

A. DIFFERENT CONFIGURATIONS

A dynamic circuit is one that performs logic by the storage and evaluation of charge on circuit nodes. DRAM cells, or models, differ by where the charge is stored. The charge can be stored on the gate, drain, or source of a transistor, or combinations of the above. Because Si is developmentally about one step ahead of GaAs, an interesting method to use in designing GaAs circuits is to try designs that worked well with Enhancement and Depletion Mode FETs in Si. The problem here is that Si and GaAs have very different properties. Where Si transistors can be considered either "on" or "off", GaAs transistors, due to leakage currents, are more "gray" in their operation. The effects of these leakage currents will be discussed later. The two different models for a DRAM cell that have been shifted to GaAs are the basic Three-Transistor Model and the One-Transistor Model.

1. Three-Transistor Model

The Three-Transistor model is obviously named for the three transistors that make up the cell. A diagram of this model can be seen in Figure 1. The three-transistor model is inverting, that means that a stored high is read as a low and vise versa. Referring to Figure 1, the charge is stored at node D. If the charge is high, a ONE is stored although a low will be read.

a. Write

Referring to Figure 1, to Write a ONE (high): Tie node C low and turn transistor 3 on by briefly pulsing node A. This effectively makes node D low, or to say it another way, a low is stored at node D. Since node D is low, transistor 2 is off.

To Write a ZERO (low): Tie node C high and turn transistor 3 on by briefly pulsing node A. This effectively makes node D high, or to say it another way, a high is stored at node D. Since node D is high, transistor 2 is on.

b. Read

To Read the Three-Transistor Cell requires that the BIT I/O (BIO) line be precharged to a high. On the next half cycle, turn transistor 1(Figure 1) on by pulsing node B. If the charge stored at node D is high, transistor 2 is on and the BIO line is dragged low through transistors 1 and 2. Therefore, a low is read. To Read a high, the BIO line is precharged high again, but this time transistor 2 is off and the BIO line is not dragged low, it stays high. Hence, a high is read.

c. Operation

The operation of the Three-Transistor Cell is not fully explained by covering a Read and Write cycle. There is also a little matter of refresh that must be considered. Refresh is the name given to the act of replenishing the charge stored. Due to leakage, the charge stored at a node will not last indefinitely and must be replenished from time to time. To do this for the Three-Transistor Cell requires Reading the cell, arranging node C to be pulled high or low (the inverse of what was read), then pulsing node A to turn on transistor

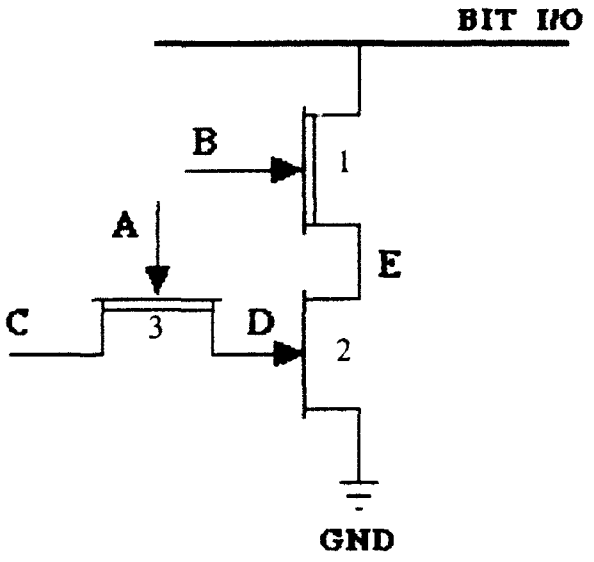


Figure 1. Three-Transistor Ram Cell

3 and replenish the charge. Basically, it is a Read followed by a Write with a period of time in between for determining whether the following Write will be a ONE or a ZERO.

2. One-Transistor RAM Cell with a Diode

The number of transistors in the cell is the obvious source for the name of the One-Transistor Cell. The second transistor is actually used as a capacitor and does not count as an active transistor. This model, with some of the required support transistors, can be seen in Figure 2. The transistor used as a diode can be either an enhancement or a depletion mode transistor. The behavior demonstrated by a reversed biased diode allow it to be used as a capacitor. From Appendix A, it can be seen that by comparing charge storage abilities, a depletion mode transistor is superior to the enhancement mode transistor for this application.

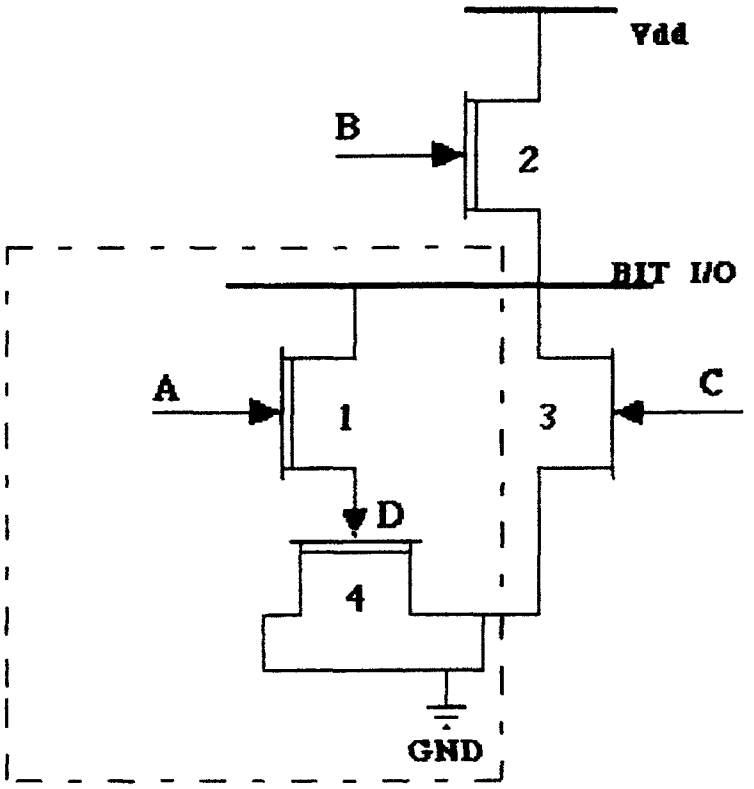


Figure 2. One-Transistor RAM Cell With A Diode

a. Write

To Write a ONE (high), pulse node B, which turns on transistor 2, and concurrently, pulse node A to turn on transistor 1. This opens a direct path from VDD through transistor 2 and transistor 1 to charge node D.

To Write a ZERO (low), pulse node C, which turns on transistor 3, and concurrently, pulse node A to turn on transistor 1. This opens a direct path from GND through transistor 3 and transistor 1 to discharge node D.

b. Read

To Read this cell, it is a simple matter of ensuring that the pullup (transistor 2) and pulldown (transistor 3) transistors are off and that the BIO line is either discharged or at a low potential, then pulse A to turn on transistor 1. This is where the Three-Transistor Model differs drastically from the One-Transistor Model. The Three-Transistor Model must have a way to deal with the inverted output and must have an elaborate plan for Refresh. The One-Transistor Model must use a sensing amplifier or a differential amplifier to be able to determine whether a ONE or a ZERO is read. Unlike the Three-Transistor Model, there is no direct path to ground to drag the BIO line to zero. A ZERO is Read by a slight drop in the potential of the BIO line. A ONE is Read by a slight rise in the potential of the BIO line. The whole BIO line does not have to be charged or discharged, the potential only has to increase or decrease enough for the sense amp to sense the change. As will be seen, refresh of the One-Transistor Model is accomplished by a Read and there is no need for extra circuitry. This makes refresh much easier for this circuit.

3. One-Transistor RAM Cell with a Capacitor

The One-Transistor RAM Cell with a capacitor is exactly the same as the One-Transistor RAM Cell with a diode, except that one uses a diode to store charge and the other uses a capacitor. This can be seen in Figure 3. The operations of Read and Write are exactly the same as described above for the case with a diode. In fact, all the operations are exactly the same.

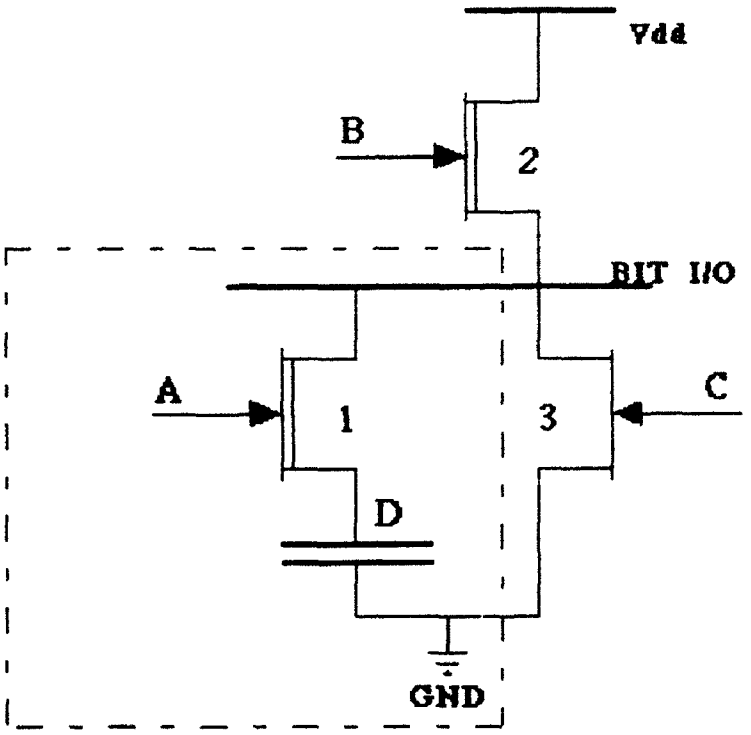


Figure 3. One-Transistor RAM Cell With A Capacitor

B. CHARGE STORAGE

There are many factors that go into the decision to use one model over another for a specific application. For this application, a prime factor is the charge storage ability, or charge maintenance. In Si, this is not as major a factor because Si does not suffer the large leakage currents that GaAs does. These leakage currents are, for most applications, secondary effects. The major simulation software packages available, namely VSPICE (Vitesse SPICE) and SPICE3, do not include these secondary effects. Testing these dynamic circuits with packages such as these tend to give one a false sense of security because these secondary effects are of major importance to these circuits. One simulation

package that does include all secondary effects and is considered the best simulation package available is HSPICE. The secondary effects that are of greatest concern are subthreshold current and substrate leakage current. Subthreshold current is the residual leakage current that flows from source to drain when V_{GS} is biased more negatively than V_T Substrate leakage current is leakage through the substrate which occurs due to injection of charge from a forward biased contact. A further discussion of these two effects can be found in the book by Long (Ref. 2).

1. Three-Transistor RAM Cell

As stated earlier, charge is stored on the gate of a transistor in the Three-Transistor Model. The circuit of Figure 1 was entered into HSPICE. The cell was written with a high potential and then left to discharge at will. Appendix A presents all the charge comparisons and calculations for the three models. The result is that this method fails miserably when compared to the other two methods. It seems a bit strange that the charge would fall off much faster for this case than for the diode case. There are three possible causes for this. The first is that the transistor is a depletion type instead of the enhancement type used by the diode. This does not fully explain the effect. In Figure A1, there is a direct comparison between an enhancement diode and a depletion diode and the difference is not great enough to account for the extremely large disagreement between the two models. The second possible cause is that HSPICE uses two different models for the two cases. The HSPICE documentation mentions some differences between the two models. It could just be that, for the application, the leakages in the transistor model are magnified when they are at a minimum for the diode model. The last possible cause is that the gate storage relies on a forward biased junction and the diode relies on a reversed biased junction. This is the most probable cause of the large differences.

2. One-Transistor RAM Cell with a Diode and Capacitor

The in-depth charge comparison and graphs are in Appendix A. The results show that the charge storage ability of the diode is very similar to that of the capacitor. Unlike

the capacitor, whose behavior is very simple and straightforward, the behavior of the diode changes drastically with transistor size and model. When research commenced on this project, HSPICE was not available. VSPICE and SPICE3 were used as tools to help make an educated guess as to which method of charge storage, diode or capacitor, to pursue. As stated earlier, these tools did not include the modeling of second order effects, so it was decided to take the more conservative approach and use the capacitor model as its abilities and characteristics were much better known. Looking at Appendix A, an argument can be made for using either one of the methods. The narrower gate-length on the diode enables the charge to rise faster and go higher than the capacitor, but the charge also dissipates faster. The larger gate lengths do not dissipate charge as fast, but they do not get charged as high. There is a point where the diode is actually a better choice than the capacitor, but this was not known when the decision was made to use a parallel plate capacitor. As will be seen, the charge maintenance of this capacitor in the finished circuit is fairly good. If the curves in Appendix A are extrapolated, it can be seen that both the capacitor and the diode converge on the same point. The next section will explore the operation of the One-Transistor model and some other differences between the use of a diode and a capacitor.

III. ONE-TRANSISTOR DYNAMIC RANDOM ACCESS MEMORY

A. DEVELOPEMENT

The development of a One-Transistor Memory array originated in VSPICE with SPICE3 being used when convergence problems prohibited the use of VSPICE. The basic functioning was fully tested in SPICE3. After the decision was made to use a One-Transistor RAM Cell with a capacitor, an appropriate method to sense the BIO line was needed. It was easy to decide that some sort of differential amplifier was needed, and that it had to be very sensitive. A few preliminary designs were done with little success before the final version was found [Ref.3]. The discussion of the sense amplifier can be found under **B. SENSE AMPLIFIER.** Once the sense amplifier was chosen, it was possible to design and simulate the basic circuit. This started the long iterative process of finding the best size transistors and capacitors to optimize circuit performance. It is interesting to note how small differences in transistor size can make a big difference to the overall functioning of the circuit. Referring to Figure 4, the first transistor that was sized was the read/write transistor. This had to be sized to give maximum potential transfer from the BIO line to the capacitor and back from the capacitor to the BIO line. This was not a task that could be done without considering the size of the pullup transistor. Everything has an influence over everything else and it was not easy to find the right combinations of transistor sizes and capacitors to optimize overall performance. The design called for the circuit to be fast enough to be competitive with what is currently available, but not too fast so the size of the array would not be a problem as far as expense of fabrication.

B. SENSE AMPLIFIER

The sense amplifier that was used was borrowed from a One-Transistor Memory application that used Si n-channel metal oxide semiconductor (NMOS) technology and enhancement-depletion mode transistors. It used five transistors and can be seen in Figure 4. The sense amplifier is the heart of any design using one-transistor memory cells because

of the need for something that is very sensitive to a change or mismatch on the BIO lines. It must also be able to quickly pull the BIO line high or low depending on what was sensed.

1. Operation

The operation of the sense amplifier determines how the entire memory array will operate. Referring to Figure 4, the basic operation of the sense amplifier is discussed. On the first half of a clock cycle, the equalization transistor (transistor 5) comes on to equalize the potentials of the two symmetric BIO lines. With the BIO lines equalized, a memory cell on one side of the sense amplifier and a dummy cell on the opposite side are turned on. This

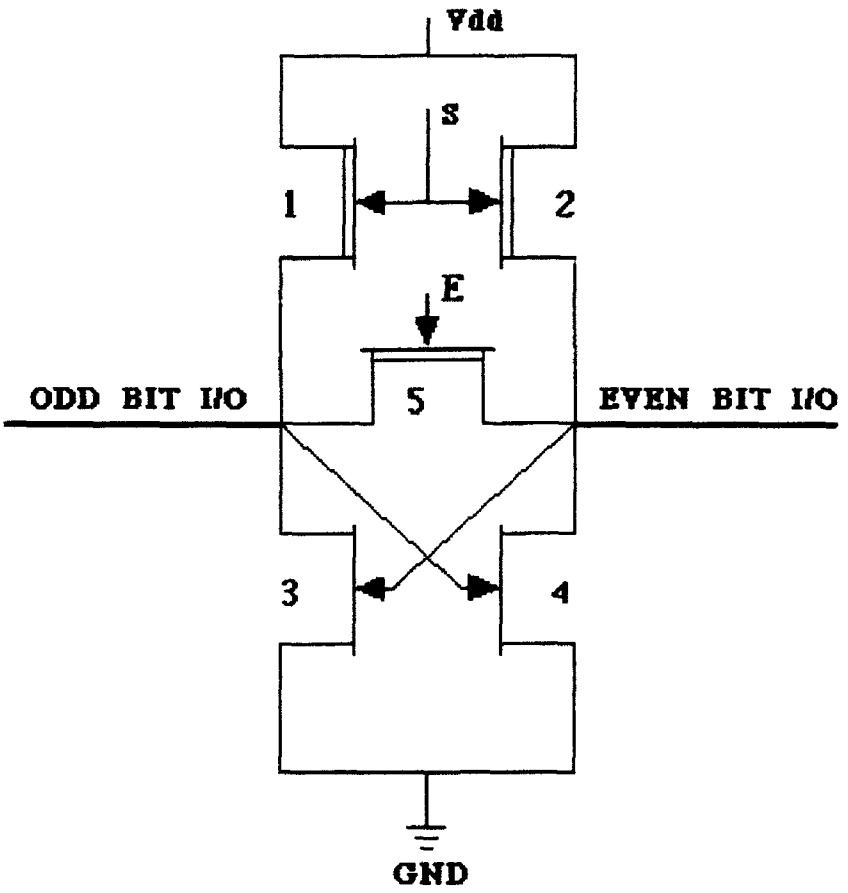


Figure 4. Sense Amplifier

unbalances the two BIO lines and the two sense transistors (transistors 1 and 2) come on and help the flip-flop action of the sense amplifier to pull the BIO lines in opposite directions. If a ONE had been stored in the memory cell, the potential would be higher on the memory cell side than on the dummy cell side and the BIO lines would be off balance in favor of the memory cell. The sense amplifier takes these unbalanced BIO lines and reinforces them by causing them to be pulled even farther in their high and low directions. The sense amplifier always causes one BIO line to go high and the other to compliment it by going low. Reading a ZERO on one side causes the BIO lines to behave exactly the same as if there was a ONE on the opposite side. This timing is very important and can be seen in Appendix B. Figure 5 gives a better view of the sense amplifier because it includes some of the memory cells and both of the dummy cells.

2. Timing

The timing of the Sense Amplifier is very straight forward and can be seen in Figure B1 and Figure B2. First the equalization pulse comes on and goes off. Then the cell read/write transistor and the opposite dummy transistor come on so that the BIO lines have a chance to be unbalanced before the sense transistors come on. This basic timing scheme is the same for a Read as well as a Write. The circuit will also work if the cell, dummy, and sense transistors come on at the same time. This though, does not allow the BIO lines to be unbalanced strictly by the stored charge, and may result in a fictitious Read should the sense amplifier and BIO lines not be symmetric. This adds a bit more to the complexity of the support circuitry because a two-phase non-overlapping clock must be generated, and one phase must also be delayed to turn on the sense transistors. To get a better feel for how this was done, refer to Michael A. Morris' thesis [Ref. 4] on GaAs DRAM support circuitry.

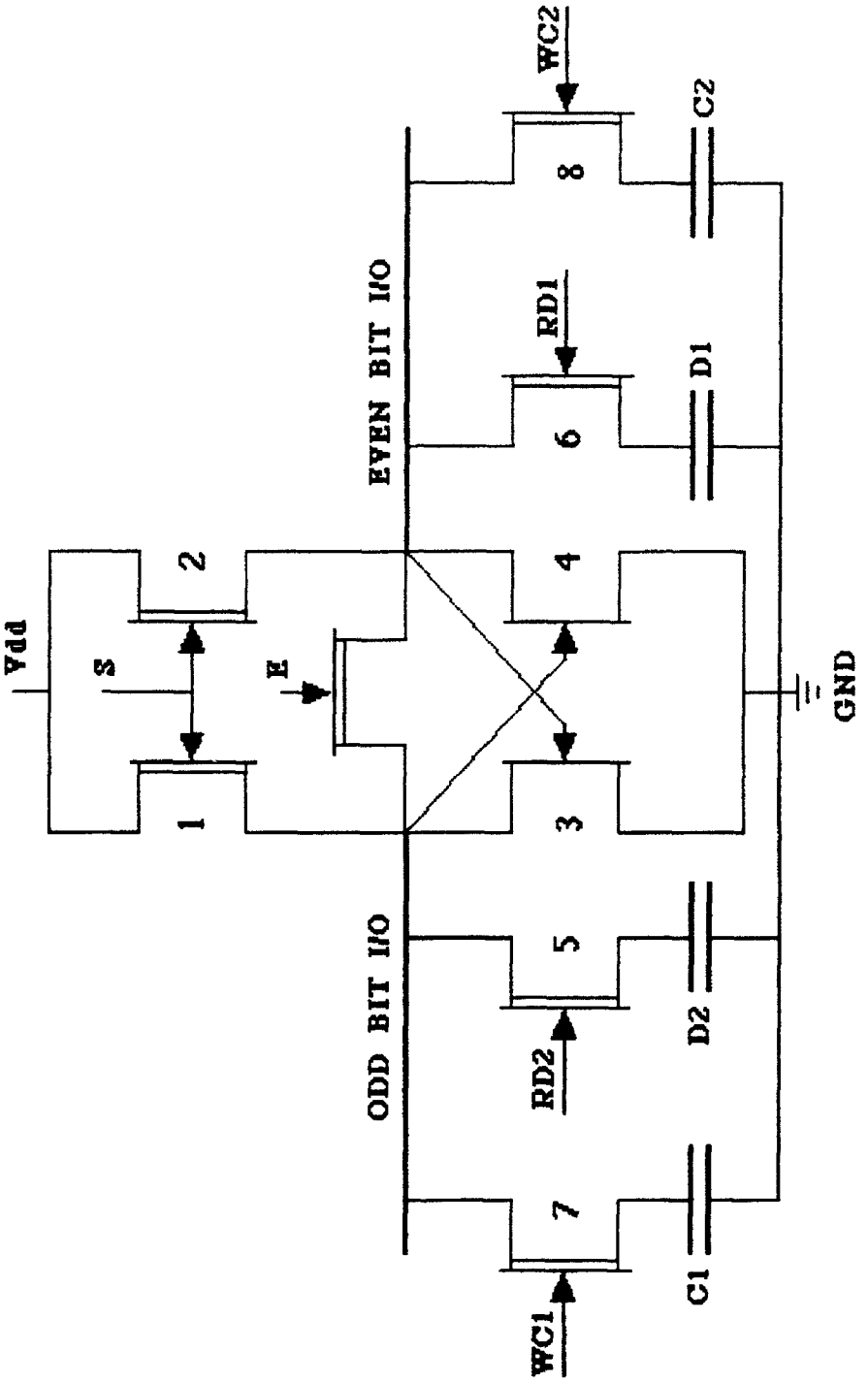


Figure 5. Sense Amplifier with Cells

3. Sensitivity

The sensitivity or robustness of the sense amplifier was tested using a spice file of the circuit of Figure 4. The driving force behind the tests performed is that during fabrication, transistor sizes and capacitance values may make the sense amplifier asymmetric. Also, temperature affects may play havoc with leakage currents and cause the whole project to fail.

(1) Change in Transistor Sizes. The following table, Table 1, presents the changes in the transistor sizes that were performed as well as the effect the change had on the ability of the sense amplifier to sense the proper value. This test was accomplished using the HSPICE initial conditions (.IC) line in the spice file, then doing a short run to see how the sense amplifier responded. Table 1 also shows the effect temperature has on the sense amplifier, the cooler temperature (23.0 deg C) is a little more forgiving than the higher (85.0 deg C) temperature. As the temperature increases, the circuit gets less and less tolerant to asymmetry.

TABLE 1
SENSE AMPLIFIER SENSITIVITY (TRANSISTOR SIZES)

SIZE TRAN 1	SIZE TRAN 2	SIZE TRAN 3	SIZE TRAN 4	INITIAL VOLT EVEN (mV)	INITIAL VOLT ODD (mV)	TEMP (deg C)	SENSE AMP PASS/ FAIL
9	9	210	210	0.499	0.500	85.0	PASS
9	8	210	210	0.500	0.494	85.0	PASS
9	8	210	210	0.500	0.495	85.0	FAIL
10	8	210	210	0.500	0.489	85.0	PASS
10	8	210	210	0.500	0.490	85.0	FAIL
11	8	210	210	0.500	0.484	85.0	PASS
11	8	210	210	0.500	0.485	85.0	FAIL
12	8	210	210	0.500	0.478	85.0	PASS

TABLE 1
SENSE AMPLIFIER SENSITIVITY (TRANSISTOR SIZES)

SIZE TRAN 1	SIZE TRAN 2	SIZE TRAN 3	SIZE TRAN 4	INITIAL VOLT EVEN (mV)	INITIAL VOLT ODD (mV)	TEMP (deg C)	SENSE AMP PASS/ FAIL
12	8	210	210	0.500	0.479	85.0	FAIL
9	8	210	210	0.500	0.495	23.0	PASS
9	8	210	210	0.500	0.496	23.0	FAIL
10	8	210	210	0.500	0.491	23.0	PASS
10	8	210	210	0.500	0.492	23.0	FAIL
11	8	210	210	0.500	0.487	23.0	PASS
11	8	210	210	0.500	0.488	23.0	FAIL
9	9	220	210	0.492	0.500	85.0	PASS
9	9	220	210	0.493	0.500	85.0	FAIL
9	9	220	210	0.493	0.500	23.0	PASS
9	9	220	210	0.494	0.500	23.0	FAIL

(2) Capacitance effects. The amount of capacitance that is felt by the sense amplifier on each of the BIO lines is also an important item to consider when discussing a symmetric circuit. If one side has more capacitance than another it can upset the balance and cause an erroneous result. This test was performed with two different capacitance values with the intent to find the capacitance mismatch that would cause an erroneous answer. Again, temperature plays an important part in how the sense amplifier will respond, so two different temperatures were used. It is very easy to see the spread of acceptable capacitance mismatch, and also very easy to see the effect of temperature.

TABLE 2
SENSE AMPLIFIER SENSITIVITY (CAPACITANCE MISMATCH)

EVEN BIT I/O CAPACIT. (FF)	ODD BIT I/O CAPACIT. (FF)	INITIAL VOLT EVEN (mV)	INITIAL VOLT ODD (mV)	TEMP (deg C)	SENSE AMP RESPONSE
550	650	0.500	0.490	85.0	PASSED
550	651	0.500	0.490	85.0	FAILED
550	672	0.500	0.490	23.0	PASSED
550	673	0.500	0.490	23.0	FAILED
1200	1364	0.500	0.490	85.0	PASSED
1200	1368	0.500	0.490	85.0	FAILED
1200	1402	0.500	0.490	23.0	PASSED
1200	1405	0.500	0.490	23.0	FAILED

(3) Speed. The speed of the sense amplifier is strictly dependent on the amount of capacitance on the BIO lines. Due to the configuration of the circuit, HSPICE will assign a capacitance value. As the circuit is made bigger, the amount of capacitance that is assigned to the BIO lines increases. This capacitance value is not dependent on the physical layout of the circuit, but is more a function of the physics of the devices that are in the circuit. With a large capacitance, it takes longer to charge or discharge the BIO lines. This can be overcome to a certain extent, by proper sizing of the transistors that make up the sense amplifier. This has a limit as a trade-off is reached between speed and size.

C. MEMORY ARRAY

1. Operation

Figure 6 shows the circuit diagram for the entire eight-address by one-bit memory array. With the aide of this figure, the operation of the array will be covered. Note the

symmetry in the diagram and that the sense amplifier is in the center with a dummy cell on each side. It is very important to maintain symmetry as discussed above under **B. SENSE AMP.**

The figures of Appendix B show the timing of the signals for a basic Read/Write operation. There are a few signals that are tied directly to the clock as can clearly be seen in Figure B1 and Figure B2. These signals happen every cycle and always perform the same function. The first group of signals are called Phase One signals and they include the Precharge signal and Equalization signal. Phase One signals all happen at the same time. The Precharge signal turns on the transistors to cause the precharging of the dummy cells and the precharging of the BIO lines. The Equalization signal causes the equalization transistor to turn on and it performs the duty that its name implies, it equalizes the potential on the two BIO lines. There is only one Phase Two signal that happens all the time and it is called the Sense signal. The Sense signal is a delayed version of the second phase of the clock, but it is still a Phase Two signal. This signal turns on the sense transistors in the sense amplifier.

a. Write

A Write starts out with the usual Phase One signals. It is followed directly be either a Pullup or Pulldown Phase Two signal. These signals turn on either the BIO line pullup or pulldown transistors. At the same time, the Phase Two signal, Read/Write, turns on the appropriate memory cell transistor. (The Read/Write signal also turns on the dummy cell on the opposite side of the memory cell, but this has no effect here.) This in effect Writes a ONE through the pullup transistor or Writes a ZERO through the pulldown transistor. Figure B3 shows two Writes to opposite side memory cells. The signals are labeled for easy identification. Note that the action of the sense transistors during a Write causes the BIO line on the side doing the Write to be pulled high, and the other BIO line to go low. In fact, the sense transistors always ensure that the two BIO lines are always opposite -- one high the other low. Figure B4 shows the same Write operation with the

addition of the plots of the actual charge stored. The cell charge follows the BIO line and when the Read/Write pulse is turned off the charge is stored on the capacitors. Figure B5 is a more expanded view of a Write of a ONE so that a better idea of the delays and rise times can be obtained. Figure B6 is a view of the waveforms for a Write of a ZERO. Note the Odd BIO Line gets dragged down and the cell charge follows, only to be stored as a very good low when the Read/Write pulse turns off. Note that the Even BIO Line goes high as expected, but that it is just as high as it would be on a Read of a ONE as in Figure B7. With this arrangement of complimentary BIO lines, it is possible and maybe even advantageous to only monitor one side. What is happening on the other side will still be known.

b. Read

A Read is done exactly the same as a Write with the exception that the Pullup or Pulldown signals do not occur. The Phase One signals happen as usual and then the Phase Two signal, Read/Write, turns on the appropriate memory cell and the opposite dummy cell. During the short pause before the Sense signal turns on, the BIO lines are being unbalanced by the memory cell on one side and the dummy cell on the other. When the Sense signal turns on the sense transistors, the BIO lines quickly go high and low depending on the preexisting unbalance. This is where the sensitivity of the sense amplifier comes into play. It needs to be able to function properly even with small differential voltages on the BIO lines. Figure B7 and Figure B8 demonstrate the Reading of a ONE and a ZERO respectively. Note the effect of the sense transistors as they pull the BIO lines high and low and replenish (refresh) the charge in the memory cells in the process.

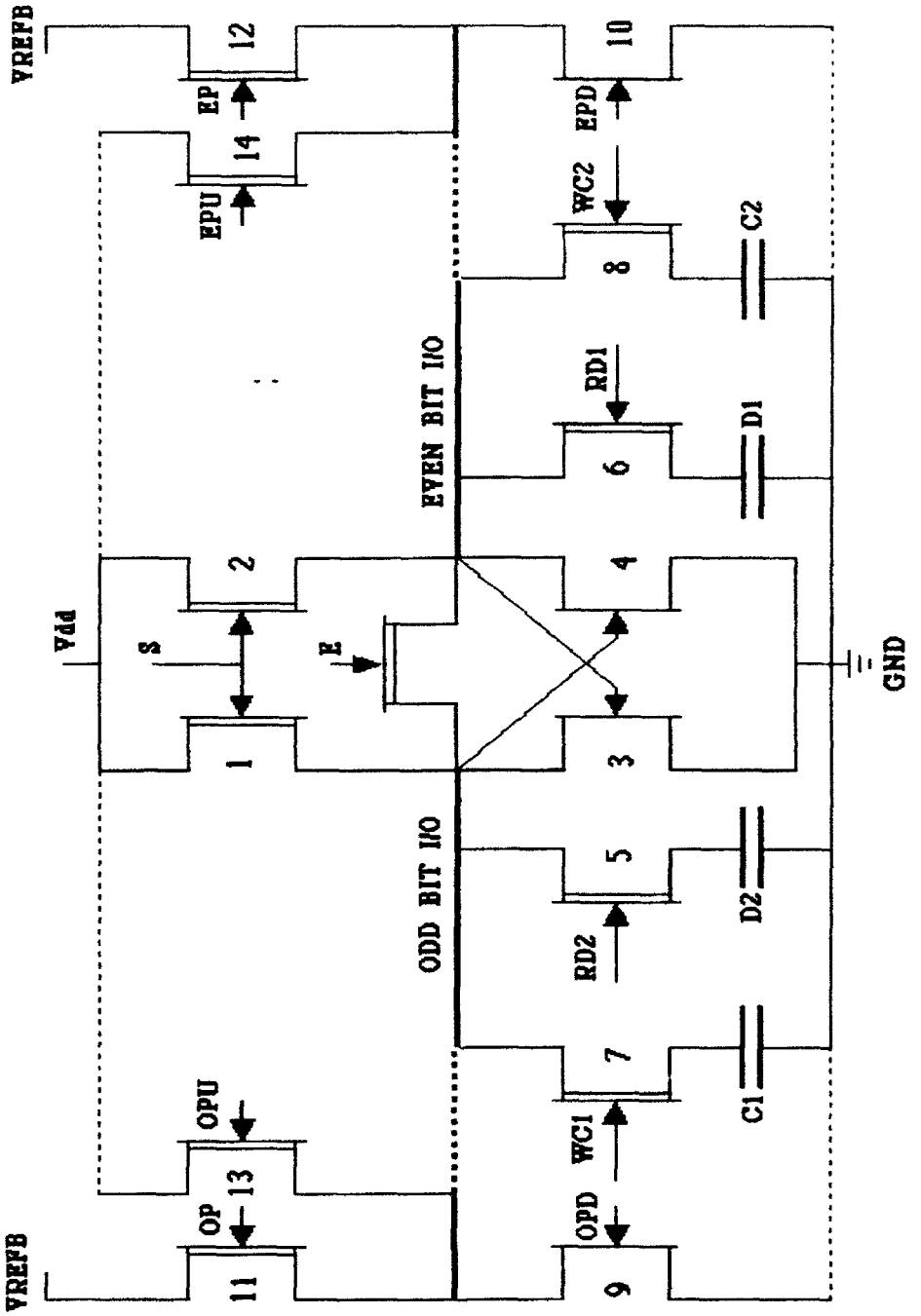


FIGURE 6. Sense Amplifier with Cells and Supporting Circuitry

c. *Refresh*

Any time that proper functioning depends on charge storage on an isolated node, as in the case of dynamic circuits, plans must be included for refresh. The stored charge will leak away and be gone forever unless refreshing is done at appropriate intervals. Refresh works in a One-Transistor Cell by simply doing a Read. When the sense amplifier is forcing the BIO lines to go high or low on a Read, the memory cell's read/write transistor is still on, and therefore the BIO lines as well as the cell's capacitor is being dragged high or low. Hence, the cell is refreshed by the act of Reading the cell. This is very convenient as it makes a refresh of all the cells a simple matter of counting through all the cells and performing a Read of each one. Looking at Read again, one can see that a one-bit by eight-address array would require eight clock cycles to perform a refresh. This is much easier and more straightforward than the Three-Transistor Model that has an inverted output.

How often a refresh must be done depends on the charge storage ability of the memory cell. A test was run on two memory cells of an array. One cell was a capacitor and one was a diode of a physical size equivalent to that of the capacitor. These cells were both written with a high, one at a time, and then left to see how long charge can be maintained on each of the two cells. To accomplish this long simulation using HSPICE, it was necessary to turn off all of the varying inputs that were not directly concerned with charge storage. The HSPICE file used for this simulation can be found in Appendix C with the resulting graph, Figure C1. At this point, it became necessary to find another way to run the simulation. It took HSPICE five days to run the simulation of Figure C1. This was due to the precharge and equalization pulse that was not turned off so that more realistic results could be obtained. To run the same simulation for ten milliseconds would be much too time consuming, especially when variations on the program would also be run. To allow HSPICE to run faster, the forever changing signal, Precharge would have to be secured. To do this required disconnecting the sense amplifier and then turning on a pullup transistor when the Writes were complete. The HSPICE file for this simulation can be found in Appendix C. The pullup transistor is tied to the desired precharge voltage level. A series of

graphs were generated for different precharge voltage levels, with the capacitor and three different diodes graphed for each level. The complete series of graphs, Figure C2 through Figure C12, were generated for the simple reason that the results were not as expected. Figure C1 shows the diode discharge rate to be slower than the capacitor, and Figure B3 shows a precharge of approximately 2.8 volts. Figure C2 through Figure C10 show that the capacitor discharge rate is far superior to the diode for any precharge greater than 2.0 volts. This apparent difference triggered the tedious job of trying to match Figure C1 with any precharge voltage. It can be seen that Figure C12, with a precharge of 1.7 volts, comes very close to Figure C1. The difference can be explained by understanding that the precharge transistors in the real circuit only turn on once every other half clock cycle. The other half of the time the BIO lines are at some other level. In fact, when charging time is taken into consideration, the BIO lines spend most of the time at some other level. The test circuit puts a precharge on the BIO lines and it stays there for eternity. Therefore, the effective precharge level is around 1.7 volts though the BIO line is actually pulled higher than that.

The series of figures in Appendix C does show the direct relation between precharge and charge storage ability. By looking at Figure C12, C12 more closely matches the circuit as designed, a refresh interval of approximately three milliseconds would be satisfactory. If the BIO lines could be consistently held at a higher effective level the refresh interval would be longer.

d. Write and Read Capacitor and Diode

With the same support circuitry, a diode was put in place of a capacitor on one side of the BIO line. This was done to get a comparison between the two as far as the Write and Read charge levels of the two different methods. It is interesting to see in Figure B9 that the capacitor initially charges to a higher value than the diode during the Write, but that during successive Reads following the initial Write the two charges become basically equal. The refreshing of charge during a Read is not as effective for the capacitor as it is for

the diode. This compounds the belief that the diode may actually be a better choice than the capacitor for charge storage in the memory array.

2. Minimize Leakage Effects

As mentioned earlier, leakage is a much more serious problem for GaAs than it is for Si. The second order effects that are of concern are subthreshold current and substrate leakage current. Subthreshold current is the residual leakage current that flows from source to drain for V_{GS} biased more negatively than V_T. Substrate leakage current is leakage through the substrate which occurs due to injection of charge from a forward biased contact. From further reading concerning these effects, it seems that the DRAM application is one in which these effects are not minor and definitely not secondary. There are two things that can help minimize their effects. The first is to precharge the BIO lines to some value that is almost equivalent to the charge on the dummy cell. This reduces the voltage across the read/write transistor and helps to minimize the leakage. The other method to minimize leakage is to use depletion type transistors and control them with a good solid 0 to -1.2 volt logic swing. The problems that these solutions raise are increased power consumption and the requirement for another power supply. The higher power consumption is a reflection of the power used to precharge the BIO lines. The requirement for another power supply is an outgrowth of the need to level shift signals to be able to use them to operate depletion type transistors. The 0 to 0.6 volt signals must be shifted to -1.2 to 0 volts, respectively.

To obtain a direct comparison between precharged BIO lines and non-precharged BIO lines, it was necessary to run the HSPICE file of Appendix C again. However, this time the precharge transistors are disconnected. The results can be found in Figure C13. Figure C13 rounds out the series on different precharge levels rather nicely, and the series is very good to demonstrate the effect precharge has on transistor leakage. Note the great change in the decay rates of the cell charges. The decay rate with no precharge will not support a

refresh interval of 0.1 milliseconds and the decay rate with higher precharge levels will support a refresh interval greater than 10 milliseconds.

3. Layout

The prime considerations in the layout of the memory cell, sense amplifier and Memory Array are the transistor sizes, the capacitor design, the power, or more precisely, the current requirements and capacitance considerations. Each one of these considerations has the ability to cause the project to fail. Therefore, each one will be addressed in turn. The layout was done using MAGIC, and can be seen in Figure 7. The total size for a 1 bit by 8 address array is 60,430 square micrometers.

a. Transistor Sizes

There are some basic limitations on the size of the transistors that can be reliably fabricated. There are also the requirements to have some large transistors in the circuit that are much larger than the basic limit. When this problem arises, it becomes necessary to make smaller transistors and put them in parallel. This causes the total number of transistors to increase, the current requirements to increase, and the capacitance effects to increase. These different problems can cause the size of the capacitors as well as the size of the transistors to change.

b. Capacitor Design

The design of the capacitors must be accomplished such that they are all approximately the same size and that they occupy the minimum amount of space. That is why a capacitor design of Figure A4 was chosen and the capacitance calculated with the nominal values of Table A1. Using the nominal values should not be a problem, because the sense amplifier is very forgiving in asymmetric capacitance loading.

c. Power /Current Requirements

The circuit was actually laid out twice. The first time it was laid out using the current measurements of the standard HSPICE file. Then, it was laid out again after getting

the current measurements from the simulation of the laid out circuit. The final measurements can be seen in Table 3. The current measurements are important because there are current limitations on the circuit imposed by the width and type of metal used. These limitations are presented in Table 4. These limitations are not important to HSPICE. In fact, the circuit can be laid out using the minimum widths, and still simulate satisfactorily. These limitations are only important to the fabrication of the circuit. When the circuit is fabricated, it is important to design the lengths of wire wide enough to be able to support the current that they will be required to pass without burning up and failing prematurely. The lengths of wire must also be wide enough to minimize the voltage drop along a wire and thus ensure the proper logic swing to maintain operation. Hence, the extra care taken in the layout of the circuit is both warranted and required.

The other aspect of current limitations/power limitations is the actual power drawn by the circuit. HSPICE will calculate this power and display it as a graph showing the instantaneous power used by the memory array. The total memory array power was calculated for three cases. The first case deals with the Write of a ONE to both sides followed by the Read of a ONE on both sides. This can be seen in Figure D1. The second case is the Write of a ONE to one side and the Write of a ZERO to the other followed by the Read of both sides. This graph can be seen in Figure D2. Figure D3 shows the last case and is a comparison between the capacitor cell and the diode cell. A ONE was written to both cells and then read. From these graphs it can be seen that the Read of a ONE or ZERO and the Write of a ZERO all use the same power whether it is a capacitor or a diode. The Write of a ONE to either a capacitor or a diode use the same higher power. With the thought of using more than one memory array in a larger system, it is nice that each array will only draw a maximum of 12.5 milli-watts. For an eight-bit word this equates to 0.1 watt.

TABLE 3
DRAM ARRAY CURRENT MEASUREMENTS

Array Input	Maximum Current @ 85 deg C
VDS	6.3 μA
BIO Line Reference Voltage	900 μA
Dummy Cell Reference Voltage	218 μA
Even Side Pulldown	19.4 μA
Even Side Pullup	60 μA
Odd Side Pulldown	128 μA
Odd Side Pullup	2.55 μA
Data Zero	180 μA
Data One	228 μA
Even Dummy Cell Control	227 μA
Odd Dummy Cell Control	228 μA
Sense Voltage	441 μA
Equalization Voltage	810 μA

TABLE 4
MAXIMUM CURRENT LIMITS FOR METAL LINES [REF.5]

Layer	Maximum Current @ 85 deg C
Gate Metal	5.0 mA/μm
Ohmic Metal	0.3 mA/μm
Metal 1	1.0 mA/μm
Metal 2	1.4 mA/μm
Metal 3	2.8 mA/μm

d. Capacitance Considerations

Anytime that a circuit is laid out, attention must be paid to the physical positioning of the items so as to minimize mutual capacitance between the lines. This is very important to the Memory Array. If the amount of capacitance on the BIO lines increase, the capacitance of the memory cells and dummy cells must likewise be increased. This increase results in larger capacitors and hence a larger array. It also results in larger transistors to pull up the BIO line and memory cell. This is a prime example of where every change that is made to the circuit can affect the functioning of the other components of the circuit, and hence cause the re-optimization of the circuit. The other consideration is that the circuit should be balanced. What is done to one side must also be done to the other so that the total capacitance effect is the same on both sides of the sense amplifier.

IV. CONCLUSIONS

To date, there has not been a documented instance of a working GaAs DRAM (utilizing standard GaAs fabrication techniques). This thesis presents an eight-address by one-bit DRAM array that was designed, simulated, laid out and tested using top of the line GaAs models and parameters from HSPICE for the Vitesse Semiconductor Corporation fabrication line. This DRAM array was then incorporated into a full blown eight-address by four-bit memory by Michael A. Morris [Ref. 4], also a student at the Naval Post Graduate School and also working with Dr. Douglas J. Fouts. This eight-address by four-bit memory is being fabricated by Vitesse Semiconductors and includes all of the supporting circuitry needed to validate this GaAs DRAM. The supporting thesis is forthcoming.

The results presented here are a product of the latest and most accurate simulation software available. Software that was specifically designed to closely approximate the circuits produced by Vitesse Semiconductor. The problems encountered by past attempts to produce a working DRAM mainly centered on the inability to store charge for any significant period of time. That is the reason so much time was spent comparing charge storage for different configurations. Before obtaining HSPICE, tests were run with SPICE3 by placing resistors in parallel with the read/write transistor to try to obtain a better feel for what the charge storage capabilities would be given the estimated worst case leakage conditions. Leakage currents of approximately 0.5 micro-Amps were still satisfactory. This was still an estimate though, and a more accurate test could not be performed without HSPICE. All of the tests performed with HSPICE on the circuit lead to the belief that the circuit will work very well. Even a margin of error of 50% would still give an acceptable refresh interval given that the clock is running at approximately 190 MHz and that a complete refresh takes eight clock cycles or about 0.4 nanoseconds. This clock rate is dependent more on the supporting circuitry than on the DRAM Array. To get the complete memory fabricated, size was a definite factor in that it determined the cost of fabrication.

Speed tests were not performed as speed was not a purpose of the research. The purpose of the research was only to develop a working GaAs DRAM for fabrication. The only goal on speed was that it be as least as fast as Si static memory. After the circuit is fabricated, it will be thoroughly tested and documented in a later thesis.

In order to meet deadlines for fabrication runs, a memory cell had to be decided upon and developed prior to obtaining HSPICE. After extensive testing with HSPICE, a better choice for the memory cell would have been a diode. The results presented here show that the diode decay curve has a flatter slope and that it can refresh to a higher level than the capacitor. These two factors alone are enough to choose the diode over the capacitor, but there is also the fact that a smaller diode could be used, thus making a smaller memory cell. One can see that there is a trade off between using a higher precharge and not using a higher precharge. A higher precharge will lead to a longer refresh interval. It will also raise the level below which a ONE will be read as a ZERO and thus make the refresh interval shorter. It is plain that the capacitor is the better candidate if a higher effective precharge is used. The diode is better at lower effective precharge levels. The bottom line for any application, is to simulate both, compare, and use the one that gives the best results.

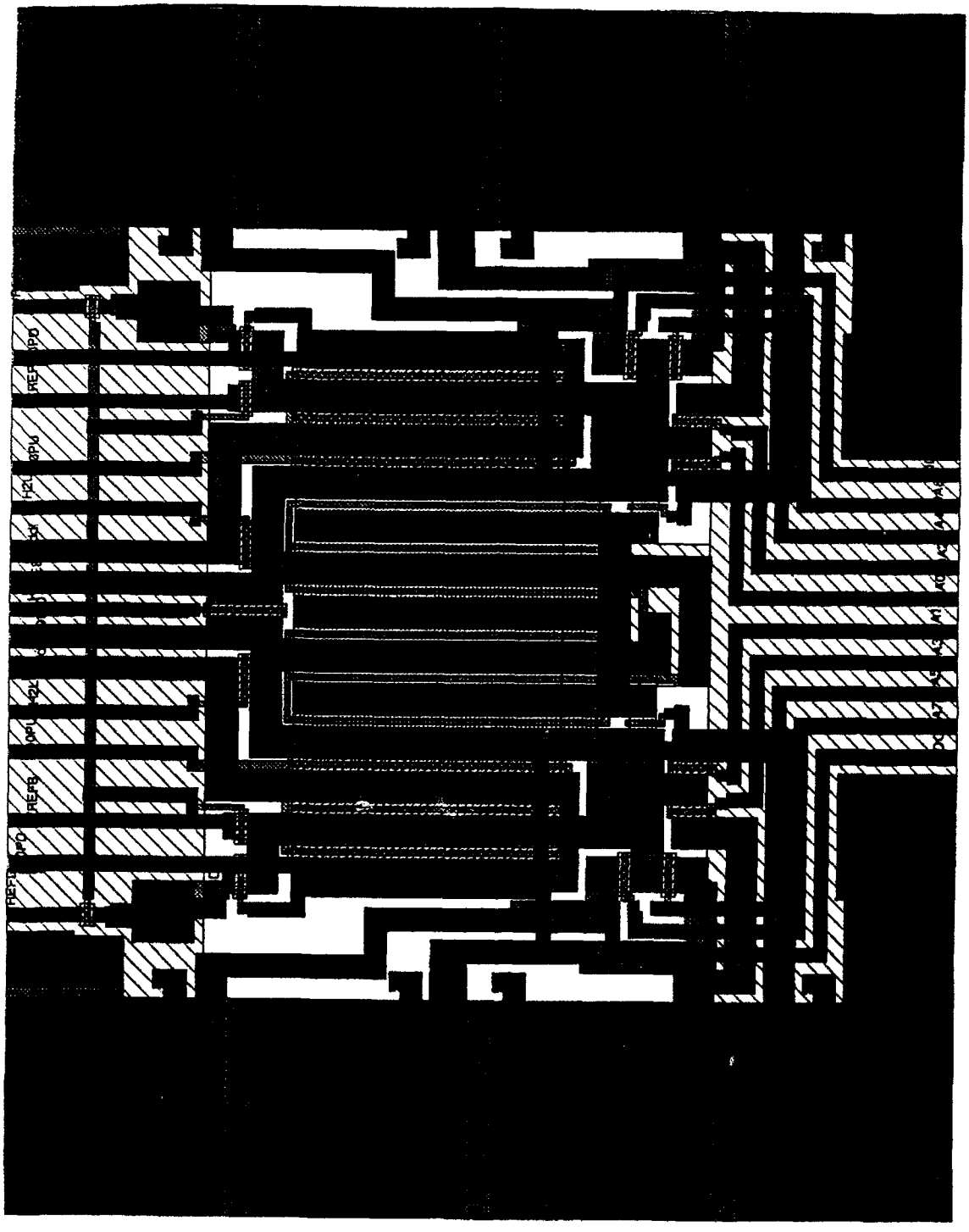


Figure 7. MAGIC Layout of Memory Array

APPENDIX A

CHARGE COMPARISONS FOR DIFFERENT

RAM CELL CONFIGURATIONS

I. RAM CELL CONFIGURATIONS

The three different RAM cell configurations are presented below. The first is called a Three-Transistor RAM cell because it uses three transistors to store a charge.The last two are One-Transistor RAM cells and only differ by the method of storing charge, one uses a reversed biased diode and the other a capacitor. To determine the best one of the three to use requires that a study of the charge maintenance of the three be performed and the results compared. The Three-Transistor cell stores charge at node D on the gate of a transistor. A Write of the cell is done with transistor CAD and a read is accomplished with transistor (BIT I/O)BE. This location for charge storage works very well with Silicon, but for GaAs it suffers much too much from leakage currents.

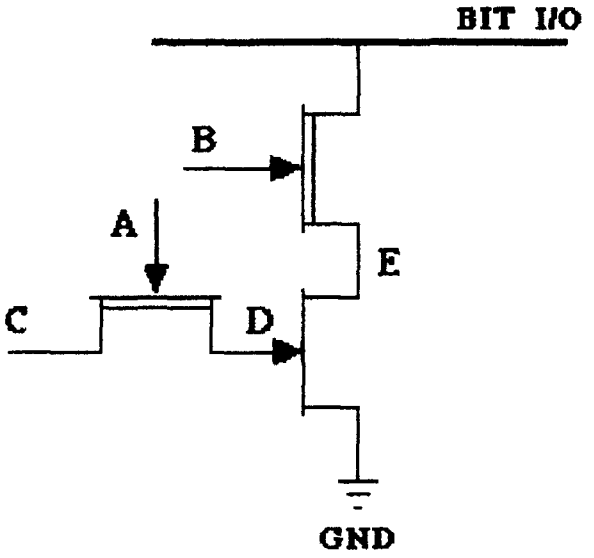


Figure A1. Three-Transistor RAM Cell

The remaining two configurations only differ by the charge storage device. The first uses a diode and the second uses a capacitor as can be seen in Figure A2 and Figure A3. The question is whether a reverse biased diode that occupies the same area as a capacitor can perform as well as a capacitor. The capacitor was made by utilizing four different layers of metal laid out as in Figure A4. The capacitance can be calculated by the use of the information in Table 1. Assuming a square capacitor, an equation can be written that can be solved for the size of a square with side L that will give the appropriate capacitance.

$$0.327 \times L^2 + 0.772 \times L = \text{Capacitance}$$

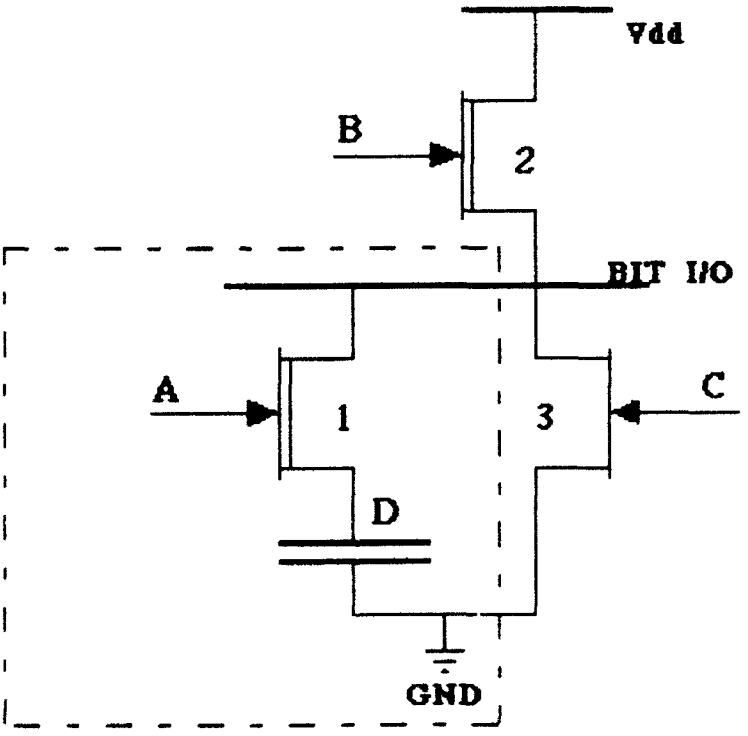


Figure A2. One-Transistor RAM Cell With Capacitor

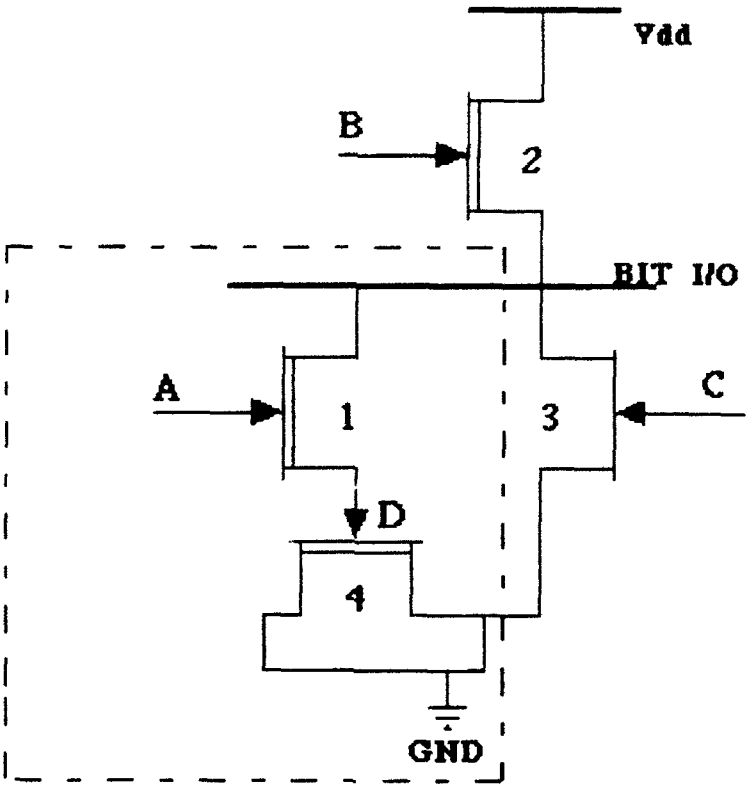


Figure A3. One-Transistor RAM Cell With Diode

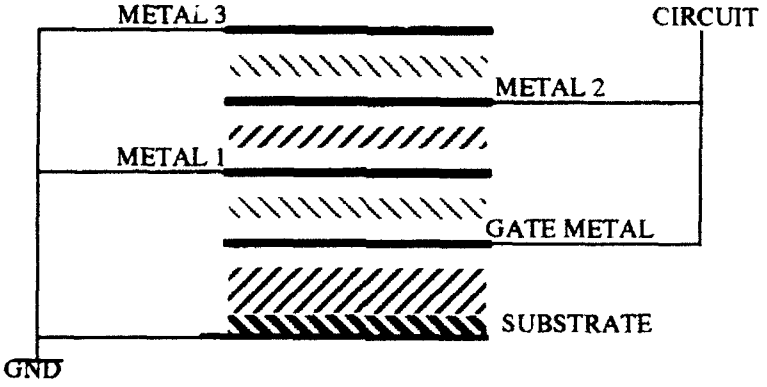


Figure A4. Capacitor Layout

TABLE A1
INTERLAYER CAPACITANCES [REF. 5]

Top Layer	Bottom Layer	Parallel Plate Capacitance ($fF/micron^2$)	Fringing Capacitance (fF/micron)
Metal 3	Metal 2	0.051	0.048
Metal 3	Metal1	0.033	0.035
Metal 3	Gate Metal	0.028	0.030
Metal 3	Ohmic Metal	0.028	0.030
Metal 3	Substrate	0.022	0.035
Metal 2	Metal1	0.073	0.049
Metal 2	Gate Metal	0.050	0.045
Metal 2	Ohmic Metal	0.050	0.045
Metal 2	Substrate	0.32	0.042
Metal1	Gate Metal	0.127	0.051
Metal1	Ohmic Metal	0.127	0.051
Metal1	Substrate	0.052	0.044
Gate Metal	Substrate	0.076	0.045

Once a capacitor value has been selected, the size of the diode can be calculated. Using minimum sizes as seen in Figure 5, the minimum width of the transistor can be found and the resulting length calculated. This can be done for the three standard gate lengths of 1.2 microns, 2.4 microns, and 3.0 microns. These sizes can also be used for the charge storage transistor in the Three-Transistor Model, though for this comparison only the 1.2 micron gate length was considered.

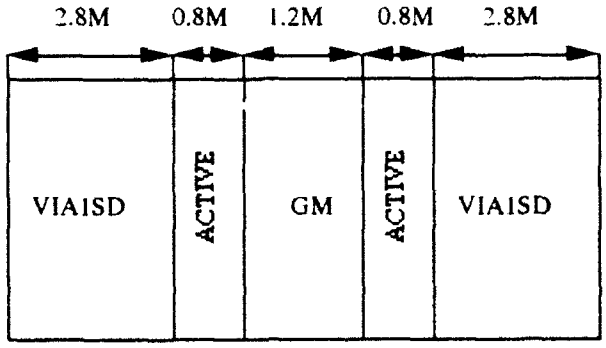


Figure A5. Minimum Size Transistor

II. CHARGE COMPARISONS

The charge comparisons were accomplished using a single spice file of the three circuits of Figures 1, 2, and 3. This HSPICE file follows this section. Three different capacitor sizes were considered, and for each size capacitor, three different sized diodes were tested. Again, the different sized diodes are derived from the different gate lengths of 1.2 Microns, 2.4 Microns, and 3.0 Microns. The following table, Table 2, lists the combinations of capacitors and transistor sizes. Referring to Figure 6 through Figure 16, the capacitor and the diode performed much better than the gate. Results show that the Gate charge storage in Three-Transistor Model is very poor. Comparison between the diode and the capacitor are a little harder. In each case, the diode with a 1.2 micron gate length was quicker to charge, but had an equally quick discharge. The capacitor performs better than the diode with gate length of 1.2 micron. In general, larger gate lengths charged q ·cker and discharged slower than the capacitor. It is interesting to note Figures 9 and 13, where the three different gate lengths are plotted together for each capacitance value. The larger the gate length the better the performance, or at least the slower the discharge. This comparison is taken one step farther in Figure 17. Here, gate lengths of 1.2, 1.5, 2.0, 2.4, 3.0, 4.0, and

5.0 are plotted against the capacitor in a very busy graph. It is easy to see the effect of varying gate length on the capacitance abilities. In Figure 18, the capacitor is plotted against a diode with a gate length of 1.8 microns. Notice how the two curves on this plot are almost exact. It is plain to see that a diode with the proper dimensions can perform better than a capacitor. This thesis though, chooses to use the One-Transistor Model with Capacitor for a few good reasons that are presented in the main body. Another interesting result that came out of this testing can be seen in Figure 6. Figure 6 shows a direct comparison between an enhancement mode diode and a depletion mode diode. The depletion mode diode is by far the better choice for use as a capacitor. The last point to make is the large discrepancy between the gate's storage ability and the diode. This can be caused by the different models used, but it is questionable that this large a discrepancy is truly realistic.

TABLE A2
CHARGE COMPARISONS

Capacitor	Gate Trans Length	Gate Trans Width	Diode Length	Diode Width	Figure Number
70 FF	1.2	21.7	1.2	21.7	6
70 FF	2.4	19.0	2.4	19.0	7
70 FF	3.0	17.9	3.0	17.9	8
150 FF	1.2	48.6	1.2	48.6	9
150 FF	2.4	42.5	2.4	42.5	10
150 FF	3.0	40.0	3.0	40.0	11
856.1 FF	1.2	297.6	1.2	297.6	12
856.1 FF	2.4	260.4	2.4	260.4	13
856.1 FF	3.0	245.1	3.0	245.1	14

III. CHARGE COMPARISON HSPICE FILE

Vitesse HGaAs3 Ram Cell Date: 17 November 1992

* include Vitesse HGaAs3 models and parameters for hspice.

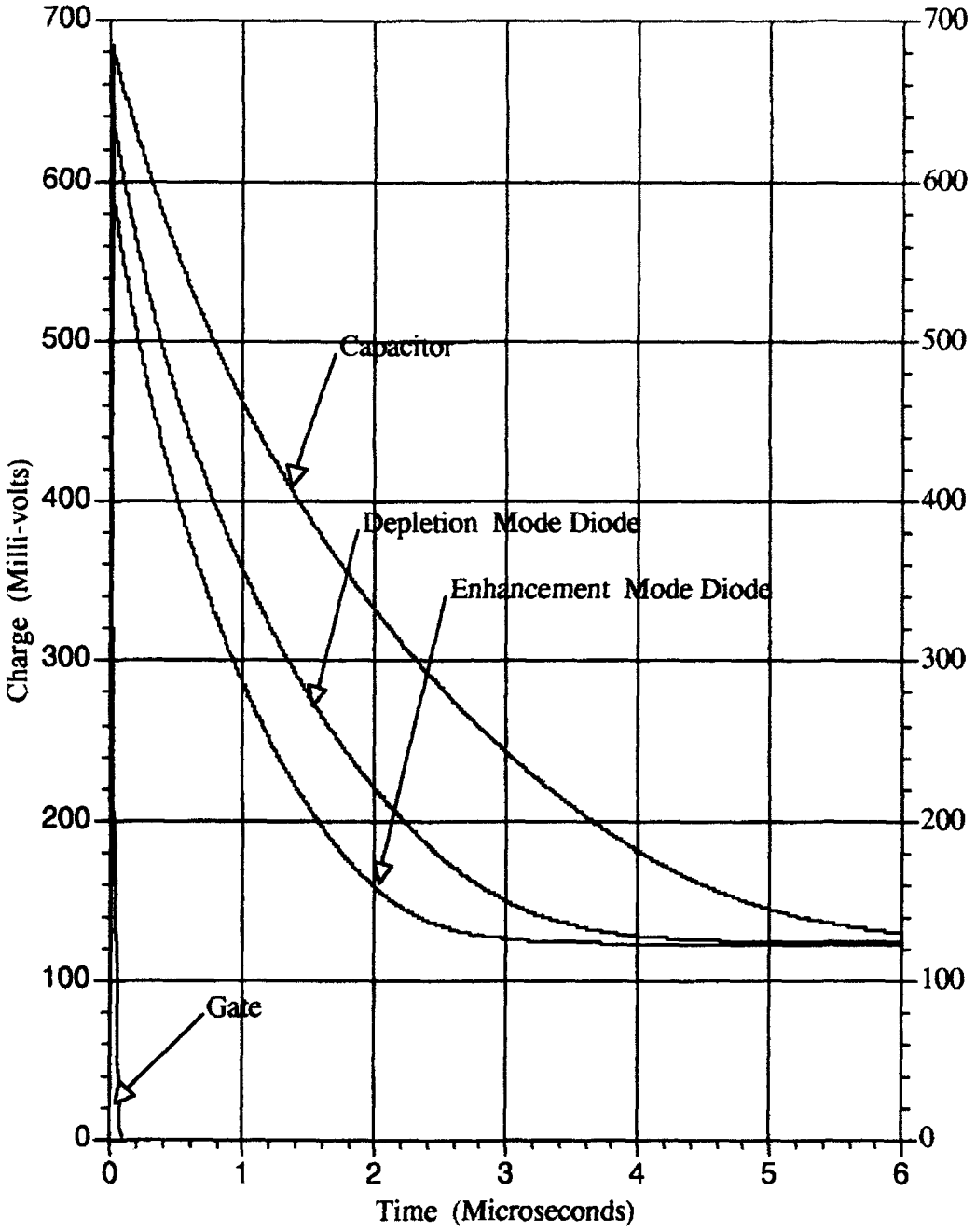
```
.protect
.include '/tools3/cad/meta/h9007/lib/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h9007/lib/vitesse/hgaas3.corners' tt
.unprotect

* power supply
vds 1 0 2.0

* Driving Control Signals

* Control signals for Three-Transistor Model.
* vh1 is the voltage level being written
vh1 3   0  PULSE(0.0  0.63 0PS 100PS 100PS 1100PS 10mS)
* vw1 is the pulse that does the writing
vw1 4   0  PULSE(-1.2 0 500PS 100PS 100PS 500PS 10mS)
* vr is the signal that does a read (no read done here)
vr  5   0  -1.2v

* Control signals for the One-Transistor Model with Diode
* vh2 is the Pullup signal that turns on the Pullup Transistor
vh2 12  0  PULSE(-1.2 0   0PS 100PS 100PS 1000PS 10mS)
* vw2 is the Read/Write pulse
vw2 9   0  PULSE(-1.2 0 500PS 100PS 100PS 500PS 10mS)
* vd1 is the Pull-down signal that turns on the Pull-down Transistor
vd1 13  0  PULSE(0 0.63 1000PS 100PS 100PS 400PS 10mS)

* Control signal for the One-Transistor Model with Capacitor
* vh3 is the Pullup signal that turns on the Pullup Transistor
vh3 15  0  PULSE(-1.2 0   0PS 100PS 100PS 1000PS 10mS)
* vw3 is the Read/Write pulse
vw3 14  0  PULSE(-1.2 0 500PS 100PS 100PS 500PS 10mS)
* vd is the Pull-down signal that turns on the Pull-down Transistor
vd  17  0  PULSE(0 0.63 1000PS 100PS 100PS 400PS 10mS)


* Three-Transistor Model -- Charge Storage transistor is as large as * the capacitor
j0   3   4   8   0   jfet16   l=1.2 w=8.0
j1   7   8   0   0   jfet10   l=3.0 w=245.1
j2   6   5   7   0   jfet16   l=1.2 w=8.0


* The following groups are all the One-Transistor Model with Diode.
```

```
* Each group uses a different diode gate length -- but all diodes
* are the same size as the capacitor.
j3    10   9    11   0    jfet16   l=1.2 w=8.0
j4    11   0    1    0    dio16    l=1.2 w=297.6
j5    1    12   10   0    jfet16   l=1.2 w=150.0
j6    10   13   0    0    jfet04   l=1.2 w=150.0


j13   7    109  711  0    jfet16   l=1.2 w=8.0
j14   711  0    711  0    dio19    l=1.8 w=277.8
j15   1    12   710  0    jfet16   l=1.2 w=150.0
j16   710  13   0    0    jfet04   l=1.2 w=150.0


j53   610  9    611  0    jfet16   l=1.2 w=8.0
j54   611  0    611  0    dio16    l=1.5 w=287.4
j55   1    12   610  0    jfet16   l=1.2 w=150.0
j56   610  13   0    0    jfet04   l=1.2 w=150.0


j63   510  9    511  0    jfet16   l=1.2 w=8.0
j64   511  0    511  0    dio19    l=2.0 w=271.7
j65   1    12   510  0    jfet16   l=1.2 w=150.0
j66   510  13   0    0    jfet04   l=1.2 w=150.0

j73   110  9    111  0    jfet16   l=1.2 w=8.0
j74   111  0    111  0    dio19    l=2.4 w=260.4
j75   1    12   110  0    jfet16   l=1.2 w=150.0
j76   110  13   0    0    jfet04   l=1.2 w=150.0

j23   210  9    211  0    jfet16   l=1.2 w=8.0
j24   211  0    211  0    dio20    l=3.0 w=245.1
j25   1    12   210  0    jfet16   l=1.2 w=150.0
j26   210  13   0    0    jfet04   l=1.2 w=150.0

j33   310  9    311  0    jfet16   l=1.2 w=8.0
j34   311  0    311  0    dio20    l=4.0 w=223.2
j35   1    12   310  0    jfet16   l=1.2 w=150.0
j36   310  13   0    0    jfet04   l=1.2 w=150.0

j43   410  9    411  0    jfet16   l=1.2 w=8.0
j44   411  0    411  0    dio20    l=5.0 w=204.9
j45   1    12   410  0    jfet16   l=1.2 w=150.0
```

```
j46   410  13   0    0    jfet04   l=1.2 w=150.0

* This is the One-Transistor Model with Capacitor
j7    16   14   18   0    jfet16   l=1.2 w=8.0
j8    1    15   16   0    jfet16   l=1.2 w=150.0
j10   16   17   0    0    jfet04   l=1.2 w=150.0

* c0 is the memory cell capacitor
c0    18   0    856FF
* the other capacitors are BIO Line capacitors that simulate the
* actual capacitance on the BIO Line
c1    16   0    1000FF
c2    6    0    1000FF
c3    10   0    1000FF
c4    110  0    1000FF
c5    210  0    1000FF
c6    310  0    1000FF
c7    410  0    1000FF
c8    510  0    1000FF
c9    610  0    1000FF
c10   710  0    1000FF

* This is the Temperature Flag that sets the simulation temperature
* to 85 degrees centigrade.
.temp 85.0
* The .probe command ensures that only the listed signals are saved
* for evaluation
.probe v(8) v(11) v(111) v(211) v(311) v(411) v(511) v(611) v(711) v(18)
* The .print command prints the signals listed to the .lis file
.print v(8) v(11) v(111) v(211) v(311) v(411) v(511) v(611) v(711) v(18)
* The .tran command tells the simulation to run for 100000 nano-
* seconds and to save data every 50000 picoseconds
.tran 50000PS 100000n
* The following line sets up the options and parameters to run.
.options scale=1E-06 post captab gmindc=1E-11 probe
.end
```

IV. HSPICE SIMULATION GRAPHS

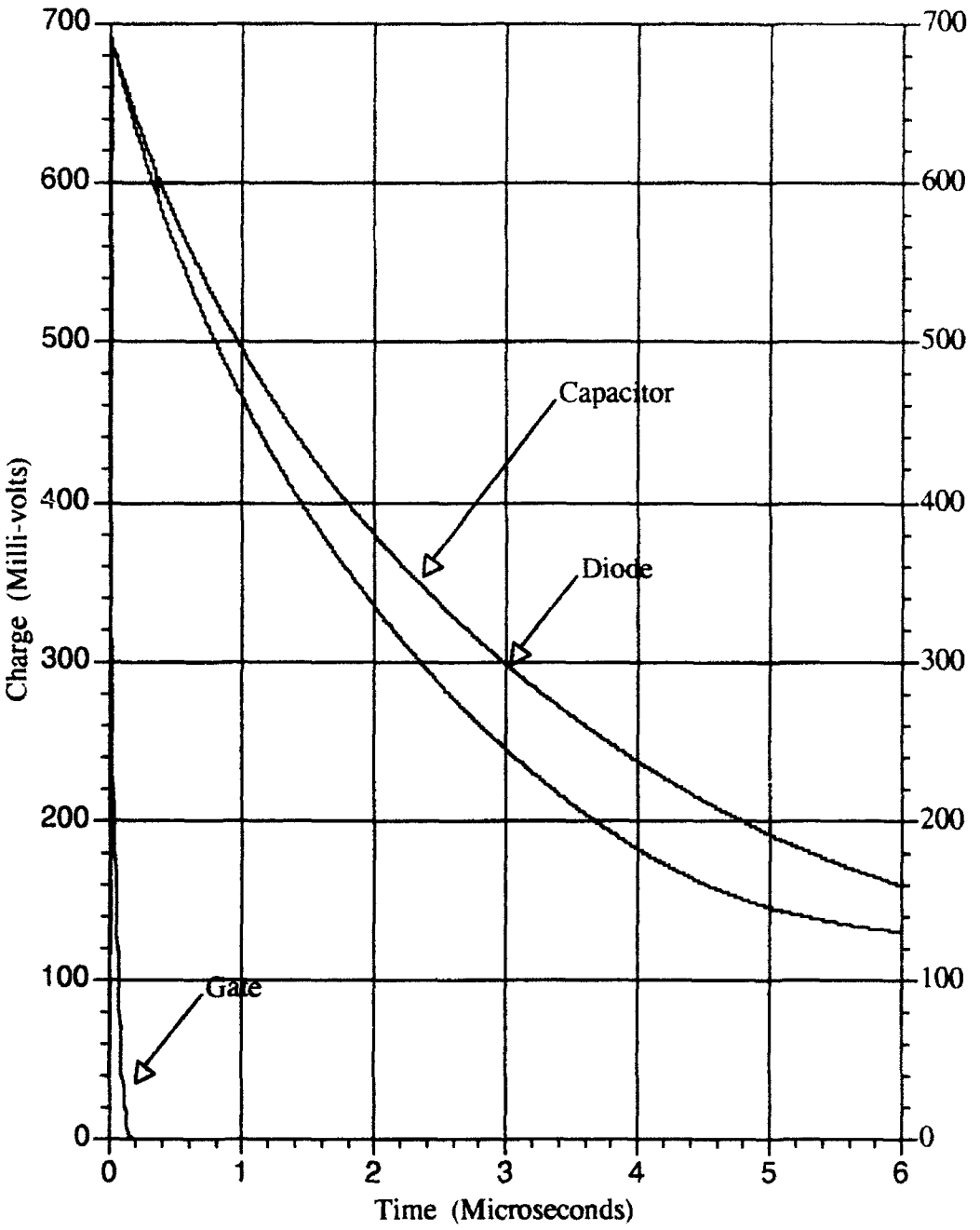
The following graphs are the results of the simulation program HSPICE.



Charge Comparisons

70 FF Capacitor -- 1.2 Micron Transistor Length

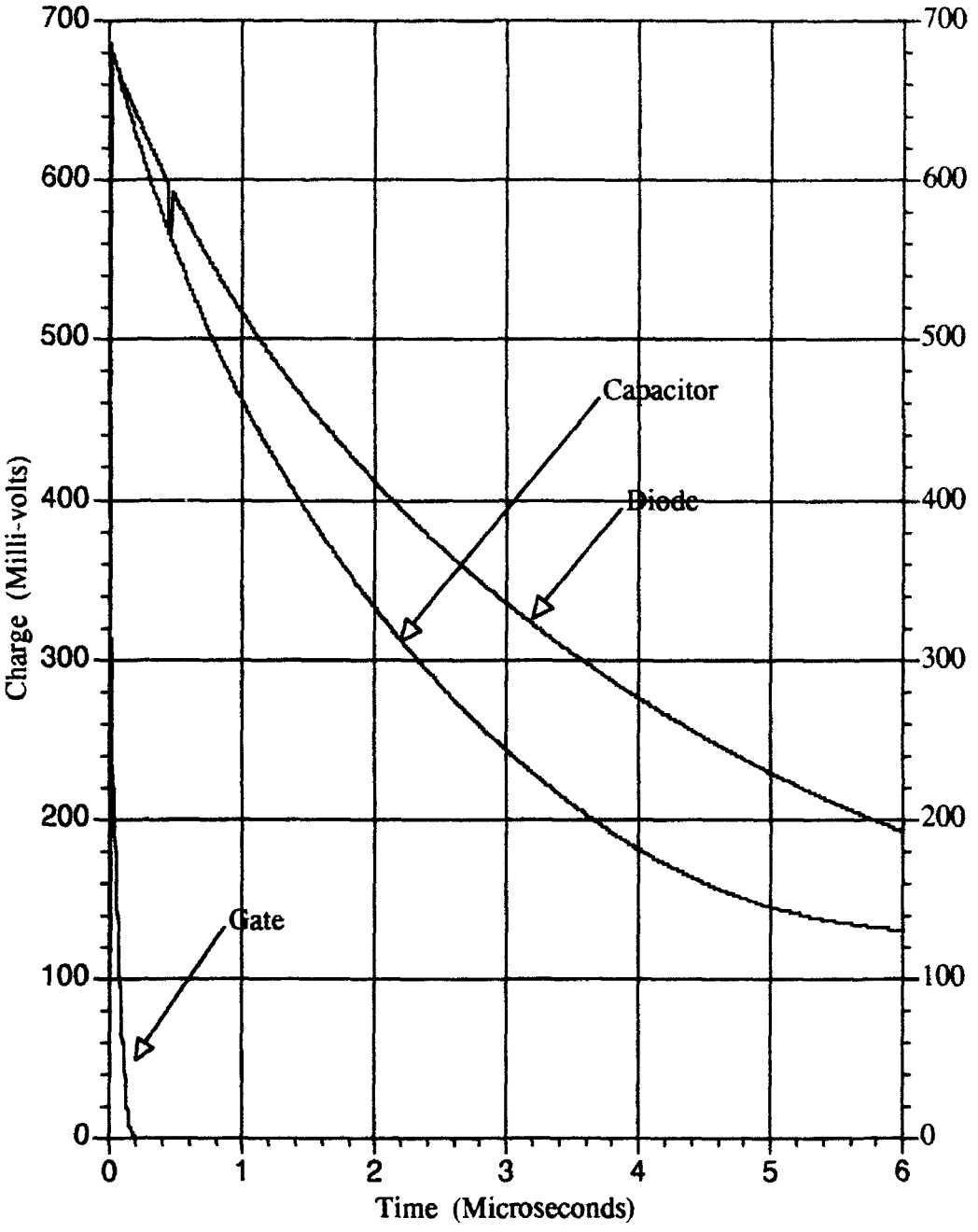
Figure A6



Charge Comparisons

70 FF capacitor -- 2.4 Micron Transistor Length

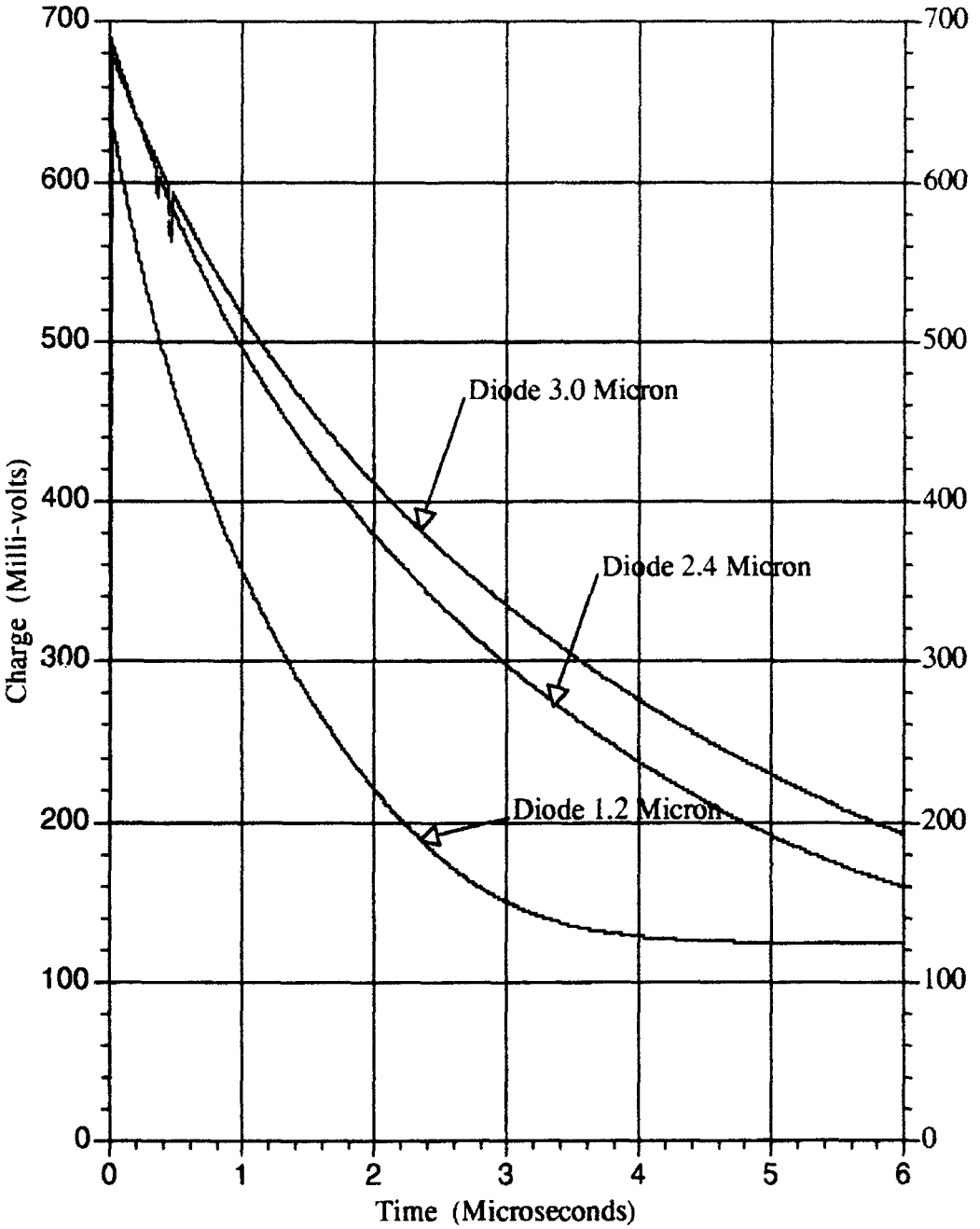
Figure A7



Charge Comparisons

70 FF Capacitor -- 3.0 Micron Transistor Length

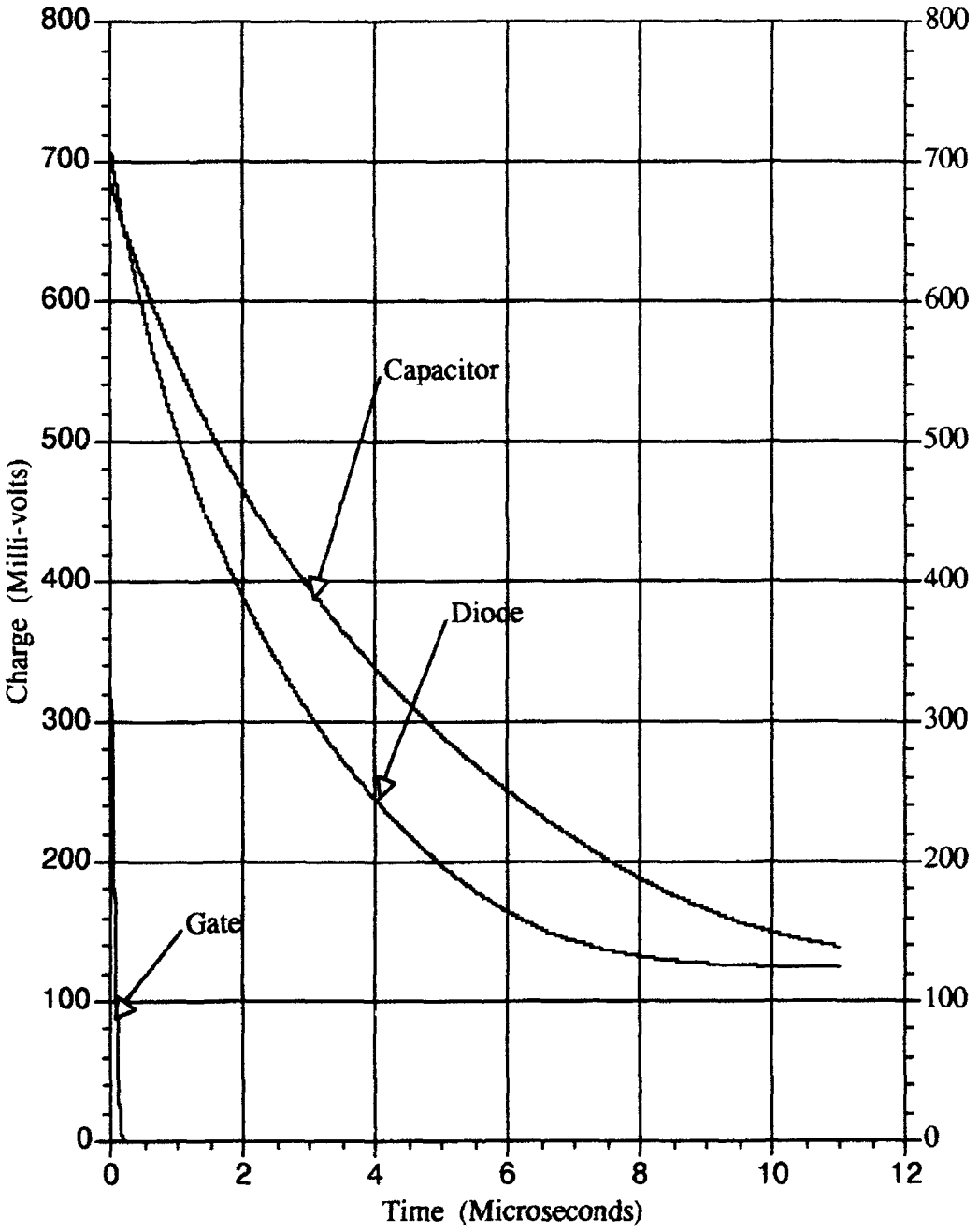
Figure A8



Charge Comparisons

70 FF Capacitor -- 1.2, 2.4 and 3.0 Micron Lengths

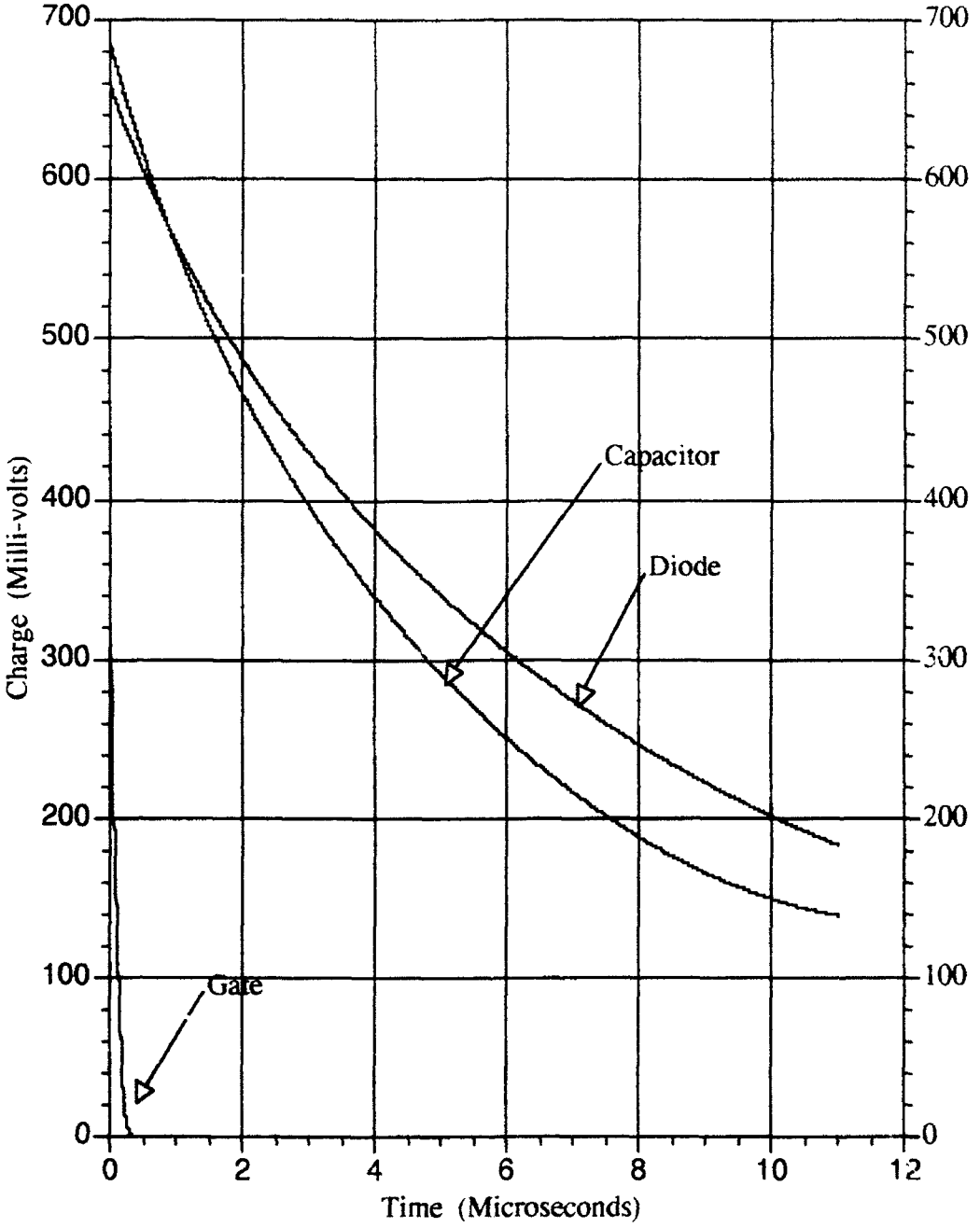
Figure A9



Charge Comparisons

150 FF Capacitor --- 1.2 Micron Transistor Length

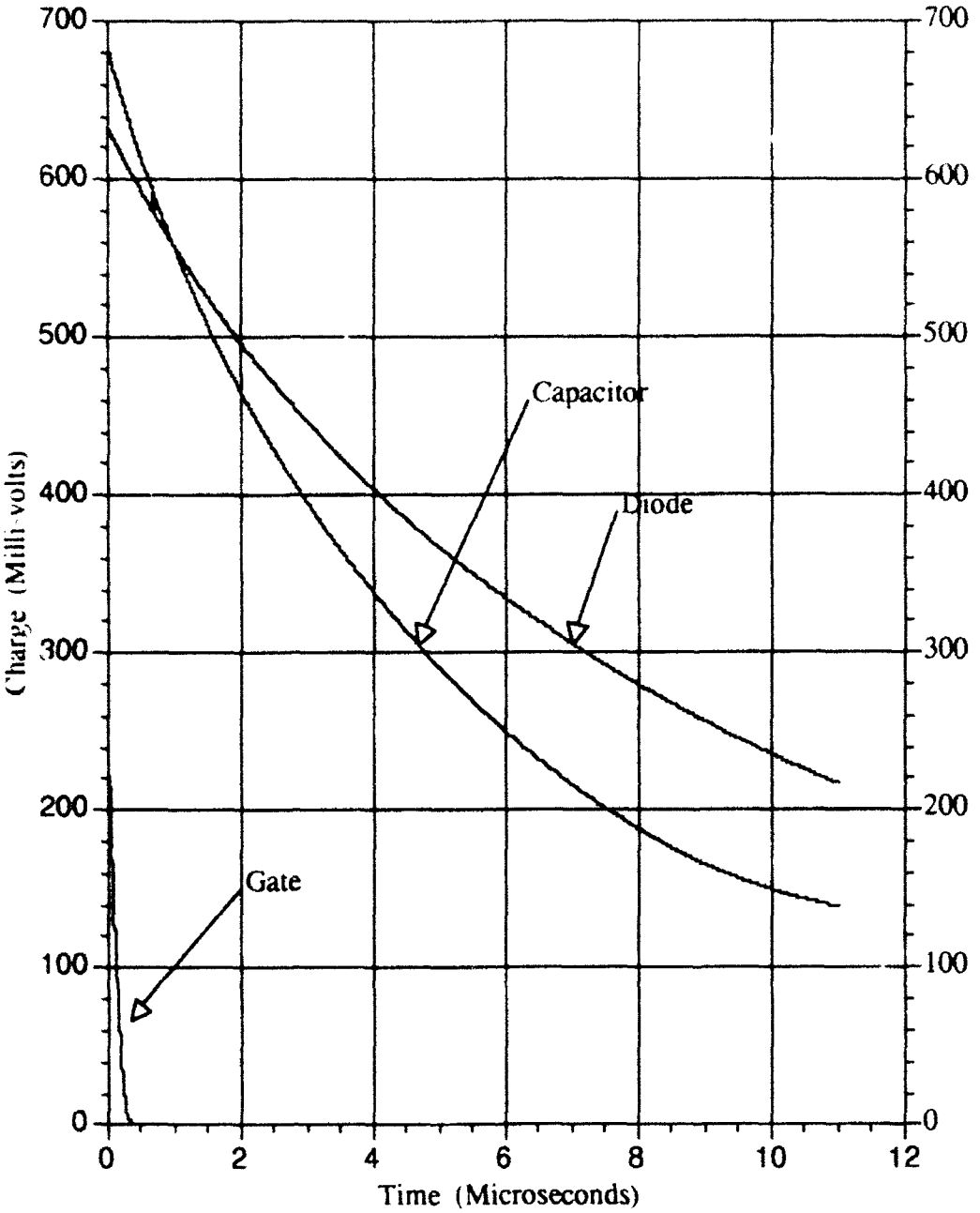
Figure A10



Charge Comparisons

150 FF Capacitor --- 2.4 Micron Transistor Length

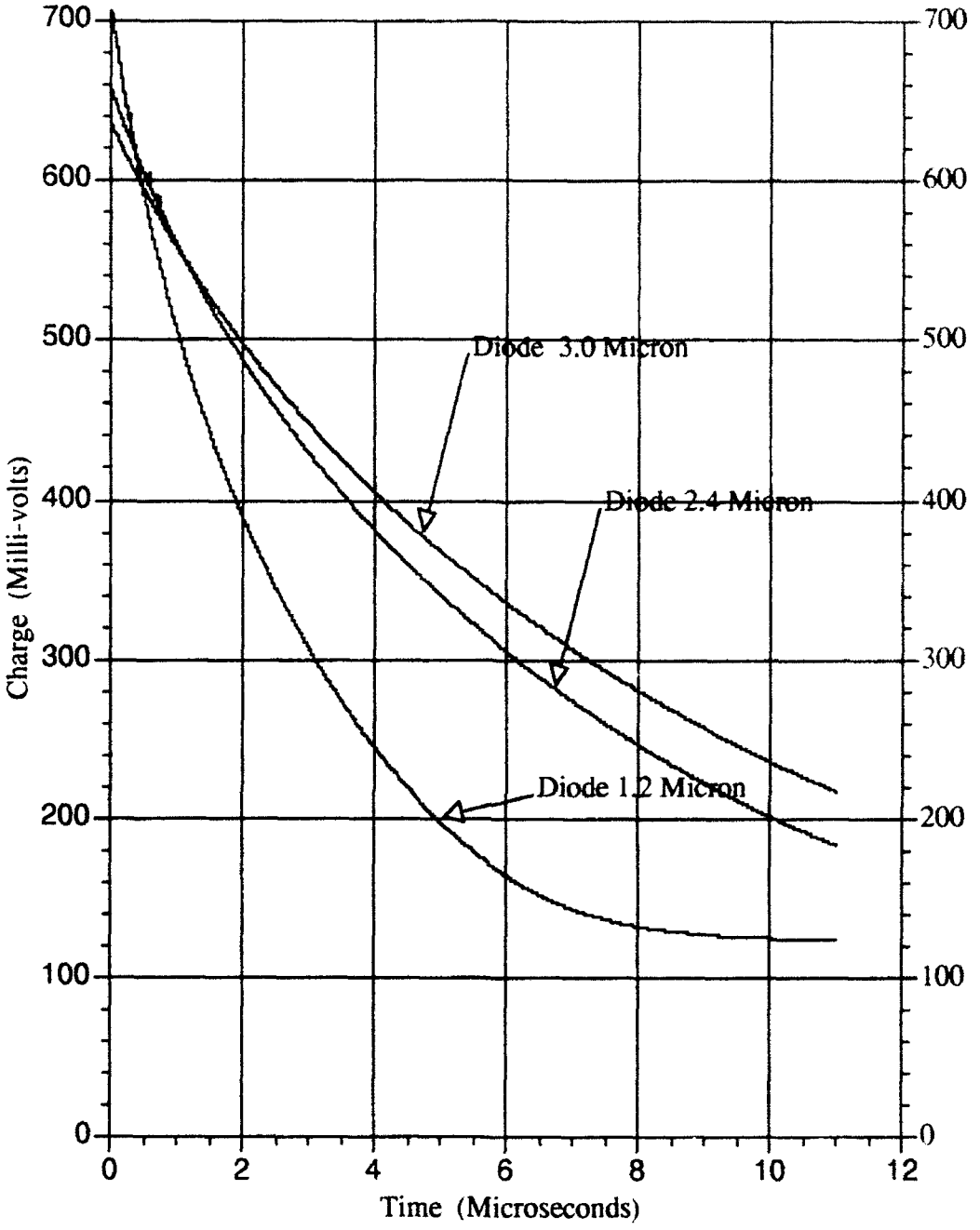
Figure A11



Charge Comparisons

150 FF Capacitor --- 3.0 Micron Transistor Length

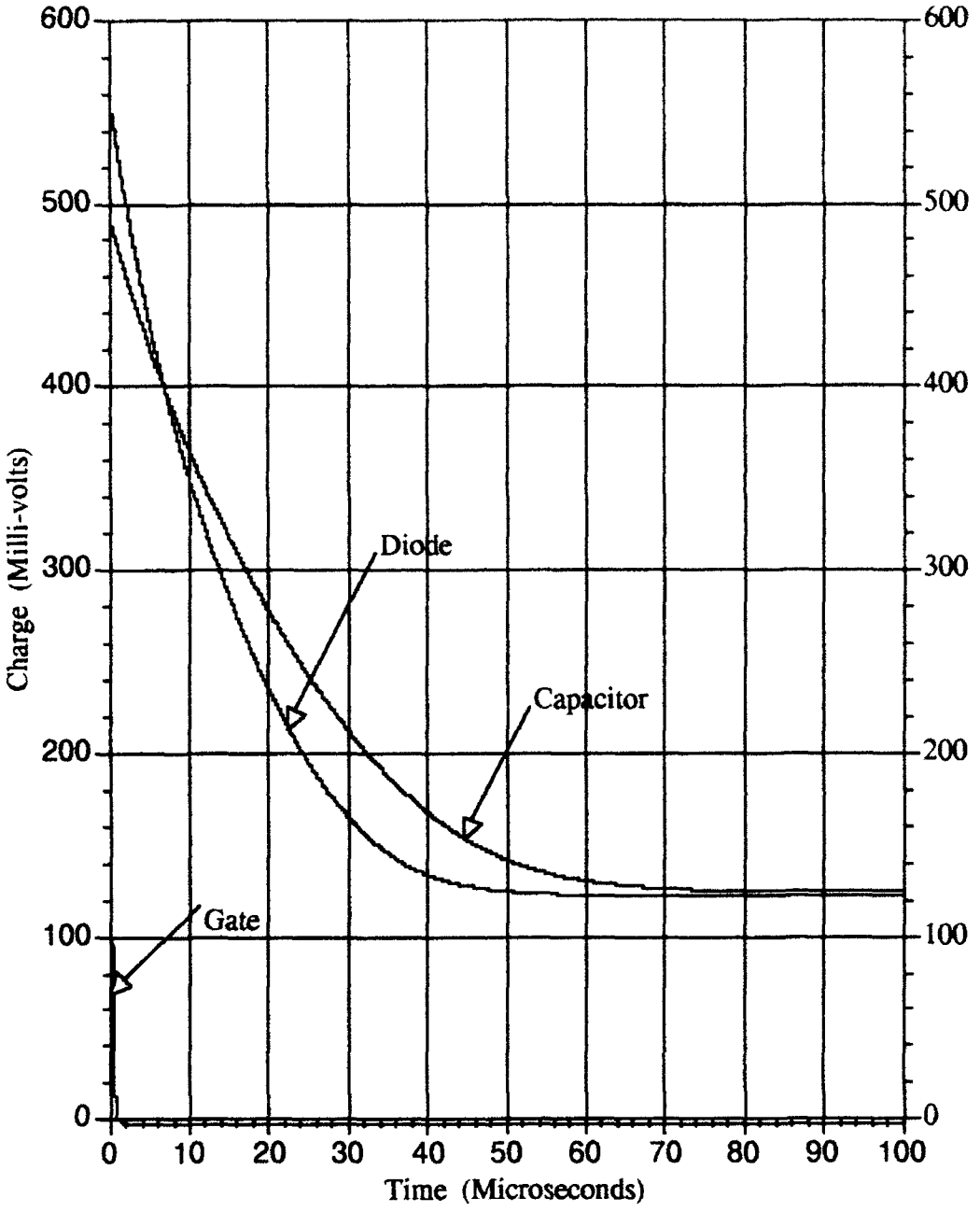
Figure A12



Charge Comparisons

150 FF capacitor --- 1.2, 2.4 and 3.0 Micron Lengths

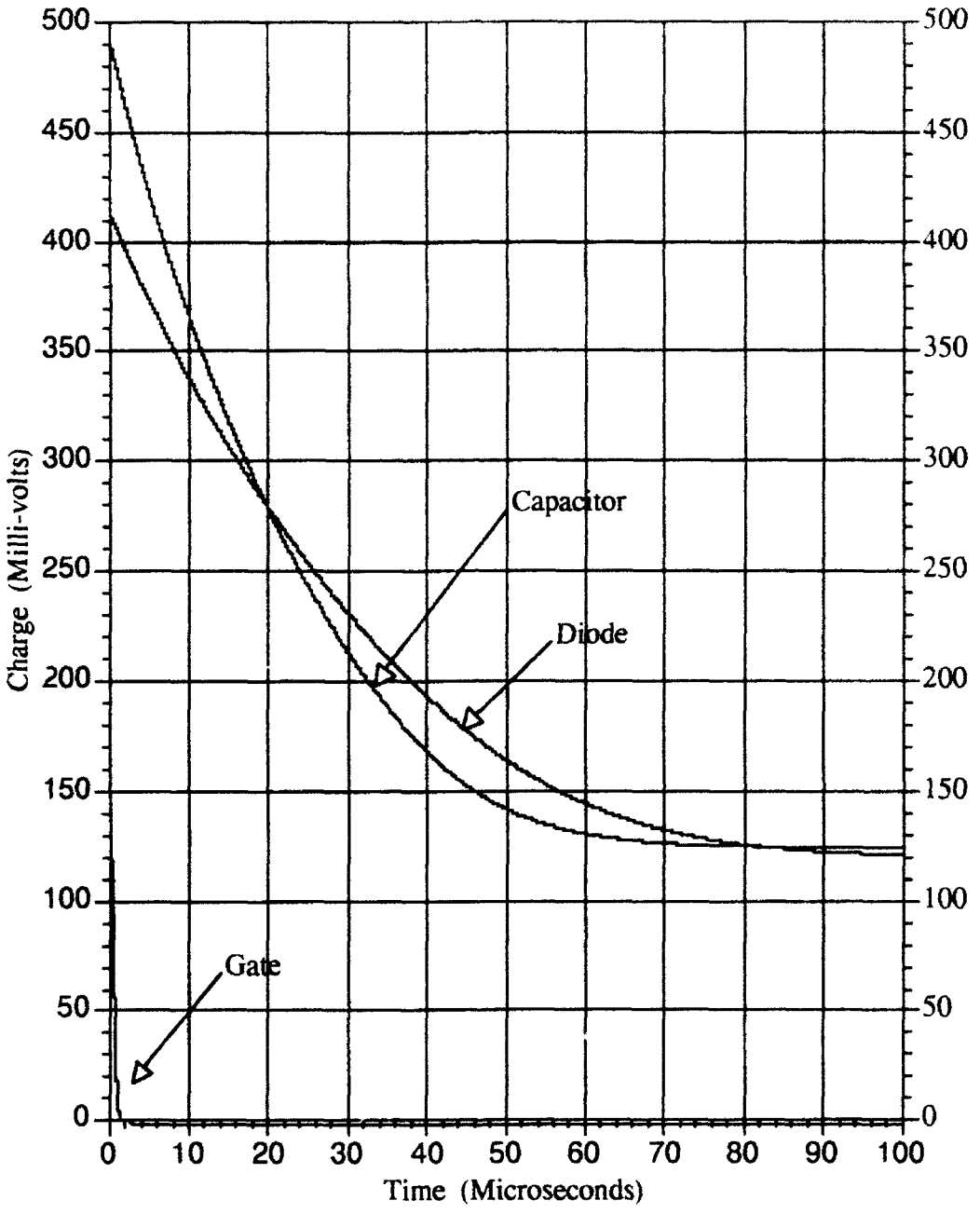
Figure A13



Charge Comparisons

856.1 FF Capacitor --- 1.2 Micron Transistor Length

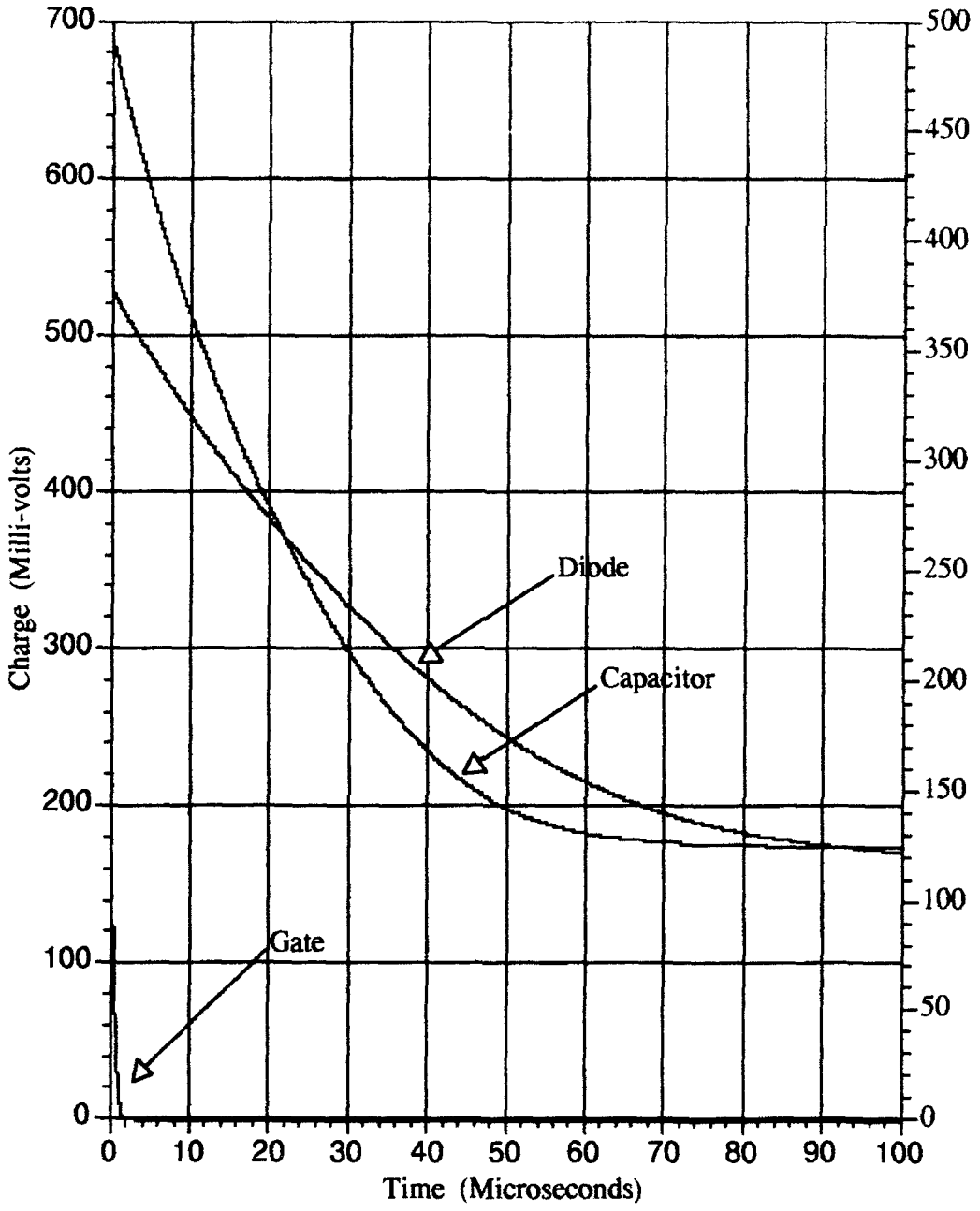
Figure A14



Charge Comparisons

856.1 FF Capacitor --- 2.4 Micron Transistor Length

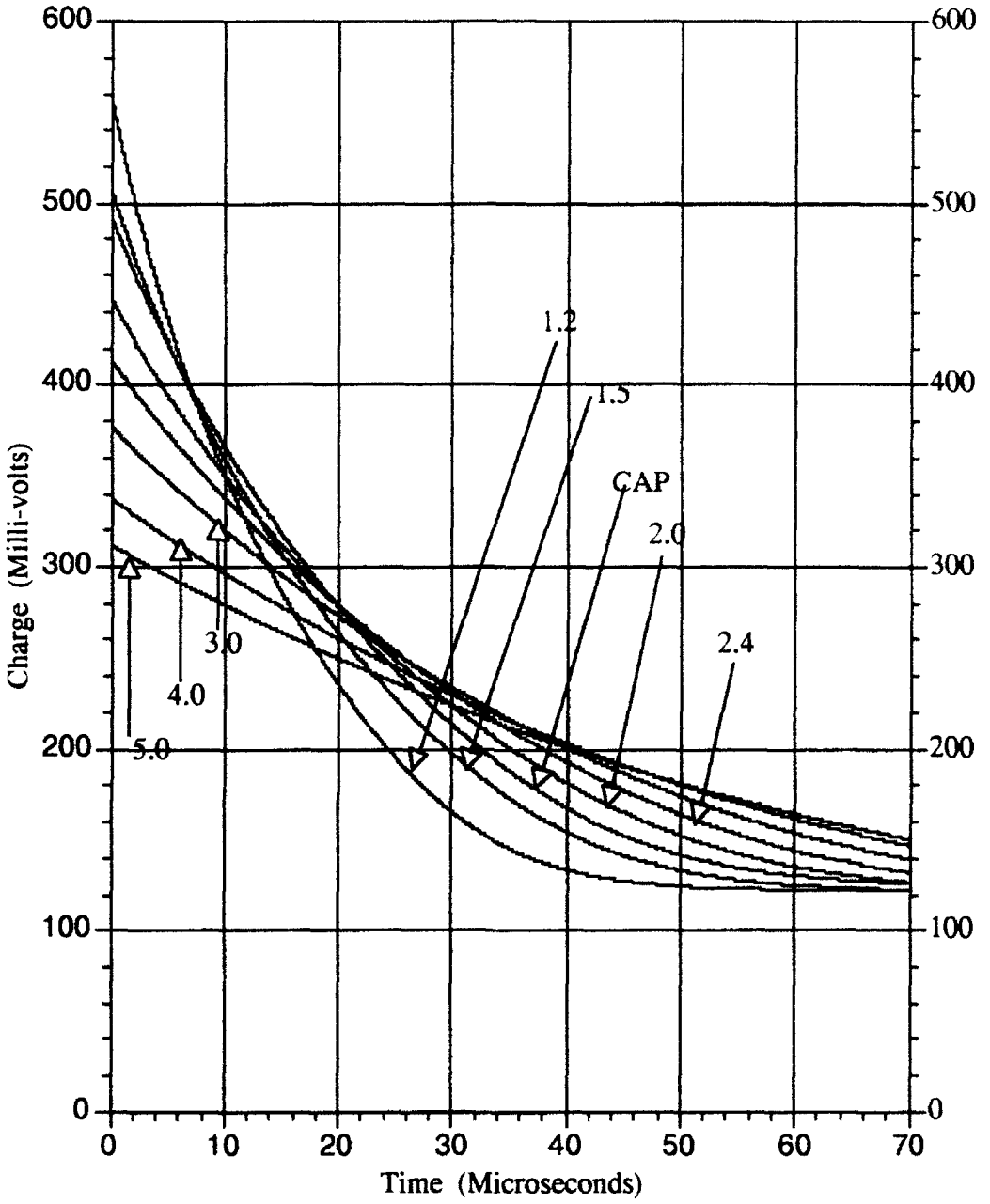
Figure A15



Charge Comparisons

856.1 FF Capacitor --- 3.0 Micron Transistor Length

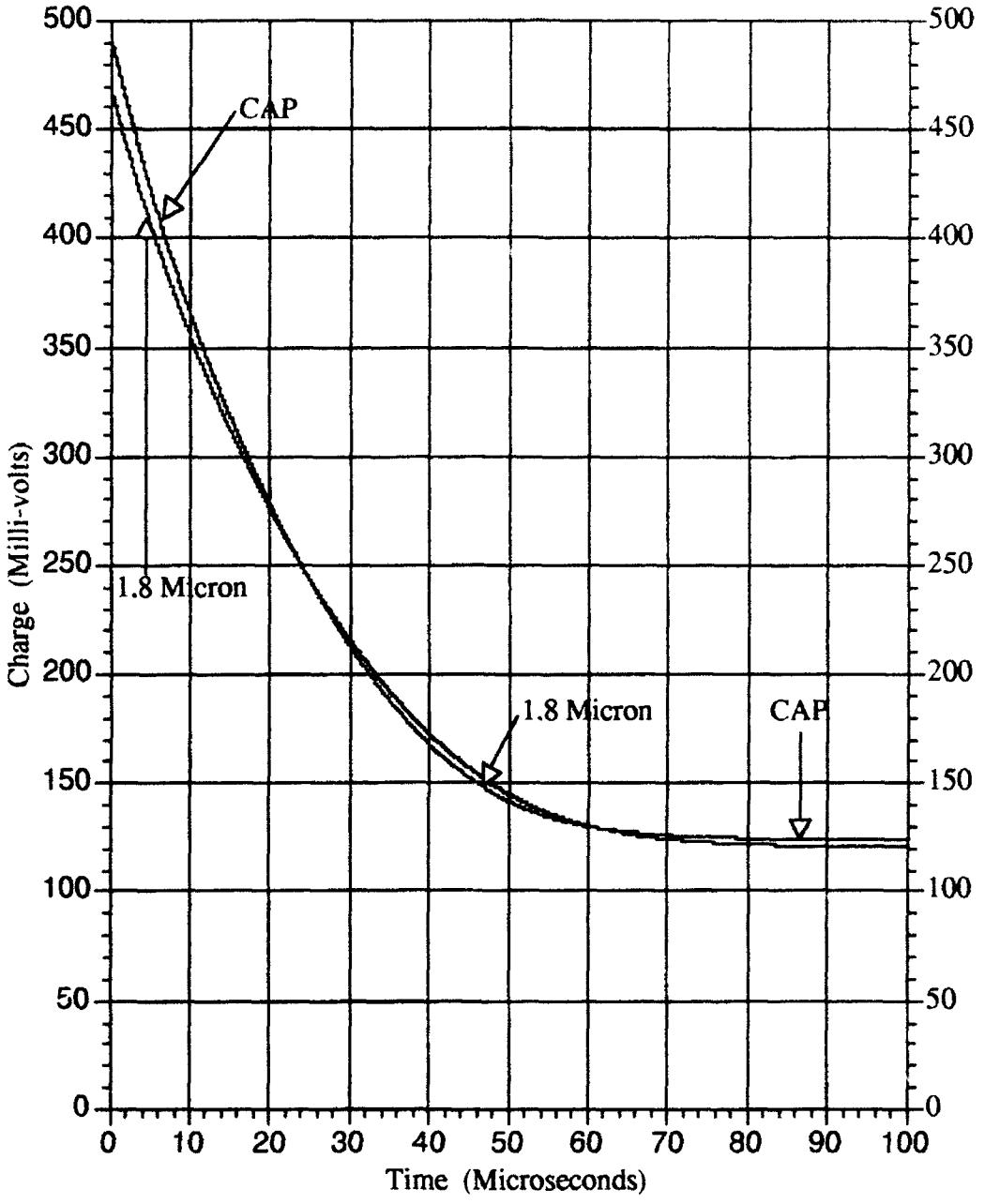
Figure A16



Charge Comparisons

856.1 FF Capacitance --- 1.2 Micron to 5.0 Micron Gate Length

Figure A17



Charge Comparisons

856.1 FF Capacitance -- 1.8 Micron Gate Length

Figure A18

APPENDIX B

WAVEFORMS

This appendix contains the waveforms that describe the functioning of the memory cell, sense amplifier, and Memory Array. A brief description of the waveforms will be given here as the operation of the circuitry is covered in the main body of the paper.

The first two figures, Figure B1 and Figure B2, show the basic control waveforms and how they are timed in relation to each other. The Sense pulse and the Equalization pulse are 180° out of phase. The Sense pulse is delayed from the Read/Write pulse to allow the memory cell and the dummy cell to upset the balance of the BIO lines before the sense transistors come on.

Figure B3 shows the Write of a ONE to both sides of the sense amplifier. It shows how the two BIO lines are precharged and equalized and how the BIO lines are pulled high for each Write. Notice that the sense amplifier action causes one BIO line to go low when one goes high. Figure B4 is also a graph of a Write to both sides of the sense amplifier, but it also includes the cell charges so that the charging rate and level can be seen. Figure B5 is an enlarged graph of a Write to one side, it also includes the Sense pulse. The action of the Sense pulse can be seen by analyzing the behavior of the Odd BIO Line.

Figure B6 shows a Write of a ZERO. The Even BIO Line is pulled high for the first half of graph because a Write of a ONE is occurring on the even side. The Write of a ZERO happens to the odd side, as can be seen by the way the Odd BIO Line is pulled low. Notice how the opposite (even) BIO line almost goes as high as it would have during a Write of a ONE on that side. This demonstrates the ability of the sense amplifier to pull the BIO lines in opposite directions and to get them to very good levels.

Figure B7 is the Read of a ONE. Here, it is easier to see the balance of the two BIO lines get upset by the memory cell and the dummy cell on the rising edge of the Read pulse.

It is also easy to see the effect of the Sense pulse coming on. The Even Cell gets read and its charge is refreshed.

Figure B8 is the Read of a ZERO. Again, the BIO lines get unbalanced, and the sense transistors pull the BIO lines in the proper directions. The memory cell charges a little by the higher potential of the BIO line, but goes back down at the end of the cycle.

Figure B9 is a comparison again between a capacitor and a diode. This time it is to see if there is any difference in charge levels on a Read. It is interesting that the Read of a diode charges about the same height as the capacitor. The capacitor will Write to a higher value, but during the Read the diode catches up.

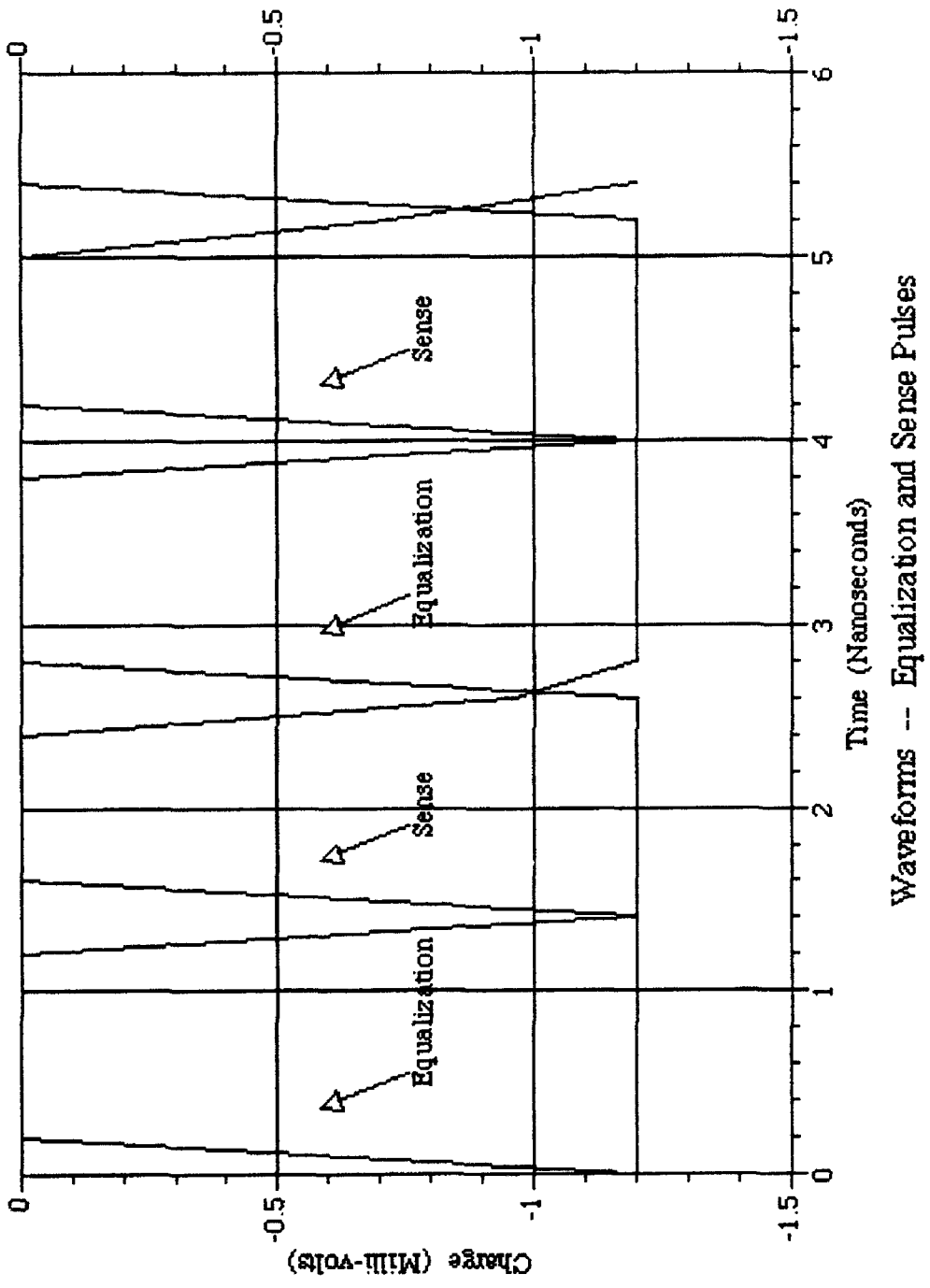

Waveforms -- Equalization and Sense Pulses
Charge (Milli-volts)
Time (Nanoseconds)
Equalization
Sense
Equalization
Sense
0
-0.5
-1
-1.5
0
1
2
3
4
5
6

Figure B1

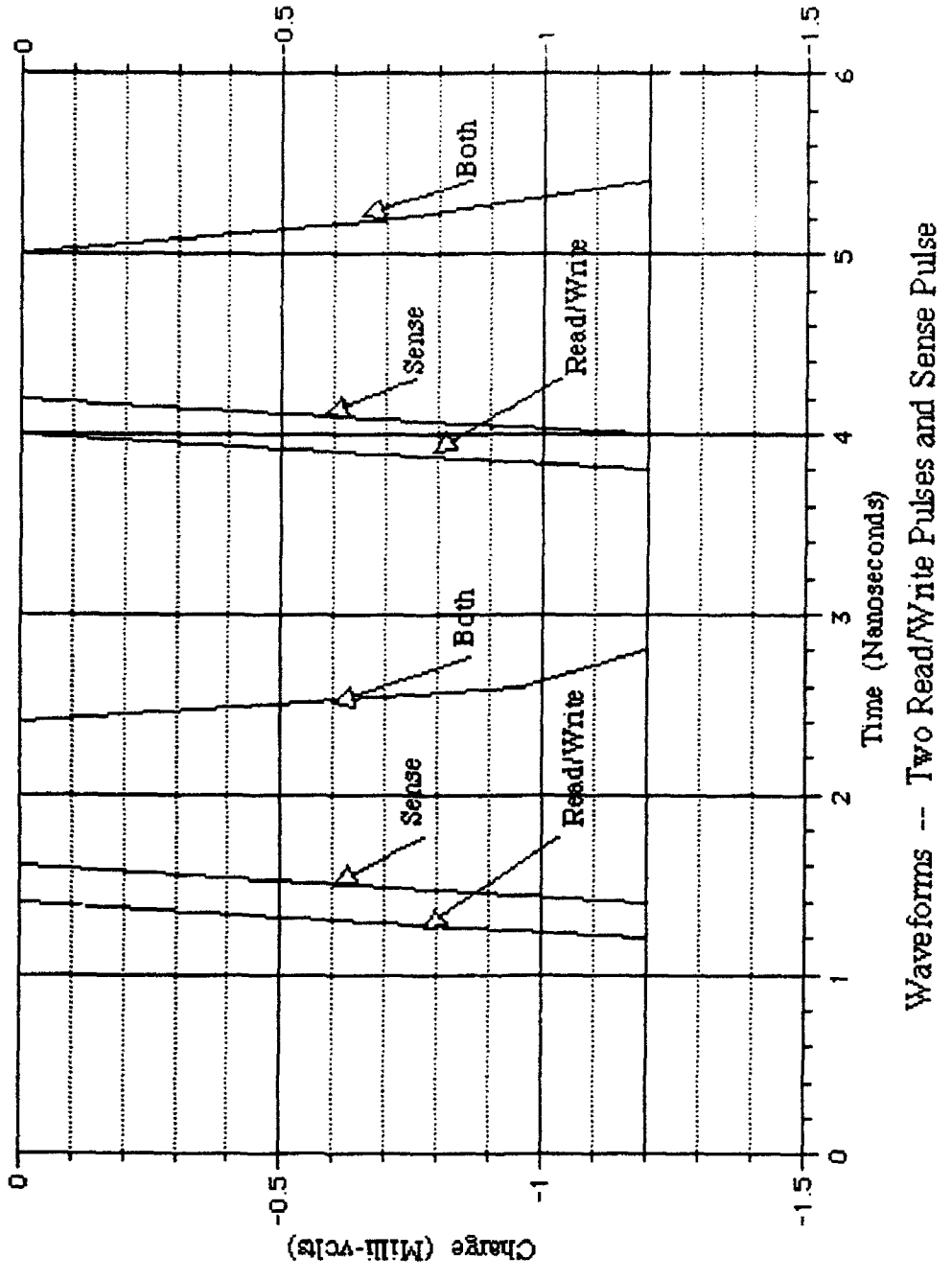

Waveforms -- Two Read/Write Pulses and Sense Pulse
Time (Nanoseconds)
Charge (Milli-volts)
Both
Sense
Read/Write
Both
Sense
Read/Write
0
1
2
3
4
5
6
0
-0.5
-1
-1.5

Figure B2

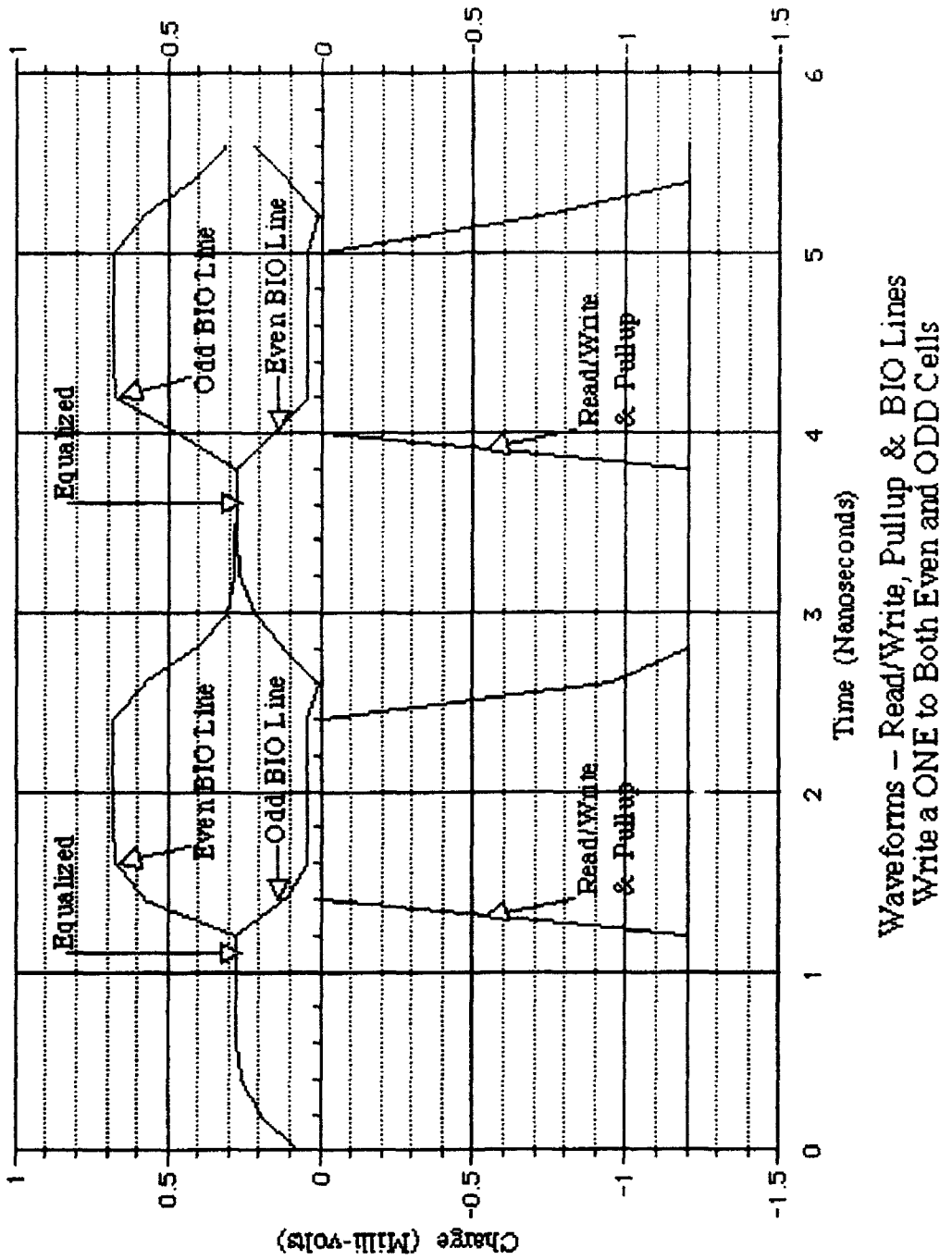

Waveforms – Read/Write, Pullup & BIO Lines
Write a ONE to Both Even and ODD Cells
Time (Nanoseconds)
Charge (Milli-volts)
Equalized
Even BIO Line
Odd BIO Line
Read/Write
& Pullup
Equalized
Odd BIO Line
Even BIO Line
Read/Write
& Pullup

Figure B3

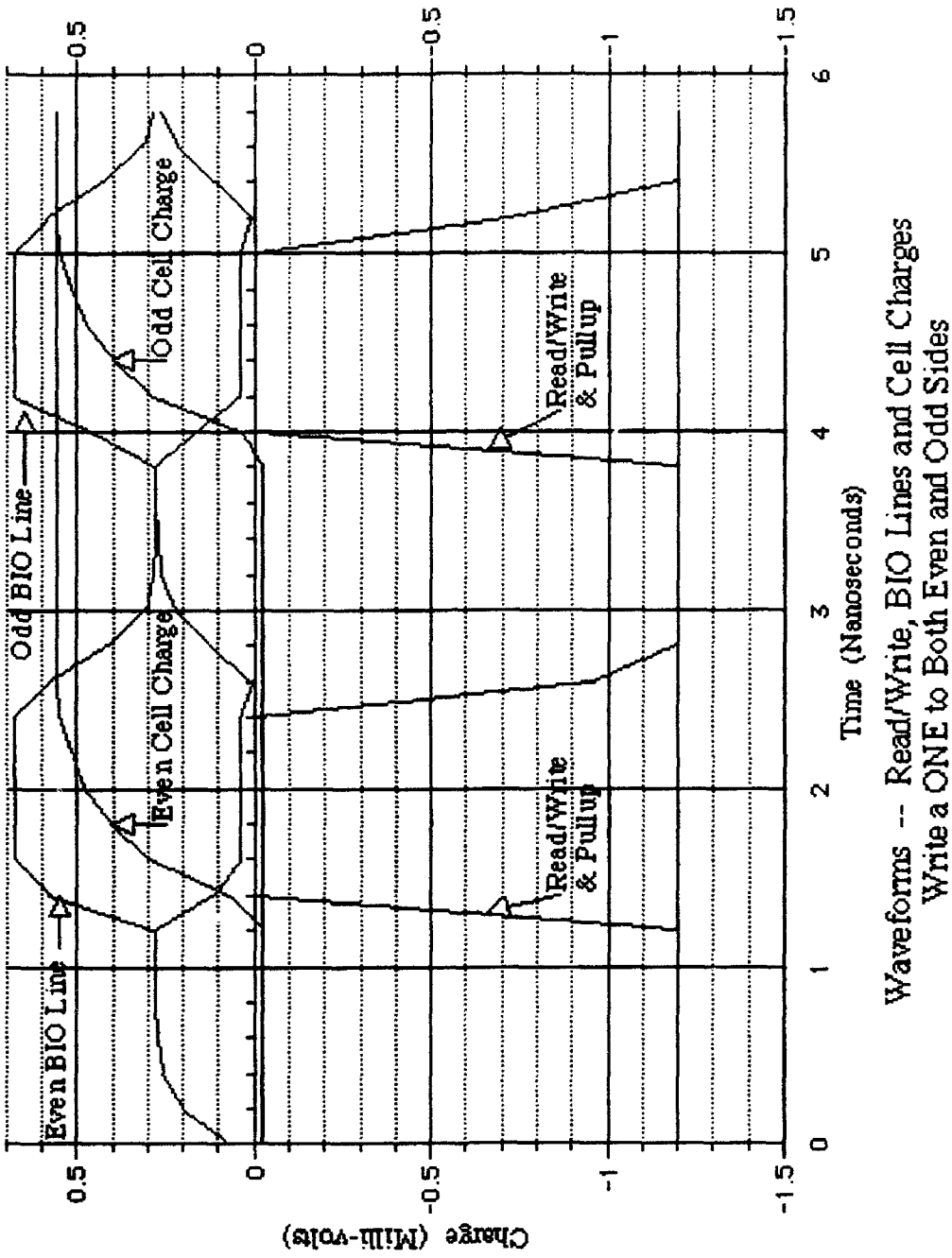
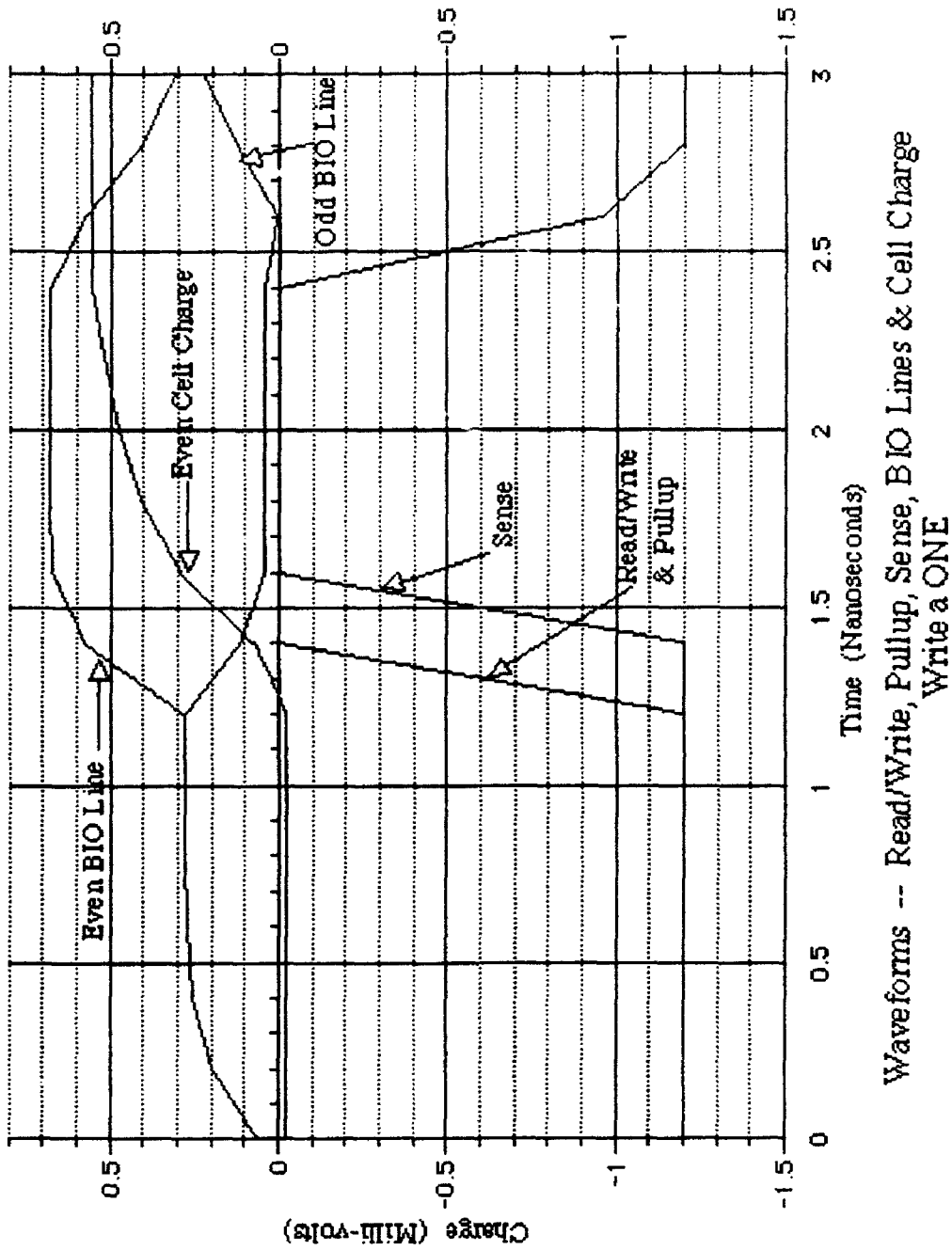
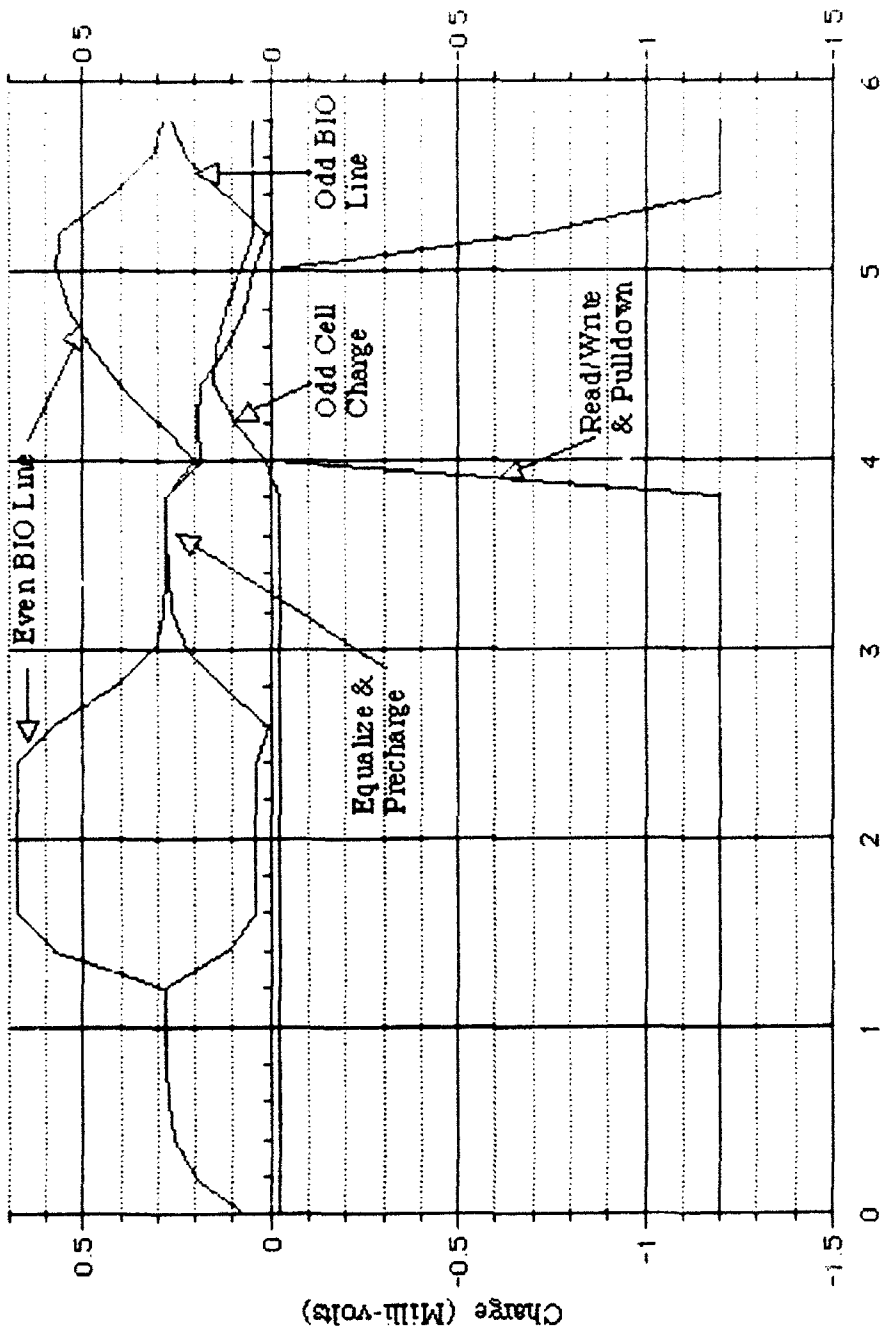

Waveforms -- Read/Write, BIO Lines and Cell Charges
Write a ONE to Both Even and Odd Sides
Time (Nanoseconds)
Charge (Milli-volts)
Even BIO Line
Odd BIO Line
Even Cell Charge
Odd Cell Charge
Read/Write & Pullup
Read/Write & Pullup
0.5
0
-0.5
-1
-1.5
0
1
2
3
4
5
6

Figure B4



Waveforms -- Read/Write, Pullup, Sense, BIO Lines & Cell Charge
Write a ONE

Figure B5



Waveforms -- Read/Write, Cell Charge and BIO Lines
Write a Zero

Figure B6

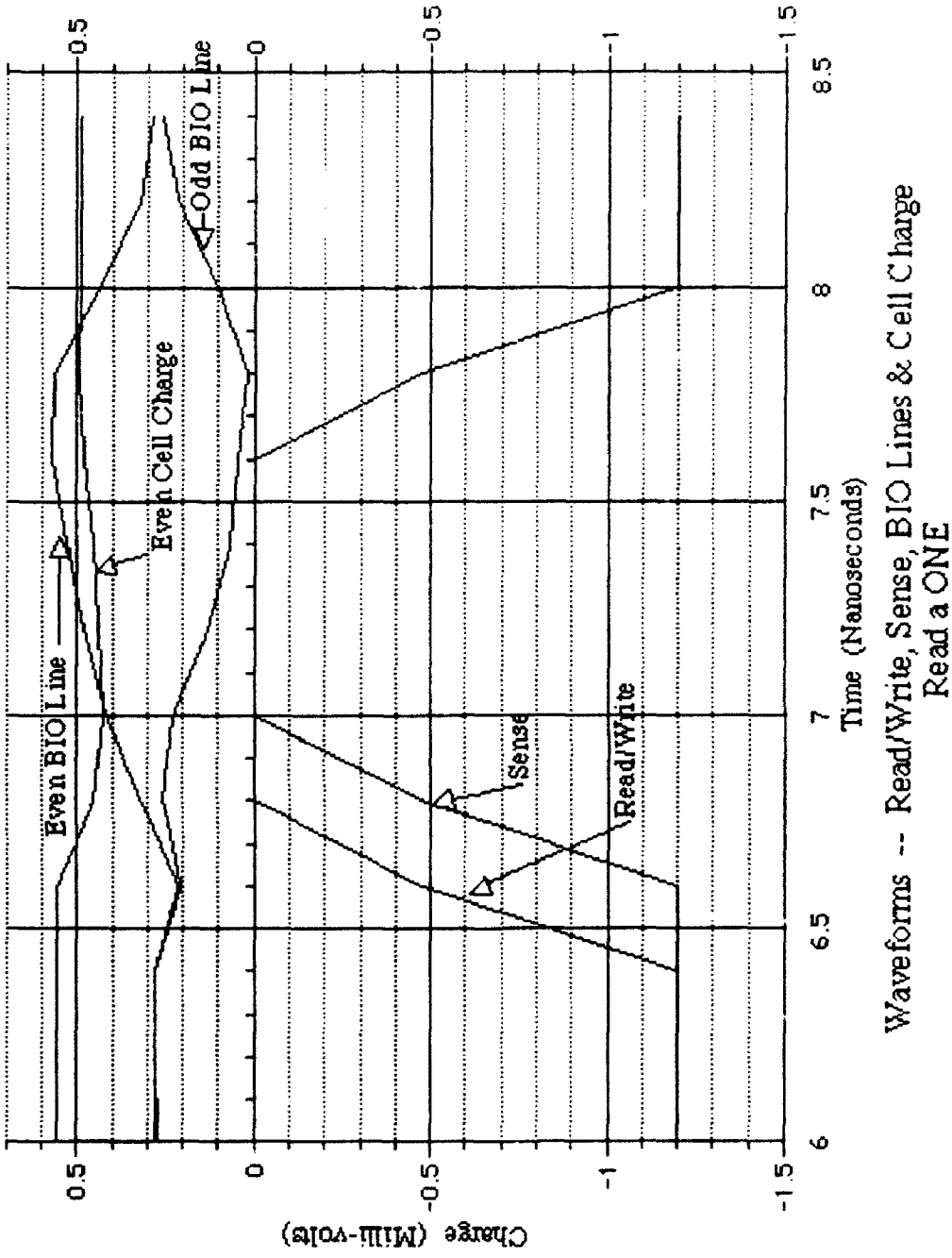

Even BIO Line
Even Cell Charge
Odd BIO Line
Sense
Read/Write
Charge (Milli-volts)
Time (Nanoseconds)
Waveforms -- Read/Write, Sense, BIO Lines & Cell Charge
Read a ONE

Figure B7

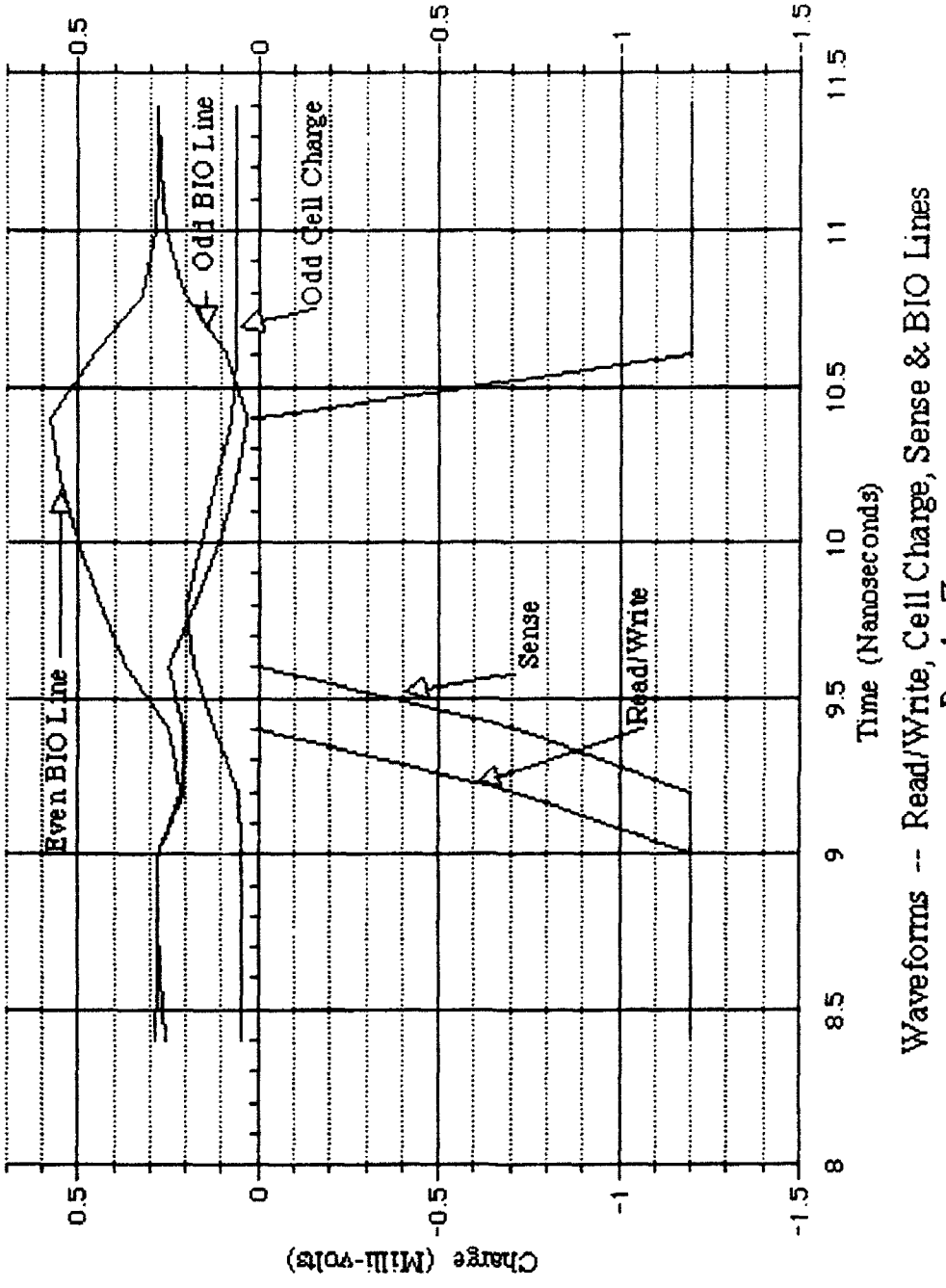
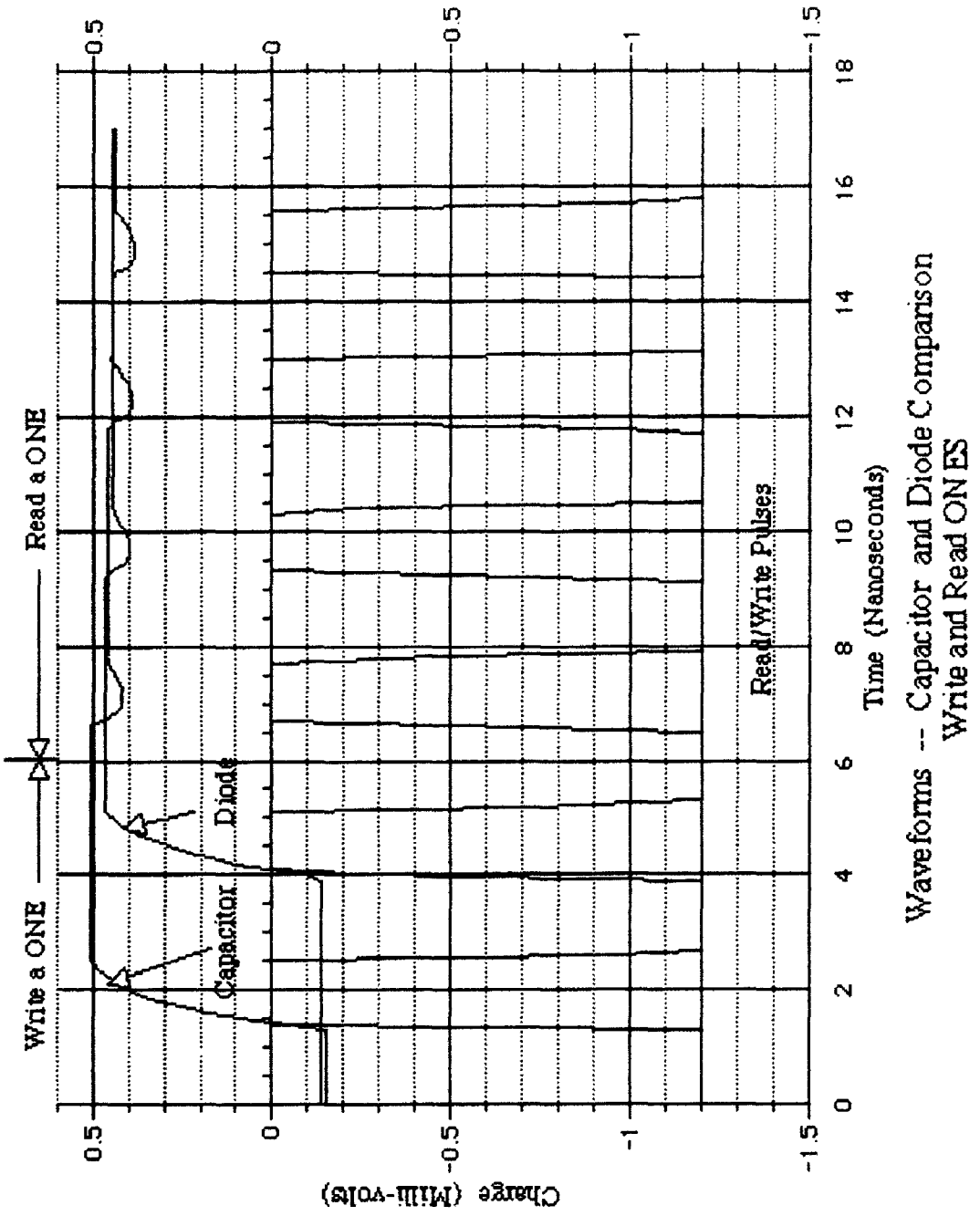

Waveforms -- Read/Write, Cell Charge, Sense & BIO Lines
Read a Zero
Time (Nanoseconds)
Charge (Milli-volts)
Even BIO Line
Odd BIO Line
Odd Cell Charge
Sense
Read/Write
0.5
0
-0.5
-1
-1.5
8
8.5
9
9.5
10
10.5
11
11.5

Figure B8



Waveforms -- Capacitor and Diode Comparison
Write and Read ONES

Figure B9

APPENDIX C

MEMORY ARRAY CHARGE MAINTENANCE

This appendix contains the charge maintenance comparisons for the entire memory array. Figure C1 through Figure C11 display the charge maintenance abilities of the array for a wide spread of precharge values. They also compare diodes with gate lengths of 1.8, 2.0, and 2.4 microns and a capacitor, all with the same physical size. The obvious thing to notice is that the higher the precharge, the better the charge maintenance. Also, notice that the capacitor is better than the diodes at precharge values over 0.20 volts. This precharge value though, is not the level of the voltage source to put into the memory array. The precharge level in these graphs is the effective precharge level. In other words, to perform the simulations in reasonable periods of time, some shortcuts had to be taken and one of them was to put the BIO lines at a voltage level and leave them there for the entire simulation. It is a perfect continuous precharge. The actual circuit precharges to a higher value, but only holds the BIO lines there for a relatively short period of time. The BIO lines precharge to approximately 0.27 volts, and this equates to a more realistic value or effective value of 0.17 volts. This can be seen by comparing Figure C1 with Figure C12. Figure C1 was simulated with the precharge of the circuit functioning as designed and it took a long time. The last figure demonstrates the charge maintenance with all precharge turned off. Figure C13 shows that with no precharge the charge will not last a tenth of a millisecond.

I. HSPICE FILES

A. HSPICE FILE FOR ARRAY WITH PRECHARGE

Vitesse HGaAs3 Ram Cell Date: 17 November 1992

```
* include Vitesse HGaAs3 models and parameters for hspice.
.protect
.include '/tools3/cad/meta/h9007/lib/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h9007/lib/vitesse/hgaas3.corners' tt
```

```
.unprotect
* power supply
* vds is the positive voltage rail
* vrefb is the precharge power supply for the BIT I/O Line
* vrefd is the precharge power supply for the Dummy Cell Capacitors
vds 1 0 2.0
vrefb 777 0 0.7
vrefd 888 0 0.26
* Driving Control Signals
* vv is the Odd BIT I/O Pull-up
*vv  84  0  -1.2V
* vv1 is the Odd BIT I/O Line Pull-down
vv1 85  0  0.0V
* vw is the Even BIT I/O Line Pull-up
*vw  82  0  -1.2V
* vw1 is the Even BIT I/O Line Pull-down
vw1 83  0  0.0V

* The vrc signals are the Read/Write Transistors for all the cells
*vrc1  21  0  -1.2v
*vrc3  23  0  -1.2v
vrc5  25  0  -1.2v
vrc7  27  0  -1.2v
*vrc2  22  0  -1.2v
vrc4  24  0  -1.2v
vrc6  26  0  -1.2v

vrc0 20  0  PULSE(-1.2  0  1300PS  100PS  100PS 1120PS  10MS)
vrc1  21  0  PULSE(-1.2 0 6540PS  100PS  100PS 1120PS  10MS)
vrc2  22  0  PULSE(-1.2 0 3920PS  100PS  100PS 1120PS  10MS)
vrc3  23  0  PULSE(-1.2 0 9160PS  100PS  100PS 1120PS  10MS)

* These signals are the Odd and Even Dummy controls
*vedc 40   0  PULSE(-1.2  0  1300PS  100PS  100PS 1120PS  5240PS)
vedc 40   0  -1.2v
*vodc 41   0  PULSE(-1.2  0  3920PS  100PS  100PS 1120PS  5240PS)
vodc 41   0  -1.2v

* This signal is the Sense signal
*vqd 189  0  PULSE(-1.2  0  1430PS  100PS  100PS  990PS  2620PS)
vqd 189  0  -1.2v

* This signal is the Precharge signal and Equalization signal
```

```
vp 88  0  PULSE(-1.2 0   0PS  100PS  100PS  1100PS  2620PS)
*vp 88  0  -1.2v

* These signals are the Pull-up and Pull-down signals for the BIT
* I/O Lines
vw 82  0  PULSE(-1.2 0 1300PS  100PS  100PS 5000PS  10MS)
vv 84  0  PULSE(-1.2 0 6500PS  100PS  100PS 6000PS  10MS)
*vw1 83  0  PULSE(0  0.6  700PS  100PS  100PS  920PS  117600PS)
*vv1 85  0  PULSE(0  0.6 2600PS  100PS  100PS  920PS  117600PS)

* The following transistors make up the memory array with j23, j24
* and j25 as the three diodes that were added for comparisons.
*   D   G   S   B
j0    1     189  98   0     jfet16 l=1.2 w=9.0
j1    1     189  99   0     jfet16 l=1.2 w=9.0
j2    98    20   50   0     jfet16 l=1.2 w=8.0
j3    98    41   52   0     jfet16 l=1.2 w=8.0
j4    98    99   0    0     jfet04 l=1.2 w=210.0
j5    99    98   0    0     jfet04 l=1.2 w=210.0
j6    99    40   53   0     jfet16 l=1.2 w=8.0
j7    99    21   51   0     jfet16 l=1.2 w=8.0
j8    888   88   52   0     jfet16 l=1.2 w=3.0
j9    1     82   98   0     jfet16 l=1.2 w=185.0
j10   1     84   99   0     jfet16 l=1.2 w=185.0
j11   98    83   0    0     jfet04 l=1.2 w=6.0
j12   99    85   0    0     jfet04 l=1.2 w=6.0
j13   98    88   99   0     jfet16 l=1.2 w=20.0
j14   98    22   54   0     jfet16 l=1.2 w=8.0
j15   98    24   56   0     jfet16 l=1.2 w=8.0
j16   98    26   58   0     jfet16 l=1.2 w=8.0
j17   99    23   55   0     jfet16 l=1.2 w=8.0
j18   99    25   57   0     jfet16 l=1.2 w=8.0
j19   99    27   59   0     jfet16 l=1.2 w=8.0
j20   888   88   53   0     jfet16 l=1.2 w=3.0
j21   777   88   99   0     jfet16 l=1.2 w=6.0
j22   777   88   98   0     jfet16 l=1.2 w=6.0
j23   51    0    51   0     dio19  l=2.0 w=271.7
j24   54    0    54   0     dio19  l=1.8 w=277.8
j25   55    0    55   0     dio19  l=2.4 w=260.4

* The 856 FF capacitors are the memory capacitors
* The 70 FF capacitors are the Dummy capacitors
* The other two capacitors are for the BIT I/O Lines
```

```
c0      50   0    856FF
*c1     51   0    856FF
c2      52   0    70FF
c3      53   0    70FF
*c4     54   0    856FF
*c5     55   0    856FF
c6      56   0    856FF
c7      57   0    856FF
c8      58   0    856FF
c9      59   0    856FF
c10     98   0    750FF
c11     99   0    750FF


.tran 0.01MS 10.8MS
.probe v(50) v(51) v(54) v(55)
.print v(50) v(51) v(54) v(55)
.options scale=1E-06 post captab probe gmindc=1E-6
.end
```

A. HSPICE FILE FOR MEMORY ARRAY WITH SEPARATE PRECHARGE

```
Vitesse HGaAs3 Ram CellDate: 18 November 1992

* include Vitesse HGaAs3 models and parameters for hspice.
.protect
.include '/tools3/cad/meta/h9007/lib/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h9007/lib/vitesse/hgaas3.corners' tt
.unprotect

* power supply
vds 1 0 2.0
* vrefb is BIO Line precharge and is not used.
vrefb 777 0 0.7
* vrefd is Dummy Cell precharge and is not used.
vrefd 888 0 0.26
* vrefx is the permanent BIO Line precharge - it is the level
* at which the BIO Line is maintained after the initial Writing
* is done
vrefx 666 0 0.17

* Pull-up, Pull-down  Control Signals
*vv  84   0   -1.2V
```

```
vv1 85  0  0.0V
*vw  82  0  -1.2V
vw1 83  0  0.0V

* Read/Write transistors vrc0, vrc1, vrc2, vrc3 are used below to
* write to the cells.
*vrc1  21  0  -1.2v
*vrc3  23  0  -1.2v
vrc5  25  0  -1.2v
vrc7  27  0  -1.2v
*vrc2  22  0  -1.2v
vrc4  24  0  -1.2v
vrc6  26  0  -1.2v

vrc0 20  0  PULSE(-1.2  0  1300PS  100PS  100PS 1120PS  10MS)
vrc1  21  0  PULSE(-1.2  0 6540PS  100PS  100PS 1120PS  10MS)
vrc2  22  0  PULSE(-1.2  0 3920PS  100PS  100PS 1120PS  10MS)
vrc3  23  0  PULSE(-1.2  0 9160PS  100PS  100PS 1120PS  10MS)

* Dummy Cell control signals are turned off.
*vedc 40  0  PULSE(-1.2  0  1300PS  100PS  100PS 1120PS  5240PS)
vedc 40  0  -1.2v
*vodc 41  0  PULSE(-1.2  0  3920PS  100PS  100PS 1120PS  5240PS)
vodc 41  0  -1.2v

* Sense transistors are removed
*vqd 189  0  PULSE(-1.2  0  1430PS  100PS  100PS  990PS  2620PS)
*vqd 189  0  -1.2v

* Control signal for BIO Lines permanent precharge
vex 87 0 PULSE(-1.2 0 13000PS 100PS 100PS 10MS 12MS)

* Normal precharge transistors are removed.
*vp  88  0  PULSE(-1.2  0  0PS  100PS  100PS  1100PS  2620PS)
*vp  88  0  -1.2v

* Pull-up signals to Write ONEs
vw  82  0  PULSE(-1.2  0  1300PS  100PS  100PS 5000PS  10MS)
vv  84  0  PULSE(-1.2  0  6500PS  100PS  100PS 6000PS  10MS)

*vw1 83  0  PULSE(0  0.6  700PS  100PS  100PS  920PS  117600PS)
*vv1 85  0  PULSE(0  0.6 2600PS  100PS  100PS  920PS  117600PS)
```

```
* Transistors for memory cell array
*       D     G     S     B
*j0     1     189   98    0     jfet16 l=1.2 w=9.0
*j1     1     189   99    0     jfet16 l=1.2 w=9.0
j2      98    20    50    0     jfet16 l=1.2 w=8.0
j3      98    41    52    0     jfet16 l=1.2 w=8.0
*j4     98    99    0     0     jfet04 l=1.2 w=210.0
*j5     99    98    0     0     jfet04 l=1.2 w=210.0
j6      99    40    53    0     jfet16 l=1.2 w=8.0
j7      99    21    51    0     jfet16 l=1.2 w=8.0
*j8     888   88    52    0     jfet16 l=1.2 w=3.0
j10     1     82    98    0     jfet16 l=1.2 w=185.0
j11     1     84    99    0     jfet16 l=1.2 w=185.0
j12     98    83    0     0     jfet04 l=1.2 w=6.0
j13     99    85    0     0     jfet04 l=1.2 w=6.0
*j14    98    88    99    0     jfet16 l=1.2 w=20.0
j15     98    22    54    0     jfet16 l=1.2 w=8.0
j16     98    24    56    0     jfet16 l=1.2 w=8.0
j17     98    26    58    0     jfet16 l=1.2 w=8.0
j18     99    23    55    0     jfet16 l=1.2 w=8.0
j19     99    25    57    0     jfet16 l=1.2 w=8.0
j20     99    27    59    0     jfet16 l=1.2 w=8.0
*j21    888   88    53    0     jfet16 l=1.2 w=3.0
*j23    777   88    99    0     jfet16 l=1.2 w=6.0
*j24    777   88    98    0     jfet16 l=1.2 w=6.0
j27     51    0     51    0     dio19  l=2.0 w=271.7
j28     54    0     54    0     dio19  l=1.8 w=277.8
j29     55    0     55    0     dio19  l=2.4 w=260.4
j30     666   87    99    0     jfet16 l=1.2 w=6.0
j31     666   87    98    0     jfet16 l=1.2 w=6.0

* Capacitors for cells without diodes.
* Capacitos for BIO Lines and Dummy Cells
c0      50    0     856FF
*c1     51    0     856FF
c2      52    0     70FF
c3      53    0     70FF
*c4     54    0     856FF
*c5     55    0     856FF
c6      56    0     856FF
c7      57    0     856FF
c8      58    0     856FF
c9      59    0     856FF
```

```
c10    98     0      750FF
c11    99     0      750FF

* Program controls.
.tran 0.01MS 10MS
.probe v(50) v(51) v(54) v(55)
.print v(50) v(51) v(54) v(55)
.options scale=1E-06 post captab probe gmindc=1E-6
.end
```

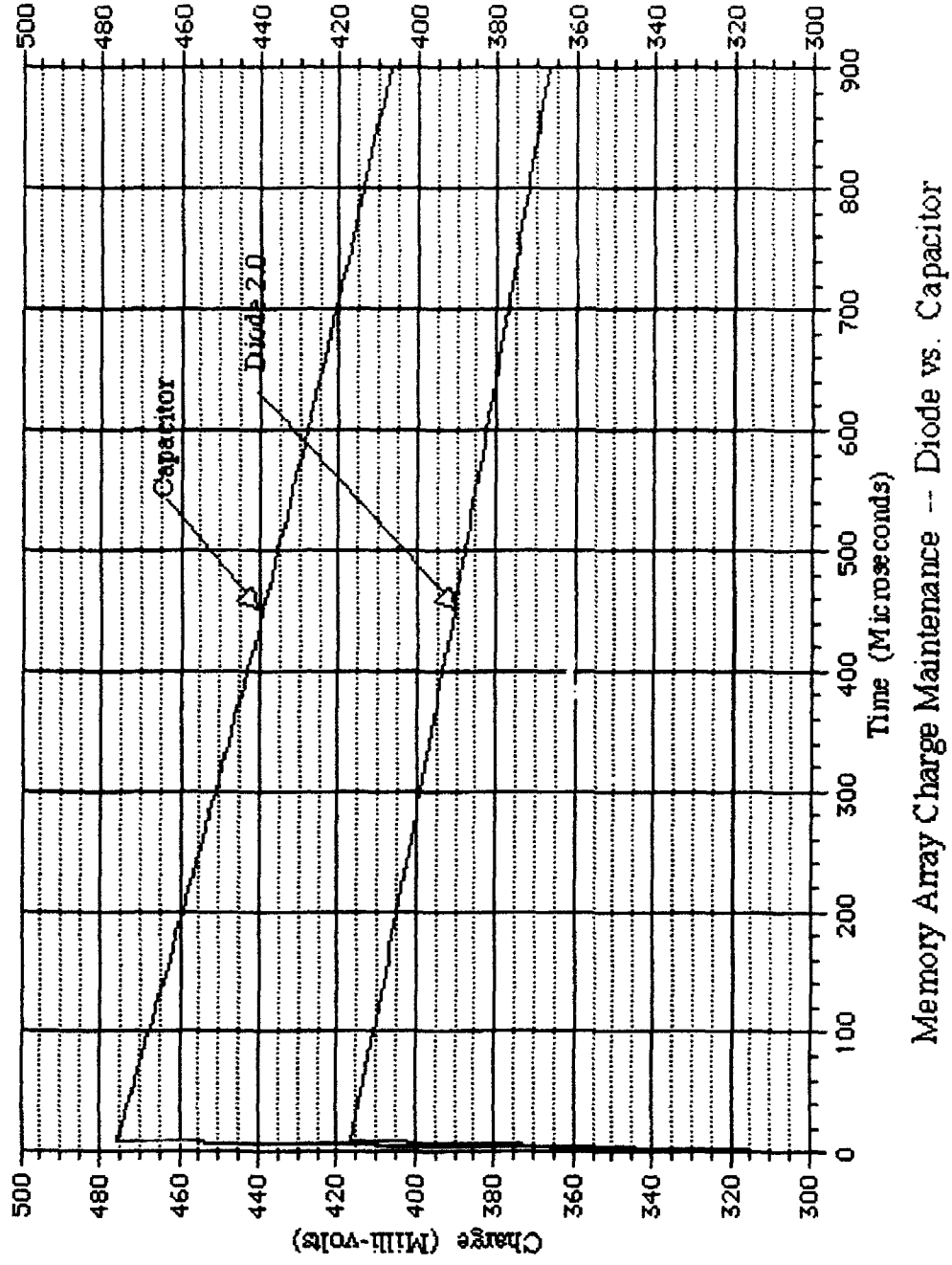

Memory Array Charge Maintenance -- Diode vs. Capacitor
Charge (Milli-volts)
Time (Microseconds)
Capacitor
Diode 2.0
500
480
460
440
420
400
380
360
340
320
300
0
100
200
300
400
500
600
700
800
900

Figure C1

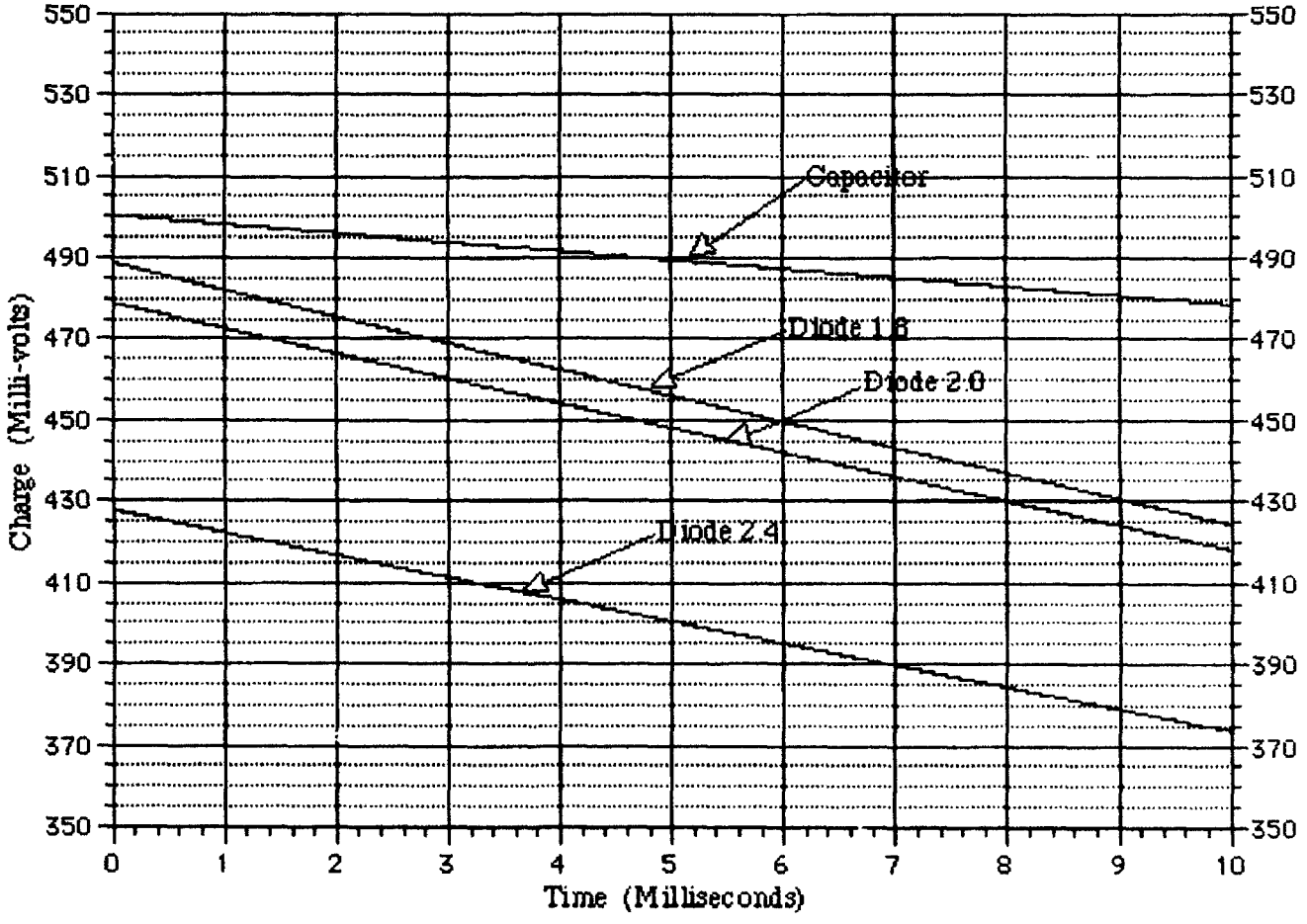


Figure C2

Memory Array Charge Maintenance -- Precharge 0.34 Volts

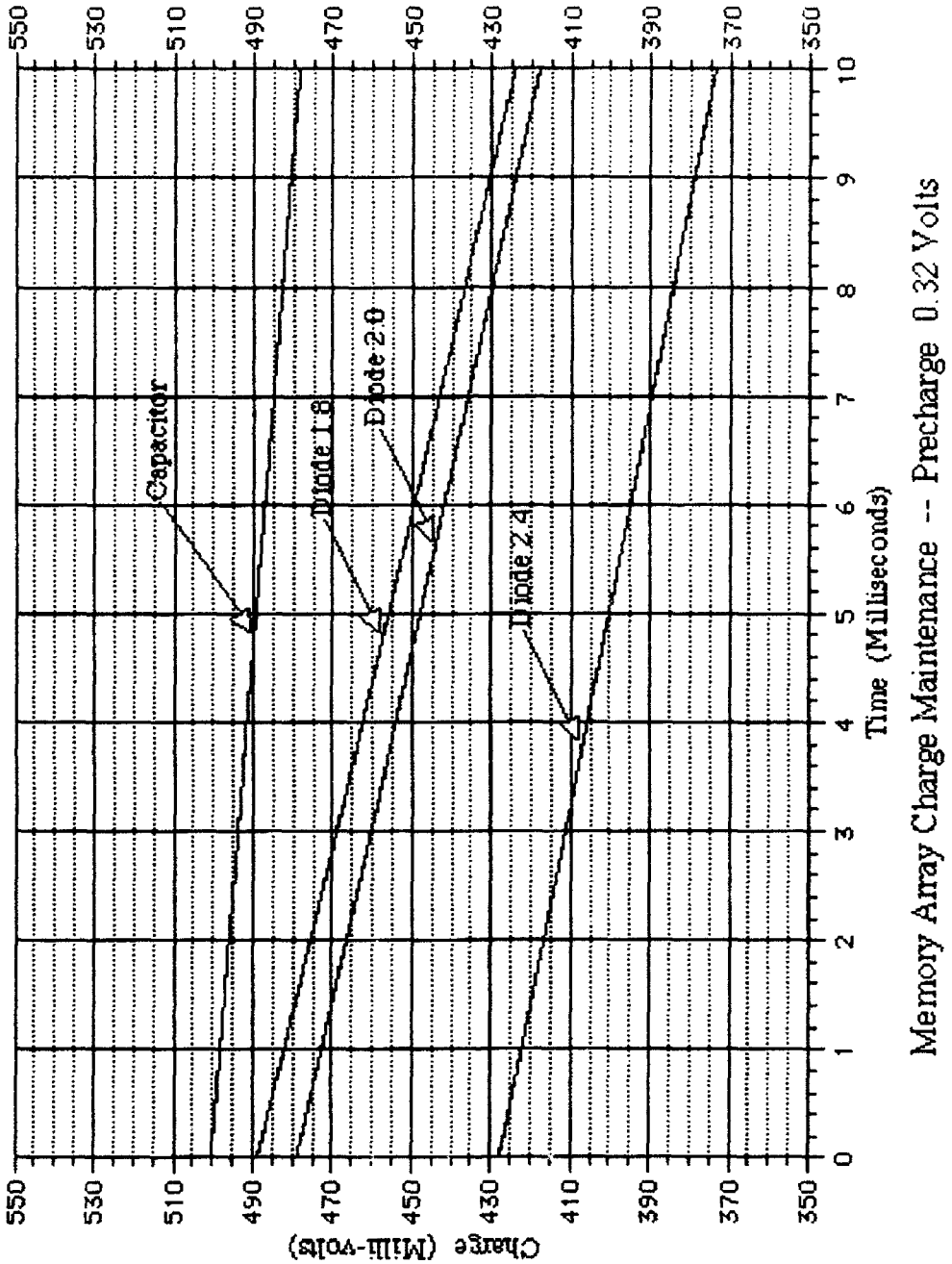

Memory Array Charge Maintenance -- Precharge 0.32 Volts
Time (Milliseconds)
Charge (Milli-volts)
Capacitor
Diode 1.8
Diode 2.0
Diode 2.4
550
530
510
490
470
450
430
410
390
370
350
0
1
2
3
4
5
6
7
8
9
10

Figure C3

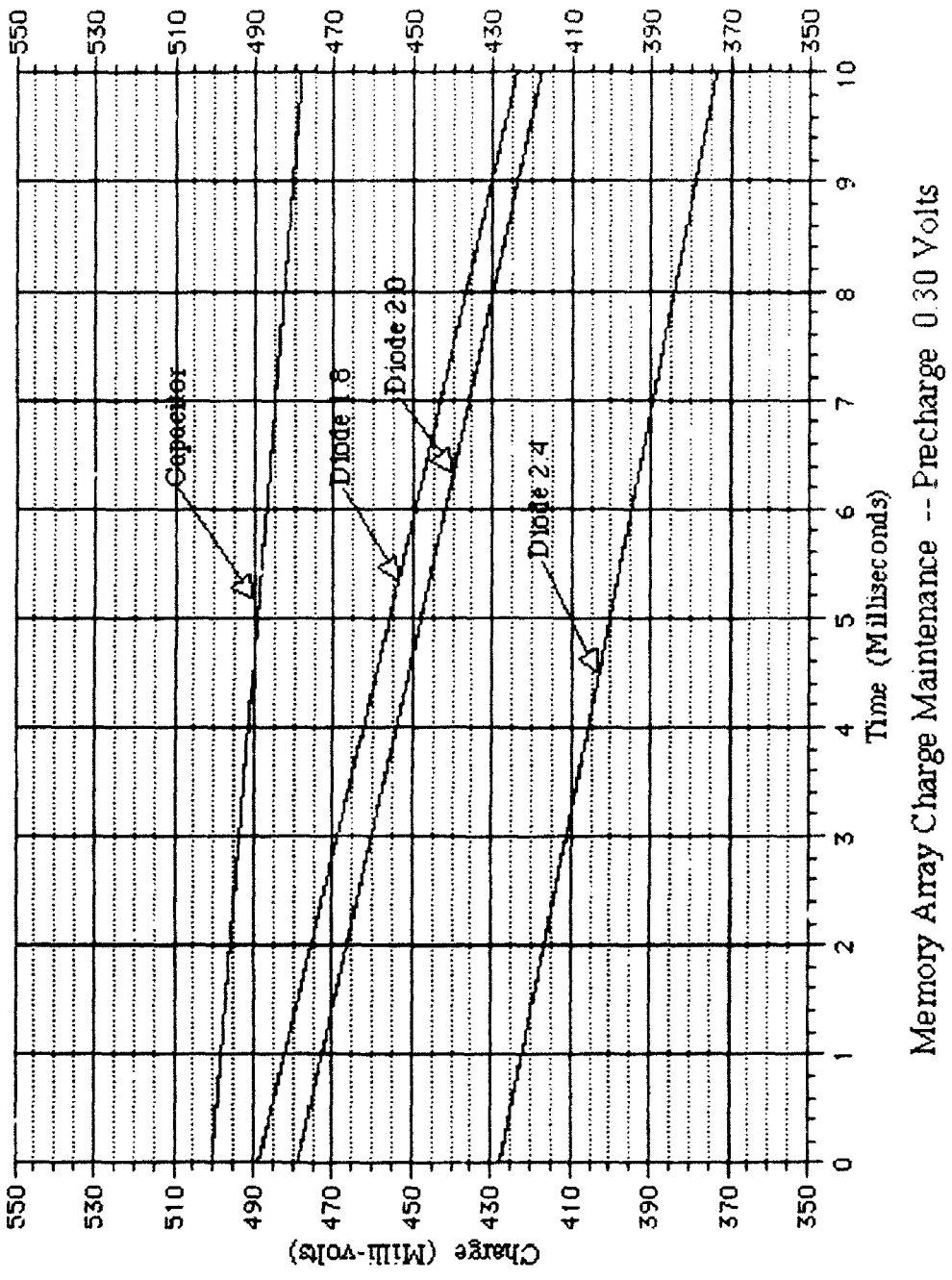

Memory Array Charge Maintenance -- Precharge 0.30 Volts
Charge (Milli-volts)
Time (Milliseconds)
Capacitor
Diode 1.8
Diode 2.0
Diode 2.4
550
530
510
490
470
450
430
410
390
370
350
0
1
2
3
4
5
6
7
8
9
10

Figure C4

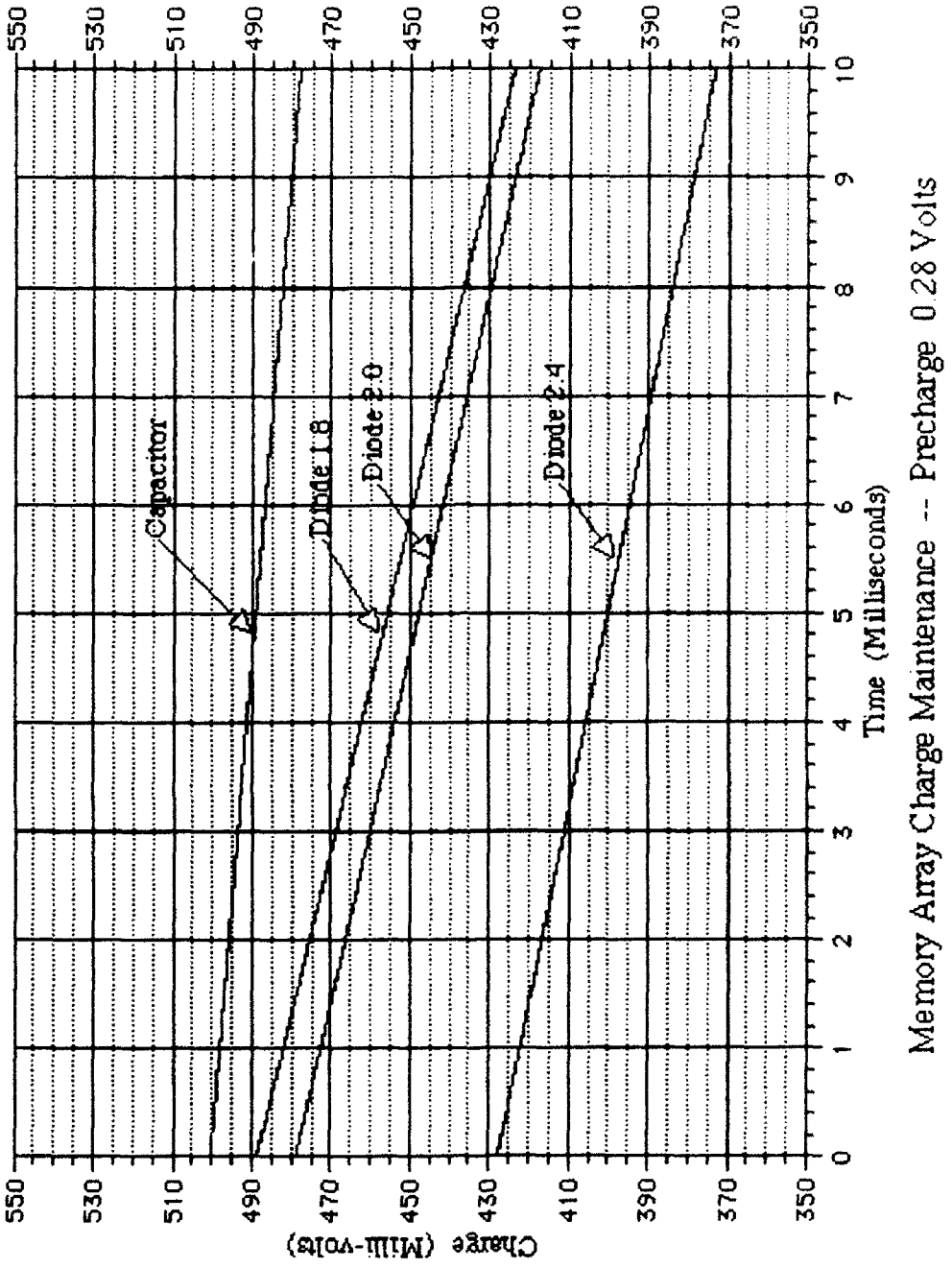

Memory Array Charge Maintenance -- Precharge 0.28 Volts
Charge (Milli-volts)
Time (Milliseconds)
Capacitor
Diode 1.8
Diode 2.0
Diode 2.4
550
530
510
490
470
450
430
410
390
370
350
0
1
2
3
4
5
6
7
8
9
10

Figure C5

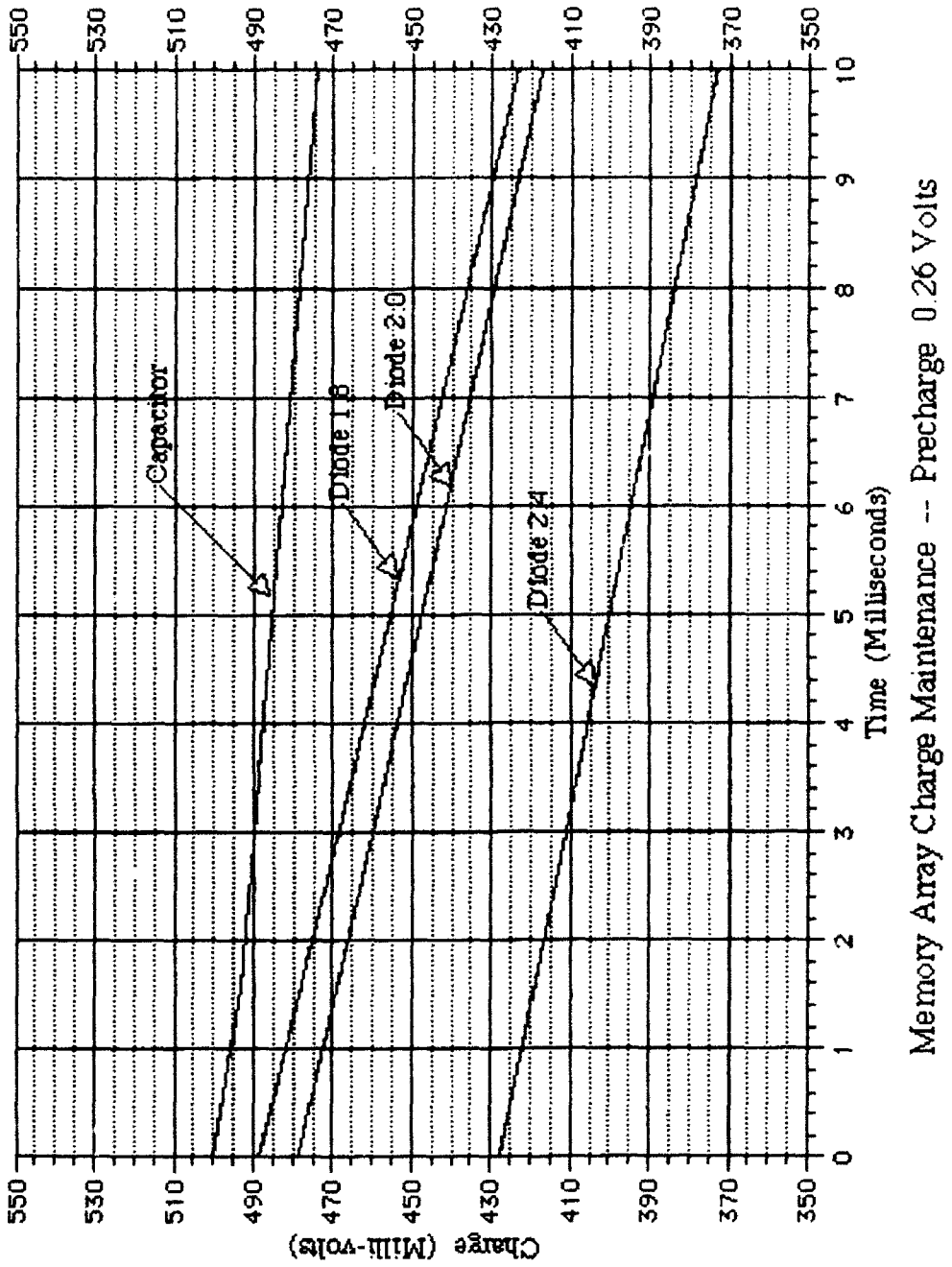

Memory Array Charge Maintenance -- Precharge 0.26 Volts
Charge (Milli-volts)
Time (Milliseconds)
Capacitor
Diode 1.8
Diode 2.0
Diode 2.4
550
530
510
490
470
450
430
410
390
370
350
0
1
2
3
4
5
6
7
8
9
10

Figure C6

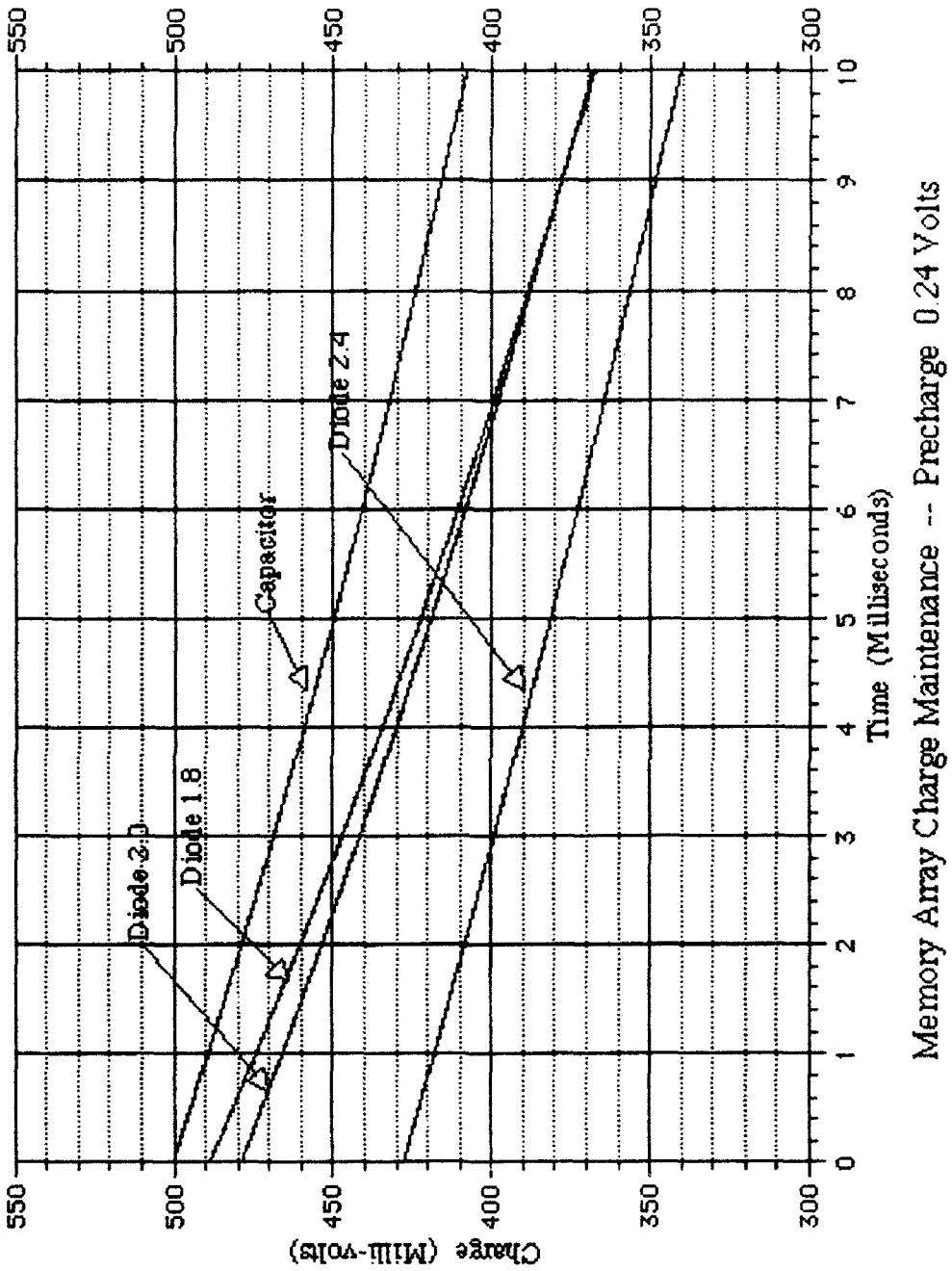
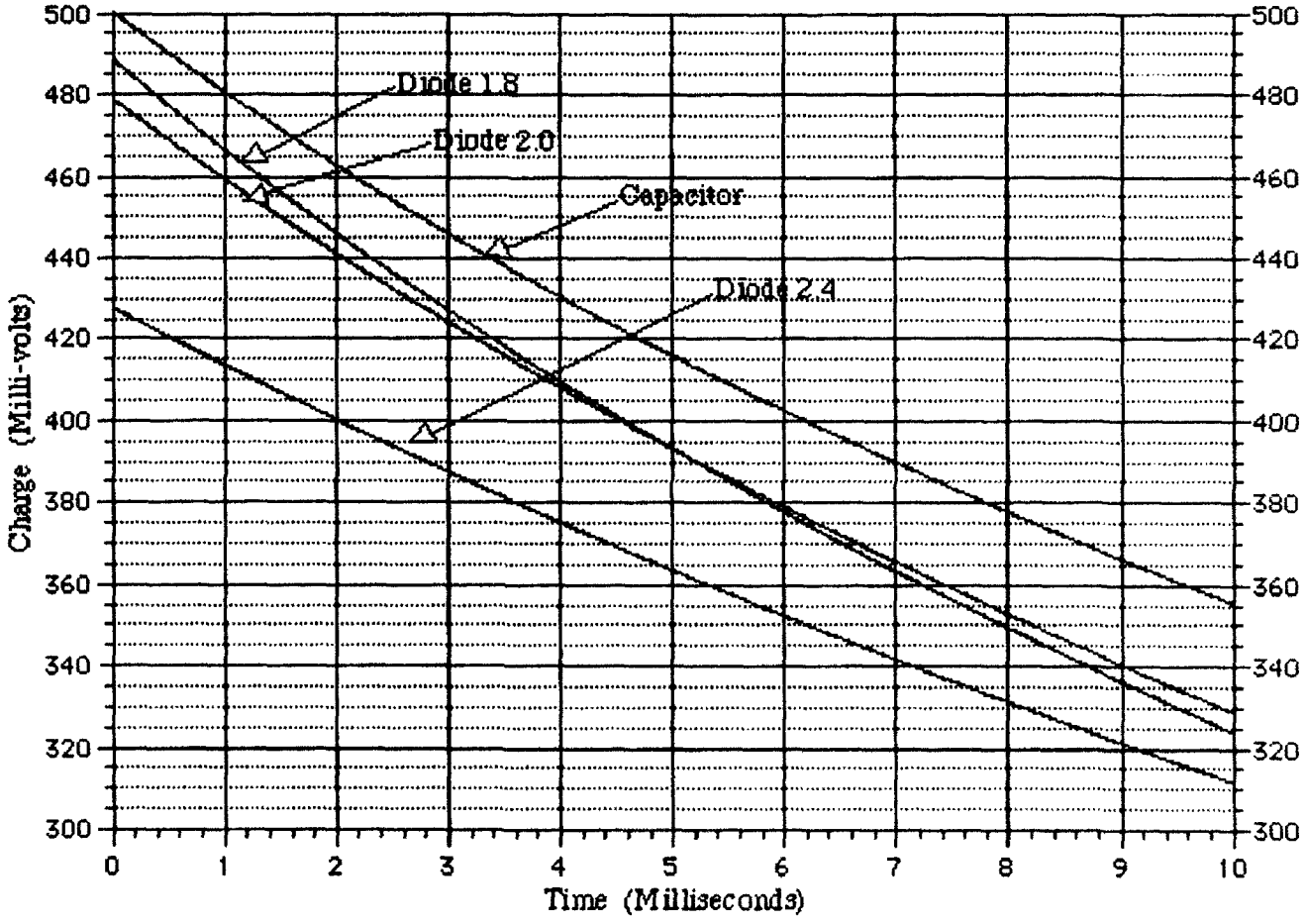

Memory Array Charge Maintenance -- Precharge 0.24 Volts
Charge (Milli-volts)
Time (Milliseconds)
Diode 2.4
Capacitor
Diode 1.8
Diode 2.0
550
500
450
400
350
300
0
1
2
3
4
5
6
7
8
9
10

Figure C7



Memory Array Charge Maintenance -- Precharge 0.22 Volts

Figure C8

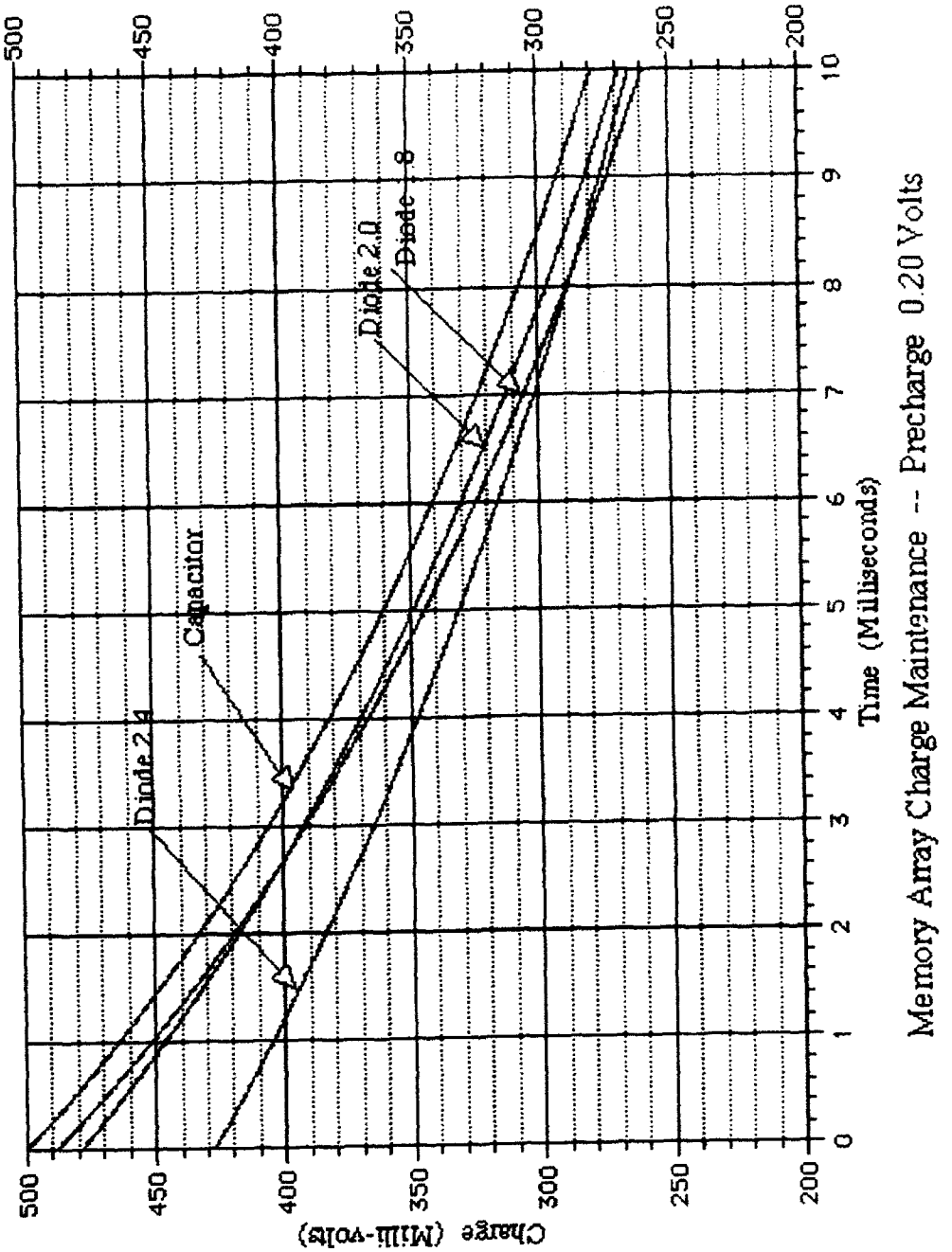

Memory Array Charge Maintenance -- Precharge 0.20 Volts
Charge (Milli-volts)
Time (Milliseconds)
Capacitor
Diode 2.4
Diode 2.0
Diode 8
500
450
400
350
300
250
200
0
1
2
3
4
5
6
7
8
9
10

Figure C9

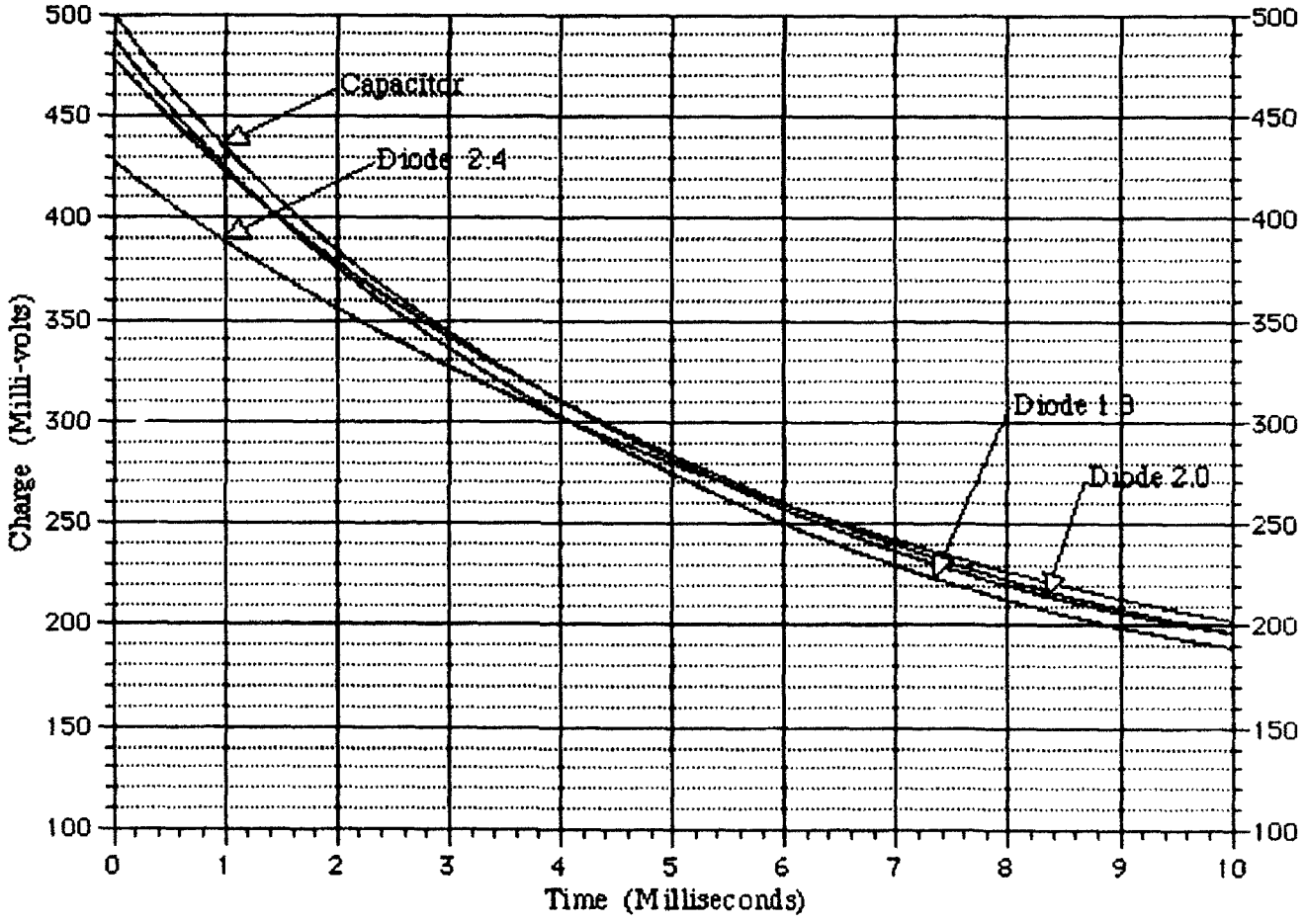


Figure C10

Memory Array Charge Maintenance -- Precharge 0.18 Volts

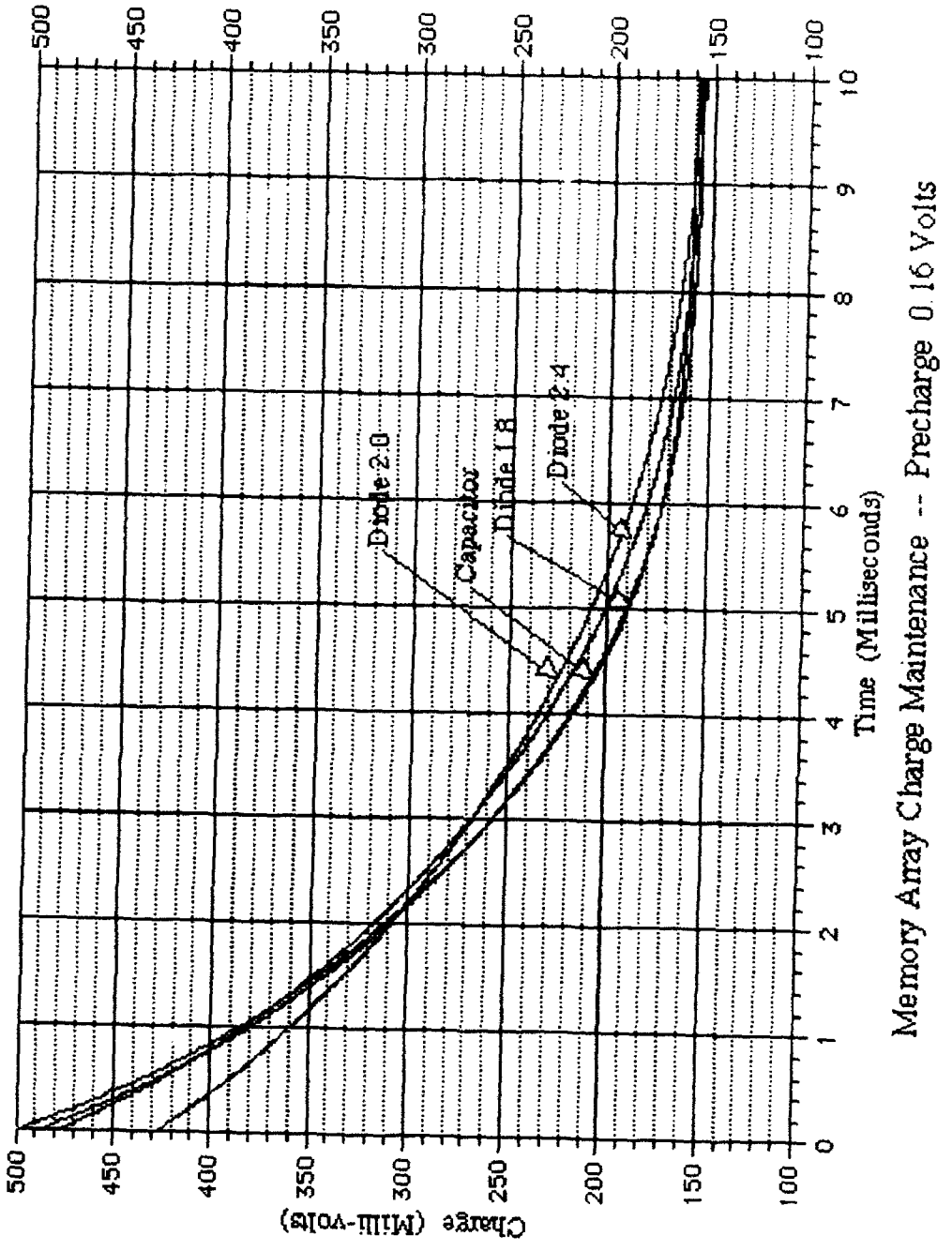

Memory Array Charge Maintenance -- Precharge 0.16 Volts
Charge (Milli-volts)
Time (Milliseconds)
Diode 2.0
Capacitor
Diode 1.8
Diode 2.4
500
450
400
350
300
250
200
150
100
0
1
2
3
4
5
6
7
8
9
10

Figure C11

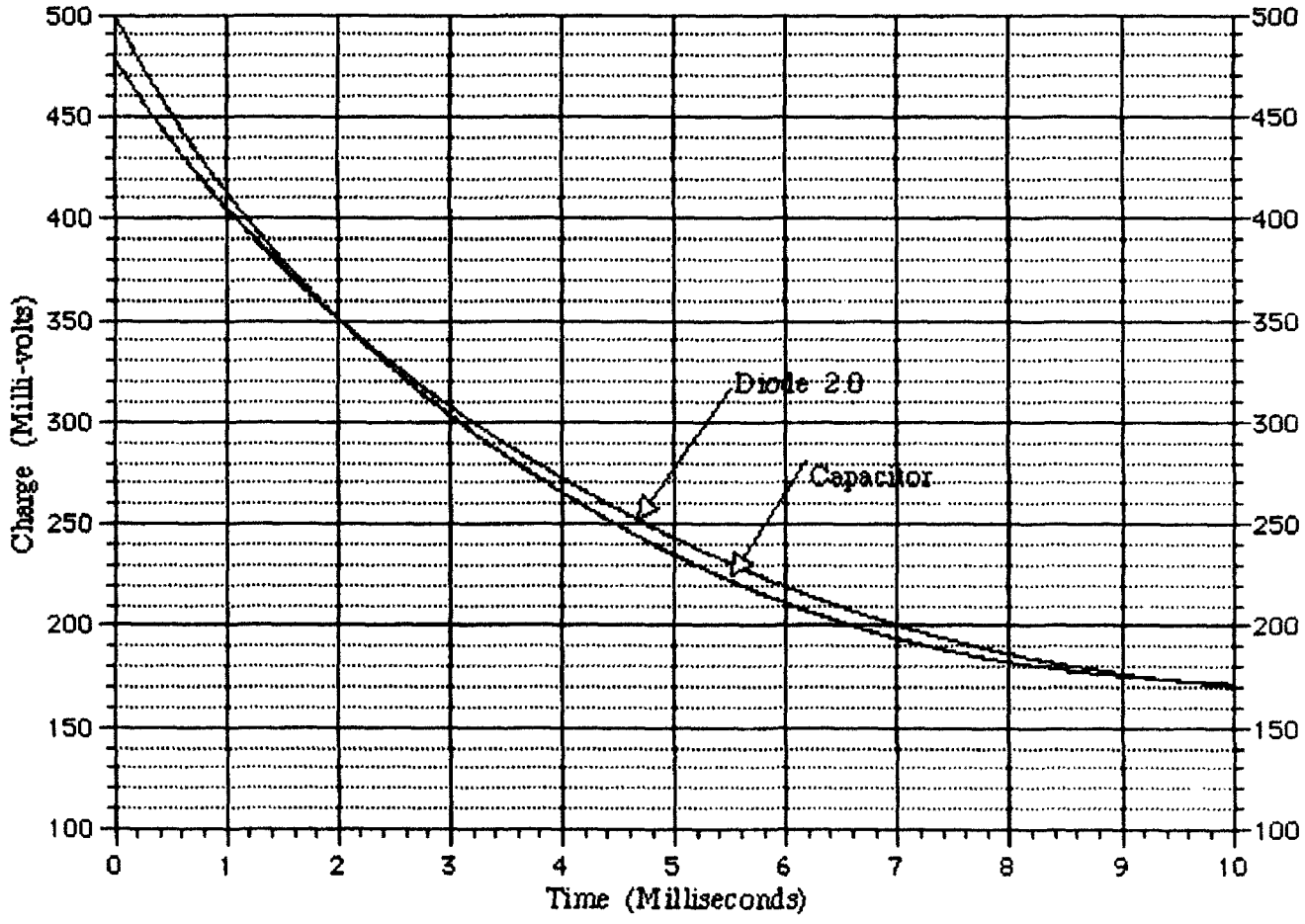


Figure C12

Memory Array Charge Maintenance -- Precharge 0.17 Volts

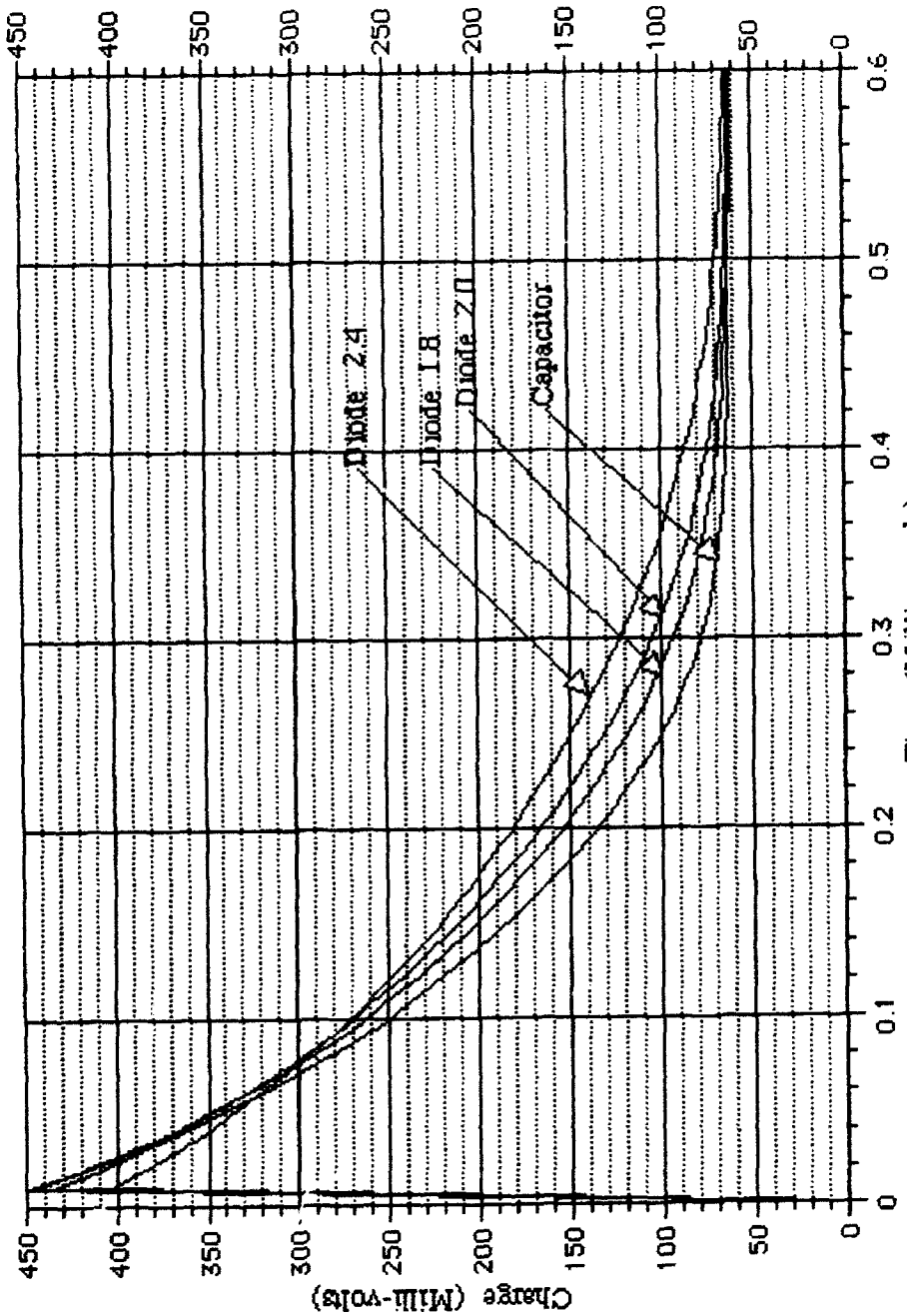

Memory Array Charge Maintenance – No Precharge
Charge (Milli-volts)
Time (Milliseconds)
Diode 2:4
Diode 1:8
Diode 2:0
Capacitor
450
400
350
300
250
200
150
100
50
0
0.1
0.2
0.3
0.4
0.5
0.6

Figure C13

APPENDIX D

POWER CONSIDERATIONS

This appendix contains the three graphs of the total power consumed by the memory array for Writing and Reading ONES and ZEROS. Figure D1 is the Write and Read of a ONE. Due to the Pullup Transistors, the power consumed during a write is three times the power consumed during a Read. Figure D2 adds the total power for Writing and Reading a ZERO. The power consumed for writing and reading a ZERO is the same as the power consumed during a Read of a ONE. Figure D3 includes the power drawn by a diode for the Write and Read of a ONE. Note that the power levels are basically the same for a diode as for a capacitor.

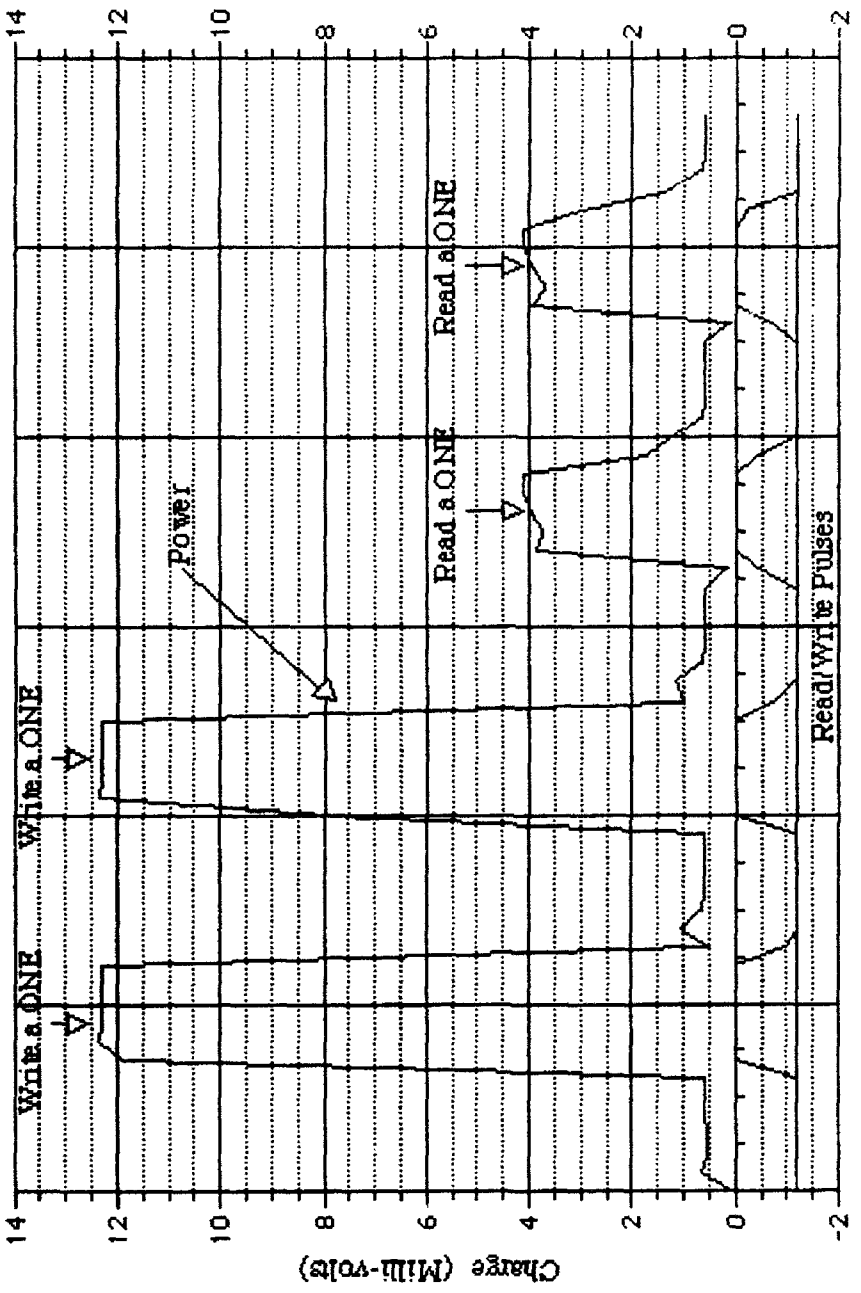

Write a ONE
Write a ONE
Power
Read a ONE
Read a ONE
Read/Write Pulses
Charge (Milli-volts)
Time (Nanoseconds)
Waveforms Total Power for Memory Array
Write and Read ONES

Figure D1

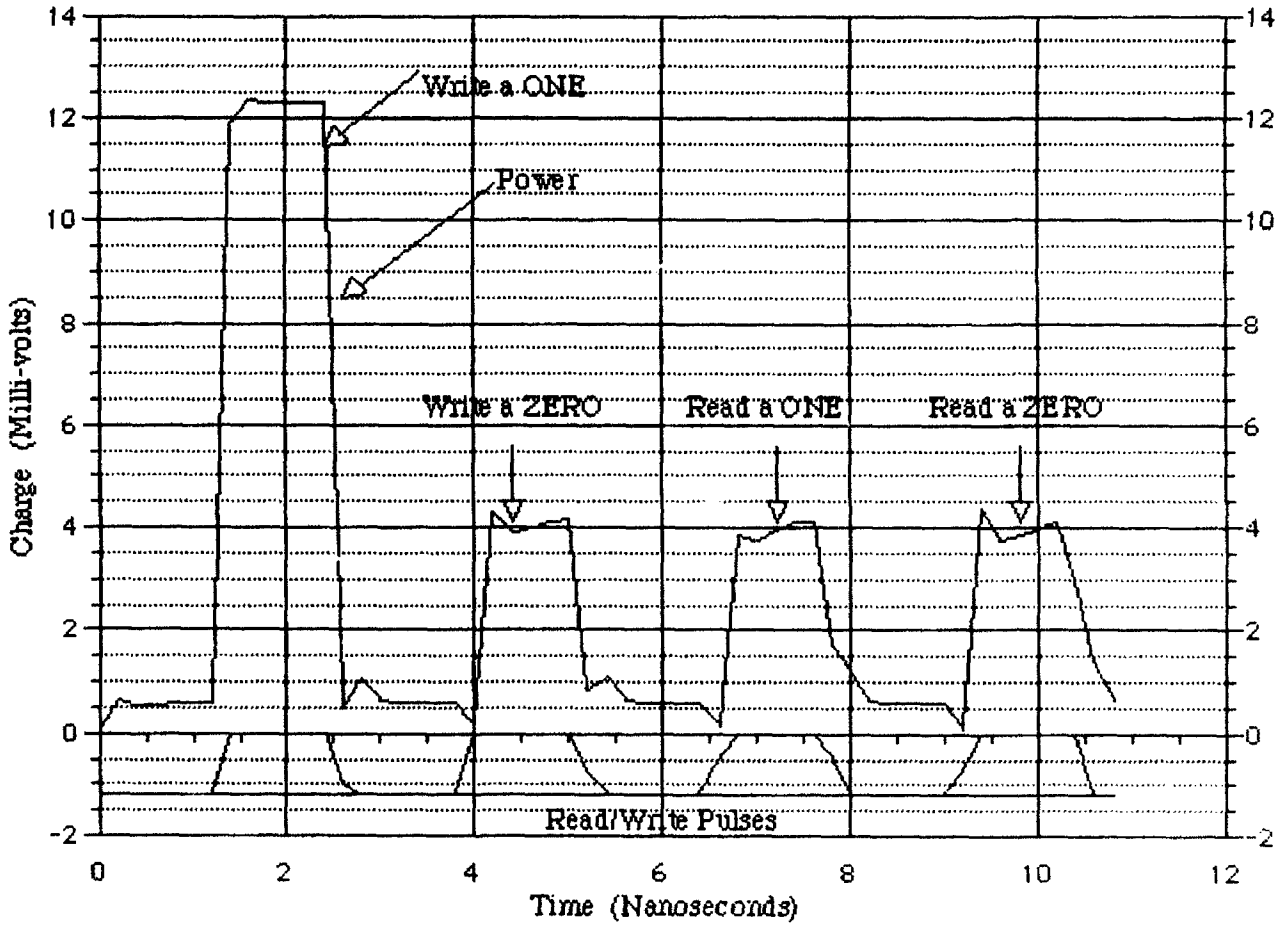


Figure D2

Waveforms -- Total Power for Memory Array
Write and Read ONES and ZEROS

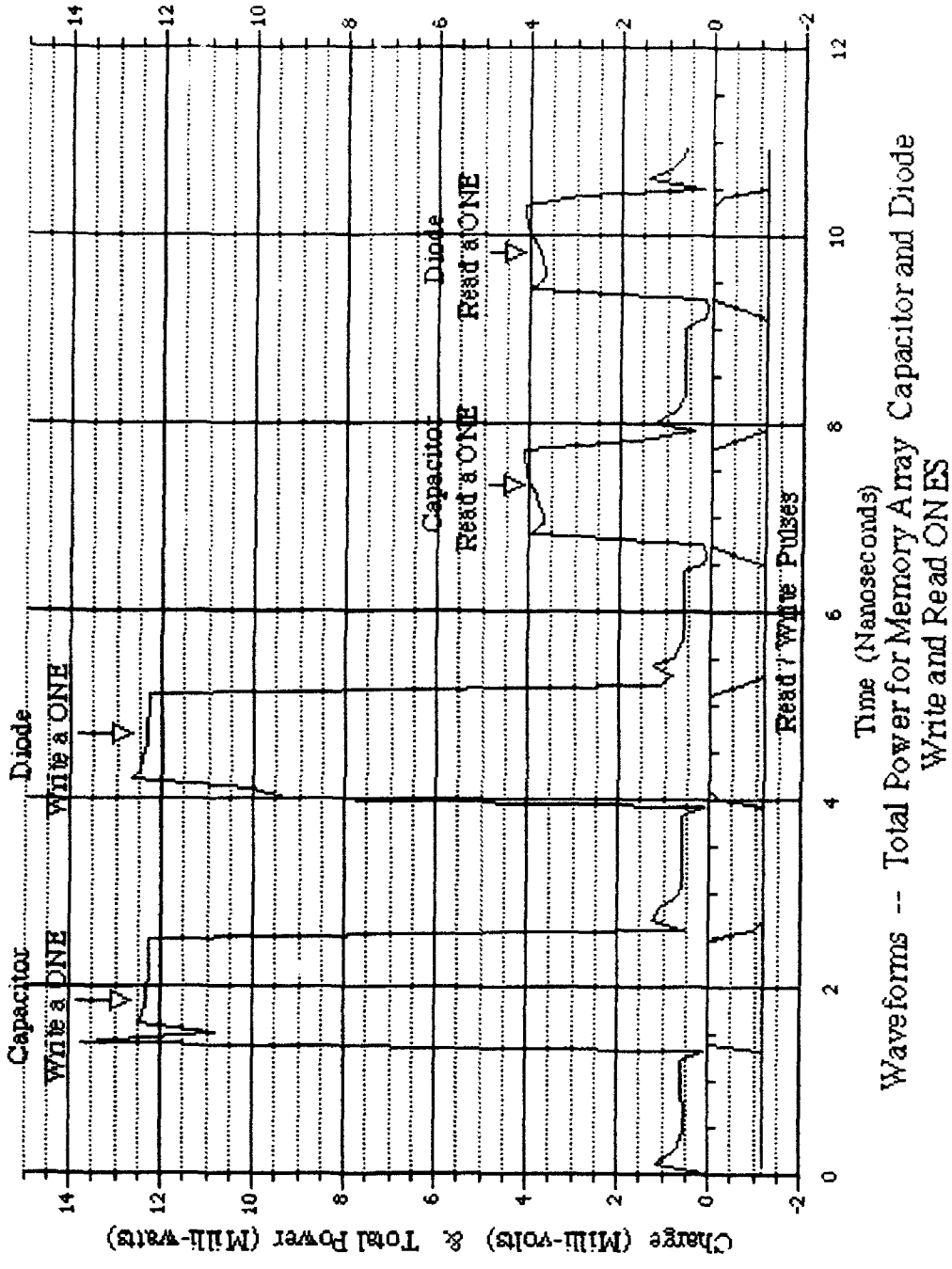

Capacitor
Write a ONE
Diode
Write a ONE
Capacitor
Read a ONE
Diode
Read a ONE
Read / Write Pulses
Charge (Milli-volts) & Total Power (Milli-watts)
Time (Nanoseconds)
Waveforms -- Total Power for Memory Array Capacitor and Diode
Write and Read ONES

Figure D3

LIST OF REFERENCES

1. Fouts, Douglas J., "Gallium Arsenide Digital IC Design," paper presented to Advanced VLSI Design Class, Naval Postgraduate School, Monterey, California, 10 February 1992.

2. Long, S. L., and Butner, S. E., *Gallium Arsenide Digital Integrated Circuit Design*, pp. 79-139, McGraw-Hill Publishing Co.,1990.

3. Kuo, C., Kitagawa, E. W., Drayer, P., "Sense Amplifier Design is Key to 1-Transistor Cell in 4,096-bit RAM," *Memory Design: Microcomputers to Mainframes*, pp. 91-96, McGraw-Hill Publishing Co., 1978.

4. Morris, Michael A., *Gallium Arsenide Dynamic Random Access Memory Array Support Circuitry*, Master's Thesis, Naval Postgraduate School, Monterey, California, March 1993.

5. *Gallium Arsenide Foundry Design Course Notes*, Vitesse Semiconductor Corporation, Camarillo, California, July 1987.

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