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DEVELOPMENT AND TESTING OF THE DIGITAL CONTROL SYSTEM FOR THE ARCHYTAS UNMANNED AIR VEHICLE

by

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December 1992

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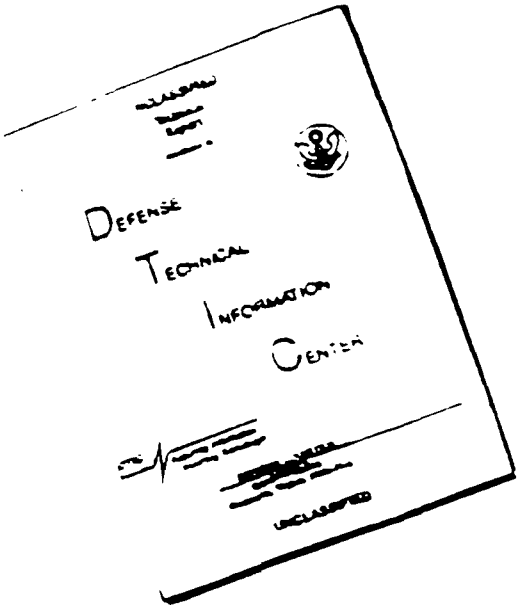

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The thesis effort includes the following four parts:

- Design of a controllable Pulse-Width-Modulated signal to command the servos which operates various aerodynamic surfaces. This control is accomplished with software written to a counter/timer card installed in the computer.
- Sampling and conversion of the signals to the sensors through the programming of an analog-to-digital card installed in the computer.
- Sensor Power-up and parameter verification of onboard devices.
- Development of various power networds to allow operation of onboard systems prior to engine start with the ability to be self-sustaining once the engine is running.

The system was fully tested during ground runs on a thrust/torque test stand. Integration of the system with the robust controller designed in a concurrent thesis will provide for the stability necessary for the innovative unmanned vehicle.

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by

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ABSTRACT

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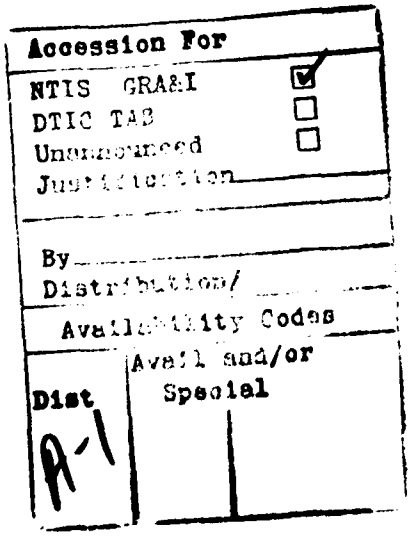


TABLE OF CONTENTS

I. INTRODUCTION

During Operation Desert Storm it did not take long for commanders of ground and Naval forces to realize the utility of intelligence gathering through the use of Remotely Piloted Vehicles (RPV). The current RPV Pioneer allowed for real-time data gathering without risk to human life. The use of RPV's allowed Marines and Naval forces alike to become self-supporting integrated platforms.

Even with the success of Pioneer in the Gulf War, there still lies room for improvement in the current system. It was noted that once the ground offensive began, Pioneer had trouble keeping pace with the rapid ground movement. A major problem with the system was the large amount of equipment and groomed runway needed for the land-based Pioneer. Due to these shortfalls, Pioneer provided little benefit during a time when it could have been irreplaceable as a real-time intelligence gatherer, or spotter for Naval and Marine gunfire.

An Unmanned Air Vehicle (UAV) based on a Vertical-Takeoff-and-Landing (VTOL) configuration could potentially help to solve many of the current UAV shortcomings. One candidate for such a platform is a ducted-fan airframe with wings attached. The advantage of the ducted-fan configuration is that it provides safety from propeller blades for close operation to ground troops. Positioning the duct and wings vertically would allow the vehicle to take off vertically, hover to

altitude and then pitch over to achieve horizontal flight. This concept has the advantage of needing limited space for takeoff and landing. Additionally, the ability to transition to horizontal flight will extend the vehicle's range, and allow faster dash speeds than for a vehicle that translates like a helicopter. The reduced fuel consumption of a fixed-wing over a hovering vehicle will allow for longer loitering periods once the air vehicle is on station. Such a platform is being developed at the Naval Postgraduate School (NPS), named Archytas.

NPS will determine:

- The proper propulsion and aerodynamic design to vertically lift the vehicle;
- The necessary stability augmentation system to control the vehicle in vertical flight;
- The optimum maneuver for transitioning the vehicle from a vertical hover to horizontal flight; and
- The necessary ground control needed to provide commanded input to the vehicle while hovering and in horizontal flight.

The goal of this work was to develop the digital sampled data control system for a VTOL UAV. The integrated system will interface a ground computer with onboard systems to allow for inputs from the onboard sensors to be sampled through the umbilical and converted to a digital signal by the computer. These digitized signals can then be applied to control the vehicle's pitch, yaw and roll

rates [Ref 1]. The control equations will generate commands that will be sent to the control vanes on the vehicle to adjust the vehicle's attitude.

This investigation examined:

- The development of a computer-generated Pulse-Width-Modulated Signal (PWMS) to command five servos through an umbilical. The signal commands the throttle and the position of four control surfaces on the vehicle.
- The development of a system to sample the signals from onboard sensors and convert them to 12-bit digitized form.
- A power system to allow all the electronics to operate prior to, and after the engines generator is up and running.
- The design of the vehicle hardware components to include the umbilical and associated connections, housing and power system and all associated wiring.

The results support the effort to digitally control a VTOL UAV in a hover. Follow-on projects will perform the integration of vehicle control for forward flight, and miniaturization of the computer for autonomous flight.

II. BACKGROUND

A. NAVY UAV APPLICATIONS AND REQUIREMENTS

The Navy's Unmanned Air Vehicle (UAV) program currently lacks an adequate vehicle that will take off in a small area and yet have a long loiter time to conduct operations once on station. The Navy has defined a need for a vehicle that will take off vertically and conduct extended reconnaissance. The concept designated as VIPER (Vertical Takeoff and Landing Integrated Platform for Extended Reconnaissance) whose specifications are described in Reference 2 call for a vehicle able to land and takeoff in an area smaller than a LAMPS flight deck. The requirements of VIPER also state that it should be able to transit 100nm from the ship in a 25-knot headwind in less than one hour and be able to loiter on station for three hours. The primary missions of the vehicle would be for Reconnaissance, Surveillance and Target Acquisition (RSTA) and Over-The-Horizon-Classification-and-Targeting (OTH-C&T). The ideal vehicle should be highly portable, have a small operations contingency, and be able to operate ashore as well as at sea.

At the Naval Postgraduate School UAV Flight Research Lab, the Navy has been developing a ducted-fan VTOL vehicle. This vehicle could be a proof of

concept vehicle to meet the requirements of VIPER or accomplish similar missions. The vehicle will encompass all the personnel safety qualities of a shrouded propeller with the dash and loiter advantages of a fixed-wing vehicle.

B. THE ARCHYTAS CONCEPT

The NPS air vehicle Archytas, named for the Greek contemporary of Plato credited with designing and flying a mechanical bird, is serving as a platform to test the concepts of a winged ducted-fan VTOL aircraft. The vehicle utilizes the technology and equipment developed in two cancelled military programs to produce a quality experimental test platform. The U.S. Marine Corps program produced the Airborne Remotely Operated Device (AROD), and the U.S. Army program developed the AQUILA (Latin for eagle). Both programs, though successful in their original missions, were cancelled, providing assets for development of new programs.

1. AROD Program

The major parts of the Archytas have come from the AROD program, the vehicle which was designed by Sandia Laboratories in conjunction with the Naval Ocean Systems Center [Ref 3]. The AROD was originally designed to be a short-ranged hovering vehicle. The vehicle was designed to be controlled by fiber optic link or remotely with a modified commercial modeler's radio. The

vehicle, which resembles a 3-ft-diameter duct, was powered with a vertically-mounted 28-horsepower engine turning a three-bladed propeller. Four vanes were positioned on the vehicle in the propwash to provide the ability to correct or change the attitude of the vehicle.

The use of a single propeller in a duct simplifies the design, but creates stability problems caused by the torque of the engine and by gyroscopic coupling of the pitch and yaw moments. This problem was overcome by Sandia with the development of a Multiple Input Multiple Output (MIMO) robust controller that utilized sensors coupled with a Motorola 68000 Central Processing Unit (CPU) to apply the devised control laws. The output from the CPU was converted into the necessary signal to position the vanes for the desired effects.

The AROD, weighing about 85 pounds and producing about 105 pounds of thrust, first flew successfully in 1986. Its endurance was limited to one hour due to the high power level needed for hovering. The vertical design and axial flow of the propwash limited the vehicle's forward speed.

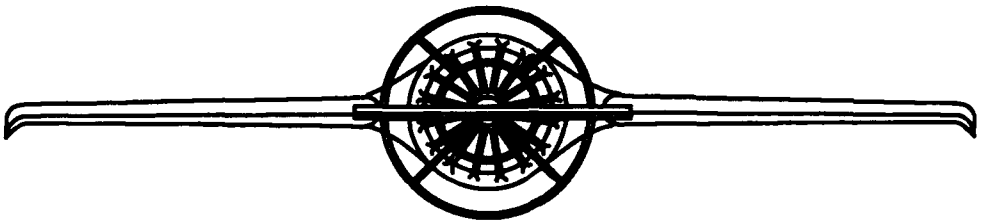
2. Aquila Program

The AQUILA, the vehicle that provides the wings for the Archytas,was an ARMY-developed UAV designed by Lockheed [Ref 3] as a mid-range fixed-wing tailless pusher platform. The airframe is a composite structure with a 13-foot wing span and length of 7 feet. The vehicle was powered by a horizontally-

mounted 24-horsepower engine. The vehicle wing elevons (acting as elevators and ailerons) were the primary surfaces to control the vehicle in flight. The AQUILA needed a sophisticated dedicated flight control electronics package to provide control and stability.

The design of the Archytas has taken the AQUILA wings and attached them to the duct used in the AROD program. It was also necessary to add a canard to provide an improved means of longitudinal control. The duct and wings will be vertically oriented as a tail-sitting airplane. The vehicle will be designed to hover to a determined altitude while the controller commands the four control vanes that will maintain pitch, yaw, and roll rates. Once at altitude the vehicle will then roll over to horizontal flight which will allow for an increased forward speed and an improved endurance. A sketch of the vehicle is shown in Figure 1.

TOP VIEW



SIDE VIEW

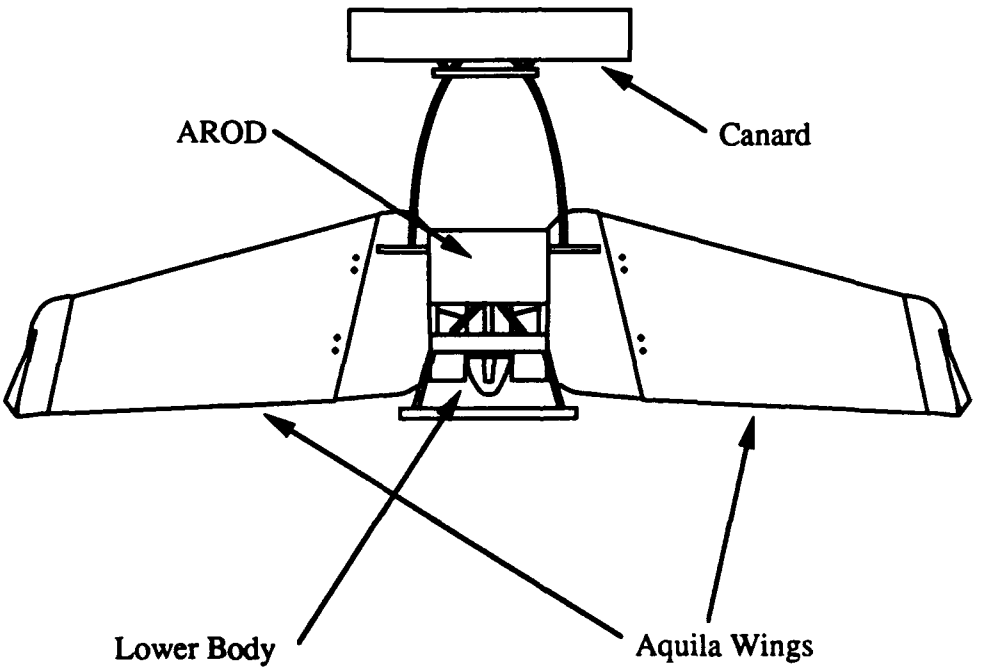


Figure 1: Sketch of Archytas

III. THE DIGITAL CONTROL INTERFACE SYSTEM

A. SYSTEM OVERVIEW

The instability of the Archytas vehicle requires a computer controller to control pitch, roll and yaw motion. A digital controller requires input from onboard sensors, and the ability to command a surface to generate the desired response. The original AROD computer, a Motorola 68000 CPU, provided the controller and interface functions. This system was not used because it was outdated and it would have been difficult to find interfacing equipment for it. With this in mind, it then became necessary to develop a new interface system.

The flexibility and low cost of personal computers made it desirable to develop the system centered around an IBM personal computer. The initial testing of Archytas will involve the vehicle in a hover. This means the vehicle can be ground linked to a personal computer through an umbilical. The umbilical will allow the computer to sample and evaluate the sensor data. After the sensors' data is evaluated, the computer can then send a command for vane angle through the umbilical to one or more of the four control vanes. The umbilical link can also

be used to control the throttle servo from the ground. Once this system is proven, the computer system can then be miniaturized to allow onboard placement.

Enabling the computer to complete its tasks required the addition of two special-function cards to the computer. The first card added (Diamond Systems Quartz I/O) generates the Pulse-Width-Modulated Signal (PWMS) to control the four control vanes and throttle. The Quartz card is a multi-purpose card with the AM9513A system timing controller as the main chip aboard the card. The chip has a versatile group of modes ranging A-X that are shown in the users manual. The card has five expandable to ten extremely versatile 16-bit counter groups. Each group of counters has a wide variety of features, including up/down counting by binary, or binary coded decimal, edge level gating, and a toggle output capability. The card has an internal series of frequencies derived from a 1 MHZ oscillator that can be exported. Additionally, the counter/timers can be used to generate retriggerable one-shots of varying duty length. A list of the card's specifications and a pin diagram for the output port can be found in the users manual.

The second card installed is the CIO-AD16jr card by Computerboards that provides sampling and analog-to-digital conversion. The card is a 16-channel open-ended input, or 8 differential input, card. Aboard the card is an 8254 chip that provides a versatile range of methods for triggering the conversion process.

The card converts from analog to digital by successive approximation with a conversion time of about 3 nanoseconds. A useful feature the card provides is the ability to vary the input through various ranges from a bipolar +/- 10V to a unipolar 0-1.25V.

The final systems to be engineered were the utility systems. These systems included the umbilical and power systems. The power system included voltage supply for the sensors, electronic ignition and a signal conditioning card. This system was difficult to design because of the diversity of each system. A major difficulty in the design of the power system was the need for it to fit compactly on the vehicle. Additionally, the various systems all needed to interface with each other as well as with the computer. A concern for the power system was the need to provide power to the various systems prior to the engine generator being up and running. A basic overview of the overall system is shown in Figure 2. Each of the basic systems SERVO CONTROL, ANALOG TO DIGITAL, and UTILITY SYSTEMS will be described in the following chapters.

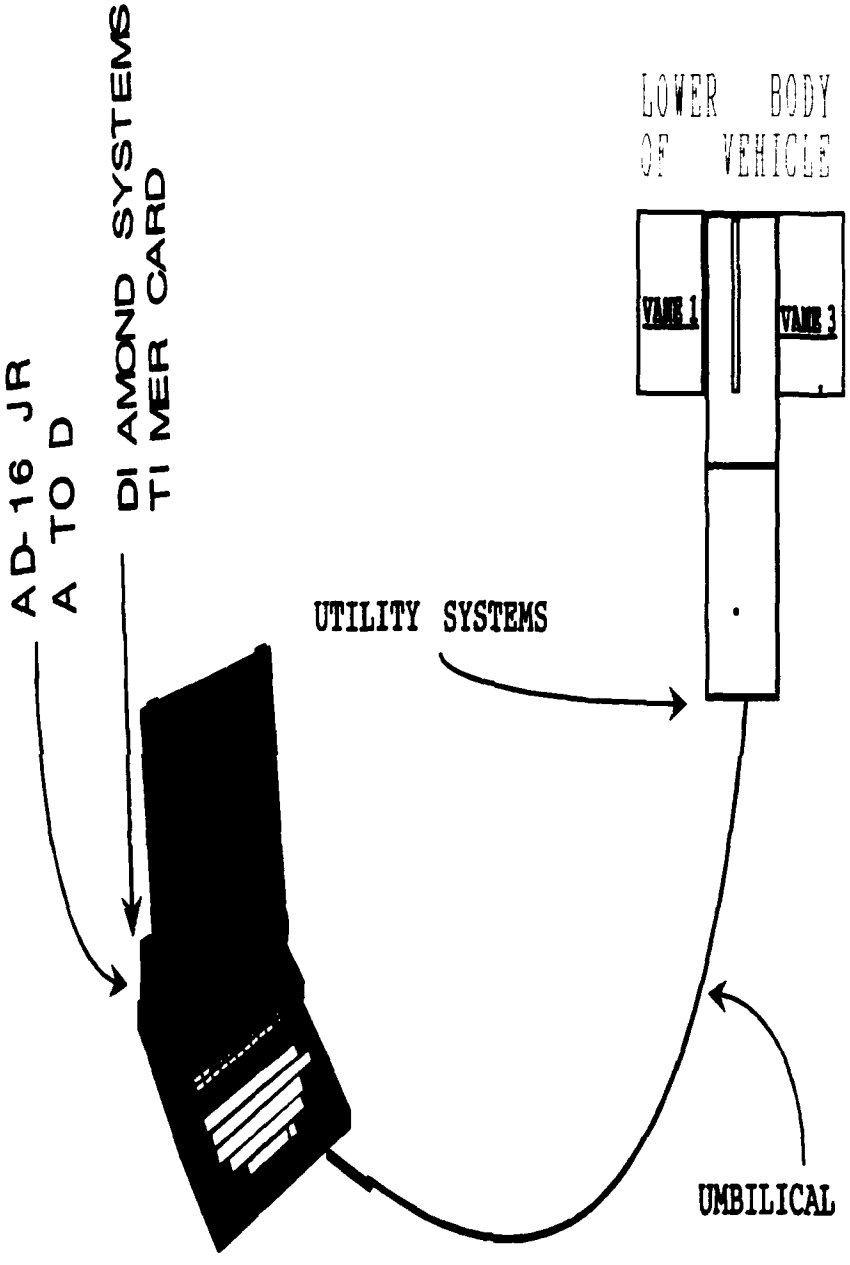


Figure 2: Basic Electrical System Design

IV. GENERATION OF THE SERVO CONTROL SIGNAL

A. GENERAL LAYOUT OF THE SERVO CONTROL AND QUARTZ I/O CARD

The digital controller needs the ability to command movement of the control surfaces on the vehicle. The original AROD design used Futaba S-134 servos to move each of the four control surfaces. These servos are general-purpose hobby remote-control items that cost about $40.00 each. The servos have three inputs: (1) 5 volts; (2) ground; and (3) a Pulse-Width-Modulated-Signal (PWMS). The 5-volt signal powers a small DC motor, and the small amount of Transistor Transistor Logic (TTL) onboard the device. A PWMS is characterized by a square wave whose duty cycle varies between 0.6 and 2.4 milliseconds. The width of the pulse drives the servo proportionally to the intended position. A narrow pulse of 0.6 milliseconds may drive the servo hard right, while a 1.0 millisecond pulse will drive the servo proportionally less right, and a 2.4 millisecond pulse may drive the servo hard left. The servo PWMS is refreshed every 10 milliseconds. The addition of the Diamond System Quartz I/O card to the PC provided the ability to create the PWMS to command the servos. Figure 3 shows a typical PWMS. The user's manual for the Quartz I/O card was

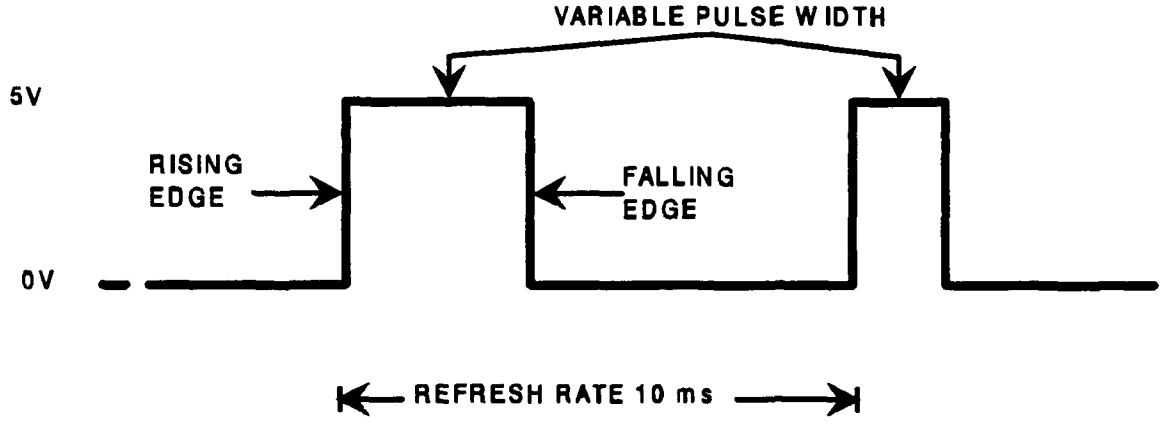


Figure 3: Pulse Width Modulated Signal (PWMS)

written with the intention of the card being used in conjunction with proprietor software written in Basic or C. This documentation was not adequate, or useful in the generation of the desired PWMS. This is mainly because the modes (A-X) set up count on a "CALL" to a routine that is only provided in object code. This "CALL" to a subroutine is not explained in the card's documentation, making it difficult to understand exactly what is being done. Additionally, the C programs are only compatible with Microsoft C, not with Borland C. Since the "CALL" routine was not provided, it was necessary to register-level program the desired mode into the AM9513A, the onboard system timing controller chip. The data sheet for the AM9513A chip is included in the manual. The data sheet allowed the card to be programmed at register level to obtain the desired output. All of the programming was done in Borland C to provide a robust environment for later use.

To allow the PC to interface with the card, the first step is to set the BASE ADDRESS dip switches to a non-interfering address that the C programs will interface with. For this application the BASE ADDRESS 225 hex was set on the onboard dip switches. The location of the dip switches on the card is shown in users manual. This selects the base address of the port the program will write to, or read from. The card is read and written to at one of three addresses which are each eight bits, or one byte wide. Table 1 describes each of the functions

associated with the base addresses and their offsets. The general layout of the AM9513A registers' access is shown in Figure 4.

The data bus multiplexor selects either the CONTROL PORT (BASE ADDRESS+1), or the DATA PORT (BASE ADDRESS), depending on which address the binary word is being written to. The CONTROL PORT determines which register incoming data will be loaded into to select the operating mode of the card. The card can be programmed in any mode chosen from those offered in the data sheet between modes A through X. The data sheet showed that programming mode F allowed generation of the desired PWMS.

TABLE 1: QUARTZ CARD INPUT/OUTPUT MAP

OFFSET FROM BASE ADDRESS	WRITE	READ
0	9513 #1 DATA REGISTER	9513 #1 DATA REGISTER
1	9513 #1 CONTROL REGISTER	9513 #1 STATUS REGISTER
2	INTERRUPT ENABLE	DIGITAL INPUT PORT AND INTERRUPT RESET
3	DIGITAL OUTPUT PORT	NO FUNCTION
4*	9513 #2 DATA REGISTER	9513 #2 DATA REGISTER
5*	9513 #2 CONTROL REGISTER	9513 #2 STATUS REGISTER

* CHANNELS ARE ONLY USABLE IF CARD IS SET UP FOR 10 CHANNEL OPERATION BY ADDING THE SECOND AM9513A TO THE CARD. NPS CARD IS NOT SET UP FOR 10-CHANNEL OPERATION.

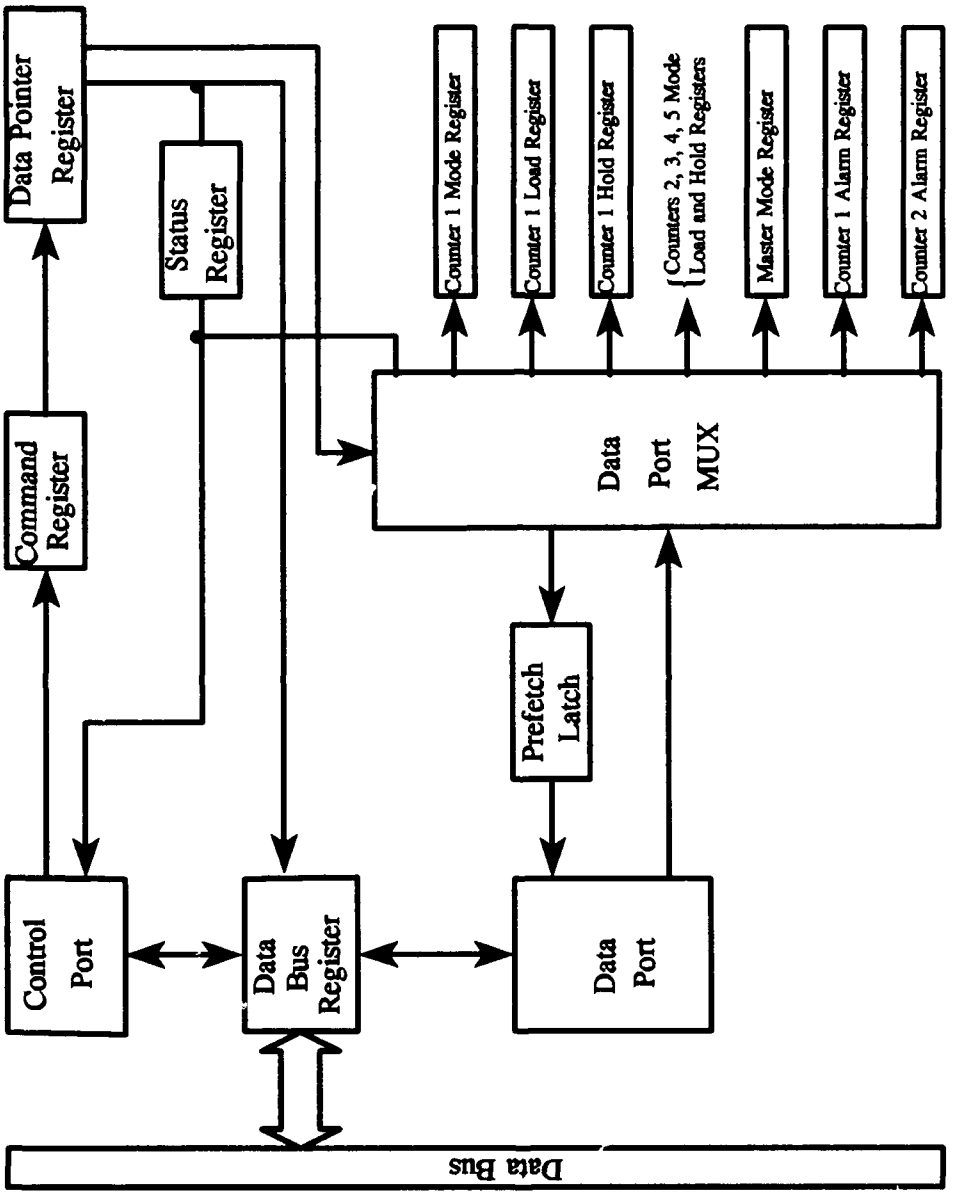


Figure 4: AM9513A Register Access

B. PROGRAMMING MODE F ON THE QUARTZ I/O CARD

1. Programming Overview

To enable the card to produce the desired PWMS, each of the five AM9513A counters is programmed for mode F. The programming is all done in Borland C. Borland C has a function called "outportb(address,command)" that outputs the 8-bit decimal number to the output port desired. To begin programming the card, the card must first be reset. Then the Master Mode Register (MMR) must be programmed to control the overall function of the card. Then each of the five counters must be programmed through each counter's Counter Mode Register (CMR). Each of the five counters has two additional multi-purpose registers that can be programmed, called LOAD and HOLD registers.

The LOAD and HOLD registers play key roles in the generation of the desired signal. The individual channel counter alternates in being loaded from its respective LOAD and HOLD registers. The HOLD register contains a number that when loaded in the counter counts down to zero and fires a one-shot high (5V) creating the 10 ms refresh rate of the signal. Once the hold register counts down, the counter is then toggled to be loaded with the number contained in the individual counters LOAD register. The signal is held high until the LOAD register count reaches zero, causing the one-shot to be reset (0V). The count in the LOAD REGISTER creates the desired pulse-width between 0.6-2.4ms. Varying the number

loaded in the LOAD register varies the pulse-width. When the LOAD register counts to zero the counter toggles and is loaded from the HOLD REGISTER beginning the count down till the signal will be refreshed again.

2. Detailed Programming of the Registers

Most register programming commands for the Quartz I/O card are two-part commands. The first command is loaded through the CONTROL PORT. It is an 8-bit command that generally points to the register to be loaded. The second command, a 16-bit command, is loaded in two 8-bit bytes through the DATA PORT, 8 bits at a time. Figure 5 shows the DATA POINTER register, which shows how to access every available register that will need to be loaded. Sending the appropriate decimal equivalent to the CONTROL PORT sets up the multiplexor to load the next DATA PORT entry into the appropriate register.

a. Programming the Master Mode Register (MMR)

The first step to program any mode in the card is to reset the card. Reset is accomplished by writing 255 (binary 11111111) to the CONTROL PORT (base address+1). This reset command is found in Figure 6.

The next step is to program the MMR. This is accomplished by writing 23 (binary 00010111), obtained from the DATA POINTER (Figure 5) register to the CONTROL PORT to select the MMR. Figure 7 shows all the possible selections of the MMR. Then the 16 bits of data are loaded into the MMR

8 bits at a time through the DATA PORT. The first 8-bit number 176 (binary 10110000) is loaded followed by the second 8-bit 65 (binary 01000001). This bit assignment selects the MMR (Figure 7) to operate in the manner described in Table 2. Most of the selections in the MMR are arbitrary and have little effect on the PWMS, but do need to be specified for operation of the card.

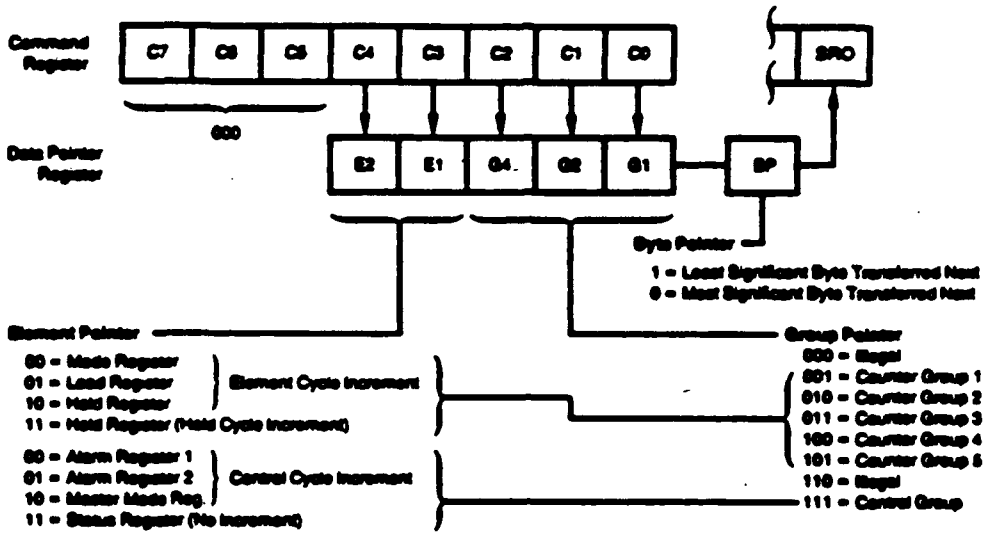


Figure 5: Data Pointer Register

TABLE 2: BIT ASSIGNMENT FOR MASTER MODE REGISTER

BIT ASSIGNMENT	BITS	FUNCTION
MM15,MM14,MM13,MM12	1011	BCD DIV,DISABLE INCR, 8BITBUS, FOUT ON
MM11,MM10,MM9,MM8	0000	FOUT IS DIVIDED BY 16
MM7,MM6,MM5,MM4	0100	FOUT SOURCE IS F1 1 MHZ (FIGURE 8)
MM3,MM2,MM1,MM0	0001	DISABLE COMPARE 1 AND 2 DISABLE TIME OF DAY

Command Code								Command Description
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	E2	E1	G4	G2	G1	Load Data Pointer register with contents of E and G fields. (E = 000, G = 110)
0	0	1	S5	S4	S3	S2	S1	Arm counting for all selected counters
0	1	0	S5	S4	S3	S2	S1	Load contents of specified source into all selected counters
0	1	1	S5	S4	S3	S2	S1	Load and Arm all selected counters*
1	0	0	S5	S4	S3	S2	S1	Disarm and Save all selected counters
1	0	1	S5	S4	S3	S2	S1	Save all selected counters in Hold register
1	1	0	S5	S4	S3	S2	S1	Disarm all selected counters
1	1	1*	0	1	N4	N2	N1	Set Toggle out (HIGH) for counter N (001 ≤ N ≤ 101)
1	1	1	0	0	N4	N2	N1	Clear Toggle out (LOW) for counter N (001 ≤ N ≤ 101)
1	1	1	1	0	N4	N2	N1	Step counter N (001 ≤ N ≤ 101)
1	1	1	0	1	0	0	0	Set MM14 (Disable Data Pointer Sequencing)
1	1	1	0	1	1	1	0	Set MM12 (Gate off FOUT)
1	1	1	0	1	1	1	1	Set MM13 (Enter 16-bit bus mode)
1	1	1	0	0	0	0	0	Clear MM14 (Enable Data Pointer Sequencing)
1	1	1	0	0	1	1	0	Clear MM12 (Gate on FOUT)
1	1	1	0	0	1	1	1	Clear MM13 (Enter 8-bit bus mode)
1	1	1	1	1	0	0	0	Enable Prefetch for Write operations (Am9513A only)
1	1	1	1	1	0	0	1	Disable Prefetch for Write operations (Am9513A only)
1	1	1	1	1	1	1	1	Master reset

Figure 6: AM9513A Command Summary Sheet

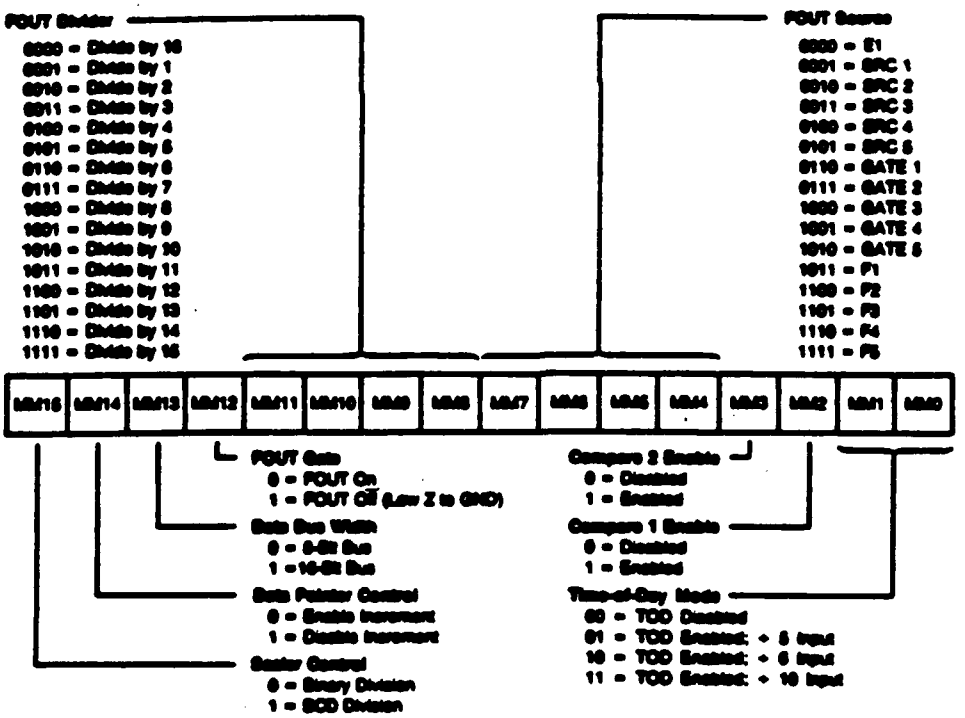


Figure 7: Master Mode Register Bit Assignment

b. Programming of the Counter Mode Register (CMR)

The Quartz I/O card and in particular the AM9513A Integrated Circuit (I.C.) has five programmable counters. The Archytas vehicle needs all five counters to output the needed PWMS. Counters one through four output the PWMS that control the servos that change the vane positions. Channel five outputs the PWMS that controls the servo for throttle movement on the engine. Therefore, all five CMR need to be programmed the same, and are done successively. Loading a 1-5 to the DATA POINTER register (Figure 5) through the CONTROL PORT selects any of the five CMR. The following example illustrates the process for loading counter one; the other four are done in the same manner.

The first step in programming CMR one is to load a one (binary 00000001) in the CONTROL PORT to select counter one CMR. The next step is to load the low and high bytes into the CMR via the DATA PORT. The low byte loaded is 98 (binary 01100010), and 27 (binary 00011011) is the high byte loaded. The bit assignment list shown in Figure 8 and Table 3 show the CMR bit assignment causing various important actions to occur.

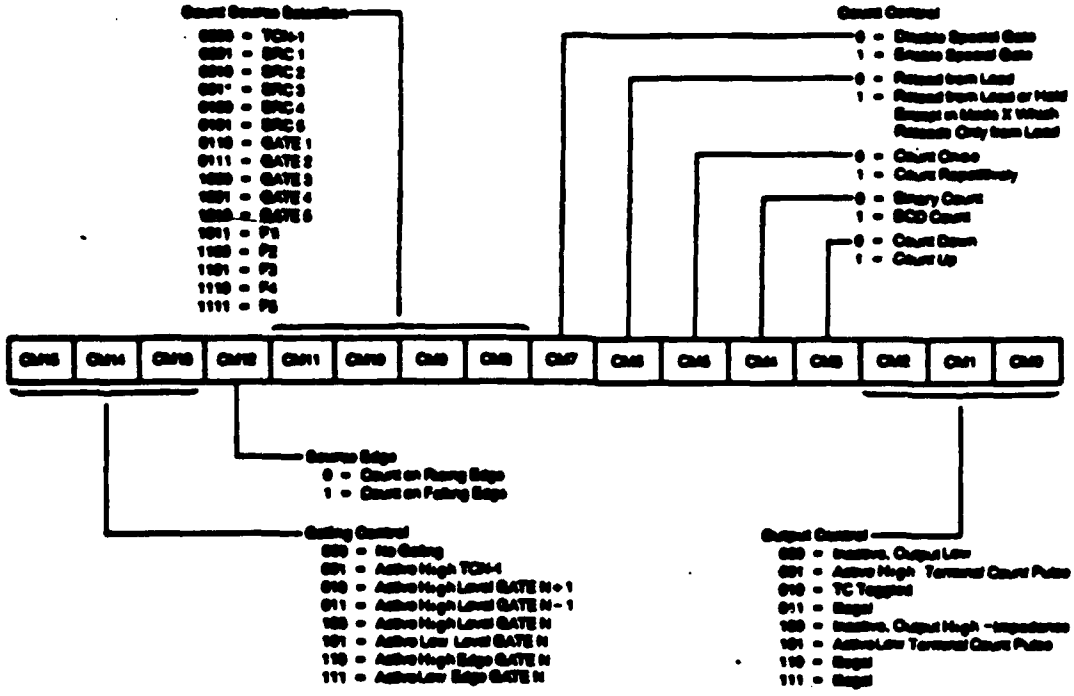


Figure 8: Counter Mode Register Bit Assignment

TABLE 3: COUNTER MODE REGISTER BIT ASSIGNMENT

BIT ASSIGNMENT	BITS	FUNCTION
CM15,CM14,CM13,CM12	0001	NO EXTERNAL GATING, COUNT ON FALLING EDGE OF CLOCK
CM11,CM10,CM9,CM8	1011	COUNTER FREQUENCY SOURCE IS F1 THE OSCILLATOR SEE FIGURE 8
CM7,CM6,CM5,CM4	0110	DIABLE SPECIAL GATE, RELOAD FROM LOAD OR HOLD, COUNT REPETITIVELY, COUNT BINARY
CM3,CM2,CM1,CM0	0010	COUNT DOWN, WHEN TERMINAL COUNT IS REACHED ON LOAD REGISTER TOGGLE COUNT TO THE HOLD REGISTER.

Most of the above settings are self explanatory. The most critical setting is that of the count being toggled between the LOAD and the HOLD register. This is the heart of the PWMS. As discussed previously, the HOLD register is loaded with a number that when counted out, refreshes the signal to the servo by firing a one-shot to a high voltage level (5V). Once high, the LOAD register then counts out and resets the one-shot to a low value. The number in the LOAD register translates to the variable pulse width desired.

c. Programming of the LOAD and HOLD Registers

There are LOAD and HOLD registers for each of the five counters, which need to be loaded successively. The selection of any of the five counter LOAD registers can be accomplished by writing a 9-13 (binary 00001001 through 00001101) as shown on the DATA POINTER register (Figure 5) through the CONTROL PORT. As before, the register is loaded with a high and low byte through the DATA PORT. The initial value loaded is a zero deflection angle of the PWMS translated to the servo that controls the vehicle vanes. To change the position of one of the five servos a new number is loaded into the LOAD REGISTER. This new number will be translated into a different width signal, which is then sent to the servo to change its position at a refresh rate of 10 ms.

The HOLD registers are also loaded successively. The selection of any of the HOLD registers is accomplished by loading a 17-21 (binary 00010001

through 00010101) into the DATA POINTER register through the CONTROL PORT as shown in Figure 5. Once this is accomplished, the low and high bytes are loaded as data into the DATA PORT. For the purpose of generating the PWMS, the HOLD register is loaded with a value that makes the refresh rate for all five channels approximately 10 ms.

3. Final Programming Notes for Mode F

The final event that must occur to initialize the Quartz I/O card is to load and arm all counters. In reference to Figure 6, it can be seen that when a decimal 127 number (binary 01111111) is loaded into the CONTROL PORT all counters will begin to operate. These programming steps will allow the counter to operate until a disarm command is given.

In Appendix A, a program used to generate the PWMS is given. The program allows for user interface to determine which counter and how much of a change of angle is desired. One equation is used in the program to convert a degree angle input to a number to load into the load register to obtain the desired pulse-width.

V. PROGRAMMING THE COMPUTERBOARD'S ANALOG-TO-DIGITAL CARD

A. COMPUTERBOARDS ANALOG-TO DIGITAL CARD OVERVIEW

With the programming of the Quartz card we have the ability to control the vehicle. The next step in the development of the digital controller is a method to convert the onboard sensor information to digital form. This is accomplished through the use of the Computerboard CIO-AD16Jr 16-channel analog-to-digital card. The card is versatile 12-bit converter with variable crystal settings, eight differential or sixteen single-ended channels, and a programmable input voltage range.

Similar to that for the Quartz card, the user's manual for this card is designed to be used with proprietor software. For the purpose needed, seven of the manual's 84 pages contain useful, but incomplete information. This is partly due to the fact that the proprietor software is provided in Basic. Additionally, a subroutine is used in every mode that requires a function "CALL" that is not provided in other than object code. To use the card for the purpose needed it was necessary to obtain the onboard counter/timer data sheet (Intel 8254), and to experiment with many of the settings.

Prior to the card being installed in the computer, the board must be strapped for a non-interfering address. For this application the address was strapped for 300

hex. The additional address options can be found by referring to users manual. In addition to the address setting, the card was strapped for 1 MHZ operation and 16-channel single-ended input. The Direct Memory Address switch selection is not relevant since a IBM 386 machine handles memory transfers.

The card is programmed in Borland C using the library functions "inportb(address)" and "outportb(address,data)" which allow access to external port addresses. The card allows for register level programming through sixteen 8-bit addresses that provide various functions. The analog-to-digital conversion method used is successive approximation with each conversion taking approximately 3 nanoseconds. The input signal is converted to a 12-bit digital number. A summary of the function of each address is shown below in Figure 9.

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Bits 9 - 12(LSB) & Channel #	Start A/D Conversion
BASE + 1	A/D Bits 1(MSB) - 8	None
BASE + 2	Channel MUX Set	Channel MUX Read
BASE + 3	Digital 4 Bit Input	Digital 4 Bit Output
BASE + 4	None	None
BASE + 5	None	None
BASE + 6	None	None
BASE + 7	None	None[21]
BASE + 8	Status EOC, UNI/BIP etc.	None
BASE + 9	DMA, Interrupt &Trigger Control	Set DMA, INT etc
BASE + 10	Pacer clock control register.	None
BASE + 11	Gain setting read-back.	Gain control
BASE + 12	Counter 0 Data	Counter 0 Data
BASE + 13	CTR 1 Data - A/D Pacer Clock	CTR 1 Data - A/D Pacer
BASE + 14	CTR 2 Data - A/D Pacer Clock	CTR 2 Data - A/D Pacer
BASE + 15	None. No read back on 8254.	Pacer Clock Control (8254)

Figure 9: A/D Card Address Overview

B. PROGRAMMING THE A/D CARD

Programming the card requires the initialization of several of the addresses from Figure 9 for various desired modes. The first initialization is that of the Multiplexor (MUX). The MUX can have various functions. The MUX can set up the number of channels to be incremented through, or be used to point at a specific channel desired (i.e., 0-15). The MUX also is the device that points to the current channel, and increments to the next channel to be converted. The conversion process can be started in one of three ways, by software trigger, external trigger, or internal pacer clock trigger. The MUX also can be used to reset to the desired channel to be read. This is done by writing to the MUX where the upper 4 bits of the MUX contain the channel desired for conversion. The layout of the MUX register is shown in Figure 10.

The MUX register is divided into two halves. The lower half (bits 0-3) of the register selects the starting channel to be converted. The upper half (bits 4-7) of the register selects the ending channel. The MUX points at the channel currently converted. Then, when triggered, the MUX increments itself and the STATUS register to the next channel to be converted in a continuous loop. Every write to this register sets the STATUS register channel and current A/D channel MUX to the number in bits 4-7.

BASE ADDRESS + 2

7	6	5	4	3	2	1	0
CH H8	CH H4	CH H2	CH H1	CH L8	CH L4	CH L2	CH L1

* CH refers to channel ** H refers to high channel
** L refers to low channel

Figure 10: Set up of the Multiplexor register

The next address to be initialized is the analog input range. All sixteen A/D channels can only input the selected voltage range. The voltage range can be one of the many values shown in Table 4. The layout of the register is shown in Figure 11. The selection of the appropriate bits from Table 4 written to base address + 11 selects the desired input voltage range. A voltage range of 0-5V is the input range for the current configuration. This range is setup by writing a decimal five (binary 00000101) to base address + 11.

BASE ADDRESS + 11

7	6	5	4	3	2	1	0
X	X	X	X	RANG	UNI/B	G1	G0

Figure 11: Analog Input Range Register

TABLE 4: BIT SELECTION FOR ANALOG INPUT RANGE

RANGE	UNI/BI	G1	G0	INPUT RNG
1	0	0	0	+- 10V
0	0	0	0	+- 5V
0	0	0	1	+- 2.5V
0	0	1	0	+- 1.25V
0	0	1	1	+- .625V
0	1	0	0	0-10V
0	1	0	1	0-5V ****
0	1	1	0	0-2.5V
0	1	1	1	0-1.25V

**** SELECTED RANGE FOR THE APPLICATION

The next address initialized is BASE ADDRESS+9 which controls the Direct Memory Access (DMA), interrupt, and trigger control. DMA allows the program to store the most recently converted channels in a specific PC memory location. Although DMA is not used during this application, DMA should be considered for later development to increase operating speeds. BASE ADDRESS+9 allows the selection of interrupts two through seven and allows them to be mapped onto the PC bus. Additionally, by the selection of the appropriate bits, the conversion trigger can be selected (bits 0 and 1). The DMA, interrupt and trigger control register is shown in Figure 12.

BASE ADDRESS + 9

7	6	5	4	3	2	1	0
INTE	IR4	IR2	IR1	X	DMA	TS1	TS0

Figure 12: DMA, Interupt and Trigger Control

Selecting INTE=1 (bit 7) enables interrupts to be placed on the PC bus, while INTE set to zero disables interrupts. Bits 4-6 select the binary number of the desired interrupt. Interrupts zero and one cannot be asserted if selected; these are

selected; these are reserved for the PC. Selecting DMA=1 allows DMA storage to PC memory, while a zero in bit two disables DMA. Bits zero and one are important because they select the source of the A/D conversion start. The conversion start selections are listed in Table 5.

TABLE 5: A/D START CONVERSION METHOD

TS1	TS0	TRIGGER METOD
0	X	SOFTWARE TRIGGERED A/D
1	0	START ON RISING EDGE TRIGGER (pin 25)
1	1	START ON PACER CLOCK PULSE (CTR2 out)

If "SOFTWARE TRIGGERED A/D" is selected, the conversion is begun by writing any number to the BASE ADDRESS. This causes the current address at which the MUX is pointed to be converted to its 12-bit digital form. The second selection allows for the conversions to be "EXTERNALLY TRIGGERED" by a rising edge digital signal placed on pin 25 of the card. The rising edge causes the address at which the MUX is pointing to be converted. The final start conversion selection utilizes the onboard pacer clock and two onboard counters to control the

conversion. In this mode counters 1 and 2 can be used to set the frequency of conversion. In this mode counter 1 is used serially in conjunction with counter 2 causing the start of conversion. The rising edge of counter 2's output square wave triggers the start of conversion.

The next five registers all work in conjunction with each other. Figure 13 shows the interrelationship of these five registers, and Figures 14 through 18 show the layout of each register.

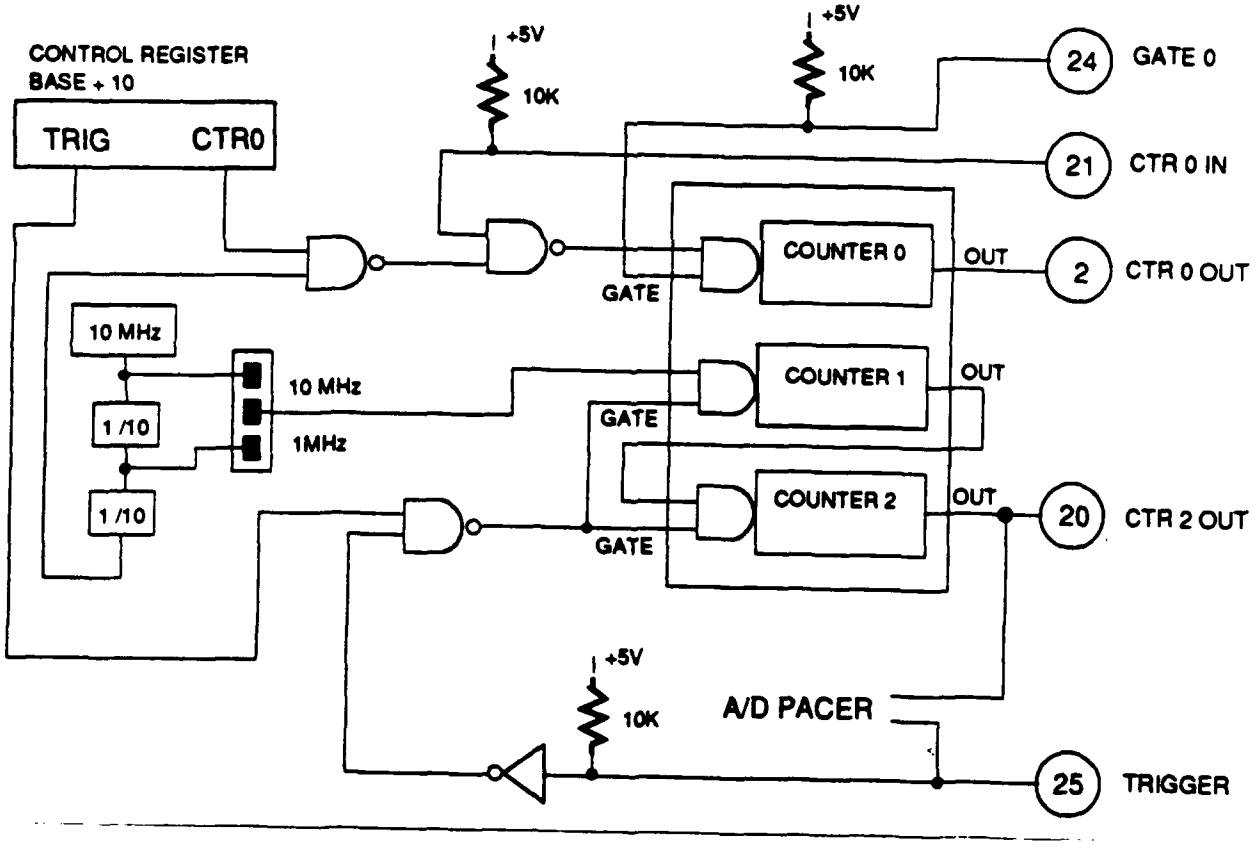


Figure 13: PACER CLOCK Control Register

BASE ADDRESS + 10

7	6	5	4	3	2	1	0
X	X	X	X	X	X	CTR0	CTR1

Figure 14: PACER CLOCK Control Register

BASE ADDRESS + 15

7	6	5	4	3	2	1	0
SC1	SC0	RW1	RW0	BCD2	M2	M1	M0

Figure 15: COUNTER CONTROL

BASE ADDRESS + 12

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

Figure 16: COUNTER 0

BASE ADDRESS + 13

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

Figure 17: COUNTER 1

BASE ADDRESS +14

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

Figure 18: COUNTER 2

The PACER CLOCK control register BASE ADDRESS+10 (Figure 14) is the interface between the board functions and the Intel 8254 programmable interval timer (PACER CLOCK). The remaining four registers are resident onboard the 8254 and are accessible from the addresses shown. Programming the PACER CLOCK

control register consists of four possibilities. The selection for the purpose desired is CTR0=0 and TRIG0=1. This selection allows the COUNTER 2 output to control the start conversion. If desired this mode also allows pin 25 of the cards connector to affect the conversion. The pin is pulled up to +5V, and will always be high unless an external connection to pin 25 pulls the pin low which would disable conversion.

The remaining COUNTERS 0 through COUNTER 2 can be loaded by selecting them through commands to the COUNTER CONTROL register (Figure 15). Additionally, the mode of the 8254 is set up through the COUNTER CONTROL register. The operating mode of the PACER CLOCK must be selected from the 8254 data sheet. From the data sheet the desired mode selected for this application is mode three. This selects a repeating square wave at a frequency determined by numbers loaded in COUNTER 1 and COUNTER 2.

To load any of the 8254 onboard registers, it is necessary to refer to the 8254 data sheet. To load a counter, the COUNTER CONTROL must point a multiplexor internal to the 8254 at the desired counter. Loading COUNTER 1 requires a binary 0111XXXX (X indicates it does not matter which binary number) to be written to the COUNTER CONTROL register (BASE ADDRESS + 15). Bits SC0=0 and SC1=1 (refer to Figure 15) select the desired register. Bits RW1=1 and RW0=1 (RW which stands for READ WRITE) select a loading scheme for the desired register,

in this case the least significant byte first, then the most significant byte. To select COUNTER 2 binary 1011XXXX is loaded into the COUNTER CONTROL register. Bits SC0=1 and SC1=0 select COUNTER 2. The read/write bits are as previously described. The counters are loaded with numbers that make mode three create a 10 ms square wave which is the desired sampling rate for the control laws' [Ref 1].

Once the registers are loaded with values, then the COUNTER CONTROL register must be loaded with a value to enable the 8254 to operate in the desired manner to produce the desired output. Mode 3 produces a square wave whose frequency depends on the values loaded in COUNTER 1 and COUNTER 2. To select this mode a binary XX11X110 is loaded into BASE ADDRESS+15 the COUNTER CONTROL. With Reference to the 8254 data sheet, RW1 and RW0, select as before which byte is loaded first. The bits of COUNTER CONTROL M2=X, M1=1 and M0=1 select mode 3 which from the 8254 data sheet produces the desired square wave output.

Once initialization is complete, the MUX begins sequencing through the desired channels scanning one channel per rising edge. The control laws' sampling rate was established to be 10 milliseconds [Ref 1]. This sampling rate is accomplished by setting up the card for "EXTERNAL TRIGGER". Then loading numbers into COUNTERS 1 and 2 that create a 10 ms square wave out of COUNTER 2. The output of COUNTER 2 is then be fed into pin 25 of the card to

provide the rising edge of the "EXTERNAL TRIGGER" for the desired sampling rate. This method is preferred over Pacer Clock driven because that mode does not produce an interupt that can be polled from the STATUS REGISTER. The program in Appendix B polls the interrupt bit till set, then the mode of conversion is changed to "SOFTWARE TRIGGERED MODE", to allow conversion of the other channels. The programmed software allows the MUX to point at the desired number of channels to be converted. This is done prior to the interrupt being cleared and trigger control being returned to "EXTERNAL TRIGGER". The interrupt is cleared by writing any value to the STATUS register. After the interrupt is cleared and the trigger is changed back to "EXTERNAL TRIGGER", the MUX increments to the next channel to be scanned and waits for the next rising edge from COUNTER 2.

After the channel is converted, the value can be read and assembled from base address and BASE ADDRESS + 1. The registers are shown in Figure 19 and 20.

BASE ADDRESS

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

Figure 19: A/D LSB Data and Channel Register

BASE ADDRESS + 1

7	6	5	4	3	2	1	0
A/D1 MSB	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7	A/D8

Figure 20: A/D MSB DATA

As shown in Figure 19, the lower four bits of the BASE ADDRESS contain the channel that has been converted. The upper four bits contain the Least Significant Bit (LSB) of the converted channel. BASE ADDRESS+1 contains the upper eight bits of the converted channel. To assemble the complete 12-bit word Borland C function "inportb(address)" is used to read the two register addresses. Then the

contents read from the BASE ADDRESS are rolled right four bits to remove the channel number, and leave the LSB. The contents read from BASE ADDRESS+1 (Figure 20) are then rolled left four bits to make room for the LSB. To assemble the two numbers, they are bitwise ORed to make the complete 12-bit word. This process takes the inputted analog signal and converts the signal to a digital number between 0-4096.

The final register that has many convenient uses is the STATUS REGISTER (BASE ADDRESS + 8). The STATUS register is shown in Figure 21.

BASE ADDRESS + 8

7	6	5	4	3	2	1	0
EOC	U/B	MUX	INT	CH8	CH4	CH2	CH1

Figure 21: Status Register

The most significant bit of the STATUS register EOC indicates that the end of conversion has been received; EOC=1 means busy converting, while EOC=0 means conversion complete. The next bit U/B tells whether the input amplifier is in unipolar (U/B=1), or bipolar (U/B=0). MUX bit tells whether the input channels

are single-ended or differential. The INT bit tells whether an external pulse has been received on pin 25; INT=0 means no pulse, and INT=1 means a pulse has been received. This bit can be conveniently used for polling to set up the control law sampling rate, and later applications can be placed on the internal PC bus to free up the CPU. The final four bits tell at which channel the MUX is currently pointed. A program that converts input channels from analog to digital is included in the Appendix B.

VI. UTILITY SYSTEM

A. UTILITY SYSTEM OVERVIEW

The utility system incorporates many diverse systems on the Archytas vehicle. In general the utility systems include the systems needed to power the sensors, control system servos, and the electronic ignition. Additionally the system includes a method for getting signals from the sensors to the computer, and commands from the computer to the vehicle. All of these systems have to be contained compactly and securely in a housing aboard the vehicle.

When NPS received the AROD vehicles they contained two forebody units which each contained all the electronics to operate the vehicles. Unfortunately no documentation was received, or available. Observations of the units' complicated wiring coupled with no schematics made the aspect of using the existing wiring impossible. With this in mind the tasks were to gather the data sheets on the sensors and establish what power systems were available and engineer a new system. The other task was to make the utility housing self contained and able to be attached to both the vehicle and the umbilical.

The direction taken was to get one control system roll-rate completely connected. This control system would unmask many hidden hardware problems and

make the addition of other sensor connections easier. The systems connected were the power for ignition, power and signal for servos, and the power and signal connections for the roll-rate sensor.

One of the first steps in the process was to adapt the housing to the vehicle. Since the early tests are to be done with the vehicle attached to the umbilical, the housing was designed to be attached to the bottom of the vehicle between the vanes. This additionally provides a degree of stability. Figure 22 shows the housing attached to the vehicle; Figure 23 shows the housing alone.

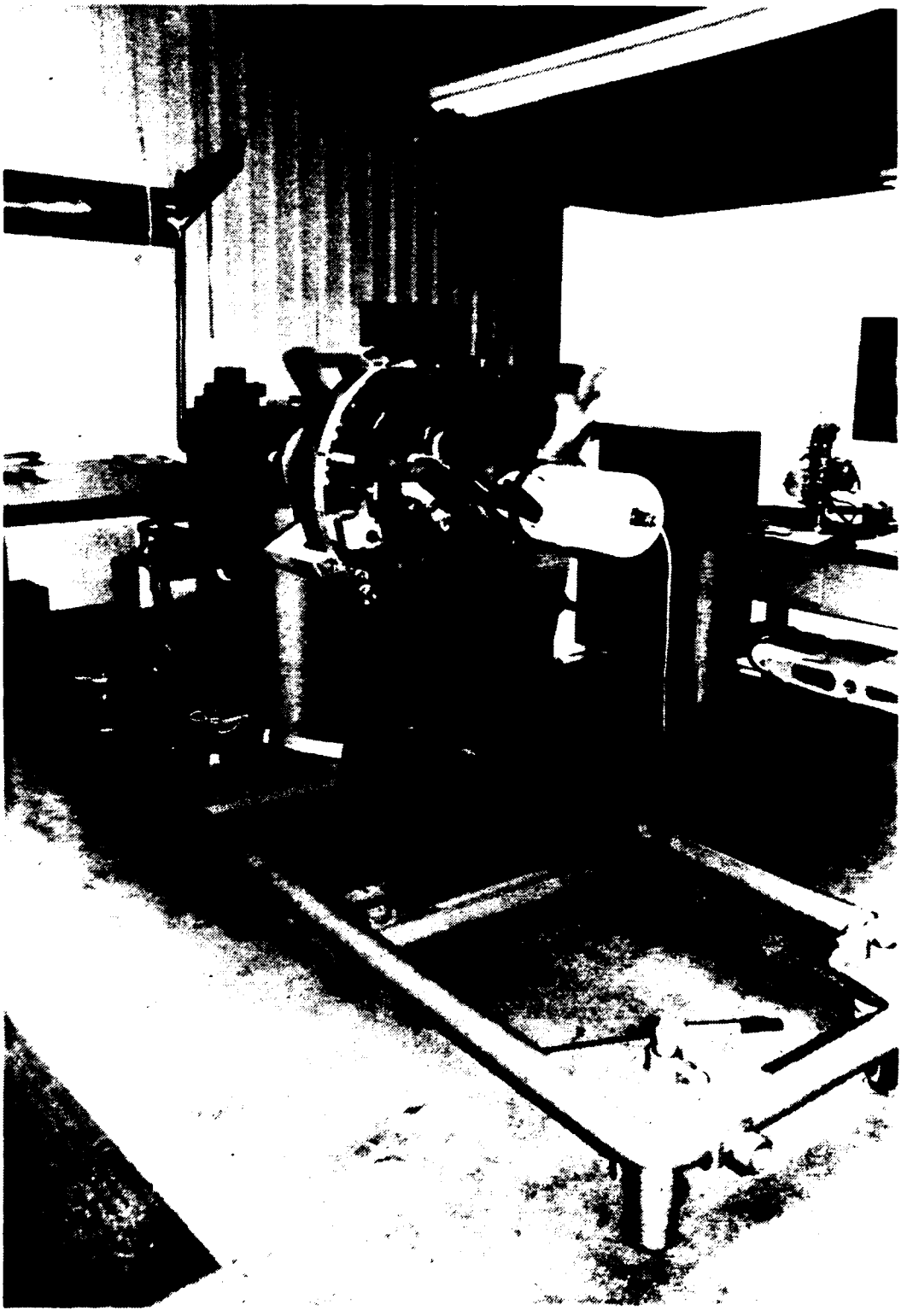


Figure 22: Housing Attached to the Vehicle

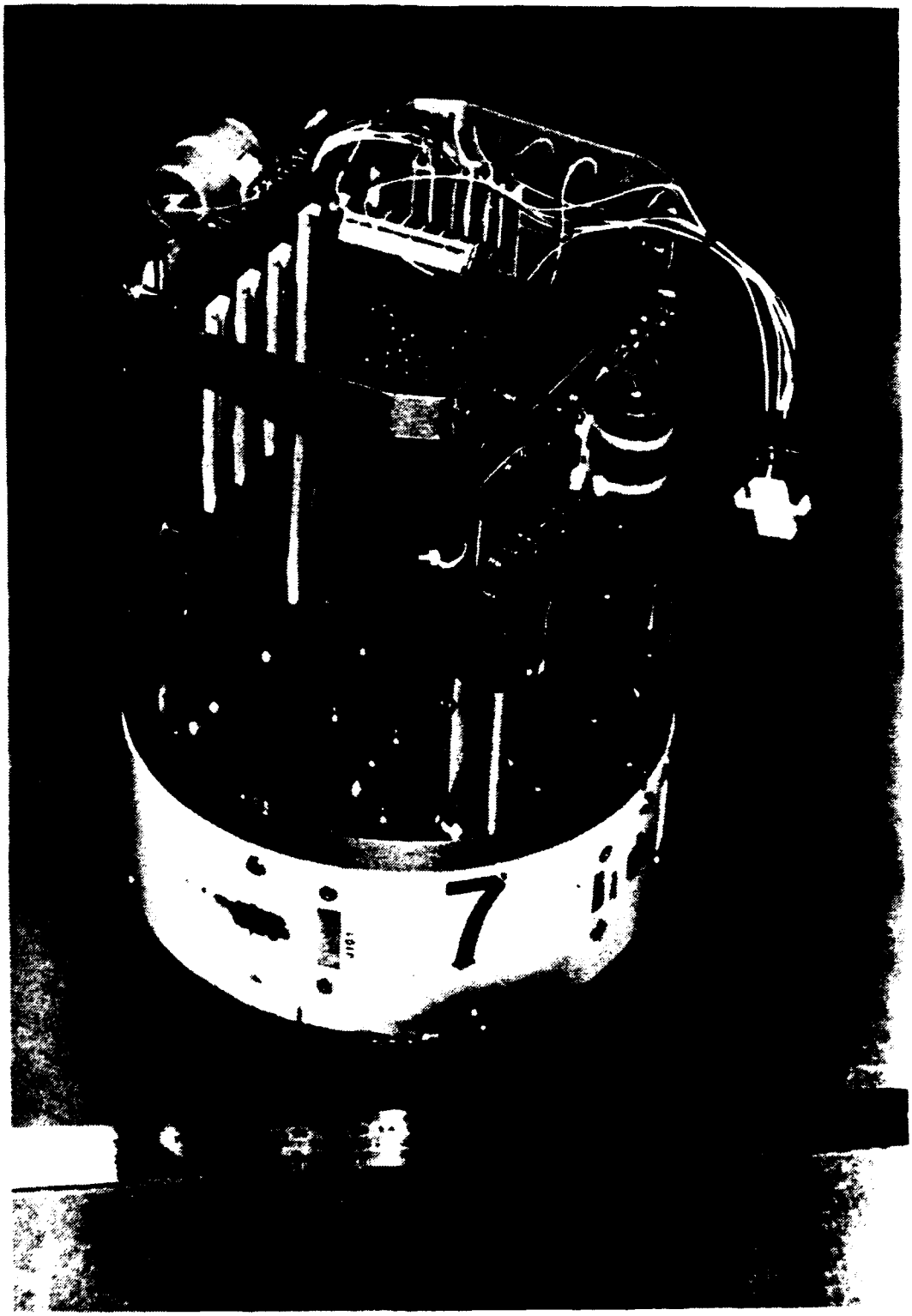


Figure 23: Housing Unit Power Routing and Connection

1. Power Routing and Connection

The next step was to begin routing power to meet each system's requirements. From the original AROD configuration the housing unit contained various DC-to-DC converters. These are units whose output is a specified constant once the input reaches a certain minimum value. The configuration from the original AROD comes with power supplies that can conveniently power the sensors, electronic ignition, and servos. Available power supplies on the unit are +/- 5V, +12V, +/- 15V, and +28V. As shown on the schematic in Appendix D, the power supply to the servos is +5V. This is wired directly from a +5V converter through Futaba J connectors (to allow disconnection for housing removal) to the five S-134 Futaba servos.

The electronic ignition for the engine requires +28V. This is wired from the +28V DC converter through a Futaba G connector. The connector contains ground, +28V and a return line for the tachometer from the electronic ignition which is routed back through to the umbilical to allow measurement of engine RPM.

The only sensor wired up is the single axis roll-rate sensor whose data sheet is in Appendix C, and picture is shown in Figure 24 and 25. Wiring this control system sensor allowed the connection of the output of the sensor through a conditioning card to the umbilical ending up at the A/D card which provides the input from the vehicle in computer-usable form. The control laws can then be applied to

the vehicle input. The computer can then generate the correct PWMS for the vehicle from the Quartz I/O card and send it back through the umbilical to the servos to correct the vehicle's roll-rate. The sensor requires +/- 15V to power up. This sensor is connected to the appropriate power supply through a Futaba G connector to allow removal of the sensor from the housing. The data sheets for the remaining sensors that will require installation are included in Appendix C along with pictures of each.

The next step in the hardware connections was to provide a means for the vehicle to receive power from the onboard generator, or have power provided externally until engine ignition. The original AROD had a card with a group of diodes arranged in a fashion to allow dual power sourcing. This card was adapted to fit inside the housing and wired to allow external connection for power through plugs, and wired to the onboard generator. This card allowed external power connection to power servos, ignition, and sensors prior to the engine running. After the engine is running and the generator is supplying power, the external connections can be removed to provide the ability for independent flight.

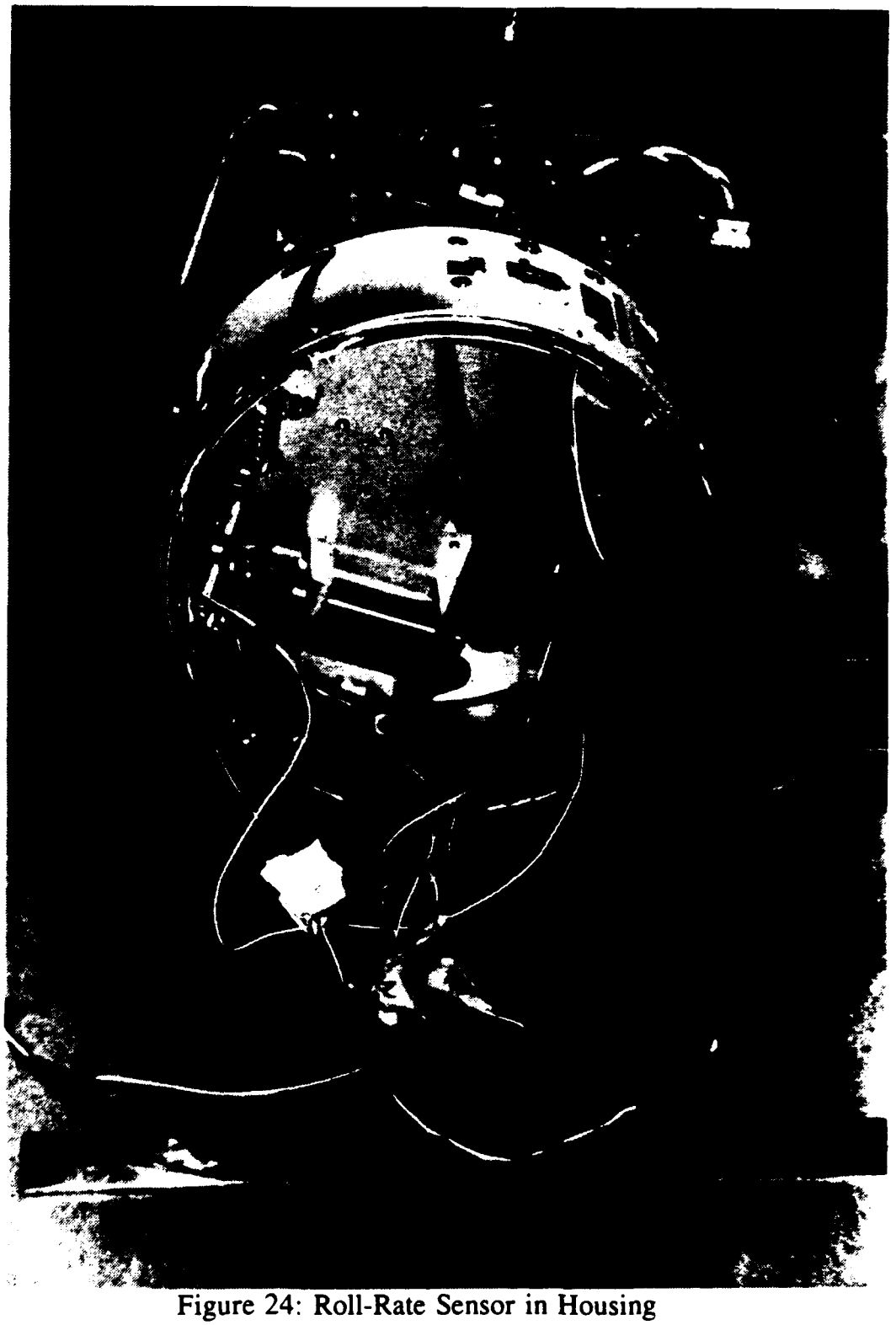


Figure 24: Roll-Rate Sensor in Housing

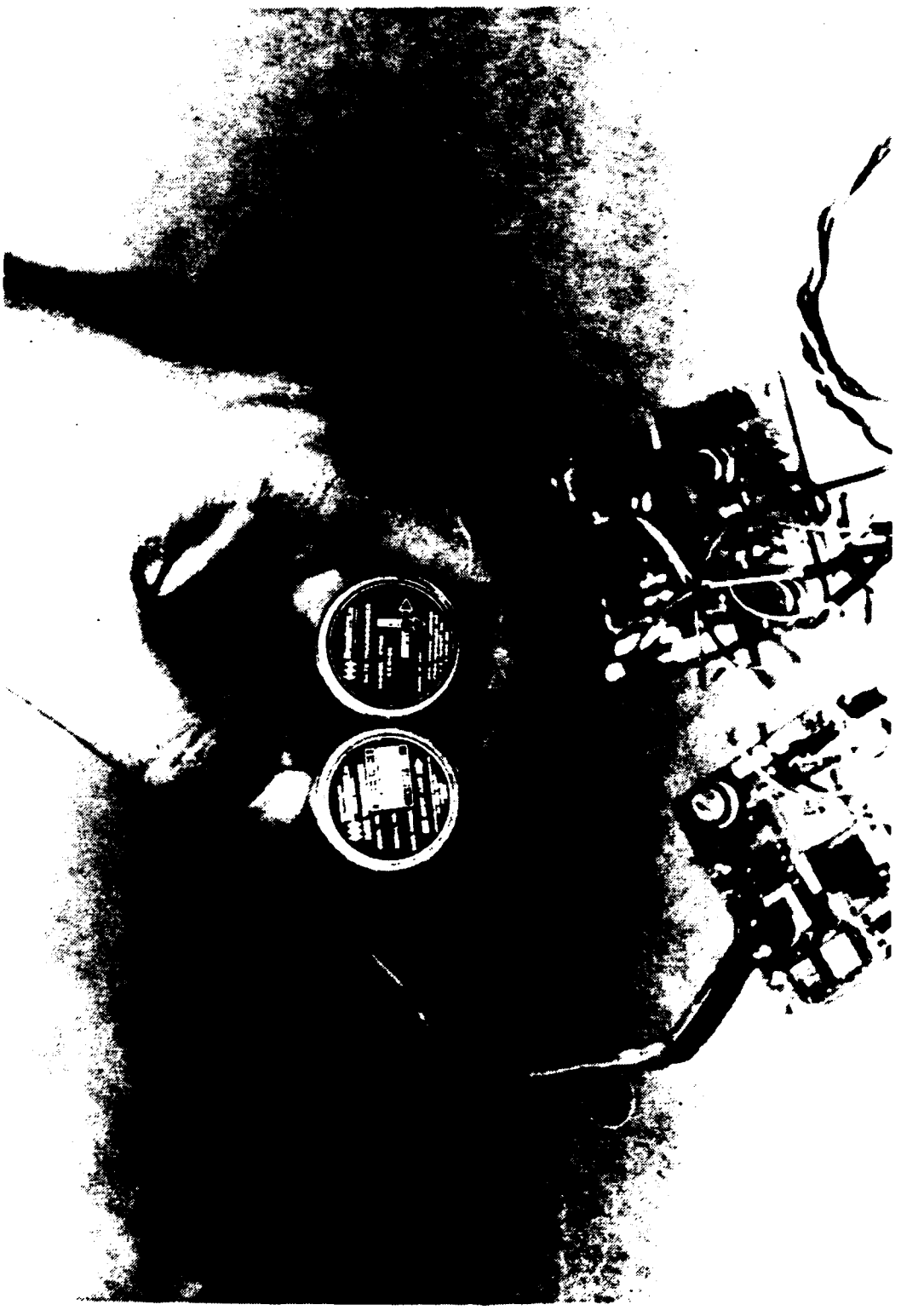


Figure 25: Roll-Rate Sensor (lower) Pitch and Yaw Sensor (upper)

2. Signal Connection and Routing

Once power is applied to each of the devices, the controlling signal must be connected. The servos each require a PWMS to be connected that is originated at the computer. This is accomplished by connections from the umbilical through a connector. Then the signal is routed through the housing and joined as the third wire in the Futaba J connectors that connect the power to each servo. This means that the servos are each connected to a 3-wire Futaba J connector that contains ground, +5V and a PWMS. This connection is shown on the schematic in Appendix D.

The connected roll-rate sensor signal output is a +/-2.5 VDC that correlates to +/-100 degrees/second of roll rate. This outputed roll rate needs to be conditioned to the 0-5V range that the A/D card is set up to convert. The signal from the roll-rate sensor is sent from the sensor to a conditioning card that was developed by AROD engineers. Once the sensor output is conditioned to the necessary voltage range of 0-5V, the signal is then routed to the umbilical through connectors as shown on the schematic in Appendix D.

The umbilical provides a means of sending the PWMS to the vehicle to control the servos. Additionally, the umbilical provides routing for the roll-rate sensor signal and the tachometer. The umbilical is an unshielded cable that is connected to the vehicle through a cannon plug on the housing shown in Figure 26, and to the computer by connections shown in Figures 27 and 28. Figures 27 and

28 show the cables run from the A/D card and the Quartz I/O card that are installed in the computer. Additionally shown in both figures is the joy stick that commands roll-rate and throttle. The terminal block shown in both figures allows connection of the Umbilical to both cables. The breadboard has a unity gain amplifier wired that was used to protect the Quartz card outputs which did not have, but needed buffered outputs.

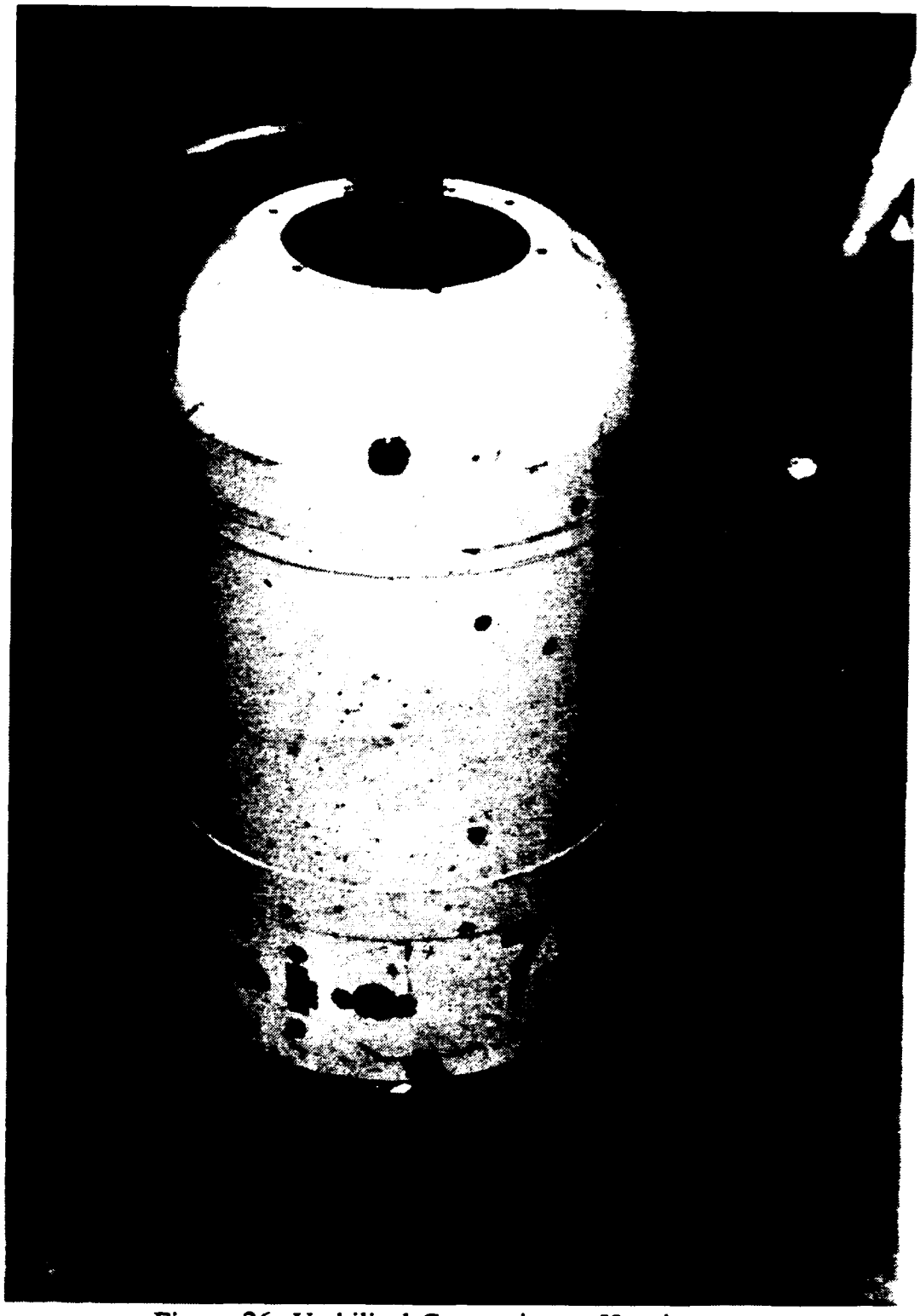


Figure 26: Umbilical Connection to Housing

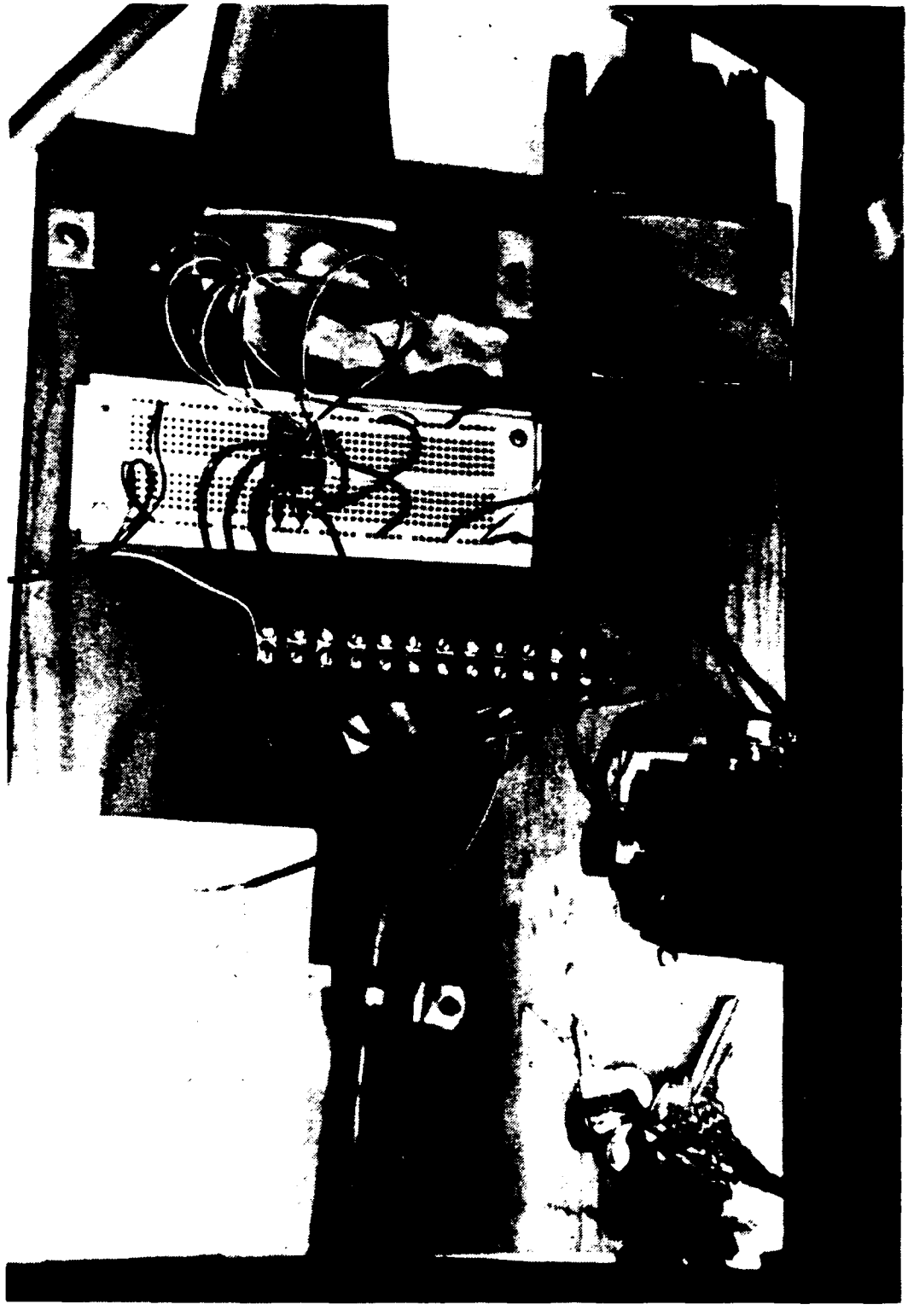


Figure 27: Umbilical Connection to Computer

Figure 28: Umbilical Connection to Computer

VII. SYSTEM TESTING, CONCLUSIONS AND RECOMMENDATIONS

A. SYSTEM TESTING

Testing of the various systems has occurred at various stages of the project. The ability to control movement of the vanes became important and was tested when static thrust and torque measurements were needed during the summer of 1992. The Archytas vehicle test stand allowed the computer to move the vanes and throttle through the umbilical during engine operation. The ability to command the throttle, and one or all four vanes incrementally was instrumental in making accurate measurements of the desired parameter.

The A/D system was tested and utilized when it became necessary to model the Futaba S-134 servos that control the vanes to determine the frequency response for incorporation in the control laws [Ref 1]. The data gathered for the modeling was accomplished by commanding a unit impulse signal into the S-134 servo. Then the programmed A/D card allowed sampling of the position of the feedback potentiometer inside the servo.

Additionally the complete roll-rate system is being tested. The system incorporates the software control laws [Ref 1] into the hardware A/D, servo control, and utility systems. Early hardware problems continue to be resolved to allow

complete testing. As with all functional systems, the addition of any individually engineered system to other individually engineered systems is not accomplished without further modifications.

B. CONCLUSIONS

The desired goal of this investigation was to create a digital interface system for the Archytas UAV. This vehicle is a VTOL fixed wing airplane that is designed to hover to altitude, then transition to horizontal flight. The emphasis was to establish a complete system to convert onboard sensor information into computer-useable form, then allow the information, once processed, to output a signal to command attitude-controlling servos on the vehicle to control pitch, yaw and roll. This investigation accomplished the following:

- The addition of a Quartz I/O card added to the PC and programming to create a Pulse-Width-Modulated Signal to control servos.
- The addition and programming of the Computerboards Analog-to-Digital card that sampled at the desired controller rate, and converted the inputed signals to a 12-bit digital useable signal.
- A self-contained housing was developed that attaches to the bottom of the Archytas vehicle and contains power supplies that allow operation of the roll-rate sensor, servos and the electronic ignition for the engine. These power supplies can operate prior to engine ignition on external power, and after ignition on the engine's generator.

Problems developed in several areas during the development of the above systems. The servos were deemed to be have limitations for the purpose of controlling the vanes. The servos limited torque, and plastic gears make failure a real possibility. The umbilical cable was determined to have noise spikes traversing the cable to the point of shorting the output amplifiers on the AM9513A (Quartz I/O card) causing replacement of the chip. This problem led to the addition of a unity gain amplifier installed in line with the cable to protect the computer card. The conditioning card schematics obtained from Sandia Laboratories were determined to be inaccurate and require further investigation for use with the remaining sensors. With any physically controlled and controllable system much time can be spent adjusting programs and locating bugs that cause unwanted behavior. The addition of wiring adds the additional problems of unwanted noise, and imperfect or sometimes bad connections. Overcoming these types of problems provide the best real-world lessons and a feeling of accomplishment.

C. RECOMMENDATIONS

In continuing work toward a fully-flyable vehicle, specific recommendations include :

- Addition of the remaining sensors, and incorporation of the remaining control laws for stability.
- Obtaining a shielded umbilical cable to remove the noise problems.
- The purchase of adequate servos that operate off PWMS and develop adequate torque for the given job.
- Investigating the addition of DMA to the Computerboards A/D card to facilitate obtaining all sampled channels quicker. This would additionally free up the CPU time.
- Establishing an interrupt system that will be generated from the Computerboards A/D card and placed on the PC bus. This would eliminate the need for polling and release the CPU to accomplish other functions.
- Development of a three-axis test stand that will allow testing of all axes of motion on the vehicle housing to establish validity of the control laws applied to the utility system.

APPENDIX A: PROGRAM GENERATES PWMS

```
/*
   Written by: Lt. Paul Merz
   Revised:    11/29/92
   For: Masters Thesis applied to the Archytas air vehicle


   This program is written in Borland C compiled and run in version
    2.0.  The program utilizes the Quartz I/O card to generate
   Pulse-Width -Modulated signals (PWMS) of varying duty cycles from
   .6 to 2.4 ms.  The signal is produced out of all 5 of the cards
   counters and is designed to vary the position of any servo connected
   to the counters.  The program is designed to be user driven with
   the following servo connections:
                    +5v pin 49 to red wire of servo
                    gnd pin 50 to black wire of servo
                   PWMS any of pins 5,11,17,23 or 39

   To operate the card must be strapped prior to installation for the
   address that will be declared as "datreg".
   Ref: Quartz I/O User's Manual                                    */


#include<dos.h>          /* preprocessor control lines: 'include'      */
#include<stdio.h>        /*   inserts a copy of <*.h> at this point    */
int datreg = 544;        /* declare 'datreg' this is the base address
                                  strapped prior to card
          installation       */
int conreg = 545;   /*declare 'conreg' as integer value 545        */

main()                /* functn 'main' executes main body of program*/

{
initialize();          /* functn calls 'initialize'sets up registers */
chgangle();          /* functn 'chgangle' executes endless loop to change
                            vane positions                          */
}
```

```
/*************************************************************************
*/
/* changle is a subroutine that converts a user input into a integer
   number that can be placed in the load register to change the width
   of the outputed pulse width.  The software allows the selection of
   any of the 5 channels on the Quartz card.  After selection the user
   inputs an integer number that will be converted to a change in PWMS.*/
/*************************************************************************
**/

chgangle()

{
int i,hibyte,lobyte,angle,cmnd,vane; /* declare variables as integers */
angle=1;              /* since angle always > 0, this causes       */
while (angle > 0)     /*   endless loop                            */
 {
  printf("ENTER THE VANE NUMBER TO CHANGE 1 TO 5\n");
  scanf("%d",&vane);   /* inputs the value of vane between 1 & 5    */
  vane=vane+8;         /* adding 8 changes the binary value so that*/
                       /*  'vane' can be used to label an address  */
                      /*that is translatable to a counter         */

  printf("ENTER THE DESIRED ANGLE \n ");
  scanf("%d",&angle);          /* input the desired vane angle in
                                  degrees */
  angle=((1900/206)*angle+600); /* algorithm to conv fm deg to dig # */
  hibyte=(angle/256);           /* forms high byte   */
  lobyte=(angle-hibyte*256);    /* forms low byte    */
  cmnd=193;                    /* 193 = 1100 0001b   */
  outportb(conreg,cmnd);       /* disarms counter 1  */
  cmnd=vane;                /* between 9 & 13= 0000 1001b & 0000 1101b*/
  outportb(conreg,cmnd);   /* select load register of desired counter */
  outportb(datreg,lobyte); /* lower byte of # to load reg             */
  outportb(datreg,hibyte); /* upper byte of # to load reg             */
  cmnd=233;                /* 233 = 1110 1001b                        */
  outportb(conreg,cmnd);   /* sets toggle high for counter 1          */
  cmnd=97;                /* 97 = 0110 0001b                         */
```

```
  outportb(conreg,cmnd);  /* loads (fm load reg) and arms counter 1  */
 } /*end while*/
} /*end chgangle*/


/* Initialize sets up the Quartz card to operate in mode j which
   allows the card to generate the PWMS out of all 5 counters.
   it also sets up various other functions that are not used for
   the purpose of the archytas                                    */

initialize()
{
int cmnd,i;

printf("start of process\n");
cmnd=255;                /* 255 = 1111 1111b                      */
outportb(conreg,cmnd);    /* resets all board functions           */

cmnd=23;                 /* 23  = 0001 0111b                      */
outportb(conreg,cmnd);    /* select master mode register          */
cmnd=176;                /* 176 = 1011 0000b                      */
outportb(datreg,cmnd);    /* low byte: FOUT source is F1          */
cmnd=65;                 /* 65  = 0100 0001b                      */
outportb(datreg,cmnd);    /* high byte: binary division,     |
                         disable increment,   | MODE
                         8-bit bus width,     |  'J'
                         FOUT on, divide by 1 |        */
cmnd=249;                /* 249 = 1111 1001b                      */
outportb(conreg,cmnd);    /* disable prefetch for write operations */

for (i=1;i<=5;i++)
{
  cmnd=i;                /* 1 to 5 = 0000 0001b to 0000 0101b     */
  outportb(conreg,cmnd); /*select ctr mode reg of group 1 thru 5  */
  cmnd=98;               /* 98  = 0110 0010b                      */
  outportb(datreg,cmnd); /* low byte: disable special gate,
                        reload from load or hold,
                        count repetitively,
                        binary count,
                        count down,
```

```
                        TC toggled                    */
  cmnd=27;              /* 27  = 0001 1011b           */
  outportb(datreg,cmnd); /* high byte: no gating for counter 1 thru 5
                        count on falling edge,
                        count source F1               */
}

for (i=25;i<=29;i++)
{
  cmnd=i;               /* 25 to 29 = 0001 1001b to 0001 1101b  */
  outportb(conreg,cmnd);  /* load hold registers for refresh rate */
  cmnd=0;               /* 0  = 0000 0000b            */
  outportb(datreg,cmnd);  /* load low byte into hold register     */
  cmnd=31;              /* 31 = 0001 1111b            */
  outportb(datreg,cmnd);  /* load high byte into hold register    */
            /* combined lo & hi: 7936 gives refresh rate */
}

for (i=9;i<=13;i++)
{
  cmnd=i;               /* 9 to 13 = 0000 1001b to 0000 1101b   */
  outportb(conreg,cmnd); /* select load register for pulse width */
  cmnd=110;             /* 110 = 0110 1110b           */
  outportb(datreg,cmnd); /* load low byte into load register     */
  cmnd=5;               /*  5 = 0000 0101b            */
  outportb(datreg,cmnd); /* load high byte into load register    */
            /* combined lo & hi: 37430 gives pulse width */
 }

for (i=233;i<=237;i++)
{                       /* 233 = 1110 1001b           */
  cmnd=i;               /* 237 = 1110 1101b           */
  outportb(conreg,cmnd);  /* set toggle high for counters 1 thru 5 */
}
cmnd=127;               /* 127 = 0111 1111b           */
outportb(conreg,cmnd);  /* load and arm counters 1 thru 5       */

printf("COMPLETED INITIALIZATION OF SERVOS\n");
}
```

APPENDIX B: PROGRAM FOR A/D CONVERSION

```
/*
    Written by: Paul Merz
    Revised: 11/29/92
    For: Masters Thesis on the Archytas air vehicle

    This program is written to be compiled in Borland C 2.0.
    The program is a combination of the program similar to
    Appendix A and a program to convert 3 channels from analog
    to digital utilizing the CIO-AD16jr Computerboards card.
    The program utilizes a 10ms interrupt to trigger conversion.
    Once the interrupt is received the mode on the CIO-AD16jr card
    is changed to software triggered then three channels are
    converted.  Once converted the status register is reset to
    allow further interrupts, and the mode is changed back to
    external triggered to allow the interrupt to begin the process again.

    The following are connections to be made:
                Pin 7 grnd
                Pin 20 connects to pin 25
                Pin 35,36 and 37 are channels to be converted

    This program was utilized to allow testing of the process of
    bringing an analog signal in similar to that of the roll rate
    sensor, throttle and commanded roll-rate, then outputing some
    new value to the control vanes to change the vane position.
                                                        */

#include<dos.h>
#include<stdio.h>

int datreg = 544;     /* QUARTZ CARD base address       */
int conreg = 545;     /* QUARTZ CARD base address +1    */
int basaddr=768;      /* A/D CARD base address          */
int basepll=769;      /* A/D CARD base address +1       */
int mux=770;          /* A/D CARD base address +2       */
int statreg=776;      /* A/D CARD base address +8       */
int intcont=777;      /* A/D CARD base address +9       */
int pclock=778;       /* A/D CARD base address +10      */
```

```
int  inrange=779;      /*  A/D CARD base address +11      */
int  cntrl=781;        /*  A/D CARD base address +13      */
int  cntr2=782;        /*  A/D CARD base address +14      */
int  cntrcon=783;      /*  A/D CARD base address +15      */
int  lookup[70],angle,newangle,throttle,nthrottle;  /* GLOBALS
                                    declared as integers */

main()
{
 initialize();
 setup();
 sample();

}


/*****************************************************************/
/* This section (initialize()) is similar to Appendix A        */
/*****************************************************************/


initialize()       /*  INITIALIZES QUARTZ CARD  */
{
 int cmnd,i,angle;

 printf("start of process\n");
 cmnd= 255;
 outportb(conreg,cmnd);       /*reset all board functions*/
 cmnd=23;
 outportb(conreg,cmnd);       /*select master mode register*/
 cmnd=176;
 outportb(datreg,cmnd);       /*low byte enables fout*/
 cmnd=65;
 outportb(datreg,cmnd);
 cmnd=249;
 outportb(conreg,cmnd);
 for (i=1;i<=5;i++)
  {
   cmnd=i;                    /*select group 1*/
   outportb(conreg,cmnd);
```

```
  cmnd=2;                  /*low byte set modes of counter 1 in cmr*/
  outportb(datreg,cmnd);
  cmnd=27;                  /*high byte  no gating for counter 1*/
  outportb(datreg,cmnd);
 }
for (i=25;i<=30;i++)
 {
  cmnd=i;                  /*load the hold register for refresh rate*/
  outportb(conreg,cmnd);
  cmnd=0;
  outportb(datreg,cmnd);
  cmnd=10;
  outportb(datreg,cmnd);
 }
for (i=9;i<=13;i++)
 {
  cmnd=i;                 /*select load register for pulse width*/
  outportb(conreg,cmnd);
  cmnd=103;                /*load low byte into load register*/
  outportb(datreg,cmnd);
  cmnd=7;
  outportb(datreg,cmnd);
 }
for (i=233;i<=237;i++)
 {
  cmnd=i;
  outportb(conreg,cmnd);
 }
cmnd=127;                  /*load and arm counter 1*/
outportb(conreg,cmnd);

for (i=9;i<=13;i++)
 {
  cmnd=i;                 /*select load register for pulse width*/
  outportb(conreg,cmnd);
  cmnd=110;                /*load low byte into load register*/
  outportb(datreg,cmnd);
  cmnd=5;
  outportb(datreg,cmnd);
 }
```

```
for (i=233;i<=237;i++)
 {
  cmnd=i;
  outportb(conreg,cmnd);
 }
cmnd=127;                    /*load and arm counter 1*/
outportb(conreg,cmnd);
for (i=1;i<=70;i++) lookup[i]=50+i;
printf("COMPLETED INITIALIZATION OF SERVOS\n");


}

/*************************************************************/
 Setup initializes the CIO-AD16jr card to provide a 10ms out
 of counter 2 out.  The square wave frequency is set up by
 the values loaded in counter 1 and 2.  The card is set up
 to sample chanels 0-3.
 /*************************************************************/

setup()                    /* INITIALIZES A/D CARD  */
{
 int cmnd;                  /* declare cmnd as integer */
 cmnd=32;                    /* 32 = 0010 0000b  */
 outportb(mux,cmnd);        /* set the mux to read channels 0-2 */
 cmnd=2;                    /*  2 = 0000 0010b  */
 outportb(intcont,cmnd); /*set up pacer clock for clock driven
                         sampling */
 cmnd=5;                    /*5 = 0000 0101b*/
 outportb(inrange,cmnd); /*set up for correct input and
                         type of voltage */

 /*********************************************/
 /*sets up 10 ms square wave out of counter 2*/
 /*********************************************/


 cmnd=118;                  /*FM DATA SHEET: SC-01, RW-11, M-011,
                         BCD-0 -  */
 outportb(cntrcon,cmnd); /*CTR 1, READ/WR LSBYTE 1ST, MODE 3,
```

```
                    BINARY  */
 cmnd=100;              /*100 IN LOWER BYTE set up counter 1*/
 outportb(cntr1,cmnd);
 cmnd=0;               /* 0 IN UPPER BYTE set up counter 1*/
 outportb(cntr1,cmnd);
 cmnd=182;              /* FM DATA SHEET: SC-10, RW-11, M-011,
                     BCD-0 -  */
 outportb(cntrcon,cmnd); /*CTR 2, READ/WR LSBYTE 1ST, MODE 3,
                    BINARY  */
 cmnd=100;              /*100 IN LOWER BYTE for counter 2*/
 outportb(cntr2,cmnd);
 cmnd=0;               /*0 IN UPPER BYTE  for counter 2*/
 outportb(cntr2,cmnd);
 printf("COMPLETED CARD INITIALIZATION\n");
}

/*****************************************************************/
/* Sample does the work of checking the interupt, once the
   interupt is found the conversion process is changed to
   software driven to sample the three desired channels.
   each of these is assembled into a 12-bit word to be used
   later.  Once all channels are sampled the interrupt is
   cleared and the trigger is changed to external triggered
   mode. This procedure allows the throttle to be input from
   a joystick then converted to a PWMS to change the position
   of a servo attached to channel 5 of the Quartz card       */
/*****************************************************************/


sample()                /*  EXERCISES A/D CARD  */
{
 int x,cmnd,lsb,lsb1,lsb2,lsb3,sreg,turnangle;
    x=1;                    /* forces continuous loop*/
    while (x==1)
    {
     sreg= inportb(statreg); /*read status reg to check
                             interrupt bit */
     sreg= sreg&16;  /* 'and' with 16 to get only 5th bit info */
     if (sreg==16)   /* 5th bit is interrupt bit- if high,
                     external pulse has been recvd,
```

```
                    i.e. ready to get data          */
  {
 cmnd=32;                /* 32 = 0010 0000b     */
 outportb(mux,cmnd);     /* set the mux to read channels 0-2 */
cmnd=0;
 outportb(intcont,cmnd); /*SOFTWARE TRIGGERED A/D ONLY */
 outportb(basaddr,cmnd); /*IMMEDIATE A/D CONVERSION   */
 lsb  = inportb(basaddr); /*READ LOW BYTE, MSB-8 TO LSB
                          + CHANNEL*/
 lsb1 = inportb(basepl1); /*READ HIGH BYTE, MSB TO MSB-7*/
 lsb  = lsb > > 4;        /*ROLL LSBYTE RIGHT 4 BITS*/
 lsb1 = lsb1 < < 4;       /*ROLL MSBYTE LEFT 4 BITS */
 lsb1 = lsb1 | lsb;       /*  'OR' TO GET 12 BIT INFO*/
cmnd=0;
 outportb(basaddr,cmnd); /*IMMEDIATE A/D CONVERSION*/
 lsb  = inportb(basaddr); /*READ LOW BYTE, MSB-8 TO LSB
                         + CHANNEL */
 lsb2 = inportb(basepl1); /*READ HIGH BYTE, MSB TO MSB-7*/
 lsb  = lsb > > 4;        /*ROLL LSBYTE RIGHT 4 BITS*/
 lsb2 = lsb2 < < 4;       /*ROLL MSBYTE LEFT 4 BITS*/
 lsb2 = lsb2 | lsb;       /*'OR' TO GET 12 BIT INFO*/
cmnd=0;
 outportb(basaddr,cmnd); /*IMMEDIATE A/D CONVERSION*/
 lsb  = inportb(basaddr); /*READ LOW BYTE, MSB-8 TO LSB
                          + CHANNEL */
 lsb3 = inportb(basepl1); /*READ HIGH BYTE, MSB TO MSB-7*/
 lsb  = lsb > > 4;        /*ROLL LSBYTE RIGHT 4 BITS*/
 lsb3 = lsb3 < < 4;       /*ROLL MSBYTE LEFT 4 BITS*/
 lsb3 = lsb3 | lsb;       /*'OR' TO GET 12 BIT INFO*/

cmnd=2;
 outportb(intcont,cmnd); /*RETURN TO PACER CLOCK DRIVEN
                         SAMPLING */

 cmnd=inportb(statreg);  /*read status register,
                         then write back  */
 outportb(statreg,cmnd); /*to it same #- causes reset
                         of flip-flop*/
                    /* so that interrupt bit is set to 0*/
 throttle= (int)((lsb2-2714)*.127+50)
```

```
                        /* calculate throttle #*/
    chgangle();         /* call function chgangle() */
    nthrottle=throttle;
      }
     }
  }
```

```
/*********************************************************/
/* Chgangle is the same as described in Appendix A     */
/*********************************************************/


chgangle()          /*  EXERCISES QUARTZ CARD  */
{
int i,hibyte,lobyte,angle,cmnd,vane;


  angle=((1900/206)*newangle+600);
  hibyte=(angle/256);
  lobyte=(angle-hibyte*256);
  cmnd=207;
  outportb(conreg,cmnd);

    for (i = 9; i <= 12;i++)
      {
   outportb(conreg,i);
   outportb(datreg,lobyte);
   outportb(datreg,hibyte);
      }
    for (i = 233;i <= 236;i++)  outportb(conreg,i);
    cmnd=111;
    outportb(conreg,cmnd);
```

```
    cmnd=208;
    outportb(conreg,cmnd);
    angle=((1900/206)*nthrottle+600);
    hibyte=(angle/256);
    lobyte=(angle-hibyte*256);
    cmnd=13;
    outportb(conreg,cmnd);
    outportb(datreg,lobyte);
    outportb(datreg,hibyte);
    cmnd=237;
    outportb(conreg,cmnd);
    cmnd=112;
    outportb(conreg,cmnd);
}
```

APPENDIX C: SENSOR INFORMATION

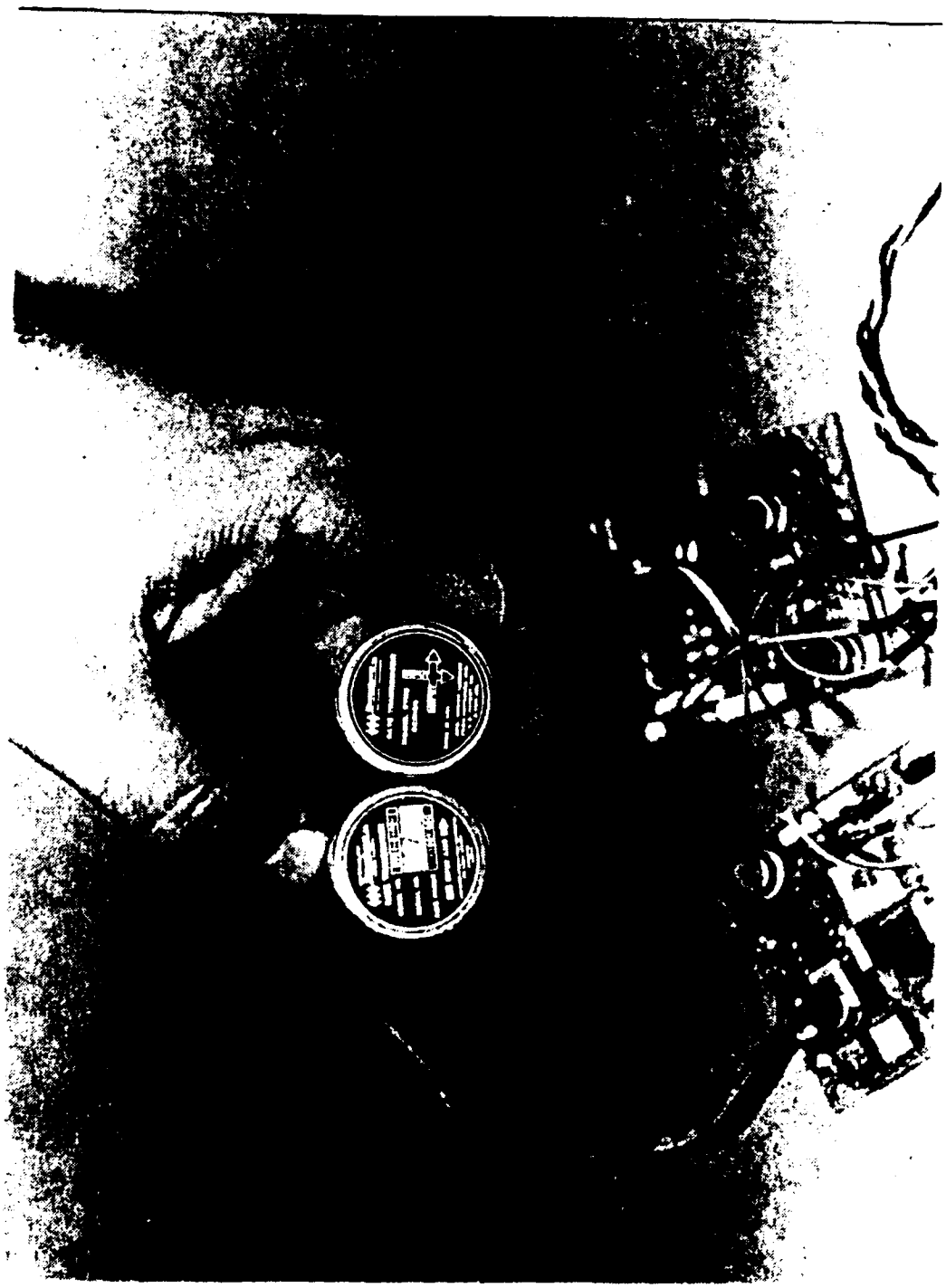
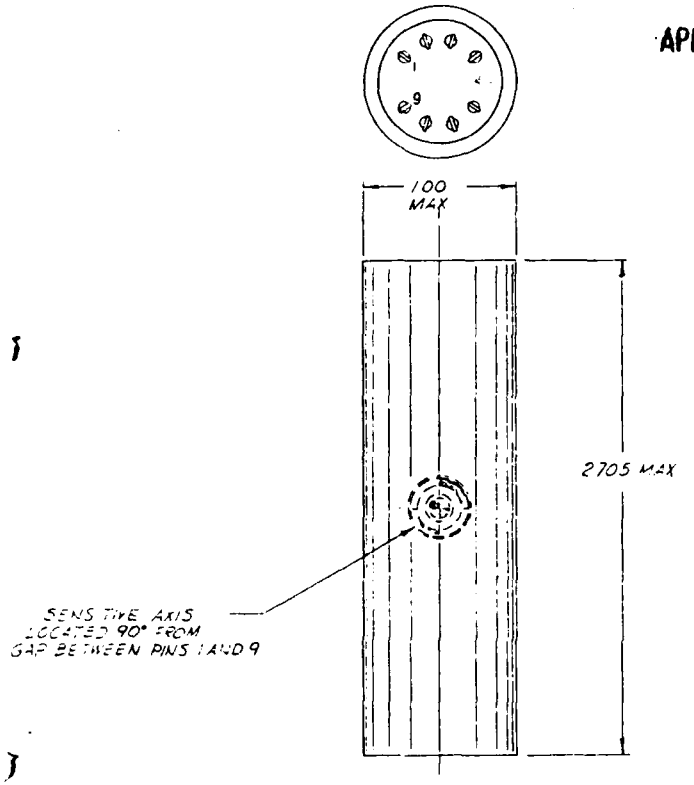
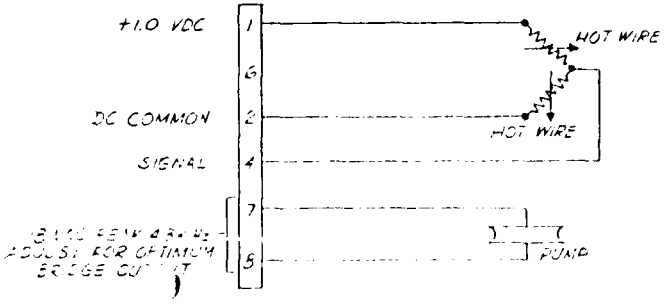


Figure 29: Roll-Rate sensor (lower), Pitch and Yaw Rate sensor (upper)

APR 10 1992





SPECIFICATIONS

X1.0	RANGE RATE	±100°/SECOND
2.0	NATURAL FREQUENCY	25 HZ MINIMUM
3.0	DAMPING	0.7 ± 0.2 TYPICAL
X4.0	OUTPUT	±2.5 MILLIVOLTS NOMINAL ±2.0V
5.0	ACCURACY	
5.1	LINEARITY	±1.0% FULL SCALE
5.2	RESOLUTION	.005% OF FULL SCALE
5.3	HYSTERESIS	NONE
X5.4	NULL SIGNAL	±2 DEG/SECOND
5.5	THRESHOLD	0.005 DEG/SECOND
5.6	NOISE	0.1% OF FULL SCALE
6.0	INPUT VOLTAGE	1.0 VDC MAXIMUM (PINS 1 TO 2)
6.1	INPUT CURRENT	600 ± 5 MILLIAMPS
7.0	TIME TO FULL OPERATION	40 MILLISECONDS
8.0	SEALING	HERMETIC
9.0	FINISH	STAINLESS STEEL PASSIVATED
10.0	ENVIRONMENTAL CONDITIONS	
10.1	ALTITUDE	UNLIMITED
10.2	SHOCK	10,000 G
10.3	VIBRATION	0.06 INCH DA OR 15G WHICHEVER LIMITS. 20 TO 2,000 HZ
10.4	TEMPERATURE OPERATING	-55°C TO +85°C
10.5	TEMPERATURE STORAGE	-65°C TO 150°C
11.0	SERVICE LIFE	10,000 HOURS
12.0	STORAGE LIFE	5 YEARS
13.0	WEIGHT	3 OZ. MAXIMUM
14.0	REMARKS	
14.1	ITEMS MARKED WITH (X) ARE CHECKED IN PRODUCTION TESTS OTHER ITEMS FOR REFERENCE MAY BE CHECKED ON ORDER BY QUALIFICATION TESTS.	

CONTROLLED DRAWING

Humphrey Inc. — ELECTRO-MECHANICAL INSTRUMENTS

TITLE: ENVELOPE DRAWING RATE TRANSDUCER

CUSTOMER REFMATL

UNLESS OTHERWISE SPECIFIED LIMITS ON DIMENSIONS ARE DECIMAL .XX ± .03 .XXX ± .010 ANGULAR ± 1°

SCALE 2/1

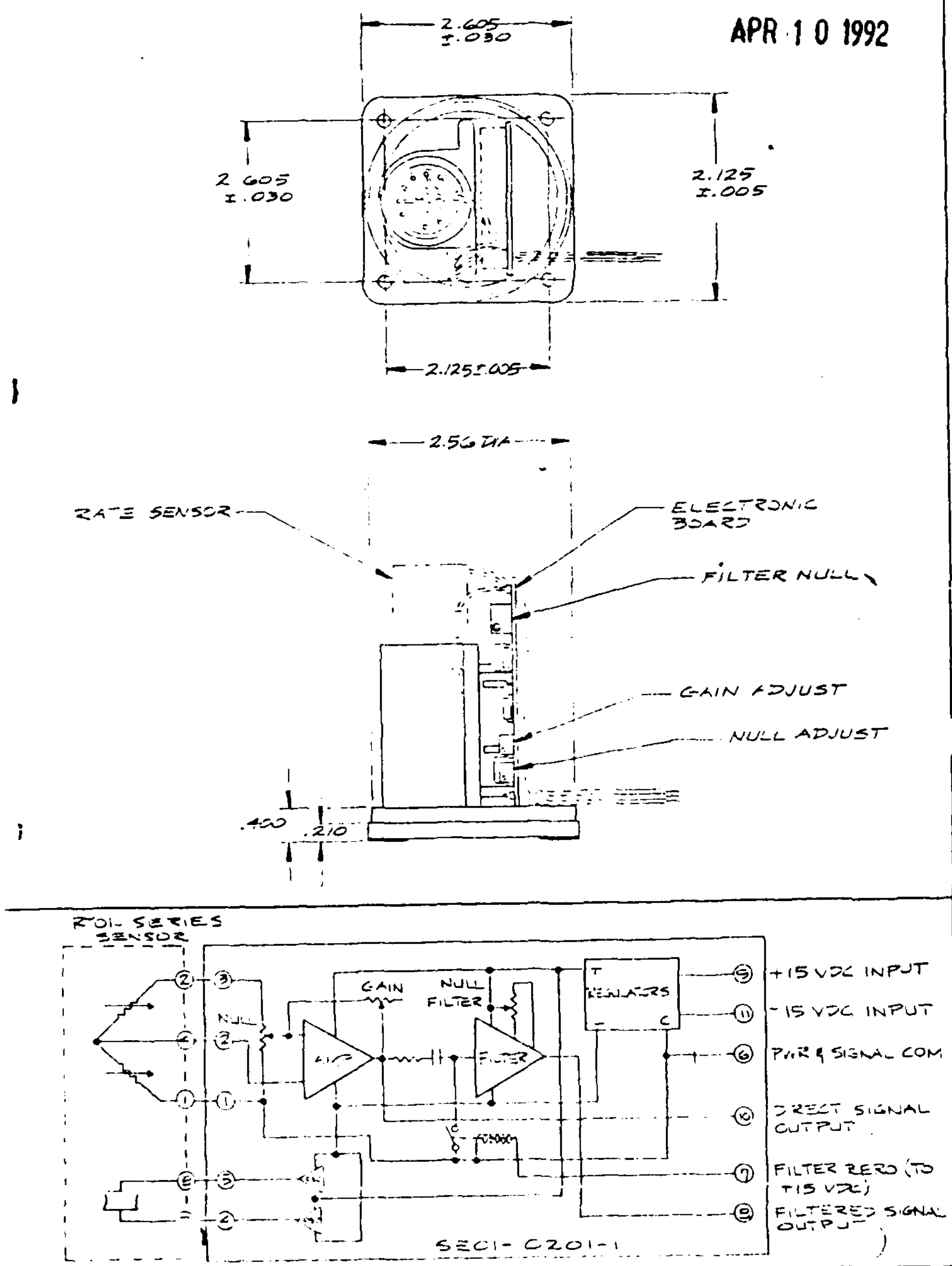
DWG SIZE C

MODEL NO RT01-01 CODE IDENT 01102

REV

ROLL RATE

APR 1 0 1992



SPECIFICATIONS

1.0 INPUT VOLTAGE ________ ±15 VOLTS D.C.

2.0 INPUT CURRENT ________ 100 MILLIAMPS MAXIMUM

3.0 OUTPUT VOLTAGE ________ ±2.5 VOLTS FULL-SCALE TYPICAL

4.0 OUTPUT SCALE FACTOR ________ ADJUST PER RT01-SERIES SENSOR BEING USED.

5.0 NOTE: THIS SENSOR ELECTRONICS IS DESIGNED TO FUNCTION WITH THE RT01-SERIES RATE TRANSDUCERS. COMPONENT VALUES AND ADJUSTMENTS ARE MADE SUCH THAT THE SE01/RT01 COMBINATION FUNCTIONS PROPERLY. THE END PRODUCT WILL CONFORM TO THE CONTROLLING SPECIFICATIONS WHICH WILL BE THE SENSOR SPECIFICATIONS MODIFIED BY PURCHASE-ORDER AGREEMENTS. THE NULL-ADJUST AND GAIN-ADJUST (SCALE-FACTOR) CONTROLS ARE READILY AVAILABLE FOR CUSTOMER ADJUSTMENTS.

CONTROLLED DRAWING

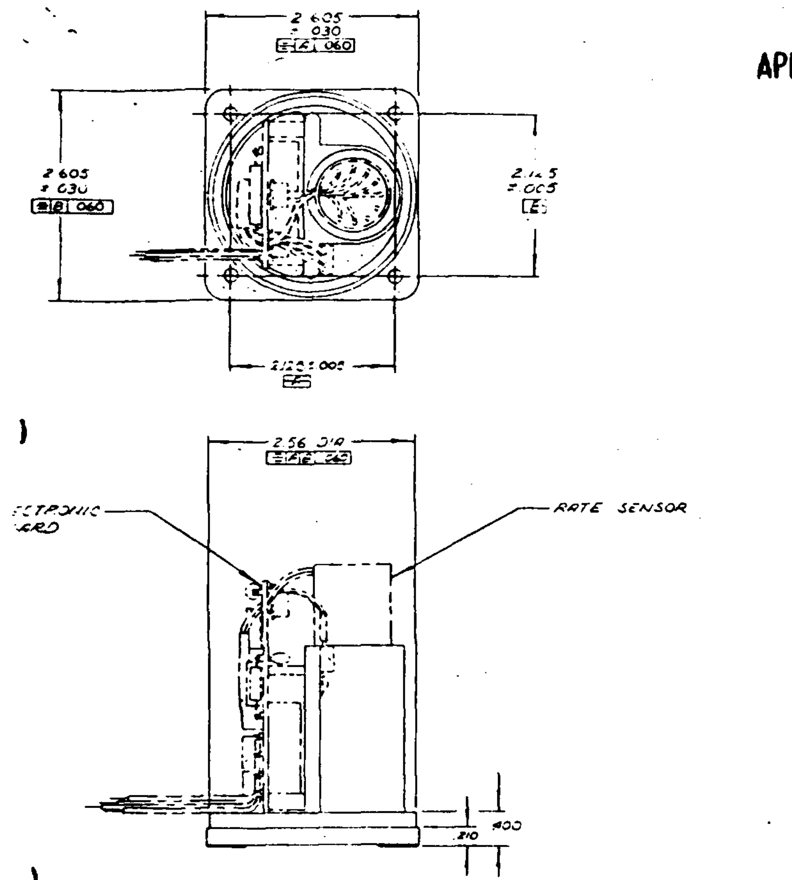
Humphrey Inc. — ELECTRO-MECHANICAL INSTRUMENTS

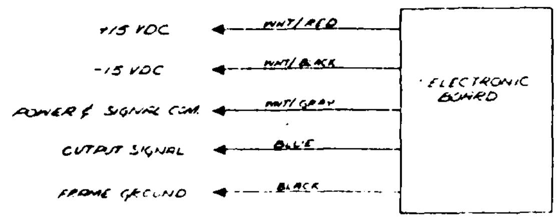
TITLE: SENSOR ELECTRONICS

SCALE 1/1 — DWG MODEL NO SE01-02 — REV A

ROLL RATE SENSOR

APR 1 0 1992





SPECIFICATIONS

1.0	INPUT VOLTAGE	±15 VDC
2.0	INPUT CURRENT	100 MA MAXIMUM
3.0	OUTPUT SIGNAL	±2.5 VDC
4.0	OUTPUT IMPEDANCE	100 OHMS MAXIMUM

CONTROLLED
DRAWING

Humphrey Inc.

ELECTRO-MECHANICAL INSTRUMENTS

TITLE: SENSOR ELECTRONICS

DRAWN BY: C. THERRIEN

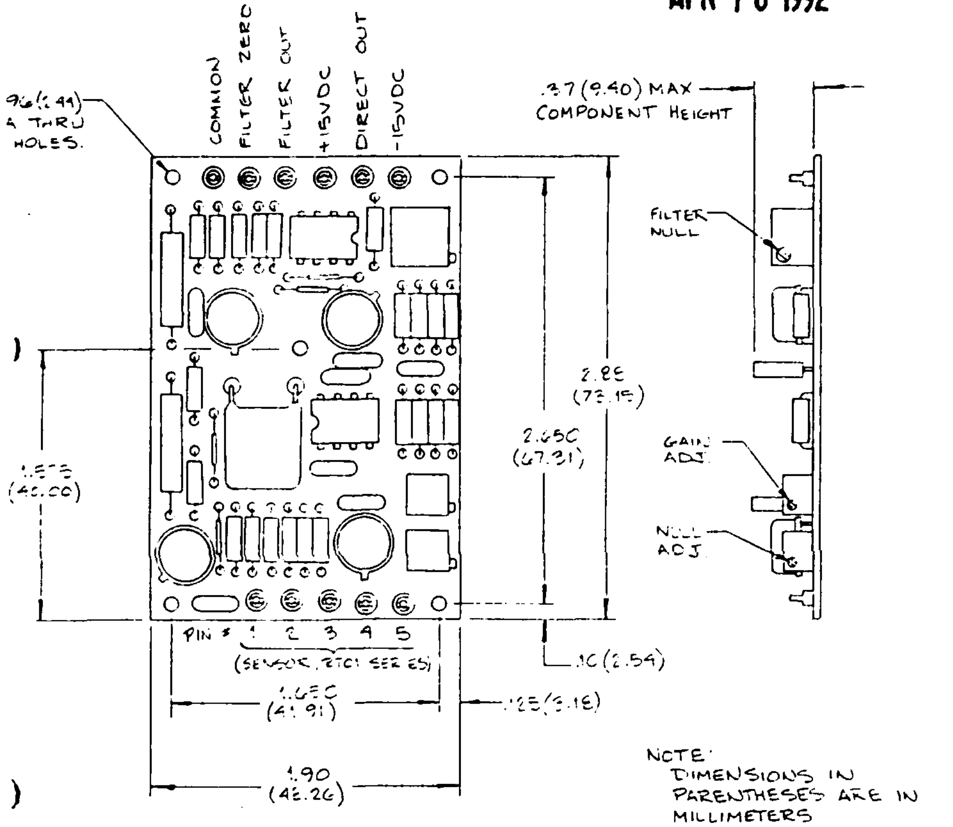
SCALE: 1/1

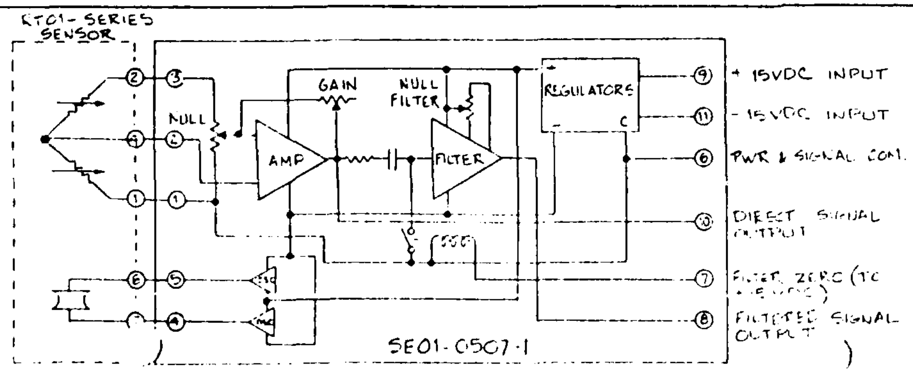
MODEL NO: SE01-0101-

REV: A

CUSTOMER REF MATL

APR 1 0 1992





SPECIFICATIONS

1.0 INPUT VOLTAGE ______ ±15 VOLTS D.C.

2.0 INPUT CURRENT ______ 100 MILLIAMPS MAXIMUM

3.0 OUTPUT VOLTAGE ______ ±2.5 VOLTS FULL-SCALE TYPICAL

4.0 OUTPUT SCALE FACTOR ______ ADJUST PER RT01-SERIES SENSOR BEING USED.

5.0 NOTE: THIS SENSOR ELECTRONICS IS DESIGNED TO FUNCTION WITH THE RT01-SERIES RATE TRANSDUCERS. COMPONENT VALUES AND ADJUSTMENTS ARE MADE SUCH THAT THE SE01/RT01 COMBINATION FUNCTIONS PROPERLY. THE END PRODUCT WILL CONFORM TO THE CONTROLLING SPECIFICATIONS WHICH WILL BE THE SENSOR SPECIFICATIONS MODIFIED BY PURCHASE-ORDER AGREEMENTS. THE NULL-ADJUST AND GAIN-ADJUST (SCALE-FACTOR) CONTROLS ARE READILY AVAILABLE FOR CUSTOMER ADJUSTMENTS.

CONTROLLED DRAWING

REVISIONS (SEE DCN)	DWG CL	BY	DATE
	1		
	2		
	3		
	4		
	5		

CUSTOMER REF MATL

Humphrey Inc. — ELECTRO MECHANICAL INSTRUMENTS

TITLE: ENVELOPE DRAWING SENSOR ELECTRONICS

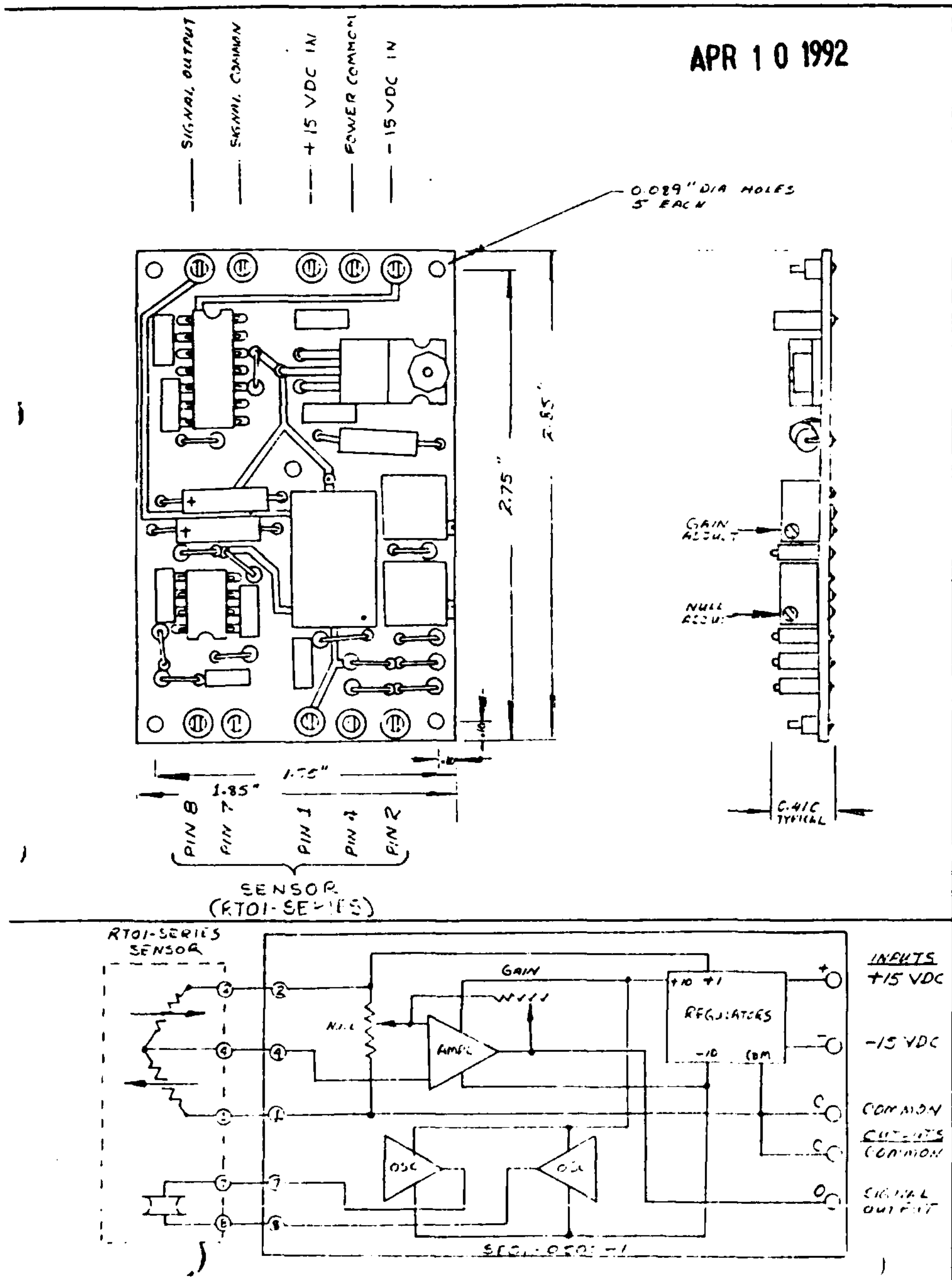
DRAWN BY: SCHWARTZ

UNLESS OTHERWISE SPECIFIED LIMITS ON DIMENSIONS ARE

SCALE 2/1 — DWG SIZE C — MODEL NO SE01-050 — CODE IDENT NO — REV

ROLL RATE

APR 1 0 1992



SPECIFICATIONS

1.0 INPUT VOLTAGE .... ±15 VOLTS D.C.

2.0 INPUT CURRENT .... 100 MILLIAMPS MAXIMUM

3.0 OUTPUT VOLTAGE .... ±2.5 VOLTS FULL-SCALE TYPICAL

4.0 OUTPUT SCALE FACTOR .... ADJUST PER RT01-SERIES SENSOR BEING USED.

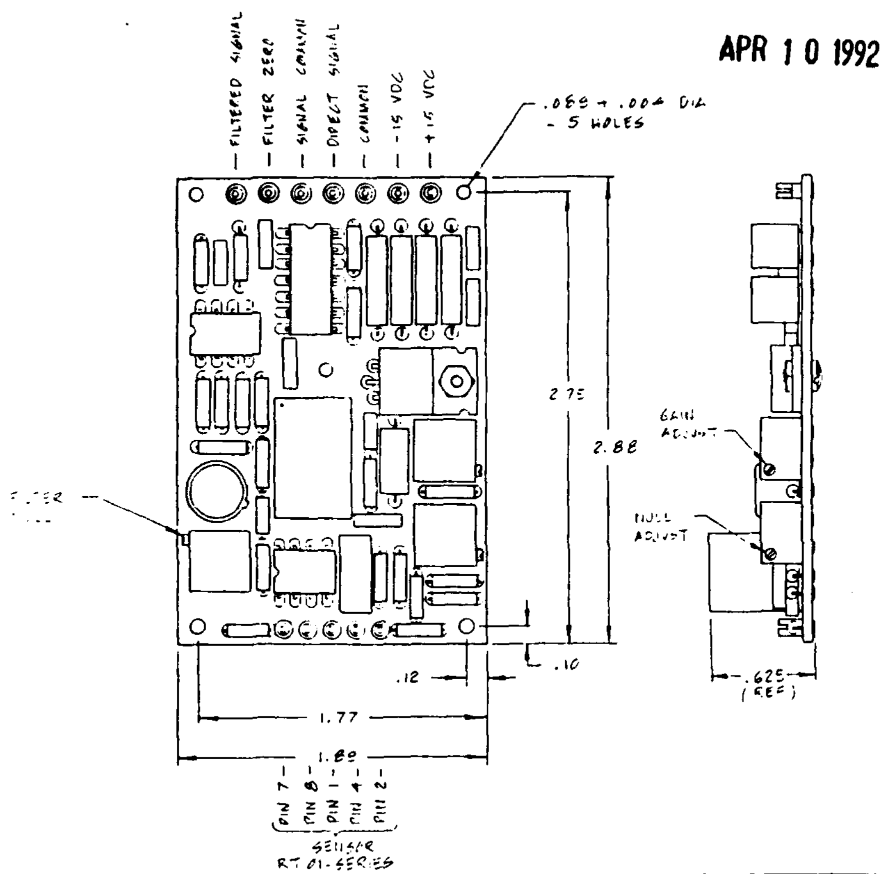
5.0 NOTE: THIS SENSOR ELECTRONICS IS DESIGNED TO FUNCTION WITH THE RT01-SERIES RATE TRANSDUCERS. COMPONENT VALUES AND ADJUSTMENTS ARE MADE SUCH THAT THE SE01/RT01 COMBINATION FUNCTIONS PROPERLY. THE END PRODUCT WILL CONFORM TO THE CONTROLLING SPECIFICATIONS WHICH WILL BE THE SENSOR SPECIFICATIONS MODIFIED BY PURCHASE-ORDER AGREEMENTS. THE NULL-ADJUST AND GAIN-ADJUST (SCALE-FACTOR) CONTROLS ARE READILY AVAILABLE FOR CUSTOMER ADJUSTMENTS.

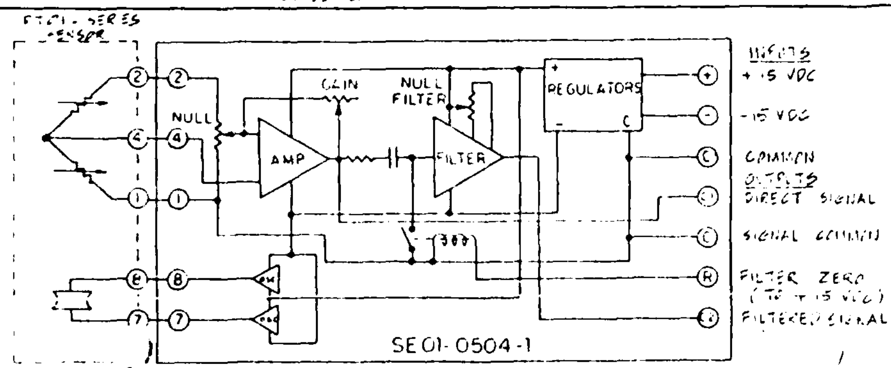
Humphrey Inc. — ELECTRO-MECHANICAL INSTRUMENTS

TITLE: SENSOR ELECTRONICS

SCALE 1/1 — SIZE C — MODEL NO SE01-05 — REV A

APR 1 0 1992





SPECIFICATIONS

1.0 INPUT VOLTAGE ______________ ±15 VOLTS D.C.

2.0 INPUT CURRENT ______________ 100 MILLIAMPS MAXIMUM

3.0 OUTPUT VOLTAGE ______________ ±2.5 VOLTS FULL-SCALE TYPICAL

4.0 OUTPUT SCALE FACTOR ______________ ADJUST PER RT01-SERIES SENSOR BEING USED.

5.0 NOTE. THIS SENSOR ELECTRONICS IS DESIGNED TO FUNCTION WITH THE RT01-SERIES RATE TRANSDUCERS. COMPONENT VALUES AND ADJUSTMENTS ARE MADE SUCH THAT THE SE01/RT01 COMBINATION FUNCTIONS PROPERLY. THE END PRODUCT WILL CONFORM TO THE CONTROLLING SPECIFICATIONS WHICH WILL BE THE SENSOR SPECIFICATIONS MODIFIED BY PURCHASE-ORDER AGREEMENTS. THE NULL-ADJUST AND GAIN-ADJUST (SCALE-FACTOR) CONTROLS ARE READILY AVAILABLE FOR CUSTOMER ADJUSTMENTS.

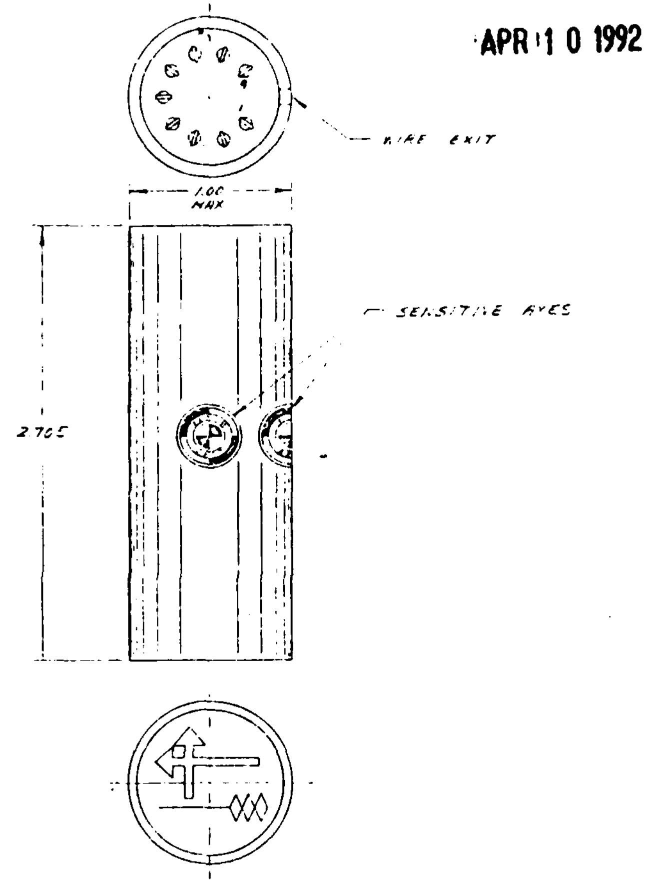
Humphrey Inc. — ELECTRO-MECHANICAL INSTRUMENTS

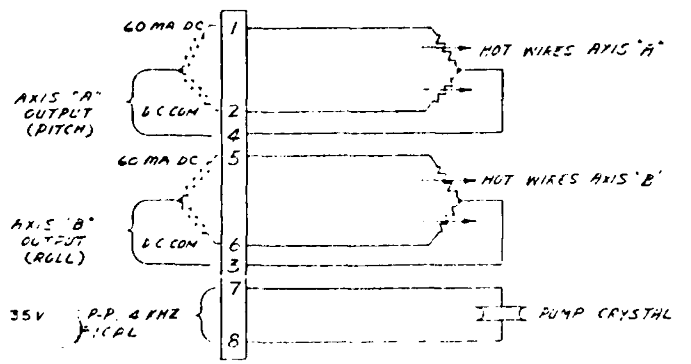
TITLE: ENVELOPE DRAWING SENSOR ELECTRONICS

SCALE: 1/1 — SIZE: C — MODEL NO: SE01-05 -1

?? ROLL RATE

APR 1 0 1992





SPECIFICATIONS

1.0	RANGE RATE	
*1.1	AXIS "A"	±100°/SECOND
*1.2	AXIS "B"	±60°/SECOND
2.0	NATURAL FREQUENCY	25 Hz (90° CROSSOVER)
3.0	DAMPING	NONE (PROVIDE THROUGH SIGNAL AMPLIFIER)
4.0	INPUT EXCITATION	
*4.1	BETWEEN PINS 1 AND 2	60 MILLIAMPS D.C.
*4.2	BETWEEN PINS 5 AND 6	60 MILLIAMPS D.C.
*4.3	BETWEEN PINS 7 AND 8	35V P-P TYPICAL AT 4 KHZ. ADJUST FOR MAXIMUM OUTPUT WITH MINIMUM NOISE.
5.0	OUTPUTS	
*5.1	AXIS "A"	95 MICROVOLTS/°/SEC. TYPICAL
*5.2	AXIS "B"	95 MICROVOLTS/°/SEC. TYPICAL
*5.3	NULL	ADJUST THRU ELECTRONICS
5.4	RESOLUTION	INFINITE
5.5	THRESHOLD	0.05% OF FULL SCALE
5.6	LINEARITY	1% OF FULL SCALE MAX
6.0	TIME TO FULL OPERATION	40 MILLISECONDS
7.0	SEALING	HERMETIC
8.0	FINISH	CLEAR STAINLESS STEEL
9.0	SERVICE LIFE	10,000 HOURS MINIMUM
10.0	STORAGE LIFE	5 YEARS
11.0	WEIGHT	3 OUNCES NOMINAL
12.0	ENVIRONMENTAL CONDITIONS	
12.1	ALTITUDE	UNLIMITED
12.2	SHOCK	10,000G, 11 ±1 MILLISECOND
12.3	VIBRATION	0.06 INCH D.A. OR 15G WHICHEVER LIMITS 20 TO 2000 HZ
12.4	TEMPERATURE (OPERATING)	-55°C TO +85°C
12.5	TEMPERATURE (STORAGE)	-65°C TO +100°C
13.0	REMARKS	
13.1	ITEMS MARKED WITH (*) ARE CHECKED IN PRODUCTION TESTS. OTHER ITEMS FOR REFERENCE MAY BE CHECKED ON ORDER BY QUALIFICATION TESTS.	
13.2	ABOVE PERFORMANCE SPECIFICATIONS ARE OBTAINED WHEN USED WITH COMPATIBLE OSCILLATOR-AMPLIFIER ELECTRONICS.	

CONTROLLED
DRAWING

Humphrey Inc.
ELECTRO-MECHANICAL INSTRUMENTS

TITLE: ENVELOPE DRAWING RATE TRANSDUCER

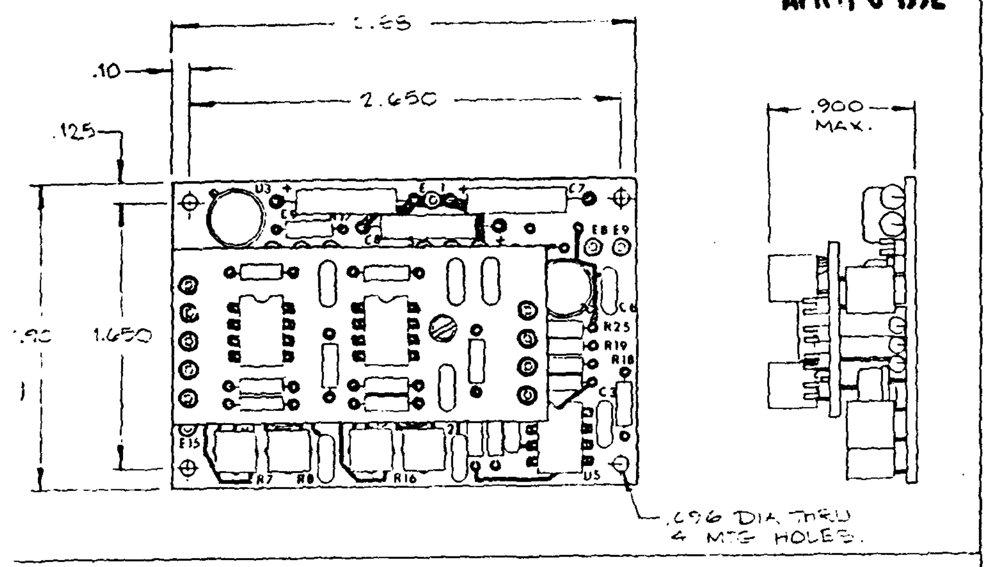
DRAWN BY: J. CHANG

SCALE: 1/1 | DWG SIZE: C | MODEL NO: RT09-0 -1 | REV: A

CUSTOMER REF MATL

APR 1 0 1992

DWG SIZE	MODEL NO	REV
C	SE01-06-01-1 (CODE IDENT NO 98384)	LTR



SPECIFICATIONS

1.0 INPUT VOLTAGE ______ ±15 VOLTS D.C.

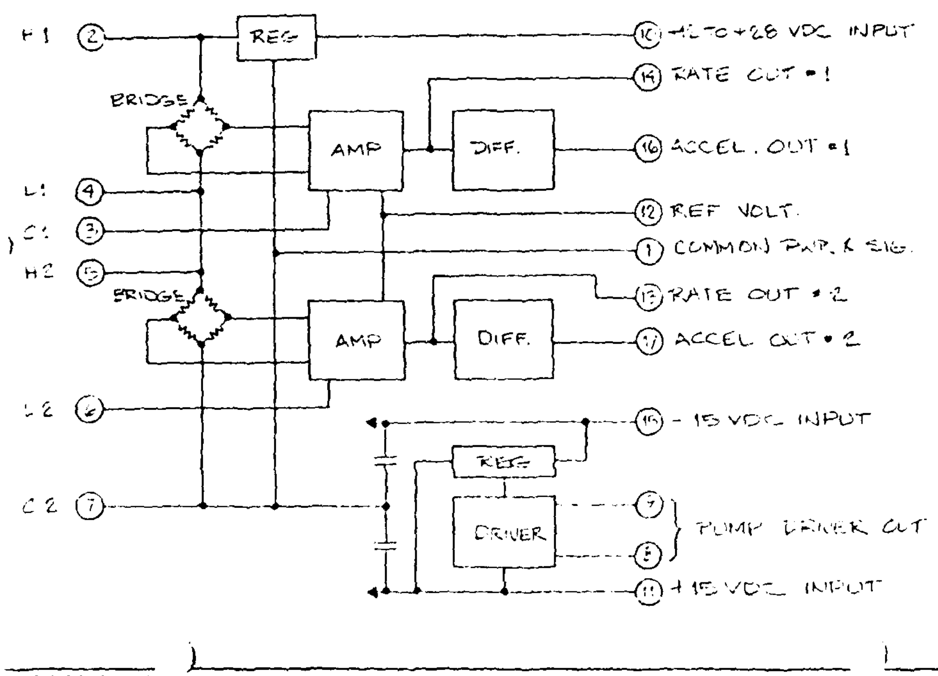
2.0 INPUT CURRENT ______ 200 MILLIAMPS MAXIMUM

3.0 OUTPUT VOLTAGES ______ ±2.5 VOLTS FULL-SCALE TYPICAL - AS REQUESTED BY CUSTOMER.

4.0 OUTPUT SCALE FACTOR ______ ADJUST WITH RT09-SERIES SENSOR BEING USED TO GIVE DESIRED SCALE FACTORS.

5.0 NOTES:

1. THIS SENSOR ELECTRONICS IS DESIGNED TO FUNCTION WITH THE RT09-SERIES RATE TRANSDUCERS.
2. OUTPUT SIGNALS WILL REPRESENT TWO AXES OF ANGULAR RATE-OF-TURN AND TWO AXES OF ANGULAR ACCELERATION.
3. COMPONENT VALUES AND ADJUSTMENTS ARE MADE SUCH THAT THE SE01/RT09 COMBINATION FUNCTIONS PROPERLY.
4. THE END-PRODUCT WILL CONFORM TO THE CONTROLLING SPECIFICATIONS WHICH WILL BE THE SENSOR SPECIFICATIONS MODIFIED BY PURCHASE-ORDER AGREEMENTS.
5. THE NULL-ADJUST AND RATE GAIN-ADJUST (RATE SCALE FACTOR) CONTROLS ARE READILY AVAILABLE FOR CUSTOMER ADJUSTMENTS.
6. ANGULAR ACCELERATION IS DERIVED BY ELECTRONICALLY DIFFERENTIATING THE RATE OUTPUT SIGNALS.



Humphrey Inc. — ELECTRO MECHANICAL INSTRUMENTS

TITLE: SENSOR ELECTRONICS

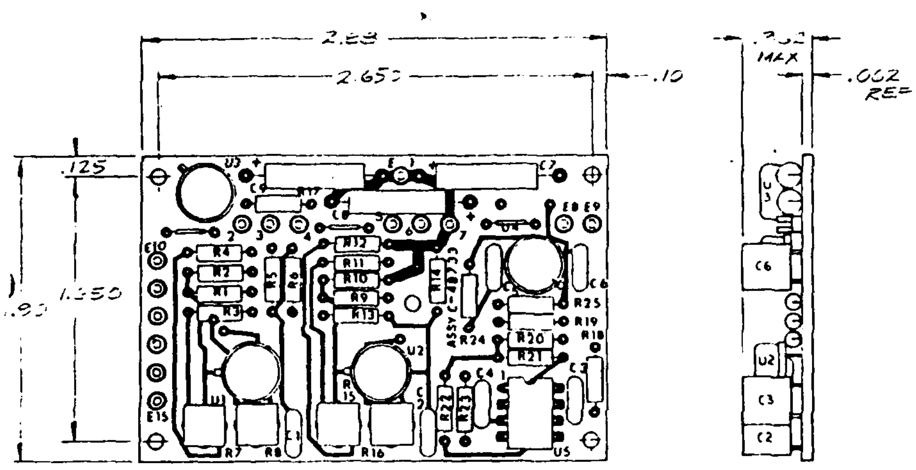
DRAWN BY: SCHWARTZ — E.C. VOGES

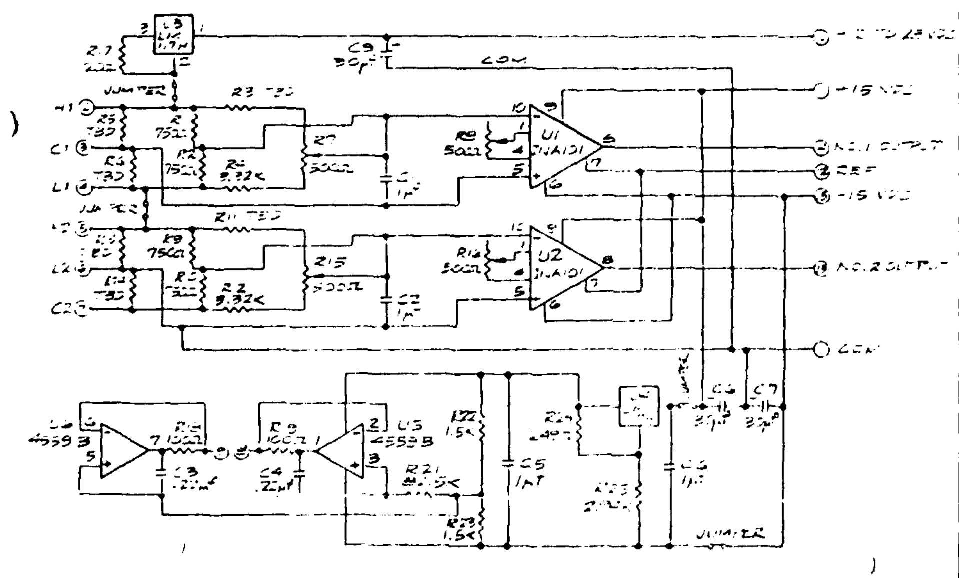
SCALE	DWG SIZE	MODEL NO	REV
1/1	C	SE01-α	LTR

UNLESS OTHERWISE SPECIFIED LIMITS ON DIMENSIONS ARE ...

CUSTOMER REF MATL

APR 1 0 1992





SPECIFICATIONS

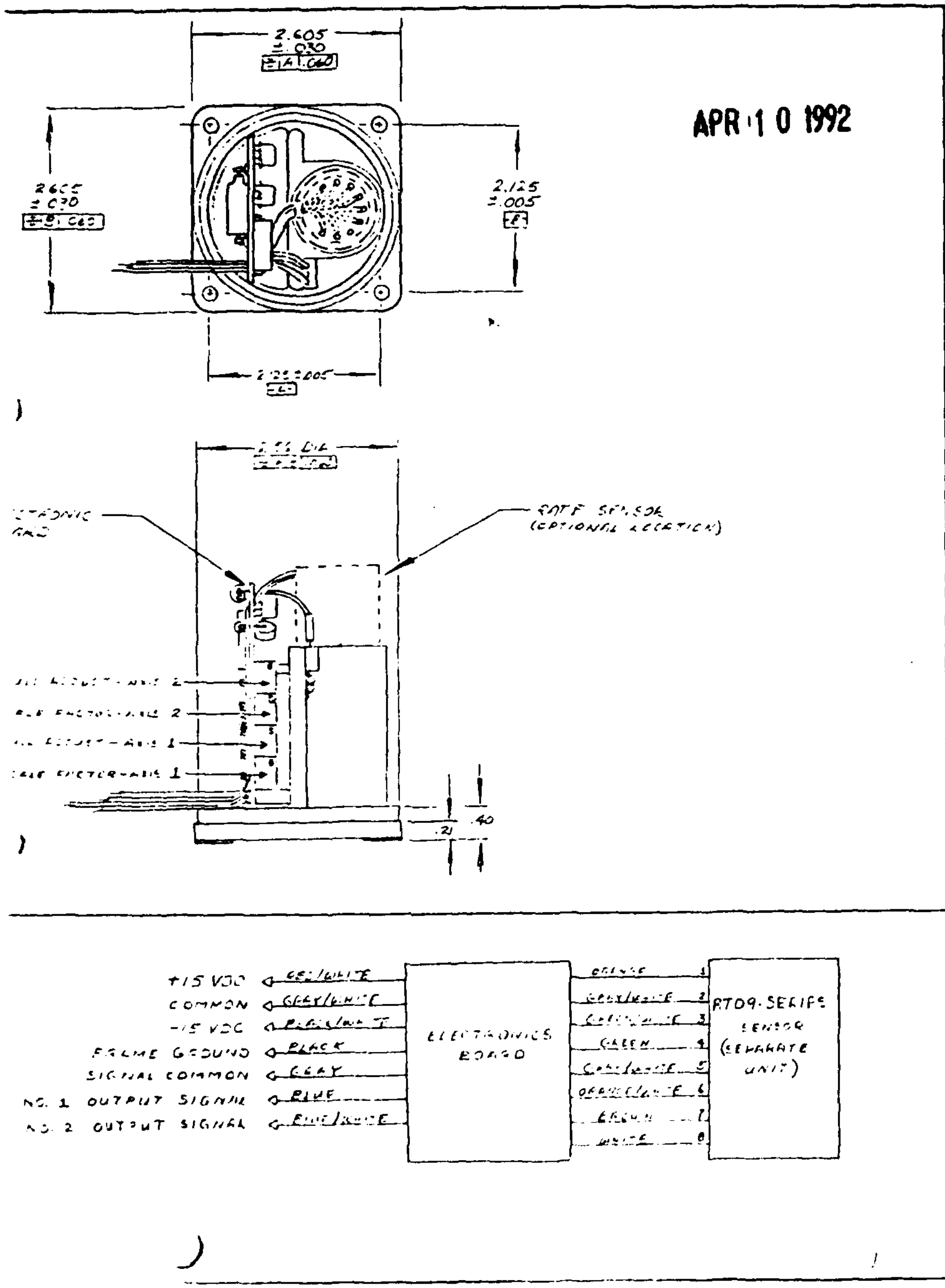
1.0	INPUT VOLTAGE	±15 VOLTS D.C.
2.0	INPUT CURRENT	200 MILLIAMPS MAXIMUM
3.0	OUTPUT VOLTAGE	±2.5 VOLTS FULL-SCALE TYPICAL AS REQUESTED BY CUSTOMER
4.0	OUTPUT SCALE FACTOR	ADJUST WITH R109-SERIES SENSOR BEING USED TO GIVE DESIRED SCALE FACTOR

5.0 NOTE. THIS SENSOR ELECTRONICS IS DESIGNED TO FUNCTION WITH THE R109-SERIES RATE TRANSDUCERS. COMPONENT VALUES AND ADJUSTMENTS ARE MADE SUCH THAT THE SE01/R109 COMBINATION FUNCTIONS PROPERLY. THE END-PRODUCT WILL CONFORM TO THE CONTROLLING SPECIFICATIONS WHICH WILL BE THE SENSOR SPECIFICATIONS MODIFIED BY PURCHASE-ORDER AGREEMENTS. THE NULL-ADJUST AND GAIN-ADJUST (SCALE-FACTOR) CONTROLS ARE READILY AVAILABLE FOR CUSTOMER ADJUSTMENTS

Humphrey Inc. — ELECTRO-MECHANICAL INSTRUMENTS

TITLE: ENVELOPE DRAWING SENSOR ELECTRONICS

SCALE 2/1 — DWG SIZE C — MODEL NO SE01-C — B-1 — REV B



APR 1 0 1992

SPECIFICATIONS

1.0	INPUT VOLTAGE	±15 VOLTS D.C.
2.0	INPUT CURRENT	200 MILLIAMPS MAXIMUM
3.0	OUTPUT	±2.5 VOLTS D.C. (EACH OUTPUT)
4.0	OUTPUT IMPEDANCE	100 OHMS MAXIMUM
5.0	SCALE FACTOR	ADJUSTED TO SPECIFICATIONS OF SENSOR BEING USED

NOTE THIS SENSOR ELECTRONICS IS DESIGNED TO WORK WITH THE RT09 SERIES TWO-AXIS SOLID STATE RATE TRANSDUCERS. RATE-RANGE AND OTHER OPERATIONAL SPECIFICATIONS CONFORM TO PARTICULAR RT09 SERIES MODEL USED.

CONTROLLED DRAWING

Humphrey Inc. ELECTRO-MECHANICAL INSTRUMENTS

TITLE SENSOR ELECTRONICS

DRAWN BY E.S. YOD

MODEL NO SE01-04 -1

CUSTOMER REF MATL

UNLESS OTHERWISE SPECIFIED LIMITS ON DIMENSIONS ARE DECIMAL

Figure 30: Vertical Gyro

SPECIFICATIONS

*1.0	MECHANICAL LIMITS	360° FREEDOM OF ROTATION ABOUT ROLL AXIS. ±80° MINIMUM FREEDOM OF ROTATION ABOUT PITCH AXIS.
2.0	OUTPUT	
2.1	PICKOFF	WIREWOUND POTENTIOMETER OUTPUT PROPORTIONAL TO ANGULAR DISPLACEMENT ABOUT THE ROLL AND PITCH AXES.
2.2	ROLL ELECTRICAL DISPLACEMENT	±90° ±1°
2.3	PITCH ELECTRICAL DISPLACEMENT	±60° ±1°
*2.4	RESISTANCE	5,000 ±5% OHMS
2.5	RESOLUTION	0.2° MAXIMUM
*2.6	LINEARITY	±1.0% OF FULL RANGE
2.7	POWER DISSIPATION	0.50 WATTS MAXIMUM AT +165°F
2.8	CONTACT RESISTANCE	100 OHMS EQUIVALENT CONTACT RESISTANCE PER N.A.S. 710
3.0	ELECTRICAL REQUIREMENTS	
3.1	ERECTION CUTOUT (ROLL)	EXTERNAL
3.2	SPIN MOTOR AND ERECTION	
3.2.1	INPUT VOLTAGE	28 ±2 VDC
3.2.2	CURRENT	1.5 AMP (MAX) STARTING, 800 MA (MAX) RUNNING
4.0	ERECTION RATES	
*4.1	TIME TO ERECT FROM MOTOR OFF CONDITION	3 MINUTES TO WITHIN ±1.5° UNDER STATIC CONDITIONS
4.2	NOMINAL OPERATING ERECTION RATE	9° ±3°/MINUTE OVER TEMPERATURE RANGE
*5.0	VERTICAL ACCURACY	±1.0° OF TRUE VERTICAL UNDER ALL CONDITIONS
*6.0	DRIFT	WITH ROLL ERECTION SYSTEM INOPERATIVE, FREE DRIFT INDEPENDENT OF EARTH'S ROTATION SHALL BE 1.0°/MIN MAXIMUM AFTER 6 MINUTES OF 3° REVERSING SCORSBY ACTION AT 6 CYCLES PER MINUTE, OVER TEMPERATURE RANGE.
7.0	ENVIRONMENTAL	
7.1	VIBRATION LEVEL	VERTICAL ACCURACY TO BE MAINTAINED AT ±1.5° DURING .036 DA (5 - 33 HZ), 2G (33 - 500 HZ) LOGARITHMIC SWEEP FROM 5 - 500 - 5 HZ IN 8 MINUTES
7.2	TEMPERATURE	-45°F TO +150°F
7.3	ALTITUDE	TO 50,000 FT.
7.4	HUMIDITY	100% RELATIVE
7.5	SHOCK	15G, 11 MS ALL AXES
*8.0	INSULATION RESISTANCE	20 MEGOHMS MINIMUM AT 100 VDC
9.0	FINISH	BLACK ANODIZE
*10.0	SEALING	MOISTURE PROOF CASE
11.0	WEIGHT	1.5 POUNDS MAXIMUM
12.0	SERVICE LIFE	200 HOURS
13.0	REMARKS	
13.1	ITEMS MARKED WITH (*) ARE CHECKED IN PRODUCTION TESTS. OTHER ITEMS FOR REFERENCE MAY BE CHECKED ON ORDER BY QUALIFICATION TESTS.	

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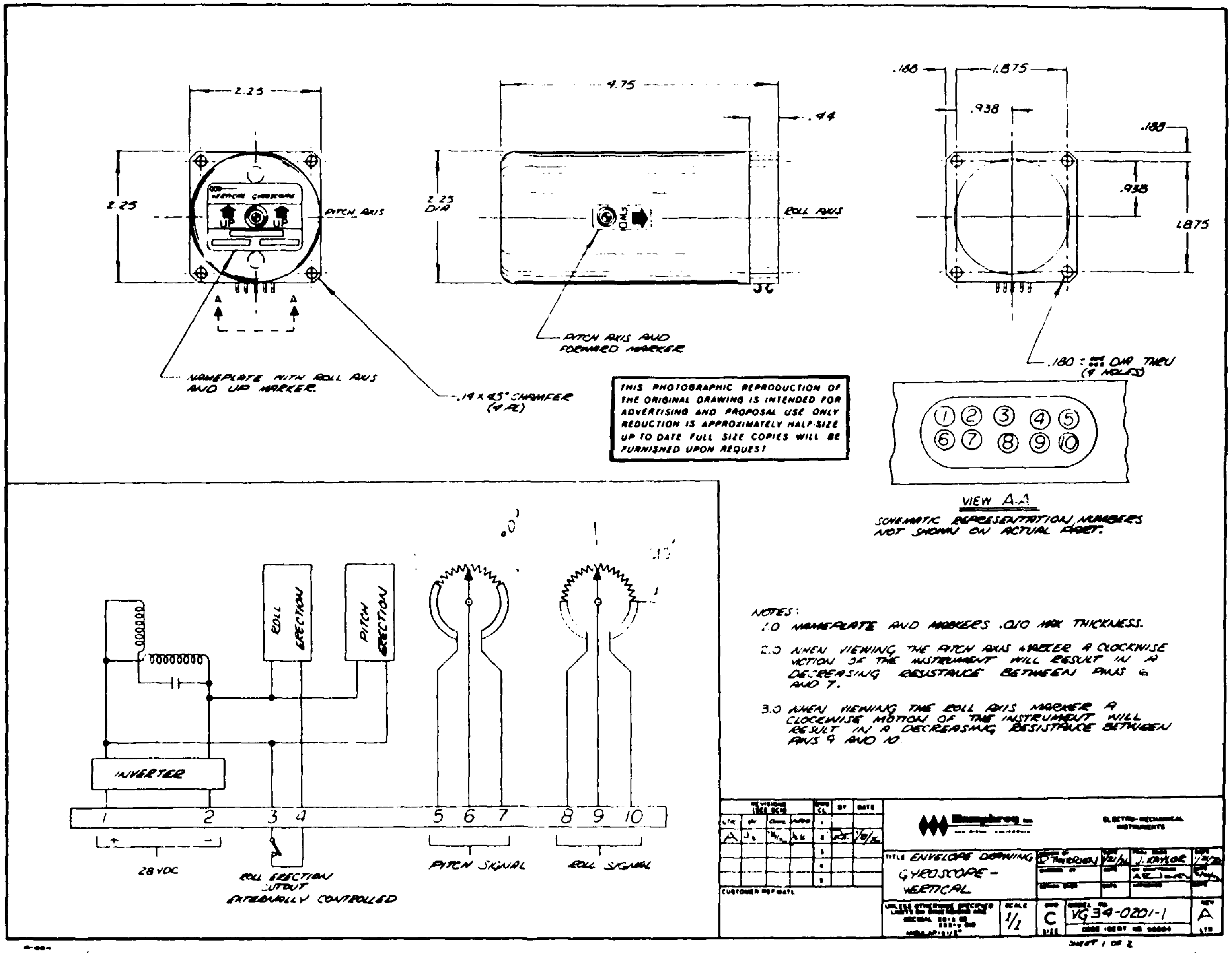
TITLE: ENVELOPE DRAWING GYROSCOPE - VERTICAL	SIZE C	VG34-0201-1	REV A

SHEET 2 OF 2


2.25
PITCH AXIS
NAMEPLATE WITH ROLL AXIS AND UP MARKER.
.14 x 45° CHAMFER (4 PL)
4.75
.44
2.25 DIA
ROLL AXIS
FWD
PITCH AXIS AND FORWARD MARKER
.188
1.875
.938
.180 DIA THRU (4 HOLES)
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VIEW A-A
SCHEMATIC REPRESENTATION NUMBERS NOT SHOWN ON ACTUAL PART.
NOTES:
1.0 NAMEPLATE AND MARKERS .010 MAX THICKNESS.
2.0 WHEN VIEWING THE PITCH AXIS MARKER A CLOCKWISE MOTION OF THE INSTRUMENT WILL RESULT IN A DECREASING RESISTANCE BETWEEN PINS 6 AND 7.
3.0 WHEN VIEWING THE ROLL AXIS MARKER A CLOCKWISE MOTION OF THE INSTRUMENT WILL RESULT IN A DECREASING RESISTANCE BETWEEN PINS 9 AND 10.
ROLL ERECTION
PITCH ERECTION
INVERTER
28 VDC
ROLL ERECTION CUTOUT EXTERNALLY CONTROLLED
PITCH SIGNAL
ROLL SIGNAL
TITLE ENVELOPE DRAWING GYROSCOPE - VERTICAL
ELECTRO-MECHANICAL INSTRUMENTS
SCALE 1/1
SIZE C
VG34-0201-1
REV A
SHEET 1 OF 2

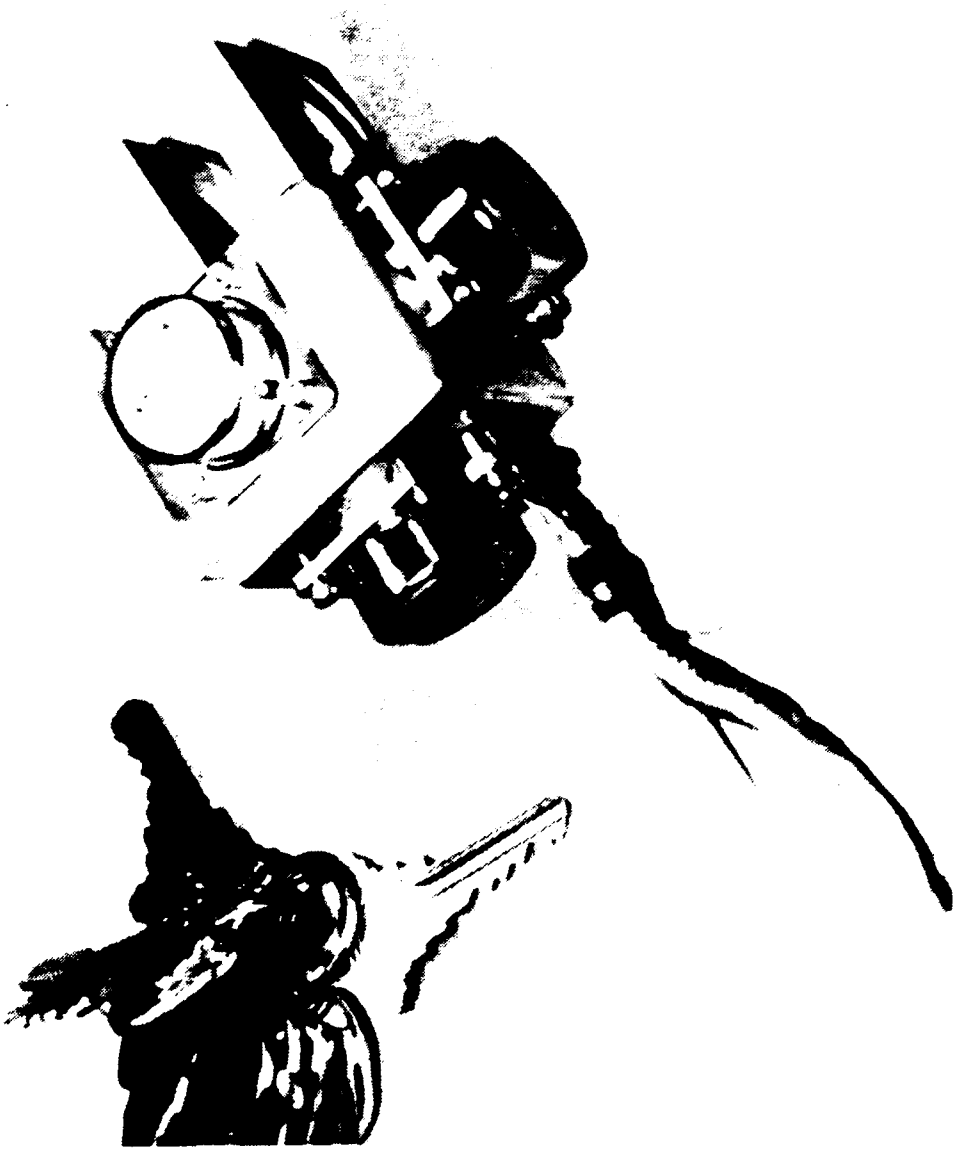


Figure 31: 3-Axis Accelerometer

QA-700 Technical Data

Output Range		±30g
Bias		8mg max
Bias Thermal Coefficient		70µg/°C max
Current Scale Factor		1.3mA/g nom
Scale Factor Thermal Coefficient		200 ppm/°C max
Linearity Error		48µg/g² max
Input Axis Misalignment		7mrad
Resolution Threshold		1µg max
Frequency Response	0-10 Hz	±0.1% max
	10-100 Hz	±4% max
	100-300 Hz	±5% max
Damping Ratio		0.3 to 0.8

ELECTRICAL

Input Voltage	±13 VDC to ±18 VDC
Quiescent Current max	20mA per supply
Isolation, case to all pins	10 megohms at 50 VDC
Temperature Sensor Output*	1µa/°K

*Temperature Modeling available on request

ENVIRONMENTAL

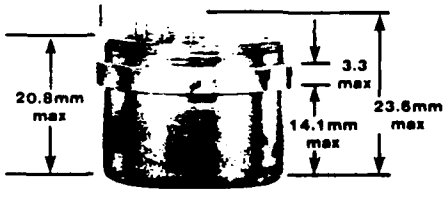
Operating Temperature For Specified Performance	-55°C to +95°C
Storage Temperature	-65° to +125°C
Static Acceleration Overrange Limit	100g peak
Shock Limit	250g peak, 6 msec. half sine
Sine Vibration Limit	25g peak, 50 to 2000 Hz

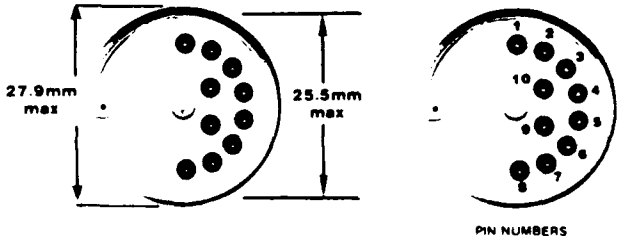
PHYSICAL

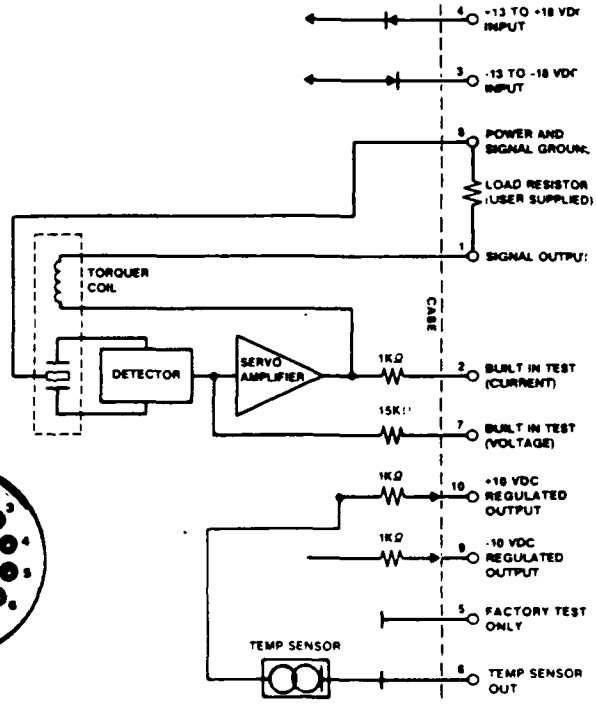
Weight	50 grams max
Case Material	Stainless Steel

MOUNTING

3 or 4 Point Mounting Adapters
Available Upon Request







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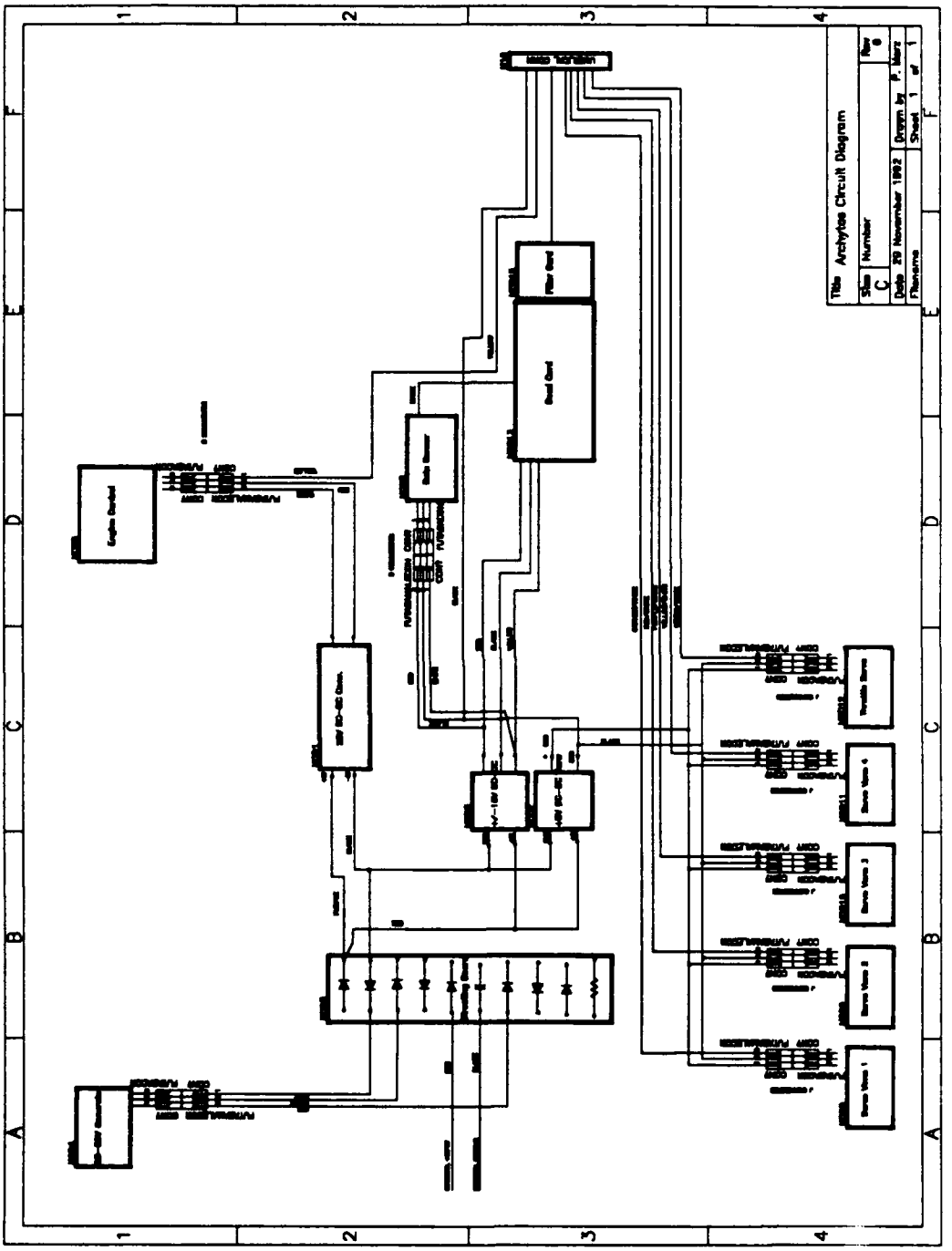
APPENDIX D: WIRING SCHEMATIC



LIST OF REFERENCES

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4. White, J. E., and Phelan, J. R., "Stability Augmentation for a Free Flying Ducted Fan," paper presented at the AIAA Controls Conference, August 1987.

5. Lloyd, S.D., "An Autopilot Design for the United States Marine Corps' Airborne Remotely Operated Device," Master's Thesis, Naval Postgraduate School, Monterey, CA, September, 1987.

6. Bassett, W. G., "A Dynamic Simulation and Feedback Control Scheme for The United States Marine Corps' Airborne Remotely Operated Device," Master's Thesis, Naval Postgraduate School, Monterey, CA, September 1987.

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