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DESIGN AND IMPLEMENTATION
OF A FIBER OPTIC LINK FOR
A TOKEN RING LOCAL AREA NETWORK

by

Thomas J. Doran

September, 1992

Thesis Advisor: John P. Powers

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This thesis describes the design and implementation of a fiber optic link for a token ring local area network (LAN). It features the use of fiber optic channels as the transmission medium between a computer system and a wiring concentrator to convert a physical ring design into a starwired configuration. The LAN was controlled by the TMS380 LAN Adapter chipset, which provided all diagnostic and network management features to include the 4 Mb/s electrical signal for operation. Since this adapter was developed for systems using twisted wire pair adapter cables, design modifications required that the fiber link be able to simulate impedance and current characteristics of copper wire link. This allows the use of adapter diagnostic checks for ring continuity and proper ring operation. Design evaluations using test signals and adapter signals from within the computer-concentrator link showed mixed resulsts. All transmission objectives were met but the circuit loaded down the LAN adapter causing hardware error messages.

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DESIGN AND IMPLEMENTATION OF A FIBER OPTIC LINK
FOR A TOKEN RING LOCAL AREA NETWORK

by

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Captain, United States Marine Corps
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Submitted in partial fulfillment
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ABSTRACT

This thesis describes the design and implementation of a fiber optic link for a token ring local area network (LAN). It features the use of fiber optic channels as the transmission medium between a computer system and a wiring concentrator to convert a physical ring design into a star-wired configuration. The LAN was controlled by the TMS380 LAN Adapter chipset, which provided all diagnostic and network management features to include the 4 Mb/s electrical signal for operation. Since this adapter was developed for systems using twisted wire pair adapter cables, design modifications required that the fiber link be able to simulate impedance and current characteristics of the copper wire link. This allows the use of adapter diagnostic checks for ring continuity and proper ring operation. Design evaluations using test signals and adapter signals from within the computer-concentrator link showed mixed results. All transmission objectives were met but the circuit loaded down the LAN adapter causing hardware error messages.

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I. INTRODUCTION

A. GENERAL

In the electronic age, the ability to gather and share information has become a primary consideration in the design and acquisition of a communication system. Demands for greater data transfer rates and data storage capacity have led to advances in two areas: computer networking and fiber optic communications. The most common form of computer networking is the Local Area Network (LAN). This concept, coupled with the increased capacity for information transfer of fiber optic links, has led to a new and expanding market within the computer field.

1. Advantages of LANs

A Local Area Network is generally defined as a computer network owned by a single organization, having a total data rate of several Mb/s and a diameter of under a few kilometers (but usually limited to a single building or office) [Ref. 2: p. 117]. A LAN offers several advantages to its users, not the least of which is improved access to the data resources [Ref. 2: p. 3]. With each computer workstation tied into the same database, information may be accessed and updated by a user and be instantly available to the entire network.

Another advantage of the LAN is the reliability provided by multiple stations. Files may be stored in several computers, ensuring access in case one source is unavailable. Networking also allows for sharing workloads, so failure of one station can be made up for by spreading functions to other stations. [Ref. 2: p. 3]

Economy also plays a major role in choosing a LAN. Networking allows sharing of peripherals and their high costs, doing away with the need for each computer to have its own support hardware. Software and software updates can also be shared by all network users, lessening the demand for costly backups. [Ref. 7: p. 16]

2. Advantages of Fiber Optics

The continual search for improved data transmission rates has frequently resulted in the choice of fiber optic links over standard coaxial cables. Since 1970, well over 10 million kilometers of optical fiber has been installed around the world in telecommunication links of all types [Ref. 1: p. 7].

Essentially a thin, lightweight strand of ultrapure glass, optical fiber offers wider bandwidths and lower transmission losses than copper wire. This allows more data to be transmitted over greater distances, reducing the number of wires and repeaters required by the system. The small size of each fiber also decreases overall system size and weight,

making it attractive to the military for use in ships, aircraft, and other devices of limited dimensions, such as man-transported equipment. [Ref. 1: p. 5]

Another advantage of optical fibers is derived from the material of which it is constructed. Fibers are strands of glass made principally from silica (SiO_2), and, since glass is an insulator, optical fibers are electrically isolated [Ref. 1: p. 5]. This means fibers are not affected by outside electromagnetic interference from machinery, other power lines, or natural causes, and are not subject to power line surges seen in copper wire cables [Ref. 2: p.65]. This electromagnetic immunity extends to electromagnetic pulse (EMP) effects caused by nuclear blasts, and makes fiber ideal for the military requirement of EMP-hardened equipment, such as communications and fire-control systems [Ref. 1: p. 5].

An additional benefit of optical fibers is the aspect of signal security. With the signal confined to the cable by the cladding, and since it is electrically isolated, data transmitted over the cable is afforded a high degree of security. A tap on the fiber attempting to intercept data could easily be detected by the loss of received signal power [Ref. 2: p. 166]. This has obvious applications within military systems where information security is a major concern, as well as civilian functions such as personnel and financial records [Ref. 1: p. 5].

B. PREVIOUS RESEARCH

The Optical Electronics Laboratory of the Naval Postgraduate School is conducting research in the design of a practical fiber optic Local Area Network. LT Mary Anderson, USN, completed initial work in the area to develop a fiber optic interface module capable of converting a typical electric signal as generated by a LAN into an optical signal [Ref. 10].

Capt Gary Bibeau, USMC, conducted follow-on research resulting in a token-ring fiber optic LAN consisting of two computers linked directly by a fiber optic channel [Ref. 11]. This ring was both a logical and a physical ring with the transmit terminals of one computer linked directly to the receive terminals of the other computer.

C. THESIS OBJECTIVES

The object of this thesis was to continue the research in the design and implementation of a practical fiber optic Local Area Network. Efforts were primarily focused on two areas which presented problems in previous studies. First, we desired a computer-to-channel interface to allow the use of system diagnostics for ring continuity checks. Second, we wanted to convert the link from a physical ring to a star-configured token ring through the insertion of a wiring concentrator to act as central hub of the network. In addition to conversion to a star configuration, efforts were

made to modify the transmission channel to single transmit and receive lines in place of the differential pairs present in a wire cable. The network was to use commercially available networking software and token ring network system boards.

D. THESIS ORGANIZATION

Chapter II provides background information on Local Area Networks, including the basic Open System Interconnection (OSI) model and the IEEE Standard 802.5 token ring system. It also includes information on the wiring concentrator and the TMS-380 LAN Adapter chipset, with an emphasis on the system diagnostics within the ring insertion process.

Chapter III discusses the design requirements as determined by the study of the wiring concentrator and system diagnostics. It continues by detailing the design and construction of each network component along with its performance characteristics and offering an evaluation of the complete fiber link

Chapter IV offers conclusions and recommendations concerning this research and for follow-on work in this area.

II. LOCAL AREA NETWORKS

A. BACKGROUND

As defined previously, a local area network is comprised of computers and supporting hardware located within close proximity to each other (less than a few kilometers) and linked by some form of transmission media. Many workspaces are equipped with LANs to profit from the advantages they offer. To encourage world-wide compatibility between the increasing number of LANs, it was clear that some form of standard networking procedures was required.

1. The OSI Reference Model

The International Standards Organization (ISO) proposed a model for networks which has evolved into the ISO Open Systems Interconnection (OSI) Reference Model [Ref. 2: p. 14]. This model does not act as a standard for network architecture specifying services and protocols; rather, it provides a definition of what each of seven network layers should be able to do. Figure 2-1 shows the seven layers of the OSI model and their relationship to one another. Information transfer between two network elements begins at the top of the model, working its way down the model hierarchy to the physical layer. From the physical layer of the sending element, the information is conveyed over the transmission

media to the physical layer of the receiving element, where it makes its way back up the model hierarchy to the top layer for use. [Ref. 6: p. 1-2]

This thesis was concerned with the actual transfer of information within the model and is driven by the choices of the transmission medium and the networking standard. The study of this transfer covered primarily the two lowest layers of the OSI model, the Physical layer and the Data Link layer.

2. IEEE Standard 802

In addition to the model put forth by the ISO, the Institute of Electrical and Electronic Engineers (IEEE) has defined several standards for local area networks which are

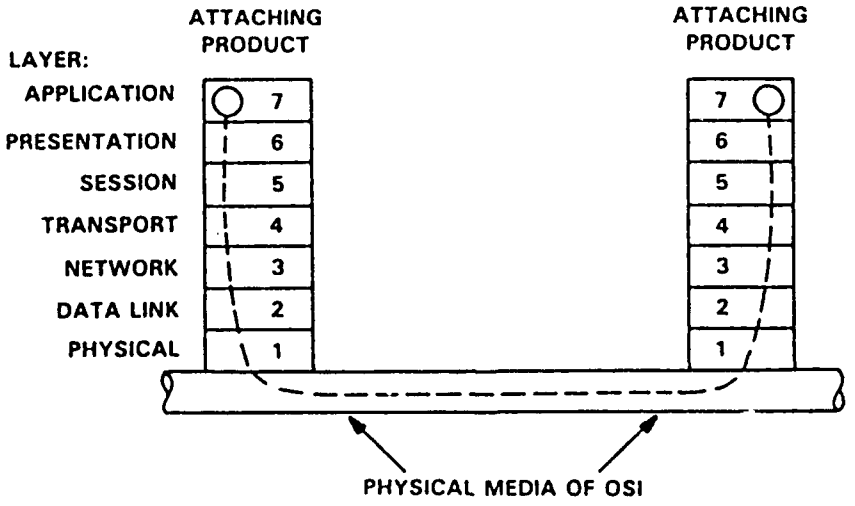


Figure 2-1. The OSI Reference Model
[from Ref. 6: p. 1-2]

based on the OSI model. These standards are known as IEEE Standard 802 and define a set of LAN standards and protocols for the two lowest layers of the OSI model. The Physical layer includes the mechanical, electrical, and procedural interfaces between the product and the transmission medium [Ref. 2: p. 15]. The Data Link layer includes the format for data transmission and procedures for controlling access to the network. IEEE Standard 802 breaks down the Data Link layer further by dividing it into sublayers: the Logical Link Control (LLC) and the Medium Access Control (MAC). The IEEE 802 Standards are shown in Figure 2-2. [Ref. 6: p. 1-2]

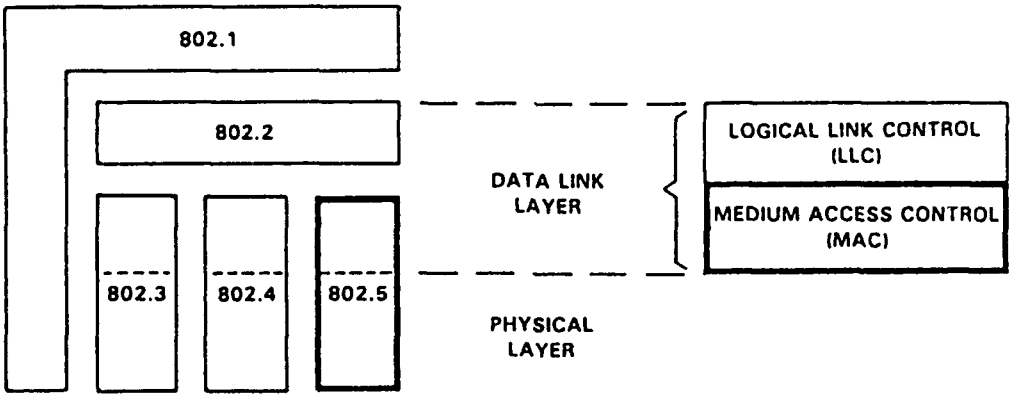


Figure 2-2. IEEE 802 LAN Standards
[from Ref. 6: p. 1-3]

The IEEE Standard 802.5 depicted in Figure 2-2 describes the network protocol for a token ring network. This standard is the basis for the research conducted for this thesis.

B. IEEE STANDARD 802.5 AND THE TOKEN RING NETWORK

A ring network consists of a number of computer workstations connected serially by a transmission medium to form a closed loop. Figure 2-3 shows several examples of token network topologies to include a ring. Systems transmit data around the link from station to station, bypassing inactive stations and with active stations receiving and regenerating each data bit as required. A token ring network, such as that described by IEEE Standard 802.5, uses a token to control access to the transmission channel. [Ref. 3: p. 24]

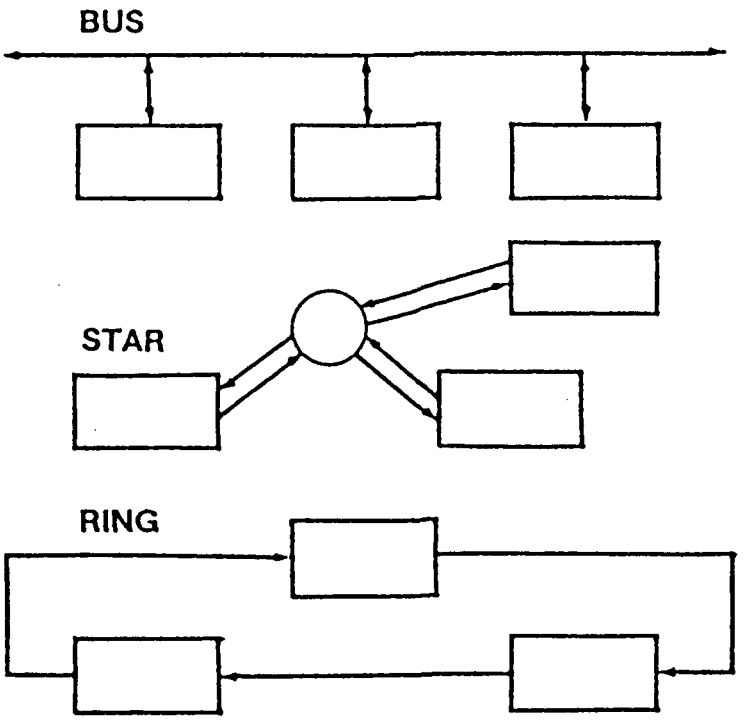


Figure 2-3. Network Topologies
[from Ref. 8: p. 35]

A token is a bit pattern which circulates around the ring giving each station an opportunity to transmit data upon receipt. The token format is included as Figure 2-4(a). It is comprised of three fields, each one byte long. The fields are listed below in order of transmission:

- Starting Delimiter (SD) - marks beginning of frame
- Access Control (AC) - token, monitor and priority bits
- Ending Delimiter (ED) - marks end of frame

The format for the data frame is shown in Figure 2-4(b). In addition to the three fields contained within the token, the data frame has the following additional fields:

- Frame Control (FC) - designates frame type
- Destination Address
- Source Address
- Data Field - contains message information
- Checksum - detects transmission errors
- Frame Status (FS) - holds acknowledgement of receipt

The process for transmitting information is shown in Figure 2-5. It begins with a station identifying a need to transmit a certain amount of data to another station on the ring (Figure 2-5a). When ready to transmit, it captures the token and sets the token status bit within the access control byte to indicate a frame. Setting the token status bit communicates to other stations on the net that a station is

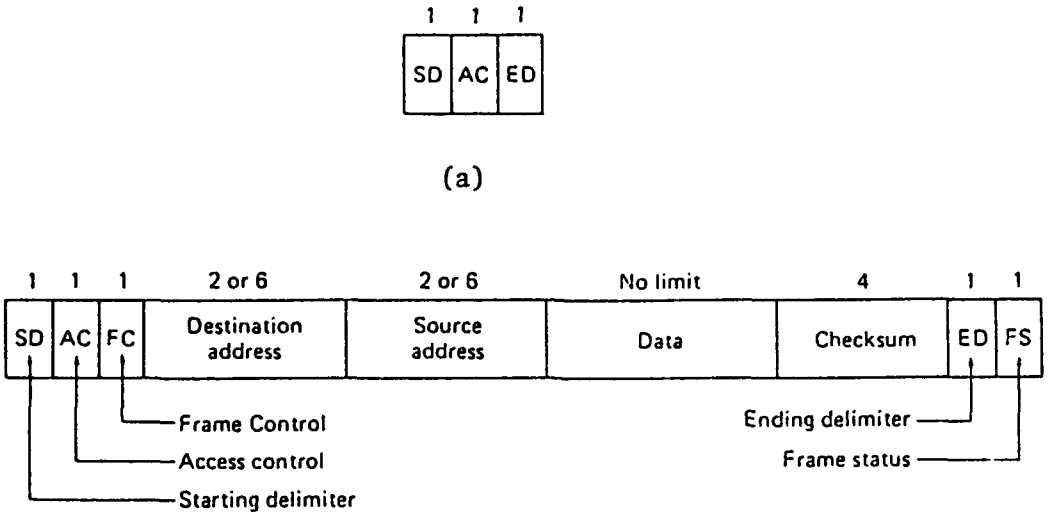


Figure 2-4. Token and Data Frame Formats
[from Ref. 2: p. 157]

transmitting, ensuring that no collisions will occur between two or more stations attempting to transmit. At the same time, the sending station adds address information and the information to be transferred and begins transmitting the frame (Figure 2-5b). Stations on the ring examine the token status bit to determine token availability, and then the destination address to see if the information is being sent to them. If they are not the addressee, then the frame is repeated on the medium.

When a station identifies a frame as being addressed to itself, it copies the data and sets the proper bits within the Frame Status byte (Figure 2-5c). It then regenerates the message and places it back on the medium. Upon recognizing

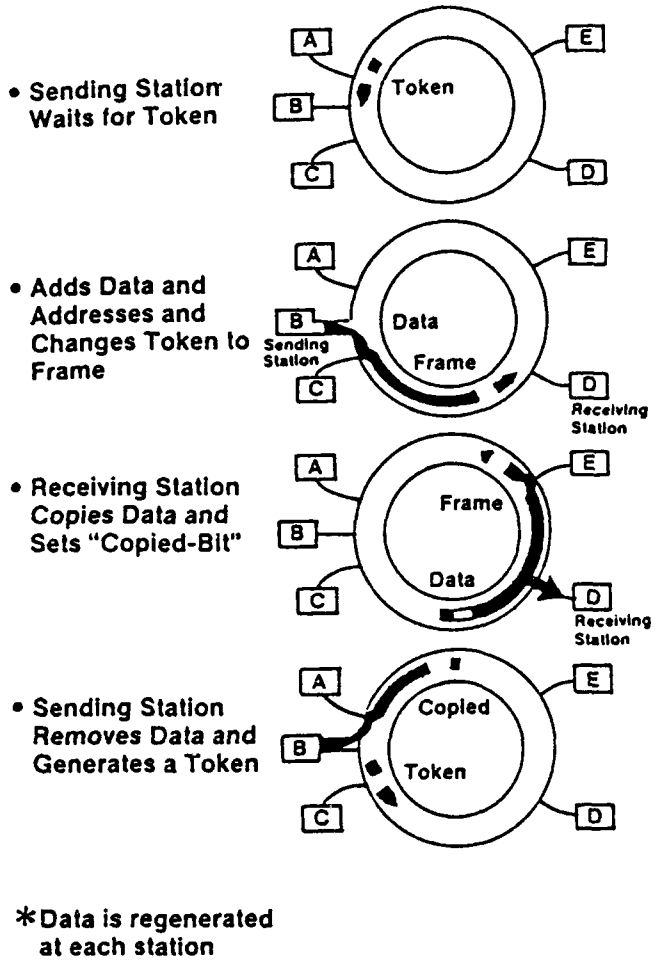


Figure 2-5. Data Transmission Sequence
[from Ref. 9: p. 27]

its original message, the sending machine removes the frame from the medium and generates a token, placing it back on the medium to circulate (Figure 2-5d). This process is the basic token ring protocol as described by IEEE Standard 802.5. A more complete account of this process to include error detection and ring management may be found in the work previously outlined in Reference 11.

C. THE WIRING CONCENTRATOR

IEEE Standard 802.5 outlines the basic protocol for a token ring network without specifying a standard ring design. To improve reliability and maintainability, however, most network applications use a star-wired configuration. In a point-to-point ring wired network, a break in a transmission cable can cause a loss of operation. A star-wired ring uses a wiring concentrator (also called a wiring center or a Multiple Access Unit (MAU)) as a central node, with each station connected to the concentrator by means of a cable made of two twisted wire pairs. Figure 2-6 shows an example of this network layout. [Ref. 2: pp. 156-157]

The cables used to connect systems into the concentrator are shielded differential-pair wires with a transmit and a receive pair, each with a (+) wire and a (-) wire. This design is used because the opposite currents present in each pair will result in any inductance effects being cancelled out.

The wiring concentrator consists of a series of ports which contain switches or bypass relays that can be closed to insert a station into the ring. The switches are thrown by a DC current provided by the work station. If the DC current is not present, the switches are not closed and the station is not part of the ring. Examples of inserted and deinserted stations are shown in Figure 2-7. Information traveling on the network bypasses a station which has not been inserted

into the ring, decreasing transmit time by decreasing path length. This also results in the improved reliability of the ring. A break occurring in a cable connecting a station to the concentrator will prevent the DC current from flowing and the station from entering the ring. This isolates the problem area and keeps the rest of the ring functioning. [Ref. 2: pp. 156-157]

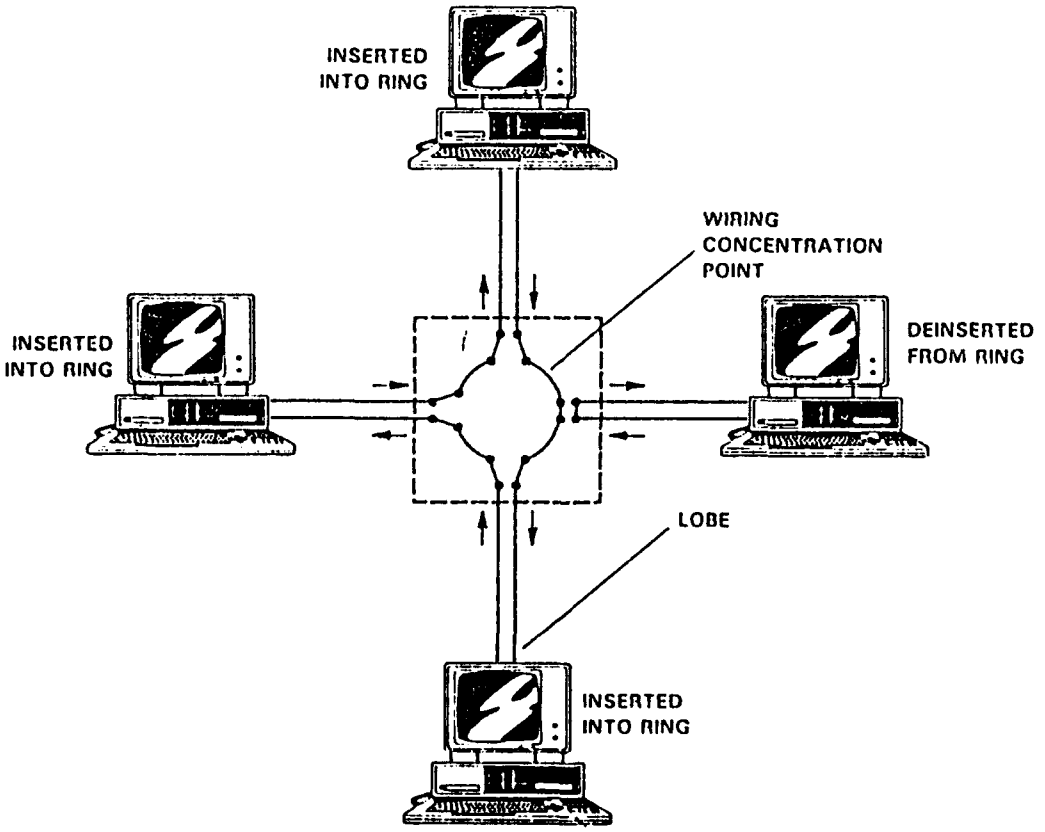


Figure 2-6. Star-wired Network Configuration
[from Ref. 6: p. 4-2]

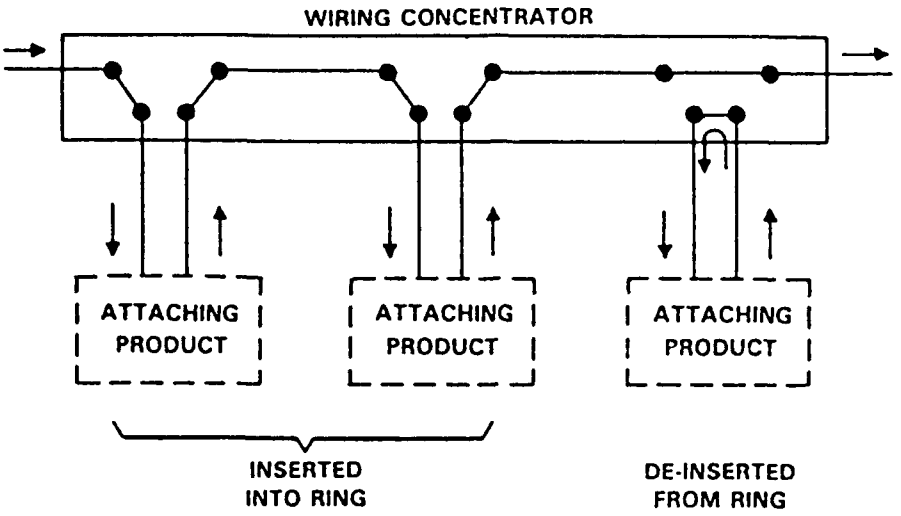


Figure 2-7. Token Ring Wiring Concentrator [from Ref. 6: p. 1-4]

D. TMS380 LAN ADAPTER CHIPSET

The network system used in this study was the National Cash Register (NCR) token ring system. This system is based on the Texas Instruments TMS380 LAN adapter chipset which uses an IEEE Standard 802.5-compatible token-passing access technology. The chipset combines high data rates with high reliability by matching a 4 Mb/s. data-transfer rate with dedicated error-checking circuits, on-chip diagnostics and error-monitoring, and other management features. [Ref. 6: p. 1-1]

Figure 2-8 shows the architecture of the adapter chipset. The TMS380 unites all the functions of an adapter on a single

card in the form of a five-chip set [Ref 6: p. 1-7]. The components of the chipset include:

1. The **TMS380 System Interface** chip provides up to 40 Mb/s of data to the host system through DMA bus transfers.

2. The **TMS38010 Communications Processor** chip provides a dedicated 16-bit CPU with 2.75 kilobytes of on-chip RAM. It executes the adapter software within TMS38030, performing instuctions received from the protocol handler and manipulating data within the memory through the system interface.

3. The **TMS38020 Protocol Handler** performs hardware based protocol functions for a 4 Mb/s IEEE 802.5 standard token ring LAN. It also has 16 kilobytes of on-chip ROM containing the adapter software to support diagnostic and LAN management services.

4. The **TMS38051** and **TMS38052 Ring Interface** chips contain the circuits to connect the chipset to 4 Mb/s token ring LAN via separate transfer and receive lines.

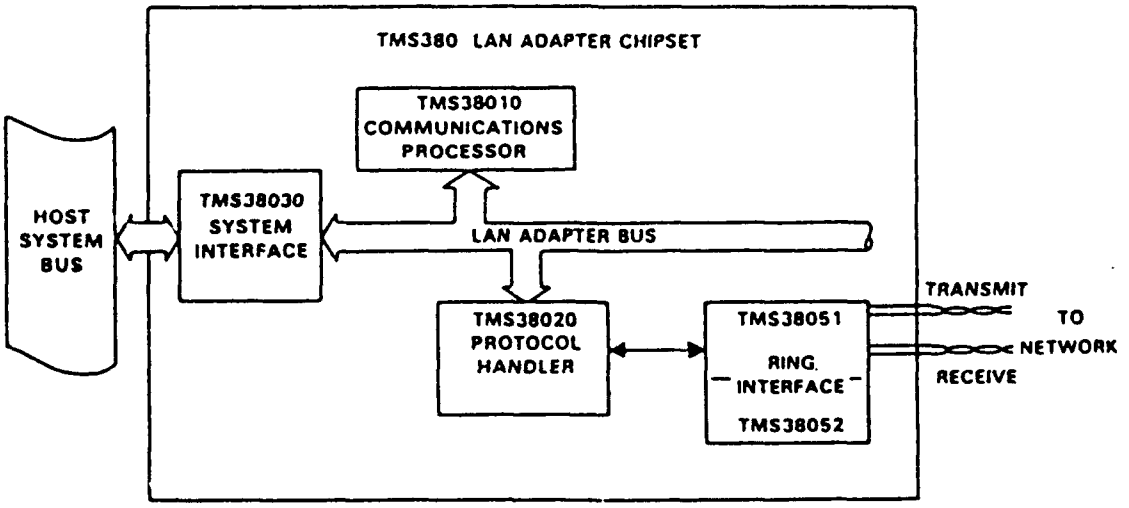


Figure 2-8. TMS380 LAN Adapter Chipset
[from Ref. 6: p. 1-7]

E. RING INSERTION PROCESS

The TMS380 adapter chipset contains the necessary hardware and software features to ensure a successful and reliable insertion of the system to the network. Information on the insertion process chipset presented in this section was obtained from Reference 6. The Ring Insertion process follows the Bring-up diagnostics and Initialization and is initiated with an OPEN command by the system. The adapter chipset then performs an initial self-check, with the Communcations Processor conducting tests on the circuitry of the Protocol Handler and the Ring Interface, as shown in Figure 2-9a. This test verifies operation of the chipset, ensuring that there are no faults within the adapter card. Upon completion of the self-check, the chipset then begins the five phases of the insertion process:

- Phase 0 - Lobe Media Check
- Phase 1 - Physical Insertion
- Phase 2 - Address Verification
- Phase 3 - Participation in Ring Poll
- Phase 4 - Request Initialization

The successful completion of the adapter self-test and the five phases of the insertion process results in the system being "logically" inserted into the ring, allowing participation within the network. [Ref. 6: p. 3-45]

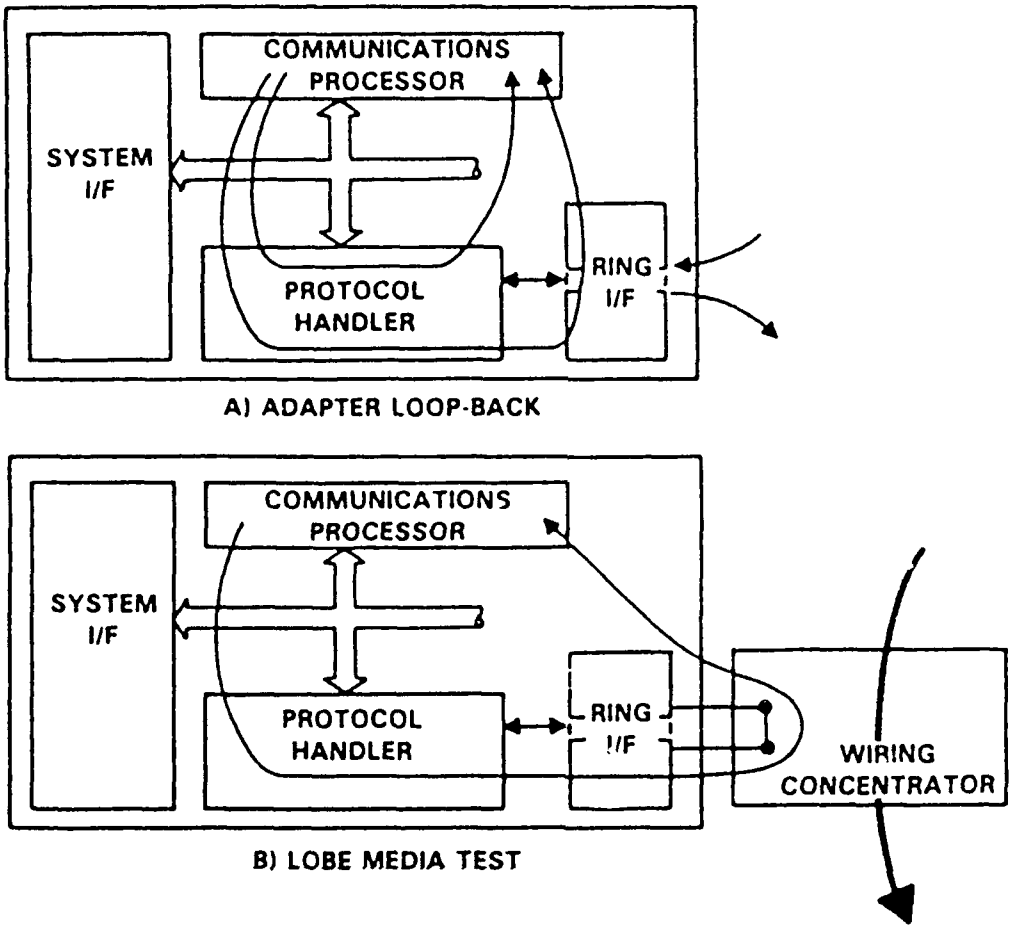


Figure 2-9. Adapter Self-tests
[from Ref. 6: p. 1-9]

1. Sequence of Insertion Process

a. Phase 0 - Lobe Media Check

The Lobe Media Check is a test of path integrity. At the beginning of the insertion process, the adapter has not been physically inserted into the ring. The Adapter proceeds to open a path from the Communications Processor through the Protocol Handler and Ring Interfaces, and on through the

transmission medium and wiring concentrator. This path is shown in Figure 2-9b. A token is then transmitted onto the medium. Token capture and transmission of a test frame must occur within 40 milliseconds or the adapter will make a second attempt by retransmitting the token. A second failure at token capture results in an unsuccessful insertion into the ring and a hardware error message to the user. A successful token capture and subsequent test frame transmission and receipt results in the adapter proceeding to Phase 2 of the process. [Ref. 6: p. 3-47]

b. Phase 1 - Physical Insertion

In this phase, the adapter physically inserts the system into the ring. The adapter impresses a DC current onto both transmit lines, which activates the bypass relays within the wiring concentrator. This connects the transmit and receive lines, opening the complete path. The DC current generated by the adapter, called the Phantom Drive, will be discussed further in the next section.

With the physical insertion complete, the adapter then checks for the presence of an active ring monitor. If no monitor is present, the adapter begins the Monitor Contention Process to initiate contention for ring monitor. After the contention process has been completed and one adapter has been declared the monitor, the adapter determines the presence of the monitor and continues with the next phase of the process.

If either of these events, the physical insertion or Active Monitor verification, do not occur, the system is deinserted from the ring and an error message is sent to the user. [Ref. 6: p. 3-47]

c. Phase 2 - Address Verification

The purpose of the Address Verification phase is to ensure that the ring address assigned to the system is unique. To accomplish this, the adapter sends a series of test frames addressed to itself onto the ring. If the adapter receives two of the test frames with no indication of a duplicate address (i.e., the Address Recognized bit is not set), the adapter assumes that there is not a duplicate address and continues the insertion process. If two frames are received which do show that a duplicate address exists, the adapter deinserts the system from the ring and sends a Duplicate Address error code to the user. [Ref. 6: p. 3-48]

d. Phase 3 - Participation in Ring Poll

To ensure that each station knows the destination address of its upstream neighbor in the ring, the ring monitor conducts the Ring Polling process. This process is conducted at seven second intervals and allows each station's adapter to acquire the upstream neighbor's address and to provide its address to the downstream neighbor. In case of signal loss or a delay of over 18 seconds before receipt of the polling frame, the adapter will deinsert the system from the ring and

send the user a signal loss or a ring failure error message. Otherwise, the adapter continues to the next phase of the insertion process. [Ref. 6: pp. 3-49 - 3-50]

e. Phase 4 - Request Initialization

The purpose of this final phase of the process is to provide a means of requesting additional operational parameters to replace default parameters. The adapter sends a request for initialization onto the ring. If a ring monitor is present, it will send the necessary parameters to station. If no monitor is present, the requesting station sets the default parameters. In either case, the system has successfully completed the insertion process. If the request for initialization is returned but no information is received within 2.4 seconds, it is retransmitted up to four additional times. No response results in the adapter deinserting the system and sending a Request Initialization error code to the user. [Ref. 6: pp. 3-50 - 3-51]

2. Phantom Drive

Phase 1 requires a DC current to be impressed on the transmit wires in order to physically insert the system onto the ring. This DC current is called the Phantom Drive, referring to the fact that the DC voltage levels are transparent to the system voltages which carry the transmitted information. The circuitry which provides the Phantom Drive is integrated into the TMS38052 Ring Interface Controller.

The DC voltage level of 5 volts, which is superimposed on the signal, results in a DC current, and this current passes through the transmission medium to the wiring concentrator. At the wiring concentrator, the DC current activates the bypass relays to physically insert the system into the ring and then returns to ground through an inductor on the receive side of the adapter. The complete Phantom Drive path is shown as Figure 2-10. [Ref. 6: p. 4-128]

Once the ring has been physically inserted into the ring, the Phantom Drive acts as a test for ring continuity. With the DC voltage placed on the PHOUTA and PHOUTB pins of the TMS38052 chip, the DC current to insert the system into the ring is generated. This current is then monitored by the adapter to detect a wire fault condition [Ref. 6: p. 4-128]. An abnormally high drive current would signal an open circuit, meaning a break in a cable. A low drive current would signal a short circuit, pointing to a hardware fault draining current to ground. Each case would result in the adapter deinserting the system from the ring by discontinuing the Phantom Drive and sending a hardware error message sent to the user. [Ref. 6: p. A-110]

The load conditions which are recognized by the adapter in making the determination of a wire fault condition are seen in Figure 2-11. Loads R_{L1} and R_{L2} in the figure are measured from PHOUTA and PHOUTB to ground, respectively. If

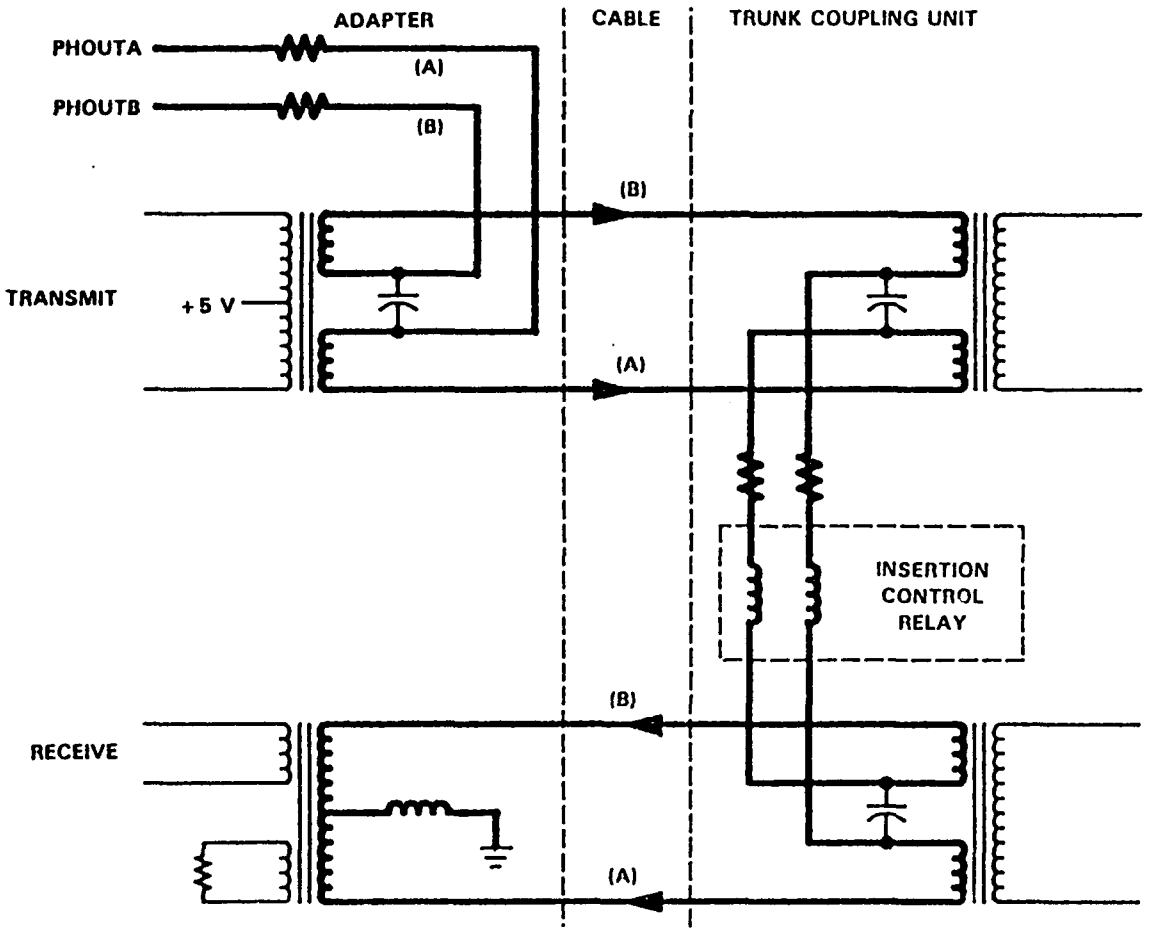


Figure 2-10. Phantom Drive Path
[from Ref. 6: p. 4-128]

either pin detects a load greater than 9.9 kΩ to ground, the adapter will determine an open circuit exists. For a load less than 100 Ω, a short circuit will be recognized. An indeterminate condition exists for loads between the regions of 100 Ω and 2.9 kΩ and 5.5 kΩ and 9.9 kΩ. This leaves a region between 2.9 kΩ and 5.5 kΩ in which the desired load condition for operation exists, allowing the system to be inserted into the ring.

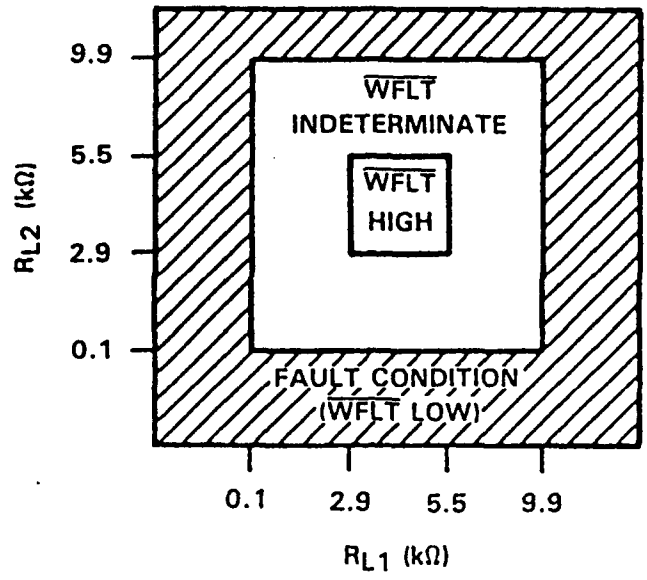


Figure 2-11. Wire Fault Conditions
[from Ref. 6: p. A-110]

The examination of the Phantom Drive completed the study of the background information of token rings and the TMS380 Adapter chipset. The next step of this thesis was to study the available equipment and how the information gathered in this chapter will affect network design.

III. SYSTEM DESIGN

A. DESIGN REQUIREMENTS

Two separate token ring LAN configurations existed at the time research was commenced. The basic commercial system consisted of a star-wired configuration with these components:

- Two IBM XT clone personal computers.
- Two NCR Token Ring LAN adapter cards (installed).
- Wiring concentrator.
- Two twisted pair token ring adapter cables.

Subsequent modifications to the basic design resulted in a system configuration with only the two XT computers connected with a fiber optic link, replacing the wire adapter cables and wiring concentrator. This resulted in a physical ring between the two computers. Figure 3-1 shows the block diagram of this all-fiber network as designed by Bibeau [Ref. 11].

With these two system designs in hand, the first phase of this thesis was to determine the design specifications which must be met by any further modifications to ensure concurrence with IEEE Standard 802.5. IEEE 802.5 defines several specifications for a token ring network to include symbol coding and timing, electrical and mechanical characteristics of the system interface and cable, and link reliablity. Any

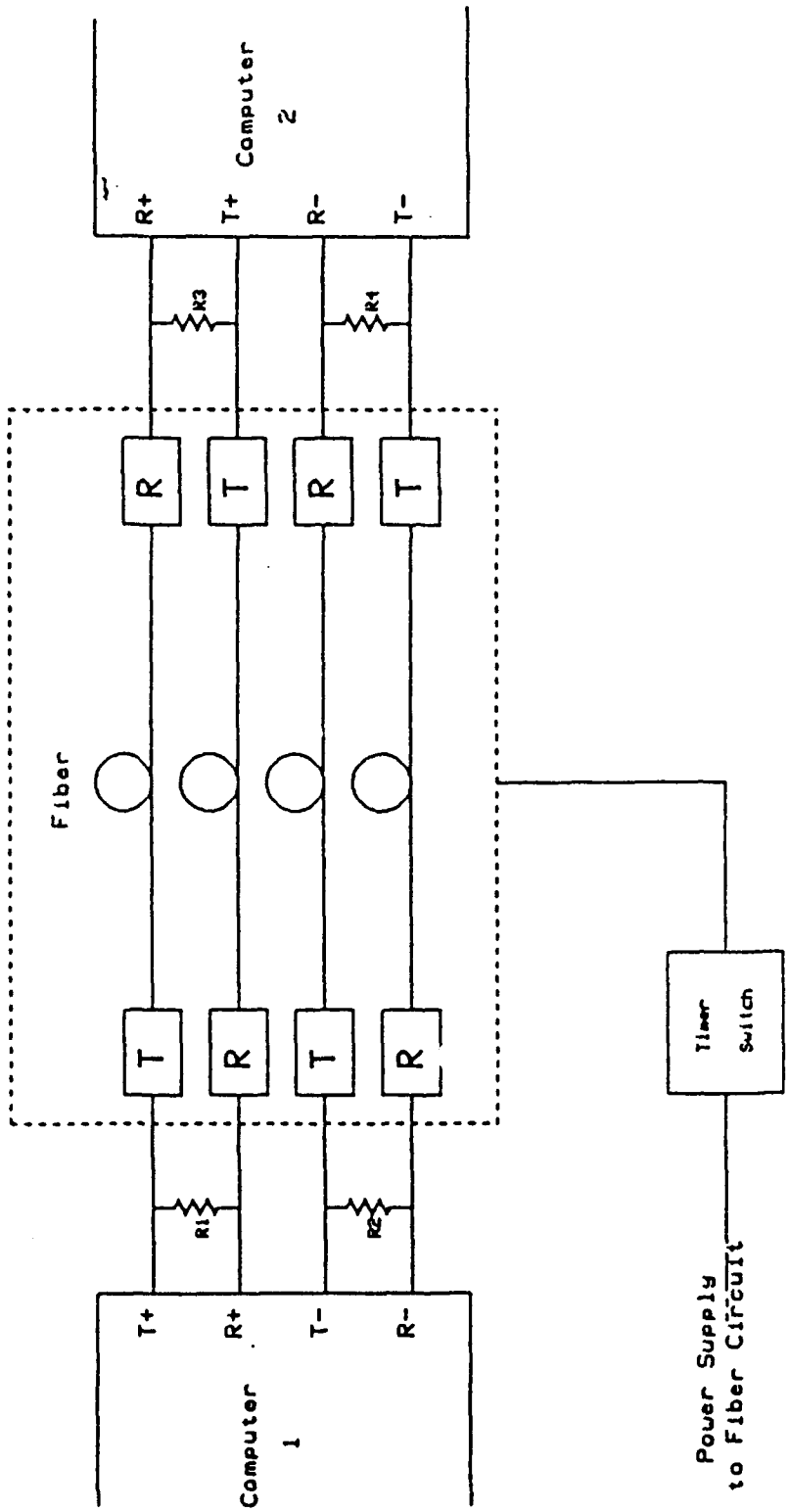


Figure 3-1. Block Diagram of Existing Network [from Ref. 11: p. 54]

attempts to modify the existing designs within these areas had to made with the thesis objectives in mind:

- Configure the ring as a star-wired network with a single transmit and receive line.
- Allow full use of system diagnostics.

To achieve these objectives, modifications would only be considered within the Physical layer (the system interface and transimission medium), with attention being paid to specifications in the Data Link layer as required to ensure a functional system.

1. Transmitted Signal Characteristics

Although rated at 4 MBaud, the TMS380 adapter chipset uses Differential Manchester coding as specified in IEEE 802.5. An example of this coding scheme is shown in Figure 3-2. Differential Manchester requires a midbit transition which effectively doubles the required transmission bandwidth. It also tests for a transition at the start of a bit transmission, with a "zero" bit being represented by a transition at the start of the interval and a "one" bit being represented by no transition. [Ref. 3: p. 73]

Another specification dealing with the signal defines the limits of the pulse shape. The Differential Manchester coding scheme used by the adapter relies on a square wave signal ranging between +2 and -2 volts to transmit data. Transitions of the signal are measured, with the time interval

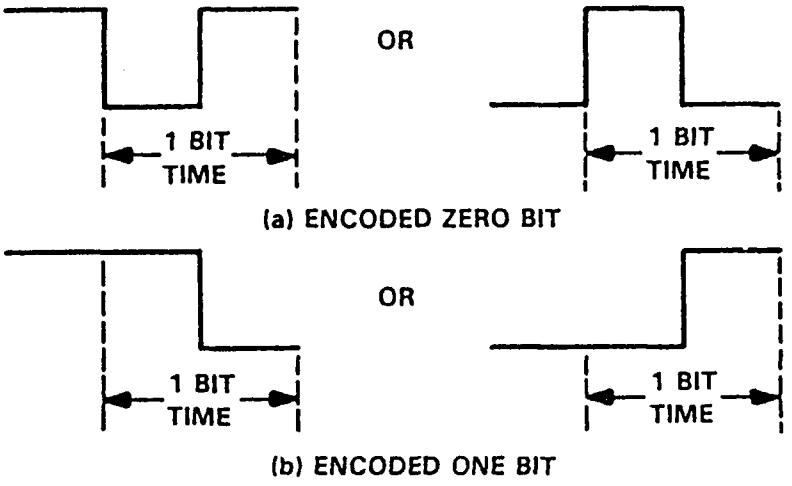


Figure 3-2. Differential Manchester Coding
[from Ref. 6: p. 3-6]

of the change between the 10% and 90% levels of the peak voltage being termed the rise or fall time. IEEE 802.5 specifies that these rise and fall times of the pulses must be less than 25 nsecs for a 4Mb/s data rate such as this system. [Ref. 3: p. 80]

This use of Differential Manchester coding required a system which would now support an 8 MBaud signal and meet the limits placed for rise and fall times. Examining the data sheets for the Hewlett-Packard components, it was found that the use of the HFBR-1412 transmitter in conjunction with the HFBR-2414 25 MHz receiver would support the requirements. These are low-cost optic components using industry-standard AT&T ST-series bayonet-style connectors for improved coupling efficiency [Ref. 12].

The HFBR-1412 transmitter consists of an 820 nm GaAlAs LED emitter and a double-lens optical system. The emitter is driven at low levels of current resulting in an efficient and reliable component. The transmitter is capable of supporting data rates of over 100 Mbaud and has a maximum rise/fall time of 6.5 nsec. These characteristics are easily within the specifications as outline by IEEE 802.5. [Ref. 5: pp. 8-43 - 8-44]

The HFBR-2414 receiver detects an optical signal and outputs an analog voltage. Its typical frequency response ranges from DC to 25 MHz and its analog output is easily converted to a digital signal with rates up to 35 MBaud. This is more than adequate to handle the 8 MBaud signal of the adapter. Rise and fall times for the output are a maximum of 19.5 nsec, within the range outlined by IEEE 802.5. Another Hewlett-Packard component, the HFBR-2412 receiver, is also available for use. It is a digital receiver capable of handling signal rates up to 5 MBaud. This is not enough to support the data signal; however, its high maximum output voltage (up to 18 volts) makes it ideal for transmission of the Phantom Voltage. [Ref. 5: pp. 8-47 - 8-49]

A final choice driven by signal rate and the rise/fall time limits was the selection of components for use in the link circuitry. The Elantec EL2020C 50 MHz current feedback amplifier was chosen due to its high speed and 25 nsec rise/fall time. In addition, it provided flexibility through

its high current output of up to 33 mA and its high voltage output of up to 18 volts. [Ref. 4: p. 1-65]

2. System Interface and Adapter Cable Characteristics

The IEEE Standard 802.5 specifications call for the use of a twisted wire pair adapter cable to attach the system to the ring. This cable connects from the computer directly to the wiring concentrator and actually forms two complete paths for the Phantom Drive diagnostics, a positive and a negative path. Any design modification must take into account that this dual-output, dual-input setup is standard in existing adapter cards and wiring concentrators.

The other primary concern of the system interface and adapter cable deals with the DC current generated by the Phantom Drive voltage. As stated previously, the Phantom Drive impresses a DC voltage onto the signal at the transmit ports. This voltage generates the drive current which closes the bypass relays inside the wiring concentrator, inserting the system into the ring. IEEE 802.5 limits the DC voltage to the range of 4.1 to 7.0 volts generating a current ranging from 0.65 to 2.0 mA [Ref. 3: p. 78]. With the TMS380 adapter card impressing a 5 volt Phantom voltage on the signal and with the wire fault load conditions discussed in the the previous chapter (see Figure 2-11), these limits lead to the choice of a 4.3 kΩ load as seen by the adapter card, generating approximately a 1 mA DC current.

B. DESIGN APPROACH

The fiber optic link design can be broken down into two sections, a link for the Phantom Drive and a link for signal transmission. A separate approach was taken for the Phantom Drive to allow for testing of the link to ensure the wiring concentrator bypass relays were being closed and were inserting the system into the ring.

1. Phantom Transmitter and Receiver

The first modification to the design was to build a link for the Phantom Drive from the computer to the wiring concentrator. The idea behind this approach was to detect when the Phantom voltage was being generated by the adapter and transmitting this information to the concentrator side of the link. At the concentrator, this signal would be received and converted to the necessary voltage to generate the DC current to operate the bypass relays. A schematic of the TMS38051/52 Ring Interface included as Figure 3-3 shows the Phantom Drive to be output from pins 19 and 18 (PHOUTA and PHOUTB) of the TMS38052 chip. The Phantom drive then passes through circuitry to smooth out the signal and is impressed on the data signal at ports T1 and T2 [Ref. 6: p. A-100]. Tests on the adapter card showed that a 5 volt DC signal was present for each line after the 50Ω resistors R14 and R15; so it was this point which was chosen as the test point for the presence of the Phantom voltage.

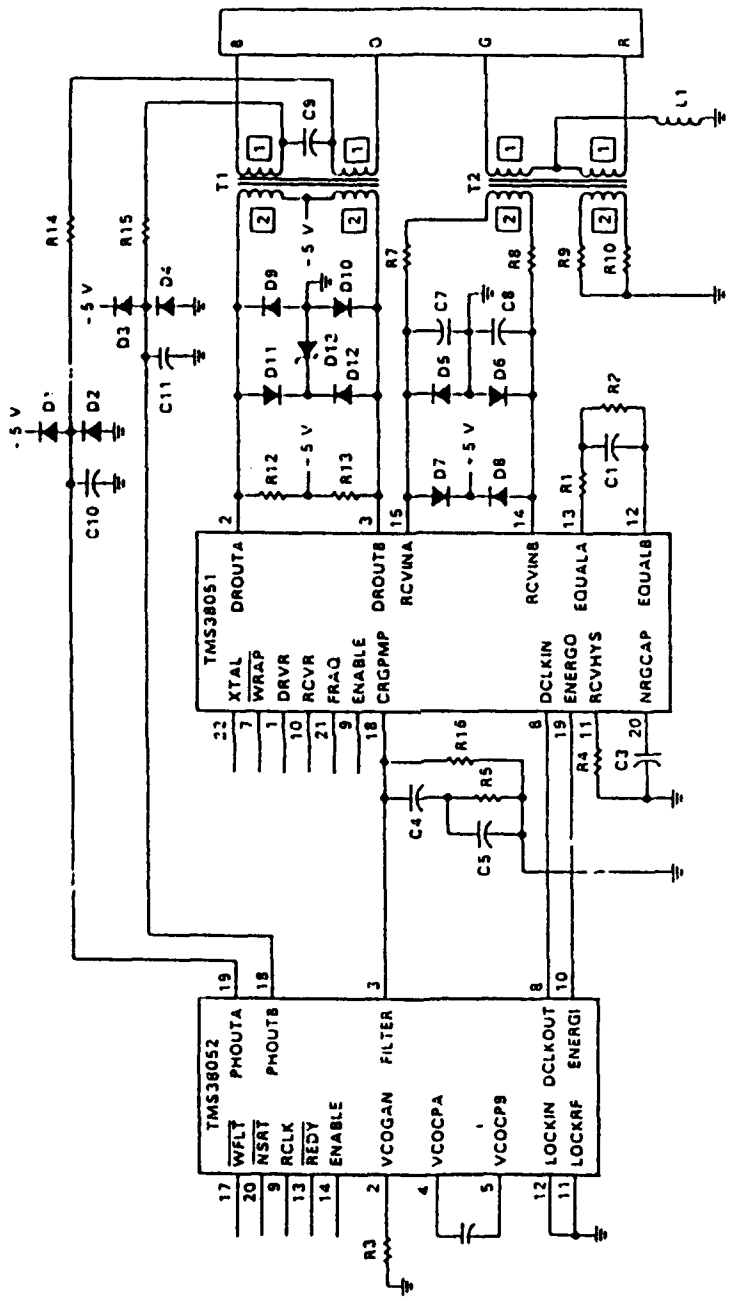


Figure 3-3. TMS38051/52 Ring Interface
[from Ref. 6: p. A-100]

Figure 3-4 shows the design for a transmitter to send a 5 volt signal. This circuit was originally connected after resistor R14 on the adapter card, as detecting the Phantom voltage on one line was enough to determine that the adapter card was attempting insertion. A unity-gain buffer was used to ensure no current was drawn from the card and prevent a wire fault condition. The actual fiber optic transmitter draws its current from a bipolar junction transistor in the active mode, as the single EL2020C amplifier was unable to provide enough current. Setting the value of resistor R3 to 62 Ω and realizing the typical forward voltage of the HFBR-1412 transmitter LED is 1.8 volts gave a forward current of 42 mA, adequate to allow the transmitter to begin functioning.

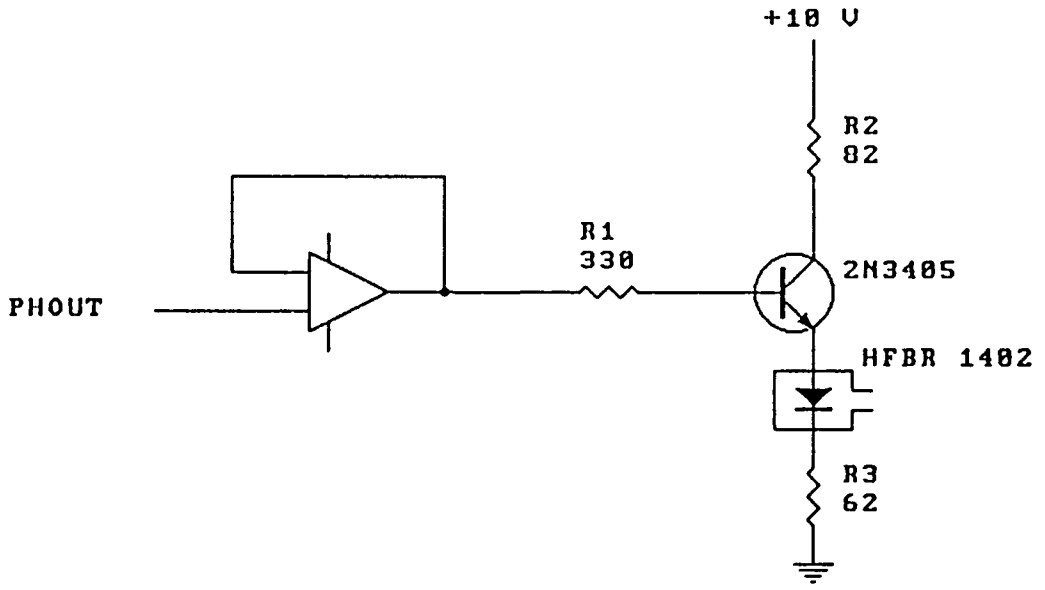


Figure 3-4. Phantom Drive Transmitter

Tests run with only the buffer attached to the adapter card found that the system would not boot properly. It was believed that this was due to some small current drain on the Phantom line which was sensed by the PHOUTA pin. To bypass this problem, an attempt was made to detect the Phantom Voltage at the transmit port. Figure 3-5 shows an additional circuit used to hook the Phantom transmitter directly into the transmit line by detecting the data signal with the impressed Phantom voltage, then smoothing the signal by passing it through an RC circuit and using a 5.1 volt zener diode.

After detecting the presence of the Phantom voltage and generating the optical signal, the signal passes through the fiber cable and is detected by the HFBR-2412 receiver. This is the optimal device to detect a DC signal, and, in this configuration, it outputs 5 volts DC when an optical signal

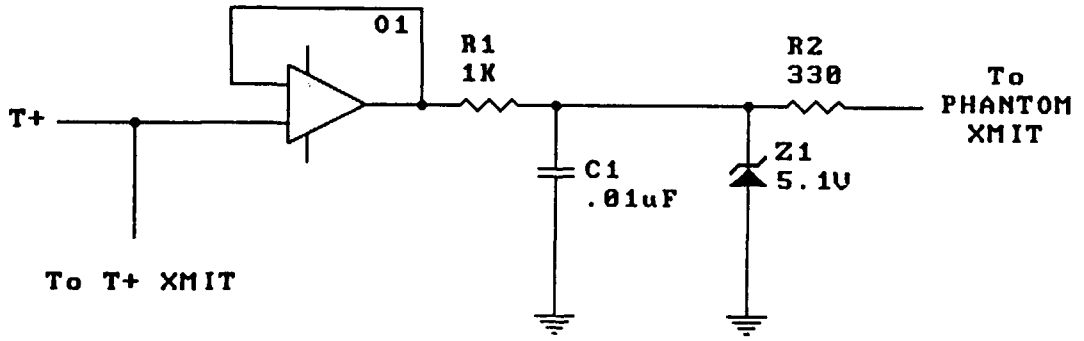


Figure 3-5. Phantom Drive Link Input

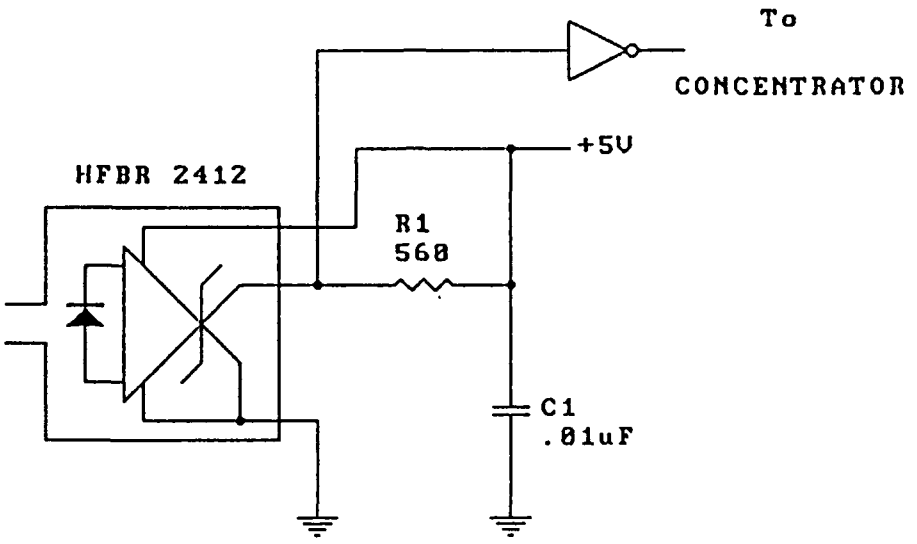


Figure 3-6. Phantom Drive Receiver

is detected and no output when no signal is present. The basic design for the receiver circuit, as shown in Figure 3-6, was provided by the Hewlett-Packard data sheets on the fiber optic components [Ref. 5: p. 8-41]. In this design the signal output pin of the transmitter is drawn to zero volts when an optic signal is detected and to the supply voltage of 5 volts when no signal is present. Adding the TTL inverter to the circuit allows for the proper output voltages, and, since a TTL inverter uses transistor output drive circuitry, it serves as a good current source from which the concentrator can draw.

Original plans called for a Phantom Drive fiber link to pass the required voltage from the computer to the concentrator, and a separate link to pass the voltage signal from the concentrator back to the computer. The signal returned from the concentrator was then to be used in a

comparator circuit with the original signal as a check for line continuity. Further study of the adapter diagnostics, however, showed the return link from the concentrator to the computer to be unnecessary, as any loss of the Phantom signal would open the bypass relays and cause a wire fault condition.

Tests run on this link showed that the optical link design functioned properly, with the HFBR-1412 transmitting an optical signal when a 5 volt test source was present. This optical signal was received by the HFBR-2412 and output by the receiver circuit as a 5 volt signal.

2. Data Transmitter

Moving to the data transmission line, the first step was to determine the signal which must be handled by any link circuitry. The signal voltage levels were determined using an oscilloscope, with the result seen in Figure 3-7. The initial boot process is broken into four periods:

(a) Adapter self-check with data signal centered around zero volts.

(b) Phase 0 Lobe Media check with Phantom voltage impressed on data signal to test entire link.

(c) Break between Phase 0 and Phase 1 with data signal centered around zero volts.

(d) Phase 1 Physical Insertion with Phantom voltage impressed on data signal.

From this study of the boot process, it was noted that the Phantom voltage is not always impressed on the data signal.

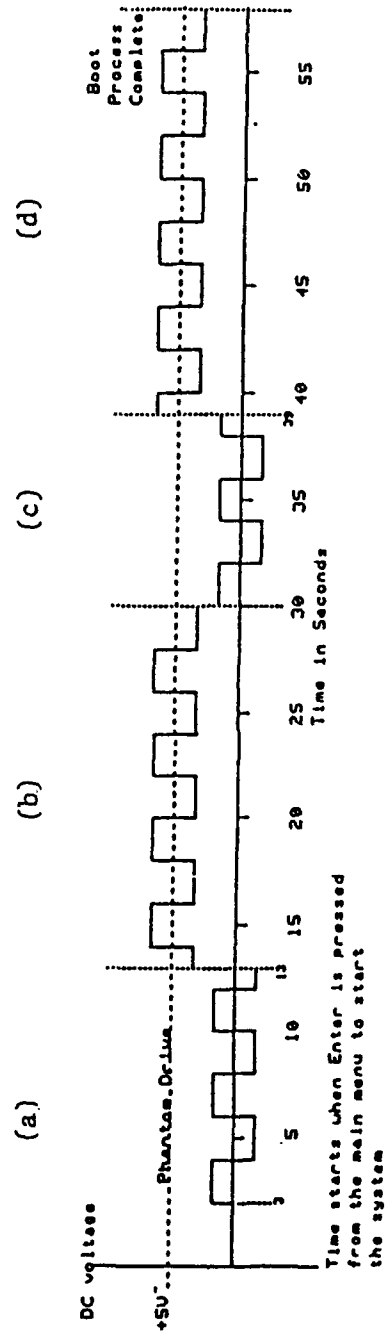


Figure 3-7. Network Boot Process
[from Ref. 11: p. 56]

This places a restriction on any link modification in that the link must be capable of handling the data signal when centered around zero volts, as well as around 5 volts. Since light is unipolar (only positive values), the entire data signal must be shifted so that no portion of the waveform is negative.

The original fiber link used a voltage divider at the transmitter input to compensate for the needed bias. This design, shown as Figure 3-8, shows an op-amp summer with the data signal from the adapter at one input and a voltage divider using a 3 volt zener diode as the second input. The use of resistor R1 with a value of 4.3 kΩ between the data signal input and the virtual-ground inverting input of the op-amp attempted to set the load condition within the limits discussed in Chapter II. The use of the voltage divider with a 3 volt zener diode placed a -3 volt bias on the data signal, which was then inverted by the op-amp summer to give the needed unipolar signal. [Ref. 11: pp. 45-47]

Analyzing this design highlighted some problems. First, the choice of resistors R3 and R4 did not provide the desired bias. These choices gave the voltage divider input leg a gain of 0.34, which caused the voltage signal to be biased negative at the input of the HFBR-1412 transmitter. The signal would then range from -1 to 3 volts without the Phantom voltage present and from -6 to -2 volts with the Phantom voltage present. After changing resistor values to allow for proper biasing, a second problem with the voltage

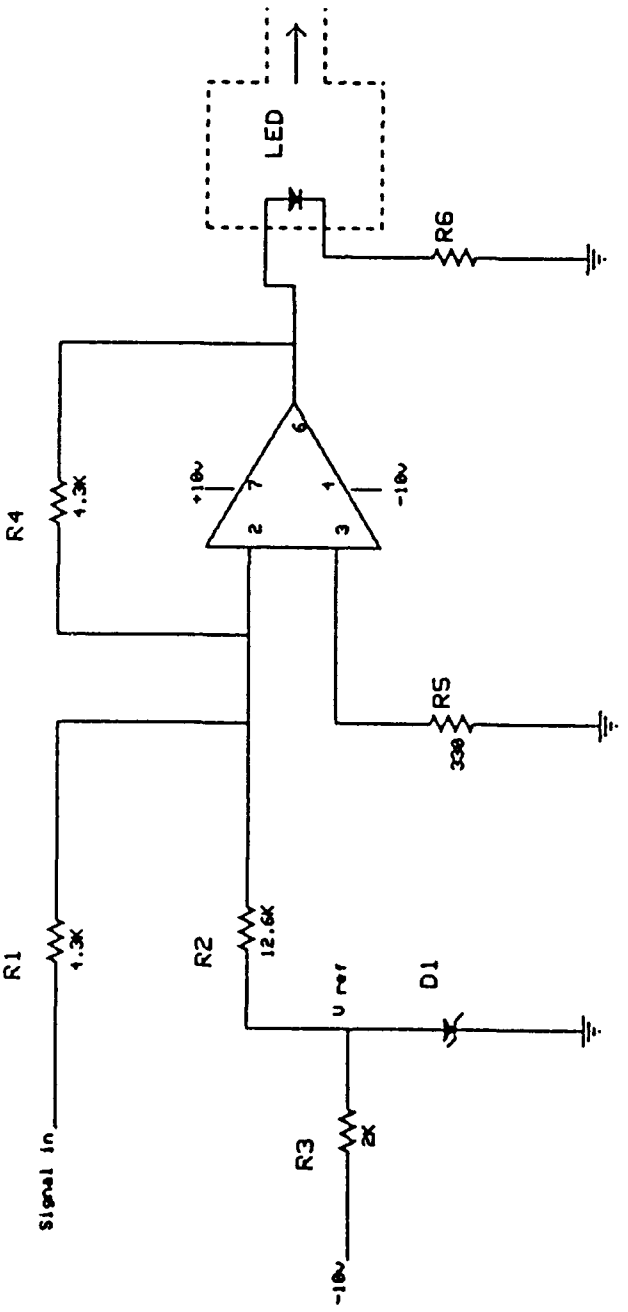


Figure 3-8. Existing Data Transmitter
[from Ref. 11: p. 46]

divider was discovered. The voltage divider acted as a current sink, drawing current away from the transmitter. This prevented the transmitter from functioning properly, allowing it to output only a weak signal which was susceptible to noise. In addition, it also negated the attempt at setting a 4.3 kΩ load condition. Using the principle of superposition, the total load resistance as seen by the adapter through the T+ port was over 8 kΩ, assuming negligible resistance within the LED. This places the load in the indeterminate range of the wire fault load conditions, outside the optimal range.

Figure 3-9 represents the new transmitter design, addressing each of the faults of the original transmitter. The inputs to the circuit from the positive and negative transmit ports of the adapter first pass through unity-gain buffers with the noninverting input pin of the op-amp tied to ground through a 4.3 kΩ resistor. This sets the load resistance as seen by the adapter within the limits stated in Chapter II. The output port of negative line buffer is then passed to ground through a 4.3 kΩ resistor. This allows for a system design based only on the use of a single transmit port, in this case the positive port.

The next stage of the circuit is an op-amp summer with the buffered transmit signals as one input and a +5 volt bias as the second input. This modification removed the problem of the current drain caused by the use of the voltage divider, but it placed the restriction that the output was now always

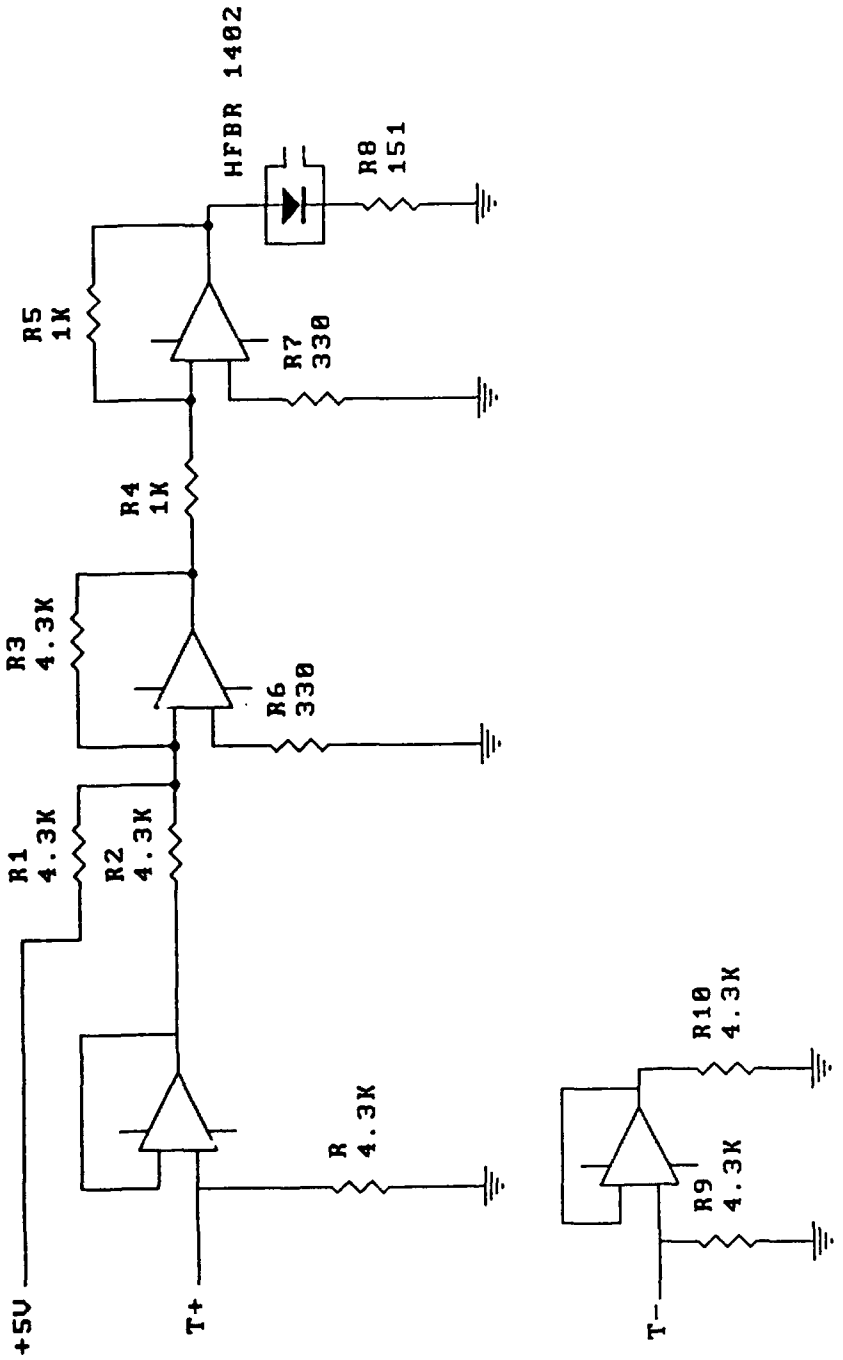


Figure 3-9. Data Transmitter

negative, ranging from -7 to -3 volts and -12 to -8 volts, depending on the presence of the Phantom voltage. To rectify this, an additional amplifier was added with a gain of -1 to invert the signal and to provide a second source of current for the transmitter.

Resistor R8 following the HFBR-1412 transmitter controls the current through the transmitter and can be adjusted to ensure proper operation. For this circuit design, a 151 Ω resistor was chosen to generate the current to produce the optical signal. This choice limited the amount of current available when the Phantom voltage was not present, but choosing a smaller resistor would cause too much current to be generated during the operation of the Phantom Drive. It was a necessary trade-off, but it allowed the system to meet the primary concern of data transmission around the ring.

3. Data Receiver

The data receiver of the existing design is included as Figure 3-10. Upon examination, it was discovered that the two capacitors and 750 Ω resistor at the output of the HFBR-2414 receiver interfered with the proper passing of the received signal. The levels of current being output by the receiver in response to the optical signal were small, and the loss of any amount of current through the resistor to ground had detrimental effects. The decision was made to forego removing the DC voltage levels from the received signal until

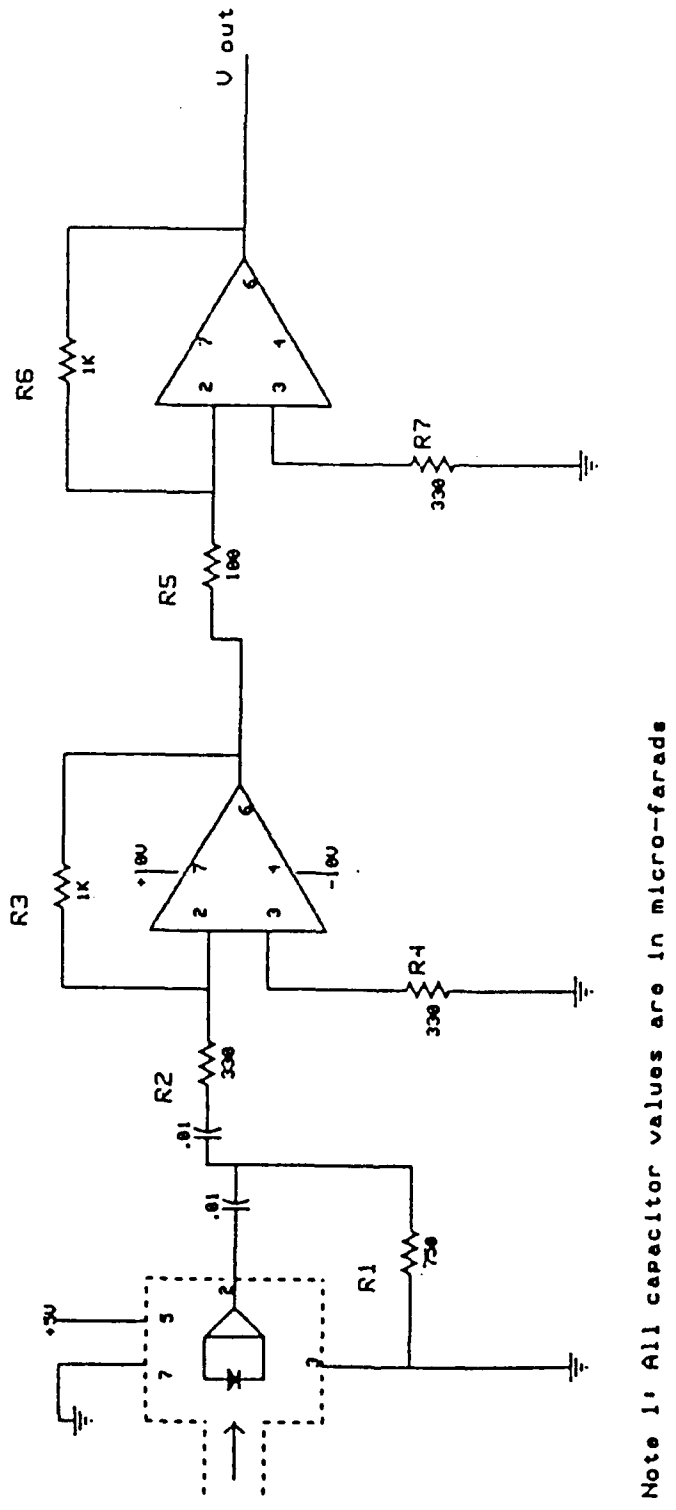


Figure 3-10. Existing Data Receiver
[from Ref. 11: p. 50]

after the signal had been amplified. These changes are seen in Figure 3-11. [Ref. 11: p. 48]

All current generated by the received optical signal passes through the two-stage amplifier to reproduce a waveform of the proper amplitude and period. After amplification, the waveform is stripped of any DC bias passed through the fiber link by the blocking capacitor.

No additional circuitry is necessary for the data link to test for ring continuity. A break in the fiber cable or a failure in the link circuitry will result in loss of the data signal which will be discovered during the Ring Polling phase of the insertion process as discussed in Chapter II.

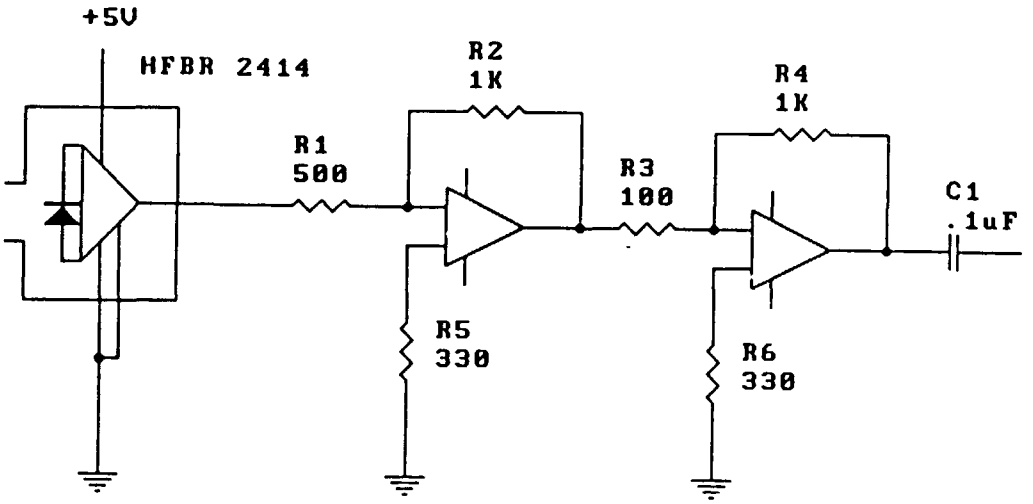


Figure 3-11. Data Receiver

4. Wiring Concentrator Input and Output Circuits

With both the Data signal and the Phantom signal passed through the fiber cables and the respective receiver circuitry, the next step was to convert the signals to the input signal levels of the wiring concentrator. Two voltage summers are used to add the Data signal and the Phantom signal, providing the concentrator with the required DC voltage to generate the proper level of current to close the bypass relays. Figure 3-12 shows an example of the voltage summer for each input. The positive and negative inputs are identical with the exception of an inverting op-amp being added to the Data signal of the positive line.

After passing through the concentrator, the two data signals are again prepared for transmission back to the computer through another fiber cable. The negative signal passes through an inverting amplifier in order to equalize any timing delay, and then the two signals are sent through a summing amplifier to form one waveform for transmission, as shown in Figure 3-13. The summing amplifier has a gain of 5.1 to compensate for loss in signal strength within the concentrator and input/output circuitry. Once amplified, the single waveform passes to a data transmitter, through a return fiber cable to an optical receiver where it is passed to the receive ports of the computer system.

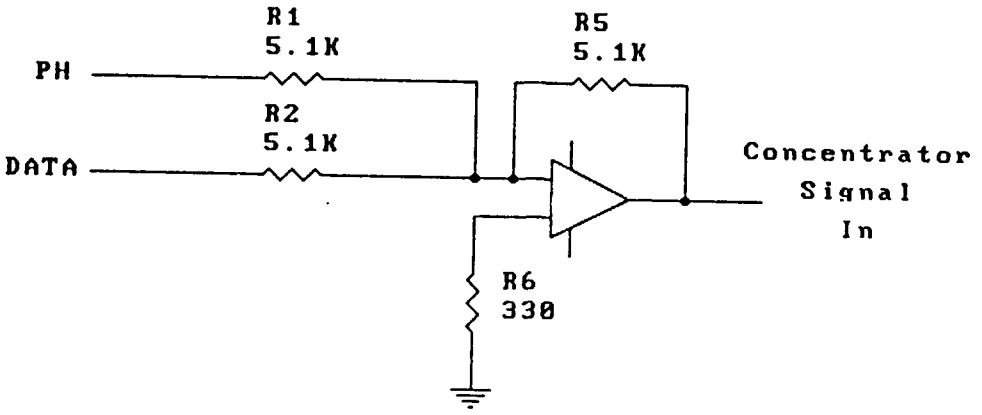


Figure 3-12. Concentrator Input Circuit

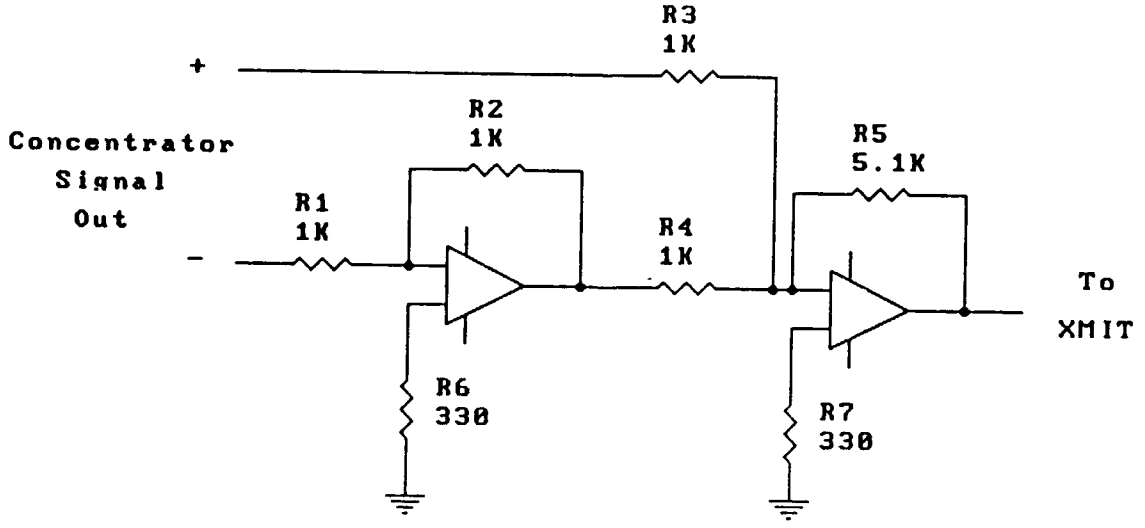


Figure 3-13. Concentrator Output Circuit

C. COMPLETE FIBER LINK EVALUATION

With each component of fiber designed, the next step was to complete the construction of the entire fiber link from computer to concentrator. A block diagram of the link design, shown in Figure 3-14, shows how each of the separate components are used in the link construction.

Having addressed the load condition and ring configuration problems found in previous research, work continued by testing the complete system. As stated before, tests run on the Phantom link showed that a 5 volt signal detected at the link input would be transmitted through to the concentrator side and recovered as 5 volts. Further tests run included summing a model square wave signal with the Phantom link signal via the concentrator input circuitry to test for proper functioning of the concentrator. Sample signals may be seen in Figure 3-15. From the results of seeing the signal at the output of the concentrator, it was determined that the Phantom link would support the system by inserting the station into the ring through the concentrator relay.

Tests were also conducted on the data transmission link beginning with transmitter circuit. Again modeling the data signal with a square-wave signal, the transmitter circuitry was examined to determine the input to the LED.

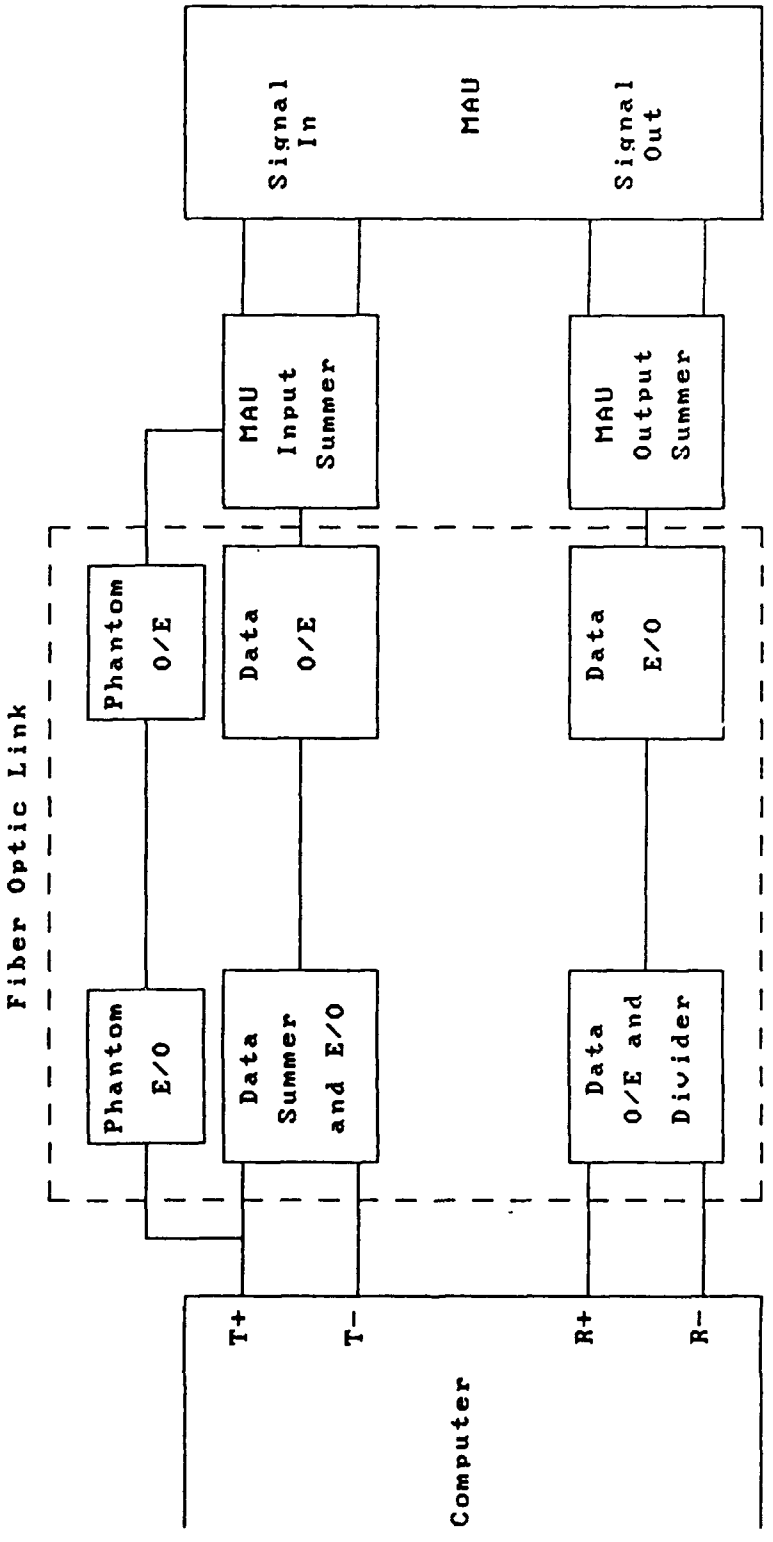
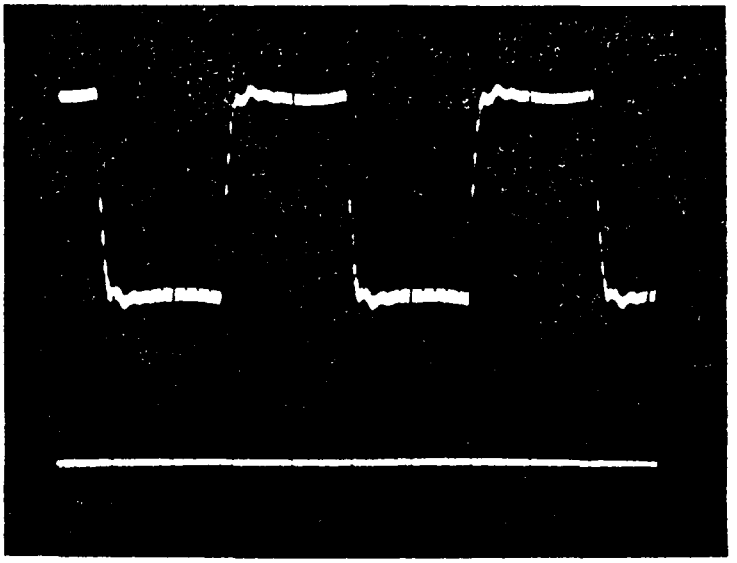
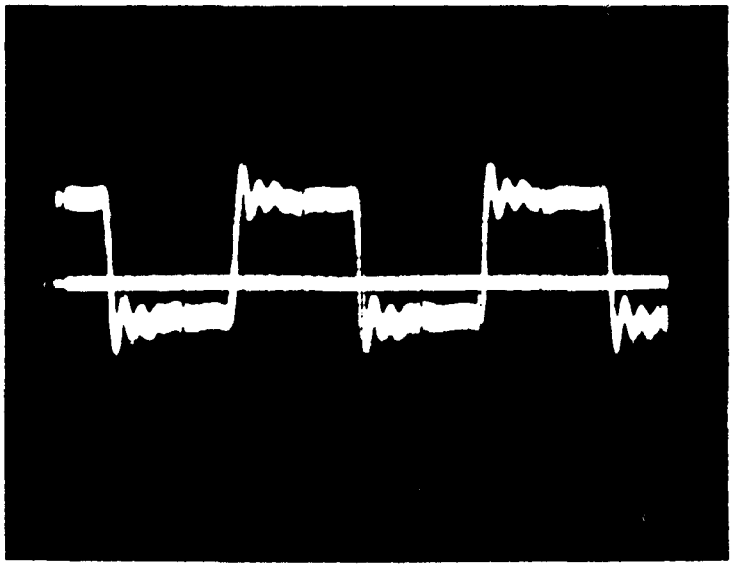


Figure 3-14. System Block Diagram



(a) Concentrator Input
(Waveform is 4 volts peak-to-peak)



(b) Concentrator Output
(Waveform is 2 volts peak-to-peak)

Figure 3-15. Concentrator Waveforms
Using Modeled Signals
(Ground reference shown as line)

Figure 3-16 shows that the data signal with correct bias was sent to the LED for transmission into the cable.

Figure 3-17a gives a view of the waveform as received by the HFBR-2414. Once output by the photodiode receiver, the amplification of the signal occurs as shown in Figure 3-17b. Some distortion of the signal may be seen as peak voltages drop off, but, since Differential Manchester coding only detects transitions from one voltage polarity to the other, it was assumed that this would not affect system performance.

With each of the links tested using modeled signals, the next test was to hook the entire link to the computer and

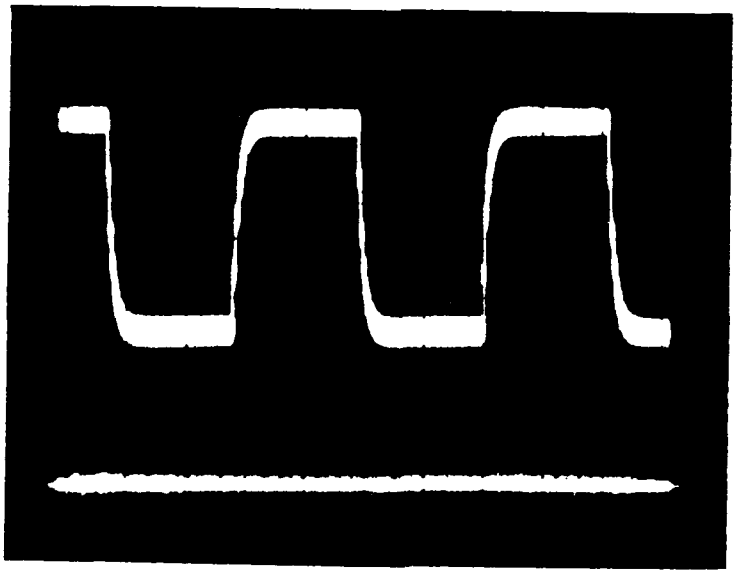
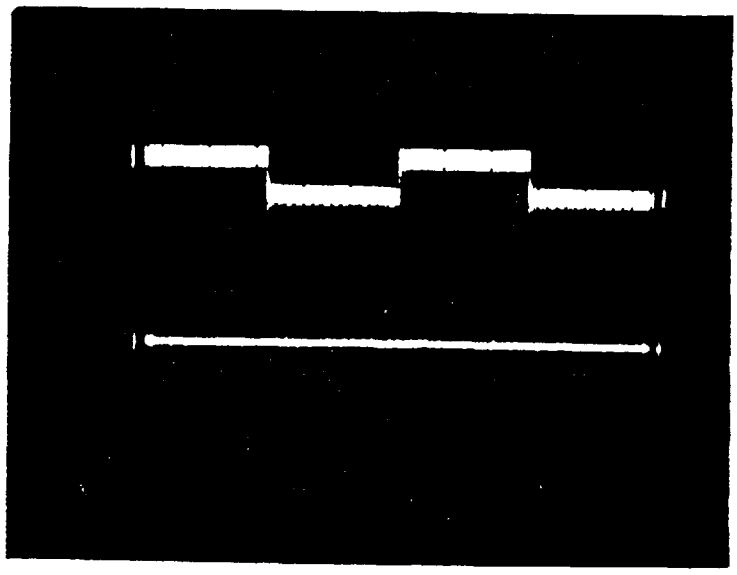
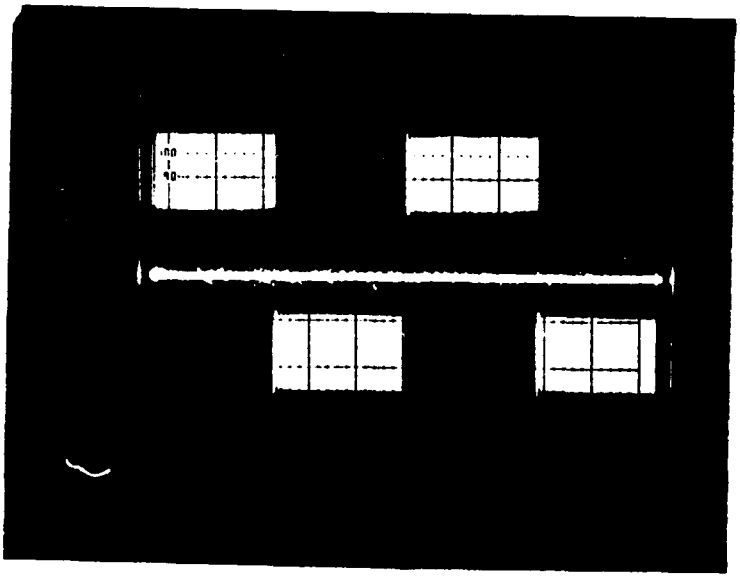


Figure 3-16. Transmitter LED
Input Waveform
(Waveform is 4 volts peak-to-peak,
with ground reference shown as line)



(a) Data Receiver Output
(Waveform is 0.1 volts peak-to-peak
with 0.4 volts DC offset)



(b) Amplified Receiver Output
(Waveform is 2 volts peak-to-peak)

Figure 3-17. Receiver Outputs
(Ground reference shown as line)

attempt the network boot process. Repeated attempts to run the network software, however, resulted in hardware error messages. Examining the signal waveforms at various positions including the immediate inputs to the link showed that the transmtter was somehow loading the system down and not allowing the system to transmit a proper data signal. Previous research had determined a way around the wire fault condition limits placed on the link by placing 4.3 kΩ resistors directly from the T+ and T- ports to the R+ and R- ports. This allowed all of the system checks to be performed, set the load condition within the acceptable limits, and allowed the system to boot properly. Another attempt with these resistors in place did allow the system to boot properly. Further tests with messages sent from the control station through the ring were not received, and, when the resistors were removed, the system again failed due to hardware error.

One final test was run with the Phantom Drive link disconnected from the system and instead modeled with a 5 volt signal at the link input. The system still was not able to transmit a proper data signal or boot properly, but the signal it did produce was transmitted throughout the entire link. This showed that the design of the link was generally sound, but some problem existed at the interface between the adapter and the link. Time constraints prevented any further study of this problem and it remains unresolved at present.

IV. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

This thesis had the objective of designing and building a functional star-wired token ring local area network. These efforts were only partially successful. A fiber link with the purpose of allowing the system to be inserted into the ring through a wiring concentrator was constructed and shown to function properly using modeled Data and Phantom Drive signals. Problems developed when the link was attached to the computer system. Tests showed that the network boot process was not successfully completed, due to problems at the adapter-link interface. These problems could be traced to the TMS380 token ring adapter diagnostics. The diagnostic tests performed by the adapter were designed for use with a wire link, and, as such, were not able to be overcome during this study.

B. RECOMMENDATIONS

Future research in the area of fiber optic local area networks should focus on the diagnostic tests and their effects on the system-to-link interface. Modifications in the design of the transmitter circuitry should be developed to allow proper functioning of the network boot process. In

addition, software changes could be made to allow the adapter card to accept the impedances and currents of the fiber link.

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