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FINAL REPORT

STRUCTURE-BASED DESIGN AND ANALYSIS FOR CONCURRENT ERROR DETECTION AND RECOVERY IN RELIABLE ELECTRONIC SYSTEMS

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W. Kent Fuchs
Center for Reliable and High-Performance Computing
Coordinated Science Laboratory
University of Illinois
1101 W. Springfield Ave.
Urbana, IL 61801
(217) 333-9731
FAX: (217) 244-5686
fuchs@crhc.uiuc.edu

Scientific Officer:
Dr. Clifford Lau
Department of the Navy
Office of Naval Research (Code 1114SE)
800 N. Quincy Street
Arlington, VA 22217-5000

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A. Description of the Scientific Research Goals

The complex digital electronic systems necessary for successfully attaining the SDIO mission will be composed of extremely large numbers of fine geometry active devices densely integrated with potentially submicron interconnect. A major problem with the integration of these complex microelectronic circuits on VLSI chips and wafer-scale integration is that they become highly susceptible to physical failures and environmental disturbances, especially intermittent and transient failures. This problem is aggravated when these electronic systems are deployed in harsh environments potentially resulting in erroneous computation due to transient failures as projected in the SDIO mission. Failures can result in disastrous incorrect computational results or complete system shutdown. The purpose of this research has been to develop techniques for the design of highly reliable electronic digital systems based on the *concurrent detection* of errors and *rapid recovery* from failures and environmentally induced upsets. Concurrent error detection consistently monitors the correctness of computational results and therefore allows for the detection of errors due to transient environmental upsets as well as permanent failures. Basic scientific results were obtained in this research concerning the derivation of design and analysis principles for concurrent error detection and recovery in electronic systems.

B. Summary of Significant Results

1) Periodic Application of Concurrent Error Detection

A new approach to concurrent error detection was developed called periodic application of concurrent error detection (PACED). The PACED approach utilizes periodic rather than constant application of checking to verify correct results. The approach is parameterized, allowing application to various computational arrays and algorithms, for varying degrees of error coverage. This research resulted in applications of the technique to signal processing algorithms and in detailed simulation and analysis of the error propagation effects with PACED.

2) High Harvest Loop-Based Reconfiguration

A new method of interconnecting good elements in a linear array so that the delay between processing and memory elements is constant was developed in this research. The reconfiguration provides the capability of interconnecting a surprisingly high percentage of the good elements.

3) Reconfigurable Pipelines and Defect-Tolerant Trees

Methods and algorithms for reconfiguring pipeline structures were developed. An accurate method of predicting the percentage of usable pipelines given the defect distribution was developed. A design for large area defect tolerant trees was also proposed. The design allows for defective interconnect and switches and guarantees that an arbitrarily high percentage of the good processing elements can be incorporated into the tree.

4) Simulation and Evaluation

A behavioral simulator was implemented for evaluating the fault coverage of test patterns for integrated circuits. The evaluation is based on the probability of failure derived from the behavioral simulator.

C. List of Publications/Reports/Presentations

1. Papers Published and Submitted to Refereed Journals

K. Kubiak, W. K. Fuchs, "Rapid Integrated Circuit Reliability Simulation with Applications to Testing," *IEEE Transactions on Reliability*, To appear: September 1992. **(ONR/SDI)**

W. Shi, M.-F. Chang, W. K. Fuchs, "Harvest Rate of Reconfigurable Pipelines," *IEEE Transactions on Computers*, Submitted. **(ONR/SDI)**

T. L. Wernimont, D. K. Hwang, W. K. Fuchs, "CSP-Based Object-Oriented Description and Simulation of a Reconfigurable Adaptive Beamforming Architecture Using the OODRA Workbench," *Journal of VLSI Signal Processing*, vol. 2, no. 3, Nov. 1990, pp. 159-172. **(ONR/SDI)**

M. F. Chang, W. K. Fuchs, "Loop-Based Design and Reconfiguration of Wafer Scale Linear Arrays with High Harvest Rates" *IEEE Journal of Solid-State Circuits*, vol. 26, no. 5, May 1991, pp. 717-726. **(ONR/SDI)**

2. Non-Refereed Publications and Published Technical Reports

none

3. Presentations

a. Invited

W. K. Fuchs, "Fault Tolerance in VLSI Architectures," General Motors Research, May 1989.

W. K. Fuchs, "Compiler-Assisted Recovery in Parallel Architectures," *Fault-Tolerant Computing Workshop*, AT&T, Naperville, IL, May 1989.

W. K. Fuchs, "Structure-Based Reliable Electronics," *SDIO/IST Workshop on Reliable Electronics*, Washington, DC, June 1989.

W. K. Fuchs, "Rapid Recovery in Parallel Architectures," *Workshop on Wafer Scale Integration and Reliable Electronics*, Stanford University, July 1990.

W. K. Fuchs, "Fault Diagnosis for Integrated Circuits," Delco Electronics, IN, Sept. 1990.

P. G. Ryan and W. K. Fuchs, "Partial Detectability Profiles," *SRC Techcon* San Jose, CA, Oct. 1990.

W. K. Fuchs, "Fault-Tolerant Computing in Parallel Architectures," *ACCA Computer Science Seminar Series* Argonne National Laboratory, Argonne, IL, Oct. 1990.

W. K. Fuchs, "Rapid Recovery in Parallel Architectures," *Workshop on Wafer Scale Integration and Reliable Electronics*, Washington, D.C., July 1991.

W. K. Fuchs and W.-M. Hwu, "Rapid Recovery in Multiprocessor Architectures," *Workshop on Fault-Tolerant Computing*, Washington, D.C., Nov. 1991.

W. K. Fuchs, "Checkpointing and Recovery in Multiprocessor Systems," *University of Iowa Faculty Seminar Series*, Iowa City, Iowa, March 1992.

W. K. Fuchs, "Checkpointing and Recovery in Multiprocessor Systems," *Texas A&M University*, College Station, Texas, April 1992.

b. Contributed (See list of refereed published conference papers below.)

4. Books (and book chapters)

none supported by SDI

5. Refereed Published Conference Papers (Supported by this Grant)

D. K. Hwang, T. L. Wernimont, W. K. Fuchs, "Use of the OODRA Workbench in Evaluating a Digital Beamforming Architecture," *Proceedings of the 26th IEEE/ACM Design Automation Conference*, June 1989, pp. 614-617. **(ONR/SDI)**

P. P. Chen, W. K. Fuchs, "Periodic Application of Concurrent Error Detection in Processor Arrays," *Proceedings of the Government Microcircuit Applications Conference*, Nov. 1989, pp. 451-454. (November) **(ONR/SDI)**

P. G. Ryan, D. Saab, W. K. Fuchs, "A Visually Oriented Architectural Fault Simulation Environment for WSI," *Proceedings of the IEEE International Conference on Wafer-Scale Integration*, Jan. 1990, pp. 167-173. (Jan 19990). **(ONR/SDI)**

P. Chen, W. K. Fuchs, "Confidence in Processor Array Outputs Under Periodic Application of Concurrent Error Detection," *Proceedings IEEE/IFIP International Workshop on Defect and Fault Tolerance in VLSI Systems*, Nov. 1990, pp. 299-305. **(ONR/SDI)**

M.-F. Chang, W. K. Fuchs, "Design and Parallel Testing of Wafer Scale Linear Arrays with High Harvest Rates," *Proceedings IEEE International Conference on Wafer Scale Integration*, Jan. 1991, pp. 285-291. **(ONR/SDI)**

W. Shi, M.-F. Chang, W. K. Fuchs, "Harvest Rate of Reconfigurable Pipelines," *Proceedings of the IEEE Workshop on Defect and Fault Tolerance in VLSI*, Nov. 1991, pp. 93-102. **(ONR/SDI)**

W. Shi, W. K. Fuchs, "Large Area Defect-Tolerant Tree Architectures," *Proceedings IEEE International Conference on Wafer Scale Integration*, Jan. 1991, pp. 127-133. **(ONR/SDI)**

W. Shi, W. K. Fuchs, "Optimal Spare Assignment for Defect-Tolerant Systems," *Proceedings of the IEEE International Conference on Wafer-Scale Integration*, Jan. 1992, pp. 193-199. **(ONR/SDI)**

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