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13. ABSTRACT *(Maximum 200 words)*

We summarize our fourth quarter and discuss fifth quarter plans for the development of an edge emitter based vacuum triode with performance goals of 10 μA/μm emission current density at less than 250V and which can be modulated at 1 GHz for 1 hour. Fabrication of two more process runs of field emitter diodes were completed. Current densitites of up to 10 μA/μm have now been measured on diode edge emitters. Total current emission of 380 μA was measured for a thin film edge emitter diode which is a factor of 25 greater than at the start of the program. Based on these results we have designed a diode array structure to achieve the 5 mA total current program requirements. The first fabrication run of this array is completed and now in test. The first fabrication run of the edge emitter vacuum triode was completed this quarter and is also in test. Equivalent circuit and FEM modeling of the vacuum edge emitter triode indicates that we should achieve 1 GHz modulation with gain with the present devices and that the device is mechanically stable.

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Quarterly Technical Report

RF Vacuum Microelectronics

7/01/92 - 9/30/92

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RF Vacuum Microelectronics
Quarterly Technical Report
7/01/92 - 9/30/92

I. Background

The objective of the RF Vacuum Microelectronics Program is to establish the technology base for the fabrication of practical, high performance gated vacuum emitters and to develop a new class of RF amplifiers based on these vacuum microelectronic emitters. Our technical approach is to utilize thin film technology and surface micromachining techniques to demonstrate an edge emitter based vacuum triode with emission current density of 10 μA/μm at less than 250V which can be modulated at 1 GHz continuously for 1 hour. Figure 1 shows a schematic cross section of our thin film edge emitter approach.

The edge emitter triode approach offers several potential advantages to achieving high frequency device operation (compared to cone emitters and wedge emitters):

- The fabrication process is a planar process, compatible with most silicon IC manufacturing.
- Thin film processes for the films used in the triode process are well controlled and reproducible. Control of film thicknesses to within 5% for the emitter film thickness is easily attainable resulting in a well-controlled edge emitter.
- Device capacitance for the edge emitter is less than that achievable for cones or wedges resulting in higher frequency operation.

Based on our experience with fabricating and testing edge emitter devices, our efforts on this program will be focussed on developing a highly stable, uniform and reliable current emission from the edge. We intend to achieve these qualities by

- use of thin film (200Å) edge emitters with small uniform radius of curvature
- use of refractory metal emitter structure to prevent electromigration and burnout
- use of comb emitter structures to prevent premature emitter burnout during edge formation
- use of current equalization series elements to set bias currents.

This program to develop an edge emitter triode started on October 1, 1991. The baseline portion of the program is for 18 months with the above mentioned objectives as goals. Upon successful completion of this phase, an option phase for 12 months can be implemented by DARPA with the objective to achieve 10 GHz modulation with the edge emitter device.

II. Technical Progress During Quarter

Key Achievements (7-01-92 to 9-30-92)

- Demonstrated current densities of up to 10 μA/μm (at ~120 V anode voltage) for a diode field emitter.
- Achieved maximum current emission of 380 μA for a single diode edge emitter.
- Designed a diode array device to demonstrate total device emission current of 5 mA and 5A cm^{-2}.
- Completed first fabrication run of diode arrays.
- Completed first fabrication run of edge emitter triodes.

- Continued equivalent circuit analysis of field emitter triode showing that present triode design will achieve >1 GHz modulation with gain. Also carried out finite-element modeling (FEM) electrostatic analysis of triode for mechanical stability under high fields.
- Presented paper on edge emitter diode/triode technology at International Vacuum Microelectronics meeting in Vienna.

III. Technical Progress

Task 1.0 Field Emitter Development

The objective of this task is to develop an an edge emitter structure with high emission current and high reliability. The goal is to achieve a current density of 5A cm^{-2} operating continuously for one hour at a gate voltage less than 250 Volts.

The technical approach is to fabricate field emitter diodes using the comb edge emitter structure shown in Figure 1-2. Each comb element has a series resistor for bias stabilization. Several emitter materials and configurations will be used to determine the structure to be used in the vacuum transistor.

During this quarter we demonstrated field emission from continuous and comb edge emitters. The highest current demonstrated is 380 μA from a continuous edge emitter. We have also demonstrated emission current density of 10 μA / μm of edge width. The devices also operated for longer period of time (≈ 70 hours) without burn out than previously reported. We have completed six fabrication runs.

There are three sub-tasks - test structure design, Emitter Fabrication and Emission Testing. We have completed the test structure design sub-task and 75 % of the emitter fabrication and emission testing sub-tasks. Below is a discussion of the accomplishments under these sub-tasks.

Sub-Task 1.1 Test Structure Design

We made design changes to the diode mask set to make arrays of edges that will meet the 5 A cm^{-2} and 5 mA total current program objective. The new mask set consists of five layers. A discussion of the design of this diode array is presented in Technical Progress, Task 3.

Sub-Task 1.2 Emitter Fabrication

We have completed the fabrication of two more runs of edge emitter diodes and two runs of diode arrays. A description of the runs and the device or material properties the devices are intended to study is given below.

Run 5316 Q5 - Fifth Diode Run
The primary objective of the run is to study the influence of emitter material on the performance of the devices. The run compares three refractory metals which have work functions of about 4.5 eV. - TiW, WNx, WSix. The secondary objective of the run is to compare TaN and sputtered boron doped polysilicon resistors. The run consists of 12 wafers - 9 quartz substrates and 3 silicon substrates with 1.4 μm of thermally grown oxide. The emitters of the devices are split into three groups (i) 250 Å TiW, (ii) 250 Å WNx and (iii) 250 Å WSix, each consisting of three quartz wafers and one silicon wafer. Each group of wafers are further split into two sub-groups. The first sub-group has 2500 Å of TaN resistors and consists of two quartz wafers and one silicon wafer. The second sub-group

consisting of one quartz wafer has 2500 Å of sputtered boron doped poly silicon. The devices are in testing now.

Run 5316 - Q6 - Sixth Diode Run

The objective of the run is study the effects of different materials on the emission current. The materials are TaN and (Si,Ta)Nx cermet. The run also had TiW/WSix/TiW layered emitters. This run is completed and is in testing.

Run 5331 - 01 - First Diode Array Run

The primary objective of the run is to fabricate an array of diodes that have comb emitters with and without series resistors. There are several emitter splits. (a) 300 Å TiW, (b) 300 Å WSix, (c) Al/TiW/Al, (d) Al/WSix/Al. Fabrication of the wafers will be completed in early October.

Run 5331 -02 - Second Diode Array Run

The objective of the run is to study the effect of Cs implants on the emission characteristics of TiW and WSix emitters. We expect that Cs will lower the work function and lead to increased emission currents at low voltages. Fabrication of this diode array run should be completed by mid-to-late October.

Sub-Task 1.3 Emission Testing

We continued testing, evaluation and analysis of the edge emitter diodes. With the field emitter diode structure we have demonstrated record performances from our edge emitters which include

- Highest current ever reported for a single edge (≈380 μA)
- Highest current densities ever reported for edge emitters (≈9.6 μA / μm)
- Long term current emission (50 μA emission from a single edge for greater than 70 hours)
- Current areal densities that have similar performance to field emitter arrays based on Mo cones.
- Comb structure emitters with and without current equalization series resistors

Below is a summary of the best results to date obtained from diodes of different device sizes and different emitter and resistor materials.

Summary of Best Data to Date

300 Å TiW Emitters

Device Width	Resistor	Max Current	Current Density
5 μm	No Resistor	48 μA	9.6 μA / μm
10 μm	No Resistor	59 μA	5.9 μA / μm
20 μm	No Resistor	165 μA	8.25 μA / μm
50 μm	No Resistor	288 μA	5.75 μA / μm
100 μm	No Resistor	383 μA	3.8 μA / μm

Summary of Results of Different Emitter Materials

Emitter Material	Max Current	Max Current Density
TiW	380 μA	9.6 μA/μm
Pt	6 μA	0.6 μA/μm
Mo	10 μA	1 μA/μm
WSix	250 μA	7.8 μA/μm
WNx	118 μA	9.1 μA/μm

As indicated by the dependence of burn-out current on edge width, we can conclude that the emission current is not coming from the two corners of the edge, but rather the emission current is coming from the length of the edge though it does not scale linearly. We see a decrease in emission current density at burn-out as the edge width decreases. We will investigate this further during the next quarter.

We also demonstrated repeatable diode-like IV characteristics. The device is a two terminal device (vacuum diode) with the anode / emitter separation determined by a PECVD silicon dioxide sacrificial layer. The gap is about 4000 Å. The device has eight fingers. Each finger is 5 μm wide and it is separated from the next finger by 5 μm space. Each finger has a 10 square resistor in series and the sheet resistance of the resistors is ≈1 MΩ/square.

The device was first tested in the forward direction by sourcing current and measuring the voltage necessary to maintain the emission. The current was increased in steps of 1 μA from 0 to 100 μA. The device was then reversed biased and tested sourcing voltage and measuring current. In the reverse direction voltage was increased in steps of 10 V from 0 to 300 V. The forward bias characteristics was then repeated by sourcing current and measuring voltage. Current was increased in steps of 1 μA from 0 till the device burnt out.

Figure 1.3 is a plot of the device characteristics. We observe from the plot that we do indeed have diode like IV characteristics that are repeatable. The gradual bend in the final forward bias IV may indicate that the resistance of the resistor was changing because of the current flowing leading to burn-out of either the resistor or the emitter. This is speculative at present and needs to be investigated further.

Task 2.0 Process Development

The focus of this task is to conduct a careful study of materials and processes used to fabricate vacuum microelectronic devices and investigate the best combination of approaches to obtain the desired device characteristics including high transconductance, low capacitance, low leakage currents and high reliability.

Sub-Task 2.3 Triode Process Development

The post-processing parametric inspection and testing of the first vacuum transistor run indicated that there are several processing steps that affect the yield of the run. These are the definition of the comb emitters and resistors, the trade-off between the emitter layer thickness and radius of curvature, and the trade-off between the sacrificial layer removal rate and the etch rate of the nitride support layer for the emitter. Experiments were conducted to solve the issues and below is a summary of these experiments.

Comb Definition Experiment

A critical step in the process is the definition of the comb emitter. At this point, we are etching both the emitter and the resistor. Since there is an overlap between the emitter and the resistor it implies that there will be some region of the underlying nitride layer that will be exposed for longer times than others. We developed processes to have an etch stop such as ZrO_2 and Al_2O_3 as etch stops. Both materials were characterized in regular laboratory chemicals and etching processes. We are also examining the possibility of using AlN.

Layered Emitter Structures

There is a trade-off between the emitter thickness and emitter radius of curvature. For the maximum emission current possible, the radius of curvature must be minimized. A distinct advantage of the thin-film-edge emitter approach is that the maximum radius of curvature is about half the thickness of the deposited thin-film-edge. Thus, for maximum emission current, the emitter should be as thin as possible. This, however, implies that current density in the emitter film will be high and the film will be susceptible to electromigration. An approach to fabricate a thin-film-edge with small radius of curvature that is not susceptible to electromigration is to deposit Al/TiW/Al layered emitter structrure. We developed a process for depositing a Al/TiW/Al layered emiter structure. The Al is etched by a wet chemical process after the definition of the edge by ion mill.

PECVD Oxide Sacrificial Layer

We are making a change in future runs from using BSQ as the sacrificial layer to PECVD oxide because of the faster etch rate of PECVD Oxide (4,000 Å/min for PECVD Oxide vs 500 Å/min for BSQ). The slower etch rate means that the nitride support layers of the emitter and the control electrodes are exposed to BOE for longer etch. We discovered in the first vacuum transistor run that the nitride support layers were completely etched because of the long etch times of the sacrificial layers. We have also developed another approach for obtaining low stress while maintaining etch resistance to BOE. We are using layered nitride structures consisting of two outer layers of etch resistant nitrides and an inner layer of low stress nitride.

TASK 3.0 Triode Development

The objective of this task is to develop a vacuum transistor with an edge emitter structure with high emission current and high reliability. The goal is to achieve a current density of 5A cm^{-2} operating at a gate voltage less than 250 Volts operating for one hour.

Our technical approach is to fabricate vacuum transistors using the comb edge emitter structure shown in Figure 3.0. Each comb element has a series resistor for bias stabilization. Several emitter materials and configurations will be used to determine the structure to be used in the vacuum transistor.

We completed the design of the vacuum transistor and the first fabrication run during this reporting period. Devices from this run are presently in test. A second triode fabrication run has been initiated. Also, device modeling of the thin film edge emitter vacuum transistor (triode) continued.

Task 3.1.1 Triode Design Considerations

Device Theory

The ratio of transconductance g_m to parasitic input capacitance C_{in} is the most important factor in microwave device gain at high frequencies. This is generally expressed as the current gain cutoff frequency f above which the magnitude of the power gain is reduced. At this point the current gain falls to unity. This parameter is approximately defined by

$$f_\tau = g_m/(2\pi C_{in})$$

However, power gain is still available up to f_{max} where the power gain also falls to unity. This is

$$f_{max} = f_\tau /(2\sqrt{(r_1 + f_\tau \tau_3)})$$

where r_1, the input-to-output resistance ratio, is

$$r_1 = (R_g+R_i+R_e)/R_{ae}$$

and the time constant τ_3 is

$$\tau_3 = 2\pi R_g C_{ag}$$

The edge emitter has the advantage that its parasitic capacitances can be reduced to very low levels by decreasing control electrode lengths and increasing the separation between the the control grid and anode. The first can be carried out by employing somewhat more complex lithography and etching procedures while the latter is just a matter of device design. However, at the present time the higher priority and more difficult issue of enhancing the device transconductance through raising the emitter current density while decreasing the bias voltages is being addressed. The expected performance characteristics based on recent results are discussed in the following pages.

If the transconductance is known, a precise calculation of the performance to be expected from a field emission triode design is straightforward since parasitic capacitances are readily determined using finite element techniques and similar modeling tools to solve Laplace's equation. On the other hand, simple approximations can also be employed to determine these parasitics which will give us an almost equally accurate estimate of device performance with the uncertainty in transconductance characteristics. This also has the advantage that the results can easily be verified by anyone using readily available software. Such an approach will be used here to generate an equivalent circuits for some field emission triode designs. The equivalent circuit will then be used to investigate device characteristics.

Figure 3-1 describes the cross section of a single cell of an edge emitter triode. Assuming that the capacitance between one of the control electrodes and the emitter is similar to that between a microstrip with similar geometry and ground--if anything it is higher--the impedance of the microstrip line is $Z_0 = 84$ ohms and its relative effective dielectric constant $_{eff} = 2.69$. This implies that the capacitance between the one control electrode and the emitter is

$$C_{ge}/2 = 1/(vZ_0) = {}_{eff}/(c_0Z_0) = 2.69/(30 \times 10^9 \times 84) = 0.65 \text{ pF/cm}$$

Assuming an equal amount of capacitance for both control electrodes gives a total capacitance to the emitter of 1.3 pF/cm. The capacitance between the control electrodes and the anode can be estimated using software which calculates the impedance between parallel strips. Using the geometries in Figure 3-1 and applying them to parallel strips we obtain $Z_0 = 141$ ohms and $_{eff} = 6.40$. This implies that the capacitance between the control electrode and the anode is quite high for a silicon substrate with coplanar electrodes

$$C_{ga} = {}_{eff}/(c_0Z_0) = 6.40/(30 \times 10^9 \times 141) = 0.6 \text{ pF/cm}$$

If the silicon has a 5 m thick layer of oxide on it the capacitance is significantly lower

$$C_{ga} = {}_{eff}/(c_0Z_0) = 2.23/(30 \times 10^9 \times 246) = 0.2 \text{ pF/cm}$$

and further reductions can be achieved by moving the anode to a separate substrate. The latter also has the advantage of improved heat sinking as well as better high frequency performance. The capacitance from the anode to the emitter can be calculated in a similar fashion. For edge emitters this capacitance is somewhat larger than for point emitters but it is not very significant in either case. Using the geometries in Figure 3-2 it is

$$C_{ea} = {}_{eff}/(c_0Z_0) = 6.40/(30 \times 10^9 \times 78.4) = 1.08 \text{ pF/cm}$$

on silicon and

$$C_{ea} = {}_{eff}/(c_0Z_0) = 1.85/(30 \times 10^9 \times 146) = 0.31 \text{ pF/cm}$$

on silicon dioxide.

Metallization resistance depends primarily on the geometry and secondarily on the frequency of operation. Since this resistance is not a dominant factor at the present time and the overall resistance can be reduced by geometry changes, frequency effects will be ignored. The resistances are then based on the geometries in Figure 3-2 with tungsten metallization.

Table 3-1 contains the calculated parameters for the equivalent circuit in Figure 3-3 for the structures listed in Table 3-2. All edge emitter parameters are based on unit cells that are 200 μm wide. The control electrode emitter resistance R_{ge} is derived from an assumed control electrode-emitter capacitive "Q" of 50 at 1 GHz. The anode-emitter resistance used is just a selected parameter which is large enough that it will have negligible effect on the maximum available gain. The transit time is an upper limit on this number which, in practice, has little effect. The other resistances are based on parameters for tungsten films similar to those presently used. The lowest transconductance listed is estimated to be equal to the conductance for diodes at currents of 10 A/m which is probably a lower limit since triodes will have smaller spacings between electrodes. Based on these parameters, the maximum available gain listed by the transconductances for the first three devices in Table 3-1 is plotted in Figure 3-4 for all frequencies where they are stable. At lower frequencies where this is not the case and the stability factor K is less than one, the maximum stable gain is plotted. The stability factor for the 144 μS transconductance device is also indicated in Figure 3-4. When it is equal to one there is a break in the corresponding (GM144US) maximum available gain curve. This power gain assumes that the input and output impedances of the device are matched at each frequency. Better performance is certainly achievable, but these numbers approximately correspond to the present state of the art. Figure 3-5 compares some of the same numbers with those for an aggressively designed 10 A/point array on 2.5 μm cell centers described in Figure 3-6. This spacing from the control electrode to the emitter contact is 1.0 micron in this point array for minimum capacitance with 0.4 μm point to control electrode spacing. From this comparison one might conclude that similar performance can be obtained from point or edge emitter devices. While this is true on paper, the dominant limitation is still the achievable average current density versus the input capacitance and edge emitters are believed to have greater potential for reproducible results.

The transconductance is closely related to the magnitude of the average current per unit area and operating voltage of the device. The capacitance between the anode and control electrodes has been ignored for edge emitters largely due to shielding effects of the emitter but it will slightly reduce the high frequency performance.

Table 3.1
Equivalent Circuit Parameters Used in Vacuum Microelectronic Simulations

Device	C_{ge} (pF)	C_{ae} (fF)	R_g (Ω)	R_e (Ω)	R_a (Ω)	R_{ge} (Ω)	R_{ae} (Ω)	g_{m0} (μS)	(pS)
GM18US	0.026	23	30	0.56	0.56	122	10,000	18	1
GM36US	0.026	23	30	0.56	0.56	122	10,000	36	1
GM72US	0.026	23	30	0.56	0.56	122	10,000	72	1
GM144US	0.026	23	30	0.56	0.56	122	10,000	144	1
GMPT40US	0.044	0.0	2	0.56	0.56	72	10,000	40	1

Table 3.2
Device Geometries Used to Calculate Equivalent Circuit Parameters

Device	Anode Length (μm)	Emitter Length (μm)	Gate Length (μm)	Anode Height (μm)	Substrate Material	Horizontal Gate-Anode Space (μm)
GM18US	20	20	0.25	0	Si	5
GM36US	20	20	0.25	0	Si	5
GM72US	20	20	0.25	0	Si	5
GM144US	20	20	0.25	0	Si	5

3.1.2 Diode Array Designs

Since the most important limitation on microwave field emitter triode performance which is not completely understood is the achievable transconductance or emitter current density, an array of high current diodes is probably one of the more effective tools for its development. These devices can be used to demonstrate high average and elevated total currents for improved emitter characteristics. A mask containing a number of diode arrays designed to deliver total currents per diode of greater than 5 mA and average current densities greater than 5 A/cm^2 is described in Figure 3-7 and Table 3-3. Figure 3-8 has an expanded view of the first die for greater clarity. The diode arrays contain multiple fingers approximately 200 microns long with varying numbers of emitters, with or without resistors connected in series with them. Interdigitated anode fingers in the same plane result in complete diodes without any external anode required. All of these devices employ tungsten metal for pads and with refractory metal emitters for high temperature and high current operation.

3.1.3 FEM Analysis of Triode Mechanical Stability

Objective:
The objective of this study is to determine the VME structure's mechanical response to both electrostatic and intrinsic stress loading. There are three main goals: an analysis of the deflections caused by electrostatic loading, an analysis of the deflections resulting from the residual stress of deposition found in the thin films (intrinsic stress), and an evaluation of the fault tolerance of these parameters to manufacturing variations in geometry and in film deposition stress.

Conclusion Summary:
The triode structure appears to be very robust in its construction. In all three study areas, the device remained little affected: electrostatic loading produced a nominal deflection of the upper control electrode of less than 10 Å, intrinsic stress caused a maximum deflection of only -84 Å, and process variations of significant proportions were able only to increase the maximum deflection to -141 Å.

Table 3-3
Summary Description of Individual Die

Die	Description	Purpose
1	5 μm finger and 5 μm space diodes with series resistors. A heated electrode diode and a self-aligned triode	Maximize total current and current density
2	5 μm finger and 10 μm space, 20 m finger and 5 m space diodes with series resistors. Dielectric test structures	As above
3	10 m finger and 5 m space diodes with series resistors and point emitter test arrays	As above with test structures for emission diagnostics
T1	Material measurement structures	Process characterization
7	Uniform edge diodes and level one serpentine	Comparison with previous designs and heating tests
T2	Alignment marks, leakage test patterns	Alignment for lithography, process monitoring
4	5 μm finger and 5 μm space diodes without series resistors and heated electrode diode	High total current and high cur-rent density
5	5 μm finger and 10 μm space, 20 m finger and 5 m space diodes without series resistors Etching test structures	High total current and high current density
6	10 μm finger and 5 μm space diodes without series resistors and point emitter test arrays	High total current and high current density

Model:
These results were achieved through finite element modeling of the structure in two dimensions using the Ansys FEM program from Swanson analysis systems. The structure is shown in figure 3.9. The electrostatic loading was calculated in the following way:

The force of attraction between two parallel capacitor plates is as follows:

$$F = \partial E/\partial x,\ E = {}^1/_2 C^* V^2,\ C = k' e_o A/d, \quad ==> F = {}^1/_2 k' e_o A V^2/d^2$$
$$\text{Pressure} = F/A, \quad ==> P = {}^1/_2 k' e_o V^2/d^2$$

k' is the effective dielectric constant. Since the gap between the emitter and control electrodes contains both vacuum ($e = e_o$) and nitride ($e = k_{ni} e_o$), the resulting dielectric constant is a combination of the two. Using the equations for two capacitors in series, the effective dielectric constant has been determined as follows (the vacuum gap is the same dimension as the oxide thickness):

$$k' = ((t_{ox}+t_{ni})*k_{ni})/(t_{ni}+t_{ox}*k_{ni}) =$$
$$= ((0.1\mu m + 0.4\mu m)*7.5)/(0.1\mu m + 0.4\mu m*7.5)$$
$$= 1.2097$$

Using the geometrical values from figure 1, the magnatude of the electrostatic "pressure" is:

$$P = 0.5*1.2097*(8.854e\text{-}12\ C^2N/m^2)*(100\ V)^2/(0.5\ \mu m)^2 = \underline{2.1421\ e\text{-}7\ N/\mu m^2}$$

Intrinsic stress effects have been included also. This is accomplished by adjusting each material's TCE such that over a given temperature rise the resulting stress is equal to input target values. The target values are intrinsic stress levels for a particular film as determined from sample measurement in the lab. This method has been verified by fixing the boundaries of all films, turning off the electrostatic loading, and running the solution; when this is done, each film has a resulting stress identically equal to the input value of intrinsic stress.

The following material properties were used:

Material	Modulus of Elasticity	Poisson's Ratio
SiO2 (sputtered):	13.3 Mpsi (92 GPa)	0.22
SiN (CVD):	21.5 Mpsi (148 GPa)	0.25
TiW (used properties of W):	59.3 Mpsi (409 GPa)	0.285

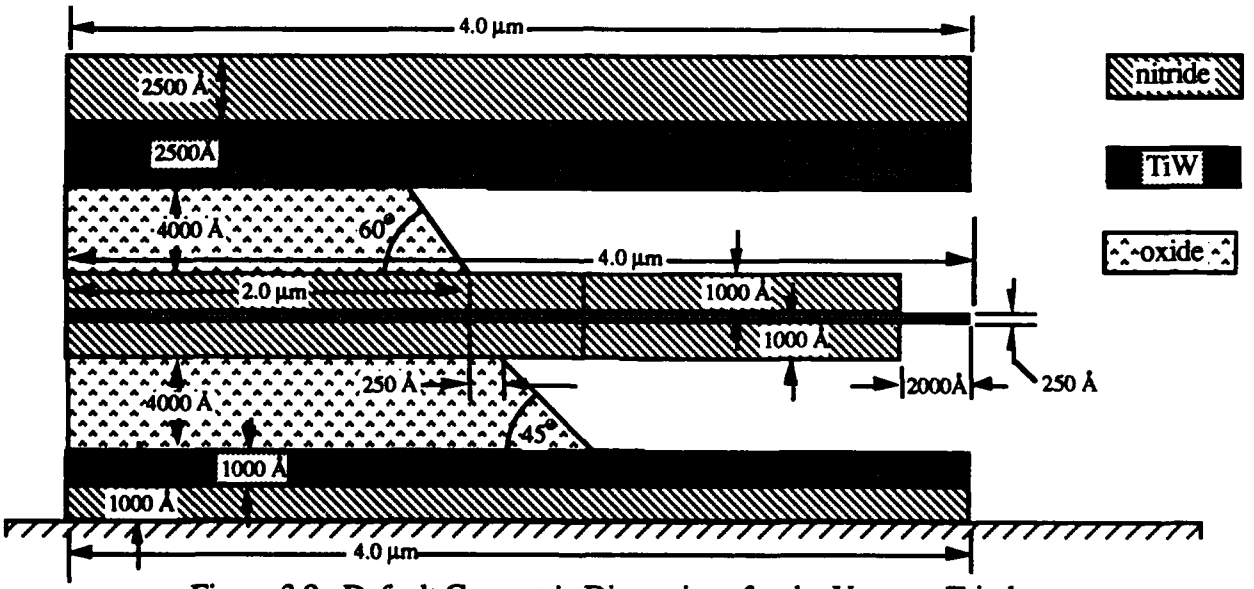


Figure 3.9: Default Geometric Dimensions for the Vacuum Triode

Results:

Model	Geometry/Loading Description	Emitter tip deflection (Å)	UCE tip deflection (Å)
Baseline models:			
1	I.S., but no electrostatic load; default geometry (except upper and lower oxides meet nitride emitter sheath at the same vertical position):	6.6 Å	-83.5 Å
2	I.S., but no electrostatic load; nitride sheath upper 800Å, lower 1000Å:	20.6 Å	-83.8 Å
UCE movement (vary the amount of UCE extension):			
3	I.S. and electrostatics; ΔUCE = 0 μm:	6.5	-89.0
4	I.S. and electrostatics; ΔUCE = -0.2 μm:	-3.4	-72.1
5	I.S. and electrostatics; ΔUCE = -0.4 μm:	-11.5	-56.7
6	I.S. and electrostatics; ΔUCE = -0.6 μm:	-18.0	-43.0
7	I.S. and electrostatics; ΔUCE = -0.8 μm:	-22.2	-30.8
8	I.S. and electrostatics; ΔUCE = -1.0 μm:	-26.3	-20.1
Increased Voltage (including I.S. and electrostatic loads):			
9	UCE and LCE = 200 Volts:	6.2	-105.8
10	UCE and LCE = 300 Volts:	1.2	-133.8
11	UCE/LCE = 200 V; UCE 0.2 μm shorter than LCE:	-33.2	-84.4
Modify Oxide Length (vary UCE, emitter, and LCE lengths):			
12	ΔOxide length = +0.500 μm:	7.3	-48.5
13	ΔOxide length = +0.333 μm:	7.1	-60.8
14	ΔOxide length = +0.167 μm:	6.8	-74.3
15	ΔOxide length = -0.167 μm:	6.3	-105.2
16	ΔOxide length = -0.333 μm:	6.1	-122.5
17	ΔOxide length = -0.500 μm:	5.9	-141.0
Modify Emitter Clamp Point (vary the difference between where the upper and lower oxides attach to the nitride emitter sheath):			
18	I.S. and Electrostatics, Δ clamp pt. = 0.025 Å:	6.4	-89.1
19	I.S. and Electrostatics, Δ clamp pt. = 0.050 Å:	6.4	-89.1
20	I.S. and Electrostatics, Δ clamp pt. = 0.100 Å:	6.4	-89.1
21	I.S. and Electrostatics, Δ clamp pt. = 0.150 Å:	6.4	-89.0
22	I.S. and Electrostatics, Δ clamp pt. = 0.200 Å:	6.5	-89.0
Modify Upper Oxide Layer Thickness:			
23	I.S. and Electrostatics; Upper oxide t = 3750 Å:	12.0	-88.9
24	I.S. and Electrostatics; Upper oxide t = 3500 Å:	18.5	-88.8
25	I.S. and Electrostatics; Upper oxide t = 3250 Å:	26.2	-88.8
26	I.S. and Electrostatics; Upper oxide t = 3000 Å:	35.5	-88.6
27	I.S. and Electrostatics; Upper oxide t = 2750 Å:	46.8	-88.3

Conclusions:

- The current triode design is extremely stable under the influence of both electrostatic loads and intrinsic stresses. In the nominal configuration (see figure 3.9), the upper control electrode (UCE) exhibits deflection of only -89.0 Å while the emitter deflects only +6.5 Å (see figure 2)--the emitter deflection is practically zero because the electrostatic pull from the UCE and LCE balance out and cancel. Intrinsic stresses account for most of the deflection--of the -89.0 Å in load case 3, -83.5 Å are due to intrinsic stress, while the remaining fraction are due to electrostatic loads. The deflection of the emitter and upper control electrode are roughly linear with load (for small deflections--at large deflections,

stiffness increases) whereas electrostatic loading is proportional to the inverse square of gap size. If the deflection is great enough, the electrostatic load will supercede the magnitude of the emitter/UCE bending restoring force, instability will occur, and the emitter and UCE will short together. Results indicate however, that the magnitude of the electrostatic forces are much smaller than the bending restoring force, and therefore the above scenario is not a concern. [Compare load cases 1 and 3]

- In the baseline configuration, the emitter deflection is negligible due to a balancing of electrostatic forces from the upper and lower control electrodes. Thus, shortening the UCE tends to unbalance the emitter and cause deflection. However, even when the UCE has been shortened 50%, the deflection at the emitter tip is still only -26.3 Å. Thus, from a mechanical point of view at least, a shorter UCE has little detrimental effect on device life. [Compare load cases 3 through 8]

- Shortening or lengthening the control electrodes and emitter structures by +/- 0.5 μm (due to a longer oxide etch for example) has a small overall effect. In the worst case, that of a 0.5 μm extension (a 25% increase in length), the UCE deflection increases from -89.0 Å at nominal to -141.0 Å when the UCE has been increased--this is a minor change in light of an overall gap size of 4000 Å. [Compare load cases 3 with 12-17]

- The lateral spacing between where the upper and lower oxides attach to the emitter structure was also varied. This geometrical study was done to examine the effects on performance due to varying oxide etch rates--if the etchant was slower on the bottomside, a small difference in clamp points could result (the default geometry in figure 1 shows an offset of 250 Å). The lateral distance was varied from 0 through 2000 Å. The result was that there was nearly zero sensitivity for both the emitter and UCE deflections in response to this change. Although this parameter is difficult to control anyway, these results show that it may be left uncontrolled with impunity.
[Compare load cases 3 with 18-22]

- The TiW layer of the emitter is encased in a nitride sheath, a layer of 1000 Å of nitride above and below it. The upper layer was decreased to 800 Å to examine the sensitivity of the emitter to such process variations. Under this modification, the emitter deflection changes an insignificant amount from +6.6 Å to +20.6 Å. Thus, nitride thicknesses for the emitter sheath do not need to be controlled with exceptional accuracy--what is more important is that low stress nitride films (or those films which are balanced) are used for the emitter sheath. [Compare load case 1 and 2]

- The upper and lower oxide layers are nominally both controlled at 4000 Å in thickness. If these thicknesses differ, then the upper and lower gaps are different and the electrostatic attractive forces on the emitter will be unbalanced. To evaluate this effect, the upper oxide thickness was varied from the nominal 4000 Å down to 2750 Å. The thinner the oxide, the greater the electrostatic loading--at its thinnest, 2750 Å,the electrostatic load is about double the baseline configuration. At an oxide thickness of 2750 Å, the emitter deflection increased from +6.6 Å to +46.8 Å. This is a small response given such a large change in oxide thickness and it suggests that the emitter design as it stands is very robust in light of these types of process variations. Note also that the deflection of the UCE stayed relatively constant at 88.8 to 89.3 Å--this suggests that most of the deflection seen is due to intrinsic stress and not electrostatic loading which shows again that the triode structure is fairly well mechanically designed to weather the overall loads that can be expected to be placed upon it. [Compare load cases 3 with 23-27]

Sub-Task 3.2 Triode Fabrication

5313 - Q1 First Vacuum Transistor Run

We completed the first run of the vacuum transistor. The run had four emitter splits. (a) 200 Å TiW, (b) 400 Å TiW, (c) 200 Å WSix and (d) 400 Å WSix. There were several fabrication issues that we encountered along the way and all of them have been addressed in the process development tasks. Some were solved by making changes in the mask set. We have two wafers with potentially working devices. They have been loaded into the vacuum system and will be tested in early October. Below is a summary of the changes made in the fabrication process :

- The emitter layer support nitride thickness was increased or an etch stop was used between the emitter and the lower nitride layer
- The sacrificial layer was changed to PECVD Oxide for faster emitter layer release. and the thickness was reduced in samples where the emitter nitride layer thickness was increased
- The nitride layer is now layered with two outer nitride layers which are resistant to buffered HF and inner layer of low stress nitride.
- The comb definition step and the emitter cap definition steps have been revised to have proper inspections to prevent incomplete etching at critical steps necessary for the self alignment of the emitter to the control electrodes.

A second triode device fabrication run . . been initiated with the above changes and should be ready for test in early November.

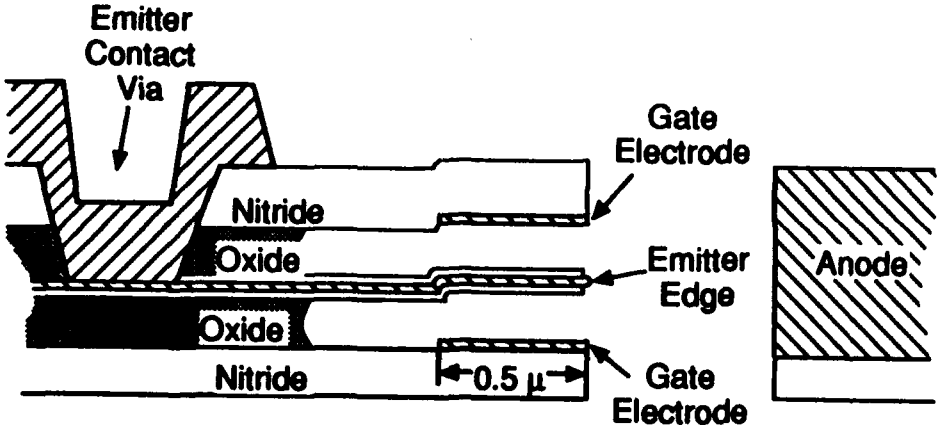
IV. Plans for Next Quarter

- Test triodes from first triode fabrication run.
- Complete 2nd fabrication of edge triodes.
- Evaluate diode arrays from first diode array fabrication run.
- Complete 2nd diode array fabrication run and test diode arrays for current levels.
- Complete high frequency test set-up for vacuum triodes.
- Demonstrate 1 GHz modulation of a vacuum edge emitter triode.

V. Attachments

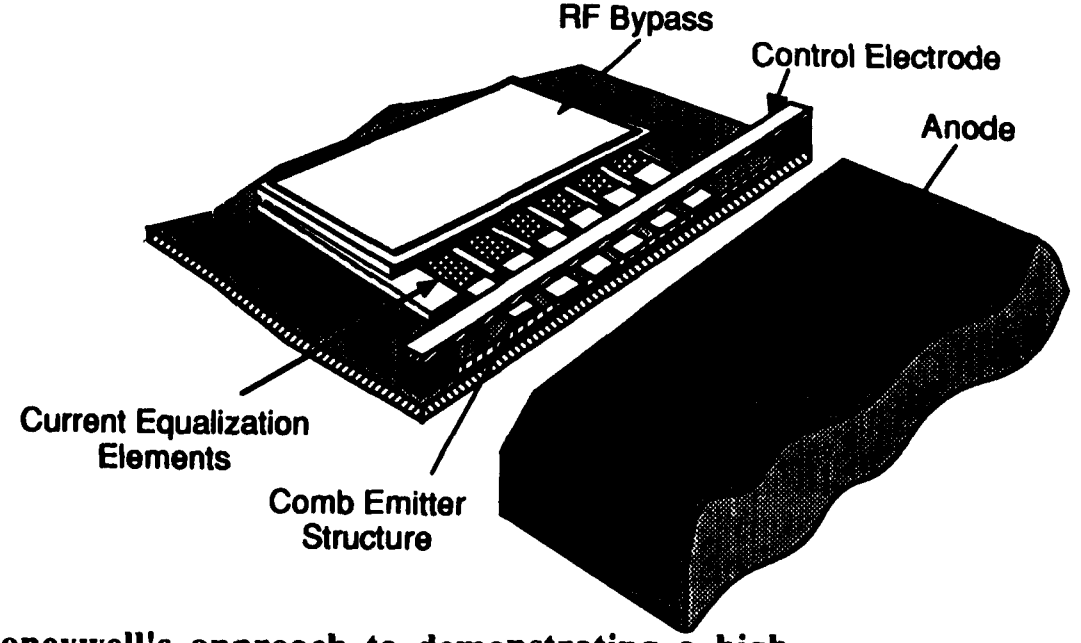
- Abstract entitled "Nanometer Thin-Film-Edge Emitter Devices" by A.I. Akinwande, P. Bauhahn, H. Gray presented at the International Vacuum Microelectronics Conference in Vienna in July, 1992.
- Abstract entitled "Nanometer Scale Thin-Film-Edge Emitter devices with High Current Density Characteristics" by A.I. Akinwande, P.E. Bauhahn, H.F. Gray, T.R. Ohnstein and J.O. Holmen. Accepted for presentation at the International Electron Devices Meeting (IEDM) San Francisco, 12/92.
- University of Minnesota Subcontractors Report on Vacuum Sealed Microdiodes.

Honeywell's Technical Approach



Cross Section of Triode Structure

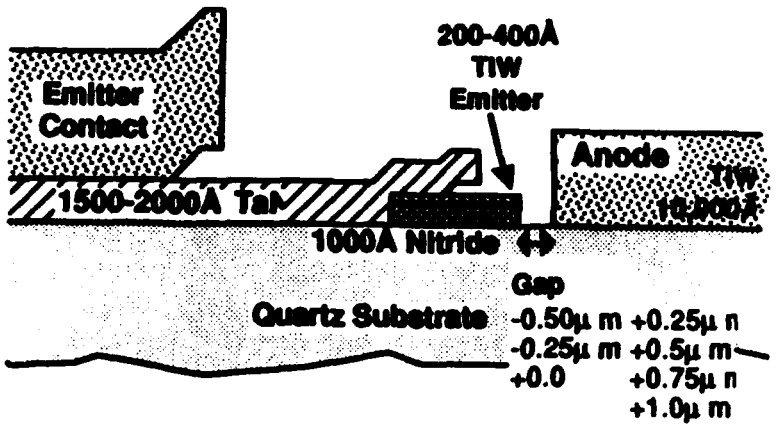
- Thin-film edge emitter
- Current equalization elements
- RF bypass



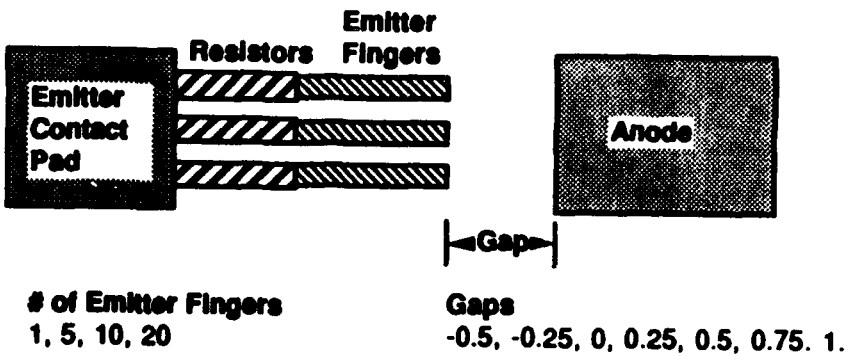
- Out-of-plane anode
- Air-bridge metallization
- Submicron control electrodes

Figure 1.1 Illustration of Honeywell's approach to demonstrating a high frequency vacuum amplifier. Thin film technology and surface micromachining techniques are utilized to form an edge emitter triode.

Field Emitter Test Structure



Cross Section of Field Emitter Test Structure



Top View of Field Emitter Test Structure

- Comb structure
- Thin-film emitter
- Thin-film resistor

- Emitter with and without combs
- Emitters with and without resistors
- Novel structures to determine electron trajectory
- Novel structures to determine positive ions or secondary electrons

Figure 1.2 Field Emitter Diode Configuration.

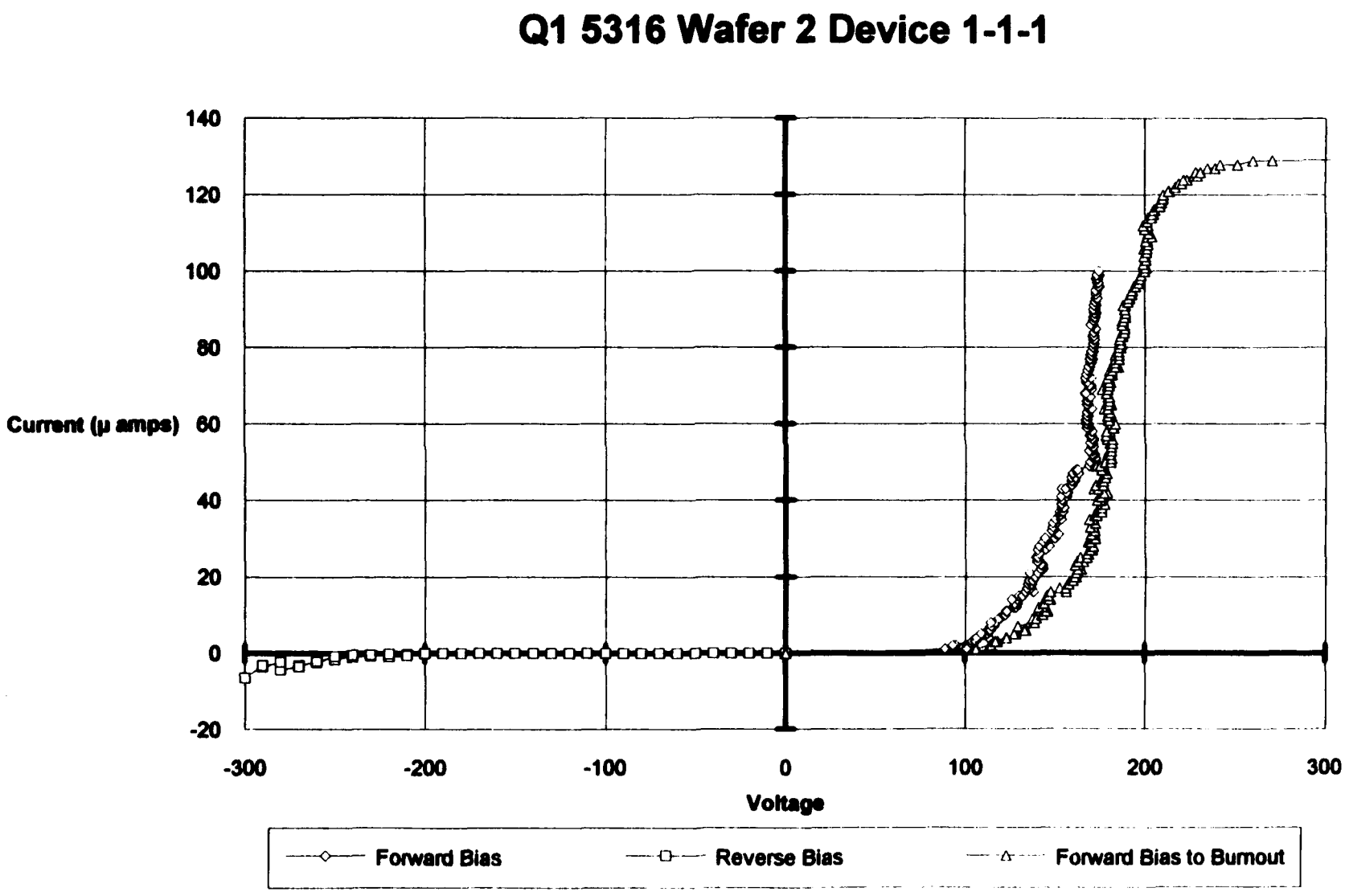
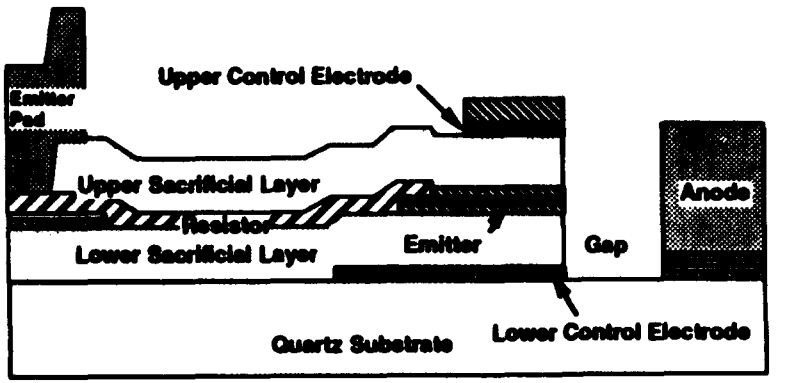


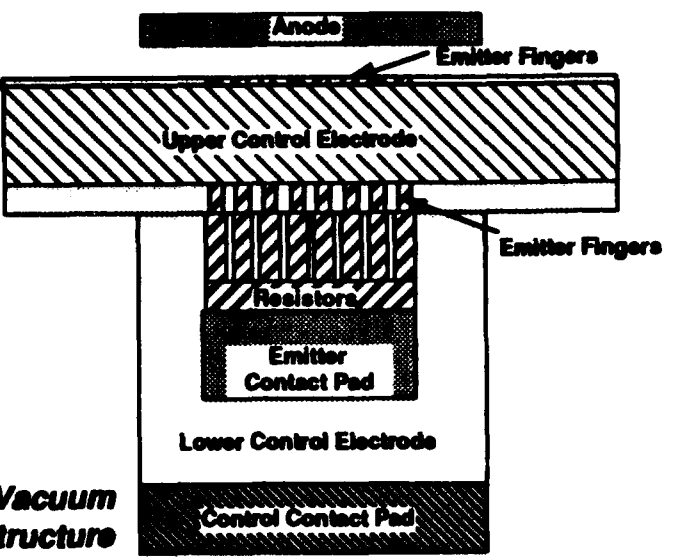
Figure 1.3 Demonstration of repeatable diode-like IV characteristics for a comb-emitter diode with series resistors.

Vacuum Transistor Structure and Design

- Comb emitter
- Thin–film resistor
- Refractory metal emitter
- Heat–sink emitter



Sideview of Vacuum Transistor Structure



Layout of Vacuum Transistor Structure

Figure 3.0 Vacuum Transistor with Comb Emitters and Series Resistors.

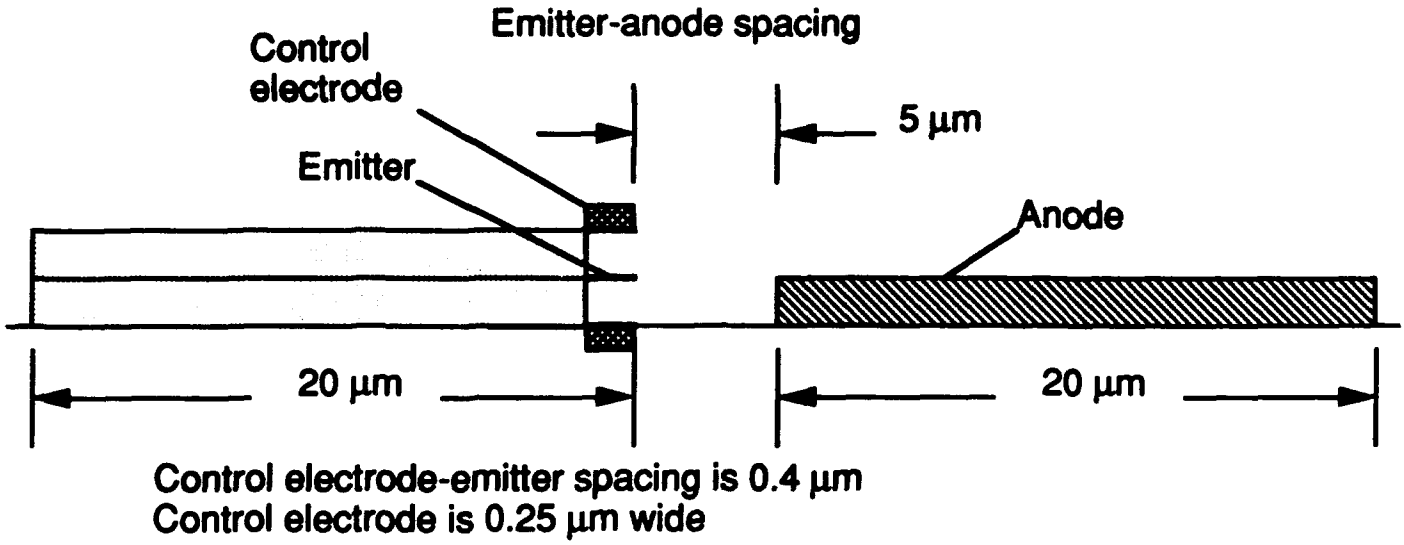


Figure 3-1 Cross Section of a Single Cell of an Edge Emitter Triode

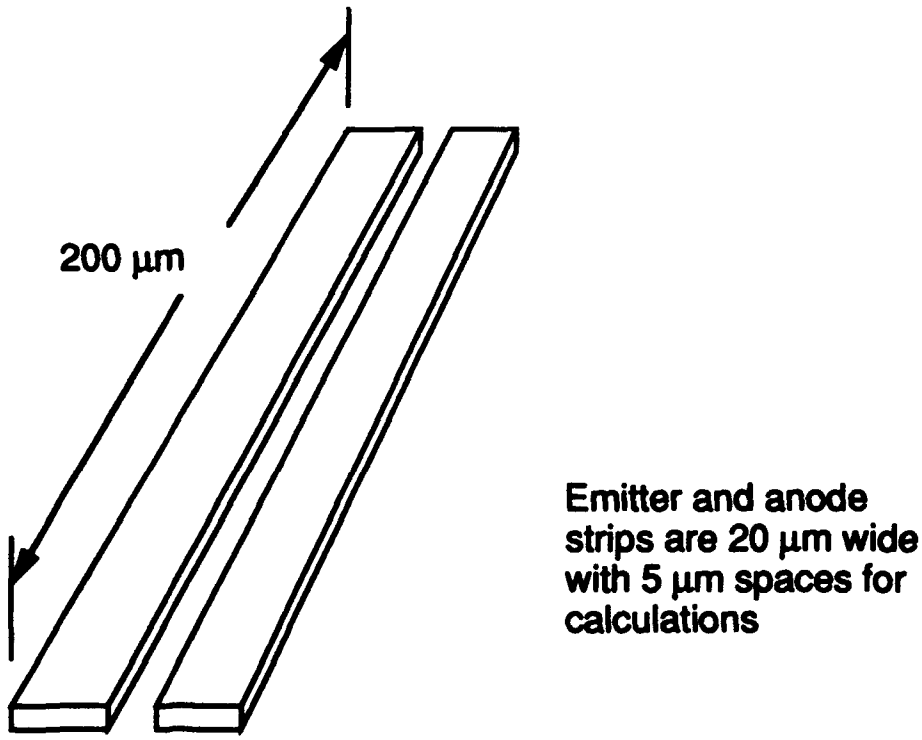


Figure 3-2 Edge Emitter Electrode Geometry Used in Calculations

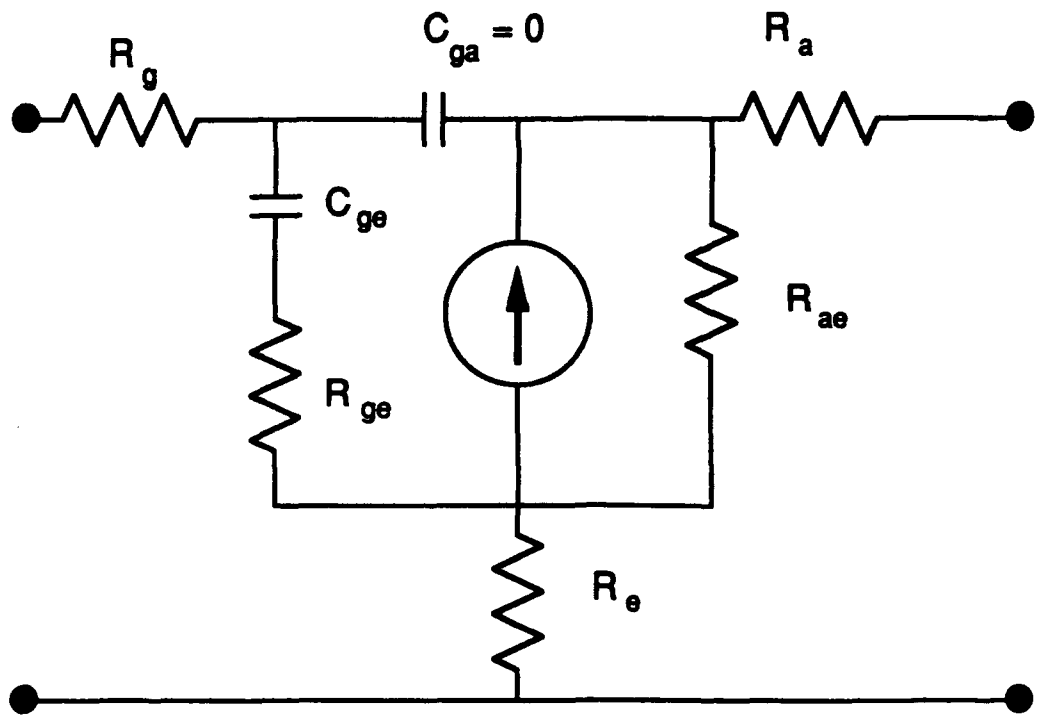


Figure 3-3 Equivalent Circuit Used for Device Performance Calculations

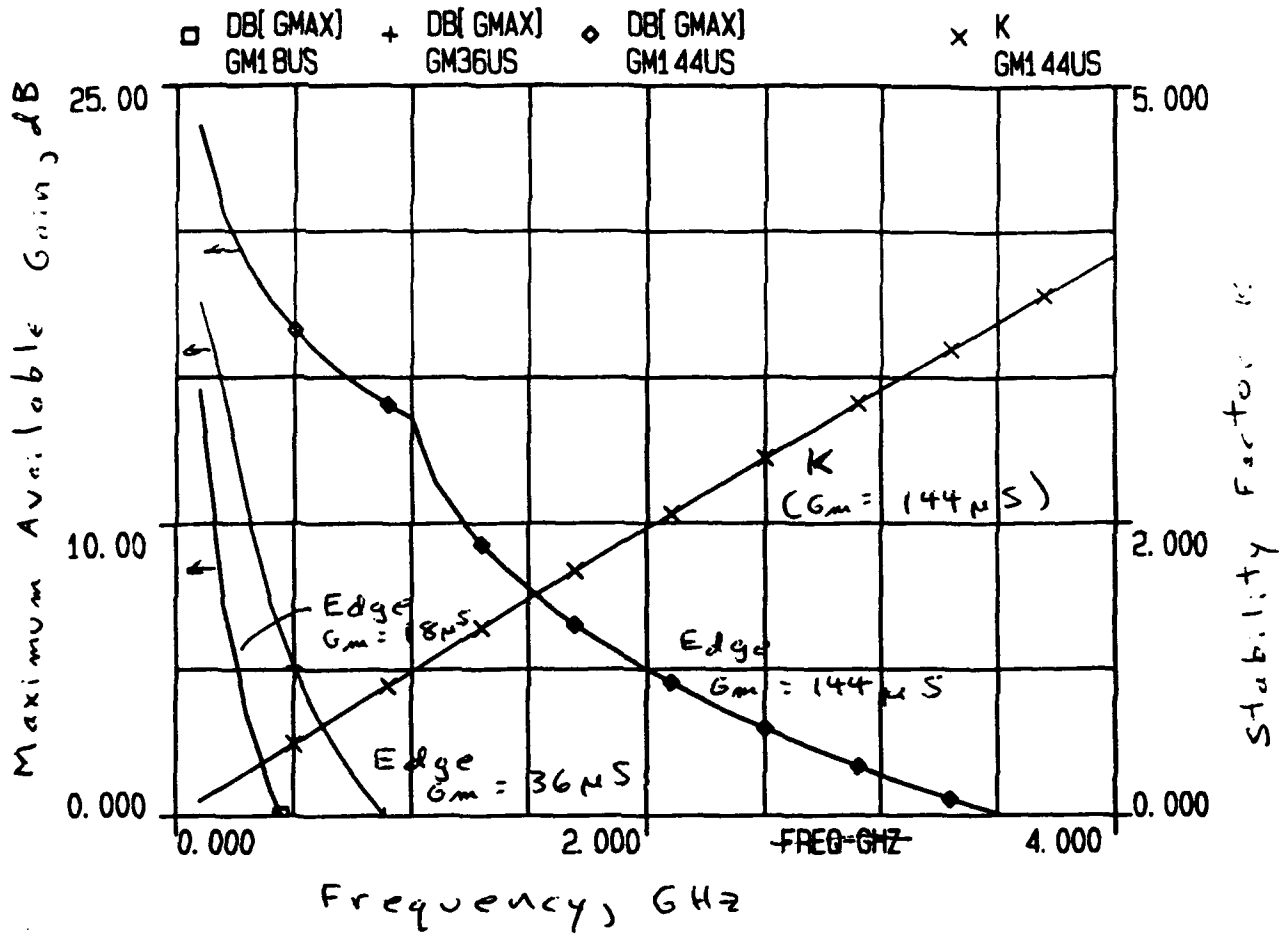


Figure 3-4 Maximum Available Gain versus Frequency and Stability Factor for Three Field Emission Triode Transconductances.

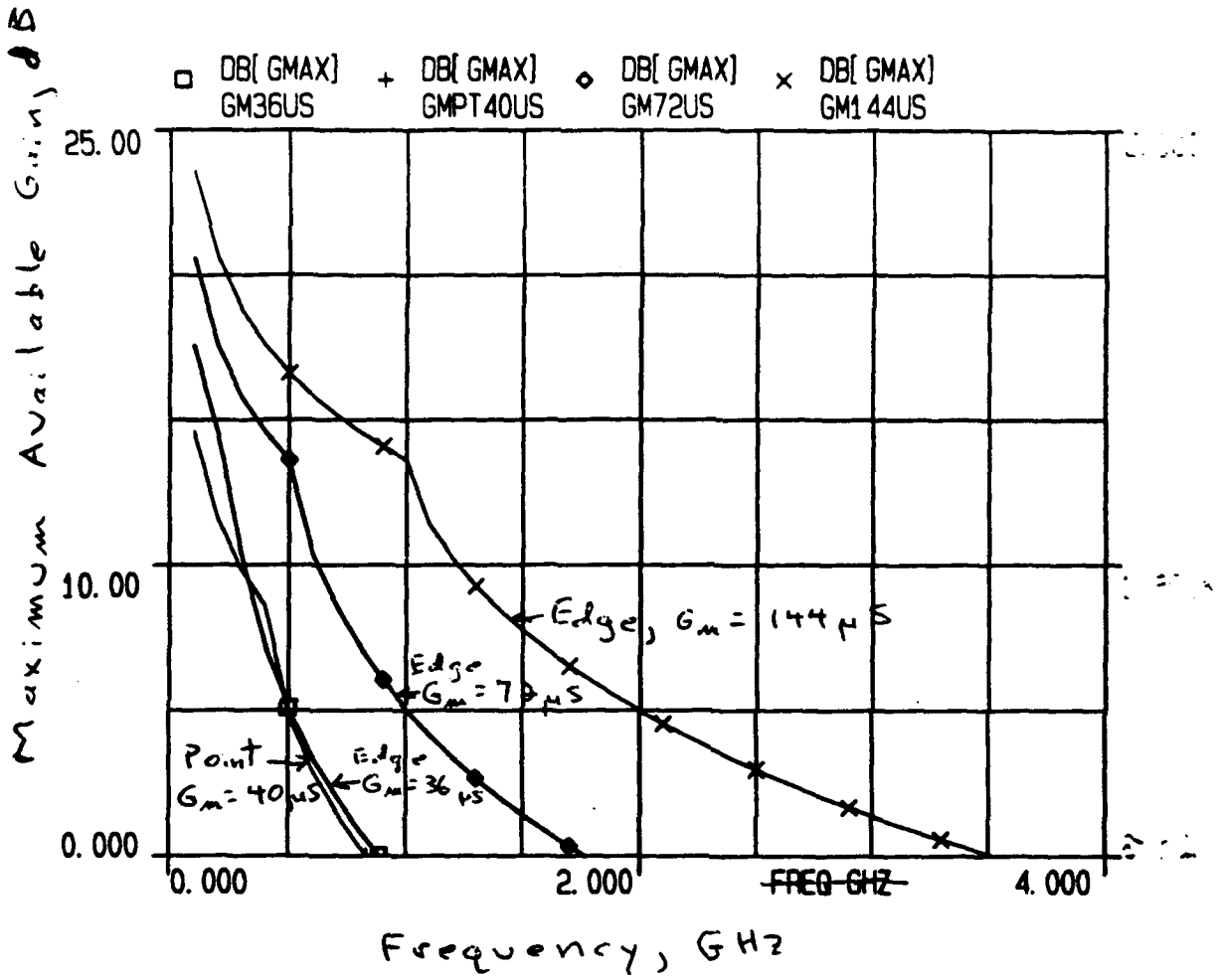


Figure 3-5 Comparison between Edge and Point Field Emitter Triodes for the Current State-of-the Art with the Same Current for a One Micron Edge and a single Point.

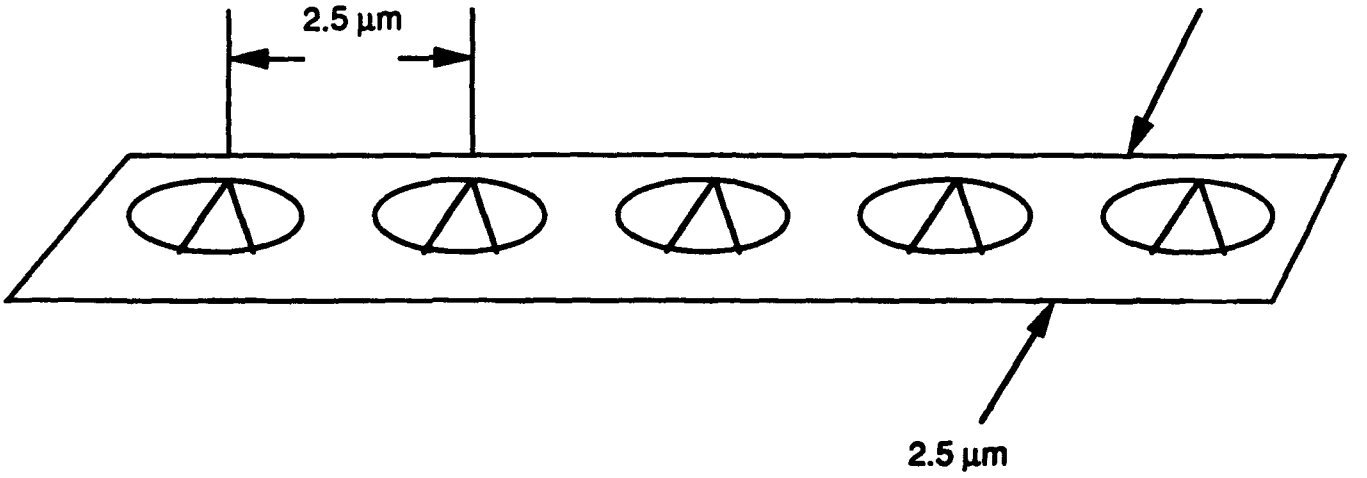


Figure 3-6 Agressive Point Emitter Structure Used in Simulations

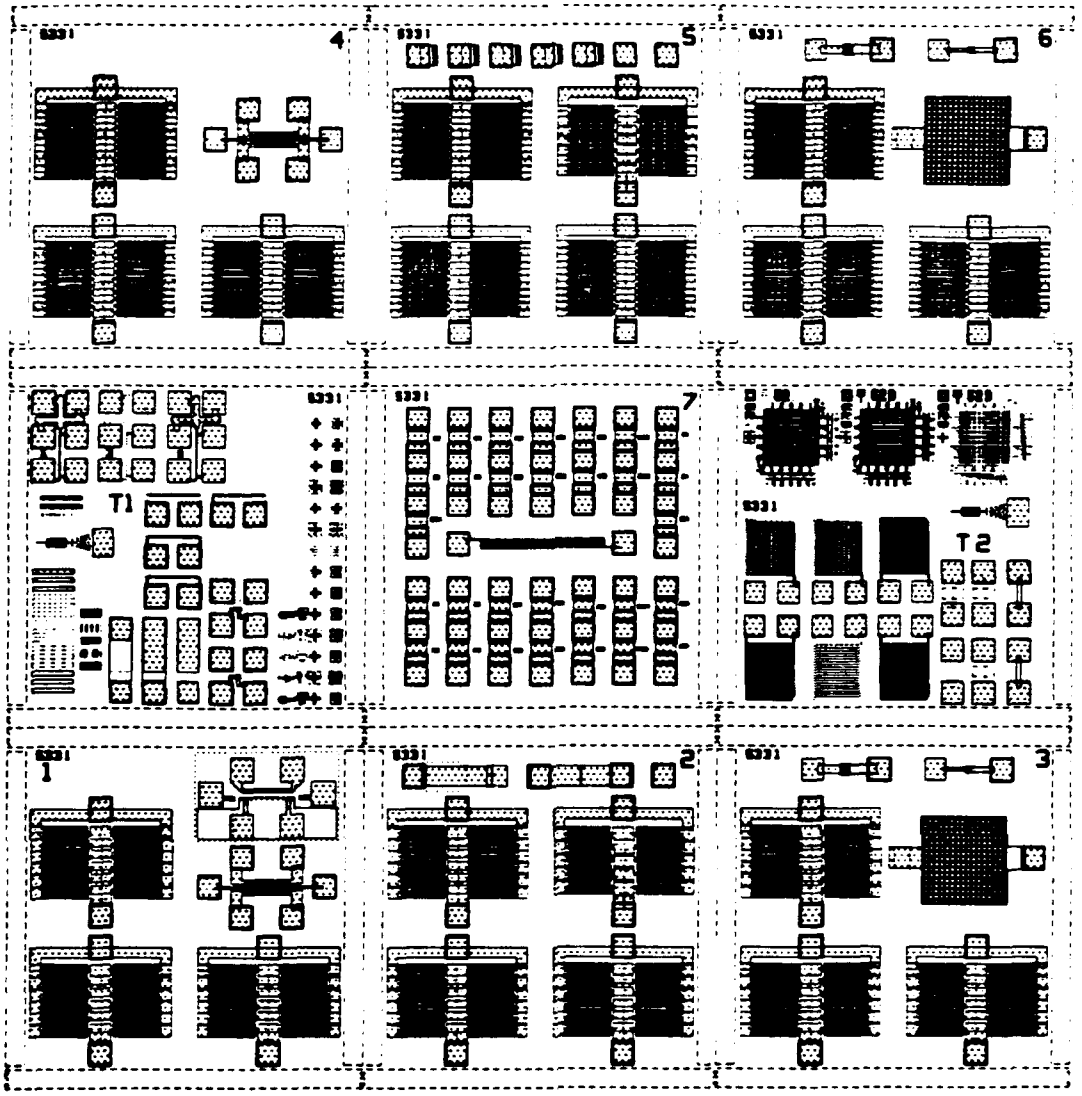


Figure 3.7 High Power Diode Array Reticle Showing the Test Patterns and High Power Diode Structures.

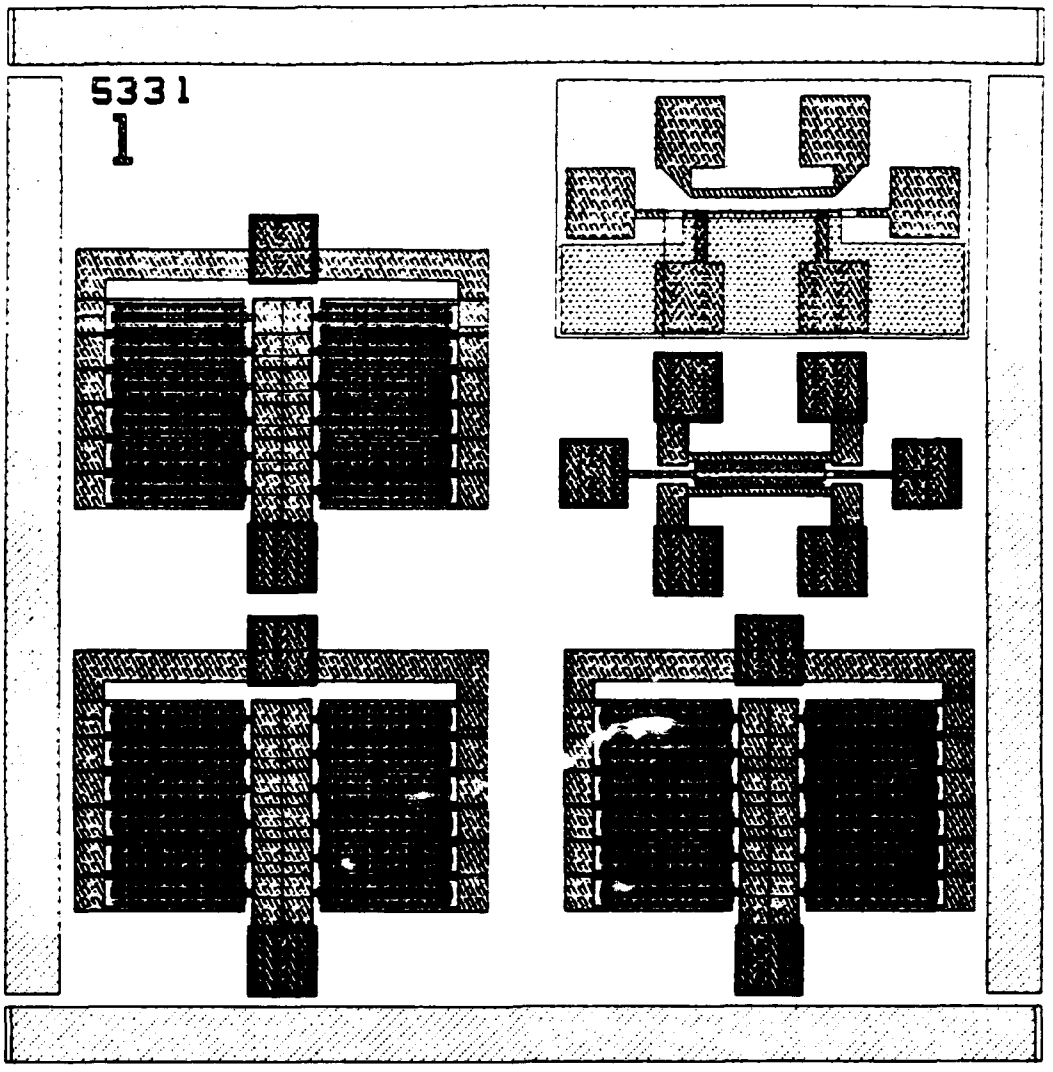


Figure 3.8 The First Die in the High Power Diode Reticle with Diodes and a Self-Aligned Triode Test Structure.

Nanometer Thin-Film-Edge Emitter Devices with High Current Density Characteristics

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Abstract

Conventional distributed interaction thermionic emission cathode tubes have demonstrated power outputs exceeding 1 megawatt for a wide range of microwave frequencies while solid state field effect transistors continue to break previous records for low noise performance up to 100 GHz. For many applications, these devices are quite appropriate. However, the tube cost, weight and power supply complexity as well as power outputs exceed many budget requirements. Solid state devices, operating at low voltages, may have insufficient power outputs. The field emission triode may offer advantages as a compromise device with more power output than the solid state approach with simpler power supplies and lighter weight than other vacuum tubes.

We report the demonstration of thin-film-edge emitter devices with reproducible high current density characteristics. The demonstrated devices include both diodes and triodes with thin film emitters, anodes and control electrodes on the same wafer. Contrasted with the usual vertical FEA structures, this particular triode design invokes two dimensional vertical symmetry for the extraction electrodes using multi-layer thin-film deposition and patterning techniques. A central nanometer thick edge-emitter film is sandwiched between two extraction electrodes (one above and one below). This design and fabrication methodology has several major advantages compared to the classical vertical FEA design: (1) The radius of curvature of the electron emitter must be less or equal to the thickness of the thin film emitter metallization. The thickness of the thin film can be controlled to nanometer dimensions by a number of known deposition processes. (2) The distance between the control electrodes and the emitter is determined by the thickness of deposited insulator thin films. These thicknesses can also be controlled to nanometer tolerances by deposition processes. (3) The total electron path can be potentially much shorter than vertical designs. This distance, which determines the total transit time, might be important for high frequency operation. (4) No critical dimension is dependent on high resolution lithography. Finite element based simulation of field emitter structures has been used to estimate the electric fields, currents and temperatures of typical devices to enhance our understanding of their operation and suggest techniques to improve their performance.

Figure 1 shows the thin-film-edge emitter triode. The 3D microstructure was fabricated with several nanometer scale deposition, microelectronic patterning and surface micromachining. The self-aligned microstructure techniques used in the fabrication the 3D devices brings the precise geometries of integrated circuit processing to the problem of making vacuum devices. Figures 2 and 3 the IV characteristics and transconductance respectively of a 5 μm wide, 300 Å thick, TiW emitter. The emitter / control spacing is 0.6 μm. At 180 V gate bias the emitted current is about 2 μA and the transconductance is about 0.09 μS.

We have also fabricated thin-film-edge field emitter diodes with the emitter and the anode on the same substrate. Figure 4 is a schematic of the diode structure, while Figure 5 shows a typical IV characteristics of a 300 Å thick TiW field emitter with an anode to emitter separation of 0.4 μm and a cavity depth of 0.5 μm. Figure 5 shows current emission of 100 μA at a voltage of about 250 V for a 20 μm wide edge. This corresponds to a current /unit width of 5 μA/μm. Figure 6 shows a 100 μm wide device. The current was limited at 100 μA to prevent current run-away. The same device was operated at a current of 50 μA for longer than 100 hours as shown in Figure 6. We were able to obtain a current of 160 μA from the same device. We shall report the results of other emitter materials and geometries.

We acknowledge the support of DARPA under the Vacuum Microelectronics Program and the COTR - Bert Hui

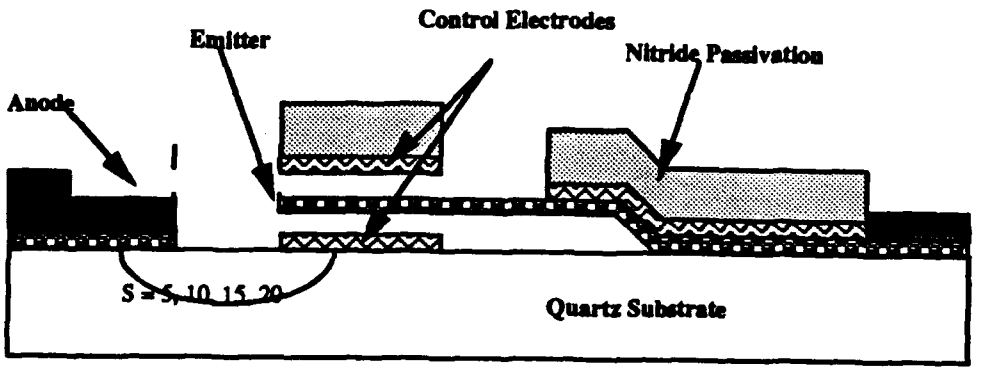

Figure. 1 Vacuum Transistor with Thin Film Edge Emitter and Symmetrical Control Electrodes.

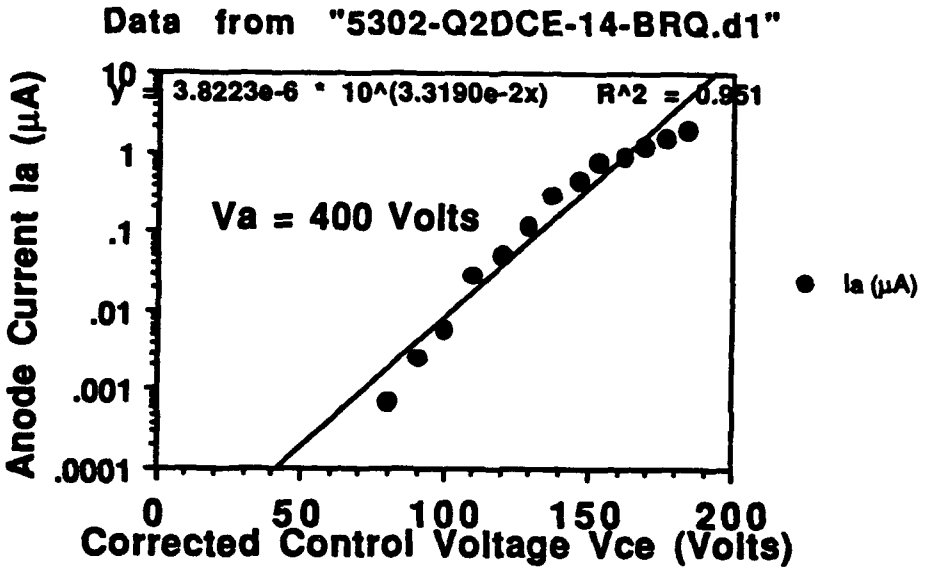

Figure 2. Vacuum Transistor IV plot. The anode voltage is 400 V.

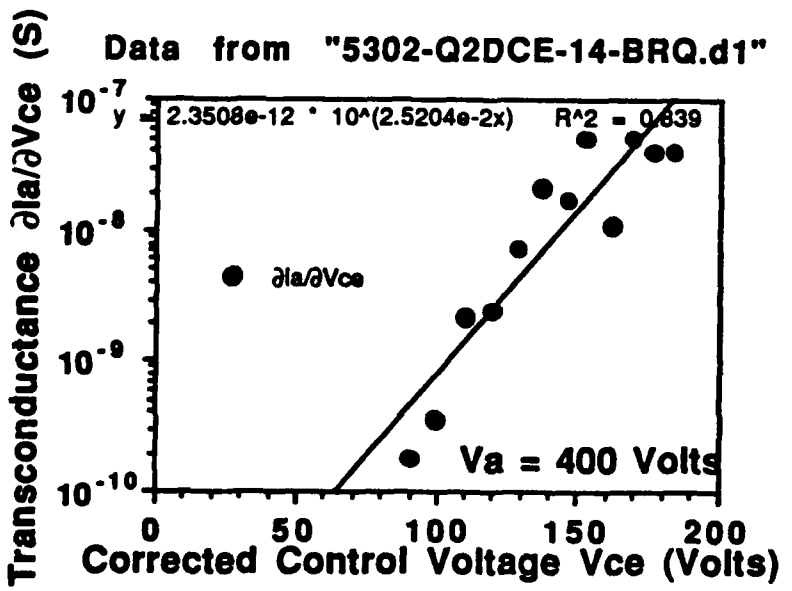

Figure 3. Vacuum Transistor Transconductance vs Control Voltage. The anode voltage is 400 V.

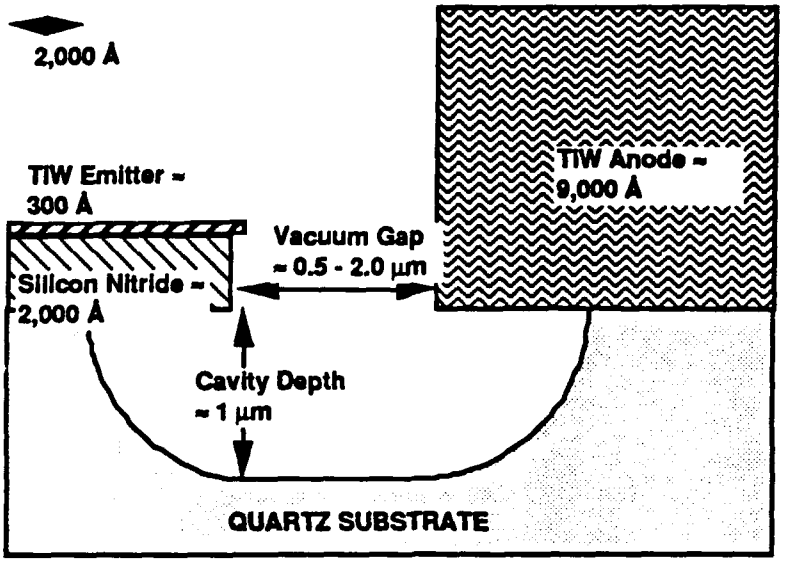

Figure 4. Thin-Film-Edge Field Emitter Diode Structure.

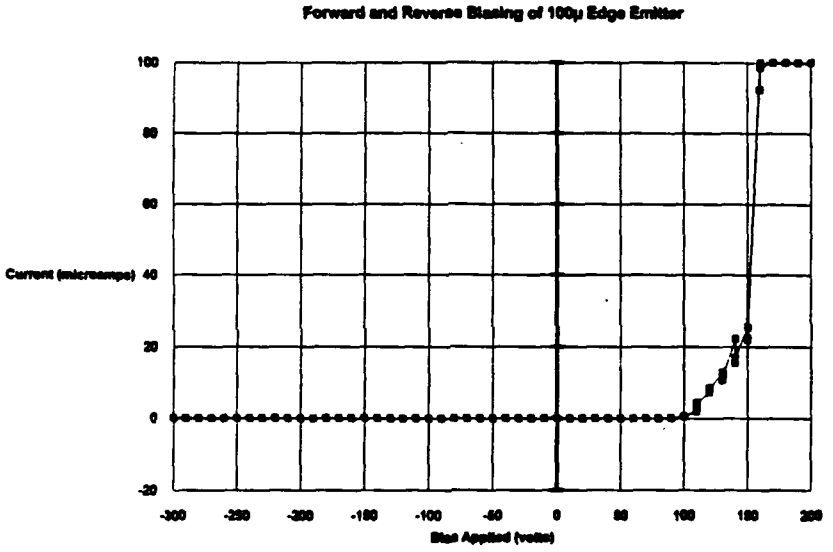

Figure 5. IV Characteristics of a 300 Å thick TiW Emitter. Anode to Emitter Spacing is 0.4 µm.

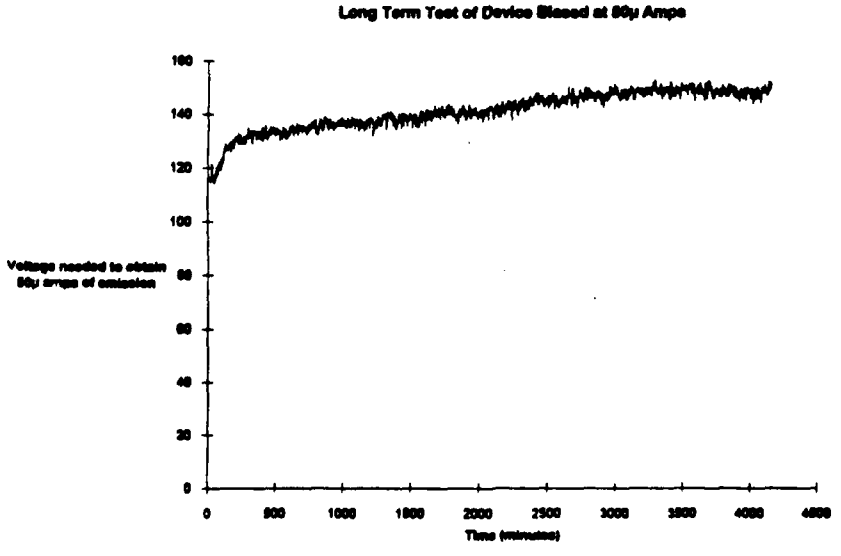

Figure 6. Long Term Test of 100 µm Wide Field Emitter Diode. Emitter Current vs Time

Nanometer Scale Thin-Film-Edge Emitter Devices With High Current Density Characteristics

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ABSTRACT

We report the demonstration of thin-film-edge emitter devices with reproducible high current density characteristics. The demonstrated devices include both diodes and triodes with thin film emitters, anodes and control electrodes on the same wafer. Contrasted with the usual vertical FEA structures, this particular triode design invokes two dimensional vertical symmetry for the extraction electrodes using multi-layer thin-film deposition and patterning techniques. Emission currents as high as 400 μA per edge have been demonstrated and current densities as high as 10 μA/μm of edge width.

INTRODUCTION

Conventional distributed interaction thermionic emission cathode tubes have demonstrated power outputs exceeding 1 megawatt for a wide range of microwave frequencies while solid state field effect transistors continue to break previous records for low noise performance up to 100 GHz. For many applications, these devices are quite appropriate. However, the tube cost, weight and power supply complexity as well as power outputs exceed many budget requirements. Solid state devices, operating at low voltages, may have insufficient power outputs. The field emission triode may offer advantages as a compromise device with more power output than the solid state approach with simpler power supplies and lighter weight than other vacuum tubes. The structure most commonly associated with the Field Emission Array is one which consists of a micron size cell with a cone-like vertical field emitter and an integrated circular aperture which surrounds the emitter tip [1,2]. While most of this work to date has focused on the vertical field emission devices, lateral emitters formed by planar lithography and surface micromachining are just beginning to be studied [3,4]. For high frequency operation, the most important figure of merit is f_τ (unity current gain cut-off frequency) which is proportional to the ratio of the transconductance to the input capacitance. Compared with conventional semiconductors, FEA based devices have lower capacitance because of the their lower effective dielectric constant. This implies that FEAs require lower transconductance to achieve the same f_τ assuming the same capacitance level. However for vertical FEAs having the cone like structure, the device capacitance is dominated by a parasitic component governed by the active and inactive area of the FEA and it is usually large compared to the intrinsic capacitance of the device. An approach to reduce the effect of parasitic capacitance is to scale devices to smaller geometries. The transconductance / unit area will increase at a faster rate than the capacitance leading to increased f_τ. However with this scheme, the capacitance is not independent of the transconductance. An approach that allows simultaneous increase in transconductance and decrease of capacitance is the lateral thin-film edge emitter shown in Figure 1.

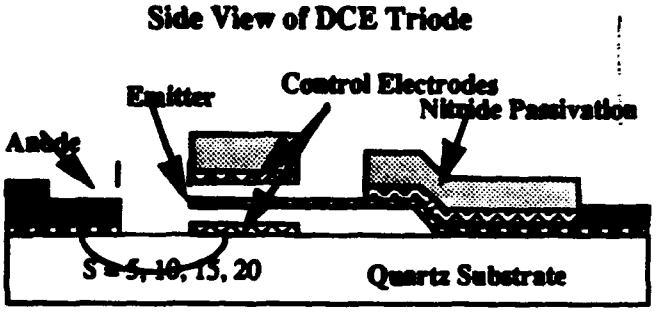

Figure 1. Vacuum Transistor with Dual Control Electrodes.

THIN-FILM-EDGE EMITTER VACUUM TRANSISTOR

Contrasted with the usual vertical FEA structures, this particular triode design invokes two dimensional vertical symmetry for the extraction electrodes using multi-layer thin-film deposition and patterning techniques. A central nanometer scale thick edge-emitter film is sandwiched between two extraction electrodes (one above and one below). The thin-film-edge emitter maximizes transconductance, g_m and minimizes the extraction electrode capacitance C because (i) emission occurs along a thin film edge, thus enabling the use of very narrow extraction electrodes with a small area per unit current and (ii) transconductance is maximized because the very small radius of curvature is ensured by the thin dimension of the emitter film. These two factors ultimately lead to improved f_τ. In essence, the edge has one key advantage : it allows more emitting points / area to be packed into the area between its control electrodes than it is possible with point emitters surrounded by extraction electrodes. This design and fabrication methodology has several other major

advantages compared to the classical vertical FEA design: (1) The radius of curvature of the electron emitter must be less than or equal to the thickness of the thin film emitter metallization. The thickness of the thin film can be controlled to nanometer dimensions by a number of known deposition processes. (2) The distance between the control electrodes and the emitter is determined by the thickness of deposited insulator thin films. These thicknesses can also be controlled to nanometer tolerances by deposition processes. (3) The total electron path can be potentially much shorter than vertical designs. This distance, which determines the total transit time, might be important for high frequency operation. (4) No critical dimension is dependent on high resolution lithography. Finite element based simulation of field emitter structures has been used to estimate the electric fields, currents and temperatures of typical devices to enhance our understanding of their operation and suggest techniques to improve their performance.

The device shown in Figure 1 is a 3D microstructure and was fabricated with several nanometer scale depositions, microelectronic patterning and surface micromachining. The self-aligned microstructure techniques used in the fabrication of the 3D devices brings the precise geometries of integrated circuit processing to the problem of making vacuum devices. The devices are 5 μm wide and have 300 Å thick TiW emitters. The emitter is supported on both sides by a 1500 Å thick layer of silicon nitride for mechanical stability. The emitter / control electrode spacing is 0.7 μm. The upper control electrode is supported on the top side by a thick nitride layer because of the expected electrostatic forces on the control electrode when the devices are biased. The sacrificial layer is removed by buffered HF.

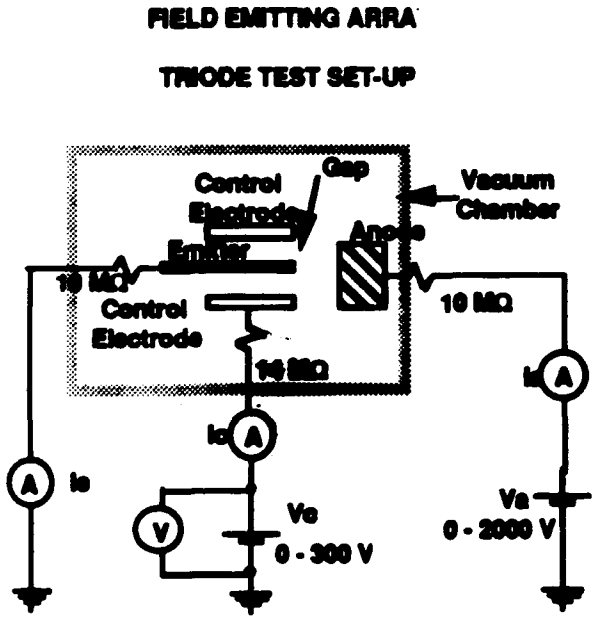

Figure 2. Vacuum Transistor Test Set-Up.

Figure 2 shows the test set up for the vacuum transistor. The vacuum was maintained at a pressure less than 1 x 10^{-8} Torr. Figures 3 and 4 show the I-V characteristics and Fowler Nordheim plot of a vacuum transistor. The device turns on at 70 V and at a gate voltage of 180V the emitted current is 2 μA. The corresponding anode voltage is 400 Volts. Figure 5 is a plot of the transconductance and it shows a maximum transconductance of about 0.1 μS. Figure 6 is the IV characteristics corresponding to an anode voltage of 600 V indicating a maximum current of 3 μA with a transconductance of 0.2 μS.

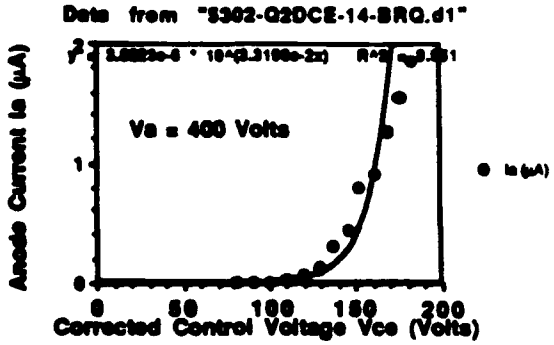

Figure 3. I-V characteristics of a Vacuum Transistor. Anode Voltage is 400 Volts.

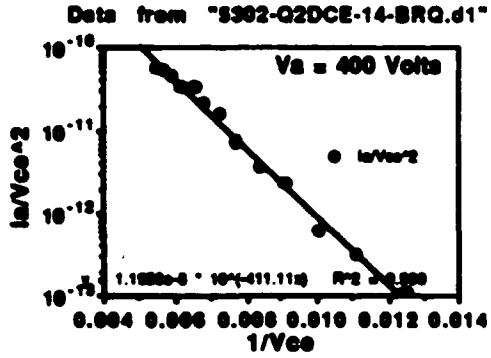

Figure 4. Fowler Nordheim Plot of a Vacuum Transistor. Anode Voltage is 400 Volts.

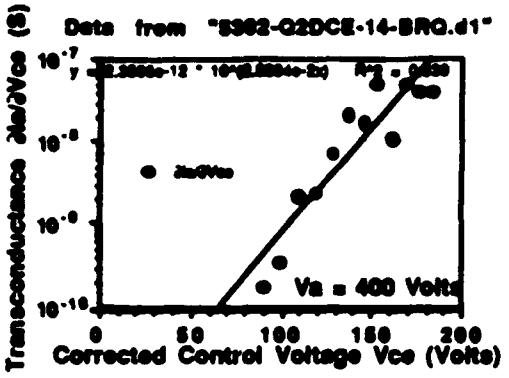

Figure 5. Transconductance of a Vacuum Transistor. Anode Voltage is 400 Volts.

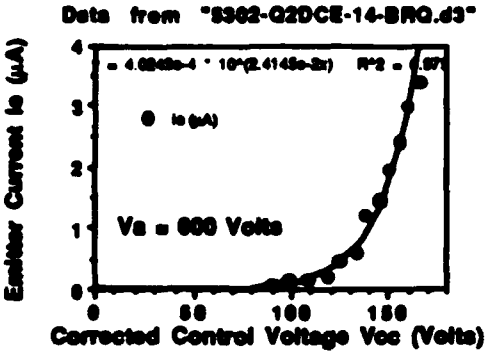

Figure 6. I-V Characteristics of a Vacuum Transistor. Anode Voltage is 600 Volts.

THIN-FILM-EDGE EMITTER DIODE

The critical part of the vacuum transistor is the thin-film edge emitter. To electrically characterize the film's field emission characteristics, we used special diode structures with submicron spacing between the emitter film edge and an in-plane anode. Figure 7 is a schematic of the thin-film edge vacuum diode. Figure 8 shows the current voltage characteristics for a 300 Å TiW emitter. Table 1 is a summary of the maximum current obtained for each device width and the maximum current density. We demonstrated a maximum current of 385 μA for a device that is 100 μm wide and maximum current density of 9.6 μA/μm of width for a device that is 5 μm wide. There is a decrease in the maximum current density as the edge width increases. It can be concluded that emission from the edge is not occurring just at the corners, however the corners may have a dominant influence. We did long term tests on the devices by measuring the voltage required to maintain 50 μA emission from a 100 μm wide edge. Data was taken every 5 seconds. The device was still operational after more than 72 hours.

Device Width	Max Current	Current Density
5 μm	48 μA	9.6 μA / μm
10 μm	59 μA	5.9 μA / μm
20 μm	165 μA	8.3 μA / μm
50 μm	288 μA	5.8 μA / μm
100 μm	383 μA	3.8 μA / μm

Table 1. Summary of Emission Current and Emission Current Density.

PREDICTED PERFORMANCE

The equivalent circuit for our devices is shown in Figure 9. We extracted the transconductance per unit width of the diode and triode devices and using a conservative transconductance value of 0.1 μS / μm and a current of 10 μA / μm of width and also assuming a gate width of 0.25 μm, we obtain from our modeling a predicted f_{max} of about 1 GHz as shown in Figure 10. The performance expected with various multiples of these currents are also displayed in the same figure. We expect the transconductance per unit width to increase as the device and process is optimized. The transconductance will increase if the radius of curvature of the emitter and the emitter / extraction electrode distance is decreased.

SUMMARY

In this paper we report the demonstration of thin-film-edge emitter devices with reproducible high current density characteristics. The demonstrated devices include both diodes and triodes with thin film emitters, anodes and control electrodes on the same wafer. The results indicate the possibility of a new type of microwave power sources with power handling capability of power tubes and high frequency performance of semiconductors.

ACKNOWLEDGEMENT

We acknowledge the support of DARPA under the RF Vacuum Microelectronics Program.

REFERENCES

[1] C Spindt et al, " Physical properties of thin film field emission cathode with molydenum cones," Journal of Applied Physics, vol. 47, no. 12, Dec 1976, p.

[2] H. F. Gray et al, "A Vacuum Field Effect Array Transistor Using Silicon Field Emitter Arrays," IEEE-IEDM Technical Digest, 1986, p. 777.

[3] H. F. Gray et al, "Film Edge Emitters : The Basis for a New Vacuum Transistor," IEEE-IEDM Technical Digest, 1991, p. 201.

[4] S. Zurn et al, "Sealed Vacuum Electronic Devices by Surface Micromachining," IEEE-IEDM Technical Digest, 1991, p. 205

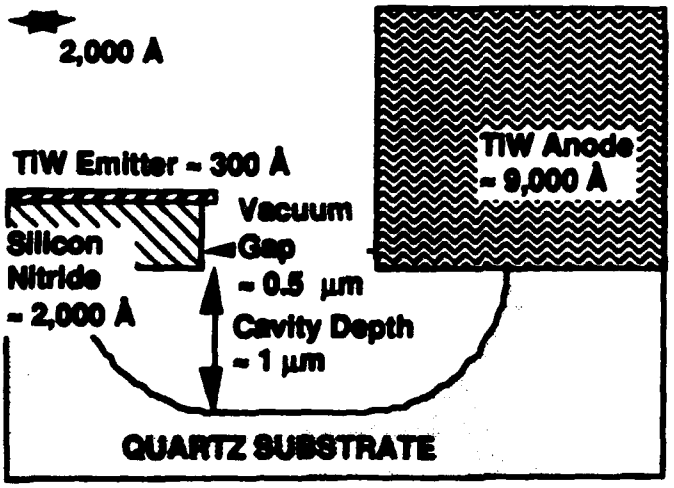

Figure 7. Thin-Film-Edge Emitter Vacuum Diode.

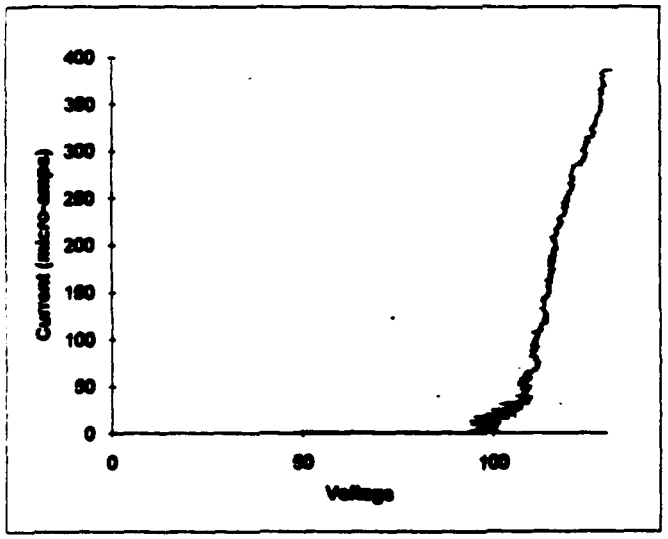

Figure 8. I-V characteristics of a 300 Å Thick TiW emitter. Edge width is 100 µm.

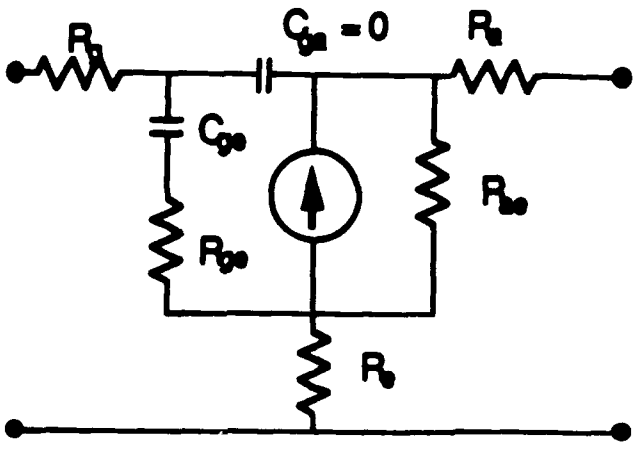

Figure 9. Equivalent Circuit Used in Calculating Performance.

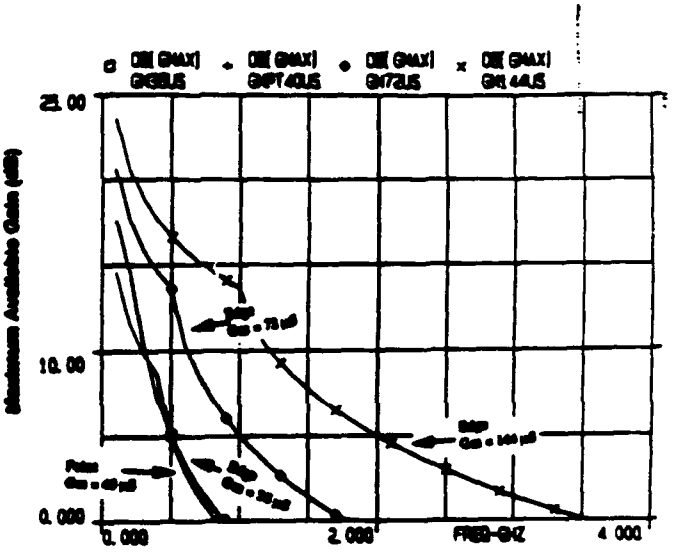

Figure 10. Predicted Maximum Available Gain for Devices with Current Densities Reported Here. A comparison is made to the array of points with comparable transconductance.

QUARTERLY PROGRESS REPORT #2
(7/1/92 - 9/30/92)

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Sub-contracted from Honeywell, Inc.
Sensor and Systems Development Center
10701 Lyndale Ave. South
Bloomington, Minnesota 55450
Attn: Dr. David Arch

Effective Date of Contract: 4/15/92

Contract Expiration Date: 12/31/92

Contract Amount: Basic $50,000
Options $ _____

Principal Investigator: Prof. Dennis L. Polla
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Title of Work: *Planar-Processed Vacuum Microelectronic Devices with On-Chip Cavity Sealing*

I. Executive Summary

Vacuum-sealed microdiode devices based on both polycrystalline silicon and tungsten emitter materials were fabricated this quarter. The processing procedures for making these devices was refined. Electrical characterization of the completed devices has been started.

The following are the key achievements for this period:

- Microdiodes were fabricated using surface-micromachining techniques with both polycrystalline and tungsten as emitter materials.
- Key fabrication steps were sequentially carried out and refinements were made to the basic process run sheet.
- Current versus voltage characterization was carried out on these microdiode devices under conditions of 1) self-sealed vacuum, 2) no vacuum, and 3) externally applied vacuum.
- Measurement of the electrical noise voltage in microdiode devices was carried out as a function of frequency.

II. MILESTONE STATUS

MILESTONES	COMPLETION DATE ORIGINAL	ACTUAL
1. Process Design		
1.1 Cavity Formation and Planarization Design	5/92	5/92
1.2 Sealing Method Design	6/92	6/92
2. Test Structure Design	6/92	6/92
3. Sealed Device Fabrication	7/92	7/92
4. Vacuum-Sealed Device Testing		
4.1 On-Chip Vacuum Evaluation	7/92	8/92
4.2 Electrical Characterization	7/92	9/92
4.3 Parasitic Capacitance Model	8/92	-
5. Microtriode Optimization		
5.1 CAD Field and Potential Modeling	8/92	8/92
5.2 Emitter Material Development	9/92	9/92
5.3 Optimized Device Design	9/92	9/92
5.4 Optimization of Sealing Method	8/92	9/92
6. Final Device Fabrication	10/92	-
7. Device Testing		
7.1 Vacuum Evaluation	11/92	-
7.2 Emitter Evaluation	11/92	-
7.3 RF Evaluation	12/92	
8. Final Report	12/92	-

III. TECNICAL PROGRESS

1. Device Fabrication

1.1 Cavity Formation

Experiments showed difficulty in consistently sealing the sides of cavity diaphragms formed above the surface of the silicon wafer. Some devices showed good current-voltage characteristics while others showed no emission current attributed to the atmospheric cavity condition.

1.2 Planarization

Fig. 1 shows a cross section for both vacuum diodes and vacuum triodes being fabricated in this program. Recessed cavities are formed with a depth of 2.0 μm below the surface of the silicon wafer. Both polycrystalline silicon and tungsten have been successfully used as emitter materials fabricated in these recessed wells.

1.3 Cavity Sealing

Because the cavity region of the vacuum devices is almost completely closed, increase reliability of good vacuum conditions has been demonstrated. We have designed a fabrication procedure in which cavity sealing takes place far away from the active region of the emitter device. In particular, via channels measuring 10 μm in wide and 1.0 μm in depth have been processed to allow hydrofluoric acid to remove the temporary PSG sacrificial layer. We have used both aluminum and silicon-compatible insulators to subsequently seal these etch via openings. At the present time a combination of both e-beam evaporated silicon nitride and silicon dioxide have realized good vacuum cavity conditions. While we have not been able to determine the internal vacuum cavity pressure, we are assuming it to be approximately the same of the vacuum ambient during the deposition of the sealing materials, on the order of 10^{-5} T.

2.1 Device Testing

Current-voltage characteristics were measured in sealed and unsealed devices. Unsealed devices showed no current for voltages up to 100 V. Sealed devices were characterized for both polycrystalline and tungsten emitters. The resulting i-v plots are shown in Fig. 2. A single polycrystalline cathode emitter tip showed 50 μA emission current for 48 V applied potential between cathode and anode. Further experiments will use multiple tips and edges to increase this current. These sealed devices showed approximately the same emission currents as unsealed devices operated in a 10^{-5} T vacuum chamber.

Preliminary electrical noise characterization measurements were carried out in vacuum microdiode devices. These initial results show considerably higher low frequency electrical noise in polycrystalline devices than that seen in tungsten devices.

3. Diagnostics

Residual oxide on the cathode emitter surfaces may be present in both our polysilicon and tungsten devices (perhaps also in devices made by other groups). This oxide usually breaks down under an intense electrical field but may be a source of electrical non-uniformity. In our process development we have been using atomic force microscopy to analyze grain size and will apply other surface analysis techniques to understand the structure and composition of the emitter surfaces.

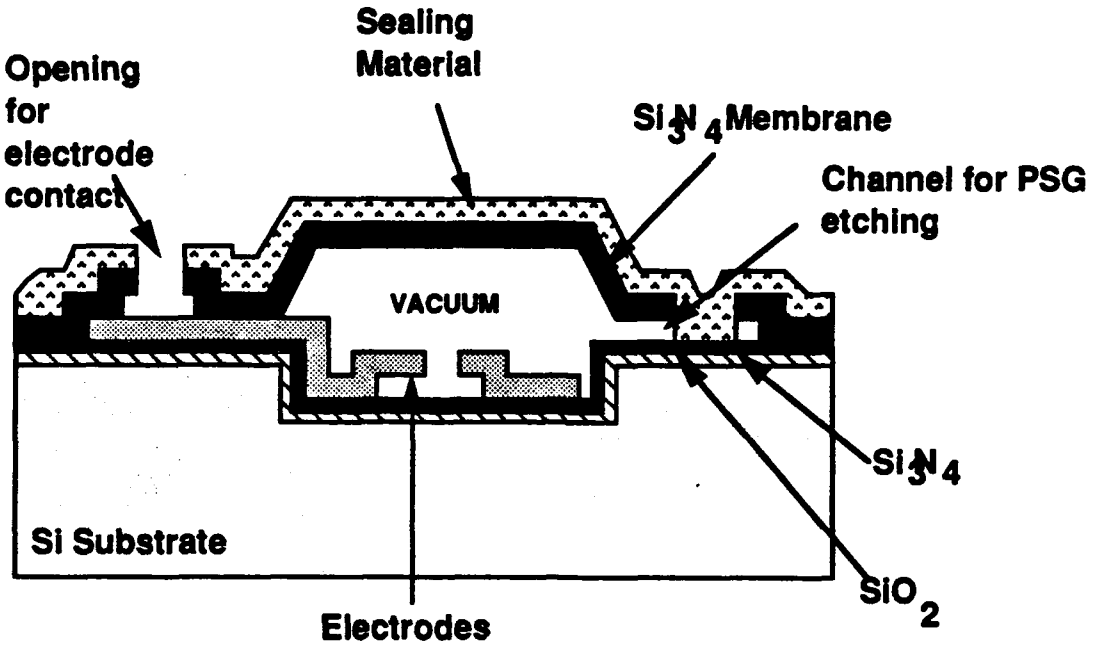


Fig. 1. Cross section of planar-processed vacuum microdiode device with on-chip vacuum cavity sealing.

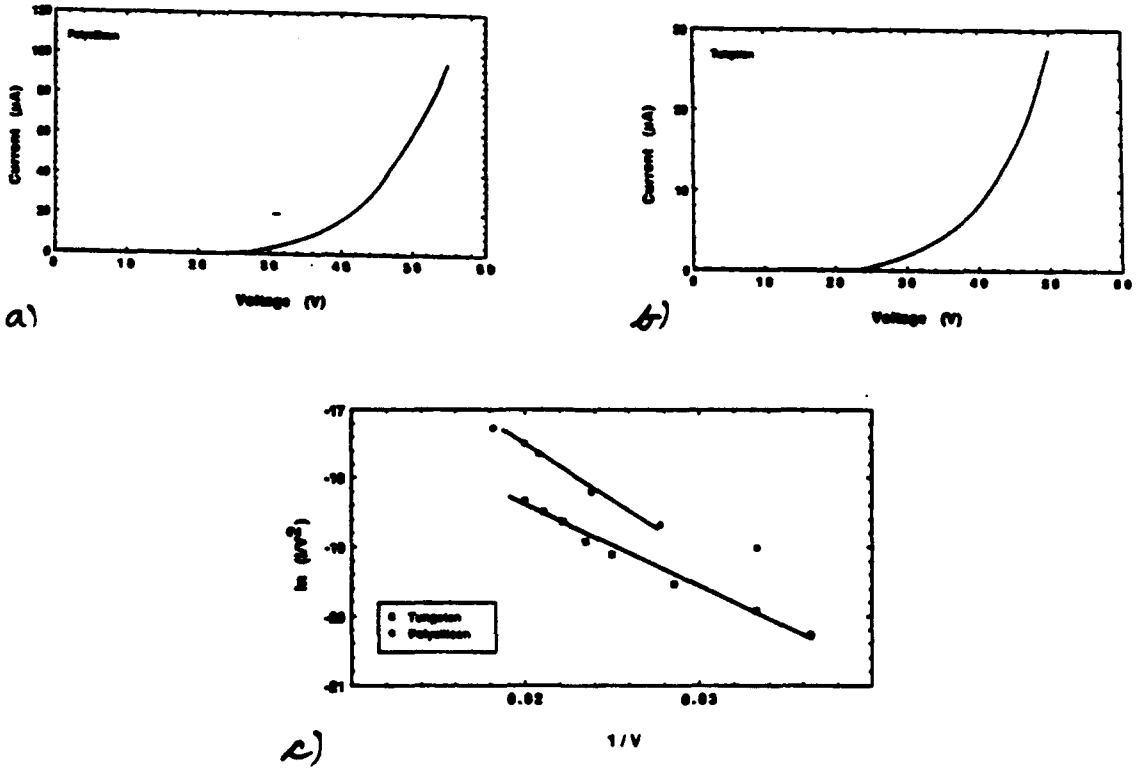
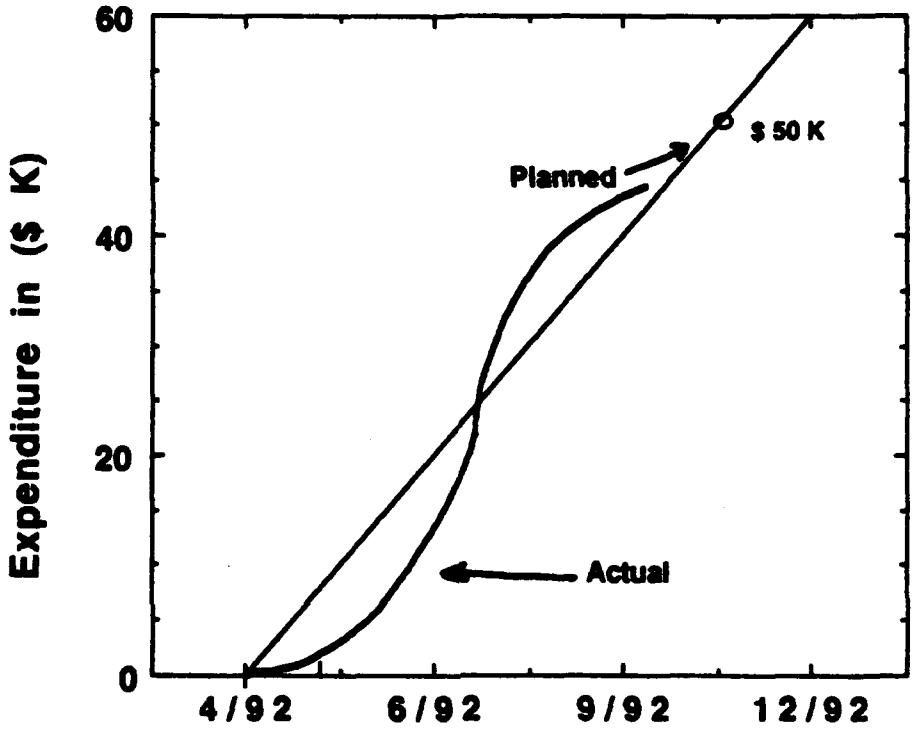


Fig. 2. Measured current-voltage characteristics for a a) polycrystalline silicon, b) tungsten microdiode, and c) corresponding Fowler-Nordheim plot.

IV. FISCAL STATUS



Expenditures this quarter	**$ 24.5 K**
Total expenditures	**Q1: $ 18.8 K**
	Q2: $ 24.5 K
Total to date	**$ 43.3 K**
Project expenditures:	
10/92 - 12/92	**$ 6.7 K**
Total Projected Cost for FY92	**$ 50.0 K**

V. PROBLEM AREAS

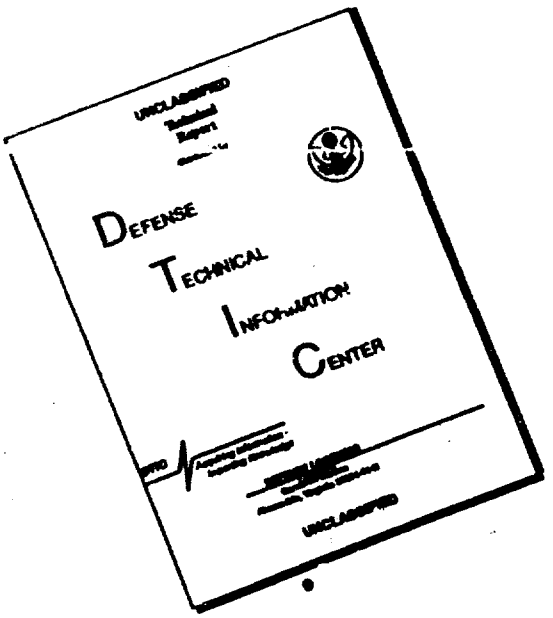
There are no problems areas identified at this time.

VI. VISITS AND TECHNICAL PRESENTATIONS

Presentation of work related to this program was made at the 1992 International Vacuum Microelectronics Conference, Vienna, Austria, Aug. 1992. Oral presentation of a paper entitled "Planar Processed Tungsten and Polysilicon Vacuum Microelectronic Devices with Integral Cavity Sealing," Q. Mei, T. Tamagawa, C. Ye, Y. Lin, S. Zurn, and D. L. Polla was contributed by Professor Polla.

No visitors received information about this project.

DISCLAIMER NOTICE



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