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Silicon Molecular Beam Epitaxy

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Preface

This proceedings contains the papers presented at the 4th International Symposium on Silicon Molecular Beam Epitaxy held at the MRS Spring Meeting in Anaheim, California, 29 April - 3 May 1991. Also included is a key paper presented at the special "Late News" session on Light from Porous Silicon.

We would like to acknowledge the help and advice we have received from the other members of the international organizing committee: Erich Kasper, Evan Parker and Yasuhiro Shiraki. We also depended upon the logistical support of the Materials Research Society staff and on the partial funding of academic travel grants provided by the Air Force Office of Scientific Research. We would also like to thank our roster of invited speakers: M. Pepper, D.J. Gravesteijn, R. Kubiak, D.C. Houghton, R. Zachai, M. Arienzo, F. Schaffler, K. Nakagawa, G. Abstreiter, H. Hirayama, and M. Hirose. Finally, we are indebted to Joanne Lo Piccolo for her assistance in assembling this volume.

Proceedings of the three earlier Si MBE symposium can be found as: Silicon Molecular Beam Epitaxy, J.C. Bean Ed., Electrochemical Society Proc. Vol. PV 85-7; Silicon Molecular Beam Epitaxy II, J.C. Bean and L.J. Schowalter Eds., Electrochemical Society Proc. Vol. PV 88-8; Silicon Molecular Beam Epitaxy, E. Kasper and E.H.C. Parker Eds., European Materials Research Society Symposia Proceedings 10A & 10B and as volume 124 of the journal Thin Solid Films. A 5th Si MBE Symposium is planned for the summer of 1993 in Tokyo, Japan. Those interested in further information should contact Prof. Y. Shiraki of the University of Tokyo.

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27 June 1991

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PART I

**Homoepitaxy and
Substrate Preparation**

INTEGRATION OF Si-MBE AND DEVICE PROCESSING

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ABSTRACT

A review is given of the requirements on MBE-grown layers as far as processing is concerned. Aspects that are considered are: defect density, particulates, background doping and metallic contamination. The stability of the grown layers against thermal anneals is considered. It is shown that normal thermal diffusion in HBT structures is not important, other effects, like transient diffusion following ion implantation, have drastic effects on the grown profiles. As an example the processing of mesa-isolated heterojunction bipolar transistors is treated. It is shown that all-Si transistors can be grown with ideal Gummel plots. The Gummel plots of SiGe HBTs show small non-idealities. The current gain enhancement of the HBTs with respect to the all-Si transistors is shown to be as large as 200 times. Due to transient diffusion, parasitic barriers are formed, that have a detrimental effect on the AC and DC performance.

INTRODUCTION

Since the introduction of Si-MBE in the seventies, this technique has reached a mature stage. The feasibility of the growth of layer structures with very steep, complicated concentration profiles has been shown. If devices are to be made from these wafers, the subsequent processing imposes stringent demands on the grown layers. First of all the wafers have to suffice the standard technology requirements for thickness uniformity, metallic contamination, defect density, particulates, etc., while also the background doping level must be well-controlled and preferably very low. Secondly the stability of the grown profiles against thermal anneals, which are always necessary, has to be sufficient. Diffusion of dopants or Ge has to be prevented.

In the case of $\text{Si}_{1-x}\text{Ge}_x$ heterojunction devices, also the structural stability of the heteroepitaxial layers is extremely important. It appears to be relatively easy to grow metastable, heteroepitaxial $\text{Si}_{1-x}\text{Ge}_x$ layers, but it is very difficult to prevent the onset of strain relaxation by the formation of misfit dislocations, even at relatively low temperatures and short anneals.

This paper starts with a description of the material properties of MBE grown layers and a comparison is made with processing technology requirements. As an example the processing of heterojunction bipolar transistors (HBTs) with a $\text{Si}_{0.8}\text{Ge}_{0.2}$ base is described. The effects of the different processing steps on the eventual transistor performance is discussed in some detail.

MATERIAL PROPERTIES

Deposition uniformity

The thickness uniformity of the deposited layers should be better than 5% to be acceptable in a standard processing line. In our Vacuum Generators V80 system, capable of handling wafers of 150 mm diameter, it has been shown that by electron-beam evaporation on a rotating substrate a thickness variation of the deposited Si can be achieved of less than 1% over a 4 inch wafer, and better than 2% over a 6 inch wafer [1].

Dopants are usually added by evaporation from Knudsen cells. In that case variation of the dopant flux is usually larger than that for the Si (see Fig. 1). For our Sb Knudsen cell we find variations of 8 % over 100 mm diameter, and even 22 % over 150 mm for room temperature deposition. Variations of this magnitude over a wafer are not acceptable in standard technology. However, because growth is usually performed at temperatures for which the surface mobility of the dopant atoms is sufficient to flatten out the deposited profile, the variation in the surface concentration of dopant atoms is usually much lower. Consequently the dopant concentration in the layer will be more uniform. Fig. 1 also shows the surface distribution over a wafer, that was not rotated during deposition of Sb, at a substrate temperature of 750 K. Due to the high surface diffusion, the variation in the Sb concentration now has become less than 4 %. So as far as uniformities are concerned, MBE equipment produces materials with quality sufficient for standard Si-technology.

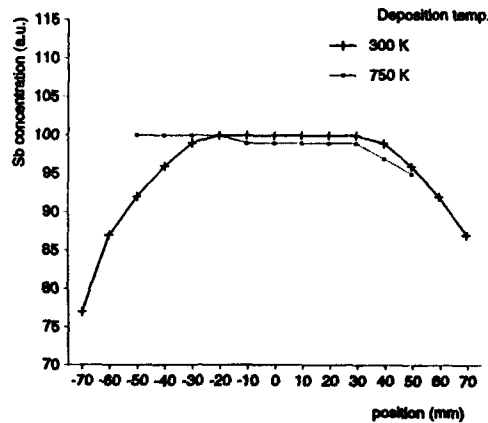


Figure 1 Sb surface concentration distribution over a wafer as measured by XPS. The drawn line depicts deposition on a rotating substrate at room temperature, the dashed represents deposition on a non-rotating substrate at 750 K.

Particulates

With the ever decreasing feature size in Ultra Large Scale Integration (ULSI) it is extremely important to have very low particulate densities. Acceptable levels are less than 1 cm^{-2} . For Si-MBE systems much higher values are found [1,2]. Important contributions seem to stem from the venting of the load-lock and from moving parts in the system (transport system of the wafer, and substrate rotation). The contribution of the electron-beam evaporators to the particle density appears to be quite different for refs. 1 and 2. Pindoria et al. report that due to the growth of Si the density of mainly particulates of all sizes strongly increases, in contrast to our findings. After growth the total density of particulates with an area $>0.3 \mu\text{m}^2$ was found to be 70 cm^{-2} (of which

40 cm⁻² have a area > 0.8 μm²) in our system [1], while Pindoria et al. found much higher densities : 220 cm⁻² with an area > 1 μm².

Concluding we can say that the particulate density of wafers grown in Si-MBE systems is still at least two orders of magnitude too high and prevents the use of this technique in the preparation of circuits with a high level of integration. For discrete applications however, the particulate density does not seem to be a serious problem.

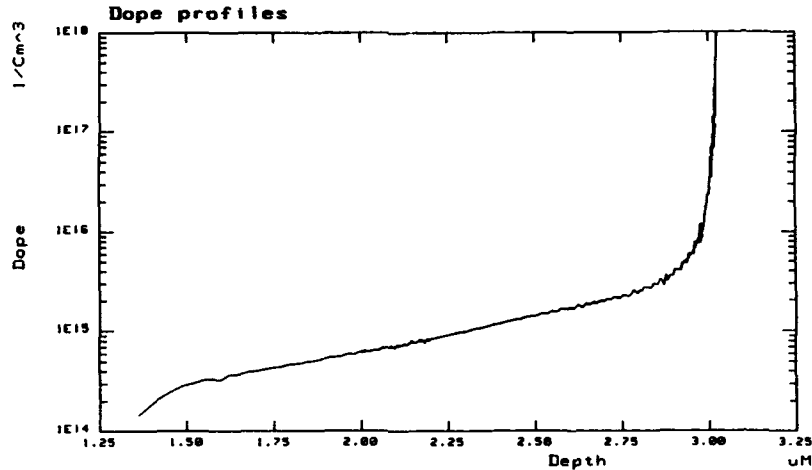


Figure 2 Dopant profile, as measured by CV-profiling, for a 3 μm thick unintentionally doped Si-layer, grown at 690°C. This layer was grown just after Sb doping experiments

Background Doping

The background doping level of the MBE epi-layers is reported to be mainly due to P impurities [1,3-5]. The probable cause for the contamination is the P present in the stainless steel in the growth chamber. Initially the background doping level in our system was $\approx 1 \times 10^{16} \text{ cm}^{-3}$. Fig. 2 shows the depth distribution of the carrier concentration as determined by CV profiling, for a recently grown unintentionally doped Si layer with a thickness of 3 μm, grown at 700 °C. The background doping in our system is n-type with a carrier concentration exponentially decreasing from $3 \times 10^{15} \text{ cm}^{-3}$ at the substrate epi-interface to $2 \times 10^{14} \text{ cm}^{-3}$ at a depth of 1.5 μm. The carrier concentration closer to the surface cannot be determined this way, because it is already depleted by the build-in voltage. These values are somewhat higher than data reported by other authors [3-5]. The origin is a memory effect caused by Sb contamination originating from Sb doping experiments just prior to the growth of this layer. This shows that also for a Si-MBE system which is continuously used for doping experiments low background doping levels can be obtained. For some devices like p-i-n diodes this background doping level is too high, For HBT's this doping level is no problem at all.

Metallic Contamination

If Si-MBE grown devices are to be used in minority carrier devices, the lifetime of the minority carriers has to be sufficiently long, which implies a low recombination center density, which in turn can only be achieved if the metallic contamination is very low. Most sensitively the metallic contamination is determined by Neutron Activation Analysis. Metallic contamination is also inferred from the presence of so-called saucer etch-pits [2,5]. After three years of operation, the main contamination is still Ta, both on the backside and to a lesser extent on the front side. The Ta contamination is not expected to originate from the Ta heater strips, since a quartz diffuser is placed between the heater and the substrate. Possible sources are the Ta heat shields or the collimator above the e-beam evaporator. During operation of our system the Ta contamination initially decreased continuously, but after one year of operation, the Ta level of $\approx 1 \times 10^{15} \text{ cm}^{-3}$ remained constant.

The contamination levels that are found are much too high compared to standard epitaxial Si: levels of around 10^{12} cm^{-3} for most metals are normal in that case. We have however been able to prepare bipolar transistors with ideal behavior [6], indicating a long minority carrier lifetime, and hence a low concentration of generation-recombination centers. A possible explanation of the high minority carrier lifetime in combination with a high metallic contamination might be the precipitation of the metals into electrically inactive clusters.

Sidebotham et al. [7] found with Deep Level Transient Spectroscopy the presence of deep states, which they tentatively assigned to metallic impurities. The concentration of these defects decreased from $\approx 10^{14} \text{ cm}^{-3}$ for growth at $500 \text{ }^\circ\text{C}$ to less than 10^{12} cm^{-3} if growth took place at temperatures above $700 \text{ }^\circ\text{C}$. Also in our layers we have not been able to find deep levels by DLTS (i.e. the concentration is less than $1 \times 10^{12} \text{ cm}^{-3}$), as was also corroborated by the ideal characteristics of the Si transistors and the observation that no Saucer shaped etch-pits were found.

Substrate Cleaning and Interfacial Peak

In all Si MBE grown layers a boron peak at the substrate-epilayer interface has been observed [1,4,8]. The origin of the peak is most probably contamination of the oxide due to B in the air[8]. HF dips largely remove the oxide and the B, however usually C contamination is found. Cleaning methods under inert atmosphere result in clean, B free surfaces[9]. In all our experiments we only performed a standard RCA clean, and desorb the grown oxide by a 5 minutes anneal at $880 \text{ }^\circ\text{C}$. Reflective High Energy Electron Diffraction (RHEED) patterns then always show a clear 2×1 reconstruction, indicative of an atomically clean Si surface. On the substrate/epilayer interface we observe a B spike with an average concentration of $4 \times 10^{12} \text{ cm}^{-2}$. For the devices grown up to now by us this spike is not a serious problem, but in many future devices removal of the interfacial B will be essential.

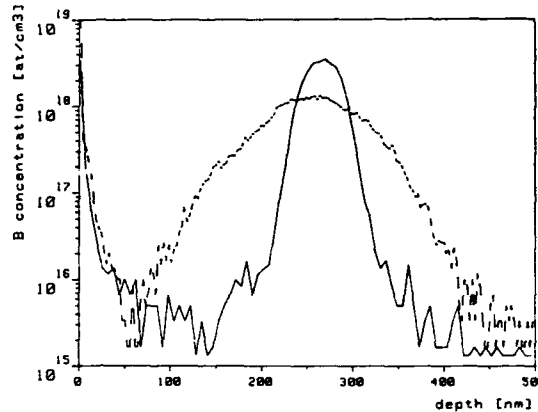
Crystal quality

Generally the quality of the MBE grown layers is found to be perfect when studied with RBS[1,10]. Defect etching usually shows numerous defects ($\approx 5 \times 10^2 - 1 \times$

10^4 cm^{-2}), which originate from the starting surface [1,3,5]. The concentration of defects appears to be strongly dependent on the cleaning method that is used[3,5], and also on the type of substrate that was grown. CZ wafers resulted in 5 x higher defect densities than FZ wafers[1]. After three years of operation we still find defect levels of the order of $1 \times 10^4 \text{ cm}^{-2}$ as determined by Secco etching. The defects we observe are mainly dislocation-associated etch pits. They usually occur in pairs, as has been observed in other systems[11]. We never observe stacking faults.

THERMAL STABILITY

After growth of the desired multilayer structures, a lengthy and usually quite severe process often consisting of many steps is necessary to construct the desired device. This section will discuss the effects of thermal anneals on the profiles of the grown structures, and the stress in the layers.



Diffusion of dopants and Ge

For most HBT structures grown to date with MBE, the thermal diffusion of the dopants is of relatively minor importance: the structures usually start to relax their strain before appreciable diffusion occurs[12,13]. Also the interdiffusion of Ge into Si is completely negligible for these structures at the temperatures and times where implants are activated in SiGe processing (in our case 10 minutes at 850°C) [14,15]. From ref. 15 one expects under these conditions a Ge diffusion length of 0.3 nm. SIMS analysis did not show significant broadening of the B and Ge profiles, while for these structures certainly some strain relaxation is expected [12]. The situation is completely different for structures with extremely thin layers, like High Hole or High Electron Mobility Transistors [16-18]. In these structures doped layers and SiGe are separated by undoped setback layers with a thickness of only 3-10 nm. Relatively modest anneals already lead to sufficient diffusion to have an appreciable effect on the electrical properties of the 2-D carrier gas at the heterojunction.

Although thermal diffusion is negligible in HBT processing, transient diffusion due to implantation damage can have a deleterious effect on the sharp as-grown profiles. Fig. 3 shows the B-profile after a 10 minutes anneal at 850 °C for an unimplanted and an implanted region of a 50 nm thick B-doped Si-layer with a capping layer thickness of 200 nm. The implantation conditions used were: a $2 \times 10^{15} \text{ cm}^{-2}$ As⁺-implantation with an energy of 40 keV, and a $2 \times 10^{13} \text{ cm}^{-2}$ 60 keV P⁺ implantation, implanted under an angle of 7°, which prevents channeling. The As and P profiles are below $1 \times 10^{16} \text{ cm}^{-3}$ at the position of the original B interface. As is

Figure 3 B SIMS profiles for a 50 nm thick B-doped Si-layer with a 200 nm thick capping layer. Drawn line: 10 minutes 850 °C anneal; Dashed line: after implantation and anneal at 850°C for 10 minutes (for details see text)

evident, extensive transient diffusion of the B over >100 nm has occurred. Even for low doses of $2 \times 10^{13} \text{ cm}^{-2}$ P^+ -ions with an energy of 25 keV severe broadening of the profiles results after annealing.

Strain relaxation in $\text{Si}_{1-x}\text{Ge}_x$ heteroepitaxial layers

It is now a familiar fact that it is possible to grow metastable epitaxial $\text{Si}_{1-x}\text{Ge}_x$ layers on Si with thicknesses far exceeding the critical thicknesses calculated from Franck-van der Merwe theory. During processing the strain should not relax. Many articles are devoted to this topic [19]. The importance of the complete absence of dislocations is not evident a priori. The presence of a few misfit dislocations in the active area of an HBT does not seem to be disastrous [20]. From a processing point of view two methods can be used to prevent dislocation formation: a) by using a base width and Ge concentration below the critical line as calculated by Tsao and Dodson[21] or b) adapt the processing in such a way that the relaxation of the material remains negligible. We followed the second approach, because otherwise the advantages of the usage of heterojunctions would remain quite small.

The data gathered by Houghton et al [12,13] for the onset of strain relaxation for base thicknesses and Ge contents around the critical line seem to be very well described by the excess stress description of Tsao and Dodson [21]. From these results we must conclude that typical bases of HBT's (thickness ≈ 100 nm and $x \approx 0.2$), will partially relax during processing. Houghton's phenomenological model [12] gives a very useful description of the relaxation of SiGe layers under thermal anneals. We repeated some of the experiments: a very good agreement was found for the dislocation glide velocities (see Fig. 4). For the nucleation rate of the misfit dis-

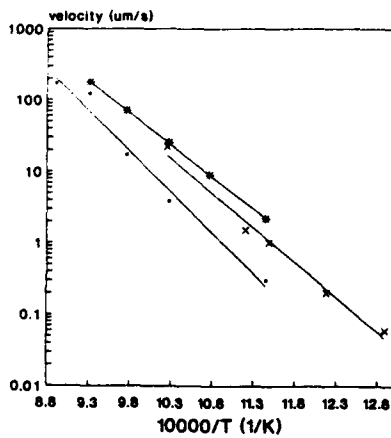


Figure 4 Temperature dependence of dislocation glide velocities for several $\text{Si}_{1-x}\text{Ge}_x$ -layers
 • : $x = 0.16$, thickness = 52 nm
 * : $x = 0.20$, thickness = 50 nm
 x : $x = 0.19$, ref. [12]

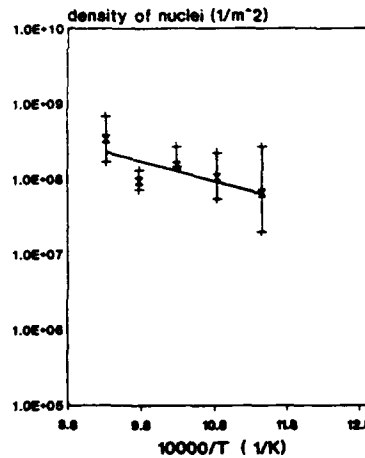


Figure 5 Temperature dependence of the density of dislocation nuclei after a 15 seconds anneal for an $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer with a thickness of 50 nm

locations we did however, find a completely different behavior. In our case the nucleation density did not appear to be very temperature dependent (see Fig. 5); within the large experimental error a density of the order of $1-2 \times 10^4 \text{ cm}^{-2}$ was found. This density is comparable to our defect density and suggests that the defects in the layer act as the nuclei. Further study will be necessary to elucidate the details.

A special point of concern is the observation by Hull et al. [22] that implantation damage can result in enhanced relaxation of strained $\text{Si}_{1-x}\text{Ge}_x$ -layers with p- or n-type dopants below the amorphization dose. A possible explanation of this effect is the increased dislocation nucleation probability due to the high point-defect concentrations arising from implantation.

HETEROJUNCTION BIPOLAR TRANSISTORS

As an example of the problems that can arise during the processing of MBE-grown structures we will discuss the processing and the electrical properties of a SiGe HBT.

Growth procedure

For the growth of our npn SiGe HBTs we did not intentionally dope the emitter and collector layers. We used the fact that our deposited, unintentionally doped Si is always n-type with a doping level around $1 \times 10^{15} \text{ cm}^{-3}$. This eliminates the necessity of time-consuming Sb build-up before growth of the collector and emitter and Sb flash-off after growth of the collector [23].

The layer structures were grown on 0.01 Ωcm Sb doped FZ Si substrates. After thermal desorption of the oxide (5 minutes at 850°C), the substrate temperature was lowered to 700°C , and the 300 nm thick collector layer was grown. After ramping down the substrate temperature to 560°C , a 50 or 100 nm thick base was deposited, by means of co-evaporation of Ge and B-doped Si from e-guns. The B-doped Si in the e-beam evaporator has a B concentration of $\approx 3 \times 10^{19} \text{ cm}^{-3}$. Next a 30 nm i-Si capping layer was deposited during subsequent ramping to the Si growth temperature [23] of 700°C , in order to prevent relaxation of the $\text{Si}_{1-x}\text{Ge}_x$. This high temperature was used to ensure the growth of high quality Si material. The total emitter thickness was 200 nm. The next wafer that was grown always had an identical layer structure, but without Ge.

Fig. 6 shows the SIMS profile of the as-grown HBT structure with the 100 nm base. The B concentration was found to be equal to $2 \times 10^{18} \text{ cm}^{-3}$ and is located fully

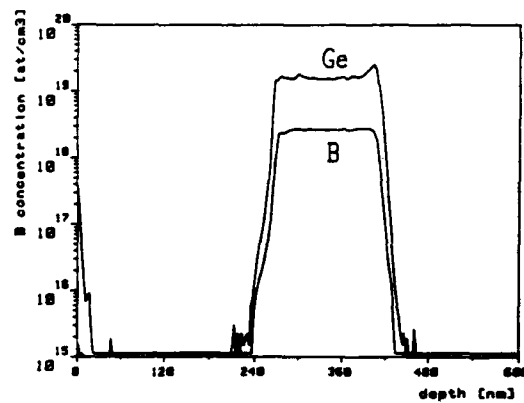


Figure 6 B and Ge SIMS profiles for an as-grown HBT structure with a 100 nm thick $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer

within the Ge profile. The Ge content was 20 %. Chemical defect etching has shown that no misfit dislocations are present in both the 50 and 100 nm base structures, indicating that they are still fully strained.

Processing

Mesa-etching by means of reactive ion etching and passivation by TEOS were used to obtain lateral isolation. Fig. 7 shows a schematic drawing of the cross-section of a transistor. Base contacts were made by double implants, consisting of a dose of $2 \times 10^{13} \text{ cm}^{-2}$ B^{+} ions with an energy of 25 keV, and a BF_2^{+} implant with an energy of 16 keV and a dose of $1 \times 10^{15} \text{ cm}^{-2}$. The actual emitter was also formed using a double implant: 90 keV P^{+} with a dose of $2 \times 10^{13} \text{ cm}^{-2}$, together with an As^{+} implantation of $2 \times 10^{15} \text{ cm}^{-2}$ with an energy of 50 keV. The implantation angle was perpendicular to the surface. These double implants with a high dose and short range together with a low dose and a larger range were used to prevent large leakage currents due to end-of-range damage of the high-dose implant that is not completely annealed-out after the furnace anneal. The low dose implants need a much lower anneal to become fully activated. The implantation activation anneal we used was a 10 minutes furnace anneal at 850 °C

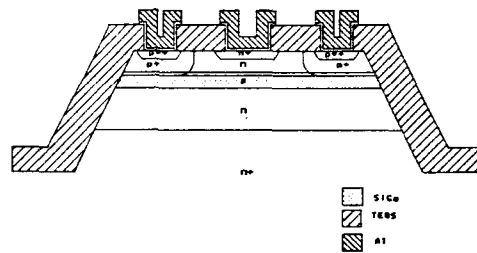


Figure 7 Schematic cross-section of the mesa-structured HBT

Structural analysis

Fig. 8 shows the SIMS profiles of the transistor after annealing. The profiles of the dopants are quite different from the ones calculated with a simulation program like SUPREM3. The causes are twofold. The phosphorous profile is much deeper than expected, due to the channeling that is very important for a light element like P. Due to the variation of the implantation angle over the 4 inch wafer, which amounts 3.5° for our ion-implanter, less channeling occurs on the edges of the wafers. As a result the P-profile is steeper on the edges of the wafer (see Fig. 8). Secondly the B profile is much broader than in the grown structure. This effect is due to the transient diffusion of the B introduced by the implantation damage, as discussed already above (cf. Fig. 4). As a consequence the emitter-base and base-collector-junctions do not coincide anymore with the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ junctions. The effects of this transient diffusion on the electrical properties will be discussed in the next section.

Electrical characterization

Fig. 9 shows the Gummel plots of the Si and $\text{Si}_{0.8}\text{Ge}_{0.2}$ base transistors from the center of the wafer[6]. The emitter area was $12 \times 62 \mu\text{m}^2$. As can be seen both the base and the collector current of the Si-transistor are ideal over more than 4 decades of collector current. This indicates for the first time that high quality transistors can be made from Si-MBE grown material. The SiGe HBT shows an ideal collector current and only a small non-ideality in the base current[17,25,26]. We found that the non-ideality decreases with increasing annealing times. Some relaxation of the $\text{Si}_{1-x}\text{Ge}_x$ will occur, as was shown above. This implies that apparently the presence of misfit dislocations does not have a disastrous effect on the electrical properties.

The collector-current enhancement of an npn HBT, with a constant band gap narrowing in the base ΔE_g with respect to a Si npn bipolar transistor is given by [20]

$$\frac{(I_C)_{\text{SiGe}}}{(I_C)_{\text{Si}}} = \frac{(N_C N_V D_n)_{\text{SiGe}}}{(N_C N_V D_n)_{\text{Si}}} \exp\left(\frac{\Delta E_g}{kT}\right)$$

where D_n is the electron diffusion coefficient in the base, and N_C and N_V are the densities of states in the conduction and the valence band, respectively.

The collector current enhancement of the fabricated HBTs depends strongly on the position on the wafer. From the center to the edge of the wafer it decreases gradually from ~ 200 to ~ 12 under otherwise identical conditions at a collector base voltage of 2 V. Also a variation in the intrinsic base resistance was found: it decreased from 5.6 to 4.5 $\text{k}\Omega/\square$. This difference can be explained in terms of the variation of the phosphorus profile over the wafer. Both in the center and on the edges the emitter-base junction is located very closely to the Si/SiGe heterointerface. The base-collector junction however, is located in the Si of the collector layer. In the center of the wafer the width of this p-Si layer is approximately 50 nm, while at the edges the base-collector junction is located at the position where the background-doping level of the collector ($2 \times 10^{15} \text{ cm}^{-3}$) equals the diffused B profile. This is approximately 100 nm away from the heterointerface. The p-Si layer results in a base-collector junction in Si instead of in SiGe. As a consequence parasitic barriers are formed in the conduction band, which lead to a deterioration of the electrical properties [6,27,28]. By applying a bias over the base-collector junction, the barrier can be effectively reduced in transistors made in the center of the wafer. As a consequence the current gain increases. This was confirmed by 1D device simulations [6,28]. On the edge of the wafer, where the barriers are much broader, they cannot be

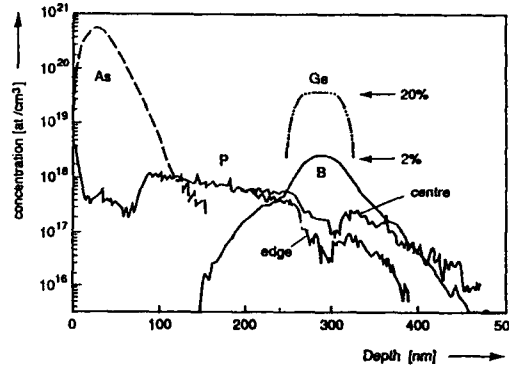


Figure 8 As, B and Ge SIMS profiles for the processed HBT. The P profile is also shown, both on the center and on the edge of the wafer

removed even for $V_{CB} = 2$ V. As a consequence the collector current is reduced, which results in a lower current gain. Since no parasitic barriers are formed in the all-Si transistors, they do not show these large variations in current gain over the wafer, and as a function of V_{CB} .

If application of a collector-base voltage reduces or removes the barrier, one should also expect a change in the temperature dependence of the gain enhancement. The effects are shown in Fig. 10 for two transistors, one from the center, and one from the edge, for two different base collector voltages. In the case of the transistor from the center of the wafer, at $V_{CB} = 0$ V an activation energy of 98 meV is found, which is lower than the band gap narrowing expected for $\text{Si}_{0.8}\text{Ge}_{0.2}$. By removal of the barrier ($V_{CB} = 2$ V) the activation energy is found to be 153 meV, which is comparable to the value found by Prinz et al. [27] for $\text{Si}_{0.81}\text{Ge}_{0.19}$.

If barriers occur, the charge storage in the base increases. Together with the decrease in I_C this leads to a strongly reduced f_T . From the center to the edge a decrease in f_T from 12 to 1.4 GHz ($V_{CB} = 2$ V) and from 6 to 1.2 GHz ($V_{CB} = 0$ V) is found, in accordance with simulations.

CONCLUSIONS

It was shown that MBE-grown layers still have some drawbacks. Especially the particulate density and the defect density are still two orders of magnitude too high for large scale integration applications. Also the contamination with metals, especially Ta, is much higher than in standard epi-layers. However, by careful processing it

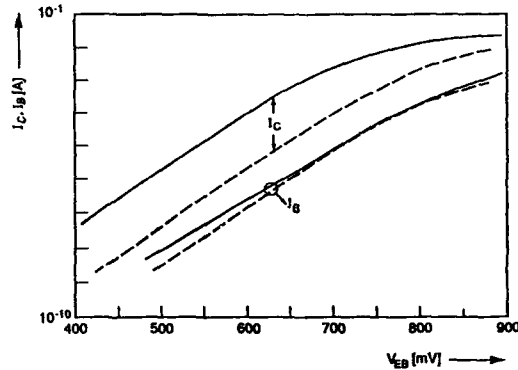


Figure 9 Gummel plot of an Si (dashed line) and an $\text{Si}_{0.8}\text{Ge}_{0.2}$ (solid line) transistor with an emitter area of $12 \times 62 \mu\text{m}^2$, on the center of the wafer.

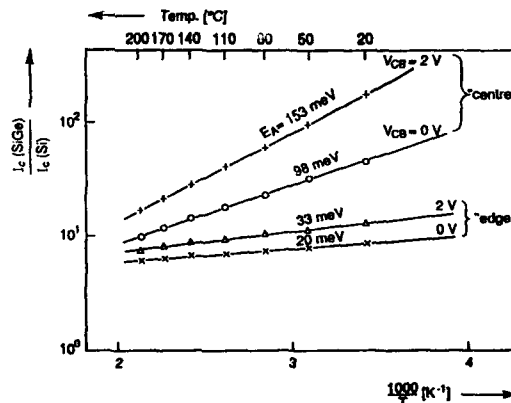


Figure 10 $I_C(\text{SiGe})/I_C(\text{Si})$ as a function of inverse temperature at 0 and 2 V, for an $\text{Si}_{0.8}\text{Ge}_{0.2}$ HBT and an otherwise identical Si base transistor, on the center and the edge of the wafer

appears to be possible to fabricate Si bipolar transistors with ideal Gummel plots, indicating that high quality material can be obtained, where apparently the metallic contamination does not play a role of importance. For the HBT's we found a current gain enhancement of up to 200 with respect to otherwise identical all-Si bipolar transistors. The current gain was close to ideal. Major problems that occurred were transient diffusion of B due to the emitter implantations, and a strong variation of the electrical properties over the wafer. These variations, which were only present in the HBT's originated from parasitic barriers that were formed due to the combination of the transient diffusion of the B and the angle-of-incidence dependence of the channeling of the P implantations.

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LOW TEMPERATURE IN-SITU PROCESSING FOR Si-MBE

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ABSTRACT

A basic process sequence for low temperature in-situ processing of metal-insulator-semiconductor (MIS) structures in an ultra-high vacuum (UHV) multichamber system is presented. It includes conditioning of the process chamber by plasma heating, in-situ cleaning of silicon wafers, and conventional silicon molecular beam epitaxy (Si-MBE). The in-situ cleaning is achieved by an argon/hydrogen plasma treatment of the wafer surface at temperatures well below 400° C. The native oxide as well as carbon compounds are removed from the silicon surface. Etch rates for SiO₂ are determined for various plasma parameters. Without additional cleaning procedures, silicon films are deposited in another process step using a quadrupole mass spectrometer controlled electron beam evaporator. Epitaxial films are obtained for substrate temperatures as low as 500°C on (100) and 600°C on (111) silicon for deposition rates of 0.05 nm/s.

INTRODUCTION

Important trends in the manufacturing of semiconductor and optoelectronic devices are moving towards in-situ processing, better vacuum, lowering the wafer temperature during deposition, and reducing the energy of particles bombarding the substrate in a plasma.

The process steps described below were developed for the Balzers modular UHV multichamber concept which is designed for advanced research and pilot production [1]. The low temperature in-situ substrate cleaning recently investigated for rf [2,3] and ECR [4] plasmas will play a key role in future processing. In this work an argon/hydrogen gas discharge is used for this procedure. It avoids damage to the substrate surface by using low energy particles. The growth of epitaxial layers by conventional Si-MBE proves the effectiveness of the substrate cleaning method. In combination with the recently developed plasma enhanced evaporation (PRE) process for silicon based dielectrics [5], in-situ processing for MIS structures in UHV and at moderate ($\leq 500^\circ\text{C}$) substrate temperatures seems possible.

EXPERIMENTAL DETAILS

Setup and process description

The Balzers UHV system used in the development of the process sequence is shown in Fig.1. It consists of a load-lock chamber (1), a preparation chamber (ULS 400) for the plasma treatment (2), and the growth chamber (UMS 630) for Si-MBE (3).

For processing, the silicon wafer as obtained from the manufacturer (i.e. without any additional cleaning) is placed in the load-lock from where it is transferred to the preparation chamber.

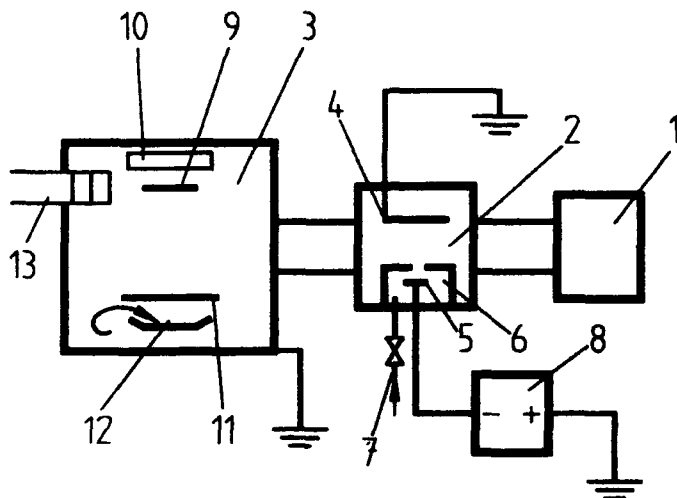


Fig.1 UHV multichamber system used for the process development (see text for description).

The preparation chamber contains a grounded substrate holder (4) and the plasma source, which is used for conditioning the chamber and for the in-situ cleaning of the wafer. This source consists of a heated filament (5) placed in a separated cavity (6). An orifice opens the cavity to the chamber. A working gas, usually argon, is fed into the cavity (7). If a potential is applied between filament and ground, a gas discharge is established. For potentials of typically 30 V, electron currents between 10 A and 100 A can easily be obtained with the power supply (8) used. The low energy electrons have high ionization cross sections for the argon as well as for admixed gases and therefore create an intense plasma in the chamber. This plasma is utilized for the conditioning of the chamber and for the in-situ wafer cleaning.

Subsequently the wafer is transferred to the substrate holder (9) in front of the heater (10) in the growth chamber and heated to the desired temperature. While the substrate temperature is stabilizing, the silicon is melted and the deposition rate is chosen. A shutter (11) protects the substrate from predeposition. For Si-MBE, a novel type of electron beam evaporator (Balzers ESQ 407U) (12) with a crucible capacity of 130 cm³ is used [6]. The deposition rates are controlled by a quadrupole mass spectrometer (13) which is mounted 585 mm above the crucible near the substrate holder. The rate control procedure is described elsewhere [7]. The substrate is rotated during deposition.

Both chambers are evacuated by a combination of turbomolecular pump and LN₂ cooled Ti-sublimation pump. The base pressure in the preparation chamber after conditioning and before

the in-situ cleaning is in the range between $5 \cdot 10^{-8}$ mbar to $2 \cdot 10^{-7}$ mbar. The high base pressure is due to the plasma source. Only a high vacuum version was available at the time the reported experiments were made. The base pressure in the growth chamber is routinely lower than 10^{-10} mbar.

Thermally oxidized silicon with a thickness of about 100 nm and diamond-like coated silicon are used as substrates for the determination of the SiO_2 etch rates and the deposition rates, respectively. Si-MBE is performed on (100) and (111) silicon wafers.

Analytical methods

Rutherford backscattering spectroscopy (RBS) [8] is performed to determine the etch rates for the SiO_2 and the silicon deposition rates. He^+ particles with 2 MeV incident energy and scattering angles of 160° are used (laboratory frame). A scattering angle of 170° for the channeling experiments is chosen. The random spectrum is obtained from the target which is 3° off relative to the aligned one.

RESULTS AND DISCUSSION

The heating of the inner chamber walls is investigated for discharge currents between 20 A and 80 A. In all the experiments an argon flow of 16 sccm is fed into the cavity of the plasma source resulting in a total pressure of $5 \cdot 10^{-3}$ mbar in the chamber. The discharge voltages are virtually independent for all the runs under these conditions. They range between 25 V and 30 V. The chamber functions as the anode for the high electron discharge currents which heat it. In Fig.2 the chamber temperature measured by a thermocouple in the chamber wall is plotted as a function of the plasma treatment. The temperature rise increases with the discharge current. The conditioning process is stopped when the temperature reaches 200°C because of the Viton seals in the high vacuum version of the plasma source. An advantage of this conditioning procedure is that sputtering of the chamber walls is avoided. The electron stimulated desorption of adsorbates from the chamber walls will be studied in more detail in the future.

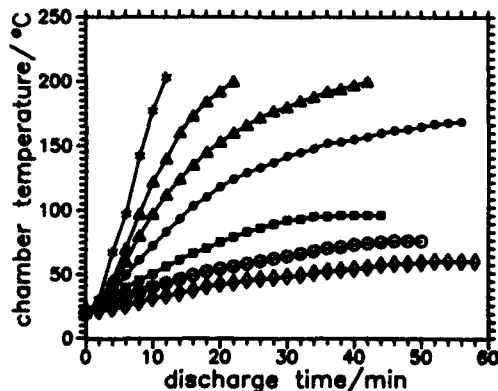


Fig.2 Chamber temperature as a function of the duration of the plasma treatment for different discharge currents: (◇) 20 A, (○) 30 A, (■) 40 A, (●) 50 A, (▲) 60 A, (△) 70 A, (*) 80 A.

For in-situ cleaning hydrogen is added to the argon. An argon flow of 12 sccm and a hydrogen flow of 14 sccm are chosen. Both gases are fed directly into the cavity and the argon/hydrogen plasma is established. Again the chamber acts as the anode for the discharge and is bombarded mainly by low energy electrons. Subsequently the wafer is placed in the grounded substrate holder which is immersed in the plasma.

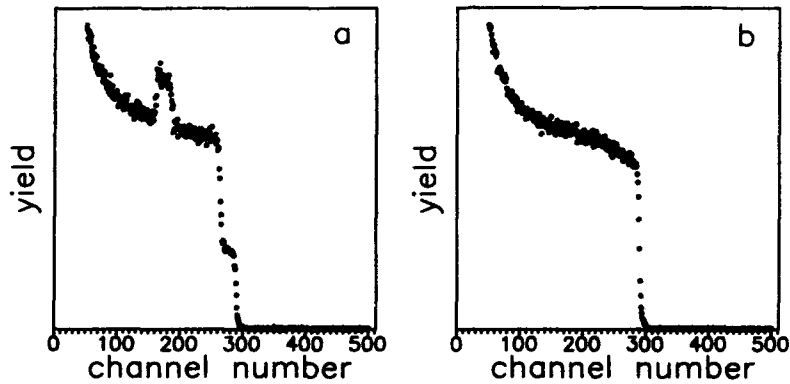


Fig.3 RBS spectra illustrate the etching effect of the argon/hydrogen plasma for thermally grown SiO_2 before (a) and after (b) plasma treatment.

In Fig.3a the RBS spectrum for an approximately 100 nm thick thermally grown SiO_2 film on silicon is shown. The plasma treatment removes the oxide from the wafer surface (Fig.3b). For the given argon/hydrogen mixture and discharge currents between 30 A and 50 A (discharge voltages about 30 V) the etch rates for thermally grown SiO_2 are determined. For that, films of the same thickness are etched back in the plasma and the remaining thickness is measured with RBS (counts of the oxygen signals). The results are given in Fig.4.

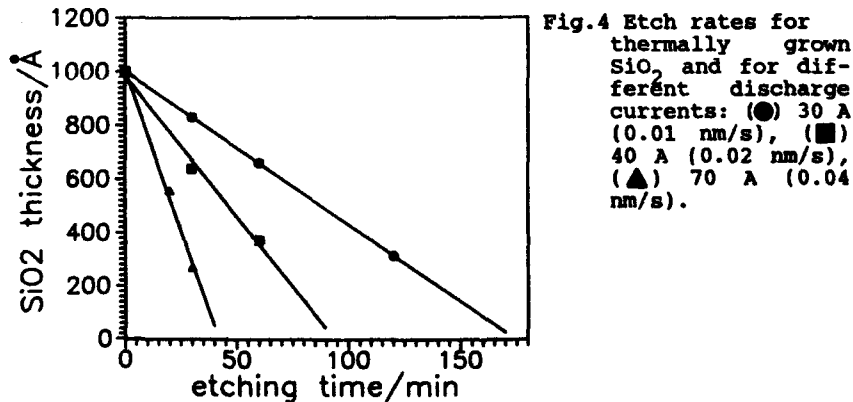


Fig.4 Etch rates for thermally grown SiO_2 and for different discharge currents: (●) 30 A (0.01 nm/s), (■) 40 A (0.02 nm/s), (▲) 70 A (0.04 nm/s).

The etch rates are increased with the discharge currents which in turn increase the substrate temperature. The temperature is measured by a thermocouple attached to the wafer backside. In the plasma discussed here, the etch rates of 0.01 nm/s to 0.04 nm/s are fairly low. However, they allow an accurate thickness control and are high enough to remove the native surface oxide in a few minutes by maintaining low substrate temperatures, for example 320°C for a discharge current of 30 A. The procedure has a broad process window and different gas mixtures with hydrogen will be studied in future experiments.

There is another advantage of this in-situ cleaning procedure. It also removes carbon and hydrocarbons from the substrate surface. Some preliminary results for diamond-like carbon yield etch rates 5 to 10 times higher compared with SiO₂.

Because there are no diagnostics in the chamber to test the wafer surface, silicon is deposited and the crystallinity of the films is investigated by RBS channeling afterwards. For that, the cleaned silicon wafer is transferred to the growth chamber and heated to the desired temperature. For (100) silicon the range between 400°C and 700°C and for (111) silicon the range between 600°C and 700°C is investigated. At no time are the wafers subjected to a temperature higher than substrate temperature. The deposition rates are calibrated via the quadrupole signals for ambient substrate temperatures with RBS. Silicon coated with 1 μm layer of diamond-like carbon serves as the substrate. This substrate has the advantage that the silicon signal is well separated from the backing in the RBS spectrum and allows a higher accuracy of the thickness measurement. Deposition rates of 0.05 nm/s are chosen for Si-MBE and layers of a total thickness of 135 nm are deposited.

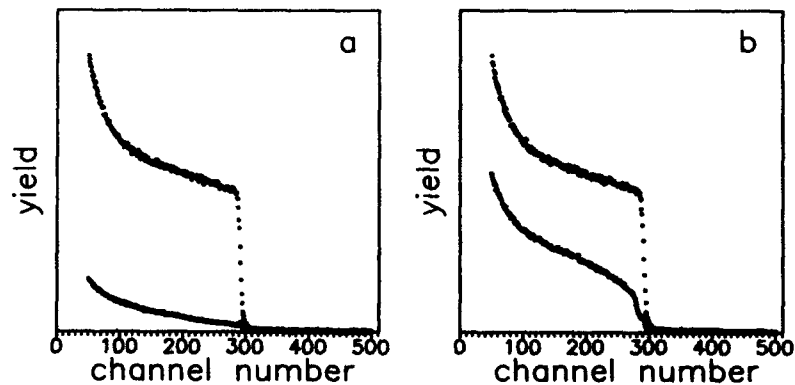


Fig.5 Comparison of the channeling results for silicon homoepitaxy at 500°C (a) and 400°C (b) on (100) silicon.

In Fig.5 the results of the channeling experiments for 500°C and 400°C on (100) silicon are compared. Whereas for 500°C (Fig.5a) no difference in the channeled yields compared with the bare wafer could be observed (about 3% minimum yield),

there is only about 10% minimum yield for the 400°C (Fig.5b) deposition. This documents the fact that the 400°C layer is not amorphous but might have misorientation with respect to the substrate or a thin amorphous layer in the interface. Perhaps some hydrogen-passivated silicon bonds are present at substrate temperatures of 400°C. However, for 500°C to 700°C epitaxy is obtained on (100) silicon and for 600°C to 700°C on (111) silicon. This proves that the low temperature in-situ cleaning is an effective procedure which might replace wet-chemical cleaning of silicon substrates.

CONCLUSIONS

The sequence of process steps presented fits into the concept of in-situ low-temperature UHV processing for MIS structures. For the chamber conditioning and for the substrate cleaning procedure, a plasma source was developed that works at low voltages (≤ 30 V) and high electron currents (up to 100 A). A single treatment of the silicon substrate with argon/hydrogen plasma at temperatures below 400°C prepares the wafer surface for epitaxy. Epitaxial films are obtained at 500°C on (100) silicon and at 600°C for (111) silicon by a quadrupole controlled electron beam evaporation process.

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LOW TEMPERATURE HYDROGEN PLASMA CLEANING PROCESSES OF Si(100), Ge(100), AND $\text{Si}_x\text{Ge}_{1-x}(100)$

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ABSTRACT

Wet chemical and *in situ* hydrogen plasma cleaning processes were studied and a low temperature cleaning process was developed for Si(100), Ge(100) and $\text{Si}_x\text{Ge}_{1-x}(100)$ surfaces. A uv-ozone and HF based spin etch were used to initially remove contaminants and oxides from the Si(100) and $\text{Si}_x\text{Ge}_{1-x}(100)$ surfaces. The Ge(100) surfaces were treated with deionized water prior to entry to UHV. Residual gas analysis (RGA) was used in the investigation of the surface removal process of the *in situ* H-plasma cleaning. Low Energy Electron Diffraction (LEED) and angle resolved UV-Photoemission Spectroscopy (ARUPS) were used to examine the surface structure and electronic states. The 2x1 LEED patterns were obtained for Si(100), Ge(100) and $\text{Si}_x\text{Ge}_{1-x}(100)$ after cleaning at a maximum processing temperature of 300°C. By varying process conditions, the LEED showed the 1x1 and 2x1 surface diffraction patterns. The ARUPS spectra showed the electronic states and the chemistry of the cleaned surfaces.

INTRODUCTION

Advanced electronic and photoelectric devices may employ silicon, Germanium, and $\text{Si}_x\text{Ge}_{1-x}$ alloy heterostructures. As a result there is a need for *in situ*, low temperature processing. H-plasma cleaning of semiconductor surfaces has been identified as a possible cleaning technique which can be employed at low temperature and low pressure [1-5]. H-plasma cleaning has been used for *in situ* surface preparation prior to and following CVD growth [2]. This study considers H-plasma cleaning of MBE deposited layers.

MBE is a widely used technique for depositing $\text{Si}_x\text{Ge}_{1-x}$ layers. The precursor to MBE deposition is a wet chemical pre-treatment to remove surface hydrocarbons followed by a high temperature UHV anneal which leaves the surface atomically clean and undamaged. The high temperature anneal results in the substrate surface having dangling bonds which is directly related to high chemical activity. Since CO and H₂O species often are present even in UHV, and these species tend to adsorb to the wafer surface to fill the dangling bond states, the high temperature UHV anneal may not suffice for all applications.

An alternative method to *in situ* cleaning of substrates is to use atomic H generated by plasma excitation. The technique has been demonstrated for the cleaning of Ge surfaces before Si epitaxy, and for the cleaning of Si surfaces prior to plasma CVD of Si [1,2]. The plasma exposure removes the residual oxide and hydrocarbon contaminants that remain after the wet chemical pre-clean [2]. Also, the H terminates the surface which results in a low chemical activity due to passivated dangling bond states.

This report establishes a basis for low thermal budget H-plasma cleaning of Si(100) surfaces [1,5] and extends the research to include Ge(100) and MBE-grown $\text{Si}_x\text{Ge}_{1-x}(100)$ surfaces. Due to the similarities of the materials it was expected that

Ge(100) and $\text{Si}_x\text{Ge}_{1-x}$ (100) surfaces would exhibit similar properties following the exposure to atomic H.

EXPERIMENTAL

The research for this study was carried out in the rf plasma system shown in Fig. 1. Atomic H is generated by an inductively coupled rf coil, and the plasma was excited in the quartz tube. The system base pressure was achieved with a cryopump, and the process pressure was controlled by a throttle valve with turbo-molecular pumping. The plasma cleaning system was interlocked with a surface analysis system with LEED, Auger electron spectroscopy (AES), and angle-resolved ultraviolet photoemission spectroscopy (ARUPS). The cleaning and analysis chambers, and transfer system were UHV compatible. The base pressure in the analysis chamber and the transfer line was $<6.5 \times 10^{-10}$ Torr, and the base pressure of the cleaning system was 1.0×10^{-9} Torr. Since the pressure recovery time of the plasma system was <2.0 min., this configuration allowed for prompt surface analysis following H-plasma processing.

The Si(100) and Ge(100) substrates used in this study were commercially obtained. The $\text{Si}_x\text{Ge}_{1-x}$ (100) layers were grown by MBE. The wafer specifications were as follows:

Si(100):	25 mm dia. phosphorous doped, n-type, a resistivity of 8-1.2 ohm-cm and a thickness of 12-20 mils.
Ge(100):	25 mm dia. antimony doped, n-type, a resistivity of 0.3-3.0 ohm-cm and a thickness of 12-20 mils.
$\text{Si}_x\text{Ge}_{1-x}$ (100):	80% Si + 20% Ge MBE layers of thickness 400 Å grown by MBE on Si(100) substrates.

The MBE alloys were prepared by co-deposition onto Si(100) substrates.

Before loading the samples into UHV, an *ex situ* preparation was carried out. The Si(100) was first exposed to an uv-ozone ambient to remove the surface hydrocarbons and produce a carbon free oxide. Then the Si(100) wafer was spin etched with a dilute HF based solution (HF:H₂O:ethanol(1:1:10)) [6]. The Ge(100) samples received no *ex situ* treatment, i.e. these samples were H-plasma cleaned right out of the box. The MBE grown Si_xGe_2 (100) surfaces received the same *ex situ* treatment as the Si(100) samples.

The H-plasma process parameters were the same for all three types of wafers. The parameters were Press.: 14.0 mTorr, Temp.: 150°C and 300°C, Flow: 10.0 sccm H₂, and rf-Power: 20 W. The wafer temperature prior to, during, and following the H-plasma clean was important. First the temperature was ramped at 50°C/min. to 150°C and kept there for 3.0 minutes. Then the temperature either was held the same or was ramped at 50°C/min. to 300°C. In either case, the sample was maintained at the final

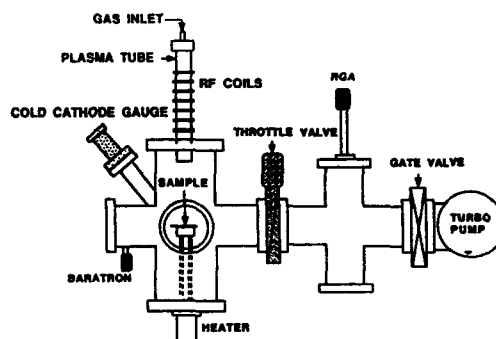


Fig. 1 H-plasma cleaning system.

temperature for 3.0 minutes. During the first 1.0 minute of the final temperature the plasma was activated and the following 2.0 minutes were required to prevent the wafers from cooling in a H_2/H ambient while the chamber was recovering from processing pressure. These processing conditions produced clean sample surfaces and depending on temperature, induced different surface reconstructions with different surface H concentrations [1].

The characterization of the plasma was accomplished by using residual gas analysis (RGA). With the RGA positioned between the throttle valve and turbo pump, RGA spectra were obtained both before and during processing. Using the RGA, evidence of surface etching was detected.

To determine the status of the surfaces following the H clean, the surface analysis systems were employed. The rear-view LEED operating at electron energies of ~ 60 eV for Si(100), ~ 41 eV for Ge(100), and ~ 57 eV for $Si_3Ge_2(100)$ was used to determine the surface reconstruction. The ARUPS measurements were excited with 21.2 eV uv-radiation from a He I discharge lamp. The photoemitted electrons were analyzed with a 50 mm radius hemispherical electron analyzer mounted on a two angle goniometer. The ARUPS spectra were obtained with an energy resolution of 0.15 eV and an angular resolution of 2° .

RESULTS AND DISCUSSION

The two components to this study were the plasma and the surface characterization of H-plasma cleaning of the Si(100), Ge(100) and $Si_3Ge_2(100)$ surfaces. In terms of the plasma characterization, the species present during the surface cleaning were determined by RGA. The RGA spectra in the 0-50 atomic mass unit (amu) range of Fig. 2a represents the status of the plasma reactor prior to discharge, *i.e.* the base pressure spectra. The peaks at 17 and 18 amu were due to H_2O fragmentation, and the peaks at 28 and 44 amu were CO and CO_2 species respectively [5,7]. Fig. 2b shows a portion of the RGA spectra of the system with the plasma excited and a wafer present. The additional peaks at 29, 30,

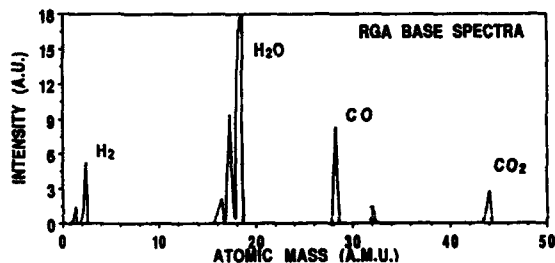


Fig. 2a RGA Spectra before plasma excitation

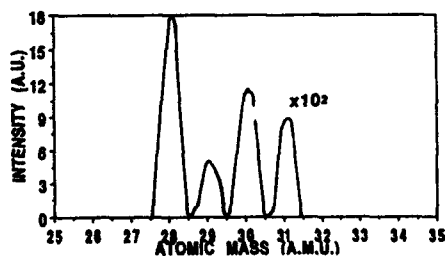


Fig. 2b RGA Spectra during Si(100) H-plasma cleaning. Peaks at 29, 30, and 31 attributed to Si-H fragmentation.

and 31 amu corresponded to silane fragmentation [1,5,7]. This is an indication of the H interacting with the Si(100) surface. The other portion of the RGA spectra showed an increase in the 15 and 16 amu peaks. These peaks were likely due to CH₃ and CH₄, respectively [7]. The origin of the C-H species may have been due to the H-plasma interacting with the chamber walls.

The RGA spectra of the Ge(100) surface cleaning showed no germane fragmentation around 72, 73, 74, 75, and 76 amu. Aside from the SiH₄ fragmentation of Fig. 2b, the Ge(100) surface cleaning had the same RGA spectra. This implies that the chemistry of the Ge(100) surface interacting with the atomic H is very different from that in the case of Si(100) in that Ge didn't show signs of etching. The RGA spectra of Si_{0.8}Ge_{0.2}(100) was essentially the same as that of Ge(100). It was expected that the silane fragmentation would be nearly the same as the Si(100) case. This data suggests that the Si_{0.8}Ge_{0.2}(100) surface is less reactive than the Si(100) surface possibly due to the presence of Ge.

The second component to this study was the surface characterization. Figs. 3a and 3b show the 1x1 LEED patterns of the Si(100) and Si_{0.8}Ge_{0.2}(100) surfaces prior to the H-plasma cleaning. The Ge(100) surface showed no LEED pattern following the *ex situ* preparation. Following the plasma exposure at a substrate temperature of 300°C, Figs. 3c-3e show the 2x1 LEED patterns of the Si(100), Ge(100) and Si_{0.8}Ge_{0.2}(100) surfaces. Since the surfaces each showed a 2x1 reconstruction, it suggests that the surfaces were well ordered following the H-plasma exposure. The diffraction also showed streaks between the half order spots in the LEED of Si(100) (Fig. 3c) which may be caused by disordered dimer rows [8]. The half order spots were diffuse following the H clean. This

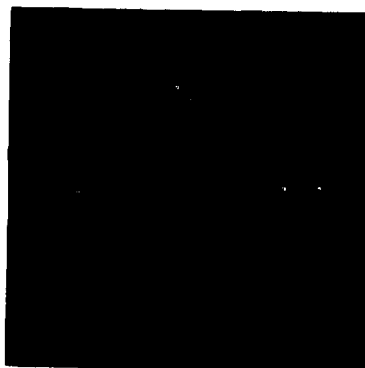


Fig. 3a. Si(100) LEED before plasma

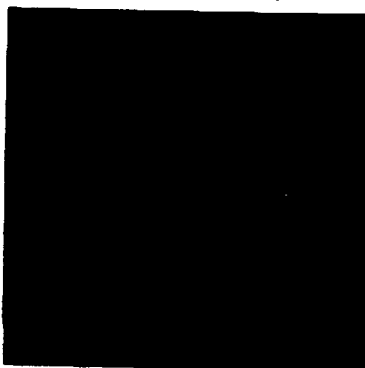


Fig. 3b. Si_{0.8}Ge_{0.2}(100) LEED before plasma

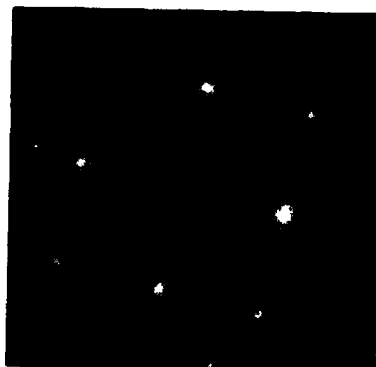


Fig. 3c. Si(100) LEED after plasma

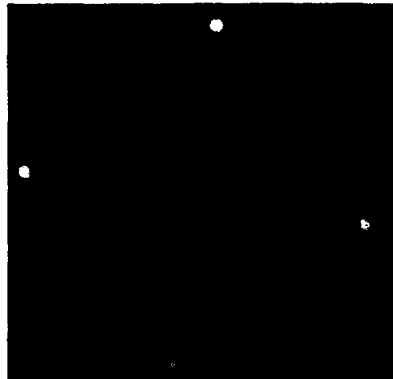


Fig. 3d. Ge(100) LEED after plasma

indicates small domains on the Si(100) surface [8]. The Ge(100) diffraction patterns (Fig. 3d) did not show streaking. The Si₃Ge₂(100) diffraction pattern of Fig. 3e showed diffuse half order spots which again implied small domains.

The surface characterization also included the ARUPS spectra before and after H-plasma cleaning. Fig. 4a shows spectra both after the *ex situ* clean (lower spectra) and after the *in situ* H clean (upper spectra) at an emission angle of 40°. The upper spectra shows the Si(100):H 2x1 states of the monohydride phase, at energies of -5.4 eV and -6.2 eV, following the H-plasma cleaning. A weak oxide feature can be observed at ~ -8 eV. This peak could be due to contamination in the plasma system or it may have remained on the samples following the *ex situ* chemical clean. The ARUPS spectra of Ge(100) is shown in Fig. 4b at an emission angle of 20°. No features due to H bonding were identified. This suggests that the hydrogen desorbed from the Ge(100) surface at temperatures below 300°C. The peak observed ~ -8 eV is due to Ge-O bonding [9] which indicates a small amount of residual oxygen contamination.

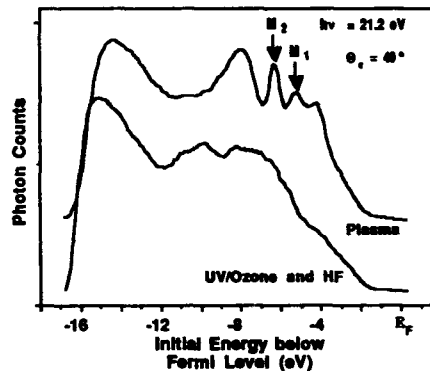
Fig. 3e. Si₃Ge₂(100) LEED after plasma

Fig. 4a ARUPS spectra of Si(100) before and after H-plasma cleaning.

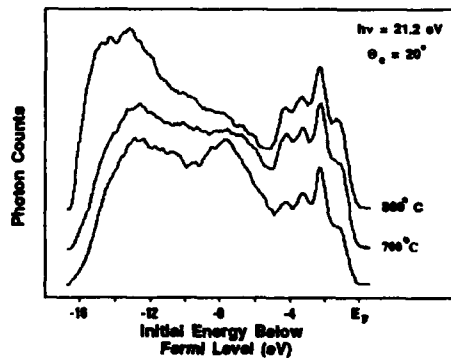


Fig. 4b ARUPS spectra of Ge(100) after H-plasma cleaning.

The peak at ~ -0.9 and -2.3 eV is a Ge(100) surface state [9]. The Ge sample was annealed to 1000°C and the surface state was still observed in the ARUPS spectra. This suggests that the Ge(100) surface was completely dimerized following the H-plasma clean.

CONCLUSION

The extension of the Si(100) *in situ* surface preparation to Ge(100) and Si_3Ge_2 (100) surfaces has demonstrated consistent results relative to the Si(100) work. This study emphasizes the capability of H-plasma cleaning as a precursor to next step processing in the future applications of Si, Ge, and Si_3Ge_2 alloy heterostructures. The evidence of the capability of H-plasma cleaning is realized in the low temperature aspect which is complimented by the well ordered surfaces as implied by the LEED patterns. The Si(100) surfaces were H terminated following the H-plasma exposure. The RGA spectra reported here show the indication of the surface removal process.

ACKNOWLEDGEMENTS

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HIGH DEFINITION MESA GROWTH BY SILICON MBE

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ABSTRACT

A novel epitaxial growth method for fabricating mesa patterns on a micrometer scale has been investigated. Electrical devices have been prepared employing this technique and their characteristics are in good agreement with those of mesa etched devices.

INTRODUCTION

Molecular beam epitaxy of silicon is capable of growing uniform layers on large area substrates with high crystalline quality and, in particular, with arbitrary doping profiles. While such epitaxial layers can be used as an early step in device fabrication, all subsequent processing is restricted to low temperatures to avoid diffusion which could deteriorate the device characteristics. Therefore the versatility of Si MBE is greatly enhanced if it can be introduced at any step of the device fabrication sequence. This is possible if the layers are patterned after deposition or if the lateral structures are defined by the epitaxy process itself. Especially for three dimensional integration of complex device structures an exact thickness control of layers to be overgrown by MBE is necessary. In contrast to the MBE process, etching does not allow a reproducible control of the layer thicknesses on an atomic scale. Thus, growing mesa patterns by MBE is preferable. Epitaxial mesa islands can be fabricated using so-called differential epitaxy [1]. In this growth mode single crystalline silicon is deposited in oxide windows determined by conventional photolithography, whereas poly-silicon forms on the oxide layer. A lift-off process removes both the masking oxide and its poly-silicon overlayer leaving single-crystalline mesa patterns on the substrate. However, the mesa sidewalls may show structural imperfections depending on the interface between the oxide and the single crystalline layer [2]. This may prohibit the overgrowth of differentially grown mesa islands and thus the integration into complex three dimensional device structures.

Therefore, we investigate a novel method for the mesa growth of epitaxial silicon layers using patterned shadow masks on the substrate. Because the mesa sidewalls are not in contact with any surrounding material during epitaxial deposition, they are determined solely by the MBE growth parameters. It will be demonstrated that epitaxial mesa islands of high crystalline quality with smooth, vertical sidewalls can be grown by this method.

EXPERIMENTAL RESULTS AND DISCUSSION

The schematic drawings shown in Fig. 1 point out the fabrication process of micro shadow masks and the subsequent steps for the production of epitaxial silicon patterns. Si (100) substrates are cleaned in a standard procedure [3] and thermally oxidized at $T=1050^{\circ}\text{C}$ up to $1\ \mu\text{m}$ oxide thickness. In a LPCVD process a $100\ \text{nm}$ thick silicon nitride (Si_3N_4) layer is deposited at $T=700^{\circ}\text{C}$ onto the oxide layer. The oxide layer acts as a spacer between the substrate and the thin silicon nitride which is deposited onto the oxide. (Fig. 1a). Conventional photolithography in combination with CF_4 -plasma etching is used in order to pattern the nitride film (Fig. 1b). After the etching process the photoresist mask is carefully removed in hot organic remover and in a subsequent oxygen plasma strip. Until now the silicon substrate was protected from plasma damage by the oxide spacer. This oxide spacer is then etched within the growth window in buffered hydrofluoric acid and, by underetching the nitride layer, forms a shadow mask for the subsequent MBE-deposition (Fig. 1c). The patterned substrates are then transferred

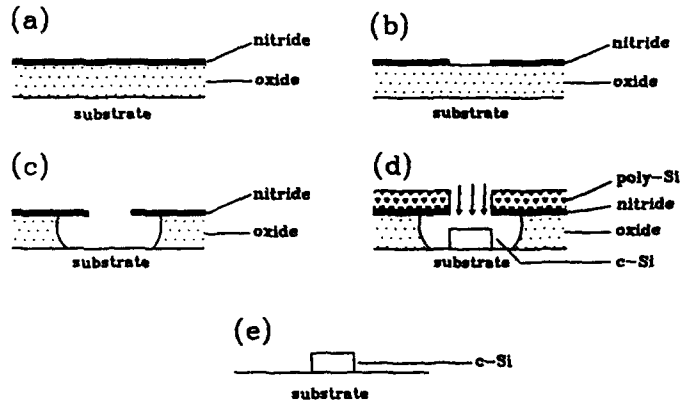


Fig. 1: Fabrication process of micro shadow masks.
 (a) deposition of the masking material, (b) patterning of the masking layer,
 (c) etching of the oxide spacer, (d) MBE growth, (e) lift-off

immediately into the MBE system. Epitaxial growth occurs within the windows, whereas poly-silicon is formed upon the nitride (Fig. 1d).

The MBE process starts with a thermal heat treatment of the substrates ($T=900^{\circ}\text{C}$, 5 minutes) to remove the native oxide in the growth windows. The deposition temperature is varied between 600°C and 700°C . During growth the total pressure ($p=3\cdot 10^{-9}$ mbar) as well as the mass analyzed partial pressure of the residual gas components is identical to that with a bare substrate. Thus, outgassing of the masking material and therefore additional substrate contamination can be excluded. Fig. 2a shows a scanning electron micrograph (SEM) of a cleaved sample after MBE growth at $T_{\text{epi}}=600^{\circ}\text{C}$. The mesa island with a thickness of $0.5\ \mu\text{m}$ appears as a perfect geometric image of the shadow mask patterns with straight, vertical mesa walls and smooth surfaces. Also, the poly-silicon on top of the nitride layer reveals a smooth surface without visible roughness, resulting in a sharp vertical poly-silicon wall at the end of the nitride cantilever. This enables the growth of mesa islands with vertical sidewalls. Remarkable is the mechanical stability of the thin nitride cantilever in spite of the wide underetching of about $5\ \mu\text{m}$ and the much thicker poly-silicon on top of it. Note that the cantilever is not cleaved exactly parallel to the substrate, so that the cantilever appears bended upwards and its end not lining up with the mesa wall underneath.

In Fig. 2b a SEM micrograph shows a magnified cross-section of the mesa island depicted in Fig. 2a. The edges of the mesa island are well defined and straight and the mesa wall is exactly perpendicular to the substrate surface.



Fig. 2: Scanning electron micrographs of epitaxial mesa grown islands.

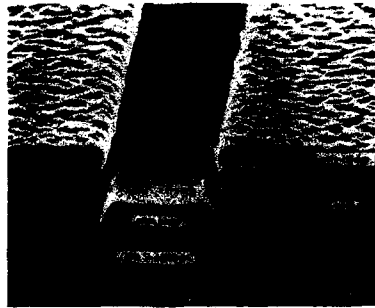


Fig. 3: SEM micrograph showing the dependence of edge slope upon poly-silicon growth.

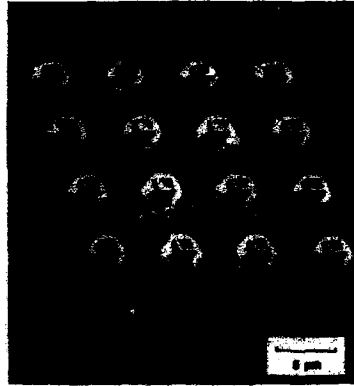


Fig. 4: SEM micrograph of $2 \times 2 \mu\text{m}^2$ mesa islands after the lift-off process.

The substrate temperature during the MBE process has a strong influence on the local growth of mesa islands. In Fig. 3 the cross-sectional view of a $2 \mu\text{m}$ wide mesa stripe locally grown at $T_{\text{sub}}=700^\circ\text{C}$ exhibits marked differences to the mesa grown at $T_{\text{sub}}=600^\circ\text{C}$. In contrast to Fig. 2a the sidewalls of the mesa bar are no longer vertical but inclined at an angle of about 20° to the substrate normal and no longer appear smooth and plane but wavy. The poly-silicon on top of the nitride layer shows a granular surface with a roughness of about 100 nm and does not form a vertical and sharp edge at the end of the nitride cantilever. An explanation of the temperature dependent slope of the mesa wall is based on the temperature sensitive growth of poly-silicon on top of the nitride layer. Because of its granular growth, the poly-silicon at the edge of the nitride cantilever continuously spreads out in the lateral direction with increasing layer thickness thereby reducing the size of the growth window. As a result of the changing geometry of the shadow mask, the slope of the locally grown mesa wall is mainly determined by and nearly identical to the slope of the poly-silicon layer at the edge of the nitride shadow mask. Herzog et. al [4] have shown experimentally that at $T_{\text{sub}}=750^\circ\text{C}$ the average size of the poly-silicon grains on top of a silicon oxide layer grows almost linearly with increasing poly-silicon layer thickness which explains the approximately linear slope of the mesa walls in our case. The notches at the rim of the mesa in Fig. 3 are due to shadowing effect during the growth by overhanging grains. The small bending in the middle of the sidewalls as well as the raised edges of the mesa bar may indicate the onset of facet growth at higher temperature. Herzog et al. also investigated the grain size dependence on epitaxial temperature and found it much smaller at lower growth temperatures ($T_{\text{sub}} = 550^\circ\text{C}$) and almost independent of the layer thickness. This is again in agreement with our results (Fig. 2, $T_{\text{sub}} = 600^\circ\text{C}$) and proves that at low substrate temperatures the geometrical size of the shadow masks remains constant during the MBE growth independent of the layer thickness. Therefore, by choosing proper MBE parameters the slope of the sidewalls of locally grown mesa islands can be varied and the walls may even be grown vertically.

In order to remove the masking material surrounding the mesa, the samples have been treated in an ultrasonic bath of hydrofluoric acid. By dissolving the SiO_2 spacer the nitride layer with poly-silicon on top of it has been completely lifted off. High resolution patterned mesa islands of single crystalline silicon remain on the substrate (Fig. 1e). A top view SEM micrograph of an array of mesa islands grown at $T_{\text{sub}}=700^\circ\text{C}$ is shown in Fig. 4 after the lift-off of the masking material. Well defined $2 \times 2 \mu\text{m}^2$ mesa squares of $0.9 \mu\text{m}$ thickness and spaced $5 \mu\text{m}$ to each other are depicted. The bright circular areas

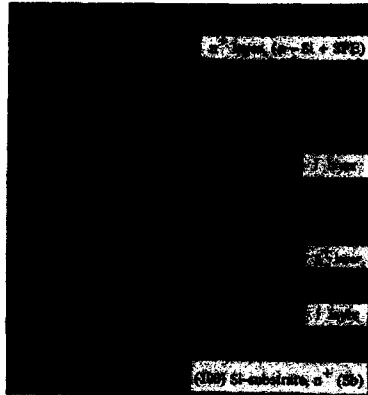


Fig. 5:

TEM micrograph of a locally grown triangular barrier diode.

around the mesa islands are caused by thin residues of photoresist spun onto the mesa before the lift-off process. It is not completely removed in order to emphasize the range of underetched masking cantilevers of about $2 \mu\text{m}$. Mesa arrays of the same size as in Fig. 4 have been grown with underetching of the nitride layer larger than the distance between two neighbouring mesa squares, i. e. the oxide spacer is completely removed within the array. In this case the very stable shadow mask of nitride was supported only by the oxide spacer at the boundary of the array. So very narrowly spaced structures of micrometer (and in principle even smaller) lateral dimensions can be achieved.

In order to demonstrate the crystalline quality of the locally grown epilayers, transmission electron microscope (TEM) investigations at a thin cross-section have been performed. In Fig. 5 a cross-sectional bright field image of a locally grown triangular barrier diode reveals no structural defects in the active layers of the device. The interface between the substrate and the epilayer is not contaminated by any visible impurity residues and shows perfect epitaxial overgrowth. Small particles typically marking the substrate-epilayer interface in Si-MBE and identified as carbon contaminations [5] are not observed in the presented section of the sample. Such particles however are occasionally found in other areas of the TEM specimen.

The boron doped layer with $N_b = 5 \cdot 10^{18} \text{ cm}^{-3}$ and a thickness of about 10 nm, embedded between two intrinsic regions, is not visible in the TEM micrographs. The boron concentration and also the difference in the atomic number between boron and silicon are too small to produce any noticeable contrast. In the upper, highly antimony doped contact layer, deposited amorphously at $T_{\text{sub}} < 200^\circ \text{C}$ and recrystallized by solid-phase epitaxy, a band of small defects appears a few tens of nm above the interface of the upper intrinsic and the n^+ -contact layer. These defects consist mainly of antimony precipitates and possibly of small dislocation loops. Small antimony precipitates are also seen in the entire n^+ -contact layer. Their formation may be understood as a consequence of segregation and subsequent precipitation during solid-phase epitaxy as a result of the very high antimony concentration. They are not specific for the local growth mode but are induced by the used MBE process. Because of their localization within the contact layer, electrical device characteristics are not deteriorated. Thus, epitaxial layers locally grown with micro shadow masks are of high crystalline quality comparable to that of MBE layers on unpatterned substrates.

ELECTRICAL CHARACTERIZATION OF LOCALLY GROWN DIODES

Electrical measurements are performed to characterize quality and applicability of the mesa growth process to device fabrication. Bipolar (pin-diodes) as well as unipolar (triangular barrier diodes) devices are prepared for this purpose. Locally grown and mesa etched devices are fabricated for comparison.

A schematic drawing of the pin-diode structure is represented in an inset of Fig. 6. Highly boron doped Si (100) substrates ($\rho < 10 \text{ m}\Omega \cdot \text{cm}$) are used to provide ohmic

behaviour of the backside contact. For the etched and mesa grown pin-diode an intrinsic layer is grown directly onto the substrate with layer widths of 4600 Å and 4900 Å respectively. The intrinsic layer is overgrown by two antimony doped layers, each with a thickness of 1000 Å. High doping levels of $5 \cdot 10^{18} \text{ cm}^{-3}$ and $5 \cdot 10^{21} \text{ cm}^{-3}$ respectively can be obtained by amorphous deposition and recrystallization by solid phase epitaxy. [6]. For the passivation of the diode surfaces, wet thermal oxidation ($T=700^\circ \text{C}$, 4 h) and annealing in a hydrogen atmosphere ($T=430^\circ \text{C}$, 20 min.) is performed. Metallization is provided by sputtering 300 Å of Ti/W and 3000 Å of Pt forming ohmic contacts to the uppermost antimony doped layer without any alloying process. Measurements reveal contact resistances of about 4 to 5 Ω .

Applying a forward bias to a pin-diode causes the injection of electrons and holes into the intrinsic region. Fig. 6a shows the current-voltage-(I-V-) characteristics of an etched and locally grown pin-diode both at room temperature as well as at liquid nitrogen temperature ($T=77.3 \text{ K}$). In cooling from room temperature to $T=77.3 \text{ K}$ the forward bias current is shifted to higher voltages indicating an increase of the built-in voltage of the junction. Differences in the characteristics of the diodes are mainly due to the larger reverse saturation currents I_s of the mesa grown diodes. A semilogarithmic plot of the curves in Fig. 6a is shown in Fig. 6b. In the case of a short pin-diode, i. e. the width of the intrinsic layer is smaller than the effective diffusion length, the forward I-V-characteristics can be described on the basis of a simple diffusion approximation [7]:

$$I = I_s \cdot [e^{q \cdot V / (n \cdot k \cdot T)} - 1] .$$

For a perfect pin-diode an ideality factor of $n=1$ is expected. Fitting the data at room temperature to the above analytical expression results in ideality factors of $n \approx 1.08$ for the mesa grown diode compared to $n=1.04$ for the etched device. The reverse saturation currents of the diodes can be determined from an extrapolation of the logI-V-characteristic to zero bias and are determined as $I_s = 1 \cdot 10^{-14} \text{ A}$ for the etched and $I_s = 1 \cdot 10^{-12} \text{ A}$ for the mesa grown device. Although the reason for this difference is not yet known, the saturation currents as well as the specified ideality factors demonstrate the high quality of the etched and the mesa grown layers.

The reverse biased diode shows a voltage breakdown as can be seen in Fig. 6a. Higher breakdown voltages for the mesa grown devices are caused by the larger width of the intrinsic layers in comparison to the etched ones. The voltage range for the breakdown is in good agreement with the theory for an avalanche breakdown in pin-diodes with an intrinsic layer smaller than the depletion-layer width [8], which for our devices states a breakdown voltage of about 20 V. The temperature behaviour of the breakdown voltage strongly supports the avalanche breakdown model by showing a shift of the breakdown voltage to lower values when the samples are cooled down.

The reversed biased pin-diodes show the case of a nearly voltage independent capacitance-voltage characteristic (Fig. 6a), demonstrating a depletion layer width mainly determined by the width d_i of the intrinsic layer and the device area A

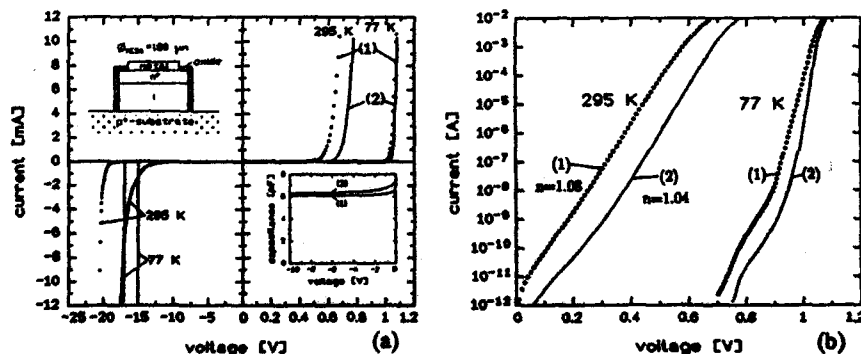


Fig. 6: Comparison of the electrical characteristics for the locally grown (1) and the etched (2) pin-diode.

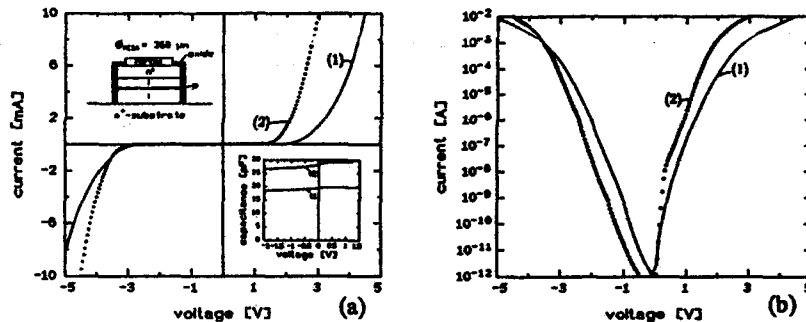


Fig. 7: Comparison of the electrical characteristics for the locally grown (1) and the etched (2) triangular barrier diode.

($C = \epsilon_0 \cdot \epsilon_{s1} \cdot A / d_1$). Calculations of the capacitances for the mesa grown and etched devices with regard to the device geometries yield $C = 5.5$ pF and $C = 5.8$ pF respectively. These values are in very good agreement with the measured ones (Fig. 6a). The junction capacitances are frequency independent in the range of 10 kHz to 10 MHz.

The second device under investigation in this work is a triangular barrier diode (TBD) that exhibits a current-voltage (I - V) characteristic dominated by thermionic emission of majority carriers over a barrier that is introduced by a doping layer into an intrinsic region. The schematic arrangement of the epitaxial layers necessary for the TBD is depicted in an inset to Fig. 7a. Except for the p-barrier, the fabrication process is quite similar to that of the pin-diodes. The effective barrier height Φ_b is determined by the thickness t and doping concentration N_a of the p-layer and the thickness of the adjacent intrinsic layers (d_1 and d_2) [9].

Fig. 7a and 7b show the I - V -characteristics in a linear and a semilogarithmic plot for two devices made by conventional etching and mesa grown MBE. Slightly different doping concentrations and thicknesses are responsible for the distinct behaviour of the devices. At higher current levels the characteristics reveal a discrepancy from the exponential form that can be attributed to shielding effects due to charge carriers reaching the saturation velocity. From the $\log I$ - V -plot one can determine the saturation currents I_s from the extrapolation to zero bias and from this the effective barrier height

$$\Phi_b = \frac{k \cdot T}{q} \cdot \ln \left[\frac{A \cdot A^* \cdot T^2}{I_s} \right].$$

The determined effective barrier heights are $\Phi_b \approx 0.9$ V (mesa grown device) and $\Phi_b \approx 0.95$ V (etched device). Forward and reverse biased TBDs do not show exactly the same barrier height. Calculated I - V -characteristics using the experimentally determined barrier heights and the device geometry show only qualitative agreement. One can also define an ideality factor similar to the case of the pin-diode. For an ideal TBD one expects ideality factors specified solely by the intrinsic layer widths [9]. The ideality factors found for both the etched and the mesa grown devices are too high. The very low saturation currents I_s suggest the high crystalline quality of the devices. It should be noted that in the present case the model for thermionic emission is only a crude approximation because for chosen geometry effect due to electron velocity saturation as well as tunneling effects through the p-type barrier have to be considered.

The capacitance-voltage characteristic is nearly constant for both the etched and mesa grown diodes as can be seen in the inset to Fig. 7a. For the TBD one can calculate the capacitance approximately using $C = \epsilon_0 \cdot \epsilon_{s1} \cdot A / (d_1 + t + d_2)$ which yields $C = 19$ pF (locally grown) and $C = 27$ pF (etched) for the represented devices which are in good agreement with the measurements.

CONCLUSION

Micro shadow masks have been fabricated on a micrometer scale. Utilization of these masks for local mesa growth was studied as a function of molecular beam epitaxial growth parameters. After lifting off the masking material and the poly-silicon grown on top of it single crystalline mesa islands remain on the substrate. Scanning and transmission electron micrographs were used to determine the crystalline quality of the grown mesa patterns. It was demonstrated that the crystalline quality of the mesa grown islands is comparable to that of conventional etched mesa structures. Electrical characterization of unipolar as well as bipolar devices confirms the high quality of the mesa islands fabricated by the novel growth technique.

ACKNOWLEDGEMENT:

We would like to thank Mrs. Teodora Fuska for the photographic work.

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INITIAL OXIDATION OF MBE-GROWN Si SURFACES

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We investigated the initial oxidation of MBE-grown Si(100) surfaces with atomic flatness using x-ray photoemission spectroscopy (XPS) and reflection high energy electron diffraction (RHEED). It was found that the MBE-grown surfaces are inert and hardly oxidized even after exposure to molecular oxygen up to 1500 Langmuir(L) at room temperature. At elevated temperatures, the surface oxidation was substantially promoted. On the contrary, the surface oxidation was found to be substantiated on a deliberately corrugated Si surface prepared by low temperature MBE growth, even at room temperature.

1 INTRODUCTION

Initial stages of oxidation of a clean Si surface are of great interest owing to both scientific interests and technological applications. For more than 20 years, room temperature (RT) adsorption of oxygen atoms on a Si surface and early stages of oxidation have been extensively investigated using electron energy loss spectroscopy [1-3] and photoemission spectroscopy [4-6]. These results have shown that the oxygen atoms, at first, rapidly adsorb molecularly or atomically on a Si surface up to 1 monolayer (ML). After this stage, the oxygen uptake tends to be saturated for further oxygen exposure. As to the first process, several models of possible bond geometries have been proposed which might be classified into either an atomic or a molecular adsorption scheme. Despite these efforts, a consistent understanding is still lacking. This is partly because the surface properties of the Si sur-

faces investigated were not well-defined. In practice, Si clean surfaces were prepared by thermal desorption of surface oxide layer or repeated ion-sputter-and-anneal. These surfaces have been revealed to be with defects or impurities which vary from one experiment to another depending on the way of the surface oxide removal. In addition, excess temperature treatment often leads to surface roughening. As Ibach et al. claimed, the sticking coefficient of oxygen atoms is severely influenced by the surface roughness [7]. It is, therefore, highly desirable to study the initial oxidation of "well-defined" Si surfaces. In this respect, a Si surface prepared by molecular beam epitaxy (MBE) stands as a promising candidate, since it is "atomically flat" with a well-defined geometry and is free of contaminants when a buffer layer with sufficient thickness is grown [8,9,10].

In this paper, we investigated the initial oxidation of MBE-grown Si(100) surfaces by

molecular oxygen (MO) exposure in a temperature range between RT and 400°C using in-situ x-ray photoemission spectroscopy (XPS) and reflection high energy electron diffraction (RHEED). It was found that the MBE-grown Si(100) surfaces are inert and hard to be oxidized at RT. On the contrary, the surface oxidation was found to proceed more rapidly on a deliberately corrugated Si(100) surface.

2 EXPERIMENTAL

Si surfaces were prepared in a Si MBE system (VG Semicon V80M). The base pressure of the growth chamber was lower than 4×10^{-11} Torr and a typical operating pressure was about 2×10^{-9} Torr. Silicon was evaporated with an electron beam gun and the growth rate was 0.1nm/sec. A p-type Si(100) wafer was pre-cleaned in a conventional method described previously [11]. A 100nm undoped Si buffer layer was grown at 700°C after removal of a thin protective oxide layer by heating at 850°C. A corrugated surface was formed by Si deposition at 300°C which is too low for a smooth epitaxial surface to grow [12]. Subsequently, the sample was transferred to the analysis chamber and was subjected to the MO exposure. The MO dose was changed from 1 to 1500L and controlled by monitoring the pressure with an ion gauge. During the exposure, the sample surface was not faced to the hot filament of the ion gauge so that the influence of excited oxygen atoms is negligible. The sample surfaces were characterized by XPS and RHEED. The XPS spectra of Si_{2p} and O_{1s} were recorded using the MgK_α line (1253.6eV).

The amount of oxygen adsorbates on a Si surface was determined by two separate meth-

ods both of which utilize the areal integration of photoemission spectra [13]. Spin doublet has been removed from the spectra. The first method is based on the comparison between the intensity of the chemically-shifted Si_{2p} signal (N_{sO}) and that of unaffected Si_{2p} signal (N_s). The oxygen coverage (X_O) is evaluated by

$$X_O = (N_{sO} / N_s) L_s \sin\theta / t \quad (1)$$

where L_s , θ and t represent the escape depth of electrons in Si, the detection angle of photoelectron and the interlayer spacing of Si(100) (0.136nm), respectively. Equation (1) gives the amount of the "chemisorbed" oxygen atoms. The second method is to evaluate the ratio between the O_{1s} and Si_{2p3/2} signals. By denoting the integrated O_{1s} intensity as N_O and the Si_{2p3/2} intensity as N_{Si} , (X_O) is expressed as

$$X_O = (S_s / S_o)(N_o / N_s) \sigma_s L_s \sin\theta / (\sigma_o t) \quad (2)$$

where σ_o and σ_s are ionization cross sections, S_o and S_s are spectrometer functions and N_o is the intensity of O_{1s} signal. Equation (2) gives the "net" amount of oxygen atoms. In general, eq.(2) gives a larger amount than eq.(1) does. The fraction of oxygen adsorbates on a Si surface which contribute to the surface oxidation is obtained by the X_O from eq.(1) divided by that from eq.(2).

3 RESULTS AND DISCUSSION

First we investigated the influence of the surface topography on the initial oxidation. Four different samples were prepared for this purpose, that is, an on-axis and a vicinal 3° off

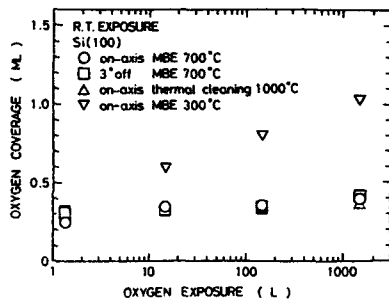


FIG.1 Oxygen coverage versus the MO exposure at RT. Only on the corrugated Si surface, the oxygen coverage grew up to 1 ML. In the other samples, the oxygen coverage is saturated at 0.4 ML within an exposure of a first few L.

toward [110] wafers with atomically flat terraces grown by MBE at 700°C, a thermally cleaned on-axis wafer and an on-axis wafer with a corrugated surface prepared by MBE at 300°C.

Figure 1 shows the oxygen coverage as a function of the MO exposure at RT. The oxygen coverage was determined using eq.(2). As can be seen, the oxygen coverage on the Si surface prepared by MBE growth at 700°C looks saturated at 0.4 ML within an exposure of a few L. This is significantly different from the previous results where the oxygen coverage is saturated at 1 ML[5,6]. Almost the same results were obtained on the vicinal and the thermally cleaned surfaces. On the contrary, the oxygen coverage grew up to 1 ML on the

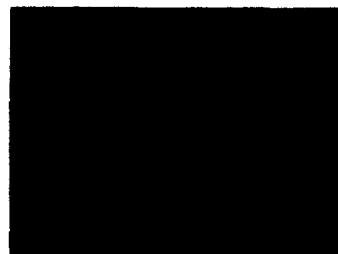
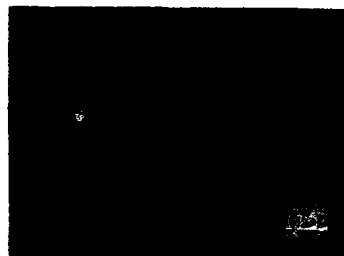
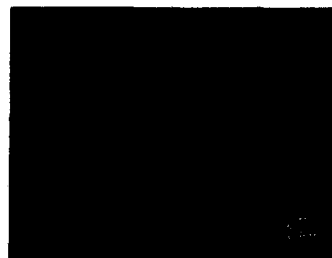


FIG.2 RHEED images from Si surfaces before(a) and after the MO exposure of 1500L (b and c). Si surfaces were prepared by MBE at 700°C. The substrate temperature during the MO exposure was RT(b) and 400°C(c). At RT, the 2x1 reconstruction is preserved even after the MO exposure of 1500L. However, at elevated temperatures, the brightness of 2x1 spots gradually loses.



corrugated Si surface. In addition, the chemical shift of $\text{Si}_{2p_{3/2}}$ photoemission spectrum due to the oxidation was observed only on the sample with a corrugated surface. The amount of oxygen chemisorbed on Si was estimated to be 0.5ML using eq.(1). Thus, approximately 50% of the oxygen on the surface is thought to contribute to the oxidation.

Next we examined how the oxidation proceeds on MBE-grown Si surfaces when the substrate temperature is increased during the MO exposure. Figures 2(a)-(c) show the RHEED patterns before and after MO exposure of 1500L. As shown in Fig.2(b), the original 2×1 reconstruction is preserved even after the MO exposure at RT. On the contrary, at elevated temperatures, although the 2×1 periodicity is preserved, brightness of the low index spots gradually loses, as seen in Fig.2(c). It is noted that the characteristic halo, which is

usually superposed on the 2×1 spots during the oxide formation, is absent. This suggests that the oxygen adsorption proceeds via bridging sites between Si dimer rows.

In the $\text{Si}_{2p_{3/2}}$ photoemission spectra, the chemical shift due to the oxidation is seen on the sample with the MO exposure of 1500L at 300°C and 400°C . The amount of chemisorbed oxygen atoms are determined by eq.(1) to be 0.2ML and 0.6ML at 300°C and 400°C , respectively. The oxygen coverage determined by eq.(2) is shown in Fig.3 as a function of MO exposure. As can be seen, the oxygen coverage increases with the increase in the substrate temperature. The net amount of the oxygen adsorbates obtained by Eq.(2) are 0.6ML and 0.9ML at 300°C and 400°C , respectively. Therefore, about 50% of the net oxygen adsorbates are thought to be involved in the surface oxidation at elevated temperatures.

Finally, we propose an oxygen adsorption model on the MBE-grown Si(100) surface, as

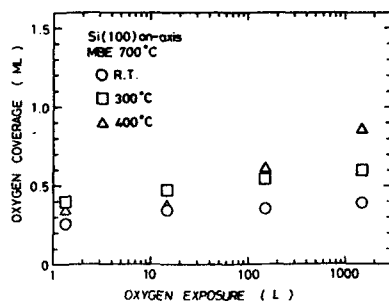


FIG.3 The oxygen coverage versus the MO exposure at RT, 300°C and 400°C . The oxygen coverage increases with the increase in the substrate temperature. At the maximum exposure of 1500L, the oxygen coverage is 0.4, 0.6 and 0.9 ML for the samples treated at RT, 300°C and 400°C , respectively.

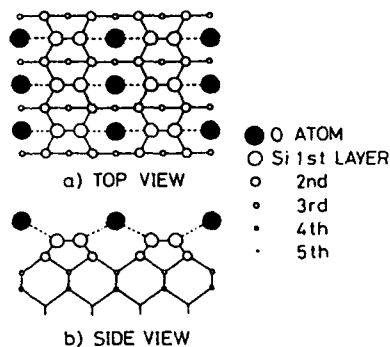


FIG.4 Oxygen adsorption model on an atomically flat and reconstructed Si(100) surface.

shown in Fig.4. This model is well reconciled with the RHEED observation that the 2×1 periodicity is preserved even after the MO exposure. It is likely that the dissociatively adsorbed oxygen atoms occupy the bridging sites, in-between the adjacent Si dimers, forming an atomic row along the Si dimer row without a loss of lattice strain energy. A total energy calculation and a detailed experiment to confirm the adsorption model are now underway.

4 CONCLUSION

It was found that the MBE-grown Si(100) surface was hardly oxidized even after exposure to MO up to 1500L and that the oxygen coverage was saturated at 0.4 ML. However, at elevated temperatures the surface oxidation was found to set in and the oxygen coverage grew up to 1 ML. On the contrary, on a corrugated surface, the surface oxidation was pronounced even at RT and the saturation coverage increased up to 1 ML.

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COLUMNAR STRUCTURE GROWTH BY SILICON MOLECULAR BEAM EPITAXY

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ABSTRACT

Si columnar structures were fabricated using Si MBE on Si substrates with column sizes in the order of ~ 100 Å. The objective is to explore a viable approach to fabricate quantum wire structures. The growth of the structures, which was due to the growth instability, was an excellent example of a self-limiting process. The dependence of column morphology on the critical parameters, e.g., Si molecular beam incident angle, substrate temperature, substrate rotation, speed, etc., were demonstrated. Comparison between the experimental and the computer simulation results demonstrated the importance of the latent heat related atom migration as compared to the normal surface diffusion at low substrate temperatures and several Å/s beam fluxes. A substrate temperature window ($\approx 125^\circ\text{C}$) was observed which allowed the fabrication of crystalline micro-columns on Si (100) substrates. RHEED studies indicated that the crystalline micro-columns were heavily twined. The twinning phenomenon was also observed in the computer simulation results and interpreted as a result of the reduction in twin formation energy due to the extremely small dimension of the columns. Thermal stability of the columnar structures is discussed. Finally, photoluminescence studies and some potential applications are also discussed.

INTRODUCTION

It has long been recognized that columnar microstructures exist in many types of thin films deposited under various conditions. [1-3] Many macroscopic properties such as the effectiveness of W-Ti(N) as barrier layers for Al in Si integrated circuit technology[4], and magnetic anisotropy in iron thin films[5], have been associated with such microstructures. We report our recent study on several aspects of the Si columnar structures grown by molecular beam epitaxy (MBE) on Si substrates. The motivation of our study is to explore any potential optoelectronic application of these structures through effects such as quantum confinement, and to understand certain aspect of this film growth mode which will hopefully improve our understanding of other growth modes of Si films on Si substrates.

EXPERIMENTS

We use a Riber Eva-32 Si MBE apparatus with in-situ RHEED capability to deposit the films on Si (100) substrates. The detailed microstructures are imaged using a tilted cross-sectional transmission electron microscopy (TTEM) technique in an under-focused or over-focused condition as illustrated in fig.1. Such a TEM geometry allows us to obtain the dimensions of individual columns, which is difficult to do using the conventional cross-sectional geometry. Our experimental results are compared with our molecular dynamics simulation results. The samples were subjected to various annealing processes including low temperature oxidation and high temperature vacuum furnace annealing to study the thermal stability of the columnar structures. An Ar-ion laser at 514 nm wavelength line and a Spex spectrometer with a cooled Ge detector are used for photoluminescence (PL) measurements.

The molecular dynamics (MD) simulation was carried out by considering the impingement of a beam of Si atoms onto a Si substrate at a 75° angle of incidence. Single atoms were inserted at

regular intervals into the computational cell at positions far from the substrate where they had no interactions with atoms in the deposit. The velocities of the inserted atoms were directed at normal incidence to the substrate, and the magnitudes of the velocities correspond to a beam temperature of 2800°K. Atomic trajectories were calculated using Newtonian mechanics and forces based on an empirical potential for Si[6]. The temperature of the substrate was regulated by frequent renormalization of the velocities of a group of atoms in the substrate. The atomic beam intensities that are about nine orders of magnitude greater than those used in practice, but they were maintained below the point where the temperature of the deposit would be increased by more than $\approx 50^\circ\text{K}$. Details of the simulations have been given elsewhere[7].

RESULTS

Fig.2A and 2B are conventional cross-sectional TEM micrographs. It is quite obvious that the columns are inclined toward the incident direction of the molecular beam when there is no substrate rotation, and are vertical when there is substrate rotation. The dimensions of each individual column can not be determined from these micrographs because of the overlapping of many columns.

The overlapping problem is alleviated by using the TTEM geometry. Fig.3 is an as-grown Si-on-Si columnar structure. The sample was grown at 150 C (thermocouple measurement). By measuring the individual column sizes, we are able to find an average column size of 130 ± 30 Å. This should be compared with the column size of another sample grown at room temperature (25°C), where the column sizes are in the order of 40 Å. This difference in column sizes with substrate temperature agrees fairly well with the MD simulation result.

The temperature dependence of the growth modes as characterized using RHEED is shown in fig.4. The temperature is determined by a thermocouple situated behind the center of the substrate. Since this temperature reading could be different from the true surface temperature by as much as 200°C (by comparing with a calibrated optical pyrometer reading at $> 500^\circ\text{C}$), the temperature quoted here should be taken as a relative temperature scale only. We see from fig.4 that the growth mode changes from the two-dimensional (streaky RHEED as in fig.4A) mode to the three-dimensional (spotty RHEED as in fig.4B) mode when the growth temperature, and thus the surface mobility of the Si adatoms are lowered. At low enough temperatures, the films grown become microcrystalline or amorphous (ring RHEED patterns as in fig.4D). This result indicates that there is a temperature "window" for growing crystalline Si columns on Si substrates. As we try to grow samples in this temperature "window", however, we find that the columns first grow in the form of twinned crystals (fig.4C), and then gradually change into polycrystalline form. This exact phenomenon is observed from our MD simulation results (fig.5) for a substrate temperature of 370°C. We believe that the phenomenon can be explained by the small dimension (≈ 100 Å) of the columns which have lower energy barriers for twinned crystal formation, and the intersection of two developing twinning planes (as indicated by the dashed pentagon in fig.5) which causes the subsequent amorphous growth.

Fig.6A and 6B are TTEM pictures of an as-grown and a 300°C annealed (in wet oxygen ambient) samples, respectively. It seems that the columns are fused into ridges when annealed even at such low temperatures. Enhanced surface diffusion is believed to be responsible for the process.

The PL results are shown in fig.7. Despite the small dimensions of the columns, no significant shift of the peak position of the luminescence is observed (as might be expected in the light of the recent luminescence results of porous Si[8]). The oxidized sample does show a shoulder on the higher energy side of the bulk Si peaks. The origin of this shoulder in the PL spectrum, however, is not clear at this point.

Although PL did not show a clear indication of quantum confinement effects from these "quantum wires", we believe this could still be an alternative approach to the quantum confined structures. Controlling the sizes of the columns and passivating defect states are going to be the key to achieving this goal.

SUMMARY

We have fabricated Si columnar structures on Si (100) substrates under various conditions. The results show that the columns incline toward the molecular beam incident direction when the substrate is not rotated, and the columns become vertical to the substrate surface when the substrate is rotated. A temperature window at $\approx 125^{\circ}\text{C}$ is found which allows the growth of crystalline columns. In this growth mode, the growth proceeds as twinned crystals, and eventually turns into micropolycrystalline. The column dimensions are determined to range from 40Å to ≈ 100 Å. Excellent agreements are observed between the experimental and the MD simulation results. Photoluminescence study did not show a clear indication of quantum confinement effects.

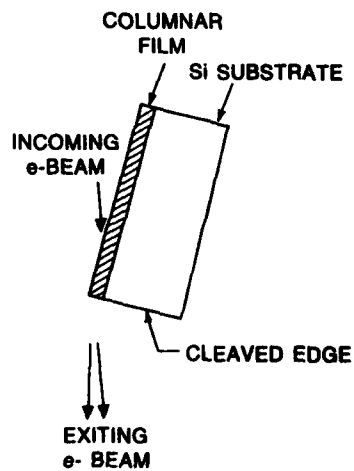


Figure 1. Illustrative geometry of tilted cross-sectional TEM.

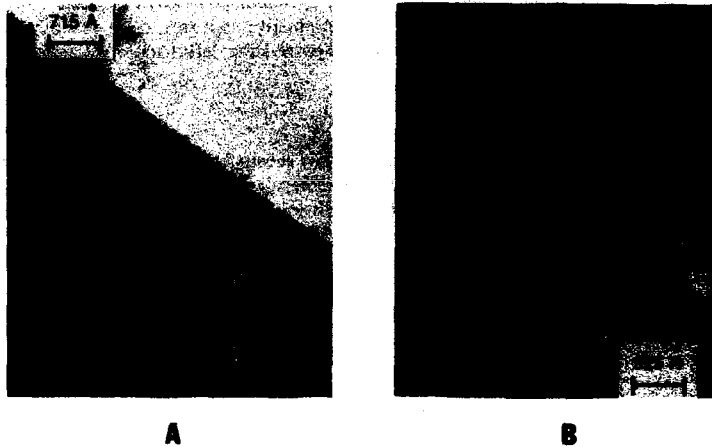


Figure 2. Conventional cross-sectional TEM micrographs of (A) a sample grown at glancing beam incidence without substrate rotation; and (B) a sample grown first without and then with substrate rotation.



Figure 3. Tilted TEM micrograph of a sample grown at 150°C substrate temperature (measured by thermocouple).

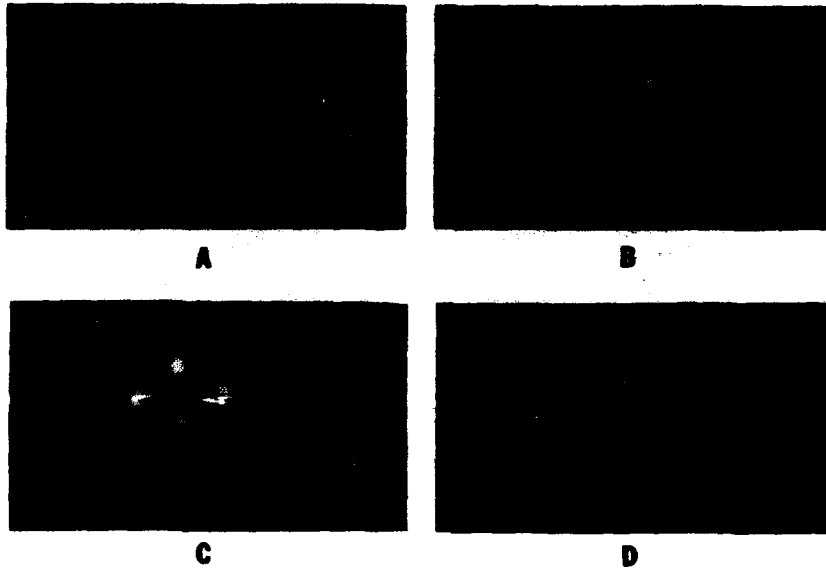


Figure 4. RHEED pictures taken at various stages of the columnar structure growth: (A) 550°C growth, (B) 125°C growth, (C) heavily twinned structure; and (D) 25°C growth, or after growing a thick layer at 125°C.



Figure 5. Molecular dynamics simulation result of Si columnar structure growth.

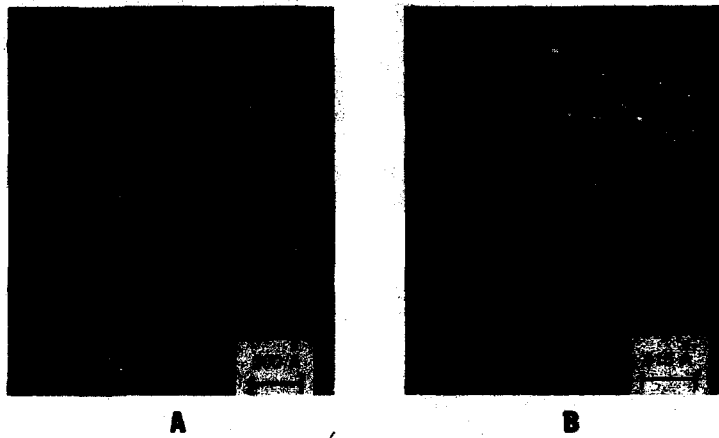


Figure 6. Tilted TEM image of (A) an as-grown columnar structure, and (B) the same sample annealed at 300°C in wet oxygen.

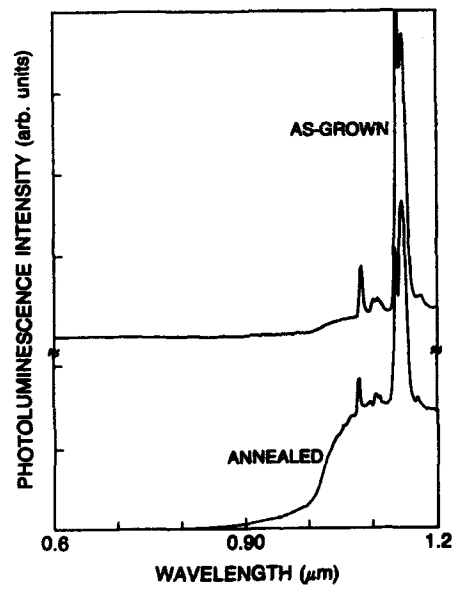


Figure 7. Photoluminescence result of the as-grown and the annealed samples.

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EQUIPMENT FOR MONITORING AND CONTROLLING RHEED-OSCILLATIONS

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ABSTRACT

A Light Oscillation Control Unit System (LOCUS) has been developed for the purpose of monitoring Reflexion High Energy Electron Diffraction (RHEED) oscillations and to use the oscillations to control the crystal growth with single atomic layer resolution. The system can be used for phase-locked epitaxy, i.e., shutters controlling the growth are actuated when monolayers are completed. To reduce the usual damping of the RHEED-oscillations, the system can also use the method of synchronization of nucleation, i.e., periodically varying the surface supersaturation by changing the substrate surface temperature during each oscillation. Four shutters can be operated automatically and the superlattice composition can be chosen in a number of different ways. LOCUS gives fast response on intensity oscillation maxima and minima beyond a programmable discrimination level. Relevant crystal growth parameters can be changed during the run of the program, which implies that even quasi-periodic superlattices can be grown. There is also a possibility to switch from automatic to manual control. The shutters and substrate heater have been designed to reduce the influence of shifts of the diffraction pattern as the growth conditions are changed.

INTRODUCTION

There is a periodic change of the surface structure and flatness that occurs for wide ranges of growth conditions during molecular beam epitaxy (MBE). By using reflexion-high-energy-electron diffraction (RHEED) or optical techniques it is possible to monitor these changes as intensity oscillations.^{2,3} For MBE-growth of Si and Ge, RHEED oscillations have been reported to have a period corresponding to completion of double(atomic)-layers on the (111) surface while both mono-layer and double-layer oscillations have been observed for different experimental conditions of growth on the (100) surface.

The use of RHEED-oscillations to monitor and control the growth of heterostructures and superlattices has been quite extensive for growth of III-V semiconductors, and e.g. the technique of phase-locked epitaxy has been developed that means that alterations of the growth conditions (fluxes, substrate temperature) are initiated in certain phases of the RHEED-oscillations.¹ For this technique to be useful it is essential that the RHEED-oscillations can be maintained over the full thickness of the structure to be grown. This can be a problem since the amplitude of RHEED-oscillations generally decay, as there is a gradual increase of the surface roughness during growth. The gradual surface roughening can be avoided if the substrate temperature is increased but then the nucleation of islands necessary for RHEED-oscillations is obstructed since the higher surface diffusion will favor growth at steps.

Markov et al.⁴ recently suggested a method to maintain RHEED-oscillations by synchronization of nucleation. By periodically increasing the surface supersaturation at the onset of growth of each mono-layer according to the RHEED-intensity variation, the aim is to nucleate island growth on wide as well as narrow terraces at the same time. It was shown that it was possible to improve the endurance of the oscillations by this method both by periodically changing the substrate heating and the impinging flux.

In this paper we describe a recently developed equipment for monitoring RHEED-oscillations and controlling the growth by modification of the growth parameters in phase with the RHEED-oscillations. Some preliminary results for Si-MBE with synchronization of nucleation using a radiating graphite heater facing the growth surface are also reported.

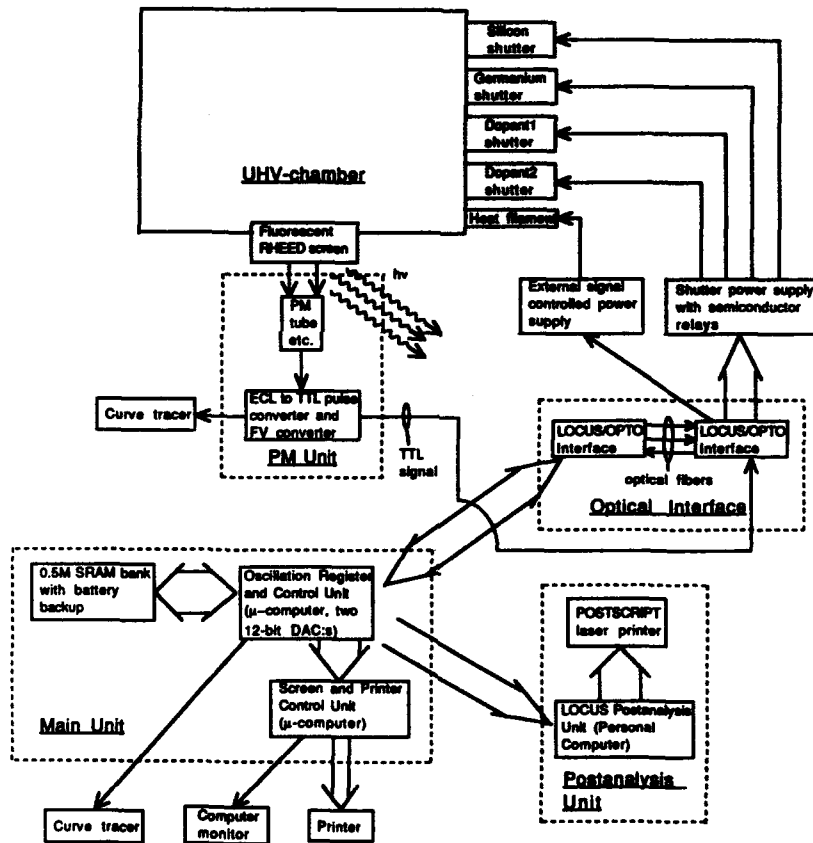


Fig. 1 LOCUS schematic block diagram

EXPERIMENTAL EQUIPMENT

The Light Oscillation Control Unit System (LOCUS) consists of Main Unit, PM Unit, Optical Interface, Postanalysis Unit and peripheral devices. A schematic block diagram of the system is shown in Fig.1.

The PM Unit contains the light sensor of LOCUS. It consists of a photomultiplier (PM) tube with HV power supply, an ECL to TTL pulse converter and a frequency to voltage (FV) converter. Optics has been developed to focus on one spot in the RHEED-pattern. The PM tube with optics is mounted on an adjustable xyz-table in front of the fluorescent RHEED-screen. The ECL to TTL converter converts the electrical signal from the PM tube preamplifier to an aperiodic signal consisting of 300ns wide TTL-pulses. The TTL-signal is converted by a fast FV converter to an analog signal (0-10V, where 10V corresponds to 2MHz). The TTL-signal is transferred via the Optical Interface to the Main Unit. The PM Unit and a Curve Tracer can be used independently of the rest of LOCUS if just recording of RHEED-oscillations is requested.

The Optical Interface isolates the LOCUS-ground optically from the ground of the MBE-system. It consists of the LOCUS/OPTO Interface, three optical fibers and the OPTO/MBE Interface. To protect the system from noise, there is also a noise protection transformer employed. One optical fiber is used to transfer the light intensity TTL-signal from the MBE-system to LOCUS. The other two fibers are used to transfer data from LOCUS to the MBE-system. One of these optical fibers transfers the growth synchronization programming pulse to the heat filament power supply. The other optical fiber transfers the eight shutter controlling pulses, which are multiplexed through the optical fiber by two UART6402 (Universal Asynchronous Receiver Transmitter)-circuits, one on each side of the optical fiber.

The heart of LOCUS is the Main Unit which consists of Oscillation Register and Control Unit (ORCU), Screen and Printer Control Unit (SPCU) and a 0.5Mbyte RAM bank memory with battery backup. The ORCU consists of one CAN09 one-card μ -computer,⁵ two 12-bit DAC:s (Digital to Analog Converter), two additional PIA6821:s etc. The SPCU consists of one CAN09. CAN09 is equipped with one MPU6809-processor, PIA6821-parallelport, PTM6840-timer module, ACIA6850-serialport, RAM, PROM etc. The system clock has the frequency of 1.4MHz. Due to the fact that the Main Unit is a real time system, a RAM bank is used to store data since it is the fastest method. The growing routines in ORCU and SPCU are written in 6809 assembler language. The software consists of three main parts: the LOC (Light Oscillation Control) program; the DT (Data Transfer) program and the TC (Time Control) program. The DT program transfers intensity data from the Main Unit to the Postanalysis Unit. The TC program can be executed if the growing crystal surface does not exhibit RHEED-oscillations of reasonable quality, and thus cannot be used to control the crystal growth. The LOC program performs the major part of the LOCUS functions.

The light intensity TTL-signal is counted by the timer module in ORCU. The data are sent parallel from ORCU to SPCU where it is graphically displayed on a computer monitor. The data is also transferred continuously to one of the DAC:s. By connecting a curve tracer to the DAC a record of the intensity signal can be

attained. Each filled screen page can optionally be dumped via the serial port on SPCU to a printer.

In this paragraph we describe the working sequence of LOCUS for synchronization of nucleation by variations in the substrate growth temperature. At each detected minimum in the intensity signal there is a growth synchronization programming pulse generated by ORCU. It passes through the Optical Interface and activates a programmable power supply which sends a high current through a graphite filament. The filament will continue to glow for some seconds after the programming pulse has finished. This after-glow has been compensated for in the LOC program. When the required number of monolayers of a certain material has been grown the shutter configuration is changed.

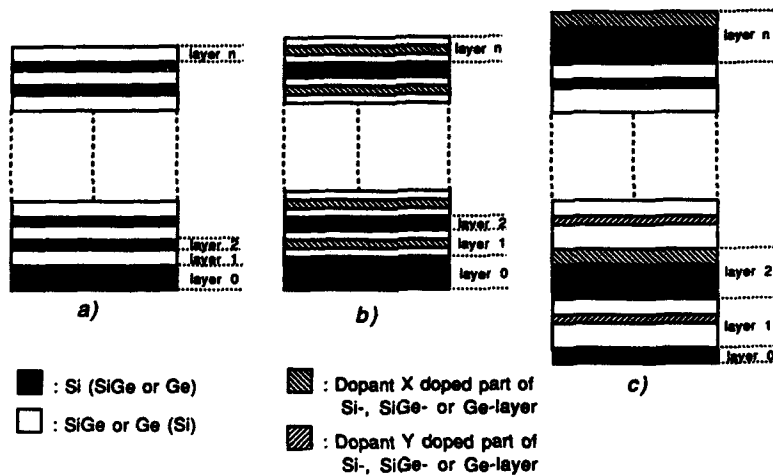


Fig. 2 Available crystal growth structures in LOCUS, a) Growth of alternating undoped layers. b) Alternating undoped and doped layers. c) Coherent doping and heterostructure superlattice.

The programming pulses for the shutters are generated via one parallel port and transferred through the Optical Interface to the shutter power box where the semiconductor relays are activated. As a result of this action the shutters will be reconfigured and a different set of shutters will be open. Crystal structures can be grown according to three different growth modes, see Fig. 2. The first type, exemplified in Fig. 2a needs two sources, one Si and one Ge. They are used alternatively, by changing the shutter configuration, until the required number of atomic layers have been grown. One Si-, one Ge- and one dopant-source are utilized to grow the crystal type shown in Fig. 2b. In this structure every second crystal layer has a doped region and the adjacent layers are undoped. If four sources are used, the structure shown in Fig. 2c can be obtained. In this crystal the used sources are Si, Ge and two dopants. All important display and growth parameters can be changed in real time during the growth. The shutters and the growth synchronization can be operated either automatically or

manually. This means that even quasi-periodic superlattices can be grown.

Postanalysis of acquired data can be performed by utilizing the Postanalysis Unit. It consists of a Personal Computer (PC) and a laser printer with installed Postscript-program. The driving routine in the PC is the Turbo Pascal-program "LOCUS Postanalysis". Intensity data can be sent in parallel from the Main Unit to the Postanalysis Unit when the acquisition is finished, by executing the DT program in the Main Unit. "LOCUS Postanalysis" saves the data and displays it graphically on the screen. The curve can be compressed and offset-compensated before the program creates a POSTSCRIPT-file and a high quality plot can be achieved from the laser printer.

RESULTS

The experiments were performed in a VG V-80 Si-MBE-system. The system and the standard substrate cleaning procedures have been described elsewhere.⁶ The final preparation of the substrates before the RHEED studies, used a similar procedure as that described in the work by Sakamoto and coworkers.¹⁻³

The system performance at the growth of a strained layer superlattice (SLS) on a Si(111) substrate at 450 °C is indicated in Fig. 3. The figure shows a part of the RHEED-intensity-variations of the specular beam, during the growth of a $((\text{Si}_{0.8}\text{Ge}_{0.2})_{10}\text{Si}_{10})_8$ -structure. In this case 80 RHEED-oscillations could be monitored before the oscillation intensity had decreased to the noise level. Two monolayers, i.e. one double-layer, correspond to one RHEED-oscillation. The sharp features in the oscillation curve indicate the movement of the Ge-shutter. It is seen that during pure Si growth the amplitude of the oscillations increases while it decreases during the growth of the alloy layers.

The method of synchronization of nucleation was tested by

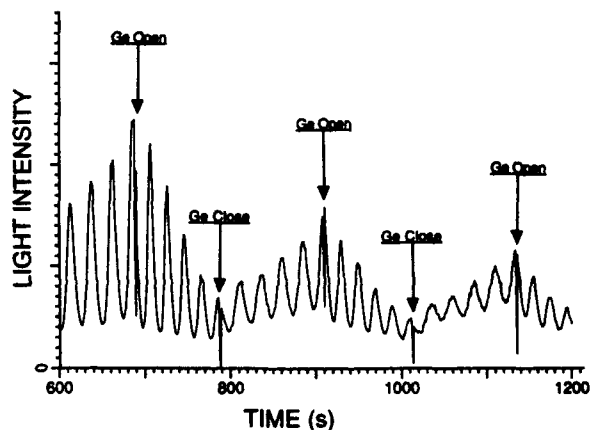


Fig. 3 $((\text{Si}_{0.8}\text{Ge}_{0.2})_{10}\text{Si}_{10})_8$ strained layer superlattice

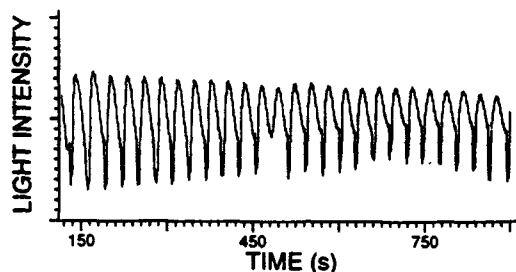


Fig. 4 Synchronization of nucleation for growth of Si on Si(111) with 5s long temperature modulation pulses. The time per growth of one double-layer is ≈ 30 s.

applying a heat pulse at each minimum in the RHEED-oscillation signal for growth of pure Si by evaporation on a Si(111)-substrate. The heat pulse was created by applying 1000W to a graphite filament positioned 30cm below the substrate. Three different experiments were performed, for different heat pulse lengths, with an initial substrate temperature of 480°C . The growth rate was kept fixed at $\approx 0.1\text{\AA}/\text{s}$. For heat pulses with the duration of 5s 120 RHEED-oscillation periods were clearly detected. Part of these oscillations are shown in Fig. 4. In the center of the figure there is one oscillation for which no heat pulse was applied and by comparing this with the other oscillations it is possible to identify the disturbance of the intensity measurement that is induced by magnetic effects from the heating current. 150 RHEED-oscillation periods were counted for 15s long heat pulses. For no applied extra heat to the substrate surface there were just 65 RHEED-oscillation periods detected. Thus it is clear that the synchronization of nucleation is a technique that can improve the growth also in the case of large area substrates, as these studies were done on a 3"-wafer.

ACKNOWLEDGEMENTS

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THE "COMPUTER-AIDED EPITAXY" Si:MBE-CONTROL SYSTEM

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ABSTRACT

A dedicated, grower-friendly MBE computer control system is described, and its performance in demonstrated in growth of high resolution doped SiGe structures.

INTRODUCTION

The physical phenomena of current scientific and technological interest in semiconductors rely on complex structures with high resolution of the matrix and doping profiles[1,2]. Accurate fabrication and reproducibility of these structures poses a major challenge to MBE growers, both in terms of the tedium involved in their growth, and the complexity of the calibration data needed to translate a desired structure into MBE system control parameters (temperatures, control currents, ped voltages etc.). In this paper, we describe our experience over a 9 month period with a dedicated MBE computer control system[3] designed to reduce the element of operator inexperience (and thus error) on material fabrication. The software is based around a *graphics user interface* to simplify operation. All calibration data is handled by the computer to facilitate data entry and display is in physically familiar ("grower friendly") terminology of deposition rates, alloy compositions and doping levels. Examples of complex high resolution structures grown under computer control are presented to demonstrate the capability of the system.

COMPUTER SYSTEM

The PE *Computer-Aided Epitaxy*[4] family of MBE controllers are IBM PS2/80 computer based, with high resolution VGA colour monitor, keyboard, pointer device (mouse or tracker ball) and printer (Fig. 1). A dedicated interface unit (IU) connects and configures interface cards internal to the computer with the MBE process and system electronics. The IU is extensible, offering up to 4 serial ports, 8 analogue inputs and 8 analogue outputs, 10 separate shutter control and shutter monitor I/O lines and 20 other programmable I/O lines. Although the control mode of each MBE source is software selectable the serial control connections have dedicated uses for ease of system interfacing. IU serial port 1 connects to the standard MBE process controller

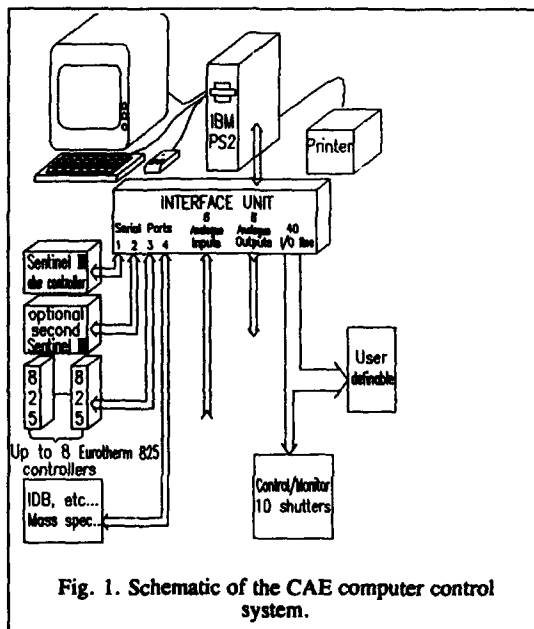


Fig. 1. Schematic of the CAE computer control system.

(Sentinel III EIES controller - Inficon Inc.,) which can control 2 electron beam evaporators. For more complex evaporation procedures (for example, growth of High T_C superconductors), a second process controller can be connected to IU serial port 2. Up to 8 other evaporation sources using shared serial communications (such as conventional effusion sources with Eurotherm temperature controllers) can be connected to IU serial port 3. The remaining serial port and the standard serial port on the computer are available for interfacing to specialist equipment (for example, ion beam doping unit, mass spectrometer...), or to further temperature controllers. The first 4 analogue outputs and inputs are configured for software selectable source control and monitor channels; the remainder are available for source or system control/monitoring. The first 20 of the 40 I/O lines control/monitor up to 10 shutters, and the remainder will be application selectable for process or system connection (for example, control over system bakeout, valve operation).

The CAE programme uses time-critical interrupts to ensure accurate process timing. Communications and layer timing procedures needed to run an epilayer specification and to control/monitor the MBE system are performed as background tasks. The programme is thus effectively multi-tasking, allowing the user to define new epilayer specifications and use other time independent modes whilst running an epilayer specification. Certain modes (e.g. calibration) are however closed to access during running to eliminate the possibility of erroneous data entry during structure growth. The grower may nevertheless interact with the programme to make changes in response to error conditions occurring during running of a process.

THE GROWER/COMPUTER INTERFACE

On startup, the programme initialization procedures take ~30 seconds to load and test configuration, calibration and communications, before entering control mode. Data entry is security protected, logging off if no keyboard action occurs within 15 mins. Most data input is via mouse/keyboard selection from a conventional-style menu bar and icon display. The main menu offers a range of modes of operation, including status, epilayer specification, run, calibration, configuration, data, security, file handling, etc. (see below). To minimize confusion and ensure ease of use, menu nesting is restricted to 3 levels within any mode, with previous menus remaining visible on the display. The main modes are briefly described:

(a) Status Mode

This mode produces a schematic representation of the MBE system (shown in Fig. 2), with data fields for source, shutter and system parameters updated every second. The grower can interact with the display to change any of the setpoints or shutter positions ("manual" operation), even during epilayer run mode to correct for error conditions occurring.

(b) Epilayer Specification

This mode facilitates programming of a complete

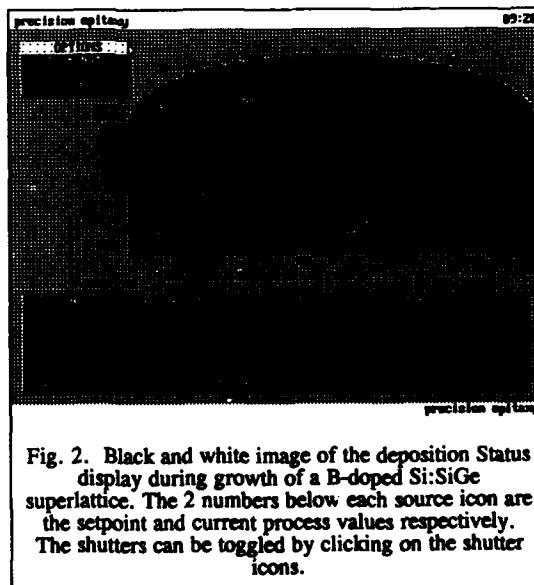


Fig. 2. Black and white image of the deposition Status display during growth of a B-doped Si:SiGe superlattice. The 2 numbers below each source icon are the setpoint and current process values respectively. The shutters can be toggled by clicking on the shutter icons.

epilayer specification list, comprising an arbitrary number of layers, and including initial substrate/source conditioning and final resetting to standby values. Facilities are included to enter superlattice repeat sequences, nesting up to 10 levels. Individual layers, as well as repeat sequences can be moved, copied or deleted by selection with the pointer device.

Each layer is specified by a thickness, surface coverage (e.g. for δ -doping) or time (if no source shutters are open). Within each layer, any of the source/substrate control parameters can be modified. A change in a source's ramp/doping level initializes a rate for that source over the period of the layer, thus allowing controllable graded compositional/doping

transitions, as well as abrupt transitions, to be executed. For ease of use, alloy compositions and doping levels are entered as such (rather than as temperatures or control currents etc!), and are translated at run time via the calibration data (see below).

Fig. 3 shows a sample specification screen during editing of a layer, in which a new B-doping level is being entered. Shutters are toggled by selection with the pointing device. Complete epilayer specifications are file named, a description added and saved on diskette for future retrieval and running.

(c) Run Mode

After selection of a file to be run from a diskette list, the file is loaded and "compiled" automatically (a process taking ~15 seconds). The software then waits for grower input to start the MBE process. Progress of growth is displayed on the status screen (see (a) above).

(d) Calibration Mode

The computer requires calibration data, to translate between the structure-related parameter (actual growth rate (nm/s), alloy composition, doping level, rotation speed etc.) and the MBE machine process variable (controller

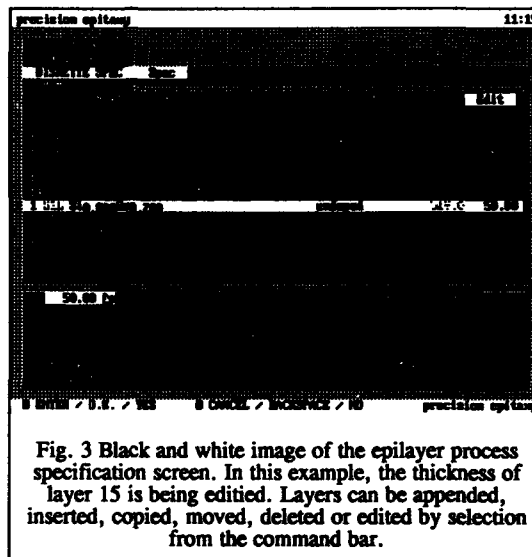


Fig. 3 Black and white image of the epilayer process specification screen. In this example, the thickness of layer 15 is being edited. Layers can be appended, inserted, copied, moved, deleted or edited by selection from the command bar.

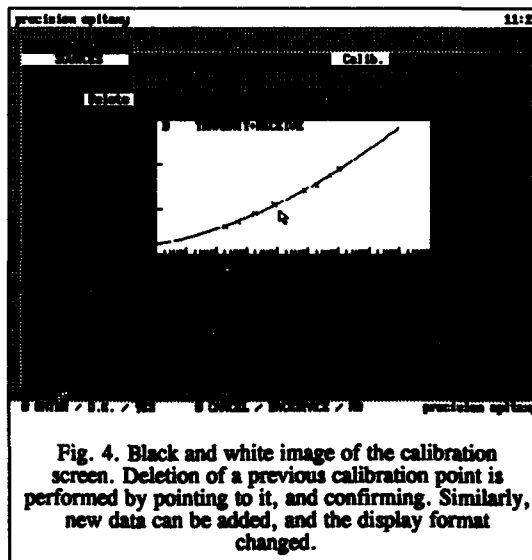


Fig. 4. Black and white image of the calibration screen. Deletion of a previous calibration point is performed by pointing to it, and confirming. Similarly, new data can be added, and the display format changed.

growth rate ($\text{\AA}/\text{s}$), source temperature/control parameter, control current etc.) at run time, and for status mode updating. Fig. 4 shows a calibration data entry screen, comprising graphical representation of the data. Axis types and range are user selectable, and data editing is rapid. A best fit curve is automatically computed after each data entry for use in interpolation routines.

RESULTS

We have employed the CAE-Si software package for MBE process control of a customized VG V90S instrument, used for deposition of high resolution B- and Sb-doped SiGe structures onto wafers up to 150mm ϕ . Si and Ge fluxes are generated by electron beam evaporation controlled by a Sentinel III controller. The substrate, and the B and Sb sources are controlled using Eurotherm 825s connected to IU serial 3. Only in the case of Sb, is the temperature control facility of the 825s employed; constant current is applied to the graphite substrate heater and to the B-source (by programming of the 825 maximum power parameter), offering reproducibility of $\pm 5^\circ\text{C}$ and $\pm 25\%$ in temperature and doping level respectively. All source shutters are also under computer control. After manual transfer of the wafer into the MBE system, each growth process is executed automatically.

(a) Flux Control

Apart from allowing use of structure-related input for epilayer specification, computer access to calibration data also allows artificial calibration factors to be applied to enhance process performance. For example, to achieve improved control over deposition,

we have implemented improvements to our Sentinel III controller, allowing calibration factors of 40 times (i.e. a rate of $0.1\text{nm}/\text{s}$ requires an indicated Sentinel rate of $40\text{ \AA}/\text{s}$) to be used, and thereby allowing accurate flux control to rates below $0.005\text{nm}/\text{s}$ and $0.002\text{nm}/\text{s}$ for Si and Ge respectively[4]. We also observed a reproducible $\sim 40\%$ non-linearity in Sentinel sensor response to Si flux over the range $0.01\text{--}0.3\text{nm}/\text{s}$ due to changes in flux

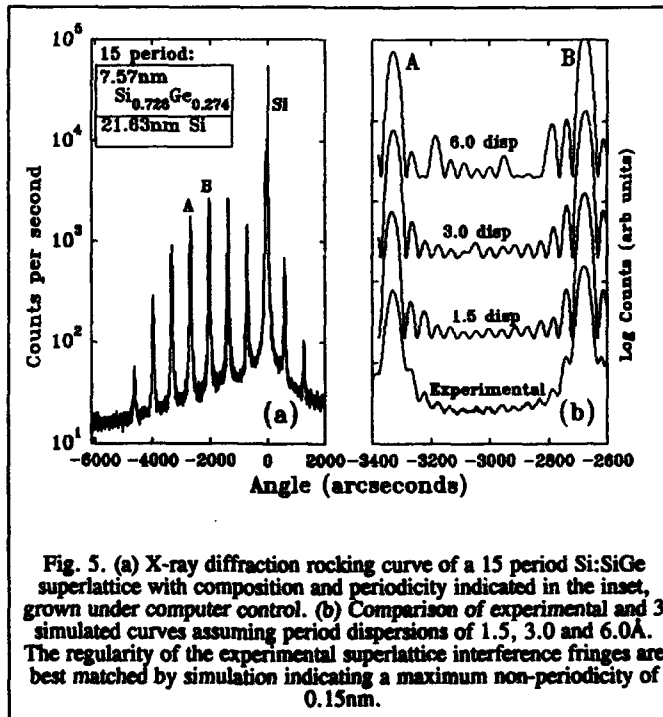


Fig. 5. (a) X-ray diffraction rocking curve of a 15 period Si:SiGe superlattice with composition and periodicity indicated in the inset, grown under computer control. (b) Comparison of experimental and 3 simulated curves assuming period dispersions of 1.5, 3.0 and 6.0 \AA . The regularity of the experimental superlattice interference fringes are best matched by simulation indicating a maximum non-periodicity of 0.15nm.

sampling geometry within the sensor head with increasing Si melt/evaporation area[4]. Automatic compensation for such effects is clearly important to ensure growth of intended structures.

Improved control and reproducibility of MBE structures requires the elimination of human error during growth of complex ramps or repeat structures. As an example, Fig. 5(a) shows X-ray rocking curves from a superlattice, as specified in the inset, and Fig. 5(b), bottom curve, an expansion between SiGe order peaks denoted A and B. The dynamical theory simulations[5] shown in the upper three curves indicate the gradual loss of regularity and envelope shape as dispersion (non-periodicity) increases from $<0.15\text{nm}$ (the resolution limit) to 0.6nm .

Comparison between the experimental and simulated curves therefore indicates a non-periodicity of better than 0.15nm in a period width of 29nm , corresponding to a flux control and shutter timing accuracy of better than $\pm 0.3\%$.

(b) Ramp Control

Figs. 6 and 7 show triangular Ge and sinusoidal B profiles, the setpoint being updated by the computer at 1 second intervals to obtain a high level of control. Arbitrary profiles of this type can easily be programmed via the text editor-like epilayer specification mode.

(c) δ Doping

Fig. 8 shows SIMS profiles through B- and Sb- δ layers in Si, executed by specifying sheet density in the layer specification. The computer used the calibration data to calculate the time needed for dopant accumulation at the previously set doping level values, whilst ensuring minimal interruption to the Si matrix flux. The B- δ structure with a sheet density of $3.8 \times 10^{14} \text{cm}^{-2}$ was grown at 480°C , and found to be completely activated. Dynamical simulations of high resolution X-ray diffraction data from this structure indicated confinement of the δ to less than 1nm [6,7]. Weak localization and associated electron-electron interaction phenomena

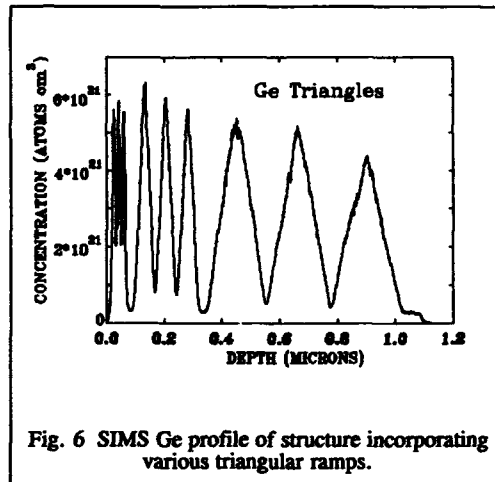


Fig. 6 SIMS Ge profile of structure incorporating various triangular ramps.

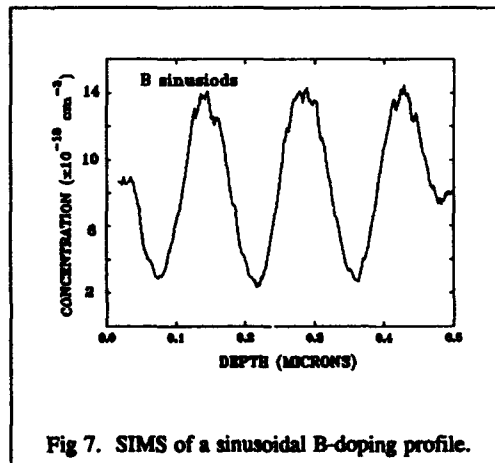


Fig 7. SIMS of a sinusoidal B-doping profile.

have been observed for the first time in these B- δ s[8].

The growth schedule for the Sb- δ was more complex, requiring deposition of the Sb at 600°C to the required density. To preclude Sb "segregation", the substrate is ramped to <250°C (taking ~70mins to get there) for Si cap growth. After cap growth, the substrate is ramped to 700°C for 10 minutes to anneal. The entire process is controlled automatically by computer. The confinement of the 2×10^{14} cm⁻² Sb- δ was determined by high resolution X-ray diffraction to be less than 2nm[6,9].

CONCLUSIONS

The new CAE MBE control software has been described, which includes: (i) a user-friendly graphics interface, (ii) on-board calibration to simplify data entry during epilayer specification and operator interpretation of the growth process, and (iii) high precision timing accuracy. To date, ~150 epilayers have been grown under CAE computer control; examples of high precision structures have been presented. Based on this experience, a variety of refinements are being implemented in execution protocol, still more sophisticated calibration procedures and inclusion of the standardized user interface[10]. MBE structures are becoming increasingly complex, and greater accuracy and reproducibility is being demanded, thus to paraphrase Adams' Marvin (the paranoid android)[11] "Computers! Loath them or hate them, you can't possibly do without them".

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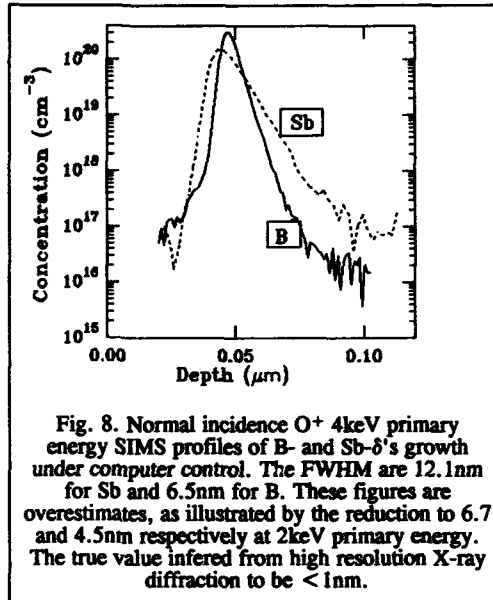


Fig. 8. Normal incidence O⁺ 4keV primary energy SIMS profiles of B- and Sb- δ 's growth under computer control. The FWHM are 12.1nm for Sb and 6.5nm for B. These figures are overestimates, as illustrated by the reduction to 6.7 and 4.5nm respectively at 2keV primary energy. The true value inferred from high resolution X-ray diffraction to be <1nm.

PART II

Doping

AN OVERVIEW OF DOPING STRATEGIES IN Si:MBE

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ABSTRACT

This paper reviews the diverse methods used to achieve doping during MBE of Si and SiGe, and the incorporation processes involved. The optimum choice of dopant and methodology depends on the most appropriate growth conditions for a given structure. At growth temperatures exceeding 750°C, Potential Enhanced *n*-type doping of coevaporated Sb is capable of achieving high resolution structures, at doping levels up to mid-10¹⁹ cm⁻³. At lower temperatures, such as those most suited to SiGe growth, Sb-doping becomes a formidable challenge, due to the high accumulated equilibrium coverages required. Low energy ion implantation appears to be the favoured route for good control. *p*-type B-doping can readily be achieved by coevaporation of compounds or, to avoid oxygen incorporation at low temperatures, the element. A "designer" chart for B-doping of Si is presented.

INTRODUCTION

At or very near the top of the average MBE grower's wish-list is precise control over positioning, level and electrical activation of both *n*- and *p*-type dopants. Motivating this is the device potential of structures incorporating compositional and doping transitions with monolayer resolution[1]. This is a perceived attribute of MBE; growth is conducted at temperatures well below those at which bulk diffusion occurs[2], so structures should directly reflect the composition of the matrix and dopant incident flux generated either by toggling shutters, or by controlling MBE process variables (cell temperatures, rate controllers, etc.). Furthermore, in an ideal world, we would wish for a dynamic range of 10¹³ to 10²¹ cm⁻³, with complete electrical activation and no indigenous material quality penalties.

So much for our dreams! Fig. 1 illustrates the surface processes occurring during MBE growth. Supplying a crystalline surface (under typical MBE growth conditions) with a flux of constituent species leads to a high supersaturation of the vapour phase. Epitaxial growth [3] occurs by incorporation of atoms at step edges which thus propagate over the substrate surface[2] from a surface "adlayer". Under steady state conditions, a balance exists between atomic arrival, desorption and incorporation rates. The arrangement of atoms on such surfaces are reordered (*reconstructed*) to minimize surface strain[4], and "addition" of an atom at a crystal lattice site involves overcoming a potential barrier associated with this strain[5]. (Indeed, this ultimately imposes a limit to the growth process at very low temperatures[2].) Dopant atoms must overcome an additional barrier to their incorporation because they differ in size from the matrix species causing an extra strain-related term [5]. It is no surprise then that doping is not an easy process.

In practice, technological factors, as well as surface processes impose restrictions on our doping capabilities. A careful balancing act is required on the part of the grower and device/structure designer to find the best compromise between the various intended material specifications. This paper briefly outlines various methods that have been, and are being developed to overcome the problems of doping Si (and SiGe), illustrating some of them with examples.

THE DOPING PROBLEM

The choice of dopants in MBE Si was governed initially by considerations other than those of low ionization energy, high solubility and low diffusion coefficient applied by the bulk-Si industry. The earliest studies of doping in MBE:Si utilized conventional III-V:MBE effusion sources[6] to coevaporate the dopant species, evaporation compatibility being the prime consideration. Doping relied on *spontaneous* incorporation under "normal" growth conditions (growth rates of 0.1 to 0.3nm sec⁻¹, and substrate temperatures of 500-900°C).

Of the available groups III and V elements, B was considered to have too low a vapour pressure for evaporation from effusion sources (despite its ubiquitous and unique role in Si devices for *p*-type doping), and P and As vapour pressures were too high to permit dopant flux control from effusion sources and low levels ($<10^{14}$ cm $^{-3}$) of unintentional doping[7-9]. With the exception of Sb, the remaining MBE-compatible dopants Al, Ga and In, have a limited usefulness in device structures due to relatively low solubility limits ($\approx 10^{18}$ cm $^{-3}$) and deep ionization levels. Pioneering work by Bean[8,9], and the groups of Allen[10-12] and Kasper[13] found that doping profiles using these dopants differed significantly from the temporal variation in incident flux composition; under equilibrium conditions, incorporation efficiency varied rapidly with growth temperature, and transient changes in doping flux resulted in smeared profiles (illustrated in Fig. 1). Measurements of residence times (the characteristic time for which atoms remain on a surface before desorption) of Ga[10] and Sb[12] exceed the period taken for growth of a monolayer by many orders therefore, a high desorption rate does not account for the low incorporation efficiency. The only alternative is accumulation of dopant on the Si surface as growth progresses, and this accounts for both equilibrium and transient effects.

A variety of phenomenologically-based formulations, which balance the competing surface processes of arrival, desorption, incorporation and surface accumulation (see Fig. 1) have been used to describe dopant behaviour in Si[10,14-17] and in III-V's[18 and refs therein]. These have been instrumental in the development of refinements to the coevaporation method (discussed below) which have permitted a variety of device structures to be realized. The reader is referred to the excellent reviews of this work[10,14-17 and refs therein] for details.

These kinetic descriptions do not, however, elucidate the *mechanism* by which dopant accumulation occurs, neither do they provide the predictive element expected of a physical account. This is because the mechanism for surface accumulation implicitly assumed was one of bulk segregation[19]. Nevertheless, some progress has been made towards a better fundamental understanding. Andrieu *et al*[20] calculated E_i , the incorporation energy of dopants, based on a model in which dopant atoms surface-accumulate by "climbing" the propagating BCF growth steps. Their model provides a more explicit formulation of the surface accumulation kinetics than earlier phenomenological descriptions, and accounts for the linear dependence of incorporation efficiency with growth rate. E_i was found to increase with dopant atom size. This is in agreement with Pindoria *et al*[5], who further noted that in compound/alloy matrix systems, site occupancy by the dopant is dependent on the relative sizes of the matrix atoms. Application of the theory for equilibrium segregation in metallic systems, in which the balance between bulk and surface dopant concentrations depends on strain energy and local bonding energy, gave qualitative agreement with the size-dependent observation. However, the regular solution model is inadequate for covalently-bonded semiconductor systems, since little is known about surface energetics, particularly when complicated by surface anisotropy, the effects of islanding

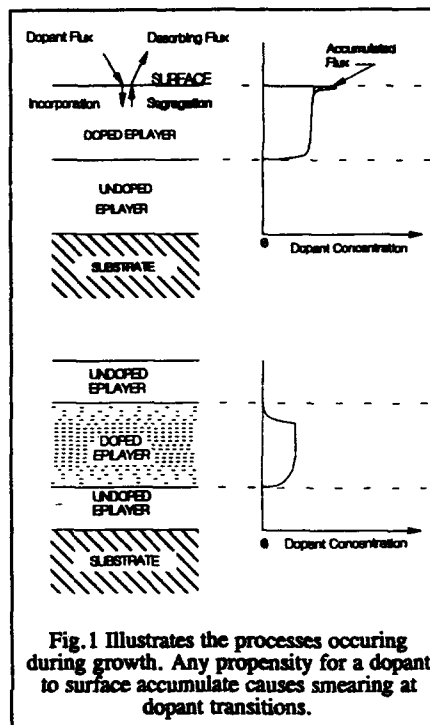


Fig. 1 Illustrates the processes occurring during growth. Any propensity for a dopant to surface accumulate causes smearing at dopant transitions.

(e.g. Ga) and molecular arrival (e.g. Sb₂). Nevertheless, these papers, as well as recent multi-well descriptions of accumulation kinetics [21,22] are beginning to provide a physical basis for the incorporation process.

Unfortunately, as well as being the most useful, Si is one of the smallest crystalline matrix atoms. On the basis of Pindoria's work[5], most dopant species will therefore surface accumulate. Fig. 2(a) represents schematically the observed dopant behaviour in Si. Al[9], Ga[9,10,14], As[23,24], In[17,25] and Sb[12-15] all surface accumulate to a significant extent, although, as mentioned above, the degree of accumulation does not directly reflect dopant-atomic size, due to differences in surface behaviour. In contrast B[26,27] and P[28] show relatively little propensity to accumulate at levels below solubility limits, although still enough to cause some problems in high resolution structures (see below). Since little work has so far been performed, we can only speculate on doping behaviour in Ge. As shown in Fig 2(b), the larger Ge atom increases the size threshold at which severe accumulation is to be expected, and suggests that As would become a "well behaved" dopant. Based on the observations made in compound semiconductors, incorporation of As in SiGe alloys will be favoured on Ge sites, thus the transition to negligible accumulation for As may well occur at reasonably low compositions. Further experimental work is required.

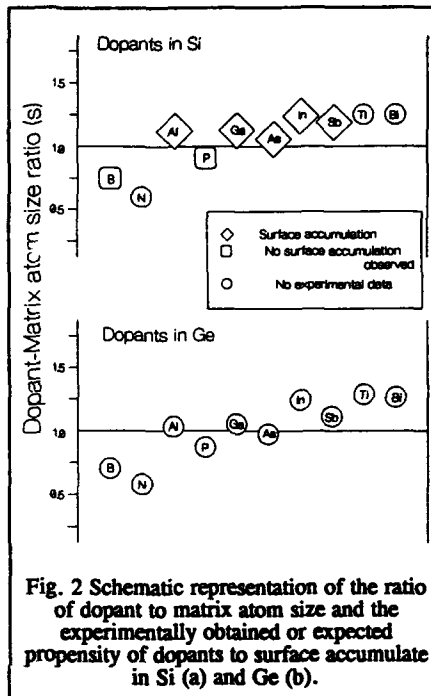


Fig. 2 Schematic representation of the ratio of dopant to matrix atom size and the experimentally obtained or expected propensity of dopants to surface accumulate in Si (a) and Ge (b).

COEVAPORATION *n*-TYPE DOPING

Sb-doping

As mentioned above, Sb is the favoured *n*-type coevaporation dopant on technological grounds, although it has a significantly lower solubility limit than P or As. Metzger *et al*[12] noted a strong tendency to surface accumulate, with residence times varying between 10 and 10⁵ seconds between 900 and 600°C. At high temperatures (> 750°C), good quality material at doping levels up to $\approx 5 \times 10^{17}$ cm⁻³ could be obtained employing reasonable Sb fluxes. Higher doping levels can be obtained, but due to the low sticking coefficients (< 1x10⁻³), extremely high Sb fluxes are required. Below $\approx 700^\circ\text{C}$, sticking coefficients rapidly approach unity, however, residence times are extreme (> 10⁵ seconds). In both regimes, doping levels above 5×10^{17} cm⁻³ result in degraded material quality[13], with mobilities approximately half of bulk values[12].

Achieving equilibrium Sb-doping at a given growth temperature occurs after equilibrium coverage of the surface is achieved, typically 2-3 times the residence time. Since these times are long even at high temperatures, introducing step changes in doping level requires a growth interruption while the desired Sb equilibrium coverage builds up. Similarly, to prevent continued doping when the Sb flux is stopped, the surface coverage needs to be removed by raising the substrate temperature to desorb the Sb. This method has been successfully applied to grow abrupt profiles[10,14], but it has the disadvantages associated with arresting growth, and requires complex and often long growth schedules.

The sticking coefficient of Sb at growth temperatures below $\approx 600^\circ\text{C}$ is essentially unity, but residence times exceed 27 hours(!) and equilibrium coverages approaching 1 monolayer disrupt epitaxial growth[12,13]. Jorke *et al*[29,30] have shown that a growth rate-dependent transition temperature exists ($\approx 530^\circ\text{C}$ at 0.1nm/s) at which the severe Sb surface accumulation seen at the higher temperatures changes from an equilibrium-limited to a kinetically-limited regime, characterized by a 10^3 increase in incorporation. Surface accumulation continues to decrease slowly, and only becomes negligible at temperatures $< \approx 200^\circ\text{C}$, at which point Si films may be amorphous. Annealing of such material causes solid state regrowth, and this technique (Solid Phase Epitaxy) has been successfully applied to grow Sb-doped epilayers at concentrations exceeding solubility limits, incorporating abrupt doping transitions[11]. Electrical activation is incomplete (0.3-0.8)[11,31] and material quality has not been carefully studied. Nevertheless, SPE has an important application in growth of δ layers.

More recently, Eaglesham *et al*[32] have shown that growth at these low temperatures does not inevitably lead to amorphous Si. At a given temperature, a limiting thickness, h_{epi} exists ($\approx 150\text{nm}$ at 325°C at 0.02nm/s growth rate) below which growth remains single crystal. Briefly annealing at 500°C for 100s to stabilize the material allows thick epitaxial structures to be built by repetition. Clearly this technique has promise, but, as with SPE, further investigations of material quality are required with respect to impurity incorporation and residual doping.

Potential Enhanced Doping (Doping by Secondary Implantation)

This method is a hybrid; although only thermal energies ($< 1\text{eV}$) are available from the coevaporated neutral dopant flux, incorporation is stimulated by provision of extra energy from ions, as with ion implantation during MBE (see below). Jorke *et al*[33,34] observed that increasing the number of Si^+ ions (using an ionization ring above the Si source), increases the incorporation of Sb. Since a small fraction of Si^+ ions are generated during electron beam evaporation anyway, the simplest method of implementing the technique (known as Potential Enhanced Doping - PED) is by application of a -ve potential to the substrate[14,23,24,33,34]. Fig. 3 shows the dramatic increase in doping level that can be achieved by PED as a function of potential, allowing doping levels up to the solubility limit ($\approx 3 \times 10^{19} \text{cm}^{-3}$) to be readily achieved[14,23,24,33,34] under surface coverage conditions corresponding to spontaneous doping levels of $< 10^{17} \text{cm}^{-3}$. Furthermore, since Sb surface coverages remain low, material quality is indistinguishable from low doped epilayers, as demonstrated in the bulk-like mobility data shown in Fig. 4.

A major strength of PED is in profile control[14,23,24]. Doping levels can be varied simply by changing potential to provide both controlled ramps and abrupt transitions, as illustrated in Fig. 5.

As with spontaneous incorporation, PED relies on the surface accumulation layer having reached equilibrium to achieve uniform doping levels, favouring use in the high temperature regime ($> 700^\circ\text{C}$). At lower temperatures, the long residence times and high

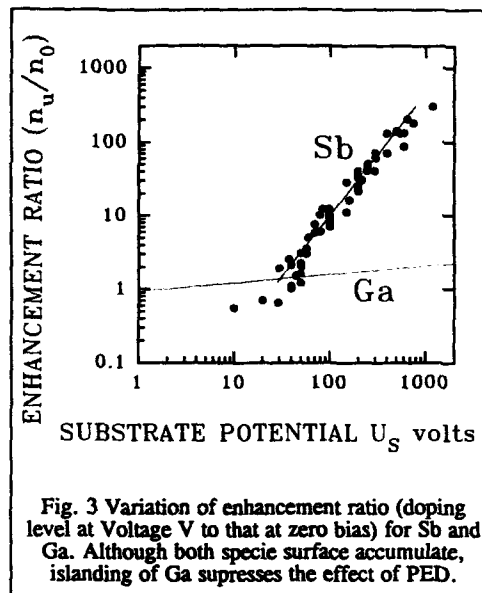


Fig. 3 Variation of enhancement ratio (doping level at Voltage V to that at zero bias) for Sb and Ga. Although both specie surface accumulate, islanding of Ga suppresses the effect of PED.

equilibrium coverages require pre-build of Sb, with the corresponding problems of material quality degradation and disruption to the growth process. A modified approach is to build-up to a level which does not effect material quality (e.g. 0.1 monolayers). This is sufficient to permit PED-assisted doping at high doping levels $> 10^{18} \text{ cm}^{-3}$ for most structure dimensions (100-500nm).

The mechanism for PED is not clear. Jorke *et al*[33,34] have proposed that incoming Si^+ ions knock Sb adatoms into the surface by direct interaction, however, preliminary calculations showed only weak correlation with the experimental results. Another possible mechanism[36] involves cracking of Sb-clusters which result in higher reactivity of monomers/dimers. Although the case for monomers cannot be categorically disputed, there was no observed difference in PED behaviour between incident Sb_4 (sublimed from the element) and Sb_2 (the dominant evaporant from an InSb compound source)[24]. Fritsch *et al*[37] simulated the experimental behaviour by performing dynamical atom block computations. These confirmed that indeed knock-in is a contributory factor, as is sputtering of the adlayer. However, the main contributory factor governing the observed enhancement behaviour was defect generation cause by cascade propagation by the Si^+ ions.

Two important questions arise in use of PED. Firstly, relying as it does, on processes occurring at the electron beam evaporator, the relationship between applied potential and enhancement ratio is likely to differ between evaporator types because the fraction of Si atoms ionized will depend on electron beam shape. Other factors such as chamber size, source/substrate spacing and source collimation are also likely to be influential, since they would affect the efficiency of Si^+ ion collection, and perhaps even their distribution across the substrate. Nevertheless, similar responses have been observed in several MBE systems.

The second question relates to reproducibility; again, the conditions at the source are likely to vary as the source depletes, and with incident electron power (energy and current), thus a variation in enhancement ration might be expected. However, we have found that provided reasonable procedures are followed (e.g. use

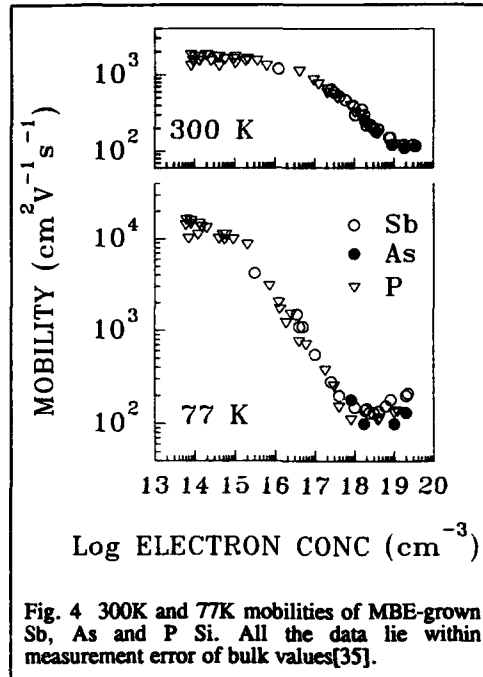


Fig. 4 300K and 77K mobilities of MBE-grown Sb, As and P Si. All the data lie within measurement error of bulk values[35].

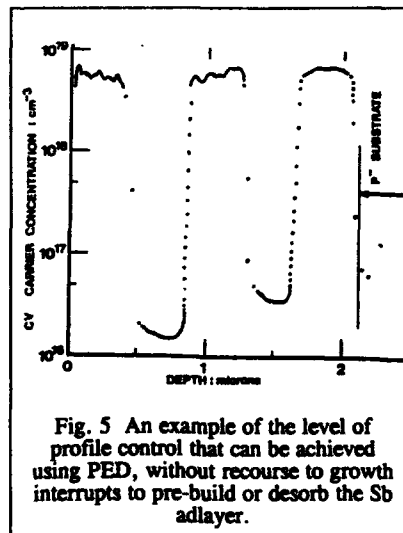


Fig. 5 An example of the level of profile control that can be achieved using PED, without recourse to growth interrupts to pre-build or desorb the Sb adlayer.

of beam scanning or a defocused beam, with occasional meltback to smooth the charge surface), reproducibility remains extremely good, as illustrated in Fig. 3, even with several replacements of Si charge.

Irradiation of an Sb-adlayer with 1- to 2-keV electrons also enhances incorporation during MBE growth by up to 100x. Delage *et al*[38] have used this technique to achieve high doping levels, and sharp doping transitions. The mechanism is not clear, though they suggest decomposition of surface Sb molecules into monomers results in improved ease of incorporation. As with PED, the surface concentration of Sb needs to be established prior to doping.

P- and As-Doping

The motivation behind use of P and As are there significantly higher solubility limits than Sb. Both elements have very high vapour pressures precluding use of the element, therefore compound sources have been used.

GaAs and InAs have been used as As doping sources[23,24], requiring evaporation temperatures $>400^{\circ}\text{C}$ to generate useable fluxes. Arsenic doping levels in the range 5×10^{16} and $2 \times 10^{19} \text{ cm}^{-3}$ were obtained, with bulk mobilities, see Fig. 4. However, at doping levels exceeding $5 \times 10^{18} \text{ cm}^{-3}$, material quality was found to degrade, possibly due to co-doping with significant quantities of the group III element (only factors of ≈ 5 -10 below that of the As). The response of As to PED was significantly weaker than for Sb, commensurate with a lower propensity to surface accumulation due to a smaller size. Unlike Sb, also, the enhancement ratio varied with surface coverage, possibly due to the influence of group III islands. Background doping gradually rose during the As-doping work from $<10^{15}$ to $\approx 10^{16} \text{ cm}^{-3}$.

A Sn-rich Sn_3P_4 charge was used for P-doping, having the advantage over GpIII-P compounds of a negligible Sn vapour pressure[28]. Carrier concentrations in the range 10^{16} to 10^{19} cm^{-3} were obtained, with bulk mobilities (Fig. 4). The complete lack of response to PED, and the ability to produce doping transitions indicated negligible surface accumulation, commensurate with its size[5]. Growth of P-doped material was accompanied by a high background pressure of P^{31} ($>10^{-7}$ mbar), which nevertheless recovered quickly after growth. This, and an anomalously low substrate temperature dependence of doping level suggests an extremely low sticking coefficient at the temperatures investigated (600 - 850°C), consistent with its high vapour pressure. This does suggest that choice of compound sources for P is important, since even the small vapour Sn flux may lead to relatively high co-doping. Although the MBE system was noticeably contaminated by P during subsequent growth of undoped material, the residual background level was comparable to after As doping ($\approx 10^{16} \text{ cm}^{-3}$), reflecting the lower sticking coefficient.

It would be interesting to use in the low growth temperature regime ($<200^{\circ}\text{C}$), since as with Sb, sticking coefficients will be high. Their higher solubility limits are likely to be more compatible with maintaining material quality after annealing.

COEVAPORATION B-DOPING

Despite the ease of evaporation of Ga, In and Al, the problems of surface accumulation, their low solubility limits and deep ionization levels, and lack of response to incorporation enhancement techniques such as PED (Fig. 3) has led recently to a gradual decline in their use. The reader is referred to refs 10 and 14, and references therein, for further detail. Another factor contributing to the demise in the use of Ga (In and Al) has been the rapid development of several different methods of circumventing the low vapour pressure of B.

B-doping from Compound Sources

Although, B as an element requires temperatures in the range 1400 - 2000°C to generate a usable doping flux, evaporation of B compounds such as HBO_2 and B_2O_3 [39-46]

provide fluxes at temperatures accessed by conventional effusion sources ($< 1300^{\circ}\text{C}$). Doping levels between 10^{16} and 10^{20} cm^{-3} have been reported.

Evaporation takes place as molecular species, requiring decomposition on the Si surface prior to incorporation. Tatsumi *et al*[40] noted a significant rise in oxygen incorporation from these B compounds at temperatures below 700°C . Lowering the growth rate provides a longer time for decomposition[42], and as expected, Lin *et al*[43,46] demonstrated a reduction in oxygen content at 0.02 nm/s compared with 0.1 nm/s . Nevertheless, at typical SiGe growth temperatures, $< 550^{\circ}\text{C}$, maximum oxygen free B-doping levels are $< 5 \times 10^{17}\text{ cm}^{-3}$, even at these reduced growth rates. With the advances being made with elemental B sources, it is the authors' opinion that compound sources will be restricted to high growth temperature applications.

B saturated Si sources

Ostrom and Allen[39] melted a Si charge in a pBN crucible to form B-saturated Si. Sublimation of this charge at temperatures below 1400°C , generated a flux capable of doping at $1 \times 10^{20}\text{ cm}^{-3}$. The evaporated Si:B flux ratio is $\approx 30:1$, thus contribution to the growth rate from the accompanying Si flux was negligible.

Kuznetsov *et al*[47] had previously used Si charges saturated with P, As, Sb and Al to grow doped Si from electron beam evaporators. The combined work of Ostrom and Kuznetsov to evaporate B-saturated Si from an electron beam evaporator has been applied by the groups at Philips[48] and IBM[49] to provide controlled B-doping, albeit over a limited range. This technologically complex method has the major benefit of indirect monitoring the B-flux by controlling the Si evaporation rate. An interesting question is whether such a source produces B atoms or SiB complexes which may modify (beneficially?) the incorporation behaviour, particularly at high doping levels.

Elemental B Evaporation

Methods of evaporating B from the element must meet two criteria: (i) providing a means of containment of the reactive B, and (ii) attaining temperatures as high as 2000°C without contamination of the flux. Crucibles of graphite, particularly if manufactured from or coated with pyrolytic carbon, have a very low vapour pressure, and are able to withstand B at high temperatures, thus meeting the first criterion. A variety of designs of high temperature sources have been reported to achieve the evaporation temperatures required. A conventional effusion source with very low thermal losses and W (rather than Ta) heater filaments is commercially available[50]. Andrieu *et al*[51] and Kibbel *et al*[52] have modified the effusion cell principle to allow the heater filaments to be biased at high voltage ($> -1000\text{V}$) compared with the crucible. The extra power required to attain temperatures above conventional effusion cell temperatures is thus supplied by electron beam heating. These methods have the facility for flux control via thermocouple feedback, as

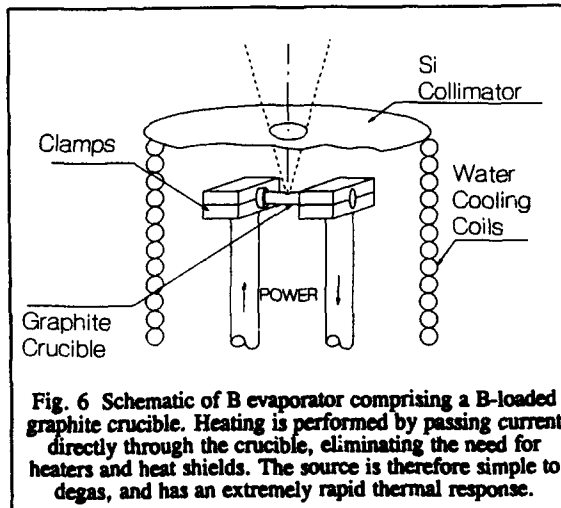


Fig. 6 Schematic of B evaporator comprising a B-loaded graphite crucible. Heating is performed by passing current directly through the crucible, eliminating the need for heaters and heat shields. The source is therefore simple to degas, and has an extremely rapid thermal response.

with conventional effusion sources. However, filament temperatures are very high and the extensive need for heat shields, etc. requires thorough outgassing if flux purity is to be maintained.

A simpler scheme[53], is illustrated in Fig. 6, in which a graphite tube crucible is directly heated by passing current. Crucible temperatures to achieve B-doping fluxes are comparable to those of the designs given above, but the absence of a subsidiary heater and surrounding heat shields ensures cleaner operation. Indeed, the source can be outgassed to UHV compatibility in < 5 min. Doping reproducibility is better than $\pm 25\%$ using a constant current ($\approx 100\text{-}180$ amps) calibrated against doping level.

Denhoff[54] has described an elegant B source which eliminates the need for a crucible and thus in principle will supply an extremely clean flux. A self-supporting boron rod is electron beam heated from a remote filament held at high voltage. Power to the boron can be varied either by controlling the emission current, or bias.

B incorporation behaviour in Si

Various studies have been conducted into characterizing the incorporation kinetics of B-doping from compound[40-43,55] and elemental sources[56-59]. The results from these diverse sources are *qualitatively* similar, therefore we concentrate only on results from the latter, which avoids problems of oxygen co-doping.

Fig. 7 summarizes the results in a "designer" chart of B-doping in Si as a function of growth conditions. 3 distinct operating regimes can be identified. Firstly, the thick solid line is the empirically established solid solubility limit of B in MBE Si at a growth rate of 0.28nm/s , i.e. the maximum amount of B that can be incorporated into Si at a given temperature[57]. B flux in excess of this limit accumulates on the surface, but only up to a limiting areal density of ≈ 0.25 monolayers[57,58]. As with large dopant atoms, this adlayer "floats" on the growing surface. On terminating the B flux, the adlayer acts as a reservoir, incorporating at the solid solubility level indicated, until the adlayer is exhausted. Attempts to increase the coverage above 0.25 monolayers results in inclusion of precipitates in the MBE material.

At growth temperatures exceeding 750°C , our data matches that of solid solubility limits established in bulk Si[57]. At temperatures below 750°C , a sharp upturn in solubility limit is observed. This corresponds to the transition from equilibrium to kinetically limited incorporation, as previously described for Sb by Barnett and Greene[16] and Jorke[29], albeit to a significantly smaller extent. Also as with Sb, the accumulation distance peaks at the transition between the two regimes. For quantitative data on B incorporation, and the influence of growth rate, the reader is referred to refs 56-58.

In summary, low resolution structures at doping levels below $\approx 5 \times 10^{18} \text{cm}^{-3}$ can be grown over the entire range of growth conditions. High doping levels and structures incorporating high resolution features (such as δ 's[59]) need to be grown at as a low

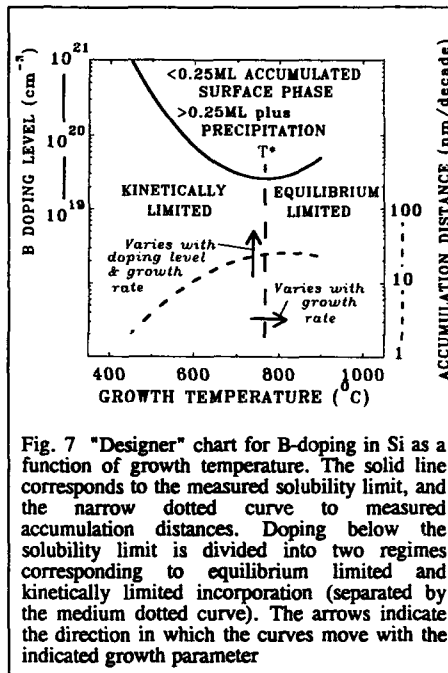


Fig. 7 "Designer" chart for B-doping in Si as a function of growth temperature. The solid line corresponds to the measured solubility limit, and the narrow dotted curve to measured accumulation distances. Doping below the solubility limit is divided into two regimes corresponding to equilibrium limited and kinetically limited incorporation (separated by the medium dotted curve). The arrows indicate the direction in which the curves move with the indicated growth parameter

temperature and high a rate as is consistent with achieving good material quality. Fig. 8 demonstrates that bulk mobilities are readily achieved over the entire doping range studied.

B-incorporation in SiGe

Despite increasing interest in *p*-type transport in SiGe structures [48, 60, 61, 62], and its importance for HJBT operation, there has as yet been little systematic work on the incorporation of B. Preliminary results by Parry *et al* [60] indicate that the kinetics of B-doping are compounded by the presence of compressive strain, and in addition to growth rate and temperature, Ge fraction is an important parameter. Fig. 9, for example, illustrates the differences in B incorporation in Si and $\text{Si}_{0.9}\text{Ge}_{0.1}$ over the temperature range 540°C to 650°C, discussed in more detail in ref 60. Consistent with Pindoria's size criterion [5], the presence of larger Ge atoms appears to reduce surface accumulation, as indicated by a gradual shift in the transition temperature from equilibrium to kinetically limited incorporation to lower temperatures, at a given growth rate. We may also expect a reduction in the peak accumulation distance with Ge content, and further work is in progress.

ION BEAM DOPING

Ion implantation during MBE growth potentially offers the most versatile choice of dopants (a wide variety of ion source-compatible materials is available), and the highest degree of accuracy by using simple dosimetry control. Ion implantation has been successfully applied with MBE to the main Si-industry standard dopants B, P, As and Sb [64-67], as well as Ga and In. The main constraints lie in selection of optimum energies at the growth conditions

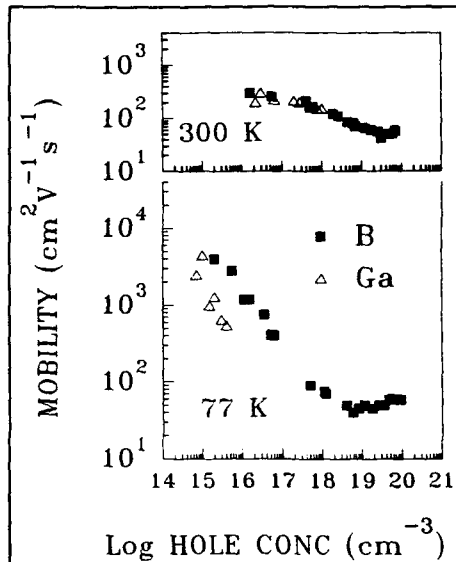


Fig. 8. 300K and 77K mobility of B-doped Si grown by MBE agree with bulk material data. Ga-doped material shows marked freeze-out at 77K, consistent with its deeper ionization level, and degraded mobilities. B mobilities are within measurement error of bulk values at both temperatures.

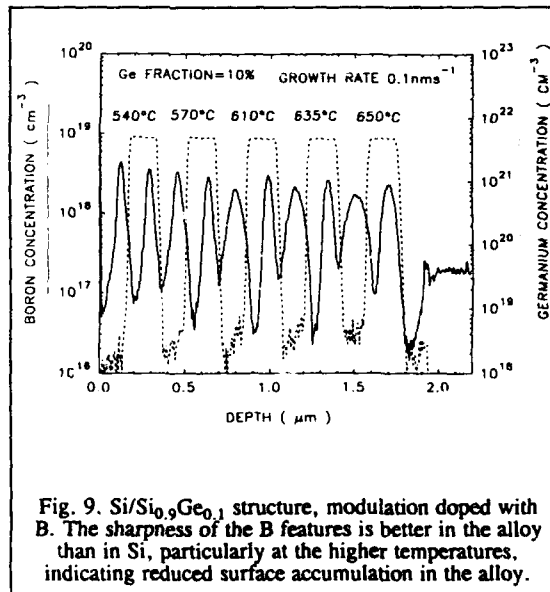


Fig. 9. $\text{Si}/\text{Si}_{0.9}\text{Ge}_{0.1}$ structure, modulation doped with B. The sharpness of the B features is better in the alloy than in Si, particularly at the higher temperatures, indicating reduced surface accumulation in the alloy.

employed. High resolution doping structures require accurate positioning of the dopant with a resolution of 1-10nm, limiting the energy of dopant ions to 100-1000eV (depending on species). Low energies are also more consistent with reducing damage, particularly important with the advent of reduced growth / processing temperature schedules. On the other hand, energies need to be kept as high as possible to ensure maximum incorporation efficiency and optimal control over ion flux distribution.

Two approaches have been employed. Firstly, conventional

effusion sources with a low efficiency Bayard-Albert style ionization chamber[64] at the orifice provide ion/neutral efficiencies of <5%. Providing non-line of sight between the source and the substrate with deflection plates ensures that only ions, and not neutrals, with their complex incorporation growth temperature-dependent characteristics, influence doping.

The second approach utilizes the technology of ion implantation interfaced to MBE, offering high beam purity, accurate dosimetry and high efficiency. Despite being as old as the Si:MBE technique[65-67], little systematic work has been reported. One reason for this is no doubt the relative complexity and cost of its implementation, another the lack of commercial equipment. Fig. 10 shows a schematic of a new source[68] currently under development, interfaced with a commercial MBE system. This implementation boasts ion energies from 1keV to 50eV[68] with ion currents of $50\mu\text{A cm}^{-1}$ (commensurate with a doping level of 10^{20} cm^{-3} for unity sticking coefficient). A normal incidence beam is used, rather than, for example 30° as used by Bean[66], since this offers improved control over flux scanning for uniformity over 150mm wafers. Doping resolution is not expected to be effected by use of normal incidence because of the large critical angles at these energies which almost guarantees some degree of channelling[68]. The lack of knowledge of ion interactions at these low energies is of importance to future success of this methods and is currently under detailed investigation[69].

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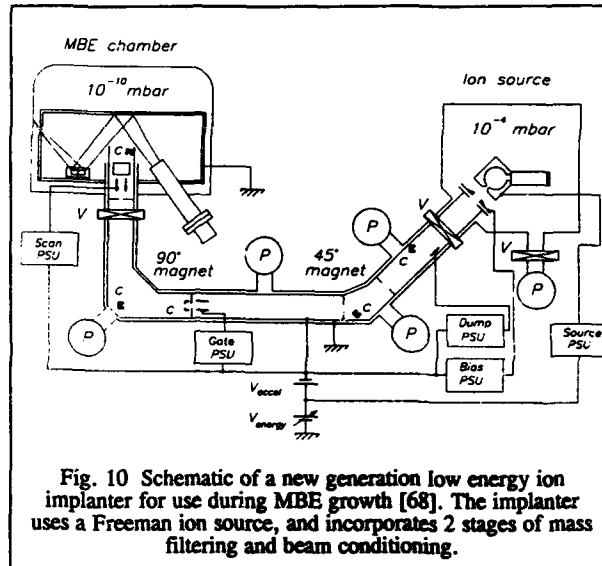


Fig. 10 Schematic of a new generation low energy ion implanter for use during MBE growth [68]. The implanter uses a Freeman ion source, and incorporates 2 stages of mass filtering and beam conditioning.

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**SCHOTTKY - BARRIER TUNNELLING SPECTROSCOPY OF Si:B
DELTA LAYERS**

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Delta doping in MBE has attracted considerable attention since its inception in 1980 [1], as a vehicle for studies of 2D phenomena and for its potential applications in, for example, FET devices [2] and I.R. detectors [3]. Boron delta doping in silicon is a recent development [4]. In previous papers we have reported on the growth, TEM, CV profiling, SIMS profiling and XRD characterisation of B delta layers [4,5,6]. It is of interest to know if the present growth method [4] produces a dopant sheet a monolayer wide or, in any event, what is the true width. Previous techniques [4,5,6] have yielded values between 0.4nm and 3nm for the width. Schottky barrier tunnelling spectroscopy provides further information on this question, but is also of interest for a study of the electronic structure of the delta layer. It has been used previously for a study of delta doping in III-V materials [7] and also for Sb delta doping in Si [8,9], but there have so far been no reports of its application to Si:B delta layers.

The present layers were grown on 1-2 ohm-cm n^- substrates after a silicon flux clean at 850°C. 0.4 μm of Si was deposited at a growth rate of 0.3 nm s^{-1} , the temperature being continuously lowered from 760°C to 480°C during this stage of growth. The Si flux was then interrupted and approximately $3 \times 10^{13} \text{ cm}^{-2}$ of B was deposited. Finally, the B cell was shuttered and growth of Si continued for a further 20 nm at 480°C. The residual doping level in the epilayer was in the range $10^{14} - 10^{15} \text{ cm}^{-3}$ and the areal density of dopant as deduced by SIMS was $2.8 (\pm 0.1) \times 10^{13} \text{ cm}^{-2}$, in good agreement with the intended value. Hall measurements at 293K yielded a carrier sheet density of $2.7 (\pm 0.2) \times 10^{13} \text{ cm}^{-2}$ and a mobility of $34 \text{ cm}^{-2} \text{ V}^{-1} \text{ s}^{-1}$.

For tunnelling measurements, ohmic contacts were made to the delta layer by sputtering of NiCr alloy which was then sintered for 10 minutes at 420°C. Ga/In alloy was then painted onto the untreated surface of the sample to form a Schottky contact, the native

oxide being intended to act as a diffusion barrier. The overall measurement configuration is shown in figure 1.

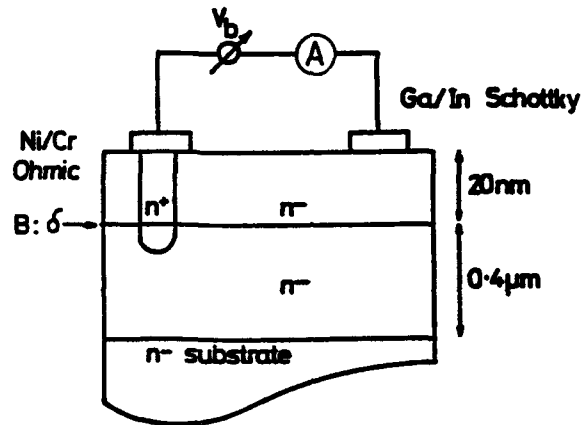


Fig 1. Experimental configuration for tunnelling measurements.

Figure 2 shows a typical I-V characteristic obtained at 4.2K, using a Hewlett-Packard HP414B Parameter Analyzer and voltage increments of 2mV.

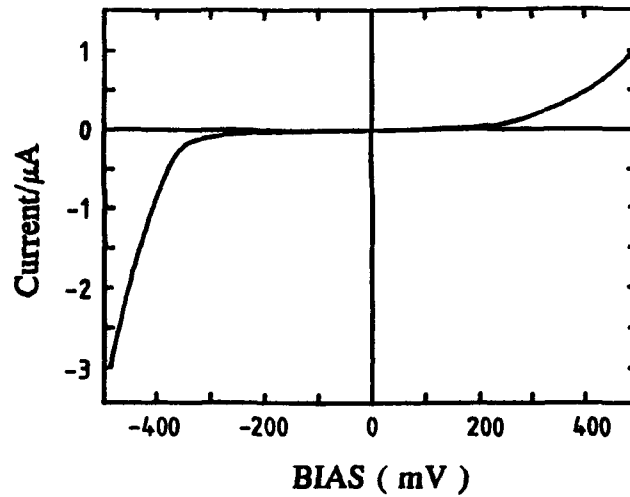


Fig 2. Typical I-V curve obtained in tunnelling experiments. Hole sheet density $3 \times 10^{13} \text{cm}^{-2}$.

It is well established that the tunnelling conductance (dI/dV) may be used to investigate the energy levels in a 2D carrier gas, peaks in the (dI/dV) versus V plot corresponding to subband minima. The results of figure 2 when differentiated and plotted against voltage display a number of peaks, as shown in figure 3. The normalized derivative curve, $(\frac{V}{I})(\frac{dI}{dV})$ which is more sensitive to the structure in the I-V plot, is also shown in figure 3.

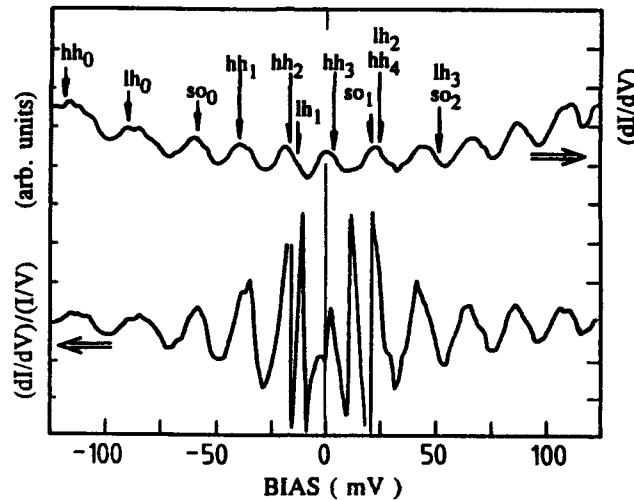


Fig 3. Typical conductance $(\frac{dI}{dV})$ and normalized conductance $(\frac{V}{I})(\frac{dI}{dV})$ curves obtained from measurements on boron delta layers of areal density $3 \times 10^{13} \text{ cm}^{-2}$. V is the potential on the Schottky electrode. The arrows represent the calculated energies of subband minima relative to the Fermi energy.

A finite difference method was used to solve Poisson's equation to obtain the potential, screening being included by assuming parabolic bands in 3D and Fermi statistics. Schrödinger's equation was solved for this potential using a transfer matrix approach to obtain the bound states in the well. The Fermi energy was then calculated from the measured carrier density and the staircase density of states function. Calculations were performed for a surface potential of 0V. It was also found that if the surface potential was varied by 1V the separations of the first four lowest lying hole-energy-states differed by not more than 6 meV over this range. The present method was also applied to electron energy levels,

compared with the self consistent calculations of Hui Min Li et al [9] for Si:Sb and good agreement was obtained. Calculated values of the heavy hole (hh) subband minima, light hole (lh) subband minima and spin split (so) subband minima are shown by arrows in figure 3. The agreement between observed and calculated subband minima is satisfactory for the examples shown. The possibility that the peaks on the right hand side of the figure also represent hole subband minima has not been tested because of the greater inaccuracy of the calculation at higher hole energies.

In conclusion, we have reported for the first time tunnelling studies of boron delta layers in silicon and have observed structure in the IV curve which has been used to measure the positions of subband minima in the 2DHG. Further work will be needed to demonstrate the sensitivity of the measured energy levels to the width of the doping distribution.

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AN INVESTIGATION OF BORON INCORPORATION IN SiGe MBE.

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ABSTRACT

The performance of many Si/SiGe devices, particularly those involving modulation doped quantum wells, will depend on the quality of the matrix and doping interfaces involved. These may be adversely affected by profile smearing of Ge and the dopant. A study of boron incorporation in SiGe, as a function of substrate temperature and Ge fraction, shows a marked difference in profile smearing for boron in Si and in the SiGe alloy. This is shown to be associated with a reduction in the temperature for transition from equilibrium to kinetically limited accumulation in the alloy.

INTRODUCTION

The emergence of elemental boron as the optimum p-type doping source in Si MBE can be attributed to its relatively well-behaved incorporation properties, especially at low substrate temperatures [1]. This temperature regime is unachievable with compound sources [2-4]. While some progress has been made in our understanding of boron doping in Si [1-9], the behaviour of boron in the $\text{Si}_{1-x}\text{Ge}_x$ system is largely uncharacterised. This is despite the importance of boron doping in the production of novel electronic devices made possible by Si and SiGe molecular beam epitaxy (MBE). These include for example the boron doped SiGe base of the heterojunction bipolar transistor [4,5]. Boron depth profiles in $\text{Si}_{1-x}\text{Ge}_x$ have been presented in the literature but no quantitative information on boron doping in $\text{Si}_{1-x}\text{Ge}_x$ has been published [5,10]. Tatsumi demonstrated that the tensile stress induced by boron doping could be compensated by compressive stress from Ge [2]. Incorporation kinetics are therefore expected to be complicated by the additional surface strain term induced by the Ge.

In this report we examine the degree of profile broadening of boron in $\text{Si}_{1-x}\text{Ge}_x$ for $0 < x < 25\%$. Incorporation parameters are given as a function of Ge fraction x and substrate temperature at a growth rate of 0.1 nms^{-1} . These are determined from the leading edge slopes of boron depth profiles obtained by secondary ion mass spectrometry (SIMS). Although SIMS has been used routinely in the assessment of doping profiles in Si, the use of the technique is relatively unproven for dopants in $\text{Si}_{1-x}\text{Ge}_x$. Hence incorporation parameters are obtained which circumvent some of the problems associated with the SIMS technique as applied to $\text{Si}_{1-x}\text{Ge}_x$.

EXPERIMENT

Layers were grown in a modified VG Semicon V90S Si MBE system on Si(100) substrates. Si and Ge fluxes were obtained from electron beam evaporators controlled using an adapted INFICON Sentinel III EIELS flux monitor. Temperatures were measured using an optical pyrometer with extrapolation of the temperature versus heater current curve for temperatures below 550°C . Boron and Ge depth profiles were obtained by secondary ion mass spectrometry (SIMS) using a commercial Cameca IMF-4F instrument. These results were obtained using a 4.5 keV O_2^+ primary beam at an angle of incidence of 43° . Profile smearing by ion beam mixing effects was found to be significant only for leading edge slopes of less than 2 nm/decade . Boron levels in Si were calibrated by comparison with an implanted standard profiled under the same conditions. Boron standards in $\text{Si}_{1-x}\text{Ge}_x$ are not

yet available so boron in Si implants were used to calibrate doping levels in $\text{Si}_{1-x}\text{Ge}_x$, the validity of which is discussed in the text.

RESULTS

Fig 1 shows a SIMS depth profile of a modulation doped structure, with 50 nm boron layers grown in $\text{Si}_{0.8}\text{Ge}_{0.2}$ and Si at temperatures of 650, 600 and 450°C, and at a rate of 0.1 nms^{-1} . The boron flux was increased by 20% in the $\text{Si}_{0.8}\text{Ge}_{0.2}$ regions to compensate for the increased growth rate. Growth was interrupted for 10 minutes during each substrate temperature change with a 75 nm Si cap added before commencing the next $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer. Finally a 100 nm Si cap was grown. The individual thicknesses of each Si and $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer was determined to be within 5% of that intended, precluding any change in SIMS erosion rate during the depth profile under these profiling conditions. It should be pointed out that the total thickness of this structure exceeded the metastable critical thickness achievable at this Ge fraction. Defect etch measurements revealed dislocations threading throughout the layer confirming that this structure had relaxed.

Comparison of boron SIMS profiles in Si and $\text{Si}_{0.8}\text{Ge}_{0.2}$ in Fig. 1 reveals two features. Firstly under the growth conditions used in this structure, dopant profiles are noticeably more abrupt in the $\text{Si}_{0.8}\text{Ge}_{0.2}$ alloy than in Si grown at the same temperature. This is seen most clearly at the growth temperature of 650°C. Electrochemical capacitance-voltage (E-CV) measurements qualitatively confirmed the difference in the degree of profile smearing observed in Si and $\text{Si}_{0.8}\text{Ge}_{0.2}$ and indicated complete activation of boron in Si and $\text{Si}_{0.8}\text{Ge}_{0.2}$ consistent with our earlier work on the temperature dependence on boron solubility in Si MBE [1]. Secondly the areal density of boron spikes are lower in $\text{Si}_{0.8}\text{Ge}_{0.2}$ than in Si over the complete temperature range by about 60%. This is caused by a difference in boron ion yield (a measure of how efficiently

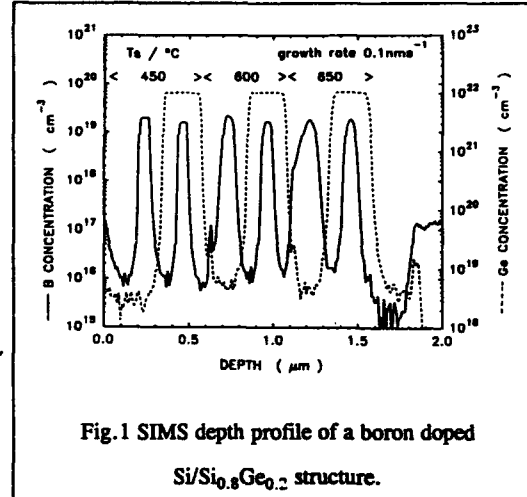


Fig. 1 SIMS depth profile of a boron doped $\text{Si}/\text{Si}_{0.8}\text{Ge}_{0.2}$ structure.

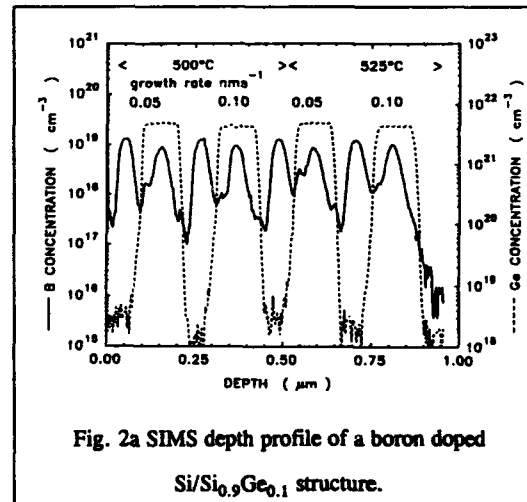


Fig. 2a SIMS depth profile of a boron doped $\text{Si}/\text{Si}_{0.9}\text{Ge}_{0.1}$ structure.

boron ions are sputtered by the primary beam) between Si and the $\text{Si}_{0.8}\text{Ge}_{0.2}$ alloy. It should be noted however that a difference in boron ion yield cannot cause an apparent increase in profile abruptness, since profile abruptness is defined as the growth distance for the observation of a fixed change in doping concentration. For this reason the profile broadening parameter Δ , defined as the exponential decay constant in the doping transient, was used to quantify the degree of profile broadening in Fig.1. Hence the non-availability of calibrated boron SIMS standards in $\text{Si}_{0.8}\text{Ge}_{0.2}$ did not contribute to a systematic error in the experiment.

Further modulation doped structures were grown to determine the temperature dependence of boron profile smearing in Si and $\text{Si}_{1-x}\text{Ge}_x$, at a growth rate of 0.1 nms^{-1} . Most structures of interest require strained $\text{Si}_{1-x}\text{Ge}_x$ heterojunctions as the active part of the device. Since incorporation of boron in strained and unstrained $\text{Si}_{1-x}\text{Ge}_x$ may be different, subsequent structures were grown with 10% Ge ensuring that they were fully strained.

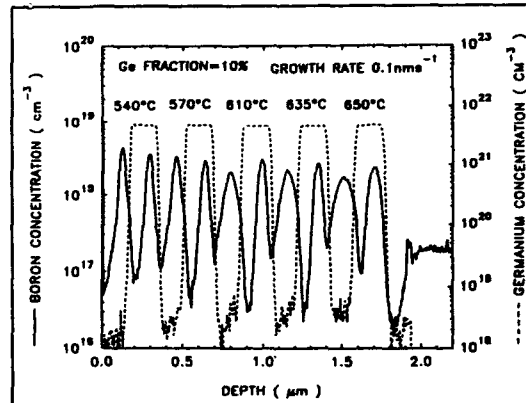


Fig. 2b SIMS depth profile of a boron doped $\text{Si}/\text{Si}_{0.9}\text{Ge}_{0.1}$ structure.

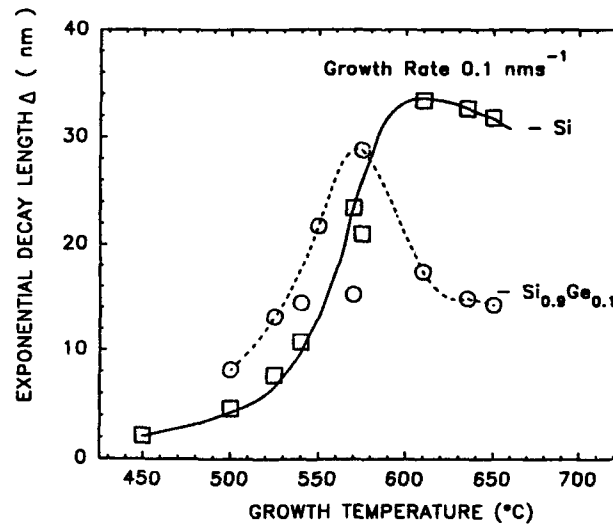


Fig. 3 Plot of the boron profile broadening parameter against temperature for the structures in Figs. 2a and 2b.

Figs 2a and 2b show boron and Ge SIMS depth profiles for boron doped layers grown under conditions indicated in the diagrams. In Fig. 2a boron profile smearing is significantly worse in the 10% alloy, for the boron doped layers grown at 525 and 500°C at 0.1 nms^{-1} . In Fig. 2b, however, for temperatures above 600°C this situation is reversed leading to more abrupt doping profiles in the 10% alloy. Fig. 3 shows a plot of boron decay lengths, in the SIMS leading edge slopes, against growth temperature using data obtained from the structures in Figs. 2a and 2b. The line through the $\text{Si}_{0.9}\text{Ge}_{0.1}$ plot is drawn only to guide the eye. The disparity in incorporation behaviour at a given temperature is clearly evident and reflects a genuine difference in profile smearing for boron doped layers grown Si and $\text{Si}_{0.9}\text{Ge}_{0.1}$ under otherwise identical conditions.

To determine any dependence of Ge fraction on boron incorporation further structures were grown, at a fixed growth rate and temperature, shown in Figs. 4a and 4b. These feature boron spikes grown in $\text{Si}_{1-x}\text{Ge}_x$ for $0 < x < 25\%$, and were grown at temperatures of 550 and 510°C respectively. Shown in Fig. 5 as a plot of boron profile broadening parameter against Ge fraction for the structures in Figs. 4a and 4b. For the structure grown at 550°C (Fig. 4a) a maximum is observed at a Ge fraction of $\approx 5\%$. Under these conditions the leading edge slope in the boron spike is not well defined making its determination difficult, although this in itself is evidence of strong profile smearing under these growth conditions. This however was a first attempt, a more satisfactory structure would feature thicker boron spikes, to allow steady state incorporation to be reached, and a wider spacer layer for a better determination of the leading edge slope. For the structure grown at a lower temperature, 510°C, any dependence of profile smearing of boron on Ge fraction is less noticeable, although some improvement is discernible in the 25% alloy. It should be noted that the values of Δ at 10% in Fig. 5 can be compared with those obtained from the $\text{Si}_{0.9}\text{Ge}_{0.1}$ Δ versus temperature plot in Fig. 3 the significance of which is discussed later.

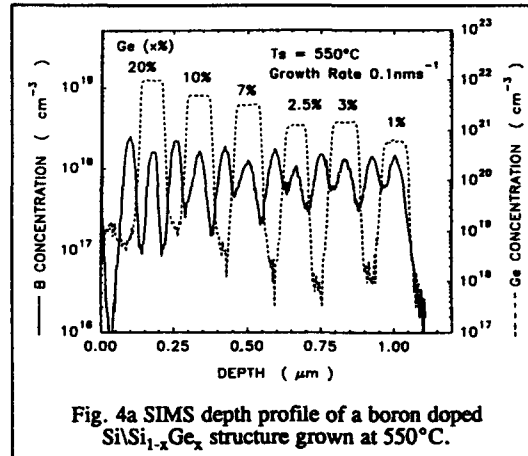


Fig. 4a SIMS depth profile of a boron doped $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ structure grown at 550°C.

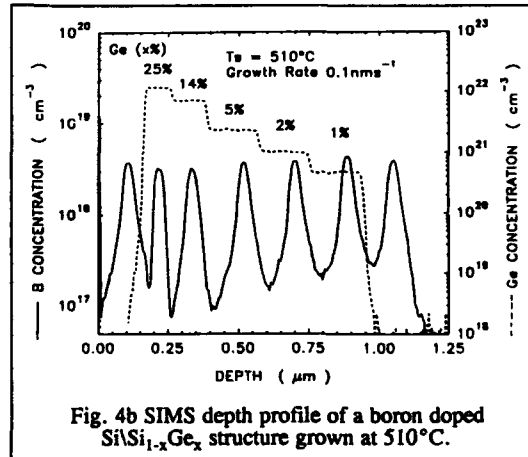


Fig. 4b SIMS depth profile of a boron doped $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ structure grown at 510°C.

DISCUSSION

The contrast in incorporation behaviour of boron in Si and $\text{Si}_{0.9}\text{Ge}_{0.1}$ can be characterised by an apparent difference, for the two matrices, in the transition temperature for which the processes causing profile smearing become kinetically limited. The reduction in temperature at which boron undergoes this transition is Ge fraction dependent, at any given growth rate. Under equilibrium incorporation conditions ($>570^\circ\text{C}$) boron profile broadening is significantly reduced in the alloy due to stress compensation by the Ge.

Profile smearing is observed when impurity species are indisposed to incorporation into the growing layer, so that some dopant remains on the surface. When a dopant flux is terminated any flux that has accumulated on the surface incorporates leading to profile smearing. This behaviour has previously been referred to as a segregation process. In fact segregation is a term more suitably applied to the separation of impurities from bulk phases in binary alloys [11]. For this paper we use the term surface *accumulation* to describe this effect, since it is not specific to any model, and for the purposes of this work the two words are interchangeable. It is well known that surface accumulation processes are growth rate and temperature dependent [11-15], since dopant accumulation is caused by diffusion effects occurring at or near the surface. The fundamental driving force for accumulation is the stress induced by the incorporation of dopants which have different covalent radii to the matrix species [11]. Different accumulation mechanisms [12-14] are not discussed in any detail here, but the work of Greene *et al* [13], later developed by Jorke [14] identified two important temperature regimes for accumulation. These are the 'equilibrium limited' and the 'kinetically limited' regimes. Accumulation in the high temperature equilibrium regime can be modelled by equilibrium thermodynamics since diffusion rates at or near the surface are much greater than growth rates allowing dynamic equilibrium to be established. Under such conditions accumulation would increase without limit for decreasing temperature, but in practice the presence of an energy barrier kinetically limits accumulation at low temperatures. This is the so-called kinetically limited regime, characterised by an abrupt decrease in accumulation below the transition temperature T^* , with a corresponding improvement in profile abruptness. T^* for a given dopant in Si is growth rate dependent since reductions in growth rate allow more time for accumulated flux to reach equilibrium with dopant in the bulk, thus extending the equilibrium regime to lower temperatures [13-15]. T^* is also species dependent since different dopant species will experience different energy barriers to the incorporation process [11, 13-15]. What is of interest in this work is how a change of *matrix*, eg Si and SiGe, affects accumulation processes for a given dopant.

Referring to Fig. 3, the complex accumulation behaviour in Figs. 2a and 2b is observed as a difference in transition temperature for boron accumulation in Si and $\text{Si}_{0.9}\text{Ge}_{0.1}$ alloy. The difference in T^* for a Ge fraction of 10% is about 40°C at this growth rate. At or near the Si transition temperature of 600°C profile broadening for boron in Si is at its maximum but profile broadening in $\text{Si}_{0.9}\text{Ge}_{0.1}$ is still in its equilibrium limited regime, making boron profiles significantly more abrupt in the alloy than in Si. At

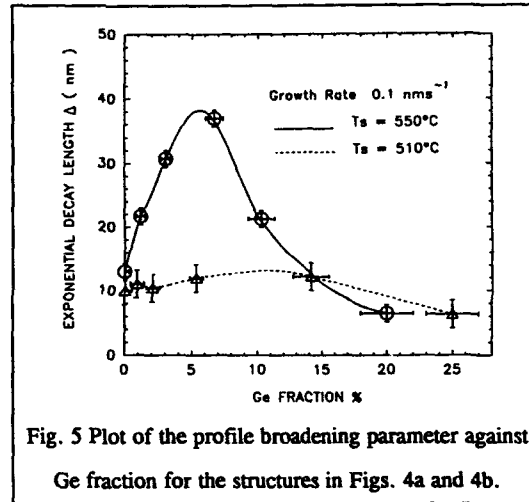


Fig. 5 Plot of the profile broadening parameter against Ge fraction for the structures in Figs. 4a and 4b.

a lower growth temperature, eg 575°C, this situation is reversed with accumulation broadening reaching its maximum in the alloy.

The mechanism by which the coevaporation of Ge decreases T^* can be related to empirical observations of accumulation behaviour of different dopants in Si and III-V systems [11]. Pindoria *et al* established that the greater the deviation of the ratio of the dopant/matrix radii differs from unity, the more likely the dopant will surface accumulate. The change of matrix induced by coevaporation of Ge effectively alters the dopant/matrix radii such that boron accumulation becomes energetically less favourable. If boron atoms can find a neighbouring Ge site they are much less likely to surface accumulate because of compensatory strain of the two species. Hence incorporation of both as a pair becomes energetically more favourable, reflected by the reduction of boron accumulation in the alloy in the equilibrium temperature regime. However there is likely to be a greater kinetic barrier to incorporation of both as a pair perhaps explaining the discernible increase in accumulation in the alloy in the kinetically limited regime.

The transition temperature, at any given growth rate, for a $\text{Si}_{1-x}\text{Ge}_x$ alloy is likely to be Ge fraction dependent. Initial results suggest that this difference increases with increasing Ge fraction. Fig. 5 shows that increasing the Ge fraction at constant temperature varies the position of the Δ versus temperature curve (see Fig. 3).

CONCLUSIONS

The effect of Ge on the incorporation of boron has been investigated using SIMS depth profile to determine the degree of profile broadening as a function of growth temperature and Ge content. From this initial study we deduce that boron accumulation in $\text{Si}_{0.9}\text{Ge}_{0.1}$ is significantly less than in Si, in the equilibrium regime ($>600^\circ\text{C}$ at 0.1 nms^{-1}). This is thought to be due to a favourable change in the ratio of the covalent radii of the dopant/matrix species.

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OBSERVATION OF INTERSUBBAND ABSORPTION IN BORON δ -DOPED Si LAYERS

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ABSTRACT

Strong hole intersubband infrared absorption in δ -doped Si multiple quantum wells is observed. The structures consist of 10 periods of boron doped Si quantum wells and undoped Si barriers. Near 100 % infrared absorption is measured by FTIR spectrometer using waveguide structures. Absorption peaks ranging between 3-7 μm are measured, and these peaks can be tuned by varying the doping concentration in the δ -doped layer. Polarization dependence has been verified to agree with the intersubband selection rule. The estimated peak energy positions using a self-consistency calculation are considerably lower than experimental values, probably due to a large exchange energy of many body effects. This observation suggests multiple quantum well IR detectors using Si- technology.

INTRODUCTION

Intersubband absorption in quantum well structures has drawn a considerable interest for potential far infrared detector applications. Intersubband infrared detectors have advantages of wavelength tunability, high detectivity and possible monolithic integration of electronics device for on-chip signal processing. Recent advance in silicon molecular beam epitaxy (Si-MBE) made it possible to demonstrate intersubband absorption in Si based heterostructures. For example, hole intersubband absorption in GeSi/Si multiple quantum wells [1], and electron intersubband absorption in antimony (Sb) δ -doped Si quantum wells [2] have been observed. More recently, we have reported intersubband absorption in boron δ -doped Si multiple quantum wells [3]. In this paper, details of further experimental results and theoretical calculations of intersubband infrared absorption in boron δ -doped Si multiple quantum wells will be discussed. The infrared absorption spectra are obtained by Fourier transform infrared spectroscopy (FTIR). Due to the large solid solubility of boron in Si, extremely sharp and high doping profiles (more than two orders of magnitude higher than that in GaAs) are obtained. This high doping capability results in high absorption strengths comparable or higher than those observed in GaAs/AlGaAs multiple quantum wells [4, 5]. The resonance transitions are shown to be tunable as a function of dopant density in the well. Integrating IR detectors using this δ -doping structures with the current Si technology can bring forth new directions and applications in optoelectronics.

EXPERIMENTAL

The samples used for this study are grown in a Si-MBE system and boron doping is achieved by thermal evaporation using a high temperature effusion cell [6]. Si wafers are chemically cleaned by Shiraki method prior to loading to the system, and thermal cleaning

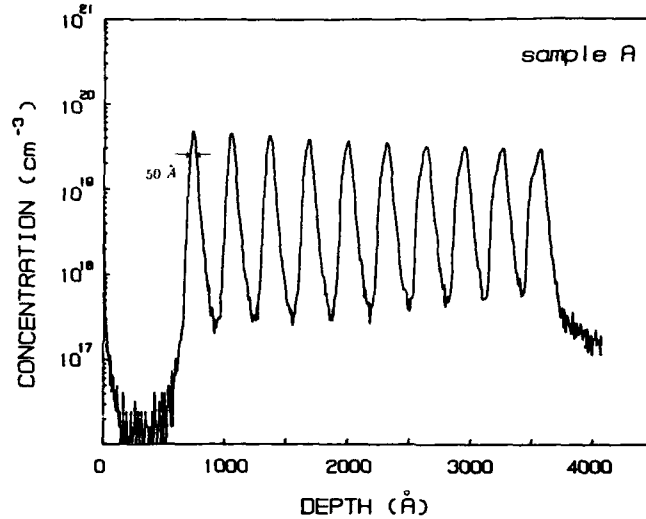


Figure 1: A typical SIMS profile of δ -doped sample (sample A). It reveals 10 periods of boron δ -doping Si layers with a FWHM of about 50 Å. The ion beam used in the analysis is a 2 keV O_2^+ incident at 60° angle with respect to the surface normal.

at 900 °C is followed *in-situ* in the MBE system. The substrate temperature is maintained at about 540 °C during the growth. The structures are grown on a high resistivity (100 Ω -cm) Si(100) substrates in order to reduce the free carrier infrared absorption within the substrate. The structure consists of an undoped Si buffer layer, followed by 10 periods of 35 Å of heavy boron-doped Si layers and 300 Å of undoped Si spacers. Four samples (A, B, C and D) with doping concentrations of about 0.7, 3, 4 and $7 \times 10^{20} \text{ cm}^{-3}$, respectively are prepared to study the subband energy and the absorption strength dependences of doping concentration. The doping density is measured by spreading resistance measurement and secondary ion mass spectrometry (SIMS).

SIMS depth profiles of the boron concentration are obtained on a Cameca/Riber MIQ 156 using a 2 keV O_2^+ primary ion beam at approximately a 60° angle of incidence with respect to the surface normal. These conditions are chosen based on the work reported by Schubert *et al.* [7], as a method of measuring the sharpest possible δ -doped profile while minimizing both sputter induced roughening and cascade mixing of the sample during SIMS analysis. Quantitation of the boron ion counts is obtained using a relative sensitivity factor derived from a known boron dose in a silicon implant. Sputter time is converted to depth based on a Dektak measurement of the final SIMS crater. Figure 1 shows the SIMS depth profile for a typical boron δ -doped sample (sample A). A full width at half maximum (FWHM) value of approximately 50 Å is measured from this profile for the B δ -doped layer closest to the surface. This value is typical of all such structures used in our study.

The absorption spectra of the samples are measured at room temperature using a Nicolet 740 Fourier transform infrared spectrometer. To enhance the absorption strength, a waveguide structures of 5 mm long and 0.5 mm thick are made by polishing a 45° angle wedge on both edges of the substrate (see inset of Fig. 2). The details of the measurement can be found elsewhere [3].

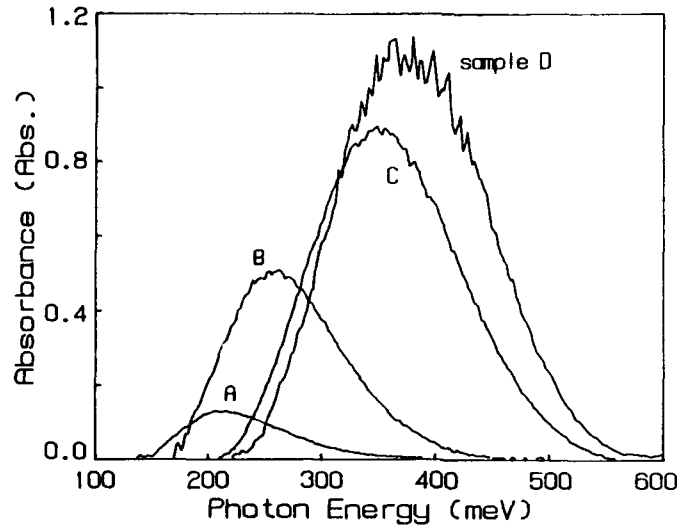


Figure 2: Absorption spectra of the four samples as a function of photon energy at 300 K. The sets of curves are due to different doping concentrations.

RESULTS AND DISCUSSION

The measured absorption spectra of the samples as a function of the photon energy are shown in Fig. 2. Absorption peaks shift toward higher energy as the doping concentration increases. Peak positions are found at near 200, 260, 360, and 380 meV with absorbance strengths of about 0.14, 0.51, 1.05, 1.17 Abs for 10 periods, for sample A, B, C and D, respectively. The measured peak absorption strengths are comparable or larger than that reported for GaAs/AlGaAs quantum wells [5] (1.3 Abs for 50 periods MQW). Such an enhancement is mainly due to the high doping level achievable in Si as compared with GaAs. The width of the absorption peaks are more than an order of magnitude larger than that observed in GaAs/AlGaAs quantum well structures (typically about 10 meV). Similar broad intersubband peaks due to electrons have also been observed in δ -doped layers in Si [2] and in GaAs [8] as well as holes in SiGe/Si multiple quantum wells [1]. The non-parabolicity of the hole bands can play a strong role in the broadening of the absorption peaks. In particular, at high doping levels, the hole bands can be filled up to several hundreds of meV, causing the holes to occupy states away from the Γ -point. This can partially be responsible for the increasing peak width as the doping concentration is increased. To further confirm the nature of intersubband transition, Fig. 3 shows the relative absorption spectra of the sample C as a function of polarization angle ϕ , where 0° corresponds to the s polarization and 90° for the p polarization (see inset of Fig. 2). The reduction of absorption strengths with the polarization angle ϕ as shown in Fig. 3 is a well-known feature of intersubband transitions. Similar polarization dependence is also observed for the other samples.

To understand the obtained data, in particular the variation of peak positions as a function of the 2D hole density in the wells, the subband energies are estimated by a self-consistency calculation (Hartree approximation). In the calculation, we assumed that the doping is uniformly distributed over a 35 Å layer of Si. The calculated potential well

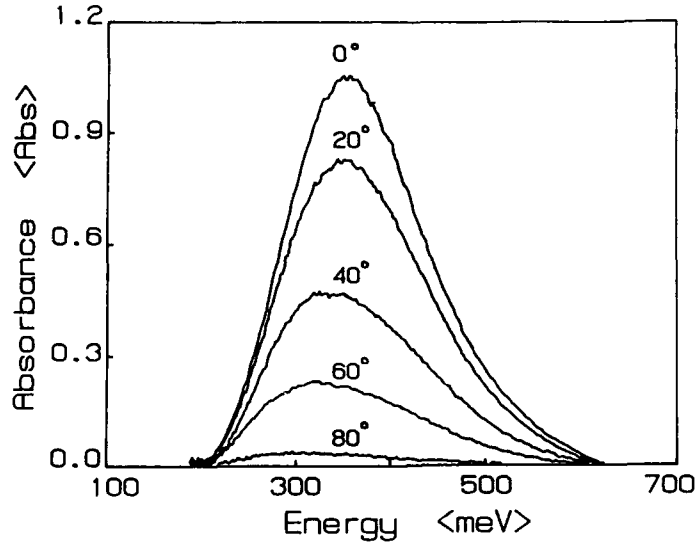


Figure 3: Polarization dependent absorption spectra of the sample C at 300K. The decrease of the absorbance with increasing polarization angle is seen.

and the wave functions of the subbands for sample C are shown in Fig. 4. In this figure, the hole energy is taken to be positive for convenience. The contribution due to the light hole is taken into account by combining the light hole density of states with the heavy hole density of states. For simplicity, we neglect the splitting of the light and heavy hole states due to the quantization with different masses. The heavy hole effective mass of 0.3 along the Si (100) direction is used for the subband energy calculation and the average density-of-states effective mass of 0.4 and 0.15 for the heavy and light holes in [100] plane is used to estimate the occupancy of subbands. The shape of the potential near the center deviates from that of an ideal δ -doping due to the finite width of the doping distribution [9]. Figure 5 shows the measured transition energy (dashed curve with open circles) and calculated values using the Hartree approximation. There is a considerable discrepancy exists between calculated and measured values. This discrepancy is believed to be due to many-body effects associated with the heavily populated subbands. A preliminary estimation of the many body effect, mainly the hole-hole exchange interaction, shows a considerable improvement of the calculated values. The calculated ground state lowering due to the hole-hole exchange interaction is of the order of 100 meV. Details of calculation including the exchange will be published elsewhere [10].

CONCLUSION

The intersubband transition in the δ -doped Si layers has been observed. By using heavy boron doping in Si by MBE, we have fabricated δ -doped Si layers with near 100% infrared absorption. High absorption which exceeds the value reported for the GaAs/AlGaAs quantum wells has been observed. The absorption strength can be further increased by increasing the number of quantum wells. In addition, the peak wavelength can be engineered by adjusting the concentration of dopants in the δ -doped layers. The polarization dependent absorption strength strongly suggests that the transitions are between

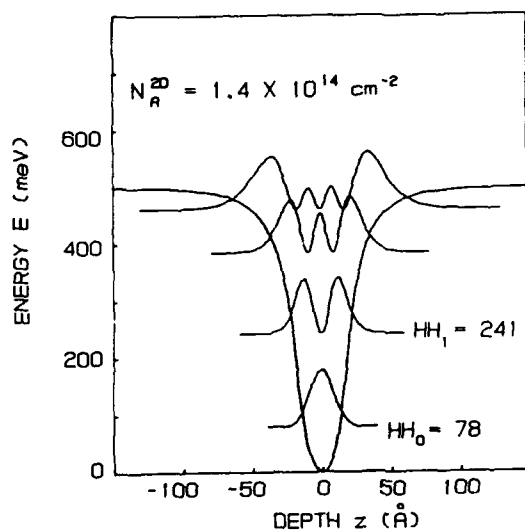


Figure 4: Calculated potential well and subband wave functions for sample C using Hartree approximation. In this calculation only the heavy hole band is considered.

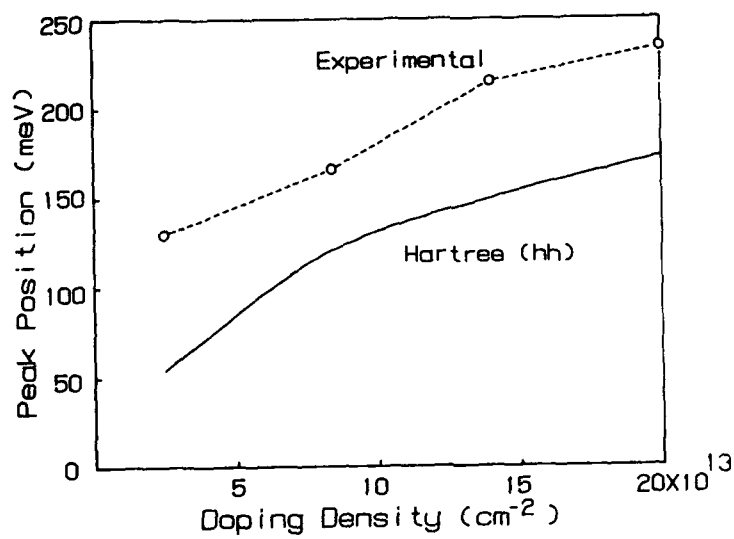


Figure 5: Subband separation as a function of doping density: (a) dashed curve with open circles from the experimental observation and (b) solid curve from self-consistency (Hartree approximation) calculation.

two hole subbands. The calculated subband separations by the Hartree approximation are lower than the experimental values, but can be improved by incorporating the exchange effect. The δ -doped structures can be directly applied for the fabrication of IR detectors and modulators. Monolithic integration of these devices with Si integrated circuits will provide a new direction in the optoelectronics.

ACKNOWLEDGEMENT

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EXPERIMENTAL AND MODEL STUDIES OF DOPANT SEGREGATION DURING GROWTH OF SILICON FILMS BY MOLECULAR BEAM EPITAXY

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ABSTRACT

Dopant incorporation and surface segregation are studied for thermal Sb and Al cases. The values of the incorporation probability and the segregation ratio have been mainly determined by SIMS measurements. The doping kinetics is discussed using a multi-site model including high dopant surface coverage effects. The calculated results were in good agreement with experimental data.

INTRODUCTION

Dopant surface segregation during growth, which is observed for most dopants used in silicon molecular beam epitaxy (Si-MBE) including As [1], Sb [2], Al [3,4], Ga [5] and In [6], results in surface accumulation during growth of doped layers and a low and strongly temperature-dependent dopant incorporation. Furthermore, when the dopant flux is interrupted, the high surface coverage of dopant atoms will be incorporated into later grown layers, and thus smear out the desired profile.

The physical origin of dopant surface segregation is, however, still not completely understood. It has been noticed that dopant surface segregation usually arises in cases where there is a significant size difference between dopant and Si atoms [7], which in turn results in strong lattice strain. The bond-strength difference between Si-dopant and Si-Si bonds, as well as static Coulomb interactions [8] also contribute as driving forces for surface segregation.

In order to overcome this problem, other doping techniques involving accelerated ions or solid phase epitaxial (SPE) regrowth have been developed. Especially, by using low-energy ion doping, ($E_{ion} \leq 400$ eV) a unity incorporation probability of dopants can be obtained over a wide temperature range ($T_s \leq 850$ °C) [9,10], due to a strong suppression of the surface-segregation. Thus, for low-energy ion beam doping virtually any desired doping profile can be obtained.

In this paper, experimental as well as theoretical studies of surface segregation mechanism during Si-MBE have been carried out. Two important parameters, incorporation probability σ and segregation ratio r , were experimentally determined, for thermal Sb doping, using SIMS measurements in combination with *in situ* AES measurements. Calculations using a multi-site model including high surface coverage effect were in good agreement with experimental results.

EXPERIMENTALS

The doped Si samples were prepared in a VG V-80 Si-MBE system. The procedures for sample cleaning, growth, and doping have been described in detail elsewhere [9]. In order to determine the segregation ratio, modulation doped films were studied by second ion mass spectroscopy (SIMS) in combination with newly developed concentration transient method [11]. *In situ* Auger electron spectroscopy (AES) was also used after quickly cooling the samples at the end of doped layer to ambient temperature to determine the dopant surface coverage Θ_d . Fig. 1 shows a SIMS profile, obtained using above-mentioned method, of a Sb doped Si layer. As is shown from this figure, a very high surface concentration peak and the gradual build-up of bulk doping concentration exist in the profile. Integration of the concentration transient

gives an estimate of Θ_d . The dopant incorporation probability σ and the segregation ratio r are also experimentally determined from the SIMS profile.

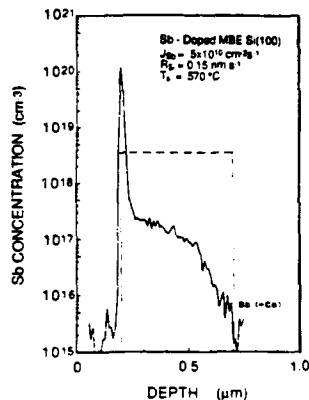


Fig. 1 SIMS depth profile from an Sb doped structure (thermal evaporation) prepared using a temperature modulation doping method. The gradual build-up of bulk doping concentration and the surface concentration peak due to the segregation process are clearly revealed in the spectrum. The dashed line indicates the desired profile assuming $\sigma=1$

BASIS FOR A MULTI-SITE MODEL TO DESCRIBE DOPING KINETICS

The model discussed here is an atomistic approach, and its formulation has been previously described in detail in ref. 9. The model has been applied to Sb doping using both thermally evaporated and a low-energy accelerated antimony beams during MBE-Si growth. Fig. 2 shows a schematic representation of the potential diagram for dopant atoms in the near surface region of a 2×1 reconstructed Si(100) surface.

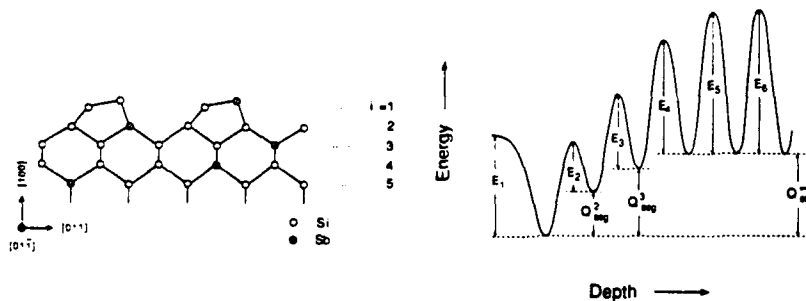


Fig. 2 Schematic representation of the energy of a dopant atom as a function of depth within a Si(100) 2×1 reconstructed layer. The different energy values E_i correspond to different subsurface sites, and Q_{seg} is an energy term accounting for the segregation driving force.

As has been shown from RHEED oscillation and STM studies, MBE growth is a quasi two-dimensional process. The growing layer is delimited by steps and the growth surface contains a number of kinks and ledges. In analogy with the growth model for Si, dopant incorporation can be described by incorporation at kink sites via surface diffusion. When dopant atoms impinge on the surface, they are first adsorbed on the surface, and then diffuse towards steps and kinks. As one Si layer is completed, dopant atoms have a strong bonding within the first layer. However, when this layer is overgrown with the next Si-layer the likely lone pair orbital on the Sb atom cannot bond to Si atoms. We propose that instead a kinetically limited exchange process occurs with a low energy barrier

(E₂) allowing the Sb atom to continue to be a surface atom. At the same time, the rate, at which the dopant atoms move back to the surface, competes with the growth rate of the epitaxial layer, i.e. the film growth rate kinetically limits such a segregation process.

Furthermore, theoretical studies [11] have shown that the formation of surface dimers can perturb the bonding energy down to layer 4. Both ion scattering experiments [12] and molecular dynamic simulations [13] have also indicated that there are substantial distortions of atom positions in the near surface region. Therefore, it is reasonable that the above formalism can be extended to a gradual diffusion barrier height variation from the first few atomic layers to the bulk.

Following the above discussion and the potential diagram in Fig. 1, the dopant incorporation in the *i*th layer can be directly described by a set of differential equations for a first-order process with the assumption of a low concentration of dopant atoms,

$$\frac{dX_1}{dt} = J_{d,1} - J_{des} - J_{1,2} + J_{2,1} - F_{1,2}, \quad (1a)$$

$$\frac{dX_i}{dt} = J_{d,i} + J_{i-1,i} - J_{i,i-1} + J_{i+1,i} - J_{i,i+1} + F_{i-1,i} - F_{i,i+1} \quad (1b)$$

$$\frac{dX_m}{dt} = J_{d,m} + J_{m-1,m} - J_{m,m-1} + F_{m-1,m} - F_{m,m+1} \quad (1c)$$

where indices $i=1,2,\dots,m$ indicate the number of successive layers below the surface, X_i is the dopant density which has been normalized to the total density of atomic sites in layer *i*. $J_{d,i}$ is the incident dopant flux to layer *i*, which in case of the thermal evaporation doping, $J_{d,1}=J_d$, $J_{d,i}=0$ ($i=2,\dots,m$). J_d is the total measured impinging dopant flux. For ion beam doping, the depth distribution of $J_{d,i}$ is approximated by a Gaussian function, and J_d is equal to the sum over $J_{d,i}$. J_{des} , $J_{i,i+1}$ and $J_{i+1,i}$ are desorption and the atomic exchange fluxes, respectively,

$$J_{des} = K_{des} X_1 = v_s X_1 \exp\left(-\frac{E_1}{kT_s}\right), \quad (2)$$

and

$$J_{i,i+1} = r_{i,i+1} X_i = v_b (1-X_{i+1}) X_i \exp\left(-\frac{E_{i+1} + Q_{seg}^{i+1}}{kT_s}\right), \quad (3a)$$

$$J_{i+1,i} = r_{i+1,i} X_{i+1} = v_b (1-X_i) X_{i+1} \exp\left(-\frac{E_{i+1}}{kT_s}\right) \quad (3b)$$

K_{des} , $r_{i,i+1}$, and $r_{i+1,i}$ are the dopant desorption and exchange coefficients, respectively, where E_i represents the activation barrier for dopant atoms transfer, and Q_{seg}^i is an energy term accounting for the surface segregation driving force. The factors $1 - X_{i,i+1}$ represent the limitation of available sites in the layer plane. $F_{i,i+1}$ is a flux that moves dopant atoms from layer *i* to layer *i+1* as one atomic layer is grown during the interval $\frac{1}{\tau}$.

$$F_{i,i+1} = \frac{X_i}{\tau} = \frac{R_{Si}}{a_0/4} X_i, \quad (4)$$

where R_{Si} is the Si growth rate. By numerical integrating Eq. (1) over a time period *t*, the distribution of dopant atoms in the *i*th layer can be determined.

The kinetic limitation to dopant segregation as Si growth is included in the model is explicit. This can be discussed in an analytical form using a simplified two-site model where we assume that there is no net dopant atom transfer between layers below the 3rd layer, i.e., the set of equations in Eq. (1) can be reduced to two. For a steady-state incorporation, $\frac{dX_i}{dt} = 0$ ($i=1,2$), the dopant density in layers 1 and 2 can then be analytically solved from the linear equations.

$$X_1 = \frac{J_d \left(r_{2,1} + \frac{1}{\tau}\right)}{K_{des} \left(r_{2,1} + \frac{1}{\tau}\right) + \frac{1}{\tau} \left(r_{1,2} + \frac{1}{\tau}\right)}, \quad (5a)$$

$$X_2 = \frac{J_d (r_{1,2} + \frac{1}{\tau})}{K_{des} (r_{2,1} + \frac{1}{\tau}) + \frac{1}{\tau} (r_{1,2} + \frac{1}{\tau})} \quad (5b)$$

By defining the segregation ratio $r = \frac{X_1}{X_2}$, one obtains

$$r = \frac{r_{2,1} + \frac{1}{\tau}}{r_{1,2} + \frac{1}{\tau}} \quad (6)$$

Two features can be noted from this equation: (i) as the Si growth rate increases, the segregation ratio approaches the value 1, implying that the surface segregation is kinetically limited; (ii) if the growth temperature is very high, or the Si growth rate is very low, i.e., $\frac{1}{\tau} \ll r_{i,j}$, Eq. (6) can be approximated as

$$r = \frac{r_{2,1}}{r_{1,2}} = \frac{1-X_1}{1-X_2} \exp\left(-\frac{Q_{seg}}{kT_s}\right) \quad (7)$$

This is a form of Langmuir isotherm to describe the classical equilibrium segregation, i.e., the distribution of dopant atoms between a surface and bulk layers is only determined by the difference of free energy.

The steady-state incorporation probability is defined as

$$\sigma = \frac{X_2}{J_d \tau} \quad (8)$$

Inserting Eq. (5b) into Eq. (8) and by utilizing Eq. (6), we obtain

$$\sigma = \frac{1}{K_{des} r \frac{(a_0/4)}{R_{Si}} + 1} \quad (9)$$

This is exactly the same expression as the one derived previously by Barnett and Greene [14] using the model developed by Rockett et al. [15].

APPLICATION OF THE MODEL TO THE HIGH SURFACE COVERAGE REGIME

The preceding model discussion was under the assumption that the dopant fraction X_i in the i th layer is $\ll 1$, i.e., site limitation is a negligible effect. This is only a good approximation for the ion doping case where dopant atoms are generally trapped in layers below the surface layer and the doping concentration is usually much smaller than the bulk Si atomic density. However, this is not valid for many of the thermal doping experiments for which the dopant surface adlayer, as it approaches the steady-state, can reach a significant fraction of a monolayer (ML). Thus, the probability for an incoming dopant atom to bond to a surface Si atom will decrease. Furthermore, nucleation processes also can occur when the surface coverage reaches a saturation value. For Sb, on Si(100) this occurs for coverages in the range 0.5-1.0 ML [16-18] at commonly used Si-MBE growth temperature.

In order to model dopant incorporation in a regime with high surface coverage of dopants, a zeroth (0th) layer is added in the model scheme. The morphology (high islands or flat layers) of the 0th layer is inexplicit, and there is no limit on the number of atoms in this layer. Basic features for the 0th layer are the following: (i) the probability for the dopant flux incident to this layer is determined by the occupation of the dopant atoms in the 1st layer (mask effect); (ii) there is a preference for dopant atoms to bond to a surface Si site, i.e., the (lateral) motion of dopant atoms, denoted by a time constant τ_s^{-1} associated with surface diffusion, from the 0th to the 1st layer is very fast but still limited by the number of available surface sites; (iii) within the layer dopants are weakly bonded with dopant-dopant bonds characterized by the bulk desorption energy; (iv) no Si growth occurs on the top of this layer, but the growth surface (the 1st layer) is still moving with Si growth, i.e., the layer always floats on the top. Furthermore, in the model it is possible to limit the maximum number of available surface sites

in the 1st layer to $X_C \leq 1$. The mathematical form of the first two differential equations in Eq. (1) are thus rewritten as follows:

$$\frac{dX_0}{dt} = J_d (1 - P) \cdot v_0 \exp\left(-\frac{E_0}{kT_s}\right) X_0 - \frac{P}{\tau_s} X_0 \quad (10a)$$

$$\frac{dX_1}{dt} = J_d P + \frac{P}{\tau_s} X_0 - J_{des} - J_{1,2} + J_{2,1} - F_{1,2} \quad (10b)$$

where, E_0 and v_0 are the activation energy and pre-exponential factor for a dopant atom evaporating from bulk material. P is the probability function for a dopant atom to impinge on an unoccupied site in the 1st layer.

$$P = 1 - \frac{X_1}{X_C} \quad (11)$$

RESULTS AND DISCUSSION

Figs. 3(a) and (b) shows the experimentally determined values of σ and r , respectively, for the case of thermal Sb doping with different growth temperatures. Comparing these results with our previous model calculations [9], the measured r values at high temperatures are about two orders higher than the predictions, while experimental σ values are smaller for high Si growth rate at low temperatures. These discrepancies can partly be attributed to the high surface coverage effect, partly due to an underestimate of the free energy term for Sb segregation (Q_{seg}). In the most recent data using the concentration transient analysis, the surface segregation studies were extended to higher growth temperatures. In this range the model calculation results are very sensitive to the Q_{seg} -value.

By increasing Q_{seg} from 1.2 to 1.85 eV and treating the high surface coverage effect by a 0th layer as above-described, we obtained the model calculation results shown in Fig. 3(a) and (b). In the calculations, E_0 was characterized from bulk Sb evaporation from a K-cell (1.52 eV) and τ^{-1} was calculated using surface diffusion data [19]. With these modifications, it is possible to get a good fit over the whole temperature range.

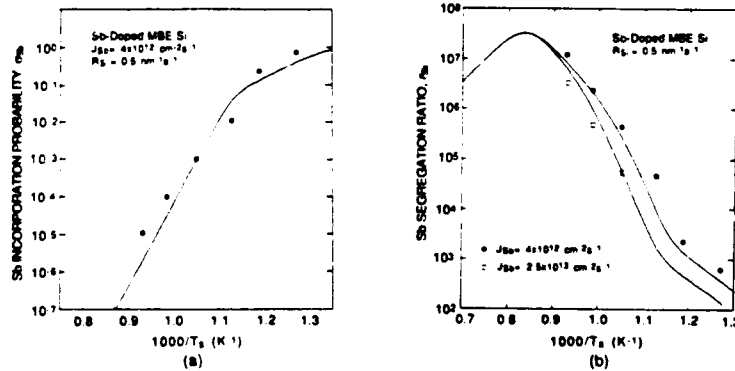


Fig.3 Experimentally determined and calculated values of (a) σ and (b) r for thermal Sb doping as a function of Growth temperature. ($RS_i=0.5 \text{ nm s}^{-1}$ and $JS_b=3.5 \times 10^{12} \text{ cm}^{-2} \text{ s}^{-1}$).

The influence of a high surface coverage of dopant atoms to dopant incorporation has also been observed for Al thermal doping [4]. As shown in Fig. 4, experimentally determined σ values are lower at low T_s but relatively higher at high T_s compared to the thermal Sb doping. This can be well explained by the

model calculations. For Al as a dopant in Si a smaller Q_{seg} value is expected from both size [7] and chemical [20] effects (0.8 eV in the present calculations). However the desorption and the bulk Al evaporation energies are high. According to preliminary results from desorption experiments [21], they were estimated to be 2.8 ± 0.2 and 3.1 ± 0.1 eV, respectively, and a maximum surface coverage was 0.5 ML. This thus results in a high surface coverage of Al, which in turn decreases the bulk steady-state incorporation (high surface coverage effect) at low T_s , while it enhances the incorporation at high T_s .

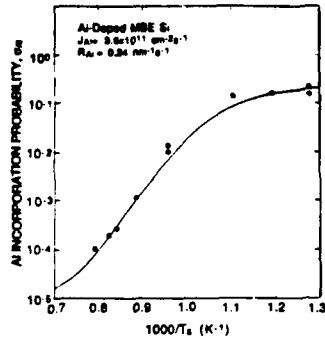


Fig. 4 Experimental determined [4] and calculated values of σ for thermal Al doping as a function of Growth temperature.

In summary, to model surface dopant segregation for thermal doping during Si-MBE growth, it is in many cases necessary to include effects of very high surface coverages. Besides the dopant atoms directly bonded to the Si surface, there can be an accumulation of more loosely bound dopant atoms in islands or multiple layers that can strongly affect the incorporation behavior.

Dr. M.-A. Hasan is acknowledged for helpful discussion.

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ASPECTS OF CRYSTAL QUALITY OF Si(100) FILMS GROWN BY MOLECULAR BEAM EPITAXY

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ABSTRACT

Silicon layers grown by molecular beam epitaxy, using both direct resistive heating and indirect radiant heating of the substrate, have been evaluated by photoluminescence measurements, diode I-V characterization, and chemical etching tests. The results show that large densities of defects could be introduced when resistively heated substrates were experiencing thermo-mechanical stress. Films with good crystal quality were grown using a carefully designed radiant type heater.

INTRODUCTION

It has been demonstrated during the last decade, that with silicon molecular beam epitaxy (Si-MBE) it is possible to obtain virtually any desired doping profile of Si layers and Si-based heterostructures grown at low temperature. However, in order to obtain Si films with device quality, efforts to improve the growth technique have been found to be necessary. There have, for example, been major improvements in the performance of Si/Si_{1-x}Ge_x heterojunction bipolar transistors in the last few years.

In this communication, we present recent results concerning improvements of crystal quality of grown films. A new heating and substrate handling system for 76.2-mm-diam wafers was installed in order to achieve uniform heating as well as to reduce any mechanical stress of the substrate for obtaining films with device quality. Characterization of grown Si layers by photoluminescence (PL), I-V measurements on p-n junctions formed by epitaxial layers, and chemical etching tests have shown that the crystal quality of layers grown using the new heater have been significantly improved compared to layers grown using the resistive heating method.

EXPERIMENTAL DETAILS

All epitaxial layers were grown in a VG V-80 Si MBE system, with a base pressure better than 10^{-10} Torr. The procedures of sample cleaning, growth, and doping have been described in detail elsewhere [1]. In order to obtain grown MBE layers with good crystalline quality, some modifications in the growth chamber were made. A cylindrical Si house was built over the e-beam source with an opening in the roof that only allowed deposition from the evaporated Si beam to the region near the substrate position. This was in order to minimize the unnecessary deposition of Si on the chamber walls, which otherwise can lead to a large number of Si flakes on the growth surface. Due to the use of this collimator, the density of Si particles ($\geq 1 \mu\text{m}$) incorporated into in the grown films has been significantly reduced ($< 10^2 \text{ cm}^{-2}$).

The main change was made in the substrate heating system. For quite a long time, a resistive heating of the substrate, as shown schematically in Fig. 1(a) was used. A Si substrate, which had to be cut in a rectangular shape, was supported by Ta clamps with thin Ta shims. The clamps were then mounted on a stainless-steel plate using ceramic insulators in a such way that they could slide. When electrical current passed through the Si substrate, it heated up resistively. This heating method in general gave efficient and rapid heating cycling with a rather good temperature control. However, it obviously suffers from that (i) the Si substrates have to be small pieces, which is limiting for device applications and

in particular it is not compatible with standard Si technology; (ii) more seriously, although a non-rigid construction was used for mounting the Ta clamps, strong mechanical stress still occurred at high temperature, which introduced a large density of dislocations and degraded the quality of substrates and grown films, as will be discussed below.

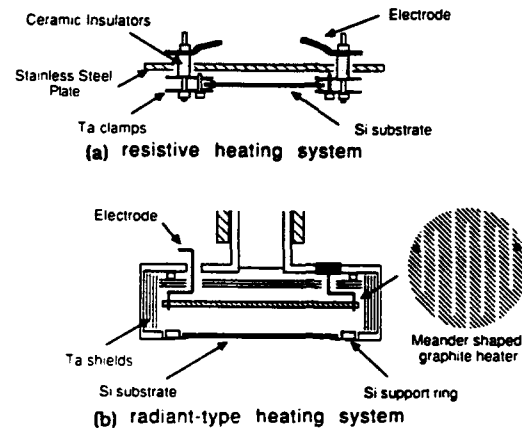


Fig. 1 (a) Resistive Si substrate heating system. (b) Radiant-type substrate heating system with a meander shaped graphite heater.

In order to reduce the thermal-expansion-induced defects, a loose mounting of the substrate has to be used. In Fig. 1(b), a graphite radiation heating unit, which is capable of handling 76.2-mm-diam wafers is illustrated. This heater can radiate a power of ~1.5 kW and heat a wafer to temperatures as high as 1000 °C. The out-gassing during growth is still comparable with that of the old resistive heater. Some main features of the heater are as follows: (i) The heating element is made of a thin slab of UHP graphite instead of commonly used Ta or Mo sheets, in order to minimize the risk of metal contamination. Furthermore, the greater emissivity of graphite drastically reduces the operation temperature of the heating element [2]. (ii) The heating element is patterned in a meander shape as illustrated in the insert of Fig. 1(b), and it is 100 mm in outer diameter. This design ensures a wafer of 76.2-mm-diam to be uniformly heated. In practice, 850 ± 10 °C across the wafer has been obtained. (iii) The Si substrate is freely held by a Si ring in order to firstly, avoid a direct contact with the metal supporting frame, and secondly, reduce thermal-expansion-induced mechanical stress since approximately the same temperature is obtained on the whole wafer and the Si ring holder.

The crystal quality of grown MBE Si layers using both heating methods were evaluated by PL measurements performed at 2K using the unfocussed 514.5 nm line of an Ar⁺ ion laser for optical excitation. A liquid nitrogen cooled North Coast E0817 Ge detector was used with a mechanical chopper and a conventional lock-in technique to recover the PL signal. The penetration depth of the exciting 514.5 nm radiation is about 1 μm in bulk Si material. However, the diffusion depth of photo-generated carriers is much larger, and it strongly depends on the concentration of defects present in the crystal. Usually, the diffusion depth can be in the order of a few tens of micrometers. Therefore, by analyzing the PL signal from the substrate through the MBE layer, one can also obtain information about defects in the epitaxial layer.

Another method to characterize epitaxial layers is utilizing diode structures, which were processed out of n⁺-p or p⁺-n double-layer structures grown at 520-650 °C. Both Sb [1] and In [3] low-energy ion sources were used to produce n and p type doping. The doping concentrations in the heavily doped layers were 5×10^{19} cm⁻³ (Sb) and 3×10^{18} cm⁻³ (In), respectively, and in the

moderately doped layers $1 \times 10^{17} \text{ cm}^{-3}$ for both cases. Heavily doped substrates, with the same type doping as the first grown doping layer were used for the back contact. The junction area, defined by mesa etching using the ion reactive etching technique, was $1 \times 10^{-4} \text{ cm}^2$. Finally, the junction surface was passivated using P-CVD SiO_x and SiN_x double layers in order to reduce the density of pinholes.

EXPERIMENTAL RESULTS

PL measurements

Typical PL spectra recorded at 2 K are shown in Fig. 2. All spectra contain the phonon replicas of the boron bound-exciton (BE): the transverse-acoustic transition B^{TA} , the transverse-optical transition B^{TO} , and two-phonon replica B^{2TO} , as well as the two-hole transition B^{2h} . These PL lines originate from the substrate from which no deep levels are observed (spectrum (a)). Dislocation related PL lines (D_1 - D_4) and a line denoted by X [4] are observed for a sample with a 5 μm thick undoped Si-MBE layer grown using the resistive heating mode at 850°C (spectrum (e)). The D type PL lines are usually associated with dislocations which appear in plastically deformed silicon, and their appearance was recently shown to need the presence of transition metal contamination [5]. Since all these PL lines also are apparent in spectrum (d) recorded from a bare substrate annealed with the same experimental conditions as growth, by the resistive heater, it is likely that thermal stress due to the temperature gradient and sample deformation at high temperatures are responsible for these defects.

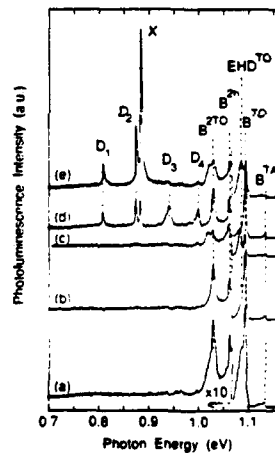


Fig.2 PL spectra at 2K of (a) substrate; (b) bare substrate that has been kept under growth conditions on the new substrate heater; (c) 9 μm thick undoped Si layer grown using the new heater; (d) bare substrate kept under growth conditions on the old substrate holder; and (e) 5 μm thick undoped epilayer grown using old heater. The substrate temperature was 850°C .

In contrast, D and X type PL lines are entirely absent in PL spectra measured from Si MBE layers grown with the new heater (Fig. 2(c)), or from a substrate just annealed under the same experimental conditions as growth (Fig. 2(b)). PL measurements on samples exposed to various heating temperatures, times, and temperature ramping rates showed that, with the new substrate heater, D type PL lines were only weakly observed when the substrate temperature was rapidly decreased with a rate $\geq 20^\circ\text{C s}^{-1}$. It is thus indicated that our new design of the radiant type heater has effectively minimized the risk of mechanical stress induced lattice damage.

Keeping the experimental conditions in particular the PL excitation power, the intensity of the B^{TO} line is found to be 30 % weaker in the spectra recorded on samples heated by either the old or the new substrate heater than in one recorded on the substrate sample. This behavior could be explained by the formation of non-radiative defects during the annealing process. More

pronounced is the further reduction of the B^0 line intensity observed from the epitaxial layers. A reduction of about 75 % for the 5 μm thick layer grown using the old heater and 60 % for the 9 μm thick layer grown using the new heater was obtained estimating the intensity over the background enhanced by the electron-hole-droplet (EHD) peak from of the B^0 PL signal. This thus means that part of the photo-generated carriers can freely move through the MBE grown layers before they recombine, giving rise to the substrate boron BE lines. With high sensitivity, neither the free-exciton nor bound-exciton related to the epilayer alone were observed in the undoped MBE layers.

Furthermore, BE lines related to dopant impurities were also observed [4] when the grown layers were intentionally doped with 200 eV accelerated In^+ ions using both substrate heating systems during growth between 500 and 850 $^\circ\text{C}$. As for the undoped MBE Si layers, no D type lines were observed for samples grown using the new heater, while still observed for the old heater. In addition, PL lines related to lattice damage as the vacancy-related line (1039.7 meV), previously observed for ion beam doped samples grown at low temperatures (500 $^\circ\text{C}$) [6], or PL lines associated to complexes containing carbon, nitrogen or copper [5] have never been observed in our large set of MBE materials with various growth temperatures (500-850 $^\circ\text{C}$) and doping acceleration energies (≤ 200 eV). It is thus also indicated that no lattice damage was induced by low-energy ion doping.

I-V characteristics of junction structures

I-V characteristics from a diode made from n^+ -p double-layer structures grown at 650 $^\circ\text{C}$ with the new graphite heater is shown in Fig. 3(a). About 60 % of the processed diodes showed hard avalanche breakdown with very small reverse leakage current ($\sim 10^{-9}$ A). Due to the non-uniformity of the dopant flux distribution along the radius of the Si substrate, the breakdown voltage was varying between 14-20 V, which corresponds well to the theoretically predicted avalanche breakdown [7] for an abrupt single-side junction with a low doping concentration side having $N=1.2 \times 10^{17} \text{ cm}^{-3}$. The hard breakdown obtained from these diodes again indicates low levels of dislocations and metal contamination in the grown films. This is a major improvement from our previously grown homo- or hetero-junctions using the old heater. The reverse leakage current for those structures was usually large, which in turn degraded the performance of processed devices [8,9]. The ideality factor for forward current at room-temperature is 1.1-1.2 (Fig. 3(b)) which is much better than for

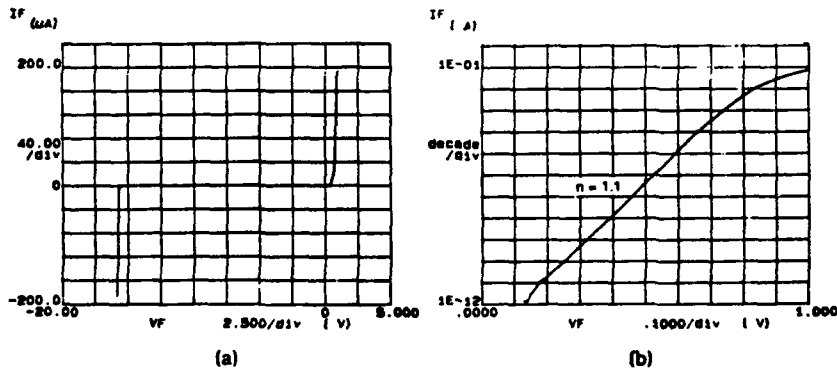


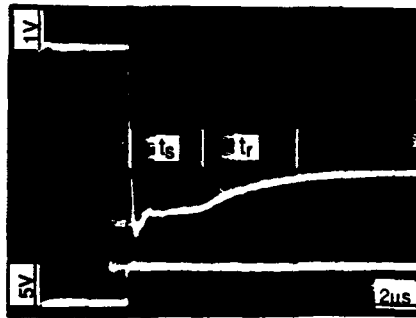
Fig. 3: (a) I-V characteristics of an MBE silicon n^+ -p diode grown using a radiant-type heater at 650 $^\circ\text{C}$. (b) a Gummel plot of the diode operated under forward bias at 300 K.

diodes grown with the previous resistive heating mode (typically 1.5 [10]), indicating that the quality of the junction interface is good with low interface recombination.

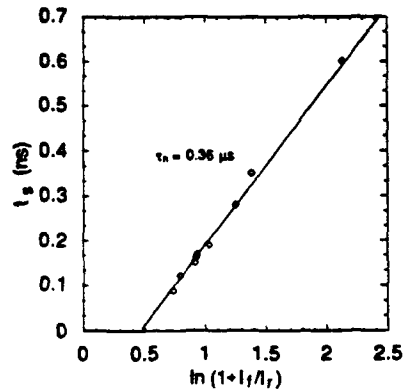
Switching properties of these diodes were studied in order to extract information on the minority carrier lifetime. Fig. 4(a), shows the pulse response of an abrupt n^+ -p diode. As a diode switches from the off- to the on-state, a very short time is required. However, as it switches from the on- to the off-state the response is much slower. As shown in Fig. 4(a), the reverse-current recovery curve exhibits two characteristic times, t_s and t_r , which represent the times required for the charge-storage and the charge-recovery, respectively. As has been suggested by Kuno [11], there is a relation between the recombination lifetime τ and t_s ,

$$t_s = \tau \left[\ln\left(1 + \frac{I_f}{I_r}\right) - \ln\left(1 + \frac{I_r Q(t_s)}{I_r Q(0)}\right) \right]. \quad (1)$$

The τ value can thus be obtained from the slope of a t_s vs. $\ln(1+I_f/I_r)$ plot. From the data in Fig. 4(b), a τ_n value of 0.36 μ s is obtained for a junction structure grown at 650°C, while 0.25 μ s was obtained for samples grown at 520°C. These values are very close to the minority carrier lifetime in bulk Si material [7] with corresponding doping concentrations.



(a)



(b)

Fig. 4: (a) The reverse-current recovery curve of a n^+ -p diode. The lower curve shows the input pulse signal. (b) a Kuno plot to determine the carrier lifetime.

The eq. (1) is based on a "long base" assumption, i.e., the junction width is much larger than the carrier diffusion length. In fact, the widths of MBE grown junctions are usually small, therefore, the value obtained by the above-mentioned method may be artificially enhanced by the high quality substrate. This was discussed when this method was applied to a p^+ -Si/ n -Si_{0.85}Ge_{0.15} diode, grown previously using the old heater, with a similar doping concentration configuration. The τ value obtained was 6-8 ns, which was larger than that measured by the small-signal admittance method (0.3 ns) [12]. However, the increase of the τ value by about two orders in the presently grown Si diodes can still be regarded as a significant improvement.

Finally, chemical preferential etching tests using Wright-Jenkins solution showed a decreased density of defect-induced etching pits on the layers grown with the present heating system ($\leq 10^2$ cm^{-2} as opposed to 10^3 cm^{-2} for the previous heater).

In summary, the results presented indicate that the density of electrically active defects in MBE Si layers grown with an appropriately designed heater has been significantly reduced compared to previously grown layers.

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SURFACE ACCUMULATION OF BORON DURING Si MOLECULAR BEAM EPITAXY

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ABSTRACT

A high temperature, elemental boron evaporation source has been used for the study of the boron doping behaviour in Si as a function of growth temperature and doping level. Significant profile smearing of boron at doping levels below $5 \times 10^{18} \text{cm}^{-3}$ is observed. Profile smearing is more severe in higher doped samples for growth temperatures above 600°C at a growth rate of 0.28 nms^{-1} . This is interpreted as arising from the formation of a surface phase of boron at higher doping levels. The marked improvement in profile abruptness at low temperatures suggests significant benefits associated with the use of an elemental boron source for the growth of high resolution Si/Si_{1-x}Ge_x device structures.

INTRODUCTION

The current interest in boron doping kinetics, particularly at low temperature, is motivated by the desire to fabricate novel devices by Si and SiGe molecular beam epitaxy (MBE) for fast switching and high current gain applications. These include the heterojunction bipolar transistor and the modulation doped quantum well, a constituent of the high mobility p-channel field effect transistor [1,2]. The efficacy of such devices is directly related to the ability to control the abruptness of dopant profiles on a nanometer scale. Indeed, the demands for dopant profile control during MBE have become so stringent that they require a reassessment of what should be regarded as 'significant' profile smearing. Despite the importance of such work, little quantitative information on boron incorporation at low temperatures has been published [3-5]. This temperature regime is only available to operators using an elemental boron source, due to increased oxygen adsorption from compound sources, such as HBO₂ and B₂O₃, below 650°C [6,7].

In a previous paper we addressed the temperature dependence of boron doping behaviour and noted a sharp increase in boron solubility limits caused by a retardation in surface segregation for substrate temperatures below 650°C [3]. Jorke and Kibbel recently discussed boron incorporation as a function of substrate temperature and growth rate for boron delta layers, using a segregation model involving diffusion of dopant to the surface from the underlying layer [4]. They observed an abrupt transition in the temperature dependence of boron segregation at a growth temperature of 600°C for a growth rate of 0.1 nms^{-1} . This is characteristic of a transition from equilibrium to kinetically limited segregation, previously predicted and verified experimentally for antimony doping [8,9]. Boron segregation was characterised by the degree of profile broadening (nm) in boron layers grown at different temperatures. This was determined by measuring the exponential decay length of the leading edge slope obtained by secondary ion mass spectroscopy (SIMS) depth profiles. Jorke and Kibbel also observed a "temporal variation" in segregation coefficient [4].

In this paper boron incorporation is discussed using a model for profile smearing involving surface accumulation, rather than segregation. Results are presented as a function of growth temperature and *particularly* of doping level, by comparing profile smearing in structures doped beyond the solubility limit with layers grown at lower doping levels. From measurements of doping transients that occur after terminating the doping flux, we reveal for the first time a self-limiting boron phase which forms by accumulation of boron during coevaporation doping.

EXPERIMENTAL

Boron doped layers were grown in modified VG Semicon V80 and V90S systems on Si(100) substrates using an elemental dopant source. Temperatures were varied between 900 to 450°C , monitored above 600°C via an optical pyrometer. The

reproducibility of temperature was $\pm 10^\circ\text{C}$ with an absolute error of $\pm 25^\circ\text{C}$ at temperatures above 600°C and $\pm 50^\circ\text{C}$ at temperatures below this. A modified INFICON Sentinel III EELS [10] was used to control growth rates. SIMS depth profiles were obtained in a commercial Cameca IMS-4F instrument.

RESULTS

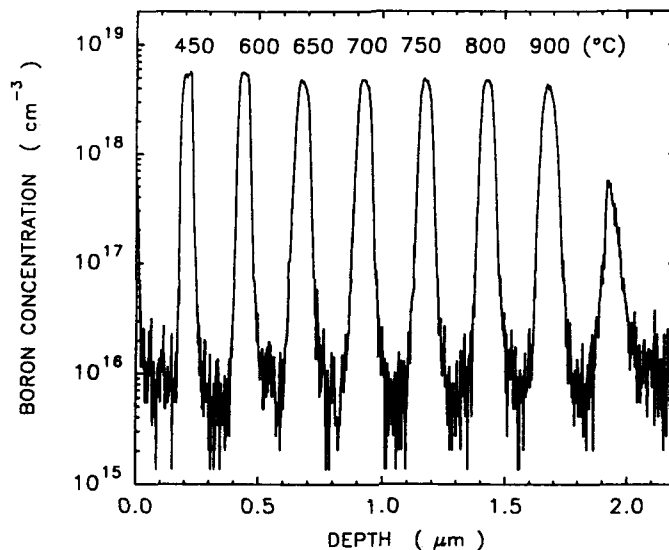


Fig 1 SIMS profile of structure A using a 4keV O_2^+ beam at normal incidence.

Fig. 1 shows a SIMS profile of a boron doped structure, denoted structure A used to determine the degree of profile broadening as a function of growth temperature at low doping levels. Structure A contains boron doped regions 50nm thick separated by 200nm of undoped material. These were grown at temperatures between 900 and 450°C at a rate of 0.28nm/s . Electrochemical capacitance-voltage (E-CV) measurements indicate that complete electrical activation of dopant throughout the temperature range at this doping level.

A number of parameters are available for quantifying profile smearing [8,9]. For the growth of modulation doped structures the profile broadening parameter Δ is the most appropriate in specifying a well-defined separation between doping spikes and heterojunction interfaces, and is usually expressed as the exponential decay length in the growth direction. This was determined from the leading edge slopes of SIMS depth profiles for boron layers grown at different temperatures. SIMS induced broadening in the leading edge, by ion beam mixing and non-uniform etching, only becomes important when considering the most abrupt ($< 2\text{nm/decade}$) slopes. For such slopes the actual profile abruptness is probably steeper than that given. The SIMS trailing edge is much more strongly affected by such effects and measurements of these slopes are not given here.

A cursory examination of Fig. 1 reveals little profile smearing in structure A although solid state diffusion is evident at temperatures at and above 800°C . However closer examination of the SIMS leading edges in structure A reveals temperature dependent profile smearing corresponding to an exponential decay length varying from

1 to 10 nm, reaching a maximum at a temperature of 700°C for this growth rate. Although this smearing is small compared with observations of Sb, In and Al incorporation behaviour [8,9], as previously mentioned it can have a critical effect on device action [1,2].

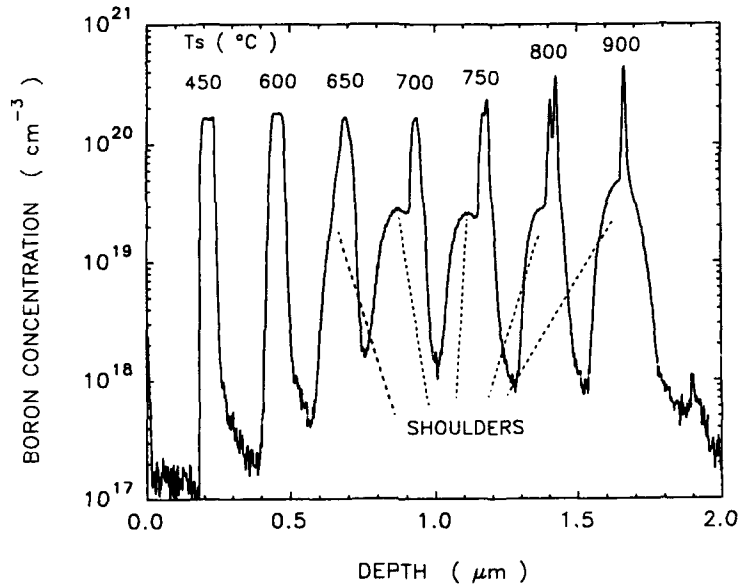


Fig. 2 Boron SIMS depth profile of structure B obtained using an O_2^+ primary ion beam at normal incidence.

A second structure was grown identical to structure A except that the intended boron concentration was set to $2 \times 10^{20} \text{cm}^{-3}$, well above published solubility data [11,12]. The SIMS profile of this structure, referred to as structure B, is given in Fig. 2. The features in this structure include narrow ($< 35 \text{nm}$) spikes arising from boron precipitates [3,5] and shoulders extending up to 100nm in the growth direction for temperatures at and above 650°C . At 600°C and below a sharp improvement in profile abruptness was observed with no evidence of precipitation or shoulder formation. E-CV measurements indicate that while the shoulders in structure B are fully activated the narrow spikes are not, and that all dopant incorporated at temperatures below 600°C was completely activated at a level of $\approx 2 \times 10^{20} \text{cm}^{-3}$.

The shoulders are often observed if solubility limits have been exceeded. The exponential decay constant Δ in the leading edge slopes of the shoulders in structure B is plotted in Fig. 3 as a function of substrate temperature. Also included in Fig. 3 is a plot of decay lengths for structure A (doped at a peak level of $5 \times 10^{18} \text{cm}^{-3}$). A difference in decay lengths for the two doping levels is clearly visible for temperatures above 600°C , suggesting differing incorporation processes occurring at high and low surface coverages.

DISCUSSION

The profile smearing occurring in structures A and B is caused by a comparatively weak tendency for boron to collect at the growing surface rather than incorporate, due to its relatively small size compared with the Si matrix [13]. Incorporation processes are temperature and growth rate dependent since they depend on diffusion rates at the surface. However the difference in decay lengths above

600°C in structures A and B needs further consideration. We shall review the processes leading to the shoulder formation in structure B and show how these can severely disrupt dopant profiles at lower doping levels.

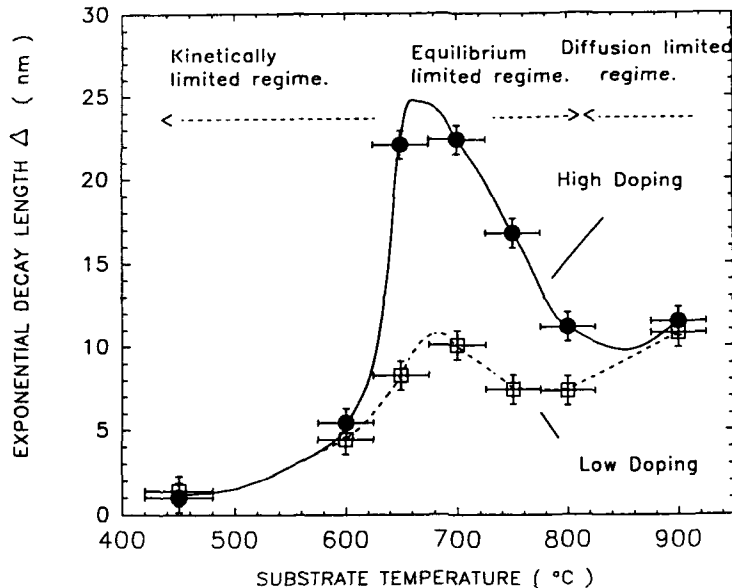


Fig. 3 Plot of the exponential decay lengths Δ of the leading edge slopes of the boron doped layers in structures A and B.

The shoulders seen at temperatures at and above 650°C in structure B are caused by the formation of a surface phase of boron on the surface during heavy doping [5]. These shoulders and those obtained from other highly doped structures have an areal density equivalent to 0.25ML (1ML = $6.8 \times 10^{14} \text{cm}^{-2}$) except for the shoulder at 800°C which contains ≈ 0.4 ML. The growth temperature of 800°C is also unique in that a double spike is formed (see Fig. 2). Equilibrium between the surface phase, the precipitates and the incorporating/accumulating fluxes, limits the surface phase to a coverage of 0.25ML. Any boron in excess of this coverage goes into the formation of inactive precipitates giving rise to the narrow spikes seen in Fig. 2. Once the boron shutter is closed the accumulated phase is no longer sustained and subsequently incorporates at a level bounded by the solubility limit. This continues until the phase is depleted leading to the shoulder formation in structure B. A comparison of the peak level in the shoulders, and results of uniformly doped boron layers grown in the same temperature range, with previously published data [11,12] provided evidence to support this assumption (see Fig. 4).

The boron surface phase diagram is as yet unknown on Si(100), but consideration of surface densities of boron led us to believe that the accumulated phase was compatible with a primitive $p(2 \times 2)$ surface structure although further LEED experiments would be necessary to prove this [5]. Headrick *et al.* however observed a self-limiting boron (2×1) superstructure on Si(100) but this was obtained under static growth conditions; after interrupting Si growth and "building up" a boron coverage on a clean reconstructed surface [14]. The boron $p(2 \times 2)$ phase is only observed during coevaporation doping, but is self-limiting in a similar manner.

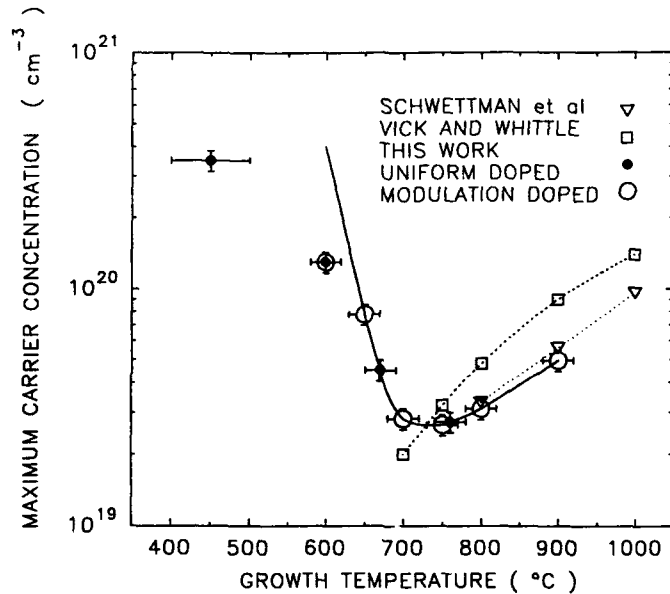


Fig. 4 Plot of solid solubility of boron in Si against growth temperature, as determined from shoulders in structure B and results of heavily doped uniform layers.

The existence of surface phases have previously been shown to modify surface impurity desorption energies, and surface diffusion through interactions between nearest and next-nearest neighbours. For instance Lifshits *et al* [15] showed that on Si(111) surfaces ad-atom impurities not in a surface phase, ie not on ordered surface sites, have a much higher mobility than impurities included in the surface phase. Observations of Ga on Si(100) surfaces, indicate that Ga forms clusters at high coverages and shows a stronger tendency to surface accumulate [16]. We deduce that properties associated with surface phases lead to the increased boron profile smearing observed in structure B, seen in Fig. 3 as an increase in exponential decay constant compared with that obtained from lower doped structures. The increase in profile smearing in structure B suggests an incorporation model based on migration in the surface plane needs to be invoked, rather than back-diffusion of dopant from underlying layers near the surface. Surface accumulation (segregation) as discussed by Andrieu [17] requires surface migration of dopant as a precondition for profile smearing. This differs from enhanced diffusion of dopant near the surface, initially proposed by Greene *et al* [8] then developed into surface-subsurface interchange model by Jorke [9] for which dopant diffusion from layers below the surface is inferred. Andrieu's model postulates accumulation occurring by a step-climbing process and that surface accumulation is due to events occurring at the growing surface. This provides evidence for the empirical observation that dopants with larger differences in covalent radii show a stronger tendency to accumulate because of the stress they induce at an incorporation site consistent with observations of accumulation behaviour in Si and III-V systems [13]. The significance of this to this work is that it accounts for the observation that boron continuously collects on the surface and need not diffuse from dopant already incorporated in underlying layers. It should be stressed that it is not necessary to dope at $2 \times 10^{20} \text{cm}^{-3}$ to observe this increased accumulation behaviour. By the time the decay transient in the shoulder has been reached, a large part of that surface phase has already been incorporated at the solubility limit. However there

exists a significant fraction of dopant at the surface in the shoulder decay transient (SIMS leading edge) equivalent to ≈ 0.1 ML. Hence enough of the surface phase still exists in smaller clusters but at a level sufficient to modify surface interactions. Hence if the increase in accumulation is observed at surface coverages of < 0.1 ML, it might be expected that layers grown under conditions of strong accumulation and doped at levels $\approx 1 \times 10^{19} \text{cm}^{-3}$ might show the profile smearing associated with high doping accumulation. We believe Jorke and Kibbel were observing this phenomenon when they noticed a 'temporal change' in profile broadening in boron delta layers doped at a peak of about $1 \times 10^{19} \text{cm}^{-3}$.

At low temperatures the processes which lead to formation of the boron phase are kinetically limited. Incorporation of boron in the absence of a surface phase is broadly similar at the doping levels used in this experiment. This is seen in Fig. 3 as the merging of the two accumulation curves at temperatures $< 600^\circ\text{C}$ into a common line with the same slope.

CONCLUSIONS

Boron accumulation has been studied in Si MBE as a function of substrate temperature and doping level in the temperature range 900 to 450°C by measuring the leading edge slopes in SIMS depth profiles. The degree of profile broadening was significantly worse in the higher doped samples for temperatures at and above 650°C , due to the formation of a accumulated surface phase of boron. Below this temperature accumulation and phase formation processes were kinetically limited so that leading edge slopes in high and low doped samples were similar within the error of the experiment. It is thought that layers grown at intermediate doping levels would exhibit this behaviour thus explaining observations of temporal changes in leading edge slopes in the literature.

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SURFACE SEGREGATION OF BORON DURING Si-MBE GROWTH

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ABSTRACT

Boron doping, using an elemental boron source during molecular beam epitaxial growth of silicon, has been studied. The boron flux was provided by a high temperature source heated by radiation and electron bombardment. The maximum boron deposition rate used was $1 \times 10^{12} \text{ cm}^{-2} \text{ s}^{-1}$ at an estimated B temperature of 1950 °C. For growth at a substrate temperature of 650 °C, there is very little surface segregation when the doping level is in the range 1×10^{16} - $1 \times 10^{19} \text{ cm}^{-3}$. For very high boron to silicon flux ratio ($\geq 7 \times 10^{-3}$) there is a strong surface segregation that results in surface accumulation of boron. This initially leads to a 2×2 reconstruction of the Si(100) surface, and further surface segregation during growth results in roughening of the surface due to the creation of (311)-facets. In a separate set of experiments, the surface segregation was studied using *in situ* Auger electron spectroscopy of predeposited layers of boron that were gradually covered by Si capping layers. Strong and surface coverage dependent surface segregation was observed both in the case of Si(100) and (111) substrates.

INTRODUCTION

Boron has emerged as the main choice for p-doping during Si-MBE growth. For a long time there was a reluctance to use an elemental boron source due to the very low vapour pressure and the corresponding need for a very high evaporation cell temperature. Low temperature sources for boron doping instead used compounds like B_2O_3 or HBO_2 or evaporation from heavily doped Si material [1]. Evaporation of elementary boron during Si-MBE-growth was first reported using a simple refractory metal B furnace [2]. Several groups have since then developed effusion- or Knudsen-cell sources with graphite crucibles for high temperature evaporation [3,4]. In most of the work, growth was done with moderate boron-concentrations ($< 6 \times 10^{19} \text{ cm}^{-3}$) and the modulation doped B-profiles were concluded to show complete incorporation and activation and negligible surface segregation.

Recently, there have been reports on strong B surface segregation when extremely high B-concentrations have been attempted using both compound and elemental B-sources for co-evaporation during growth [5,6]. Also in the case of capping of a Si(111)- $\sqrt{3} \times \sqrt{3}$ -B surface with silicon, strong surface segregation has been reported [7]. In this paper we briefly report on the characteristics of a home-built high

temperature B Knudsen-cell. This has been used for *in situ* studies using Low Energy Electron Diffraction (LEED) and Auger Electron Spectroscopy (AES) of the growth behaviour of Si(100) and (111) surfaces with high B fluxes or surface concentrations.

EXPERIMENTAL DETAILS

The experiments were performed in a VG V-80 Si-MBE-system. The system and the standard substrate cleaning procedures have been described elsewhere [8]. The boron Knudsen-cell is similar to the design described in refs. 3 and 4 and a schematic diagram is shown in Fig.1. A graphite crucible is heated by radiation and electron bombardment from a surrounding W-filament. Figure 2 shows a SIMS-profile from a modulation doped structure grown at 650 °C, that has been used to characterize the source. Figure 3 shows the obtained relationship between the flux of B at the substrate surface and the inverse of the cell temperature, T_{cell} , as measured with a thermocouple mounted within the graphite, a few mm below the B charge. From separate calibration measurements with a pyrometer seeing into the empty source, without the top orifice, the temperature within the cell is estimated to be ≈ 150 °C higher than the thermocouple reading at normal working temperatures. The measured, approximately linear, dependence of the flux with $1/T_{cell}$ has been used to extrapolate the cell temperature for fluxes up to 1×10^{12} cm^{-2} s^{-1} .

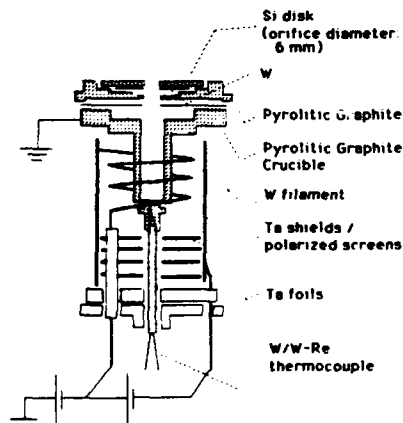


Figure 1. A schematic drawing of the high temperature B cell.

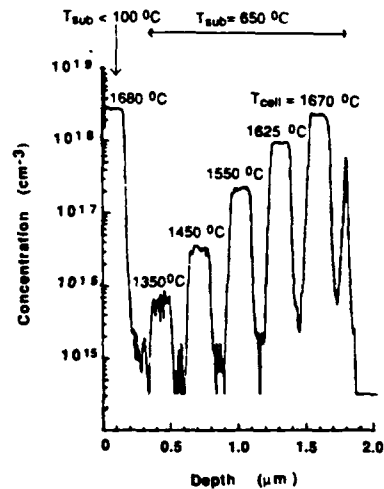


Figure 2. SIMS profile of the B concentration in modulation doped Si grown using different T_{cell} values.

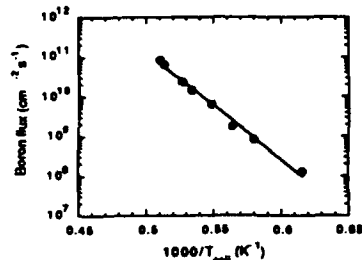


Figure 3. The boron flux at the substrate surface ≈ 30 cm above the source as a function of $1/T_{\text{cell}}$.

RESULTS AND DISCUSSION

Weak surface segregation for doping levels below $1 \times 10^{19} \text{ cm}^{-3}$

The profile control of B-doping for moderate doping levels is excellent as shown in Fig. 2. Similar results have been reported previously in refs. 3 and 6, where it was concluded that surface segregation is negligible. In a detailed analysis of the profile shapes it is possible to see that there are some minor surface segregation effects in the profiles. The leading edge (closest to the top surface) is $\approx 30\%$ broader than the trailing edge, which is opposite to the expected relationship if the broadening was only due to SIMS ion-mixing effects. However, to get accurate results on this low surface segregation, it is probably necessary to grow specially designed growth structures, using, e.g., the recently developed concentration transient analysis method [9].

Growth behaviour with extremely high B-flux

As reported by Parry et al. [6,10] there is, for high growth temperatures (≥ 650 °C), a transition to a stage with very strong surface segregation if the doping level is above $\approx 1 \times 10^{20} \text{ cm}^{-3}$. Based on measurements of the integrated SIMS-intensity of shoulders penetrating into intentionally un-doped regions in modulation doped structures, it has been proposed that the saturation coverage for the B surface segregated layer on Si(100) is 0.25 monolayer (ML). Excess B would form precipitates that are incorporated during growth. An ordered Si(100) 2×2 -B reconstruction was proposed to explain the indications of a highly stable surface with 0.25 ML surface B coverage.

With this hypothesis in mind we first studied with LEED and AES the resulting growth surface after depositing 1200 Å of highly B-doped Si(100) at 650 °C. The co-evaporated B-flux corresponded to a bulk concentration of $6 \times 10^{20} \text{ cm}^{-3}$. With a solid solubility of $4 \times 10^{19} \text{ cm}^{-3}$ [10] an amount of B corresponding to ≈ 8 monolayers should be available for the surface accumulated layer and precipitates. The Auger B/Si signal ratio was ≈ 0.9 , which is estimated to correspond to ≈ 0.7 ML, based on the SIMS calibration of the flux and assuming a linear relationship between B/Si signal ratio and coverage up to 0.7 ML. This supports qualitatively the idea of a strong B surface



Figure 4. LEED patterns for surfaces with high boron coverages.
 (a) The superposition of (100)2x1 and (311)3x1 patterns for ≈ 0.12 ML.
 (b) The weak (100)2x2 pattern at ≈ 0.07 ML.

segregation up to a significant fraction of a monolayer, while further boron surface accumulation does not occur, due to incorporation of B precipitates. The quantitative difference between the estimates of B surface coverage may be due to the kinetical limitations in the present experiments as the growth temperature used is at the low end of the range where SIMS indicated the 0.25 ML B surface coverage. Furthermore, the present studies show that the B overlayer affects the surface morphology as LEED indicated that the surface contained facets. Besides the normal 2x1 pattern there was strong intensity of an overlapping 3x1 reconstruction of (311) facets as is shown in Fig. 4a.

A more detailed study of the development of the B-rich (100) surface was performed at a growth temperature of 750 °C. The AES and LEED results are indicated in Fig. 5 together with one data point for the thicker layer growth at 650 °C. It is very interesting to note that a 2x2 LEED pattern, as suggested by Parry et al., develops during

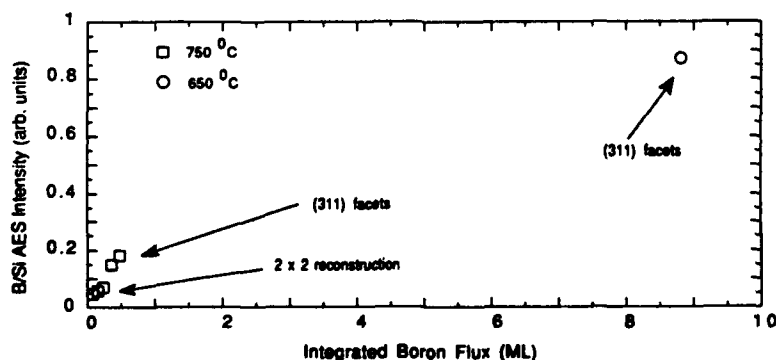


Figure 5. The Auger B/Si intensity ratio vs. integrated B flux.

initial stage of surface accumulation. The pattern was however not very strong, as shown in Fig.4b, and the surface coverage of the most intense 2x2 patterns corresponds to a coverage of only 0.05-0.1 ML. For higher B coverages there was again the appearance of (311) facets and the 2x2 pattern disappeared.

Surface segregation during capping of B-overlayer

If the B flux is turned off after B has been accumulating on a growth surface, it is important to know how quickly it can be incorporated by a growing Si layer. As we will show, it is very suitable to discuss the behaviour in terms of a temperature dependent solid solubility. Figure 6 shows the decay of the B/Si Auger intensity ratio for overgrowth of different B overlayers in the Si(100) and (111) surfaces. The filled symbols all indicate results for overgrowth at 650 °C at a rate of 0.2 ML/s. It is very striking that the initial linear decay rate is the same for both experiments with different initial coverages on the (111) surface. The same is true for the two sets of data for the (100) surface the same growth conditions. However, the initial decay rate is a factor of two larger for the (100) surface. From these data we can estimate solid solubilities of 5 and $10 \times 10^{19} \text{ cm}^{-3}$ for the (111) and (100) surfaces, respectively. This is in good agreement with the SIMS results in ref. 10 which was $8 \times 10^{19} \text{ cm}^{-3}$ for growth on (100) at 650 °C.

Capping of a B-overlayer on the (100) surface was also studied at 450°C as shown in Fig. 6b. The apparent solid solubility then increases to $4 \times 10^{20} \text{ cm}^{-3}$ which again is in very good agreement with the result in ref. 10 ($3.5 \times 10^{20} \text{ cm}^{-3}$ at 450 °C). We also studied the Si-rate dependence of the solid solubility and, as shown in Fig. 6b, there is no change as the Si rate was increased from 0.2 to 0.8 Å/s. These results indicate that the B-induced strain of the near surface layers is the dominant factor for the surface segregation. It is interesting to note that the magnitude of this segregation depends on the growth surface

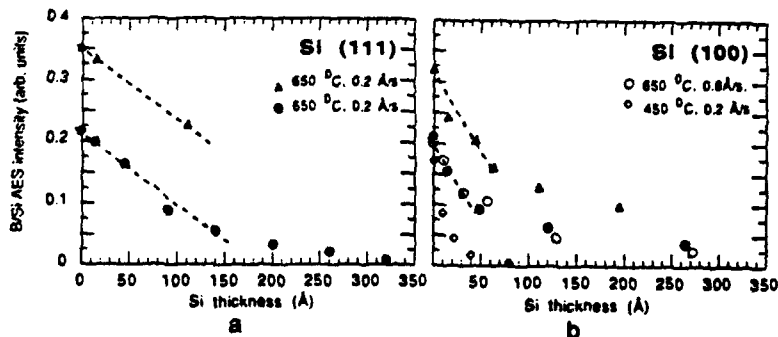


Figure 6. The Auger B/Si intensity ratio as a function of silicon film thickness for (111) and (100) surfaces at different growth conditions.

orientation. In other words, the apparent solid solubility during MBE-growth is surface dependent.

The surface order was also studied with LEED in these experiments. For the (111) surface there is a $\sqrt{3}\times\sqrt{3}$ reconstruction at high coverage, but there is a transition to a dominating 7x7 reconstruction at B/Si ≈ 0.05 which corresponds to ≈ 0.035 ML. On Si(100), the starting high coverage surface, prepared and maintained at 650 °C, has a 2x1 reconstruction, then the 2x2 reconstruction appears at around 0.03 ML coverage. Finally at very low B coverage the surface again exhibits a 2x1 reconstruction.

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X-RAY CHARACTERISATION OF BORON DELTA LAYERS IN Si AND SiGe

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ABSTRACT

We demonstrate the growth, by MBE, of high sheet density B delta layers in both Si and SiGe epitaxial layers. Double Crystal X-Ray Diffraction is shown to be a non-destructive method of characterising the width of very narrow (0.3 nm) delta layers and the sheet density of the activated B. The ability of delta layers to withstand high temperature anneals is considered and it is found that a 750 °C anneal for 1 hour broadens the delta layer to beyond the width required for carrier confinement.

Introduction

A delta doping distribution can be produced by restricting the dopant atoms to several atomic layers within the matrix material. Such delta layers can be used in a number of novel devices, such as delta MOSFETS[1] where they offer considerable advantages particularly with channel lengths < 0.3 microns. Thin sheets of dopant can also be used for selectively doping Si/SiGe structures where the Si and SiGe layers can be < 5 nm in width. In such structures the free carriers migrate to the adjacent potential wells where they can move parallel to the interface with much reduced ionised impurity scattering [2].

Growth of the Delta Layers

The growth of the delta layers was carried out in a VG Semicon V90S MBE system using electron beam evaporated Si and Ge sources and an elemental B effusion cell. The Si substrates were given an in-situ 850 °C anneal to remove SiO₂ and then a Si buffer was deposited as the temperature cooled to the growth temperature of 480 °C. Si or SiGe layers were then grown to a thickness of 50 nm. The matrix fluxes were then shuttered off and elemental B was allowed to accumulate on the surface for up to ten minutes. Finally the capping layer was deposited.

Uniform Boron doping

In order to determine the strain produced by B in Si, five highly B doped layers were grown at temperatures varying from 500 to 800 °C. This provided samples with different levels of dopant activation and allowed the strain induced by activated and unactivated B to be found.

Table 1

Growth Temperature (°C)	Boron Density (SIMS) (cm ⁻³)	Carrier Density (Hall Measurements) (cm ⁻³)	Strain per Atom (X-ray Diffraction)
500	5.6 * 10 ¹⁹	5.6 * 10 ¹⁹	-6.0 * 10 ⁻²⁴
600	1.3 * 10 ²⁰	1.3 * 10 ²⁰	-6.1 * 10 ⁻²⁴
670	1.4 * 10 ²⁰	4.1 * 10 ¹⁹	-1.7 * 10 ⁻²⁴
760	1.3 * 10 ²⁰	2.8 * 10 ¹⁹	-1.2 * 10 ⁻²⁴
800	2.0 * 10 ²⁰	3.5 * 10 ¹⁹	-1.2 * 10 ⁻²⁴

The results of these analyses are given in table I and the derived values of induced strain per atom are:

$$\begin{aligned} \text{Activated B} &= -6.05 \pm 0.2 * 10^{-24} \\ \text{Unactivated B} &= 0.03 \pm 0.2 * 10^{-24} \end{aligned}$$

The value for activated B agrees with the values obtained previously [3,4]. Unactivated B can be seen to have little effect on the lattice constant as one might expect since there is not the effect of replacement of Si on the lattice site by a smaller atom and there is no strain due to the presence of holes in the valence band [5]. As is evident from table 1 the growth temperature has a very marked effect on dopant incorporation [6] and fully activated delta layers demanded that growth temperatures be kept below 600°C.

X-ray Characterisation of Delta layers in Si

With X-ray diffraction it is not possible to see the B directly due to the low concentration of B and its low structure factor. To characterise delta layers using X-ray diffraction it is necessary to consider and model the strain induced by the dopant. The strain induced by the delta layer locally contracts the lattice. Therefore the diffracted signal from the Si or SiGe capping layer is no longer in phase with the diffracted signal from the material layer underlying the delta layer and thus interference fringes are produced. The measurements were taken on a BEDE 150 diffractometer with a four bounce [004] beam conditioner [7], which was required to reduce the intensity of the tails associated with the Si main diffraction peak. Both [004] and [113] glancing incidence reflections were used with the same beam conditioner; this leads to the subsidiary peak next to the main substrate peak (eg see Figs 3 and 4). However this has no significant effect on the delta layer fringes. Fig 1 shows simulated [004] rocking curves for 1 nm wide B delta layers of uniform B concentration, buried 52 nm down in Si where the B concentration varies from 1 At% to 41 At% (Atomic %). These simulations were obtained using a dynamical theory program [8].

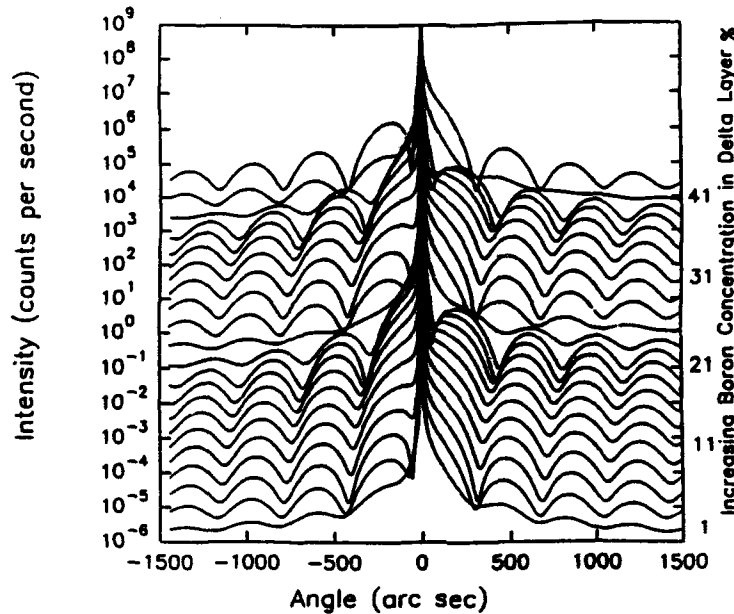


Fig 1 Simulations of the [004] rocking curve obtained from a 1 nm wide delta layer with uniform B concentrations rising from 1 to 41 At%.

It can be seen that the interference fringes move to the right as the degree of strain increases. However, there are discontinuities where the B concentrations are 25 At% and 41 At% corresponding to where the X-ray path difference between the diffracting planes of the capping layer and underlying material is equivalent to an integer number of wavelengths. It is also seen that the fringe pattern repeats itself and hence it is necessary to take a second reflection (ie in the [113] direction) in order to determine uniquely the degree of strain present. For the delta layers grown comparison of the X-ray analysis with SIMS measurements indicated that the B atoms were fully activated.

The depth of the delta layer can be determined simply from the period of the interference fringes which is inversely proportional to the depth in a manner similar to the Pendellosung fringes associated with single epitaxial layers. For sample 10-33, a highly doped B delta layer, SIMS gave the sheet density of B as $3.8 \pm 0.4 \times 10^{14} \text{ cm}^{-2}$ and the X-ray diffraction results gave the net contraction in the [001] direction to be $31 \pm 2 \text{ pm}$ which corresponds to full activation of the dopant. Hall measurements also confirmed that this delta layer was fully activated [9]. The depth determined by X-ray diffraction was $52 \pm 1 \text{ nm}$ which agreed with Si flux measurements during growth and with XTEM analysis.

Once the depth and sheet density of the delta have been determined, the width of the delta layer can be found by considering the relative heights of the peaks on the right hand side of the main Si peak with those on the left hand side. Fig 2 shows the 3:5 and 2:4 peak height ratio for sample 10-33, shown in Fig 3. The line shown represents the values obtained from the dynamical theory simulation program [8] for a square well strain profile 51 nm deep with differing widths but constant sheet density of $4 \times 10^{14} \text{ cm}^{-2}$ of B.

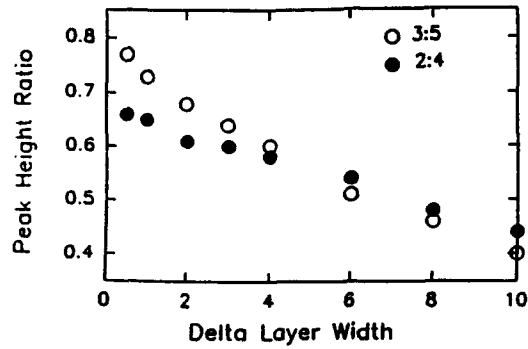


Fig 2 Peak height ratios for a B delta layer with a sheet density of $4 \times 10^{14} \text{cm}^{-2}$ for increasing delta layer width assuming a uniform doping profile.

The measured 3:5 peak height ratio for sample 10-33 was 0.8 ± 0.04 indicating that this delta layer has the bulk of its B within $0.3 \pm 0.5 \text{ nm}$. Combining this with the known sheet density from SIMS indicates that the peak doping concentration of the delta layer is greater than 10 At%.

Anneals of Boron Delta Layers in Si

To investigate the effects of heat treatments on delta layers as would be required for device processing we annealed a B delta layer, 10-33, at temperatures from 650 to 850 °C and the [113] rocking curves obtained from these samples are shown in Fig 3.

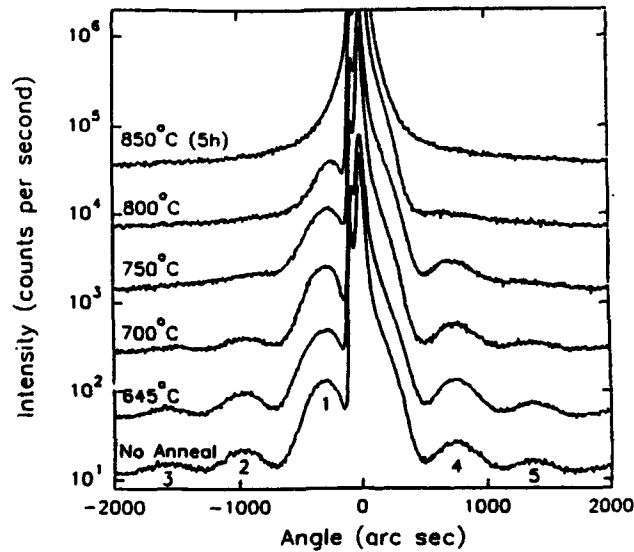


Fig 3 The effect of 1 hour anneals (unless stated) on a B delta layer indicates significant broadening at temperatures above 700°C

As the annealing temperature is increased diffusion broadening of the delta layer is evident. At temperatures above 750 °C the diffusion becomes too great and it seems likely that inhomogeneities in the strain profile of the delta layer reduce the interference effects seen. At lower temperatures the delta width can be deduced and it is given in table 2.

Table 2

Anneal Temperature	Peak ratio		Delta Layer Width
	3/5	2/4	
No Anneal	0.8	0.67	0.3 ± 0.5 nm
650 °C 1 hour	0.75	0.65	0.8 ± 0.5 nm
700 °C 1 hour	0.6	0.55	4.5 ± 1 nm
750 °C 1 hour	-	0.3	15 ± 10 nm

These results show that even with the B concentration in the delta layer as high as 10 At% the layer can be annealed at 700 °C for 1 hour and still retain delta layer characteristics. Experiments in our laboratory on B delta layers subject to similar thermal budgets have shown that the width remains sufficiently small to allow confinement of the carriers to form a two dimensional hole gas.

Boron Delta Layers In SiGe

We have also recently measured and modelled B delta doping layers in SiGe Fig 4 shows the [113] glancing incidence rocking curve for a B delta layer with a sheet density of $1.5 \pm 0.3 \times 10^{14} \text{cm}^{-2}$ (SIMS) buried 50 nm down in a 100 nm layer of $\text{Si}_{0.84}\text{Ge}_{0.16}$.

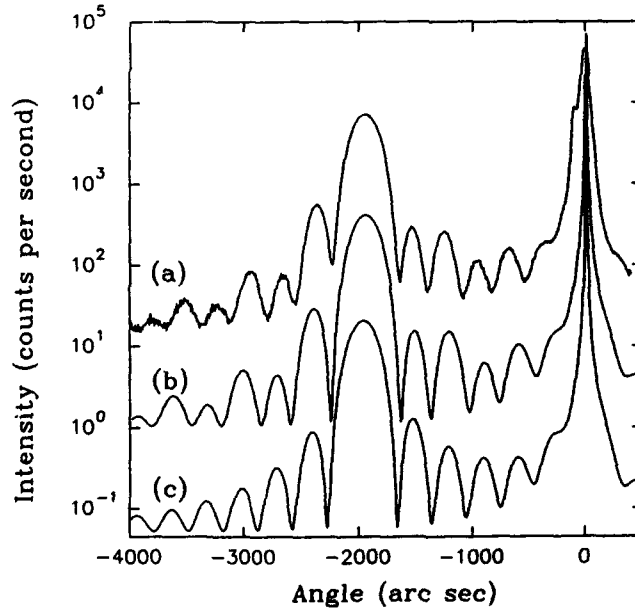


Fig 4 (a) Experimental rocking curve obtained from a 100 nm SiGe layer with a B delta layer at a depth of 50 nm. (b) Simulation with a B delta layer with a sheet density of $1.3 \times 10^{14} \text{cm}^{-2}$. (c) Simulation of the SiGe epitaxial layer with no delta layer.

With no delta layer the Pendellosung fringes decay uniformly away from the SiGe diffraction peak. The modulations of the Pendellosung peaks can be clearly seen with the delta

later present. By using dynamical theory simulation the sheet density of activated Boron was found to be $1.3 \pm 0.2 * 10^{14} \text{cm}^{-2}$ which agrees with the sheet B density as determined by SIMS. This result indicates that as with the delta layer in Si the B is fully activated in the SiGe matrix.

Conclusions

In this work we have demonstrated that X-ray diffraction is capable of resolving sub monolayer coverages of dopant atoms in both Si and SiGe. It has enabled determination of delta layer widths to high precision and shows that the majority of B present in the delta layer is contained within only one or two monolayers. It may also be used to monitor annealing effects and we have demonstrated that the delta layer characteristics are retained providing low thermal processing budgets are used.

Acknowledgements

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BORON DOPING IN SI-MBE

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ABSTRACT

We have investigated p-type doping of Si and SiGe layers in MBE by using two different boron sources. One is a SiB alloy which is prepared in situ by melting elemental boron into Si. Typical B concentrations in the source material are a few percent. Doping levels within $1 \times 10^{18} \text{ cm}^{-3}$ and $5.5 \times 10^{19} \text{ cm}^{-3}$ can be adjusted within the temperature range of 350°C to 850°C. No indication of segregation or memory effects is found. The activation is between 90 and 100%. The second p-type doping source investigated is a diborane (B_2H_6) gas source. Diborane provides doping capability in the range between 10^{16} to 10^{20} . The incorporation efficiency at 550°C is about 2×10^{-3} . It depends on the diborane exposure and the substrate temperature. The activation at 550°C is above 90%. For lower growth temperatures the activation is considerably reduced. The problem of memory effects is discussed.

INTRODUCTION

Several different species and evaporation techniques have been investigated for p-type doping in Si-MBE [1][2][3]. For several requirements such as high doping level, high incorporation, and shallow ionization level, boron is probably the most desirable candidate. Using elemental boron as source material requires very high temperatures between 1500°C and 2000°C, consequently graphite must be used as crucible material [4]. However, the vapor pressure of graphite is only some 200 times smaller than that of boron. An elemental boron source using electron bombardment heating has been presented and might provide a solution [5]. Source stability and reproducibility are concerns in this method. Another method for boron doping is the evaporation of compounds, such as B_2O_3 [6] or HBO_2 [7]. This techniques present problems at low growth temperatures, because of oxygen incorporation. In this article we report investigations on two different boron doping sources which can be used in Si-MBE. One is based on co-evaporation of an in situ prepared Si:B alloy/mixture. The second is by using a diborane gas source. SIMS, Hall-effect and spreading resistance measurements are used for characterization. The samples are prepared in a Si-MBE system using 125mm diameter Si wafers which are rotated during deposition.

SiB ALLOY SOURCE

The solid boron source used in this study is described in detail elsewhere [8]. Briefly it consists of an in-situ alloyed Si-B mixture. The exact composition of the source is difficult to ascertain, but depends on the initial composition of the prepared mixture. We have used compositions with total boron concentrations ranging from a few percent by weight to several percent, which is then fused using e-beam evaporation in the hearth of a specially engineered Si crucible, itself made of degenerately boron-doped Si. Ex-situ analysis of the fused mixture confirmed the presence of boron corresponding to the initial concentration, but the exact phases present were difficult

to identify by either X-ray or electron diffraction. However Armigliato *et al.* [9] have identified several SiB phases that are expected to precipitate after solubility limits are reached. These phases are expected to quench in when the melt solidifies after the e-beam power is turned off. We believe that the long term stability of the source is regulated by the availability of B for dissolution in the source from this phase. We expect the dissolved B to be a few percent.

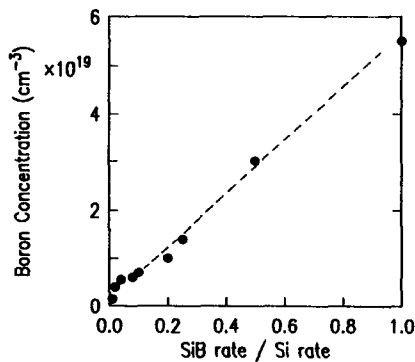
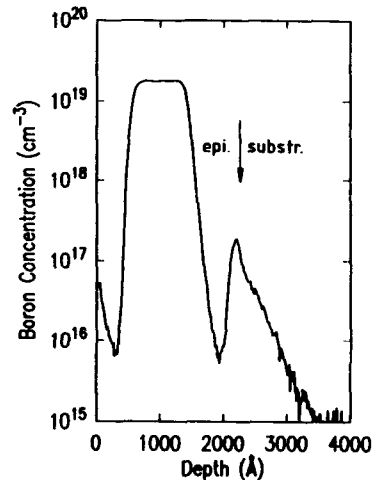


Fig. 1: Boron concentration measured by SIMS as a function of the ratio of the growth rates for the SiB alloy and the Si source.

Fig. 2: SIMS profile of the boron concentration of a structure composed of 800Å Si buffer, 1000Å boron doped Si and 500Å undoped Si cap layer. The growth rate within the doped layer was 1Å/sec for SiB alloy and 3Å/sec for Si.



Prior to initial use the source must be conditioned. This is done by fusing the source and maintaining it in a molten state. Usually, this is combined with rate calibration run where the source is run at as high a rate as permits the melt to be contained in a region well within the Si hearth. This also has the added advantage of fusing the charge to the hearth and ensuring excellent thermal sinking. Thereafter, prior to every usage, the source must be preconditioned. This consists of bringing the Si rate from the source up to the maximum rate determined in the first conditioning for a brief period. we usually grow a dummy film i.e., shutter closed, of 2 - 10 nm. The source is then brought down to standby power and is ready for use.

As we might expect, the boron flux strongly correlates to the Si flux generated by the source. This allows for convenient monitoring the B flux incident on the substrate by merely monitoring the Si flux via a rate monitor. (We use the Sentinel III rate monitor). Furthermore, the Si rate can be feed-back controlled which permits for a very stable boron flux. In practice, we use two sources for Si, one which is essentially undoped and the other being the Si:B source. The doping level in the film, can be controlled by adjusting the ratio of Si from the Si:B source to that from the pure Si source. Fig. 1 shows the doping level in the film as a function of this ratio. To within the accuracy of SIMS, the doping level is proportional to this ratio. The Si growth rate is the sum of these two fluxes. The dynamic range of doping levels that are obtainable from this source depends on the flux control capability one has. Typically for

our system this is about a factor of 50. Thus for a typical source this allows us to dope from about $5 \times 10^{19} \text{cm}^{-3}$ to $1 \times 10^{18} \text{cm}^{-3}$ a useful range for most device applications. Fig. 2 shows the SIMS profile for boron from this source. The Si rate from the Si:B source was 1Å/sec and that from the pure Si source 3Å/sec . The profile is flat over the entire thickness of the film and falls to the SIMS background of $1 \times 10^{16} \text{cm}^{-3}$ abruptly. (SIMS resolution is about 15nm/decade .) The doping level obtained is experimentally found to be independent of growth temperature for the entire dynamic doping range for temperatures between 350°C - 850°C making it an extremely unique doping source. Oxygen levels were measured to be comparable to SIMS background levels i.e., below $1 \times 10^{16} \text{cm}^{-3}$.

The structural quality of homoepitaxial films grown using this source has been evaluated by planar Transmission Electron Microscopy and defect etching. Using the later technique an upper limit of $1 \times 10^3 \text{cm}^{-2}$ was estimated. Hall and spreading resistance measurements show that the boron is almost fully activated for all temperatures of growth attempted. Hall mobilities were measured to be within 80% of bulk mobilities.

Several devices have been fabricated using B from this source. These include heterojunction bipolar transistors [10], and multi-quantum well (MQW) pin detectors [11]. These devices require ultra-sharp doping transitions. Indeed, we have grown doping superlattices and see no evidence for smearing or segregation of B at least to the mid 10^{19}cm^{-3} level. We have also used this source extensively to dope $\text{Si}_{1-x}\text{Ge}_x$ films with excellent results. In summary, this source has been found to be a clean efficient and versatile source and is easily implemented using an e-beam evaporator.

B_2H_6 GAS SOURCE

Diborane is mainly used in CVD growth techniques for p-type doping in Si and SiGe epilayers [12][13]. In this section we report measurements to the doping properties of a diborane gas source in a solid source Si MBE system. The doping gas consists of electronic grade 1% B_2H_6 diluted in H_2 . The partial pressure of $\text{B}_2\text{H}_6:\text{H}_2$ in the growth chamber is adjusted manually through a leak valve. It is measured using a remote ion gauge which is not in direct view of the substrate to avoid B_2H_6 cracking. The diborane is delivered to the substrate by a gas injector that terminates 300mm in front of the substrate.

Fig. 3 shows a SIMS profile of a boron doped Si epilayer. The doping level was adjusted by changing the $\text{B}_2\text{H}_6:\text{H}_2$ pressure and the Si growth rate was 2Å/sec . In the highest doped layer (100nm below the surface), which is 25nm the Si flux was reduced to 0.2Å/sec and the $\text{B}_2\text{H}_6:\text{H}_2$ pressure was 2×10^{-4} mbar. The substrate temperature for the sample shown in Fig. 3 was $T_s = 550^\circ\text{C}$. The measured boron concentration follows the nominally adjusted boron profile within 50%. However, after the last 250Å thick layer which is doped to almost $1 \times 10^{20} \text{cm}^{-3}$ the doping level did not come all the way down as expected indicating a considerable memory effect. It takes about 20 minutes after closing the leak valve to get the pressure in the system down below 1×10^{-4} mbar if the $\text{B}_2\text{H}_6:\text{H}_2$ pressure was 1×10^{-5} mbar for 10 minutes. The growth chamber is pumped by a cryopump and an ionpump. A considerable reduction of the memory effect can probably be achieved by using a turbopump. Turbo pumps are usually employed in gas source MBE to avoid saturation when exposed to high gas loads.

Fig. 3: Boron concentration profile of a Si epilayer grown at $T_g = 550^\circ\text{C}$. B_2H_6 was used as doping source. The doping level was adjusted by changing the ratio between the $\text{B}_2\text{H}_6:\text{H}_2$ pressure and the Si growth rate. The arrow indicates the interface between substrate and epilayer.

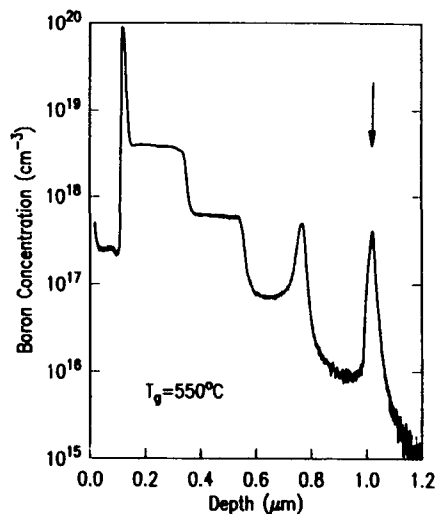


Fig. 4 shows the boron concentration measured by SIMS as a function of the $\text{B}_2\text{H}_6:\text{H}_2$ pressure normalized to the growth rate for different diborane doped Si and SiGe alloy layers. Three different substrate temperatures were used. The incorporation within this doping levels is almost linear and corresponds to an incorporation rate of $(2 \pm 1) \times 10^{-3}$. The Si growth rate was always between 0.2 and $4 \text{ \AA}/\text{sec}$. Hall and spreading resistance measurements indicate, that the activation is 100% and about 90% for the growth temperatures of 750°C and 550°C respectively. Whereas, only $(20 \pm 10)\%$ of the incorporated boron atoms are electrically active in the samples grown at 400°C . Thermal desorption measurements for B_2H_6 adsorpt on Si surface were performed by Yu et. al. [14]. They reported a H_2 desorption peak between 400°C and 500°C . This suggests, that the B_2H_6 molecules are not completely decomposed at 400°C . In addition some hydrogen could be incorporated in the growing film and cause electrical passivation of the boron atoms. After annealing at 650°C for 30 minutes the activation for the samples grown at 400°C did not increase significantly. The limited carrier activation at low substrate temperatures may be a problem for doping of SiGe alloy layers with high Ge concentrations, which must be grown at low temperatures to avoid relaxation and three dimensional growth.

Fig. 4: Boron concentration measured by SIMS as a function of the $\text{B}_2\text{H}_6:\text{H}_2$ partial pressure in the system normalized to the growth rate.

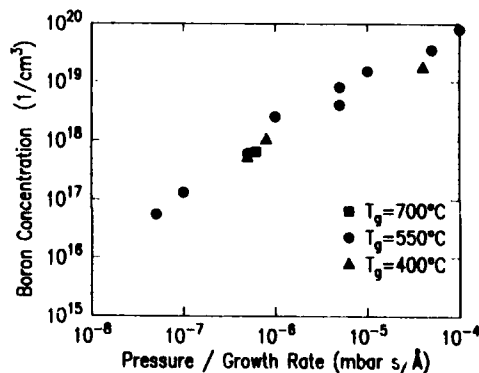


Fig. 5: Boron concentration profile of a delta doped Si layer. The doping was performed by exposing the Si surface to a $B_2H_6:H_2$ pressure of 1×10^{-6} for 600 sec.

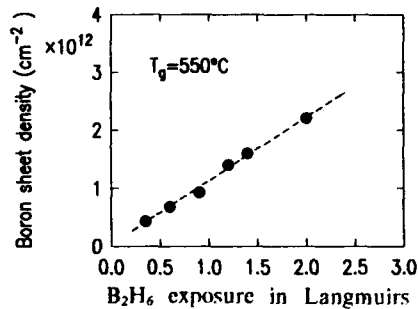
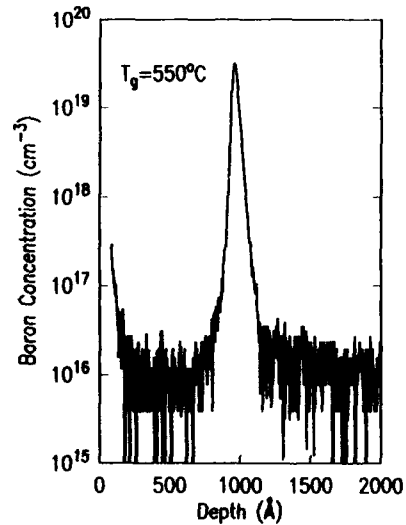


Fig. 6: Boron sheet density versus B_2H_6 exposure in Langmuirs ($1L = 1 \times 10^{-6}$ Torr s).



We have achieved sharp doping profiles using the diborane gas source by introducing a growth interruption after closing the leak valve and before growing the undoped Si cap layer as shown in Fig. 5. The delta doping was accomplished by exposing the surface of a 3000Å thick Si buffer to a $B_2H_6:H_2$ pressure of 1×10^{-6} mbar for 600 sec. The growth interruption was 30 minutes. As substrate we used 40-60Ωhcm Si (001). The thickness of the Si cap layer is 1000Å. The whole structure was grown at $T_g = 550^\circ\text{C}$. The carrier density and the mobility are $5 \times 10^{12} \text{cm}^{-3}$ and $150 \text{cm}^2/\text{Vs}$ respectively, as determined by Hall measurement. Fig. 6 shows the B sheet density measured as the integrated density in SIMS as a function of the B_2H_6 exposure in Langmuirs ($1L = 1 \times 10^{-6}$ Torr s). The samples are composed of a delta layer similar to the sample shown in Fig. 4 but without a growth interruption. Within the region shown in Fig. 6 the boron coverage is linear with exposure and the rate is about $1.1 \times 10^{12}/L$ at 550°C . The sticking coefficient is 1.5×10^{-3} in this case. With further increasing coverage the sticking coefficient reduces. For boron coverages which are higher than 10^{14}cm^{-3} the sticking coefficient is found to be about 0.3×10^{-3} [14].

CONCLUSIONS

We demonstrated, that both Si:B alloy coevaporation and a B_2H_6 gas source can be used for p-type doping up to $1 \times 10^{20} \text{cm}^{-3}$ in Si MBE. For both techniques there is no O and C contamination of the doped layer detected in SIMS. Sharp doping profiles can also be achieved using the B_2H_6 gas source by introducing a growth interruption after the deposition of the doped layer in order to pump the remaining B_2H_6 out. Pre-cracking of the B_2H_6 molecules is expected to increase the sticking coefficient and the electrical activation of the boron atoms especially at low growth temperatures.

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PART III

GeSi Growth

MBE Alloy Clustering Kinetics - A Stochastic Model Study

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Abstract

A theoretical study of alloy clustering in an hypothetical diamond cubic alloy, $a_{0.5}b_{0.5}$ in which thermodynamics favors phase separation is performed based on a master equation approach. The a-b atom pair interaction is assumed weaker and repulsive (-0.25 eV). It is shown that below 375°C, due to negligible surface migration, there is no clustering of the alloy, but, the surface roughness is very large. In the intermediate temperature range of 300 – 625°C, with increasing temperature, surface migration increases, resulting in more clustering and decreased surface roughness. Above 500°C, due to very high surface migration, complete phase separation and smooth surface result. It is shown that the conventional MBE growth techniques are incompatible with the growth of good quality heterostructures which consist of alloys having large positive enthalpy of mixing.

1. Introduction

Clustering in alloys can occur during fabrication of the heterostructures by conventional MBE or MOCVD if the heat mixing of the alloy is very large. The phenomenon of clustering is dictated by both the thermodynamics of the alloy and the kinetics of the growth process. Nonequilibrium nature of the MBE growth can be exploited to grow cluster-free alloys by a proper choice of growth conditions.

Experimental work based on photoluminescence line width of the excitonic spectra and transport properties of MBE grown heterostructures consisting of ZnS_xSe_{1-x} and $In_{1-x}Al_xAs$ alloys have indicated the presence of alloy clusters [1-4]. The role of kinetics and thermodynamics in alloy clustering of MBE grown $InGaAs$ has been studied theoretically by Singh et al [5].

In this manuscript, the stochastic model approach discussed in Ref.[6,7] is employed to study the MBE alloy clustering kinetics. In section 2, development of the stochastic model for the MBE alloying studies is discussed. A hypothetical diamond cubic alloy, $a_{0.5}b_{0.5}$ for which enthalpy of mixing is large positive value is chosen. The results of MBE clustering kinetic study of this alloy is presented in Section 3. A discussion of the results of this study in the context of suitability of conventional MBE growth technique for growing good quality heterostructures, is also presented in section 3. Conclusions are stated in Section 4.

2. Stochastic Model for Alloy Kinetic Studies

In this section, the necessary modifications to the stochastic model to make it suitable for alloying of a sublattice is presented. The growth direction is chosen as [001].

2.1 Macrovariables

Let us consider an hypothetical diamond cubic alloy, $a_{0.5}b_{0.5}$, in which both a and b belong to the same sublattice. The number of macrovariables necessary for the description of the time evolution of the binary alloy of the type mentioned, is five, unlike the case of a binary compound semiconductor, in which it is only four. This difference is due to the fact that both the elements belong to the same sublattice in the alloy, whereas in the case of binary compound semiconductor, the elements belong to two different sublattices.

tices. The macrovariables considered for a layer n , are: concentration variables, $C_a(n)$ and $C_b(n)$, atom-vacancy bond densities, $Q_a(n)$ and $Q_b(n)$ and a-b bond density, $\tilde{N}_{ab}(n)$. These macrovariables are related to the bond densities of the other three types of bonds, a-a, b-b and v-v bonds, as:

$$\tilde{N}_{aa}(n) = 2 C_a(n) - \frac{1}{2} Q_a(n) - \frac{1}{2} \tilde{N}_{ab}(n)$$

for a-a bond density,

$$\tilde{N}_{bb}(n) = 2 C_b(n) - \frac{1}{2} Q_b(n) - \frac{1}{2} \tilde{N}_{ab}(n)$$

for b-b bond density and

$$\tilde{N}_{vv}(n) = 2 (C_v(n)) - \frac{1}{2} Q(n) \quad (1)$$

where

$$C_v(n) = (1.0 - C(n))$$

and

$$C(n) = C_a(n) + C_b(n)$$

and

$$Q(n) = Q_a(n) + Q_b(n)$$

where $C_v(n)$ is the vacancy density, and $C(n)$ is the total atom concentration in the n^{th} layer. In Eq 1, the inplane coordination number is four.

2.2 Derivation of the Kinetic Equations

The time evolution of the primary macrovariables, $C_a(n)$, $C_b(n)$, $Q_a(n)$, $Q_b(n)$ and $\tilde{N}_{ab}(n)$ can be derived by a similar approach using the random distribution approximation and the master equation scheme discussed elsewhere [6]. The introduction of the additional macrovariable, $\tilde{N}_{ab}(n)$ warrants modifications in the terms involving pair interaction energies and also an additional time evolution equation for the macrovariable, $\tilde{N}_{ab}(n)$. These modifications are discussed below.

The fraction of a layer exposed to vapor so that it is free to migrate or evaporate, $(C(n) - 2C(n+1) + \frac{\tilde{N}_{cc}(n+1)}{2})$ consists of both a and b atom fractions. The fraction of exposed a and b atoms which appear in the time evolution equation, are approximately taken as:

$$C_a(n) \text{ (exposed)} = \left(\frac{C_a(n)}{C(n)} \right) \left(C(n) - 2C(n+1) + \frac{\tilde{N}_{cc}(n+1)}{2} \right)$$

and

$$C_b(n) \text{ (exposed)} = \left(\frac{C_b(n)}{C(n)} \right) \left(C(n) - 2C(n+1) + \frac{\tilde{N}_{cc}(n+1)}{2} \right) \quad (2)$$

where $\tilde{N}_{cc}(n+1)$ is given by:

$$\tilde{N}_{cc}(n+1) = \tilde{N}_{aa}(n+1) + \tilde{N}_{bb}(n+1) + \tilde{N}_{ab}(n+1)$$

The four nearest neighbor sites around either a or b atom in an alloy can be occupied by a combination of vacancies, a atoms and b atoms. Therefore, the binding energy of an atom in an alloy depends on the numbers of vacancy, a atom and b atom as nearest neighbors. Because of this difference, the pair interaction energy terms appearing in evaporation, and intralayer and interlayer migration terms need to be modified as:

$$\left[\frac{\tilde{N}_{cc2a}(2n)e^{-K_a} + 1/2q_a(2n)e^{K_a}}{2c_a(2n)} \right]^2 \rightarrow \left[\frac{\tilde{N}_{aa}(n)e^{-2k_{aa}} + \tilde{N}_{ab}(n)e^{-2k_{ab}} + 1/2Q_a(n)}{2C_a(n)} \right]^2$$

for a atoms and

$$\left[\frac{\tilde{N}_{ca2b}(2n)e^{-K_b} + 1/2q_b(2n)e^{K_b}}{2c_a(2n)} \right]^z \rightarrow \left[\frac{\tilde{N}_{bb}(n)e^{-2k_{aa}} + \tilde{N}_{ab}(n)e^{-2k_{ab}} + 1/2Q_b(n)}{2C_b(n)} \right]^z$$

for b atoms, where z is 3 or 4 as discussed in Ref.[6] and $2k_{aa}$, $2k_{bb}$ and $2k_{ab}$ are the pair interaction energies of a-a, b-b and a-b atom pairs.

With these modifications, the time evolution equations for the macrovariables, $C_a(n)$, $C_b(n)$, $Q_a(n)$, and $Q_b(n)$ are derived. These equations are similar to those reported in Ref.[5] and are not presented here due to limited space. The additional time evolution equation for the macrovariable, $\tilde{N}_{ab}(n)$ can be derived in terms of the incorporation, evaporation, and intra- and inter-layer migration processes. This additional equation is very similar to the ones for the other macro-variables and is not presented here due to lack of space.

2.3 Hypothetical Alloy System and Model Parameters

The alloy system studied is $a_{0.5}b_{0.5}$ diamond cubic alloy, in which a-a and b-b second nearest neighbor pair interactions are identical (0.25eV), but a-b pair interaction is weaker or repulsive (-0.25eV). In other words, in the alloy system chosen thermodynamics favors phase separation. The model parameters employed in this study are reported in Table I for various growth temperatures. The flux rate was chosen as 0.7 atoms/sec for a and b type atoms, so that the flux ratio was 1.0. The temperature range of (300 - 525°C) is chosen for this study.

Since the equations governing the time evolution of the macrovariables are coupled nonlinear first order differential equations and were numerically integrated using a predictor-corrector numerical integration scheme on a SUN Sparc station. The average computational time for a typical growth of 5-8 monlayers was 5 CPU hours.

3. Results and Discussion

The macrovariables, $c_a(n)$, $c_b(n)$, $q_a(n)$, $q_b(n)$, and $\tilde{N}_{ab}(n)$ were obtained as a function of time for various temperatures in the range of (300-525°C). The growth rate, G (atoms/sec.) and the time averaged surface roughness parameter, $(\sum q_i)_{ave}$, were obtained for various temperatures. The short range order parameter, SRO, given by:

$$SRO = \frac{\sum_{i=1}^{i=5} \left(\frac{\tilde{N}_{aa}(n) + \tilde{N}_{bb}(n) - \tilde{N}_{ab}(n)}{C(n)} \right)}{\sum_{i=1}^{i=5} \left(\frac{\tilde{N}_{aa}(n) + \tilde{N}_{bb}(n) + \tilde{N}_{ab}(n)}{C(n)} \right)} \quad (3)$$

were evaluated for various temperatures. The layers numbered 1 to 5 are the first five layers and are about 95% complete. Plots of SRO parameter versus temperature, growth rate versus temperature and roughness parameter versus temperature are shown in Figures 1a-c, respectively.

The SRO parameter is constant and zero below 375°C indicating completely random alloy. At temperatures above 500°C, it is constant and is almost equal to unity, indicating complete phase separation. In the intermediate temperature range of 375 - 500°C, the SRO parameter increases with increasing temperature due to surface migration induced clustering of the alloy.

In the temperature range below 375°C, the intralayer and interlayer migrations are small. Therefore, the randomly adsorbed atoms stay at sites of their incorporation, resulting in a perfectly random alloy with negligible clustering. In the high temperature range above 500°C, the surface migration rates are very high resulting in breaking of weaker a-b

Table I. The model parameters, flux parameter, L , adsorption and evaporation time constant, τ_r , surface diffusion parameter, τ_d , and the second nearest neighbor pair interaction energy parameters, k and k_{ab} , for various substrate temperatures. It is assumed that $L = L_a = L_b$, $k = k_{aa} = k_{bb}$, $\tau_r = \tau_{ra} = \tau_{rb}$ and $\tau_d = \tau_{da}^{inter/intra} = \tau_{db}^{inter/intra}$.

T(°K)	$\tau_r(sec.)$	L	$\tau_d(sec.)$	k	k_{ab}
548	8.43×10^{28}	61.64	9299.0000	5.286	-1.057
573	1.33×10^{25}	57.49	1469.3000	5.055	-1.011
598	2.96×10^{23}	53.69	270.8860	4.844	-0.969
623	8.93×10^{21}	50.19	57.2000	4.650	-0.930
648	3.54×10^{20}	46.96	13.6180	4.471	-0.894
673	1.78×10^{19}	43.97	3.6070	4.305	-0.861
698	1.11×10^{18}	41.19	1.0510	4.151	-0.830
723	8.39×10^{16}	38.61	0.3333	4.007	-0.801
748	7.52×10^{15}	36.20	0.1140	3.873	-0.775
773	7.90×10^{14}	33.94	0.0420	3.748	-0.750
798	9.55×10^{13}	31.83	0.0160	3.631	-0.726
823	1.31×10^{13}	29.848	0.0068	3.521	-0.704
898	6.60×10^{10}	24.557	0.0006	3.227	-0.645

G atoms/sec., SRO parameter ($\sum q_i$)_{ave} (arb. units),
 ($\sum q_i$)_{ave} (arb. units)

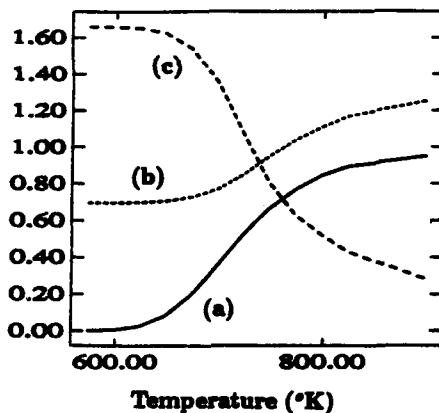


Fig. 1. Temperature dependence of (a) SRO parameter (b) growth rate G (atom/sec.) and (c) surface roughness parameter, $(\sum q_i)_{ave}$.

bonds and favoring stronger a-a and b-b bonds. This kinetic effect of increased surface migration results in the formation of a and b clusters. In the intermediate temperature range of 375 – 500°C, as the temperature increases, the surface migration increases, providing more opportunities for breaking weaker a-b bonds and forming stronger a-a and b-b bonds, which results in increased clustering with increasing temperature.

The effect of increased surface migration is also evidenced in the behavior of growth rate and surface roughness with temperature as shown in Figure 1b,c and is discussed below. Below 375°C, the surface migration rate is negligible and therefore, the subsurface layers are

inefficiently packed and at a slower rate. Thus, the growth rate small and the surface is very rough. In the intermediate temperature range of 375–500°C, as the temperature increases the surface migration rate increases. There are also a large number of less efficiently packed subsurface layers in to which interlayer migration can result. Thus, the subsurface layers fill up more efficiently and faster, resulting in newer sites on the top surface layer for more atoms to adsorb. This surface phenomenon results in increased growth rate with increasing temperature. At temperatures above 500°C, still the surface hop rate is very high, but, the number of available subsurface layer sites for interlayer migration saturates and therefore, the number of newer sites created for adsorption becomes a constant with increasing temperature. Thus, the growth rate becomes a constant. Due to the same kinetic effect, the minimum surface roughness reachable is attained around 500°C and therefore, the surface roughness does not change any further with increasing temperature.

To fabricate heterostructures with sharp interfaces and good stoichiometry, high growth temperatures are preferred. But, high growth temperature causes alloy clustering as discussed in the context of Figure 1a. To avoid alloy clustering, it is preferable to adopt low growth temperatures. But, low growth temperatures usually result in rough interfaces and poor stoichiometry as indicated by Figure 1c. Thus, this study shows that for the hypothetical alloy system chosen, the conventional MBE growth is incompatible with the growth of heterostructures of materials in which phase separation is favored by thermodynamics. These conclusions are general and may not apply to all realistic alloy systems. Experimentally, a growth temperature window can usually be found for most alloy systems, with in which good quality hetero-structures can be grown.

4. Conclusion

A stochastic model for studying kinetics of alloy clustering is developed. A hypothetical alloy system, $a_{0.5}b_{0.5}$ in which thermodynamics favors phase separation (a-b atom pair interaction energy = -0.25 eV) is studied for clustering behavior. As expected, high temperature favors alloy clustering. It is shown that conventional MBE growth is unsuitable for growing heterostructures with the hypothetical alloy system chosen having sharp interfaces and homogeneous alloys.

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COMPARISON OF GROWTH AND STRAIN RELAXATION OF Si/Ge SUPERLATTICES
UNDER COMPRESSIVE AND TENSILE STRAIN FIELD

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ABSTRACT

Optimization of growth parameters of short period Si/Ge superlattices (SLs) has been achieved via *in situ* low-energy electron diffraction (LEED) and Auger electron spectroscopy (AES) measurements during homo- and heteroepitaxy on Si(001) and Ge(001) substrates. Transmission electron microscopy (TEM) reveals that pseudomorphic $\text{Si}_m\text{Ge}_{12-m}$ ($m = 9$ and 3 for growth on Si and Ge, respectively) SLs with extended planar layering can be prepared almost defect-free by a modified molecular beam epitaxy (MBE) technique. Whereas the SLs on Ge can be deposited at a constant substrate temperature, high-quality growth on Si demands for temperature variations of more than 100°C within one superlattice period. Strain relaxation of these SLs with increasing number of periods has been directly compared by means of TEM. For the compressively strained structures grown on Si we found misfit dislocations of the type $60^\circ (a/2)\langle 110 \rangle$. Under opposite strain conditions i.e. for growth on Ge, strain relief occurs only by microtwin formation through successive glide of $90^\circ (a/6)\langle 211 \rangle$ Shockley partial dislocations. This is consistent with a calculation of the activation energy for both cases based on a homogeneous dislocation nucleation model.

INTRODUCTION

Pseudomorphic Si/Ge alloys and superlattices are among the most promising materials in view of novel device applications such as the heterojunction bipolar transistor (HBT) or the modulation-doped field effect transistor (MODFET). However, due to the 4.2 % lattice mismatch between Si and Ge, the overall thickness of such structures is limited. The lattice mismatch, on the other hand, causes pseudomorphic layers to be strained which can be positively exploited for band-structure engineering [1]. For example a direct band-gap material is only expected for a Si/Ge SL if the strain is accommodated by the Si layers which can be realized by using a $\text{Si}_x\text{Ge}_{1-x}$ buffer layer or a Ge substrate. [2]. Since the misfit dislocations, which are generated at the critical thickness to relax part of the mismatch-induced strain, are undesirable in the electrically active region of semiconductor devices, the understanding of strain relaxation is of particular importance. Although there exists extensive theoretical and experimental work on this subject [3] a direct comparison of strain relief in inversely strained Si/Ge SLs i.e. under compressive and tensile strain field, has not been reported so far.

In this paper we present a detailed investigation of growth and strain relaxation of equivalent structures pseudomorphically grown on [001] oriented Si and Ge substrates. First, the consequences of the substrate material on the growth conditions of short-period Si/Ge SLs are discussed on the basis of LEED and AES results. Starting from almost perfect superlattices we then report on a TEM investigation of the transition from coherent to incoherent growth on both substrate types with increasing superlattice thickness.

EXPERIMENTAL

MBE growth of homoepitaxial [Si on Si(001) and Ge on Ge(001)] and 1 ML thick heteroepitaxial layers [Ge on Si(001) and Si on Ge(001)] has been studied by LEED and AES as a function of the substrate temperature T_s . Spot profiles of the (00) reflection

have been recorded in the energy range from 18 eV to 180 eV. Samples with SLs having a unit cell of 3 ML Ge (Si) and 9 ML Si (Ge) in the [001] direction were prepared on Si (Ge) substrates [Si_3Ge_3 on Si(001) and Si_3Ge_9 on Ge(001)]. Thus, by treating the superlattice as an alloy with the same average composition [4], the absolute value of the misfit f [$f \equiv (a_s - a_o)/a_o$, a_s and a_o are the intrinsic lattice constants of substrate and film] between SL and substrate is about 1% for pseudomorphic structures on both substrate materials. We used extremely low growth rates of ≈ 0.1 nm/min and ≈ 0.5 nm/min for Si and Ge, respectively. Details of the MBE system have been presented elsewhere [5]. Cross-sectional TEM specimens were prepared in [110] orientation by mechanically polishing and Ar ion milling. Microscopy was performed in a 200 kV (JEOL 200 CX) and a 400 kV (JEOL 4000 EX) instrument.

RESULTS AND DISCUSSION

Figure 1 shows the mean terrace widths of Si and Ge surfaces measured by LEED spot profile analysis following the concept of Henzler [6]. After deposition of

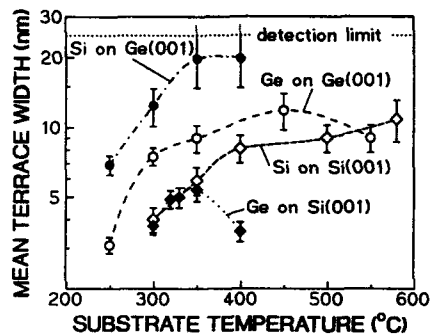


Fig. 1: Mean terrace widths after Si and Ge growth on Si(001) and Ge(001) substrates as a function of the substrate temperature.

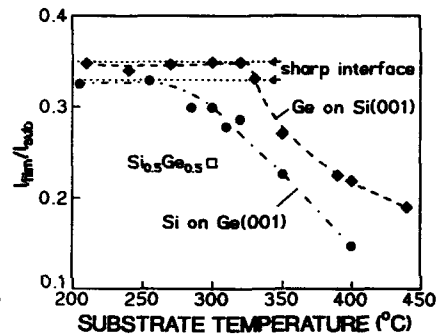


Fig. 2: Normalized film/substrate AES intensity ratio for heterointerfaces on Si(001) and Ge(001) substrates as a function of the substrate temperature.

1 ML Si on Ge at $T_s = 350^\circ\text{C}$ and $T_s = 400^\circ\text{C}$, extended terraces with a mean width at the detection limit of the LEED-system (≈ 25 nm) are obtained. For the reverse case of 1 ML Ge on Si the mean terrace widths are considerably smaller. However, there is a maximum in terrace width in the temperature range of 310°C to 360°C . For homoepitaxial growth, optimum surface quality is achieved at $T_s = 700^\circ\text{C}$ and $T_s = 450^\circ\text{C}$ for Si and Ge, respectively. Although smoother surfaces can be prepared on Si at these high substrate temperatures which have been used for buffer layer growth, the Ge surfaces exhibit larger terraces at temperatures below 500°C as can be seen in Fig. 1. In addition to this information about the surface morphology, we evaluated the AES intensities of the $\text{Si}^{29\text{eV}}$ and $\text{Ge}^{47\text{eV}}$ lines to study interface sharpness and intermixing at the heterointerfaces. The normalized film/substrate intensity ratios of 1 ML Ge on Si(001) and 1 ML Si on Ge(001) as a function of T_s are depicted in Fig. 2. The expected values for atomically sharp interfaces are indicated. Whereas we observe a deviation from the ideal curve already at $T_s = 280^\circ\text{C}$ for the Si/Ge(001) interface, Ge growth on Si(001) produces a sharp interface even at $T_s = 320^\circ\text{C}$. This different behaviour for the two substrate materials is mainly caused by the tendency of Ge to segregate on the Si layer [7]. Only at higher temperatures diffusion-induced intermixing must be taken into account. In order to provide information on the sensitivity of this measurement we also included the AES intensity ratio of a 2 ML thick $\text{Si}_{0.5}\text{Ge}_{0.5}$ alloy layer grown on Ge(001) ($T_s = 300^\circ\text{C}$) in Fig. 2.

As a consequence, in view of atomically abrupt superlattice structures, T_s should be below about 320°C and 280°C during the formation of the interfaces

(Fig. 2). However, especially for high-quality growth on Si substrates this low temperature is clearly unacceptable (Fig. 1). For this reason the substrate temperature during deposition of a Si_3Ge_3 SL on Si [Fig. 3(a)] has to be modulated according to the temperature profile shown in Fig. 4. In this case the optimum substrate

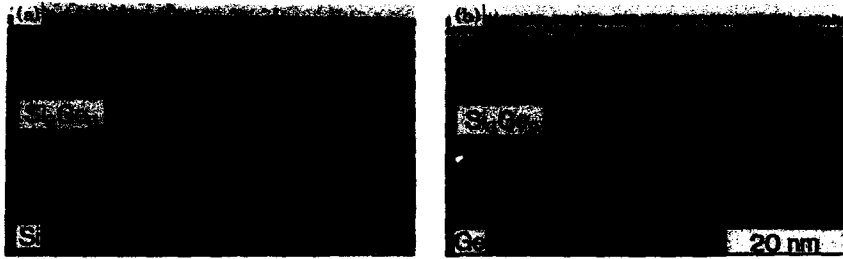


Fig. 3: TEM cross sections of 20-period Si_3Ge_3 (a) and Si_3Ge_9 (b) SLs on Si(001) and Ge(001) substrates using the (004) bright-field condition near the [110] zone axis.

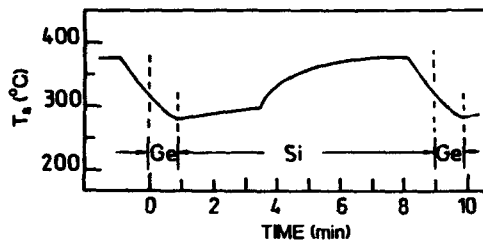


Fig. 4: Optimized substrate temperature profiles during growth of the Si_3Ge_3 SLs on Si(001). The dashed vertical lines mark the times when the Si or Ge shutter is opened.

temperatures of 320°C and 280°C have been adjusted when the interfaces are formed. After deposition of about 3 ML Si, however, T_s has been increased during growth of the following 5 ML Si to about 380°C. This leads to an enlargement of the mean terrace width to about 8 nm (Fig. 1). In order to achieve maximum surface flatness even higher temperatures would be required. This would cause, on the other hand, increased intermixing and Ge segregation. For growth on Ge(001) the mean terrace widths at $T_s = 310^\circ\text{C}$ are already above 8 nm for both materials. As a consequence a Si_3Ge_9 SL can be grown at a constant temperature of 310°C on Ge [Fig. 3(b)]. However, substrate temperature modulation in the range of 280°C to 340°C should lead to a further improvement of the interface quality.

As can be seen on the cross-sectional bright-field images of Fig. 3, 20-period SLs with extended planar layering can be prepared on both substrate types by this low-temperature growth technique. The parallel bright and dark lines correspond to the individual Si and Ge layers. Although there are only relatively small regions visible in Fig. 3, almost the whole TEM specimen area transparent to the electron beam exhibits defect-free (dislocation density $\leq 10^6/\text{cm}^2$) perfectly layered superlattice structures. This material system is therefore well suited to compare directly strain relaxation at positive and negative misfit values when the critical thickness is exceeded. For this reason a TEM investigation of 40, 60 and 120-period $\text{Si}_3\text{Ge}_3/\text{Si}(001)$ and $\text{Si}_3\text{Ge}_9/\text{Ge}(001)$ superlattice structures has been carried out. Figure 5 - bright-field images with the (004) reflection strongly excited - summarizes the results. Whereas the lattice mismatch between the 40-period Si_3Ge_3 SL and the Si substrate is completely absorbed by elastic strain, we observed planar misfit defects in the corresponding superlattice on Ge [Fig. 5(b)]. We recently identified these defects as stacking faults (STFs) and microtwins lying on the (111) lattice planes [8]. Based on a high-resolution electron microscopy study of the twin ends [marked by arrows in Fig. 5(b) and (d)] which reveals the presence of $90^\circ (a/6)\langle 112 \rangle$ Shockley partial dislocations at the twin boundaries, the following model for the relaxation mechanism of these tensely

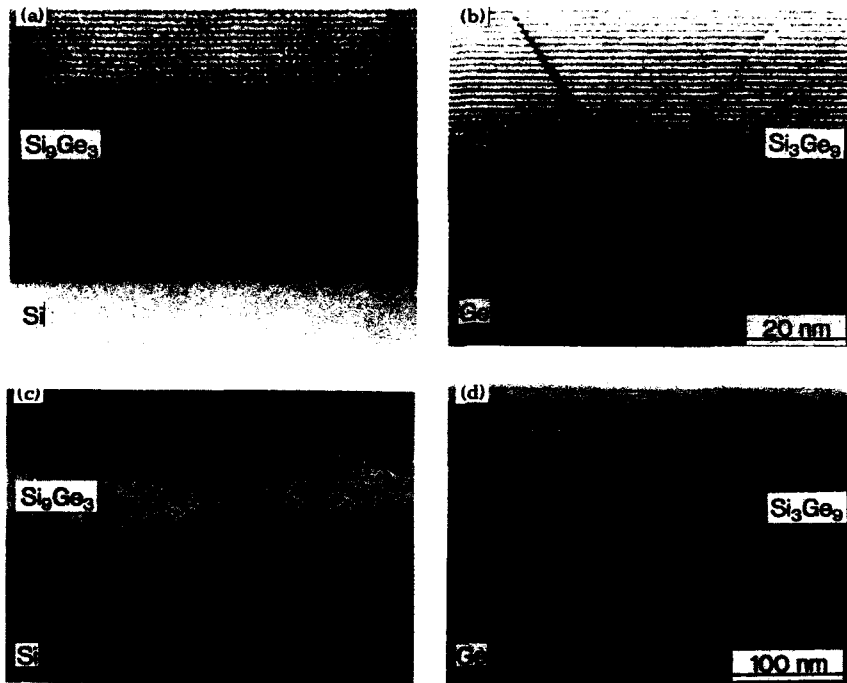


Fig. 5: Cross-sectional bright-field images [$g = (004)$] of 40 period $\text{Si}_3\text{Ge}_3/\text{Si}(001)$ (a) and $\text{Si}_3\text{Ge}_3/\text{Ge}(001)$ (b) as well as 120-period $\text{Si}_3\text{Ge}_3/\text{Si}(001)$ (c) and $\text{Si}_3\text{Ge}_3/\text{Ge}(001)$ (d) superlattice structures. The arrows indicate misfit dislocations.

strained structures has been proposed [8]. When the critical thickness for pseudomorphic growth is exceeded, 90° partial dislocations successively nucleate on adjacent $\{111\}$ planes probably at a surface step and glide down towards the SL/substrate interface. In this way an intrinsic STF, an extrinsic STF and finally a microtwin is formed. With each partial dislocation, the thickness of the microtwins increases by one $\{111\}$ plane as shown in the high-resolution lattice image of Fig. 6.

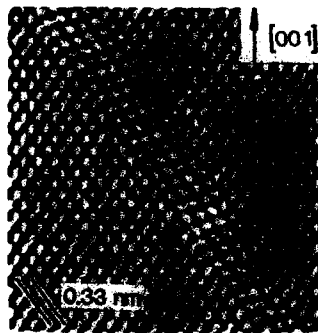


Fig. 6: High-resolution lattice image in $[110]$ projection of a 90° partial dislocation leading to a widening of the microtwin.

TEM micrographs of the 60-period SLs (not shown) reveal again the absence of misfit dislocations for growth on Si and strain relaxation through the formation of microtwins for growth on Ge. At a superlattice thickness of 120 periods, however, we observe in the compressively strained structures on Si misfit dislocations lying in the SL/Si interface [one example can be seen in Fig. 5(c)]. They show only a dot-type contrast at the imaging conditions chosen for Fig. 5 since the electron beam has been aligned almost parallel to the dislocation line ($[110]$ direction). A complete two-beam $g\cdot b$ characterization (Fig. 7) with the specimen tilted to the $[1\bar{1}\bar{1}]$ and the $[211]$ poles clearly identifies the dislocations to be of $60^\circ (a/2)[\bar{1}01]$ type. The $g\cdot b = 0$ invisibility criterion is fulfilled when imaging is carried out with (202) and (131)

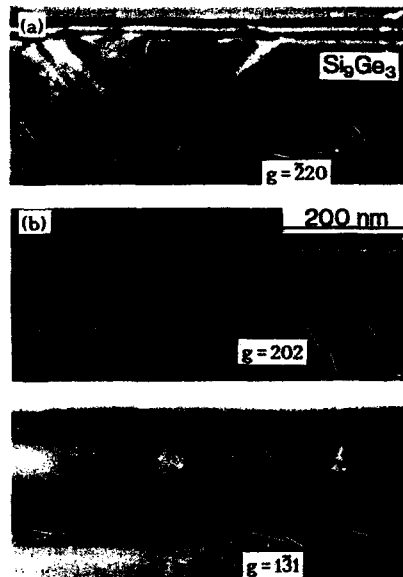


Fig. 7: Cross-sectional bright-field images of the 120-period Si_3Ge_3 SL on Si(001) close to the $[110]$ (a), $[11\bar{1}]$ (b) and $[211]$ (c) poles recorded with different diffraction vectors. The arrows mark the interfacial dislocations.

Table I: Product of the relevant Burgers vectors of $(a/2)\langle 110 \rangle$ dislocations lying along the $[110]$ direction with the diffraction vectors used in Fig. 7.

	g	$(\bar{2}20)$	(202)	$(1\bar{3}1)$
60°	$\frac{1}{2}[011]$	1	1	-1
	$\frac{1}{2}[\bar{1}01]$	1	0	0
	$\frac{1}{2}[10\bar{1}]$	-1	2	1
	$\frac{1}{2}[0\bar{1}1]$	-1	1	2
0°	$\frac{1}{2}[110]$	0	1	-1
90°	$\frac{1}{2}[1\bar{1}0]$	-2	1	2

diffraction vectors. For pure screw or edge dislocations of this type, distinct contrast should be visible on both of these images (Table I). In addition to the interfacial dislocations Fig. 7 shows also threading dislocations which seem to nucleate at a node near the SL/Si interface. We attribute these dislocations to growth defects which may be caused by contaminations at the starting surface. Although there is no direct evidence for a correlation between the dislocation nodes and the interfacial misfit dislocations in the cross-sectional specimen, it is conceivable that they act as heterogeneous nucleation sites for the misfit dislocations.

In order to understand the different behaviour of strain relaxation in compressively and tensily strained layers we calculated the activation energy for homogeneous half-loop nucleation of 60° $(a/2)\langle 110 \rangle$ perfect and $(a/6)\langle 112 \rangle$ Shockley partial dislocations of the 90° and 30° type in analogy to Matthew's fundamental work (Fig. 8) [9]. For the major unknown quantities, the core energy parameter α and the stacking fault energy, the values 4 and 50 mJ/m^2 have been used. As first pointed out by Marée *et al* [10] the type of the leading partial dislocation of a dissociated 60° dislocation depends on the direction of strain. For growth on $[001]$ oriented substrates the geometrical arrangement of the atoms on the close-packed (111) planes restricts nucleation of 90° partial dislocations which can be followed by 30° partial dislocations to tensily strained layers. For the given misfit of about 1% for a Si_3Ge_3 SL on Ge, Fig. 8(a) shows that half-loop nucleation of such a 90° partial dislocation requires by a factor of 4 less energy than nucleation of 60° perfect dislocations. In contrast to observations of dissociated 60° dislocations in Si layers on GaP(001) ($f = 0.37\%$) [10], in our SLs grown on Ge the 90° partial dislocations have not been followed by 30° partial dislocations on the same glide planes. Figure 8(b) compares the activation energies as a function of the misfit for these two cases, i.e. the nucleation of a 30° partial dislocation which follows a 90° partial dislocation on the same glide plane and the nucleation of a 90° partial dislocation on an (111) plane adjacent to the glide plane of a previously nucleated 90° partial dislocation. These results indicate that for tensily strained layers microtwin formation is only energetically favorable for misfit values $f > 0.4\%$. If the strain field is compressive, i.e. for growth on Si, the nucleation of partial dislocations, which have to be of the 30° type in this case, does not lead to a substantial lowering of the activation energy over the whole misfit range [Fig. 8(a)]. In full agreement with our experimental observations the misfit dislocations should therefore be of the 60° $(a/2)\langle 110 \rangle$ type.

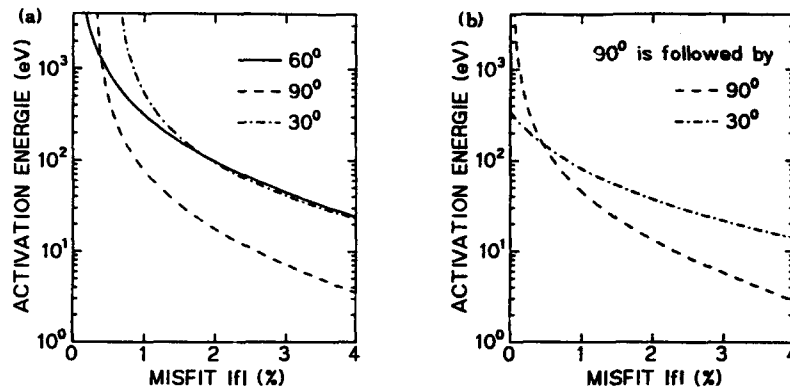


Fig. 8: Variation of the activation energy for surface half-loop dislocation nucleation with misfit. (a) homogeneous nucleation of 60° perfect as well as 90° and 30° partial dislocations; (b) a 90° partial dislocation is followed by a 30° partial dislocation on the same glide plane or by a 90° partial dislocation on an adjacent glide plane.

CONCLUSIONS

We have demonstrated that short-period Si/Ge SLs with a high degree of crystal perfection and nearly atomically sharp interfaces can be synthesized on Si(001) and Ge(001) substrates by a low temperature MBE technique which involves substrate temperature modulation. For the first time strain relaxation of equivalent Si/Ge SLs under compressive and tensile strain field could be compared directly. The different mechanisms of strain relief observed in these superlattices – the formation of 60° interfacial dislocations for growth on Si and microtwin formation for growth on Ge – are found to be consistent with a theoretical calculation of the activation energy for both cases based on a homogeneous dislocation nucleation model.

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DIRECT IMAGING OF ORDERING IN Si-Ge ALLOYS, ULTRATHIN SUPERLATTICES, AND BURIED Ge LAYERS

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ABSTRACT

We review recent Z-contrast imaging studies of Si-Ge ultrathin superlattices, alloys, and buried Ge layers. It is found that whenever Si is deposited onto a Ge (2×1) surface, Ge is pumped into the growing Si layer, and this is accompanied by interfacial ordering. This is explained by a novel Ge atom pump mechanism which occurs during MBE growth. Codeposition and alloy growth results in long range $\langle 111 \rangle$ ordering as a consequence of lateral segregation during nonequilibrium growth.

INTRODUCTION

Since the first diffraction evidence for ordering in Si-Ge alloys was reported by Ourmazd and Bean [1], numerous experimental and theoretical studies have attempted to elucidate this intriguing aspect of MBE growth [2, 5]. The aim has been to determine the structure and origin of the ordering and establish its relationship to growth conditions. Such information may provide the key to manipulating the ordered microstructure for potential applications in optoelectronics as well as answering fundamental questions concerning the atomistic processes which occur during MBE growth.

More recent observations [6] that ordering can also occur at Si-Ge interfaces in superlattice structures has created even more intriguing questions. For example, is the ordered phase the same as in the alloy case? Is it related to interdiffusion, and is it principally located in the Si or Ge (or both) layers? Such questions can be addressed only qualitatively (if at all) using selected area diffraction, and despite extensive studies of the Si-Ge interface by conventional high-resolution electron microscopy, no images of the ordering have been reported to date.

In this paper, we review recent Z-contrast imaging studies of Si-Ge interfaces and alloy layers. This new technique [7] is ideally suited for investigating the atomic scale ordered microstructure in the Si-Ge system [8-11]. Images possess a strong compositional sensitivity since columnar intensities approach the atomic number squared or Z^2 dependence of unscreened Rutherford scattering. In addition, no Fresnel interference effects can occur at interfaces to obscure interfacial ordering. Thus, we have intuitive imaging on the atomic scale. We utilize the same microscope operating conditions for all specimens so that it is not necessary to pretune the microscope based on the anticipated structure of the ordering. In this way, the ordered microstructure can provide its own unique insight into the fundamental atomistic processes occurring during Si-Ge MBE growth.

SUPERLATTICE MYTHOLOGY

It has become customary in the literature to regard ordering in Si-Ge superlattices as simply a spatially constrained manifestation of the long-range ordering found in alloys. Implicit in this assumption is that sequential deposition followed by strain-enhanced interdiffusion at the interface plays a similar role to codeposition in creating and stabilizing the ordered microstructure. The question, therefore, naturally arises as to which of the two ordered phases, proposed by Ourmazd and Bean to explain ordering in alloys [1], corresponds to the true ordered phase in superlattices. To answer this question, we applied our intuitive Z-contrast imaging method which immediately revealed the question (and hence the original assumptions concerning superlattice growth) to be totally inappropriate. Figure 1 is an image of a $(\text{Si}_4\text{Ge}_8)_{24}$ superlattice grown on a Ge substrate at 350°C . Remarkably, three distinct types of interfacial ordering can be observed to occur within the Si layers. In the top Si layer, we observe a strong $(2 \times n)$ interfacial periodicity. In the central layer, we observe alternate (111) planar ordering, with Ge columns running all the way through the Si layer. In the bottom layer, we see cross-like structures. Intuitive imaging tells us a different phase variant can occur (within the Si layers) at each interface. In general, we also observe an asymmetric interfacial abruptness; i.e., the Si grown on Ge interface is less abrupt than the Ge grown on Si interface. Clearly, the situation is far more complicated than previously imagined, and our images provide a unique signature of the atomistic processes which have occurred during MBE growth.

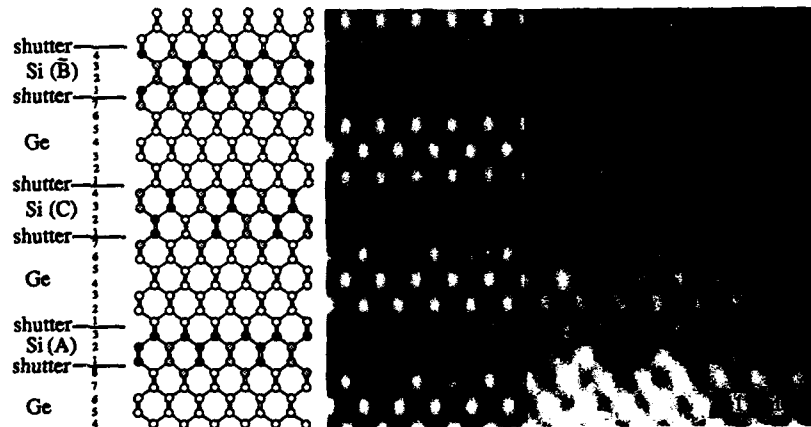


Fig. 1. [110] Z-contrast STEM image of a nominal $(\text{Si}_4\text{Ge}_8)_{24}$ superlattice showing interfacial ordering. Each bright spot in the image corresponds to a pair of atoms or "dumbbell" in the [110] projection. The [001] growth surface is toward the top of the image. Our interpretation of the superlattice structure based on the image simulation indicates the sequential deposition of Si and Ge layers together with ordered structures B, C, and A (see Ref. 9) resulting from the atom pump mechanism. Solid circles represent Si columns, open circles Ge columns, and shaded circles alloy columns. A convergence angle of 10.3 mrad, objective lens C_s of 1.3 mm, and defocus of -70 nm was assumed in the simulations.

THE ATOM PUMP

How can we explain the Ge in the Si layers, the ordered phases, and the asymmetric interfacial abruptness? The $(2 \times n)$ periodicity occurring within the Si layers is very suggestive that ordering is linked to Si deposition on a Ge free surface which is known to possess a (2×1) reconstruction [12]. By analogy with Si homoepitaxy studied by STM [13], we also know that growth at around 350°C occurs via monolayer height island formation and the consecutive interchange of (1×2) and (2×1) surface domains. The islands are elongated indicating strongly anisotropic growth via one type of step. This step, by convention, is referred to as a type S_B step using the notation of Chadi [14]. Thus, from STEM, we have the final ordered microstructure; a cross-sectional fingerprint of the atomistic processes which have occurred during growth. STM provides detailed complementary information on the processes occurring at the surface. It therefore remains to piece together the puzzle and link the two sets of observations to understand how the superlattice has grown.

In Fig. 2, we consider in cross section the growth of a narrow island (or single dimer string) along $[1\bar{1}0]$. In response to the translational symmetry of the Ge (2×1) surface, the growth is forced through two distinct type S_B step configurations. It is well known that a Ge reconstructed surface has a lower surface energy than the corresponding Si (2×1) surface, primarily because of the difference in surface dangling bond energies. It therefore makes sense to look for possible candidate sites involving an interchange between a Si surface atom and a Ge subsurface atom. The activation energy for such a process will be much lower at the step edges where the atoms are weakly bound and possess higher mobilities.

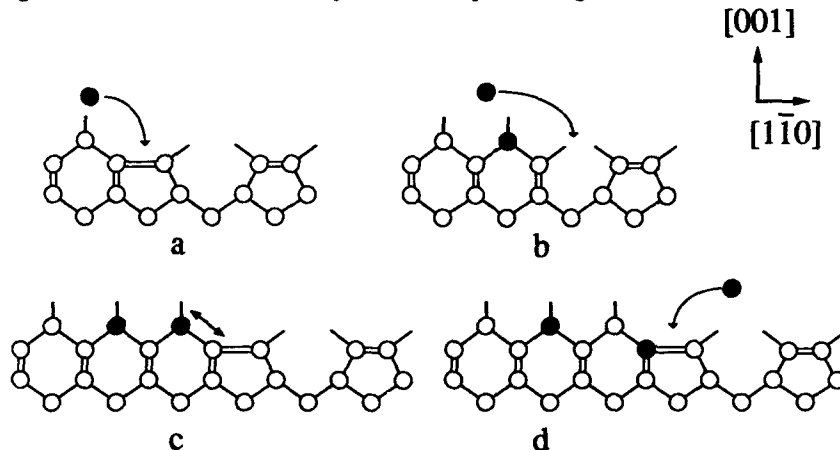


Fig. 2. Growth kinetics model for Ge segregation and ordering resulting from Si deposition on a Ge (2×1) reconstructed surface. Solid circles represent Si columns and open circles Ge columns. The exchange arrowed in (c) replaces a Si surface dangling bond with a Ge dangling bond (d).

In the nonrebonded edge configuration [Fig. 2(b)], an interchange between a surface Si edge atom with the Ge edge atom will conserve the number of dangling bonds and is energetically unfavorable. However, the rebonded edge step

configuration [Fig. 2(c)] allows the possibility of burying a surface Si dangling bond and replacing it with a more stable Ge surface dangling bond [Fig. 2(d)]. We estimate an energy saving of 0.45 eV per exchange [9] so that the rebonded edge step acts as a chemically driven atom pump for Ge segregation. The growth is forced sequentially through the stable-unstable step configurations, which configures the dimer string(s) into alternating Si and Si-Ge alloy columns as growth proceeds along [110]. Thus, compositional ordering within the Si layers can be attributed to surface growth dynamics.

We find a very small lateral ordered domain size (<10 nm) which is in excellent agreement with the surface domain size observed by STM. Carrying our atom pump model through for successive layers of growth reveals that many different phase variants are possible depending on the direction of step propagation and precisely how the proceeding layers have grown in the superlattice [9]. Ordering may propagate, terminate, or reverse during each successive monolayer growth step. The Ge concentration x^n in the n -th deposited Si layer ($n > 1$) is given by

$$x^n = \alpha^n(1 - \alpha)/2, \quad (1)$$

where the pumping parameter α specifies the fraction of available Ge atoms which are propagated during each growth step. Using Eq. (1), we can generate Z-contrast image simulations of the ordered phases, and we find this explains all of the features observed in Fig. 1. The asymmetric interfacial abruptness is clearly associated with the decay in Ge concentration (Eq. (1)) into the growing Si layer.

Assuming α has the usual Arrhenius hopping form, we can also generate the temperature dependence of the pump mechanism, relate the ordering to growth conditions, and suggest ways of controlling or eliminating the ordered microstructure during growth [9]. Such considerations may prove to be important in creating direct transitions in superlattice structures via zone folding effects.

BURIED Ge LAYERS

The atom pump mechanism described in the previous section is a general effect which also occurs at isolated interfaces. Figure 3 shows four monolayers of Ge buried in Si at 350°C. The Ge on Si interface is very abrupt, which would be expected since Ge has the lower surface energy so that no atom pump can occur. However, the pump mechanism operates when Si is deposited on the Ge surface so that Ge can be seen to decay over several monolayers into the deposited Si layer. This pumped Ge is also ordered which is the characteristic signature of the pump mechanism. The atom pump mechanism explains very nicely Ge segregation effects observed by Raman spectroscopy [15] and EXAFS [16]. It also establishes a direct link between Ge segregation and ordering. Note that the pump mechanism occurs independently of the strain imposed by the substrate. The superlattice in Fig. 1 was grown on a Ge substrate whereas the buried Ge layer is laterally compressed to the Si lattice constant. Thus, in growing ultrathin superlattices, the obvious conclusion is to concentrate on improving the problematical Si on Ge interface.



Fig. 3. Z-contrast image of four monolayers of Ge buried in Si at 350°C. The [001] growth direction is toward the top of the image.

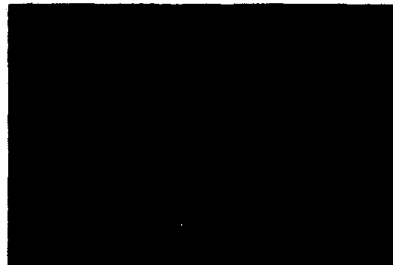


Fig. 4. Z-contrast image of a $\text{Si}_{0.6}\text{Ge}_{0.4}$ alloy layer grown at 350°C on Si (100). Note the long-range $\langle 111 \rangle$ planar ordering.

ALLOY LAYERS

We now address the related question of alloys grown by codeposition. The superlattice results have shown that many different ordered phase variants can occur and that the ordering may propagate, terminate, or reverse during each monolayer growth step. Codeposition of Si and Ge at the same temperature might therefore be expected to produce a similar effect. However, intuitive imaging again provides surprises and long-range $\langle 111 \rangle$ planar ordering is clearly visible in Fig. 4. This is a remarkable result which clearly indicates a phase-locking mechanism is occurring at low temperatures.

At 350°C, where we observe strong ordering, growth proceeds via monolayer height island formation [13, 17], and it is unreasonable to assume significant subsurface diffusion (even in the proximity of the (2×1) reconstruction). We must therefore seek an alternative explanation to the surface stress induced ordering mechanism proposed by LeGoues et al. [5] which assumes both a bilayer growth mode and appreciable subsurface diffusion.

THE ATOM TRAP

To explain alloy ordering, we invoke a model consistent with the highly nonequilibrium nature of MBE growth. As before, we note that growth proceeds alternately through low (rebonded edge) and high (nonrebonded edge) energy type S_B steps. For codeposition, we have a constantly replenishing supply of Ge atoms, and based on total energy minimization, both configurations would prefer Ge to occupy the sites at the step edges. However, the deep potential well associated with the low-energy step acts as an atom trap, freezing the incoming flux of atoms at the composition of the reservoir. Conversely, we calculate that atoms arriving at the high-energy configuration will have a much greater diffusivity away from the step, which therefore becomes rich in the more stable Ge species. A rate equation analysis accurately predicts the observed temperature and deposition rate dependence of alloy ordering and the treatment can, for example, be modified to include the effect of surfactants [18]. The long-range nature of the ordering is explained by the strain set up initially which locks the translational phase of surface dimer bonds during

successive layers of growth. Unlike sequential deposition and the atom pump, the direction of the ordering is insensitive to the direction of step propagation. This produces a new long-range ordered phase which differs from the phases previously proposed by Ourmazd and Bean [1]. Image simulation of this new ordered structure is in excellent agreement with the experimental result of Fig. 4 [18].

CONCLUSIONS

We have seen by direct imaging that Si-Ge MBE growth is far more complicated than previously imagined. A novel Ge atom pump mechanism occurs during the deposition of Si on a Ge (2×1) reconstructed surface leading to different interfacial phases. Long-range ordering is produced during codeposition as a result of nonequilibrium growth.

ACKNOWLEDGMENT

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**STRUCTURAL CHARACTERIZATION OF P-I-N DIODE SUPERLATTICE
STRUCTURES GROWN ON <100>, <110>, AND <111> ORIENTATION SI
SUBSTRATES**

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ABSTRACT

P-I-N diodes whose intrinsic region consists of strained layer superlattices (SLS), separated by 40 nm Si spacers, have been grown by MBE on Si substrates with <100>, <110>, and <111> orientations. These structures have been characterized by x-ray diffraction (XRD) and cross-sectional transmission electron microscopy (XTEM). The dual periodicities in these structures produced unique XRD effects and the quality was highly dependent on substrate orientation. The <100> sample was in general free of defects, whereas the <110> and <111> specimens contained significant numbers of twins and dislocations.

INTRODUCTION

With advances in silicon molecular beam epitaxy (MBE) the growth of high quality Si-Ge layers has become possible. The large lattice mismatch between Si and Ge permits heteroepitaxial layers to be grown under a variety of controlled strain conditions. Through bandgap engineering, the fabrication of novel devices, based on Si_{1-x}Ge_x strained layer superlattices (SLS's) has been suggested, and much effort has been directed toward their growth. As part of a study to investigate the optical and electrical properties of Si_{1-x}Ge_x SLS's as a function of substrate orientation, a series of three samples, each having the same P-I-N structure, with the SLS in the undoped intrinsic region, were grown by MBE on <100>, <110>, and <111> Si substrates under identical conditions at 450° C. The details of the growth are summarized from Reference 1. The structures consisted of 300 nm of a B-doped (p) Si buffer layer, followed by the undoped SLS and was capped with 500 nm of Sb-doped (n) Si. The intrinsic region was composed of a sequence of twelve 10 nm thick Si_{1-x}Ge_x SLS's each separated by 40 nm undoped Si spacers. The purpose of the Si spacers was to reduce the strain in the SLS in order to avoid the creation of misfit dislocations.

X-ray diffraction (XRD) has been used extensively to characterize and evaluate the quality of multilayer SL structures [2]. Briefly, the layers in the SL act as artificial planes for Bragg diffraction producing a series of peaks whose positions occur in the low angle (2θ) region. The number of higher harmonics that are observed is a direct indication of the overall quality of the SL, sharpness of interfaces, and uniformity in layer thicknesses. Since the Si_{1-x}Ge_x multilayers are epitaxial, a series of satellite SL reflections are associated with the reflections from the Si substrate. The position of the 0 order SL reflection is determined by the average perpendicular strain in the structure while the spacing between the SL satellite reflections is a function of the SL period [3]. Since the P-I-N structures under study consist of a small period (~1.5 nm) SLS

imbedded in a larger period SL (~50 nm), one would expect diffraction effects from both modulations.

Cross-sectional transmission electron microscopy (XTEM) can image interfaces at very high resolution and characterize the quality of structures through the identification of defects. It thereby complements the XRD measurements which are sensitive to the levels of defects but cannot identify their exact nature.

EXPERIMENTAL

Theta two-theta XRD scans were performed using Cu radiation and powder diffractometer equipped with a θ compensating slit and diffracted beam monochromator. X-ray rocking curves were recorded with a double-crystal diffractometer using Cu $K_{\alpha 1}$ radiation and a $\langle 100 \rangle$ Ge crystal monochromator. The comparison of observed rocking curves with those calculated from a kinematical model of x-ray diffraction [4] and a trial SL structure allows for an evaluation of the perfection and strain in a sample. Rocking curves were calculated using the measured periods as constraints and assuming that the Ge in the SLS was elastically strained.

Sample preparation for XTEM analysis followed standard procedures, including mechanical thinning and polishing, followed by dimpling and Ar ion milling. Specimens were examined in a Philips Electronics Instruments model 430 STEM operated at 300kV under brightfield and darkfield conditions.

RESULTS

$\langle 100 \rangle$ Substrate

The XRD data from the P-I-N structure grown on the $\langle 100 \rangle$ Si substrate are given in Figure 1. The low angle θ - 2θ scan (Fig. 1a) is very complicated but shows features that can be attributed to both the large and small period SL structures. A large number of very sharp closely spaced peaks were observed and represent higher orders ($N=10-43$) of the (000)⁺ reflection from the large period SL. In contrast, the broad peak at $8^\circ 2\theta$ can be attributed to the first order ($n=1$) of the (000)⁺ reflection arising from the small period SLS and yields a period of 1.1 nm. This peak was expected to be considerably broader than those observed from the large period SL because the interfaces between the individual Si and Ge layers are not perfectly abrupt on an atomic scale. Based on the extreme number of higher order reflections from the large period structure, and the presence of a strong first order reflection from the small period SLS, it is felt that the overall quality of the P-I-N structure is very good with sharp interfaces and few defects. It is noted that the combination of the two SL periods in the P-I-N structure produces a convolution of the diffraction effects from each structure. Within the overall envelope of the +1 reflection from the small period SL, two separate alternating sets of reflections, which differed in intensity, were observed. The positions of reflections in each set are consistent with integer differences in n for a large period SL. The displacement between the two sets corresponds to a difference in the large SL period of approximately 0.6 nm, and may be a result of nonuniformity in the sample, whereby the larger period changed by 0.6 nm sometime during growth. Double peaks were not observed at lower 2θ values ($<3^\circ$) because the predicted separations (0.04°) were below the

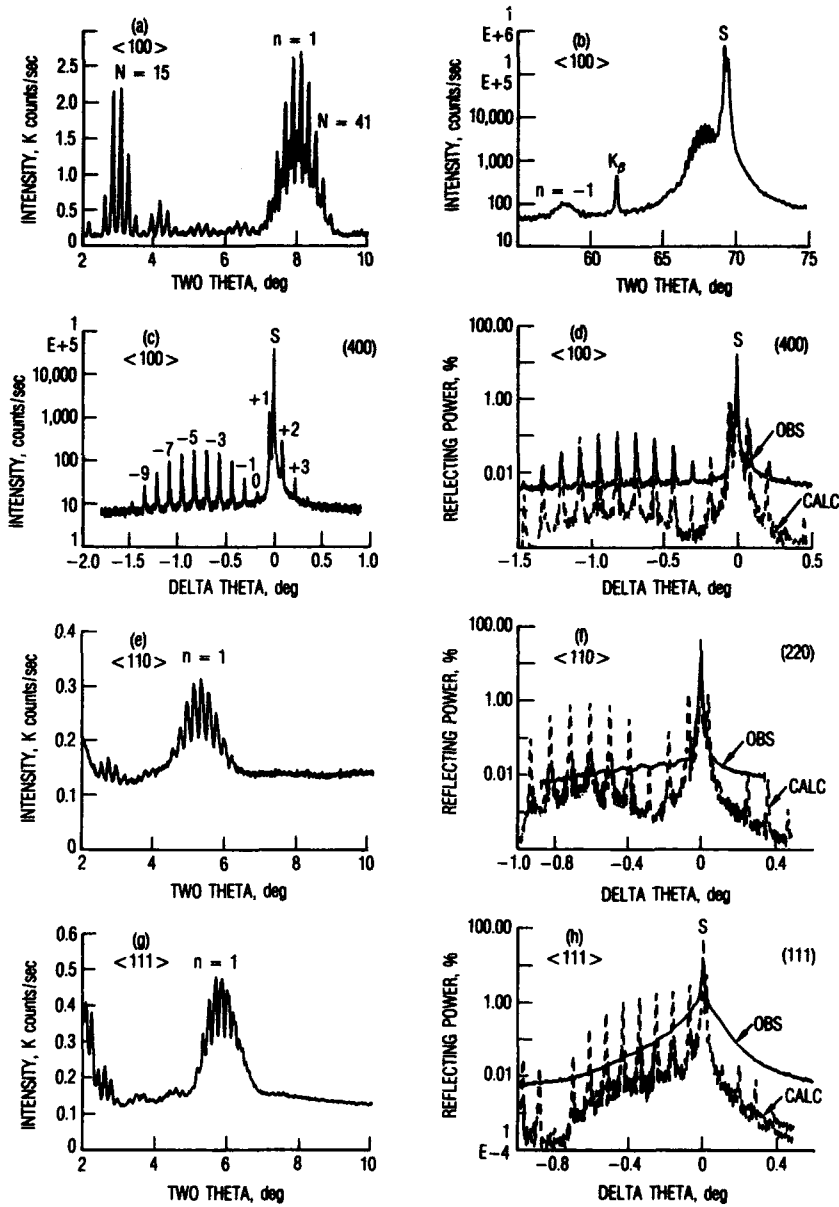


Fig. 1. Low angle (2° - 10°) and high angle (55° - 75°) θ - 2θ x-ray diffraction scans and x-ray rocking curves (-2 to $+0.5^\circ \Delta\theta$) of P-I-N diode structures grown on <100>, <110>, and <111> Si.

instrumental resolution. As in the low angle scan, the (400) reflection θ - 2θ scan (Fig. 1b) exhibits diffraction effects resulting from both the small and large period SLS structures. The closely spaced peaks near the Si substrate reflection (S) are produced by the large period structure while the -1 order reflection from the small period SLS is observed at approximately $58^\circ 2\theta$. The 0 order SL reflection from the small period SL is unresolvable under the intensity envelope of the large period SL. A summary of the SL periods measured from the various XRD methods is given in Table I, and the average periods for the small and large SLS structures were 1.2 nm and 42 nm respectively.

The (400) x-ray rocking curve (Fig. 1c) displays a series of satellite peaks produced by the large period SLS. The rocking curve is a better indication of the quality of a sample since its open ended detector records all misorientations resulting from defects. The large number of very sharp higher order satellite peaks in the rocking curve implies that the structure of the SLS is nearly perfect, with few defects and sharp interfaces, on the scale of the large period. This was confirmed by the good match between the observed rocking curve and that calculated from the kinematical model (Fig 1d). It was necessary to alter the Si/Ge ratio to 2:1 (from the targeted 6:4) in order to produce an acceptable match with the observed positions of the superlattice satellites without assuming some relaxation of the Ge layers. The large number of parameters (i.e. thicknesses, strains) needed to model these structures, however, precludes arriving at a unique characterization.

<110> and <111> Substrates

The low angle θ - 2θ scan from the <110> (Fig. 1e) sample bears some resemblance to that obtained from the <100> sample in that it displays diffraction effects from both the small and large period SLS's, but is notably different since the breadths of the peaks are greater and intensities of the reflections are much lower. This suggests that the quality of the structure is not as good as the <100> SLS. This overall trend is repeated in both the high angle (220) θ - 2θ scan and x-ray rocking curve where SL satellite reflections are just resolvable (Fig. 1f). The small and large periods of the SLS's were measured to be 1.7 nm and 44.2 nm respectively.

The results from the <111> substrate sample are similar in appearance to the <110> specimen. The low angle SL reflection (Fig. 1g) are broader and less intense than those from the <100> sample and the (111) rocking curve (Fig. 1h) shows no trace of resolvable SL satellites, but only diffuse scattering around the Si substrate reflection.

The rocking curves calculated for the <110> and <111> samples produced sharp superlattice reflections with sufficient intensity to be observable if the samples were of good quality.

The absence of these features in the observed curves is a clear indication that these samples are highly defected, in particular the <111> specimen, and the superlattices are of poor quality.

Cross Sectional Transmission Electron Microscopy (XTEM)

Brightfield XTEM images of the <100> P-I-N structure are presented in Figures 2a and 2b. Few defects were observed and a period of 39.6 nm was measured for the large SL structure. The interfaces are sharp and individual layers including, those in

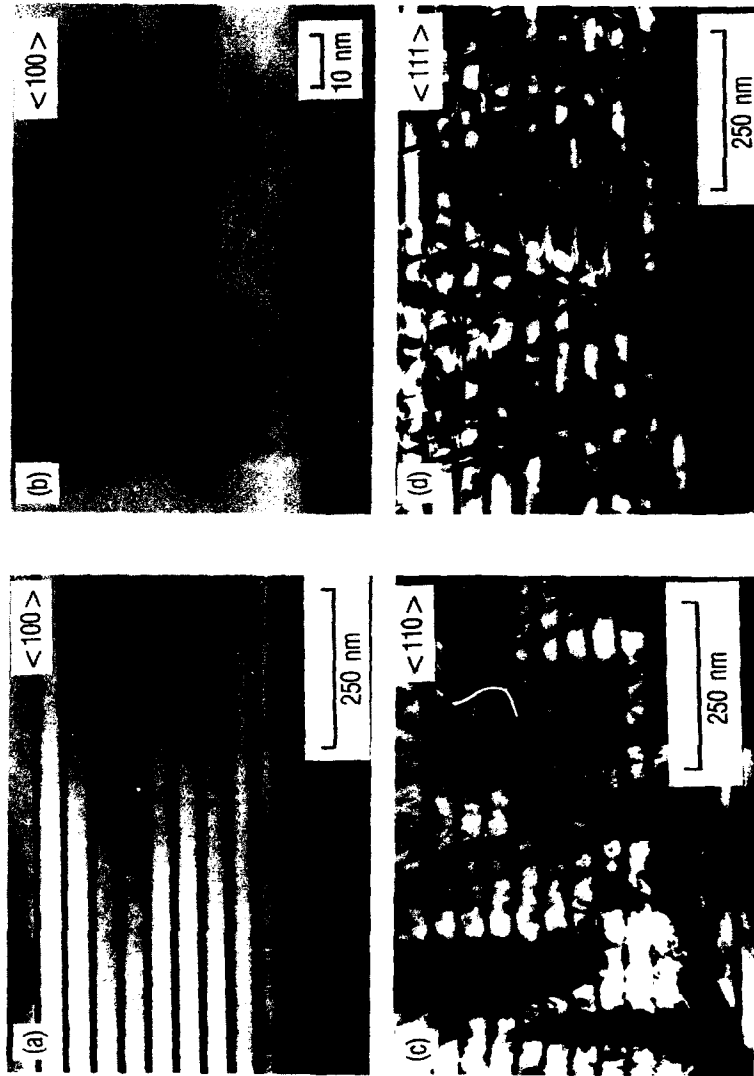


Fig. 2. Cross-sectional transmission electron micrographs of P-I-N structures grown on $\langle 100 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$ Si substrates.

TABLE I

Superlattice Periods (nm) Derived from XRD Data

SUBSTRATE	LOW ANGLE θ -2 θ	HIGH ANGLE θ -2 θ	ROCKING CURVES
<100>	1.1 (p)	1.2 (p), 42.2 (P)	41.9 (P) {400}
<110>	1.7 (p)	1.7 (p), 44.6 (P)	43.7 (P) {220}
<111>	1.5 (p)	1.5 (p), 50.6 (P)	Not Observed

the small period SLS's, are well resolved, uniform, and parallel. In contrast, the images of the <110> (Fig. 2c) and <111> (Fig. 2d) structures display significant numbers of defects. The <111> SL contains numerous 60° type dislocations which begin growth from the interface with the p-type buffer. Structure in the <110> sample is much more complicated. The first several SLS's are relatively free of defects but subsequent layer contain great numbers of microtwins and larger misoriented columnar grains. The irregularities observed in the <110> and <111> samples are similar, in many respects, to those observed in Ge_{0.50}Si_{0.50}/Si superlattices grown on the same orientation substrates [5].

SUMMARY AND CONCLUSIONS

The dual periodicities in these structures have produced unique diffraction effects, which appear as a convolution of the effects from the individual modulations. The quality of the structures was highly dependent on the orientation of the substrates, as indicated by the number and sharpness of the higher order harmonics of the SLS XRD reflections. The <100> sample produced many orders of narrow XRD peaks, characteristic of few defects and sharp interfaces, whereas the <110> and <111> samples displayed weak and less well defined SLS reflections. XTEM analysis of these samples revealed that the <100> sample had few defects and possessed sharp parallel interfaces, while the <110> and <111> samples contained significant numbers of twins and dislocations.

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GROWTH OF $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ ALLOYS ON Si (100), (110)
AND (111) SURFACES

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ABSTRACT

We compare and contrast $\text{Ge}_x\text{Si}_{1-x}$ alloys grown on Si(100), (110) and (111) surfaces. The geometry of interfacial misfit dislocations are observed to be different on these three surfaces, as the intersections of available {111} glide planes are of different symmetries for the different interfaces. In addition, angular factors resolving the applied and line tensor stresses onto misfit dislocations vary over the different surfaces, producing different effective stresses for identical layer thicknesses, compositions and microstructures. Finally, markedly different dislocation microstructures are observed on the different surfaces, as geometrical considerations show that partial dislocations may separately propagate on the (110) and (111) surfaces, in contrast to the (100) surface.

INTRODUCTION

There have been many studies of misfit dislocation energetics and kinetics for the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ surface, e.g. [1] [2] [3] [4] [5] [6] [7] [8] but very few studies of other interfaces in this system. Misfit dislocations would be expected to show very different symmetries, structures and properties on different surfaces, and in this study we report results from $\text{Ge}_x\text{Si}_{1-x}$ alloys grown on (110) and (111) surfaces, as well as the conventional (100) surface.

In diamond cubic structures, such as Si, Ge and $\text{Ge}_x\text{Si}_{1-x}$, dislocations almost invariably glide on {111} planes, as these are the widest-spaced lattice planes and the Peierls barrier to dislocation motion is therefore lowest. [9] The Burgers vectors of total dislocations (i.e. those dislocations which represent a lattice vector) in the diamond cubic lattice are almost invariably of the type $\frac{a}{2}\langle 110 \rangle$, as this represents the minimum magnitude lattice vector and therefore the minimum dislocation energy configuration as the self-energy of a dislocation varies as b^2 . [9] The intersection of available {111} glide planes with the relevant heteroepitaxial interface therefore defines the interfacial dislocation symmetries. The relevant symmetries for (100), (110) and (111) interfaces are shown in Figure 1. The (100) surface exhibits the classic orthogonal misfit dislocation grid along in-plane $\langle 011 \rangle$ directions. The (110) surface has only a uniaxial strain relief along the in-plane $\langle 1\bar{1}0 \rangle$ direction, as this represents the only line of intersection of the interface with inclined {111} glide planes - the other {111} glide planes are normal to the interface, and as will be shown in the next section, dislocation Burgers vectors lying within these normal planes experience no resolved lattice mismatch force. The (111) surface has three in-plane $\langle 011 \rangle$ lines of intersection with inclined {111} planes, producing a hexagonal interfacial dislocation symmetry. These different symmetries are confirmed experimentally by plan-view TEM imaging in Figure 2.

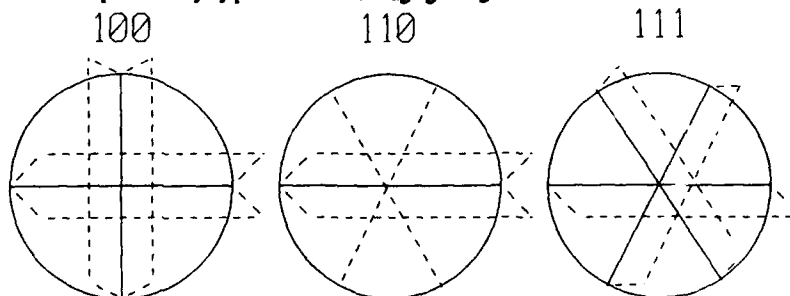


Figure 1: Schematic illustration of the symmetries of interfacial misfit dislocations at (100), (110) and (111) interfaces. Solid straight lines show the interfacial misfit dislocations; dashed lines outline intersecting {111} glide planes.

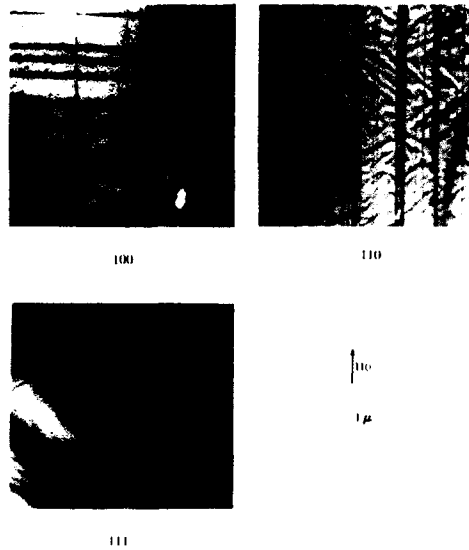


Figure 2: Plan-view TEM images of misfit dislocation symmetries at (100), (110) and (111) $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ interfaces.

CRITICAL THICKNESS AND EXCESS STRESS

The critical epilayer thickness, h_c , at which interfacial misfit dislocation length is first energetically favorable was defined for semiconductor heterostructures by Matthews and Blakeslee^[10] who balanced the resolved force due to the lattice mismatch, F_ϵ (which promotes generation of interfacial misfit dislocations), with the dislocation line tension, F_T (which opposes misfit dislocation creation). Substituting standard expressions for F_ϵ on the left hand of equation (1) and F_T on the right side yields:

$$2\cos\lambda\epsilon Gbh_c \frac{1+\nu}{1-\nu} = \frac{Gb^2(1-\nu\cos^2\theta)}{4\pi(1-\nu)} \ln\left(\frac{\alpha h_c}{b}\right) \quad (1)$$

where λ is the angle between the dislocation Burgers vector and the interfacial normal to its line direction, θ is the angle between Burgers vector and line direction, G is the epilayer shear modulus, ν is the epilayer Poisson ratio, α is a factor describing the dislocation core energy^[9] and ϵ is the strain between $\text{Ge}_x\text{Si}_{1-x}$ and Si. [In subsequent analysis we assume elastic isotropicity and that $G = 6.4$ GPa, $\nu = 0.28$, $\alpha = 4$, $b = 3.9$ Å and $\epsilon = 0.041x$.

The Matthews-Blakeslee model is an equilibrium model; the first relatively complete attempt at modelling the kinetics of strain relaxation in $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterostructures was by Dodson and Tsao^[11] who assumed that the heterostructure will relax at a rate proportional to individual misfit dislocation propagation velocities, v ; by analogy to experiments in bulk semiconductors^{[11] [12] [13]}^[14] the form of v was assumed to be:

$$v = v_0 \sigma_{\text{ex}} e^{\left(\frac{-E_v}{kT}\right)} \quad (2)$$

where v_0 is a constant. E_v is the activation energy for dislocation glide, known to be of the order 1.6 eV and 2.2 eV at moderate stresses (of the order tens to one hundred MPa) in bulk Ge and Si respectively^{[11] [12] [13] [14]}. σ_{ex} is the "effective" or "excess" stress driving dislocation motion,

found by converting the difference $F_e - F_T$ to an equivalent stress. This yields:

$$\sigma_{ex} = 2\cos\lambda\cos\phi\epsilon Gh \frac{1+\nu}{1-\nu} - \frac{Gb\cos\phi(1-\nu\cos^2\theta)}{4\pi h(1-\nu)} \ln\left(\frac{\alpha h_c}{b}\right) \quad (3)$$

where $\cos\phi$ is the angle between the $\{111\}$ glide plane and the interfacial normal.

The angular factors λ , θ and ϕ vary over different surfaces, which makes the critical thickness and effective stress for otherwise equivalent structures a function of substrate orientation. We tabulate the variation of $\cos\lambda$, $\cos\phi$ and the "Schmidt factor", $\cos\lambda\cos\phi$ for the 3 different surfaces in Table 1, together with the effective stress for a 1000 Å $\text{Ge}_{0.2}\text{Si}_{0.8}$ layer grown on the different substrates. Note that we are assuming elastic isotropy. In Figure 3, we plot the predicted critical thicknesses for the three surfaces, again assuming elastic isotropy.

	100	110	111
$\cos\lambda$	0.50	0.71	0.29
$\cos\phi$	0.82	0.58	0.94
$\cos\lambda\cos\phi$	0.41	0.41	0.27
σ_B (MPa)	760	760	540
σ_E (MPa)	610	660	390

Table 1: Angular factors, $\cos\lambda$, $\cos\phi$, $\cos\lambda\cos\phi$ for 60-degree $a/2\langle 110 \rangle$ dislocations in different surfaces. Also shown are the magnitudes of σ_B and σ_E for a coherent 1000 Å $\text{Ge}_{0.2}\text{Si}_{0.8}$ heterostructure.

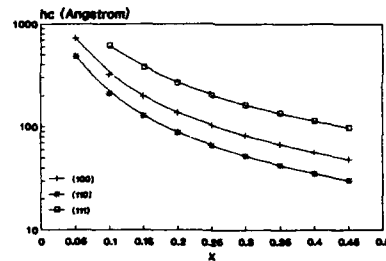


Figure 3: Predictions of the Matthews-Blakeslee theory for the critical thickness of $\text{Ge}_x\text{Si}_{1-x}$ layers on Si(100), (110) and (111) surfaces, assuming materials parameters given in the text and elastic isotropy.

EXPERIMENTAL

Structures are grown by MBE as described elsewhere.^[15] All structures described here on (100) and (110) surfaces are grown at $\sim 550^\circ\text{C}$. Growth on (110) was found to be very similar to growth on (100), with comparable effectiveness of standard substrate cleaning techniques and comparable surface morphologies (in contrast to growth of compound semiconductors on (110) where the non-polar surface makes planar surface morphologies very difficult to achieve). Growth on (111) surfaces, however, was found to be substantially more challenging with respect to substrate cleaning; for growth at 550°C , many stacking fault tetrahedra were found to penetrate the Si buffer layer and $\text{Ge}_x\text{Si}_{1-x}$ epilayer. Even growth at 650°C suffered to a lesser extent from relatively high densities of stacking fault tetrahedra; these defects then acted as very effective nucleation sites for subsequent misfit dislocation nucleation.

The microstructure of the $\text{Ge}_x\text{Si}_{1-x}$ layers and the defects within them was studied using transmission electron microscopy (TEM) using a JEOL 2000FX electron microscope operated at 200 kV. Studies were performed at both ambient temperature, and during in-situ heating, and consequent strain relaxation, of structures in the TEM. Samples are prepared for TEM by mechanical thinning and argon milling for cross-sectional imaging, and back-side chemical etching for the plan-view

geometry.

Layer thicknesses were calibrated using cross-sectional TEM, and $\text{Ge}_x\text{Si}_{1-x}$ compositions were calibrated using a combination of cross-sectional TEM and Rutherford Backscattering Spectroscopy, as described elsewhere [7].

MISFIT DISLOCATION MICROSTRUCTURES

For the Ge composition range studied here ($x < \sim 30\%$), the vast majority of misfit dislocations observed at (100) interfaces were 60-degree (angle between Burgers vector and line direction) $a/2\langle 110 \rangle$ glide dislocations. This in agreement with our previous work, and studies of many other authors.

In bulk semiconductors, it is known that 60-degree $a/2\langle 110 \rangle$ dislocations generally dissociate into two partial dislocations (a partial dislocation is a dislocation that does not connect two lattice points) of smaller Burgers vector, $a/6\langle 112 \rangle$, known as "Shockley" partials. These partials may move by glide on the same {111} plane as the parent dislocation, but produce a stacking fault in that plane. The driving force for this dissociation process is that the b^2 dislocation energy is less after dissociation than before. A typical reaction, for dissociation on a (111) plane would be:

$$a/2[101] = a/6[2\bar{1}1] + a/6[112] \quad (4)$$

These partials' Burgers vectors make angles of 30-degrees and 90-degrees with respect to their dislocation line direction. After dissociation, the partials glide apart as they exert a mutually repulsive stress upon each other. As they move apart, they generate a ribbon of stacking fault between them and when this stacking fault energy balances their interaction energy, the partials reach equilibrium. This typically occurs at dissociation widths of the order a few nm implying stacking fault energies of the order 50-80 mJ m^{-2} [12] (we assume an average value of 65 mJ m^{-2} in subsequent modelling for both Si and Ge). Dissociation, should be considered in the energetics of misfit dislocations in strained layer epitaxy, but rarely is. More significantly, it is also in principle possible for partial dislocations to move separately, substantially modifying driving forces and stresses. The partial dislocations may remain separate or eventually recombine to form a total dislocation.

For (100) epitaxy, application of equations (1) and (2) actually predicts a greater effective stress, and hence lower critical thickness, for a 90-degree $a/6\langle 112 \rangle$ partial than for an undissociated or narrowly dissociated 60-degree $a/2\langle 110 \rangle$ total dislocation for a wide Ge composition range. (Note that in these calculations an extra force / stress is required, of the same sign as the line tension contribution, for the partial dislocation due to the stacking fault created by its motion). The 30-degree partial has a significantly lower effective stress acting on it than either of the other two types of dislocation.

As first pointed out by Vieggers et al and Maree et al [16] [17], however, for compressive strain on the (100) surface, the 90-degree partial may not lead the 30-degree partial as it produces a very high energy stacking fault of the type ABCABCABCAB involving violation of nearest-neighbour stacking at the fault, rather than the second-nearest neighbour stacking violation (e.g. ABCABC/BCABCAB) at conventional stacking faults (the required order of partials to produce the lower energy fault is generally determined by a geometrical construction, the "Thompson tetrahedron", due to Thompson [18]). For tensile strain on (100) epitaxy, the required order of partials is reversed, and Wegscheider et al [19] have observed separate 90-degree partials nucleating and propagating in Ge/Si short period superlattices grown on Ge. For compressive strain, however, the slower 30-degree partial is forced to lead if the dislocation is dissociated, and the 90-degree partial follows very close behind it.

On (100) and (111) surfaces, however, consideration of the Thompson tetrahedron construction shows that for compressive strain, the 90-degree partials may lead and still produce the lower energy stacking fault. For a wide Ge composition range, the 90-degree partial will now have a higher effective stress and lower critical thickness than an undissociated 60-degree dislocation as is illustrated for (111) epitaxy in Figure 4. Plan-view TEM images of misfit dislocations at (110) and (111) interfaces reveal many 90-degree partials dislocation segments which become almost invisible when the imaging diffraction vector g becomes parallel to their line direction, $g \cdot b = 0$ and $g \cdot b_{\text{core}} =$

0, see [20]) as is illustrated in Figures 5 and 6. As is shown in Figure 7, these partial dislocations produce stacking faults throughout the epitaxial layer. This will clearly be detrimental to technological application of strained layers on these surfaces!

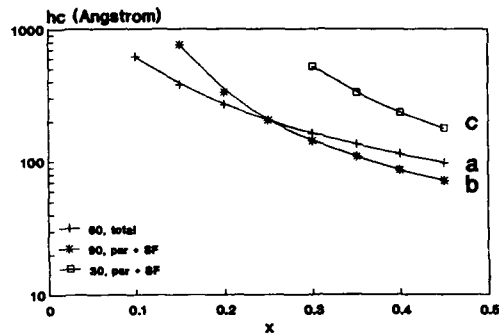


Figure 4: Equilibrium critical thickness for misfit dislocations at the $Ge_xSi_{1-x}/Si(111)$ interface for (a) undissociated 60-degree $a/2\langle 110 \rangle$, (b) $a/6\langle 112 \rangle$ 90-degree, (c) $a/6\langle 112 \rangle$ 30-degree. (b) and (c) include a stacking fault energy of $65 \text{ mJ} \cdot \text{m}^{-2}$.



Figure 5: Bright field plan view images of a 400 Å $Ge_{0.16}Si_{0.84}/Si(110)$ structure. Relevant diffraction vectors are shown in each image.



Figure 6: Bright field plan view TEM images of a 1600 Å $Ge_{0.13}Si_{0.87}/Si(111)$ structure. The relevant $\langle 220 \rangle$ diffraction vector is shown for each image.

We have not yet unambiguously established whether these 90-degree partials nucleate independently, or whether they are segments of very widely dissociated 60-degree $a/2\langle 110 \rangle$ dislocations. The presence of high densities of co-existing 60-degree $a/2\langle 110 \rangle$ dislocations suggest the latter. During in-situ relaxation studies in the TEM, we have often observed 30-degree partials propagating along the length of a pre-existing 90-degree partial, repairing the stacking fault and producing a 60-degree $a/2\langle 110 \rangle$ dislocation. Nevertheless, the observed lengths of 90-degree segments can often be as high as tens of microns, implying enormous dissociation widths. Our preliminary conclusions are that both separate nucleation of 90-degree partials and very wide dissociation of 60-degree $a/2\langle 110 \rangle$ dislocations are occurring.

One exciting prospect for studies of these partial dislocations is that we can separately measure propagation velocities and activation energies for the two partials, a subject of intense interest in dislocation theory (e.g. [12]). Calculations suggest that the Peierls barrier for motion of the 30-degree partial will be significantly higher than for the 90-degree partial. [21] Preliminary velocity data from our in-situ TEM observations (see [7] for a fuller description of the technique) appear to support the above conclusions and fuller details will be published elsewhere.

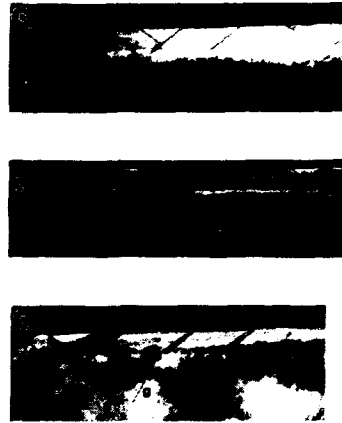


Figure 7: Cross-sectional images in the $[1\bar{1}0]$ pole of a 410 Å $\text{Ge}_{0.33}\text{Si}_{0.67}/\text{Si}(110)$ structure with $g =$ (a) $[220]$, (b) $[111]$ and (c) $[111]$.

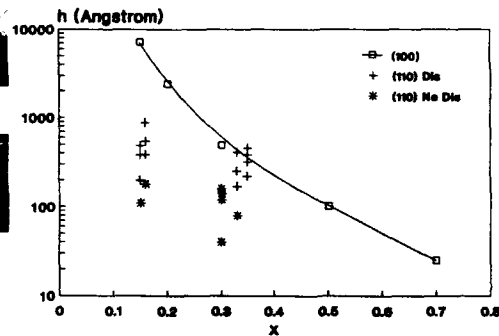


Figure 8: Comparison of measured critical thicknesses of $\text{Ge}_x\text{Si}_{1-x}$ layers on $\text{Si}(100)$ (from [15]) and $\text{Si}(110)$ (present work).

CONCLUSIONS

We have shown that geometrical and angular factors predict different dislocation symmetries, critical thicknesses and effective stresses for otherwise identical structures on (100), (110) and (111) surfaces. The critical thickness is expected to vary in the ratio $h_c(111) > h_c(100) > h_c(110)$. This is partially confirmed by experimental data in Figure 8 where we directly compare critical thicknesses on (100) and (110). The critical thickness is clearly significantly less at a given composition on the latter surface. This ability to modify (particularly increase) critical thickness by optimum choice of substrate orientation may be important for minority carrier devices, such as heterojunction bipolar devices, where it is desired not to exceed the critical thickness. A difference of the order $2x$ in h_c may be obtained between the three different surfaces. Substrate cleaning on (111) remains a challenge, however.

It is also shown that isolated partial dislocation segments may exist on the (110) and (111) surfaces. This may provide new insights into fundamental dislocation theory, but the resulting stacking faults extending throughout the epitaxial layer are clearly technologically incompatible.

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X-RAY AND RAMAN STUDIES OF INTERLAYER MIXING IN Si_nGe_n SUPERLATTICES

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ABSTRACT

Interface mixing between the Ge and Si layers in symmetrically strained Si_nGe_n superlattices occurs during post growth thermal anneals. Interdiffusion coefficients were obtained from intensity changes in the low angle superlattice x-ray satellites on samples with nominal periodicities between 1.4nm and 5.6nm. A common activation energy of 3.0 ± 0.1 eV was found. The bulk interdiffusion coefficients for Si_nGe_n were derived since measurements were made on samples with different layer thicknesses. Intermixing appears to occur by diffusion of Si atoms into the Ge layers via a vacancy mechanism. Raman scattering measurements support this process as well as the formation of $\text{Si}_{1-x}\text{Ge}_x$ alloy layers during the anneals.

INTRODUCTION

The growth and properties of symmetrically strained Si_nGe_n superlattices have recently received much attention [1-5]. This interest is primarily stimulated by possible direct or quasi-direct band gap transitions that would permit development of novel optoelectronic devices. The thermal stabilities of Si_nGe_n superlattices with respect to interlayer mixing and lattice strain relaxation are very important to the behavior of these structures. We had previously used [4,6-8] Raman scattering and x-ray diffraction (XRD) measurements to study the effects of thermal anneals on a symmetrically strained Si_nGe_n superlattice that had been grown on a nominal 200nm $\text{Si}_{0.5}\text{Ge}_{0.5}$ buffer layer. Substantial intermixing was found for annealing temperatures above 910K where an activation energy of 3.0 ± 0.2 eV was deduced [6-8] for the interdiffusion coefficient. In this paper we summarize similar x-ray and Raman studies on symmetrically strained Si_nGe_n superlattices after annealing. Since measurements were made on samples with different period thicknesses, the bulk interdiffusion coefficients could be obtained. From comparisons with the self and impurity atom diffusion parameters for crystalline Si, Ge, and $\text{Si}_{1-x}\text{Ge}_x$ alloys it has been concluded that intermixing in the Si_nGe_n superlattices primarily occurs by diffusion of Si into the Ge layers via a vacancy mechanism.

EXPERIMENTAL DETAILS

The samples have been grown by molecular beam epitaxy (MBE) on (100) Si substrates using Perkin-Elmer equipment and previously described procedures [4]. The Si_nGe_n superlattices with nominal n -values of 5, 10, 15, and 20 were grown at temperatures around 380° C. Prior to the growth of the superlattices relaxed $\text{Si}_{0.5}\text{Ge}_{0.5}$ alloy buffer layers had been deposited at temperatures

between 450-500° C. As reported previously [5], as-grown structures have been characterized by XRD, Raman spectroscopy, and cross-sectional transmission electron microscopy (XTEM). These measurements revealed that the periodicities (λ) of Si_mGe_m superlattices ranged from $\lambda = 1.4\text{nm}$ to $\lambda = 5.0\text{nm}$ and the $\text{Si}_{0.5}\text{Ge}_{0.5}$ buffer layer thicknesses varied between 150-185nm, which greatly exceed the critical thicknesses for strain relaxation at this alloy composition [2].

The thermal stabilities of the Si_mGe_m superlattices were examined after furnace anneals (FA) between 950K and 1120K and rapid thermal anneals (RTA) between 1150K and 1210K for various times using procedures previously described [4,8].

The XRD experiments used the conventional θ - 2θ scanning mode and $\text{Cu } k_\alpha$ radiation where the first order superlattice satellite of the low-angle (000)⁺ x-ray reflection was used to determine the interdiffusion coefficients [6,8,9]. Raman light scattering experiments were performed using a previously described system [4,8] with excitation by the 457.9nm line from an argon-ion laser in order to limit the sampling depth to just the superlattice layers.

RESULTS AND DISCUSSION

The low-angle x-ray diffraction traces for the four symmetrically strained Si_mGe_m superlattices (identified as VA25, VA27, VA28, and VA30) are compared in Fig. 1 for the as-grown condition and after a 50s anneal at 1124K. The positions of the peak maxima correspond to periodicities where λ decreases from 4.2nm to 1.4nm [5]. As expected [9], the main impact of the anneal is to reduce the intensities of the x-ray peaks. In fact, the decay of the normalized intensity, I , is directly related [9] to the interdiffusion coefficient $D_\lambda(T)$ by:

$$\frac{d}{dt} \ln\left(\frac{I}{I_0}\right) = -\frac{8\pi^2}{\lambda^2} D_\lambda(T) \quad (1)$$

where I_0 is the normalized intensity of the low-angle peak prior to annealing and t is the annealing time at temperature T . Equation (1) has been used to determine the $D_\lambda(T)$ values for the Si_mGe_m samples (except for VA25 since the peaks for this sample were too close to the instrumental cutoff for reliable analyses). The results are summarized in Fig. 2 where the lines are least-square fits based upon Arrhenius temperature dependencies to yield the activation energies (E_a) given in this figure. These E_a values agree within experimental accuracy to the activation energy of $3.1 \pm 0.2\text{eV}$ previously found [6,7] for the symmetrically strained Si_mGe_m superlattice with $\lambda = 3.3\text{nm}$. Since our present measurements were made on samples with different λ values, we can use the expression [9]:

$$D_{\text{bulk}}(1 + C_n/\lambda^2) = D_\lambda \quad (2)$$

to obtain D_{bulk} , the bulk interdiffusion coefficient, where C_n is a parameter reflecting gradient energy and possible inhomogeneous strain contributions. A least-square fit of the pre-exponential

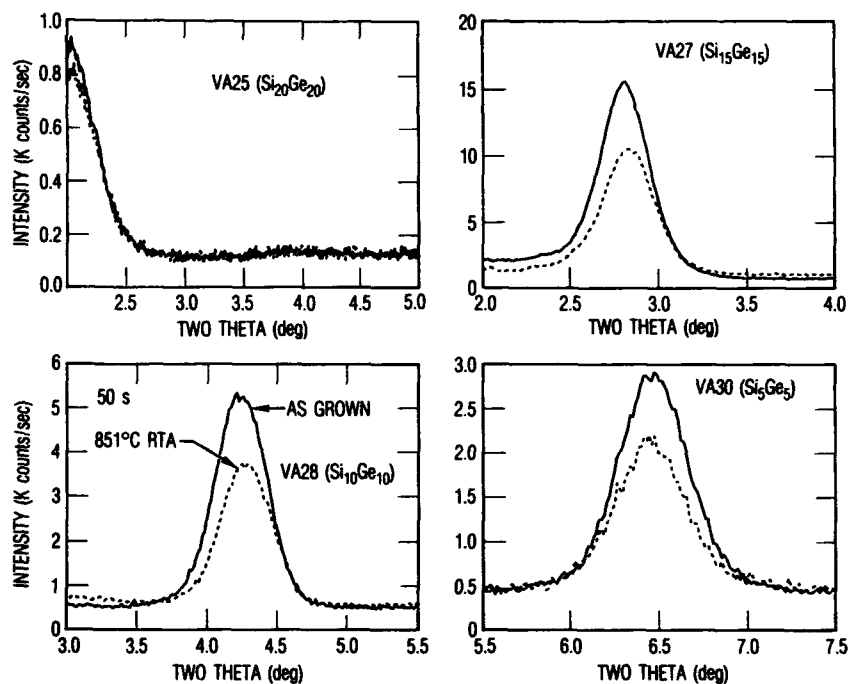


Fig. 1. Low-angle XRD peaks for symmetrically strained Si_nGe_n superlattices in as-grown condition (solid) and after a 50s rapid thermal anneal (RTA) at 851°C (dashed).

parameters D_λ^0 versus $1/\lambda^2$ is given in Fig. 3. Thus, the bulk interdiffusion coefficient for Si_nGe_n is $(8.8 \times 10^{-6} \text{m}^2/\text{s}) \exp(-3.05 \text{eV}/k_b T)$ where k_b is the Boltzmann's constant and 3.05 eV is the average activation energy measured from the three Si_nGe_n samples. The negative C_r indicated by the data in Fig. 3 corresponds [9] to an ordering system at the Si-Ge interfaces. Although this observation is surprising at first glance in light of $\text{Si}_{1-x}\text{Ge}_x$ alloy formation [4,7,8] during thermal anneals, direct evidence of interfacial ordering in Si_nGe_n superlattices has been published [10]. However, the underlying relationship warrants closer scrutiny for a better understanding of the microscopic mechanisms during interface mixing.

In Table I and Fig. 4, we compare our bulk interdiffusion coefficients for Si_nGe_n and $\text{Si}_{2n}\text{Ge}_{16}$ superlattices (where previous [7,8] D_λ values for the later sample have been corrected with the C_r parameter obtained in this study) to various tracer diffusion coefficients in crystalline Si, Ge, and $\text{Si}_{1-x}\text{Ge}_x$ materials [11-15]. It is clear from Fig. 4 that the interdiffusion coefficients for the symmetrically strained Si_nGe_n superlattices (i.e. the lines 1 and 2) are larger than self or Ge diffusion in silicon (i.e. lines 9 and 10 respectively) but lie well below the corresponding tracer diffusivities in pure Ge or $\text{Si}_{1-x}\text{Ge}_x$ alloys with $x > 0.3$ (i.e. lines 3,7,8 or 5,6 respectively). Furthermore, the activation energies for the superlattices are identical to the value of

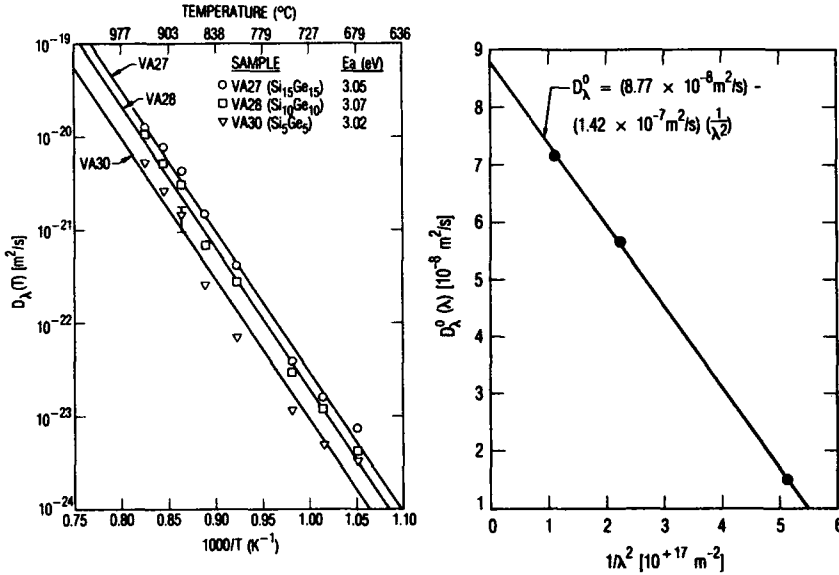


Fig. 2. Temperature dependencies of the interdiffusion coefficients $D_{\lambda}(T)$ for three symmetrically-strained Si_mGe_n superlattices.

Fig. 3. Effect of layer thickness (λ) on interdiffusion coefficient for Si_mGe_n superlattices.

Table I. Diffusion Parameters for $\text{Si}_{1-x}\text{Ge}_x$ Systems

Line in Fig. 4	System	Temperature Range (K)	E_a (eV)	D_0 (m^2/s)	Data Source
1	Si_mGe_n	953-1172	3.05 ± 0.10	8.8×10^{-8}	Present
2	$\text{Si}_{24}\text{Ge}_{16}$ ^a	910-1259	3.15 ± 0.20	1.6×10^{-7}	Refs. 7,8
3	^{30}Si in Ge	923-1173	2.88	2.4×10^{-5}	Ref. 12
4	^{71}Ge in Si	1473-1654	4.7 ± 0.15	1.5×10^{-1}	Ref. 11
5	^{71}Ge in $\text{Si}_{0.69}\text{Ge}_{0.31}$	1241-1424	3.1 ± 0.15	4.3×10^{-5}	Ref. 11
6	^{71}Ge in $\text{Si}_{0.45}\text{Ge}_{0.55}$	1129-1323	2.9 ± 0.15	1.0×10^{-4}	Ref. 11
7	^{71}Ge in Ge	1004-1189	3.0 ± 0.15	1.1×10^{-3}	Ref. 11
8	^{71}Ge in Ge	822-1164	3.14	2.5×10^{-3}	Ref. 13
9	^{30}Si in Si	1103-1473	4.4	2.0×10^{-3}	Ref. 14
10	1.6 nm Ge/Si	1073-1340	5.0	3.0×10^{-6}	Ref. 15

^aCorrected for bulk interdiffusion coefficient using the factor obtained in Fig. 3 for Si_mGe_n superlattices.

3.0eV that is attributed [16] to the vacancy mechanism in Ge and not the 4-5eV value for various mechanisms proposed [16] for diffusion in Si. Consequently, we have concluded that initial stages of interface mixing in the Si_mGe_n superlattices occur by transport of Si atoms into the Ge layers by a vacancy mechanism. This interpretation is supported by our Raman spectra of the optical phonon modes.

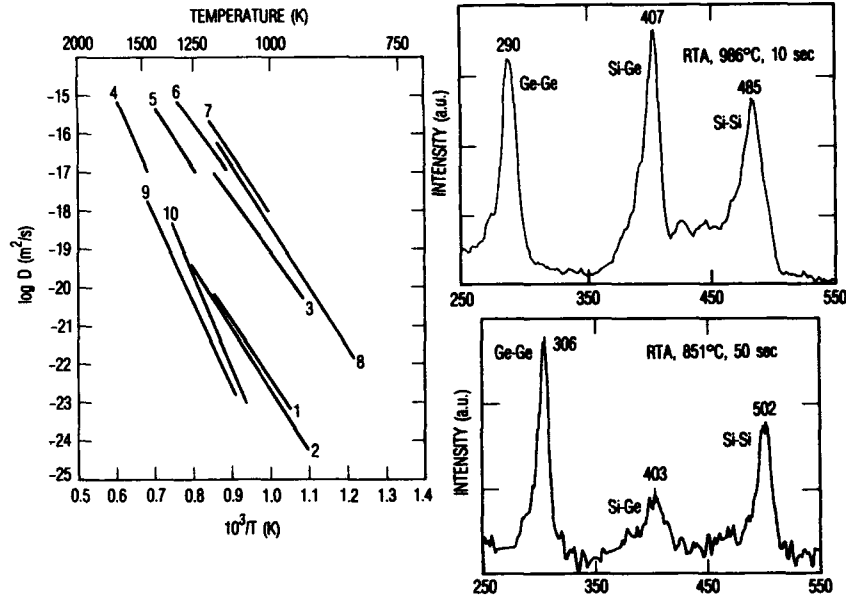
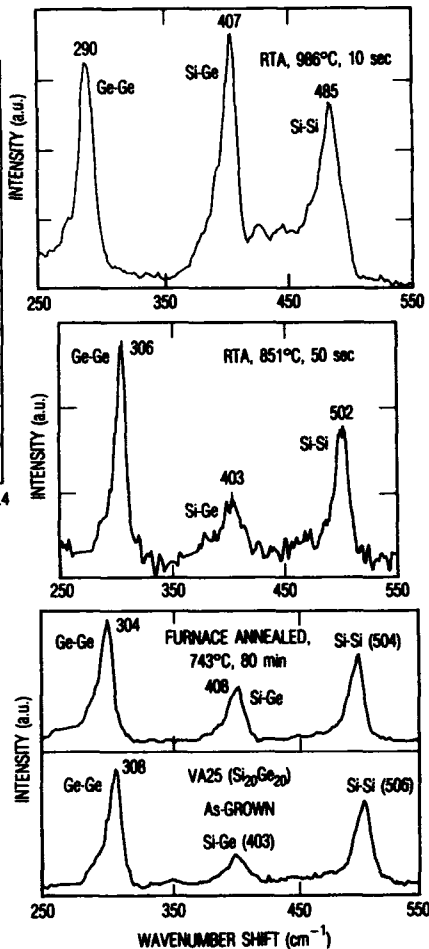


Fig. 4. Comparison of various diffusion coefficients in crystalline Si, Ge, $\text{Si}_{1-x}\text{Ge}_x$ alloys, and Si_mGe_n superlattices where the numbers correspond to diffusion systems from Table I.

Fig. 5. Raman spectra for the optical phonons obtained from a symmetrically strained $\text{Si}_{20}\text{Ge}_{20}$ superlattice in as-grown condition and after three annealing treatments as indicated. Frequencies (in cm^{-1}) at peak for each phonon mode are also indicated.



The effects of thermal anneals on the Raman spectra for the nominal $\text{Si}_{20}\text{Ge}_{20}$ superlattice (i.e., sample VA25) are illustrated in Fig. 5. The anneals led to an increase in the intensity of the Si-Ge phonon vibration near 400 cm^{-1} as well as shifts of the Ge-Ge and Si-Si modes to lower energies. Similar behavior was observed in the Raman spectra obtained from the other Si_mGe_n samples after annealing. These changes have been previously attributed [4,7] to interlayer diffusion and a decrease in the effective Ge content in the Ge layers of the nominal $\text{Si}_{20}\text{Ge}_{16}$ superlattices grown on a $\text{Si}_{0.6}\text{Ge}_{0.4}$ buffer layer. Hence, the same processes occur for the symmetrically strained Si_mGe_n structures. However, a more complete description will require additional studies.

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STRUCTURAL CHARACTERIZATION OF SHORT-PERIOD Si_mGe_n
SUPERLATTICES BY TRANSMISSION ELECTRON MICROSCOPY AND X-RAY
DIFFRACTION

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ABSTRACT

High resolution and analytical transmission electron microscopy (TEM) and X-ray diffraction (XRD) were used to characterize short-period strained-layer Si_mGe_n superlattices (m monolayers Si, n monolayers Ge, total number of periods $N \leq 145$, total thickness ≈ 200 nm). The superlattices were grown by low-temperature molecular beam epitaxy ($T = 300\text{-}400^\circ\text{C}$) on different SiGe alloy buffer layers on Si(100) substrates. The combination of these two methods shows that detailed informations can be obtained about superlattice periodicity, interface roughness, strain, and average composition.

INTRODUCTION

In a periodic superlattice the intrinsic band structure of the host materials Si and Ge is modified by the superlattice period L as is most easily demonstrated by the Brillouin zone folding scheme. For Si_mGe_n strained layer superlattices (SLS) quasi direct transitions are predicted when strain is adjusted from Si unstrained towards symmetrically or even Ge unstrained [1]. Several groups have now realised such ultrathin short-period Si_mGe_n - SLS [2,3]. So far, the characterisation of the SLS structure and quality is partly incomplete or only qualitative, however.

Although Si_mGe_n - SLS are now the object of fundamental studies attention should be given to some aspects of a future broad application in microelectronics. Integration of heterostructure devices with conventional Si-based microelectronics (heterointegration) would require the choice of a (100)Si substrate (compatibility with CMOS), thin buffer layers (planar process), and device relevant doping structures [4]. Strain adjustment can be achieved by a relaxed SiGe alloy buffer layer on Si. Partly relaxed $\text{Si}_{1-y}\text{Ge}_y$ buffers together with the Si substrate can be considered as a virtual SiGe substrate with an in-plane lattice constant equal to an alloy of effective Ge content y^* [5]. Inherently, by this virtual substrate a misfit dislocation network is created at the Si/SiGe buffer interface. Thin buffers (thickness > critical thickness required for strain relaxation) frequently suffer from problems with threading dislocations and wavy interface and surface morphology.

This paper presents results of structural characterisations by TEM and XRD of short-period Si_mGe_n - SLS grown on different $\text{Si}_{1-y}\text{Ge}_y$ buffer layers. Comparisons with results obtained by other techniques are performed.

EXPERIMENTAL PROCEDURES

The short-period Si_mGe_n - SLS were prepared by low-temperature molecular beam epitaxy at 300°C and 400°C on Si(100) substrates. The substrates were RCA cleaned or HF dipped and in situ heated to 900°C for 5 min before growth. The SiGe buffers were grown on an intermediate Si layer (typically 20 - 50 nm thick) on the Si(100) substrate. Thin buffers (< 100 nm) were grown without the help of surfactants. The Si_mGe_n - SLS (typically 0.2 μm total thickness, 145 periods) were grown either on the Si substrate (process PM) or after the buffer growth at 300°C and subsequent annealing at 450°C for 5 min (processes SA: 15 nm SiGe/1.5 nm Si, $y = 0.6-0.8$; process GA: 5 nm Ge/60-80 nm SiGe, $y=0.3-0.4$); SA2: growth at 100°C, annealing for 90 min. By suitable choice of the buffers the strain ϵ_{Si} in the Si layers of the superlattice was expected to range from 1.2 % to 3 % (corresponding to $\epsilon_{\text{Ge}} = -3\%$ to -1.2% for the Ge layers).

Microstructural characterisation by TEM was performed on $\{110\}$ cross-section specimens at 200 kV (JEOL 2000EX) and at 400 kV (JEOL 4000EX/FX). Electron-transparent samples were prepared by mechanical polishing and subsequent Ar ion milling on a liquid-nitrogen cooled sample holder. The average composition of the superlattices was determined by energy-dispersive X-ray spectroscopy (EDS) at 200 kV. XRD experiments were performed in a $(4+1)$ -crystal high resolution diffractometer using $\text{Cu K}\alpha_1$ radiation. The intensity distributions around the $\{400\}$ and the $\{444\}$ reflections were investigated with the help of a position-sensitive detector.

RESULTS AND DISCUSSION

The TEM investigations of $\langle 110 \rangle$ cross-section specimens show considerable differences in both morphology and defect structure of the superlattices and buffer layers for the different conditions investigated. Fig. 1a gives as an example a TEM bright field micrograph of a Si-rich superlattice of high perfection without any defects which was grown pseudomorphically on the Si substrate at 300°C. A rather high degree of superlattice perfection with good lateral uniformity of the layers, good periodicity and a high degree of interface sharpness is observed. By comparison with the nominal structure the dark line contrasts in this image can be attributed to the Ge layers, and the bright lines to Si layers. Similarly a high quality in the superlattice morphology is observed also for superlattices grown on virtual substrates at 300°C. Fig. 1b shows as example a cross-section of a Si_5Ge_5 superlattice (process SA). High resolution lattice imaging with the electron beam parallel to the interfaces of the superlattice layers along $\langle 110 \rangle$ lattice directions showed for all cases investigated coherent interfaces between the individual Si- and Ge - layers indicating pseudomorphic growth of these superlattice (Fig. 2). Either the dark or the bright contrast dots correspond to projections of columns of atomic pairs in $\langle 110 \rangle$ direction. On this atomic scale generally sharp interfaces are observed.

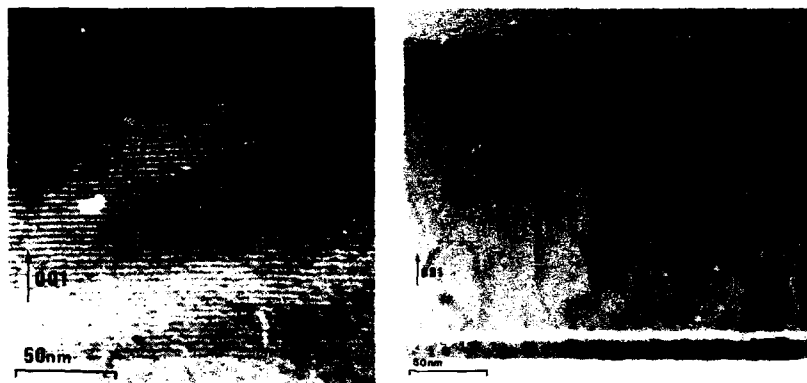


Fig 1
Cross-sectional TEM bright-field images of superlattices (a) 51-period $\text{Si}_{17}\text{Ge}_3$ (b) 145-period Si_5Ge_5 . Electron beam $\parallel \langle 110 \rangle$.

The generally rather good morphology of the superlattices is not preserved under all process conditions for the buffers (Tab.1) and for superlattice growth at higher temperatures i.e. at 350°C and 400°C . Undulations are observed which can be clearly correlated with a broadening of satellite reflections (SR, width w in Tab.1). Under such conditions the very good surface planarity of superlattices of high perfection is lost. High resolution lattice imaging shows that the undulations (typical "wavelengths" < 200 nm, amplitudes < 6.5 nm) are connected with changes in the lattice site occupation from Si to Ge along individual $\{100\}$ planes of the superlattice which can be explained by steps of atomic height in the Si-Ge-interfaces. Only close to the virtual substrate such undulations are correlated with roughness of the buffer/superlattice interface. A rather large degree of roughness is observed for processes SA2 and GA (< 2 nm). Frequently superlattices with rather large undulations show also strong fluctuations in the local periodicities or the complete absence of SR locally in extreme cases.

For all superlattices grown on virtual substrates defects such as threading dislocations extending from the interfaces to the surfaces (Fig.1b) and planar defects on $\{111\}$ planes such as stacking faults or microtwins are observed. These defects originate predominantly at the interfaces or in the buffer layers. Densities of these strain-induced defects are of the order of 10^{10}cm^{-2} for the threading dislocations and 10^5cm^{-1} for the planar defects, showing the tendency for the densities of planar defects to be generally higher in the buffer layers as compared to the superlattices. The buffer grown by a solid-phase epitaxy process (SA2) shows an increased defect density ($\approx 1.6 \cdot 10^6\text{cm}^{-1}$).

Superlattice periods D and average lattice parameters \bar{a}_1 and \bar{a}_H of the superlattices and of the buffer layers were determined from $\langle 110 \rangle$ zone axis selected area electron diffraction patterns (SAD). These were taken from thicker areas of the cross-section TEM specimens in order to avoid thin film effects. For the lattice parameter measurements (Tab.1) internal cali-

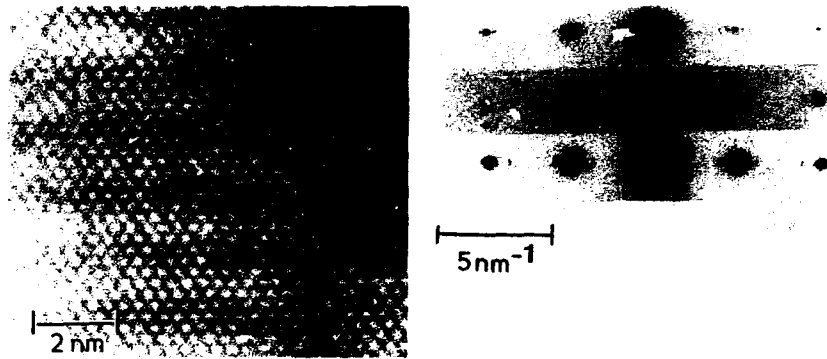


Fig 2
High resolution lattice image of a Si_5Ge_5 superlattice. Electron beam parallel to interfaces in $\langle 110 \rangle$ direction.

Fig 3
 $\langle 110 \rangle$ selected area electron diffraction patterns of superlattices with different periodicity and perfection (a) $\text{Si}_{17}\text{Ge}_3$ (b) Si_6Ge_4 (c) Si_4Ge_4 . Sections show $(n00)$ -FR ($n=-4,-2,0,2,4$) and SR.

brations were performed with Si $\langle 110 \rangle$ SAD patterns and tabulated lattice constants for bulk Si. Fig.3 compares $\langle 110 \rangle$ SAD patterns of superlattices with different periodicities, perfection, and composition. Along the growth direction additional superlattice reflections (SR) appear besides the fundamental reflections (FR) of high intensity due to the artificial superlattice period D. The SR intensity is very sharply peaked, and reflections up to several orders are visible indicating the high degree of perfection of these superlattices (Fig.3 above, center). Superlattices with undulations (Fig.3, below) lead to a broadening of SR intensities perpendicular to the (100) growth direction and to reduced numbers of visible SR orders (SR in Tab.1). For all superlattices investigated the distances between FR are non-integer multiples of the SR distances. Comparison with numerical simulations of the SR positions by kinematical calculation of the diffracted intensities for linear chains of Si and Ge show that the SR positions can be explained by deviations from the nominal superlattice periodicity in growth direction caused by incorporation of additional monolayers. The simulations show in addition that the asymmetry in the intensities of SR around the (400)FR which is observed in all cases is predominantly caused by the different a_{\perp} for the Si and Ge layers of the strained superlattice. From the distance between the SR which is inversely proportional to the average superlattice period D the average number of superlattice monolayers ($m+n$) was determined within an accuracy of ± 0.1 monolayer (Tab.1). Incorporation of additional monolayers is observed for all cases leading to a deviation in the nominal compositions of $< 25\%$.

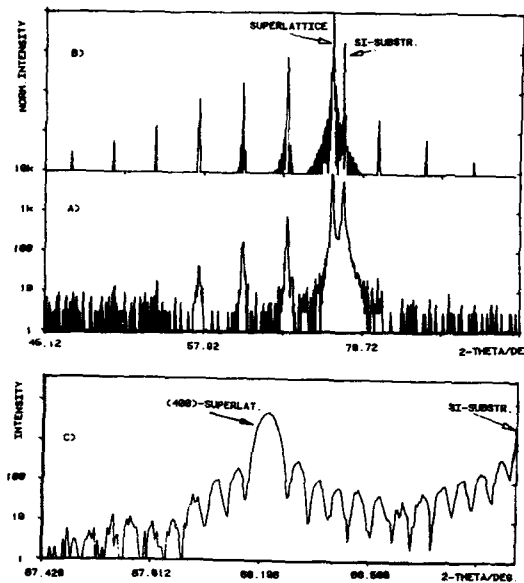


Fig 4
XRD intensity
distribution near
the (400) reflection
for $\text{Si}_{17}\text{Ge}_3$. (a)(b)
Experiment and simu-
lation with $m+n = 21$.
Intensities normalized
to the (400)FR of the
SLS. (c) Enlarged 20-
scale revealing thick-
ness oscillations near
(400). The total thick-
ness deduced is 148.5
nm. Oscillations are
smeared out for super-
lattices of lower per-
fection.

For some cases the structural characterisation was also performed by XRD on the same wafer but for different locations (Tab.1). This method averages over an area of typically 0.5 mm^2 as compared with the local information from electron diffraction (area $\approx 0.2 \mu\text{m}^2$). Fig.4 show the measured diffracted X-ray intensities around (400) for a superlattice of high perfection (cf.Figs.1a and 3 above). The intensities of the (400) FR of the Si substrate is strongly suppressed in this plot. The comparison with Fig.3 shows the qualitatively good agreement with the local information obtained by electron diffraction. Quantitative data are generally in reasonable agreement for superlattices of high quality (Tab.1). A quantitative fit of experimental and numerically calculated data confirm the deviations from the nominal superlattice periodicities. The intensity distribution in the SR could be matched in this case of a $\text{Si}_{17}\text{Ge}_3$ superlattice by assuming a composition $\text{Si}_{17.7}\text{Ge}_{3.3}$ and a mixed Si-Ge interface occupancy with a width of three monolayers. Also the average tetragonality for a Si_6Ge_4 superlattice as deduced from the average lattice parameters (Tab.1) shows satisfactory agreement. Considerable deviations are obtained for superlattices of lower perfection. This has to be ascribed to strong local fluctuations in the superlattice perfection across the wafer (see above).

The comparison of average lattice parameters of superlattices, buffers and Si substrate ($a_{\text{Si}} = 0.5431 \text{ nm}$) are used to characterise the average strain ϵ_{B} and ϵ_{SLS} of buffer and SLS, respectively, and the strain $\epsilon_{\text{Si}}^{\text{SLS}}$ of the Si layers (Tab.1). For pseudomorphic growth the lattice parameters a_{B} of the respective layers are perfectly matched. This condition is met by process PM ($\text{Si}_{17}\text{Ge}_3$). For superlattices grown on virtual substrates (processes SA, GA) the superlattices are not perfectly matched.

Process	Si _m m	Ge _n n	Si _{1-y} Ge _y buffer		m+n ML	w	SR	S L S				C _{Ge} (EDS) at. %	C _{Ge} (RBS) at. %
			a nm	c _B %				a nm	a nm	c _{SLS} %	c _{Si} %		
PM	17	3			21.1 (21.0)	s (s)	5 (4)	0.547 (0.5494)	0.544 (0.5430)	-0.3 (-0.65)	0.2 (0)	15.9 (15.7)	
SA 1	5	5	0.551	-1.5	11.3	s	2	0.556	0.556	-0.1	2.4	50.9	49
	4	4	0.549 (0.544)	-1.1 (-2.70)	8.6 (8.8)	vb (vb)	1 (1)	0.554 (0.5534)	0.547 (0.5497)	-0.7 (-0.37)	0.8 (1.21)	44.8 (40)	46
	5	5	0.552	-0.9	10.5	s-b	3	0.552	0.553	-0.1	1.9		43
	6	4	0.544	-1.4	10.9	s	3	0.554	0.551	-0.3	1.4		41
	6	4	0.547	-1.5	11.8	b	3	0.555	0.549	-0.7	1.1		37
SA 2	6	4	0.543 (0.584)	-1.6 (-0.8)	10.5 (10.8)	s (b)	3 (2)	0.555 (0.5514)	0.551 (0.5487)	-0.3 (-0.28)	1.6 (1.0)	39.7 (34)	37
CA	6	4			12.6	b	2	0.5588	0.559	0	3.0		

Tab.1

Experimental data. $\epsilon_{||}^{\parallel} = (a_{||} - a_0)/a_0 \approx 0.56 \cdot (a_{||} - a_{\perp})/a_0$
 $(a_0 = \text{bulk lattice constant})$. $\epsilon_{Si}^{\parallel} = (a_{||} - a_{Si})/a_{Si}$ with
 assumption $a_{Si}^{\parallel} = a_{||}^{\parallel} = a_{||}$ (pseudomorphic growth). $\epsilon_{Ge}^{\parallel}$ can be
 obtained from $\epsilon_{Si}^{\parallel}$ in good approximation from $\epsilon_{Ge}^{\parallel} \approx 4.2 - \epsilon_{Si}^{\parallel}$.
 Average number of monolayers (ML) $m+n = 4D/a_{\perp}$ with $D =$
 superlattice period. Broadening of SR in $\langle 220 \rangle$ given by $w : s =$
 sharp, $b =$ broad, $vb =$ very broad, SR = number of visible
 orders of SR close to (400) reflections. XRD results are given
 in brackets.

This is consistent with the observation of a misfit dislocation network at the interfaces (not shown). Buffer stoichiometries as deduced from diffraction deviate from nominal y appreciably towards smaller values. Comparison with XRD show differences in the calculated values for the strains of up to a factor of 2 which are attributed to limitations in the accuracy of average lattice parameter measurements by TEM and to the effect of local inhomogeneities leading to deviations from averaged values.

The average composition of superlattices was determined locally (area $\approx 0.1 \mu\text{m}^2$) by EDS on cross-section specimens. The different compositions of the superlattices were deduced from the integrated intensities of the SiK and GeK lines using the thin film approximation [6]. The data given are averaged values from up to four local composition measurements. Tab.1 shows results for the averaged Ge concentration, C_{Ge} , together with measurements taken by Rutherford Backscattering Spectroscopy (RBS) [7] and values deduced from XRD lattice parameter measurements. In general the data agree well for superlattices of good perfection. Significant deviations in the Ge concentrations deduced from XRD are observed for SLS of lower perfection.

CONCLUSIONS

The combination of transmission electron microscopy of cross-section specimens and X-ray diffraction allows a comprehensive and detailed structural characterisation of short-period Si_mGe_n superlattices. The morphology and defect structure of such superlattices grown on different virtual substrates depends sensitively on the growth conditions. By choice of improved growth parameters for the virtual substrates superlattices of good morphology can be obtained. However, defects are still present for the conditions investigated so far. The comparison between the results obtained by the two techniques show that it is essential at least for superlattices of lower perfection to consider the effects of local inhomogeneities.

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VERY THICK COHERENTLY STRAINED $\text{Ge}_x\text{Si}_{1-x}$ LAYERS GROWN IN A NARROW TEMPERATURE WINDOW

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ABSTRACT

Strain relaxation of $\text{Ge}_x\text{Si}_{1-x}$ layers is studied as a function of growth temperature. Extremely thick coherently strained layers whose thicknesses exceed more than fifty times of the critical thicknesses predicted by Matthews and Blakeslee's model were successfully grown by MBE. There exists a narrow temperature window from 310 °C to 350 °C for growing this kind of high quality thick strained layers. Below this temperature window, the layers are poor in quality as indicated from RHEED patterns. Above this window, the strain of the layers relaxes very fast accompanied with a high density of misfit dislocations as the growth temperature increases. Moreover, for samples grown in this temperature window, the strain relaxation shows a dependence of the residual gas pressure, which has never been reported before.

INTRODUCTION

Since $\text{Ge}_x\text{Si}_{1-x}$ heterostructures and superlattices with band structures of either type I or type II have been successfully grown by molecular beam epitaxy (MBE), device quality films of strained-layer $\text{Ge}_x\text{Si}_{1-x}$ grown on Si have shown a great deal of promises for many high-speed electronic and optical device applications. The SiGe system offers many advantages. First of all, high performance devices can be intergrated at low cost by using compatible and matured Si VLSI technology. Secondly, its tunable band gap which is in the near infrared range (1.3 μm to 1.55 μm) with a minimal fiber glass loss, makes the monolithic integration of opto-electronics devices possible. So far, high-speed devices, such as modulation doped field effect transistors (MODFET)[1, 2] heterojunction bipolar transistors (HBT)[3, 4, 5, 6] have been successfully demonstrated. For optical devices, photodectors near 1.3 μm [7, 8, 9] also have been successfully fabricated. Yet, due to the nature of the strain layer (the lattice mismatch between Si and Ge is $\approx 4.2\%$) misfit dislocations can result if the film thickness is too large. $\text{Ge}_x\text{Si}_{1-x}$ heterointerfaces with good quality (free of or few misfit dislocations)[10] have been fabricated on both Si and $\text{Ge}_y\text{Si}_{1-y}$ buffer, provided that the strained layers are below the so called "Critical Thickness". To achieve high crystallinity of $\text{Ge}_x\text{Si}_{1-x}$ strained films with a larger critical thickness, it appears necessary to grow the films at lower temperature[11].

EXPERIMENT

The crystal quality and the relaxation of a strained layer are well known to be dependent on the growth parameters such as growth temperature, growth pressure, and the growth rate. Therefore, with the growth rate fixed, samples used in this study were grown at different substrate temperatures and different growth pressures by MBE. Before the growth, the substrates were prepared by Shiraki's method. The native oxide was removed by *in situ* heating to 900 °C after loading the samples into the growth chamber. After removing the oxide, an 1500 Å Si buffer layer was deposited first prior to the growth of $\text{Ge}_x\text{Si}_{1-x}$ layers. The growth temperature in our strained layer study was varied from 250

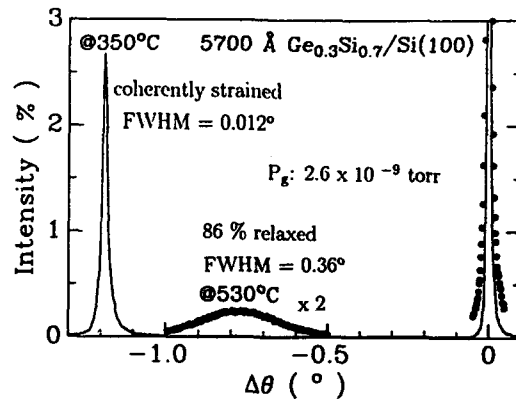


Figure 1: X-ray rocking curve measured on a 5700 Å thick $\text{Ge}_{0.3}\text{Si}_{0.7}$ layer grown at 310 °C at the (400) reflection. The result measured from a sample with the same composition and thickness but high growth temperature, 530 °C, also shown for comparison.

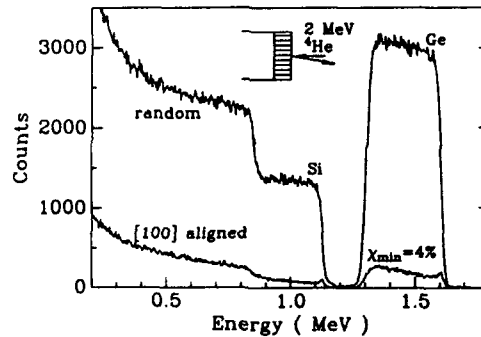


Figure 2: RBS channeling data in (100) direction for sample CH114. The χ_{\min} is $\sim 4\%$.

°C to 530 °C at a fixed growth pressure for one set of samples having 30% Ge. For the second set of samples, the growth pressure was varied while the growth temperature was fixed at 350 °C. In another set of samples, the Ge concentrations of 60% and 80% were grown at the same growth temperature of 350 °C. After the growth, samples were characterized by RBS for the Ge concentration and the total thickness. Channeled RBS and double crystal X-ray were used to probe the crystallinity and the amount of strain. Cross-sectional transmission electron microscopy (X-TEM) was used to assist the observation for interface dislocations.

RESULTS AND DISCUSSIONS

Fig. 1 shows the result of X-ray rocking curve for sample CH114 which was grown at a temperature of 310 °C with a Ge concentration of 30%, and a layer thickness of 5700 Å. The result shows a highly strained film with a parallel strain $\approx 0\%$. Moreover, a high intensity peak of the strained layer was observed and a full-width at half-maximum (FWHM) of only $\sim 2 \times 10^{-4}$ radian indicated that the $\text{Ge}_{0.3}\text{Si}_{0.7}$ film was of high crystallinity. The

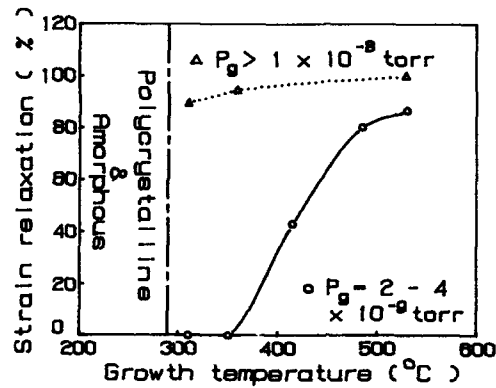


Figure 3: Temperature dependence and growth pressure dependence of strain relaxation for $\text{Ge}_{0.3}\text{Si}_{0.7}$ alloy films with a thickness of 5700 Å. The — o — data line is for varying growth temperature but at a fixed growth pressure $\sim 2-3 \times 10^{-9}$ torr. The ... Δ ... indicates for a similar temperature variation but at a higher fixed growth pressure $> 8 \times 10^{-9}$ torr. There is a boundary of growth temperature at 290 °C. Below the boundary, the film was either polycrystalline or amorphous as indicated from RHEED patterns.

finite FWHM arises from the thin film nature, a finite thickness of 5700 Å in this case. The film quality was confirmed by the [100] channeling of the sample as shown in Fig. 2, indicating a channeling yield χ_{min} of 4%. The film quality was further confirmed by X-TEM and there was no observable defects at the interface and in the film. All of these results show that the $\text{Ge}_{0.3}\text{Si}_{0.7}$ buffer layer is highly coherently strained and defect free. As the growth temperature increased from 310 °C to 530 °C at the fixed growth pressure of about 2.5×10^{-9} torr, the layer relaxed, accompanied with the generation of a high density of dislocations, especially when the temperature was above 410 °C. This behavior can be easily seen in Fig. 3. The maximum allowable growth temperature for achieving a highly coherently strained film is 350 °C as indicated in this figure. Therefore, a temperature window in the range of 310 °C - 350 °C may be defined for the coherent growth. Above this temperature window, the layers relaxed very fast when the growth temperature increased as discussed before. Below this window, the layers are poor in quality as indicated from RHEED patterns and subsequent *ex situ* analysis. Moreover, when the growth pressure was increased, the relaxation of the $\text{Ge}_{0.3}\text{Si}_{0.7}$ layers became prominent as shown in Fig. 4. The degree of the relaxation in the layer reached $\sim 86\%$ as the growth pressure increased to $\sim 1 \times 10^{-8}$ torr. Fig. 5 shows that the FWHM of the X-ray rocking curve increases from $\sim 2 \times 10^{-4}$ radian to $\sim 6 \times 10^{-3}$ radian as the growth pressure increases from $\sim 3 \times 10^{-9}$ torr to $\sim 1.6 \times 10^{-8}$ torr. Two thicker samples grown at 350°C with the Ge concentration of 30% were used to probe the pseudomorphic thickness. The results of X-ray rocking curve measurements are shown in Fig. 6(a). For the 7000 Å thick sample, a coherently strained film was obtained; for the 8800 Å sample, however, the strain was partially relaxed and two peaks were observed. Fig. 6(b) also shows the X-ray results measured from 2000 Å and 700 Å thick $\text{Ge}_{0.6}\text{Si}_{0.4}$ layers. For the 2000 Å film, the strain was relaxed completely while for the 700 Å layer, the strain was only partially relaxed (a careful inspection showed that there were two peaks).

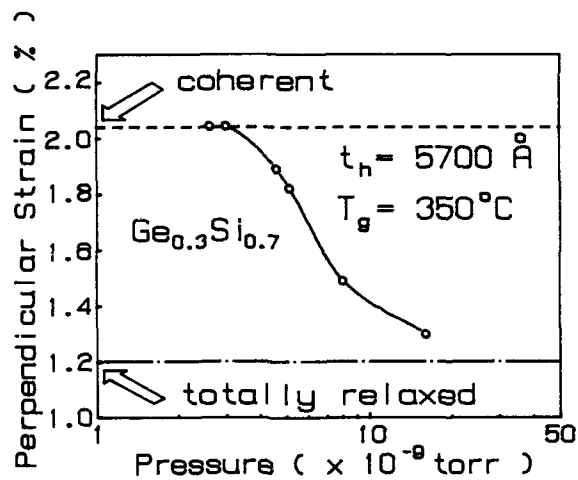


Figure 4: Growth pressure dependence of strain relaxation characterized by X-ray rocking curve measurement.

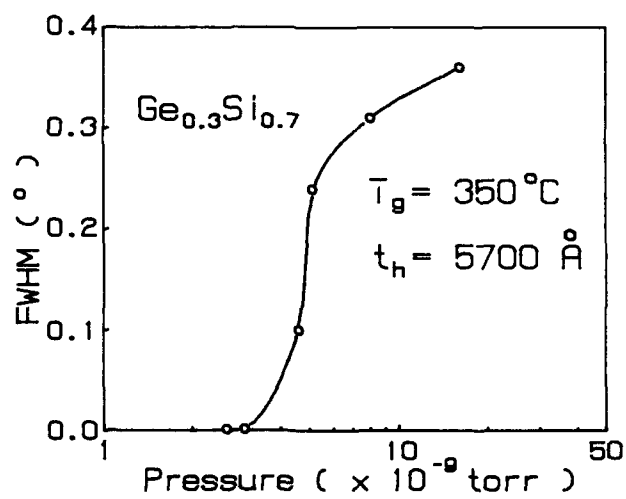


Figure 5: FWHM from the X-ray rocking curve measurement for samples grown at different growth pressure.

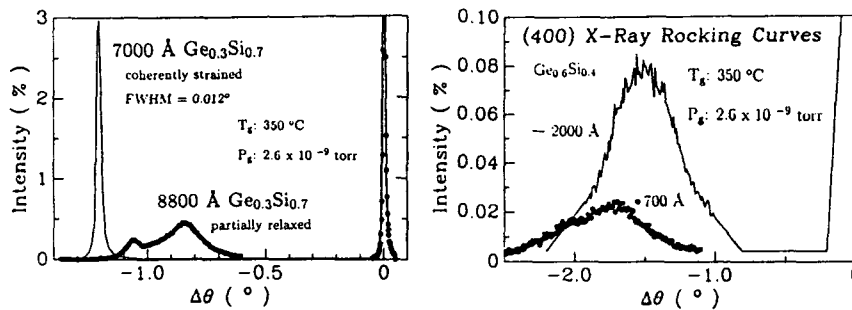


Figure 6: (a) X-ray rocking curve measurement for $\text{Ge}_{0.3}\text{Si}_{0.7}$ alloy films with thicknesses of 7000 Å and 8800 Å grown at same growth condition. (b) X-ray rocking curve data for $\text{Ge}_{0.6}\text{Si}_{0.4}$ alloy films grown at the same growth condition as (a) but with different thicknesses.

There are a vast number of reports discussing critical thickness[12, 13, 14]. These works indicate a large discrepancy of the so-called critical thickness. For example, the critical thickness observed by Houghton et al.[15] was in a good agreement with the equilibrium theory of Matthews and Blakeslee which showed that the critical thickness was 80 Å for a Ge concentration of 30%. On the other hand, Bean et al. reported a critical thickness of about 500 Å for the same Ge concentration. Similarly, Croke et al.[16] and Miles et al.[17, 18] observed a substantially large critical thickness beyond that of the equilibrium theory for a slightly different Ge concentration (20%). Nevertheless, for the film thickness exceeding the critical thickness obtained by Bean et al., they also observed segregation of Ge and appearance of threading dislocations near the interface. In our study, however, we did not. It implies that there are other factors involved in the nucleation of defects, depending on growth parameters. It is clear from our study that the critical thickness depends on the growth pressure as well as the growth temperature. For high growth pressure, a significant amount of impurities can be incorporated to the film and they act as nucleation sites for dislocations to form, causing strain relaxation. It is interesting to compare our data of a coherently strained layer thickness of more than 7000 Å for the Ge concentration of 30% Ge with that of Croke et al.. It is apparent that the strain relaxation in the present study is slower than that of Croke et al.. This may be due to their higher growth pressure of 5×10^{-9} torr compared with 2.5×10^{-9} torr used in our experiment. This observation supports our assertion of the strain relaxation dependence on the growth pressure.

SUMMARY

In summary, extremely thick coherently strained films with high crystallinity can be grown at low temperature. In the narrow temperature window, the relaxation of a strained film increases as the growth pressure increases. When the growth parameters are controlled properly, very thick and high quality strained $\text{Ge}_x\text{Si}_{1-x}$ layers can be obtained with thicknesses much greater than the "critical thickness" reported previously.

ACKNOWLEDGMENT

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MEASUREMENT OF VALENCE BAND OFFSET IN STRAINED Ge_xSi_{1-x}/Si HETEROJUNCTIONS

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ABSTRACT

The valence band discontinuity ΔE_v in the coherently strained Ge_xSi_{1-x}/Si heterostructure is determined using I-V-T measurement. The electrical measurements of the band discontinuity of the pseudomorphic layers are difficult due to the thin layer imposed by the strain. Recently, low temperature growth of thick layer (>100 nm) of coherently strained Ge_xSi_{1-x} on Si has been achieved and thus made it possible for an accurate electrical measurement of band offset. The results obtained are in good agreement with the theoretical calculations by pseudopotential method.

INTRODUCTION

In recent years, Ge_xSi_{1-x}/Si heterostructures have been the subject of increasing theoretical and experimental interest. Strain induced band gap narrowing has been theoretically predicted by People [1], and experimentally demonstrated by Lang et al. [2]. In the Si-Ge heterosystem, strain effects add a new degree of freedom in design of novel band engineered heterostructures. Both the band gap and the band alignment are dependent on how each layer is strained. At the same time, due to critical thickness limitation on the coherently strained layer, it is difficult to make accurate measurement of important physical parameters such as mobility and band discontinuity. In this paper, we will discuss the measurement of valence band offset in Ge_xSi_{1-x}/Si heterostructure using thick, metastable, coherently strained Ge_xSi_{1-x} layers.

Early experimental observations by People et al. [3] had indicated that the major portion of band gap discontinuity in GeSi/Si system is in the valence band. This was later substantiated by the theoretical calculations of Van de Walle et al. [4] and People et al. [5]. There have been several attempts on experimental verification of band alignment using x-ray photoelectron spectroscopy (XPS) of Ge_xSi_{1-x}/Ge_ySi_{1-y} layers with different Ge compositions [6, 7, 8]. They reported large experimental error (> ±60 meV) associated with the XPS method.

Figure 1: Schematic diagram showing typical sample used to measure valence band offset.

Cap	Ge _x Si _{1-x}	$p = 5 \times 10^{17} \text{ cm}^{-3}$
Barrier	Si	i
Buff	Si	$p = 5 \times 10^{17} \text{ cm}^{-3}$
Sub	Si	p^+

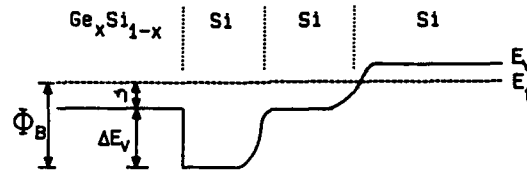


Figure 2: Band diagram for typical heterostructure used for I-V-T analysis.

In the present work, we have employed I-V-T measurement to investigate the valence band discontinuity in the strained $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterosystem. This method has been used extensively to study the band alignment in AlGaAs/GaAs heterostructures [9, 10], which is a lattice matched system with no critical thickness limitation. In pseudomorphic heterostructures, such as in the Ge-Si heterosystem, this method can not be readily applied. Due to the lattice mismatch, at least one of the layers in $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterostructures is strained. Moreover, only a limited thickness of a coherently strained layer can be grown. For example, if a coherently strained $\text{Ge}_x\text{Si}_{1-x}$ layer is grown on a relaxed Si buffer layer, the Ge composition must be kept low for growth of a thick contact layer. On the other hand, if a strained silicon layer is grown on a relaxed $\text{Ge}_x\text{Si}_{1-x}$ buffer layer, the barrier thickness must be kept small at high Ge compositions. However, when the barrier is thin, the tunneling through the barrier obscures the thermionic process at low temperatures.

In order to overcome the critical thickness problem, we have used a low temperature growth technique [11] to obtain metastable $\text{Ge}_x\text{Si}_{1-x}$ layers with considerably larger pseudomorphic thickness than the conventional critical thickness. The structure as shown in Fig. 1 is designed such that the main component of the current is due to thermionic emission, and thereby the I-V-T method is fully exploited.

EXPERIMENTAL DETAIL

Figure 1 shows a schematic diagram of the typical sample structure used for the measurement. The samples used for this study were grown in a Si-MBE system on a p^+ Si substrate. Si wafers were chemically cleaned by Shiraki's method prior to loading in the system. Once inside the MBE chamber, the wafers were heated to 900 °C for desorption of the protective oxide layer. The substrate temperature was maintained at about 550 °C during the growth of the Si layer, and later it was reduced to 350 °C for the growth of the strained $\text{Ge}_x\text{Si}_{1-x}$ layer. The structure consists of a 300 nm p-type Si buffer layer, followed by a 50 nm of an undoped Si layer, and capped by a thick p-type strained $\text{Ge}_x\text{Si}_{1-x}$ layer. Depending on the Ge concentration, x , the thickness of the strained $\text{Ge}_x\text{Si}_{1-x}$ layer was varied from 100-400 nm.

Table I. Sample structure and results.

sample i.d.	Ge Mole fraction	Thickness $\text{Ge}_x\text{Si}_{1-x}$ (Å)	Acceptor concentration (cm^{-3})	Measured ΔE_v (meV)	Theoretical calculation (meV)
CH162	0.3	3200	5×10^{17}	250 ± 20	252
CH180	0.38	1500	5×10^{17}	330 ± 20	320

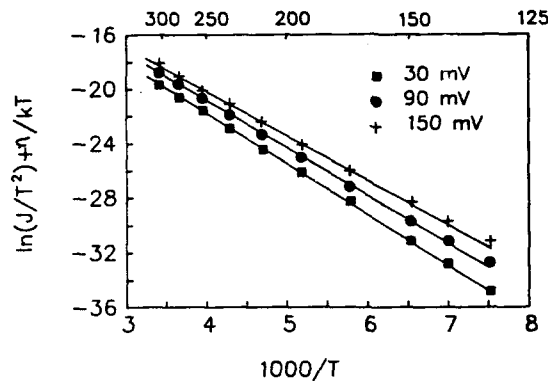


Figure 3: Arrhenius plot of I-T data for several different bias points.

In order to avoid complications associated with the heavily doped semiconductors such as bandgap narrowing effect and strain relaxation, the layers were chosen to be lightly doped. The crystallinity and the quality of these layers has been verified by x-ray rocking technique and the Ge composition was checked by RBS.

The samples were processed using standard photolithography and lift-off procedures. Due to the metastability of the strained layers, high temperature alloying of ohmic contacts was avoided. The contacts were formed by evaporating Al and followed by annealing at 300 °C for 5 min. The top contacts which were circles of 25–100 microns in diameter were defined by a lift-off procedure. Device isolation was achieved by mesa etching down to the p^+ substrate. Several pieces of the processed sample were mounted on TO-5 headers and selected devices were wire-bonded for I-V-T measurement.

The I-V setup consists of a Keithley 602 electrometer, one Pd power supply model 2005, and two HP 3478A multimeters. Temperature control was accomplished with a resistive heater, a Harrison laboratories Inc model 6224A power supply, and L & N temperature controller. Temperature was measured by reading the voltage across a double junction J-type thermocouple wire. We were able to measure current levels down to 100 femto-Amperes, and the accuracy of our temperature reading was in the range of ± 0.5 °C.

DATA ANALYSIS

The low voltage I-T data are analyzed based on the assumption that the current transport is governed by simple thermionic emission theory:

$$J = A \cdot T^2 \exp\left\{\frac{-\Phi_B}{kT}\right\} \quad (1)$$

where

$$\Phi_B = \Delta E_v + \eta. \quad (2)$$

As Batey and Wright [12] have pointed out, in heterostructures Φ_B is from the top of the barrier to the Fermi level, as shown in Fig. 2. Moreover, the band offset can not be obtained by simply subtracting the ionization energy η , from Φ_B . We need to take into consideration the temperature dependence of the Fermi level in our data analysis. In the Ge-Si heterosystems, the ionization energy of dopant impurities such as boron varies from 10 meV to 45 meV, which may result in significant temperature dependence of the

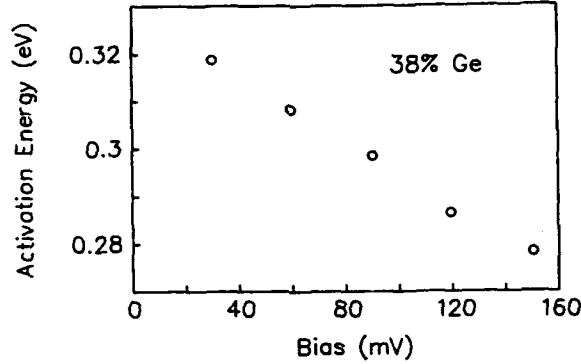


Figure 4: Activation energy for the $\text{Ge}_{0.38}\text{Si}_{0.62}/\text{Si}$ at different bias points.

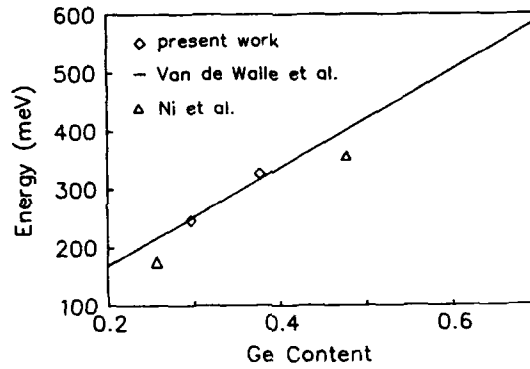


Figure 5: Valence band alignment in strained $\text{Ge}_x\text{Si}_{1-x}$ on Si substrate heterostructures.

Fermi level. For simplicity, we have assumed linear variation of ionization energy with germanium concentration, i.e.

$$E_i(x) = 10(\text{meV}) + x(45 - 10) \quad (3)$$

where x is the germanium concentration in $\text{Ge}_x\text{Si}_{1-x}$ alloy. The ionization energy obtained by this approximation has been used in the calculation of η , which has been incorporated in the data analysis.

The Arrhenius plot of I-V-T data of $\text{Ge}_{0.38}\text{Si}_{0.62}/\text{Si}$ sample is shown in Fig. 3. Straight lines are plotted by the linear least-squares fitting method. The linear fitting shows a small standard deviation, ± 3 meV, which justifies the use of thermionic emission theory for data analysis.

The valence band offset is extracted from the extrapolation of the activation energy versus bias data, as shown in Fig. 4. At zero bias, we estimated the band bending close to hetero-interface is negligible. This might be a major source of error, which is included in the data uncertainty. We have designed all the semiconductor layers in and around the barrier with such a low level of doping that no significant band bending can occur (see

table I). The band offsets we obtained by I-V-T method are generally larger than the values reported by Ni et al. [6] using x-ray photoelectron spectroscopy (see Fig. 5). Our results are within 10% of pseudopotential calculations.

SUMMARY

The valence band discontinuity for strained layer $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ was investigated using I-V-T method. The sample thicknesses and doping levels were designed to realize flat bands close to the heterointerface. The results obtained are in good agreement with pseudopotential calculations. Typical band offset measurement for $\text{Ge}_{0.38}\text{Si}_{0.62}/\text{Si}$ is about 330 meV. This implies that the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterosystems have high potential in band-engineered devices where a large band discontinuity is desirable.

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LOW THREADING DISLOCATION DENSITIES IN THICK, RELAXED Si_{1-x}Ge_x BUFFER LAYERS

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ABSTRACT

A series of relaxed Si_{1-x}Ge_x alloy layers with germanium contents up to 70% has been deposited on silicon. Although direct deposition of these highly mismatched layers on silicon gave dislocation densities of 10⁹ - 10¹⁰cm⁻² and poor morphology, it was found that the use of a linear grade enabled completely relaxed Si_{0.3}Ge_{0.7} layers with defect densities of ~3.10⁵cm⁻² to be obtained. However, if the grading was too rapid the dislocation density was much higher. The role of dislocation nucleation and propagation in determining the required thickness of graded layer is discussed.

INTRODUCTION

Heteroepitaxy of mismatched materials has tended to involve thin fully strained layers, such as in the SiGe heterojunction bipolar transistor, or thick relaxed layers, such as GaAs on Si. In the SiGe materials system in particular several structures require a "substrate" with an in-plane lattice constant between that of silicon and germanium. High electron mobility transistors have been demonstrated on relaxed Si_{0.75}Ge_{0.25} layers [1], and it has been proposed that certain Si/Ge superlattices on Si_{0.3}Ge_{0.7} relaxed layers should have a pseudo-direct bandgap [2]. The attraction of such structures is their compatibility with silicon technology, but to make use of them it is necessary to produce relaxed alloy layers on silicon with a low density of threading dislocations and good surface morphology.

The relaxation of Si_{1-x}Ge_x layers on Si(001) has been shown to involve glissile 60° dislocations at low mismatch (x<0.5) and sessile 90° dislocations at higher mismatch [3]. To minimise the threading dislocation density it is important to make the interfacial segment of each dislocation as long as possible. It is therefore unlikely that relaxation in a system dominated by 90° dislocations, which only extend slowly by climb, will give rise to a low threading dislocation density. A further complication is that three dimensional growth of alloy layers occurs above a certain temperature [4], which is ~550°C for x>0.5. This imposes an upper limit on growth temperature which will tend to restrict average dislocation length.

EXPERIMENTAL DETAILS

The layers in this study were deposited in a VG Semicon V80 Si MBE system on 100mm n+ (001) substrates. An Inficon Sentinel III unit controlled the silicon and germanium fluxes from two 156cm³ Airco Temescal e-beam evaporators. The oxide removal and growth procedure are described in detail elsewhere [5]. The density of dislocations threading from the substrate/epitaxial interface to the surface in homoepitaxial silicon grown under these conditions is

typically $<10^3\text{cm}^{-2}$. Particle induced defect levels are in the range $10^2\text{--}10^3\text{cm}^{-2}$.

Transmission electron microscopy (TEM) was carried out on a JEOL 200CX electron microscope operated at 200kV. Cross-sectional and plan-view specimens were prepared by a combination of mechanical dimple polishing and argon ion beam milling.

RESULTS

Ungraded Layers

A range of $\text{Si}_{.3}\text{Ge}_{.7}$ layers were deposited at various temperatures between 500°C and 750°C . A rough guide to the threading dislocation density was obtained from the width of the alloy peak in the 004 reflection of the X-ray rocking curve. Densities $>10^8\text{cm}^{-2}$ were generally indicated. The surface morphology under Nomarski optical microscopy tended to be rougher for the layers deposited at higher temperatures. TEM study of such layers showed that the threading dislocation densities were indeed extremely high ($>10^{10}\text{cm}^{-3}$). The layers also had rough surfaces and contained stacking faults. A TEM cross-section of a $\text{Si}_{.3}\text{Ge}_{.7}$ layer deposited directly on silicon at 500°C is shown in figure 1.



Figure 1: TEM cross-sectional micrograph of a 130nm $\text{Si}_{.3}\text{Ge}_{.7}$ layer grown directly on Si at 500°C .

In contrast, dislocation densities in germanium layers on silicon tended to be somewhat lower ($\sim 10^9\text{cm}^{-2}$) and a smooth top surface was obtained. Use of a $0.1\text{--}1\mu\text{m}$ germanium buffer layer between the silicon substrate and $\text{Si}_{.3}\text{Ge}_{.7}$ alloy layer was found to give extremely good alloy morphology. This was confirmed by the well defined layering in superlattices of 0.28nm Si and 1.12nm Ge studied by TEM. However, a threading dislocation density of $1\text{--}4 \cdot 10^8\text{cm}^{-2}$ from the relaxed Ge and alloy layers was still observed.

Graded Layers

As stated previously, there is a tendency to form non-glide defects such as 90° dislocations and stacking faults at interfaces with high mismatch. The simplest way of avoiding such interfaces is a linear grade from silicon to the required alloy concentration. A study of layers graded to 70%Ge was undertaken, allowing comparison with the layers in the previous section. Layer thicknesses of 1, 3 and $10\mu\text{m}$ were investigated, the latter involving a deposition time of 5 hours. The growth temperature of 740°C was designed to maximise the glide velocity [6], and hence the average length of the in-plane segment of the misfit dislocation. For a given degree of relaxation, and ignoring wafer edge effects, the threading defect density should be inversely proportional to this average length.

Figure 2 shows a cross-sectional TEM image of the $10\mu\text{m}$ graded layer, capped with a $2\mu\text{m}$ layer of $\text{Si}_{.3}\text{Ge}_{.7}$ layer which is remarkably defect free. Indeed, the density of threading dislocations was too low to measure in cross-section, and plan-view specimens were needed to measure a level of 3.10^5cm^{-2} .



Figure 2: TEM cross-section of a $2\mu\text{m}$ $\text{Si}_{.3}\text{Ge}_{.7}$ layer deposited on a $10\mu\text{m}$ graded layer on silicon. Only the top $2\mu\text{m}$ of the graded layer is shown.

An investigation of the minimum grade thickness necessary to achieve low dislocation density was undertaken, with the intention of reducing the growth time. Graded layers of 1 and $3\mu\text{m}$ were deposited at the same growth rate (approximately 0.7nm/s) as the $10\mu\text{m}$ sample. One effect of this reduction in growth time is that the maximum distance that dislocations can glide during deposition is reduced, and the average in-plane dislocation length may decrease proportionately. This would lead to an increase in threading dislocation density of a factor of ten for the $1\mu\text{m}$ layer. However, the results from these layers were disappointing. The $3\mu\text{m}$ layer had a dislocation density of about 10^6cm^{-2} (in fact the effective defect density is somewhat lower, as the dislocations are clustered in

groups of 3 to 10). The $1\mu\text{m}$ graded layer had a threading dislocation density of $10^9 - 10^{10}\text{cm}^{-2}$ and severe surface undulations of approximately 100nm compared with 30nm on the other layers. The wavelength of these undulations was $\sim 1\mu\text{m}$.

Nomarski contrast microscopy showed that the furrows and ridges along (110) directions appeared to be unbroken for several millimetres in the case of the $10\mu\text{m}$ layer. For the thinner layers the lines only tended to run for 5 - $10\mu\text{m}$, and there was a patchiness on this scale.

DISCUSSION

From the above results it is apparent that grading from silicon to the required alloy concentration can be extremely effective in reducing the threading dislocation density. There must be a line density of $1.5 \cdot 10^6\text{cm}^{-1}$ 60° dislocations beneath the top $\text{Si}_{.3}\text{Ge}_{.7}$ layer to completely relieve the strain. At an abrupt interface, as in figure 1, the average lateral spacing between the dislocations is only 6nm. In a $10\mu\text{m}$ graded layer the dislocations can be distributed laterally and vertically, with an average spacing of 250nm.

If the average in-plane dislocation length is quite short, then it can be deduced from the final density of threading dislocations and the total length of misfit dislocation necessary to cause the observed relaxation. However, this calculation breaks down if the length becomes comparable to the wafer dimension, as dislocations which have reached the edge of the sample will not be counted in the final threading dislocation density. The average dislocation length will then be over-estimated. The calculated length for the $10\mu\text{m}$ graded layer is 10cm. This cannot be the actual average length, as it is the same as the wafer diameter which implies that some dislocations will have reached the wafer edge, while others may have been trapped at a dislocation "pile-ups" [7] - highly slipped planes which pin dislocations that run up to them. Examination of the surface morphology suggests that dislocations run at least 10mm before meeting a "pile-up", and threading dislocations restricted to these widely spaced regions would not tend to be counted by plan-view TEM.

The free glide of dislocations in the thickest graded layer, compared to the high threading densities and short dislocation lengths in the $1\mu\text{m}$ and $3\mu\text{m}$ graded layers suggests that, below a certain minimum grade thickness, the resistance to dislocation motion increases. This could be due to interactions when dislocations in orthogonal $\langle 110 \rangle$ directions cross each other.

The relaxation process is initiated by dislocation generation at specific centres. A study of $\text{Si}_{.95}\text{Ge}_{.05}$ layers on silicon showed that there are approximately 10^3 centres per cm^2 in our material [8]. Dislocations glide from these centres in the four $\langle 110 \rangle$ directions, and their eventual average length will depend critically on the way in which they interact with dislocations from other nucleation points when they cross their path. This topic has been discussed by Freund [9], who analysed the strain field associated with a misfit dislocation line lying at the substrate-epilayer interface and its interaction with a dislocation gliding towards it in an orthogonal $\langle 110 \rangle$ direction. Blocking was found to occur below a certain thickness which depended on the elastic strain in the epilayer. There are several important differences between a graded layer and a uniform alloy layer:

(1) Using a very thick graded layer to achieve a high alloy concentration will tend to increase the thickness above the gliding dislocations, as there will be a region at the surface where dislocation glide is not energetically favourable, because the stress in that region is not sufficient to overcome the line tension of a

misfit dislocation. A schematic representation of dislocation glide in the graded layer as it is being deposited is given in figure 3. A calculation based on that of Matthews and Blakeslee [10] leads to the following expression for the depth h below the surface at which the forces on the dislocation balance,

$$\frac{(1+\nu)}{(1-\nu)} \frac{h^2}{2L} \times \frac{(a_{Ge} - a_{Si})}{a_{Si}} = \frac{b}{4\pi} \frac{(1-\nu/4)}{(1-\nu)} \ln(4h/b) \quad (1)$$

where L is the total linear grade thickness, ν is Poisson's ratio, b is the dislocation core parameter, a_{Si} and a_{Ge} are the Si and Ge lattice constants and x is the germanium concentration at the top of the graded layer. It has been assumed that $h \sim (1-f)L$ - i.e. that once glide is energetically favourable the elevated growth temperature ensures that relaxation takes place. For a $10\mu\text{m}$ graded layer with $x=0.7$ the thickness h is found to be $\sim 400\text{nm}$, whereas relaxation in a $\text{Si}_{0.3}\text{Ge}_{0.7}$ layer deposited directly on silicon begins at a thickness of $< 2\text{nm}$ [10].

(2) The layer strain associated with relaxation at the top of a graded layer must be much less than that in a single alloy layer. If relaxation is almost complete for a fraction f of the graded layer, as shown in figure 3, then the average mismatch strain operating on dislocation above this level will be only $(1-f)(a_{Ge} - a_{Si})x/2a_{Si}$.

(3) Dislocations at the $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ substrate/epilayer interface cannot move downwards without increasing the strain energy of the system, because the silicon will be put in tensile stress. In the course of relaxation of a weakly graded layer, however, it is generally true that downward dislocation motion will contribute to further relaxation, unless 100% relaxation has already been achieved, which is unlikely. Therefore it is expected that there will be little resistance to downward motion in graded layers, and it should be easier for dislocations which might otherwise have blocked one another to cross. In figure 2 there is evidence of dislocation movement relative to the surface, especially at crossing points, suggesting that this type of interaction may have taken place.

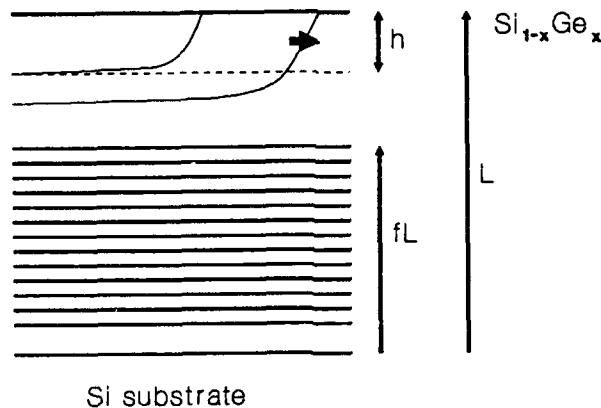


Figure 3: Schematic diagram of the relaxation process in a graded layer. A fraction f is almost fully relaxed. Above this 60° dislocations glide as shown. At depth h below the surface the strain and dislocation line tension forces balance.

From the above it can be seen that two factors reducing the likelihood of pinning in the 10 μ m graded layer are the increased effective thickness above crossing dislocations relative to ungraded layers and the possibility of downward dislocation movement. However, the excess stress driving the dislocation through the material is reduced in comparison with a single alloy layer. In the light of the uncertainties in the reduction in pinning force and the smaller effective stress a quantitative estimate of the minimum grade thickness is not possible. Even without detailed calculations it can be seen that if the thickness is reduced to the point at which pinning is possible, then a huge increase in the threading density will be result, as seen experimentally.

CONCLUSIONS

We have shown that it is possible to improve greatly the properties of relaxed Si₃Ge₇ alloy layers on silicon. The introduction of a germanium buffer layer results in a very much smoother surface, although threading dislocation levels are still high. A 10 μ m graded layer and 740°C growth temperature gave rise to a threading dislocation density of only 3.10⁵cm⁻². The graded layer is used to avoid a highly mismatched interface, which would generate 90° dislocations.

The pinning of dislocations as they cross each other in a graded layer was also discussed. Such pinning effects may account for the very much larger threading dislocation densities found in 3 μ m and 1 μ m graded layers.

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SUPPRESSION OF INTERFACIAL MIXING BY Sb DEPOSITION IN Si/Ge STRAINED-LAYER SUPERLATTICES

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We have studied interfacial mixing of Si/Ge strained-layer superlattices during Si molecular beam epitaxy. The mixing has been shown to be primarily due to the surface segregation of Ge atoms during Si overlayer growth. It has been found that only the Ge atoms on the topmost Ge layer dominantly segregate to the growing surface. It has also been found that the surface segregation of Ge is effectively suppressed by depositing Sb atoms on the Ge layers. It has been demonstrated that Si/Ge superlattices with abrupt Si/Ge interfaces can be grown by depositing Sb. The two state exchange model is used to discuss the surface segregation of Ge and the suppression of the segregation by Sb deposition.

1 INTRODUCTION

Si/Ge strained-layer superlattices (SLS's) are interesting not only from scientific point of view but also with regard to device applications. Short-period Si/Ge SLS's are, in particular, receiving much attention due to the possibility of type conversion from the indirect to the direct bandgap. Realizing abrupt Si/Ge heterointerfaces is essential for desired SLS structures. However, it has been shown that atomic mixing at Si/Ge interfaces occurs during growth of Si/Ge SLS's by using molecular beam epitaxy (MBE). Eberl and his coworkers attributed the origin of the interfacial mixing to surface segregation of Ge atoms during Si MBE growth [1]. However, conclusive data to support their idea have not been obtained yet. On the other hand, it has been recently reported that the Ge segregation is suppressed by depositing dopant atoms such as As, Ga and Sb on the surface of Ge [2-4].

In this paper, the interfacial mixing at Si/Ge heterojunctions was systematically investigated by using x-ray photoemission spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) techniques. The mechanism of the mixing was shown to be the surface segregation of Ge. It was also found that the surface segregation of Ge is effectively suppressed by depositing Sb atoms before Si overgrowth. These phenomena are well understood in terms of the two-state exchange model [5].

2 EXPERIMENTAL

In the present work, we prepared the samples in a conventional silicon MBE system consisting of a growth chamber and a preparation/analysis chamber. Si/Ge heterostructures were formed at 500°C on Si(100) substrates after growing undoped Si buffer layers. Si was

evaporated with an electron beam gun and Ge and Sb were evaporated from Knudsen cells. The growth rates of Si, Ge and Sb were 0.4-0.8 ML/s, 0.23 ± 0.03 ML, and $(3.8 \pm 0.4) \times 10^{-3}$ ML/s, respectively. XPS measurement was performed in the preparation/analysis chamber, where photoelectrons ejected from Ge 2p (1217 eV) and Sb 3d (528 eV) levels were analyzed. SIMS measurement was performed using an ATOMIKA 6500 instrument. O_2^+ primary ions were used for Ge profiling, while Sb profiles were separately obtained using Cs^+ ions.

3 RESULTS AND DISCUSSIONS

In order to study Si/Ge interfacial mixing we made Si/Ge/Si double heterostructures. The Ge layer was commensurately grown on Si buffer layers and the thickness was changed from 1 ML to 4 ML. Ge XPS signal intensities were measured varying the thickness of Si overlayers. Figure 1 shows Ge XPS signal intensities, $I(x)$, as a function of the Si overlayer thickness, x . Here, the intensities are normalized by the initial intensity, $I(0)$, before Si overgrowth. It should be noted that Ge atoms are detected even after overgrowth of 10 nm thick Si which is thicker than the photoelectron escape depth. This strongly suggests that the origin of the interfacial mixing at Si/Ge heterojunctions is surface segregation of Ge atoms during Si MBE growth.

It is interesting that the surface segregation depends on the thickness of the Ge layer. This tendency can be understood by considering the Ge XPS signal as superposition of photoelectrons ejected from Ge atoms in three regions; Ge atoms staying at the original Ge layer, Ge atoms segregating to the Si surface

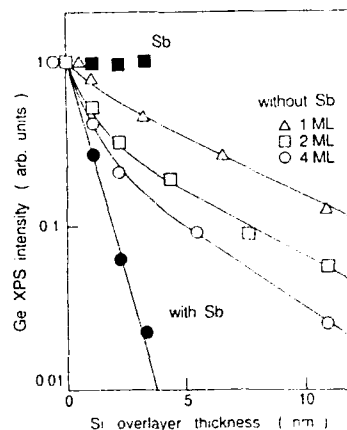


FIG. 1. Normalized Ge XPS signal intensities as a function of Si overlayer thickness. Solid lines indicate XPS intensities calculated by eq.(1).

and Ge atoms incorporated in the Si overlayer, as shown in Fig. 2. That is, the Si overlayer thickness dependence of the Ge XPS signal intensity is described as follows;

$$I(x)/I(0) = (1 - \theta/N) e^{-x/a} + \theta/N e^{-x/b} + \theta/N \int_0^x (1/b) e^{-x'/b} e^{-(x-x')/a} dx', \quad (1)$$

where a is the escape depth of photoelectrons through the Si overlayer, b is the $1/e$ segregation decay length of Ge, N is atomic layer number of the initial Ge layer, and θ represents the number of Ge layers segregating to the surface. Here, the value of a is known to be about 0.8 nm. We calculated eq.(1) by treating b and θ as fitting parameters and excellent results were obtained when $b=4.4, 5.4, 6.0$ nm, and $\theta=1.0, 0.7, 0.7$ ML for the case of $N=1, 2,$ and 4 ML, respectively, as shown in Fig. 1. It

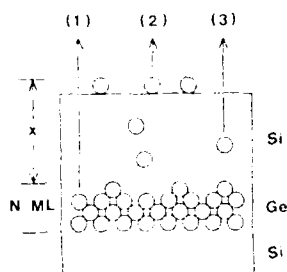


FIG. 2. Schematic view of photoelectrons ejected from Ge atoms in three regions.

is noteworthy that θ is equal or less than 1 ML in all cases. This means that only Ge atoms of the topmost Ge layer leave the original Ge region and segregate to the Si surface and that the underlying Ge atoms remain at the original site during MBE growth and do not take part in the segregation.

This result gives a foundation that the two-state exchange model, where only atoms in surface and subsurface states are taken into account for the segregation, can be used to explain the Ge segregation. The details of the model will be discussed later.

Next we investigated the role of Sb which is known as a strong segregant in MBE-grown Si in the formation of Si/Ge heterointerfaces. Before Si overgrowth on commensurately grown Ge layers, 0.75 ML of Sb was deposited on the Ge surface. Then Ge XPS intensities were measured as a function of the thickness of Si overlayer. Normalized XPS intensities of Ge and Sb are shown in Fig. 1 by filled circles and squares, respectively. It is remarkable that the Ge segregation is significantly suppressed by Sb deposition and it was found that the variation of the Ge XPS intensity can be de-

scribed by taking into account of only the first term in eq.(1). This implies that the segregation decay length of Ge becomes less than the escape depth of photoelectrons, that is, 0.8 nm. On the other hand, the XPS intensity of Sb does not change regardless of the Si overlayer thickness, suggesting that almost all Sb atoms segregate to the surface of the Si overlayer at the growth temperature.

In order to confirm the effectiveness of Sb deposition even for growth of Si/Ge superlattices, SLS's with eight periods each of which consists of 3 ML Ge and 30 nm Si layers were grown at 500°C. 0.75 ML Sb was deposited only on the surface of the 5th Ge layer. Figure 3 shows SIMS profiles of Ge and Sb in

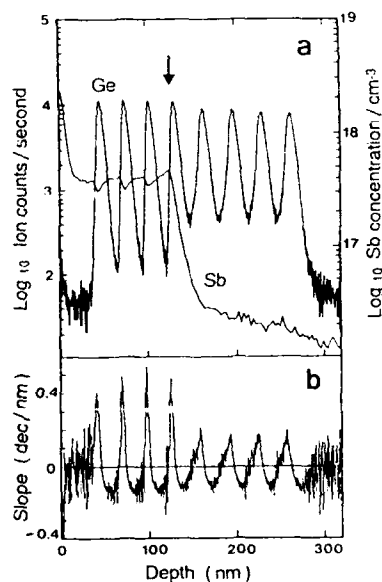


Fig. 3. SIMS profiles of Ge and Sb in the Si/Ge SLS (a) and the slope of the Ge profile (b). 0.75 ML Sb has been deposited on the surface of the 5th Ge layer (arrow) before Si overgrowth.

the SLS (a) and the slope of the Ge profile, i.e., the first derivative, (b) as a function of the depth. It can be seen in this figure that the Ge profile exhibits a sudden change and becomes very sharp after the 5th Ge layer where Sb is deposited. The change is more conspicuous in Fig. 3(b), where the maximum of the slope after Sb deposition is twice as large as that before Sb deposition. This result shows that the Ge surface segregation in SLS structures is effectively suppressed by Sb deposition. The Ge segregation decay lengths before and after Sb deposition are estimated to be 1.9 nm and 0.7 nm, respectively. On the other hand, almost all Sb atoms deposited on the 5th Ge layer are seen on the surface of the SLS. Sb atoms always float on the growing surface and suppress the Ge segregation during the SLS growth. This result obtained by SIMS measurement is consistent with that of XPS measurement where the segregation decay length of Ge is reduced from about 5 nm to less than 0.8 nm by Sb deposition. The small difference in the segregation decay length between XPS and SIMS measurements will be quantitatively discussed elsewhere.

The mechanism of the suppression of Ge surface segregation by Sb deposition can be also understood in terms of the two-state exchange model. In this model, we consider the exchange of atoms in subsurface and surface states. Figure 4 schematically shows the potential energy diagram for Sb atoms in the Si/Sb/Ge system. The surface state is below the subsurface state by the amount of E_b which is a characteristic energy for surface segregation. The atom in the subsurface jumps over the activation energy barrier denoted by E_a . Since this energy is less than the barrier for bulk diffusion, we may neglect the thermal diffu-

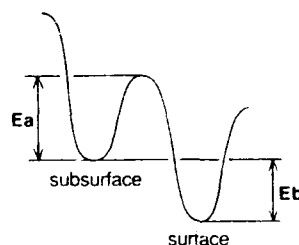


Fig. 4. Schematic potential energy diagram to describe exchange processes between atoms in surface and subsurface states.

sion into substrates. Before Si deposition, Sb atoms situate on the surface and Ge does not segregate to the surface. This is because E_b of Sb is much larger than that of Ge. Once Si deposition starts on the Sb-covered Ge layer, the site of Sb changes to the subsurface and Si is located on the surface. Since E_b of Sb is much larger than that of Si, this situation is very unstable and then the exchange between Sb and Si atoms takes place to reduce the total energy. The exchange between Si and Ge, i.e. intermixing, does not take place in this case, since the mixing corresponds to the bulk diffusion which hardly occurs at this temperature. This is an explanation for the reason why Sb suppresses the intermixing of Si/Ge heterostructures and it is noteworthy that the energy of E_b is a key for the effect.

So far, the value of E_b has been estimated for several materials in the case of Si MBE as listed in Table I. It can be expected from this table that Ga is also very effective to suppress Ge segregation and this is true as Zalm et al. reported. This scheme is fairly general and there are many other possible combinations. For example, we observed that B surface segregation is also suppressed by Sb deposi-

tion. In order to make this technique more practical, however, it is desired to find atoms or molecules which are electrically inactive and have large segregation energy E_b , since such atoms as Sb and Ga are dopants for Si and Ge.

more, it was found that the surface segregation of Ge is suppressed by depositing Sb atoms before Si overgrowth. Using this technique, it was demonstrated that Si/Ge SLS's with abrupt heterointerfaces can be grown.

Table I

Free energy (E_b) of surface segregation on Si(100).

Dopant	E_b (eV)
Sb	1.2 ref. 6
Ga	1.0 ref. 6
Ge	0.3 ref. 7
B	0.3 ref. 8

4 CONCLUSION

It was clarified by XPS measurement that the interfacial mixing is dominated by the surface segregation of Ge atoms during Si overlayer growth. Only the Ge atoms on the topmost Ge layer were found to dominantly contribute to the segregation. This result supports the two-state exchange model. Further-

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DEFECT CENTERS FORMED DURING
WET OXIDATION OF SI-GE/SI HETEROSTRUCTURES

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ABSTRACT

Germanium incorporated oxide films formed by wet oxidation of SiGe substrates have been studied using Electron Paramagnetic Resonance. SiGe layers 400 nm thick were prepared by molecular beam epitaxy and oxidized in a steam ambient at 900° C. After a 10 Mrad x-ray irradiation, an oxide defect with a zero crossing at $g=1.995$ is observed. Comparison of the spectrum with that obtained from Ge-doped silica suggests that the defect observed in the thin film is an oxygen vacancy related defect, a Ge E' center.

INTRODUCTION

Today efforts are being actively pursued to tap the advantages of Ge as an electronic material by employing SiGe heterostructures in optoelectronic and microelectronic components [1,2]. Several investigators have reported that thermal oxidation of silicon, a key step in microelectronic processing, is altered by the presence of germanium. In an effort to understand the mechanisms responsible for the oxidation of SiGe layers many studies have focused on the structural and electronic properties of the Ge-rich Si layer beneath the overlying oxide [3-6]. Here we concentrate on the point defects in the oxide film grown on MBE SiGe layers.

Several types of Ge related defects have been investigated through electron paramagnetic resonance (EPR) studies of irradiated Ge-doped silica optical fibers [7,8]. The centers pertinent to our study are the Ge-E' center and the Ge(1) and Ge(2) centers. The first is an unpaired electron on a Ge atom back-bonded to three oxygen atoms and is thought to be positively charged. Both Ge(1) and Ge(2) are thought to consist of an electron trapped at a Ge atom bonded to four oxygen atoms. The difference between Ge(1) and Ge(2), according to the model, is the type of second nearest neighbors belonging to the germanium atom. The former has four Si second nearest neighbors and the latter three Si and one Ge.

Recent work of Prokes and co-workers shows that a center similar to that observed in the SiO₂ fibers appears in irradiated

wet thermal oxides grown on SiGe layers [9]. In the work presented here, we use spectroscopic analysis and annealing studies to investigate in more detail the Ge-related defects observed in irradiated oxide films and compare the results with those obtained from Ge-doped optical fibers and GeO₂ glass.

EXPERIMENTAL DETAILS

A 400 nm thick SiGe layer was deposited by molecular beam epitaxy onto high resistivity (>1500 ohm-cm) (100) p-type Si substrates held at approximately 500° C. The concentration ratio of Ge:SiGe, determined from the energy shift in the peak locations of the SiGe Raman spectra, were 0, 0.19, 0.27, and 0.42 [10]. The MBE samples received a pyrolytic oxidation at 900° C for 1 hr. This resulted in oxide thicknesses of approximately 100, 110, 150, and 200 nm for Ge concentrations of 0, 15%, 25%, and 40%, respectively. For the EPR experiments, the samples were then cut into 1.5 X 0.23 cm² pieces.

The anneals were performed in air at temperatures between 50° and 300° C. The etching was carried out at room temperature using a 30:1 solution of deionized water and HF (49%). Thickness measurements were made using an Alpha-Step 250 automated high sensitivity profilometer. Samples were irradiated with x-rays at 3.7 krad/sec to 10 Mrad(SiO₂).

Electron Paramagnetic Resonance spectroscopy was conducted at room temperature using a Bruker-300 X-Band spectrometer, 1G modulation, and 200 μW incident power. To obtain an absolute concentration for the number of centers, the double integral of the EPR signal was compared with that obtained from weak pitch. The absolute accuracy is 50% and the relative accuracy about 20%.

RESULTS and DISCUSSION

In all the samples with the oxidized 40% Ge layers, a 10 Mrad irradiation produced the signal illustrated in figure 1a. From double numerical integration of the signal intensity, a defect density of approximately 3x10¹³ cm⁻² is calculated. Irradiation of samples with oxidized 0, 15%, and 25% Ge layers produced no new features in the EPR spectra. Under the conditions used here, this indicates that the maximum concentration of irradiation induced defects in these samples is less than 1x10¹² cm⁻².

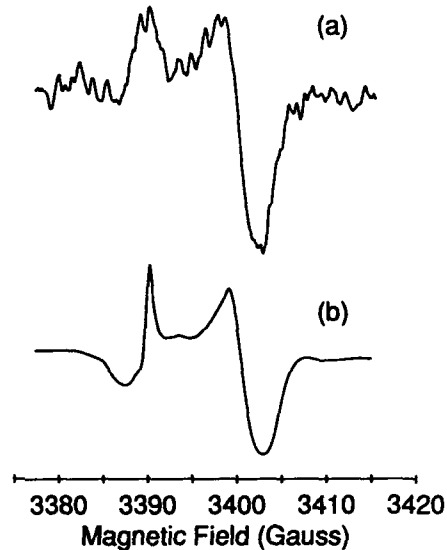


Figure 1. EPR spectrum for irradiated (a) wet thermal oxide grown on 40% Ge SiGe layer; (b) GeO₂ glass (ref. 11).

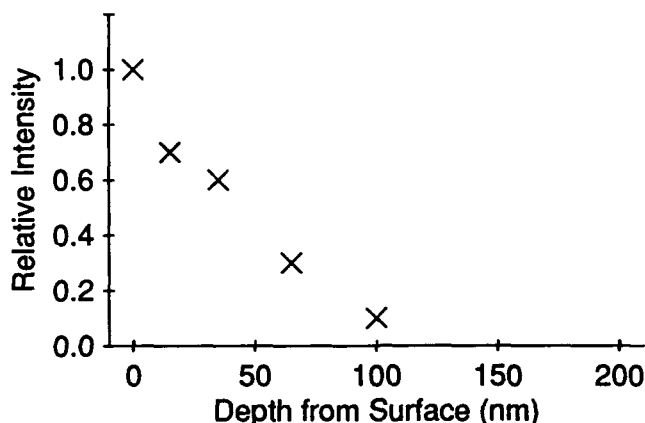


Figure 2. Depth profile for Ge E' centers in irradiated oxidized SiGe layers with 40% Ge. Oxide thickness, 200 nm.

Figure 1b shows an EPR spectrum obtained from irradiated GeO₂ glass [11]. Note the similar shape for the two spectra of figure 1, one for bulk glass (b), the other for an oxide film on SiGe (a). Both signals exhibit a width of 12G and a zero crossing at $g=1.995$. In contrast, another center typical of irradiated SiO₂, a Si E' center, is only 2.3 G wide and has a zero crossing at $g=2.001$. Other centers reported for Si/SiO₂ systems are considerably different in both shape and g value.

The location of the defect is determined from etch back experiments, the results of which are shown in figure 2. The data reveal a factor of 10 decrease in signal intensity after the first 100 nm of oxide is removed. (Measurement of a smaller signal intensity is beyond the sensitivity of the instrument.) Thus, at least 90% of the defects are located in the top 100 nm of the 200 nm oxide film.

Several features of the data presented in figures 1 and 2 support the assertion that the center observed in the oxidized 40% SiGe layers is a Ge-related oxide defect. First, the signal is observed only in the sample with the greatest amount of Ge in the substrate and, to the authors' knowledge, the center has never been observed in any other type of oxidized silicon. Second, from the depth profile of the samples, we have determined that the defect is located in the oxide layer of the SiO₂/SiGe/Si system and that the volume concentration of defects is approximately $1 \times 10^{18} \text{ cm}^{-3}$. This indicates that the minimum relative abundance of Ge in the oxide is 0.01%, a number consistent with the concentration determined by sputtering X-ray photoelectron spectroscopy (8%) and Rutherford Backscattering spectroscopy (<0.1%) of oxide films thermally grown on e-beam [3] or MBE [5] deposited SiGe layers. Finally, the EPR signal appears strikingly similar in shape and g value to a center previously assigned to Ge-related defects. From our experimental data on thin films and from the comparison with the previous work on bulk material, we conclude that the $g=1.995$ defect measured in our oxidized SiGe samples is a Ge-related oxide center.

The centers observed in irradiated optical fibers have been resolved into at least three types of defects, the Ge E' center, and Ge(1) and Ge(2) centers [7,8]. Powder pattern simulations, shown as dashed lines in fig. 3, were generated using a similar distribution of g tensors as was used by Friebele and co-workers [11]. Figure 3a shows the Ge(1) center, 3b the Ge(2) center, and 3c the Ge E' center. The solid line spectrum repeated in 3a-c represents the data obtained on an unannealed oxidized 40% Ge sample. Clearly, the Ge E' center best fits the experimental data. Further manipulation indicates that no more than 10% of the Ge(1) and Ge(2) centers may be added to the Ge E' center spectrum without significantly degrading the quality of the fit.

The annealing data of the Ge center observed in the thin films grown here and Ge-doped optical fibers studied by Friebele and Griscom are shown in figure 4 [12]. The difference in annealing temperatures between thin film (symbols) and bulk (solid line) Ge E' centers is consistent with what is observed for the Ge defect's Si analogue, the Si E' center. Reports from different groups indicate that in standardly grown wet thermal SiO₂ films irradiated under positive bias the Si E' center anneals at or below room temperature while in bulk silica there are Si E' centers which anneal at temperatures as high as 500° C [13,14]. The different annealing temperatures for the Ge E' centers is most likely related to a variation in the defect's environment as was suggested by Griscom for the Si E' center in bulk silica [14]. Based on observations of standard wet thermal oxide films [15], we suggest that hydrogen or a hydrogen-related species is responsible for the annealing behavior observed in the Ge-incorporated oxide thin films.

As was stated earlier, the concentration of Ge E' centers in the oxide is on the order of $1 \times 10^{13} \text{ cm}^{-2}$. It should be noted here that this is ten times the concentration of Si E' centers typically found in oxide films fabricated on 100% Si substrates [13]. Since, like its Si analogue, the Ge E' center is thought to be positively charged [7], this greater susceptibility towards irradiation induced defect formation should be considered if the oxide is to be used in device applications.

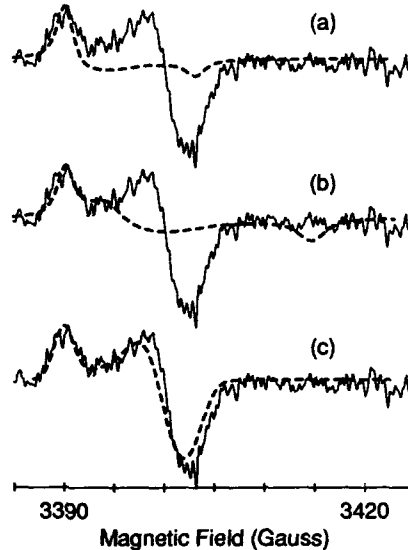


Figure 3. Ge E' center in oxidized SiGe layers (solid lines); Simulations: a. Ge(1) b. Ge(2) c. Ge E' centers (dashed lines).

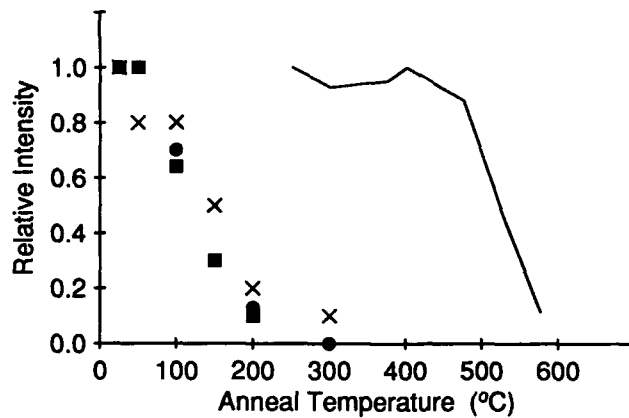


Figure 4. Annealing data for Ge E' center: symbols - oxidized SiGe layers (the different symbols refer to oxide films grown separately under nominally the same conditions); solid line - Ge doped silica (ref. 12).

In summary, we have observed irradiation-induced point defects in oxide films grown on MBE deposited SiGe layers. Based on our observation and comparisons with data obtained on the Ge-doped bulk SiO₂, we conclude that the thin film defect is a Ge E' center, an unpaired electron on a Ge atom back-bonded to three oxygen atoms.

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DISLOCATION GLIDE VELOCITY IN N- AND P-DOPED
Si_{1-x}Ge_x LAYERS ON Si(001)

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ABSTRACT

Misfit dislocation glide velocities in Si_{0.94}Ge_{0.06} layers doped to 2.10¹⁸cm⁻² with boron were measured over the temperature range 500 - 600°C and found to be up to two times slower than that of undoped material. Arsenic doped Si_{0.932}Ge_{0.068} layers on silicon were also studied, and the glide velocity was found to be enhanced by a factor of 80 at the lowest temperature (500°C) and highest doping level (9.10¹⁸cm⁻²) consistent with a decrease in the activation energy for glide from approximately 2eV to 1.3eV as the doping level was increased.

INTRODUCTION

The deposition and subsequent processing conditions for strained Si_{1-x}Ge_x layers on silicon are subject to limitations set by the nucleation and propagation of misfit dislocations. There is great interest in strained SiGe devices such as the heterojunction bipolar transistor (HBT), where maximising the Ge content gives significant performance advantages [1] but runs the risk of misfit dislocation propagation. The glide velocities of these dislocations in nominally undoped material have recently been the subject of several papers [2-4]. From previous studies undertaken with mechanical deformation of Si and Ge [5,6] it is known that doping can dramatically affect the glide velocity. Both n- and p- doping levels in the HBT are quite high (~10¹⁹cm⁻³) and so significant effects might be expected. This paper reports a preliminary investigation of doping effects in strained Si_{1-x}Ge_x on silicon.

THEORY

Dislocation glide velocities in silicon and germanium subject to mechanical deformation have been studied in detail [7]. Alexander and Haasen [7] proposed a general expression for the variation of glide velocity with temperature T and applied effective stress τ_{eff} :

$$v_{gl} = B\tau_{eff}^n \exp(-E_a/kT) \quad (1)$$

Tuppen and Gibbings [2] studied Si_{1-x}Ge_x layers on silicon and found that the propagation of 60° dislocations could be fitted to equation (1) using a value of n=1, a linear interpolation of activation energy E_a between that of Si and Ge, and a value for B that was consistent with both strained layer and mechanical deformation data:

$$E_a = 2.156 - 0.7x \quad (eV) \quad (2)$$

On a microscopic scale, dislocation glide is due to the motion of atomic scale kinks up and down the threading segment of the dislocation. This motion has the effect of displacing the dislocation in the glide direction, and the number of kinks and the speed at which they move along the dislocation therefore determine the dislocation glide velocity. One important consequence of this mechanism is that equation (1) must be modified when the strained layer thickness is comparable to the mean free path of the kinks. The effect of doping on glide velocity is also believed to be due to changes in the number of kinks and the speed at which they move [8,9].

Mechanical deformation studies of Si and Ge have shown that the addition of impurity atoms modifies the glide velocity of 60° dislocations. Neutral impurities such as nitrogen and oxygen pin the dislocations at low stresses [10], whilst at higher stresses these impurities have no effect. Electrically active dopant atoms influence the glide velocity at all stress levels, as long as the extrinsic carrier concentration at the temperature studied is greater than the intrinsic carrier concentration. N-type doping can raise the glide velocity in both Si and Ge by more than an order of magnitude [11]. A reduction in the activation energy has also been observed. Both increased and decreased glide velocities relative to undoped silicon have been reported in p-type silicon, depending on the doping level and temperature. P-type germanium has a lower glide velocity than undoped material.

Hirsch [8,9] related the effect of doping to the concentration of kinks on the dislocation. As described above, the glide velocity of the dislocation depends on the speed at which the kinks move and on their concentration, which for charged kinks is dependent on the Fermi level in the semiconductor. Negatively charged kinks are assumed to have a lower migration energy. Hirsch was able to model the velocity changes from p- or n-type doping in both Si and Ge. The dislocation energy levels used to fit the data were comparable to those obtained from Hall conductivity. The variation of glide velocity v_n with n-type doping level N_D was found to follow the equation:

$$\log (v_n/v_0) = \log N_D + C \quad (3)$$

in the extrinsic regime, where v_0 is the glide velocity in undoped material and C is a constant.

EXPERIMENTAL DETAILS

The dislocation glide velocity was measured by cleaving a 1cm square sample, damaging the alloy layer with a diamond scribe, and then annealing at the required temperature in a furnace. The leading dislocations, which are always propagating into fully strained material, would then glide from the damage at constant velocity and give rise to a well defined "front". Diluted Schimmel etch (5 parts 0.3M CrO₃: 4 parts 48% HF) was used to reveal these dislocations. This procedure was discussed in detail in a previous work [2]. It should be noted that a different annealing furnace was used in this work, which may explain why the random scatter on the data reported here is larger.

Strained Si_{1-x}Ge_x layers were grown by molecular beam epitaxy in a VG Semicon V80Si MBE system. Silicon and germanium were evaporated from Airco Temescal 156cm³ e-beam evaporators, and controlled by an Inficon Sentinel III. P-type layers were doped using either boric oxide evaporated from a conventional Knudsen cell, or using elemental boron from an EPI high temperature cell with a

pyrolytic graphite crucible. N- type doping was achieved with low energy (1000eV) arsenic ion doping. The ion beam was focussed on the centre of the wafer to give a radial distribution of doping levels across the sample. Glide velocities could then easily be measured over a wide range of As concentrations using strips cut from the centre of the wafer to the edge in $\langle 110 \rangle$ directions. The doping levels were measured using SIMS and x-ray diffractometry was used to measure the thickness and composition of the alloy layers.

RESULTS AND DISCUSSION

N-type doping

Figure 1 shows the increase in glide velocity with doping level at constant temperature in a $0.65\mu\text{m}$ thick $\text{Si}_{.932}\text{Ge}_{.068}$ alloy layer on silicon. The intrinsic carrier concentration at the anneal temperature (525°C) is indicated. At high doping levels the enhancement in glide velocity v/v_0 is proportional to N_d , as predicted by equation (3). If the full temperature dependence of the glide velocity is plotted, as in figure 2, the glide velocity of the undoped layer has an activation energy of approximately 2eV, consistent with the 2.1eV expected [2]. As the doping level is increased the activation energy decreases. The activation energy of about $1.3\text{eV} \pm 0.2\text{eV}$ at $N_D = 9 \cdot 10^{18}\text{cm}^{-3}$ is comparable to the 1.4 - 1.6eV reported for highly doped silicon [6,10,11]. In 10^{19}cm^{-3} n-type germanium a value of 1.2eV has been reported [6].

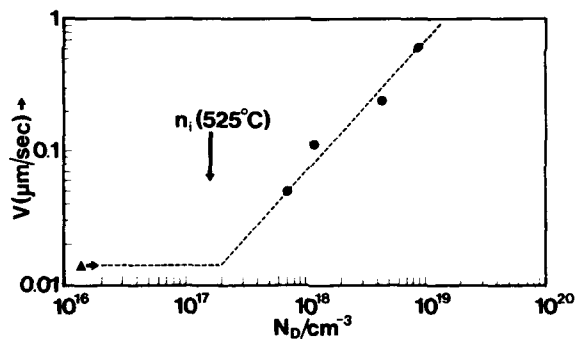


Figure 1: The variation in glide velocity with n-type doping level at an anneal temperature of 525°C . [undoped layer (\blacktriangle); doped layers (\bullet)]

P-type doping

The variation of dislocation glide velocity with p-type doping at 650°C is shown in figure 3. Three sets of data are shown - B-doped $\text{Si}_{.9}\text{Ge}_{.1}$ and $\text{Si}_{.94}\text{Ge}_{.06}$ layers and boric oxide doped $\text{Si}_{.94}\text{Ge}_{.06}$ layers. As expected, doping levels below the intrinsic carrier concentration at the anneal temperature (arrowed on the figure) do not give rise to any significant changes in velocity. In the doping range 10^{18} - 10^{19}cm^{-3} there appears to be a decrease in glide velocity, with a maximum reduction of about 30% at $2 \cdot 10^{18}\text{cm}^{-3}$. At the highest doping levels studied the glide

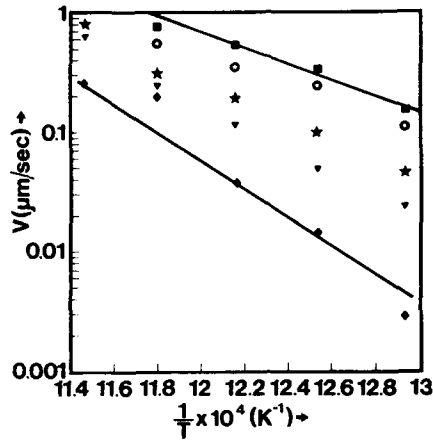


Figure 2: Temperature dependence of dislocation glide velocity in n-Si._{0.932}Ge._{0.068} on Si. [undoped layer (\blacklozenge); 7.10^{17}cm^{-3} (\blacktriangledown); $1.2.10^{18}\text{cm}^{-3}$ (*); $4.5.10^{18}\text{cm}^{-3}$ (o); 9.10^{18}cm^{-3} (\blacksquare)]

velocity increases again. Figure 4 plots $\log(\text{glide velocity})$ against inverse temperature for undoped and 2.10^{18}cm^{-3} B-doped Si._{0.94}Ge._{0.06} layers, showing activated behaviour in both cases. A least squares fit to the data gives activation energies of 2.44eV (undoped) and 2.58eV (p-doped).

As in the case of n-type doping, the SiGe alloy results can be compared to previous mechanical deformation work. The closest set of parameters to the present work is given by George and Champier [11], who reported reductions of up to 50% in p-doped silicon at 520°C, with an increase in activation energy from 2.2eV in undoped material to 2.3eV in $2.7.10^{17}\text{cm}^{-3}$ B-doped silicon. Enhancement in the glide velocity was seen above 10^{18}cm^{-3} and below 600°C [5,12]. Therefore it appears that the glide velocity variations found for p-type doped Si._{0.94}Ge._{0.06} are consistent with previous mechanical deformation work on silicon.

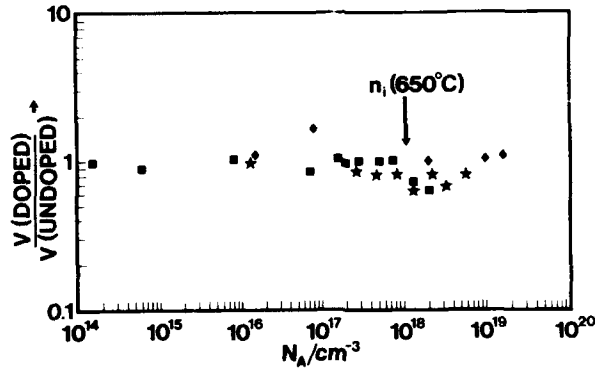


Figure 3: The variation in glide velocity with p-type doping level in $0.75\mu\text{m}$ Si_{1-x}Ge_x layers at 650°C. [B-doped Si._{0.94}Ge._{0.06} (\blacksquare); B₂O₃-doped Si._{0.94}Ge._{0.06} (\blacklozenge); B-doped Si._{0.9}Ge._{0.1} (*)]

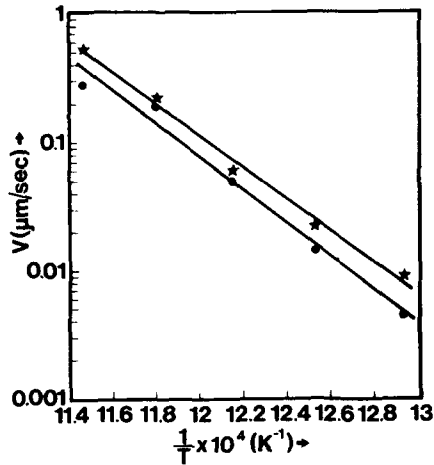


Figure 4: Temperature dependence of dislocation glide velocity in $0.75\mu\text{m Si}_{.94}\text{Ge}_{.06}$ layers on Si. [undoped layer (*); B-doped $2 \cdot 10^{18}\text{cm}^{-3}$ (●)]

Oxygen in doped layers

The availability of both boric oxide and elemental boron as dopants meant that the effect of oxygen in the layers could easily be investigated. Figure 3 compares the results obtained for both dopant sources. At a growth temperature of 550°C and a growth rate of 1nm/s , all oxygen from the boric oxide would be incorporated (i.e. oxygen level = $1.5 \times$ boron doping) [13]. No significant change in glide velocity can be attributed to oxygen incorporation. Oxygen concentrations in the range $10^{17}\text{-}10^{18}\text{cm}^{-3}$ were only found to affect the dislocation glide velocity in silicon at stresses below 20MPa [10]. As the stresses in $\text{Si}_{.94}\text{Ge}_{.06}$ layers are $>120\text{MPa}$ the alloy layer data again agree with the previous work on silicon.

CONCLUSIONS

The effects of p- and n-type doping on dislocation glide velocity in SiGe layers on Si(001) have been studied. A detailed study of p-type $\text{Si}_{.94}\text{Ge}_{.06}$ at 650°C confirmed that doping levels below the intrinsic level made no difference to the dislocation glide velocity. In the range $10^{18}\text{-}10^{19}\text{cm}^{-3}$ a decrease was seen. The temperature dependence of glide velocity in a sample doped to $2 \cdot 10^{18}\text{cm}^{-3}$ had a slightly higher activation energy than undoped alloy, with a maximum reduction of 50% in speed. At the highest doping levels studied the glide velocity was increasing with increasing doping level. These effects are consistent with results on silicon.

Low energy ion doping was used to obtain a wide range of As doping levels across a SiGe alloy layer deposited on the same silicon substrate. N-type $\text{Si}_{.932}\text{Ge}_{.068}$ layers showed large increases in glide velocity over undoped material, consistent with previous work on silicon. The activation energy at the highest

doping level ($\sim 1.3\text{eV} \pm 0.2\text{eV}$ at 9.10^{18}cm^{-3}) was close to values reported in highly doped silicon.

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STRAIN-FREE $\text{Ge}_x\text{Si}_{1-x}$ LAYERS WITH LOW THREADING DISLOCATION
DENSITIES GROWN ON Si SUBSTRATES

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ABSTRACT

We have grown linearly compositionally graded $\text{Ge}_x\text{Si}_{1-x}$ structures at high temperatures (700-900°C) on Si substrates to form a surface which resembles a $\text{Ge}_x\text{Si}_{1-x}$ substrate. We have obtained completely relaxed structures with $x \leq 0.50$ and threading dislocation densities in the 10^5 cm^{-2} - 10^6 cm^{-2} range. Because of the very low threading dislocation densities, the structures appear dislocation free in conventional transmission electron microscopy (TEM) cross-section and plan view. Employing the electron beam induced current technique (EBIC), we were able to consistently measure these low threading dislocation densities. A direct comparison of two $x=0.35$ films, one graded in Ge content and one uniform in Ge content, shows that compositional grading decreases the dislocation density by a factor of 100-1000. These higher quality graded buffers have been used as templates for the subsequent growth of InGaP light emitting diodes (LED) and $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ two-dimensional electron gas (2DEG) structures. Room temperature operation of orange-red LEDs were obtained at current densities of $\approx 600 \text{ A/cm}^2$, and mobilities as high as $96,000 \text{ cm}^2/\text{V-s}$ were achieved at 4.2K in the 2DEG structures.

INTRODUCTION

Much of the research in the mismatched epitaxy field has been concentrated on the boundary between dislocated and strained mismatched epilayers. This interest has been derived from a few applications which require nearly totally strained epilayers, such as mismatched III-V high electron mobility transistors (HEMTs)[1] and heterojunction bipolar transistors in both the III-V[2] and GeSi/Si materials systems.[3] Examples of these devices have been demonstrated, but all are limited by the physical constraint of critical thickness and critical strain, i.e. the thickness or strain at which it is energetically feasible to introduce strain-relieving dislocations.[4,5]

The introduction of dislocations into the crystal structure is deleterious to device performance, usually because either the misfit dislocations themselves lie in an interface of critical importance in the device, or the termination of the misfit dislocations at the surface, termed threading dislocations, penetrate device layers purposely located a far distance from the mismatched interface.[6]

Because the limits of Si technology are on the horizon, means to increase the functionality of Si technology through hybrid materials is a critical long term research interest. Most of these hybrid materials advances involve the integration of reliable, proven devices with core Si technology. Two natural areas of interests are high speed electronic and optical components which can be integrated with Si. However, most of the materials of interest have larger lattice constants than Si. Because the materials to be integrated need a strain-free environment, an adjustable larger lattice constant on Si must be produced, but the material must have a low defect density.

One such material which can provide an adjustable large lattice constant on Si is the $\text{Ge}_x\text{Si}_{1-x}$ alloy system. In this paper, we describe methods to produce a lattice constant of choice between Ge and Si with a reasonably low threading dislocation density.

EXPERIMENTAL PROCEDURE

Previous experiments with substrate patterning have shown that despite high temperature growth (900°C) of low mismatched (<1% strain) $\text{Ge}_x\text{Si}_{1-x}$ on Si, dislocation nucleation was not rampant, i.e. dislocations were observed to nucleate at relatively few inhomogeneities.[7] In-plane misfit dislocation lengths were on the scale of millimeters, and dislocation velocities are very high at these temperatures.[8] Thus, dislocation nucleation is the limiting factor during strain relief in low misfit systems at high temperatures. It has also been shown that undamaged $\text{Ge}_x\text{Si}_{1-x}$ /Si heterostructures only approach complete relaxation at high temperatures ($\geq 800^\circ\text{C}$).[9,10] Thus, since the threading dislocation density is directly proportional to the number of dislocation nucleation events, high temperatures and low strain encourage long misfit dislocations and low threading dislocation density.

In principle, then, by grading a $\text{Ge}_x\text{Si}_{1-x}$ at a slow rate (i.e. low Ge% per unit thickness) at high temperature, one should be able to reach any desired lattice constant with low threading dislocation density.

We have grown such layers with both rapid thermal chemical vapor deposition (RTCVD) and molecular beam epitaxy (MBE). All layers reported here were graded at 10%Ge/ μm , and growth on Si was initiated at 900°C. When the desired Ge concentration was achieved, grading was ceased and a uniform $\text{Ge}_x\text{Si}_{1-x}$ cap was deposited, usually including a p-n junction near the surface for electron beam induced current analysis (EBIC).

RESULTS

Fig. 1 is a cross-sectional TEM (XTEM) micrograph of the top of a $\text{Ge}_x\text{Si}_{1-x}$ linearly graded structure grown with RTCVD, graded to 53% Ge. Triple-crystal x-ray diffraction shows that the structure is completely relaxed. We can immediately get a sense of the misfit dislocation length by noting that the many misfit dislocations buried in the graded region are quite extended in the growth plane, despite the small field of view achieved with XTEM samples. Also note that no dislocations are observed to thread to the surface. It is well known that the sensitivity of XTEM is only in the $10^8 - 10^9 \text{ cm}^{-2}$ range. Therefore, to determine this relatively low threading dislocation density, we have employed the EBIC technique.

Fig. 2 is a plan-view EBIC image of a graded MBE structure grown to 50% Ge, and capped with a 1.5 μm -thick layer containing a p-n junction. We can observe low threading dislocation densities with great confidence and investigate the influence of grading rate and temperature.[11] The threading dislocation density in this sample is $3 \pm 2 \times 10^6 \text{ cm}^{-2}$.

To properly investigate the influence of the graded layer, we have grown by MBE an abrupt, 4.5 μm -thick $\text{Ge}_{0.32}\text{Si}_{0.68}$ layer on Si, and a graded 3.5 μm -thick $\text{Ge}_{0.32}\text{Si}_{0.68}$ layer with a 1 μm -thick cap layer. The graded layer was grown at 900°C, and the RHEED pattern indicated two-dimensional growth throughout. Complete relaxation was confirmed with triple-crystal x-ray diffraction. However, with the control sample, we found it necessary to initiate the $\text{Ge}_{0.32}\text{Si}_{0.68}$ uniform layer growth at 550°C instead of 900°C to avoid three-dimensional nucleation. After a few thousand angstroms of growth, the temperature was raised to 900°C to completely relax the layer, and growth was continued at 900°, again preserving the two-dimensional growth throughout.

Fig. 3 is a comparison of the two structures with EBIC. Fig. 3(a) is the graded structure, and a dislocation density of $1.7 \times 10^6 \text{ cm}^{-2} \pm 1.5 \times 10^5 \text{ cm}^{-2}$ is present in the cap layer. However, the uniform layer shown in Fig. 3(b) has such a high dislocation density that EBIC can not resolve the individual threading dislocations in many regions. Plan-view TEM shows that the average threading dislocation density in this sample was $\text{mid-}10^8 \text{ cm}^{-2}$. 'Dislocation annihilation' did not reduce the density to that of the graded buffer, even though the uniform



Figure 1: XTEM image of a graded $\text{Ge}_x\text{Si}_{1-x}$ layer on Si, graded to $x=0.50$ at the sample surface.

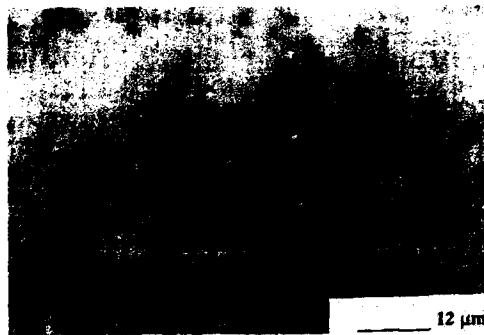


Figure 2: Plan-view EBIC image revealing a threading dislocation density of $\approx 3 \times 10^6 \text{ cm}^{-2}$ in a MBE-grown structure, graded to $x=0.53$.

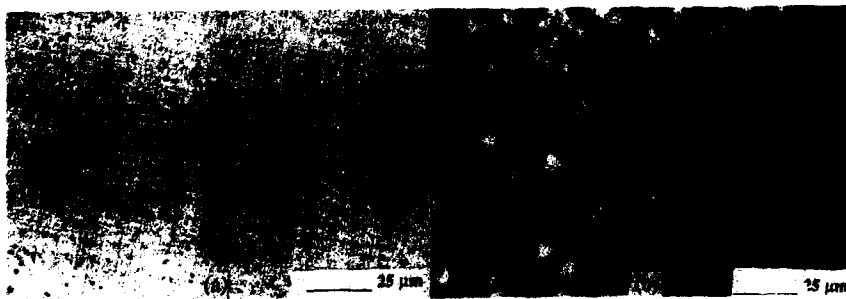


Figure 3: (a) EBIC image of a graded $\text{Ge}_{0.32}\text{Si}_{0.68}$ structure showing a dislocation density of $1.7 \times 10^6 \text{ cm}^{-2}$; (b) EBIC images of a uniform $\text{Ge}_{0.32}\text{Si}_{0.68}$ structure showing a dislocation density too high for EBIC resolution. TEM reveals an average dislocation density in this sample of $5 \times 10^8 \text{ cm}^{-2}$.

layer thickness was $4.5\mu\text{m}$. Note also that the dislocation density in Fig. 3(b) is so high that the dislocations are arranged in a cell-structure.

In principle, the threading dislocation density in any of these graded structures, regardless of Ge concentration, should not increase with thickness (and therefore with Ge concentration) since the threading dislocations, which have glided to relieve strain, can continue to glide in-plane for the remainder of the graded structure when needed. However, particulate introduction during growth and dislocation interactions may increase the threading dislocation density slowly with thickness.

As mentioned in the introduction, two areas which may benefit from such buffer layers on Si are optoelectronics and high-speed electronics. Fig. 4 is a XTEM micrograph showing a HEMT $\text{Ge}_{0.30}\text{Si}_{0.70}/\text{Si}$ structure (using Si as the channel) grown on the linearly graded buffer by MBE. The thin white layer is the Si channel, and the thicker top layer is the modulation-doped $\text{Ge}_{0.30}\text{Si}_{0.70}$ cap. The buffer has a dislocation density of $\approx 10^6\text{cm}^{-2}$, although it appears dislocation-free in TEM. This relatively low threading dislocation density limits electron scattering due to dislocations, and record electron mobilities of $96,000\text{cm}^2/\text{V}\text{-s}$ have been achieved at 4.2K . [12]

Fig. 5 shows a cathodoluminescence (CL) and electroluminescence (EL) spectra from an $\text{In}_{0.36}\text{Ga}_{0.64}\text{P}$ LED grown on a lattice-matched, totally relaxed $\text{Ge}_{0.75}\text{Si}_{0.25}$ graded layer on a Si substrate grown by MBE. The InGaP layer has a rough surface morphology due to non-optimized InGaP growth, which also contributed to an apparent phase separation into orange ($\approx 608\text{nm}$) and red ($\approx 667\text{nm}$) emitting areas. The EL spectra emits mostly in the red since the carriers recombine predominately in the smaller band gap material. These LEDs were operated at current densities as high as $600\text{A}/\text{cm}^2$. Optimization of the III-V growth should allow the fabrication of visible LEDs and lasers on Si substrates.

SUMMARY

We have demonstrated that the growth of unstrained, $\text{Ge}_x\text{Si}_{1-x}$ linearly graded structures on Si at relatively high temperatures produces low threading dislocation density $\text{Ge}_x\text{Si}_{1-x}$ layers. Lattice constants corresponding to relaxed $\text{Ge}_{0.5}\text{Si}_{0.5}$ have been reached with dislocation densities as low as $3 \times 10^6\text{cm}^{-2}$. These $\text{Ge}_x\text{Si}_{1-x}$ 'substrates' on Si have been used to produce InGaP LEDs on Si and record electron mobilities of $96,000\text{cm}^2/\text{V}\text{-s}$ in $\text{Ge}_{0.30}\text{Si}_{0.70}/\text{Si}$ modulation doped structures.



Figure 4: XTEM image of a $\text{Si}/\text{Ge}_{0.30}\text{Si}_{0.70}$ 2DEG structure grown on a graded, completely relaxed buffer. The structure achieved an electron mobility of $96,000\text{cm}^2/\text{V}\text{-s}$ at 4.2K .

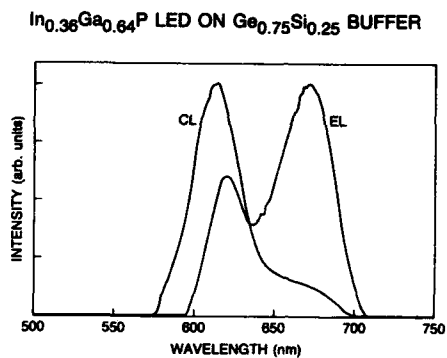


Figure 5: CL and EL spectra from $\text{In}_{0.36}\text{Ga}_{0.64}\text{P}$ LEDs grown on a relaxed, graded $\text{Ge}_{0.75}\text{Si}_{0.25}$ buffer layers on a Si substrate.

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KINETICS OF Ge SEGREGATION IN THE PRESENCE OF Sb DURING MOLECULAR BEAM EPITAXY

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Kinetics of Ge segregation during molecular beam epitaxial growth is described. It is shown that the Ge segregation is self-limited in Si epitaxial overlayers due to a high concentration effect when the Ge concentration exceeds 0.01 monolayer(ML). As a result, segregation profiles of Ge are found to decay non-exponentially in the growth direction. This unusual Ge segregation was found to be suppressed with an adlayer of strong segregant, Sb, during the kinetic MBE growth. We develop a novel scheme to realize sharp Si/Ge interfaces with strong segregants. Lower limit of the effective amount of Sb for this was found to be 0.75ML.

INTRODUCTION

Abrupt interface formation in Si/Ge heterostructures has been recognized as an central issue in realizing Si/Ge based devices of desirable properties. Surface segregation of Ge atoms during Si overlayer growth addresses a major problem against this in the case of molecular beam epitaxy (MBE). A comprehensive understanding has not been, however, reached although observations on the Ge surface segregation[1-8] are being accumulated. Recently, several groups have reported non-exponential decay profiles of Ge surface segregation in Si overlayers and a peaked temperature dependence of Ge decay length[5,7]. On the other hand, several researchers have found that the interfacial abruptness once lost due to Ge segregation can be restored by depositing an adlayer of typical dopants, such as As, Ga and Sb[4,5,8,9]. Some has claimed this is driven merely by surface free energy reduction associated with the dopant segregation. However, no detailed studies on the operative mechanism

have been conducted and the feasibility of superlattice formation has not been tested.

In this study, we investigated the role of surface bond geometry and interaction between segregants which drastically influence the atomic segregation. We developed a novel scheme to atomistically describe the Ge segregation during Si MBE. It was further shown that, during kinetic growth like MBE, the interfacial abruptness restoration in Si/Ge heterostructures with an adlayer of strong segregants is driven by overwhelming segregation of the segregants compared to Ge atoms.

Ge SEGREGATION

Characteristic segregation profiles of Ge atoms are shown Fig.1. Profiles were recorded by a secondary ion mass spectrometer (SIMS)(ATOMIKA 6500), in a 90nm thick Si overlayer for Ge concentration ($n(\text{Ge})$) of 0.01, 0.1 and 1 monolayer(ML). Obviously, the Ge profile in the growth direction bears a kink

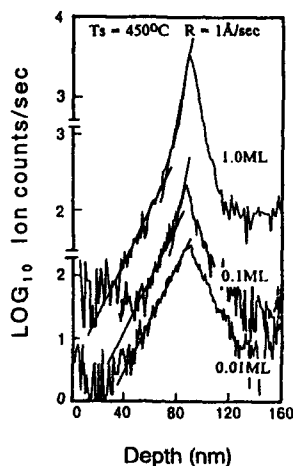


FIG. 1. Segregation profiles of Ge atoms in a 90nm thick Si overlayer. Ge profiles are kinked with extended heels for $n(\text{Ge}) > 0.1\text{ML}$.

when $n(\text{Ge})$ exceeds 0.1ML. It consists of two exponential profiles in the initial decay and at the heel. This is considered to be a consequence of high concentration effect of Ge atoms. Figure 2(a) illustrates possible exchange processes between surface and subsurface atoms on a Si(100) surface, where open and closed circles represent Ge and Si atoms, respectively. Atomic exchange is allowed within the framework of the two-state-exchange scheme[10-14] as in Fig.2(b). It is easily seen that the Ge segregation is retarded when the subsurface Ge atom (n_1) is interchanged with a surface Ge atom (n_2). The Ge segregation occurs only by the interchange of the subsurface Ge with a surface Si atom.

Following rate equations taking account

of the second-order kinetics are hence derived for the description of Ge exchange between the two states[15],

$$dn_1/dt = -2 p n_1(1-n_2) + 2 q n_2(1-n_1), \quad (1)$$

$$dn_2/dt = -2 q n_2(1-n_1) + 2 p n_1(1-n_2). \quad (2)$$

An important feature is that the multiplier $(1-n_2)$ ($(1-n_1)$) appears, though absent in the previous formalism[12], which represents the self-limiting process arising from the presence of over(under)lying Ge atoms in the way up(down). Ge segregation profile is

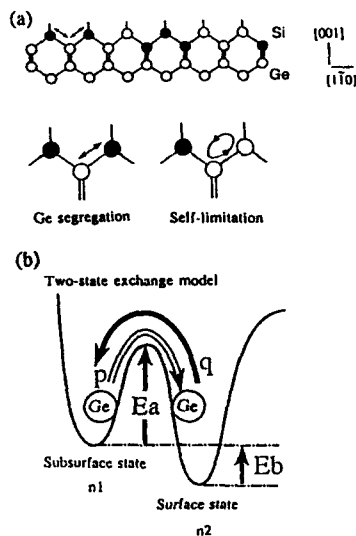


FIG. 2 (a) Possible atomic exchange between subsurface and surface Ge atoms on Si(100); Ge surface-segregates upon exchange of the subsurface Ge with the surface Si(left); Ge segregation is retarded when the subsurface Ge atom is replaced by the surface Ge instead of Si (self-limitation)(left). (b) Energy diagram in the two-state-exchange scheme.

calculated by integrating Eqs. (1) and (2) over a growth period $t_m = (a_0/4)/R$, where a_0 and R are the lattice constant of Si and growth rate, respectively. Note that $p = f_0 \exp(-E_a/kT)$ and $q = f_0 \exp(-(E_a + E_b)/kT)$ represent jumping rates for Ge atoms toward the surface and back into the subsurface, where E_a and E_b are the kinetic barrier and the Gibbsian heat of segregation, respectively. E_b and E_a have been determined from high temperature behavior of the Ge decay length of Ref. 7 to be 0.28 ± 0.1 eV and from the decay length of the heel in the SIMS profile to be 1.63 ± 0.1 eV, respectively [15]. The trial frequency f_0 is taken to be comparable to the Debye frequency, $5 \times 10^{12}/\text{sec}$ [12]. Thermal desorption of the Ge atoms is neglected. For simplicity, we also neglected the influence of surface reconstructions, steps and lattice strain. A boundary condition of the calculation is the conservation of Ge atoms in a single layer growth,

$$n_1 + n_2 = n_0, \quad (3)$$

where n_0 is the initial amount of Ge in the surface state.

Figure 3 shows the calculated profile taking account of the self-limitation (solid curve) along with the profile obtained by a conventional kinetic theory (dotted line). The parameters are $n(\text{Ge}) = 1 \text{ ML}$, $T_s = 380^\circ\text{C}$ and $R = 1 \text{ \AA}/\text{sec}$. Obviously, the heeled Ge profiles in Fig. 1 and in Ref. 5 are reconciled only with the self-limited calculation. The initial decay is strongly self-limited, which renders the interface atomically sharp. In contrast, conventional theory merely gives a simple exponential decay with a decay length $\lambda^* = 75 \text{ \AA}$. The self-limitation becomes pronounced for $n(\text{Ge}) > 0.01 \text{ ML}$. A quantitative agreement was

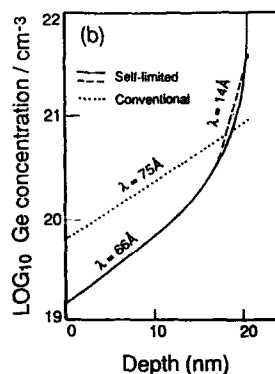


FIG. 3 Calculated incorporation profile of Ge atoms in Si overlayer (solid curve). For comparison, the exponential decay profile obtained by a conventional kinetic theory (dotted line) is also shown. The initial decay in the self-limited calculation (broken line) has been obtained taking account of the stochastic averaging due to ion sputtering.

obtained by considering the stochastic mixing in the first 3.5 nm in the SIMS profile. The kink concentration and λ at the heel of the profile are $4 \times 10^{20} \text{ cm}^{-3}$, 61 \AA in the experiment and $3 \times 10^{20} \text{ cm}^{-3}$, 66 \AA in the calculation, respectively.

SEGREGANT-ASSISTED GROWTH (SAG)

We previously demonstrated a method in which the Ge segregation is effectively suppressed with an adlayer of Sb over Ge atoms prior to Si overgrowth [8]. Sb is known to be a strong segregant and floats up the surface during Si and Ge overgrowth [16]. On the other

hand, Ge segregation is retarded as a consequence of the self-limitation and weak in strength compared to Sb. At typical growth temperatures, 350-600°C, of Si/Ge strained-layers, Sb segregation overwhelms that of Ge, resulting in the formation of abrupt Si/Ge interfaces. Hereafter we call this method as segregant-assisted growth (SAG).

One drawback of SAG method is that Sb incorporation in Si cannot be eliminated. This is derived from the thermodynamics of the two-state exchange. The Sb incorporation in Si becomes pronounced when the Sb segregation is kinetically-limited. As is known, the MBE growth is kinetically controlled by the growth rate at a fixed temperature. With Sb incorporated and therefore consumed in the overlayer, effective suppression of the Ge segregation is reduced in the consecutive overlayer growth.

To discuss SAG theoretically, we conducted a calculation assuming the copresence of Sb and Ge in the kinetic MBE growth. Basic equations of the atomic exchanges taking account of kinetic limitations due to overlying atoms are similar to Eqs.(1) and (2). We calculated how λ of Ge changes upon Sb deposition of various concentration, $n(\text{Sb})(0.01-1.0\text{ML})$. The result is shown by solid curve in Fig.4 as normalized by λ in the absence of Sb adlayer. Solid circles are the experimental data from the samples consisting of alternate layers of 3ML Ge and 30nm-thick-Si with Sb adlayers for SAG. The growth parameters were $T_s=500^\circ\text{C}$ and $R=1\text{\AA}/\text{sec}$. A good agreement was obtained for $n(\text{Sb}) < 0.75\text{ML}$. This clearly shows that the suppression of the Ge segregation in the presence of Sb is a result of the competition between the Sb and Ge atoms in Si. Reduced λ of Ge for increased $n(\text{Sb})$ is thought to be a result of strong segregation of

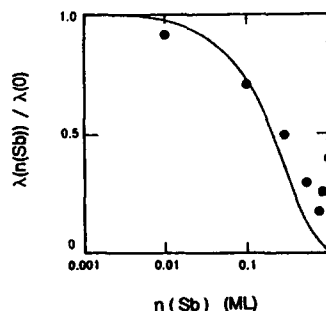


FIG. 4. Ge decay length (λ) after Sb deposition normalized by that in the absence of Sb plotted against Sb concentration. Solid curve is the calculation and the solid circles are the experimental data.

Sb in Ge layers. A slight disagreement for $n(\text{Sb})$ larger than 0.75ML suggests crystalline quality change on the surface due to excessive Sb. The details are not clarified at present.

The applicability of SAG to the Si/Ge superlattice formation was investigated using the same samples. Special attention was focused on the requisite amount of Sb for and the retention range of the suppression of the Ge segregation. To accentuate the degree of sharpness of the Ge profile, the contrast factor, C , was used. C is defined as the ratio of the difference and the sum of heights of the valley between the Ge layers and the neighboring peak in the substrate side. In terms of C , one can evaluate the change of the Ge profile at the heel associated with Sb deposition. Note that C takes unity for a truly abrupt interface. It was found that C increases monotonically with increasing $n(\text{Sb})$ and reaches unity for $n(\text{Sb})=0.75\text{ML}$. With this amount of Sb, the

interface is said to be abrupt within the SIMS spatial resolution, 3.5nm. We next examined how long the suppression of Ge segregation lasts, once the Sb adlayer is deposited. It was found that the contrast factor in SIMS profiles decays rapidly in the growth direction for Sb deposition less than 0.75ML. For $n(\text{Sb})=0.75$ and 1 ML, the suppression lasts as long as 60nm, without noticeable decay. Qualitatively the same results were obtained with respect to the profile half width and the decay length. Therefore, the amount of 0.75ML is considered to be most practical for SAG with Sb. It is noteworthy that the Sb incorporation amounts to 10^{17} - 10^{18}cm^{-3} and increases with $n(\text{Sb})$.

CONCLUSIONS

Ge segregation in Si overlayers was found to be self-limited for $n(\text{Ge}) > 0.01\text{M}$ and leads to kinked-SIMS profiles. As a result, a sharp interface is obtained for higher Ge concentration while an extended heel is observed for lower concentration. Ge segregation was found to be suppressed by segregant-assisted growth (SAG) with Sb. Lower limit of the requisite amount of Sb adlayer for both efficient suppression and retention range was found to be 0.75ML. Kinetics of Ge segregation in the presence of Sb was describable in terms of the two-state-exchange scheme taking account of second-order kinetics.

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* λ corresponds to b in Ref.8.

ELECTRON MICRODIFFRACTION INVESTIGATION OF A $\text{Ge}_x\text{Si}_{1-x}$ BUFFER FOR STRAIN-SYMMETRISED SUPERLATTICE STRUCTURES

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ABSTRACT

A candidate GeSi buffer layer structure suitable for strain-symmetrised GeSi/Si superlattice overgrowth is grown by molecular-beam epitaxy and its strain state characterised using microdiffraction in a dedicated scanning transmission electron microscope. The structure consists of five alloy layers of increasing Ge concentration grown on a Si (100) substrate, with all but the last annealed at high temperature. Analysis of higher order Laue zone deficit lines in the microdiffraction patterns acquired from each layer indicate that relaxation is complete in all the layers. Images of the structure in the transmission electron microscope show good crystallinity of the final layer with low concentrations of threading dislocations.

INTRODUCTION

The beneficial properties of pure Si wafers (excellent crystallinity, good strength and thermal conductivity together with ready availability at low cost) have made them the preferred substrates in GeSi growth. However the strain energy of any $\text{Ge}_x\text{Si}_{1-x}$ /Si superlattice grown on a pure Si substrate will increase monotonically with growth thickness, limiting the number of superlattice periods that can be grown without introducing misfit dislocations. With the short period, high Ge concentration superlattices now being investigated, a buffer of lattice parameter intermediate between Si and Ge is required to symmetrise the strain between the GeSi and Si layers. Such a buffer, grown on a Si substrate, should ideally terminate in a fully relaxed $\text{Ge}_x\text{Si}_{1-x}$ composition of perfect crystallinity.

Two factors prevent such a buffer from being readily realised. Firstly, relaxation is a continuous process: growth of a single epilayer of a thickness well above the accepted value for the strain-relaxation transition produce dislocation densities insufficient for complete plastic relaxation [1]. The equilibrium models of Van der Merwe [2] and Matthews-Blakeslee [3] give expressions for the critical thickness of growth at the onset of relaxation of a strained epilayer but a consideration of the dislocation dynamics [4] is necessary to predict the final degree of relaxation. Secondly, with every misfit segment lying at substrate-epilayer interface, two threading segments will be produced, degrading the crystallinity of the epilayer. Both factors prevent the growth of a single composition epilayer from producing a good buffer.

Previous analyses of single $\text{Ge}_x\text{Si}_{1-x}$ layers grown on a Si substrate suggested that through thermal annealing an epilayer thicker than the Matthews-Blakeslee critical thickness could be completely relaxed and furthermore, for low mismatches, the threading dislocation density minimised [5]. The candidate buffer was constructed by growing and then annealing a series of layers of increasing Ge content on a Si substrate. The relaxation state of the buffer structure was determined using microdiffraction in a dedicated scanning transmission electron microscope (STEM). This technique can give an accuracy comparable to that of X-ray diffraction (XRD) but with a spatial resolution of the order of a nanometre. Hence, unlike with XRD, the strain in each of the layers can be measured independently.

EXPERIMENTAL

The buffer structure was grown in a VG V90S molecular-beam epitaxy system. The (100) Si substrate was initially cleaned at 850°C under a Si flux to remove the native oxide before the growth of a 150nm Si layer. Subsequent layers were of the following (nominal) thicknesses and compositions: 300nm of $\text{Ge}_{0.10}\text{Si}_{0.90}$, 200nm of $\text{Ge}_{0.20}\text{Si}_{0.80}$, 200nm of $\text{Ge}_{0.28}\text{Si}_{0.72}$, 200nm of $\text{Ge}_{0.36}\text{Si}_{0.64}$ and 400nm of $\text{Ge}_{0.45}\text{Si}_{0.55}$. The substrate temperature throughout the

growth of each layer was 550°C. After the growth of all but the last alloy layer, the structure was annealed at a temperature of 850°C for 10 minutes. Specimens were prepared through cleavage, producing an electron transparent cross-section at the cleaved corner for microdiffraction analysis, and by ion-beam thinning for cross-sectional imaging.

The cleaved specimen was analysed in a VG HB501 dedicated STEM capable of producing a probe less than a nanometre in diameter at a nominal accelerating voltage of 100kV. The structure was imaged in scanning mode prior to positioning the probe on an individual layer and collecting the microdiffraction pattern. The pattern can be acquired at very high angular resolution with a recently developed energy-filtered microdiffraction technique [6]. The electrons are passed through a spectrometer and only the elastically scattered electrons selected to form the diffraction pattern. Energy filtering of the electrons greatly increases the signal-noise ratio of diffraction information in the pattern. The ion-beam thinned specimen was imaged in an ABT 002B conventional transmission electron microscope (CTEM) and energy-unfiltered convergent-beam electron diffraction (CBED) patterns recorded.

RESULTS AND ANALYSIS

Figure 1 shows a bright field cross-sectional image of the structure taken in the CTEM. Large numbers of misfit dislocations are evident at all the interfaces as well as many threading segments within the first four annealed layers. The top, unannealed $\text{Ge}_{0.45}\text{Si}_{0.55}$ layer contains a single threading segment in the field of view of the micrograph (arrowed). The average threading dislocation density, as determined from several micrographs most of which contain no such segments, is about $10^7/\text{cm}^2$.

In figures 2a, 3a, 4, 5, 6a and 7a are shown microdiffraction patterns from the [012] zone axis of the cleaved sample in the STEM with the probe positioned on the substrate and at the centre of each of the alloy layers. The patterns are slightly distorted due to the quadrupoles used to increase the camera length after the spectrometer. Only the transmitted disc is shown, crossed with deficit lines corresponding to high angle reflections in the higher order Laue zones (HOLZ). The thicker lines come from the first order Laue zone (FOLZ), the thinner lines from the second order Laue zone (SOLZ). These lines are very sensitive to both homogeneous and inhomogeneous strain fields. The effect of an inhomogeneous strain field is to split the HOLZ lines. Homogeneous strains shift the HOLZ line positions, changing the appearance of the

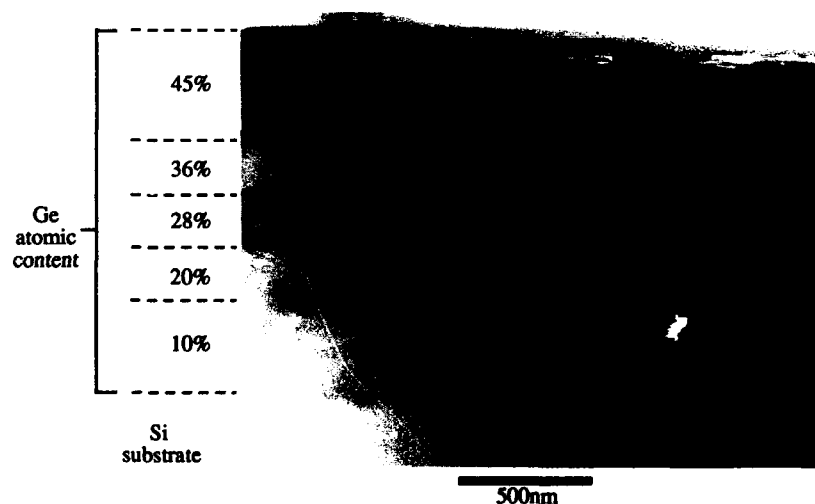


FIGURE 1: Cross-sectional CTEM bright field micrograph of the buffer structure. A segment of a threading dislocation in the $\text{Ge}_{0.45}\text{Si}_{0.55}$ layer is indicated.

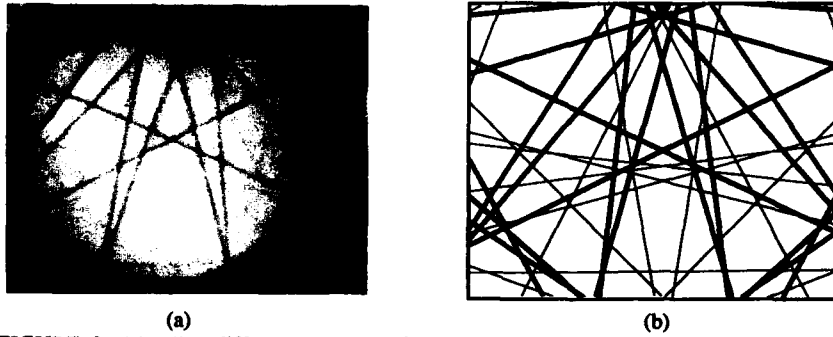


FIGURE 2: (a) Microdiffraction pattern from the Si substrate with (b) a kinematical simulation of the HOLZ line positions. The parameters for the simulation are listed in Table 1.

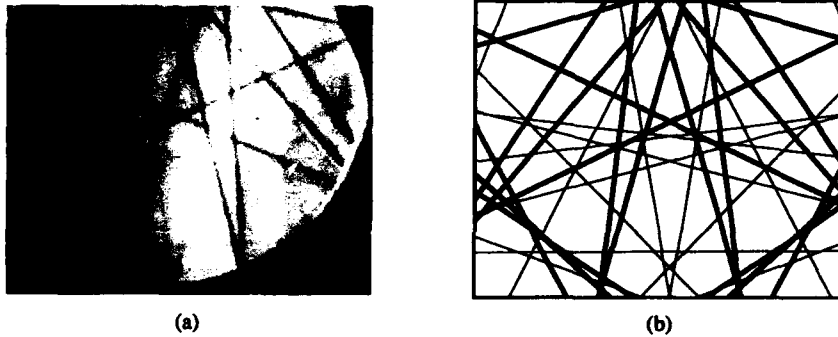


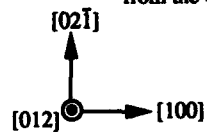
FIGURE 3: (a) Microdiffraction pattern from the $\text{Ge}_{0.10}\text{Si}_{0.90}$ layer with (b) a kinematical simulation of the HOLZ line positions. The parameters for the simulation are listed in Table 1.



FIGURE 4: Microdiffraction pattern from the $\text{Ge}_{0.20}\text{Si}_{0.80}$ layer.



FIGURE 5: Microdiffraction pattern from the $\text{Ge}_{0.20}\text{Si}_{0.72}$ layer.



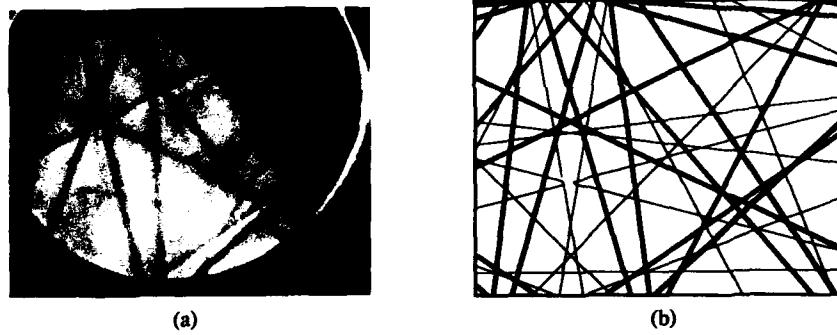


FIGURE 6: (a) Microdiffraction pattern from the $\text{Ge}_{0.36}\text{Si}_{0.64}$ layer with (b) a kinematical simulation of the HOLZ line positions. The parameters for the simulation are listed in Table 1.

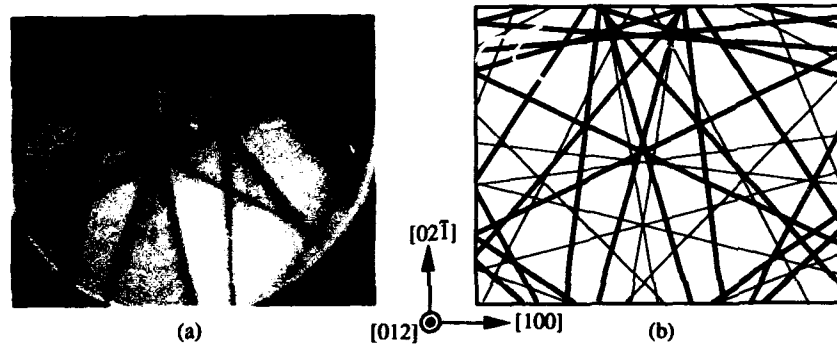


FIGURE 7: (a) Microdiffraction pattern from the $\text{Ge}_{0.45}\text{Si}_{0.55}$ layer with (b) a kinematical simulation of the HOLZ line positions. The parameters for the simulation are listed in Table 1.

diffraction pattern. Composition changes are equivalent to a hydrostatic strain whilst incomplete relaxation will be accompanied by a biaxial strain. These two types of strain field can be readily distinguished from their different effects on the HOLZ line position. The most accurate way of determining the strain from the microdiffraction patterns is through comparison with simulations computed kinematically. However the simple kinematical theory must be modified to take account of dynamical shifts of the electron dispersion surface [7]. These dynamical effects are dependent on the chemical composition of the crystal and have been computed for the dominant highest kinetic energy Bloch state in the various GeSi alloys (Table 1). Although these corrections are small, their neglect would seriously degrade the accuracy of simulations. The Si substrate pattern is used through matching to the simulation (figure 2b) to determine the exact accelerating voltage of the microscope assuming a Si lattice parameter of 0.5431 nm. The corresponding electron wave number, corrected for the dynamical effects on the FOLZ and SOLZ lines separately, is then used for simulating the HOLZ line patterns in the alloy layers.

TABLE 1: Parameters used in HOLZ line simulations. $\epsilon^{(1)}$ is the computed shift of the dispersion surface of the first Bloch wave from the kinematical value. * indicates the parameter determined from the simulation.

Nominal Ge content / at%	$\epsilon^{(1)} / \text{nm}^{-1}$	Accelerating voltage / kV	Lattice constant / nm	Inferred Ge content / at%
0	0.0021	96.30±0.05*	0.5431	0
10	0.0027	96.30	0.5450±0.0005*	8±2*
36	0.0035	96.30	0.5505±0.0005*	35±2*
45	0.0051	96.30	0.5530±0.0005*	44±2*

The microdiffraction patterns from the alloy layers all contain split HOLZ lines indicating the presence of inhomogeneous strain fields from dislocations. In particular, patterns from the second and third layers show gross splitting of the HOLZ lines, preventing an accurate determination of the homogeneous strain field. The overall shift of the patterns from the second, third and fourth alloy layers is due to a rigid body rotation of the lattices from the underlying substrate. It would appear that the alloy lattices have locally rotated to help accommodate the misfit. The fifth alloy layer is almost perfectly aligned to the substrate. The small discrepancy is probably due to small electronic shifts of the incident beam direction used to accurately position the beam on the sample.

The best fitting simulations for the first, fourth and fifth alloy layers are shown beside the experimental patterns. All correspond to a strain free state with lattice constants corresponding to Ge compositions just below the nominal values (Table 1). The compositions are in good agreement with recalibration of the molecular-beam fluxes subsequent to growth. It would thus appear that the alloy layers have, as desired, completely relaxed back to their bulk lattice parameters. However such relaxation could be due to surface relaxation of the wedge corner, although such relaxation should be associated with considerable inhomogeneous strains [8] and HOLZ line splitting. The minimal splitting seen in the patterns from the first, fourth and fifth layers suggests that relaxation at the wedge corner is unlikely. In order to further discount the presence of surface relaxation, CBED patterns were acquired from the ion-beam thinned sample with the accelerating voltage of the CTEM adjusted to the value determined for the STEM. CBED differs from microdiffraction only in the size of probe (several tens of nanometres in diameter) used. The thin foil geometry of the ion-beam thinned sample permits relaxation of any residual strain only in the foil surface normal direction. Hence any discrepancy between the microdiffraction and CBED patterns indicates the presence of residual strain. No such discrepancy was observed and so plastic rather than surface relaxation is the dominant energy-minimisation mode in these samples.

CONCLUSIONS

Layer-by-layer analysis of this candidate buffer structure by electron microdiffraction indicates that each alloy layer has completely relaxed. The good crystalline quality of the top layer, as deduced from the cross-sectional TEM micrographs, suggests that such a structure could provide a suitable template for subsequent strain-symmetrised growth.

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X-RAY STUDY OF NON-PERIODIC Si/SiGe MULTILAYERS

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ABSTRACT

X-ray diffraction is applied for the assessment of structural data such as lattice mismatch and layer thickness of MBE grown Si/Si_{1-x}Ge_x heterobipolar transistor and double-barrier resonant-tunneling structures. Rocking curves from the former structure show distinct features which are obviously correlated to the individual layer parameters. The diffraction profile of the resonant tunneling structure is not only more complicated because of the larger number of parameters but also due to the strong interference effects resulting from the layer set-up. For a determination of the structural parameters a comparison of the experimental diffraction pattern with simulated rocking curves is performed.

INTRODUCTION

The heterosystem SiGe on Si substrates is presently of broad interest both in scientific view and beyond that for device applications. By using suited growth techniques, as Si molecular beam epitaxy (MBE), various SiGe heterostructures on Si substrates have successfully been prepared with good crystal quality ranging from single Si_{1-x}Ge_x layers to Si_{1-x}Ge_x strained layer superlattices (n and m denote the number of monolayers)[1]. Among the structural characterization methods Bragg-case double crystal X-ray diffraction is a widely used and non-destructive technique for measurement of lattice mismatch and elastic strain in heteroepitaxial layers on thick substrates. With single layers the lattice mismatch and the degree of relaxation can be relatively easily and fast deduced from the angular peak separation in X-ray rocking curves (XRC)[2]. Moreover, the thickness of a layer having good crystal quality can be derived from the Pendellösung fringes surrounding the main layer peak. On the other hand, period length and average strain in high quality strained layer superlattices (SLS) can be assessed without major effort from the superlattice related diffraction peaks [3]. However, if the XRC of a single layer with small thickness and/or lattice mismatch is analyzed a peak shifting caused by interference effects must be taken into account [4,5]. Moreover, if a non-periodic multilayer structure is considered the diffraction profiles generally show a complex line pattern and simple analysis is no longer applicable [6-11]. The only way to interpret such profiles is by elaborate simulation.

The present study deals with X-ray analysis of two device related non-periodic SiGe/Si multilayers which are pseudomorphically grown by Si MBE on (100) oriented Si substrates: The first structure is a heterobipolar transistor (HBT) structure consisting of two submicron Si layers (collector and emitter) with a thin Si_{1-x}Ge_x layer (base) in between. The other is a double-barrier resonant tunneling (DBRT) structure for hole tunneling with six individual layers where the essential resonant tunneling feature consists of a thin Si_{1-x}Ge_x well for holes confined by two Si barriers [12].

The layer parameters of the samples have been extracted by a fit of computer simulations to the experimental rocking curves. We used a computer simulation program based on the dynamical X-ray diffraction theory, which is commercially available from Bede Scientific Ltd., Durham, Great Britain.

EXPERIMENT

The HBT structures are grown on (100) oriented 3" Si standard substrates. The Si MBE apparatus described in Ref. [13] has been extended by a Ge effusion cell for heterostructure growth and a B cell [14] for p type doping. A typical HBT structure consists of a ≈ 300 nm thick Si collector layer ($3 \times 10^{16}/\text{cm}^3$, Sb doped), a 50-80 nm $\text{Si}_{1-x}\text{Ge}_x$ base layer (10^{18} - $10^{20}/\text{cm}^3$ B doped, $x = 20$ -30 %) and ≈ 300 nm thick emitter layer ($\approx 10^{18}/\text{cm}^3$ Sb). The DBRT samples are prepared on (100) oriented 4" Si standard wafers (p⁺ type) in an Atomika Si MBE machine described elsewhere [15]. The six layers of a tunneling structure are as follows (see insert in Fig. 3): Two typically 5 nm thick Si barriers with a ≈ 3 nm thick $\text{Si}_{0.8}\text{Ge}_{0.2}$ well in between are embedded in ≈ 30 nm thick $\text{Si}_{0.8}\text{Ge}_{0.2}$ cladding layers. Well, barriers and cladding layers are undoped. The structure is capped by a p⁺ type Si contact layer. The XRC were recorded with $\text{Cu}\alpha$ radiation in the symmetric (+,-) configuration using a Si (100) crystal in (004) reflection as monochromator.

RESULTS

HBT structure

The experimental and calculated XRC from an HBT structure are shown in Fig. 1a and 1b, respectively. There are three distinct features in the diffraction pattern which have a distinct relation to the structural data. The angular

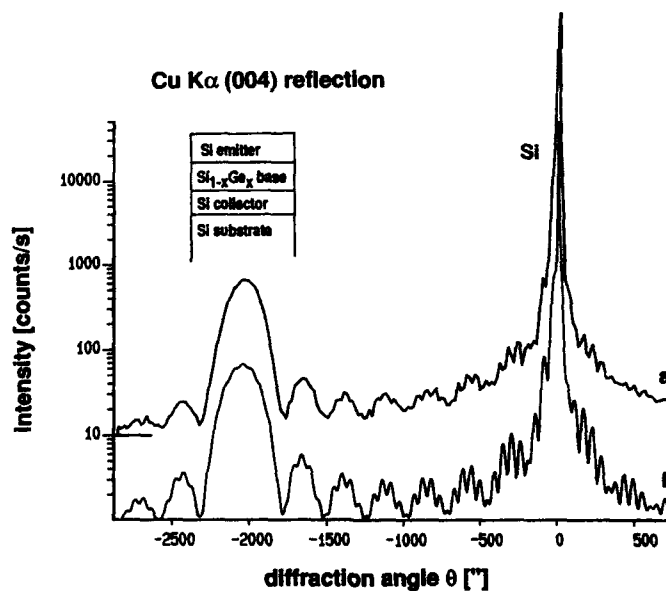


Fig. 1: Experiment (a) and calculated (b) diffraction pattern of an HBT structure. The insert shows the schematic layer set-up. The parameter for the simulation are: Ge content x in the base 22 %, base thickness 72.5 nm, and emitter thickness 295 nm. For clarity, curve (a) is shifted upward.

position of the main SiGe peak is determined by the lattice mismatch of the base layer to the Si substrate. For a conversion of the lattice mismatch into the desired Ge content X the deviation of the Si/Ge system from Vegard's Law is taken into account [16]. A parabolic relation between the lattice mismatch $f(\text{Si}_{1-x}\text{Ge}_x/\text{Si})$ and the chemical composition x well resembling the experimental data reads: $f(\text{Si}_{1-x}\text{Ge}_x/\text{Si}) = 0.00501 x^2 + 0.03675 x$. The subsidiary fringes around the $\text{Si}_{1-x}\text{Ge}_x$ peak are correlated with the thickness of the base, whereas the short period oscillation around the Si position is due to the thickness of the emitter. Thus a step by step fit in a straight manner can be undertaken because the variation of one parameter changes only the corresponding diffraction features. A nearly perfect agreement between experiment and calculation is achieved with a base thickness and Ge content of 72,5 nm and 22 % respectively, and an emitter thickness of 295 nm. The full width at half maximum of the diffraction lines agree well with that of the simulation indicating good crystal quality of the layers. The collector layer is not detectable because there is no X-ray relevant interface between the Si substrate and the Si collector layer.

Admittedly, for this HBT structure an approximation by kinematical diffraction would be sufficient because the different diffraction features are well separated and interference effects will not play an important role. However, the infinitely thick substrate cannot be simulated by a kinematical approach. We could overcome this problem by theoretically replacing the substrate by a $\approx 10 \mu\text{m}$ thick Si layer but at the cost of closely spaced subsidiary interference maxima that would disturb the Pendellösung oscillations of the emitter layer. The lattice mismatch of the $\approx 10^{18}/\text{cm}^3$ Sb doped emitter layer to the Si substrate is with $\approx 10^{-6}$ [17]) too small to produce any detectable shift towards smaller diffraction angles. If a lattice contraction coefficient of $5 \times 10^{-24} \text{cm}^3/\text{atom}$ [18] for the $2 \times 10^{19}/\text{cm}^3$ boron doped base is taken into account the Ge content is to be corrected from 22 % to 22.25 %.

DBRT structure

The X-ray diffraction from a quantum well structure typically consisting of two cladding layers of the same crystalline material and thickness separated by a thin well layer with different interplanar spacing have been studied and analyzed by different authors [6-11 and references therein]. In XRC from such structures interference effects between the diffracted waves from the two cladding layers play a crucial role. One obtains a rather complex pattern of the diffracted peaks which contain informations on the thickness of the separating well with a sensitivity on a nm or even an Å scale. In the DBRT structure the thin SiGe well is even inserted into the Si which separates the two SiGe claddings. The interference contribution resulting from this further layer makes the diffraction pattern more complicated and more difficult to interpret. Assuming coherent growth the DBRT sample consists of six layers with nine independent structural quantities, in the most general case. In order to reduce the numbers of parameters we assume (i) that the Ge content x of the three $\text{Si}_{1-x}\text{Ge}_x$ layers is constant and equal, and (ii) that both Si barriers and both $\text{Si}_{1-x}\text{Ge}_x$ claddings have the same thickness t_b and t_{cl} , respectively, leaving x , t_{cl} , t_b , t_w and t_c as independent parameters. With exception of the Si cap layer which induces only thickness fringes around the Si Bragg position, a variation of one of the residual thickness parameters influences the whole diffraction pattern in a non-straightforward manner due to interference effects. In Fig. 2a-2d the calculated diffraction profiles demonstrate the response of the X-ray diffraction if the well thickness t_w within the two Si barriers is increased from 0 to 6 nm in 2 nm steps. The Si cap layer is omitted in this calculation. The other parameters are kept constant with $x = 20 \%$, $t_{cl} = 25 \text{ nm}$, and $t_b = 5 \text{ nm}$. Apart from the substrate the only feature which remains unchanged is the peak at -1800 arcsec , whereas the other lines are modulated in intensity and shifted in their angular position. For comparison, the XRC from a 25 nm

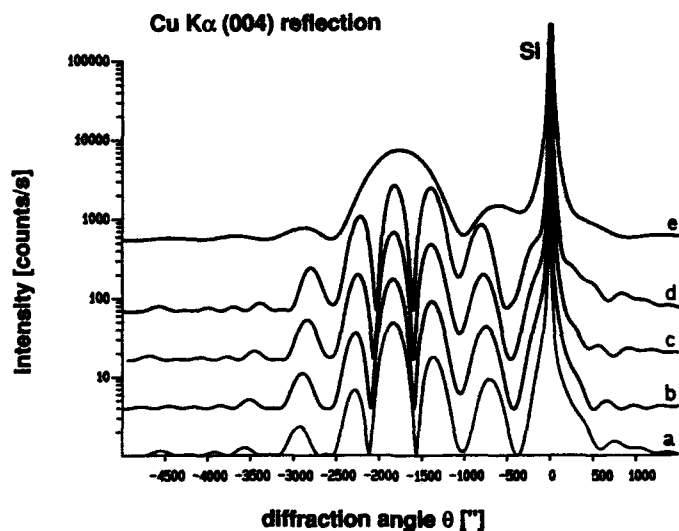


Fig. 2: The calculated curves (a)-(d) demonstrate the influence of the well thickness t_w on the diffraction pattern of a DBRT structure (layer set-up: see insert in Fig. 3). (a): $t_w = 0$, (b): $t_w = 2$ nm, (c): $t_w = 4$ nm, (d): $t_w = 6$ nm. The other parameters are held constant: $x = 20$ %, $t_{cl} = 25$ nm, $t_b = 5$ nm. The Si cap is omitted. For comparison, curve (e) is the calculated XCR of a 25 nm thick $\text{Si}_{0.8}\text{Ge}_{0.2}$ alloy layer which envelopes the curves (a)-(d). For clarity, the curves (b)-(e) are shifted upward.

thick single $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer is also displayed in Fig. 2e. This curve acts as an envelope for the curves a-d which means that the diffraction pattern shifts as a whole if the Ge content x is changed. Hence the x value is the only parameter the influence of which on the diffraction pattern is comparatively evident. In Fig. 3a the experimental XRC from a DBRT structure is shown with the following nominal data: Two $\text{Si}_{0.75}\text{Ge}_{0.25}$ claddings with $t_{cl} = 30$ nm, two Si barriers 5 nm thick, a 3 nm $\text{Si}_{0.75}\text{Ge}_{0.25}$ well, and a Si cap layer with $t_c = 200$ nm. Before starting the simulation a Ge content $x = 16$ -18 % (assumed to be constant and equal for all three SiGe layers) has been estimated from a graphically approximated envelope. Then following trial and error a reasonable fit to the experimental XRC both in intensity and line position can be achieved with $x = 17$ %, $t_{cl} = 28$ nm, $t_b = 5.5$ nm, $t_w = 3.5$ nm, and $t_c = 205$ nm.

We note that the structural characterization may suffer from the necessity to reduce the number of parameters in order to limit the simulation effort. The assumptions made are based on the growth procedure in which a constant x and equal thicknesses of the claddings and the barriers, respectively, were intended.

An additional line occurs in the particular sample in Fig. 3 which is due to a highly B doped chemical vapour deposition layer co-doped with Ge for strain compensation. The peak close to the Si line towards higher diffraction angles stems from this layer indicating that the strain is not fully compensated but there is a residue strain of some 10^{-4} in this layer.

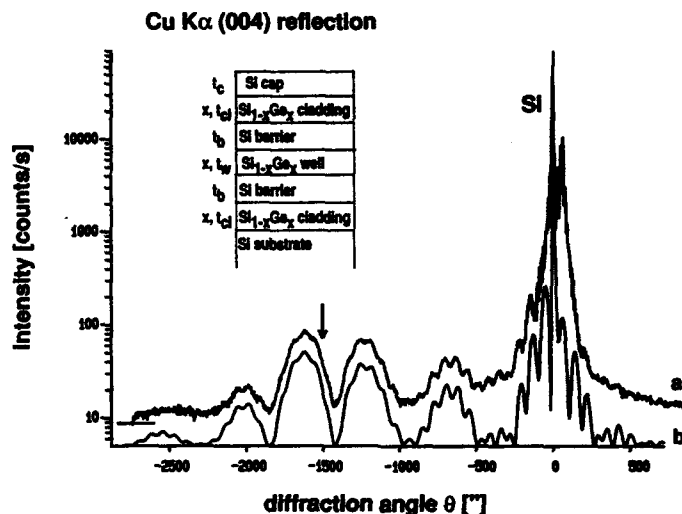


Fig. 3: Experiment (a) and calculated diffraction pattern of a DBRT structure schematically sketched in the insert including the layer parameters. The calculation with $x = 17\%$, $t_{cl} = 28$ nm, $t_b = 5.5$ nm, $t_w = 3.5$ nm, and $t_c = 205$ nm matches the experiment. The arrow indicates the angular position for a $Si_{1-x}Ge_x$ alloy layer with $x = 17\%$. For clarity, curve (a) is shifted upward.

DISCUSSION AND CONCLUSION

X-ray diffraction is used for an analysis of pseudomorphically grown $Si_{1-x}Ge_x/Si$ HBT and DBRT structures. Structural data, as layer composition and thickness, are determined by a fit of computer simulations to the experimental XRC. The diffraction pattern of a HBT structure shows well separated features which allow for an accurate determination of lattice mismatch and thickness of the base and the emitter layer. With a DBRT structure pronounced X-ray interference effects between the individual layers make an interpretation of the diffraction pattern rather difficult. An elaborate fit procedure by computer simulation is indispensable to resolve the layer parameters in this latter case. The simulations in Fig. 2 indicate that the diffractogram contains much information in the tails away from the Bragg peaks. Some of these weak details cannot be resolved in the experimental XRC because of a background of about 2 counts/s.

It is widely believed that an XRC is unique to a particular layer structure. However, the complicated behaviour of the diffraction lines obtained from a sandwich structure like the DBRT arises the question for a potential ambiguity of the results derived from the XRC. Cockerton and coworkers [19] reported on such a problem in the interpretation of a thin layer at the interface between a GaInAsP epilayer on InP substrate and they recommend to use additional analytical techniques. In the present study, the finite background and also the reduced number of parameters limit the accuracy of the results. On the other hand, the layer set-up is known and very likely layer parameters were available from the growth record as starting values for the simulations and therefore, an unambiguous determination of the structural data is possible when fitting both line positions and intensities.

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INTENSITY MODULATION OF GLANCING ANGLE X-RAY DIFFRACTION
SPECTRA OF $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ SUPERLATTICES

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ABSTRACT

The glancing angle x-ray diffraction spectra of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ superlattices grown by MBE under different temperatures are investigated. Three different types of the intensity distributions of diffraction peaks are observed, which are believed to be corresponded with different situations of interfaces. If all the interfaces in superlattice structure are highly flat, up to 17 orders diffraction peaks are identified with their intensities modulated by a periodical envelope function, otherwise the distribution of diffraction intensities follows simply a decaying function. A quantitative analysis using computer simulation based on the modified Bragg's law and the optical multilayer theory is used to derive the structural parameters including the thicknesses of Si and $\text{Ge}_x\text{Si}_{1-x}$ layers, superlattice period, Ge content x and the degree of interfacial roughness.

INTRODUCTION

X-ray diffraction is the most commonly used technique to characterize the structural parameters of semiconductor superlattices. When the diffraction wave vector is parallel to the growth direction of the superlattice, there appears around the small angle region and the Bragg angle region of the crystal a series of diffraction peaks arising from the periodical structure of superlattice. For $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained-layer superlattices, x-ray diffraction patterns investigated so far have been mainly focused around the Bragg reflections[1,2,3]. The structural parameters extracted were the periodicity, the thicknesses of the two component materials and the strain distribution in alternated layers. No information concerning the situation of interfaces in the superlattice structure was derived from the Bragg angle diffraction spectra.

In this work, we have investigated the glancing angle x-ray diffraction spectra of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ superlattices grown by molecular beam epitaxy (MBE) at different temperatures, and found that the intensity distribution of diffraction peaks relates closely with the interfacial roughness. A quantitative analysis of the experimental spectra was carried out to derive the structural parameters and the interfacial roughness of the samples.

EXPERIMENTAL

The samples were grown by MBE in a Riber electron beam evaporator system. The base pressure in the growth chamber was 6×10^{-8} Pa and the pressure during evaporation was lower than 1×10^{-7} Pa. The n-type Si(100) substrate wafers were chemically treated by a method similar to Shiraki's procedure[4] before loading into the vacuum chamber. A pre-heating treatment to 800°C under the irradiation of a low flux Si beam in the MBE system was carried out to remove the atmospheric contaminations. Before the superlattice growth, a Si buffer layer with the thickness of about 200 nm was deposited at 620°C, and the surface of the buffer layer showed a sharp streaky (2×1) reflection high

energy electron diffraction (REED) pattern. The superlattices with 20 periods of alternatively stacked 4.5 nm thick $\text{Ge}_{0.5}\text{Si}_{0.5}$ layers and 21.5 nm thick Si layers were grown at three different temperatures, 420, 570 and 620°C. All the samples were capped with a 18.0 nm thick Si layer. The thicknesses of alternated layers and the Ge content x in alloy layers were controlled by the beam fluxes of Ge and Si sources and monitored by two quartz crystal oscillators. The deposition rates of Si and alloy layers were about 0.1 nm/s.

The x-ray measurements were performed by using a computer controlled diffractometer with a rotating Cu anode x-ray source. The $\text{Cu K}\beta$ radiation was eliminated by using a 15 μm thick nickel filter attached to the exit of the slit. The narrow x-ray beam was formed by a 70 μm entrance slit. The beam spot size on the sample was 5 mm long and about 0.02 mm/sin θ wide. The diffraction spectra were measured in θ -2 θ scans with the scanning angle spread from 0.5 to 6° in a step of 0.002° and a scanning rate of 0.25°/min. The zero point of the 2 θ axis was set in the direct path.

RESULTS AND DISCUSSIONS

Three different types of x-ray diffraction spectra were observed for the samples A, B and C grown at the temperatures of 420, 570 and 620°C respectively, as shown in Fig.1(a), (b) and (c). For samples A and B, up to the 17th order diffraction peak could be seen clearly, which indicates that the periodicity of these two superlattices are fairly good; while for the sample C grown at higher temperature, only 9 orders of interference peaks could be identified.

The most notable aspect in Fig.1 is that the intensity distributions of diffraction peaks are quite different for different samples. In Fig.1(a), the relationship of peak intensity versus diffraction angle follows a decaying function modulated with a periodical varying envelope rather than a simply decaying function as that in Fig.1(b) and (c). As to our knowledge, the phenomenon of intensity modulation shown in Fig.1(a) has not been reported and analyzed in previous literatures. We suggest the different intensity distributions in Fig.1 may be attributed to the different situations of interfacial flatness in the samples.

A phenomenological explanation is presented by simply considering the structure factor of the superlattice. The total reflection intensity of a superlattice with glancing angle x-ray incidence is the superposition of the reflection intensities from two sets of interfaces, i.e. the interfaces formed by GeSi grown on Si and that formed by Si grown on GeSi. Both sets of interfaces have the same interplanar spacing as the superlattice period but may have different degrees of flatness. The peak positions for the two sets of diffraction beams coincide with each other. The intensity distribution is thus determined by the structure factor in a superlattice period, which could be expressed as

$$F = f_1 + f_2 \exp(i2\pi \frac{2t_2 \sin\theta + \lambda/2}{\lambda})$$

$$= f_1 + f_2 \exp[i(2\pi m t_2 / T + \pi)], \quad (1)$$

where f_1 and f_2 are the scattering factors of two interfaces respectively, t_2 the thickness of GeSi layer, θ the diffraction angle, λ the wavelength of x-ray, m the diffraction order and T the period of superlattice. If we assume there is no diffuse scattering or other reflection losses, the total reflection intensity is proportional to the square of the module of structure factor.

$$I(m) \propto |F|^2 = (f_1 - f_2)^2 + 4f_1 f_2 \sin^2(\pi m t_2 / T). \quad (2)$$

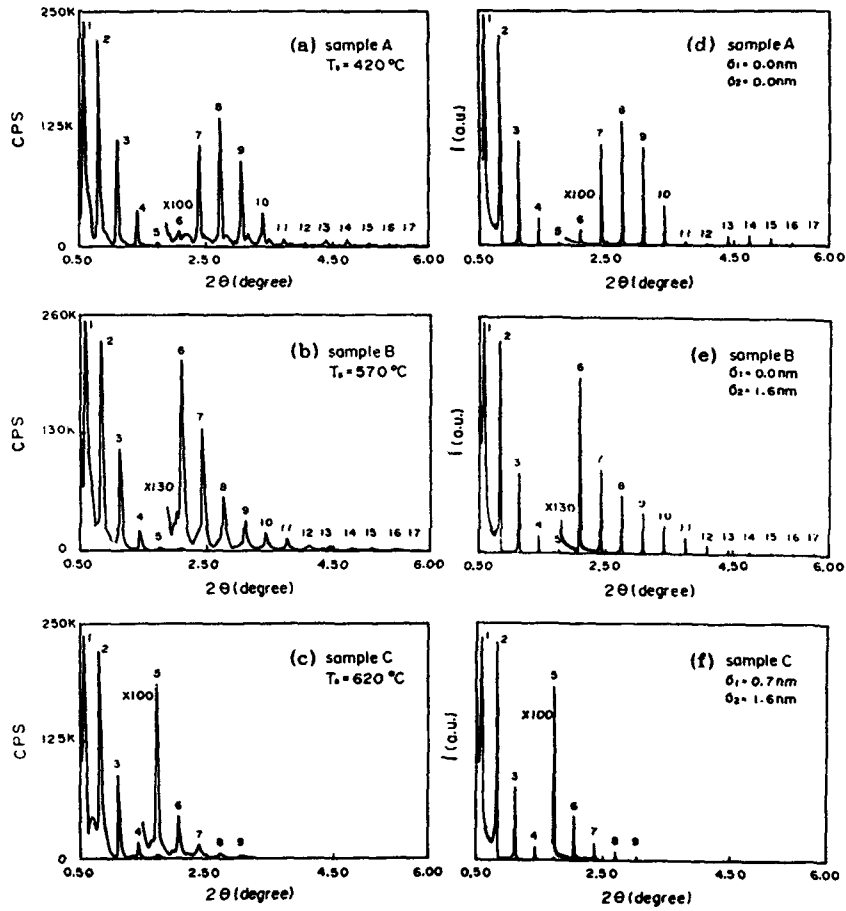


Fig.1 Glancing angle x-ray diffraction spectra of $GexSi_{1-x}/Si$ superlattices grown at different temperatures. (a)-(c) measured, (d)-(f) calculated.

The x-ray diffraction spectrum of sample A agrees qualitatively with the above expression. The envelope function is approximately the square of a sinusoid. The numbers of diffraction peaks involved in each envelope hump equals approximately the ratio T/t_2 . If one set of interfaces is not very flat, diffuse scattering of x-ray will cause the reduction of intensities of one diffraction component relative to another. This could be equivalent to $f_2 \ll f_1$ in Eq.(2). The sinusoidal term is not dominant, therefore the effect of intensity modulation is rather weak to be visible as in Fig.1(b). If both sets of interfaces are rough, the peak intensity will decay rapidly as the diffraction order increases.

The quantitative analysis of the diffraction spectra to derive the structural parameters is carried out following the method of Sugawara et al. [5]. At small incident angles, the x-ray refraction at the superlattice surface and interfaces should be taken into account, thus the interference peak angles θ_m obey the following modified Bragg's law:

$$\sin^2 \theta_m = (\lambda/2T)^2 m^2 + 2\delta, \quad (3)$$

where δ could be written in the following form:

$$\delta = \delta_{s_1} - x(1-t_1/T)(\delta_{s_1} - \delta_{Ge}), \quad (4)$$

where $(1-\delta_{s_1})$ and $(1-\delta_{Ge})$ are the refractive indices of Si and Ge respectively, x the Ge content in GeSi alloy layer, t_1 the thickness of Si layer. For Cu K α radiation, the values of δ_{Ge} and δ_{s_1} are 1.452×10^{-3} and 7.585×10^{-6} respectively [6].

The experimental data for all the three spectra in Fig.1 fit very well with the linear relation of $\sin^2 \theta_m \sim m^2$. From the slope and the intercept of the straight line, one can determine the values of T and δ , the later in turn gives the average Ge content $x(1-t_1/T)$ in a superlattice period by using Eq.(4) and the known values of δ_{Ge} and δ_{s_1} . The results for samples A, B and C are listed in Table I.

Table I. Structural Parameters of Ge_xSi_{1-x}/Si Superlattices

Sample	A	B	C
Growth temperature(°C)	420	570	620
Nominal parameters			
t_{s_1} (nm)	21.5	21.5	21.5
t_{GeSi} (nm)	4.5	4.5	4.5
x	0.5	0.5	0.5
Measured values			
T (nm)	26.2	26.0	26.4
t_{s_1} (nm)	21.7	21.5	21.9
t_{GeSi} (nm)	4.5	4.5	4.5
x	0.49	0.48	0.50
σ_1 (nm)	0	0	0.7
σ_2 (nm)	0	1.6	1.6

The next step is to determine the layer thicknesses t_1 and t_2 of Si and GeSi alloy as well as the value x . The optical multilayer theory can be employed. At a boundary of two materials of complex refractive indices \tilde{n}_1 and \tilde{n}_2 , the amplitudes of reflection waves are given by the Fresnel equations:

$$r_s = \frac{\tilde{n}_1 \cos \alpha_1 - \tilde{n}_2 \cos \alpha_2}{\tilde{n}_1 \cos \alpha_1 + \tilde{n}_2 \cos \alpha_2}, \quad (5)$$

$$r_p = \frac{\bar{n}_1 \cos \alpha_2 - \bar{n}_2 \cos \alpha_1}{\bar{n}_1 \cos \alpha_2 + \bar{n}_2 \cos \alpha_1}, \quad (6)$$

where subscripts s and p denote the polarized components of the light, $\alpha_1 = 90^\circ - \theta$, θ is the glancing angle, α_2 is related to α_1 by Snell's law. The reflectivities R_s and R_p are given by $R_s = |r_s|^2$ and $R_p = |r_p|^2$. For a single layer of thickness d , the reflection amplitude is given as

$$r = \frac{r_t + r_b \exp(2i\Delta)}{1 + r_t r_b \exp(2i\Delta)}, \quad (7)$$

where r_t and r_b are the reflection amplitudes at the top interface and the bottom interface of the film, which could be obtained from Eq.(5) and Eq.(6), is the phase shift of the wave at a propagation angle α through the film,

$$\Delta = 2\pi d \bar{n} \cos \alpha / \lambda. \quad (8)$$

In the glancing angle region, the reflectivity is essentially independent of polarization. In the case of superlattices, the reflectivity is calculated by recursive application of Eq.(7). That is, taking the reflection amplitude at the interface of superlattice and substrate calculated by Eq.(5) as r_b , the reflection amplitude at the interface of first layer ($\text{Ge}_x\text{Si}_{1-x}$) and the second layer (Si) as r_t , we calculate r_1 of the first layer ($\text{Ge}_x\text{Si}_{1-x}$) which is the layer in superlattice just next to the substrate. Then we calculate the reflection amplitude r_2 of the second layer (Si) by using r_1 as r_b and the reflection amplitude at the interface between the second and third layers as r_t . Successively calculating the reflection amplitudes until the multilayer is fully transversed, the reflectivity of an N period superlattice is finally obtained and the intensity of diffraction x-ray is proportional to $|R|^2$.

The relative intensities of higher order peaks to the first order peak, especially I_2/I_1 , have been found to be sensitive to the thickness ratio of the two components in superlattice. By comparing the experimental I_2/I_1 to the calculated value, one can determine the thickness t_1 and t_2 of Si and GeSi layers, which in turn give the value x since the average Ge content has been obtained from the modified Bragg's law described above. The experimental I_2/I_1 for these samples are almost the same, however, since the intercept of $\sin^2 \theta_0 \sim m^2$ straight line is a small number which could not be extrapolated with sufficient accuracy, a small deviation of δ will cause big difference on the derived values of x , although the designing parameters for these three samples are not different.

The above mentioned method treats the interfaces as ideally flat, therefore it does not provide any information about the interfacial roughness which would likely exist in a real superlattice. Imperfect boundaries can easily be incorporated into the calculation by introducing a roughness factor (RF) multiplied on the Fresnel coefficients [Eq.(5) and (6)],

$$RF = \exp[-2(2\pi \sigma \cos \alpha / \lambda)^2], \quad (9)$$

where σ represents the width of a transition layer at the boundary caused by the interfacial roughness [7]. The transition layer reduces the reflectivity but increases the transmission by an equivalent amount. With the above approximation, we assume that there exist transition layers of σ_1 and σ_2 at the two boundaries of $\text{Ge}_x\text{Si}_{1-x}$ on Si and Si on $\text{Ge}_x\text{Si}_{1-x}$. By adjusting the parameters t_1 , t_2 , x , σ_1 and σ_2 , the computer simulations of the x-ray diffraction patterns were carried out by using the same recursive procedure described above. The best fits for samples A, B, C are shown in Fig 1 (d)-(f) with the derived structural parameters listed in Table I, where the experimental layer thicknesses and Ge content coincide satisfactorily with the

designing parameters.

The above results show that for the sample grown at 420°C, the two sets of superlattice interfaces are both highly flat; for the sample grown at 570°C, the interfaces formed by GeSi grown on Si are flat but the another set of interfaces are not; while for the sample grown at higher temperature, both sets of interfaces are not flat. This has been further illustrated by cross sectional transmission electron microscopic observations(not shown here).

CONCLUSION

We have studied the x-ray diffraction spectra of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ superlattices at glancing angle incidence. Different types of intensity distributions of the diffraction peaks have been observed. The phenomenon of intensity modulation which is revealed in the first time is believed to be related with the higher flatness of interfaces in superlattice structure. A computer simulation based on the modified Bragg's law and optical multilayer theory incorporating roughness factors could reproduce the diffraction spectra fairly well and extrapolate the structural parameters including the period, thicknesses of alternated layers, Ge content in GeSi alloy layer as well as the degree of interfacial roughness. For the sample grown at lower temperature, all the interfaces in superlattice are shown to be very flat. For the sample grown at moderate temperature, the interfaces formed by GeSi grown on Si are flat while those formed by Si grown on GeSi are rough. For the sample grown at higher temperature, both sets of interfaces are not flat.

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TEMPERATURE DEPENDENCE OF CRITICAL THICKNESS FOR TWO DIMENSIONAL
GROWTH OF $\text{Ge}_x\text{Si}_{1-x}$ ON Si SUBSTRATE

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ABSTRACT

For obtaining good structural perfection, the molecular beam epitaxial (MBE) growth of $\text{Ge}_x\text{Si}_{1-x}$ on Si substrate should not only be kept in the pseudomorphic form but also in layer-by-layer growth stage. We found that the two dimensional layer-by-layer growth of $\text{Ge}_x\text{Si}_{1-x}$ on Si could persist to a certain deposition thickness, beyond that the transition to islanding growth occurs. The transition thickness is significantly dependent on the growth temperature and germanium content, and is always smaller than the critical thickness of pseudomorphic growth. In order to obtain good crystalline quality in growing $\text{Ge}_x\text{Si}_{1-x}$ superlattices on Si substrates, the thickness of $\text{Ge}_x\text{Si}_{1-x}$ layers should be controlled below the transition thickness and lower growth temperature is favorable.

INTRODUCTION

$\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ is a lattice mismatched semiconductor heterojunction system. The large lattice misfit can be accommodated either by misfit dislocations within the interface region or by elastic strain in the epitaxial film. It is well known that if the thickness of epilayer is controlled below a critical value, the lattice misfit could be fully accommodated by the built-in strain such that the epitaxial film is completely coherent with the substrate. In previous mechanical equilibrium theory [1] and energy equilibrium theory [2], the critical thickness of the pseudomorphic growth of $\text{Ge}_x\text{Si}_{1-x}$ on Si has been considered as only depending on the germanium content x , or in other word on the lattice misfit. On the other hand, the growth of $\text{Ge}_x\text{Si}_{1-x}$ on Si is in a Stranski-Krastanow mode. If islanding occurs, the surface of epitaxial $\text{Ge}_x\text{Si}_{1-x}$ layer becomes corrugated. For the purpose of device applications, it is necessary to grow $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterojunctions or superlattices with flat and abrupt interfaces and free of misfit dislocations. Therefore, the heteroepitaxial growth should be carried out not only in the pseudomorphic form but also at the layer-by-layer deposition stage. In this work, we present that the transition from two dimensional to three dimensional growth of $\text{Ge}_x\text{Si}_{1-x}$ on Si(100) occurs at the thickness well below the critical thickness of pseudomorphic growth. This transition thickness depends not only on the alloy composition but also on the growth temperature significantly.

EXPERIMENTAL

The epitaxial growth of $\text{Ge}_x\text{Si}_{1-x}$ on Si was performed in a molecular beam epitaxy system and the transition from 2D to 3D growth was monitored in situ by the observation of reflection high energy electron diffraction (RHEED) patterns. The Si(100) substrates were chemically treated first and then heated in the ultra-high vacuum chamber to remove the atmospheric contaminations and surface oxidized layer. A Si buffer layer of 100nm was deposited at 620°C to make the substrate surface more flat as shown by the sharp and streaky RHEED pattern. The growth of $\text{Ge}_x\text{Si}_{1-x}$ epilayers was carried out at different

substrate temperatures and different Ge contents. The ratios of Ge to Si, i.e. the value of x , was controlled by the beam fluxes of Ge and Si, which were monitored separately by two quartz crystal oscillators. The overall growth rate of $\text{Ge}_x\text{Si}_{1-x}$ was about 0.6Å/s. The RHEED pattern was watched during the growth. The transition from 2D to 3D growth was determined by the change of a streaky (2×1) RHEED pattern to a spotty one. Although this is not a rigorous criteria, it provides an easy way to access the beginning of islanding growth and also the upper limit of epilayer thickness beyond which the interfacial flatness could not be guaranteed. We found that sometimes the change of streaky RHEED pattern to a spotty one was happened within a quite narrow thickness range, especially for larger x and higher growth temperature. So the judgment of 2D to 3D growth transition by RHEED pattern variation in our case is acceptable.

RESULTS

The thickness of $\text{Ge}_x\text{Si}_{1-x}$ epilayer at which the transition from 2D to 3D growth occurs is defined as the transition thickness h_c . h_c is not only related with the germanium content but also depends on the growth temperature, as shown in fig.1. The decrease of growth temperature increases the transition thickness but in all cases it is smaller than the critical thickness at the same Ge content determined by People and Bean [2].

The influence of growth temperature on the growth mode has been verified by the cross sectional transmission electron microscopy (XTEM) observations. In order to see whether the surface of epilayer is flat (2D growth) or not (3D growth), the samples were fabricated into the multi-layered structures. In fig.2 show the XTEM pictures for two $\text{Ge}_{0.5}\text{Si}_{0.5}$ /Si superlattice samples grown at 470°C and 570°C. The dark areas correspond to the $\text{Ge}_{0.5}\text{Si}_{0.5}$ layers grown on the top of Si (white areas). According to fig.1, the transition thicknesses of $\text{Ge}_{0.5}\text{Si}_{0.5}$ grown at these two temperatures are 4.5 and 2.0 nm respectively, while the nominal thickness controlled by the growth process is 4.5 nm. So in sample A (470°C) the interfaces are very flat, the whole growth process was in the Frank-vander Merve mode; while in sample B (570°C), the thicknesses of $\text{Ge}_{0.5}\text{Si}_{0.5}$ layers are larger than h_c , the corrugation of $\text{Ge}_{0.5}\text{Si}_{0.5}$ alloy layer surfaces could be clearly seen.

Although in sample B the alloy layer thickness has exceeded the transition thickness but it still within the limitation of pseudomorphic growth. Therefore, in the GeSi alloy layers still remains large misfit strain. If we compare the Raman spectra and the X-ray large angle diffraction spectra of samples A and B, it can be found that all the peak positions coincide each other as shown in fig.3 and fig.4. In the Raman spectra, the Ge-Ge, Ge-Si and

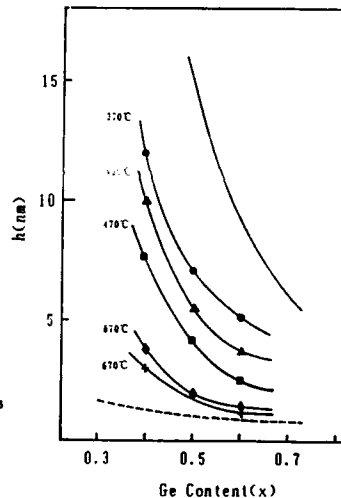


Fig.1. Transition thickness of 2D to 3D growth for $\text{Ge}_x\text{Si}_{1-x}$ on Si(100). Dashed line: Predicted by free energy consideration, Dots: Experimental data, Solid line: Critical thickness of pseudomorphic growth after People and Bean.

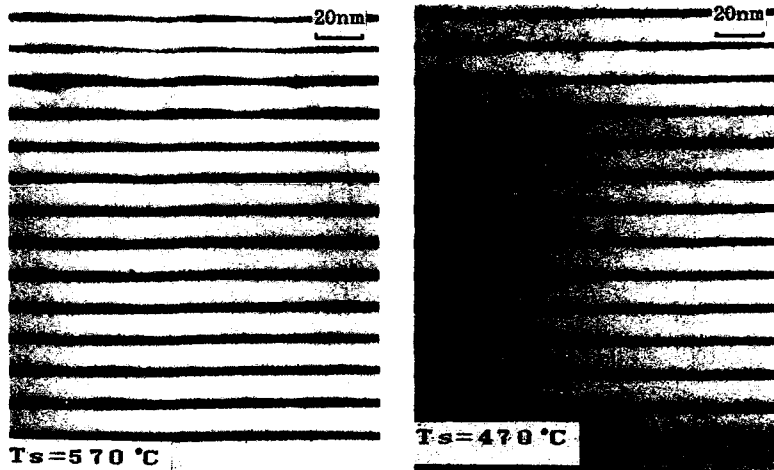


Fig.2. XTEM pictures of two $\text{Ge}_{0.5}\text{Si}_{0.5}/\text{Si}$ superlattices grown at different temperatures. The upper faces of GeSi alloy layers grown at higher temperature show significant corrugation.

Si-Si peaks from the alloy layers locate at 302 , 421 and 506 cm^{-1} , which are all higher than the corresponding peak positions in an unstrained bulk GeSi alloy with same Ge content [3]. The upward shifts of these three peaks in our samples indicate the existence of a compressive lateral strain. The sample B has the same Raman peak positions as that of sample A, the later is an unrelaxed superlattice with flat interfaces, except that the shape of Si-Si peak in sample B appears as a shoulder of Si phonon peak rather than a separated peak as in sample A. The resolution of Raman spectra is about 1 cm^{-1} , which corresponds to the variation of lattice misfit of ± 0.002 . That is, the relaxation of misfit strain if happened in a $\text{Ge}_{0.5}\text{Si}_{0.5}$ epilayer with the thickness smaller than the critical thickness but larger than transition thickness is less than 10%. The result of X-ray diffraction spectra gives the same conclusion, where the peak

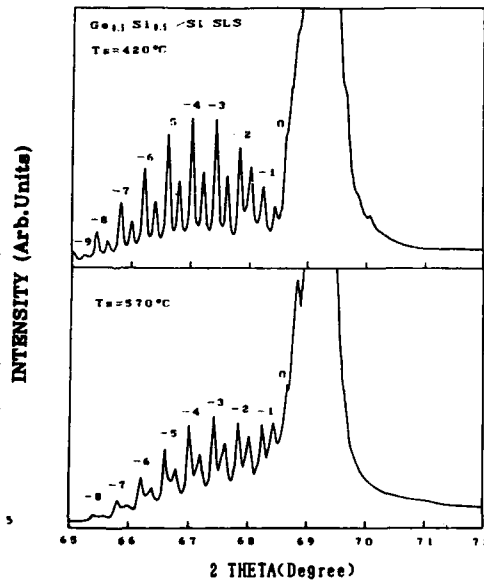


Fig.3. X-ray diffraction spectra of two $\text{Ge}_{0.5}\text{Si}_{0.5}/\text{Si}$ superlattices grown at 420°C and 570°C .

shifts are below the precision of $0.002^\circ(2\theta)$, correspondingly, the relaxation of misfit strain is smaller than $\pm 2\%$.

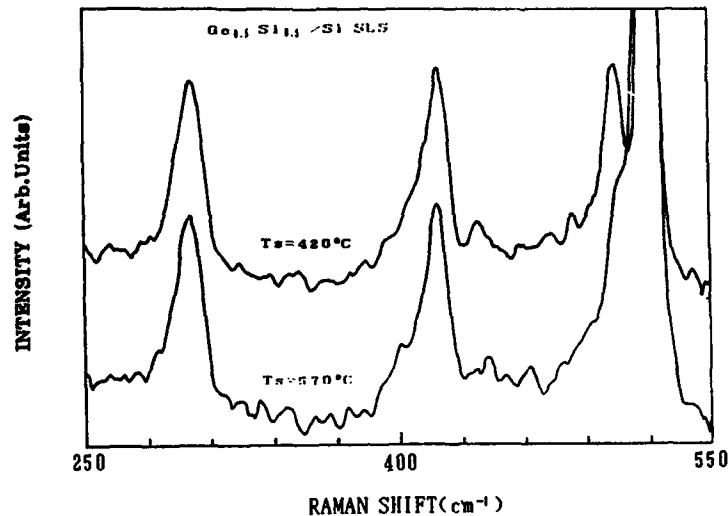


Fig.4. Raman scattering spectra of two $\text{Ge}_{0.5}\text{Si}_{0.5}/\text{Si}$ superlattices grown at 420°C and 570°C .

DISCUSSIONS

It has been known from the thermodynamic models of epitaxial growth that the growth of $\text{Ge}_x\text{Si}_{1-x}$ on Si is in the Stranski-Krastanow mode. Here the free energy plays a central role. For growing a definite thickness of lattice mismatched epilayer, the change of surface free energy is

$$\Delta\sigma = \sigma_f + \sigma_i - \sigma_s + \delta, \quad (1)$$

where σ_f , σ_i and σ_s are the free energies of epilayer surface, interface and substrate surface respectively, δ the free energy term arising from the strain in the epilayer. For $\text{Ge}_x\text{Si}_{1-x}$ on Si, the free energy of epilayer surface could be roughly expressed as

$$\sigma_f = x\sigma_{\text{Ge}} + (1-x)\sigma_{\text{Si}}, \quad (2)$$

where σ_{Ge} and σ_{Si} are the surface free energies of Ge and Si respectively. δ is a function of x and epilayer thickness h [2]:

$$\delta(h,x) = 2G \left(\frac{1+\nu}{1-\nu} \right) h f_0^2 x^2, \quad (3)$$

where G is the shear modulus of epilayer, ν the Poisson's ratio, $f_0 \approx 0.042$ is the lattice misfit between pure Ge and Si. The Bauer criteria for 2D growth is $\Delta\sigma < 0$. If we neglect the term σ_i in Eq.(1), since it is very small for chemically compatible interface, the transition thickness h_c derived from Eqs.(1)-(3) is given by:

$$h_t = \frac{\sigma_{Si} - \sigma_{Ge}}{2(1+\nu/1-\nu)f_0^2 Gx} \quad (4)$$

The above expression explains the experimental $h_t \sim x$ relation qualitatively. To make a rough estimation, we use the following parameter values: $\sigma_{Si} = 1240$ erg/cm², $\sigma_{Ge} = 1100$ erg/cm² [4], $G_{Si} = 5.09 \times 10^1$ dyne/cm², $G_{Ge} = 4.01 \times 10^1$ dyne/cm² [5,6], $\nu_{Ge} = 0.273$, $\nu_{Si} = 0.280$. The ν and G of Ge_xSi_{1-x} layer in Eq.(4) could be considered as the averages of that of Ge and Si. The calculated $h_t \sim x$ relation is shown as the dashed line in fig.1.

The above argument does not take into account the effect of growth temperature, so it is valid only when the thermodynamics is dominant. This is only true under high growth temperature. At lower growth temperature, the kinetics is considered to be dominant over energetics. The slow down of the surface migration makes the "frozen" of deposited atoms to prevent the occurrence of clustering although the thickness of epilayer is large enough to cause the change of $\Delta \sigma$ from negative to positive. Therefore, a "quasi" - two dimensional growth may occur. In our case, the transition thicknesses of Ge_xSi_{1-x} on Si observed at 670°C is still deviated from the values derived from Eq.(4).

It could be seen from fig.1, for growing Ge_xSi_{1-x}/Si superlattices with highly flat interfaces, the thicknesses of alternatively stacked layers should be controlled below the transition thicknesses of 2D to 3D growth, and therefore lower growth temperature is preferable. In our experiment, we found that the optimized growth temperature is about 420°C, below that the crystallinity of superlattice structure could not be guaranteed. The Rutherford backscattering and ion channeling spectra of two Ge_{0.5}Si_{0.5}/Si superlattices grown at 420°C and 370°C show that the minimum channeling yields χ_{min} of these two samples are 3% and 10% respectively.

In conclusion, the growth of strained Ge_xSi_{1-x} on Si is in the Stranski-Krastanow mode. The transition from 2D to 3D growth is determined predominantly by the kinetics rather than thermodynamics. The transition thickness is a function of Ge content x and growth temperature, and is in all cases smaller than the critical thickness of pseudomorphic growth. In growing high quality Ge_xSi_{1-x}/Si strained layer superlattices, it is better to remind that the layer thicknesses should be controlled below the transition thickness rather than the critical thickness.

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The Effect of Oxygen on the Thermal Stability of Si_{1-x}Ge_x Strained Layers Grown by Limited Reaction Processing

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ABSTRACT

Si_{1-x}Ge_x layers containing 2×10^{20} oxygen atoms/cm³ exhibit an enhancement in thermal stability when compared to similar films (comparable Ge content and thickness) with 2 orders of magnitude less oxygen. X-ray measurements of the lattice constants in the strained films indicate that the oxygen does not substantially change the amount of strain in the layers. A prediction of the effect of oxygen based on solid solution strengthening theory is shown to be consistent with experimental annealing results. In addition, experimental measurements of slower misfit dislocation velocities in the layers with high oxygen content compared to those measured in films with low oxygen content, support the idea of solid solution strengthening. It is therefore likely that oxygen impedes the kinetics of dislocation formation.

INTRODUCTION

The Si_{1-x}Ge_x films in this report were grown by the chemical vapor deposition technique Limited Reaction Processing (LRP) [1]. We have previously reported on the thermal stability of single strained layers and capped structures where the Si_{1-x}Ge_x films contained $\sim 2 \times 10^{20}$ oxygen atoms/cm³ [2]. Such films, with high oxygen content, have been used as the base layers in high speed heterojunction bipolar transistors with near-ideal characteristics [3]. The recent addition of a turbo-pumped load-lock to the LRP growth chamber has made it possible to grow Si_{1-x}Ge_x films at 625 °C with an oxygen content below the detection limit of secondary ion mass spectrometry (SIMS) [4,5].

In the present report, the thermal stability of similar Si_{1-x}Ge_x films with high and low oxygen contents are compared. Solid solution strengthening theory is then used to estimate the expected amount of strengthening due to 2×10^{20} cm⁻³ oxygen. Finally, the effect of the oxygen on misfit dislocation velocities, measured using *in situ* heating in the high voltage transmission electron microscope (HVTEM), is presented.

EXPERIMENTAL DETAILS

The goal of these experiments was to quantify the effect of oxygen on misfit dislocation formation during post-growth annealing of Si_{1-x}Ge_x layers with high and low oxygen contents. Such an experiment requires layers with both high and low oxygen contents of various thicknesses. Hence, appropriate films were grown with Ge fractions of 14.5% and 21%. In each case the film thickness was varied from one to about five times the Matthews equilibrium critical thickness ($h_c = \text{about } 135 \text{ \AA} \text{ and } 250 \text{ \AA} \text{ for } 21\% \text{ and } 14.5\% \text{ Ge alloys respectively}$) [6]. The resulting layers for the annealing experiments ranged in thickness from about 135 Å to 550 Å for the 21% films and from 220 Å to 900 Å for the 14.5% layers and had few if any misfit dislocations in the as grown condition. Film thicknesses and compositions were measured using Rutherford backscattering spectrometry (RBS) in a grazing angle geometry, with a scattering angle of 92°. Computer simulations were used to extract the film thickness and Ge fraction from the raw spectra. In some cases film thickness values were also measured using cross sectional TEM.

Annealing experiments were carried out in a lamp heated rapid thermal annealing (RTA) furnace using small pieces cleaved from the LRP wafers. An annealing condition of 850 C for 4 minutes was chosen to allow ample thermal exposure for the initially metastable films to substantially relax towards equilibrium. Because of concerns about possible differences in the number of misfit dislocation nucleation sources among samples, large scratches were hand scribed into the $\text{Si}_{1-x}\text{Ge}_x$ layers in each specimen to make nucleation equally easy in all cases. Prior to annealing, the scribed samples were prepared using a modified RCA clean followed by a dip in a dilute solution of hydrofluoric acid (HF) in water (1:50). TEM specimens were made from the annealed samples using standard backside etching methods and were examined using either the conventional TEM or a HVTEM. In some cases x-ray topography was employed to confirm the results from the TEM experiments. The intent of these examinations was to determine whether or not misfit dislocations formed in the samples during the severe anneal and not to quantify the amount of dislocation formation by measuring average misfit dislocation spacings. In some cases it was necessary to examine more than one TEM specimen to reach the correct conclusion. For example in several specimens, misfit dislocations were not present far removed from the scratch but were evident in large numbers immediately adjacent (within 100 microns) to this region of crystalline damage. It is important to note that oxide precipitates were not observed in any of the samples either prior to or after annealing.

Measurements of misfit dislocation velocities were performed using *in situ* heating in the Kratos HVTEM at the National Center for Electron Microscopy at Lawrence Berkeley Laboratories using electrons accelerated at 1.2 MeV. The techniques employed here are similar to those described by Hull et. al. [7] for measurements made using the conventional TEM. A Gatan single tilt, water cooled heating stage was employed to anneal the samples. Temperature was monitored using a type K thermocouple attached to the Gatan furnace. Images of moving misfit dislocations are projected onto a video monitor via an optical fiber bundle in the final TEM image plane coupled with a video camera. A VCR records images from the video monitor. All images were recorded at a microscope magnification of 2000x.

RESULTS AND DISCUSSION

Annealing Experiments

Figure 1 summarizes the TEM data from the annealing experiments for both the high and low oxygen $\text{Si}_{1-x}\text{Ge}_x$ layers. For the high oxygen films, no misfit dislocations were found in either 14.5% or 21% Ge layers as thick as two times the equilibrium critical thickness (Fig. 1 (a)). In contrast, misfit dislocations were found in the low oxygen layers at thicknesses very near the equilibrium values (Fig. 1 (b)). Care should be taken in interpreting this data because there are limits to the resolution of the TEM and x-ray topography for defining the yes/no dislocation transition. In addition, limitations exist in the RBS measurement of film thickness and Ge fraction. Such experimental errors when compounded make it difficult to conclude that the low oxygen layers exactly match the predictions of equilibrium theory. On the other hand, the large increase in thermal stability observed in the high oxygen films cannot be explained by these experimental uncertainties. Figure 2 shows Lang transmission x-ray topographs of two 14.5 % Ge samples after annealing. These specimens have approximately the same thickness and Ge fraction and are the ones represented by the circled data points in Fig.1. Misfit dislocations can be seen as the narrow white lines running perpendicular to the single scratch in the topograph of the low oxygen sample. Dislocations are not visible in the topograph of the high oxygen specimen. The long wavelength oscillatory

contrast in the topographs is an artifact of the measurement. From these results we conclude that approximately twice as much film thickness is necessary to produce misfit dislocations in the high oxygen case compared to the low oxygen films.

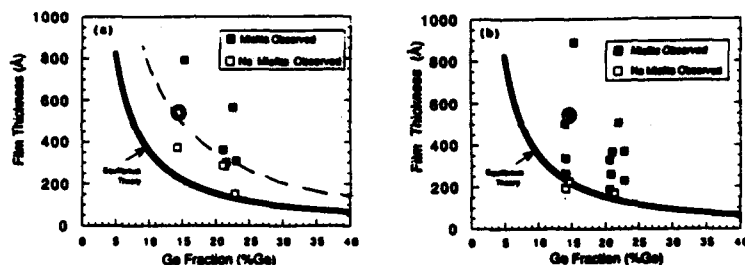


Figure 1: Thermal stability plots for (a) high oxygen films and (b) low oxygen films. Shaded squares represent layers in which misfit dislocations were observed after annealing at 850 C for 4 minutes. Open squares signify samples in which no misfit dislocations were found after the same anneal.

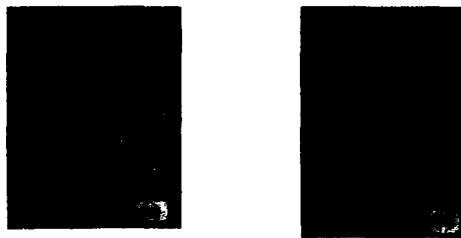


Figure 2: Lang Transmission x-ray topographs of two $\text{Si}_{1-x}\text{Ge}_x$ films after annealing: (a) $2 \times 10^{20} \text{ cm}^{-3}$ oxygen, 14.5% Ge, 550Å thick; no dislocations found after annealing and (b) $< 2 \times 10^{17} \text{ cm}^{-3}$ oxygen, 14.2% Ge, 520Å thick; many dislocations present.

Oxygen Strengthening

Before considering a possible explanation for how oxygen may strengthen the $\text{Si}_{1-x}\text{Ge}_x$ layers, it is necessary to investigate the possibility that oxygen reduces the equilibrium lattice parameter of the films and thereby reduces the strain which is driving misfit dislocation formation. This idea is analogous to strain compensation by B in Ge doped Si [5]. X-ray double crystal rocking experiments were performed to measure the lattice parameters of the strained layers for both the high and low oxygen films. This data can be converted to an equivalent Ge fraction in the layer using standard elastic constants. Germanium fractions measured in this way match those found using RBS to within 1 atomic percent Ge. We conclude that the oxygen does not substantially reduce the amount of strain in the high oxygen layers. Another way to think of this result is to ask the question: "how much strain (Ge fraction) reduction would be necessary to explain the observed increase in thermal stability ascribed to the oxygen?" Assuming the elastic constants are not substantially changed due to the oxygen, the data in Fig. 1(a) can be explained by strain compensation only if the strain in a 21% Ge layer corresponds to that expected in a 12% Ge oxygen-free

film. In the same way the strain in the 14.5% layer would have to correspond to that expected in a 7% Ge film.

A simple solid solution strengthening model can be used to predict a retarding stress due to the oxygen acting on the dislocation threading arm. This predicted retarding stress can in turn be compared to the experimentally measured retarding stress in the high oxygen films. To make such a comparison possible the experimental data, which is in terms of an additional film thickness necessary to produce misfit dislocations during annealing, must be translated into an equivalent amount of stress by utilizing the concept of excess or effective stress [8]. We will see that the prediction of the model matches the experimental result quite well.

A. The predicted retarding stress

In classical solid solution strengthening theory, the strain field associated with the dislocation interacts with the strain field due to the size mismatch between the solute (oxygen) atoms and the host lattice, resulting in an additional amount of stress necessary to move the dislocation in the presence of the solute. We emphasize that it is the threading arm and not the misfit dislocation which is of interest here. The retarding stress due to the oxygen can be found using the following equation [5]:

$$\tau_{\text{retarding}} = \frac{\sqrt{3}}{8\pi} \frac{1+\nu}{1-\nu} \frac{\mu \Delta V}{b^3} \sqrt{X_s} \quad (\text{eq. 1})$$

where ν is Poisson's ratio, b is the Burgers vector of the dislocation, μ is the shear modulus of the solvent, ΔV is the difference in volume between an oxygen solute atom and the solvent atom and X_s is the area fraction of oxygen on the dislocation's slip plane (X_s is identical to the atom fraction for a uniform distribution of oxygen atoms). Since we have assumed that the oxygen in the $\text{Si}_{1-x}\text{Ge}_x$ is uniformly distributed, only ΔV is unknown. Using the precision lattice parameter measurements of Windisch and Becker [9] for elemental Si with dissolved oxygen, together with the method of King [10] for calculating the effective size of solute atoms, we find a ΔV for oxygen in Si of $1.3 \times 10^{-23} \text{ cm}^3$. This same value is assumed to apply for oxygen in $\text{Si}_{1-x}\text{Ge}_x$. Thus, from equation (1), the predicted retarding stress is 110 MPa for a uniform distribution of 2×10^{20} oxygen atoms/cm³. It is important to note that this calculation is sensitive to the value chosen for ΔV .

B. Experimental measurement of the retarding stress

An "experimental" value of retarding stress for comparison to the predicted value above can be found by translating the experimental result represented in Fig. 1 into an equivalent amount of stress using the idea of effective stress. The effective stress is a measure of the driving force for dislocation formation. At the equilibrium critical thickness this driving force is zero. However, according to equation 2, for film thicknesses larger than the equilibrium value the driving force (effective stress) increases with increasing thickness [8]:

$$\tau_{\text{eff}} = \frac{\sqrt{2}\sigma}{2\sqrt{3}} \left(1 - \frac{h_c}{h} \frac{\ln \frac{\beta h}{b}}{\ln \frac{\beta h_c}{b}} \right) \quad (\text{eq. 2})$$

Here σ is the biaxial stress in the layer ($\sigma = Me$), b is the Burgers vector, β is a constant that enters the dislocation core energy, h_c is the equilibrium critical thickness and h is the $\text{Si}_{1-x}\text{Ge}_x$ film thickness. From Fig. 1, the film thickness at which dislocations first form in the high oxygen $\text{Si}_{1-x}\text{Ge}_x$ is $\sim 250\text{\AA}$ for a 21% Ge layer and 520\AA or more for a 14.5% Ge film. Using these values together with the appropriate elastic constants and equilibrium critical thickness values for the 21% Ge and 14.5% Ge films [6] in equation 2, the experimental retarding stress is found to be about 160 MPa for high oxygen $\text{Si}_{1-x}\text{Ge}_x$ films of both Ge compositions. Since the low oxygen layers in this study closely match equilibrium theory, we cannot estimate a retarding stress for this case. The measured value of retarding stress, 160 MPa, matches the value predicted by solid solution strengthening theory, 110 MPa, quite well. This observation suggests that solid solution strengthening by oxygen may explain how misfit dislocation formation is impeded in these strained layers.

Misfit Dislocation Velocity Experiments

If oxygen is strengthening the $\text{Si}_{1-x}\text{Ge}_x$ layers by way of solid solution strengthening, then for thick strained layers the velocity of the misfit dislocation threading arms should be reduced in the high oxygen case when compared to those measured in a similar film with a low oxygen content. Figure 3 shows misfit dislocation velocities as a function of annealing temperature from experiments performed using *in situ* heating in the HVTEM. The velocities are slower in the layers with high oxygen levels by a factor of 6 to 10. In the following analysis, we can see that this reduction in velocity is close to what would be expected based on the predicted retarding stress of 160 MPa from the solid solution strengthening model described above.

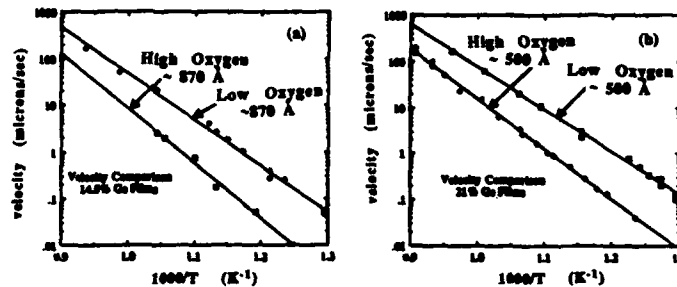


Figure 3: Velocity versus inverse temperature measurements illustrating the effect of oxygen on dislocation velocity for : (a) 14.5% Ge 870Å thick $\text{Si}_{1-x}\text{Ge}_x$ layers, and (b) 21% Ge, 500Å thick films. In both cases the velocities in the high oxygen films are slower by a factor of 6-10x.

The rate of motion of the misfit dislocation threading arm in the $\text{Si}_{1-x}\text{Ge}_x$ film is assumed to be governed by the thermally activated nucleation and motion of kinks along the dislocation line. Because these are near-atomic scale processes, it is expected that the kinetics of dislocation motion in thin films will be the same as that for bulk crystals. Accordingly, based on the experimental work of Alexander and Haasen [11], we assume that the misfit dislocation threading arm velocity can be expressed by an equation of the form

$$v = B \left(\frac{\tau_{\text{eff}}}{\tau_0} \right)^n \exp\left(\frac{-U}{kT}\right) \quad \text{eq. (3)}$$

where U is the activation energy for dislocation motion, B and τ_0 are constants, τ_{eff} is the effective stress for dislocation motion given by eq.(2) and n is an empirical stress exponent ($n=1.2$ for Si and Ge [10] and $1 < n < 2$ for $\text{Si}_{1-x}\text{Ge}_x$ strained layers [12]). Here we will use a value of 1.2 for n . We can calculate an effective stress of 235 MPa for the low oxygen film in Fig. 3(a) using equation 2. The effective stress in the equivalent layer with high oxygen content (Fig. 3a) can be estimated by subtracting the predicted retarding stress, 160 MPa, from the effective stress found for the film with low oxygen content (235 MPa) giving a value of 75 MPa. The reduction in effective stress can then be translated into an expected reduction in dislocation velocity by using a ratio derived from equation 3. The estimated reduction in misfit dislocation velocity due to $2 \times 10^{20} \text{ cm}^{-3}$ oxygen from this ratio is $\sim 4x$. This value is close to the measured velocity difference in the two types of layers (6-10x). The slower dislocation velocities in the samples with high oxygen levels are further evidence supporting the contention that oxygen may be acting as a solid solution strengthening agent in the $\text{Si}_{1-x}\text{Ge}_x$ films.

CONCLUSIONS

LRP-grown $\text{Si}_{1-x}\text{Ge}_x$ layers containing 2×10^{20} oxygen atoms/cm³ are substantially more stable against misfit dislocation formation during high temperature annealing than are similar LRP-grown layers with at least 2 orders of magnitude less oxygen. In addition, misfit dislocation velocities appear to be substantially slower in the films with high oxygen content. These experimental observations are consistent with the predictions of a solid solution strengthening model for the effect of this high oxygen content on thermal stability and misfit dislocation velocities.

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INTERFACE STRUCTURE OF Ge/Si SUPERLATTICES DETERMINED BY X-RAY ABSORPTION FINE STRUCTURE

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ABSTRACT

We illustrate the usefulness of the Extended X-ray Absorption Fine Structure (EXAFS) technique to determine the amount of interface mixing and strain condition in the study of $(\text{Si}_m\text{Ge}_n)_p$ short-period superlattices. It is found that for $n < 4$, the number of Ge and Si nearest neighbours to Ge atoms is consistent with ~25% interfacial mixing and that the Ge-Ge bond length corresponds to that of coherently strained Ge. The Si-Ge bond length is shorter, close to that of a strained $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy. For $n > 4$, the Ge-Ge bond length and the number of Si-Ge nearest neighbours increase significantly consistent with partial relaxation and interdiffusion. Raman scattering spectroscopy and x-ray reflectometry measurements are also presented and are consistent with the conclusions of the EXAFS analysis.

INTRODUCTION

$(\text{Si}_m\text{Ge}_n)_p$ short-period superlattices have attracted considerable attention due to the possibility of unique device properties,¹ but they are also of fundamental interest because of the small dimensionality, high strain and composition gradients. For example, three dimensional growth is known to occur in Ge_n films on (100)Si for a number of monolayers (ML) $n > 4$,²⁻⁵ but there is still debate as to the mechanism of the 2D-3D transformation. Strain at the Si-Ge interface may also significantly enhance interdiffusion making atomically sharp short-period superlattices hard to achieve or preserve upon thermal processing.⁶ Ordering phenomena⁷⁻¹² have been widely reported in this system, but there is no general agreement on its exact nature or the mechanism for formation.

To date, most studies of that system have involved diffraction or microscopy-based techniques. In this paper, we present results obtained using EXAFS which are directly complementary (e.g. short range probe) to those obtained using diffraction techniques and provide a means of testing proposed structural models. The relative numbers of Ge and Si atoms in the first co-ordination shell of Ge and first nearest neighbor distances are determined for a series of $(\text{Si}_m\text{Ge}_n)_p$ superlattices with varying geometry grown on (100) Si. X-ray reflectometry and Raman scattering measurements providing complementary information are also presented.

Table I. Structural data of the $(\text{Si}_m\text{Ge}_n)_p$ atomic layer superlattices.

Sample	T_{Growth} (°C)	λ (nm)	p	m (ML)	n (ML)
698	400	1.2	48	6.6 ± 0.1	2.0 ± 0.1
700	400	1.4	100	8.0 ± 0.1	2.2 ± 0.1
674	400	1.8	24	9.3 ± 0.1	3.7 ± 0.1
844	350	1.5	15	6.8 ± 0.1	3.8 ± 0.1
861	350	3.5	8	16.9 ± 1.0	8.7 ± 1.0
867	350	3.7	8	18.5 ± 2.0	8.0 ± 2.0

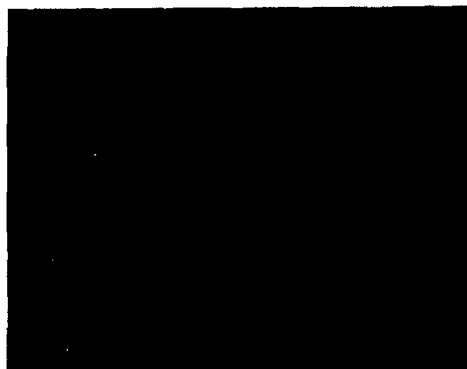


Fig. 1. Transmission electron micrograph of sample 674 demonstrating the two dimensional nature of the superlattice.

EXPERIMENT

The epitaxial layers were produced in a VG Semicon V80 MBE system using a growth methodology described elsewhere.¹³ The samples were grown on (100) Si at a temperature between 350 and 400 °C at a growth rate of ~ 0.4 nm/s. Table I presents the average structural parameters of the films as determined by x-ray diffraction methods.¹⁴ As can be seen from the electron micrograph shown in Fig. 1, the growth has been two-dimensional. This is also true for the $n \sim 8$ layers which although obviously relaxed grew predominately two dimensionally. The specimens may be subdivided in three sets of two samples having a Ge thickness n of 2, 4 and 8-10 and in one case two different growth temperatures.

RESULTS AND DISCUSSION

Raman scattering spectroscopy

Raman scattering from phonons in $(\text{Si}_m\text{Ge}_n)_p$ superlattices can provide information on interface blurring (from, in particular, the folded acoustic modes¹⁵) and intralayer strain,¹⁶ as well as provide an assessment of the overall epitaxial quality of the structure.¹⁷ The Raman spectra of the superlattices were recorded in a quasi-backscattering geometry¹⁸ using 300 mW of 458 or 468 nm laser light. The spectra of all the superlattices could be readily classified into one of three types: best ($n \sim 2$), intermediate ($n \sim 4$) and poor ($n > 4$) quality. Spectra representative of these three categories are shown in Fig. 2. In the best superlattices, the folded acoustic modes, which generally occur at frequencies below 200 cm^{-1} , have an intensity and linewidth comparable to the higher frequency optic modes (see Fig. 2). In the intermediate case (e.g. 674), the folded acoustic modes are significantly broader than the optic modes, and in the poor quality samples, these modes are very broad and weak.

The Raman spectrum of superlattice 698 has been analyzed previously¹⁶ using a model that included possible intermixing, but did not include the effects of strain within the Ge layers. In addition, only integral numbers of monolayers were considered. The observed spectrum was well represented by the superposition of computed spectra for a $(\text{Si}_6\text{Ge}_2)_{48}$ structure (25%) and a blurred interface structure (75%). In these calculations the Si-layer force constants had to be increased by a few percent to allow for strain within the Si layers. In the blurred interface structure the Ge layers were taken to contain a 7.5 % admixture of Si and the neighboring Si interface layers likewise contain a 7.5 % admixture of Ge. Such modeling has shown that detailed information about the structure can be obtained from the Raman spectrum, but the results depend on the details assumed for the average interface blurring/disorder and strain distributions. Specific information about atomic arrangements at the interfaces is needed, before more detailed modeling can be attempted.

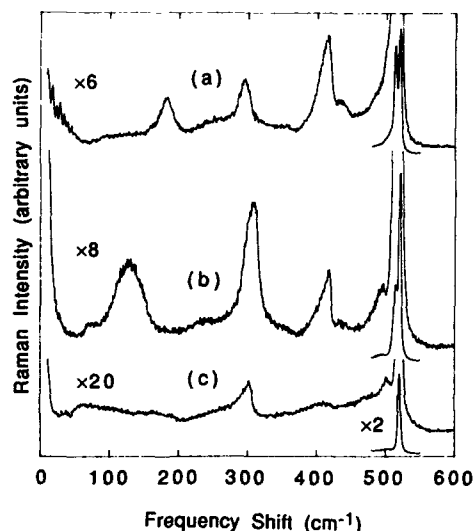


Fig. 2. Raman spectrum of sample (a) 700, (b) 674, and (c) 867. The strong peak at 520 cm^{-1} arises from the Si substrate.

In an earlier study,⁸ it was shown that the optic phonon peak near 435 cm^{-1} can be related to ordering in $\text{Si}_{1-x}\text{Ge}_x$ alloys. This Raman peak is quite weak in all the superlattices (see Fig. 2) indicating little, if any, ordering is occurring at the Si-Ge interfaces in the as-grown structures.

X-ray reflectometry

X-ray reflectometry curves can be used to study the density, periodicity and interface roughness of crystalline or amorphous thin multilayer films. A Philips PW1820 vertical goniometer in a θ - 2θ geometry (using $\text{Cu K}\alpha$ radiation, $\Lambda = 1.54\text{ \AA}$) was used to obtain reflectivity curves on the various samples. At glancing incidence, x-ray scattering by a solid surface is governed by the near-surface electron density. The reflectivity curve from an ideal superlattice of p periods λ exhibits satellite reflections at $2\theta \approx s\Lambda/\lambda$ ($s = 1, 2, 3$) and $(p-2)$ side maxima between each satellite. The reflectivity sharply decreases above a critical angle of total external reflection θ_c ($\sim 0.23^\circ$ for Si) and falls off as $\sin^4\theta$ at high angles. Thickness errors and boundary imperfections can be estimated from the line shape of the reflected intensity curve and this has been discussed in detail elsewhere.¹⁹ For superlattice samples, the effects of structural imperfections on the x-ray reflectivity may be summarized as follows:

- (1) *surface* roughness causes a global reduction of the reflectivity at increasing angle of incidence and possibly disappearance of high order satellite reflections,
- (2) *interface* roughness progressively reduces the intensity of side maxima with increasing angle of incidence,
- and (3) fluctuation of the periodicity causes irregular spacing between the side maxima and a broadening or an asymmetric shape of the satellite reflections.

Figure 3 displays the low-angle θ - 2θ scans from samples 698, 674 and 867. In these spectra, the first superlattice reflection is clearly seen and confirms the two dimensional and periodic nature of the structure. Visual inspection of the spectra reveals structural imperfections that become more significant with increasing Ge thickness n . In samples 698 and 674 the second order satellite is clearly visible at $\theta = 15^\circ$ and 10° , respectively, and indicates little surface rough-

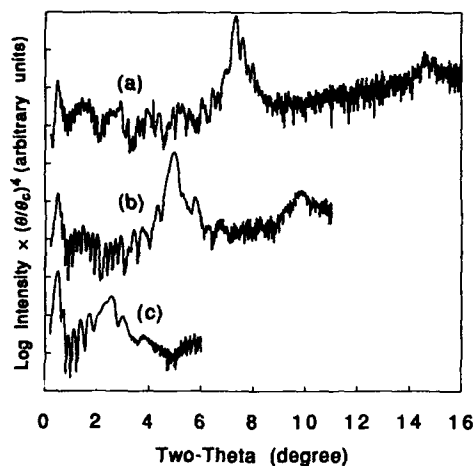


Fig. 3. Grazing incidence x-ray reflectivity of sample (a) 698, (b) 674 and (c) 867. The vertical axis is multiplied by $(\theta/\theta_c)^4$ to enhance details at high angles. The sloping background at high angle is due to the instrumental background.

ness (1-2 monolayers). In contrast, the x-ray reflectivity for sample 867 has reached the instrumental background signal at $\theta = 5^\circ$ consistent with a larger surface roughness (3-5 monolayers). The damping of the side maxima occurs at progressively lower angle with increasing n and indicates higher interface roughness. Preliminary data analysis indicates that the interface roughness in sample 698 is less than half a monolayer, about half a monolayer in sample 674 and about two monolayers in sample 867. These are values averaged over a macroscopic area on the wafer and account for both corrugation and atomic mixing at the interfaces. The irregularities in the side maxima spacing and intensity seen on all samples are consistent with a Gaussian distribution of the superlattice period with standard deviation equal to 5% of the periodicity. A complete analysis of the x-ray reflection data will be presented elsewhere.

EXAFS

EXAFS is the energy dependent interference of the outgoing photoelectron wave created by x-ray absorption above inner-shell ionization thresholds with that component backscattered from the nearby atoms. Quantitative structural parameters pertaining to the superlattices are derived using backscattering amplitudes and phases for the Ge-Ge and Ge-Si components based upon experimental spectra of model compounds (in our case a bulk Ge crystal and a $\text{Ge}(\text{SiMe}_3)_4$ molecule.²⁰) In the study of bulk alloys, EXAFS can determine nearest neighbour bond distances, R , accurate to 0.02 Å, co-ordination numbers, N , to 20% and elemental identity to $\pm 2Z$ units. EXAFS is now beginning to be applied to thin layer systems.^{21,22}

The Ge K-edge experiments were performed at the A3 and C2 beam lines at CHESS using total electron yield detection, measured with a gas-flow electron detector with sample rotation.²³ The detection system has been described in detail elsewhere in conjunction with measurements on Si(As)²⁴ and Si/Ge/Si epilayers.^{25,26} The most significant advance has been in the area of data analysis where a flexible, non-linear least-squares fitting program (MFIT)²⁷ has been developed which can simultaneously fit four spectra, each with up to four components, each component having four (potentially) adjustable parameters. The advantage that MFIT provides is the ability to establish relationships among the parameters in a flexible way in order to constrain the fit within physically significant boundaries. By varying the combinations of the spectra, we fit all six superlattices plus the two model spectra to a consistent set of parameters. This is essentially impossible without the parallel analysis. It is noteworthy that the relative errors in certain parameters (especially the co-ordination) using this analysis is better than quoted above, which makes this a powerful technique to examine the thermal stability of interfaces.²⁸

Table II. Summary of the EXAFS results.

Sample	n (ML)	$R_{\text{Ge-Ge}}$ (± 0.0005 nm)*	$R_{\text{Si-Ge}}$ (± 0.0005 nm)*	$N_{\text{Si-Ge}}/N_{\text{Ge-Ge}}$	
				expt	ideal
698	2.0	0.2410	0.2392	1.35 ± 0.15	1.00
700	2.2	0.2413	0.2386	1.43 ± 0.10	0.83
674	3.7	0.2403	0.2390	0.61 ± 0.03	0.37
844	3.8	0.2409	0.2397	0.58 ± 0.03	0.36
867	8.0	0.2422	0.2408	0.48 ± 0.03	0.14
861	8.7	0.2424	0.2435	0.40 ± 0.03	0.13

*Relative uncertainty (e.g. stability of fitting, sample to sample variations), absolute uncertainty estimated to 0.002 nm.

The results are presented in Table II. In the space allotted, it is not possible to discuss these results in terms of the models proposed,⁶⁻¹² but this will be discussed in detail together with annealing studies of the same samples elsewhere.²⁸ Briefly, a few conclusions from Table II are immediately apparent if one assumes symmetrical intermixing within one layer of the Si-Ge interface:

- (1) for $n < 4$ layers, the Ge-Ge bond length is consistent with the value expected for a fully strained layer (0.2412 nm for Ge, 0.2396 nm for $\text{Si}_{0.25}\text{Ge}_{0.75}$ calculated using classical elasticity theory),
 - (2) for $n > 4$ layers, the Ge-Ge bond length increases, consistent with removal of the strain (relaxation) as has been demonstrated by x-ray diffraction.⁵ (The Ge-Ge bond length is 0.2450 nm for relaxed Ge and 0.2425 nm for relaxed $\text{Si}_{0.25}\text{Ge}_{0.75}$),
 - (3) for $n \sim 2$, the $N_{\text{Ge-Ge}}/N_{\text{Si-Ge}}$ ratio (ideally given by $1/(n-1)$) is consistent with 25% interchange of Si and Ge atoms at both interfaces. For $n \sim 4$, the results are consistent with the same amount of mixing at the interfaces,
 - (4) for $n \sim 8$ layers, there is a significant increase in the number of Si-Ge bonds beyond what was observed for $n \sim 2, 4$. This suggests that strain relief has in part proceeded by interdiffusion,
- and (5) the Si-Ge bond length is consistently shorter than the Ge-Ge bond length. (The Si-Ge bond length for $\text{Si}_{0.25}\text{Ge}_{0.75}$ is 0.2396 nm (strained) and 0.2425 nm (relaxed)).

CONCLUSION

This study has demonstrated that EXAFS can supply "short-range" information (bond lengths, nearest neighbour types) necessary for interpretation of "long-range" techniques such as Raman scattering and diffraction probes. With EXAFS, strain relaxation in the very thin Si-Ge structures could be detected from a change in the Ge nearest neighbour distances. The study has also shown that significant mixing occurs at interfaces of pseudomorphic Si-Ge short period superlattices and should provide a basis for testing models of ordering and growth of strained Si-Ge systems. EXAFS should also be a very powerful probe for studying the thermal stability (onset of interdiffusion) of atomic layer superlattices.

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WET OXIDATION OF EPITAXIAL $\text{Ge}_{.36}\text{Si}_{.64}$ ON (100)Si

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ABSTRACT

The thermal oxidation of epitaxial $\text{Ge}_{.36}\text{Si}_{.64}$ on (100)Si is investigated experimentally for a wet ambient at 700°C and 1000°C. A pure silicon dioxide layer with pile-up of Ge behind the oxide is formed at 1000°C. At 700°C, however, both Ge and Si are oxidized. The Ge is included uniformly into the oxide layer without changing the initial Ge/Si ratio. The result at 1000°C follows the thermodynamical picture which predicts the same result at 700°C also, contrary to observation. The different result at 700°C is due to kinetic constraints which can be explained by different activation energies for the rate of the oxidation reaction and for the Ge or Si diffusivities in GeSi.

INTRODUCTION

Ge-Si heterostructures are currently of interest due to their potentially useful optical and electronic properties. One of the main attractions of this system over other compound semiconductors is its compatibility with Si processing technology, and the possibility of manufacturing very large scale integrated circuits on Si substrates. Thermal oxides play an important role in Si technology. They can be used as insulator, capacitor dielectric, gate oxide, and for masking. The growth of a good quality thermal oxide on GeSi is therefore desirable for many device applications. Several studies of the oxidation of epitaxial GeSi layers have been published [1-4] in which only SiO_2 is formed and Ge piles up behind the oxide. Ge inclusion, however, was occasionally found in the oxide of some high dose Ge^+ -implanted Si [5]. In the present work, Ge is regularly included in the oxide and uniformly distributed in depth. By controlling the temperature, pure SiO_2 can also be formed. A simple model is given that explains the difference.

EXPERIMENT

The GeSi samples used in this study were grown epitaxially onto (100)Si substrates by molecular beam epitaxy. The sample considered here is a layer of $\text{Ge}_{.36}\text{Si}_{.64}$ about 470 nm thick. The film is elastically relaxed as determined from x-ray double crystal diffractometry. The oxidation was done in a tube furnace at 700°C and 1000°C in a wet ambient obtained by bubbling nitrogen gas through 95°C water. Before oxidation the tube was flushed with nitrogen for approximately 1 hr. The samples were then introduced into the furnace.

After about 10 min, the furnace atmosphere was switched from nitrogen to the wet ambient. The samples were analyzed after oxidation by backscattering and infrared absorption spectrometry.

RESULTS AND DISCUSSION

Figure 1 compares the backscattering spectra of two samples oxidized at 1000°C and 700°C.

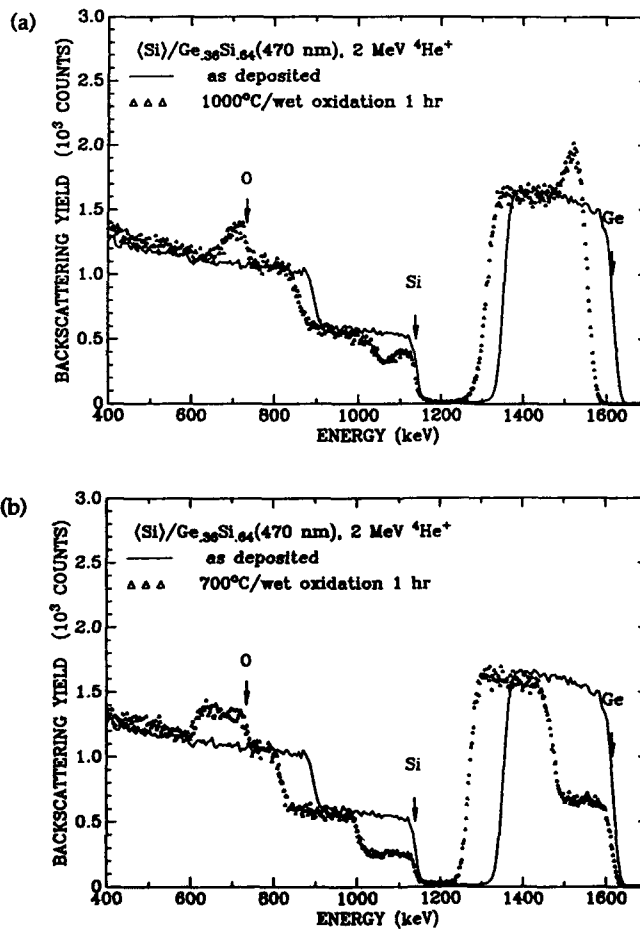


Fig. 1. 2 MeV $^4\text{He}^+$ backscattering spectra of epitaxial $\text{Ge}_{36}\text{Si}_{64}$ films on (100)Si oxidized for 1 hr in steam: (a) at 1000°C (b) at 700°C

It is clear that at 1000°C a surface of pure SiO_2 is formed and Ge piles up behind it as has been seen in previous studies.[1-4] However, the oxide formed at 700°C obviously includes Ge which is uniformly distributed in depth. Within the resolution of backscattering spectrometry, no germanium is lost in both cases. The composition of the oxide at 700°C is $\text{Ge}_{.35}\text{Si}_{.65}\text{O}_2$ which differs insignificantly from the original epilayer of composition of $\text{Ge}_{.36}\text{Si}_{.64}$. No pile-up of Ge or Si is seen behind the oxide. Its structure is x-ray amorphous. These facts strongly suggest that the GeSi layer is oxidized and that the oxide is a mixture of SiO_2 and GeO_2 . The consumption rate of the GeSi layer is 120 nm per hour which is quite large when compared to that of pure Si which is a few nm of Si per hour for similar conditions.

To test the oxidation state of the layer grown at 700°C, a sample was oxidized for 48 hours which completely consumed the GeSi layer and also some of the Si. A Nicolet Model MX-1 Fourier transform infrared spectrometer was used to obtain infrared absorption spectra of the layers. The instrument was calibrated using a polystyrene standard to an accuracy of $\pm 4 \text{ cm}^{-1}$ (25.0 to 6.7 microns). A prominent absorption band centered at 884 cm^{-1} was attributed to antisymmetric Ge-O-Ge stretching vibrations related to hexagonal GeO_2 . In addition, a second, small band at 733 cm^{-1} was attributed to an O-vacancy complex in Ge, i. e. an O substituted for Ge in the tetrahedral building block of Ge. Other bands attributed to SiO_2 were observed.

To interpret these results, we show in Fig. 2 some thermodynamical data of silicon oxide and germanium oxides.

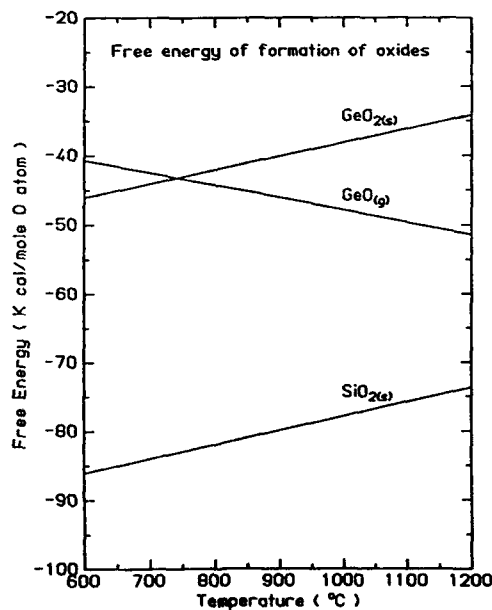
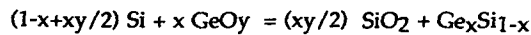


Fig. 2. The free energies of formation of $\text{GeO}_2(\text{s})$, $\text{GeO}(\text{g})$, and $\text{SiO}_2(\text{s})$; the reference states: $\text{Ge}(\text{s})$, $\text{Si}(\text{s})$, and $\text{O}_2(\text{g})$

Since the GeSi oxidation reaction is governed by the addition of oxygen, the free energy of reaction should be measured in terms of kilocalorie per gram atom of oxidant. Therefore, we describe our system by the reaction



The free energy of formation of the GeSi alloy, when approximated by an ideal solution, only contributes an entropy term which amounts to some thousands of calories over the experimental temperature range and is much smaller than the free energy of formation of the oxides. We can therefore compare the free energies of formation of the oxides to determine the equilibrium state of the system. We find that it is SiO_2 with the GeSi alloy that has the lowest free energy over the temperature range of interest. This is so for every x and means that, barring the unlikely possibility of ternary compounds, there is a tieline between Ge and SiO_2 in the ternary phase diagram. In other words, as long as there is Si, SiO_2 is the only stable oxide in this system. The pure SiO_2 formed at 1000°C follows this thermodynamical prediction. The uniform GeSi oxide formed at 700°C , however, does not, which must be due to kinetic constraints.

There are two kinetic factors involved with the reaction: the velocity of oxidation front (proportional to oxidation rate) and the Si supply rate (proportional to Ge or Si diffusivity). For pure Si, the activation energy for the linear rate constant is about 2 eV in both dry and wet ambients [6]. That of the diffusivities of Si and of Ge in either Si or Ge ranges from 3 to 5 eV. The same values apply for the diffusivity of Ge in GeSi (Fig. 3).

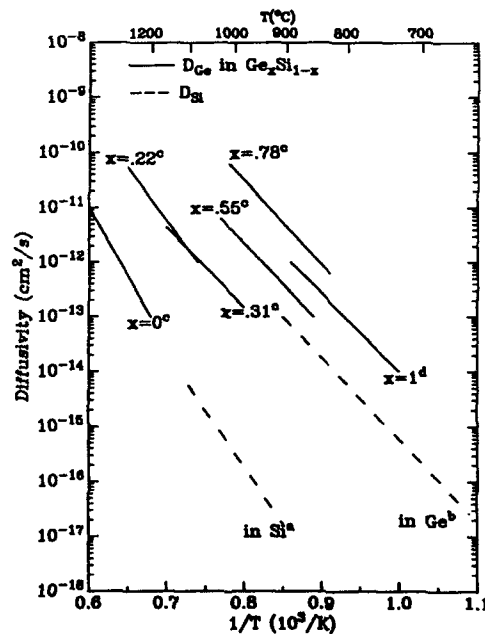


Fig. 3. Temperature dependence of the diffusion coefficient of Ge and Si; activation energies range from 3 to 5 eV
a: ref. 7 b: ref. 8 c: ref. 9 d: ref. 10

Our preliminary results suggest that the rate of oxidation of these samples is linear with the annealing duration employed here. If we assume that the activation energy for the reaction in GeSi is about 2 eV as for Si, the oxidation reaction will slow down little compared to the decrease of the diffusivities in GeSi when the temperature falls. The reason for the different oxide formed at 1000°C and at 700°C becomes clear: at 1000°C, the diffusion of Ge and Si relative to each other is fast compared to the motion of the oxidation front. Thermodynamics controls the outcome in that case and only SiO₂ forms. At 700°C, Ge and Si are immobile compared to the oxidation velocity. Germanium and Si are uniformly oxidized in this case. A similar situation is found in the oxidation of TiSi₂, which is explained in the same way [11]. Experiments are in progress to test the validity of this explanation.

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**MBE GROWTH AND CHARACTERIZATION OF $\text{Si}_x\text{Ge}_{1-x}$
MULTILAYER STRUCTURES ON Si(100) FOR USE AS A SUBSTRATE
FOR GaAs HETEROEPITAXY**

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ABSTRACT

Investigation has continued into the use of $\text{Si}_x\text{Ge}_{1-x}$ multilayer structures (MLS) as a buffer layer between a Si substrate and a GaAs epitaxial layer in order to accommodate the 4.1% lattice mismatch. $\text{Si}_x\text{Ge}_{1-x}$ 4-layer and 5-layer structures terminating in pure Ge have been grown using molecular beam epitaxy. Subsequent GaAs heteroepitaxy has allowed evaluation of these various GaAs/ $\text{Si}_x\text{Ge}_{1-x}$ MLS/Si(100) structures. Antiphase domain boundaries have been eliminated using vicinal Si(100) substrates tilted 6° off-axis toward [011], and the etch pit density in GaAs grown on a 5-layer $\text{Si}_x\text{Ge}_{1-x}$ MLS on vicinal Si(100) was measured to be 10^6 cm^{-2} .

INTRODUCTION

Heteroepitaxial GaAs-on-Si continues to be developed as a potentially viable alternative to bulk and homoepitaxial GaAs crystal technology. Unfortunately, the high threading dislocation density in the GaAs epilayer still remains an impediment for GaAs-on-Si technology to reach full potential. As briefly discussed elsewhere [1,2,3], various means have been employed to reduce the GaAs threading dislocation density from typically $\sim 10^8 \text{ cm}^{-2}$ for GaAs grown directly on Si. It is highly desirable to reduce this threading dislocation density to values obtainable in bulk or homoepitaxial GaAs ($\leq 10^4 \text{ cm}^{-2}$).

The method that employs a multilayer $\text{Si}_x\text{Ge}_{1-x}$ buffer between the GaAs epilayer and the Si substrate has been proposed previously [3,4]. The essence of the concept of using a step-graded $\text{Si}_x\text{Ge}_{1-x}$ multilayer structure (MLS) as a buffer is to segregate the total misfit dislocation density into successive interfaces, thereby minimizing dislocation-dislocation interaction that can potentially form the deleterious threading component of dislocations (referred to simply as threading dislocations). Each $\text{Si}_x\text{Ge}_{1-x}$ epitaxial layer is intentionally grown beyond the critical thickness to form a buried array of misfit dislocations. The final layer is pure Ge, which lattice matches GaAs within 0.2%. In this manner, it is anticipated that the 4.1% total lattice mismatch between GaAs (Ge) and Si will be accommodated plastically in discrete increments. Ge termination is also advantageous because of the relative ease of nucleating GaAs on Ge in contrast to Si. It should also be mentioned that different Ge-terminated $\text{Si}_x\text{Ge}_{1-x}$ buffer layer structures, which incorporated continuous composition grading and/or strained layer superlattices, have been previously investigated for GaAs heteroepitaxy on Si substrates [5].

Initial investigation of GaAs growth on $\text{Si}_x\text{Ge}_{1-x}$ MLSs on Si(100) using a 3-layer $\text{Si}_x\text{Ge}_{1-x}$ MLS grown by remote plasma-enhanced chemical vapor deposition (RPECVD) at 350° C (with a 450° C in situ anneal) showed there were certain deficiencies in these structures [3]. For example, incomplete strain relaxation in the first $\text{Si}_x\text{Ge}_{1-x}$ layer led to the catastrophic production of threading dislocations in the

second $\text{Si}_x\text{Ge}_{1-x}$ layer. It was also believed that a 3-layer structure did not allow sufficiently small increments of lattice mismatch; the lattice mismatch between each layer was $\sim 1.3\%$. Lastly, the GaAs films contained antiphase domain boundaries (APBs) because nominally-oriented Si(100) wafers were used.

This paper describes the growth of 4-layer and 5-layer $\text{Si}_x\text{Ge}_{1-x}$ MLSs on vicinal Si(100) by molecular beam epitaxy (MBE) for use as engineered substrates for GaAs growth by organometallic chemical vapor deposition (OMCVD).

EXPERIMENTAL PROCEDURE

Vicinal Si(100) substrates (4° , 6° , and 8° tilt toward [011]) were chemically cleaned prior to loading into an MBE system. The wafer was maintained at $\sim 925^\circ\text{C}$ for 15 minutes in the MBE chamber to desorb the native oxide. The $\text{Si}_x\text{Ge}_{1-x}$ films were grown using a dual e-beam MBE at 500°C at a growth rate of $\sim 0.5\text{nm}\cdot\text{s}^{-1}$, as determined from quartz crystal rate monitors. Raman spectroscopy and Rutherford backscattering spectrometry (RBS) were used to establish the $\text{Si}_x\text{Ge}_{1-x}$ compositions and to calibrate the quartz crystal rate monitors. The system has a base pressure $\approx 5 \times 10^{-10}$ Torr, and pressures in the 10^{-9} – 10^{-8} Torr range are typical during deposition. Multilayer structures were chosen to be 4-layer $\text{Si}_x\text{Ge}_{1-x}$ structures ($x = 0.75, 0.50, 0.25, \text{ and } 0$ sequentially) and 5-layer $\text{Si}_x\text{Ge}_{1-x}$ structures ($x = 0.80, 0.60, 0.40, 0.20, \text{ and } 0$ sequentially) with each layer thickness being chosen to intentionally exceed the critical thickness for coherent epitaxy [6]. All $\text{Si}_x\text{Ge}_{1-x}$ MLS samples were terminated with pure Ge. Additionally, different thickness $\text{Si}_x\text{Ge}_{1-x}$ layers ($0.5\mu\text{m}$ and $1.0\mu\text{m}$ individual $\text{Si}_x\text{Ge}_{1-x}$ layer thicknesses) were investigated in the context of a 5-layer structure.

GaAs growth was subsequently accomplished by OMCVD at 670°C as described briefly elsewhere [6]. A thin ($\sim 50\text{nm}$) InGaAsP epilayer grown on the Ge [8] initially was found to improve the quality of the subsequently grown $1\mu\text{m}$ GaAs film.

These films were characterized with scanning electron microscopy (SEM) [topographically and with electron beam-induced current (EBIC)], cross-section transmission electron microscopy (TEM), ambient temperature photoluminescence spectroscopy (PL) and etch pit density (EPD) measurements.

RESULTS AND DISCUSSION

Scanning electron microscopy results from GaAs grown on a 4-layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS on 4° off-axis Si(100) are shown in Fig. 1. Each individual $\text{Si}_x\text{Ge}_{1-x}$ layer is $0.5\mu\text{m}$ thick for a total $\text{Si}_x\text{Ge}_{1-x}$ MLS thickness of $2.0\mu\text{m}$. These individual layers each represent a lattice mismatch of $\sim 1\%$ and sufficiently exceed the experimentally observed critical thickness ($\sim 100\text{nm}$) by a factor of approximately five [6]. Topographically, certain non-planar features are observed in relief. EBIC imaging of this sample showed most of these features to be associated with nonradiative carrier recombination as evidenced by the dark contrast. It has been shown previously that darkly contrasting closed loops that are observed with EBIC in GaAs grown on Si are antiphase domain boundaries (APBs) [9]. The combination of the closed-loop type of contrast observed topographically and the dark contrast observed in EBIC (albeit not necessarily closed loop) indicates that these surface features are due to APBs intersecting the free-surface of the sample. This is verified by cross-section TEM, where APBs can be seen propagating to the GaAs free-surface (Fig. 2). Some APBs, however, appear to terminate within the GaAs film. Moreover, a substantial number ($\sim 10^8\text{ cm}^{-2}$) of threading dislocations are seen to be present in the GaAs epilayer. Many threading dislocations can be observed to go from the Ge epilayer to the GaAs layer.

From a phenomenological point of view it is clear that this $\text{Si}_x\text{Ge}_{1-x}$ 4-layer MLS has not been effective in appreciably reducing the GaAs threading dislocation density, and APBs act as additional nonradiative recombination sites.

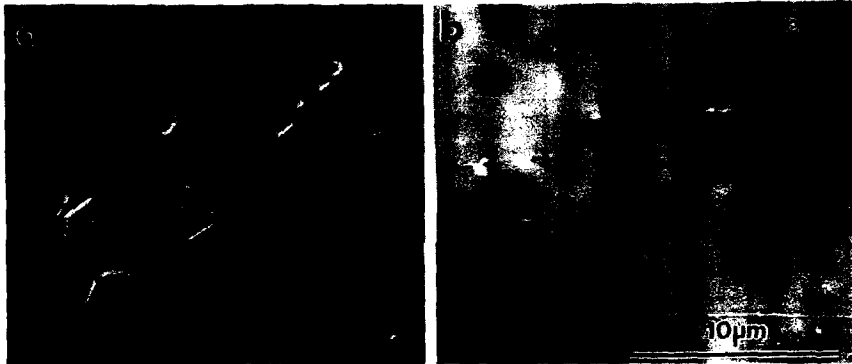


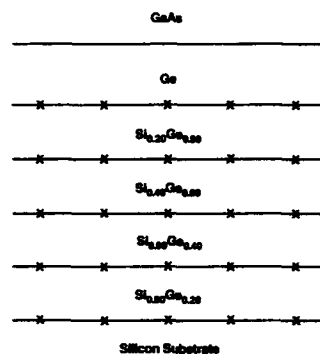
Fig. 1 SEM micrographs from GaAs/4-layer, $0.5\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS/ 4° off-axis Si(100): (a) topographic and (b) EBIC.



Fig. 2 Cross-section TEM from GaAs/4-layer, $0.5\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS/ 4° off-axis Si(100). $1\mu\text{m}$ GaAs on $0.5\mu\text{m}$ Ge on $0.5\mu\text{m}$ $\text{Si}_{0.25}\text{Ge}_{0.75}$ is shown.

$\text{Si}_x\text{Ge}_{1-x}$ MLS consisting of 5 layers were then investigated. This structure is shown schematically in Fig. 3. The lattice mismatch for each layer is reduced to $\sim 0.8\%$. Individual layer thicknesses of $0.5\mu\text{m}$ ($2.5\mu\text{m}$ total $\text{Si}_x\text{Ge}_{1-x}$ MLS thickness) and $1.0\mu\text{m}$ ($5.0\mu\text{m}$ total $\text{Si}_x\text{Ge}_{1-x}$ MLS thickness) were grown on 4° off-axis Si(100) and 6° off-axis Si(100), respectively. After subsequent OMCVD GaAs growth, the topography of the respective surfaces appears different. Fig. 4 shows SEM (topography and etched surfaces) results from these samples. The GaAs grown on 4° off-axis, 5-layer, $0.5\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS on Si(100) shows features indicative of APBs intersecting the GaAs free-surface, consistent with the results presented above. Neither the topographic nor the EBIC images show evidence for APB formation in the GaAs grown on 5-layer, $1.0\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS on 6° off-axis Si(100). We have consistently seen no evidence for APB formation in the GaAs when 6° and 8° off-axis Si(100) wafers are used in conjunction with $\text{Si}_x\text{Ge}_{1-x}$ MLS growth.

Fig. 3 Schematic diagram of GaAs on a 5-layer $\text{Si}_x\text{Ge}_{1-x}$ MLS grown on Si. The "X" signifies misfit dislocations residing in the heteroepitaxial interfaces.



Etching of these samples to assess the defect density was accomplished with A-B etching for 1 min. [10]. SEM examination of the etched surfaces shows that APBs are selectively etched in the GaAs grown on the 5-layer, $0.5\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS on 4° off-axis Si(100) making a dislocation density measurement impractical (Fig. 4). The

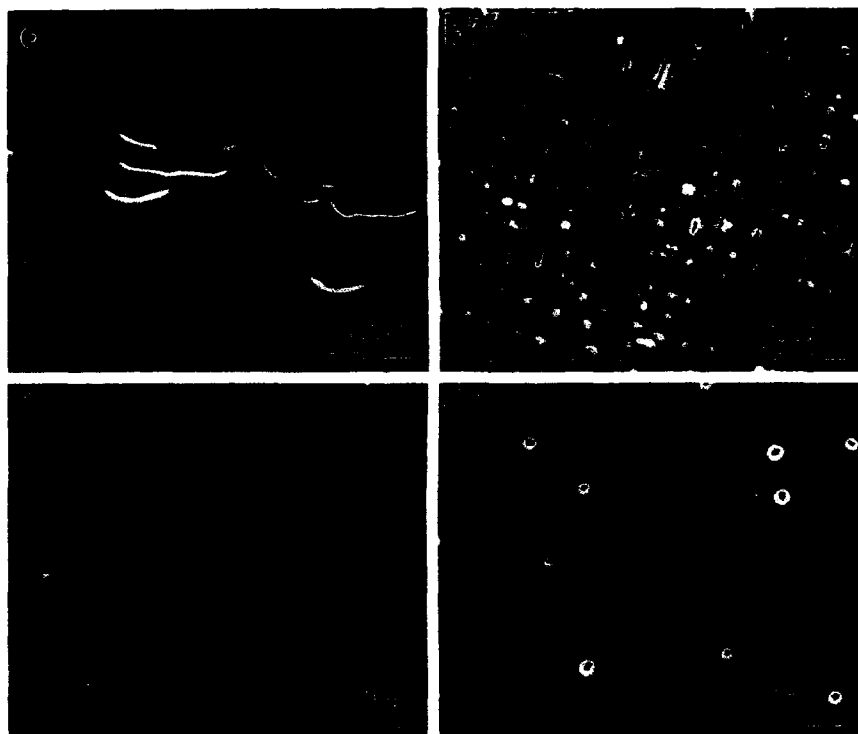


Fig. 4 SEM micrographs from: GaAs/5-layer, $0.5\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS/ 4° off-axis Si(100), (a) topographic and (b) etched; and GaAs/5-layer, $1.0\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS/ 6° off-axis Si(100), (c) topographic and (d) etched.

etched surface of the GaAs grown on the 5-layer, $1.0\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS on 6° off-axis Si(100) shows square, crystallographic etch pits of $\leq 1\mu\text{m}$ size with a density of 10^6 cm^{-2} . Use of the same etching conditions on polished GaAs wafers revealed the same type of crystallographic etch pits with an etch pit density (EPD) of $5 \times 10^3\text{ cm}^{-2}$. Cross-section TEM results from both of these GaAs/ $\text{Si}_x\text{Ge}_{1-x}$ MLS/Si samples are consistent with the above results (Fig. 5). In particular, the threading dislocation density is found to be $\sim 10^7\text{ cm}^{-2}$ for the GaAs grown on the 5-layer, $0.5\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS on 4° off-axis Si(100), whereas the threading dislocation density is $< 10^7\text{ cm}^{-2}$ for the GaAs grown on the 5-layer, $1\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS on 6° off-axis Si(100). The low magnification cross-section TEM image of one of the entire GaAs/5-layer $\text{Si}_x\text{Ge}_{1-x}$ MLS/Si(100) heterostructures also demonstrates that most of the dislocations do indeed reside in the $\text{Si}_x\text{Ge}_{1-x}$ heteroepitaxial interfaces.

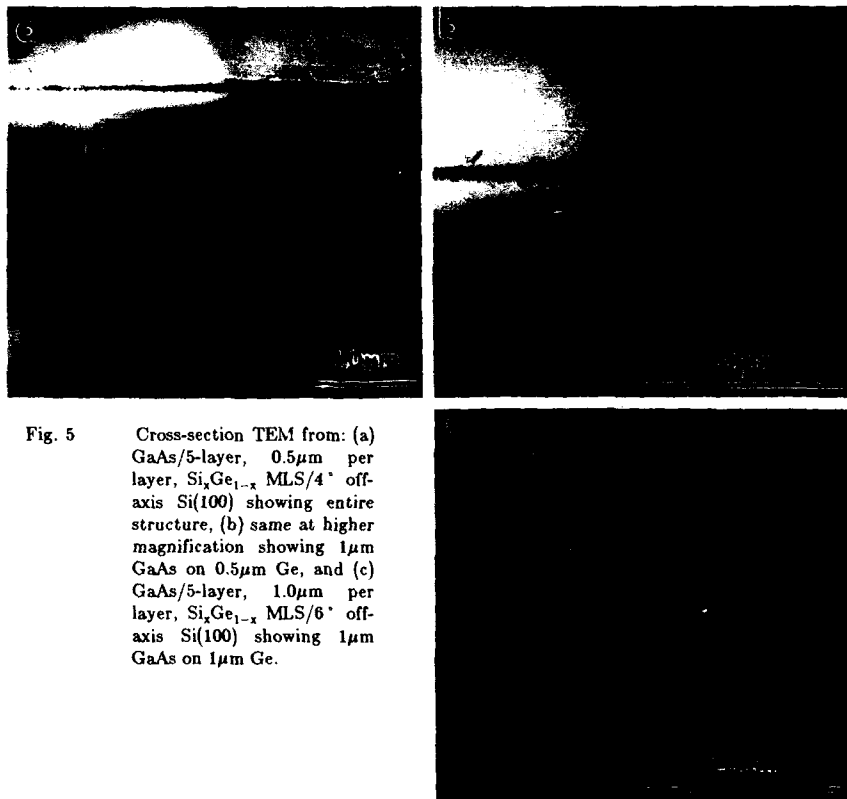


Fig. 5 Cross-section TEM from: (a) GaAs/5-layer, $0.5\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS/ 4° off-axis Si(100) showing entire structure, (b) same at higher magnification showing $1\mu\text{m}$ GaAs on $0.5\mu\text{m}$ Ge, and (c) GaAs/5-layer, $1.0\mu\text{m}$ per layer, $\text{Si}_x\text{Ge}_{1-x}$ MLS/ 6° off-axis Si(100) showing $1\mu\text{m}$ GaAs on $1\mu\text{m}$ Ge.

These results are summarized in Table I. Also included is the full-width at half-maximum (FWHM) of the ambient temperature photoluminescence (PL) spectra. We have found this to be a useful and semiquantitative method to compare different heteroepitaxial GaAs layers [7]. Again, the trend toward a narrower FWHM is observed in the less defective GaAs epilayer.

TABLE I Summary of GaAs/Si_xGe_{1-x} MLS/Si Results

Wafer and MLS Description	PL FWHM (meV)	APBs Present?	EPD (cm ⁻²)	Dislocation Density via TEM (cm ⁻²)
4° off-axis 5-layer 0.5μm per layer	58±3	Yes	—	10 ⁷
6° off-axis 5-layer 1μm per layer	43±3	No	10 ⁶	<10 ⁷

CONCLUSIONS

In the context of using Si_xGe_{1-x} multilayer structures as a buffer between the Si substrate and a GaAs epilayer, we have found that 6° and 8° off-axis (tilted toward [011]) vicinal Si(100) wafers eliminate APB formation. Five-layer Si_xGe_{1-x} multilayer structures have been found to be superior to 4-layer Si_xGe_{1-x} multilayer structures, and somewhat thicker (1.0μm as compared to 0.5μm) individual Si_xGe_{1-x} layers are also beneficial. Although not yet optimized, the basic concept of "confining" the majority of dislocations as misfit dislocations in the Si_xGe_{1-x} heteroepitaxial interfaces has been demonstrated.

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CHARACTERIZATION OF $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ HETEROSTRUCTURES USING
OPTICALLY-DETECTED MAGNETIC RESONANCE

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ABSTRACT

$\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures with varying layer-thicknesses have been characterized using photoluminescence and magnetic resonance detected on photoluminescence. Three of the four samples studied exhibit sharp photoluminescence bands at different energies. For a 120 Å Si/40 Å $\text{Si}_{1-x}\text{Ge}_x$ heterostructure, magnetic resonance of an electron in the Si and of a hole in the $\text{Si}_{1-x}\text{Ge}_x$ layers were observed. These results indicate cross-interface, or Type II, excitonic recombination. Further, anisotropic magnetic resonance spectra indicate the presence of dangling-bond defects in the heterostructures.

INTRODUCTION

The current interest in $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures stems from the success of heterojunction bipolar transistors in this material system and the prospect of optical devices formed from $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures integrated with existing Si technology. The large lattice mismatch and the ability to grow thin layers using MBE provide a great deal of latitude in engineering the band structure of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ superlattices. In particular, structures have been designed and tested for strong optical absorption and emission. Fairly sharp photoluminescence bands have now been observed by many groups [1-5]. However, there is still some uncertainty about the exact physical origin of these bands [6].

This paper describes the characterization of a set of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures using optically-detected magnetic resonance (ODMR). This technique combines photoluminescence with electron paramagnetic resonance to detect the spin-dependent part of a radiative recombination process. ODMR reveals the symmetry and structure of the electron- and hole-states undergoing recombination. ODMR studies of the excited states of donor-acceptor pairs [7], bound excitons [7], and indirect excitons in AlAs/GaAs superlattices [8] have been reported.

The results for $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures can be grouped in three categories. First, three of the samples studied show sharp photoluminescence bands. Second, the ODMR of these bands provides evidence in two of the samples for indirect, or cross-interface, recombination [9,10]. Third, further ODMR results demonstrate the presence of Si and SiGe dangling-bond defects in these structures.

EXPERIMENTAL BACKGROUND

The samples were grown by MBE on (001) Si substrates. Four samples were studied with three having widely different SiGe and Si layer widths (See Table I). The 16 x 4 superlattice was grown at 380 °C and the strained-alloy superlattices were grown at 530 °C. The 120 Å/ 40 Å samples had different Ge mole-fractions in their alloy layers.

The photoluminescence experiments were performed using a SPEX 0.22 m double-grating spectrometer with the slits set to give a resolution of 9 meV for energies around 1 eV. The 476 nm line from a Kr^+ laser was used for excitation since the blue light is better absorbed by a su-

Table I. Sample Parameters

Sample	Buffer Layer		Superlattice			
	%Ge	t	t(Si)	t(SiGe)	%Ge	t(total)
16x4 VA 39	20	2 μ m	16 ML	4 ML	100	3000 Å
45/15 CH 72	0	1000 Å	45 Å	15 Å	40	6000 Å
20% CH 93	0	600 Å	120 Å	40 Å	20	5760 Å
35% CH 79	0	1000 Å	120 Å	40 Å	35	8000 Å

perlattice than the longer wavelengths [9]. Power densities ranged from 0.1 to 1 W/cm². The emission was detected with a Northcoast liquid-nitrogen-cooled Ge photodiode. The sample temperature was 1.6 K.

The ODMR was detected as a change in the intensity of the photoluminescence which was coherent with the switching on and off of 50 to 100 mW of microwave power. Two ODMR spectrometers were used. The first operates at 24 GHz in the Voigt geometry and the second at 35 GHz in the Faraday geometry.

PHOTOLUMINESCENCE RESULTS

Photoluminescence results have been obtained for the energy range from 0.7 to 1.2 eV (See Fig. 1). All four samples show some emission at 1.091 eV from the Si substrate or buffer layer. Below this energy however, the spectra are different for each sample reflecting the different structural parameters of the samples.

The 16 x 4 sample has its highest energy feature at 1.023 eV. This energy has been related to the band structure of this sample in a previous study of Si_mGe_n superlattices [4]. Deeper luminescence is also strong in this sample.

The photoluminescence of the 45/15 sample is strong with sharp features dominating the spectrum. Both the spectrum and the structure are similar to results published very recently for a sample grown by chemical vapor deposition [5]. These authors assigned the higher energy feature to a no-phonon line and the strong, lower energy feature to a TO phonon replica. They attributed the recombination to excitons confined in the strained Si_{1-x}Ge_x wells. The lower-energy emission is considerably weaker than the sharp structure in our 45/15 sample.

The final two samples have the same structure but with different Ge mole-fraction in the alloy layers. The 20 % sample does not exhibit any sharp emission attributable to the superlattice while the 35 % has a sharp peak at 0.870 eV. X-ray analysis of the superlattice satellites to the Si (400) reflection show that the 35 % sample is a better superlattice than the 20 % sample [11]. Both 120/40 samples exhibit broad, deep emission.

ODMR REVEALING THE BAND STRUCTURE

The ODMR experiments were performed to gain further information on the symmetry of the electrons and holes recombining to produce luminescence. Data were obtained at 35 GHz with the magnetic field and the k-vector of the emitted light parallel to the superlattice growth axis (See Figure 2). Filters were chosen to emphasize the highest energy, superlattice-related emission for the three samples which exhibited sharp structure. Despite this filtering, angular rotation studies showed that the broad, negative features below 1 T in the 16 x 4 and 45/15 samples were due to hole cyclotron resonance in bulk silicon. The other features will be discussed separately for each sample.

The 120/40 sample with 35 % Ge layers exhibits a rich and revealing spectrum. The positive resonance near 0.6 T has harmonics at two and three times its field. The resonance position can be related to the Zeeman splitting of the magnetic state through the equation

$$h\nu = g\beta B \quad (1)$$

where h is Planck's constant, ν the microwave frequency, g the Zeeman splitting factor, β the Bohr magneton and B the magnetic field for resonance. Angular studies show that $g = 4.46 \pm 0.05$ for the line near 0.6 T with the field in the [001] and $g \sim 0$ with the field in the plane of the superlattice. From these g -values, the resonance can be uniquely assigned to holes with $M_J = \pm 3/2$ in the $\text{Si}_{1-x}\text{Ge}_x$ layers [9]. The positive resonance near 1.25 T has an isotropic g -value of 1.998 ± 0.001 . This g -value is characteristic of conduction electrons in Si. The electron and hole are linked by their positive (luminescence-enhancing) character, their dominance of the spectrum in this sample, and by an anisotropy in the intensity of the electron line. These facts indicate Type II, or cross-interface, recombination for the 35 % sample with the hole in the alloy layer and the electron in an adjoining Si layer.

The 45/15 sample exhibits many of the features just described for the 120/40 sample. There is a strong negative (luminescence-quenching) feature near $B = 1.25$ T which is related to dan-

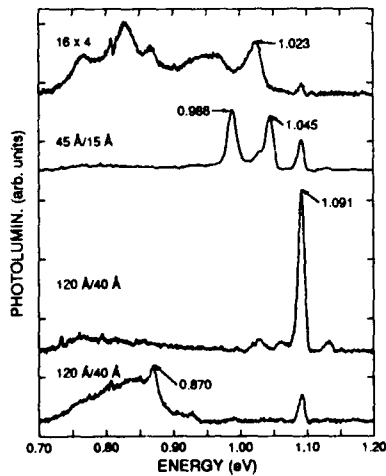


Figure 1. Photoluminescence spectra taken at 1.6 K for the four samples. Prominent peaks are labelled by their energies in eV.

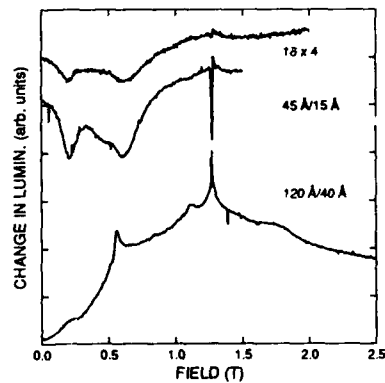


Figure 2. ODMR spectra taken in Faraday geometry at 35 GHz with $B \parallel [001]$. The spectral range was limited by a $1.3 \mu\text{m}$ short-pass filter for the 16 x 4, a $1.0 \mu\text{m}$ long-pass for the 45/15, and a $1.3 \mu\text{m}$ long-pass for the 120/40.

gling bonds and will be discussed in the next section. However, a portion of the response with $B \parallel [001]$ is positive like the electron line in the 120/40 sample. A hole resonance can also be revealed from the following analysis. The data for the 45/15 sample shown in Figure 2 was taken in a spectral range which included the bulk Si emission (the 1.091 eV line). In a separate experiment, the ODMR of that line alone was obtained (See Figure 3). Subtraction of the two spectra removes the hole cyclotron resonance and reveals a positive line at 0.55 T with a g -value of 4.68 ± 0.10 . The positive lines may be the hole and electron from the interface-bound exciton in this sample. The increased linewidths may indicate an increased exchange interaction between the electron and hole due to the smaller well-widths.

For the 16 x 4 sample, only the slightest hint of a resonance remains near 1.25 T. There are a number of possible reasons why the ODMR might not be detected for this sample. For example, the confinement of the electron in the Si layers may be lost for very narrow layers. It is also possible that the recombination becomes so fast that resonance in the excited state is not possible without stronger microwave fields than are available.

ODMR REVEALING DANGLING BONDS

A second type of ODMR has been detected in these samples which differs from the ODMR attributed to bandedge electrons and holes in two respects. First, the signals are often negative. This luminescence-quenching response indicates a recombination process which is competing with, and hence drawing from, the radiative process under observation. Second, the resonance positions indicate g -values very close to that of the free-electron ($g = 2.0023$). This implies that the orbital angular momentum of the electron or hole is quenched, which is often the case for states bound by localized point defects.

The ODMR of the 45/15 sample at 24 GHz in the field-region around the free-electron (and excitonic electron) contains many distinct resonances (See Figure 4). The strongest feature is the

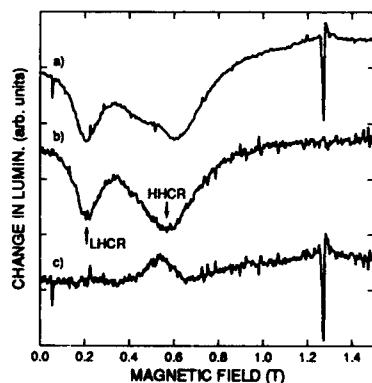


Figure 3. Data subtraction for the 45/15 sample to remove the Light- and Heavy-Hole Cyclotron Resonance. A spectrum (b) taken on the bulk-Si exciton (1.091 eV) is subtracted from data (a) taken with a 1.0 μm long-pass filter to give a difference-spectrum (c). A hole resonance is evident near 0.55 T.

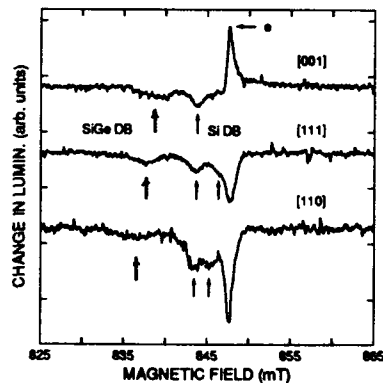


Figure 4. ODMR taken in Voigt geometry at 24 GHz for three directions of magnetic field. Anisotropic dangling-bond spectra, indicated by vertical arrows, are seen in addition to the excitonic electron line.

electron line which changes from positive to negative as the field is rotated from the superlattice axis ([001]) to the [110]. This indicates the coupling of the electron to an anisotropic hole. At lower fields, there are negative resonances from localized defects. One anisotropic set of lines was observed near the electron line with a particular amplitude and linewidth. The g -tensor for this set is axial about a bond direction ($\langle 111 \rangle$) with $g_{\parallel} = 2.0002 \pm 0.0002$ and $g_{\perp} = 2.0071 \pm 0.0002$. This spectrum can be assigned to Si dangling bonds by comparison with results obtained in neutron-irradiated Si [12]. At still lower fields, there is a second set of anisotropic lines, which are broader and weaker than the first set. Although some of the lines are obscured by the Si-dangling-bond resonances, the broader lines can be modeled by a second g -tensor which is axially symmetric about $\langle 111 \rangle$ with $g_{\parallel} = 2.007 \pm 0.001$ and $g_{\perp} = 2.023 \pm 0.001$. Increasing linewidth and g -shift with increasing Ge mole-fraction have been reported for dangling bonds in amorphous SiGe alloys [13,14]. Because this spectrum in the superlattice has broader lines and larger g -shifts than the Si dangling bonds, it is assigned to dangling bonds in the $\text{Si}_{1-x}\text{Ge}_x$ layers.

The 120/40 sample with 20 % Ge shows the strongest ODMR from Si dangling bonds. Since it exhibits the weakest X-ray satellites, no sharp bands in photoluminescence, and no conduction- or valence-band features in ODMR, it appears to be of poorer quality than the 35 % sample.

The g -tensors for the dangling bonds indicate equal numbers of defects with the broken bond in each of the $\langle 111 \rangle$ directions. This is consistent with the fact that the samples were grown on [001] substrates and hence there is no preferred [111] direction.

CONCLUSION

The application of ODMR to $\text{Si}_{1-x}\text{Ge}_x$ heterostructures has provided information in two areas. First, the photoluminescence from a 120/40 sample, and also possibly a 45/15 sample, has been attributed to a Type II, or cross-interface, exciton. Second, dangling bonds have been detected in both Si and $\text{Si}_{1-x}\text{Ge}_x$ regions of a 45/15 superlattice.

These results suggest some interesting future work. ODMR can be used to study the effect of annealing on both the excitonic emission and the dangling bonds. This would help to clarify the role of the interface on the excitonic recombination and to determine the exact location of the dangling bonds.

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RESIDUAL STRAIN AND DEFECT ANALYSIS IN AS GROWN AND ANNEALED SiGe LAYERS

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ABSTRACT

In this paper we address the problem of producing SiGe buffer layers of acceptable quality for the growth of symmetrically strained SiGe structures. Initially we consider SiGe layers grown to well beyond the metastable critical thickness and examine the degree of residual strain both as-grown and post-anneal. The defect levels in metastable SiGe layers following high temperature anneal were also studied. A buffer layer was grown consisting of stacked metastable SiGe layers each of which is annealed in situ prior to the growth of the next layer and terminating with a 0.45 SiGe alloy. This produces nearly fully relaxed 1.15 μm thick structures with threading dislocation densities of $4 \times 10^6 \text{ cm}^{-2}$. Limited area growth on Si suggests that elastically relaxed material free of both threading and misfit dislocations can be produced.

Introduction

The growth of relaxed SiGe buffer layers is required to allow maximum flexibility for adjusting the strain in Si/Ge and Si/SiGe structures [1]. Control of the in-plane lattice constant enables strain induced variation of the valance and conduction band discontinuities at the heterojunction between Si and SiGe layers [2,3]. Of interest also is the growth of symmetrically strained structures which in the case of Si/Ge monolayer superlattices offer prospects of a quasi-direct band gap material compatible with Si technology. The major problem associated with growth of such buffer layers has been the presence of a very high density of threading dislocations, (typically 10^{10} cm^{-2}), which are associated with the misfit dislocations formed along the buffer/Si substrate interface needed to relax the epitaxial layer. These threading dislocations can detrimentally affect the properties of structures grown on the buffer.

Thick SiGe Layers

Early work on symmetrically strained structures involved growth on "thick" SiGe buffer layers - well above the metastable critical thickness (t_{cm}) [4] - so that significant strain relaxation occurs aiming at giving an in-plane lattice constant midway between that of the overlying composite layers. It was found however that there was significant residual strain remaining in the layers, although this has not as yet been well quantified. In this work X-ray diffraction taken at two reflections (004) and (113) has been used to deduce the in-plane lattice parameter and also that along the growth direction for a number of thick SiGe layers [5]. Figure 1 shows the relationship between the normalized thickness (thickness/metastable critical thickness) and the degree of relaxation and includes layers with compositions varying between 22 and 90%. Two of the data points are from material from a different laboratory [6]. Although the data is sparse it suggests a reciprocal relationship between these two

parameters which is independent of composition [7]. It seems also that the films as grown were in a quasi-equilibrium relaxed state since on annealing at 850°C for one hour there were only small changes in the strain. It seems possible that the relaxation occurs during growth to a point which is limited by dislocation interactions. We do not expect such a relationship to hold for layers grown closer to the metastable critical thickness.

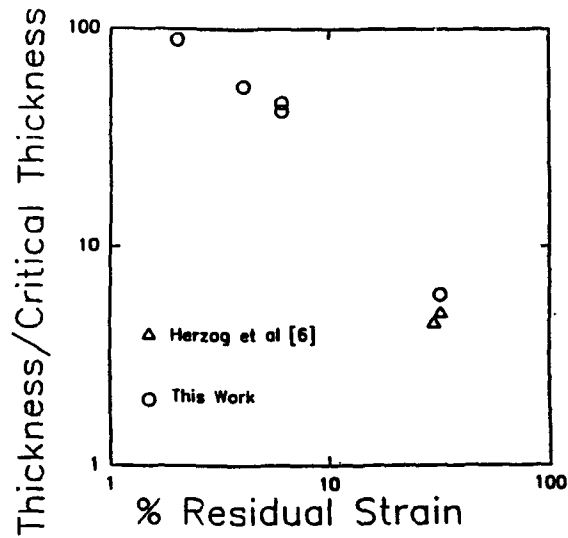


Fig 1 Plot of (thickness/metastable critical thickness) vs. residual strain for SiGe layers with composition ranging from 22 to 90%.

Annealed layers

An alternative method of achieving a relaxed layer is to anneal layers grown to thicknesses below the metastable critical thickness but above the equilibrium critical thickness [8]. A range of $\text{Si}_{1-x}\text{Ge}_x$ samples with x varying from 0.05 to 0.3 was subject to an anneal at 850°C for 1 hour. X-ray diffraction enabled determination of the degree of residual strain in the annealed layers and thus misfit dislocation density. Fig 2 shows how the misfit dislocation density is related to the normalised thickness (layer thickness/equilibrium critical thickness). It indicates that to grow a layer that will relax significantly upon annealing it must be grown to beyond 10-20 times its equilibrium critical thickness. Conversely, if a device structure is to remain nearly fully strained throughout subsequent processing then it should only be grown only to 3-4 times its equilibrium critical thickness for these uncapped layers.

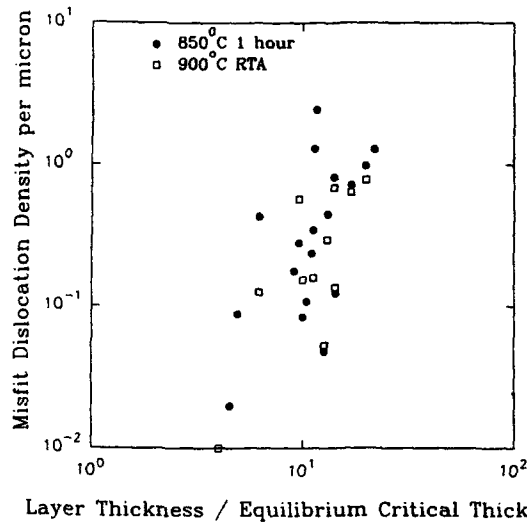


Fig 2 Plot showing the post-anneal misfit density plotted against the normalised thickness for metastable SiGe layers.

Examination of the misfit dislocations associated with these annealed layers via defect etch and Nomarski microscopy Fig 3 showed that the layers of thickness $< 0.5 t_{cm}$ had misfit dislocations which were surprisingly long, in fact too long to measure by the defect reveal technique (ie > 2 mm).

Fig 3 Defect etch pictures of SiGe layers

Fig 3a SiGe_{0.3}, $t = 6t_{cm}$, no anneal

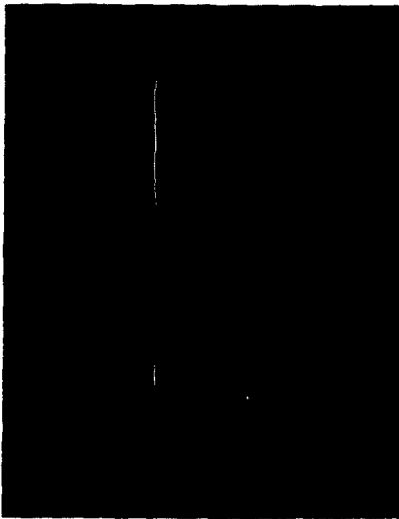


Fig 3b SiGe, $t = 0.62t_{cm}$ annealed



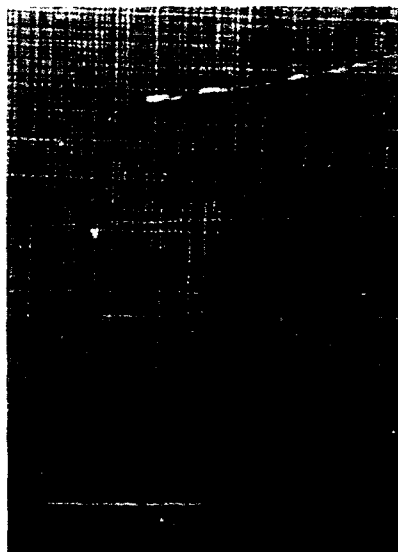
Fig 3c SiGe_{0.123}, $t = 0.38t_{cm}$, annealed

Fig 4 Defect etch of buffer structure

The layers with less as-grown strain produce longer misfit dislocations after anneal. As each misfit dislocation has two threading dislocations associated with it, elongation of the threading dislocations will lead to a reduction in the density of threading dislocations. Thus for the layer in Fig 3a grown well beyond critical thickness we see that the misfit dislocation length is $2\mu\text{m}$ whereas for sample in Fig 3c the misfits are greater than 2mm in length which leads to a reduction of threading dislocation density of at least 3 orders of magnitude.

Similar experiments were carried out with rapid thermal annealing of the same sample set at 900°C for six seconds and the data is included in Fig 2. This anneal schedule produces similar effects to the long anneal and again the misfit dislocations were found to be in excess of 2mm in length for most of the samples.

Step Graded Buffer Layers

The growth/anneal schedule for this buffer layer is given in Table 1. A $0.3\mu\text{m}$ thick SiGe_{0.13} was first deposited on the Si buffer and then subject to a twenty minute 850°C in-situ anneal. This should predominantly relax the layer producing long misfit dislocations and consequently giving a low threading dislocation density. On top of this layer a $0.2\mu\text{m}$ SiGe_{0.22} layer was grown which, because, of the relaxed state of the underlying layer should have a strain equivalent to approximately a SiGe_{0.15} layer. This was then annealed and the process continued through to the deposition of the final layer - SiGe_{0.45}, which was not annealed.

Table 1

Composition % Ge	Thickness microns	850°C Anneal
13	0.35	Yes
22	0.2	Yes
31	0.2	Yes
40	0.2	Yes
45	0.2	No

Fig 4 shows the layer after defect etching. Long misfit dislocations can be clearly seen and a misfit dislocation length of 0.2 mm is found for the final interface which corresponds to a threading dislocation density of $5 \times 10^6 \text{cm}^{-2}$. This is comparable to the threading dislocation density of $4 \times 10^6 \text{cm}^{-2}$ obtained from defect etch observations.

Following a further anneal which would normally take place in the MBE system the residual strain in the layer was measured by X-ray diffraction using the two [113] reflections. Comparison of the two curves obtained indicated the structure was 90% relaxed.

Growth on Mesa Columns

A new approach to producing relaxed SiGe layers is to use limited area growth and allow the SiGe layer to expand in the x and y directions as well as in the growth direction. This enables the SiGe to relax elasticity and by that means reduce strain fields which cause misfit dislocation formation and the associated threading dislocations. Theoretical support for elastic relaxation of small area samples has been given by Luryi and Suhir [9]. They derive an expression for the maximum radius of a pad upon which SiGe can be grown to infinite thickness without the creation of misfit dislocations, which for SiGe_{0.15} alloy gives 5 μm .



Fig 5 SEM picture of two mesa islands, 2 and 4 μm across with 0.75 microns of SiGe deposited on top.

Plasma etching was used to produce very steep sided $2.5\mu\text{m}$ high Si mesa islands on Si substrates. This enables deposition of areas of SiGe which are detached from the SiGe covering the remaining substrate as shown in Fig 5. Growth on such Si columns may also aid elastic relaxation of SiGe overgrowth.

The mesas consisted of two groups, one being square mesas ranging in size from 1 to $1500\mu\text{m}$ across, the second group consisting of rectangular islands $200\mu\text{m}$ long and ranging in width from 3 to $150\mu\text{m}$. $\text{SiGe}_{0.15}$ was grown to $0.75\mu\text{m}$ in thickness, well beyond its metastable critical thickness. The misfit dislocation density was then determined using a defect etch and Nomarski microscopy (see Fig 6).

For the square islands a gradual reduction in misfit dislocation density was observed as the island size was reduced and for islands $< 10\mu\text{m}$ across no misfit dislocations were seen. This can be explained by a lack of nucleation sites required for the production of the misfit dislocations [10]. However examination of the misfit dislocation density on the rectangular islands provides evidence that elastic relaxation is also occurring on the small mesas. Whereas misfit dislocations running perpendicular to the long dimension were evident on all the rectangular mesas, there are no misfit dislocations running parallel to this dimension for the $5\mu\text{m}$ wide mesas. This implies that structures of such finite extent are able to relax elastically (perpendicular to the x direction) making the strain fields insufficient to generate misfit dislocations.

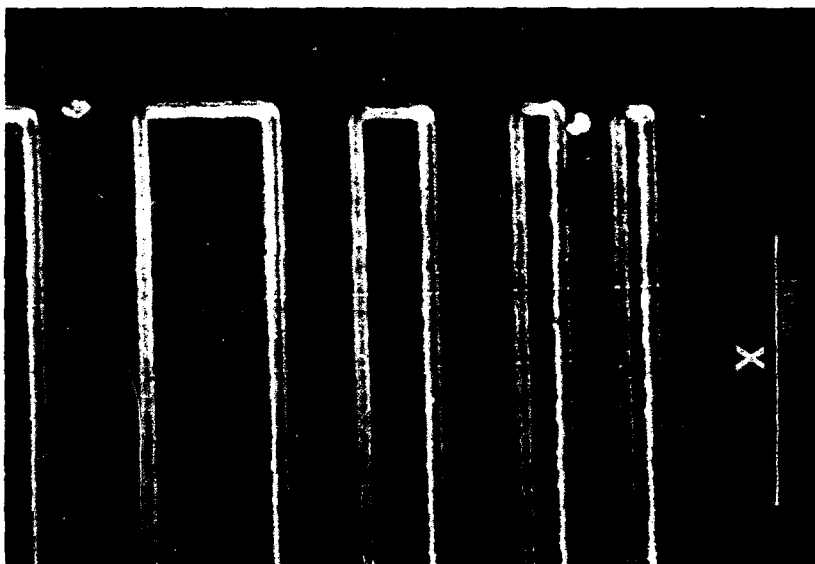


Fig 6 Defect etch of rectangular mesa islands showing misfit dislocations crossing but not running along the long islands.

Conclusions

We have considered two methods for reducing the threading density in SiGe buffer layers both of which have been remarkably successful. The first technique involving step grading and high temperature anneals and showed a significant improvement of the buffer layer quality which may with further refinement of the annealing regime allow buffer layers to be grown with the same threading dislocation densities, (10^4 cm^{-2}) as seen with the single annealed layers.

The second buffer technique offers the possibility of mesa islands free of both threading and misfit dislocations, again with a lattice parameter between Si and Ge, upon which devices could be fabricated. There is an additional benefit in that novel devices could be considered where the strain and therefore the electronic properties vary depending upon whether the carriers are travelling along a long thin mesa structure or across it. The possibility of electrical characterisation of the threading dislocations also exists as a structure can be grown with dislocations present in one direction and not the other. It may also prove possible to combine both techniques such that long misfit dislocations terminate at the edge of the mesa instead of with a threading dislocation.

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GROWTH OF $\text{Si}_{1-x}\text{Ge}_x$ STRAINED LAYERS USING ATMOSPHERIC-PRESSURE CVD

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ABSTRACT

The objective of this paper is to demonstrate the epitaxial growth of SiGe strained layers using atmospheric-pressure chemical vapor deposition (APCVD). We have grown SiGe layers with various thicknesses and Ge concentrations at temperatures ranging from 800-1000°C. The samples were studied using a variety of methods, including transmission electron microscopy (TEM), high resolution X-ray diffraction (HRXRD) and Raman spectroscopy (RS). Both HRXRD and RS results indicate that samples with about 10% Ge and a thickness of about 1000 Å are almost fully strained. TEM analyses of these samples indicate a film defect density less than $10^5/\text{cm}^2$. SIMS results indicate that the oxygen concentration in the epitaxial layers is lower than that found in CZ substrates.

Our analyses also indicate that as-grown epitaxial Ge layers several microns thick have a defect density less than $10^7/\text{cm}^2$. The relatively low defect density in both SiGe and Ge layers grown on Si has been attributed to far higher dislocation glide velocity at the relatively elevated growth temperatures employed in CVD and to very good growth cleanliness.

INTRODUCTION

Molecular beam epitaxy (MBE) has been the primary method used to grow epitaxial SiGe layers [1-5]. Other methods also being studied for GeSi and Ge layer growth include ultrahigh vacuum chemical vapor deposition (UHV/CVD), [6,7] rapid thermal processing CVD (RTPCVD) [8], limited reaction processing (LRP) [9,10], and solid phase epitaxy (SPE) [11]. The growth temperature for most of these techniques is below 700°C. Many of these films are metastable, and the strain is relaxed upon annealing above the growth temperature [12,13]. Very little attention has been given to APCVD, a high temperature process (800-1000°C).

We have investigated the high temperature growth of thin and thick SiGe layers and thick Ge layers using APCVD. Our results focus on the growth of SiGe strained layers with 10% Ge using high temperature APCVD. The oxygen content of these epilayers, determined using secondary ion mass spectroscopy (SIMS), is below the oxygen level found in the CZ substrate of an oxygen ion implanted silicon sample ($<5 \times 10^{17}/\text{cm}^3$). SiGe layers with greater thicknesses and/or higher Ge concentrations begin to (partially) relax. Pure Ge layers a few microns thick are fully relaxed and have relatively low defect densities (around $5 \times 10^6/\text{cm}^2$). This technique appears to be very attractive because of its simplicity and high growth rate (thus short growth time), especially for thick SiGe layers which are useful as a buffer for MBE grown superlattices or for waveguides [14]. In addition, Ge-on-Si grown by this technique could be used as a substrate for growing III-V compounds.

EXPERIMENTAL PROCEDURE

SiGe/Si heteroepitaxial layers were grown on Si(100) wafers in an Applied Materials AMV-1200 vertical epitaxy reactor at temperatures ranging from 800-1000°C with a growth rate of up to 1 $\mu\text{m}/\text{min}$. Silane (SiH_4), trichlorosilane (SiHCl_3), and germanium tetrachloride (GeCl_4) were used as Si and Ge sources. SiGe layers were 0.03 - 4 μm thick and had Ge concentrations from 0-20 atomic percent. A 1000 \AA thick Si cap was grown on some of the thin SiGe samples. Epitaxial Ge layers were grown on Si(111) and Si(100) wafers cut on axis and cut 2° off the [111] axis.

The epitaxial layer thicknesses and Ge concentrations were determined using Rutherford backscattering spectroscopy (RBS). Plan-view transmission electron microscopy (TEM) and cross-sectional TEM (XTEM) were used to determine the defect densities in the epitaxial layers, and channeling was used to determine the crystalline quality. The strain in the layers was measured using cross-sectional electron diffraction and high resolution X-ray diffraction (HRXRD), and Raman spectroscopy (RS). Finally, oxygen impurities were evaluated using SIMS.

EXPERIMENTAL RESULTS

Thin SiGe (Strained) Layers with 900 \AA Si Cap

A. Crystalline Quality and Strain

Figure 1 shows an XTEM of a sample with a SiGe layer about 1200 \AA thick and a Ge concentration of about 8%. The Si cap layer is about 900 \AA thick. Both SiGe/Si interfaces are abrupt and easily distinguishable. RBS/channeling measurements have shown that the aligned spectrum from the sample shows good channeling throughout with no visible de-channeling ledge caused by defects. Measured minimum yield values from the various layers of the sample range from 3-4% [15]. Plan-view TEM analysis over a $10^4 \mu\text{m}^2$ area on the Si top layer revealed no threading dislocations, indicative of a defect density less than $10^8/\text{cm}^2$, at worst, $10^9/\text{cm}^2$. The spacing between misfit dislocations at the Si(Sub)/SiGe interface as determined using this method is 3.5 μm [16]. However, a Schimmel etch indicates that the spacing is about 20 μm [17].

High resolution X-ray diffraction was performed with a Blake Industries diffractometer, capable of 0.5 arcsec angular step-size and equipped with a four-crystal monochromator supplying Cu $K\alpha$ radiation. Figure 2 shows X-ray rocking curves of sample T338 for the (004) Bragg reflection and the asymmetric (224) reflections for high and low incident angles obtained using the procedure described in reference 18. These results clearly indicate that the SiGe layer of #T338 is almost 100% strained. Table I gives the values of the lattice parameters perpendicular and parallel to the surface.

Raman spectroscopy studies were done using spectroscopic techniques described previously [19]. The RS experiments were performed at room temperature with the 514.5 nm line of an Ar⁺ laser. An oblique angle scattering geometry was used. The spectral features were independent of the laser power and generally a few hundred mW were used with the laser polarization parallel to the plane of incidence.

The Si-Si Raman shift for $\text{Si}_{1-x}\text{Ge}_x$ is shown in Figure 3. The solid curve shows the pseudo alloy shift with Ge composition [20], and the dashed line shows a fully strained SiGe layer on a Si substrate [21]. Samples #N370 (10 μm) and #1026E (2 μm) are fully relaxed, #T338R (120nm) is almost fully strained, and #T339R (150nm) is about 80% strained. The RS and HRXRD results correspond for the two latter samples (T338 and T339), and are also consistent with cross-sectional electron diffraction results [15].

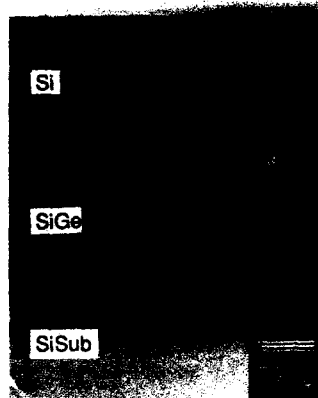


Figure 1. XTEM of SiGe Strained Layer Shows a Si/SiGe/Si Heteroepitaxial Structure with Sharp, Smooth Interfaces.

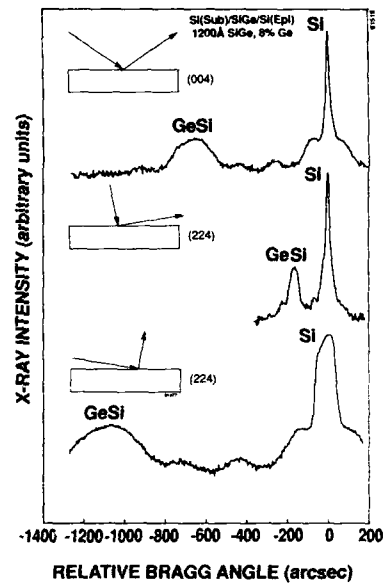


Figure 2. X-Ray Rocking Curves for Sample T338 (1200 Å SiGe, 8% Ge) Indicate that the Layer is Almost Fully Strained.

Table I. Strain in SiGe Layers as Determined Using X-Ray Rocking Curves. (See Figures 1, 2, and 5.)

Sample	a_L	a_I	a_s	R
T338	5.456	5.431	5.445	0
GER1023E	5.464	5.430	5.449	0

B. Oxygen Impurity

SIMS was applied to determine the existence of oxygen in thin SiGe films. A Perkin Elmer 6300 secondary ion mass spectrometer with a Cs^+ ion source was used. An oxygen ion-implanted silicon sample was used as a reference to determine the oxygen content in our samples. Figure 4 shows the oxygen and Ge profiles for a typical sample (#T338). A comparison of these results with SIMS results of the silicon standard indicate that the oxygen content detected in the SiGe films was lower than that in the CZ Si substrate.

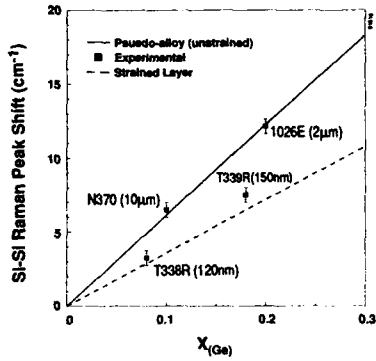


Figure 3. Si-Si Raman Peak Shift as a Function of Ge Concentration.

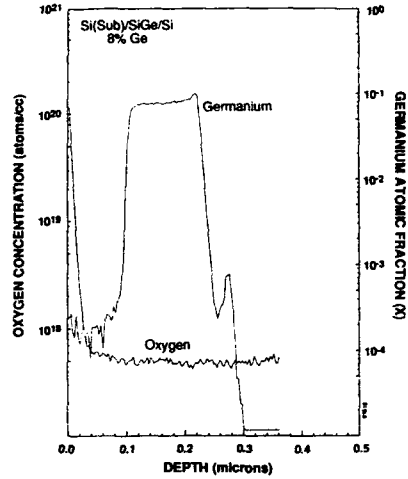


Figure 4. SIMS Depth Profile of Sample #T338 (see Figs. 1 and 2)

SiGe Thin Film Without a Silicon Cap

Figure 5 shows an XTEM of sample (#GER1023) with a Ge concentration of 10% and a thickness of 800 Å. No defects can be observed in this region. Plan-view TEM analysis of large areas is in progress. We also studied this sample using HRXRD to determine the strain in the SiGe layer. The results, shown in Table I, indicate that the SiGe layer is almost fully strained.



Figure 5. XTEM of SiGe Layer 800 Å Thick with a Ge Concentration of 10% (#GER1023).

Epitaxial Ge on Si

Samples with Ge layers epitaxially grown to 0.5 μm and 4.5 μm thick on Si(100) and Si(111) wafers were studied using cross-sectional and plan-view TEM. Plan-view TEM results indicate a defect density in the $10^6/\text{cm}^2$ range. Figure 6 shows typical TEM results for Ge epitaxially grown on Si(111).



Figure 6. Plan-view TEM of the Surface of a 4 μm Thick Ge Epitaxial Layer.

CONCLUSION

We have demonstrated the high temperature growth of SiGe alloys and pure Ge layers on Si substrates using APCVD. HRXRD and RS results indicate that SiGe about 1000 Å thick and about 10% Ge is almost fully strained and has a defect density less than $10^6/\text{cm}^2$, as determined by plan-view TEM. Plan-view TEM indicates the existence of 60° type dislocations [22] at the Si(Sub)/SiGe interface with an average spacing of 3.5 μm . Using the measured spacing and the measured threading dislocation density, the length of interfacial misfit dislocations is over 6 nm [16].

The oxygen concentration of this material is lower than that of the Si substrate, indicating that no oxygen is incorporated into the epitaxial layer during growth. Our results are consistent with those of J. Hoyt *et al.* [9], which suggest no oxygen incorporation above 800°C in a low pressure CVD system.

On the basis of HRXRD data alone, capping the silicon thin film has not influenced the presence of strain. On the other hand, J. Hoyt *et al.* report an effect on dislocation spacing for samples annealed with a Si cap [9]. However, we will verify our HRXRD data using large area survey plan-view TEM results.

The possible explanation for the low defect density in this material is described elsewhere [23], where it was anticipated that the increased glide velocity in CVD-grown material (as compared to MBE material) is responsible for the production of lower defect material. Another possible explanation is that dislocation nucleation sites operate differently in high temperature CVD than in MBE. Nucleation is clearly suppressed in these materials, indicating that very clean growth is possible with CVD.

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Fabrication of Bond and Etch Back Silicon on Insulator Using SiGe-MBE and Selective Etching Techniques

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ABSTRACT

Undoped thin layer silicon on insulator has been fabricated using wafer bonding and selective etching techniques using an MBE grown $\text{Si}_{0.7}\text{Ge}_{0.3}$ layer as an etch stop. Defect free, undoped 200-350 nm silicon layers are routinely fabricated using this procedure. A new selective silicon-germanium etch has been developed that significantly improves the ease of fabrication of the BESOI material.

INTRODUCTION

Silicon on insulator (SOI) technology is evolving as the older silicon on sapphire technology is replaced by newer technologies capable of supporting smaller geometry devices. Several technologies are competing to produce the next generation of SOI materials, and among the most important are silicon implanted with oxygen (SIMOX) and bond and etch back silicon on insulator (BESOI). There is also a subset of BESOI technologies under study that uses a combination of thinning techniques and different etch stops. The etch stops currently under study in the BESOI community include a heavily boron doped silicon layer¹ and a silicon-germanium alloy^{2,3}.

This work has focused on BESOI fabrication because the buried oxide found in SIMOX material is not well behaved in a radiation environment. As a result, large threshold voltage shifts are experienced following irradiation by ionizing sources. BESOI utilizing a SiGe etch stop is preferred over boron doped silicon because of defects induced in the silicon device layer by the presence of the boron etch stop when the silicon epilayer is grown on top of it. Residual electrically active elements (boron) following the etch stop removal is also undesirable.

EXPERIMENTAL

A schematic of the BESOI fabrication process is shown in figure 1. Prime wafers are fabricated using molecular beam epitaxy (MBE) from Si(100) substrates that are cleaned chemically prior to loading into the MBE system by a modified Shiraki procedure. The oxide was removed *in vacuo* by heating to 800°C in a 0.1 Å/sec silicon flux. The structure was fabricated by growing the following layers: a 20 nm silicon buffer layer, a 60 nm $\text{Si}_{0.7}\text{Ge}_{0.3}$ alloy etch stop layer, and a 200-350 nm silicon epilayer.

Thermal oxides are grown on both the MBE prime wafer (850°C) and the handle wafer. The oxides are both hydrolyzed in an $\text{NH}_3:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solution, and then

stacked together oxide to oxide. The bonding between the two wafers was established at 50°C, and set at 850°C for 30 minutes³.

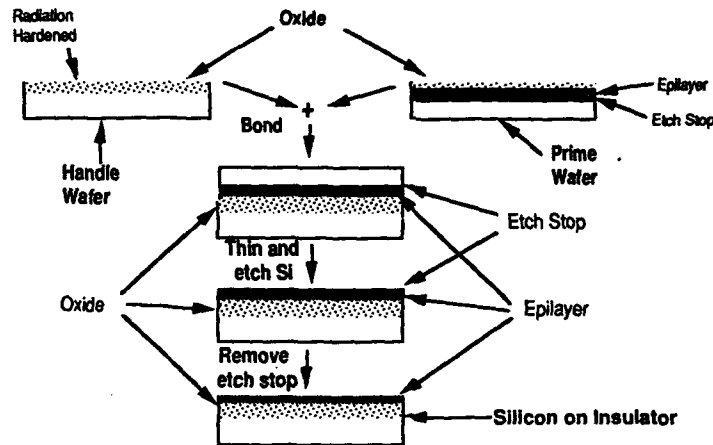


Figure 1. Schematic representation of bond and etch back silicon on insulator fabrication.

The back side of the bonded prime wafer was thinned to 200-350 nm by a combination of mechanical thinning, non-contact polishing, and followed by selective etching³. The process is as follows: An initial standard grind and polish brought the silicon epilayer thickness to 25 microns. Precision machining was then used to reduce the film thickness to 3 microns. Machining damage was removed by a non-contact polishing resulting in a silicon film around 1-2 microns thick with an unpitted surface. Further thinning used a selective silicon etch composed of 100 g. KOH, 4 g. $K_2Cr_2O_7$, 100 ml. propanol, and 400 ml. H_2O_2 ³. Finally, the $Si_{0.7}Ge_{0.3}$ alloy etch stop layer was selectively removed by a $HNO_3:H_2O:HF(0.5\%)$ solution, 40:20:5 vol:vol⁴.

RESULTS AND DISCUSSION

The focus of the present work is the development of selective etching techniques and the fabrication of bond and etch back silicon on insulator. The first etch must remove the silicon remaining following the mechanical thinning of the prime wafer bonded to the substrate, stopping at the $Si_{0.7}Ge_{0.3}$ etch stop layer. The second etch must remove the $Si_{0.7}Ge_{0.3}$ etch stop layer, leaving a polished silicon device layer.

As noted above, bonding of the wafers was performed successfully at 850°C. Although this temperature was sufficiently high to cause some relaxation of the alloy etch stop layer, it did not have a negative impact on the stopping capability of the etch stop as discussed below. In addition, dislocations formed by relaxation in the

etch layer did not propagate into the epitaxial layer as shown by plan view transmission electron spectroscopy². This sets an upper limit of dislocations in the epilayer at 10^4 cm^{-2} .

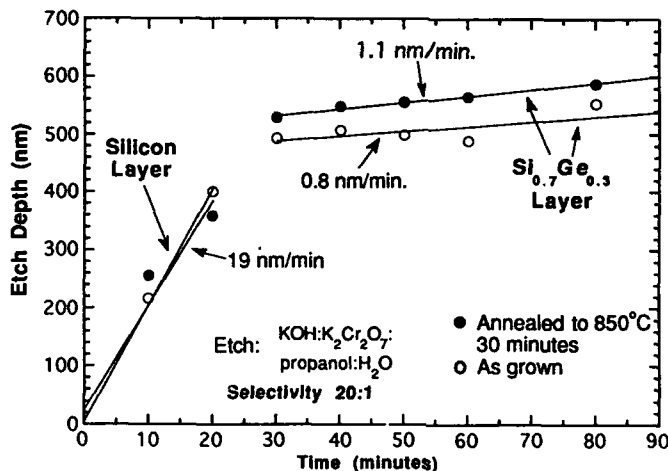


Figure 2. Silicon selective etch.

The selective silicon etch showed the behavior indicated in figure 2. The slope of the steep curves on the left side of the plot is the etch rate of the silicon layer. The rate obtained was 19 nm/minute and did not change following heat treatment to 850°C as shown in the plot. The shallow curves on the right give the etch rates through the alloy etch stop layer and were 0.8 and 1.1 nm/minute for the as grown alloy layer and the layer heated to 850°C for 30 minutes respectively. The selectivity defined as the ratio of etch rates of the silicon and alloy layers was around 20.

The selective removal of the $\text{Si}_{0.7}\text{Ge}_{0.3}$ alloy etch stop layer is shown in figure 3. The slope of the left side of the curve gives the etch rate through the etch stop layer which was 22 nm/minute. The etch rate through the underlying silicon layer was 1.8 nm/minute, giving a selectivity for the etch stop removal of 13. The alloy etch had the desirable result of leaving the surface polished.

Following the removal of the etch stop layer, the finished silicon on insulator material is obtained. The BESOI layers were characterized with transmission electron spectroscopy (TEM) and spreading resistance profiling. In figure 4 is shown a cross sectional transmission electron micrograph of a 200 nm silicon on insulator film. Spreading resistance profiling showed the fabricated semiconductor layers to have a residual doping level of 8×10^{14} p-type, resulting from the

background of the MBE system³. Thus we have the basis for fully depleted BESOI technology.

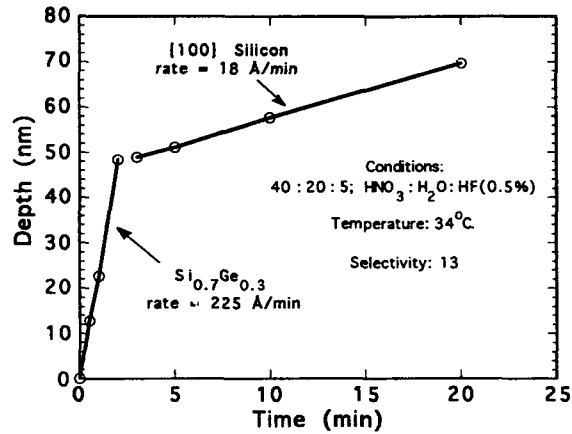


Figure 3. SiGe (30% Ge) selective etch.

Future work will focus on improving the selectivity of the silicon and SiGe etch stop selective etches. MOS devices have been fabricated, and their performance will soon be reported. The improvement in radiation tolerance compared to other SOI technologies will also be explored.

CONCLUSION

The use of an epitaxial Si_{0.7}Ge_{0.3} layer etch stop in the fabrication of BESOI has been developed. This technique utilizes thermal and deposited oxides to form the buried oxide layer, thereby enabling the use of standard radiation hardening techniques in the growth of the buried oxide. The use of an epitaxial Si_{0.7}Ge_{0.3} layer as an etch stop results in a defect free and undoped silicon on insulator film. The silicon film can be grown to any thickness desired, and silicon films in the 200-350 nm range are routinely fabricated.

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Figure 4. Silicon on insulator fabricated by bond and etch back using a SiGe alloy as etch stop.

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PART IV

GeSi Optical Properties

SI-BASED PHOTONIC DEVICES BY MBE.

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ABSTRACT

The prospect of efficient electroluminescence and photodetection in Si-based heterostructures has stimulated considerable interest in recent years. Si-based optoelectronic devices would allow monolithic integration of mature Si technology with optical signal processing. However, Si and epitaxial $\text{Si}_{1-x}\text{Ge}_x/\text{Si}(100)$ alloys are indirect semiconductors and band structure perturbations are necessary to enhance luminescence efficiencies to practical levels. In this review we consider the relative success of the various approaches used to obtain efficient luminescence from Si based heterostructures after first considering the optical properties of Si grown by MBE and doped by several techniques. Exciton binding centers such as isoelectronic defect complexes, zone folding in atomic layer superlattices, e.g. Si_mGe_n , and rare earth doping, e.g. Er in Si and $\text{Si}_{1-x}\text{Ge}_x$ alloys are discussed. The internal quantum efficiencies for the above processes will be compared in both electroluminescence and photoluminescence together with the prospects for room temperature light emission. The twin requirements of band structure engineering and superlattice crystal quality extend the challenge to the materials scientist / crystal grower further into the nanoscopic regime. It is a formidable task involving the controlled removal of non-radiative point defects and complexes, controlled introduction of radiative centers, and simultaneous maintenance of coherent interfaces without misfit dislocation injection. Recent progress in our study of intense photoluminescence (wavelength range 1.2 - 1.7 μm) from random $\text{Si}_{1-x}\text{Ge}_x$ alloys ($0.53 > x > 0.06$) grown by MBE, a 1.5 μm $\text{Si}_{0.82}\text{Ge}_{0.18}/\text{Si}$ LED and a novel $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ optoelectronic switch will be highlighted.

INTRODUCTION

Intense activity has been focussed on the optical and electronic properties of Si and $\text{Si}_{1-x}\text{Ge}_x$ alloys in the last 5 years. Fig.1 schematically illustrates the functionality presently available to the optoelectronic circuit designer using Si-based materials. Hitherto, the most success has been realised in an electronic device, the SiGe/Si heterojunction bipolar transistor [1]. The other components necessary for a monolithic Optoelectronic Integrated Circuit (OEIC) have also been demonstrated with varying quantum efficiencies; the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ digital optoelectronic switch (DOES device) [2] and the p-i-n diode [3] illustrate possibilities for optical detectors, resonant tunneling in SiGe / Si double barrier diodes (holes [4], electrons [5]) provides the potential for a high frequency (>100GHz) oscillator, the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$, $\lambda \approx 1.5\mu\text{m}$ LED[6], Si (C) [7] and Si (Er) LED's [8] which show some promise for efficient light emission at room temperature. $\text{Si}_{1-x}\text{Ge}_x$ alloy and superlattice waveguides (optimized for 1.3 or 1.5 μm) are readily fabricated to act as conduits for optical signals in a Si-based OEIC[9]. Furthermore, the possibility of optical amplification or stimulated emission through rare earth (eg. Er, Nd) doping of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ waveguides is discussed below[10].

It should be emphasized that the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ HBT is the most successful and mature [1] device in Fig. 1. It has the potential to enhance the high frequency performance of Si bipolar technology ($f_t \sim 100\text{GHz}$) and would be an essential component of a monolithic Si OEIC.

There have been many approaches toward efficient light emission from indirect Si and epitaxial SiGe alloys. Isoelectronic centres such as Be [11] and S [12] and others including C, In, Cu, Li, Tl and Se provide binding sites for excitons which then undergo a radiative transition characteristic of the centre. This approach has been only moderately successful in $\text{Si}_{1-x}\text{Ge}_x$ alloys and Si, although orange and yellow room temperature LED's have been fabricated using the same technique in GaAsP doped with nitrogen[13]. Defect complexes such as those in irradiated C doped Si [7] exhibit sharp features in photoluminescence and electroluminescence (an LED) has been demonstrated at low temperatures. However, quantum efficiencies in Si remain low ($\sim 10^{-4}$) and room temperature luminescence has proved elusive.

Porous Si is presently of some interest since mesoporous Si layers (pedestal/pore width 2 - 50nm) exhibit visible (red) photoluminescence at room temperature [14] when stimulated by green or blue incident laser light. Although electroluminescent devices compatible with conventional Si processing appear unlikely.

Atomic layer superlattices, Si_mGe_n , have also been the subject of many theoretical and experimental studies in recent years [15]. In our laboratory, however, no evidence for direct transitions (due to zone folding or otherwise) or photoluminescence uniquely ascribable to Si_mGe_n layers has been obtained. In contrast, intense luminescence from thick random $\text{Si}_{1-x}\text{Ge}_x$ alloy layers and $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ multilayers in the wavelength range 1.2 to $1.7\mu\text{m}$ has been observed [16] and a $1.5\mu\text{m}$ LED [6] has been demonstrated which operates at temperatures up to $\sim 100\text{K}$.

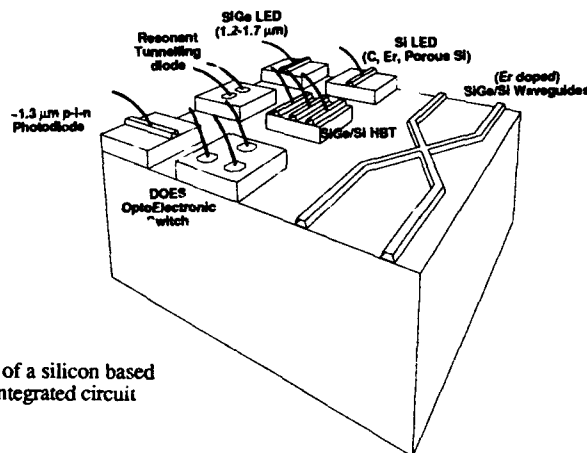


Fig. 1 Schematic illustration of a silicon based (all epitaxial) optoelectronic integrated circuit (OEIC).

The above methods of band structure perturbation present considerable technological challenges to the crystal grower. The simultaneous introduction of radiative centres and controlled removal of point defects and complexes must be accomplished while maintaining low extended defect densities ($< 10^3\text{ cm}^{-2}$). Coherent, misfit dislocation-free interfaces are also essential for photonic devices. The vigilant crystal grower must also take cognizance of the characteristic luminescence from extended defects such as dislocations which have been well documented in Si [17] and $\text{Si}_{1-x}\text{Ge}_x$ alloys [18]. Furthermore it must be stressed that efficient optical devices can be fabricated only in materials containing few non-radiative centres. It is therefore essential to first establish the integrity of the epitaxial layers of both Si and $\text{Si}_{1-x}\text{Ge}_x$ alloys deposited by techniques such as MBE and make comparisons with low temperature chemical vapour deposition (eg RTCVD) and other CVD based techniques. First we describe a photoluminescence study of MBE Si, undoped and doped in-situ with As and B, then we consider rare earth doping of MBE Si and $\text{Si}_{1-x}\text{Ge}_x$ through coevaporation of Er from a Knudsen cell. Finally, we discuss recent progress with $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ optoelectronic devices.

PHOTOLUMINESCENCE SPECTROSCOPY OF MBE SILICON

Photoluminescence (PL) is routinely used in the assessment of III-V MBE material and PL is emerging as a characterization tool for MBE Si homo- and hetero-epitaxy [19, 20]. MBE Si and $\text{Si}_{1-x}\text{Ge}_x$ have been particularly difficult to analyze using optical techniques due to persistent contamination problems [21] associated with electron beam evaporation, high point defect densities due to the low growth temperatures $\approx 500^\circ\text{C}$ and difficulties in dopant incorporation. We illustrate below that all these problems have been overcome and that homoepitaxial Si grown by MBE is comparable with bulk Czochralski Si [22] and high temperature CVD Si [23] as determined by PL spectroscopy. Furthermore, this bodes well for Si based photonic and electronic devices synthesized by MBE since PL is a stringent test of material quality [22] as it is effectively a measure of carrier lifetime.

The growth methods for Si and $\text{Si}_{1-x}\text{Ge}_x$ strained layers on both Si and Ge substrates have been described earlier [24]. Briefly, the combined Si and Ge growth rate was 0.5 nms^{-1} and the growth temperature was maintained constant in the range $400\text{--}600^\circ\text{C}$ for $\text{Si}_{1-x}\text{Ge}_x$ alloys and

varied from 500-750°C for Si epitaxy. Photoluminescence was excited by the 514 nm line of an Ar⁺ laser from samples in liquid He and analyzed with a BOMEM DA3.02 FTIR spectrometer using a cooled Ge⁺ detector. PL measurements were also made at temperatures up to ~100K.

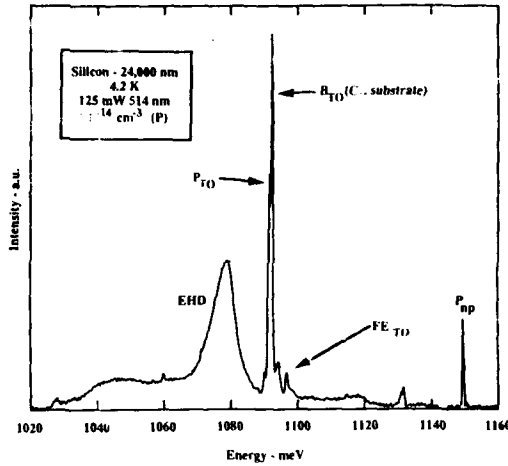


Fig. 2 Photoluminescence spectra from a nominally undoped MBE Si epitaxial layer.

Fig. 2 shows the 4.2K PL spectra from a 24 μm thick Si homoepitaxial layer with no intentional doping deposited by MBE at 700°C. The residual impurity was identified as P from the energies of the characteristic no phonon and TO phonon replicas (boron doped Czochralski Si substrate, $N_A = 2 \cdot 10^{15} \text{cm}^{-3}$). The carrier concentration was confirmed by Hall measurements to be (n-type) $2.7 \times 10^{14} \text{cm}^{-3}$. The ratio of intensities of bound exciton (phosphorus) to free exciton peaks (P_{np} : FE_{TO}) of Fig. 2 following McL Colley and Lightowers[25] (after correcting the FE_{TO} intensity to allow for the contribution from the B doped substrate) provides a similar estimate of the phosphorous level ($1 \times 10^{14} \text{cm}^{-3}$). The good agreement between Hall and PL estimates for the carrier concentration suggest minimal compensation and low levels of other impurities.

The PL spectrum in Fig. 2 was obtained at a power density of $\sim 1 \text{W/cm}^2$ at 4.2K and exhibits an electron hole droplet. The observation of this electron-hole condensate implies [22] a large exciton mean free path between capture sites, consistent with the low background doping level and low concentrations of other traps or electrically active impurities in the MBE layer.

Fig. 3 presents PL spectra from 5 μm thick Si layers following the incorporation of As during MBE using in-situ low energy (100, 500 and 1000eV) ion implantation for As⁺ ions at three growth temperatures 500°C, 650°C and 800°C [19]. Minimal influence of incident ion energy (in the range 100-1000eV) on Si(As) quality was evident from PL data. However, the dominant influence of growth temperature is clear from the rapid degradation in 500eV As⁺ PL spectra in the series 800°C, 650°C to 500°C. The As incorporation probability remains constant with temperature (\approx unity). The deterioration in PL spectra at lower growth temperatures (the poor S/N and rising background intensity to energies below 1050meV) is due only to the high density of quenched-in point defects (eg excess vacancies and interstitials). At growth temperatures below $\sim 600^\circ\text{C}$ the optical quality of Si and $\text{Si}_{1-x}\text{Ge}_x$ alloys rapidly deteriorates [19,20] but bulk-like optical properties may be restored by a single post-growth Rapid Thermal Anneal (RTA) treatment (typically 650°C, 100s) as shown below (Fig. 6) for a MBE Si epitaxial layer doped by in-situ ion doping at 500°C with 100eV B⁺ ions.

Fig. 4 shows PL spectra from MBE Si epitaxial layers deposited under identical conditions to the Si:As of Fig. 3 but doped now with low energy ($\sim 100 \text{eV}$) B⁺ ions [20]. The incorporation of boron is closely similar to the As⁺ case, exhibiting only a weak dependence of optical quality on incident B⁺ ion energy. The dominant growth parameter is again substrate temperature. Boron may also readily be incorporated through B coevaporation illustrated here using a novel elemental boron source[26]. Fig. 5 depicts the PL characteristics of elemental B-doped Si epitaxial layers

grown under otherwise identical conditions to those of Figs. 3 and 4. The Si substrate temperature was again varied from 500°C, 650°C to 800°C maintaining a doping level in the range 5×10^{15} to $2 \times 10^{16} \text{ cm}^{-3}$. The same trend with growth temperature is followed as with the ion doped layers but in the MBE Si layers of Fig. 5 only the thermal energies of incident B and Si atoms are involved. This observation suggests that Si MBE at temperatures below $\sim 600^\circ\text{C}$ results in the incorporation of traps (probably point defect complexes) inherent to the low epitaxial growth temperature, which have a deleterious effect on both optical and electronic [20] properties.

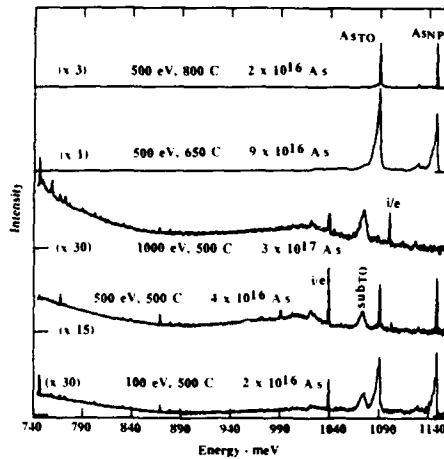


Fig. 3 Photoluminescence (PL) spectra from in-situ low energy As^+ ion doped Si MBE layers.

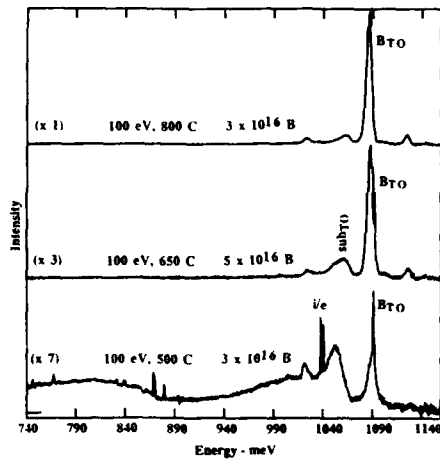


Fig. 4 PL Spectra from B^+ ion doped Si MBE layers deposited at 500°C, 650°C and 800°C.

Thus boron may be incorporated equally well using the doping technique of either Fig. 4 or 5 (ion doping or coevaporation). Similar bound multi-exciton complex features are produced in each case associated with the self-annihilation of excitons at boron sites. The dominant feature in both series of spectra is the transverse optic phonon replica B_{TO} arising from the phonon assisted recombination of excitons in the lightly B doped ($\sim 10^{16} \text{ cm}^{-3}$) epitaxial layer. The broader features at 1120, 1060 and 1025 meV arise from the recombination of electrons and holes in the degenerately doped substrate. Clearly, either dopant incorporation technique is capable of producing MBE Si with photoluminescence characteristics similar to high temperature CVD Si [23] or Czochralski-Si doped to an equivalent level. This observation implies that the MBE Si investigated in this study contains low concentrations of non-radiative centres or traps unlike earlier reports on MBE Si [21]. Deep levels such as transition metal impurities or point defect complexes even at modest concentrations ($\leq 1 \times 10^{13} \text{ cm}^{-3}$) would compete for exciton capture and lead to non-radiative recombination [22].

Fig. 6 illustrates how post-growth RTA annealing of Si MBE layers of apparently poor optical quality (due to a high point defect density inherited from low temperature $\sim 500^\circ\text{C}$ growth step) may recover PL integrity. In Fig. 6 the PL spectrum from a MBE Si layer grown at 500°C and ion beam doped with 100eV B^+ ions is compared with the identical sample after post growth annealing at 800°C. The sharp features and rising background at energies $< \sim 1050 \text{ meV}$ can all be attributed to point defect complexes [eg 22]. However, the annealed spectrum is indistinguishable from Si MBE material grown at 800°C and these bound multi-exciton features are comparable to those observed from B doped bulk Czochralski Si.

In summary, high quality homoepitaxial Si has been epitaxially grown by MBE. Doping in the range 10^{16} to 10^{20} cm^{-3} was carried out either p-type (B) or n-type (As) with in-situ low

energy B^+ or As^+ ions or by using a novel thermal B source. Si MBE epitaxial layers exhibit comparable optical properties to B doped Czochralski Si or high temperature CVD Si homoepitaxy [23]. Our observation of donor and acceptor bound exciton luminescence indicates the absence of impurities and defect complexes which would compete for exciton capture and may lead to non-radiative decay processes as was observed by Lightowers [21] in an earlier survey of MBE Si. Strong luminescence from MBE homoepitaxial Si is however not observed in Si with dislocation densities of $>10^6\text{cm}^{-2}$ or in epitaxial Si deposited at temperatures lower than $\sim 600^\circ\text{C}$ (although $\sim 100\text{s}$ RTA anneals $\sim 650^\circ\text{C}$ fully recover bulk-like bound exciton PL).

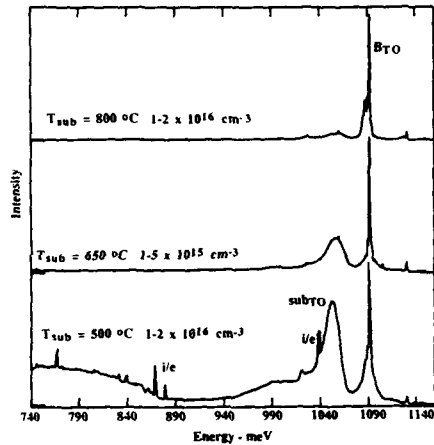


Fig. 5 PL spectra from Si MBE layers doped with coevaporated B at 500°C , 650°C and 800°C .

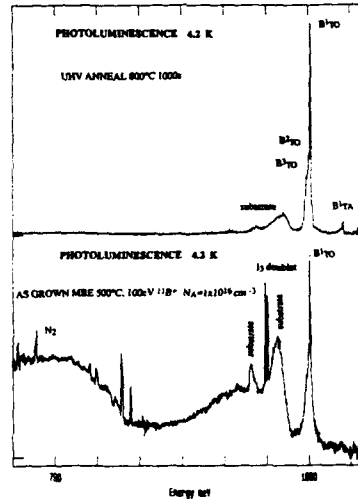


Fig. 6 PL spectra from in-situ B^+ doped Si MBE layer as grown at 500°C and after annealing at 800°C .

ERBIUM INCORPORATION IN Si AND $\text{Si}_{1-x}\text{Ge}_x$ BY MBE

Er doped Si homoepitaxial layers have shown photoluminescence and Er doped Si diodes have demonstrated weak electroluminescence. This work of Ennen and co-workers showed how *in-situ* implantation at high energies (350 keV) of Er in MBE Si led to Er^{3+} photoluminescence [27] and an LED [8] which showed weak electroluminescence at temperatures up to 77K. Almost simultaneously, rare earth doped silica waveguides appeared in ~ 1985 and have since been developed as high gain optical fibre amplifiers [10]. In particular, Er doped optical fibres are attractive since the dominant emission wavelength of $\sim 1.54\mu\text{m}$ coincides with the low loss/minimum dispersion region of SiO_2 . Er doped III-V compound semiconductors have recently received considerable attention [28]. In addition, the structural [29], electrical [30] and optical characteristics of ErSi_2 have been studied in both polycrystalline and epitaxial forms on Si (100) substrates. Rare earth silicides have low electrical resistivity, low Schottky barrier height on n-type Si, together with some interesting magnetic [30] and optical properties. However, to date, no study of Er / ErSi_2 solubility, Er incorporation or structural perfection of Er doped Si grown by MBE has been carried out. Similarly, the optical properties of Er in coherently strained $\text{Si}_{1-x}\text{Ge}_x$ alloys have not been investigated.

The Er^{3+} ($4f^{11}$) energy level diagram of Fig. 7 illustrates how incident light energy (eg. $\lambda = 980\text{nm}$) may be absorbed by a ground state Er^{3+} ion and subsequently re-emitted as $1.54\mu\text{m}$ luminescence by intra $4f^{11}$ transitions. The internal transfer of energy to the level at $1.54\mu\text{m}$ occurs quickly but the $1.54\mu\text{m}$ state is long lived and acts as a reservoir prior to decay to the ground state. Hence, it is conceivable that stimulated emission of $1.54\mu\text{m}$ light exhibiting gain, as

demonstrated by Er doped optical fibre amplifiers, could be realised in an analogous way in a $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructure. There are several spectral bands available for "pumping" or resonantly exciting the Er^{3+} ion. In SiO_2 fibres the most efficient processes have been experimentally determined as the 980nm band and the 1.46 - 1.49 μm band. Although these wavelength ranges may be accessible through external optical sources; efficient excitation at these energies, for example by impact ionization in an electroluminescent $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ device, poses a considerable problem to the device designer and materials engineer.

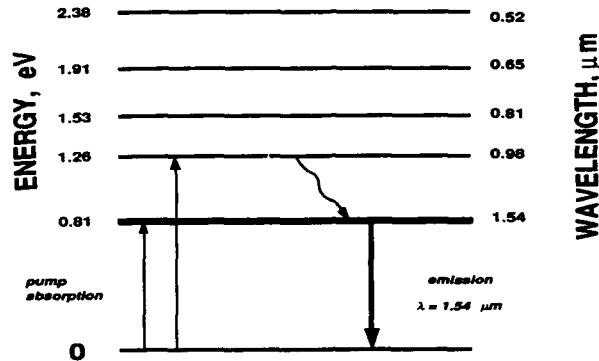


Fig. 7 Energy level diagram of erbium showing 1.54 μm emission.

In the present study, molecular beam epitaxy (MBE) has been used to incorporate (by coevaporation) Er in Si, Ge and $\text{Si}_{1-x}\text{Ge}_x$ alloys and SLS's grown on both Si and Ge (100) substrates. The Er concentration was varied from $\sim 10^{17}\text{cm}^{-3}$ to $5 \times 10^{21}\text{cm}^{-3}$ as measured by SIMS and RBS ion channeling. Cross-sectional TEM was used to determine crystal perfection and detect the onset of silicide formation (ErSi_2 precipitation) as the Er level was increased stepwise through the solubility limit. Electrochemical CV and SIMS depth profiling revealed the electrical activation of Er^{3+} as a function of Er concentration and MBE growth parameters. Photoluminescence was used in the optimization of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}:\text{Er}$ heterostructures and MBE growth parameters.

The Er doped $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layers were grown in a conventional (VG Semicon V80) MBE apparatus utilizing e-beam evaporation for Si and Ge [24], and a standard Knudsen cell for coevaporation of elemental Er. The Er doping level was varied by increasing the Er Knudsen cell temperature from 800°C to 1200°C, while maintaining the Si growth rate constant at $\sim 5\text{\AA s}^{-1}$. Cross sectional TEM was carried out on conventionally ion thinned specimens in a Philips EM430. Compositional depth profiling was performed by SIMS in a Cameca IMF 4F using either Cs^+ or O^+ and extracting positive secondary ions.

The XTEM micrographs in Fig. 8 illustrate two Er doping staircases showing the morphological changes as the solid solubility limit is exceeded at growth temperatures of 500°C and 700°C by increasing the Er to Si flux ratio, stepwise, maintaining other growth parameters constant. Fig. 8 also reveals the difference in morphologies of ErSi_2 precipitates appearing during epitaxial growth at 500°C and 700°C. At the growth temperature of 700°C the ErSi_2 appears as platelets on (111) Si habit planes with orientation relationships (111) Si// (0001) ErSi_2 and (422) Si// (1010) ErSi_2 [30]. The lower substrate temperature of 500°C leads to a similar estimate of Er solid solubility $\sim 10^{19}\text{cm}^{-3}$ but the ErSi_2 morphology forms a random distribution of spheroidal precipitates $< 20\text{ nm}$ in diameter. The Si crystal perfection at both substrate temperatures is excellent, even after extensive precipitation through the preceding layers. However, since the silicide is $\sim 1.5\%$ mismatched to Si misfit strain relaxation occurs once the critical thickness, h_c , for ErSi_2 on Si is exceeded [31] (the equilibrium h_c for ErSi_2/Si is only $\sim 6\text{ nm}$). Exceeding h_c causes misfit dislocation injection as can be seen in Fig. 8 where dislocations initiated in the uppermost Er doped layers propagate threading dislocations which extend into the Si capping

layer. Electrochemical CV profiling of the doping superlattices of Fig. 8 revealed an almost constant, low carrier density $< 10^{16} \text{ cm}^{-3}$ even though the Er concentration increased from $\sim 10^{18} \text{ cm}^{-3}$ to $5 \times 10^{21} \text{ cm}^{-3}$. This suggests a low ionization level for Er into the Er^{3+} state. In all subsequent photoluminescence experiments the Er level was maintained below the Er solid solubility limit ($\sim 5 \times 10^{18} \text{ cm}^{-3}$) in Si and $\text{Si}_{1-x}\text{Ge}_x$ alloys to avoid problems with precipitation and misfit strain relaxation.

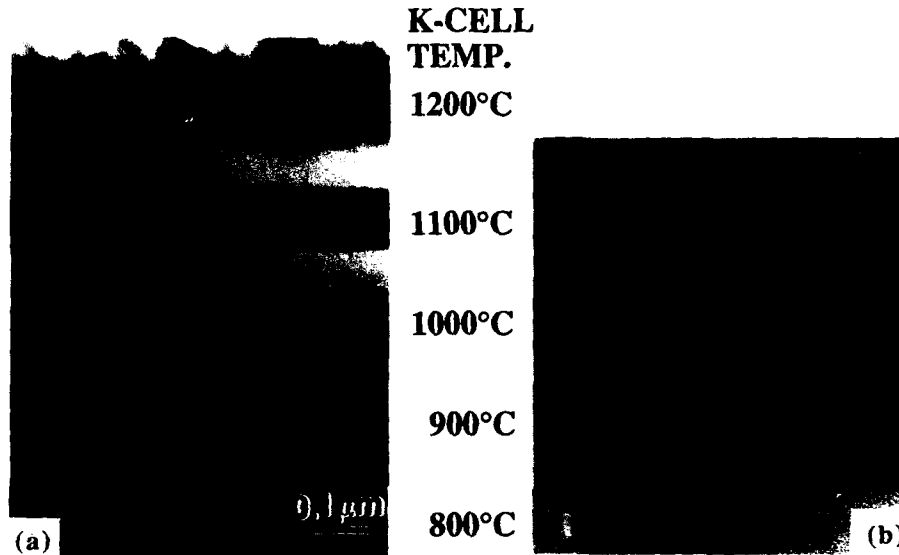


Fig.8 Cross sectional TEM micrographs showing five levels of Er concentration after coevaporation during Si MBE (a) $T_g = 500^\circ\text{C}$ (b) $T_g = 700^\circ\text{C}$.

The photoluminescence spectra in Fig.9 compare luminescence from Er doping (Er concentration $5 \times 10^{18} \text{ cm}^{-3}$) in a Si homoepitaxial layer, a coherently strained $\text{Si}_{0.9}\text{Ge}_{0.1}$ alloy layer and a uniformly Er doped 40 period $\text{Si}_{0.75}\text{Ge}_{0.25}/\text{Si}$ superlattice. Fig. 9 (a) shows PL from Er doped Si with a high energy peak at 805 meV ($1.54 \mu\text{m}$) and several minor peaks to lower energy characteristic of Er^{3+} ion as observed by earlier workers[8,27] from Er implanted Si. The minor PL peaks at lower energy are due to discrete transitions between the weakly crystal field split spin-orbit levels of Er^{3+} , $^4I_{13/2}$ to $^4I_{15/2}$. Comparison of Figs. 9(b) and (c) with Fig.9(a) illustrates the modification of the PL spectrum due to the lattice location of Er in a strained $\text{Si}_{1-x}\text{Ge}_x$ host crystal lattice versus Si. The dominant peaks in Fig.9(b) and (c), are split possibly due to crystal field effects. Furthermore, several well defined features to lower energy are present in the $\text{Si}_{1-x}\text{Ge}_x$ PL spectra (absent from the Si:Er spectrum) which reflect the symmetry of the tetragonally strained lattice and are likely due to the weak interaction of 4f electrons with the tetragonally strained SiGe crystalline environment.

Fig. 10 shows photoluminescence as a function of PL temperature for the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ SLS of Fig 9 (c). The bound multi-exciton features in the 4.2 K spectrum of Fig. 10 (c), due to exciton diffusion into the B doped substrate, indicate that exciton capture in the epitaxial layers is incomplete. The substrate peaks decay rapidly with increase in PL analysis temperature while the Er related luminescence persists to temperatures in excess of $\sim 100\text{K}$. This suggests that larger exciton binding energies are involved in the capture and energy transfer processes associated with Er luminescence.

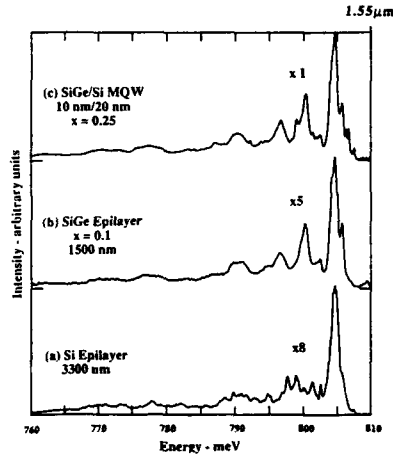


Fig. 9 PL spectra from $5 \times 10^{18} \text{cm}^{-3}$ Er epitaxially incorporated by MBE at 500°C in (a) Si, (b) $\text{Si}_{0.9}\text{Ge}_{0.1}$ alloy and (c) a $\text{Si}_{0.75}\text{Ge}_{0.25}/\text{Si}$ SLS

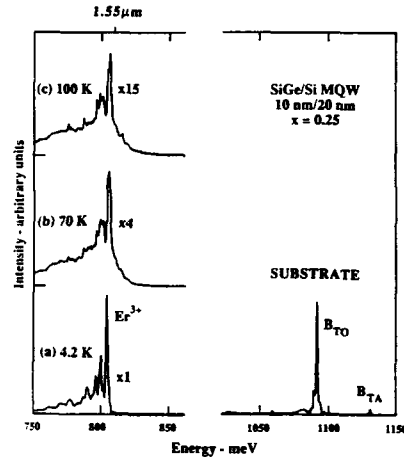


Fig.10 PL spectra from an Er doped $\text{Si}_{0.75}\text{Ge}_{0.25}/\text{Si}$ SLS for three PL temperatures.

PHOTOLUMINESCENCE FROM $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ GROWN BY MBE, RTCVD AND CVD

Fig. 11 presents PL spectra from an unstrained (fully relaxed) $\text{Si}_{0.82}\text{Ge}_{0.18}$ alloy grown by conventional CVD ($T_g = 1000^\circ\text{C}$), a coherently strained $\text{Si}_{0.82}\text{Ge}_{0.18}/\text{Si}$ SLS grown at $\sim 625^\circ\text{C}$ by RTCVD [32] and a $\text{Si}_{0.75}\text{Ge}_{0.25}$ Si SLS [16] grown by MBE using conventional electron beam evaporation (from solid sources), MBE growth temperature $\sim 450^\circ\text{C}$. The PL spectrum from the high temperature CVD $\text{Si}_{1-x}\text{Ge}_x$ layer is closely similar to the PL data of Weber and Alonso [33] for polycrystalline bulk-like $\text{Si}_{1-x}\text{Ge}_x$ crystals grown by liquid phase epitaxy. The PL spectrum of Fig. 11(b) from an RTCVD deposited [32] $\text{Si}_{0.82}\text{Ge}_{0.18}/\text{Si}$ SLS exhibits qualitatively similar near-band-edge features comparable with PL data of the unstrained alloy of Fig. 11(c) but shifted to lower energy due to the biaxial compression from misfit strain. The PL spectrum from the MBE grown $\text{Si}_{0.75}\text{Ge}_{0.25}/\text{Si}$ SLS in Fig. 11(a) [16] however, exhibits a more intense, broader peak (FWHM ~ 80 meV) and the peak energy is ~ 120 meV below the established band gap of tetragonally strained $\text{Si}_{1-x}\text{Ge}_x$ [3]. The PL features of Fig. 11 are typical of layers deposited by MBE, CVD and low temperature CVD techniques obtained from several laboratories.

The bandgap versus Ge concentration plots in Fig. 12 summarize the PL data illustrating that $\text{Si}_{1-x}\text{Ge}_x$ PL peak energy depends on x , the strain tensor, quantum confinement and growth technique. The open circle data points of Fig. 12 plot the SiGe PL peak energy versus Ge fraction, x , (within the alloy region) for a range of MBE heterostructures [16]. The MBE SiGe peak energies follow the strained Eg curve shifting predictably and consistently to lower energy with increasing x , but are displaced ~ 120 meV below the strained bandgap data of Lang et al [3]. The lower solid curve in Fig. 12 represents the coherently strained bandgap of SiGe alloys coherently grown on (100)Si. PL data () showing the fully strained no phonon peak energies from CVD and RTCVD material from several laboratories are seen to closely follow the strained bandgap curve. The upper curve of Fig. 12 shows the variation with x for the unstrained bandgap determined by PL from polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ alloys [33]. The single data point (X) is from the fully relaxed $\text{Si}_{0.82}\text{Ge}_{0.18}$ alloy of Fig. 11 (c) grown by CVD at $\sim 1000^\circ\text{C}$ and lies very close to the unstrained bandgap curve.

RTCVD and CVD no phonon peak energies from coherently strained epitaxial layers are, in general, close to the strained bandgap curve [3] in Fig. 12 displaced to slightly lower energy due to

exciton binding energies. Two data points appear to slightly higher energy due to quantum confinement in the 2 to 3nm $\text{Si}_{1-x}\text{Ge}_x$ wells of the two SLS [32]. However, the large difference between CVD and MBE PL peak energies at constant x and the much higher quantum efficiencies found in analogous MBE samples suggest a different mechanism prevails in MBE $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ compared to CVD grown material. Growth temperature, T_g , is one major difference; for MBE typically $T_g < 500^\circ\text{C}$ whereas for RTCVD (and CVD) $T_g > 625^\circ\text{C}$. An excitonic mechanism involving Ge rich complexes (isoelectronic centres) inherited from the kinetically-limited epitaxial growth process of low temperature MBE provides the most likely explanation. These nanostructural features would most probably be absent from $\text{Si}_{1-x}\text{Ge}_x$ alloys, grown from a mixture of SiH_4 and GeH_4 in the higher temperature regime of $625^\circ\text{C} - 900^\circ\text{C}$ [32]. Thus, the ≈ 120 meV discrepancy between the present MBE PL peak energies [16] and the strained band gap energy curve of Lang et al.[3] is probably due to an exciton phenomenon in which binding to an isoelectronic centre (related to Ge complexes) occurs.

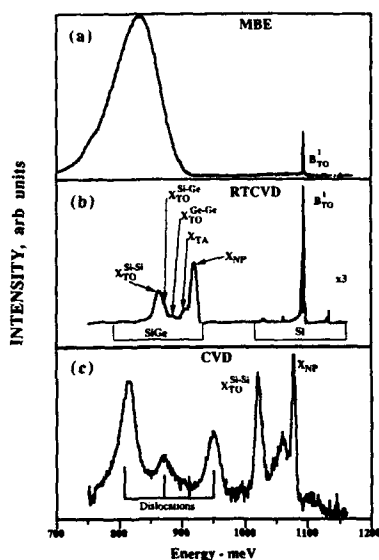


Fig.11 Photoluminescence from SiGe/Si heterostructures : (a) MBE $\text{Si}_{0.75}\text{Ge}_{0.25}/\text{Si}$, 40 period SLS $T_g = 500^\circ\text{C}$ (b) RTCVD [32] $\text{Si}_{0.82}\text{Ge}_{0.18}$ 50 period SLS $T_g = 625^\circ\text{C}$, (c) CVD $\text{Si}_{0.82}\text{Ge}_{0.18}$ alloy $T_g = 1000^\circ\text{C}$.

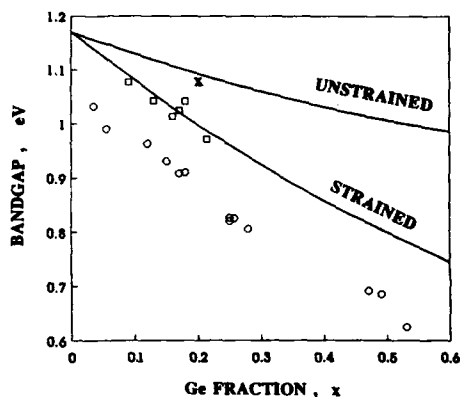


Fig. 12 PL peak energies from MBE (o) and RTCVD (□) and CVD (X) $\text{Si}_{1-x}\text{Ge}_x$ as a function of x . Solid curves represent bandgap vs x for unstrained [33] and coherently strained [3] $\text{Si}_{1-x}\text{Ge}_x/(100)\text{Si}$.

$\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ LIGHT EMITTING DIODE AND OPTOELECTRONIC SWITCH

The schematic of Fig.13(c) illustrates the distribution of dopants and geometry of electrodes for the LED used in an electroluminescence measurement[6]. Fig. 13 also compares photoluminescence (a) and electroluminescence (b) from the same ~ 200 nm thick $\text{Si}_{0.83}\text{Ge}_{0.17}/\text{Si}$ heterostructure. The excitation mechanism in EL involves the introduction of electrons by minority carrier injection into the $\text{Si}_{1-x}\text{Ge}_x$ alloy region under forward bias while holes are provided by acceptors in the p-type SiGe region. The spatial distribution of excitons will peak at the edges of the depletion regions in the $\text{Si}_{1-x}\text{Ge}_x$ alloy and Si. However, in PL the incident beam creates excitons throughout the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructure which may explain the presence of the substrate Si TO peak in PL and its absence in the EL spectrum. The similarities in spectral shape and peak energies of PL and EL in the present work also point strongly to a common luminescence mechanism. The temperature dependencies for our PL and EL were similar and suggest that the luminescence mechanism is excitonic in nature in both cases.

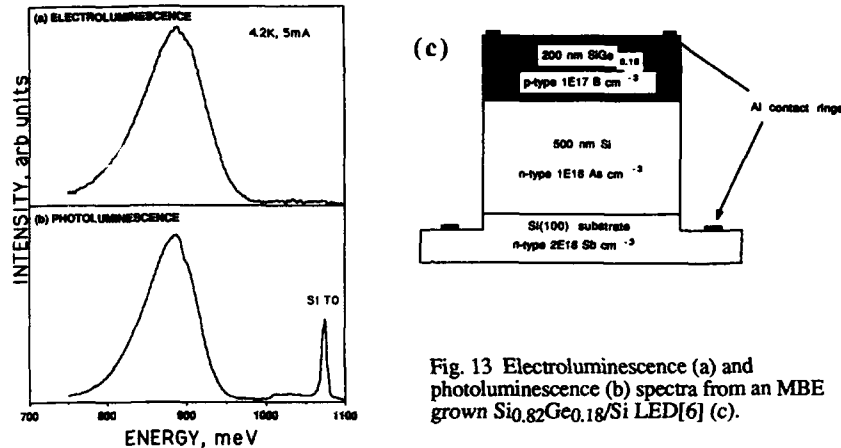


Fig. 13 Electroluminescence (a) and photoluminescence (b) spectra from an MBE grown $\text{Si}_{0.82}\text{Ge}_{0.18}/\text{Si}$ LED[6] (c).

In general, for both EL and PL peaks from MBE $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures the peak energy for any value of x is less than the corresponding strained band gap energy by ~ 120 meV (see Fig. 12). PLE measurements have shown that the no-phonon transition is dominant [32]. Thus, it is likely that the broad intense MBE peak, known to involve no phonons at its high energy edge, is made up from the convolution of individual phonon replicas, probably broadened due to Ge rich complexes. Ge:Si flux fluctuations inherent to MBE material deposited at low growth temperatures by electron beam evaporation may further broaden the PL peaks. When the excitation (electrical or optical) was confined to the alloy region, the EL was similar in all respects to PL from material with the same Ge concentration; i.e., the same peak energies, persistence to ~ 80 K, and comparable internal quantum efficiencies (estimated in the present case for EL to be $\sim 0.25 - 0.75\%$). As in previous PL studies on the same material, [16] the peak energy of the luminescence depended on the Ge concentration x and was ~ 120 meV lower than the previously published alloy band gap energy[3], at any value of x .

An optoelectronic binary device is possibly the most basic element of the next generation of computer and telecommunication systems. The switching properties of such a binary device capable of both optical and electrically switched binary states has recently been demonstrated for the first time in SiGe/Si [2]. The Digital Opto Electronic Switch (DOES) is a novel device, which both emits and detects light, is shown schematically in Fig. 14 together with its I-V characteristics under three illumination conditions. The DOES device can be configured as a 2 or 3 terminal device exhibiting a negative differential region (between on and off states) which in turn permits fast switching either by injected charge or incident light.

The operation of this light sensitive binary switch is described in detail elsewhere[2]. The switching voltage and current taking the device to the "on" state are considerably reduced by $\sim 500\mu\text{w}$ incident He-Ne ($\lambda \sim 632.8\text{nm}$) light as shown by the full power curve in Fig. 14 (c). Three terminal devices where charge may be extracted (or injected) directly from the active layer, switching the device off after an optical response have also been demonstrated. The DOES device also exhibits electroluminescence at low temperatures $\lambda = 1$ to $1.1\mu\text{m}$, (emission intensity peaks as the device switches on) although the internal quantum efficiency remains low.

SUMMARY

MBE has been shown to produce excellent optical properties in homoepitaxial Si doped *in-situ* with low energy As^+ , B^+ and coevaporated B from a novel thermal source. Photoluminescence spectroscopy of thick undoped Si epitaxial layers indicates background doping level (phosphorous) of $\sim 1 \times 10^{14} \text{ cm}^{-3}$ with optical quality comparable to Czochralski Si or conventional CVD epitaxial Si. However, low temperature ($< \sim 600^\circ\text{C}$) growth introduces point defect complexes which quench photoluminescence. These are readily removed on annealing ($> 650^\circ\text{C}$) restoring optical characteristics typical of Czochralski Si or high temperature CVD epitaxial Si indicating negligible residual impurities or other traps are present.

Erbium (emission $\lambda = 1.54\mu\text{m}$) has been successfully incorporated in Si and $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures by coevaporation of Er in conventional Si, Ge MBE. PL spectroscopy revealed only subtle differences in the luminescence spectrum from Er in the various host lattices with a generally low luminescent efficiency due to low activation of the Er^{3+} ion.

Photoluminescence from MBE grown $\text{Si}_{1-x}\text{Ge}_x$ layers is dominated by a ~ 80 meV wide peak centered ~ 120 meV below the alloy bandgap which shifts predictably with Ge fraction between $x = 0.06$ and ~ 0.6 ($1.2\mu\text{m} < \lambda < 1.7\mu\text{m}$). This luminescence peak, which had a low temperature internal quantum efficiency as high as $\sim 10\%$, persisted to ~ 80 K. PL spectra from $\text{Si}_{1-x}\text{Ge}_x$ alloys, Si capped layers and SLS with constant x in the $\text{Si}_{1-x}\text{Ge}_x$ region are closely similar. The PL peak energy and line shape were independent of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ geometry and appear to be intrinsic properties of MBE deposited $\text{Si}_{1-x}\text{Ge}_x$ alloys.

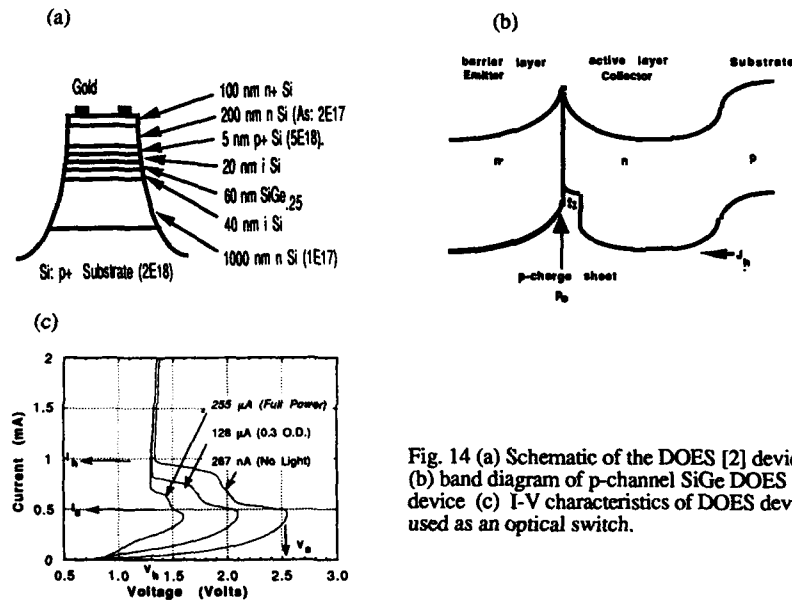


Fig. 14 (a) Schematic of the DOES [2] device (b) band diagram of p-channel SiGe DOES device (c) I-V characteristics of DOES device used as an optical switch.

Electroluminescence has been observed for the first time from $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures. These devices emitted light in the range 1350 - 1550 nm. The electroluminescence was similar in all respects to PL from material with the same Ge concentration. The process producing the EL appears to be the same as that for PL, i.e. emission from the self annihilation of bound excitons with a strong no phonon component.

The weaker near-band-gap PL with resolved phonon replicas obtained from CVD $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures has been compared with the strong, broad band of luminescence typical of PL and EL from MBE SiGe. The luminescence mechanism involves excitons in indirect gap $\text{Si}_{1-x}\text{Ge}_x$ in all cases but significant differences between exciton binding in MBE SiGe alloys and equivalent structures deposited by CVD techniques are evident.

A heterojunction device such as the SiGe / Si digital optoelectronic switch looks extremely promising as a candidate binary device for Si based optoelectronic circuits.

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SI/GE SUPERLATTICES FOR OPTICAL APPLICATIONS: POSSIBILITIES, PROBLEMS, AND PROSPECTS

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ABSTRACT

Si/Ge superlattices offer the possibility to study the influence of various effects on the electronic band structure. Strain, quantization, zone folding, and wave vector mixing effects are expected to create novel optical properties in these Si-based multilayer structures. New optical transitions were observed by various experimental methods like photoluminescence and modulation spectroscopy. In this article we will review the present state of knowledge of the optical properties of short period strained layer Si/Ge superlattices and discuss the problems and prospects for optical applications.

INTRODUCTION

One of the most interesting topics in Si based research during the past five years was the development of Si-Ge heterostructures. With the realization of high quality heterojunctions, multi quantum wells, and superlattices new potential device applications come into consideration. Most fascinating for optical applications is the idea of a fundamental direct band gap formation originated in the artificial layer period in a Si/Ge superlattice. Using simplified assumptions Gnutzmann and Clausecker in 1974 [1] showed that the Brillouin zone folding effect opens the possibility to achieve a direct band gap in a Si based material. Their results were the basis of a huge amount of theoretical [2-14] and experimental work [14-26] during the past few years. Strong inter-subband transitions and optical nonlinearities were predicted as well [27]. Excellent overviews on the results obtained up to 1989 are given in Ref. 28 and 29. The main results resp. predictions from the band structure calculations on the optical properties of Si/Ge superlattices will be discussed in the first chapter. An overview about the most important experimental results with emphasize on light emission results will be given in the second chapter. Finally we will discuss the main problems and corresponding prospects of Si/Ge superlattices with respect to their potential use in Si based optical devices.

BAND STRUCTURE

The intrinsic lattice constant a of Ge is about 4.2% larger than the one of Si. Both Si and Ge are indirect semiconductors with conduction band extrema at the Δ -, L- and Γ -point in k space. In Si the Δ conduction band minimum and in Ge the L minimum is lowest in energy giving a fundamental indirect band gap of about 1.1 eV resp. 0.7 eV. The band structure of a strained layer superlattice (SLS) composed of Si and Ge layers is strongly influenced by strain, confinement, zone folding, and wave vector mixing effects. The fundamental band gap energy can be tuned by strain and confinement. The matrix elements for radiative band gap transitions are in strongly depend on zone folding and wave vector mixing. From the majority of the band structure calculations common structural parameters favoured for the achievement of a fundamental direct band gap with enhanced transition rate can be summarized.

Brillouin zone folding

The influence of the artificial layer period on the electronic band structure of a (100) oriented Si/Ge superlattice is schematically shown in Fig. 1. The dashed curves indicate the conduction and valence band of Si resp. Ge in (100) X-direction. The bulk Δ -minima occur at approximately $0.8 \cdot 2\pi/a$. The superlattice Brillouin zone boundaries of a (100) oriented Si/Ge SLS with a period D of 10 monolayers (ML) are depicted by the vertical dashed lines. The twofolded Δ_{\perp} -minima in growth direction (perpendicular to the layer plane) are folded into the SLS Brillouin zone. The geometrical zone folding picture gives nearly perfect Δ_{\perp} -folding onto the Γ -point for periods of an integer multiple of five monolayers, e.g. for the 10 ML period (see Fig.1). The fourfolded Δ_{\parallel} -minima (parallel to the layer plane) cannot be folded onto the Γ -point by the layer period in growth direction. In agreement with this simple picture microscopic bandstructure calculations [9,10,13] also favour 10 ML period SLS's for perfect $\Delta_{\perp} - \Gamma$ folding.

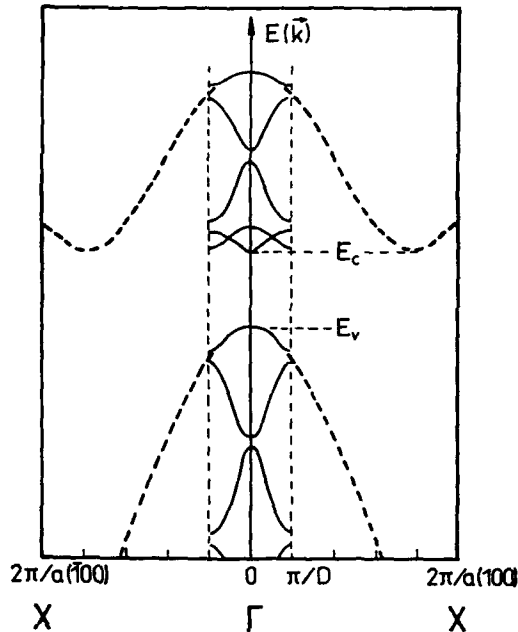


Fig. 1: Geometrical Brillouin zone folding of a Si (Ge)-like conduction and valence band in a (100) oriented Si/Ge superlattice with a period D of 10 monolayers

Strain and confinement

We restrict our considerations to (100) oriented pseudomorphic superlattices. Under pseudomorphic strain conditions the lateral lattice constant a_{\parallel} of both the Si and Ge layers in the SLS is equal to the lateral lattice constant of the substrate resp. buffer layer. Pseudomorphic growth on Si (Ge) substrate without buffer layer influence leads to lateral compression (tension) of the Ge (Si) layers of about 4%. The displacement of the atoms from their intrinsic positions results in significant changes of the band gaps and offsets in the layered structure [30-32]. The sixfold degenerated Δ -minima are splitted into the fourfolded Δ_{\parallel} -minima parallel to the layer plane and the twofolded Δ_{\perp} -minima perpendicular to the layer plane. Although in the valence band splitting of the degenerated maxima, heavy hole (hh) and light hole (lh), occur. The strain induced energy shift of the relevant band edges can be calculated by means of linear deformation potential theory [33] combined with valence band offset results calculated by Van de Walle and Martin [32]. The results for a Si/Ge superlattice with an intermediate lateral lattice constant $a_{\parallel} = a(\text{Si}_{0.6}\text{Ge}_{0.4})$ are depicted in Fig. 2. In the Si layers with lateral tension ($\epsilon_{\parallel} = 1.4\%$) the Δ_{\perp} -minima are lower in energy than the Δ_{\parallel} -minima. In the Ge

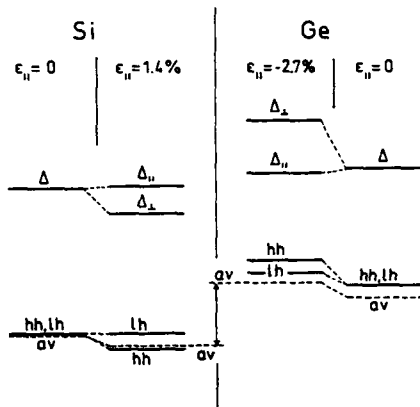


Fig. 2: Energy shifts and offsets of the relevant band edges in a Si/Ge superlattice with intermediate lateral lattice constant

layers (lateral compression, $\epsilon_{||} = -2.7\%$) the splitting both in the valence and conduction band is reversed. The calculated offset [32] between the averaged valence band edges is about 0.5 eV. It turns out that Si/Ge superlattices have a staggered band lineup for all possible strain distributions [29]. The conduction band well is formed in the Si layers, whereas the top of the valence band is highest in the Ge layers. Good agreement between the results of microscopic band structure calculations and macroscopic deformation potential theory (used in Fig. 2) is obtained.

The energies of the relevant superlattice states (Δ_1 , Δ_2 , hh, lh) can be calculated in the envelope function approach using a Kronig-Penney type model as, for example, described in Ref. 34. Both the "bulk" band edges in the individual layers (dashed and dashed-dotted lines) and the superlattice minibands (hatched regions) for a Si_6Ge_4 SLS (6 ML Si, 4 ML Ge) are shown in Fig. 3a as a function of lateral strain in Si. In structures with no strain in Si ($\epsilon_{||}^{\text{Si}} = 0$) the fundamental conduction band minimum is formed by the nonfolded Δ_2 -superlattice states (Δ_2^1). Therefore no fundamental direct band gap can be achieved for pseudomorphic growth on Si. For high enough strain in Si, ($\epsilon_{||}^{\text{Si}} > \approx 1\%$), however, the Γ -folded Δ_1 -states (Δ_1^1) are lowest in energy opening the possibility of a fundamental direct band gap. The Δ_1 -states are more localized in the Si layers (miniband width ≈ 70 meV), whereas the Δ_2 -states are totally delocalized. In the valence band both the hh- and lh-states (hh^1 , lh^1) are delocalized. Like in the valence band a crossing of the relevant states is obtained. For low (high) strain in Si the hh (lh) states are highest in energy. As a result the fundamental band in a Si_6Ge_4 SLS with high Si strain is determined by the Γ -folded Δ_1 -states and the lh states. The estimated band gap is in the near infrared region around 0.8 eV. Due to the type II behaviour (staggered band lineup) the degree of localization of the relevant states plays a major role with respect to the optical transition rate. Delocalization of at least one of the corresponding carriers is necessary for high transition rates, as it is

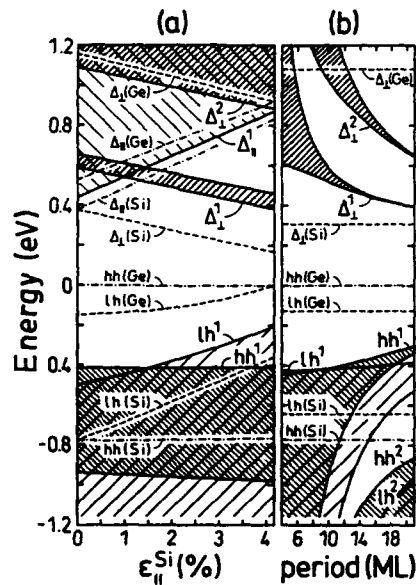


Fig. 3: Band edges in the individual layers (dashed and dashed-dotted lines) and superlattice states (hatched regions) calculated with a Kronig-Penney type model: a) for a Si_6Ge_4 superlattice as a function of lateral strain in the Si layers, b) for a Si_mGe_n superlattice with $m/n = 6/4$ and symmetric strain distribution ($\epsilon_{||}^{\text{Si}} = 1.4\%$) as a function of period

the case for 10 ML period. The influence of period on the superlattice states in symmetrically strained Si_mGe_n superlattices with layer thickness ratio $m/n = 6/4$ is given in Fig. 3b. As expected, with larger periods both the conduction and valence band states get more localized in the corresponding layers. Even for a period of 20 ML the Δ_1 ground states are strongly localized in the Si layers (miniband width ≈ 1 meV). In addition the hh ground states more localized in the Ge layers become dominant for the band gap. Therefore high transition rates for band gap transitions are only expected for periods of the order of ten monolayers.

Wave vector mixing

Due to the difference in the atomic form factors (chemical effect) and the lattice constants a_z in growth direction (structural effect) in the Si and Ge layers, the folded Δ_1 -states get mixed with other momentum states. The degree of wave vector mixing with "true" Γ -states is essential for the overlap of the folded Γ -states with the valence band states in k space. The optical transition rate, therefore, is expected to be highest in short period superlattices composed of pure Si and Ge layers [9]. Although the wave vector mixing enhances the optical transition matrix element, the value of the enhanced matrix element is expected to be at least one to two orders of magnitude smaller than in real direct band gap semiconductors [11].

Substrate window

With regard to band gap light emission the energy ordering of the relevant superlattice states inside the whole system superlattice/buffer layer/substrate needs to be considered. Efficient radiative band gap emission can only take place if the potential minimum for both carrier types (electrons and holes) is inside the superlattice region. Consequently the superlattice band edges have to be fundamental extrema in the whole sample system or at least in the system superlattice/buffer layer. This condition is only fulfilled for pseudomorphic growth on a SiGe alloy substrate resp. on a relaxed SiGe alloy buffer layer on Si or Ge substrate [9].

From the theoretical arguments discussed above one can conclude structural parameters of a Si based superlattice favoured for the achievement of a fundamental direct band gap with enhanced optical transition rate. It turns out that symmetrically strained Si/Ge superlattices with periods of about 10 monolayers are the most promising candidates.

OPTICAL EXPERIMENTS

The most crucial point from the technological point of view is the preparation of high quality short period Si/Ge superlattices with large enough overall thickness due to the large lattice mismatch between Si and Ge. The improvements caused by the use of low substrate temperatures ($\approx 350^\circ\text{C}$) and low growth rates in molecular beam epitaxy (MBE) [35-37] and the symmetric strain concept initiated by Kasper and coworkers [38] enabled a considerable amount of optical experiments in the past few years. In 1986 first experimental evidence for new optical transitions was obtained from electroreflectance of a 4 period Si_4Ge_4 superlattice grown on (100) Si [15]. The first light emission results discussed with respect to the fundamental direct band gap in a 10 ML period Si/Ge superlattice were obtained from photoluminescence experiments on 150 period strain symmetrized Si_6Ge_4 superlattices [19,20] grown on partly relaxed SiGe alloy buffer layers on (100) Si substrate.

Light emission experiments

The photoluminescence (PL) spectrum obtained from a strain symmetrized Si_6Ge_4 superlattice sample is given in the lower part of Fig. 4. The superlattice with an overall thickness of about 200 nm was prepared by MBE technique on (100) Si substrate. To achieve strain symmetrization a thin (20 nm) partially relaxed $\text{Si}_{0.6}\text{Ge}_{0.4}$ alloy buffer layer was incorporated. For detailed growth conditions see Ref. 38. In the high energy region at about 1.1 eV the wellknown excitonic luminescence from the Si substrate is measured. At about 0.85 eV a rather strong and broad luminescence signal arising from the superlattice is emitted. From the corresponding SiGe alloy reference sample grown on the same buffer layer much weaker luminescence signals are obtained. (see upper part of Fig. 4). The arrows mark the energetic positions of similar PL signals measured by Weber and Alonso [39] from a corresponding SiGe alloy grown by liquid phase epitaxy. The alloy luminescence signals can be ascribed to dislocation related transitions (D1 to D4) and the Si-Si vibration (transversal optical phonon) assisted bound exciton transition ($\text{BE}_{\text{Si-Si}}^{\text{TO}}$). The typical dislocation related transitions D1 to D4 in pure Si were extensively studied in former years by, for example, Sauer and coworkers [40]. Due to the growth conditions the dislocation density not only in the alloy layer but also in the superlattice is of the order of 10^9 to $10^{10}/\text{cm}^2$. Therefore a possible influence of dislocation related transitions on the observed superlattice luminescence have to be taken into account. Both the much stronger intensity and the total different spectral behaviour of the superlattice signal, however, strongly indicate that this PL cannot be explained by alloy-related dislocation transitions, but most likely can be ascribed to the fundamental folded superlattice band gap. This is underlined by the absence of strong luminescence from a corresponding 20 ML period $\text{Si}_{12}\text{Ge}_8$ superlattice with the same symmetric strain distribution (see Ref. 20). As discussed in the previous chapter, both the type II behaviour of the superlattice band alignment and the wave vector mixing drastically reduce the band gap optical matrix element with increasing period.

To obtain more information on the possible nature of this superlattice luminescence we also performed strain dependent investigations [20]. The measured photoluminescence peak energies from Si_6Ge_4 superlattices with different strain distributions and the energies of the low energy band gaps obtained from Kronig-Penney type band structure calculations are given in

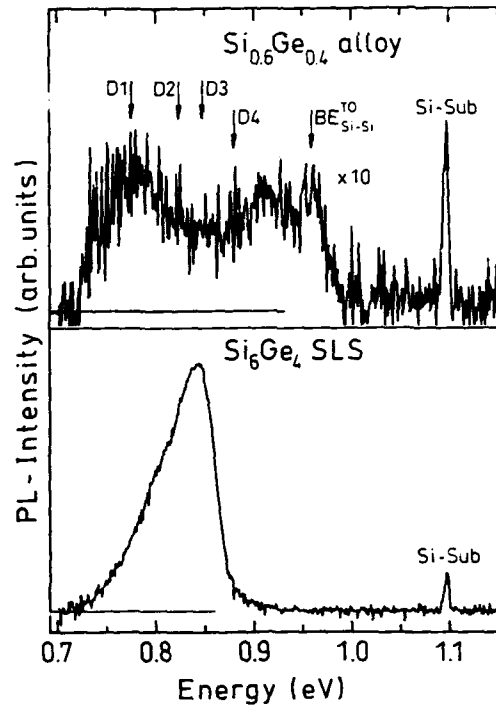


Fig. 4: Low temperature ($T \approx 5\text{K}$) photoluminescence spectra from a strain symmetrized Si_6Ge_4 superlattice ($\epsilon_{\parallel}^{\text{Si}} \approx 1.4\%$, $\epsilon_{\perp}^{\text{Ge}} \approx -2.7\%$) (lower part) and from the corresponding $\text{Si}_{0.6}\text{Ge}_{0.4}$ alloy layer reference sample (upper part) measured under same experimental conditions

Fig. 5 as a function of lateral strain in the Si layers. The estimated fundamental band gap between the lh-states and the folded Δ_1 -states ($\Delta_1^1 - lh^1$) shifts to lower energies with increasing Si strain from about 0.95 eV for $\epsilon_{||}^{Si} \approx 1.4\%$ to about 0.6 eV for the highest possible strain ($\epsilon_{||}^{Si} \approx 4.2\%$). In agreement with the theoretically expected behaviour of the superlattice band gap the superlattice luminescence shows a similar red shift with increased Si strain. The peak energies are about 100 meV lower in energy than the calculated band gap. Microscopic band structure calculations of a strain symmetrized Si_6Ge_4 superlattice [14,41] give a folded fundamental direct band gap with an energy of about 1.1 eV, 250 meV higher in energy than the luminescence peak energy of the corresponding superlattice (see lower part of Fig. 4).

The discrepancy in the absolute energy values between experiment and theory, however, is understandable taking into account the uncertainty of band structure calculations. Besides the inherent uncertainty of the calculations procedures, it has to be considered that the calculations cited here neglect both any interface roughness resp. intermixing and strain resp. layer thickness fluctuation. It is expected that these effects in ultrashort period Si/Ge SLS's, e.g. strain and layer thickness fluctuations, lower the optical transition energies considerable with respect to the expected energies of "perfect" structures and, furtheron, cause a rather broad luminescence.

Strong luminescence was observed only from Si/Ge superlattices on (100) Si substrate with periods of the order of 10 monolayers and with both kind of layers strained (see also results given in Ref.42). Both the observed strain and period dependence is in good agreement with the expected behaviour of the fundamental band gap in this new Si based material, which is predicted to be zone folded direct in k space. Consequently the photoluminescence results support the direct band gap predictions.

We also prepared a buffer layer sample as reference to the symmetrically strained superlattice on the same wafer by using a shutter partially covering the wafer surface after the buffer layer growth. Only a much weaker signal at about 0.77 eV [19] was measured from this buffer layer (thickness 20 nm), probably caused by defect related transitions. Northrup et al. [43] showed by etching experiments on similar but much thicker buffer layers (300 nm thickness) that this weak signal at around 0.77 eV indeed arises from the buffer layer. In addition their results on two Si_6Ge_4 SLS's with different strain distribution prepared by Kasper and coworkers on partly relaxed thin alloy buffer layers confirm the strain dependence shown in Fig. 6.

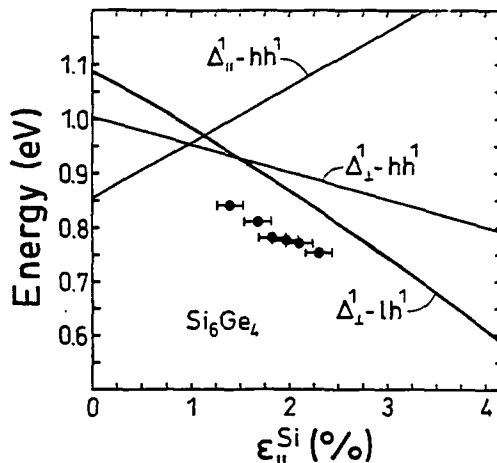


Fig. 5: Photoluminescence peak energies of Si_6Ge_4 superlattices (dots) compared with values of the relevant band gaps (solid lines) obtained from Kronig-Penney type calculations as a function of lateral strain in the Si layers. The estimated uncertainty of the strain values is given by the error bars.

Recently Noël et al. [44] reported on new photoluminescence results from single strained SiGe alloy layers grown on (100) Si substrate. From the as grown alloy layers only weak luminescence features are obtained, similar to the alloy luminescence given in the upper part of Fig. 4. After a special annealing procedure (600 °C, 100 s) a broad but wellresolved, rather strong luminescence in the near infrared spectral region is observed. Originally [44] the luminescence signal was discussed with respect to electron-hole droplets or high density exciton phases. Recent results [45] favour impurity related transitions broadened by MBE growth fluctuations as origin for the strong luminescence. Higher annealing temperatures (800 °C), correlated with the formation of misfit dislocations at the substrate/film interface, however, quench this PL signal totally. Only very weak but sharp dislocation related signals are obtained after this high temperature annealing procedure. For comparison with the strained layer superlattice luminescence (Fig. 4) it has to be considered that the SLS luminescence is obtained from structures with high built-in dislocation density, whereas the strong single alloy layer luminescence disappears, when a high density dislocation network is building up by high annealing temperatures.

Light absorption experiments

Mainly the initial electroreflectance results obtained by Pearsall et al. on a 4 period Si_4Ge_4 structure pseudomorphically grown on (100) Si [15] encouraged a lot of theoretical groups to work on Si/Ge SLS's. New high energy optical transitions were obtained in this experiment in the energy range between 1.5 eV and 4.0 eV. These results for the first time gave strong evidence for the structurally induced new band structure of a short period Si/Ge superlattice. The observed low energy oscillations (in the energy range 0.5 eV - 1.5 eV) are ascribed by the majority of the theoretical groups to the fundamental non zone folded indirect band gap [see for example Ref. 4]. The main results were confirmed by various groups using conventional electro-/photoreflection [23] or electron-beam electroreflectance [26]. Strong superlattice related oscillations in the high energy range were also obtained from photoreflection experiments on strain symmetrized $\text{Si}_8\text{Ge}_{32}$ grown on (100) Si [24] and various short period Si/Ge SLS's pseudomorphically grown on (100) Ge substrates [25]. Furtheron ellipsometry results on strain symmetrized Si_6Ge_4 superlattices [14] demonstrate the new superlattice band structure by the observation of high energy superlattice related transitions.

In 1989 low energy electroreflectance results from 10 ML period Si_4Ge_6 and Si_3Ge_7 superlattices were reported [17]. Photoreflection experiments on a Si_2Ge_9 SLS [25] also show strong oscillations in the low energy range. The SLS's of both experiments were pseudomorphically grown on (100) Ge substrate. The energies of the observed oscillations are within the energy range of the estimated zone folded direct band gaps [41,11]. The interpretation of these results, however, is very complicated due to possibility of strong oscillations, not originated in absorption via the fundamental superlattice band gap, but caused by optical etalon effects [26] or high field Franz-Keldysh effects [46] combined with absorption via the E_0 -gap (≈ 0.9 eV) of the Ge substrate.

The main conclusion which can be drawn from the available absorption results is the confirmation of the structurally induced new superlattice band structure in short period Si/Ge superlattices, e.g. for the high energy critical points. Valuable low energy absorption results from symmetric strained 10 ML period superlattices, most interesting from the point of view of light emission, are not available so far. Photocurrent investigations on these structures [47] show a broad low energy tail down to 0.5 eV, most probably originated in defect related transitions via dislocations. Photocapacity experiments on symmetrically strained Si_4Ge_4 superlattices grown on (100) Si show a similar low energy tail with a variety of sharp features. These sharp features are discussed with respect to the Wannier-Stark ladder effect [42].

PROBLEMS AND PROSPECTS

From the theoretical point of view the prospects of short period superlattices for potential use in optical devices are rather good. Nearly each theory predicts that indeed a fundamental direct band gap can be achieved in short period Si/Ge superlattices. The corresponding optical matrix elements for band gap transitions, however, are expected to be considerable smaller than in real direct gap semiconductors like GaAs. This is mainly reasoned by the limited degree of wave vector mixing of the folded Δ_1 -states with real zone center states, as a consequence of the similarity of Si and Ge material.

The most promising experimental results come from the observation of strong photoluminescence in symmetrically strained 10 monolayer period Si/Ge superlattices, which are also favoured by theory. Although the behaviour of the photoluminescence is in consistence with the predicted behaviour of the fundamental zone folded direct band gap, the actual nature of the luminescence cannot be unambiguously deduced from the experiments on these structures. One of the major difficulties arises from the dislocation related growth problems of symmetrically strained Si/Ge superlattices on (100) Si. Strain symmetrization is important not only from theoretical arguments but also from the technological point of view. Because of unlimited overall thickness for pseudomorphic growth only strain symmetrized Si/Ge superlattices can be grown up to a thickness of technological importance for optical applications. So far strain symmetrization was only achieved by incorporating a relaxed SiGe alloy buffer layer with high dislocation density at the surface. This dislocation density exceeds into the superlattice. Very recent results, presented at this conference, show, however, that several μm thick SiGe alloy buffer layers with essential dislocation free surfaces can be grown on (100) Si substrates by graded layer deposition [48,49]. The results obtained from strain symmetrized superlattices grown on these buffer layers have to be waited for with great interest.

In conclusion we recognize an exciting development of Si/Ge superlattices with respect to their potential use in optical devices from the actual start in 1986 up to the present time. The prospects for future real optical applications are expected to depend mainly on the improvements of the preparation methods.

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DEEP LUMINESCENCE FROM "RELAXED" $\text{Si}_{1-x}\text{Ge}_x$ EPITAXIAL LAYERS

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ABSTRACT

In MBE $\text{Si}_{1-x}\text{Ge}_x$ which is grown to thicknesses greater than the critical thickness h_c , the dislocation-related luminescence peaks D1 and D2 have energies which are independent of x up to $x \approx 0.3$, and then decrease, as observed in LPE $\text{Si}_{1-x}\text{Ge}_x$. In MBE $\text{Si}_{1-x}\text{Ge}_x$ layers grown to thicknesses less than h_c , post-growth annealing produces dramatic changes in the luminescence, giving spectra as from *relaxed alloy*, even though the relaxation determined by X-rays is negligible. These results establish photoluminescence as a sensitive diagnostic tool for detecting dislocations in $\text{Si}_{1-x}\text{Ge}_x$.

1. INTRODUCTION

Photoluminescence has become a widely used tool for characterising $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layers, partly motivated by the desire to achieve high photo-emission from silicon-derived technology. However, luminescence studies have so far concentrated on the near-band-gap region, particularly for alloys with $x < 0.2$ [1]. In this paper we investigate dislocation-related luminescence spectra from MBE $\text{Si}_{1-x}\text{Ge}_x$ over the full range of x and over a wider range of photon energies than has been previously used.

One important parameter in determining the properties of a $\text{Si}_{1-x}\text{Ge}_x$ layer grown on silicon is its strain. A coherent epitaxial layer has an in-plane strain of $0.042x$ resulting from the 4.2% difference in the lattice spacings of free-standing crystalline silicon and germanium. The elastic energy involved in this deformation can be reduced if the layer is able to relax by creating dislocations. We can identify two different regimes of relaxation. One is when the $\text{Si}_{1-x}\text{Ge}_x$ layer is grown thick enough that it relaxes during growth [2]. The second is when a strained layer is grown at a relatively low temperature but is subsequently relaxed by heating to a higher temperature than was used in growth. The relaxation is usually not complete [3], and depends on variables such as the temperature of annealing relative to the growth temperature [4] and the presence of defects able to nucleate the dislocations [5,6].

Luminescence from relaxed $\text{Si}_{1-x}\text{Ge}_x$ layers is therefore expected to be dominated by the effects of dislocations. Dislocation-related luminescence is well-known from both silicon [7] and germanium [8] (although its origin is still controversial [9,10]) and also from $\text{Si}_{1-x}\text{Ge}_x$ alloys grown by liquid-phase epitaxy [11].

2. SAMPLES AND EQUIPMENT

Samples of $\text{Si}_{1-x}\text{Ge}_x$ have been grown by evaporating silicon and germanium on to Czochralski silicon (001) substrates in a VG V90S MBE system. Substrate temperatures were in the range 400 to 650 °C. Compositions and average lattice strains have been determined by double-crystal X-ray diffraction. Photoluminescence was generated using the 457.9 nm line of an Ar^+ laser, typically at a power density at the sample of about

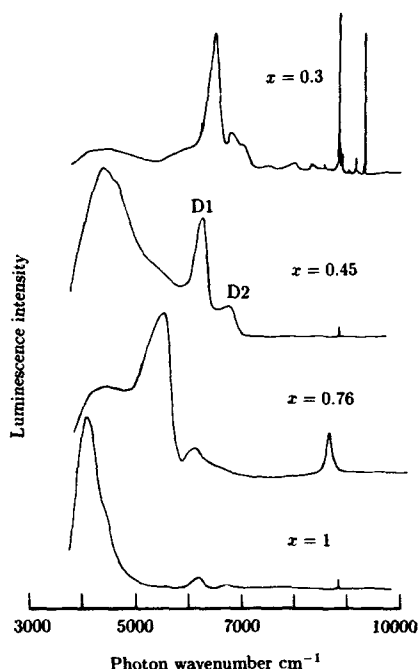


Figure 1. Luminescence of samples grown to beyond the critical thickness, with $x = 0.3$ to $x = 1$. Features near 9000 cm^{-1} are from excitons bound to shallow impurities in the substrate.

50 mW/mm^2 . The samples were either immersed in liquid helium or, for variable temperature measurements, were mounted in helium gas on the cold finger of a helium flow cryostat. The photoluminescence was detected using a modified Nicolet 60SX Fourier transform spectrometer fitted with a cold-windowed InSb detector, giving a low-energy cut-off at 3600 cm^{-1} . For better signal to noise ratios at photon energies above 6000 cm^{-1} we have also used a germanium detector.

3. SAMPLES RELAXED DURING GROWTH

Figure 1 shows the luminescence from representative samples grown to a thickness exceeding the critical thickness, so that they undergo some relaxation during growth [2]. The total luminescence yield from the samples varies only slightly through the set. The highest energy features, above about 8000 cm^{-1} , are the well-known luminescence transitions caused by the decay of excitons bound to the shallow impurities in the substrates [12]. The energies of the other peaks are plotted (as the squares) in Fig. 2. The triangles on Fig. 2 show the corresponding features from LPE samples provided by Jörg Weber.

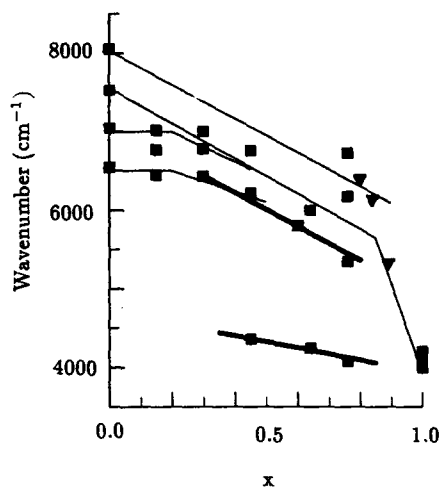


Figure 2. Squares show measured data for the energies of deep luminescence at 4.2K from MBE $\text{Si}_{1-x}\text{Ge}_x$ alloys grown to thicknesses greater than the critical thickness. The thin lines are the variations in energy of D1 to D4 as reported by Weber and Alonso [11] for LPE alloys, and show the regions of their data. The triangles are data measured from three of their samples. The thick lines show the different variation of the energy of D1 with x found in the present work, and the variation in energy of the deep broad band centred near 4200 cm^{-1} .

In crystalline silicon, the four major dislocation-related luminescence bands (labelled D1 to D4) occur at photon wavenumbers of 6550, 7050, 7530 and 8060 cm^{-1} . Weber and Alonso [11] have reported their energies as x increases for $\text{Si}_{1-x}\text{Ge}_x$ liquid-phase alloys. Their results are shown by the thinner lines on Fig. 2, and the extent of the lines shows the range of their data. Our results confirm that the energies of D1 and D2 are essentially constant at small x , and then decrease with increasing x . However, we have been able to extend the range of our data for D1 to larger x , although the intensity of the D1 peak decreases rapidly above $x = 0.5$. We find that the energy of D1 decreases linearly over the range $0.3 < x < 0.8$ at

$$dE_{D1}/dx = -2160 \text{ cm}^{-1}. \quad (1)$$

The magnitude of this gradient is twice that reported by Weber and Alonso [11], but is equal to their gradient for D3.

For $0.4 < x < 0.7$ the fraction of the intensity in the relatively sharp D peaks decreases, and most of the intensity falls in a broad continuum (Fig. 1). In particular there is a very broad band centred at 4200 cm^{-1} for $x = 0.45$ and decreasing slowly to 4080 cm^{-1} at $x = 0.76$. We have not measured the luminescence efficiency of this band, but in general terms its luminescence output is closely comparable to that of typical deep luminescence centres in crystalline silicon. Given the interest in finding high temperature luminescence from silicon, we have measured the temperature dependence of the band using the sample with $x = 0.45$ whose spectrum is on Fig. 1. Over the temperature range used, 6 to 80 K, there is no detectable broadening of the luminescence, and so the intensities of the broad band and of D1 and the peak labelled D2 have been defined by the peak heights on the spectra. The luminescence of the D1 and D2 bands decrease rapidly above 30K, as observed in crystalline silicon [7,13], but the luminescence from the broad band is readily observable up to at least 80 K (Fig. 3). The lines on Fig. 3 have been calculated assuming that the bands decrease in intensity by a thermal ionisation process with an activation energy E , so that the intensity $I(T)$ at temperature T is

$$I(T) = I(0)/[1 + g \exp(-E/kT)]. \quad (2)$$

Here g is the ratio of the degeneracies of the ionisation states and the excited state of the luminescing transition, and is either a constant or, for ionisation to a continuum, is proportional to $T^{3/2}$. Since we have no *a priori* knowledge of which form of g should be used, the calculated values of E (between 6 and 11 meV for both D1 and the broad band) are not reliable. However, the observed data on Fig. 3 demonstrate that the broad band is more stable against temperature than most deep centres in silicon [12]. The origin of the broad band is not known, but it has recently been observed to have a greater intensity in samples which have been deliberately contaminated with copper [14].

Proceeding to still higher x , the spectra sharpen as x approaches unity, and we observe dislocation-related luminescence characteristic of germanium [8] (Fig. 1).

The strains in the alloys of the as-grown samples of Fig. 1 vary from 4% for the $x = 0.76$ sample to 32% for the $x = 0.3$ sample: these samples are far from being fully relaxed. Nevertheless, the energies of the dislocation-related lines agree with those reported for thick LPE samples (Fig. 2). This point is shown more dramatically in the next section.

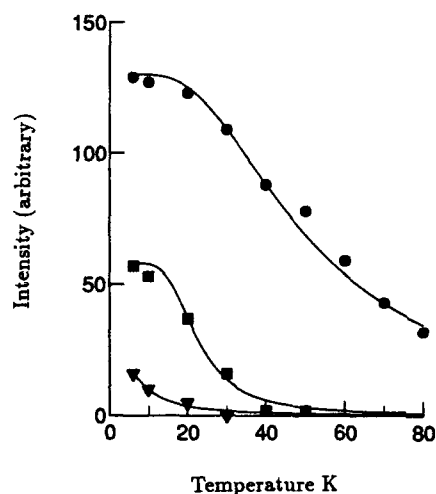


Figure 3. Points show measured intensity of (from top to bottom) the broad band centred on 4200 cm^{-1} , the D1 and the D2 peaks in a relaxed (as-grown) sample with $x = 0.45$ as functions of temperature. The lines are Eq. 3.

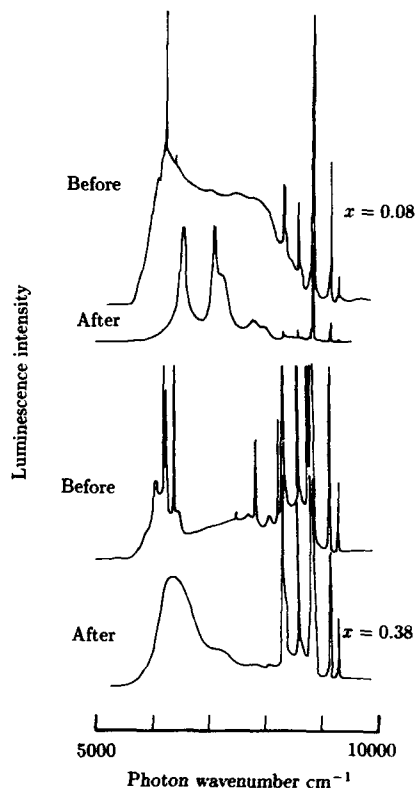


Figure 4. Luminescence from two samples with $x = 0.08$ and $x = 0.38$ respectively measured in the as-grown state ("before") and after annealing for 1 hour at $850\text{ }^{\circ}\text{C}$. Transitions near 9000 cm^{-1} are from excitons bound to the shallow impurities in the substrates.

4. SAMPLES RELAXED AFTER GROWTH

Samples have also been grown to less than the critical thickness, and then annealed in a nitrogen atmosphere at $850\text{ }^{\circ}\text{C}$ for 1 hour. The relaxation as measured by X-ray diffraction was usually small, so that over 90% of the initial strain usually remained in the annealed samples. Nevertheless, all the annealed samples showed major changes in their luminescence spectra, with sharp D1 and D2 dislocation peaks dominating after the anneal (Fig. 4). The energies of the D1 and D2 peaks are close to 6500 and 7000 cm^{-1} in all our samples with $x < 0.2$.

In Sec. 3 we confirmed that the energies of D1 and D2 are independent of x for $x < 0.3$ in thick alloys. Consequently, the energies of D1 and D2 in the thin post-annealed indicate either that the luminescence originates either from the silicon substrate or from relaxed alloy. To distinguish between these possibilities we have examined one sample

with $x = 0.38$. Fig. 4 shows how the annealing, which leaves $94 \pm 3\%$ of the initial strain as measured by X-ray diffraction, produces a peak centred on 6300 cm^{-1} . This energy is exactly as expected for D1 in a relaxed as-grown sample with this alloy composition (Fig. 2).

The experimental evidence is thus that the dislocation-related luminescence observed in samples which have been annealed after growth occurs from relaxed parts of the alloy. The extent of the relaxation can be gauged from the lack of splitting in the D1 line. The change in energy $h\nu$ of D1 with externally applied stresses is known for crystalline silicon [7]. D1 responds to external stresses as would a random array of tetragonal defects. (There is some controversy as to whether this is the correct assignment [10], but it gives an accurate parameterisation of the stress response, which is all that we require here). Denoting the major axis of one of the tetragonal orientations as Z and two perpendicular cube axes as X and Y , the response to stress tensor components s_{II} is [7]

$$\Delta h\nu = A_1 s_{ZZ} + A_2 (s_{XX} + s_{YY}) \quad (3)$$

where $A_1 = -46 \text{ meV/GPa}$ and $A_2 = 11.3 \text{ meV/GPa}$ and compressive stress is taken to be positive. An alloy of $\text{Si}_{1-x}\text{Ge}_x$ grown on a $\langle 001 \rangle$ silicon substrate has in-plane strains of $e_{zz} = e_{yy} = 0.041x$, resulting in a Poisson's ratio effect of $e_{zz} = -2c_{12}e_{xx}/c_{11}$. Using the elastic constants of silicon, and A_1 and A_2 for dislocations in silicon, Eq. 3 gives energy perturbations to D1 of

$$\Delta h\nu_1 = 1400x, \text{ and } \Delta h\nu_2 = -2150x \text{ cm}^{-1} \quad (4)$$

for a fully strained alloy of germanium content x . In contrast, no splitting is detected for the relaxed alloy with $x = 0.08$ in Fig. 4, which has a mean residual strain of 90% as determined by X-ray diffraction. Any splitting is less than 50 cm^{-1} , and so, from Eq. 4, must originate from regions of the alloy in which less than 20% of the strain remains.

In addition to the change in spectral features produced by the annealing, there is also a considerable increase in luminescent intensity of the annealed samples relative to the as-grown samples. The cause of the increase is not determined by our data; one possibility is that the dislocations getter non-radiative impurity-traps from the alloy.

We conclude that the photoluminescence from partially relaxed $\text{Si}_{1-x}\text{Ge}_x$ is dominated by dislocation-related luminescence. This luminescence then necessarily occurs from the most relaxed (least strained) regions of the alloy, giving transitions at the energies characteristic of the fully relaxed alloy grown beyond the critical thickness. The first stage in producing photoluminescence by an Ar^+ laser is the creation of excitons, which would be expected to diffuse towards the more highly strained parts of the alloy, where the energy gap is smaller. Evidently the dislocations either have a high capture cross-section for excitons or a high luminescence efficiency to allow them to dominate the luminescence spectra.

5. SUMMARY

We have shown that in MBE $\text{Si}_{1-x}\text{Ge}_x$ which is partially relaxed during growth, the dislocation-related luminescence peaks D1 and D2 have energies which are independent of x up to $x \approx 0.3$; this independence is not understood. For $x > 0.3$ the energy of D1 decreases as Eq. 1. When $0.4 < x < 0.8$, the dominant luminescence is a broad band observed at low energies, centred on $\approx 4200 \text{ cm}^{-1}$; this luminescence persists to over 80K in contrast to the D1 and D2 features which die away above $\approx 30 \text{ K}$. Post-growth

relaxation of MBE $\text{Si}_{1-x}\text{Ge}_x$ layers produces dramatic changes in the luminescence, giving spectra as from *relaxed* alloy, even though the relaxation determined by X-rays is negligible. The heightened sensitivity of photoluminescence to relaxations in $\text{Si}_{1-x}\text{Ge}_x$ is similar to its increased sensitivity in InGaAs strained layers [15].

ACKNOWLEDGEMENTS We thank Jörg Weber for providing LPE $\text{Si}_{1-x}\text{Ge}_x$ layers. The work was supported by the Science and Engineering Research Council of the UK.

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CHARACTERIZATION AND OPTICAL STUDIES OF SHORT-PERIOD Si_mGe_n SUPERLATTICES

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ABSTRACT

Short-period Si_mGe_n (m monolayer (ML) Si, n ML Ge, $n+m \approx 40$ ML ≈ 5.5 nm) strained layer superlattices (SLS) are grown on $\langle 100 \rangle$ silicon by low temperature molecular beam epitaxy. Various characterization tools such as X-ray diffraction, transmission electron microscopy, Rutherford backscattering, Raman spectroscopy and photocapacitance measurements are used to analyze the growth quality, strain distribution, periodicity, interface sharpness and optical properties of the SLS. Recent photoluminescence experiments give hints of a direct bandgap transition from a 10 ML Si_6Ge_4 SLS in the near infrared spectral region. I-U and C-U measurements on mesa diodes ($A_M = 2 \cdot 10^{-4} \text{ cm}^2$) are performed at various temperatures down to $T = 35$ K. Photocapacitance measurements show a Wannier-Stark localization of the superlattice states in a p^+-n doped Si_4Ge_4 SLS diode, for the first time observed in type II superlattices. The observed transitions are believed to be defect or impurity related and are discussed in terms of a Wannier-Stark ladder behaviour.

I. INTRODUCTION

Short-period strained layer Si_mGe_n superlattices (SLS) grown on Si substrates are of increasing technological interest because of the possibility to modify the electronic and optical properties of the host crystal silicon. The bandstructure of the SLS is strongly influenced by strain distribution, composition (i.e. Si/Ge thickness ratio) and period. As early as 1974 it was predicted that for distinct period lengths and composition of the SLS Brillouin zone folding effects are expected to create a quasidirect bandgap in a silicon type bandstructure [1]. For the experimental realization of these structures by molecular beam epitaxy (MBE) it is essential to study the strain distribution, the interface sharpness, the period length and the composition of the SLS by X-ray diffraction and transmission electron microscopy (TEM). The new optical properties due to the folded bandstructure of the SLS can be investigated by photoluminescence (PL) [2] and modulation spectroscopy (e.g. electroreflectance spectroscopy [3]) as well as by photocapacitance measurements [4]. After a brief description of the growth of the SLS structures by MBE we show PL spectra of SLS samples with period lengths around 10 ML. We discuss photocapacitance measurements on p^+-n doped SLS structures which exhibit the Wannier-Stark localization of the SLS observed in the photoionization cross section spectrum as a function of the applied reverse bias.

II. GROWTH OF THE Si_mGe_n SLS BY MOLECULAR BEAM EPITAXY

We have grown various series of short-period Si_mGe_n ($L = m+n < 40$ monolayers (ML) ≈ 5.5 nm) superlattices on p^+ (series B1585-B1590) as well as on semi-insulating $\langle 100 \rangle$ -oriented silicon substrates (series B1760-B1768) by molecular beam epitaxy (MBE). Details of the growth apparatus and the chemical pretreatment of the 3 inch diameter wafers are

described elsewhere [5]. The starting silicon buffer layer was grown at a temperature of $T_g=550C^\circ$ with a thickness of 20nm in both series where for the subsequent equally thick $Si_{1-y_b}Ge_{y_b}$ alloy layer the growth temperature was reduced to $T_g=450C^\circ$. The Ge content of the alloy buffer layer was adjusted to achieve strain symmetrization of the subsequent SLS [6] in both series ($y_b=0.75$ for series B1585-B1590; $y_b=0.6$ for series B2063-B2068). The SLS was grown at a temperature of $T_g=450C^\circ$ (series B1585-B1590) and $T_g=350C^\circ$ (B2063-B2068) and consist of $N=145$ periods with composition 6:4 (=6 ML Si : 4 ML Ge; B2063-B2068) and N periods of composition 16:16, 8:8, 4:4, and 2:2 for the p^+-n doped SLS series (B1586, B1587, B1589, B1590 resp.). The SLS has a total thickness of about 200nm in all samples. In the p^+-n doped series (B1585-B1590) superlattice and buffer layer were n -doped by incorporation from a prior to growth deposited Sb-adlayer (adlayer density $n_{30} = 1 \cdot 10^{14}cm^{-2}$). A thin Si cap layer terminates the growth to provide a Si surface for postepitaxial process steps which in case of the series B1585-B1590 was grown with a thickness of 10nm (1nm for B2063-B2068) and has been n^+ doped using solid phase epitaxy (amorphous deposition at room temperature, recrystallization at $T_{rec}=575C^\circ$).

Table I :

Composition $m:n$, period length L , and biaxial strain ϵ_{Si} in the Si layers of the Si_mGe_n SLS samples of series B2063-B2068 as obtained from a Raman analysis [8]

sample No	$m : n$ [ML]	$L=m+n$ [ML]	ϵ_{Si} [%]
B2063	9 : 6	15	1.8
B2064	6.9:6.7	13.6	1.5
B2067	5.1:4.4	9.5	2.1
B2068	5.5:3.7	9.2	1.4

III. PHOTOLUMINESCENCE SPECTRA

Figure 1 compares the PL signals of 4 samples from series B2063-B2068 with period lengths around 10 ML and Si/Ge thickness ratios of $m/n=6/4$. The SLS's of these samples are grown on a strain symmetrizing buffer where theory predicts quasidirect transitions around $\hbar\omega=0.9$ eV [7]. Table I lists the different period lengths, the Si/Ge thickness ratio and the biaxial strain in the Si-layers of these samples obtained from a Raman analysis [8]. The PL spectra were measured at $T=5K$ and excited by the $\lambda=457.9nm$ Ar^+ -laser line with an intensity of $I_0=100W/cm^2$ and a focus size of roughly $1mm^2$. The observed signals around $\hbar\omega=0.8eV$ are believed to stem from quasidirect transitions in the zone folded SLS bandstructure as is confirmed by a simple Kronig-Penny type calculation [2], [9]. Sample B2068 exhibits the strongest PL signal at $\hbar\omega=0.85eV$ having a period length close to 10 ML ($L=9.2ML$) and the smallest in-plane strain value ϵ_{Si} in the Si layers of all samples ($\epsilon_{Si}=1.4\%$, see table I). As can be seen from figure 1 and table I the PL peak shifts to lower energies with increasing ϵ_{Si} as expected from theory [2], [9].

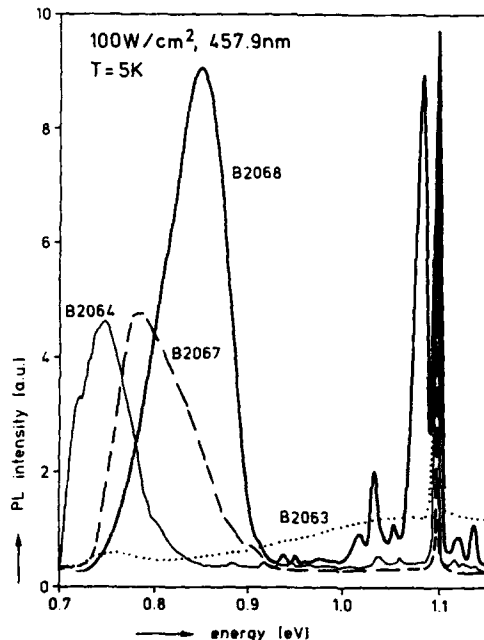


Figure 1 : Comparison of the PL-spectra of 4 samples from series B2063-B2068 with a period length around 10ML and a Si/Ge ratio of $m/n=6/4$ grown on a strain symmetrizing buffer layer. The PL intensities of these samples are normalized to the strongest signal which is exhibited by sample B2068 at $\hbar\omega=0.85$ eV having a period length of $L=9.2$ ML and a strain value in the Si layers of the SLS of $\epsilon_{Si} = 1.4\%$. The peak at 1.1eV is the bulk luminescence of the Si-substrate while the PL signals around $\hbar\omega=0.8$ eV are believed to stem from the quasi-direct transition at $k=0$ in the zone folded SLS bandstructure.

IV. OPTICAL AND ELECTRICAL PROPERTIES OF Si_mGe_n MESA DIODES STUDIED BY JUNCTION SPACE CHARGE SPECTROSCOPY

From the series B1585-B1590 mesa diodes ($A_M=2 \cdot 10^{-4} \text{cm}^2$) were fabricated by standard semiconductor processing techniques. The C-U analysis reveals an n-doping level of $n=3 \cdot 10^{16} \text{cm}^{-3}$ in the SLS with a depletion width of $W=140 \text{nm}$ at $U=0$. Figure 2 shows the photoionization cross section of electrons as a function of incident photon energy measured by the junction space charge technique (JSCT) [12] in the Si_4Ge_4 SLS diode (B1589) at a reverse bias voltage of $U_{rev}=0.2 \text{V}$. The inset in this figure shows the layer sequence and the dimensions of the mesa together with the illumination window of the top contact layer (epitaxial side n^+) through which the light is impinging and subsequently being absorbed in the 200nm thick SLS layer. The observed oscillatory structures in the photoionization spectrum of Figure 2 can be even seen more pronounced when plotted as a function of reverse bias voltage for fixed incident photon energy as done in Figure 3. The observed structures are believed to originate from electronic transitions of donor type impurity or defect levels into the conduction band of the SLS. When we measure the photocapacitance (PC) spectrum for different photon energies as a function of reverse bias field the peak energies of the oscillatory structures shift to lower energies with increasing field strength.

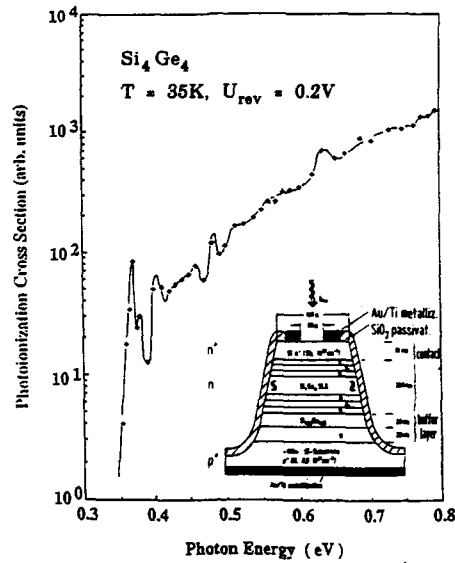


Figure 2 : Photoinitiation cross section of electrons from a p^+-n doped Si_4Ge_4 SLS (B1589) measured by the Junction Space Charge Technique at $T=35K$ and an applied reverse bias of $U_{rev}=0.2V$. The inset shows the dimensions of the mesa and the illumination window on the top contact of the SLS diode.

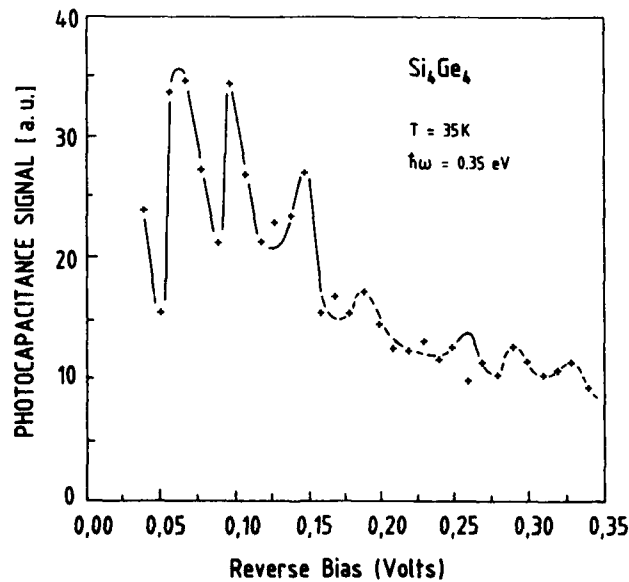


Figure 3 : Photoinitiation cross section of the Si_4Ge_4 SLS at $T=35K$ measured as a function of reverse bias voltage for a fixed incident photon energy ($\hbar\omega=0.35eV$). The peaks in this spectrum shift to lower energies with increasing field strength as expected from theory of the Wannier-Stark localization.

V. DISCUSSION

The PL results of the SLS series B2063-B2068 are in agreement with a quasi direct transition via zone folding but there is no proof possible by the shown experimental results. Additional measurement techniques such as modulation spectroscopy (e.g. electroreflectance, photoreflectance) or short circuit current measurements are required elucidating the nature of this PL. For the p-n doped samples it was shown that the JSCT can be used to obtain additional information from the bandstructure of the SLS and from type and energy levels of defects and impurities. The bandstructure together with the transitions from deep impurity or defect levels into the conduction band of the SLS are shown schematically in Figure 4. When we analyze the data according to the theory of the Wannier-Stark localization [13] - routinely applied in III-V compounds [14,15] - the observed peak energies in the PC spectrum for fixed incident photon energies decrease linearly with applied electric field strength. When plotted as a function of increasing field strength these peak energies lie on straight lines which can be indexed by integer or half-integer numbers reflecting transitions from impurity levels dominantly situated in the Si or Ge layers of the SLS respectively [11]. These transitions which both lead to an evenly spaced Wannier-Stark ladder spectrum are depicted in Figure 4. These experiments constitute the first observation of a Wannier-Stark localization in type II superlattices.

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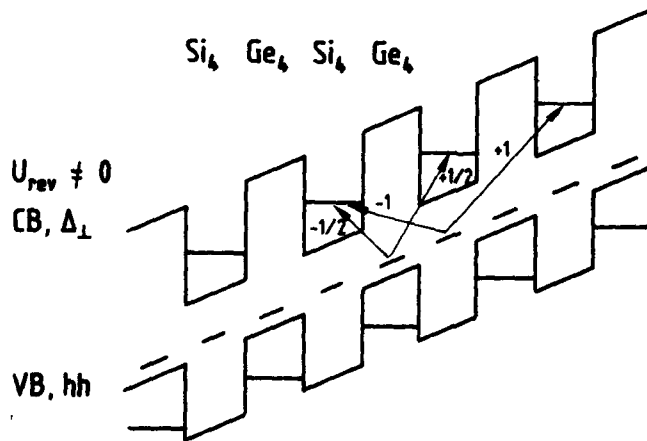


Figure 4 : Sketch of the energy levels of the defects in the conduction- and valence band potential profile for a strain adjusted Si_4Ge_4 SLS under applied electric field. Depicted are the transitions from defect levels into the conduction band leading to the evenly spaced Wannier-Stark ladder in the absorption spectrum. Transitions from levels in the Si and Ge layers lead to full- and half-integer ladder spectrum.

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RAMAN STUDY OF STRAIN AND CONFINEMENT EFFECTS IN Si/Ge STRAINED LAYER SUPERLATTICES UNDER HYDROSTATIC PRESSURE

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ABSTRACT

The effects of strain and confinement on optical phonons in a $\text{Si}_{12}\text{Ge}_4$ strained layer superlattice grown by MBE on c-Si (001) were studied as a function of hydrostatic pressure ($T = 295 \text{ K}$) using Raman scattering. The change of phonon frequency with pressure, $d\omega/dP$, for the principal quasi-confined LO mode in the Ge layers is found to be significantly smaller than that for bulk crystalline Ge because the magnitude of biaxial strain decreases in the Ge layers with added pressure and because the Grüneisen parameter of the confined mode is smaller than that of the Γ -point optical phonon. More generally, it is noted that the magnitude of biaxial strain in many strained layer superlattices initially decreases with the application of hydrostatic pressure, making the structures more stable.

INTRODUCTION

Ultrathin Si/Ge strained layer superlattices (SLS) have been grown recently with high quality crystallinity, by using molecular beam epitaxy (MBE), despite the significant lattice mismatch ($\sim 4\%$) between Si and Ge.[1-2] The electronic properties of Si/Ge superlattices are of particular interest because of the possibility of obtaining quasi-direct gap behavior through a combination of zone folding and strain effects.[3,4] Raman studies of the structural properties of Si/Ge superlattices have yielded useful information on strain, confinement and interfacial disorder.[5-7]

The application of high pressure provides a new method to study the effects of strain and confinement in layered structures. When hydrostatic pressure is applied to a SLS, the lattice mismatch between alternating layers changes because of the different compressibilities of the two materials in these layers, and consequently biaxial strain can be tuned. Moreover, the shift of each confined mode frequency with applied pressure differs from that of the zone-center longitudinal optical (LO) phonon because the Grüneisen parameter varies across the LO phonon dispersion curve. In this work, we study strains in a Si/Ge superlattice by subjecting the SLS to high pressure in a diamond anvil cell (DAC), and then analyzing it by Raman spectroscopy. More details are provided in Ref.[8].

EXPERIMENTAL PROCEDURE AND RESULTS

The superlattice was grown by MBE on top of a 2700 Å Si buffer layer which had been grown on a Si substrate cut 2° from the [001] plane. The growth temperature was 375 - 400°C. The superlattice consists of 12 monolayers of Si followed by 4 monolayers of Ge (Si₁₂Ge₄), repeated 25 times, and is covered by a 140 Å Si cap layer. The SLS substrate was mechanically thinned to 50 μm, and then loaded into a gasketed Mao-Bell diamond anvil cell in order to apply hydrostatic pressure. The pressure (P) in the DAC was determined by the standard ruby calibration scale. Raman spectra of Si/Ge SLS were taken at room temperature using the 4880 Å line from a CW argon ion laser in the backscattering configuration.

The Raman spectrum of this Si/Ge SLS is characterized by the presence of three main peaks, assigned in order of increasing energy to Ge, Ge-Si-like and Si vibrations. Two representative Raman spectra are shown in Figure 1, corresponding to ambient pressure (1 bar) and 62.5 kbar, the maximum applied pressure in the experiment. Only one Ge peak was found, at 308.0 cm⁻¹ for P = 1 bar; it was asymmetric with a tail towards lower energy. This peak corresponds to the principal quasi-confined mode in the Ge layers, and is shifted in energy with respect to that in bulk c-Ge (301.3 cm⁻¹ at P = 1 bar). The big Si peak near 520 cm⁻¹ is from the unstrained c-Si contributed by the cap layer, superlattice Si layers, the buffer layer and the substrate.

The least square straight lines of the Raman shifts of each feature vs. pressure yield $d\omega/dP$ values for each peak. $d\omega/dP$ is 0.31 ± 0.03 , 0.45 ± 0.03 and 0.47 ± 0.02 cm⁻¹/kbar for the Ge, Ge-Si-like and Si peaks, respectively. For comparison, the Raman shifts vs. pressure for bulk c-Ge and c-Si were also measured in this same pressure range, giving 0.37 ± 0.02 and 0.49 ± 0.02 cm⁻¹/kbar for c-Ge and c-Si, respectively. $d\omega/dP$ for the Ge phonon in the SLS is 0.06 cm⁻¹/kbar smaller than that in c-Ge.

ANALYSIS AND DISCUSSION

Lattice dynamics and linear chain model calculations of Si/Ge SLS's [7,9] show that there are confined modes in thin Si layers, and quasi-confined modes in thin Ge layers, even though the Ge optic and Si acoustic modes overlap in energy. There is no biaxial strain in the Si layers because the SLS is commensurately grown on c-Si and the Si layers in the SLS are so thick that confinement effects are small. Consequently, the Si layer Raman peak overlaps that of the cap and buffer layers and it is of no interest here. The observed principal quasi-confined Ge mode is affected by strain and confinement. At ambient pressure, the frequency of the principal confined Ge optic phonon in the SLS (ω) is 6.7 cm⁻¹ higher than that of zone center LO phonons in c-Ge (ω_0). The compressive

stress in the Ge layer is expected to increase ω by 15.8 cm^{-1} ($\Delta\omega_{\text{strain}}$), suggesting that the quasi-confinement decreases ω by $\sim 9 \text{ cm}^{-1}$ ($\Delta\omega_{\text{confinement}}$). This conclusion agrees with other experimental results and with an estimate from the LO phonon dispersion curve.[5,7] The measured Raman shift at ambient pressure can be expressed as

$$\omega = \omega_0 + \Delta\omega_{\text{strain}} + \Delta\omega_{\text{confinement}} \quad (1)$$

Similarly, the change in Raman shift with applied pressure $\delta\omega(P)$ can be attributed to changes due to strain and confinement

$$\delta\omega(P) = \delta\omega_{\text{strain}}(P) + \delta\omega_{\text{confinement}}(P) \quad (2)$$

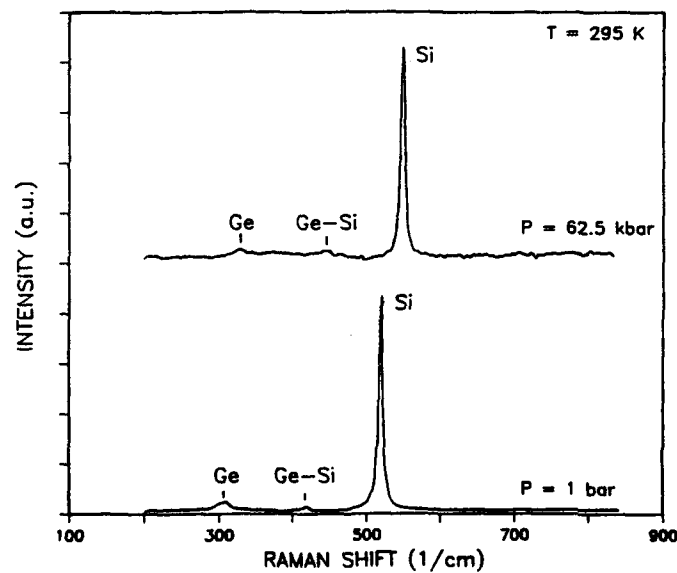


Figure 1. Raman spectra taken at $P = 1 \text{ bar}$ and $P = 62.5 \text{ kbar}$ are shown ($T = 295 \text{ K}$). The peaks in order of increasing energy are the principal quasi-confined Ge mode, Ge-Si-like mode and Si mode.

The Effect of Strain

The Raman frequency for an optical phonon in Ge layers of the SLS along the [001] direction, in the absence of confinement and interfacial disorder, is

$$\omega = \omega_0 + \frac{1}{2\omega_0} [p \epsilon_{zz} + q (\epsilon_{xx} + \epsilon_{yy})] \quad (3)$$

where p and q are the Ge deformation potentials defined in Ref. [10], and ϵ_{ii} are the diagonal elements of the strain tensor. In the presence of hydrostatic pressure and biaxial stress, ϵ_{ii} can be decomposed into $\epsilon_{ii} = \epsilon_{ii}^{(h)} + \epsilon_{ii}^{(b)}$. $\epsilon_{ii}^{(h)}$ is the hydrostatic strain, which has the form

$$\epsilon_{xx}^{(h)} = \epsilon_{yy}^{(h)} = \epsilon_{zz}^{(h)} = - \frac{P}{C_{11}^{Ge} + 2C_{12}^{Ge}} \quad (4)$$

where C_{11}^{Ge} and C_{12}^{Ge} are the elastic constants for Ge, and P is the applied hydrostatic pressure. The biaxial strain in the Ge layers is

$$\begin{aligned} \epsilon_{xx}^{(b)} = \epsilon_{yy}^{(b)} &= \frac{a^{Si}(P) - a^{Ge}(P)}{a^{Ge}(P)} \\ &= \frac{a_0^{Si} - a_0^{Ge}}{a_0^{Ge}} + \frac{a_0^{Si}}{a_0^{Ge}} \left[\frac{1}{C_{11}^{Ge} + 2C_{12}^{Ge}} - \frac{1}{C_{11}^{Si} + 2C_{12}^{Si}} \right] P \end{aligned} \quad (5)$$

where $a(P)$ is the lattice constant at pressure P and a_0 is the lattice constant at ambient pressure. Also

$$\epsilon_{zz}^{(b)} = - \frac{2C_{12}^{Ge}}{C_{11}^{Ge}} \epsilon_{xx}^{(b)} \quad (6)$$

Inserting Eqs. (4) - (6) into Eq. (3) gives

$$\Delta\omega_{\text{strain}} = \frac{1}{\omega_0} \left(q - p \frac{C_{12}^{Ge}}{C_{11}^{Ge}} \right) \left(\frac{a_0^{Si}}{a_0^{Ge}} - 1 \right) \quad (7)$$

which is the usual lattice mismatch correction due to the compressive strain in Ge layers at ambient pressure, which gives the $+15.8 \text{ cm}^{-1}$ contribution mentioned earlier, and

$$\begin{aligned} \delta\omega_{\text{strain}}(P) &= - \frac{p+2q}{2\omega_0(C_{11}^{Ge} + 2C_{12}^{Ge})} P \\ &+ \frac{1}{\omega_0} \frac{a_0^{Si}}{a_0^{Ge}} \left(q - p \frac{C_{12}^{Ge}}{C_{11}^{Ge}} \right) \left[\frac{1}{C_{11}^{Ge} + 2C_{12}^{Ge}} - \frac{1}{C_{11}^{Si} + 2C_{12}^{Si}} \right] P \end{aligned} \quad (8)$$

The first term is due to hydrostatic pressure applied to bulk Ge. The second term is due to the change in Ge and Si lattice constants with pressure because Ge and Si have different compressibilities; this results in a decrease in compressive strain in Ge layers with increasing pressure.

The Effect of Confinement

At ambient pressure, the confined Ge modes for an n -atom layer are at frequencies $\omega_c^{(m)}$, which are obtained approximately by zone folding the bulk LO dispersion curve at $k^{(m)} = m\pi/nd_0$ [7] where d_0 is the monolayer spacing and $m = 1, 2, \dots, n$. The $m = 1$ mode corresponds to the principal confined mode, which is at $0.5(2\pi/a)$ for the Ge layers of the SLS, where $a = 4d_0$ is the lattice constant. Consequently, ω_0 should be replaced by $\omega_c^{(1)}(k = \pi/a)$. Since the Grüneisen parameter γ varies across the bulk LO phonon dispersion curve, the pressure-dependent "bulk" contribution, which is the first term on the right hand side in Eq. (8), will be different for each confined mode. Using the notation introduced earlier, the changes in phonon frequency and Grüneisen parameter for a given confined mode can be treated as leading to perturbations from the $k = 0$ Raman shifts. Calculations suggest that γ for LO phonons decreases by ~ 0.044 [11] or ~ 0.059 [12] as k increases from 0 to π/a along (001) in Ge. Since the principal confined mode in the Ge layers is at π/a , the difference in $d\omega/dP$ between $k = \pi/a$ and $k = 0$ is estimated to be

$$\begin{aligned} \Delta\omega_{\text{confinement}}(P) &= 3P(\gamma\Delta\omega_{\text{confinement}} + \omega_0\Delta\gamma_{\text{confinement}})/(C_{11}^c + 2C_{12}^c) \\ &= \begin{cases} -0.028 P & \text{cm}^{-1} \text{ (for } \Delta\gamma = -0.044) \\ -0.034 P & \text{cm}^{-1} \text{ (for } \Delta\gamma = -0.059) \end{cases} \quad (9) \end{aligned}$$

where $\Delta\omega_{\text{confinement}} = -9.0 \text{ cm}^{-1}$ and P is in kbar. With $\gamma = -(p+2q)/6\omega_0^2$, p and q at $k = \pi/a$ can be obtained assuming either that p , q , and γ change proportionately from $k = 0$ to π/a or that $(p - q)/2\omega_0^2 = 0.23$, as for c-Ge. [10] In either case, it is seen that the effect of confinement on the second term in Eq. (8) is negligible.

Using the parameters in Refs. 10 and 13 for Si and Ge, $d\omega/dP$ for principal confined Ge mode in the Si/Ge SLS, and the zone center optic phonons in c-Ge and c-Si are expected to be 0.314, 0.355 and 0.481 $\text{cm}^{-1}/\text{kbar}$, respectively, excluding confinement effects. From Eq. (8), the effect of strain in the Ge layers is expected to decrease $d\omega/dP$ by 0.041 $\text{cm}^{-1}/\text{kbar}$ relative to c-Ge. Inclusion of the confinement effect using the first estimated value in Eq. (9) decreases the expected value of $d\omega/dP$ in the Ge layers of the SLS to 0.286 $\text{cm}^{-1}/\text{kbar}$, which is 0.069 $\text{cm}^{-1}/\text{kbar}$ lower than the c-Ge value. The second value in Eq. (9) gives $d\omega/dP$ that is 0.075 $\text{cm}^{-1}/\text{kbar}$ lower. Our corresponding

experimental values are 0.31 ± 0.03 , 0.37 ± 0.02 and 0.49 ± 0.02 $\text{cm}^{-1}/\text{kbar}$ for the SLS Ge, c-Ge and c-Si. This experiment shows that the effects of strain and confinement decrease $d\omega/dP$ in the Ge layers by 0.06 $\text{cm}^{-1}/\text{kbar}$ relative to that in c-Ge, which is within experimental error of the prediction. Our measured $d\omega/dP$ values for c-Si and c-Ge are in agreement with the values obtained using p and q , and with previously measured values 0.52 ± 0.03 $\text{cm}^{-1}/\text{kbar}$ for c-Si [14] and 0.385 ± 0.005 $\text{cm}^{-1}/\text{kbar}$ for c-Ge, [15] which included a P^2 term in analyzing $\omega(P)$. Including this P^2 term in our analysis brings our $d\omega/dP$ values even closer to those in Refs. 14 and 15.

As applied pressure is increased to the limit of 62.5 kbar applied here, Eq. 5 shows that the biaxial strain in the Ge layers decreases from $\sim 4.0\%$ to $\sim 3.3\%$. If the pressure were increased to the maximum possible before a phase transition occurs ($P \sim 110$ kbar), phase transitions occur at ~ 110 and ~ 125 kbar in Ge [15] and Si [14] respectively, the biaxial strain in Ge decreases to $\sim 2.8\%$ and remains compressive. As is true for Si/Ge structures, it is also generally found for other SLS's that the superlattice layer with the larger lattice constant is also the more compressible. Therefore the magnitude of biaxial strain initially decreases with pressure and, as in Si/Ge SLS's, the structure becomes more stable. In some structures, compressive layers will eventually become tensile with added pressure (and vice versa) and eventually they will become larger than the critical thickness and misfit dislocations will form.

In conclusion, the difference between $d\omega/dP$ for the principal quasi-confined LO mode in Ge layers in a Si/Ge SLS and that in bulk c-Ge can be explained by biaxial strain and confinement. The perturbation on $d\omega/dP$ for Ge due to confinement is comparable in magnitude and has the same sign as that due to strain. In contrast, confinement and strain lead to perturbations of roughly comparable magnitudes but opposite signs in the Raman frequency measurement at ambient pressure for the SLS studied here. With improved precision, the Grüneisen parameter for Si and Ge LO phonons from the Γ to the X point can be determined from Raman measurements of $d\omega/dP$ in Si_nGe_m SLS's on the [001] substrates for different n and m . Similarly, γ for LO and TO phonons propagating in other directions can be obtained using SLS's grown on substrates with different crystal orientations and the proper Raman polarization selection rules. This method can be used to determine the Grüneisen parameter for optical phonons with arbitrary wavevector in any bulk material by analyzing confined phonons in ultrathin layers of this material.

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WELL-RESOLVED BAND-EDGE PHOTOLUMINESCENCE FROM
STRAINED $\text{Si}_{1-x}\text{Ge}_x$ LAYERS GROWN BY
RAPID THERMAL CHEMICAL VAPOR DEPOSITION

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ABSTRACT

Well resolved band-edge luminescence of excitons in silicon-germanium alloy strained layers, quantum wells, and superlattices has been observed in films grown by Rapid Thermal Chemical Vapor Deposition. The signal is due to bound excitons at low temperatures and free excitons at higher temperatures, and has a strong no-phonon signal which is caused by alloy scattering. Bandgaps inferred from photoluminescence agree well with those measured by absorption spectroscopy, inferring that a no-phonon process dominates the band-edge absorption.

INTRODUCTION

The optical properties of silicon-germanium strained layers for potential application as optical emitters have recently been of extreme interest. Photoluminescence efficiencies of over 10% have been reported in strained layers (not superlattices) grown by MBE, but at energies substantially below the bandgap (~ 120 meV) and with a very broad linewidth (~ 80 meV) [1]. Theoretical work has predicted the possibility of achieving pseudo-direct gap structures by the zone-folding concept [2,3]. Experimental results on such structures [4,5] have been far from convincing and subject to dispute, however, in large part because of the high density of dislocations in those structures [6]. In this paper the first clearly identified optical transitions from the band-edges in strained silicon germanium structures with germanium fractions up to 0.4 is reported.

RAPID THERMAL CHEMICAL VAPOR DEPOSITION

The RTCVD technique is a combination of susceptorless lamp-heating and chemical vapor deposition, and is similar to Limited Reaction Processing (LRP) [7], except that the gas flow and not the wafer temperature is used to switch the growth reaction on and off. The growth is done at 6 torr in using dichlorosilane and germane in a hydrogen carrier. After chemical cleaning, a 1000°C H₂ bake and a 1000°C Si buffer layer, silicon layers are grown at 700°C and Si_{1-x}Ge_x at 600-625°C. The growth temperature is controlled to within a few degrees centigrade during growth by in-situ measurement of the infrared absorption in the silicon substrate [8]. The structure of all samples reported in this paper was confirmed by x-ray diffraction and/or transmission electron microscopy (TEM). All samples were fully strained to match silicon substrates with threading dislocation densities ~ 10³/cm⁻² and misfit dislocation spacing ≥ 10 μm. Other growth system details can be found in ref. 9. The degree of control made possible by the technique is demonstrated by a cross-section TEM of a 50 period Si(23 Å)/Si_{0.82}Ge_{0.18} (23 Å) superlattice in which the individual layers are clearly resolved (fig. 1).

PHOTOLUMINESCENCE SPECTRA

A typical low temperature (2K) photoluminescence (PL) spectrum (in this case for a sample with 10 isolated 29 Å Si_{0.82}Ge_{0.18} quantum wells) is shown in fig. 2. The excitation was provided by an Ar⁺ laser with a spot size of several mm, and a power density from 1-10 W/cm². The spectrum is most easily interpreted by comparing it to results on bulk unstrained Si_{1-x}Ge_x, which have been studied previously in great detail [10]. The highest energy signal is due to non-phonon (NP) recombination of bound excitons, and the lower energy signals are due to phonon-assisted recombination (phonon replicas). By comparison with the work of Weber and Alonso [10], the phonons may be identified as the transverse acoustic (TA) and the transverse optical (TO) phonons. The TO is separated into three peaks corresponding to the different local vibrational nodes depending on nearest neighbor pairs. The phonon energies (difference between the NP signal and the phonon replicas) are in excellent agreement with the previous bulk alloy results, implying that strain has little effect on the phonon dispersion curves. The FWHM of the NP line is ~ 5 meV, which agrees well with the previous best reported results in bulk alloys of ~ 4 meV [10], implying good uniformity throughout the films. The linewidths are an order of magnitude wider than those in silicon because of the random alloy nature of the films.

At higher germanium fractions, the PL energies are reduced because of the lower bandgap, but the TO phonon energies do not change within the experimental resolution. At higher germanium fractions, however, the relative intensity of the various TO phonon replicas changes to reflect more Ge-Ge and fewer Si-Si bonds. The spectra in uniform films, quantum wells, and superlattices (period > 45 Å) are also qualitatively similar, except for the appropriate quantum confinement increase in the bandgap. For narrow wells however (< 30 Å) the relative strength of the TO replicas is shifted towards a lower x than is representative of the composition of the well only [11]. This is thought to be due to the

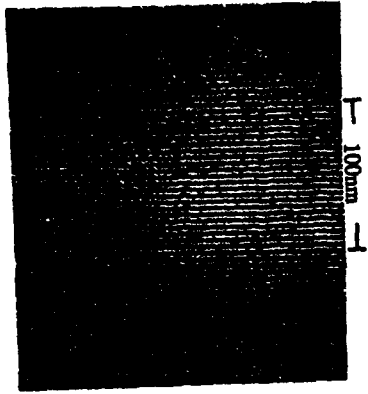


Fig. 1. Cross section TEM of a 50 period 23 Å Si/23 Å $\text{Si}_{0.82}\text{Ge}_{0.18}$ superlattice.

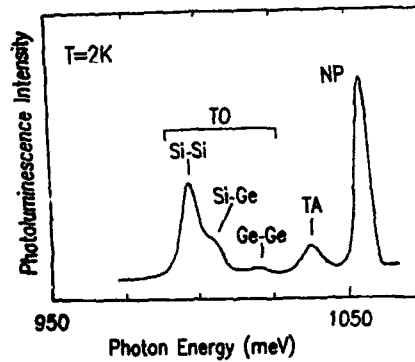


Fig. 2. 2K photoluminescence spectrum of a sample with 10 isolated strained $\text{Si}_{0.82}\text{Ge}_{0.18}$ -23Å quantum wells.

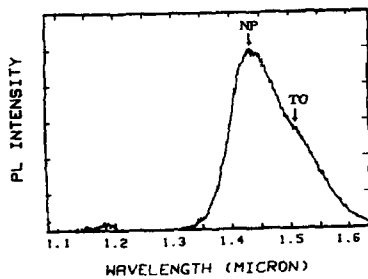


Fig. 3. 77K photoluminescence spectra of a sample with a single strained $\text{Si}_{0.8}\text{Ge}_{0.4}$ quantum well (~ 80 Å).

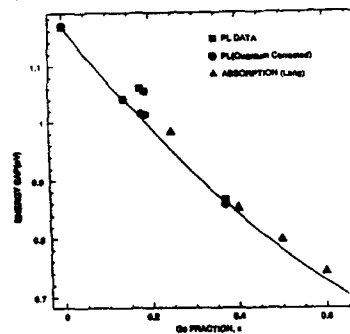


Fig. 4. Bandgap of strained $\text{Si}_{1-x}\text{Ge}_x$ as determined by the NP PL line. The data has been corrected for quantum confinement effects (indicated) and excitonic binding energies, and adjusted to give the bandgap at 0 K. Also shown is the bandgap determined by photocurrent spectroscopy (Lang [13]) (adjusted to 0 K).

fact that the exciton wavefunction penetrates substantially into the Si barriers, so that some fraction of the phonon-assisted radiative recombination actually takes place in the silicon.

Similar well-resolved band-edge luminescence of strained $\text{Si}_{1-x}\text{Ge}_x$ layers has been reported for single $\text{Si}_{1-x}\text{Ge}_x$ layers grown by MBE only for germanium fractions up to $x = 0.04$ (4% Ge) [12], and not at all for superlattices. At present it is not known why such spectra have not been reported by MBE for larger germanium fractions.

At higher temperatures (> 20 K), the excitons are no longer bound to shallow impurities and become free excitons. The spectra remain similar, except for shifts in energy due to temperature dependence of the bandgap, the exciton binding energy, and thermal broadening [11]. Typical spectra at 77 K, in the case of a single $\text{Si}_{0.6}\text{Ge}_{0.4}$ quantum well, are shown in fig. 3. The various phonon replicas have broadened to form a single peak, and the strong NP line is still present. This NP line of the free excitons is of great interest. While it is sometimes observed with bound excitons in silicon (due to localization of the exciton), it is not observed for free excitons in silicon due to the indirect bandgap. The NP free exciton signal is strong in our samples, however, and increases as the Ge fraction is raised to $x = 0.4$. (Contrast, for example, the relative NP/TO strengths in figure 2 ($x = 0.2$) vs. figure 3 ($x = 0.4$)). Similar results have been reported in bulk unstrained alloys [10]. This signal is not due to superlattice or zone folding effects but simply due to the *random* nature of the alloy [13]. The randomness breaks the translational symmetry of the lattice, with the result that crystal momentum k is no longer a "good" quantum number. Therefore an electron in the indirect conduction band valley also possesses some k component at all other k 's, including $k=0$ for a NP transition. As x increases towards $x = 0.5$, this randomness and hence the NP strength should increase. This random nature of the Si and Ge atomic location is also what physically causes alloy scattering.

BANDGAP AND COMPARISON TO ABSORPTION DATA

By observing the NP line as a function of composition, the bandgap of the $\text{Si}_{1-x}\text{Ge}_x$ alloys can be determined (fig. 4). This is in principle more precise than absorption measurements such as those by Lang [14] since the absorption energy edge may differ from the true band-edge in indirect materials because phonon emission or absorption may be required for an optical transition. The actual data plotted in ref. 14 is the measured absorption edge, with no correction made for phonon energies. The excellent agreement between the reported absorption edge of ref. 13 and the true bandgap as measured by PL in the strained silicon-germanium alloys implies that the dominant optical absorption process in $\text{Si}_{1-x}\text{Ge}_x$ alloys is by a no-phonon process. This is consistent with the observed PL spectra since absorption is the inverse of the photon-emission process. Dominant no-phonon absorption in the alloys is however in direct contradiction with one of the major conclusions of Braunstein et al. [15], which is commonly accepted to give the bandgap of the relaxed $\text{Si}_{1-x}\text{Ge}_x$. This work concluded that optical absorption in the alloys proceeded by a phonon-assisted process, and then subtracted a phonon-energy to the measured absorption edge to obtain the bandgap.

Our work then suggests that the relaxed bandgap energies reported in [15] are underestimated by a phonon energy or some weighted average of various phonon energies.

It has been assumed for several years that the bandgap offset in strained $\text{Si}_{1-x}\text{Ge}_x$ alloys on bulk Si is of type I configuration for small x [16] (up to $x = \sim 0.7$ according to Ref. 17), while that of relaxed $\text{Si}_{1-x}\text{Ge}_x$ vs. strained Si is type II (lower E_C in the Si) [18]. Recently, however, optically detected magnetic resonance experiments have suggested that strained $\text{Si}_{0.65}\text{Ge}_{0.35}$ on relaxed Si might already be type II, although the strain of the superlattice was not made clear and the results were not conclusive [19]. If the type II case were assumed for our samples, the PL measurements at $x \sim 0.4$ would measure an energy less than that of the bandgap, and certainly less than the absorption edge independent of whether phonon emission was part of the absorption process. To within the resolution of our measurements (± 30 meV due to uncertainties in the well width and hence the confinement energy), this was not observed.

CONCLUSION

Well resolved band-edge photoluminescence of excitons in single strained $\text{Si}_{1-x}\text{Ge}_x$ layers, quantum wells, and superlattices with $x = 0.4$ has been reported for the first time. The spectra are characterized by a NP transition and various phonon replicas. Comparisons with absorption measurements suggest that the dominant absorption in $\text{Si}_{1-x}\text{Ge}_x$ alloys is by a no-phonon process. That such well-resolved PL signals are observed also confirms the excellent minority carrier properties and uniformity of $\text{Si}_{1-x}\text{Ge}_x$ layers grown by Rapid Thermal Chemical Vapor Deposition.

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Ge_xSi_{1-x} WAVEGUIDES GROWN BY RAPID THERMAL PROCESSING CHEMICAL VAPOR DEPOSITION

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ABSTRACT

We report the growth and characterization of Ge_xSi_{1-x} films for optical waveguiding. Ge_xSi_{1-x}/Si waveguides were grown by rapid thermal processing chemical vapor deposition. An average attenuation of 3.3 dB/cm was achieved for a 1 μm thick Ge_{0.04}Si_{0.96} layer patterned into rib waveguides 2000 Å deep with widths of 5 μm. Directional couplers were also fabricated. Average coupling efficiencies of 85% were achieved for 1.5 μm interwaveguide separation.

INTRODUCTION

Optoelectronics has been the subject of considerable research. Historically, III-V compounds have played the dominant role in optoelectronics. However, due to advances in growth technology and material understanding, the Ge_xSi_{1-x} materials system [1] has opened up numerous opportunities for Si-based optoelectronic applications such as photodetection, waveguiding, and optical modulation. Recently, interest has focused on Ge_xSi_{1-x} as a waveguiding material for Si-based optoelectronics [2-4]. Waveguides can be formed by Ge_xSi_{1-x} layers grown on Si by utilizing the change in refractive index between the two materials. The use of crystalline Ge_xSi_{1-x} offers the prospects of further vertical device integration, hence incorporation into device structures is possible.

Soref *et al.* [2] have demonstrated waveguiding in 10 μm Ge_{0.1}Si_{0.9} layers grown by conventional chemical vapor deposition (CVD) at 1100°C with losses as low as 1.9 dB/cm for TM polarization. Schüppert *et al.* [3] have demonstrated waveguiding in Ge_{0.27}Si_{0.73} layers formed by diffusion at 1200°C for 69 hrs with losses of 4 dB/cm for TE polarization. Splett *et al.* [4] have demonstrated waveguiding in 3.45 μm Ge_{0.01}Si_{0.99} layers grown by molecular beam epitaxy (MBE) at 550°C with losses of 3-5 dB/cm for TE polarization. Each of the prior techniques, however, has involved processes which are of low throughput or which involve relatively long exposure to high temperatures.

We have utilized the refractive index difference between Ge_xSi_{1-x} and Si to fabricate Ge_xSi_{1-x} waveguides on Si substrates. The Ge_xSi_{1-x} films were grown by rapid thermal processing chemical vapor deposition (RTPCVD) [5]. RTPCVD, similar to the techniques of limited reaction processing [6] and rapid thermal chemical vapor deposition [7], has received considerable attention because of its ability to reduce many of the processing problems associated with thermal exposure in conventional chemical vapor deposition, such as autodoping, outdiffusion, and the inability to reproducibly grow thin layers. At the same time, RTPCVD can achieve high crystalline perfection and dopant activation while minimizing the degradation of the dopant transition profile. The principles and advantages of RTPCVD are described in greater detail elsewhere [8]. We have previously demonstrated the ability of RTPCVD to grow high quality epitaxial Si [8] and Ge_xSi_{1-x} [9] films.

EXPERIMENT

The substrates used were phosphorus-doped (100)Si wafers with resistivities of 8-12 Ω -cm. The wafers were cleaned *ex-situ* by etching in dilute HF, rinsing in deionized water, and blow-drying with N_2 prior to loading into the chamber. The chamber was then pumped down to a base pressure of 5×10^{-4} mbar. An *in-situ* H_2 pre-bake was performed for 60s at temperatures of 800°C to 1000°C using a flow of 1 lpm. The chamber processing pressure was 5 Torr. After the pre-bake, the source gases were introduced into the chamber. H_2 was used as the carrier gas while SiH_2Cl_2 and GeH_4 were used as the Si and Ge source gases. Deposition temperatures of 900°C and 1000°C for 1 min to 3 min were used. Defects in the Ge_xSi_{1-x} layer were characterized by Nomarski optical microscope and transmission electron microscopy (TEM). Film thickness was also determined by TEM micrographs. Ge fraction and strain were determined by high resolution x-ray diffraction (HRXRD).

Both slab and rib waveguides were studied. The waveguide structures were patterned by conventional photolithography techniques and etched by reactive ion etching (RIE). Optical measurements were performed by end-fire coupling light into the edge of the polished rib structures with a microscope objective. The near field optical beam intensity was measured and recorded using a Ge photodiode, a lock-in amplifier, and a plotter. Optical losses were determined using the Fabry-Perot interference technique [10].

RESULTS AND DISCUSSION

The material and waveguiding properties of the samples studied are summarized in Table I. The defect densities listed are for defects in the epitaxial layer that have propagated to the surface and do not include misfit dislocation densities. Since our processing was not performed in a clean room environment and no RCA clean was done before loading the wafers into the chamber, the defect densities can be expected to be no better than 10^2 - 10^3 cm^{-2} . The Ge fractions of sample #3 has not been measured, but is greater than 1%.

Single TM guiding was observed for $\lambda = 1.52$ μm . All samples were grown at 900°C except for sample #1. The samples were 40% to 70% strained. Relaxation in samples #1, #4, and #5 occurred primarily through misfit dislocation formation. Defects consisted of misfit dislocations and threading dislocations. On the other hand, relaxation in samples #2 and #3 was due primarily to a high density of stacking faults. No misfit dislocations were observed in samples #2 and #3, although threading dislocations were observed. The density of threading dislocations was much lower than the stacking fault density. Significant changes in defect densities were achieved by deliberately utilizing H_2 pre-clean conditions which produced significant surface damage to the Si surface prior to epitaxial growth [11]. Therefore, in the discussion below, scattering loss due to defects is also associated with heterointerface roughness.

Table I. Summary of samples.

Sample#	Deposition Temperature (°C)	Defect Density (cm^{-2})	SiH_2Cl_2/GeH_4 Flow Rate	Ge Fraction (%)	Thickness (Å)	Guiding
1	1000	3×10^4	20/0.46	5	4000	good
2	900	2×10^8	20/0.23	1	5000	poor
3	900	6×10^8	15/0.3	--	5000	fair
4	900	8×10^5	20/0.5	4	10000	very good
5	900	2×10^4	20/0.5	4	10000	excellent

At higher deposition temperatures ($\geq 1000^\circ\text{C}$), however, surface mobility of adsorbed reactants is sufficiently high to overcome the surface damage and epitaxial quality improves.

Waveguiding loss is described only qualitatively for slab waveguides in Table I. Actual loss measurements were made for samples #4 and #5, with the further results discussed below. For comparison, the average loss for sample #4 was 5.5 dB/cm while sample #5 had an average loss of 3.3 dB/cm. Samples #4 and #5 were identical except for defect densities. Since the difference in defect densities was generated by differences in surface damage, the loss is due to a combination of scattering from threading dislocations and $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ interface roughness. The increase in loss was surprisingly small, considering that an order of magnitude difference in defect densities occurred.

We were surprised to detect any semblance of guiding in samples #2 and #3, considering that defect densities were so high and the layers were only half a micron thick. Guiding is better for sample #3, which has a slightly higher Ge fraction with comparable defect density. Our results suggest that $\text{Ge}_x\text{Si}_{1-x}$ waveguides are relatively forgiving in terms of defect/heterointerface scattering loss. Lower defect densities, of course, do still lower waveguide loss as demonstrated by samples #4 and #5. For the processing window described in Table I, guiding is observed to improve significantly when slab thickness is increased (compare samples #1 and #4), even though the defect density is higher and the Ge fraction is slightly smaller.

Rib waveguides were fabricated from samples #4 and #5. The results presented below are for sample #5. As mentioned previously, the loss for sample #4 is higher. Figure 1 shows a schematic of the rib waveguide structure and also a Nomarski micrograph of a cross-section of

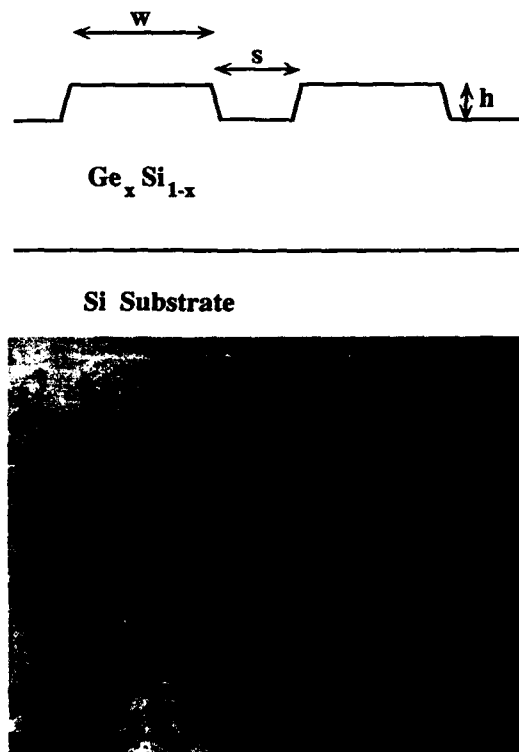


Figure 1: Schematic (top) and Nomarski micrograph (bottom) of waveguide cross-section.



Figure 2: Photograph of single mode (right) and multi-mode (left) waveguiding.

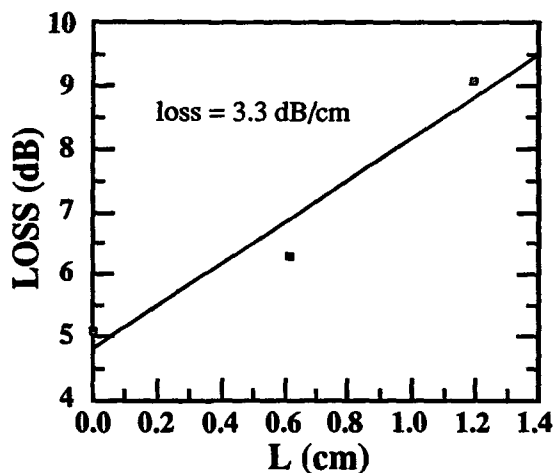


Figure 3: Plot of loss as a function of waveguide length.

the rib waveguide. Note that in Figure 1, overetching of the rib structure was deliberately performed so that the waveguide could be resolved by the microscope. Actual rib heights were 2000 Å. Single mode guiding was observed for rib widths of $\leq 5 \mu\text{m}$. Second order modes were observed for $10 \mu\text{m}$ widths. Single mode and multi-mode guiding are shown in Figure 2. Figure 3 shows a plot of waveguide loss as a function of waveguide length, indicating an average loss of 3.3 dB/cm. The data point for zero length is a theoretical extrapolation.

Sample #5 was also patterned into the simple directional coupler structure shown in Figure 4 (note that the micrograph also shows straight waveguides as well). An interaction length (L) of 3 mm was used with a rib waveguide width of $5 \mu\text{m}$. Figure 5 is a semi-log plot of percentage of power coupled from one arm into another arm. Average coupling efficiencies ($P_2/(P_1+P_2)$) are 75% to 85%, depending on interwaveguide separation. The change in average coupling efficiency with interwaveguide spacing is approximately $-8\%/ \mu\text{m}$. An interwaveguide gap of $3 \mu\text{m}$ exhibits a transfer length of 0.46 cm and a coupling coefficient of 3.4 cm^{-1} . An interwaveguide gap of $1.5 \mu\text{m}$ exhibits a transfer length of 0.41 cm and a coupling coefficient of 3.9 cm^{-1} . Thus, the coupling coefficient changes by 0.17 cm^{-1} for each $0.5 \mu\text{m}$ change in interwaveguide spacing and the transfer length depends directly on interwaveguide spacing. The coupling coefficient and transfer length were calculated assuming identical waveguides and neglecting coupling near the Y-shaped bend region.



Figure 4: Plan-view Nomarski micrograph of couplers.

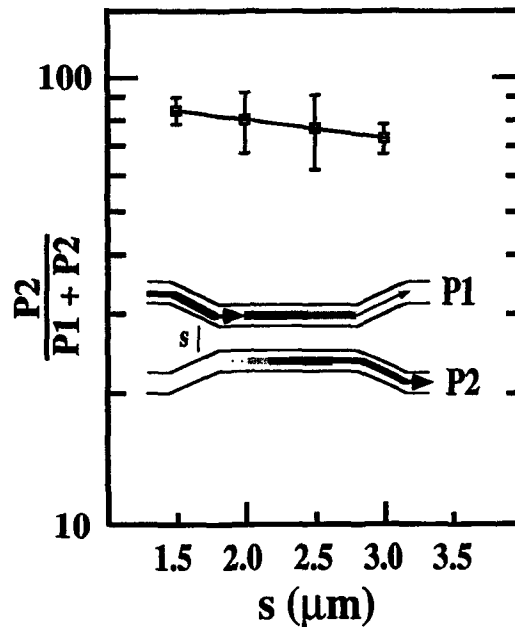


Figure 5: Plot of coupling efficiency as a function of interwaveguide spacing.

SUMMARY AND CONCLUSIONS

We have demonstrated the ability of RTPCVD to grow high quality $\text{Ge}_x\text{Si}_{1-x}$ films for waveguiding. An average waveguiding loss of as low as 3.3 dB/cm at 1.52 μm for TM polarization has been achieved for rib structures. Although our losses are not as low as for dielectric waveguides, the use of crystalline materials opens opportunities in device and circuit integration. Optimization of material quality and parameters (Ge fraction, film thickness, etc.) as well as waveguide dimensions and processing is expected to further decrease waveguide loss.

In addition, we have demonstrated coupling of light between waveguides. Average coupling efficiencies of as high as 85% for an interwaveguide spacing of 1.5 μm have been achieved. Our results indicate that the waveguiding properties of $\text{Ge}_x\text{Si}_{1-x}$ are promising for further device and circuit integration. The $\text{Ge}_x\text{Si}_{1-x}$ layer can serve as the waveguiding structure in a $\text{Ge}_x\text{Si}_{1-x}$ modulator or as a waveguide for integration with a $\text{Ge}_x\text{Si}_{1-x}$ photodetector.

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THE SELECTIVE EPITAXY OF SILICON AT LOW TEMPERATURES

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ABSTRACT

Low-temperature selective epitaxial growth (SEG) of silicon using a dichlorosilane-hydrogen mixture in an LPCVD hot-wall reactor has been discussed with respect to the wafer preparation and the deposition cycle. The surface morphology and the quality of epilayers are strongly affected by residual oxide islands at interface. A reduction of local growth rate near interfacial oxides is attributed to the dissolution of oxide at interface, and this reduction can lead to pits and textured features on the Si epitaxial surface. An ex-situ HF vapor or an HF dip with an in-situ small DCS 900°C prebake step can completely remove surface oxide prior to the deposition and achieve defect-free Si epilayers at the deposition temperatures of 850°C and 800°C. It is also found that fluorine atoms can play a major role in the removal of surface oxide.

INTRODUCTION

Selective epitaxial growth (SEG) of silicon at low temperatures is a new and important manufacturing technology for submicron ULSI applications [1-4]. The SEG of silicon requires three main process steps -- one oxidation for isolation, one plasma etching step to define epitaxial windows, and one LPCVD epitaxial step to grow Si layers. The quality of epilayers is highly controlled by the wafer preparation and the deposition cycle. Improper wafer preparation or deposition cycles can result in defective epilayers that show undercuts, microtwins, dislocation loops, threading dislocations, and interfacial oxide islands. It is found in our experiments that the plasma-etch-induced surface defects and contaminants can lead to defective epilayers. Therefore, one of the goals of this paper is to understand the formation of defective epilayers resulted from the plasma etching step, and then modify the wafer preparation to get high quality epilayers. Our previous studies [5-6] have shown that an ex-situ HF vapor treatment and an in-situ low dichlorosilane (DCS) prebake can improve the surface oxide removal, and achieve defect-free epilayers at low deposition temperatures. In this paper, we employ F⁺ ion implantation to model the removal of the fluorinated surface oxide during the 900°C prebake. Pits and textured features on the surface of Si epilayers are observed near the wafer periphery, and, according to process condition, sometimes in prime wafer sites. We found that these surface features are associated with residual patches of oxide at the substrate surface. For that reason, the third goal of this paper is to understand the formation of pits and textured features on the surface of epilayers, as well as show the relationship between surface preparation, deposition temperature, and reaction conditions on the quality of epilayers.

EXPERIMENTAL PROCEDURE

The epitaxial substrates are boron-doped (100) Si wafers of resistivity 30-50 ohm-cm. A photolithographic step was used to define the bare and oxide-covered regions on a 570 nm thermal oxide layer grown at 1000°C. The oxide was plasma etched in a LAM 590 AutoEtch system using He+CHF₃+CH₄ gases. The plasma etch process is continued to reach to a depth of 40 nm below the Si/SiO₂ interface. After the plasma etching and the photoresist removal, sacrificial oxide films are grown at 900°C. The wafers are then subject to a pre-epitaxial clean step consisting of two piranha cleaning treatment separated by a dilute HF dip that removes the sacrificial oxide. Subsequently, the wafers were exposed to the HF vapor over a 1:2 mixture of H₂O:49% HF for 5

seconds to remove the chemical oxide and passivate the wafer surface, then immediately loaded into a horizontal hot-wall reactor at 525°C. Controlled wafers with no sacrificial oxide film growth or HF vapor treatment have also been prepared. The deposition cycle for different growth temperatures is shown in Fig. 1. All wafers are prebaked at either 1000°C or 900°C in a 6 torr H₂ ambient prior to the deposition. The deposition is achieved in a mixture of 7.4% DCS in H₂ at 0.6 torr. In most runs a low-concentration of DCS (0.025%) is applied during the prebake and the ramp-down periods.

The surface morphology of epilayers are inspected by Nomarski microscopy and scanning electron microscopy (SEM). Crystallographic defects are studied by cross-sectional transmission electron microscopy (XTEM), as well as Nomarski inspection following a the dilute Schimmel etch⁷. The profiles of impurities in epilayers are determined by secondary ion mass spectroscopy (SIMS) analysis.

RESULTS AND DISCUSSION

PLASMA ETCH EFFECTS

In the absence of a sacrificial oxide, epilayers deposited at 850°C after a 1000°C prebake show precipitates and dislocation loops at the epi/substrate interface, as well as microtwins and threading dislocations in the epilayer. An example of an XTEM micrograph of such a sample is illustrated in Fig. 2(a). The defects are attributed to ion-bombardment-induced defects and reactive-ion-induced surface contaminants. During the 1000°C prebake step, simple intrinsic lattice defects would be expected to anneal out. However, reactive-ion-induced impurities just below the surface may either nucleate precipitates or move to dislocation loops to freeze the shrinkage of these dislocations near the Si surface. In order to remove the plasma-etch-induced defects and imbedded contaminants, a 25 nm sacrificial oxide is grown at 900°C and subsequently removed. As shown in Fig. 2(b), a high quality epilayer, albeit with undercuts near the corners of epitaxial windows, results. It is believed that the plasma-etch-induced defects and surface contaminants are incorporated into the sacrificial oxide layer and subsequently removed during the HF dip to leave a clean defect-free Si surface for the deposition. More recently, it is found that a 5 nm 900°C grown sacrificial oxide is thick enough to remove the plasma-etch-induced damage; Fig. 3 shows an XTEM of such a sample. In this case the prebake were performed at 900°C, and no undercut is observed.

PREBAKE TEMPERATURES AND THE EFFECT OF A SMALL CONCENTRATION OF DCS

The removal of surface oxide prior to the deposition determine the quality of epilayers. High temperature prebake (e.g., above 1000°C) leads to undercuts, as shown in Fig. 2. It is believed⁸ that these undercuts are attributed to the decomposition of SiO₂ at the SiO₂/Si substrate interface in H₂. Undercuts also result in rough edges at epi/SiO₂ boundaries. In order to avoid the formation of undercuts, a 900°C prebake is employed. To get high quality epitaxial growth with a 900°C prebake, we found it necessary to add a low concentration of dichlorosilane (DCS) in the prebake and the ramp down steps⁶. The XTEM of Fig. 3 is an example of a defect-free film thus obtained. If the prebake or preclean is inadequate, an epilayer with dense oxide islands at the epi/substrate interface and threading dislocations in the epilayer results; an example is shown in Fig. 4. SIMS analysis in Fig. 5 indicates large O, C, and F peaks at the epi/substrate interface.

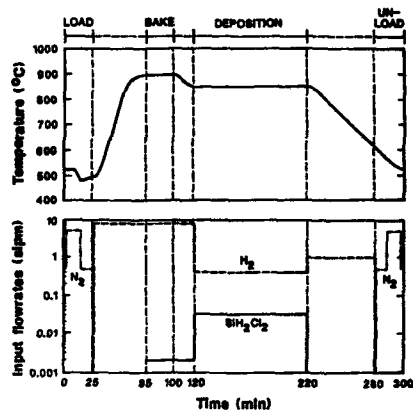


Fig. 1 The standard deposition cycle for the selective epitaxial growth at 850°C. T_1 is the time to add a small DCS.

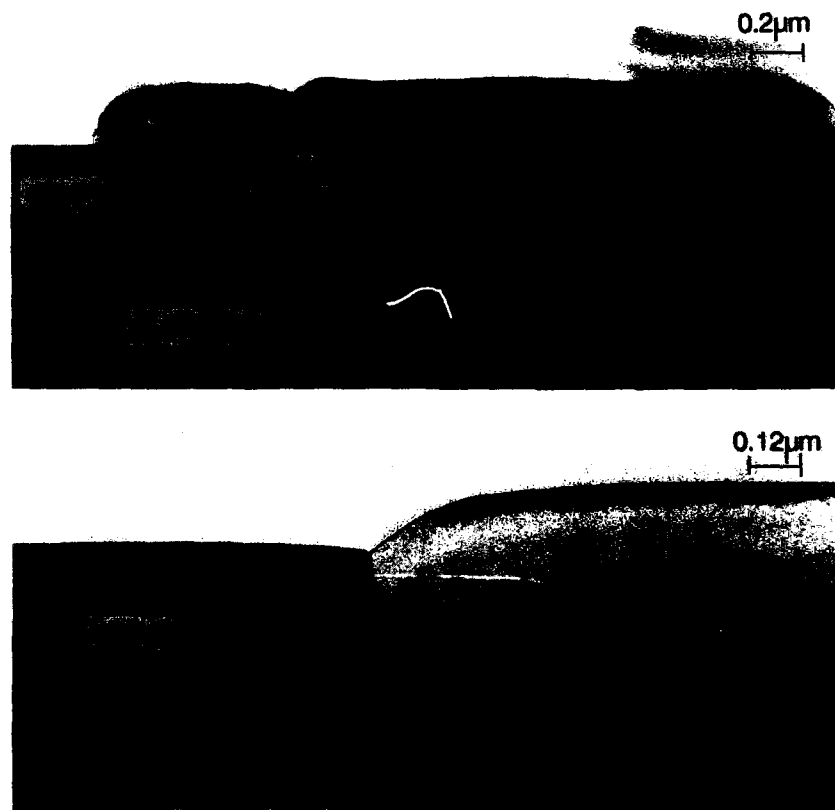


Fig. 2 XTEM micrographs of epilayers deposited at 850°C after a 1000°C prebake. (a) With no sacrificial oxide, the epilayer is defective. (b) With a 25 nm sacrificial oxide, it shows a large undercut but no defect in the epilayer.



Fig. 3 With a 5 nm thin 900°C grown sacrificial oxide, the XTEM micrograph shows a defect-free epilayer deposited at 850°C after a 900°C prebake. An ex-situ HF vapor treatment and an in-situ small DCS are applied.



Fig. 4 A small DCS is applied in the prebake and ramp-down periods. In the absence of the HF vapor treatment, the epilayer is defective with interfacial oxide islands and threading dislocations.

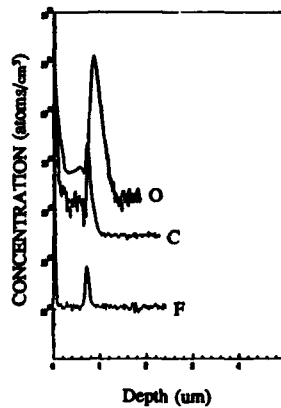


Fig. 5 SIMS results of the defective epilayer in Fig. 4. It shows large O, C, and F peaks at the epi/substrate interface.

FLUORINE INCORPORATION

As noted above, if the ex-situ/in-situ oxide removal is inadequate, there are dense oxide patches on Si surface prior to the deposition. Such oxide patches lead to textured Si epilayers. In order to completely remove these oxide films to achieve high quality Si epilayers, an HF vapor treatment is applied before the loading of wafers into the reactor [5]. Nomarski micrographs show a high quality Si epilayer with specular surface morphology and smooth pattern edges; an example is given in Fig. 6. Furthermore, oxide areas are completely free of Si nuclei. The XTEM micrograph in Fig. 3 shows no oxide islands at the epi/substrate interface, no threading dislocations in the epilayer, and no undercuts near the corners of SiO₂/substrate interface. SIMS analysis indicates no oxygen, carbon, or fluorine peaks at the epi/substrate interface. A dilute Schimmel etch reveals no extra etched pits either in the film or at the epi/substrate interface. Consequently, with adequate removal of interfacial oxide a defect-free Si epilayer deposited at 850°C after a low DCS 900°C prebake is achieved.

The Si surface is known to be passivated after the HF vapor treatment. The presence of a hydrogen- and fluorine-terminated Si surface can retard the oxidation [9-11]. During furnace insertion at 500°C and during the ramp-up step, the reactivity of Si surface with the residual oxidants increases with the temperature because of the passivation desorption. As a result, a thin surface oxide film (several nm) is formed while fluorine atoms may desorb out of the Si surface, diffuse into the surface oxide film, or stay at the SiO₂/substrate interface. Fluorine atoms in the surface oxide may cleave Si-O bonds to form Si-F bonds that may further form volatile SiF₄ [12-13] and create more small holes in the surface oxide. Such a porous fluorinated surface oxide film would favor the invasion of hydrogen to catalyze the reduction of the surface oxide.

In order to reveal the fluorine incorporation induced effect on the surface oxide removal, an F⁺ ion implantation experiment was performed. Wafers were patterned with conventional photolithography and photoresist used as mask for the ion implantation. F⁺ ions were implanted into (100) Si wafers at 20 Kev with a dose of 10¹³/cm², 10¹⁴/cm², and 10¹⁵/cm², respectively. With the same wafer preparation and the deposition cycle as those received by the epilayer in Fig. 4, Nomarski micrographs show textured surface morphology on implanted and un-implanted regions for the flux of 10¹⁴/cm² or less. However, for the flux of 10¹⁵/cm², as shown in Fig. 7(a), specular epilayers on implanted regions but textured epilayers on un-implanted regions are observed. The XTEM micrograph in Fig. 7(b) further shows the interface between the implanted and un-implanted regions. It indicates a defect-free epilayer on the implanted region, but a defective epilayer, similar to Fig. 4, with a high density of interfacial oxide islands, voids and dislocations on the un-implanted region. Again, for the same specimen, SIMS analyses of un-implanted regions indicate large oxygen, carbon, and fluorine peaks at the epi/substrate interface. However, no oxygen, carbon, or fluorine peak is observed on the F⁺ implanted regions.

SURFACE MORPHOLOGY

For epilayers deposited at 850°C after a 900°C prebake, with an ex-situ HF vapor treatment and the addition of a concentration of small DCS in the ramp-down step only, pits are observed near the centers of the wafers, and a textured surface is observed near the peripheral areas of epitaxial wafers. SIMS analysis shows an oxygen peak of 4×10^{18} /cm³ in the areas with pits. It is believed that these pits are oxide-related. The XTEM micrograph in Fig. 8(a) shows an interfacial oxide inclusion beneath the pit. The oxide island is about 85 nm wide and 7 nm thick, much smaller than the size of the concave pits (about 1 μm wide, 100 nm thick). Moreover, we also find many smaller oxide inclusions not leading to observable surface pits. The critical dimension of interfacial oxide islands below which pits are not observed on the surface of this epilayer is about 40 nm. A 2 minute Dilute Schimmel etch (etching rate ~ 400 nm/min), shows many extra etch pits near the epi/substrate interface (the epi thickness is 0.7 μm), and further consistently reveals the smaller oxide inclusions at the epi/substrate interface. In Fig. 8(b) the XTEM of textured areas, where SIMS analysis indicates a peak of oxygen in the range of 10²⁰/cm³, shows a semi-continuous interfacial oxide film, a high density of threading dislocations originating at the epi/substrate

Fig. 6 With the HF vapor treatment as well as a small DCS in the 900°C prebake and ramp-down steps, Nomarski micrograph shows a specular epilayer with smooth pattern edges.

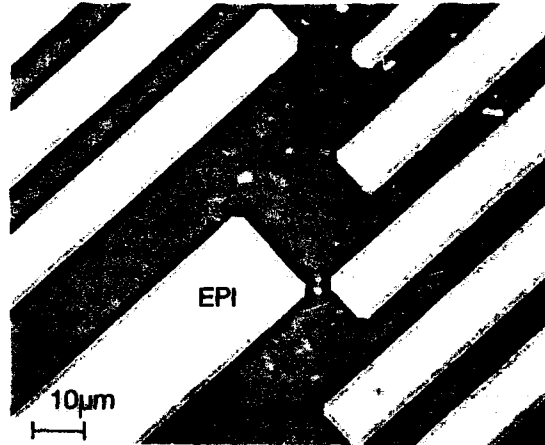
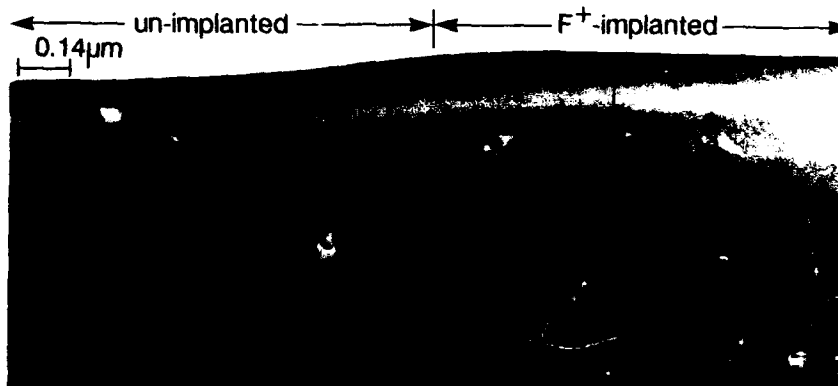


Fig. 7 In the absence of an HF vapor treatment, with an F^+ ion implantation ($10^{15}/\text{cm}^2$, 20 Kev) and a small DCS in the 900°C prebake and the ramp-down steps, (a) The Nomarski micrograph (1000x) shows specular epilayers on F^+ implanted regions but textured epilayers on un-implanted regions. (b) The XTEM micrograph shows a defect-free epilayer on F^+ implanted region but a defective epilayer on un-implanted region.



interface, and interfacial voids. The voids could be generated by the decomposition of buried or near-buried oxide inclusions during the deposition, or be the result of the coalescence of two un-aligned growth fronts.

An oxygen-ion-implantation was performed to study the possibility of oxygen in surface morphology. Wafers were patterned and the photoresist used as a mask for an O^+ ion implantation at 20 Kev. With a large diffusivity of $8 \times 10^{-5} \text{ um}^2/\text{sec}$ at 850°C [14], the implanted oxygen atoms can diffuse from the substrate into the Si epilayer during the Si epitaxial growth. For doses of $10^{13}/\text{cm}^2$ or greater, a difference in growth rate on implanted and un-implanted regions is observed, as shown in Fig. 9. Apparently, the incorporation of oxygen can retard the Si epitaxial growth rate. Thus the formation of pits and textured features on the surface of epilayers may be owing to the oxygen effect resulting from the dissolution of the interfacial oxide islands. As mentioned above, with an HF vapor treatment and a small DCS during the 900°C prebake and the ramp-down periods, surface oxide can be completely removed and a defect-free epilayer can be achieved.

CONCLUSIONS

The selective epitaxy of Si at low temperatures is studied. A sacrificial oxide growth is found necessary to remove the plasma-etch-induced surface damage and contaminants. A 5 nm 900°C -grown sacrificial oxide is adequate. A low concentration of DCS applied in the 900°C prebake and the ramp-down steps can improve the epitaxy of Si. This cycle, combined with an ex-situ HF vapor treatment, presents defect-free epilayers to be deposited at low temperatures. The formation of pits and textured morphology on the surface of SEG silicon layers is related to interfacial oxide islands. The formation of these surface features may result from the local depression of the Si growth rate owing to the dissolution of interfacial oxide islands. It is also found that with a 900°C prebake, a F^+ ion implantation can produce a clean Si surface for the subsequent epitaxial growth, and result in defect-free epilayers. A possible model to explain the surface oxide removal attributes weak points in the interfacial oxide to fluorine; accelerating its removal in H_2 . High quality Si epilayers can be obtained as low as 800°C in our reactor.

ACKNOWLEDGEMENTS

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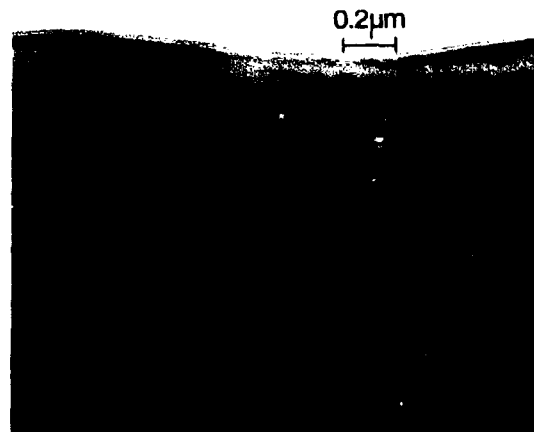


Fig. 8 (a) An XTEM micrograph of the epilayer with dense pits on the surface. This concave pit is centered above a thin interfacial oxide island. (b) An XTEM micrograph of the epilayer with textured surface features. It shows dense interfacial oxide islands, threading dislocations, and voids.

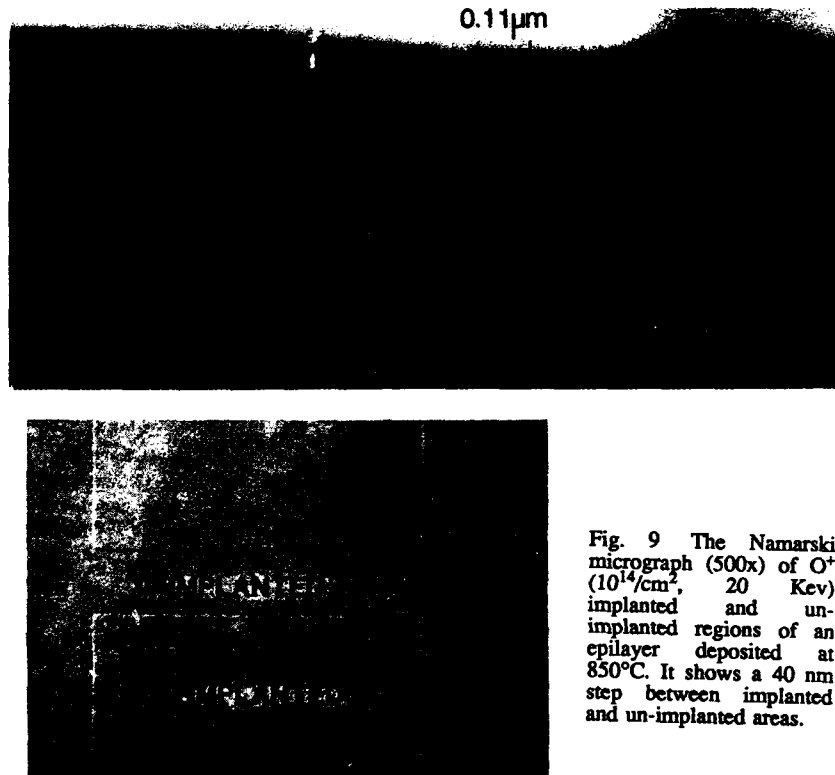


Fig. 9 The Namarski micrograph (500x) of O^+ ($10^{14}/cm^2$, 20 Kev) implanted and un-implanted regions of an epilayer deposited at $850^\circ C$. It shows a 40 nm step between implanted and un-implanted areas.

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PHOTOREFLECTANCE AND RESONANT RAMAN SCATTERING IN
SHORT PERIOD SI/GE SUPERLATTICES ON GE(001) AND SI(001)

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ABSTRACT

Short period Si/Ge superlattices have been grown on Ge(001) and Si(001) substrates by molecular beam epitaxy. The optical properties of the superlattices have been studied with photoreflectance (PR) and resonant Raman scattering (RRS). With PR we are able to observe new, structural induced transitions for all superlattices which are related to E_0 - and E_1 -like gaps. The analysis of PR spectra is complicated by an optical etalon effect if the samples are sufficiently thick. The E_1 -like transitions in the range between 1.9eV and 2.7eV are also studied with RRS. Due to the confinement of the optical phonons in the Ge and Si layers RRS is able to probe the bandstructure in each layer separately. Localized electronic states in the Ge layers can be observed with RRS for a $\text{Si}_4\text{Ge}_{18}$ superlattice and are compared with PR measurements.

INTRODUCTION

Short period Si/Ge superlattices are of considerable interest both due to their fundamental physical properties and their potential future device applications [1]. The work in this field was stimulated by an early theoretical study which predicted the possibility of creating 'zone folded' superlattice states allowing direct optical transitions across the superlattice bandgap [2]. Due to the development of low temperature Si MBE short period superlattices with sharp interfaces could be realized on Si [3] and Ge substrate [4] or on Si/Ge alloy buffer layers [5]. First electroreflectance measurements on Si/Ge superlattices grown on Si(001) [6] stimulated a large number of theoretical investigations [7-11]. These theoretical studies favour a Si/Ge superlattice with a period length of about 10 monolayers and a lateral lattice constant between the lattice constant of a corresponding alloy and bulk Ge. Until now, however, there are no experimental results which unambiguously prove the existence of a quasidirect fundamental gap. Taken into account that the calculated interband transition probability for a quasidirect transition is still some orders of magnitude less than the transition probability of a direct transition in bulk materials, they are difficult to measure. Direct transitions which are related to E_0 -, E_1 - and E_2 -like energy gaps could be observed with electro- and photoreflectance [12-16], ellipsometry [11], and resonant Raman scattering [15,17].

EXPERIMENTAL

The superlattices were grown on Ge(001) or Si(001). Details of the growth procedure are published elsewhere [18]. All samples grown on Ge are lattice matched to the substrate. For the investigated sample on Si substrate a partly relaxed Ge buffer layer was included between the superlattice and the substrate to achieve strain symmetrizing.

Photoreflectance (PR) is a powerful technique to investigate direct transitions in bulk semiconductors [19] and semiconductor superlattices [20]. We used a standard PR setup. The light of a quartz halogen lamp is dispersed through a monochromator with 320mm focal length. The reflected light was analyzed with a InAs- or Si-photodiode. An argon ion laser ($\lambda_{\text{laser}}=457\text{nm}$) or a HeNe laser ($\lambda_{\text{laser}}=633\text{nm}$) was used to modulate the surface reflectance. Diffuse scattered laser stray light was suppressed by filters or a second monochromator. The intensity of the reflected light was kept constant by regulating the halogen lamp power supply. In this way a normalization of the spectra is easy to perform.

Resonant Raman scattering (RRS) is a further technique to study the electronic bandstructure of bulk semiconductors [21] or semiconductor superlattices [22]. RRS measurements were performed using several discrete lines of krypton and argon lasers, and a R6G dye laser. Our Raman setup included a DILOR triple spectrometer and a multichannel detection system.

PR and RRS measurements were performed either in a He continuous flow cryostat at $T=5\text{K}$ or in a liquid nitrogen cold finger cryostat at $T=80\text{K}$. Low temperatures were essential to take the PR spectra.

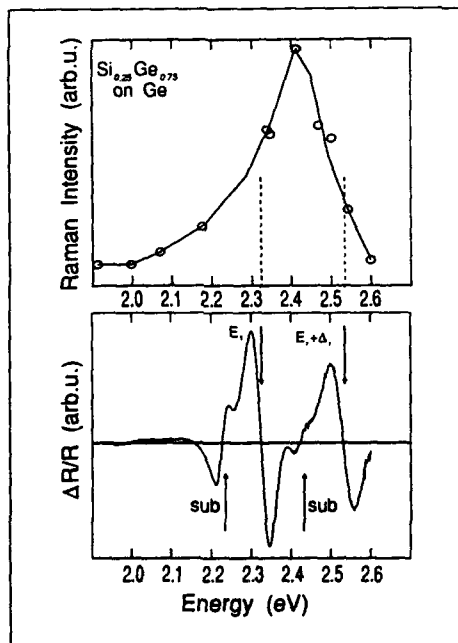


Fig.1 Photoreflectance and Resonant Raman spectrum of a $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy on Ge(001).

In Fig.1 PR and RRS spectra for a $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy grown on Ge(001) are compared. The PR spectrum shows narrow signals which are related to E_1 and $E_1+\Delta_1$ transitions of the strained alloy and the underlying substrate. The alloy optical phonons show a resonance peak between the E_1 and $E_1+\Delta_1$ transitions. This behaviour is typically for the Raman scattering mechanism in Si/Ge alloys [23].

RESULTS AND DISCUSSION

In Fig.2 PR spectra for bulk Ge, a $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy and a Si_3Ge_9 superlattice both grown on Ge(001) are compared. For bulk Ge four transitions can be observed. The structures at about 0.89eV and 1.19eV originate from E_0 and $E_0+\Delta_0$ transitions at the Brillouin zone center. At about 2.22eV and 2.42eV E_1 and $E_1+\Delta_1$ transitions between the conduction band and the spin

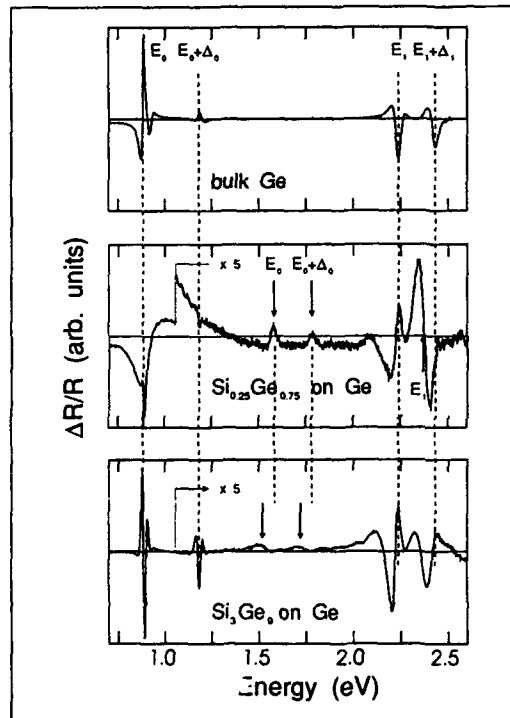


Fig.2. Photoreflectance spectra for bulk Ge, a $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy and a Si_3Ge_9 superlattice on Ge(001).

orbit split valence band in Γ -L direction can be observed. These transitions are still visible in PR spectra of the alloy and the superlattice due to the underlying Ge substrate. At 1.58eV, 1.78eV and 2.38eV additional signals are observed for the strained $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy which can be assigned to E_0 , $E_0+\Delta_0$ and E_1 transitions, respectively. The energy of these gaps for unstrained alloys can be linearly interpolated between those of Si and Ge [24]. Fixing the lateral lattice constant of the alloy to the lattice constant of the underlying Ge substrate causes a strain induced downward shift of the transition energy. For the Si_3Ge_9 superlattice E_0 and $E_0+\Delta_0$ -like transitions are observed which are shifted to lower energies compared to the corresponding $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy. This energetic shift is expected with the development of the superlattice bandstructure and fits well to the results of a simple Kronig-Penney typed bandstructure calculation. In the energy range between 1.9eV and 2.6 eV new structures build up which can be assigned to E_1 -like transitions in the superlattice. The analysis of these structures is complicated by the superposition of signals arising from the superlattice and the substrate. The zone-folded quasi-direct transitions which are expected in the energy range between 0.7eV and 1.0eV are not observed. This can be understood in terms of the

orbit split valence band in Γ -L direction can be observed. These transitions are still visible in PR spectra of the alloy and the superlattice due to the underlying Ge substrate. At 1.58eV, 1.78eV and 2.38eV additional signals are observed for the strained $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy which can be assigned to E_0 , $E_0+\Delta_0$ and E_1 transitions, respectively. The energy of these gaps for unstrained alloys can be linearly interpolated between those of Si and Ge [24]. Fixing the lateral lattice constant of the alloy to the lattice constant of the underlying Ge substrate causes a strain induced downward shift of the transition energy.

For the Si_3Ge_9 superlattice E_0 and $E_0+\Delta_0$ -like transitions are observed which are shifted to lower energies compared to the corresponding $\text{Si}_{0.25}\text{Ge}_{0.75}$ alloy. This energetic shift is expected with the development of the superlattice bandstructure

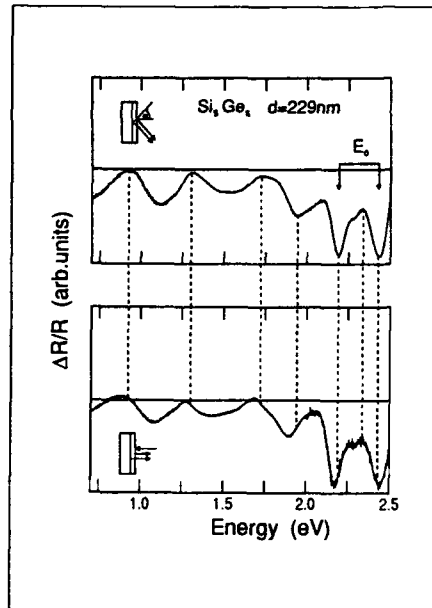


Fig.3 Photoreflectance spectra for a strain symmetrized Si_5Ge_5 superlattice on Si(001) taken under different scattering geometries.

low transition probability for zone folded transitions and the small superlattice thickness of about 33nm.

For a Si_5Ge_5 superlattice theoretical studies predicted strong oscillator strength for the zone folded transitions [10,11]. For this superlattice the Δ minima of the Si-like bandstructure in growth direction are directly folded back to the Brillouin zone center fulfilling one criterion for the achievement of a quasi-direct gap semiconductor. In Fig.3 PR spectra for a Si_5Ge_5 superlattice taken under different scattering geometries are compared. Below 2.0eV broad and strong signals can be observed which are shifting to higher energies with increasing angle of incidence (α). These structures can therefore be assigned to interference oscillations originating in an optical etalon built up by the superlattice. Similar observations are reported in Ref. [14]. The signals at about 2.2eV and 2.4eV do not shift in energy with different scattering geometries. They can be

attributed to E_0 -like transitions. This assignment is confirmed by the results of a simple Kronig-Penney typed bandstructure calculation. Interference oscillations, as described above, are always observed if the superlattices are sufficiently thick. The appearance of these interference oscillations prevents the observation of weak signals expected for zone-folded transitions in the spectral region below 1.5 eV.

To learn more about the origin of the E_1 -like transitions between 1.9eV and 2.7eV we performed Resonant Raman measurements. The optical phonons in Si/Ge superlattices are strongly confined to the Si and Ge layers, respectively [25]. RRS of these confined optical phonons is able to probe the electronic bandstructure in each layer separately.

In Fig.4 a PR and RRS spectrum for a $\text{Si}_4\text{Ge}_{18}$ superlattice grown on Ge(001) are compared. The PR spectrum is fitted to a theoretical line shape function [18,19]. The transition energies obtained in this way are marked by arrows. In RRS we observe for the Ge phonon a strong resonance at about 2.4eV and a shoulder at about 2.1eV. The Si phonon shows only one resonance for the higher energy. Thus we conclude that the lower resonance corresponds to transitions, observed with PR at

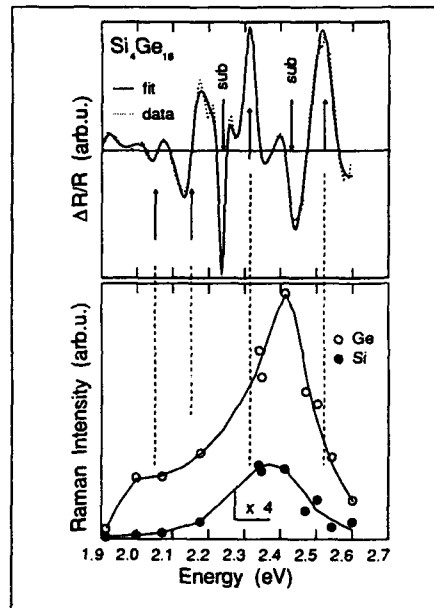


Fig.4 Photoreflectance and RRS spectrum of a $\text{Si}_4\text{Ge}_{18}$ superlattice on Ge(001). The arrows mark the transitions energies obtained by the fit.

2.05eV and 2.15eV which are connected to electronic states confined strongly to the Ge layers. The observation of a resonance enhancement at 2.4eV for both phonons is evidence for transitions between more extended states. These transitions are seen with PR at 2.32eV and 2.52eV.

CONCLUSIONS

Transitions, confirming the development of a superlattice bandstructure, could be observed with PR and RRS. These transitions are evolving from the E_0 - and E_1 -transitions of the corresponding alloy with increasing superlattice periodicity. The assignment of PR signals to E_0 -like transitions is also confirmed by the results of simple Kronig-Penney typed bandstructure calculations. For a strain symetrized Si_5Ge_3 superlattice with an entire thickness of 229nm the PR spectrum below 2.0 eV is dominated by interference oscillations. These oscillations are

originating in an optical etalon built up by the superlattice. With PR and RRS a splitting of E_1 -like transitions can be observed for a $\text{Si}_4\text{Ge}_{18}$ superlattice. Due to the confinement of the optical phonons in the individual layers RRS is able to assign the PR signals to transitions between extended and localized electronic states.

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ELECTRICAL AND OPTICAL PROPERTIES OF ERBIUM IN MBE SILICON AND SI/Ge ALLOYS.

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ABSTRACT

This paper reports the incorporation of erbium into MBE Si and Si/Ge alloys with substrate temperatures of 500°C and 700°C. Using a solid source MBE system, concentrations of erbium between 10^{18} and 10^{22} cm⁻³ have been studied by photoluminescence, electrical measurements, SIMS and TEM. We find no shallow donors or acceptors attributable to erbium but we observe a high concentration of deep states with an activation energy of ~360 meV. The photoluminescence output is of greatest magnitude when $[Er] = 2 \times 10^{18}$ cm⁻³. Above this concentration the onset of erbium precipitates can just be observed using TEM and at even higher concentrations structured growths of erbium silicide are apparent. The effect on the optical activity of Si:Er that has subsequently been implanted with oxygen is also reported.

INTRODUCTION

Rare earth (RE) doped semiconductors have recently attracted interest because of their potential use in LEDs¹ for telecommunications. The wavelength of the intra-4f-shell radiative transition is relatively unaffected by external parameters such as temperature and host material²⁻⁵ and consequently the emission should remain sharp even at room temperature. Erbium exhibits an atomic like spectral line at 1.54 μm in a semiconductor host. This wavelength coincides with the minimum loss wavelength region of silica optical fibres.

Most studies of Si:Er have concentrated on implanted material; little has been reported for REs that have been grown into Si by MBE. Ennen et al² compared MBE-grown Si:Er and Er implanted into Si; the PL spectra was sharper for MBE layers than the implanted structures. Due to the large mass of the Er, very large energies are required during implantation to produce a doped region thick enough to study systematically by electrical and optical techniques. In addition, MBE gives the opportunity to produce Si/Ge structures. The use of Si/Ge and quantum wells offers the possibility of band-gap engineering, and tailoring the exciton or electron-hole pair energy to investigate the excitation process.

We have characterised the behaviour of Er in Si, Si/Ge and Si/Ge-Si quantum wells by PL, electrical measurements, TEM, SIMS and RBS. We have also studied oxygen implanted MBE Si:Er (implanted at Surrey University, UK), to compare with the results of Favennec et al⁶. We report on preliminary findings in this study.

MBE GROWTH

The Er-doped Si and Si_{1-x}Ge_x epitaxial layers were grown in a conventional (VG Semicon V80) MBE apparatus utilizing e-beam evaporation for Si and Ge, and a standard Knudsen cell for co-evaporation of elemental Er. The combined Si and Ge growth rate was 5 Å s⁻¹ and the growth temperature was maintained constant at 500°C for Si_{1-x}Ge_x alloys and at 500 or 700°C for Si epitaxy. Compositional depth profiling was performed by SIMS in a

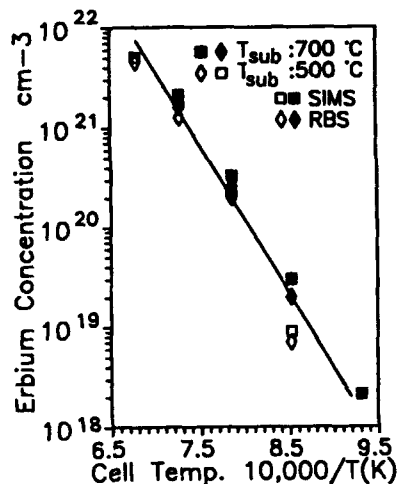


Figure 1. The dependence of erbium concentration in the grown layer on cell temperature, for two substrate temperatures, 500°C and 700°C.



Figure 2. A doping staircase in silicon alternating erbium doped and undoped regions. The labels indicate the erbium cell temperature for each layer.

Cameca IMF 4F using either Cs^+ or O^+ and extracting positive secondary ions. An implanted Si:Er layer was used as a calibration standard. The Er doping level was varied from 10^{18} cm^{-3} to 10^{22} cm^{-3} by increasing the Er Knudsen cell temperature from 800°C to 1200°C. Over the range studied, the substrate temperature made no difference to the rate of incorporation of erbium. Figure 1 shows the dependence on cell temperature.

TEM RESULTS

Cross sectional TEM was carried out on ion-thinned specimens using a Philips EM430. The XTEM micrograph in Figure 2 illustrates an erbium doping staircase in a silicon sample showing the morphological change as the solid solubility limit is exceeded while maintaining other growth parameters constant ($T_0=700^{\circ}\text{C}$). For $[\text{Er}]=2 \times 10^{18}$ ($T_{\text{Er}}=800^{\circ}\text{C}$) a few isolated precipitates can just be observed, indicating that the solid solubility limit for Er in Si is approximately 10^{18} cm^{-3} for substrate temperatures of 500-700°C. At an Er concentration of 10^{19} cm^{-3} ($T_{\text{Er}}=900^{\circ}\text{C}$), ErSi_2 precipitates are clearly visible and at the highest erbium concentration ($5 \times 10^{21} \text{ cm}^{-3}$) the silicide platelet structure was so pronounced that it prevented the subsequent growth of single crystal silicon.

OXYGEN IMPLANTATION

After we characterised the as-grown samples, oxygen was implanted into the layers. A uniform oxygen distribution was achieved by using a sequence of implantation energies. We produced 10^{18} cm^{-3} oxygen distribution to a depth of $0.6 \mu\text{m}$ by this method. The ion ranges and longitudinal straggles were calculated using the TRIM simulation program. Four different ion energies were used to obtain the uniform oxygen profile after implantation. These were

260, 160, 90 and 45 keV. The respective doses were 2.6×10^{13} , 1.6×10^{13} , 1.2×10^{13} and $0.78 \times 10^{13} \text{ cm}^{-2}$. After oxygen implantation the samples were annealed for various times, in order to establish the optimum anneal time to produce the maximum PL output.

ELECTRICAL PROPERTIES

Layers of undoped Si (no Er) grown in this study had a background hole concentration $8 \times 10^{14} \text{ cm}^{-3}$. This material thus provided a sensitive test of the electrical activity of Er in Si.

The Er produced some additional electrical activity but the material remained p-type (hence the Er related states are acceptors) and the additional carriers froze out on cooling. Because of the low level of background doping, the MBE layers were not thick enough to undertake reliable capacitance DLTS, but conductivity studies gave an activation energy of 360meV and a concentration of around 10^{16} cm^{-3} in a layer with an erbium concentration of $5 \times 10^{18} \text{ cm}^{-3}$.

This contrasts with the ion-implantation work of Widdershoven and Naus⁷, who reported the formation of a 270 meV donor at a concentration $1/2$ orders below the implant concentration.

PHOTOLUMINESCENCE MEASUREMENTS

PL was carried out with the 514nm line of an Ar⁺ laser as the excitation source. Detection was by conventional lock-in techniques and a cooled North Coast Ge detector.

Figure 3 shows the photoluminescence spectra obtained from Si:Er, and Er in a Si/Ge alloy, measured at 4K. The spectra consists of one sharp line at $1.54 \mu\text{m}$ (0.805eV) plus some low energy features, which we attribute to crystal-field splitting². This illustrates that the Er atomic levels are slightly influenced by the host material into which they are grown. The fine structure of each spectrum is different, but the central wavelength is essentially host independent.

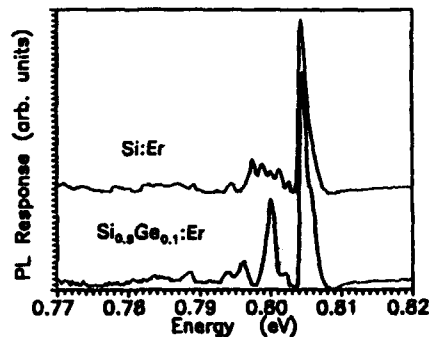


Figure 3. Photoluminescence from erbium doped MBE Si and MBE $\text{Si}_{0.9}\text{Ge}_{0.1}$ both grown with a substrate temperature of 500°C . The measurement temperature was 4K.

The maximum PL output was obtained from the Si:Er layer with $[\text{Er}] = 2 \times 10^{18} \text{ cm}^{-3}$. The PL signal intensity from a Si:Er layer with $[\text{Er}] = 1 \times 10^{20} \text{ cm}^{-3}$ was an order of magnitude smaller than this. This can be explained on a qualitative basis by the TEM results and the onset of ErSi_2 precipitates.

We found that oxygen implantation did not affect the overall line-shape to any great degree when we measured the PL at 4K and higher temperatures. However, some of the low energy structure altered after implantation. The PL intensity from the $1 \times 10^{20} \text{ cm}^{-3}$ Er-doped Si was not changed by oxygen implantation and annealing, as measured at 18K.

Figure 4 shows the dependence of the PL intensity at $1.54 \mu\text{m}$ for various anneal times as a function of measurement temperature. The luminescence intensities are normalised at 77K. Although the oxygen implant and optimum anneal did not significantly affect the magnitude of the luminescence at 4K, at temperatures of 77K and above the implanted layers

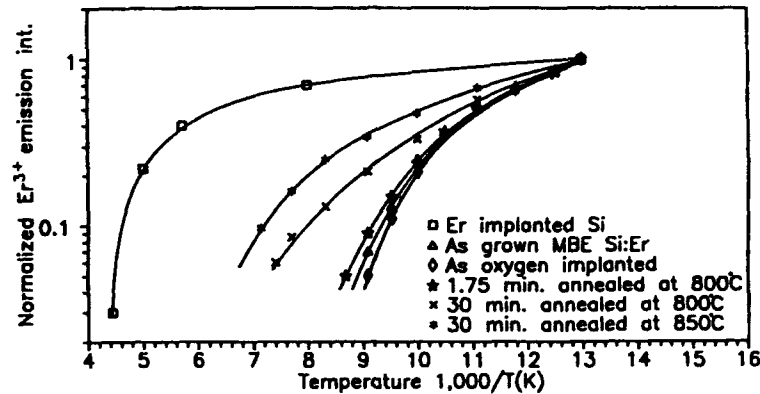


Figure 4. The dependence of the integrated photoluminescence intensity at $1.54 \mu\text{m}$ on measurement temperature, for an erbium implanted layer⁵, as grown MBE, and oxygen implanted MBE for different anneal times.

exhibit more efficient luminescence than the as-grown layers. This is similar behaviour to that reported for Er-implanted layers, enhanced with an oxygen implant⁹ although the effect is not as pronounced.

DISCUSSION

All PL lines attributable to Er are sublinear with excitation power, and saturate at laser powers of approximately 50mW, (measured outside the cryostat window). This is to be expected when observing PL from low concentrations of radiative states that have very long decay times. Klein et al⁸ have measured Er luminescence decay in various semiconductor matrices, and find that in MBE Si:Er the radiative lifetime is about 0.8ms.

In our material, there is very little or no PL from other spectral regions, and none from the silicon substrate below the erbium doped region. This has also been observed in implanted Er layers⁹. Therefore, it appears that the photo-created carriers do not diffuse through the Er doped layer into the substrate. In all our layers this is $< 3.5 \mu\text{m}$ below the surface, so we should expect to see substrate luminescence, unless there were other powerful recombination mechanisms. We did, however, observe substrate luminescence from a layer which contained $50 \times 100 \text{ \AA}$ $\text{Si}_{0.75}/\text{Ge}_{0.25}$ quantum wells, where the wells were doped with $5 \times 10^{18} \text{ cm}^{-3}$ Er. This could be due to the reduction in the total number of Er atoms present in this layer compared to the $5 \times 10^{18} \text{ cm}^{-3}$ $\text{Si}_{0.9}/\text{Ge}_{0.1}/\text{Si:Er}$ layer, which was $1.5 \mu\text{m}$ thick.

In general, there is a low luminescence intensity observed at $1.54 \mu\text{m}$, but in Si:Er there are very few carriers which do not recombine in the Er-doped regions. There are two possible explanations for this. Either there is a low probability of efficient energy transfer from the bound electron-hole pair to the radiative $4f$ RE states, (the energy being lost in some internal non-radiative process) or else the carrier recombination is via an external non-radiative path. We found that a very short anneal of 105 seconds under nitrogen led to the most efficient optical activity. Longer anneal times degraded the PL signal, presumably because the anneal itself was introducing competing mid-gap states into the material.

We also observe some evidence of other impurity-bound excitonic and implant-damage related PL emission from the oxygen-implanted layers, though these are weak compared to the Er-related emission.

CONCLUSIONS

A major problem in the growth of Si:Er by MBE is the onset of precipitation at erbium concentrations in the low 10^{18} cm⁻³ range. It is unlikely that such precipitates will be active in the luminescence process and so the precipitate behaviour places an upper limit on the number of active centres of around 10^{18} cm⁻³. There is no shallow donor or acceptor behaviour due to the incorporation of erbium in MBE growth. A deep acceptor with an activation energy of 360 meV is observed; we do not at this stage attribute this directly to the erbium doping as its concentration is more than two orders below that of the dopant.

The luminescence spectra indicates that the Er³⁺ ion sees different environments in Si and Si/Ge, and the detailed siting is modified by oxygen implantation and anneal. In Si_{0.9}Ge_{0.1} the spectra are subtly different implying that the presence of germanium has played a definitive role in establishing the local environment of the erbium.

The magnitude of the luminescence peaks shows that the radiative recombination via the erbium is much more probable than any other excitonic route even at low temperatures. However, the overall efficiency in our erbium doped material is low and appears to be due to a powerful competing non-radiative path. This is almost certainly associated with the 360 meV acceptor. It remains to be seen whether this is intrinsic to the erbium incorporation or due to inadvertent impurities.

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WAVE FUNCTION ENGINEERING OF LINEAR AND NON-LINEAR OPTICAL RESPONSE IN Si-Ge QUANTUM WELL STRUCTURES AND SUPERLATTICES

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ABSTRACT

We show that the infinite Si-Ge superlattices predicted to exhibit strong optical transitions across the fundamental gap and between conduction subbands also give rise to significant optical nonlinearities. Efficient optical transitions can also be achieved in finite-length structures grown on Si or Ge substrates. However, the zone folding argument does not apply and the electronic structure strongly reflects the finite length of such systems.

LINEAR AND NONLINEAR RESPONSE IN INFINITE SUPERLATTICES

The interest [1] in Si-Ge superlattices has been fuelled by the possibility of breaking the bulk conduction bands of Si into minibands whose absolute minimum falls upon the center of the Brillouin zone. This is a simple physical

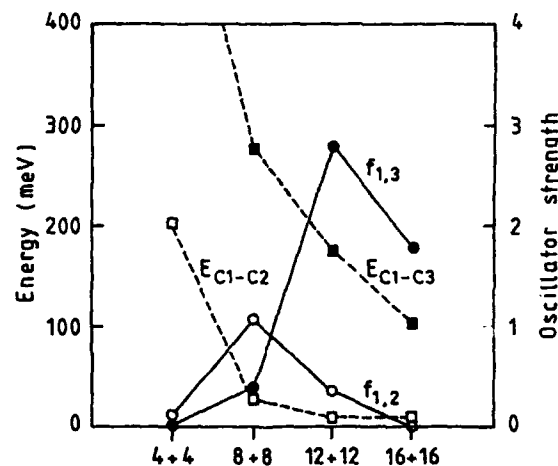


Figure 1

concept which can be translated into numerical predictions in terms of the Kronig-Penney type calculations of energy levels. The ease with which such modelling can be done has appealed to experimentalists, particularly when large scale calculations confirmed that, in the absence of any detailed spectroscopic evidence, the energies predicted from simple models provided as good a guide as any other model. As a result the "zone folding" argument has dominated the discussion of Si-Ge structures, so much so that it has been used to interpret properties of structures in which the periodic boundary conditions characteristic of an infinite system assumed in the zone-folding argument were not applicable. We shall address this problem in the second section of this paper and focus on infinite systems here.

Detailed calculations show that within the accuracy accessible to present day techniques the key prediction of the zone folding model concerning the position of the conduction band minimum in Si-Ge superlattice is correct. This means that the structure of interest is a ten monolayer period. Several strain distributions are permitted in spite of the constraints imposed upon the choice of substrate by the requirement that the zone folded minimum in the direction of the growth axis must lie lower in energy than the conduction band minima lying in the interface plane [2]. The band gap of the superlattices with a ten monolayer period ranges from about 1 eV for Si_7Ge_3 to 0.6 eV in Si_6Ge_4 . In larger period structures, e.g. with 20 or 30 monolayer periods which may

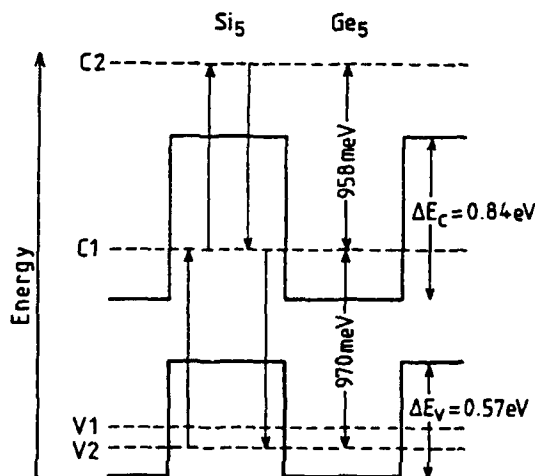


Figure 2

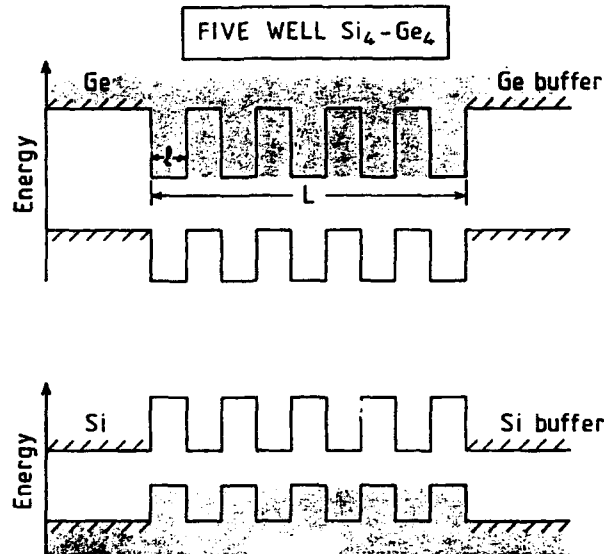


Figure 3

also satisfy the zone folding condition, the strength of the optical transition across the gap is significantly reduced and renders such systems uninteresting for applications. In shorter period systems the conduction band minimum lies away from the zone center and this reduces the transition probability at the band edge where the relevant recombination must occur. This limits the range of wavelengths amenable for applications. However, our quantitative studies of the conduction minibands in 10 monolayer superlattices show that the optical transition between the lowest minibands is strong and depends weakly on the distribution of strain in the system. Furthermore, unlike the transitions across the gap, the strength of this effect decreases only slowly with the increase of the period. This is shown in Fig. 1 where we plot the results of our calculations of the energy and oscillator strengths of the transitions between conduction minibands 1 and 2. In a ten monolayer structure, minibands 1 and 2 become near degenerate in energy and the transition of interest is between minibands 1 and 3. We can see that these transitions extend the range of applicable wavelengths well into the far infrared.

The ten monolayer structure also exhibits a strong virtual optical nonlinearity. This is indicated in Fig. 2. The lines with arrows connecting the conduction (C1, C2) and valence (V1, V2) states of the ten monolayer symmetrically

strained Si-Ge superlattice indicate the four photon virtual process [3] which makes the third order susceptibility of order 10^{-6} e.s.u. This is thanks to the strong optical transition probabilities associated with the transitions in question and the near equality of the energy separations C1-C2 and C1-V2 which appear in the denominator in the expression for nonlinear susceptibility. The response is excited at photon energies just below the band gap energy, with any negligible absorption. Another interesting nonlinear mechanism is associated with the band nonparabolicity [4] in Si-Ge superlattices. We find that the magnitude of the conduction band nonparabolicity along the growth axis can be varied by two orders of magnitude by changes of superlattice period of order 2-3 bulk lattice constants and that it exceeds that in III-V materials. The nonparabolicity is also increased significantly in the interface plane.

ELECTRONIC STRUCTURE AND OPTICAL PROPERTIES OF FINITE LENGTH SI-Ge SUPERLATTICES

When thin layers of Si and Ge are grown directly on Si or Ge substrates no more than five or six periods can be grown. The confining potential then looks like that sketched in Fig 3. As the shaded area indicates, in addition to the short wavelength reflections given by the superlattice period l , there are also reflections associated with the finite length of the system L . The latter mechanism has been ignored in existing theoretical studies of such a system. Accordingly, we have applied our pseudopotential method to a Si_4Ge_6 five period structure grown on Ge. Such a structure has recently been studied experimentally by Pearsall *et al* [5]. The electron charge density associated with the lowest conduction state is shown in Fig 4. Clearly,

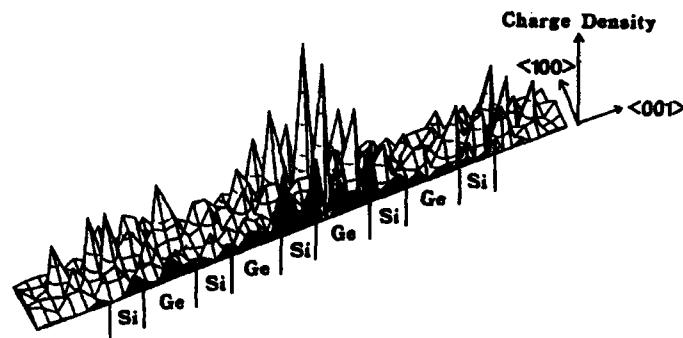


Figure 4

the confining effect across the full length of the structure cannot be ignored; in fact it dominates the shape of the wave function. We also find localised wave packets at the interfaces which are quite unlike anything we have seen in direct gap III-V superlattices. Although these states do not introduce levels in the gap, they might play a part in carrier dynamics.

The energy levels obtained in our calculation for this system are shown in Fig 5. When compared with experimental values, the discrepancy concerning the principal transition at 0.88eV reported in the experiment appears to be about 80meV, i.e. not very significant given the uncertainties in experimental as well as theoretical results. However, the oscillator strengths reported by Pearsall *et al* are by about a factor of two larger than our prediction. Since in our calculation we have ignored any deviations from perfect symmetry, the theoretical results for zone folded states should be regarded as an upper limit. This casts some doubt on the interpretation of the observed spectra in terms of an idealised picture of the electronic structure normally adopted in the literature and suggests that a more realistic model including deviations from perfect composition, nonideal strain distribution, and defects might be more appropriate.

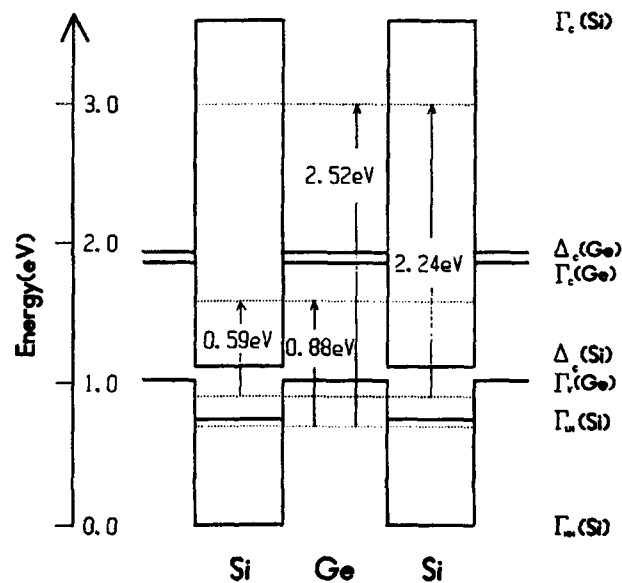


Figure 5

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**INTERSUBBAND ABSORPTION IN THE CONDUCTION BAND OF
SI/SI_{1-x}GE_x MULTIPLE QUANTUM WELLS**

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EXTENDED ABSTRACT

The intersubband absorption of electrons in modulation doped Si/Si_{1-x}Ge_x multiple quantum wells has been observed [1]. Various samples with different well widths and carrier densities have been studied. Narrow absorption lines are observed in waveguide geometry. Self consistent subband calculations are in good agreement with the experimental values.

In strain symmetrized Si/Si_{1-x}Ge_x multilayer structures the conduction band minimum is lowest in the Si layers [2]. This is due to the biaxial tensile stress in the Si layers, which causes a lowering and splitting of the six-fold degenerated conduction band [3]. The two-fold degenerated states are localized in the Si wells, while the SiGe layers act as barriers in the MQW structure. This leads to a localization of electrons in the Si layers. The inset in Fig.1 shows the self-consistently calculated potential and three subbands of a 50Å quantum well. Due to the large effective electron mass of Si, in comparison with GaAs, the energy separation between the subbands is lower and therefore the intersubband absorption is expected in the far infrared. Fig 1 shows the calculated subband energies and the Fermi energy versus the well width. For well widths of less than 75Å and a two-dimensional carrier concentration of 2.0·10¹² cm⁻² only the ground state is occupied, while broader wells lead to an occupation of two subbands. In the latter case in addition to the intersubband absorption from the ground to the first excited state (0→1) a transition from the first to the second subband (1→2) is expected.

The samples are grown in a Si-MBE [4] on (100) p⁻-Si wafers. They consist of a 3000Å Si_{0.7}Ge_{0.3} buffer layer followed by 5 Si quantum wells, which are embedded in 250Å wide barriers. The center 50Å of these barriers are Sb doped using the secondary implantation technique [5]. The carrier concentrations per well were determined by Hall- and Shubnikov-de Haas measurements [6]. Low temperature mobilities up to 17000 cm²/Vs were observed. The backsides of the samples are polished and a 38° multipass waveguide geometry was prepared. The transmission spectra are recorded with a Fourier transform spectrometer at 8K using a continuous flow cryostat. A far infrared polarizer is placed in front of the cryostat. The transmission spectra represent measurements at perpendicular polarization divided by spectra recorded at parallel polarization.

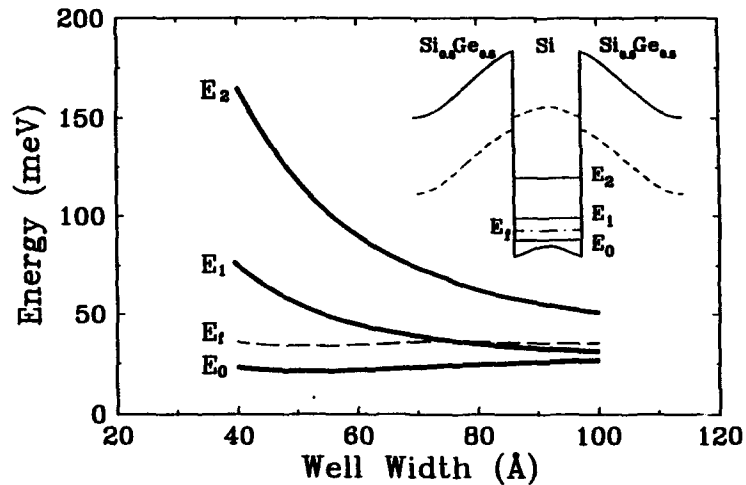


Figure 1: Calculated dependence of the subband energies versus the well width using a constant carrier concentration of $2.0 \cdot 10^{12} \text{ cm}^{-2}$. The dashed line shows the Fermi energy. The inset shows the conduction band structure of the Si/Si_{0.5}Ge_{0.5} modulation doped quantum well with the potential of the two-fold (solid) and four-fold (dashed) degenerated states. The ground state and two excited bound states are shown in solid lines, the Fermi energy in a dashed dotted line.

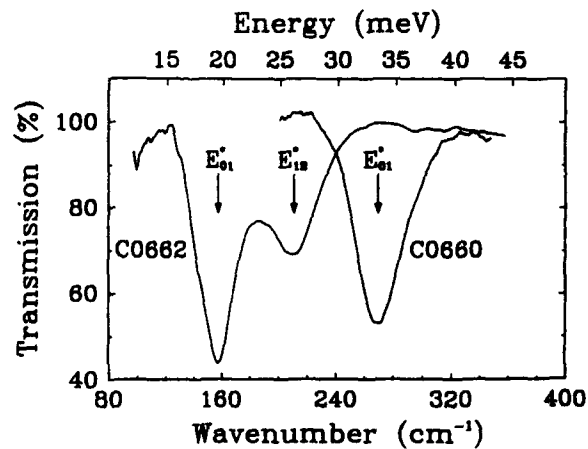


Figure 2: Measured transmission spectra as a function of wavenumber at 8K of the samples C0660 and C0662. The arrows indicate the observed transitions with their assignment.

Fig.2 shows the transmission spectra of the samples C0660 and C0662. C0660 has 50Å wide wells with an electron density of $2.1 \cdot 10^{12} \text{ cm}^{-2}$ per well. The absorption is peaked at 270 cm^{-1} with a full width at half maximum (FWHM) of 36 cm^{-1} . The sample C0662 has a well width of 75Å and a carrier concentration of $1.9 \cdot 10^{12} \text{ cm}^{-2}$. This sample exhibits two definite transmission minima. The stronger one is at $E_{01}^* = 157 \text{ cm}^{-1}$ (FWHM = 28 cm^{-1}), the weaker is at $E_{12}^* = 210 \text{ cm}^{-1}$ with a FWHM of 36 cm^{-1} . The differences between these two samples can be explained using Fig.1. For a well width of 50Å the Fermi energy is between the ground (E_0) and the first excited state (E_1). Therefore the sample C0660 shows a single absorption line corresponding to the $0 \rightarrow 1$ transition. In contrast to this for well widths of 75Å (C0662) or more the Fermi energy moves into the first subband. This means that in addition to the ground state E_1 is occupied and the $1 \rightarrow 2$ transition is also possible. Due to the increasing subband splitting of the lower energy levels in the more or less rectangular quantum well the transition energy E_{12}^* is larger than E_{01}^* .

In conclusion, we have measured intersubband transitions in the conduction band of modulation doped Si/Si_{1-x}Ge_x multiple quantum wells. Very narrow absorption lines are observed. In good agreement with our self-consistent calculations one sample shows in addition to the $0 \rightarrow 1$ transition the excitation of electrons from the first to the second subband.

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PART V

GeSi Electronic Transport

THE EXTRACTION OF MINORITY CARRIER LIFETIME FROM THE CURRENT-VOLTAGE CHARACTERISTICS OF Si/Si_{1-x}Ge_x DEVICES

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ABSTRACT

The extraction of recombination lifetime from the current-voltage characteristics of diode structures containing Si_{1-x}Ge_x strained layers is discussed. Electrical measurements are used in conjunction with computer simulations to extract minority carrier lifetime in Si_{1-x}Ge_x layers with various oxygen concentrations. The minority carrier lifetime in Si_{1-x}Ge_x increases from several psec at an oxygen concentration of 2X10²⁰ cm⁻³, to greater than 0.5 μs at concentrations below 3X10¹⁷ cm⁻³. The structures are analyzed for sensitivity of the current characteristics to Si_{1-x}Ge_x minority carrier lifetime. Calculations predict that the maximum lifetime which can be extracted from such structures is greater than 100 μsec. However, due to limitations imposed by perimeter currents, the maximum lifetime which can be extracted from our diode structures is on the order of 3 μsec. Maximizing area to perimeter ratio of the diode structures and moving the Si_{1-x}Ge_x-SiO₂ interface away from the active device region is required in order to increase the maximum extracted lifetime from such structures.

INTRODUCTION

Recombination lifetime is an important parameter in minority carrier devices such as heterojunction bipolar transistors (HBTs). In this paper we consider the extraction of recombination lifetime in strained Si_{1-x}Ge_x films using various diode structures. The diodes have been fabricated by the chemical vapor deposition technique, limited reaction processing (LRP) [1,2]. A combination of electrical measurements and computer simulations of the forward current-voltage characteristics is used to extract the lifetime. The diode structures are used specifically to evaluate the effect of oxygen incorporation on the recombination lifetime in Si_{1-x}Ge_x. We have previously reported an appreciable difference in the oxygen incorporation in Si_{1-x}Ge_x films, compared to the Si films, grown at a given temperature by LRP [3,4]. A comparison of Si/Si_{1-x}Ge_x/Si HBTs grown by LRP, with similarly fabricated Si homojunction transistors, shows evidence of high recombination in the Si_{1-x}Ge_x base relative to the Si base [1]. The large difference in oxygen concentration between the Si_{1-x}Ge_x and Si material suggests that oxygen may be playing a key role in reducing carrier lifetimes in the Si_{1-x}Ge_x base [5,6,7]. In this work the oxygen concentration in the Si_{1-x}Ge_x films is varied from above 1X10²⁰ cm⁻³ to below 1X10¹⁷ cm⁻³.

EXPERIMENT

The Si and Si_{1-x}Ge_x layers for all devices were grown in a lamp-heated reactor using limited reaction processing as explained in references 2, 4 and 5. The addition of a load-lock chamber to the apparatus has enabled the growth of Si_{1-x}Ge_x at 625°C with low oxygen concentrations [3]. Four types of diode layer structures were grown for this experiment: (1) p⁺SiGe-iSiGe-n_{Si} diodes, (2) corresponding p⁺SiGe-n_{Si} diodes with the

same total $\text{Si}_{1-x}\text{Ge}_x$ thickness and oxygen concentration, (3) $\text{p}^+\text{SiGe-nSiGe-nSi}$ diodes and (4) $\text{p}^+\text{Si-nSiGe-nSi}$ diodes. The Ge fractions were 0.21 ± 0.011 and 0.14 ± 0.012 . The fabrication process for these devices is described in Ref. 8. The background doping in the $\text{Si}_{1-x}\text{Ge}_x$ i-layer was n-type and determined to be $5 \times 10^{15} \text{ cm}^{-3}$ by C-V analysis. Oxygen and boron concentrations were measured by Secondary Ions Mass Spectrometry (SIMS). The electron concentrations in the $\text{Si}_{1-x}\text{Ge}_x$ were measured by C-V analysis. Rutherford backscattering spectrometry was used to determine $\text{Si}_{1-x}\text{Ge}_x$ thicknesses and composition.

Experimental results

Figure 1 shows measured current versus forward voltage characteristics for $\text{p}^+\text{SiGe-nSi}$ and $\text{p}^+\text{SiGe-iSiGe-nSi}$ heterojunction diodes [7]. Measurements of diodes with various area to perimeter ratios indicate that these currents scale with the diode area. The p-n diodes show comparable intercept current (curves (a) and (b)) and the ideal inverse slope of 59 mV/decade, irrespective of the oxygen concentration in the $\text{Si}_{1-x}\text{Ge}_x$. Large recombination currents are observed in the corresponding p-i-n diodes (curves (c) and (d)). No such space charge recombination is observed in p-i-n diodes fabricated in Si epitaxial layers or in $\text{Si}_{1-x}\text{Ge}_x$ layers with oxygen concentrations less than $3 \times 10^{17} \text{ cm}^{-3}$.

We can explain the p-i-n diode current characteristics by inspecting the concentration profiles shown in figure 2. The profiles have been calculated using the device simulation program, SEDAN [9]. $\text{Si}_{1-x}\text{Ge}_x$ band-gap parameters from Ref. 5 were used in the simulations. The total diode current can be expressed as the sum of the minority carrier diffusion current at the two depletion layer edges and the total recombination current within the space charge regions (SCR) of the device:

$$I_{\text{diode}} = I_{\text{diff}}(\text{p-SiGe}) + I_{\text{diff}}(\text{n-Si}) + I_{\text{rec}} \quad \text{.....Eq. 1}$$

$$I_{\text{rec}} = qA \int_{\text{SCR}} \frac{p(x)n(x) - n_i^2}{\tau [p(x) + n(x) + 2n_i \cosh(E_t - E_i)/kT]} dx \quad \text{.....Eq. 2}$$

The recombination component can be calculated by integrating the Shockley-Read-Hall recombination equation over the $\text{Si}_{1-x}\text{Ge}_x$ and Si space charge regions within the device. The appropriate values of n_i , mid-gap energy level E_t and lifetime τ ($\tau = \tau_n = \tau_p$) are used in the integral on each side of the heterojunction. Since the integrand is a weak function of the trap level for $E_t - E_i < 10kT$ [10], we assume that the trap level is at the mid-gap for simplicity.

These relationships can be used to explain the dramatic difference between the forward current characteristics of the p-i-n and p-n heterojunction diodes when the $\text{Si}_{1-x}\text{Ge}_x$ lifetime is low. The diffusion component is roughly comparable for both diodes but the recombination current is different. The integrand in equation 2 is approximately given by $n(x)/\tau$ within the space charge region on the $\text{Si}_{1-x}\text{Ge}_x$ side of the heterojunction, since the hole concentration is greater than both n and n_i throughout i- $\text{Si}_{1-x}\text{Ge}_x$ region. In the evaluation of the recombination component, the key difference between the two diodes is the electron concentration in the $\text{Si}_{1-x}\text{Ge}_x$ region. The p-i-n structure has a high concentration of electrons within the i-SiGe region, close to the heterojunction interface.

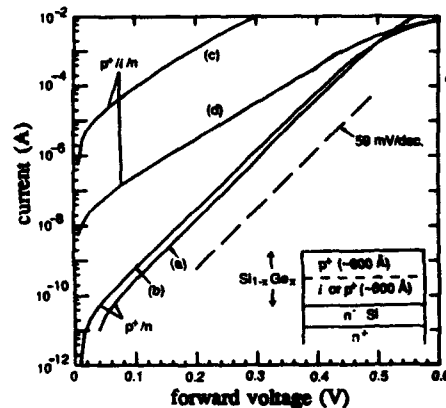


FIG.1. Room-temperature current vs voltage for p^+-i-n and corresponding p^+-n heterojunction diodes with various oxygen concentration in the $SiGe$. The oxygen concentrations are (a) 2×10^{20} , (b) 8×10^{18} , (c) 3×10^{20} and (d) $2 \times 10^{18} \text{ cm}^{-3}$.

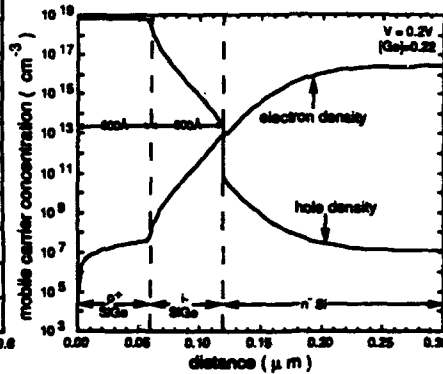


Fig. 2. Calculated carrier concentration profiles as $V = 0.2V$ for a p^+-i-n diode with a germanium fraction of 22% and p^+ layer and i -layer thicknesses of 600 Å.

The large electron concentration, combined with low lifetimes in oxygen doped $Si_{1-x}Ge_x$ implies that the diffusion currents are much smaller than $I_{rec}(Si_{1-x}Ge_x)$ in Eq 1. In contrast, in the corresponding $p-n$ structure the space charge region in the $Si_{1-x}Ge_x$ is extremely thin and the electron concentration in this region is low. Therefore, the space charge region recombination is small compared to the diffusion current.

SEDAN was used to fit the measured I-V characteristics by varying the minority carrier lifetime in the $Si_{1-x}Ge_x$ in the Shockley-Read-Hall (SRH) model. Figure 3 illustrates a comparison of measured (solid lines) and simulated I-V characteristics (symbols) for $p^+SiGe-iSiGe-nSi$ and corresponding $p^+SiGe-nSi$ diodes. The simulations indicate the high sensitivity of the $p^+SiGe-iSiGe-nSi$ device to minority carrier lifetime. The sensitivity of the $p-i-n$ structure, whose I-V characteristics are shown in figure 3, to various physical parameters has been analyzed in reference [7]. Calculations also indicate that for Auger coefficients comparable to Si, Auger recombination is negligible in these thin $p^+SiGe-iSiGe-nSi$ structures.

MAXIMUM EXTRACTED LIFETIME

In order to extract the lifetime from the current characteristics of $p-i-n$ diodes, the diode current must be dominated by recombination in the $Si_{1-x}Ge_x$ layer. For large lifetimes, the recombination current in the $p-i-n$ diode becomes negligible compared to the diffusion component, and therefore, the current is independent of the lifetime in $Si_{1-x}Ge_x$. Thus, the magnitude of the diffusion current determines the maximum lifetime which can be extracted from the current characteristics of $p-i-n$ diodes. The diffusion current can easily be calculated using SEDAN by simulating the I-V characteristics of the $p-i-n$ diodes for arbitrarily large minority carrier lifetimes. We define the maximum lifetime, τ_{max} , to be the lifetime at which the recombination current is equal to the diffusion current. The lifetime

arbitrarily large minority carrier lifetimes. We define the maximum lifetime, τ_{max} , to be the lifetime at which the recombination current is equal to the diffusion current. The lifetime parameter is varied in SEDAN until the recombination and diffusion currents are equal at a fixed bias. Figure 4 shows the qualitative trend of diode current with respect to lifetime. The diode current becomes insensitive to the minority carrier lifetime for all times greater than τ_{max} (the shaded region on the graph). Neglecting the peripheral current, the maximum lifetime which can be extracted from a given diode structure can be increased by performing I-V measurements at a lower temperature. This is because the diffusion current decreases as n_i^2 while the recombination current decreases as n_i . The ratio of the recombination to diffusion components is, therefore, higher at the lower temperatures. Device modelling using SEDAN indicates that there is a factor of three increase in the maximum extracted lifetime, τ_{max} , for a drop in temperature from 300°K to 260°K.

OTHER STRUCTURES

a. $p^+SiGe-nSiGe-nSi$ and $p^+Si-nSiGe-nSi$ diodes:

The $p^+SiGe-nSiGe-nSi$ device, in which the i-region of a $p^+SiGe-iSiGe-nSi$ diode is replaced by an intentionally doped (10^{17} cm^{-3}) $n-Si_{1-x}Ge_x$ region, is also quite suitable for extraction of minority carrier lifetime. In general, the maximum recombination occurs at the point where the hole concentration is equal to the electron concentration, $p=n=n_i \exp(qV/2kT)$. The increase in the dopant concentration in the $n-Si_{1-x}Ge_x$ moves the point of maximum recombination away from the $Si-Si_{1-x}Ge_x$ interface, towards the bulk of the $Si_{1-x}Ge_x$. This shift in the position of maximum recombination rate is important in order to differentiate interfacial recombination from bulk recombination.

In order to increase the maximum extracted lifetime, τ_{max} , the diffusion current needs to be reduced. Assuming otherwise identical layer dopings and thicknesses, replacing the $p^+Si_{1-x}Ge_x$ cap in the p-i-n or p-n-n diode by a p^+Si cap reduces the diffusion current at the depletion layer edge. This results from the smaller intrinsic carrier concentration in Si compared to $Si_{1-x}Ge_x$. Lifetimes in excess of 100 μs can be extracted by increasing the thickness and doping of Si cap and $n-Si$ regions. However at small diode currents, peripheral leakage starts to dominate and, therefore, becomes the limiting factor in extracting high lifetimes in $Si_{1-x}Ge_x$. For our p-i-n diodes, with Ge fraction of approximately 22%, the typical peripheral current density, J_p , is on the order of $1 \times 10^{-9} \text{ A/cm}$ at 0.1V forward bias. Table 1 shows the magnitudes of maximum extracted lifetimes, τ_{max} , for various diode structures with cap thickness of 600Å, $Si_{1-x}Ge_x$ thickness of 600Å and $n-Si$ buffer layer thickness of 2 μm . The drop in the maximum extracted lifetime, τ_{max} , by a factor of ten between the ideal case ($J_p=0$) and real case (finite J_p) implies that the limitations imposed by the peripheral current on extraction of high lifetimes in $Si_{1-x}Ge_x$ can be important. For a given interfacial r_{sp} density, maximizing area to perimeter ratio of the diode structure is required in order to increase the maximum extracted lifetime. The peripheral current can also be reduced by moving the $Si_{1-x}Ge_x-SiO_2$ interface away from the active device region.

TABLE 1

STRUCTURE	Ideal $J_p = 0$	Realistic Finite J_p
	τ_{max} (300K)	τ_{max} (300K)
$p^+(SiGe) - i(SiGe) - n(Si)$	1 μsec	1 μsec
$p^+(SiGe) - n(SiGe) - n(Si)$	0.6 μsec	0.6 μsec
$p^+(Si) - i(SiGe) - n(Si)$	30 μsec	2-3 μsec

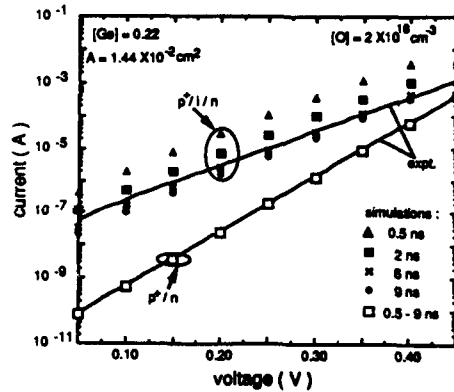


Fig. 3. Comparison of measured (solid lines) and simulated (symbols) diode currents for p-i-n and corresponding p-n diodes. The layer structure is shown in the inset of Fig. 1.

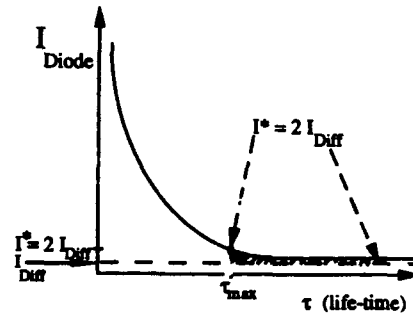


Fig. 4. Qualitative trend indicating the variation in the p⁺-i-n diode current with respect to the lifetime in Si_{1-x}Ge_x. The shaded region shows the insensitivity of the diode current to the lifetime in Si_{1-x}Ge_x for all $\tau > \tau_{max}$.

[O] VS LIFETIME

Various two terminal and three terminal structures have been used to extract the lifetime in oxygen-doped Si_{1-x}Ge_x. Fig. 5 summarizes the lifetime trends. The lifetime increases by more than four orders of magnitude as the oxygen concentration decreases from 2X10²⁰ to 3X10¹⁷ cm⁻³. A sensitivity analysis was used to determine the vertical error bars, which include the effect of uncertainties in the value of intrinsic carrier concentration, n_i in Si_{1-x}Ge_x. The shaded region is associated with diodes with (1) oxygen content below the SIMS detection limit, and (2) I_{Rec} < I_{Diff} ($\tau > \tau_{max}$). We have also extracted lifetimes in Si_{1-x}Ge_x for oxygen concentrations in the range of 5X10¹⁹ cm⁻³, from HBT base current and current gain data reported in Refs. 5, 6 and 11. In these HBTs, the base current is dominated by recombination in the Si_{1-x}Ge_x base.

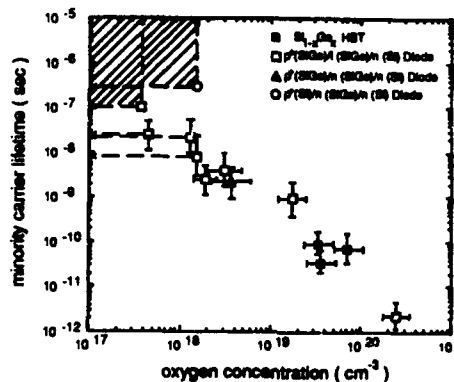


Fig. 5. Lifetime trends in oxygen doped Si_{1-x}Ge_x films, for 0.13 < x < 0.22. The open symbols represent lifetime data from various diodes, while the closed symbols represent lifetimes extracted by simulating data for Si/Si_{1-x}Ge_x HBTs. The shaded region indicates the approximate sensitivity limits for determining the oxygen content and lifetime in the p⁺-i-n diodes. The data points with arrows pointing to the left are associated with diodes with oxygen content below SIMS detection limits and I_{rec} >> I_{diff} ($\tau < \tau_{max}$).

SUMMARY

Extraction of the recombination lifetimes from the forward current characteristics of $p^+SiGe-iSiGe-nSi$, $p^+SiGe-nSiGe-nSi$ and $p^+Si-nSiGe-nSi$ diodes has been presented. A comparison of the maximum lifetimes, τ_{max} , which can be extracted from such structures is discussed. Neglecting the peripheral current component and assuming identical layer thicknesses for all diodes, the $p^+Si-nSiGe-nSi$ diode has the highest τ_{max} , with a magnitude on the order of 30 μ sec at 300K. However, with the typical peripheral current density, which is on the order of 1×10^{-9} A/cm at 0.1V bias, the maximum lifetime which can be extracted from the $p^+Si-nSiGe-nSi$ diode drops to 3 μ sec. These diode structures have been fabricated in order to evaluate the effect of the oxygen incorporation on the recombination lifetime in the $Si_{1-x}Ge_x$. Results indicate that oxygen plays a key role in determining the recombination lifetime in the $Si_{1-x}Ge_x$ at concentrations above 3×10^{17} cm^{-3} . The magnitude of the recombination lifetime increases from 4 psec at an oxygen concentration of 2×10^{20} cm^{-3} to above 0.5 μ sec at concentrations below 3×10^{17} cm^{-3} .

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SINGLE AND SYMMETRIC DOUBLE TWO-DIMENSIONAL HOLE GASES
AT Si/SiGe HETEROJUNCTIONS GROWN BY RAPID THERMAL
CHEMICAL VAPOR DEPOSITION

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ABSTRACT

Two dimensional hole gases have been investigated in Si/SiGe modulation doped heterostructures grown by RT-CVD for the first time. Single, both normal and inverted, and double heterostructures were studied. The results suggest that any asymmetry due to dopant segregation or autodoping between the normal and inverted structures occurs on a scale of less than 1 nm.

INTRODUCTION

The last few years have seen enormous advances in our understanding of the Si/SiGe material system for its potential applications in the fabrication of high-speed devices and optoelectronic circuits on Si [1]. Rapid Thermal CVD (RT-CVD) has emerged as a competing growth technology for fabricating these structures. Unlike MBE or UHV-CVD, this does not require ultrahigh vacuum techniques, and the growth temperature can be optimised for each individual layer. State-of-the-art devices like the MODFET and the resonant tunneling diode place stringent requirements on doping profiles and interface quality. It is therefore very desirable to characterize interface abruptness of epitaxial films grown in such an environment. Material analysis techniques like SIMS and RBS lack resolution on the scale of angstroms. The two dimensional hole gas confined at a modulation doped interface is however very sensitive to the heteroepitaxial interface region, making it an excellent probe for characterization. No previous modulation doping results have been reported for RT-CVD. Initial double heterostructures grown by MBE showed good carrier confinement and low temperature mobilities [2]. Further investigations of single heterostructures by SIMS showed that dopant segregation in MBE destroys the symmetry of the normal and inverted interfaces [3] resulting in different carrier mobilities. This is reminiscent of the well established AlGaAs/GaAs system, where an order of magnitude difference in mobility has been observed for a number of years in the best quality structures. Si/SiGe structures grown by a UHV-CVD technique apparently did not show this effect [4].

We have fabricated p-type modulation doped structures using RT-CVD and characterized the two interfaces using electrical measurements. Double heterojunction structures were also investigated using low-temperature magnetoresistance experiments. The results are described in the next section.

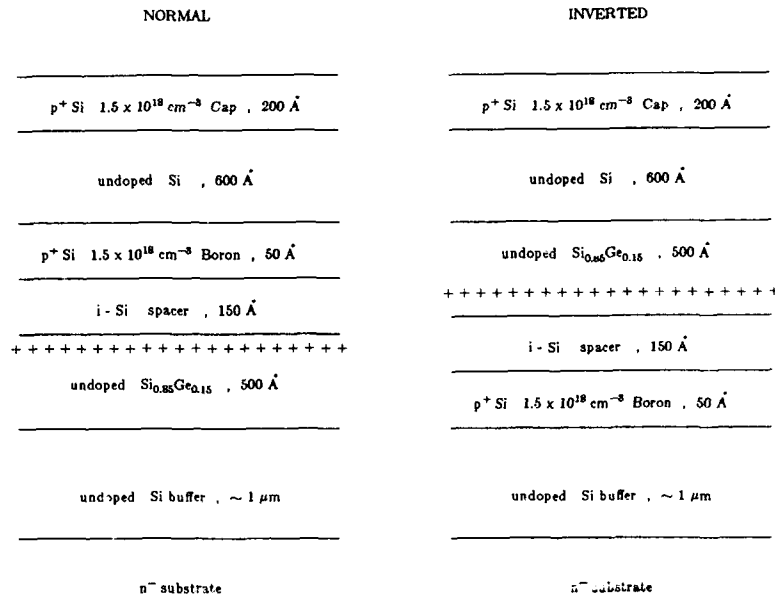


Fig. 1. Normal and inverted modulation doped heterostructures.

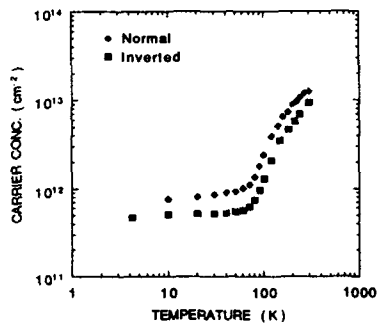


Fig. 2. Carrier concentration as a function of temperature for the normal and inverted heterostructures.

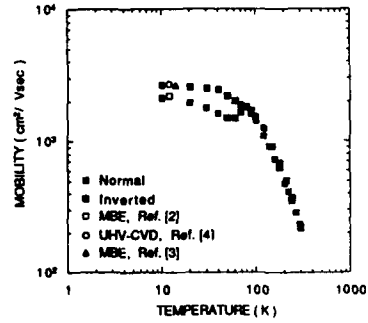


Fig. 3. Mobility as a function of temperature. The open symbols represent data from similar structures grown by MBE and UHV-CVD obtained from references [2],[3], and [4].

EXPERIMENT AND RESULTS

The growth system used is an RT-CVD reactor. The wafer sits on a quartz stand inside a cold wall quartz tube and is heated by a bank of tungsten halogen lamps. Dichlorosilane and germane are used as source gases while diborane is used for the p-type doping. The temperature of the wafer is accurately monitored using a novel infrared transmission technique with resolution of one degree [5]. All structures are grown on lightly doped n-substrates. Growth of epitaxial films is controlled by switching gas flows, not wafer temperature. The growth temperature is optimized individually for each layer. Growth starts with a silicon buffer layer grown at 1000 °C. The subsequent Si layers are grown at 700 °C while the SiGe alloy layers are grown at 625 °C. Single modulation doped heterostructures are shown in Fig. 1. The normal and inverted structures had a spacer width of 150 Å, doping concentrations $1.5 \times 10^{18} \text{ cm}^{-3}$ and germanium fractions of 15%. The doping and thicknesses are estimated from SIMS and calibrated growth conditions.

Standard van der Pauw and Hall bar geometries were lithographically defined and mesa-etched using a plasma etching system. Aluminum contacts were then evaporated and annealed at 500 °C for 20 minutes in a forming gas atmosphere. This yielded good ohmic contacts down to very low temperatures. Gold wires were bonded to the contacts for external electrical measurements.

Hall measurements were carried out from room temperature down to 10 K in a magnetic field of 0.2 T. Mobility is calculated from the measured resistivity and carrier density of the sample. The results are plotted in Figs. 2 and 3. The mobility rapidly increases as the temperature is lowered and saturates at about $2500 \text{ cm}^2/\text{V}\cdot\text{s}$ for the single heterostructures. The carrier concentration at the same time decreases and saturates at about $5 \times 10^{11} \text{ cm}^{-2}$. No freeze-out is observed even at 4.2 K. This indicates a degenerate system of carriers well separated from ionized impurities. The peak mobilities at 10 K in these structures compare very well with those reported in similar structures grown by UHV-CVD and MBE techniques [2,3,4]. To confirm the two-dimensional carrier confinement at the heterointerface, magnetoresistance experiments were carried out at liquid He temperatures in high magnetic fields. The longitudinal resistance of the sample shows well defined Shubnikov-deHaas oscillations which are periodic in the reciprocal field [6]. From the period, we obtain a carrier density of $4.8 \times 10^{11} \text{ cm}^{-2}$ which agrees very well with $4.7 \times 10^{11} \text{ cm}^{-2}$ obtained from the Hall slope. This indicates little parallel conduction and a single carrier channel as expected. The low temperature mobilities and carrier densities in the normal and inverted structures however differ by 20%. This could either be due to small changes in growth conditions between the two samples or some physical asymmetry induced during growth. In order to resolve this, we carried out measurements on a symmetric double heterojunction structure shown in Fig. 4. The sample had a 50 Å spacer with a doping level of $3 \times 10^{18} \text{ cm}^{-3}$ and a germanium fraction of 20%. Electrical results are shown in Figs. 5 and 6.

The double heterostructure shows lower mobility and higher carrier density because of the smaller spacer width and higher doping level. The mobility saturates at $1000 \text{ cm}^2/\text{V}\cdot\text{s}$ with no carrier freeze-out. Tilted field Shubnikov deHaas experiments were carried out at 2.3 K in magnetic fields upto 9 T. The oscillations follow the component of the magnetic field perpendicular to the sample, indicating good two dimensional confinement of the carriers. Fig. 7 shows the longitudinal resistivity of the sample as a function of magnetic field normal to the surface. The periodic nature of the oscillations is evident from the calculated fourier spectrum shown in Fig. 8. The single peak indicates one carrier channel or two or more channels with

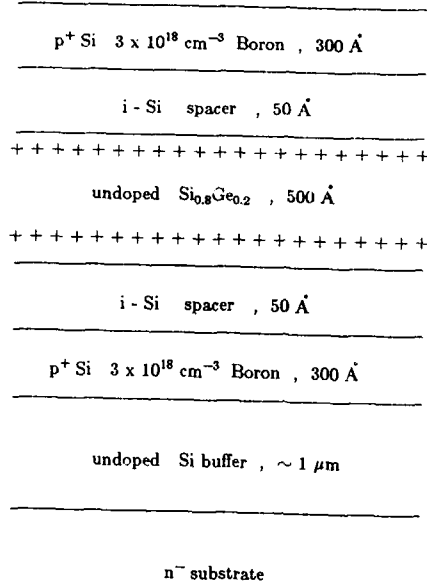


Fig. 4. Symmetric double heterostructure.

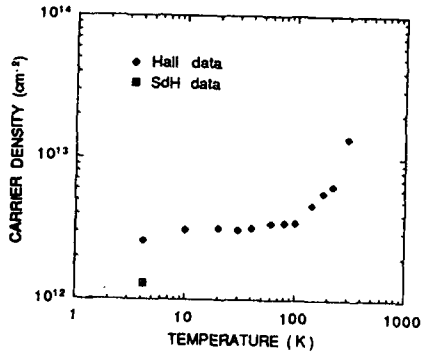


Fig. 5. Carrier density as a function of temperature for the double heterostructure. For comparison, the density obtained from the Shubnikov deHaas oscillations is also shown.

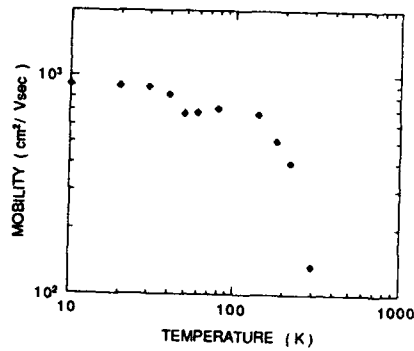


Fig. 6. Mobility as a function of temperature for the double heterostructure.

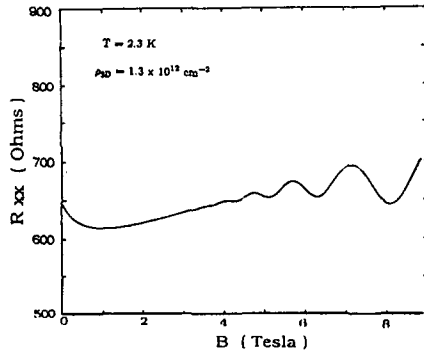


Fig. 7. Longitudinal resistivity of the double heterostructure sample as a function of the normal magnetic field, showing well known Shubnikov deHaas oscillations.

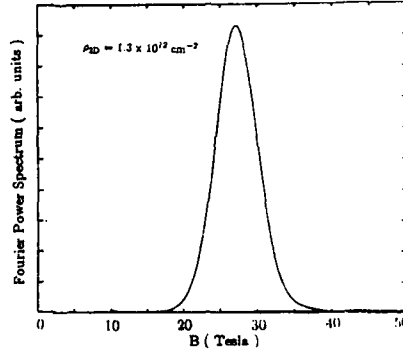


Fig. 8. Fourier analysis of SdH oscillations for the double heterostructure.

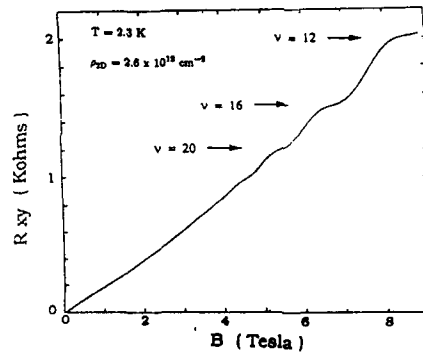


Fig. 9. Quantized Hall Effect in the double heterostructure. The plateau values are quantized at $R_H = h/e^2\nu$, where ν is even.

similar densities. From the position of the peak, we obtain a carrier density of $1.3 \times 10^{12} \text{ cm}^{-2}$ which is half of the value $2.6 \times 10^{12} \text{ cm}^{-2}$ obtained from the Hall slope. This indicates that the double heterostructure has two symmetric hole gases at the two interfaces, as expected. To rule out any parallel conduction accounting for the difference, we examined the high field Hall data shown in Fig. 9 more carefully. The sample shows the Quantized Hall plateaus with the resistance value, without resolving spin degeneracy, normally given by $R_H = h/e^2\nu$ where h is Planck's constant, e is the electron charge and ν is an even integer. The data shows plateaus for $\nu = 12, 16, 20$ but is missing $\nu = 14$ and $\nu = 18$. The fact that we see only multiples of even integers confirms that we indeed have two symmetric 2-D channels with no parallel conduction elsewhere, since two symmetric channels in parallel would have resistance plateaus at $R_H = h/2e^2\nu$. Similar results for symmetric double heterostructures have been obtained by UHV-CVD growth at a temperature of 550° C [4].

DISCUSSION

The low temperature mobilities and carrier concentrations of the normal and inverted structures differ only by 20%. Moreover the inverted structure shows lower carrier density, contrary to what one might expect if there was any dopant segregation. The small difference is therefore attributed to slightly different growth conditions, as the two samples were grown three weeks apart. Low temperature magnetoresistance experiments on the double heterostructure clearly reveal the symmetry of the two interfaces. From the width of the Fourier spectrum, we estimate a difference of 10% in the carrier densities at the two interfaces. Simulations of band structures of single heterojunctions correlate this to a difference of 10 Å in spacer widths, indicating that any segregation or outdiffusion of boron in our samples is of this order. That similar results have only been reported by UHV-CVD [4] suggests that a hydrogen (or chlorine) terminated surface during CVD growth suppresses dopant segregation, even up to growth temperatures of 700 °C in our case.

SUMMARY

Growth of high-quality Si/SiGe modulation doped heterostructures has been demonstrated using the RT-CVD technique. Peak mobilities in these structures are comparable to those grown by other UHV techniques. Normal and inverted modulation doped interfaces show similar characteristics indicating negligible dopant segregation, which may be due to a hydrogen or chlorine terminated growth surface. Abrupt doping profiles for high-speed device applications can thus be achieved.

ACKNOWLEDGEMENTS

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MAGNETO-TRANSPORT MEASUREMENTS ON Si/Si_{1-x}Ge_x
 RESONANT TUNNELING STRUCTURES

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ABSTRACT

We have investigated magneto-transport properties of differently strained Si/Si_{1-x}Ge_x resonant tunneling devices. The built-in strain was either put in the Si layers, by means of a thick, relaxed Si_{1-x}Ge_x buffer layer, or in the Si_{1-x}Ge_x layers, in which case all Si_{1-x}Ge_x layers were grown below the critical thickness, and a Si_{1-x}Ge_x spacer layer with graded Ge content was used. Magnetic fields parallel to the interface have been employed to probe the in-plane dispersion in the quantum well. This is used to study the effect of band-mixing in the two strain configurations. A field perpendicular to the interface resolves some Landau level splitting. Most strikingly, however, is the similarity in the spectra with the case when the magnetic field is applied parallel to the interfaces. This indicates broadening of the levels, possibly due to scattering, and the importance of 3-dimensional band structure effects.

INTRODUCTION

Recently, a number of groups have demonstrated Si/Si_{1-x}Ge_x resonant tunneling devices (RTD) [1-4]. The strain and strain relaxation in these structures play an important role for the tunneling characteristics. Two basic RTDs are of interest: (a) The double barrier is grown on a thick, relaxed Si_{1-x}Ge_x layer, so that only the Si barriers are strained. The buffer introduces dislocations, some of which propagate through the structure, and are expected to influence the tunneling characteristics by increasing carrier scattering. (b) Structures which are pseudomorphically grown, with the strain in the Si_{1-x}Ge_x well. The critical thickness of the Si_{1-x}Ge_x layers limits the thickness to which the layers can be grown. Due to dopant diffusion, it is necessary to introduce an undoped spacer layer in front of the Si barriers. Preferably, this is made as large as possible, to limit any interference in carrier transport by the band offset at the interface between the Si contact and the Si_{1-x}Ge_x spacer layers. In order to reduce the constraint imposed by the critical thickness, it is possible to use graded Si_{1-x}Ge_x spacer layers. By adjusting the Ge gradient and placing of the p⁺ doping interface, nearly flat equilibrium valence band profiles on either side of the double barrier structure can be achieved.

The I-V characteristics of hole-RTDs display complicated resonance spectra due to the light-hole and heavy-hole valence bands. Strain affects both the positions and the band-mixing between the two sets of resonances. Magnetic field transport studies provide a valuable tool to study the carrier conduction through these struc-

tures. It has recently been shown that magnetotunneling can be used to probe the dispersion relations of the levels in the quantum well [5]. These measurements can thus be used to obtain information on the conduction mechanism in Si/Si_{1-x}Ge_x hole RTDs. We have grown structures of both type (a) and (b), in order to investigate the effect of strain on transport characteristics. Magneto-transport measurements have been performed, with magnetic fields up to 30 T, with the field both parallel ($B_{||}$) and perpendicular (B_{\perp}) to the interfaces of the structures. In-plane dispersion relations of the quantum well states studied with $B_{||}$ shows large non-parabolicity, and negative in-plane effective masses for some of the levels. With B_{\perp} , Landau level splitting of some resonances is observed, but a large similarity between the spectra for the two field directions is also seen. This is further investigated by tilting the B-field with respect to the plane of the interfaces.

EXPERIMENTAL

Samples with strained and unstrained well were grown using MBE. Two such structures are shown in Figs. 1a and 1b. Cross-sectional TEM revealed no defects in the structure (b), whereas (a) displayed a large dislocation density at the start of the buffer layer, which is then reduced closer to the double barrier structure. In both cases the interfaces are sharp to within a couple of monolayers. Calculations of the band diagram for the structure (b), using a Poisson solver, indicate that the valence band edge in the spacer layer and contact is relatively flat. To test the importance of the graded spacer, similar RTDs were grown, with and without the Ge gradient. The I-V characteristics of the samples without graded spacer show a marked degradation, displaying only very weak resonances in the dI/dV -V characteristics (see Fig. 2).

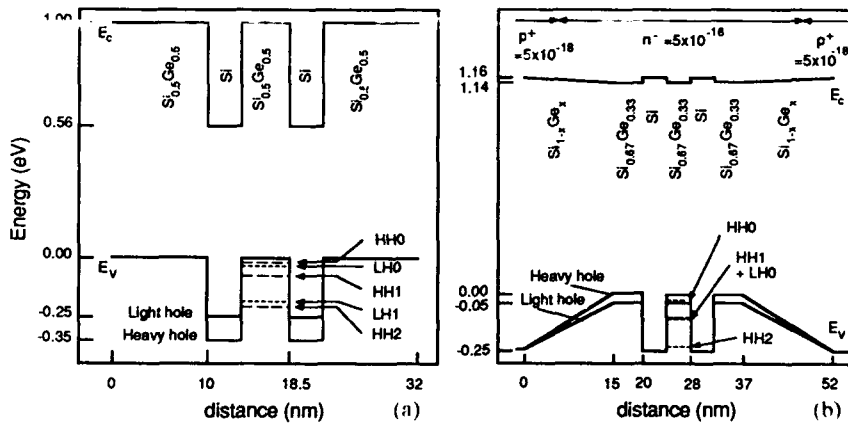


Fig. 1. Schematic band diagram of the RTD structures used in the measurements. (a) Structure with strained barriers, grown on a relaxed Si_{1-x}Ge_x buffer layer. (b) Fully pseudomorphic structure with strained well and spacer layers with graded Ge content.

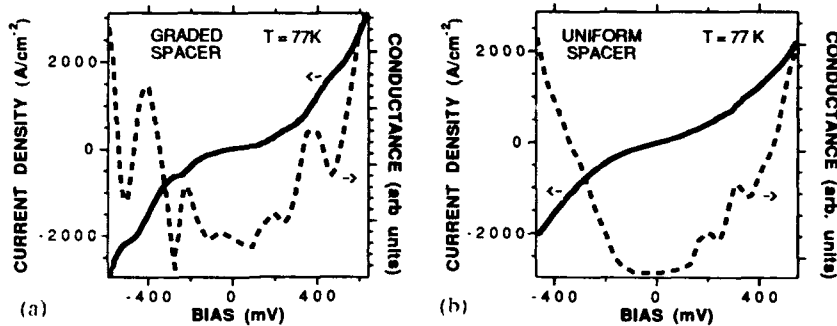


Fig. 2. I-V and dI/dV -V characteristics for structures with strained $\text{Si}_{0.75}\text{Ge}_{0.25}$ wells. (a) Sample with graded spacer. (b) Sample with 250 Å thick spacers with uniform Ge content.

I-V and dI/dV -V characteristics for Sample (a) and (b) exhibited five and three resonances, respectively. In order to observe all resonances, small devices (diameter $\leq 5\mu\text{m}$) were used. Calculations by self-consistently solving the Schrödinger's Equation separately for the light hole and heavy hole bands indicate the existence of three heavy hole states and two light hole states for structure (a) (see Fig. 1a). The effective masses for the $\text{Si}_{1-x}\text{Ge}_x$ layers used in these calculations were obtained by interpolating between the Si and Ge effective masses, without considering any band-mixing. Structure (b) has 4 states; however, the light hole 0 (LH0) and heavy hole 1 (HH1) states lie very close together, and may not be distinct (see Fig. 1b).

dI/dV characteristics for Sample (a), for different magnetic fields applied parallel to the interfaces, are shown in Fig. 3. The resonance voltages experience shifts, and the peaks broaden, as the field increases. Surprisingly, the fifth peak moves to smaller voltages. In Fig. 4a we show the shifts as a function of B_{\parallel} . The field probes the quantum well states away from the $k = 0$ minima, and maps out the in-plane dispersion relations, $E(k_{\parallel})$ [5]. The states display a large non-parabolicity, especially in the case of the highest resonance, which shows a negative in-plane effective mass. Corresponding curves are shown for the resonances of structure (b) in Fig.

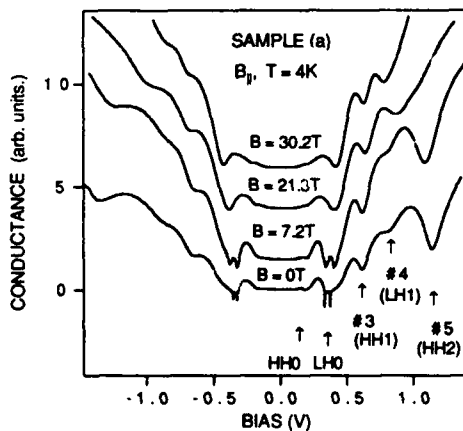


Fig. 3. dI/dV -V characteristics for Sample (a) at $T = 4\text{ K}$, with different magnetic fields applied parallel to the interfaces. The y-axis has been shifted between each curve.

5. Here, the shifts appear more regular at low fields, but for $B_{\parallel} \geq 24$ T the second resonance starts moving towards lower voltages.

In Fig. 4b we show the resonance voltages for Sample (a), as B_{perp} is applied. Two observations can be made: First, two extra resonances emanate from the HH0 resonance. By tilting the field, from B_{perp} to B_{\parallel} , we are able to show that they are due to Landau level splitting. Only the perpendicular component of the field determines the separation of the levels, as one expects for Landau levels. Secondly, the other resonances experience shifts conspicuously similar to those due to B_{\parallel} . This indicates a 3-dimensionality of the magnetic effects in the system, in spite of the 2-dimensional confinement of the carriers in the quantum well, as manifested by the Landau-level splitting of HH0. This effect is further investigated by tilting the field. In Fig. 6 the shift of LH0 is shown as a function of the tilt-angle θ , for different values of the magnetic field. As the curves traced out are qualitatively comparable, the similarity between the two field directions is further demonstrated. In contrast, for resonances in electron RTDs, where conduction occur through a single, parabolic band minima, the B_{\parallel} induced shift depends quadratically [6], and the B_{perp} induced shift linearly [7] in the magnetic field. Such a dependence is not observed here. We also note that there are quantitative differences in the shifts due to B_{\parallel} and B_{perp} . The LH0 resonance experiences a larger shift in the parallel direction, whereas the fifth peak, for fields were #4 and #5 still can be distinguished, shifts more in the perpendicular direction.

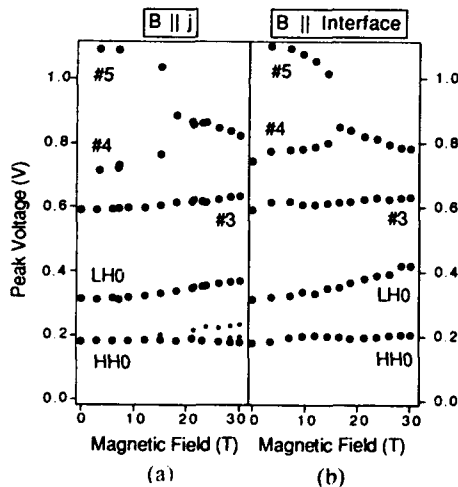


Fig. 4. Resonance voltages of Sample (a) as a function of magnetic field, a) applied parallel to the interfaces, b) applied perpendicular to the interfaces.

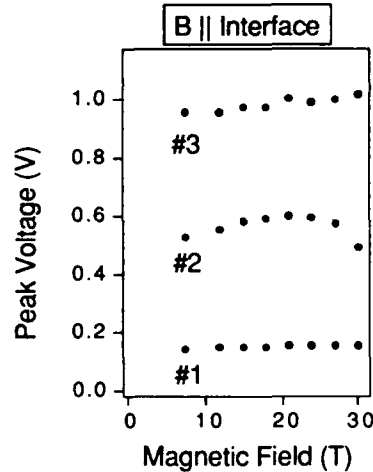


Fig. 5. Resonance voltages of Sample (b) as a function of magnetic field applied parallel to the interfaces.

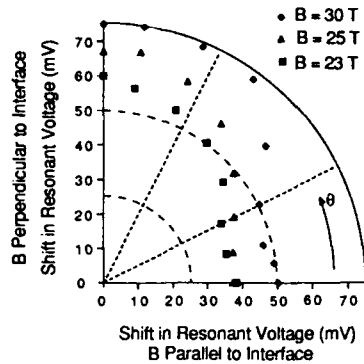


Fig. 6. Shift of the LHO resonance of Sample (a) as a function of angle θ between the magnetic field and the interfaces, for different values of the magnetic field.

DISCUSSION

During the tunneling process, the transverse canonical momentum is conserved. With the magnetic field parallel to the interface, the tunneling carriers receive additional transverse momentum through the Lorentz force. The holes tunnel through states with in-plane momentum $k_{\parallel} = qB\Delta_s$, where Δ_s is the average separation between the carriers in the emitter and the well. The magnetic field also adds to the energies of the well states, but for small magnetic fields this contribution is smaller than the in-plane kinetic energy. Thus Figs. 4a and 5 shows the in-plane dispersion relations for each level, and it is possible to compare the in-plane effective masses with each other. However, to obtain quantitative values of the effective masses, the potential drop in the depletion layer has to be taken into account. When the magnetic length, $L = (\hbar/eB)^{1/2}$, is of the order of the well width, w , the magnetic energy will be important. At the highest fields measured this may have to be taken into account, as in the case of the second peak in Sample (b), where the resonance shifts to lower energies. As no spin splitting is observed, the spin appears to be conserved during tunneling, and no shift will therefore be seen due to spin effects.

We believe the lack of observed Landau level splitting may be due to broadening of the levels (due to alloy scattering, interface roughness, or scattering from dislocations) too large for most of the splittings to be resolved. The similarity between the shifts for B_{perp} and B_{\parallel} is not yet well understood. However, due to the broadening, it is possible that the resonances only are seen where there is a large density of coalesced Landau states. The comparable shifts for the two field directions is thus a manifestation that both in-plane dispersion relations and Landau levels in the valence band are influenced more by the repulsion of other levels than their individual behaviour, which would be linear and quadratic as a function of the magnetic field, respectively.

CONCLUSION

Two types of Si/Si_{1-x}Ge_x hole resonant tunneling structures, with the strain either in the Si or in the Si_{1-x}Ge_x layers have been investigated. For the latter, we have presented a new design, where the Si_{1-x}Ge_x spacer layer has a graded Ge content, to improve the I-V characteristics. Magneto-transport measurements of the RTDs, with the magnetic field parallel to the interfaces, probe the in-plane dispersion relations of the Si_{1-x}Ge_x quantum wells. Band-mixing can be considerable, producing negative in-plane effective mass. When the magnetic field is applied perpendicular to the interfaces, Landau level splitting can be seen for the lowest level. However, the most striking observation is the similarity between the effects of magnetic field parallel and perpendicular to the interfaces. The absence of more Landau levels than those observed shows that the levels are broadened, possibly due to scattering, whereas the shifts of the observed levels indicate the importance of 3-dimensional band structure effects in interpreting the results.

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HIGH MOBILITY TWO-DIMENSIONAL ELECTRON GAS IN MODULATION-DOPED Si/SiGe HETEROSTRUCTURES

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ABSTRACT

We report record-high electron mobilities obtained in the Si/SiGe alloy system via single-junction n-type modulation-doped Si/Si_{0.7}Ge_{0.3} heterostructures grown by the ultra-high vacuum chemical vapor deposition technique. Peak electron mobilities as high as 1,800 cm²/Vs, 9,000 cm²/Vs and 19,000 cm²/Vs were measured at room temperature, 77K and 1.4K, respectively. These high mobilities resulted from excellent Si/SiGe interfacial properties by employing a compositional graded Si/SiGe superlattice prior to the growth of a thick Si_{0.7}Ge_{0.3} buffer, which brought about a dramatic reduction of the threading dislocation density in the active Si channel. Two thin phosphorous-doped layers were incorporated in the SiGe barrier and at its surface to supply electrons to the Si channel and to suppress the surface depletion, respectively. The transport properties of these heterostructures were determined to be those of a two dimensional electron gas at Si/SiGe heterointerfaces at low temperatures.

INTRODUCTION

Recent advances in low temperature epitaxial growth techniques have stimulated a great deal of research in heteroepitaxy. The Si/SiGe system has received additional interest because it provides not only the advantages of bandgap engineering but also the maturity of Si and Ge technology, which can be easily blended into advanced device fabrication [1]. Though there are many low temperature growth techniques which have been developed in the last few years, the ultra high vacuum/chemical vapor deposition (UHV/CVD) technique has been shown to be one of the best methods for growing high quality Si/SiGe heterostructures [2]. To date, the highest f_T PNP and NPN Si/SiGe heterojunction bipolar transistors have been fabricated by exploiting this growth technique [3]. We have also reported the highest hole mobility obtained for Si-like materials in UHV/CVD grown p-type modulation-doped Si/SiGe heterostructures [4]. In this work, we report the highest electron mobility and sheet conductance ever obtained for this material system via n-type modulation-doping techniques.

For Si/SiGe heterostructures, under equilibrium, the conduction band edge of Si is slightly higher than that of SiGe, and most of the bandgap offset between Si and SiGe is at the valence band, i.e. $\Delta E_c \gg \Delta E_v$. It has been shown that, in order to form a significant conduction band offset at Si/SiGe heterointerfaces, Si has to be under tensile strain and higher Ge content in SiGe layer is demanded [5]. To achieve the above requirements without facing problems of critical layer thickness, a thick strain symmetrization/relaxation SiGe buffer with a Ge content equal to the average of the Si and SiGe layers were grown prior to the growth of the Si/SiGe modulation doped structures. In this case, the Si layers were in tensile strain and SiGe layers were in compressive strain. For Ge at 50%, Abstreiter et. al. obtained a conduction band edge offset of 150 meV between Si/SiGe with the band edge of the Si lower than that of the SiGe. Therefore, a n-type modulation-doped Si/SiGe heterostructure was realized when the SiGe was doped by Sb and Si was left undoped [5]. However, in that work the thick SiGe buffer was relaxed, with a misfit dislocation density of $10^9 - 10^{10} \text{ cm}^{-2}$, the threading of these dislocations to the active Si/SiGe heterointerfaces degraded the transport properties of those heterostructures. An electron mobility of 2,000 cm²/Vs has been reported. Recently, much higher electron mobility has been reported by Schäffler and Jorke in a multi quantum well n-type modulation-doped structure, presumably in part due to the reduction of extended defects [6].

In view of device applications, especially for field effect transistors, a single well structure is required to obtain optimal performance.[7]. We present the first observation of two-dimensional electron gases in a single-heterojunction n-type modulation-doped Si/SiGe structure.

EXPERIMENTAL PROCEDURES

Figure 1 shows a schematic drawing of the layers deposited for n-type modulation-doped Si/SiGe heterostructures. All layers were grown in a UHV/CVD system at 550°C on twelve 5" p-Si substrates. Typically, this growth technique offers a very low background impurity concentration [8]. In order to minimize the density of threading dislocations at the active Si/SiGe junction, a compositionally graded Si/SiGe superlattice, 100 nm thick, with Ge concentrations up to 30%, was first grown and followed by a 60 nm thick $\text{Si}_{0.7}\text{Ge}_{0.3}$ buffer layer. Detailed transmission electron microscopic work, both plane and cross-sectional views, showed that most, if not all, the threading dislocations were blocked by such a superlattice buffer [9]. An etched pit density of low 10^4 cm^{-2} was measured for such layers after a dilute Schimmel etch. Following the thick $\text{Si}_{0.7}\text{Ge}_{0.3}$ buffer, a Si channel layer of 6 nm was deposited and followed by a $\text{Si}_{0.7}\text{Ge}_{0.3}$ spacer layer with thickness ranging between 1.5 and 4 nm. In this case, the Si layer was fully strained and resulted in a maximum conduction band offset at Si/SiGe interface. In a separate study, we found a conduction band offset of $\approx 150 \text{ meV}$ for such a heterostructure [10]. Because the incorporation of phosphorous decreased dramatically as Ge content in the SiGe layer increased with the UHV/CVD technique, we imbedded a $2.5 \times 10^{18} \text{ cm}^{-3}$ phosphorous doped $\text{Si}_{0.86}\text{Ge}_{0.14}$ layer between two undoped $\text{Si}_{0.7}\text{Ge}_{0.3}$ layers. Finally, these layers were capped by a 4 nm $\text{Si}_{0.86}\text{Ge}_{0.14}$ and a 4 nm Si layers doped with phosphorous to $2.5 \times 10^{18} \text{ cm}^{-3}$. These layers were employed to ease ohmic contacts fabrication and to screen the electron gas from the surface states.

Conventional Hall methods using a standard van der Pauw configuration with a magnetic field of 0.5 T were used to measure the electron concentration and mobility across a temperature range of 12-300 K. Au/Sb alloy was evaporated onto these samples and followed by a 30 seconds anneal at 300 °C in forming gas ambient to form ohmic contacts. Shubnikov-de Haas (SdH) measurements with magnetic fields up to 12 T were performed at 1.4 K to characterize the transport properties of the two-dimensional electron gas in these heterostructures.

n - Si	4nm
n - $\text{Si}_{0.86}\text{Ge}_{0.14}$	4nm
i - $\text{Si}_{0.7}\text{Ge}_{0.3}$	4nm
n - $\text{Si}_{0.86}\text{Ge}_{0.14}$	5nm
i - $\text{Si}_{0.7}\text{Ge}_{0.3}$	4nm
i - Si	6nm
i - $\text{Si}_{0.7}\text{Ge}_{0.3}$	60nm
Si/SiGe SL	100nm
p-Si substrate	

Figure 1. Schematic cross-section of a typical layer structure grown for this work (not drawn to scale).

RESULTS AND DISCUSSION

Figure 2 shows a typical temperature dependence of Hall mobilities and sheet densities for one of these Si/SiGe n-type modulation-doped heterostructures with a 4 nm thick undoped SiGe spacer layer. A Hall mobility of $1800 \text{ cm}^2/\text{Vs}$ with a sheet electron concentration of $1.2 \times 10^{12} \text{ cm}^{-2}$ was obtained at room temperature. The high sheet electron concentration was in part due to the top doped layers. However, this high room temperature electron mobility, even higher than that of intrinsic Si, is of great value and requires further study. One of the potential explanations for this observation is that electrons are spilled into intrinsic layers, which are of extremely high quality, analogous to the effect sought when delta doping. The top phosphorous-doped $\text{Si}_{0.86}\text{Ge}_{0.14}$ and Si layers were found to be crucial in this study. If they were doped too heavily, the measured electron mobility of the heterostructure was degraded dramatically at low temperatures due to parallel conduction in these layers. On the other hand, if they were doped too lightly, a surface potential depleted the layers such that the formation of the two-dimensional electron gas (2DEG) was suppressed. As a result this series of experiments, we deduce that the density of surface states is in the range of $1\text{-}2 \times 10^{12} \text{ cm}^{-2}$.

As temperatures decrease, Hall mobilities increase rapidly. Mobilities of 9,000 and 13,000 cm^2/Vs were measured with sheet electron concentrations of 8.5×10^{11} and $8 \times 10^{11} \text{ cm}^{-2}$, respectively, at 77 and 12 K. Continued increase in Hall mobilities at even lower temperatures was observed, and determined by SdH measurements to be as high as 19,000 cm^2/Vs at 1.4 K. This is evidence of the presence of a 2DEG in these heterostructures [11]. The high electron mobilities obtained by us as compared to those by others are probably due to both the low density of threading dislocations and background impurities at the Si/SiGe heterointerfaces. For various samples from different wafers, we obtained mobility values in a range of 7,000-9,000 cm^2/Vs and sheet electron concentrations ranged between 8.1 and $8.5 \times 10^{11} \text{ cm}^{-2}$ at 77 K. For these samples, the mobility-density product at 77 K ranges between $2.16 \times 10^{15} \text{ V}^{-1} \text{ sec}^{-1}$ and $7.5 \times 10^{15} \text{ V}^{-1} \text{ sec}^{-1}$, which is equivalent to a sheet resistance of $\approx 3000 \text{ } \Omega/\square$ and $850 \text{ } \Omega/\square$, respectively. These values are of great interest for the modulation-doped field effect transistor (MODFET) applications.

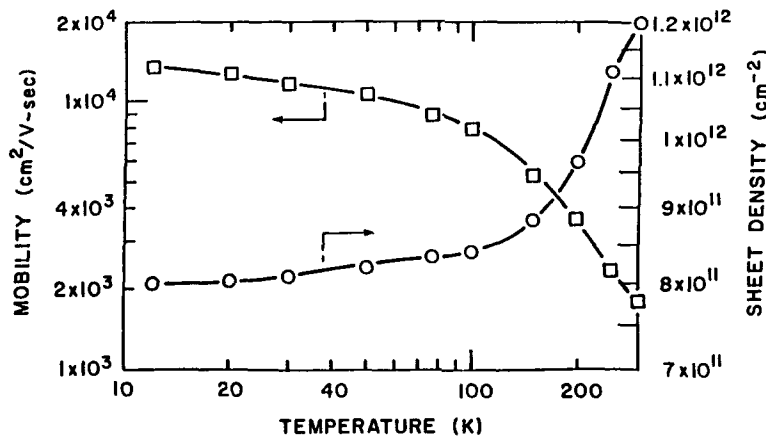


Figure 2. Hall mobility and sheet electron concentration as a function of temperature for a heterostructure with 4 nm thick spacer layer.

Fig. 3 shows a plot of Hall mobility and sheet electron density as a function of SiGe spacer layer thickness at 12 K. It is noted that the mobility increases whereas the sheet electron density decreases with the SiGe spacer layer thickness. This is indicative of the decreased density of remote ionized impurity scattering across the SiGe spacer layer. Even though the electrons, which transfer from the doped SiGe barrier to the undoped Si channel, and their parent ionized impurities are spatially separated by the undoped SiGe spacer layer, the scattering from the remote ionized impurity still dominates the transport properties of 2DEG at low temperatures if the spacer layer is thin. On the other hand, the remote impurity scattering also dominates if spacer layer is too thick, due to the slower Fermi velocity of the carriers and weaker screening effect. We expect to obtain even higher electron mobility if the the spacer layer thickness is optimized.

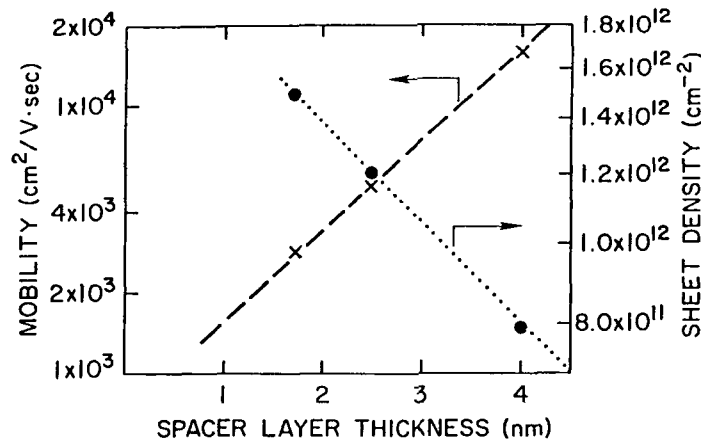


Figure 3. Hall mobility and sheet electron concentration as a function of spacer layer thickness for heterostructures at 12 K.

In order to confirm the existence of 2DEG and to characterize its transport properties at low temperatures, SdH measurements are conducted [12]. Figure 4 shows a plot of longitudinal magnetoresistances (ρ_{xx}) and Hall resistance (ρ_{xy}) as a function of magnetic fields at 1.4 K. Quantum Hall effect, distinct Hall resistance plateau, is clearly evident in curve ρ_{xy} . The longitudinal magnetoresistance oscillation, i.e. the SdH oscillation, at a magnetic field of ≈ 5 T in curve ρ_{xx} and the Hall resistance plateaus at ν , the filling factor, equal to 2 and 6 in curve ρ_{xy} resulted from the spin splitting. If we take $\Delta(1/H)$, where H is the the magnetic field at which magnetoresistance oscillations occur, and substitute in the equation $n_{2D} = (g_s g_v e) / (2\pi\hbar[\Delta(1/H)])$, a 2DEG density of $7.5 \times 10^{11} \text{ cm}^{-2}$ is calculated by assuming that the spin degeneracy $g_s = 2$ and the valley degeneracy $g_v = 2$ for electrons [13]. This 2DEG density value is in close agreement with that obtained from the extrapolation of Hall data shown in Fig. 2. We also found that SdH oscillations were strongly dependent on the angle between the magnetic field and the surface normal of the heterostructure. Therefore, it can be concluded

that the transport properties of these heterostructures are dominated by those of a 2DEG at Si/SiGe interface.

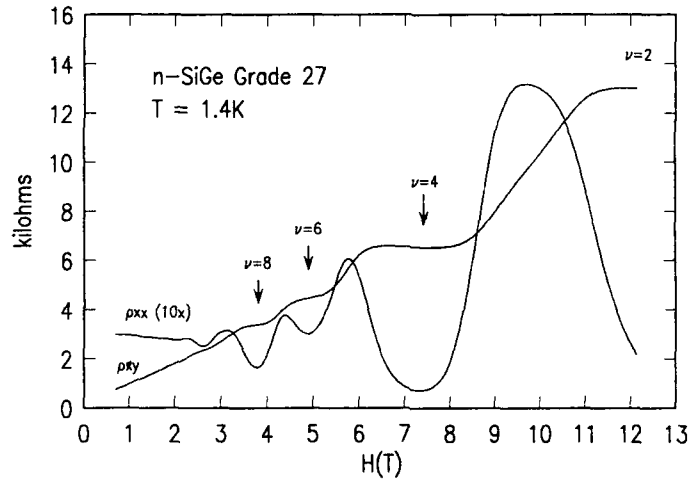


Figure 4. Longitudinal magnetoresistance (ρ_{xx}) and Hall resistance (ρ_{xy}) as a function of the strength of applied magnetic fields at 1.4 K.

CONCLUSIONS

We have shown for the first time record-high electron mobilities in a single junction n-type modulation-doped Si/SiGe heterostructure grown by the UHV/CVD technique. Electron mobilities of 1,800, 9,000 and 19,000 cm^2/Vs with corresponding sheet electron densities of 1.2×10^{12} , 8.3×10^{11} and $7.5 \times 10^{11} \text{ cm}^{-2}$ were obtained from the Hall and SdH measurements at room temperature, 77 K and 1.4 K, respectively. The high sheet conductance obtained for such a single channel heterostructure is of great potential for high speed MODFET applications. Quantum Hall effect and spin splitting were observed for these heterostructures by SdH measurements at 1.4 K. The 2DEG has been found and the transport properties of these heterostructures are dominated by the 2DEG at low temperatures.

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RESONANT TUNNELING OF HOLES IN Si/Si_{1-x}Ge_x QUANTUM WELL STRUCTURES

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EXTENDED ABSTRACT

We investigated resonant tunneling of holes in Si/Si_{1-x}Ge_x double barrier resonant tunneling (DBRT) diodes grown by MBE [1]. The aim of this study was an unambiguous identification of the quantum states involved in the two dominating resonances (Fig. 1), which have been observed by several groups [2],[3],[4]. For this purpose we calculated the transmission probabilities as a function of the well width by means of a transfer matrix method in a one-particle model [5]. The respective effective masses of heavy-holes (hh) and light-holes (lh) in the strained SiGe layers were calculated following Refs. [6] and [7], with appropriate strain corrections added according to Ref. [8]; hh/lh mixing [9] was introduced *a posteriori*. The calculated resonance positions are in reasonable agreement with experiments (Fig. 2), if the resonance at lower energy is attributed to a hh channel in the well, and the second resonance to a lh channel. Since only hh states are occupied in the emitter cladding layer at the temperatures (≈ 1.5 K) studied, hh/lh conversion due to the loss in rotational symmetry is involved in the second resonance.

The identification of the two main resonances hh-hh and hh-lh are consistent with magneto transport experiments performed in magnetic fields B up to 15T. For B parallel to the current j an overall shift of the second resonance is observed, and, moreover, the leading edge of this resonance shows structures in the derivatives due to Landau-quantization (Fig. 3). From the Landau-level splitting an in-plane effective mass of $m_{\parallel}^* = 0.20m_0$ is determined, which is in excellent agreement with the calculated lh effective mass in the strained SiGe well ($m_{\parallel}^* = 0.195$). The shift of the second resonance with B is consistently explained, if non-conservation of the Landau-quantum state during tunneling is assumed, a behavior that has also been observed in AlGaAs/GaAs DBRT structures [10].

A magnetic field perpendicular to j leads to a shift of both resonances proportional to B², albeit with different slope. The slope is proportional to the average in-plane effective mass of the respective carrier during tunneling [11], and is expected to be dominated by the Si-barrier. Indeed, the experimental slope-ratio is in excellent agreement with the ratio of the average lh and hh masses in unstrained Si, again confirming the lh and hh tunneling states involved.

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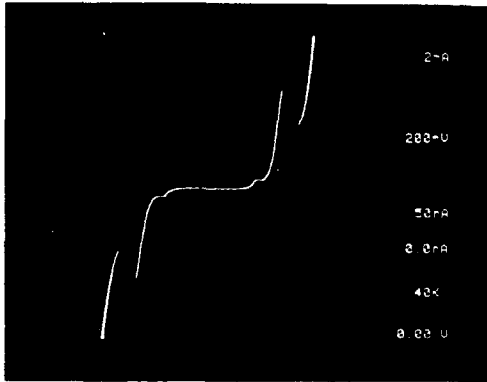


FIGURE 1
 I-V characteristics of a typical Si/SiGe DBRT structure with 30A well width at 77K (upper frame) and at 4.2K (lower frame).

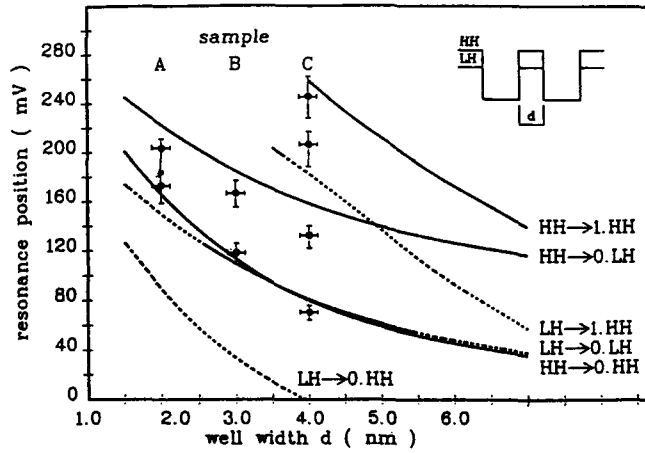
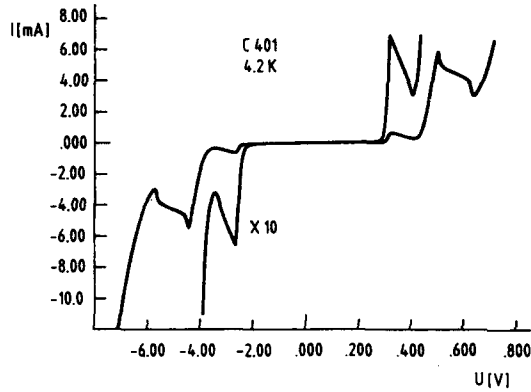


FIGURE 2 Comparison between calculated and experimental resonance positions as a function of the well width. Solid lines represent incoming hh states, dashed lines incoming lh states.

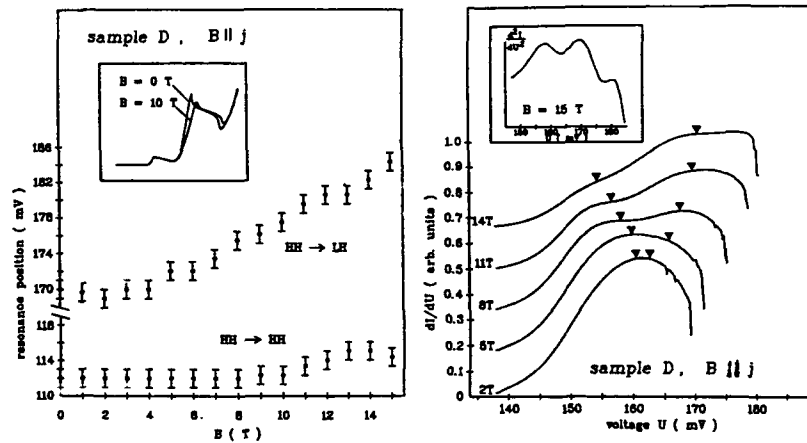


FIGURE 3 Resonance positions vs. applied magnetic field (left) and conductivity vs. applied voltage over the range of the second resonance (right) for the sample in Fig.1. The second derivative is plotted in the insert. Arrows mark Landau-levels.

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**Molecular Beam Epitaxial Growth of Very High Mobility Two-Dimensional
Electron Gases in Si/GeSi Heterostructures**

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ABSTRACT

We report the fabrication of modulation doped Si/Ge_xSi_{1-x} heterostructures by molecular beam epitaxy. The samples are characterized by Rutherford backscattering spectrometry, cross-sectional transmission electron microscopy, electron beam induced current, Hall measurement, and the magnetoresistance (Shubnikov-de Haas) measurements. Threading dislocation densities of $\approx 10^6 \text{ cm}^{-2}$ are observed for relaxed Ge_{0.3}Si_{0.7} films on Si (100). The modulation doped structures fabricated on these Ge_{0.3}Si_{0.7} films contain two-dimensional electron gases with mobilities ranging from 60,000 to 96,000 $\text{cm}^2/\text{V-s}$ at 4.2 K.

INTRODUCTION

The switching speed of a Si metal-oxide-semiconductor field effect transistor (MOSFET) (the fundamental building block of the very large scale integrated logic circuits) is affected significantly by the two-dimensional (2D) carrier mobility in the channel of the field effect transistors.[1] A five-fold increase in the channel mobility is expected to decrease the switching time by about 25%. [2]

Despite these obvious need for higher carrier mobility in Si, the highest reported 2D carrier mobility is still about 41,000 $\text{cm}^2/\text{V-s}$ at 4.2 K, [3] more than two orders of magnitude lower than the highest 2D carrier mobility in a GaAs/AlGaAs modulation-doped structure. [4] The main reason is the lacking of a good quality carrier confining heterojunctions in Si material systems to fully take advantage of the modulation-doping effect. [5]

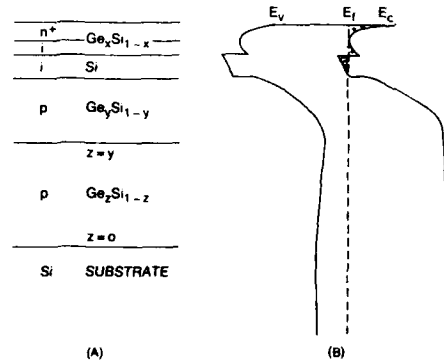
We report an initial success in the direction of achieving such a heterojunction. By fabricating a totally relaxed Ge_xSi_{1-x} buffer layer, [6] two-dimensional electron gases (2DEG) of record high mobilities are obtained in the Si/Ge_xSi_{1-x} heterostructures.

EXPERIMENTAL PROCEDURE

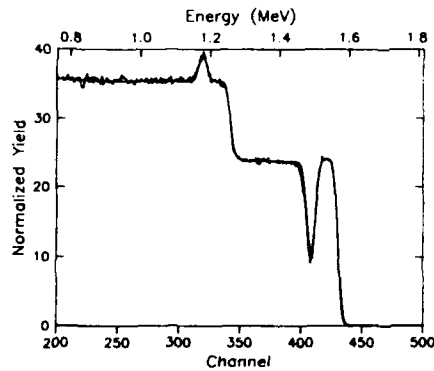
The samples are grown in a Riber Eva-32 MBE system with two electron beam evaporation sources for Ge and Si. Two effusion cells with B and Sb charges are used for p-type and n-type dopings, respectively. The typical layer sequence and the energy band diagram are shown in fig.1a and 1b. The 2DEG is expected to be located inside the biaxially strained Si layer, either at the top Ge_xSi_{1-x}/Si interface, or distributed throughout the entire Si layer (in the case of thin Si layers). Rutherford backscattering spectroscopy (RBS) at grazing angle is used to examine the sample structure, especially to determine the Ge content in the alloy layers. Cross-sectional transmission electron microscopy (XTEM) and the electron beam induced current (EBIC) technique are used to determine the crystalline quality and the threading dislocation density in the films. The temperature dependent mobility and sheet carrier density are measured by the Hall technique. Shubnikov-de Haas (SdH) measurements are used to study the properties of the 2DEGs.

RESULTS

Fig.2 shows a RBS spectrum of one of the samples. The anticipated layer structure (fig.1) is confirmed. The corresponding XTEM micrograph shows the layered structure under high magnification (fig.3). Since all the misfit dislocations due to the lattice mismatch between Si and



1. (a) Schematic diagram of our typical modulation-doped sample; (b) the corresponding energy band diagram.



2. Rutherford backscattering spectroscopy of one of the high mobility samples.

$\text{Ge}_x\text{Si}_{1-x}$ are buried inside the graded $\text{Ge}_x\text{Si}_{1-x}$ layer, [6] the only portion of the dislocation that may contribute to carrier scattering is the threading segments. Not a single threading dislocation is visible in fig.3, which means that the density is lower than 10^9cm^{-2} ! (this is an excellent example illustrating the poor detectivity of XTEM for a low dislocation density structure). In order to obtain a statistically significant counting of the threading dislocation densities, we used the EBIC technique. A plan-view EBIC picture is shown in fig.4, in which threading dislocations are imaged as black dots. We calculated the threading dislocation density, ρ_1 , to be $\approx 4 \times 10^6\text{cm}^{-2}$, a very low value for a totally relaxed $\text{Ge}_{0.3}\text{Si}_{0.7}$ film.

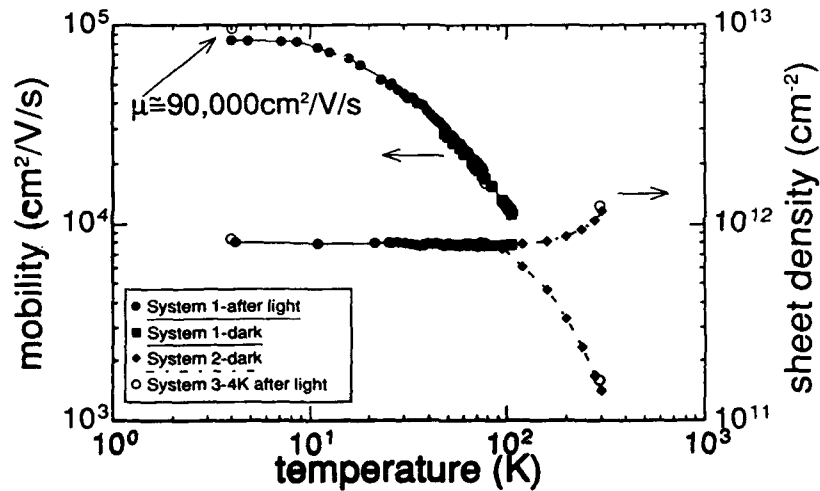


3. Cross-sectional transmission electron micrograph of one of the high mobility samples. The 150 Å thick Si layer shows up as the white band across the picture. There is no dislocation observable in the field of view.



4. Electron beam induced current image of one of the high mobility samples. The black dots in the picture are from threading dislocations.

Fig.5 shows the temperature dependent Hall mobility (μ_H) and sheet carrier density (n_s) data from our highest mobility sample measured by three different Hall apparatus. The $\mu_H = 1600 \text{ cm}^2/\text{V-s}$ at 300 K is comparable to the value from intrinsic Si where the mobility is limited by phonon scatterings.[7] The $\mu_H = 96,000 \text{ cm}^2/\text{V-s}$ at 4.2 K is the highest value ever reported for 2D electron gases in Si (compare to the previous record of $41,000 \text{ cm}^2/\text{V-s}$ at a Si/SiO₂ interface [3]). The product of $\mu_H = 96,000 \text{ cm}^2/\text{V-s}$ and $n_s = 8 \times 10^{11} \text{ cm}^{-2}$ at 4.2 K result in the highest sheet conductance ever achieved in Si material. The 4.2 K μ_H s of our other samples range between 64,000 to 85,000 $\text{cm}^2/\text{V-s}$. The experimental uncertainty in the above measurements is estimated to be $\pm 10\%$.

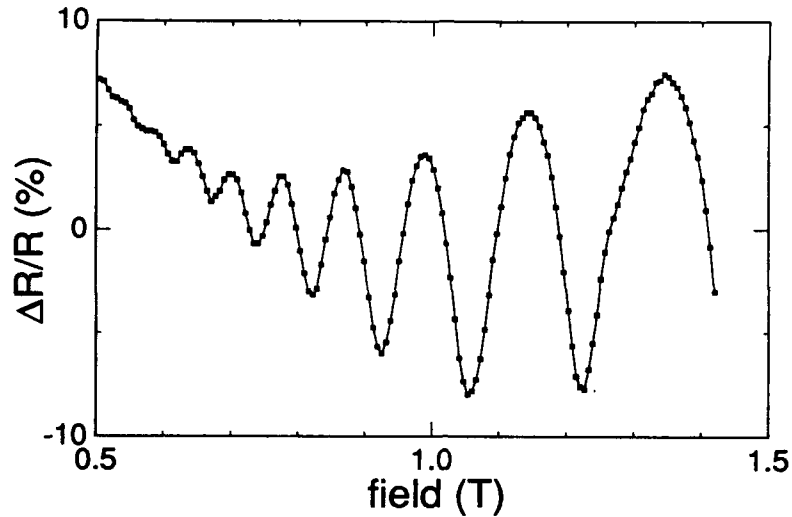


5. Temperature dependent two-dimensional electron gas mobility and sheet electron density measured by the van der Pauw method.

Preliminary SdH measurement result is plotted in fig.6, where the x axis is the magnetic field, B. The sheet carrier density derived from the magnetoresistance oscillation period, $\Delta \frac{1}{B}$, is $n_s^{\text{SdH}} \approx 7 \times 10^{11} \text{ cm}^{-2}$ at low magnetic fields, assuming a valley degeneracy of 2. The cyclotron effective mass of the 2DEG is measured to be $\approx 2m_0$, essentially that of the transverse effective mass of Si ($0.19m_0$) [8]. These results indicate strongly that only two of the six valleys of the Si conduction band are occupied by electrons under the experimental conditions. The lifting of the valley degeneracy is believed to be due to the tensile strain in the Si layer, as first suggested by Abstreiter et al [9]. Further signs of the very high 2DEG mobility can be found in fig.6 by noticing that (1) the oscillation of the magnetoresistance starts at very low magnetic fields (< 0.5 tesla), and (2) the lifting of the spin degeneracy at low magnetic fields (≈ 1.3 tesla).

SUMMARY

The fabrication of $\text{Si}/\text{Ge}_x\text{Si}_{1-x}$ modulation-doped structures on totally relaxed $\text{Ge}_x\text{Si}_{1-x}$ buffer layers is described. The resulting two-dimensional electron gas shows mobilities as high as $1600 \text{ cm}^2/\text{V}\cdot\text{s}$ at 300 K and $96,000 \text{ cm}^2/\text{V}\cdot\text{s}$ at 4.2 K. The experimental results indicate strain induced lifting of the six-fold degeneracy of the Si conduction band. As a result, the effective mass of the two-dimensional electron gas has the value of the transverse effective mass in Si ($0.19m_0$). The successful fabrication of the relaxed $\text{Ge}_x\text{Si}_{1-x}$ buffer layer with low densities of threading dislocations is believed to be the key for achieving such high mobilities.



6. Shubnikov-de Haas measurement result of the $\mu_{H,4.2K} = 96,000 \text{ cm}^2/\text{V-s}$ sample.

ACKNOWLEDGEMENTS

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PART VI

Device Applications

SiGe HETEROJUNCTION BIPOLAR TRANSISTORS

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ABSTRACT

Strained layer growth of SiGe on Si by either Molecular Beam Epitaxy (MBE) or various methods of Chemical Vapor Deposition (CVD), including Limited Reaction Processing (LRP) and Ultra High Vacuum CVD (UHV/CVD) have been used to realize narrow bandgap base double heterojunction bipolar transistors (HBTs). This review paper will focus on the fabrication of high performance transistors, and on the material and process challenges facing the implementation of SiGe HBT technology. In particular, the use of SiGe alloys for bandgap engineering of bipolar devices and the development of self-aligned, epitaxial base bipolar device structures will be discussed, including the most recent accomplishment of 75 GHz f_T heterojunction bipolar transistors, and the record sub-25 ps ECL ring oscillator delay. The design flexibility and trade-offs offered by SiGe heterojunction technology, like junction field/capacitance control, liquid nitrogen operation and complementary processes, are also reviewed, to assess the leverage of a SiGe base bipolar technology in high speed circuits.

I. INTRODUCTION

Advances in epitaxial techniques and the ability to deposit high quality epitaxial silicon-germanium alloys at lower temperatures, together with tight coupling between material science and device understanding, have allowed these alloys to become quickly a high leverage item incorporated in a number of high performance devices. The leverage is provided by the ability to build heterostructures and bandgap-engineered devices, until recently exploited only in compound semiconductor systems, in the silicon system. The good quality material, necessary for manufacturability, has been provided by advances in epitaxial techniques.

The application of SiGe alloys to heterojunction bipolar transistors (HBT's) is discussed in this paper. Over the past few years, a very exciting set of results have been achieved and will be reviewed in this paper. One of the key results has been the near doubling of the performance level of silicon NPN transistors ($f_T = 75$ GHz [1]), as shown in figure 1. This has been achieved in a poly-emitter bipolar process by grading the Ge content across a 45-60 nm base (fig.2), resulting in a smaller and graded base bandgap (fig.3). The effect of a smaller bandgap in the base is to increase minority carrier injection into that region for a given base-emitter bias, resulting in an increase in collector current and current gain. This, in turn, implies less minority-carrier charge storage in the emitter at a given collector current level ($\tau_E \approx 1/\beta$, where β is current gain and τ_E is the emitter transit time [2]). The base transit time (τ_B) is reduced by the drift field created by the bandgap grading. This grading is not required over the entire base region (fig.2), since only the heavily doped region contributes to τ_B , and only a 100 meV bandgap variation across the base can improve significantly (35-40%) the base transit time at room temperature. Figure 4 shows the bandgap reduction expected and measured for various Ge fractions in silicon. From this figure it can be inferred that high performance levels can be achieved at low Ge percentages (< 8%), and that the material challenges include the formation and the maintenance of a defect free SiGe strained layer on silicon (fig.5).

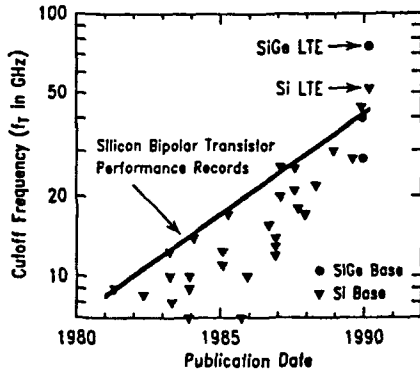


Fig. 1. Performance history of silicon bipolar transistors

In this paper, we will review in section II the various SiGe alloy growth methods and the properties of the deposited films. The application of these alloys to bandgap engineering of advanced bipolar devices is discussed in section III. Section IV will conclude this paper.

II. GROWTH OF SI/SI-GE STRUCTURES

Silicon and germanium are completely miscible over the entire compositional range and give rise to alloys with the diamond crystal structure. As shown in figure 5, due to the lattice mismatch (4.17 percent at room temperature), two types of epitaxial growth are possible on a bulk substrate: pseudomorphic, or strained; and relaxed, or dislocated. Figure 5 illustrates the occurrence of pseudomorphic growth when the strain due to the lattice mismatch is accommodated at or near the interface by tetragonal strain, rather than being relaxed by the formation of misfit dislocations. The interest in pseudomorphic growth is not only due to the lack of interfacial dislocations which could give rise to interface states, band discontinuities, and unwanted electrical effects, but also to the fact that the presence of tetragonal strain in the alloy produces a further reduction

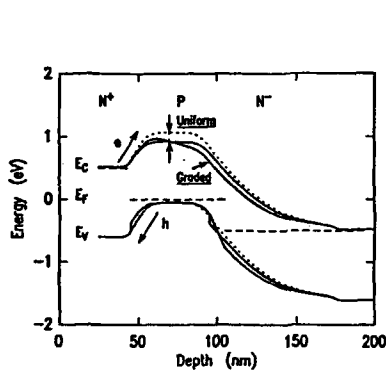


Fig. 3. Band diagrams of SiGe-base heterojunction devices. Grading across the junction avoids the presence of spikes at the interface, while grading across the base introduces an aiding quasi-electric field.

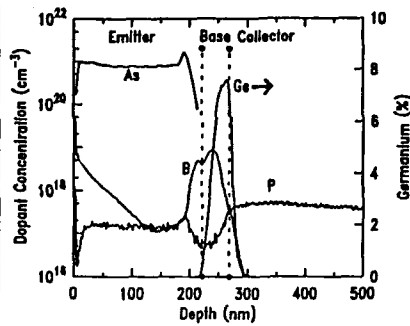


Fig. 2. SIMS profile of a completed SiGe-base device. A base width of 45 nm was achieved [1].

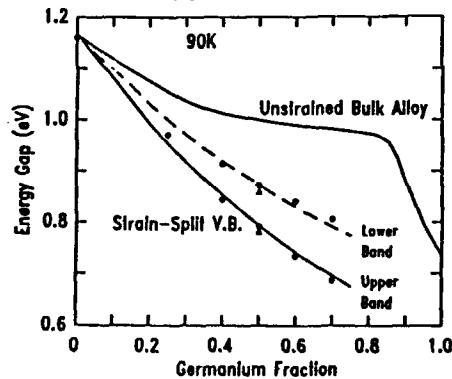


Fig. 4. Band gaps for unstrained bulk $\text{Si}_{1-x}\text{Ge}_x$ alloys [39] and pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ alloys. Both the strain split light and heavy hole bands [40] are shown along with the experimental optical absorption data [41].

in the bandgap, with respect to the bulk alloy layer, due to the splitting of degenerate valence and conduction bands [3], as it was shown in figure 4.

Device quality SiGe layer growth necessitates both a low-temperature growth method to minimize islanding and strain relaxation by dislocation nucleation and an oxygen-free surface passivation method to reduce the oxygen incorporated at the interface causing crystalline defects and degradation of the electrical characteristics. Low temperature epitaxial growth techniques such as molecular beam epitaxy (MBE) [4] and low temperature epitaxy by chemical vapor deposition [5-7] are essential for the growth of metastable alloys and for the preservation of sharp doping profiles. For these epitaxial growth methods to succeed, an atomically clean starting surface is mandatory and furthermore the same level of atomic cleanliness must be preserved during growth. In UHV/CVD, the growth is performed at a much lower temperature than standard epitaxy, 550°C and the preparation of the surface is accomplished chemically, by the creation of a passivating layer of hydrogen bound to silicon. An air stable hydrogen passivated surface [8] is thus obtained, preserving the initial growth interface and allowing the growth to proceed without recontamination by oxides or carbon. It is to this objective [9] that the base pressure of the UHV/CVD system at idle is kept in the range of 10^{-9} Torr, and the partial pressures of the oxidants O_2 and H_2O are maintained below those required to form the stable SiO_2 phase, as it can be quantitatively deduced from [10, 11]. Under typical operating conditions, the partial pressures of oxygen and water are maintained at or below 10^{-10} Torr, and the gases employed for film growth are free of oxygen and water to below the 1 ppm level.

The films grown by this technique have very abrupt transitions in both alloy composition and doping, since UHV/CVD operates under conditions of molecular flow, with very short gas residence times (several milliseconds). The films can be grown in-situ doped, with active supersaturated amounts of dopant with high dynamic range, and do not require subsequent annealing steps to either activate the dopant or to remove the damage, as it is in the case of ion-implanted layers. Because of all of the above, junction

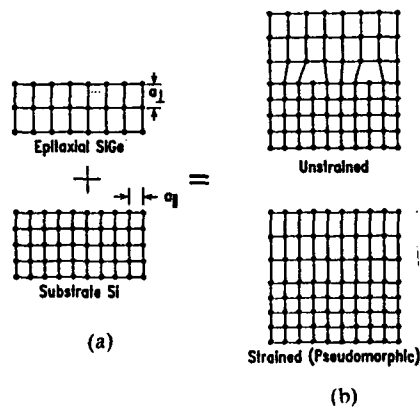


Fig. 5. A two dimensional representation of pseudomorphic growth. An unstrained SiGe film is deposited on a silicon substrate (a). Depending on growth parameters, the growth could be pseudomorphic (b), with the lattice constant difference accommodated by tetragonal strain or it could be dislocated (b).

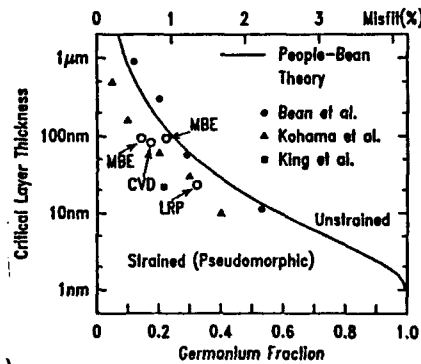


Fig. 6. Critical thickness plotted as a function of Ge content. Shown are the empirical curve of People and Bean [42] and their experimental points obtained from channeling and TEM; EBIC determined points of Kohama et al. [43]; and, points determined from bandgap measurements from HBT's due to King et al. [28]. Also shown are some representative compositions and thicknesses used in HBT fabrication.

depths are determined by the deposition thickness, and not by the difference between two dopant fronts that diffuse during thermal annealing. An example of the overall flexibility of this process is shown in figure 2, which depicts the secondary ion mass spectroscopy (SIMS) profile of a SiGe heterojunction bipolar transistor. The entire profile consists of less than 100 nm of material deposited and, as long as the subsequent processing time-temperature cycles can be kept to a minimum, these as-grown complex junctions can be used to make record performance bipolar transistors as we will show in section III.

Conventional cleaning in MBE involves the growth of a non-stoichiometric chemical oxide and its in-situ desorption at $\approx 850^\circ\text{C}$. More recently [12] it has been demonstrated that HF treatment of Si is effective also in MBE, provided that the epitaxial process is commenced on the hydrogen passivated surface left after the HF treatment. This passivation, indicated by a 1×1 pattern in the low energy electron diffraction (LEED) patterns, is inert for several minutes in air, and several days in UHV at room temperature [13]. The passivation is lost if the wafer is heat treated in UHV above 400°C , resulting in the reconstruction of the surface to an unpassivated 2×1 . To grow on the passivated surface, lower temperature growth, at least during the initial growth stages, is necessary in MBE in order to supply enough Si flux to keep exposing a fresh Si surface while the hydrogen passivation is being lost. As discussed previously, in the case of UHV/CVD growth using hydrides, the passivation is replenished in the course of the dissociative absorption of the hydride, and growth proceeds on an 1×1 terminated surface [12].

The maximum thickness for pseudomorphic growth ("critical thickness") of SiGe alloys is simply defined as the thickness at which strain relaxation occurs due to the onset of dislocations. This quantity is clearly function of the germanium fraction, and it is an important parameter for device designers, since it is necessary to prevent strain relaxation and dislocation generation to occur. The critical thickness as defined either by theory or by experiments is summarized in figure 6 [14] for $\text{Si}_{1-x}\text{Ge}_x$ grown on Si (100) as a function of x . Also shown in fig. 6 are points of composition and thickness at which SiGe-base heterojunction bipolar transistors have been fabricated. In the case of pseudomorphic III-V layers, it is generally accepted that relaxation is sudden and almost complete once the critical thickness is exceeded. However, in the case of covalent alloy semiconductors such as Si-Ge, the onset of relaxation is gradual, and film thicknesses much greater than the critical thickness may be required before significant relaxation occurs, as suggested by Fiory et al. [15]. Also, as complex Ge profiles are grown, like triangular or trapezoidal, with the Ge percentage varying during the growth, the onset of relaxation will become dependent on the growth sequence.

After the material is grown, subsequent processing will be necessary to complete the device formation. The maintenance of a high quality strained layer is considered best from the standpoint of mechanical stability as defined by Matthews and Blakeslee [16]. A layer may be considered stable if there is no driving force for dislocation glide, and metastable if the strain is sufficient to induce misfit dislocation formation in the presence of a pre-existing extended defect. For an arbitrary profile of Ge in Si (i.e. box, trapezoid, triangular), a stability limit may be defined as a function of the peak Ge fraction [17]. Fig. 7 shows the results of such a calculation with and without a 25 nm Si capping layer. The figure suggests that for a 60 nm metallurgical basewidth, a triangular profile is mechanically stable up to a peak concentration of 12% Ge. If the layers are metastable, several restrictions are placed on the way this material may be processed. During thermal annealing, the layers may relax. The mode of relaxation may be either via intermixing or via additional misfit dislocation formation. Work by LeGoues et al. [18] shows that the initial condition of the interface plays a crucial role in determining which relaxation mechanism will dominate.

From a device perspective, a single threading dislocation through the active area of the device will have little electrical effect. However, the threading component can act as a diffusion "pipe" leading to enhanced impurity diffusion and consequent junction leakage. Clearly, limiting processing temperatures will minimize this effect. On the other hand, the edge component of the dislocation that lies in the depletion region is potentially a source of high density of recombination centers which would contribute to junction leakage, particularly when decorated with metallic impurities.

If SiGe technology has to be introduced in an advanced bipolar manufacturing process, the situation is further complicated by the presence of isolation (oxide regions) and topography on the wafer on which one has to grow the epitaxy. The requirement for the epitaxial layer defect density is less than 10 cm^{-2} , for a layer thickness on the order of 100 nm, a Ge content in the 0-20% range, and an arbitrary Ge and doping profile. If the strain relaxation is via dislocation formation, the electrical effects may be felt long before the relaxation is determined by structural methods, and we have routinely used the measurement of the reverse leakage across appropriate p-n heterojunctions, the ideality of the forward injection, and measurement of band discontinuities to assess the quality of the interface. One of the complications is that the electrical activity of the dislocations is not well understood, and it is very dependent on the interaction with impurities (from the process itself or from subsequent processing). Therefore, while we cannot quantitatively correlate the electrical measurements to relaxation, they serve as a very sensitive measure of the heterojunction quality. These electrical measurements indicate that excellent junctions can be obtained. Our experience suggests that proper substrate preparation, the use of buffer layers, and particulate contamination during growth all play a key role in dislocation formation, and may be more important than the energy and mechanical equilibrium theories would suggest, at least for the growth of low ($\leq 20\%$) Ge content films on Si (100) substrates. In figure 8, the forward and reverse base-emitter characteristics of SiGe-base devices grown by UHV/CVD are shown. As it can be observed, consistent with the TEM observations of material quality, excellent electrical characteristics were obtained for two types of poly-emitter anneals: (1) furnace anneals of 850-900°C and (2) a furnace anneal of 850°C followed by a rapid thermal anneal (RTA) at 950-1050°C. The base-emitter junction is positioned, in all cases, within the epitaxial grown layer. Forward characteristics for the

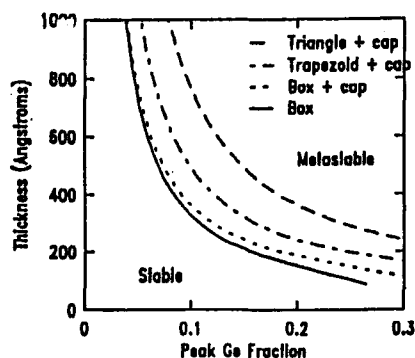


Fig. 7. Critical thickness versus peak Ge content for various geometric Ge profiles relevant to fabrication of SiGe HBTs. The critical thickness refers to the total distance over which Ge is present in the structure (i.e. the expected basewidth) [17].

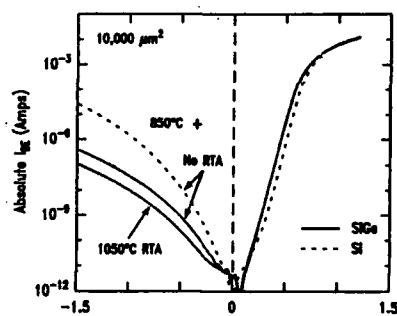


Fig. 8. Base-emitter junction characteristics of SiGe-base devices given a furnace anneal at 850°C and, in one case, a subsequent rapid thermal anneal (RTA) at 1000°C. In both cases, the base-emitter space charge region lies completely within the LTE layer [1].

base-emitter junctions show ideality factors near unity into the picoampere range for devices as large as $10,000 \mu\text{m}^2$. Reverse leakage levels were the same for both the Si and SiGe-base transistors. This leakage was "tunneling"-related, as confirmed by temperature measurements and by the dependence of this leakage on the peak base doping level.

III. SI/SI-GE HETEROJUNCTION TRANSISTORS

By depositing in-situ doped layers at temperatures below 700°C with high level of control, UHV/CVD has the unique capability to form very shallow active layers of silicon and silicon-germanium. This has to be contrasted with the conventional method of ion implanting silicon and determining the junction depth by the difference between two doping profiles, and eliminates the need of high temperature heat treatments to activate dopants and eliminate the damage generated during implantation. As a result, very sharp and narrow doped regions can be obtained.

The major application of SiGe alloys in integrated processes has been in the bipolar transistors area. As mentioned earlier, pseudomorphic SiGe layers provide a bandgap reduction in the base which is dependent on the Ge content and the strain in the layer. Careful design of the bandgap profile is crucial in optimizing the device performance. When abrupt heterojunctions are used, conduction band spikes can form at the interfaces. At the base-emitter junction, such a spike can reduce the bandgap improvement, introduce a potential source of non-uniformity, and provide a sink for space charge recombination. At the edge of the base-collector junction, a conduction band spike can act as a barrier to minority-carrier transport across the base, resulting in increased charge storage and neutral base recombination [19]. These problems can be avoided [20-22] and a possible improvement in the stability of the SiGe film [23] can be achieved by grading the bandgap across the space charge regions as shown in figure 3.

The effect of a smaller bandgap in the base is to increase minority carrier injection into that region for a given base-emitter bias, resulting in an increase in collector current and current gain. This, in turn, implies less minority-carrier charge storage in the emitter at a given collector current level ($\tau_E \approx 1/\beta$, where β is current gain and τ_E is the emitter transit time [2]). As proposed and analyzed by Kroemer [24], the base transit time in a heterojunction bipolar transistor (HBT) can be shortened by providing a quasi-field across the base, i.e., grading the bandgap (Ge concentration) across the base, as also shown in figure 3.

The total collector current increase depends exponentially on the bandgap reduction integrated over the heavily-doped portion of the neutral base (W_b^*):

$$\frac{I_c(\text{Si})}{I_c(\text{SiGe})} \propto \frac{R_{bi}(\text{Si})}{R_{bi}(\text{SiGe})} \times \int_0^{W_b^*} e^{-\Delta E_g(x)/kT} dx \quad (1)$$

where R_{bi} is the pinched base resistance. When the germanium is linearly graded across the base, and for grading $\gg kT$, this can be written as [24,25]:

$$\begin{aligned} \frac{\tau_E(\text{SiGe})}{\tau_E(\text{Si})} &= \frac{\beta(\text{Si})}{\beta(\text{SiGe})} = \frac{I_c(\text{Si})}{I_c(\text{SiGe})} \\ &\approx \frac{R_{bi}(\text{Si})}{R_{bi}(\text{SiGe})} e^{-\Delta E_{g(\text{BE})}/kT} \frac{kT}{\Delta E_{g(\text{BC} - \text{BE})}} \end{aligned} \quad (2)$$

and the base transit time, τ_B , is

$$\frac{\tau_B(\text{SiGe})}{\tau_B(\text{Si})} \approx \frac{2kT}{\Delta E_{g(\text{BC} - \text{BE})}} \left[1 - \frac{kT}{\Delta E_{g(\text{BC} - \text{BE})}} \right] \quad (3)$$

where $\Delta E_g(BE)$ is the germanium-induced bandgap reduction at the base-emitter depletion edge and $\Delta E_g(BC - BE)$ is the bandgap grading across the heavily-doped portion of the neutral base profile.

As it can be observed, the decrease in τ_E (due to the increase in current gain β) depends exponentially on the bandgap reduction at the edge of the base-emitter junction, and is inversely proportional to the variation in bandgap across the base. The decrease in τ_B depends solely upon the field induced by the variation in bandgap across the base. As mentioned earlier, only a 100 meV variation in bandgap across the base can improve the base transit time by 38% at room temperature due to a drift field of approximately 20 kV/cm in the base. Therefore, the leverage of a SiGe-base transistor lies not exclusively in a higher current gain, but rather in the ability to reduce the pinched base resistance and emitter and base transit times. If the emitter delay is small, as it is in the case of polysilicon emitter devices, the gain improvement can be traded for lower base resistance and thus better circuit performance at high current. Fig. 9 shows the simulated delay components and cut-off frequency showing the reduction of the base transit time and emitter charge storage time with a SiGe base.

The SiGe base HBT has become a prototypical device in Si-based heterostructure bandgap engineering and has been the subject of sustained focus in several laboratories worldwide. These include, other than our laboratories, AT&T, NEC, Daimler Benz, Philips, and British Telecom Laboratories, as well as Stanford, Princeton, and Carnegie Mellon Universities. Solid and Gas source MBE as well as CVD techniques have been employed. Much of this work has been presented in the last International Si MBE conference [26]. Early work in this field has been summarized in reference [14] and will not be repeated here.

Sturm et al. [27] have used rapid thermal CVD to fabricate graded SiGe HBTs, with maximum Ge concentrations of 20% and Ge grading of up to 20% across the base, to achieve a built-in drift field. One important distinction from earlier work in similar systems [28], besides the grading, is the reduced oxygen concentration in the SiGe layer, they achieved through the use of a load lock. This resulted in lower base currents and the collector current enhancements they report are in close agreement with those predicted by Equations 1 and 2. More recently, the effect of oxygen on the minority-carrier lifetime and recombination currents have been studied in detail by the Stanford group

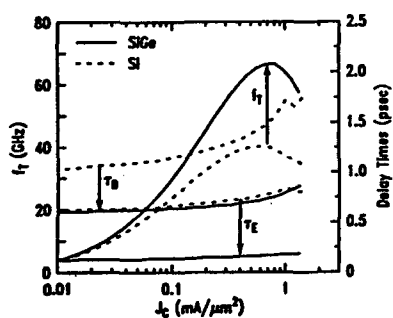


Fig. 9. Simulation of delay components for Si (dashed line) and SiGe-base (solid lines) devices showing reduction in both τ_E and τ_B due to the graded Ge profile. Also shown are the time constants for the emitter base (τ_{EB}) and base-collector (τ_{BC}) depletion regions [34].

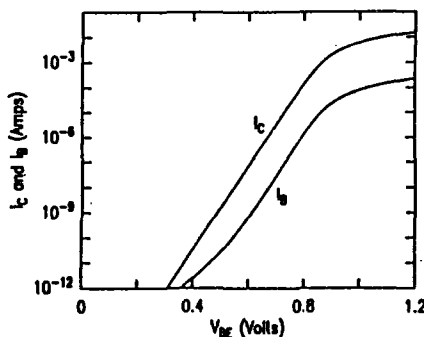


Fig. 10. Gummel plot of the SiGe-base transistor. The intrinsic base sheet resistance is $17 \text{ k}\Omega/\square$ and the on-wafer emitter area is $0.9 \times 4.5 \mu\text{m}^2$ [1].

[29]. Hirayama et al [30] used Selective Gas Source MBE to selectively grow the base and emitter layers. The emitter deposit step did include a relatively high temperature cleaning step. They report however, that the use of high phosphorous doping in the emitter may have led to degraded junction ideality ($n = 1.25$). This structure is a self aligned structure and if optimized has potential for reduction of device parasitics.

An example of the final intrinsic transistor profile that we have been building in our labs is shown in fig. 2. The polysilicon/silicon interface is indicated by the peak in the arsenic profile, while the base-emitter junction is marked by the dip in the boron profile (caused by the electric field coupling between arsenic and boron during diffusion [31, 32]). The base-collector junction occurs where the measured boron and phosphorus concentrations intersect. As reported in [1], we have built, using UHV/CVD, and measured the performance of transistors with the profiles shown in fig. 2, obtaining an emitter junction depth and a base width of 30 and 45 nm, respectively. We also have applied such profiles to a self-aligned bipolar process [33] obtaining record performance for silicon bipolar transistors. Fig. 10 shows the typical Gummel characteristics of the SiGe-base transistors. As can be seen in this figure, the junction characteristics are nearly ideal and the devices have a peak current gain in excess of 100. The frequency response of these transistors was measured obtaining a peak cut-off frequency (f_T) of more than 70 GHz, and higher f_T than the corresponding Si-base devices over a wide range of output current levels, as shown in fig. 11. Figure 12 shows the power delay curve of ECL ring oscillators fabricated with SiGe in the base. A record minimum delay of 24.6 ps was achieved with $0.4 \times 4.3 \mu\text{m}^2$ emitters.

The optimization of such scaled bipolar transistors requires increased doping in the base and in the collector that lead to high capacitances and high electric fields which result in performance degradation, junction leakage and low breakdown voltages. In HBT's these problems can be minimized by introducing a lightly doped emitter (LDE) [33, 34] and a lightly doped collector [35]. These low doped regions help reduce electric fields, and are deposited using low temperature epitaxy, as shown schematically in fig. 13. LDE reduces the tunneling current and reverse leakage current of the E-B junction, while also lowering the E-B capacitance, giving a higher cutoff frequency over a wide range of current densities, as shown in fig. 14. This effect is due to the quasi electric field introduced by the graded SiGe profile in the HBT that overcomes the retarding field present in the homojunctions due to the retrograde boron profile at the E-B junction, and results in a net gain in the cutoff frequency, E-B leakage and breakdown voltage. LDC reduces the impact ionization with minimal penalty on B-C transit time and therefore on f_T since carriers travel at saturation or even faster velocity.

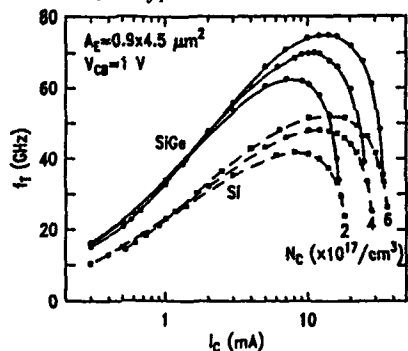


Fig. 11. Dependence of f_T on collector current for $V_{CB} = 1$ V: a peak f_T value of 75 GHz was obtained at 12.2 mA [1].

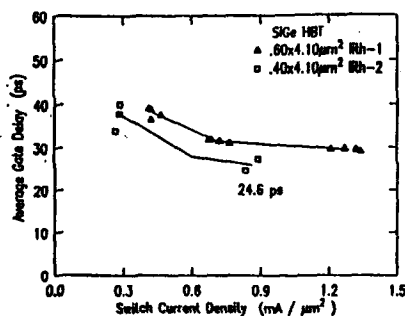


Fig. 12. Measured average gate delay of self-aligned SiGe ECL circuits. The minimum delay of 24.6 ps is obtained with the tighter lithography [33].

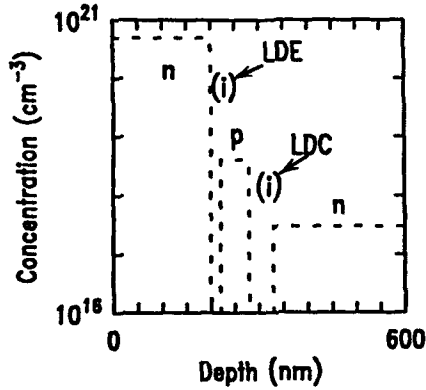


Fig. 13. Schematic NPN doping concentration profile showing the lightly doped emitter (LDE) and the lightly doped collector (LDC).

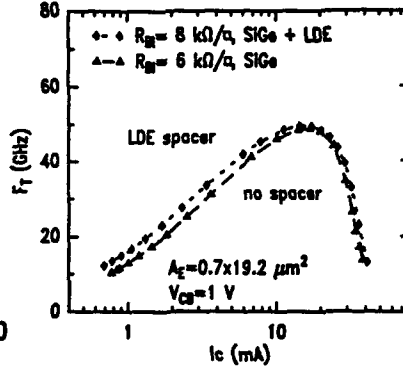


Fig. 14. Measured cutoff frequency improvement using LDE [33].

These devices also offer great potential for bipolar circuit operation at liquid nitrogen [36, 37]. The thin, abrupt base profile attainable with LTE is less susceptible to base freeze-out and the resultant high base resistance. The LDE reduces the tunneling leakage at the emitter-base junction, thus increasing the collector current operating range by more than 2 orders of magnitude at low bias. The LDC alleviates the problem of high impact ionization rate at high temperature. An improvement of 25% in f_T is observed by cooling the devices from room temperature to 85K, as shown in fig. 15 [37]. A record ECL ring oscillator delay of 28 ps at 85K is obtained for the self-aligned devices [36].

We have also applied all the above concepts to the fabrication of high performance vertical PNP HBTs. In the PNP case, both the n-type dopant needed in the base, and the valence band barrier effect, shown in fig. 16 [38], have proven to be quite challenging. As discussed before, the bandgap is graded in the base-collector space charge region to avoid energy spikes and wells, and this can be observed in the NPN energy band in

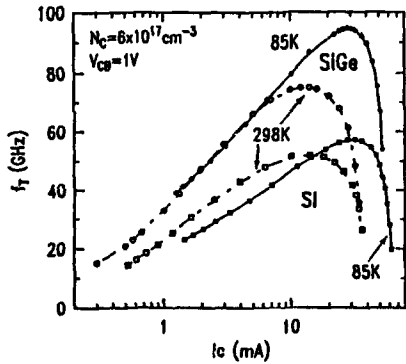


Fig. 15. Collector current dependence of f_T at 298K and at 85K for Si and SiGe devices [37].

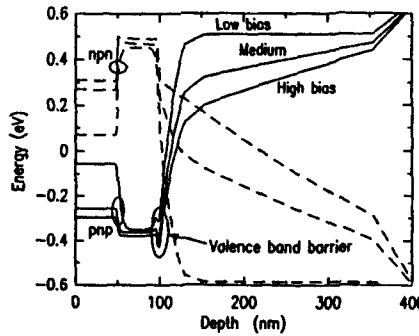


Fig. 16. Energy band simulation of NpN and PnP SiGe-base HBTs showing valence band barrier in PnP. No barrier is observed in the NpN transistor [38].

fig. 16. In the case of SiGe PNP devices, the band offset that occurs in the valence band does create a barrier at the base-collector junction, causing carriers to pile-up in the base. Recent 2-D modeling and experiments, show that this can be overcome by burying the heterojunction deeper in the collector to avoid excess hole storage in the base [38].

The importance of PNP transistors with comparable performance to NPN is for high performance and low power complementary circuits.

IV. CONCLUSIONS

Excellent quality strained SiGe alloys have been used to leverage band structure modifications and heterostructure engineering in silicon technology. Abrupt doping transitions and ultrathin, heavily doped layers have contributed to obtain record performance in heterojunction bipolar transistors (HBTs) in a process that can be easily integrated in conventional bipolar technology. The performance of these transistors is even increased at liquid nitrogen temperature, making them serious contenders for advanced microwave applications. The advances in performance of the complementary PNP transistor will continue to stimulate material research and novel device designs. The remaining challenges include the integration of these devices in advanced circuits, their manufacturability and long-term reliability.

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MODULATION DOPED Si/SiGe HETEROSTRUCTURES

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ABSTRACT

An overview of SiGe-based, modulation doped heterostructures is given. Strained layer handling, a prerequisite for realizing both n- and p-type devices, is treated in terms of band engineering. The main emphasis is put on recent results obtained with high-electron mobility n-type Si/SiGe structures. Hall, Shubnikov-deHaas, and cyclotron resonance measurements are presented. The thermal stability of the heterostructures and the dopant distribution are treated with respect to device applications. Room temperature and 77K dc-measurements on very recent modulation doped field effect transistor (MODFET) implementations using implanted source/drain contacts are discussed. Device concepts with n- and p-type MODFETs combined in a superior complementary layout (CMODFET) are proposed.

1. INTRODUCTION

The spatial separation of dopant atoms and two-dimensional (2D) free carriers in a heterosystem can lead to a significant enhancement of the carrier mobilities due to reduced Coulomb scattering at ionized dopant atoms. High performance field effect transistors based on this principle of modulation doping (MODFET) are commercially fabricated of III-V compound semiconductors. In the strained Si/SiGe heterosystem modulation doping experiments led to the discovery of a strain induced type II band ordering [1], [2] which can be exploited for both n- and p-type MOD devices. Recent progress in growth techniques and strain handling resulted in Si/SiGe MODFET implementations that demonstrate the inherent potential for superior future devices. These will combine the closely matched performance characteristics of n- and p-MODFETs to a fast complementary device that will overcome the limits of such devices in other material systems, which are all characterized by the poor performance of the p-type element. The following discussion will be restricted to (100) oriented material, the only surface compatible with very large scale integration (VLSI) techniques.

2. BAND ALIGNMENT AND STRAIN EFFECTS

The lattice constant of $\text{Si}_{1-x}\text{Ge}_x$ is to good approximation (Vegard's law) a linear function of the Ge content x , and reaches a maximum mismatch of 4.17% between pure Si and Ge. Up to a critical thickness t_c , which can be extended to some extent by choosing non-equilibrium growth conditions, lattice mismatch is accommodated by tetragonal distortion of the lattice, whereas strain relaxation by nucleation of misfit dislocations commences beyond t_c [3]. The band ordering at a Si/Si $_{1-x}$ Ge $_x$ interface depends strongly on the built-in strain distribution caused by this lattice distortion. Besides a strain dependence of the overall band gap, the sixfold and threefold (in unstrained Si) degenerate conduction and valence bands, split into two and three components, respectively [1], [4]. This does not affect the principal nature of the valence band offset, which is under all conditions in favour of the narrow bandgap material SiGe. However, the conduction band offset in (001) oriented material can reach from flatband (or even slightly type I) to a pronounced type II ordering, i.e. the larger band gap material Si provides the conduction band minimum of the heterosystem. The latter situation requires the Si layers to experience an in-plane tensile strain, which pulls down the two degenerate

conduction band valleys in the (001) growth direction, whereas the fourfold degenerate in-plane valleys are shifted upward [5]. Electrons are under such conditions confined to the Si layers where they occupy the two valleys with the light electron mass $m_e^* = 0.19m_0$ parallel to the layers. The strain induced conduction band ordering is plotted schematically in Fig.1 for a symmetric strain distribution, i.e., the same amounts of tensile and compressive strain are present in the Si and SiGe layers, respectively. Note that the twofold degenerate valleys move twice as far in energy compared to the fourfold degenerate valleys, which leaves the weighted average of the conduction band position basically unaffected.

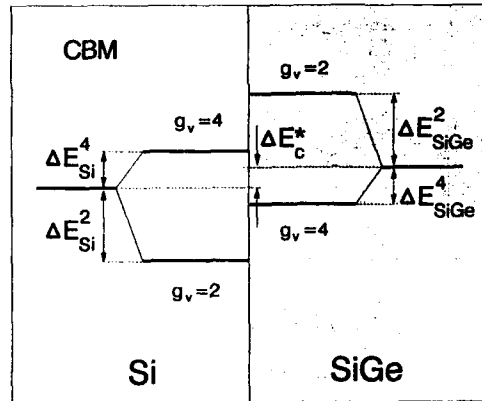


FIGURE 1 Strain splitting and conduction band alignment at a strain symmetrized Si/Si_{0.5}Ge_{0.5} heterointerface (Ref.5)

The strain dependent band alignment offers an additional degree of freedom in tailoring the properties of the system, but also implies limitations due to critical thicknesses. While p-type quantum well (QW) structures can, in principle, be grown pseudomorphically on Si substrates, a starting layer with a larger lattice constant is necessary for n-type devices to achieve the appropriate strain conditions in the Si layers. The latter is realized by first growing a relaxed SiGe buffer on the Si substrate [3].

3. MATERIAL PROPERTIES

3.1. p-type Si/SiGe heterostructures

The first modulation doped Si/SiGe quantum well structures (MODQW) were pseudomorphically grown by molecular beam epitaxy (MBE) on Si(100) substrates. According to the aforementioned strain dependence of the band alignment only hole confinement (in the SiGe-layers) is possible under these conditions. For a Si_{0.5}Ge_{0.5} quantum well clad between Si layers, which were doped p⁺ throughout except in a narrow, undoped spacer layer adjacent to the well, People et al. [6] found a 2D hole gas with maximum Hall mobilities in excess of 3000cm²/Vs at 4.2K (square symbols in Fig.2). Typical 2DHG carrier concentrations were in the middle 10¹¹ cm⁻² range. Some improvements, especially at lower temperatures, have more recently been reported for similar structures (Ge content of 15%, comparable 2DHG concentrations) grown by UHV-CVD [7] (cross symbols in Fig.2). Both samples showed partial carrier freeze-

out due to a parallel channel in the highly doped Si layers, which is expected to lead to an underestimation of the 2DHG Hall mobility at higher temperatures. Nevertheless, the observed room temperature (RT) mobilities, which differ only slightly in the two samples, correspond to about $5 \cdot 10^{16} \text{ cm}^{-2}$ p-doped Si bulk material. Obviously, the desired mobility enhancement by modulation doping could not be achieved by pseudomorphic Si/Si_{0.5}Ge_{0.5} heterostructures, at least not at device relevant temperatures. A reason for this behavior is the additional alloy scattering in the SiGe layer which impedes the mobility enhancement due to reduced Coulomb scattering.

A very attractive alternative to SiGe alloys is the use of pure Ge channels. This not only rules out alloy scattering but also introduces the material with the highest hole mobility of all device relevant semiconductors. The inherent problem of Ge channels is the extremely small critical thickness of only a few atomic layers for Ge on Si. This requires relaxed SiGe buffers to reach acceptable channel thicknesses of several 10 Angströms. First such experiments were reported by Ostrom et al. [8], who grew Si_{0.5}Ge_{0.5}/Ge MODQW structures on relaxed Si_{0.3}Ge_{0.7} buffer layers. Their results are quite promising (diamond symbols in Fig.2), with a RT mobility of $520 \text{ cm}^2/\text{Vs}$ at a sheet carrier density of about 10^{12} cm^{-2} . This corresponds to the hole mobility of a $5 \cdot 10^{17} \text{ cm}^{-3}$ bulk Ge sample and exceeds a Si bulk sample of the same doping concentration by a factor of two. At lower temperatures a mobility saturation and finally a crossover with the aforementioned Si/Si_{0.5}Ge_{0.5} samples is observed. This is indicative of material problems in the Ostrom samples, which certainly require improvements in growth and doping techniques. An attempt to overcome such problems has recently been published by Murakami et al. [9], which also made use of relaxed SiGe buffer layers, but used Ge(100) substrates for their samples. Their best value for the hole mobility was reported as $4200 \text{ cm}^2/\text{Vs}$ at 77K and at a carrier concentration of $5 \cdot 10^{11} \text{ cm}^{-2}$ (triangle symbol in Fig.2). This is a very promising value for future device applications, However, Si substrates will be required for compatibility reasons. Hence, efforts to achieve such results on Si substrates are urgently demanded.

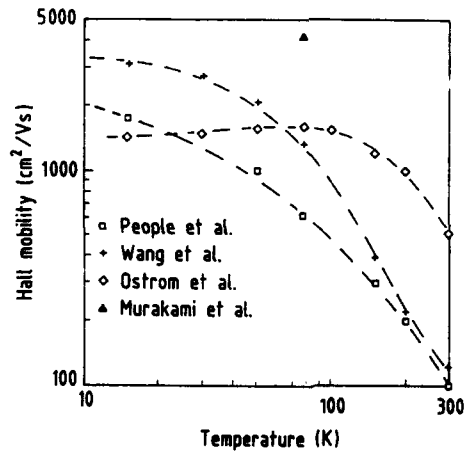


FIGURE 2 Hole mobilities in modulation doped heterostructures with SiGe and Ge channels. (Data from Refs. [6-9])

3.2. n-type Si/SiGe heterostructures

The first n-type MODQW structures, which led to the discovery of the strain dependent type II band ordering, were based on the principle that a Si/SiGe strained layer superlattice can be grown to infinite thickness if the strain in the layers is symmetrized [10]. For this purpose a starting surface is required that offers the in-plane lattice constant corresponding to the average Ge content of the superlattice. Under these conditions, the Si layers experience an in-plane tensile strain whose amount equals that of the compressive strain in the SiGe layers, leading to the desired conduction band ordering discussed above (Fig.1). For a first realization of this concept, Jorke et al. [1] grew a 10 period Si/Si_{0.5}Ge_{0.5} superlattice on a SiGe buffer relaxed to the in-plane lattice constant of an unstrained Si_{0.75}Ge_{0.25} crystal. With high n-doping concentrations in the center of the SiGe layers and undoped spacers left next to the Si wells, they found a significant mobility enhancement as compared to bulk Si of the same average doping concentration.

Meanwhile, refinements in buffer layer design and growth conditions led to further mobility improvements. The best results so far achieved by MBE growth are depicted in Fig.3 for a 5 period Si/Si_{0.5}Ge_{0.5} superlattice grown on a relaxed Si_{0.75}Ge_{0.25} buffer layer [11]. The Si wells are 75Å, the Si_{0.5}Ge_{0.5} layers 250Å thick of which 100Å on either side were left undoped, whereas the center 50Å were Sb doped to a level of $5 \cdot 10^{18} \text{ cm}^{-3}$. An electron concentration of $1 \cdot 10^{12} \text{ cm}^{-2}$ per channel and no indications for carrier freeze-out upon cooling was observed in Hall experiments. When measured in the dark, the Hall mobility of this sample reached 1500 cm²/Vs at room temperature and more than 13000 cm²/Vs at 1.5K. Under permanent illumination the 2D carrier concentration is increased by 40% concomitant with a mobility increase to almost 16000 cm²/Vs at 1.5K [12].

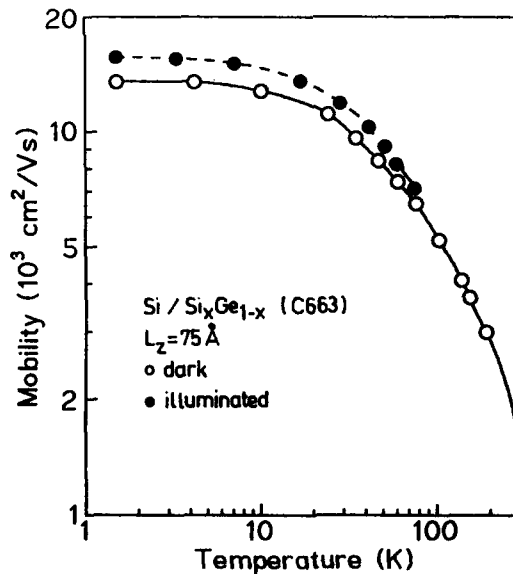


FIGURE 3 Temperature dependent Hall mobilities of a modulation doped Si/SiGe multiple quantum well sample with and without illumination (Ref. 12)

The status reached with these improved n-type MODQW structures compares at all temperatures favourable with standard MOSFETs, and is already comparable to GaAs/AlGaAs MODFETs with the same well, spacer and carrier density parameters, provided the difference in effective transport mass is taken into account [13].

For further characterization of the 2DEG properties cyclotron resonance and Shubnikov-deHaas (SdH) experiments were performed at the Walter-Schottky-Institute (Munich) [12]. Fig.4 shows infrared absorption data of the same sample as in Fig.3 in magnetic fields B of 6 and 14T applied perpendicular to the layers. From the position of the well resolved transmission minimum the Landau-level splitting $\hbar\omega_c = eB/m_s^*$, and thus the effective electron mass m_s^* in direction parallel to the layers can be deduced. We find a value of $m_s^* = 0.20m_0$, which is slightly higher than the bulk transport mass $m_t^* = 0.19m_0$, but is in excellent agreement with former measurements on inversion layers of Si MOSFETs [14], which also have only the twofold degenerate electron valleys populated at low temperatures. A fit to the resonance width allows to derive a scattering lifetime of $\tau = 1 \cdot 10^{-12}$ s which is comparable to the τ extracted from the measured Hall mobilities.

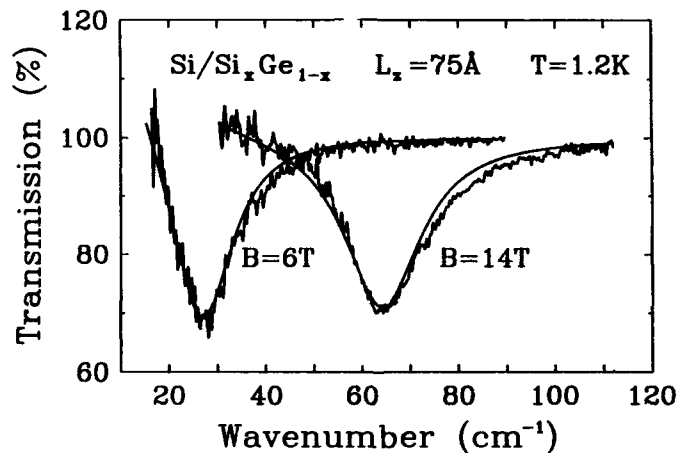


FIGURE 4 Cyclotron resonance measurements at 6 and 14T. The same sample as in Fig.3 is shown. (Ref. 12)

Fig.5 shows the magnetoresistance components ρ_{xx} and ρ_{xy} versus magnetic field B for a single quantum well sample with otherwise similar parameters as the one depicted in Figs.3 and 4. From the SdH-oscillations in ρ_{xx} a 2DEG density of $9.5 \cdot 10^{11} \text{ cm}^{-2}$ (without illumination) can be derived that is in excellent agreement with Hall measurements on the same sample. This means that the dominating amount of carriers are really confined to the Si well, because a parallel channel in the doping region would contribute to the averaging Hall measurement, but not to the SdH result. The second curve in the ρ_{xx} frame, which was also measured in the dark, demonstrates the persistent increase in carrier density and mobility upon short illumination. These high mobility Si/SiGe samples allowed for the first time in this material system the observation of the quantum-Hall effect [12]. This is demonstrated in the ρ_{xy} frame in Fig.5: Under the improved conditions reached after brief illumination, Hall plateaus corresponding to filling factors of $\nu = 4, 8, 12$ (dashed lines) are readily seen. Under permanent illumination an additional shoulder appears at $\nu = 6$ due to spin splitting at such high magnetic fields.

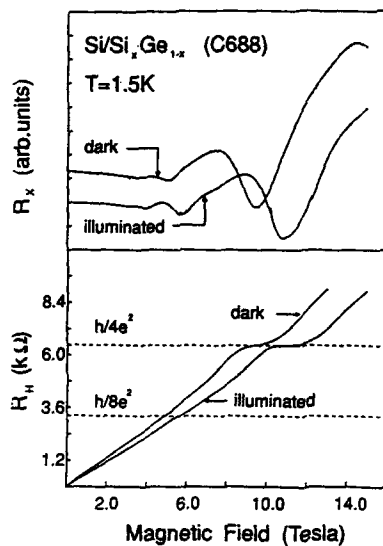


FIGURE 5 Magnetoconductance measurements on a single quantum well sample in ρ_{xx} and ρ_{xy} geometry with and without illumination (Ref.12)

4. DEVICE APPLICATIONS

4.1 p-type MODFET

The first p-channel MODFET devices [16] were based on the mentioned investigations of pseudomorphic Si/SiGe p-MODQW structures. The active layers consist of a 250Å thick Si_{0.3}Ge_{0.7} channel and a Si cap layer, which is p⁺ doped only in a narrow range between the Schottky gate and the channel leaving undoped spacers on either side (Fig.6). Standard VLSI processing techniques

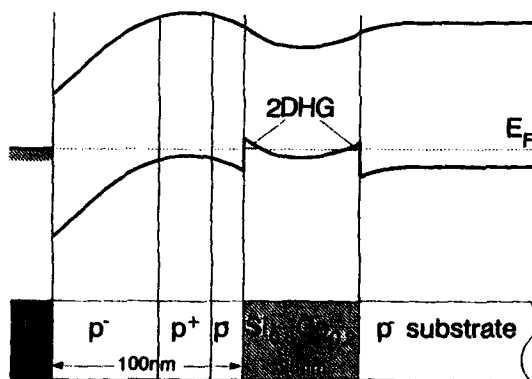


FIGURE 6 Bandedge variation and layer sequence of the first p-MODFETs. (Schematic view using the parameters given in Ref. 15)

were employed for device definition, which included BF_3 implantation for the source and drain contacts. Annealing of the implanted structures was restricted to temperatures below 700°C to keep defect formation and interdiffusion in the SiGe layers low. Both depletion and enhancement devices were fabricated, the latter by thinning the region underneath the gate by reactive ion etching prior to gate deposition.

Besides incomplete pinch-off behavior, which was attributed to faulty surface passivation, these devices showed very well behaved characteristics. Maximum transconductance values g_m in excess of 3mS/mm for depletion- as well as for enhancement-type devices were measured for gate length around $2\mu\text{m}$. These values, although quite comparable to standard p-MOSFETs, suffer from the relatively high parasitic lead resistances, which are caused by the low RT hole mobilities and the relatively low carrier concentrations of only about $2.5 \cdot 10^{11}\text{ cm}^{-2}$ in these particular structures. The new results of Murakami et al. [9] with Ge-channel structures let expected significant improvements due to the much higher hole mobilities and the easier realization of higher sheet carrier concentrations.

4.2 n-type MODFET

The first n-channel MODFETs were reported by Dämbkes et al. [16], which used strain symmetrized single channel structures similar to the mentioned multiple MODQW structures of Jorke et al. [1]. Using standard lithography and simple contact alloying techniques, very well-behaved transistors with extrinsic transconductance values of up to 50mS/mm were fabricated.

Based on the new high-mobility MODQW structures König et al. [17] processed devices, which were designed to overcome some of the earlier shortcomings. Special emphasis was put on a reduction of the parasitic lead resistances by using contact implantation and higher sheet carrier densities. To study the influence of thermal annealing, which is unavoidable in connection with contact implantation, a systematic series of annealing experiments on the same sample as in Fig.3 was performed [11]. The results are shown in Fig.7, where the temperature dependent Hall mobilities are plotted for various annealing temperatures at constant annealing times of 1000s. At all annealing

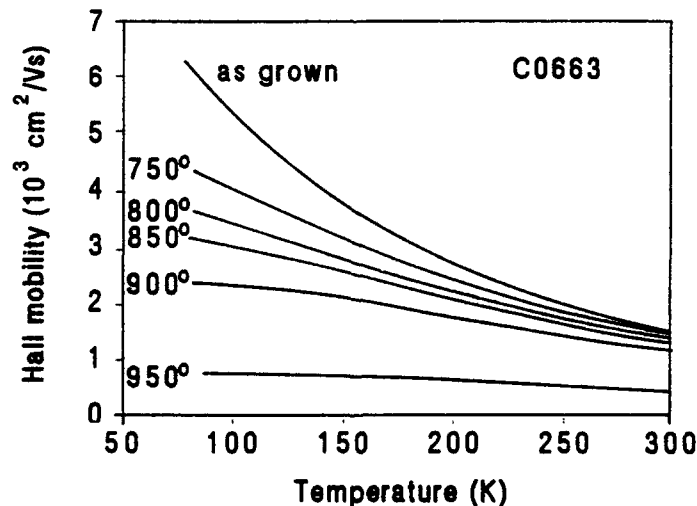


FIGURE 7 Mobility degradation due to various thermal annealing treatments

temperatures studied a reduced Hall mobility was found, but this effect is, as expected, much more pronounced at lower measurement temperatures, where Coulomb scattering begins to dominate. At RT, which is most relevant for device applications, a quite moderate effect on the mobility is observed up to annealing temperatures of 900°C. Beyond that temperature the drastic reduction and virtual temperature independence of μ_{Hall} , as well as a carrier freeze-out behavior [11] indicate a complete breakdown of the modulation doped structures. The mobility reduction upon annealing, which could be identified to be mainly due to dopant (Sb) diffusion into the undoped SiGe spacer layers [18], suggests a moderate heat load to be applied during implantation annealing.

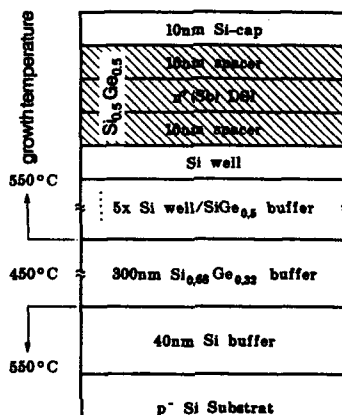


FIGURE 8 Layer sequence of the n-channel MODFETs studied

The new device structures were grown on relaxed Si_{1-x}Ge_x buffer layers on p- (>1000Ωcm) Si(100) substrates. An additional Si/Si_{1-x}Ge_x superlattice buffer was grown for some of the structures (Fig.8). The active region consists of a 75 to 100Å wide Si well followed by a 300Å thick Si_{1-x}Ge_x layer, the center 100Å of which were Sb doped to a level of $6 \cdot 10^{18} \text{ cm}^{-3}$, and finally a 100Å thick Si cap layer. The purpose of the latter is protection of the SiGe layers against oxidation and reproducible formation of a Schottky gate contact with a Pt/Ti/Au gate metallization. Phosphorus was implanted at 20 to 40keV and doses up to 10^{16} cm^{-2} into the source/drain contact windows and subsequently annealed at 800°C for 5s in a rapid thermal annealer. Reference Hall measurements revealed that under these annealing conditions RT Hall mobilities as high as $1200 \text{ cm}^2/\text{Vs}$ could be maintained.

The devices show very good saturation behavior and complete pinch-off at gate voltages of -1.4V at RT (Fig.9). Under regular operation conditions (gate reverse biased) maximum transconductance values of $g_m=80$ and 132 mS/mm at RT and 77K, respectively, were measured on devices with a gate length of 1.5μm and a gate width of 40μm. These significant improvements can be attributed to the reduced parasitic resistivities in the source/drain region, which were demonstrated by direct comparison with simultaneously processed transistors utilizing standard contact alloying procedures [17].

Under forward bias conditions, which are usually characterized by a decrease in g_m , a second, much more pronounced transconductance maximum occurs at around +0.7V. This is due to the Si cap layer which can in principle act as a second channel, but is completely depleted under regular operation conditions.

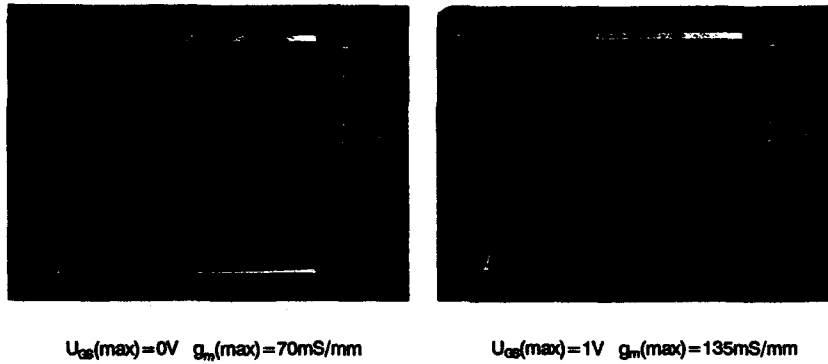


FIGURE 9 I-V characteristics of a n-MODFET under regular conditions (left) and with forward biased gate (right)

At forward gate bias, however, this parallel channel is pulled down below the Fermi level, and can therefore contribute very efficiently to the source/drain current (Fig.10). The large transconductance values reached this way (Fig.11), with maxima of 165 and 490mS/mm at RT and 77K, respectively, are due to its location right underneath the gate.

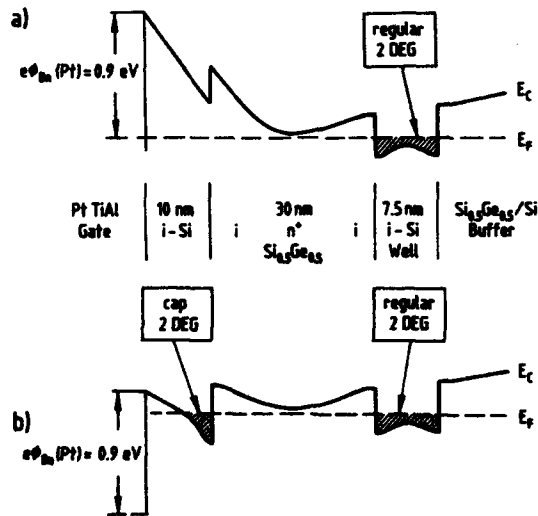


FIGURE 10 Conduction band variation across the studied n-MODFETs at zero gate voltage and under forward bias condition (Ref.17)

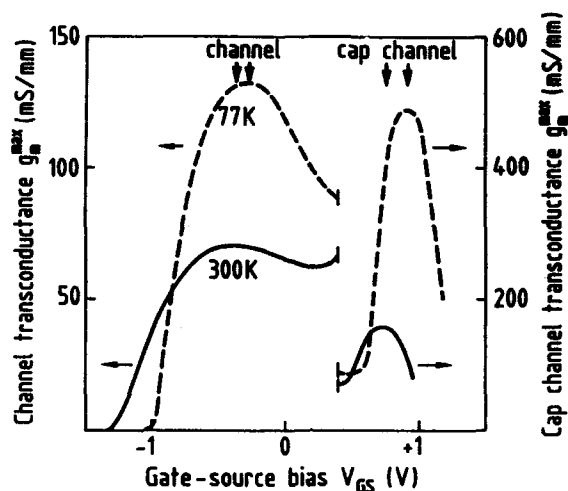


FIGURE 11 Extrinsic transconductance vs. gate voltage at room temperature and at 77K. Note the different scale in forward bias direction. (Ref.17)

Although gate leakage currents prevent the cap-channel to be exploited in a simple device application, its appearance in the output characteristics demonstrates the potential for further improvements: In order to achieve higher transconductance values the channel has to come closer to the gate electrode. This will certainly reduce the thickness of the undoped spacer layers and thus decrease the carrier mobility. However, part of this loss, which mainly affects the parasitic lead resistivity outside the gate-controlled region, can be compensated by an increase in 2D carrier concentration made possible by a narrower spacer layer. Hence, an adequate compromise has to be found in a future optimization procedure.

5. OUTLOOK

Si/SiGe modulation doping structures have reached a status that allows to speculate about future larger scale applications. A unique property of the SiGe material is the unchallenged hole mobility brought in by the Ge component. Hence the most likely application is that of a complementary (CMODFET) device, which uses n- and p-components of almost identical performance characteristics. For this purpose p-MODFETs with Ge or Ge-rich channels are required, which have already demonstrated their inherent device potential. Certainly single p-MODFET devices will have to be fabricated and optimized before considering CMODFET implementations. The n-MODFET, on the other hand, has reached a somewhat more advanced status, however further optimization and HF-characteristics are also necessary for this transistor type. Both types will require relaxed buffer layers, and it has to be clarified, whether critical thickness considerations allow for the design of a common SiGe buffer for both devices. If this is not the case, two relaxed buffers have to be grown, which add to the complexity of the design.

A possible design could consist of a common-gate, common-drain

implementation realized in two planes, which are successively grown in one epitaxial run. The straightforward pile up of the two device types allows to adapt either a single buffer or a two-buffer design. The planes will be separated by selective mesa-etching, which can make use of SiGe etch-stop layers incorporated into the layer sequence. The common gates and drains allow a quite compact arrangement which promises reasonable integration density. Such high performance devices can, in principle, be integrated with standard Si-VLSI circuits [19] to combine ultimate performance with high complexity on a single chip.

ACKNOWLEDGEMENTS

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REDUCTION OF p^+-n^+ JUNCTION TUNNELING CURRENT FOR
BASE CURRENT IMPROVEMENT IN Si/SiGe/Si
HETEROJUNCTION BIPOLAR TRANSISTORS

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ABSTRACT

A reduction of parasitic tunneling current by three orders of magnitude in epitaxial p^+-n^+ junctions grown by Rapid Thermal Chemical Vapor Deposition (RTCVD) compared to previously published ion implantation results is reported. These results are very important for the reduction of base current in scaled homojunction and Si/SiGe/Si heterojunction bipolar transistors. High reduction in tunneling currents allows higher limits to transistor base and emitter dopings. Significant tunneling was observed when the doping levels at the lighter doped side of the junction were of the order of $1 \times 10^{19} \text{cm}^{-3}$ for both Si/Si and SiGe/Si devices. These results were confirmed by I-V measurements performed at different temperatures. Since the tunneling current is mediated by midgap states at the junction, these results demonstrate the high quality of the epitaxial interface.

INTRODUCTION

Heavily doped layers are desired for optimum performance of homojunction (BJT's) and heterojunction bipolar transistors (HBT's). Increased base doping is required to avoid punchthrough when scaling these devices and is also desired for low base resistances and high Early voltages. High emitter dopings are desired for increased emitter efficiencies and low series resistances. However, it has been shown that the forward current of heavily doped silicon junctions at low bias levels is dominated by a parasitic tunneling current [1-5]. This is not band-to-band tunneling, but rather the tunneling of both electrons and holes to midgap states at the $p-n$ interface where they recombine. A schematic diagram of ideal and tunneling currents at a heavily doped p^+-n^+ junction is shown in Fig.1. An increase in the doping of the lighter doped side of the base-emitter junction reduces the width of the space charge region increasing the tunneling probability. After a certain

doping level ($>10^{18} \text{ cm}^{-3}$ according to [1]) is exceeded, the tunneling barrier becomes very narrow and causes non-negligible tunneling to midgap states. Since the hole and electron currents to midgap states must be equal, the current is limited by the side of the junction with lighter doping where the tunneling barrier is wider. Therefore the tunneling current is expected to increase with the doping on the lighter doped side. This tunneling current becomes a significant component of the transistor base current, especially at low forward biases.

In this paper, a significant reduction of tunneling current is reported in epitaxial p^+n^+ junctions grown by RTCVD compared to the previously reported ion implantation results [1]. The implications of these results for HBT performance are also shown. Since it is desirable for Si/SiGe/Si HBT's to contain high base dopings (e.g. 10^{19} cm^{-3} [6] or more) the tunneling base current component becomes especially important. This is illustrated in Fig.2 where it is shown how the tunneling current is predicted to limit the current gain in a Si/Si_{0.85}Ge_{0.15}/Si HBT with a base doping of $N_B=5 \times 10^{19} \text{ cm}^{-3}$ as the emitter doping is increased. In the absence of tunneling, the gain would follow the ideal curve shown in the figure. (At higher emitter doping levels, the ideal curve bends due to the silicon bandgap narrowing.) With tunneling, the gain curves are predicted to drop rapidly after a certain doping level is reached since tunneling causes a significant increase in the base current.

EXPERIMENTAL RESULTS AND DISCUSSION

Epitaxial p^+n^+ (i.e. like a base-emitter) Si/Si and Si_{0.85}Ge_{0.15}/Si diodes were fabricated by RTCVD. Thick silicon (phosphorous doped) n^+ layers (3-13 μm) were grown on n -type substrates. The growth temperature varied from 850°C to 1000°C for different samples. The dopings ranged from $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$. After the relatively high temperature step, the growth was stopped for 30 seconds and the temperature was lowered. P-type (boron doped) layers were then grown at low temperature to prevent outdiffusion and provide an abrupt junction. On some of the samples, a thin p^+ (30nm) Si_{0.85}Ge_{0.15} strained epitaxial layer was grown at 625°C (doped $5 \times 10^{19} \text{ cm}^{-3}$). This provided a $n^+ \text{-Si/p}^+ \text{-SiGe}$ junction. Thin epitaxial p^+ silicon layers (50nm), doped $5 \times 10^{19} \text{ cm}^{-3}$, were then grown at 700°C on all of the samples. The dopings were confirmed by spreading resistance and C-V measurements. The junctions were isolated by a simple mesa process.

Room temperature forward bias I-V curves are shown in Fig.3. The tunneling effect is clearly evident in the heavily doped devices at low

Fig.1. Schematic band diagram of ideal and tunneling currents at heavily doped p⁺-n⁺ junction

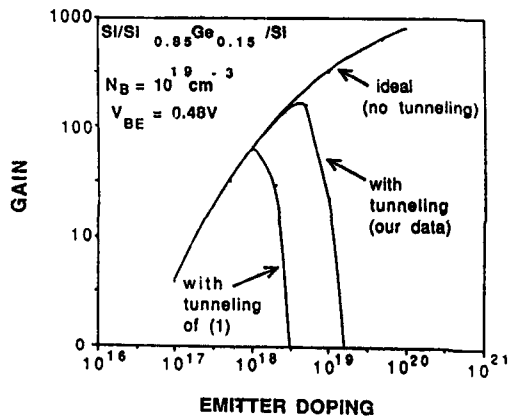
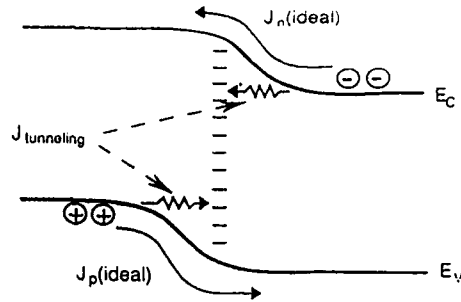


Fig.2. Calculated effects of the tunneling current on the gain of Si/Si_{0.85}Ge_{0.15}/Si HBT's as the emitter doping is increased. Both curves based on the data of [1] and our data are given for comparison, as well as the ideal curve (no tunneling).

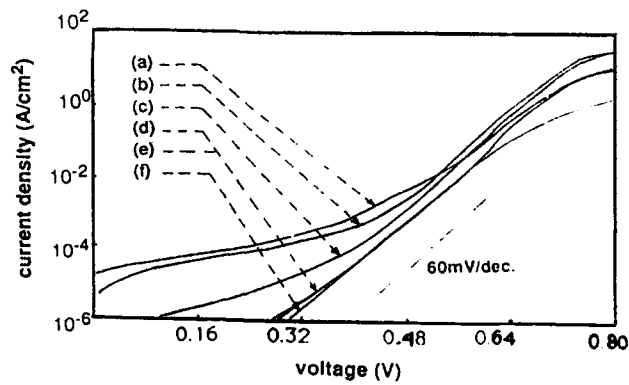


Fig.3 Room temperature forward bias I-V curves of several devices with the following n-type dopings: (a) $1 \times 10^{19} \text{ cm}^{-3}$ (Si/SiGe), (b) $9 \times 10^{18} \text{ cm}^{-3}$ (Si/Si), (c) $7 \times 10^{18} \text{ cm}^{-3}$ (Si/Si), (d) $3 \times 10^{18} \text{ cm}^{-3}$ (Si/Si), (e) $1.5 \times 10^{18} \text{ cm}^{-3}$ (Si/Si and Si/SiGe), (f) $1.3 \times 10^{17} \text{ cm}^{-3}$ (Si/Si)

bias levels as the large "n>2" current. The current increases with the doping on the lighter doped side, as expected. This is not the typical space charge recombination current ($1 < n < 2$), which would increase at low doping levels with larger space-charge regions. I-V curves among the devices with the same area and doping were similar, and measurements on several different area devices ($1.4 \times 10^{-2} \text{cm}^2$ - $9.5 \times 10^{-5} \text{cm}^2$) confirmed that the peripheral current components were negligible. Significant tunneling was observed at doping levels of the order of $1 \times 10^{19} \text{cm}^{-3}$ for both Si/Si and SiGe/Si devices.

Further evidence that these large currents at low biases are indeed tunneling is provided by temperature-dependent I-V measurements (175K - 350K). Since the injected currents are vastly reduced at lower temperatures and the tunneling currents are fairly insensitive to temperature, the effect of tunneling is even more significant at low temperatures. The observed concave shape of the current vs. temperature curve of heavily doped devices is consistent with the expected shape of excess tunneling current curves [4,5].

Calculations of band diagrams showed a slightly lower tunneling barrier (of the order of 100meV) for electrons in the $\text{Si}_{0.85}\text{Ge}_{0.15}/\text{Si}$ devices compared to the Si/Si devices for the same n-doping densities (Fig.4). This predicts slightly higher currents (~3 times) of SiGe/Si junctions. However, due to the resolution of the measurement, no significant difference in the behavior of Si/Si and SiGe/Si devices at the same doping levels was observed.

In Fig.5a, the current density at the forward bias of 0.32V is plotted as a function of doping. Also plotted are calculated values of the ideal diode current, which is dominated by electron injection into the p⁺-Si layer. The ideal current should be the same in all devices since the total electron barrier is the same for both Si/Si and SiGe/Si devices. Previous results for tunneling limits in ion implanted p⁺-n⁺ junctions [1] are also shown for comparison to the tunneling current lines fitting our data. At low doping levels, or high biases, ideal current dominates over tunneling. At lower bias levels tunneling causes an increase of several orders of magnitude in the current of heavily doped devices. A similar plot at V=0.48V is shown in Fig.5b. Also plotted are some typical base current densities extracted from Gummel plots of several published HBT and BJT results [7-12]. These reported base currents, of course, consist of several components besides tunneling, but tunneling is a fundamental lower limit to this number. It is interesting to note that except for devices also fabricated by another CVD epitaxial base technology (UHV CVD) [9], all base currents lie substantially above our results and even above the ion implantation results [1].

Fig.4 Band diagram of a forwardly biased junction ($V=0.48V$):
 a) $p^+-Si_{0.85}Ge_{0.15}/n^+-Si$ (solid)
 b) p^+-Si/n^+-Si (dashed)
 $N_A = 5 \times 10^{19} cm^{-3}$
 $N_D = 10^{19} cm^{-3}$

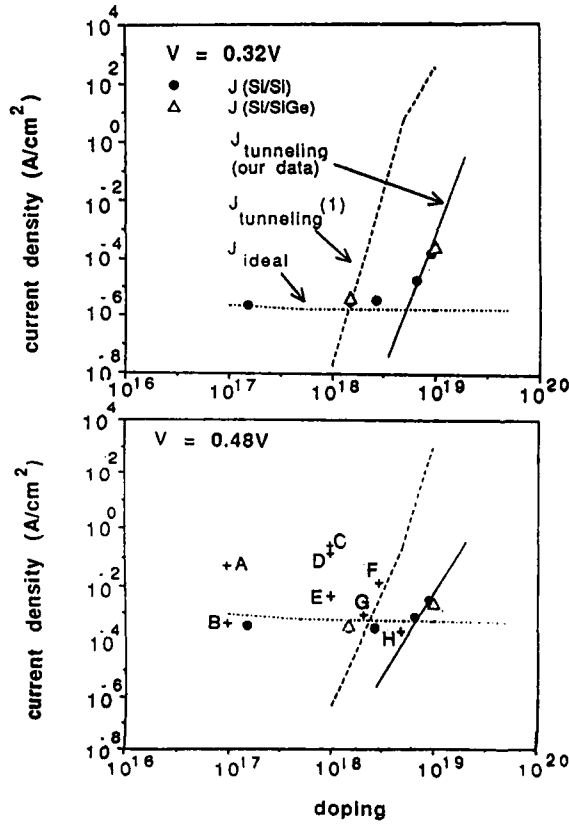
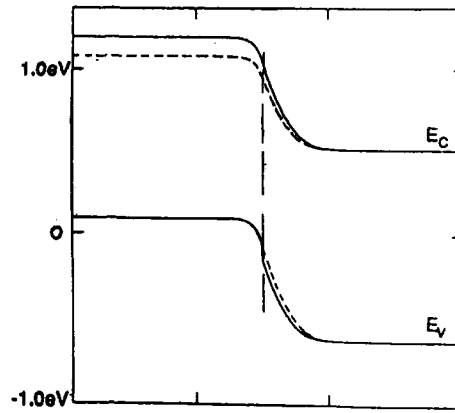


Fig.5 Current density vs. n-type doping for:
 (a) $V=0.32V$;
 (b) $V=0.48V$.
 Also shown are the following data points:
 A) SiGe HBT grown by LRP [11]
 B) SiGe HBT grown by RTCVD (in our lab)
 C) SiGe HBT grown by MBE [8]
 D) SiGe HBT grown by MBE [7]
 E) Si BJT grown by MBE [7]
 F) SiGe HBT grown by UHV/CVD [10]
 G) Si BJT [12]
 H) SiGe HBT grown by UHV/CVD [9]

SUMMARY

For identical n-type doping levels, the tunneling currents in our devices are approximately three orders of magnitude lower than those of the ion implanted devices previously reported [1]. The reduction in parasitic tunneling current that we observed predicts that higher emitter dopings can be used, as well as predicts an increase in the peak transistor gain (Fig.2). The low tunneling current allows high gain to be maintained to higher base doping levels, enabling reduced base resistances and increased Early voltages. Since the tunneling current is mediated by midgap states at the junction, the vast reduction in tunneling currents of the devices fabricated by RTCVD implies a commensurate reduction of density of defects at the interface.

ACKNOWLEDGMENTS

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SILICON GERMANIUM HETEROBIPOLAR TRANSISTOR STRUCTURES WITH EXTREMELY HIGH BASE DOPING

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ABSTRACT

The complete layer sequence of a SiGe-HBT including the emitter contact is grown by Si-MBE. The base doping level was increased from $10^{18}/\text{cm}^3$ up to $10^{20}/\text{cm}^3$ which resulted in very low intrinsic base sheet resistivities ($0.27 \text{ k}\Omega/\square$ for a 50 nm base). With a base Ge content $x = 32\%$ the highest current gain $\beta=5000$ could be obtained. A SiGe spacer between base and collector improved the DC-characteristics considerably.

INTRODUCTION

The proposal of a heterojunction bipolar transistor (HBT) was made by Shockley in 1948 [1]. Several years later, Krömer formulated the current gain relations of the HBT by a diffusion model [2]. The basic idea was the use of a wide-gap emitter in the emitter/base junction to provide a higher emitter efficiency - that is, a higher current gain in an HBT than in a homojunction bipolar transistor with the same doping levels. Wide band gap emitter HBT's were realized in the group III/V material system (for a review, see [3]). A corresponding principle - the use of a narrow band gap base in a double heterostructure bipolar transistor (DHBT) - can be realized in the material system SiGe/Si. Probably, our group was one of the first proposing a SiGe-DHBT in 1977 [4]. The SiGe-base (Fig. 1) is nearly ideal because the band offset is almost completely in the valence band as needed for perfect DHBT operation. At that time Si-MBE

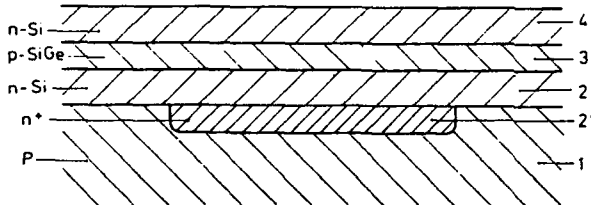


Fig. 1:
Layer sequence of the
SiGe-DHBT. From Ref.
[4], Fig. 12. Collec-
tor 2/SiGe base 3/
emitter 4/. Grown on
an n⁺-buried layer 21
in an p⁻-substrate 1.

development did not reach the level required to handle metastability and doping of HBT's. At the second Si-MBE symposium 1987 first experimental results about SiGe-HBT's were given [5]. From then on one of the most rapid device developments ever seen in modern microelectronics evolved, resulting in an exciting push of transit frequency f_T up to 75 GHz at room temperature [6], or 94 GHz at $T = 77 \text{ K}$ [7], respectively.

MAIN ADVANTAGE: FREEDOM FOR DEVICE DESIGNERS

The basic effect of the emitter/base heterojunction is given by the sub-

stantial increase of the current gain β compared to that of a homojunction transistor of the same layer widths and doping levels. Neglecting parasitic effects this increase in gain is proportional to $\exp(\Delta V_b/V_{th})$ where ΔV_b is the band offset which is determined by the Ge content x of the base (V_{th} is 25 mV at room temperature).

Table I: Increase in gain $\beta(\text{HBT})/\beta(\text{BT})$ caused by the heterojunction barrier at the emitter/base transition (Ge content x of the base).

Ge content $x(\%)$	18	20	22	24	26	28	30
Gain increase $\beta(\text{HBT})/\beta(\text{BT})$	155	300	580	1115	2150	4150	8000

As shown by table I the current gain increases several hundred times around a base Ge content of 20 % and several thousand times around a base Ge content of 30 %, respectively. This gain increase was already demonstrated impressively by extremely high current gains from transistors doped to about the same level in base and emitter, respectively [8]. We have obtained (in cooperation with Ruhr-University, Bochum [8]) the highest current gains of 5000 with a transistor (B 1835) with a 30 nm SiGe base (Ge content $x = 32\%$) (Fig.2).

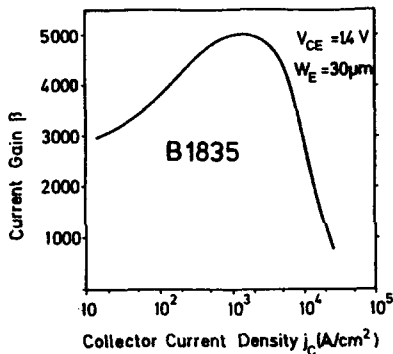


Fig. 2: Current gain β versus collector current density j_c . Sample B 1835 was completely grown by Si-MBE (emitter doping $N_E = 1 \cdot 10^{18}/\text{cm}^3$, base doping $N_B = 5 \cdot 10^{18}/\text{cm}^3$) and processed to transistors at Ruhr-University, Bochum [8].

The current gain of a homojunction transistor for comparison grown with similar doping levels was about ten (Fig. 3).

Indeed, extremely high current gains are not needed for circuit applications. Instead, device designers will get more freedom to optimize circuits by decreasing the current gain to the usual levels (30-200). Emitter and base doping levels can be varied within a wide range, and the base width can be decreased when increasing the base doping. By these changes capacitances, resistances and transit times can be influenced in a controlled manner.

The device designer is able to lead the optimization into different directions. One very spectacular direction is the enhancement of the transit frequency f_T , most clearly shown by the work of the Stanford/HP group [9] and the IBM group [6,7]. Integrated devices for digital applications also benefit from a decrease in base sheet resistance R_{sh} and in base-collector capacity C_{bc} , respectively. For the broad commercial market around 1 GHz - 10 GHz essential targets are reduction of noise (reduction of resistances) and relaxed production conditions (pitch width).

In this paper we will mainly describe our efforts to increase the base doping, decrease the base sheet resistance and to simplify device fabrication.

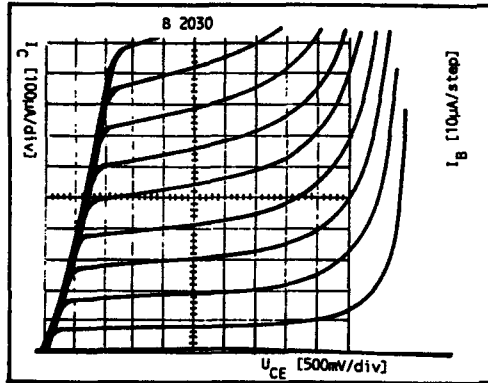


Fig. 3: Transistor characteristics - collector current I_C versus V_{CE} with base I_B as parameter - of a homojunction transistor (B 2030) with about the same doping levels ($1-2 \cdot 10^{18}/\text{cm}^3$) in emitter and base, respectively. Base width $w_B = 80 \text{ nm}$.

UNINTERRUPTED GROWTH OF THE COMPLETE LAYER SEQUENCE

For the experiments we used the elder Si-MBE equipment [10] additionally equipped with a substrate voltage supply for Sb-doping by secondary implantation (DSI) and a home made elemental boron effusion cell for p-doping [11]. Silicon is evaporated from an electron beam source, germanium from a PBN effusion cell. The growth chamber is connected to a storage chamber with a ten wafer magazin for wafer diameters up to 100 mm diameter. Samples grown in this equipment are coded B plus growth run number.

The complete layer sequence (table II) including the emitter contact is grown without interruption on either n^+ -substrates (As, 4 Ωcm) or on p^- -substrates with n^+ -buried layers (subcollector).

Table II: Typical layer sequences

Layer	Collector	Spacer	Base	Emitter	Emitter Contact
thickness (nm)	300	0-40	30-80	200	100
doping (cm^{-3})	Sb: $3 \cdot 10^{16}$	-	B: 10^{18} - 10^{20}	Sb: 10^{18}	Sb: 10^{20}
Ge-content (%)	0	20-30	20-30	0	0

For Sb-doping by DSI an Sb-adlayer of a certain fraction of a monolayer (ML) is pre-built up, and a substrate voltage U_s is applied for acceleration of the Si ions generated at the Si-source (electron gun evaporator). The high doping level of the emitter contact is realized by coevaporation Sb/Si at low temperatures or sometimes by a solid phase MBE process (table III).

Table III: Typical process parameters

Layer	Collector	Spacer	Base	Emitter	Emitter Contact
Temperature (°C)	550	450	450	550	300
Adlayer (ML)	Sb: 0.02	-	-	Sb: 0.1	-
Voltage U_s (V)	285	-	-	500/1000	-
Co-evaporation	-	-	B	-	Sb

An undoped SiGe-spacer was sometimes placed between collector and base to decouple the neutral base from the first critical heterojunction.

The layers were investigated by SIMS, X-ray diffraction, defect etching and electrical measurements. For conductivity and Hall effect measurements also single SiGe layers on p-substrates were provided. SIMS profiles (Fig. 4) showed very abrupt junctions as expected. But only at the emitter/base interface a

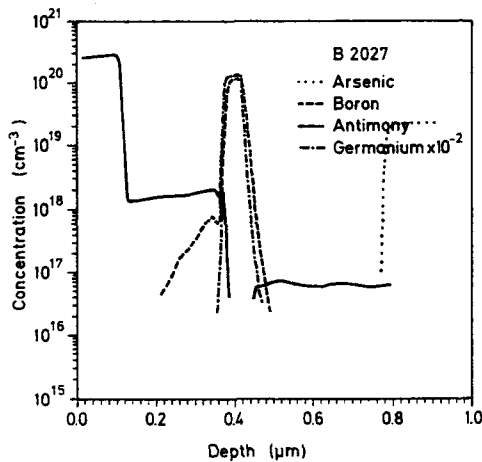


Fig. 4: SIMS profile of sample B 2027 with a base doping $N_B = 10^{20}/\text{cm}^3$. The Ge profile is scaled down by a factor 100.

considerable outdiffusion [12] of boron took place driven by defects (vacancies, interstitials) generated during the secondary implantation process (DSI). This boron outdiffusion causes a reduction of the effective emitter doping level near the E/B interface but even at the highest boron doping levels ($10^{20}/\text{cm}^3$) the p/n-junction was not shifted into the Si.

The base layer width was always smaller than the critical thickness t_c , which is decreasing from 160 nm ($x = 20\%$) to 94 nm ($x = 25\%$) to 60 nm ($x = 30\%$) for 550 °C growth temperature. The majority of samples did not exhibit a misfit dislocation network after defect etching, but with base layer thicknesses $> 0.5 t_c$ frequently the onset of dislocation networks could be seen. For the above described process sequence a base layer thickness below $t_c/2$ is recommended (ranging from 80 nm for $x = 20\%$ to 30 nm for $x = 30\%$).

BASE SHEET RESISTIVITY

A 100 nm thick base doped with $10^{18}/\text{cm}^3$ ($\rho = 4.5 \text{ m}\Omega\text{cm}$) yields a sheet resistivity of more than $4.5 \text{ k}\Omega/\square$ considering the effect of the depletion layers. With decreasing base width the situation gets worse, e.g. the fastest Si bipolar transistor [13] with $f_t = 51 \text{ GHz}$ showed $R_{sb} > 50 \text{ k}\Omega/\square$. We have grown SiGe-HBT structures with intrinsic base sheet resistivities R_{sb} ranging well below $1 \text{ k}\Omega/\square$ by increasing the base doping. The lowest value of the intrinsic sheet resistivity we found was $0.27 \text{ k}\Omega/\square$ for a 50 nm thick base with $10^{20}/\text{cm}^3$. Within the base dose from $5 \cdot 10^{13}/\text{cm}^2$ to $5 \cdot 10^{14}/\text{cm}^2$ the approximate relationship between dose ($N_B w_B$) and sheet resistivity R_{sb} was found as given in table IV.

Table IV: Base sheet resistivity R_{sb} ($\text{k}\Omega/\square$) versus base dose $N_B w_B$ (cm^{-2}). Ge content x and base width w_B of the samples varied between 0.18-0.3 and 80 nm - 35 nm, respectively. $N_B = 10^{19}/\text{cm}^3 - 10^{20}/\text{cm}^3$.

Dose	$5 \cdot 10^{13}$	$1 \cdot 10^{14}$	$3 \cdot 10^{14}$	$4.5 \cdot 10^{14}$
R_{sb}	1.75	0.95	0.4	0.3

These sheet resistivities correspond to a hole mobility between $70 \text{ cm}^2/\text{Vs}$ (dose: $5 \cdot 10^{13}/\text{cm}^2$) and $50 \text{ cm}^2/\text{Vs}$ (dose: $4.5 \cdot 10^{14}/\text{cm}^2$). Below a dose of $5 \cdot 10^{13}/\text{cm}^2$ the strong increase in sheet resistivity is not only a function of dose but also of the individual doping levels and widths (influence of depletion layers), e.g. with $N_B = 4 \cdot 10^{18}/\text{cm}^3$, $w_B = 65 \text{ nm}$ an R_{sb} of $7 \text{ k}\Omega/\square$ was obtained.

DEVICE PROCESSING

The complete layer structure is processed in two different ways into devices. In cooperation with Ruhr-University, Bochum [8,14,15] implantation is applied for contact definition. With conventional $1.5 \mu\text{m}$ optical lithography transit frequencies of 20 GHz - 27 GHz could be obtained. This group already demonstrated a 11.4 Gbit/s multiplexer IC with 12 GHz Si-bipolar transistors [16]. It is not unreasonable to aim for a 30 GHz multiplexer IC with HBT's of the above type. Within our own laboratory a simple process is under development which completely avoids additional diffusion or implantation steps for device

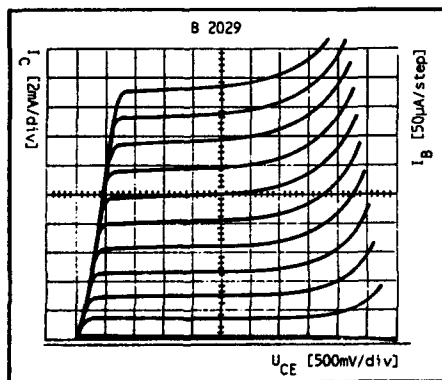


Fig. 5: Nearly ideal DC-characteristics of a SiGe-HBT with a 40 nm SiGe-spacer between base and collector (B 2029). $N_B = 1 \cdot 10^{19}/\text{cm}^3$, $w_B = 40 \text{ nm}$, $x = 0.18$.

fabrication [17,18]. A maximum frequency of oscillation $f_{max} = 23$ GHz could be obtained with structures grown on n^+ -buried layers. The device characteristics is influenced by recombination centers and surface leakage currents. A clear improvement could be obtained by a collector-up operation and by normal operation with SiGe spacer between collector and base (Fig. 5).

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CHARGE CONTROL IN SiGe QUANTUM-WELL MOSFETs AND MODFETs

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ABSTRACT

A one-dimensional charge control model based on the self-consistent numerical solution of the Schrodinger and Poisson equation has been developed for n- and p-channel quantum-well (QW) MOSFETs and MODFETs in the strained-layer SiGe heterostructure material system. Results are presented for prototype QW n-channel MODFET and MOSFET structures experimentally demonstrated in the literature. Side channel formation limits the maximum usable QW channel densities and voltage swings. The optimization of the charge control characteristics of the p-channel QW-MOSFET is achieved by maximizing the Ge content of the QW SiGe layer and minimizing the Si spacer thickness to the oxide. Channel densities on the order of $1 \times 10^{13} \text{cm}^{-2}$ are feasible.

INTRODUCTION

Recent advances in epitaxial growth technology and understanding of the strained-layer SiGe material system have opened the exciting prospect of an enhancement of current silicon microelectronics by compatible high-performance heterostructure and QW devices that could offer possibilities hitherto reserved to the field of III-V heterostructure materials. Superior results have already been demonstrated for SiGe heterostructure bipolar transistors. In 1985 and 1986 the first SiGe p- and n-channel modulation-doped field-effect transistors (MODFETs) have been reported by pioneering groups at AT&T Bell Labs [1] and at AEG [2]. Last year prototypes of SiGe QW p-channel MOSFETs have been demonstrated at UCLA, IBM and Princeton University.[3,4,5]

N-channel MODFETs (FETs) in the SiGe system have to use electron transport in Si layers lattice matched to SiGe substrates or to relaxed buffers in order to obtain significant conduction band discontinuities for the channel confinement.[2] In these transistors the in-plane electron mobility is expected to be improved not only because of the modulation doping but also due to the effect of the bi-axial tensile strain in the Si QW-channel. The 2-fold degenerate X-valleys normal to the plane are lowered compared to the 4-fold degenerate in-plane X-valleys so that the low transverse effective masses determine the electron transport.

SiGe QW p-MOSFETs are of particular interest because they combine the advantage of an insulating SiO_2 gate with an improved hole transport in undoped buried SiGe QW layers lattice matched to the Si substrate. In such strained layers the in-plane hole mobility is predicted to be significantly improved as compared to silicon due to the Ge content and the bi-axial compressive strain [6] because the in-plane effective hole mass of the highest valence band is reduced and the degenerate heavy and light hole bands are strain-split leading to a reduction in scattering probability. Monte Carlo transport calculations [6] suggest an in-plane hole mobility for $\text{Ge}_{0.4}\text{Si}_{0.6}/\text{Si}$ of about 4 times the value of undoped Si at room temperature that could yield a factor of about 8 as compared to p-channel mobilities of conventional MOSFETs. SiGe p-channel QW-MOSFETs might thus, e.g., lead to an improvement of CMOS circuits that are limited by low transconductances and currents of standard p-MOSFETs.

This paper presents the first theoretical investigation of the charge control characteristics of n-channel MODFETs and of p-channel QW-MOSFETs in the strained-layer SiGe system based on an one-dimensional quantum-mechanical model. The charge control characteristic is the dependence of the channel charge and its distribution on the applied gate voltage and thus constitutes the most fundamental property of any heterostructure or QW-FET structure. Of particular importance is the maximum usable channel density that together with the carrier velocity determines the maximum achievable currents. First, the analysis focuses as an example on the prototype of the n-channel MODFET structure realized by Kasper and Daembkes[2] and then on the prototype p-channel QW-MOSFET structure demonstrated by Nayak et al.[3]. Starting from the latter, the study investigates the improvement of the SiGe p-channel QW-MOSFET epitaxial layer structure for optimized charge control characteristics of this transistor. A classical model calculation of p-channel QW-MOSFETs has been reported recently in [5].

MODEL

The model is based on the self-consistent numerical solution of the one-dimensional Schroedinger and Poisson equation by means of a finite-difference method similar to [7,8] to obtain the charge and potential distribution in the gated FET structure. The quantum-mechanical electron or hole distributions are determined from the subband eigenenergies, corresponding envelope wavefunctions and 2-dimensional subband occupation statistics.[7] Either electrons or holes are quantized for n- or p-channel structures, the respective opposite carrier type is taken into account classically. For comparison, also full classical calculations with 3-dimensional densities of states could be made. The model comprises the following features:

- 1) Arbitrary position dependent strained $\text{Ge}_x\text{Si}_{1-x}$ layer structure lattice matched to a $\text{Ge}_y\text{Si}_{1-y}$ substrate. The strain and composition dependent conduction and valence bands are calculated according to the phenomenological deformation potential theory [9] and theoretical valence band off-sets [10].
- 2) Two strain-split conduction band types (X-valleys) according to the lifting of the 6-fold degenerate valleys into 2-fold degenerate valleys normal to and 4-fold degenerate valleys in the plane. Strained $\text{Ge}_x\text{Si}_{1-x}$ longitudinal and transverse effective electron masses of the X-valleys are assumed to be constant and equal to Si. That is accurate within a few percents. (P. Vogl, 1991)
- 3) Three strain-split valence bands (HH, LH and SOH) using the parameters and interpolations of [9,13]. Also included are the strain dependent respective hole masses for z-direction quantization normal to the plane.[11] For the 2D hole subband occupations appropriately averaged 2D effective density of states masses [12] are assumed on the basis of the unstrained $\text{Ge}_x\text{Si}_{1-x}$ alloy values.
- 4) The Ben Daniel Duke form [12] of the single particle Schroedinger equation to account for the position dependent effective masses of the conduction and valence bands. For the latter this is a first order approximation to avoid the complications of the mixing of valence band states.[12,13]
- 5) Equilibrium Fermi-Dirac statistics with no current flow with a constant Fermi level in the SiGe structure. The gate voltage determines the difference to the gate Fermi level. The calculations included the occupation of 10 quantized subbands for each of the conduction or valence bands. All model simulations in this paper are done for a temperature of 300 K.
- 6) Arbitrary donor and acceptor profiles with Fermi-Dirac occupation statistics
- 7) Metal (PolySi)-Oxide or Schottky gates for MOSFET or MODFET structures, respectively.

SIMULATION OF THE N-CHANNEL MODFET

Fig. 1 shows the structure of the first SiGe n-channel MODFET realized by Kasper and Daembkes[2]. Because of some ambiguity in the data a delta-doping level of $N_d = 1.8 \times 10^{19} \text{cm}^{-3}$ and a Schottky barrier of 0.6 eV were assumed. The calculated results for the conduction band(s), quantum-mechanical electron density and the six lowest subband eigenenergies are depicted in Fig. 2. It is seen that the electron channel charge in the strained Si V that is formed by the lower two-fold degenerate valley energy $E_c(2)$ has a sharp peak at the heterointerface to the $\text{Ge}_{0.5}\text{Si}_{0.5}$ top layer. The charge distribution is similar to the one in a single heterostructure FET because the Si channel layer is comparatively wide (20 nm) and the quantized energy levels have a small spacing due to the heavy longitudinal effective electron mass ($m_l \approx 0.98$).

A secondary charge peak is formed in the triangular potential well created by the delta-doping in the $\text{Ge}_{0.5}\text{Si}_{0.5}$ top layer that corresponds to the 4-fold degenerate valley energy $E_c(4)$. Here the small transverse effective mass ($m_t \approx 0.19$) of the valleys determines the quantization. The side channel formed in the delta-doped $\text{Ge}_{0.5}\text{Si}_{0.5}$ top layer strongly increases with applied gate voltage and eventually shields the Si channel charge. This can be seen in Fig. 3 that shows the dependence of the integrated QW-channel and side channel density on the gate voltage. At larger gate voltages the side channel density rises sharply leading to a saturation of the QW-channel density. The maximum usable channel density of this MODFET structure is thus limited to about $1.8 \times 10^{12} \text{cm}^{-2}$. At the same time the maximum voltage swing is limited to about 1V. In the actual structure additional limitations in the forward bias gate voltage arise due to the Schottky leakage current. The optimization of the charge control of the n-channel MODFET structure is not pursued further here, it follows similar lines as the optimization of the analogous III-V MODFET.

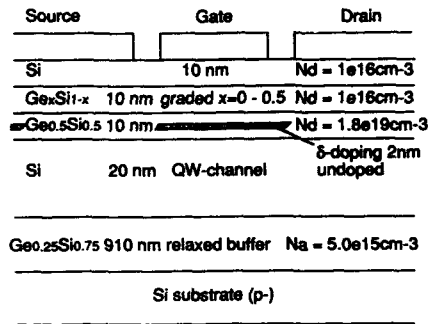


Fig. 1. N-channel SiGe MODFET structure after Kasper and Daembkes [2]. The QW-channel of this structure consists of a strained-Si layer lattice matched to a relaxed Ge_{0.25}Si_{0.75} buffer. Modulation doping is achieved with delta-doping in the Ge_{0.5}Si_{0.5} top layer.

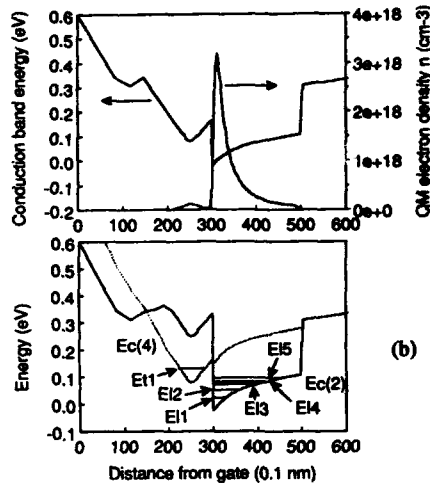


Fig. 2. N-channel SiGe MODFET simulation. (a) conduction band diagram and quantum-mechanical electron density distribution and (b) six lowest electron subband quantum levels. Ec(2) is the 2-fold and Ec(4) is the 4-fold degenerate X-valley energy. V_g = 0.0V, the Fermi level is at energy zero.

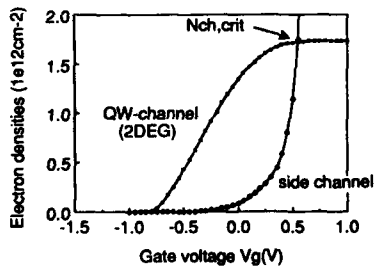


Fig. 3. N-channel MODFET charge control characteristics showing the integrated (areal) Si QW-channel and parasitic side channel electron densities as a function of the applied gate voltage. At N_{ch,crit} the side channel density becomes equal to the QW-channel density.

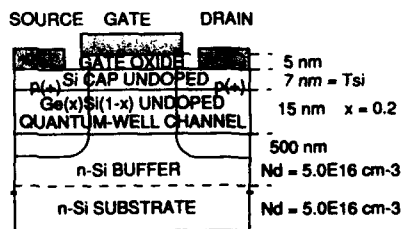


Fig. 4. P-channel SiGe QW-MOSFET cross section after Nayak et al. [3]. The original structure has a Ge_{0.2}Si_{0.8} quantum well and a Si spacer thickness T_{si} = 7 nm to the oxide. The Ge mole fraction x and T_{si} are varied in the optimization analysis.

P-CHANNEL QUANTUM-WELL MOSFET ANALYSIS AND OPTIMIZATION

Fig 4 shows the prototype p-channel QW-MOSFET structure of Nayak et al.[3]. The SiGe quantum well of the original structure has a Ge mole fraction of 0.2, a channel width of 15 nm and a Si spacer layer (cap) to the oxide of $T_{Si} = 7$ nm. The calculated energy band diagram, quantum-mechanical hole density distribution and the 5 lowest hole subband energy levels (heavy and light) are shown in Fig. 5. Although the hole distribution peaks in the SiGe QW forming the desired p-channel it can be seen that a secondary peak occurs in the Si cap layer at the oxide interface. This corresponds to an unwanted parasitic MOSFET side channel that increases rapidly with increasing gate voltage for this structure. This is seen in Fig.6a that shows the calculated integrated QW-channel and side channel hole densities as a function of the applied gate voltage. With increasing negative gate bias the QW-channel density saturates because the gate control of the SiGe channel is shielded by the side channel charge. Eventually the side channel density becomes larger than the QW-channel density so that the device essentially behaves like a conventional p-MOSFET.

A rough measure of the maximum usable QW-channel density is the value $N_{ch,crit}$ where it becomes equal to the side channel density. This amounts only to about $1 \times 10^{12} \text{cm}^{-2}$ in this structure. This also determines a maximum useful voltage swing that is only about 0.5 V. An additional important characteristic is the small signal charge control behavior of the QW-channel that is the capacitance vs gate voltage curve shown in Fig. 7a. This capacitance is related to the expected QW-transconductance of the device. The voltage range where the QW-capacitance dominates is very small. It can be concluded that the design of the considered prototype structure [3] can still be improved, the contribution of the QW-channel to the device performance is probably quite small at room temperature.

In order to optimize the structure, the influence of the epitaxial layer parameters on the charge control characteristics has been investigated. It turns out that the key parameters for the charge control optimization are the Ge mole fraction x of the $\text{Ge}_x\text{Si}_{1-x}$ QW that determines the valence band offset to the Si (depth of the QW) and the thickness T_{Si} of the Si spacer layer between the QW and the oxide interface (see also [5]). The thickness of the $\text{Ge}_x\text{Si}_{1-x}$ QW layer has practically no influence on the modeled charge control behavior down to at least 6 nm.

The effect of the Ge mole fraction of the QW is demonstrated by the result of calculations for the case that the Ge mole fraction x is changed from 0.2 to 0.4 while all other parameters are kept unchanged. Fig. 8 shows that for the same gate voltage the QW-channel hole density increases by more than a factor of 2, and that the side channel at the Si/Oxide interface disappears. In Fig.6b the influence of the increase in x on the charge control characteristics is seen. The side channel formation sets in only at a much higher negative gate voltage leading to a significantly improved critical channel density of about $2.7 \times 10^{12} \text{cm}^{-2}$ and a much larger voltage swing of about 1.5 V. The range where the QW-well channel density dominates the device behavior is thus much wider than in the original structure. This can also be recognized from the calculated capacitance-voltage behavior (Fig. 7b) that exhibits a wide voltage range where the QW-channel dominates leading to a characteristic knee in the total capacitance-voltage curve.

The reason for the improved charge control characteristics of the higher Ge mole fraction QW is essentially the increased energetic depth of the well that reduces the level occupations responsible for the side channel formation. Similarly, a reduced Si spacer layer thickness T_{Si} between the QW and the oxide energetically raises the hole energy of the side channel levels and thus also reduces the side channel formation. Fig. 9 shows the results of the calculated critical channel densities $N_{ch,crit}$ as a function of the key parameters of the p-channel QW-MOSFET, the Ge mole fraction x and the Si spacer thickness T_{Si} . It can be seen that in the original structure with $x = 0.2$ and $T_{Si} = 7$ nm a reduction of the spacer thickness to 2 nm would increase the usable maximum QW-channel density by almost a factor of 6. Generally, it is obvious that the charge control characteristic of the p-channel SiGe QW-MOSFET is optimized by choosing the highest possible Ge mole fraction for the SiGe QW and the smallest possible Si spacer thickness to the oxide. Theoretically, usable QW channel densities on the order of $1 \times 10^{13} \text{cm}^{-2}$ can be achieved.

The described optimization of the charge control properties will, of course, be limited by many other physical and technological factors leading to trade-offs in the performance and feasibility of device fabrication. To name a few: Increased Ge mole fractions require thinner QW thicknesses for the stability of the strained SiGe layers. This in turn can reduce the transport properties by interface roughness. Similarly, the reduction of the Si spacer thickness leads to increased interface states [4] and remote scattering. Furthermore, the x of the QW probably also influences the channel transport by alloy scattering. Therefore, beyond the optimization of the charge control

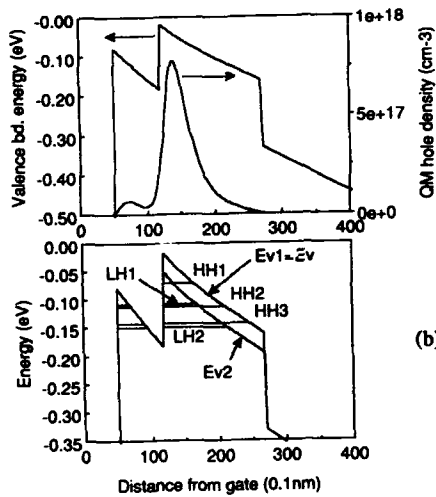


Fig. 5. P-channel SiGe QW-MOSFET structure simulation for $\text{Ge}_{0.2}\text{Si}_{0.8}$ quantum-well at a gate voltage of -1.25V . (a) Valence band energy diagram and quantum-mechanical hole density distribution showing the side channel peak at the Si/Oxide interface; (b) five lowest heavy and light hole subband energy quantum-levels: HH1, LH1, HH2, HH3, LH2. The heavy and light hole valence bands Ev_1 and Ev_2 are strain-split in the well. Fermi energy is at zero.

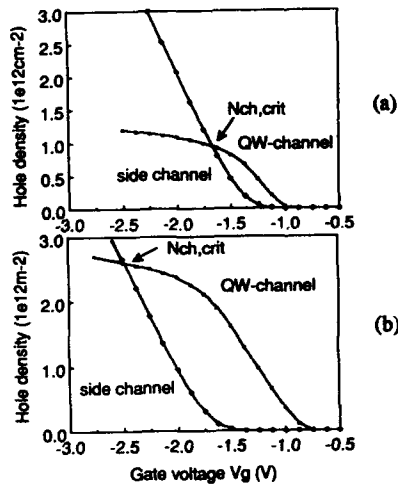


Fig. 6. P-channel SiGe QW-MOSFET structure charge control characteristics. (a) for the prototype structure [3] (Fig. 4) with a $\text{Ge}_{0.2}\text{Si}_{0.8}$ QW, and (b) for the same structure with a $\text{Ge}_{0.4}\text{Si}_{0.8}$ QW.

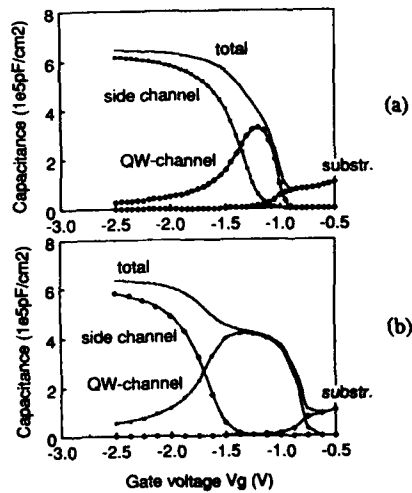


Fig. 7. P-channel SiGe QW-MOSFET structure small-signal capacitances. (a) for the prototype structure[3] (Fig. 4) with a $\text{Ge}_{0.2}\text{Si}_{0.8}$ QW, and (b) for the same structure with a $\text{Ge}_{0.4}\text{Si}_{0.6}$ QW.

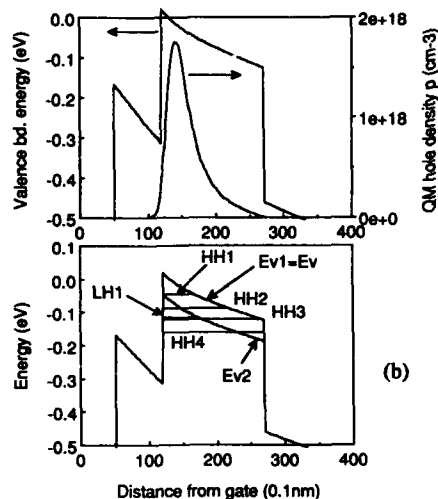


Fig. 8. P-channel SiGe QW-MOSFET structure simulation for a $\text{Ge}_{0.4}\text{Si}_{0.6}$ QW. Otherwise identical to case to Fig. 5. Because of the larger x the QW-channel density is larger and the side channel formation is negligible.

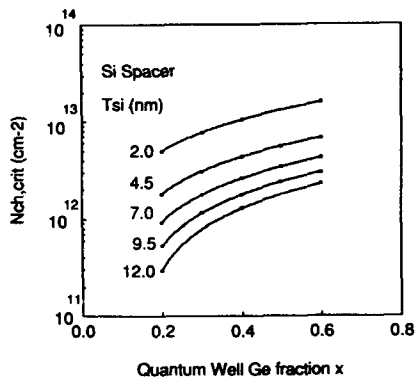


Fig. 9. Critical QW hole channel densities $N_{ch,crit}$ of p-channel SiGe QW-MOSFET structures as a function of the QW Ge mole fraction x and the Si spacer thickness with T_{si} as a parameter. $N_{ch,crit}$ indicates the maximum usable SiGe hole channel density for a given structure. For $x = 0.6$ the calculations were done for a QW thickness of 6 nm. Otherwise the structures had the parameters of Fig. 4.

characteristics also a careful investigation of all these factors has to be carried out to determine the conditions for a p-channel SiGe QW-MOSFET with superior device characteristics.

CONCLUSIONS

A quantum-mechanical charge control model has been developed for the strained-layer SiGe heterostructure material system to investigate the properties of n- and p-channel QW-MOSFETs and MODFETs. Results for prototype n-channel MODFETs and p-channel QW-MOSFETs have been presented. In both cases side channel formation between the QW-channel and the gate determines the maximum usable channel densities. The first demonstrated p-channel QW-MOSFET prototype with a $\text{Ge}_{0.2}\text{Si}_{0.8}$ quantum well and comparatively thick 7 nm Si spacer layers to the oxide had only a comparatively small maximum usable channel density ($N_{ch,crit} \approx 1 \times 10^{12} \text{cm}^{-2}$) and voltage swing at room temperature. It can still be considerably improved by optimizing the epitaxial device structure. Optimization for maximum usable channel densities and voltage swings is achieved by maximizing the QW Ge mole fraction and minimizing the Si spacer thickness to the oxide. The thickness of the SiGe QW-layer has little influence on the charge control down to at least 6 nm. QW hole channel densities on the order of $1 \times 10^{13} \text{cm}^{-2}$ can be achieved. Trade-offs have to be considered regarding the channel transport and technological factors to achieve p-channel SiGe QW-MOSFETs with overall superior device performance.

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CHANNEL PROFILE ENGINEERING OF MOSFETS USING DELTA DOPING.

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ABSTRACT

The influence of the location, dose and width of the doping spike in a delta doped MOSFET is investigated theoretically. Calculations are performed for a range of n and p type δ MOSFETs, and the importance of each design parameter of the device is assessed. The optimum device has a delta layer around 20nm deep, with a sheet doping density around 10^{12}cm^{-2} for the pMOSFET and 5.10^{11}cm^{-2} for the nMOSFET. The effect of diffusion of the dopant during processing on the device performance is also considered, and it is found that this causes a shift in the threshold voltage of the device. The layer width should ideally be kept below 5nm.

INTRODUCTION

The technique of atomic layer doping (ALD), or delta-doping (δ -doping), involves the deposition of a single atomic plane of dopant atoms. Such structures can be grown by molecular beam epitaxy (MBE), and have been reported in both silicon [1-3] and GaAs [4,5] for n and p type dopants. These δ -layers have been used in a range of device applications including the planar doped barrier diode [6], and as conducting channels [5,7] and punchthrough stoppers [8,9] in field effect transistors (FETs). In this paper we study the use of the δ -layer as the conducting channel in a silicon MOSFET using a 2D model to simulate the device characteristics. Such δ MOSFETs have recently been grown by Nagakawa and coworkers [9], and are of particular interest because of the advantages these devices are expected to offer over conventional structures in the sub-micron regime. The removal of the channel from the Si-SiO₂ interface can result in an improvement in mobility and a reduction in the injection of hot electrons into the gate oxide.

There are reports of calculations on the properties of δ -doped FETs in the literature [10,11], but there has been no systematic study of the importance of the various design parameters of such a device. In this paper we discuss the way in which the doping profile of the device (i.e. the depth, dose and width of the δ -layer) influences the current-voltage characteristic of the device. Sample devices (both n and p type) have been modelled and the range of useful devices isolated. The optimum design is discussed and the impact of dopant diffusion during processing of the device is considered.

CALCULATION DETAILS

The basic design of a δ MOSFET is shown in figure 1. A δ -doped layer is grown around 10-50nm below the gate oxide to

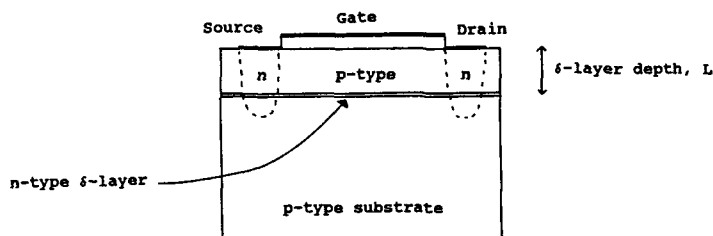


Figure 1.
n-type δ MOSFET.

act as the conducting channel. In some designs [8,9] a second δ -layer of the opposite polarity is grown deeper into the device to act as a punchthrough stopper. In a conventional MOSFET there are several design parameters which can be adjusted to achieve the desired characteristics, such as the gate length, oxide thickness, substrate doping and source and drain implant doping profile. In a δ MOSFET there is additional scope for tailoring the device performance, since the dose and position of the δ -layer can also be specified. In principle, it is also possible to dope the substrate and surface regions independently in such a device. Another important factor is the width of the doped layer, which will be governed primarily by the controllability of the MBE growth of the epilayer and by thermal diffusion of the dopant during processing of the device.

The calculations presented were all carried out using the HFIELDS device model [12], which solves the Poisson and current continuity equations in two dimensions using a finite element method. The current densities are obtained in the drift-diffusion approximation, and to assist with convergence only continuity of the current contribution due to the primary carrier (electrons for nMOSFETs and holes for pMOSFETs) is required. Boltzmann statistics are used, and dopant atoms are assumed to be fully ionised. All simulations were performed for room temperature operation.

In the specification of the δ -layer, a top hat doping distribution is used. The δ -layer is assumed to behave as a very thin slice of uniformly doped bulk material. In practice quantum effects can become important in such ultra-thin layers, but these are not expected to be significant at room temperature. The major inaccuracy in this classical approach is likely to arise from a modification in the mobility of the layer, resulting from a combination of heavy doping, strain and quantum effects. There has been no theoretical study of the mobility in such a layer which includes all these effects, however, and the limited experimental data available from Hall measurements [3] suggests that the mobility is not greatly modified from that for bulk materials of the same doping density.

The basic MOSFET designs used were based on those of standard industrial $3\mu\text{m}$ or $5\mu\text{m}$ processes, with 50nm oxide thickness. pMOSFETs ($3\mu\text{m}$ gate) and nMOSFETs ($5\mu\text{m}$ gate) were simulated with δ -layers positioned between 10 and 40nm below the Si-SiO_2 interface and sheet doping densities in the range $5 \cdot 10^{11}$ to $2 \cdot 10^{12} \text{cm}^{-2}$. Typical layer widths of δ -layers reported are of the order of a few nm, although precise determination of the achieved layer widths is difficult because of the

resolution limits of characterisation techniques. Layer widths of 1nm to 10nm were modelled to investigate the likely impact of dopant diffusion during processing on the device characteristics. The starting point for both sets of devices was a structure with a δ -layer 2nm wide, 20nm deep, and a sheet doping concentration of 10^{12} cm^{-2} . All calculations were carried out on a VAXstation 3100, and typically required one hour of CPU time to obtain results for 10 applied bias points.

RESULTS

The effect of the sheet doping concentration of the δ -layer on the current-voltage characteristic of a p-type δ MOSFET is shown in figure 2. The characteristic of a conventional pMOSFET of the same geometry is shown for comparison. At the highest density considered, $2 \cdot 10^{12} \text{ cm}^{-2}$, the density of mobile charge in the δ -layer is so high that the device is virtually impossible to switch off. Conversely, at the lowest doping level, $5 \cdot 10^{11} \text{ cm}^{-2}$, there is too little charge in the layer and the device is prone to the formation of a parasitic surface channel. The optimum device has a sheet carrier concentration of 10^{12} cm^{-2} . Clearly even a relatively small change in the doping density of the δ -layer has a dramatic effect on the viability of the device, so precise control of the number of dopant atoms deposited during growth is essential for these devices. An important factor which emerges from these results is the size of the 'window' of δ -channel operation. All of the devices operate in a two channel mode (surface channel and δ -layer channel) at gate voltages for which the conventional MOSFET with the same substrate doping would be switched on. It would appear to be undesirable to operate in this regime, and hence δ MOSFETs can only operate over a finite range of applied gate bias, corresponding to the difference in threshold voltages between the δ -layer device and the equivalent conventional structure. This range can be adjusted by varying the doping of the region of the device between the oxide and the δ -layer, so the tendency of a particular structure to exhibit surface channel operation does not necessarily rule out its viability as a useful device.

Figure 3 shows the transconductance of the above devices. The onset of surface channel operation is clearly seen in this figure, since the transconductance of the δ -layer structures is lower than that of a conventional long channel device. It is believed that δ -layer devices do not suffer the same degradation in transconductance in the short channel regime as conventional devices [7]. For submicron structures the δ MOSFET is expected to have a higher transconductance than the standard structure. This result confirms the tendency of the $5 \cdot 10^{11} \text{ cm}^{-2}$ device to operate in a 'bi-channel' mode.

The effect of the position of the doping spike on the device characteristics is shown in figure 4, with the corresponding transconductances in figure 5. If the δ -layer is too far from the gate, it becomes difficult to switch off. As the layer depth is reduced, the gate control is improved and the transconductance of the device is increased. At the same time, the voltage window for δ -channel operation is reduced, and the device with the 10nm deep layer is prone to surface channel formation. The position of the δ -layer also indirectly affects the reliability of the device, through its impact on

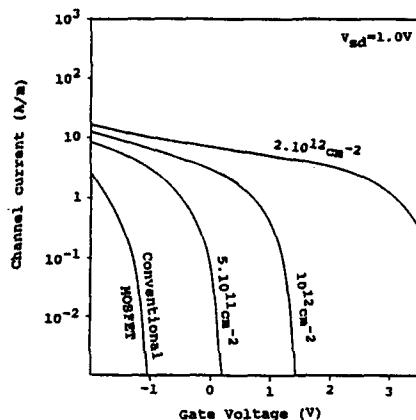


Figure 2.
Effect of sheet doping concentration on p-type δ MOSFET : I-V curve.

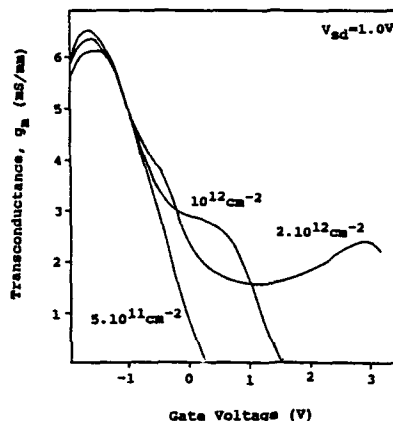


Figure 3.
Effect of sheet doping concentration on p-type δ MOSFET : transconductance.

the degree of hot carrier injection into the gate. The gate current can be shown by a lucky electron model [13] to be reduced by a factor of $\exp(L/d)$ in the δ -doped device compared to a conventional MOSFET, where L is the depth of the δ -layer relative to the Si-SiO₂ interface, and d is the hot carrier mean free path, which is of the order of 10nm. The effect of the channel depth on the transconductance and on the gate current must thus be traded off, and it is likely that the device with the 20nm deep layer offers the best compromise.

The 5 μ m n-type devices show qualitatively similar behaviour to the 3 μ m pMOSFETs, but the optimum design is slightly different due to the different effective mass and mobility of the carriers, and the devices are deeper into the depletion mode regime. Figure 6 shows how the current-voltage curve depends on the doping level of the δ -layer. Clearly a lower dose is required than for the p-type devices; the optimum sheet doping density is around 5.10^{11}cm^{-2} . Figure 7 shows the effect of the δ -layer depth on the device characteristic. As for the p-type structures, the depth must be kept below 40nm if the device is to switch easily. Again, a depth of 20nm would appear to achieve a good compromise between transconductance and oxide damage.

Another important consideration in δ MOSFETs is the possibility of dopant diffusion during the growth and processing of the device. Figure 8 shows the effect of the width of the δ -layer on the device characteristics of the n-type structure for a constant sheet doping concentration of 6.10^{11}cm^{-2} . The main consequence of a change in the δ -layer width is to shift the threshold voltage. It can be seen that for layer widths up to 4nm no degradation occurs and it is thus desirable, where possible, to ensure that the final processed device has a doping spike no wider than 5nm. For this particular device, with the δ -layer 25nm deep, the device still appears to have reasonable characteristics even if the dopant diffuses still further, although the threshold voltage

then becomes difficult to control.

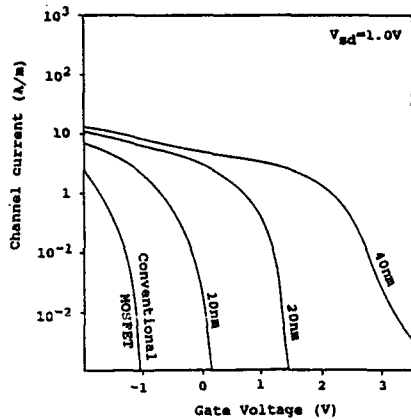


Figure 4.
Effect of δ -layer depth on p-type δ MOSFET : I-V curve.

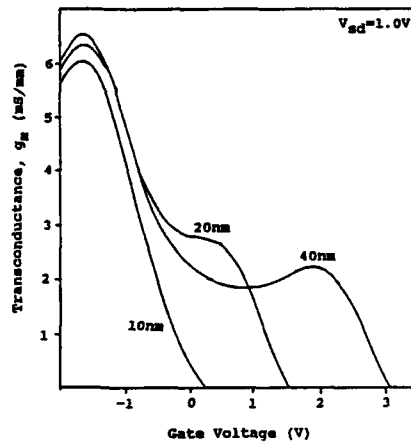


Figure 5.
Effect of δ -layer depth on p-type δ MOSFET : transconductance.

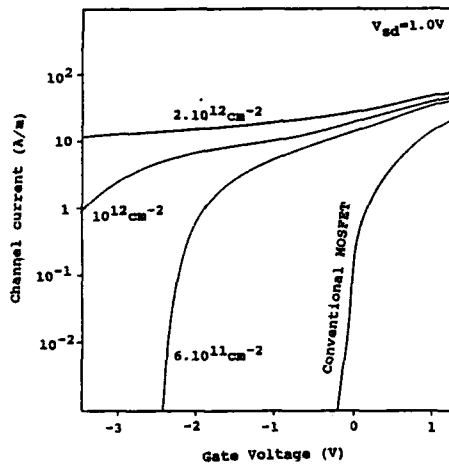


Figure 6.
Effect of sheet doping concentration on n-type δ MOSFET : I-V curve.

SUMMARY

The role played by the doping profile of the δ -layer in a δ MOSFET has been analysed using a two dimensional device modelling package. The sheet doping concentration is found to play a critical role, with the optimum level found to be 10^{12}cm^{-2} in the pMOSFET structures studied, and $5 \cdot 10^{11} \text{cm}^{-2}$ in the nMOSFETs. The δ -layer should be positioned 20nm below the oxide (for a 50nm oxide) to balance the requirements of high transconductance and low gate current. Diffusion of the dopant should ideally be kept to below 5nm, although the main effect of an increase in the layer width is to shift the threshold voltage without causing a major change in the transconductance.

In this paper we have investigated the role played by the doping profile of the δ -layer in δ MOSFETs. Only long channel devices were studied in order to be able to test the predictions against devices grown by MBE [14]; results of this

comparison will be reported elsewhere. The promise of the δ MOSFET, however lies in the prospect of overcoming the short-channel effects inherent in standard MOSFET structures.

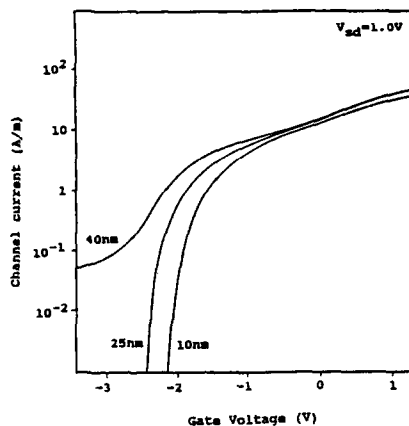


Figure 7.
Effect of δ -layer depth on n-type δ MOSFET : I-V curve.

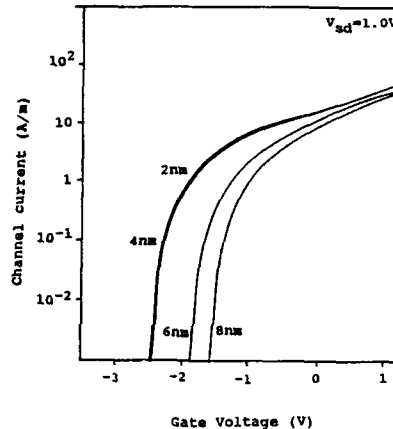


Figure 8.
Effect of δ -layer width on n-type δ MOSFET : I-V curve.

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Si/Si_{1-x}Ge_x p-CHANNEL MOSFETs FABRICATED USING A GATE QUALITY DIELECTRIC PROCESS

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ABSTRACT

The use of Si_{1-x}Ge_x alloys for p-channel high transconductance MOSFETs requires a high quality dielectric system. Direct oxidation of Si_{1-x}Ge_x alloys or even low temperature deposition of SiO₂ directly on Si_{1-x}Ge_x results in a very high interface state density. We show that low interface state densities (below 10¹¹ eV⁻¹cm⁻²) can be obtained using both thermal and PECVD oxides through the use of a thin (6-8 nm) Si cap between the oxide and the Si_{1-x}Ge_x layer. The Si cap layer leads to a sequential turn-on of the Si_{1-x}Ge_x channel and the Si cap channel, as clearly observed in low temperature C-V curves. We show that this dual channel structure can be designed to suppress the parasitic Si cap channel. High quality, fully isolated Si_{1-x}Ge_x p-channel MOSFETs have been fabricated in an integrable, low Dt process using both thermal or PECVD gate oxides and selective UHV/CVD for the Si/Si_{1-x}Ge_x channels. We show that optimally designed Si/Si_{1-x}Ge_x MOSFETs exhibit up to 70% higher transconductance at 300K than control Si devices fabricated on n-doped 10¹⁷/cm³ Si substrates. Si/Si_{1-x}Ge_x p-channel MOSFETs with thermal and PECVD gate oxides show comparable device characteristics.

INTRODUCTION

The application of Si_{1-x}Ge_x alloys to Si-based heterojunction devices such as the heterojunction bipolar transistor [1] can enhance the performance of silicon-based technology. Motivation to use SiGe channels instead of conventional Si channels, especially in p-channel devices, both in a CMOS and also BiCMOS technology is strong in light of the higher hole channel-mobilities predicted in this system [2]. However, the application of SiGe alloys to field-effect devices has been more difficult. The oxidation of Si_{1-x}Ge_x alloys is complex, and a transient enhancement in thermal oxidation rate has been observed. Silicon is preferentially oxidized leading to a pile-up of Ge at the SiGe/SiO₂ interface. We find that this pileup results in a degraded oxide/semiconductor interface with interface state densities much greater than 10¹² eV⁻¹cm⁻². The use of a deposited oxide such as a Plasma Enhanced Chemical Vapor Deposited (PECVD) oxide directly on SiGe does not significantly reduce the interface state density, because the initial stages of oxidation consist of oxide growth rather than pure deposition. We have investigated the use of a thin (6-8 nm) Si cap layer over the SiGe alloy to prevent the SiGe alloy from being exposed to the oxidizing ambience. To be useful, this cap layer thickness should be minimized so that the dominant conduction channel is contained in the SiGe layer. The relative

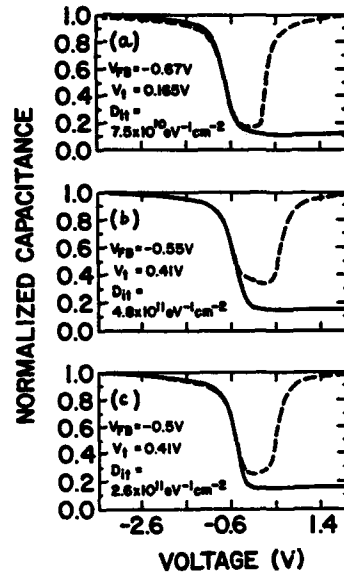


Fig. 1: High frequency (solid) and quasi-static (dashed) C-V curves for $\text{Si}_{1-x}\text{Ge}_x$ capacitor structures after post-metal anneal. (a) Si control, (b) $x = 0.15$, Si cap thickness = 3 nm, (c) $x = 0.15$, Si cap thickness = 4.5 nm. Interface state density, D_{it} , flat band voltage, V_{FB} , and threshold voltage, V_T are also indicated.

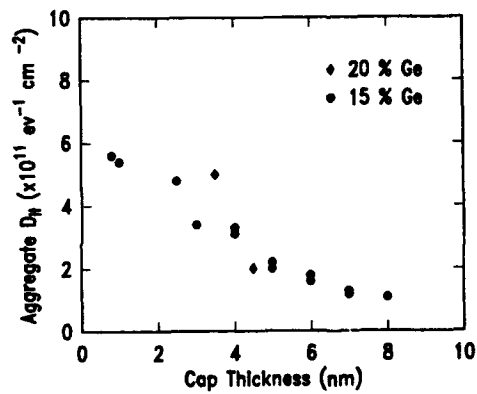


Fig. 2: Interface state density, D_{it} plotted as a function of Si cap thickness. At a cap thickness of 10 nm, the D_{it} is comparable to a control Si MOS capacitor. Note the relative insensitivity of D_{it} to the Ge concentration in the underlying $\text{Si}_{1-x}\text{Ge}_x$ layer.

carrier population in the Si and SiGe layers in this dual channel MOSFET [3, 4] is dependent on gate and drain biases and operating temperature.

EXPERIMENT AND RESULTS

Si/Si_{1-x}Ge_x(0<x<0.3)/Si structures were grown on a variety of p- and n- type substrates typically with a resistivity of 2-5 ohm-cm using Molecular Beam Epitaxy (MBE) and ultra-high vacuum chemical vapor deposition (UHV/CVD). The Si cap thickness in the MBE wafers was varied between 0 and 10 nm. MOS capacitor structures were fabricated using procedures described elsewhere [5]. The composition and thickness of the oxide/Si cap/Si_{1-x}Ge_x channel structure was verified using spectroscopic ellipsometry and C-V measurements.

High frequency (100KHz) and quasi-static C-V (ramp rate = 0.045 V/sec) curves were obtained for aluminum gate, Si/Si_{1-x}Ge_x (x≤0.3) capacitors with a 14 nm thick PECVD oxide. The residual interface state density decreases as the Si cap thickness is increased (see Figs. 1 and 2). D_{it} decreases rapidly at first from over 5×10^{12} eV⁻¹cm⁻² for no Si cap (off scale in Fig. 1) and then slowly decreases to values comparable to control Si devices (around 4×10^{10} eV⁻¹cm⁻²) for a cap thickness of 10 nm. In addition, on some wafers with a Si cap thickness of 12 nm, thermal oxidation at 800°C to yield a oxide thickness of 10 nm (leaving behind a 7 nm Si cap) was carried out. Low interface state densities of 6×10^{10} eV⁻¹cm⁻² were consistently measured on these thermally oxidized Si/Si_{1-x}Ge_x structures.

Ramped C-V curves ($C = 1/(dV/dt)$) taken at low temperature (83K) at a ramp rate of 0.1 V/sec (see Fig. 3) reveal additional features not observed at room temperature. As negative bias on the gate is increased, the sequential population of first, the Si_{1-x}Ge_x channel, and subsequently the cap Si channel, is observed (see Fig. 3). The mobile positive charge in the structure is exclusively contained in the Si_{1-x}Ge_x channel for negative gate voltages below about 1.7 V. This accounts for the first plateau in the C-V curve. At greater negative gate biases, the charge is added mainly to the channel at the Si/ interface, and the capacitance saturates to the oxide capacitance. Fig. 3 also shows that as the Si cap is reduced, the parasitic Si cap channel is dominant. However, as shown earlier in Fig. 2, the resulting high D_{it} is a severe concern for Si cap thicknesses below 5 nm. At room temperature both the Si and SiGe channels are populated, and the relative carrier densities in these two channels is a function of the two channel thicknesses, Ge content, gate and drain biases, and the gate electrode material.

P-channel Si/Si_{1-x}Ge_x MOSFETs were fabricated using the dielectric process described above. The devices were isolated using a conventional semi-recessed oxide process. The Si/Si_{1-x}Ge_x (0≤x≤0.2) epitaxial layers were selectively grown in the device-active regions on these patterned wafers using UHV/CVD. Gate oxides (7 nm and 10 nm) were then either thermally grown at 800°C or deposited using PECVD at 350°C. The Si cap thickness was designed to be 7 nm in the completed structures. Details of the MOSFET fabrication procedures have been described elsewhere [6].

Fig. 4 shows the room temperature output characteristics for a representative 1μm gate p-channel MOSFET with 10nm thick thermal oxide and a 7nm Si/30nm

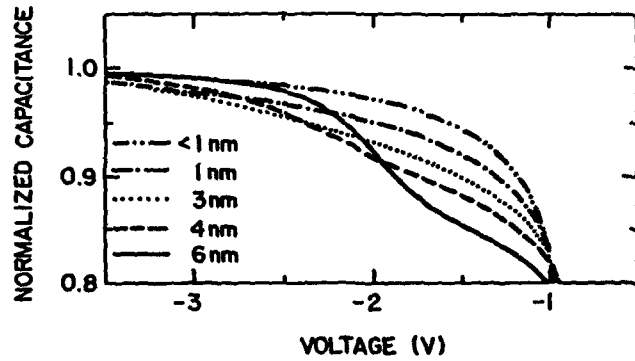


Fig. 3: Low temperature (83K) ramped (quasi-static) C-V curves for $\chi = 0.15$, $t_{ox} = 15$ nm, for different Si cap thicknesses. Note that for a cap thickness below 4 nm dual channel turn-on is not clearly observed. However, the interface state density for such thin Si cap layers is high (see Fig. 2).

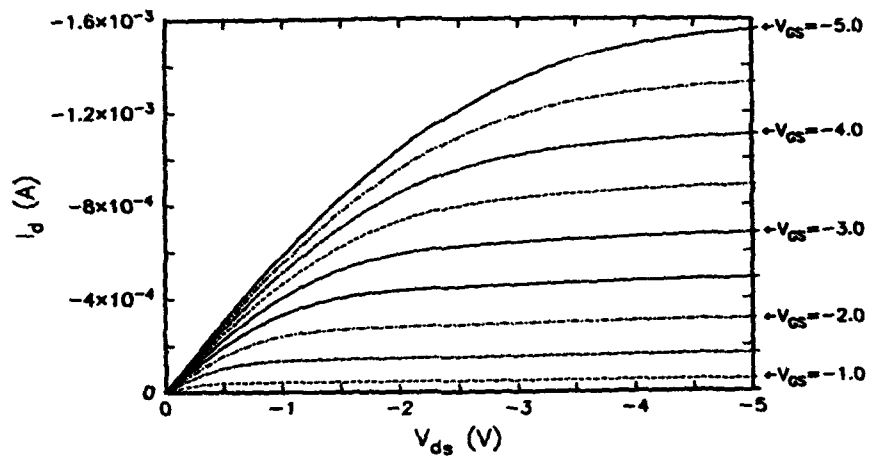


Fig. 4: Output characteristics at 300K for a 7 nmSi/30 nm $\text{Si}_{0.8}\text{Ge}_{0.2}$ p-channel MOSFET ($W/L = 10\mu\text{m}/1.3\mu\text{m}$) with a 100Å thermal oxide.

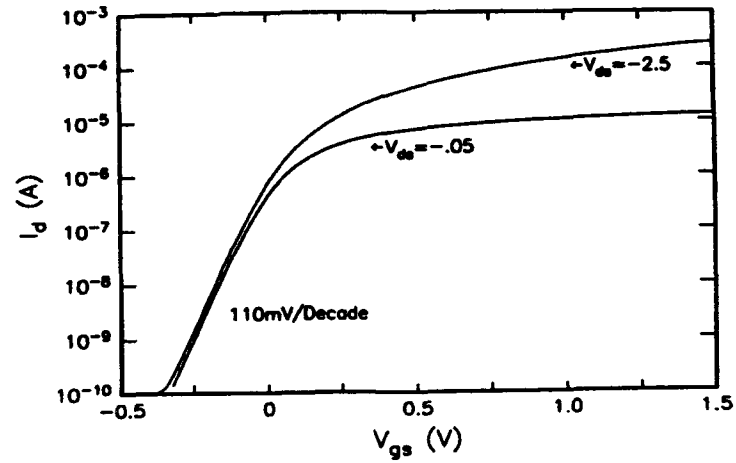


Fig. 5: Subthreshold characteristics at 300K for a 7 nm Si/30 nm $\text{Si}_{0.8}\text{Ge}_{0.2}$ p-MOSFET ($W/L = 10\mu\text{m}/1.3\mu\text{m}$) with a 100\AA thermal oxide.

Table I: Summary of $1\mu\text{m}$ effective channel length p-MOSFET Results at 300K

	%Ge	Thermal oxide	PECVD oxide	
		(10nm)	(10nm)	(7nm)
V_T (V)	0% control	-0.45	-	-0.5
	10%	-0.6	-0.6	-0.6
	20%	-0.38	-0.65	-0.55
g_m (mS/mm) ($V_D = -5V$)	0% control	26	-	35
	10%	45	44	53
	20%	46	40	54

$\text{Si}_{0.8}\text{Ge}_{0.2}$ channel. There is little difference in the output characteristics between devices fabricated with either thermal or PECVD gate oxides. The subthreshold characteristics (see Fig. 5) for the same device as in Fig. 4 show sharp turn-off with a subthreshold slope of 110 mV/decade. The subthreshold slope does not depend appreciably on the Ge content in the channel. However, the subthreshold slope for devices with PECVD oxide were lower (around 88 mV/decade) than those fabricated with thermal oxides. Table I summarizes the threshold voltage and maximum saturated transconductance obtained for the different structures used in this experiment. The n-type $10^{17}/\text{cm}^3$ Si control wafers contained no epitaxial layer and was processed alongside the Si/SiGe wafers. The SiGe devices with 10% and 20% Ge concentration exhibit as much as 70% larger maximum saturated transconductance, compared to the Si control device at $V_D = -5\text{V}$ (see Table I).

SUMMARY

We have demonstrated for the first time a high quality dielectric system for use with $\text{Si}_{1-x}\text{Ge}_x$ alloys - a prerequisite for MOSFET applications of $\text{Si}_{1-x}\text{Ge}_x$ alloys. The system employs either a PECVD deposited or thermally grown SiO_2 layer on a thin (6-8 nm) layer of pure silicon grown epitaxially on the $\text{Si}_{1-x}\text{Ge}_x$ layer. The Si cap layer prevents the accumulation of Ge at the oxide-semiconductor interface, and thus keeps the interface state density low. The use of the Si cap layer creates two charge channels. At low temperatures the $\text{Si}_{1-x}\text{Ge}_x$ channel is dominant, though at room temperature and at higher operating voltages both Si and SiGe channels are important. We have exercised a fully integrable, low Dt process using thermal or PECVD gate oxides for the fabrication of SiGe p-channel MOSFETs. We observe significant improvement in transconductance even at room temperature using a Si/Si $_{1-x}$ Ge $_x$ channel.

ACKNOWLEDGEMENTS

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**SILICON-BASED LONG WAVELENGTH INFRARED DETECTORS
FABRICATED BY MOLECULAR BEAM EPITAXY**

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ABSTRACT

SiGe/Si heterojunction internal photoemission (HIP) long wavelength infrared (LWIR) detectors have been fabricated by molecular beam epitaxial (MBE) growth of p^+ SiGe layers on p -type Si substrates. The SiGe/Si HIP detector offers a tailorable spectral response in the long wavelength infrared regime by varying the SiGe/Si heterojunction barrier. Degenerately doped p^+ SiGe layers were grown by MBE using either HBO_2 or elemental boron as the dopant source. Improved crystalline quality and lower growth temperatures were achieved for boron-doped SiGe layers as compared with the HBO_2 -doped layers. The dark current density of the boron-doped HIP detectors was found to be thermionic emission limited and was drastically reduced as compared with that of HBO_2 -doped HIP detectors. The heterojunction barrier was determined to be 0.066 eV from activation energy analysis of the HIP detectors, corresponding to a $18 \mu\text{m}$ cutoff wavelength. Photoresponse of the detectors at wavelengths ranging from 2 to $12 \mu\text{m}$ has been characterized with corresponding quantum efficiencies of 5 - 0.1%.

INTRODUCTION

Recently, we reported a new SiGe/Si heterojunction internal photoemission (HIP) IR detector which exhibits tailorable response in the long wavelength infrared (LWIR) regime [1,2]. The SiGe/Si HIP detector offers several important Si-based advantages. It can be easily integrated with Si readout circuitry either monolithically or by indium bump bonding to form large uniform focal plane arrays (FPAs), which are required for a variety of space and defense applications. The HIP detector consists of a degenerately doped p^+ -SiGe layer as the emitter and a p -type Si substrate as the collector. The band diagram of the HIP detector is shown in Fig. 1. The detection mechanism involves infrared absorption of the incident photons in the p^+ -SiGe emitter followed by internal photoemission of photoexcited holes over the SiGe/Si heterojunction barrier into the Si substrate. Strong infrared absorption is achieved by degenerately doping the p -type SiGe layer through free carrier absorption and intraband transitions [3]. The spectral response of the HIP detector can be tailored by adjusting the Ge ratio in the SiGe layer to vary the heterojunction barrier, and consequently, vary the detector cutoff wavelength.

HBO_2 was used as boron dopant source for the growth of boron-doped SiGe layers of the previously reported HIP detectors [1,2]. The advantage of using HBO_2 as the boron dopant source is that its relatively high vapor pressure allows the use of a conventional Knudsen cell to evaporate the required high dopant flux. [4,5] The doping mechanism for HBO_2 involves an initial reaction with the Si surface to form elemental boron and silicon dioxide, followed by subsequent removal of the incorporated oxygen by reaction of silicon dioxide with silicon to form volatile SiO.

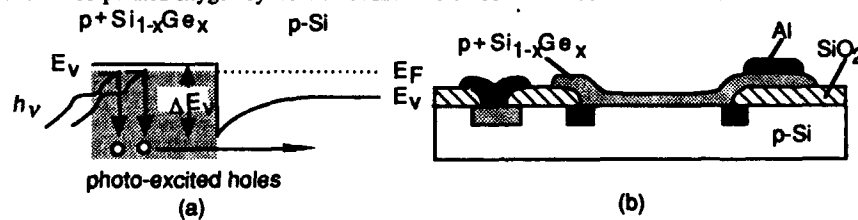


Figure 1. (a) Energy band diagram of the p^+ -SiGe/ p -Si HIP detector.
(b) Schematic cross-section of the p^+ -SiGe/ p -Si HIP test device.

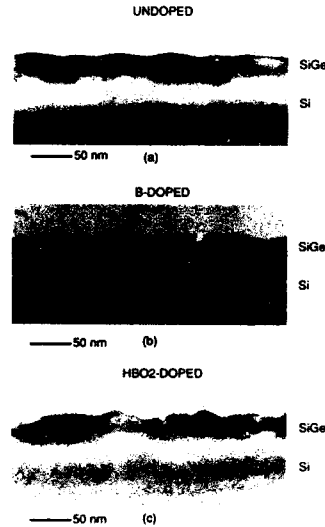


Figure 2. Cross-sectional TEM micrographs of 25-nm-thick undoped (a), B-doped (b) and HBO₂-doped (c) Si_{0.7}Ge_{0.3} layers grown by MBE at 500°C.

Relatively high growth temperatures are required for these reactions: 500 °C for the initial reaction to form elemental boron and 650°C for the removal of oxygen. Boron concentrations of $1 - 4 \times 10^{20} \text{ cm}^{-3}$ have been achieved in HBO₂-doped SiGe layers MBE grown at 500-600°C. Strong infrared absorption has been achieved in these degenerately doped SiGe layers (>20% absorption at 10 μm for a 30-nm-thick Si_{0.7}Ge_{0.3} layer) and QEs of 3-5 % in the 8-12 μm range have been measured for HIP detectors with -1.5V bias at 20K[2]. However, the use of HBO₂ at growth temperatures of 500-600 °C introduces a high level of oxygen contamination in the SiGe layers. Furthermore, the lower growth temperature (< 500°C) required for good crystal quality prevents the use of HBO₂ as the boron source due to its incomplete reaction with Si to form elemental boron. In this study, we report the SiGe HIP detectors fabricated by MBE growth of p⁺ SiGe layers using elemental boron evaporated from a high-temperature Knudsen cell.

EXPERIMENTAL PROCEDURE

The HIP detectors were fabricated by MBE growth of SiGe layers on patterned Si wafers with a resistivity of 30 Ω-cm. The wafers were oxidized, patterned, and implanted to provide p⁺ contact regions and incorporate n-type guard rings to minimize edge leakage current. After the oxide in the active detector areas and portions of the wafer surface to be used for later material studies was removed by chemical etching, the wafers were cleaned using the "spin-clean" method, which involves the removal of a chemically grown surface oxide using an HF/ethanol solution in a nitrogen glove box [6]. The p⁺-SiGe layers were grown in a commercial Riber EVA 32 Si MBE system at growth temperatures of 350 - 550 °C. Ge and Si were co-evaporated from two electron gun sources. The growth rate ranges from 0.5 to 1.0 Å/s, using HBO₂ or B as the dopant source. The fabrication of HIP detectors was completed by patterning the SiGe layers and metallization. The HIP detectors were characterized using current-voltage measurements and photoresponse measurements. The SiGe layers were characterized by transmission electron microscopy (TEM) and Fourier Transform Infrared Spectrometer (FTIR). Both plan-view and cross-section TEM was performed. The samples were prepared by mechanical thinning using dimpling, followed by argon ion beam sputtering to achieve electron transparency.

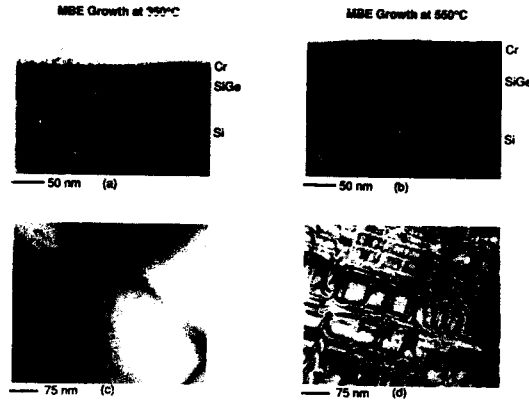


Figure 3. Cross-sectional and plan-view TEM micrographs of two $\text{Si}_{0.7}\text{Ge}_{0.3}$ layers MBE grown at 350 °C (a & c) and 550 °C (b & d).

RESULTS AND DISCUSSION

Figure 2 shows the cross-sectional TEM micrographs of 25-nm-thick undoped (sample A), B-doped (sample B) and HBO_2 -doped (sample C) $\text{Si}_{0.7}\text{Ge}_{0.3}$ layers grown by MBE at 500 °C. The boron concentration is $2 \times 10^{20} \text{ cm}^{-3}$ for sample B and sample C. The crystalline quality is similar for the undoped sample and the B-doped sample, both exhibiting a sharp SiGe/Si interface. The wavy surface of these two samples results mainly from the relatively high (500 °C) growth temperature. The quality of the HBO_2 -doped sample is significantly worse than that of the undoped and the B-doped samples. It has a high defect density ($2 \times 10^{10} \text{ cm}^{-2}$) and a very rough surface morphology. At the high growth temperature, a high level of oxygen contamination and an incomplete reaction of HBO_2 with Si is expected [4]. The poor crystalline quality of the HBO_2 -doped sample and the low growth temperature requirement for improved SiGe surface morphology make the use of HBO_2 undesirable as the boron dopant source.

The surface morphology and the crystalline quality of SiGe layers are improved significantly when the growth temperature is lowered. The cross-sectional and plan-view TEM micrographs of two SiGe layers: sample D grown at 350 °C and sample E at 550 °C, are shown in Fig. 3. Both samples are boron-doped with $[\text{B}] = 5 \times 10^{20} \text{ cm}^{-3}$ and the growth rate is 0.5 Å/s. The lower growth temperature of sample D minimizes the islanding tendency and strain relaxation of the SiGe layer, resulting in a good surface morphology and a low misfit dislocation density ($1.5 \times 10^4 \text{ cm}^{-1}$ compared to $1 \times 10^5 \text{ cm}^{-1}$ for sample E).

The infrared absorption of the degenerately doped SiGe layers was characterized by FTIR. The transmission, reflection, and absorption spectra of sample D, which has a SiGe thickness of 45 nm and a boron doping concentration of $5 \times 10^{20} \text{ cm}^{-3}$, is shown in Fig. 4a. With this high boron doping concentration, a strong infrared absorption (40 - 60 % at 3-20 μm) is achieved. The theoretical absorption in a thin layer of p⁺-type SiGe on a Si substrate, with contributions from both the intraband transition and the free-carrier absorption, is shown in Fig. 4b. The absorption is calculated from the complex dielectric constant of the SiGe layer by matching electric and magnetic fields at the interfaces[7]. The dielectric constant of the layer is derived from the frequency-dependent conductivity, which is a sum of the free-carrier and intervalence band conductivity. The free-carrier conductivity is derived by semiclassical transport theory; for simplicity, a one-band model is used. The carrier concentration is estimated from the doping level, whereas the relaxation time is an adjustable parameter. The intervalence band conductivity is derived using k-p perturbation theory for the energy bands and transition rates[8].

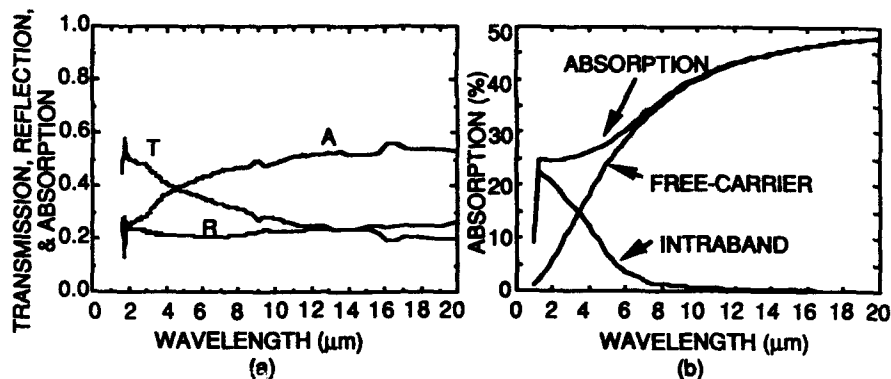


Figure 4. (a) Transmission (T), reflection (R) and absorption (A) of a 45-nm-thick boron-doped $\text{Si}_{0.7}\text{Ge}_{0.3}$ layer with a boron doping concentration [B] of $5 \times 10^{20} \text{ cm}^{-3}$ measured by FTIR spectrometer at 300K. (b) Theoretical absorption calculation of the p^+ -type $\text{Si}_{0.7}\text{Ge}_{0.3}$ layer, with contributions from both the intraband transition and the free-carrier absorption.

As a first approximation, the energy bands and transition rates are taken as isotropic, and the spin-orbit splitting is neglected. The valence band masses of the alloy are estimated by interpolating the values of the pure components. It is seen from Fig. 4 that at longer wavelengths free-carrier absorption is the dominant process, explaining approximately both the shape and magnitude of the observed absorption.

Infrared absorption of 22%, 31% and 49% at $10 \mu\text{m}$ are measured for boron-doped ($[B] = 5 \times 10^{20} \text{ cm}^{-3}$) $\text{Si}_{0.7}\text{Ge}_{0.3}$ layers with thicknesses of 10, 20, and 50 nm, respectively, corresponding to an absorption coefficient of $1.7 \times 10^5 \text{ cm}^{-1}$ as shown in Fig. 5. The high absorption at long wavelengths is advantageous for LWIR response.

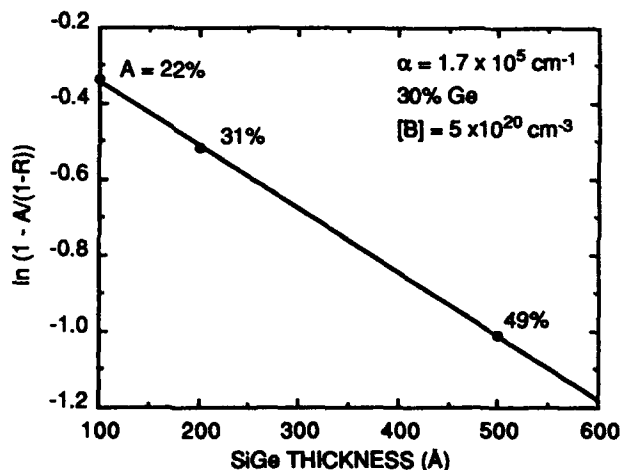


Figure 5. Infrared absorption of 22%, 31% and 49% at $10 \mu\text{m}$ measured for 10, 20, and 50 nm thick p^+ - $\text{Si}_{0.7}\text{Ge}_{0.3}$ layers, corresponding to an absorption coefficient of $1.7 \times 10^5 \text{ cm}^{-1}$.

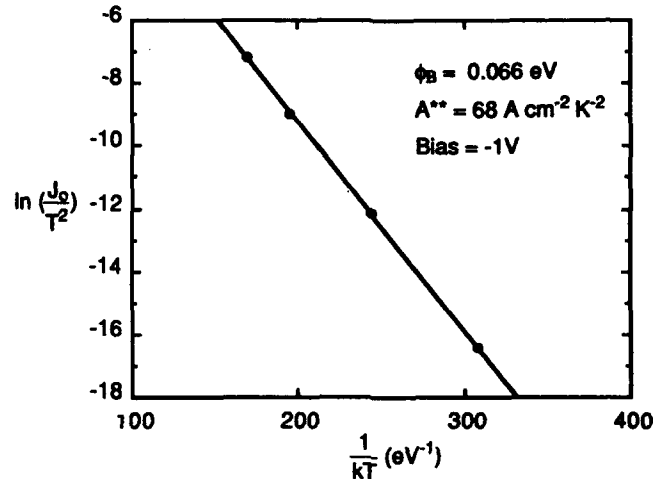


Figure 6. Activation energy analysis of a typical HIP detector with a 45-nm-thick $\text{Si}_{0.7}\text{Ge}_{0.3}$ layer.

to an absorption coefficient of $1.7 \times 10^5 \text{ cm}^{-1}$ as shown in Fig. 5. The high absorption at long wavelengths is advantageous for LWIR response.

The heterojunction barrier of the SiGe/Si HIP detectors was characterized by activation energy analysis at temperatures ranging from 30 to 70 K. The thermionic emission current density J_0 is given by:

$$J_0 = A^{**} T^2 \exp(-\phi_B/kT) \quad (1)$$

where A^{**} is the Richardson constant, T is the temperature, ϕ_B is the effective heterojunction barrier and k is Boltzmann constant. Figure 6 shows the plot of $\ln(J_0/T^2)$ vs $1/kT$ of a typical HIP detector on sample D. The active device area is $1 \times 10^{-4} \text{ cm}^2$ and the detector is biased with -1V. The heterojunction barrier height ϕ_B was determined to be 0.066 eV from the slope of the linear portion of the plot, corresponding to a 18 μm cutoff wavelength. The heterojunction barrier is lower than the valence band offset ($\sim 0.2 \text{ eV}$) between Si and SiGe with the same Ge composition because the Fermi level moves below the valence band edge due to the degenerate p-type doping concentration in the SiGe layer. The dark current density of the HIP detectors is thermionic emission limited and the Richardson constant A^{**} was determined from the ordinate intercept at $1/kT = 0$ in Fig. 6 to be $56 \text{ A/cm}^2/\text{K}^2$. The dark current density of the HIP detectors at 38K is $50 \mu\text{A/cm}^2$, which is significantly lower than that of our previous HBO_2 -doped HIP detectors.

The spectral response of HIP detectors on the same wafer (sample D) was measured with front-side illumination using a 940K blackbody source. Figure 7 shows the response of a typical SiGe HIP test device biased with -1V at 40K. No attempt was made to enhance the QE of these test devices through the use of anti-reflection coating or multiple passes (through a reflector or optical cavity). The SiGe layers of these detectors are 45 nm thick and doped with $5 \times 10^{20} \text{ cm}^{-3}$ boron. QEs of 5 - 0.1% were measured at wavelengths ranging from 2 to 12 μm .

SUMMARY

In conclusion, a p^+ -SiGe/ p -Si HIP LWIR detector approach has been demonstrated. HBO_2 and elemental boron were each studied for use as the dopant source. At a growth temperature of 500°C , poor crystalline quality and rough surface morphology were observed for the HBO_2 -doped SiGe layer. A good crystalline quality was obtained for boron-doped SiGe layers, similar to that of the undoped SiGe layer. At a lower growth temperature (300°C), the surface morphology of the boron-doped SiGe layer improves and a lower misfit dislocation density was observed. A strong

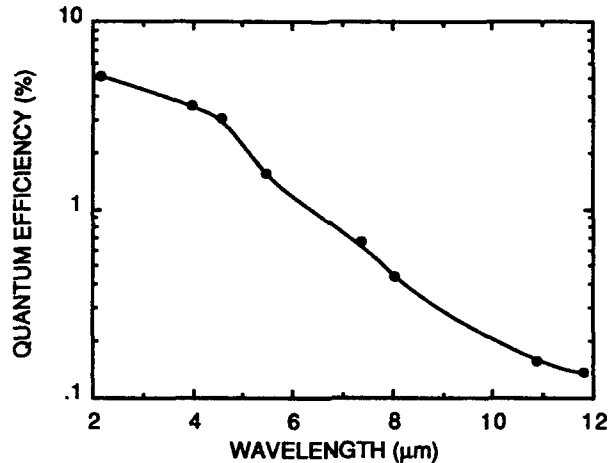


Figure 7. Photoresponse of a typical HIP detectors with a 45-nm-thick boron-doped $\text{Si}_{0.7}\text{Ge}_{0.3}$ layer with a boron concentration of $5 \times 10^{20} \text{ cm}^{-3}$.

IR absorption (40 - 60 % at 3-20 μm) was achieved for a 45-nm-thick boron-doped SiGe layer, attributed to intraband transition and free carrier absorption. A heterojunction barrier of 0.066eV, corresponding to a 18 μm cutoff wavelength, was determined from activation energy analysis of the HIP detector. Photoresponse at wavelengths from 2 to 12 μm has been measured with QEs of 5-0.1 %. By utilizing an optical cavity structure and anti-reflection coating, further improvement of the QE is expected. Finally, with mature silicon processing, our relatively simple device structure offers potential for low-cost producible arrays.

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INTEGRATED RIB WAVEGUIDE-PHOTODETECTOR USING Si/
Si_{1-x}Ge_x MULTIPLE QUANTUM WELLS FOR LONG WAVELENGTHS

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ABSTRACT

We have investigated the structural, electrical, and optical quality of epitaxial Si and Si_{1-x}Ge_x films grown by MBE on SIMOX (Separation by Implanted OXYgen) silicon substrates. Epitaxial films grown on these SOI substrates have been characterized using planar and cross-sectional TEM, high resolution X-ray diffraction, SIMS, and Seeco chemical etching to delineate defects. We have fabricated Si/SiGe P-i-N photodetectors integrated with Si waveguides on SOI for long wavelength applications. Low reverse leakage current densities were seen in these device structures. The photodetector exhibited an internal quantum efficiency of 50% at 1.1 μm with a frequency response bandwidth of 2 GHz.

INTRODUCTION

The use of silicon-germanium heterostructures permits the realization of Si-based optoelectronic detectors in the 1.3 μm wavelength regime, without the use of III-V technology. P-i-N photodetectors and avalanche photodiodes (APDs) using Si/SiGe strained layers have been fabricated by Temkin and co-workers [1, 2]. Silicon-on-Insulator (SOI) structures are useful for Si-based integrated optoelectronics since the buried oxide layer forms a low index confinement region that permits effective waveguiding in the silicon overlayer. The use of SOI thus permits the integration of active optoelectronic devices with passive waveguide elements. In order to realize these integrated device structures epitaxial growth of Si/Si_{1-x}Ge_x strained layer heterostructures on SOI substrates is required.

We have investigated the structural, electrical, and optical quality of epitaxial silicon films grown by MBE on SIMOX (Separation by Implanted OXYgen) silicon substrates. We have fabricated the first integrated Si rib waveguide-Si/SiGe P-i-N photodetector structures on SOI substrates with excellent electrical and optical characteristics. MBE and CVD epitaxial films grown on SIMOX substrates were characterized using planar and cross-sectional TEM, SIMS, and Seeco chemical etching to delineate defects. The P-i-N Si/SiGe integrated waveguide-detector exhibited low reverse leakage currents (10-30 pA/ μm^2 at 15 V reverse bias) and 50% internal quantum efficiency at 1.1 μm with an impulse response time of 200 ps.

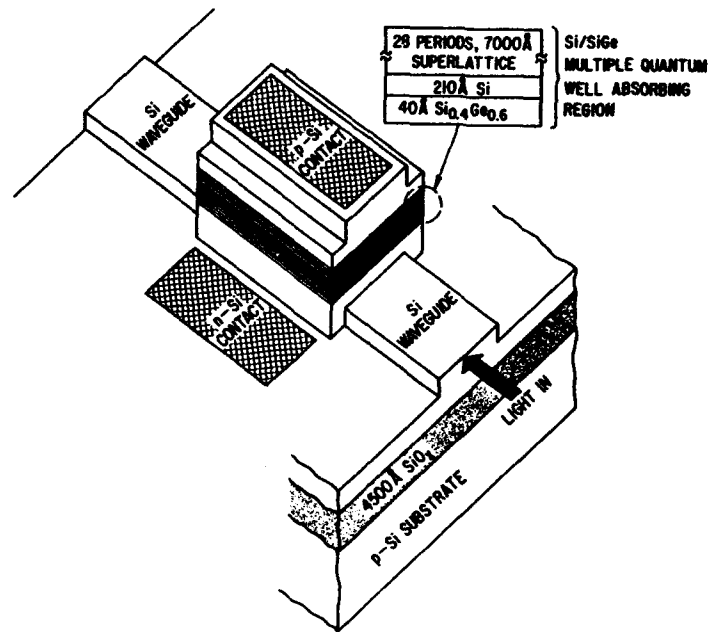


Fig. 1: Schematic view of the integrated waveguide-detector structure showing both device geometry and epitaxial layer structure.

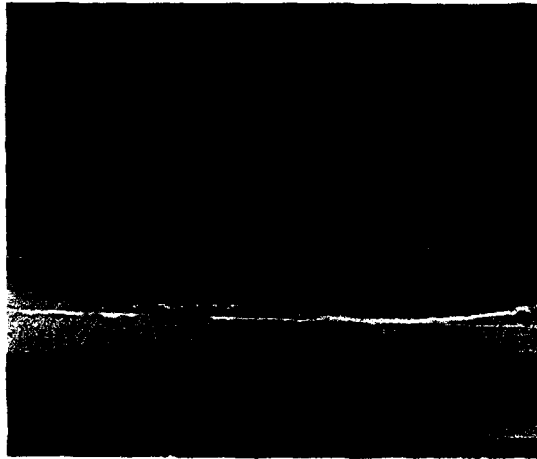


Fig. 2: TEM cross-section of the entire P-i-N Si/SiGe structure grown on SIMOX.

EXPERIMENT AND RESULTS

The SIMOX substrates used in these experiments employed a three stage implant/anneal cycle resulting in an integrated dose of 1.8×10^{14} ions/cm² at 200 KeV with a total anneal cycle of 6 hrs. at 1300°C. This results in a 4000Å SiO₂ layer buried 2000Å beneath the top silicon surface of the substrate. The defect density in the virgin SIMOX wafers was determined using the Seeco etch [3] (2:1 HF:K₂Cr₂O₇(0.15M)). A defect density of 2.5×10^3 /cm² was seen in the silicon overlayer after etching. High resolution TEM cross-sections of the Si/SiO₂ top interface show the Si overlayer to be defect free (below TEM resolution) and atomic fringes in the film point to its good structural quality. Thick ($\approx 1 \mu\text{m}$) nominally undoped epitaxial Si films were grown on these SIMOX substrates by MBE and high temperature (1050°C) conventional CVD. Defect densities in both the MBE grown and CVD grown Si were found to be around 10^3 /cm², suggesting that these defects originate from the SIMOX substrate.

Si/SiGe P-i-N integrated rib waveguide-detector structures were grown on SIMOX substrates by MBE. The undoped Si waveguide layer was grown at 650°C after which the substrate temperature was dropped to 375°C for the growth of the Si/SiGe multilayer structure. The substrate temperature was raised back to 450°C for the growth of the p⁺ contact layer. The device geometry consisted of a nominally undoped, Si/Si_{1-x}Ge_x multiple quantum well absorbing region, with Si p- and n-doped cladding layers on either side, grown on a Si waveguide structure (see Fig. 1). The absorbing region consisted of a 40Å Si_{0.4}Ge_{0.6}/180Å Si, 28 period, superlattice.

Cross-sectional TEM showed the structural and interface quality of the complete device structure to be excellent (see Fig. 2). The effective Ge concentration in the Si/SiGe layers and the doping concentration in the contact layers were determined by RBS and SIMS respectively. For comparison, the identical Si/SiGe multilayer structures were also grown on Si substrates. (400) HRXRD rocking curves for the Si/SiGe superlattice grown on Si show satellite peaks with a FWHM of 30 arcsecs, while those grown on SIMOX have a FWHM of 100 arcsecs. The waveguide-detector structure (see Fig. 1) was fabricated using conventional silicon fabrication techniques-- RIE etched mesas, PECVD oxide passivation, and Ti/Al contacts. For comparison, P-i-N detectors were fabricated on both Si and SIMOX substrates. I-V characteristics measured on large area devices grown on SOI, and ranging from 100μm x 100μm to 260μm x 260μm, showed low reverse-leakage current densities. At 5 V and 15 V reverse bias, the leakage current density was 1-3 pA/μm² and 10-30 pA/μm² respectively, with a reverse breakdown voltage of 35-40 V (see Fig. 3).

Optical measurements were made by coupling light both directly into the Si/SiGe absorbing region and into the silicon waveguide, remote from the detector active area. In separate experiments, optical waveguides 30μm x 1μm x 1mm were fabricated in 1 μm epitaxial Si films grown on SOI. These waveguides exhibited low attenuation losses of 2-3 dB/cm at 1.3 μm. The P-i-N detectors with an active device area of 930 μm x 30 μm exhibited an internal quantum efficiency of 50% at 1.1 μm (external quantum efficiency of 12%) at 10 V reverse bias. The

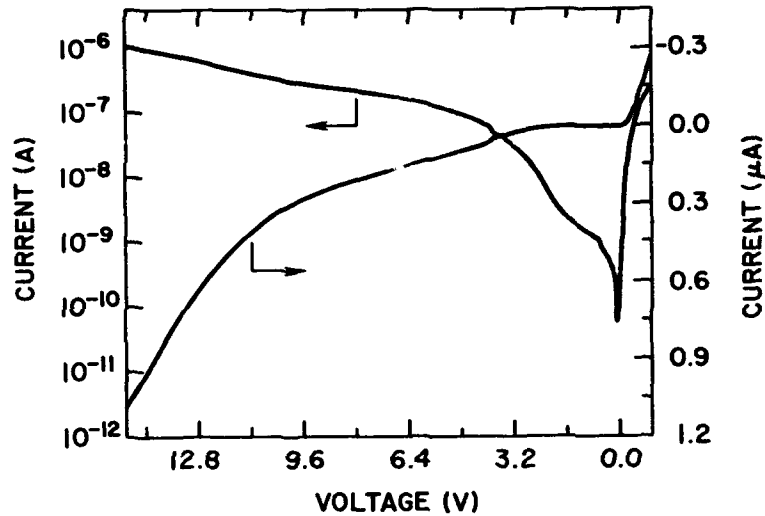


Fig. 3: Logarithmic (left vertical axis) and linear (right vertical axis) dc I-V characteristics of the Si/SiGe p-i-n detector fabricated on SOI with an on-chip device area of $260 \mu\text{m} \times 260 \mu\text{m}$. The reverse leakage current density at 15 V reverse bias is $16 \text{ pA}/\mu\text{m}^2$.

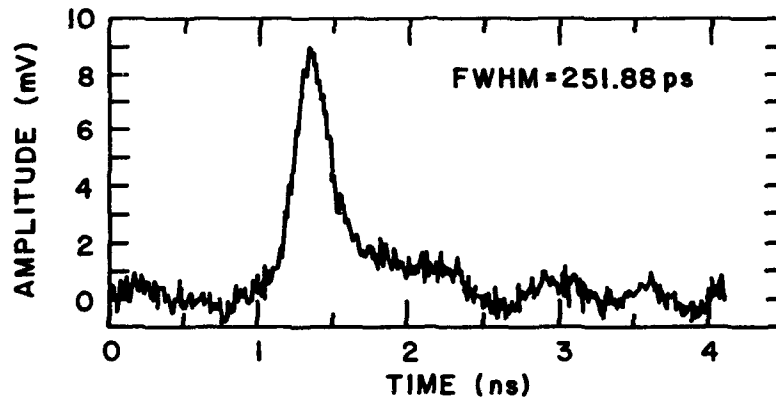


Fig. 4: Device impulse response when illuminated by 100 ps pulses from a $1.3 \mu\text{m}$ Nd:YAG laser at 10 V reverse bias by coupling evanescently through the Si waveguide. The full width half maximum of the impulse response is 250 ps.

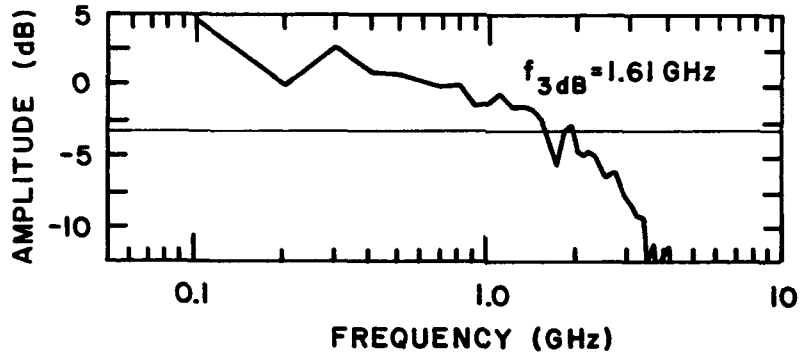


Fig. 5: Response as a function of frequency for the Si/SiGe photodetector. The frequency corresponding to a 3dB response roll-off is 1.6-2.0 GHz.

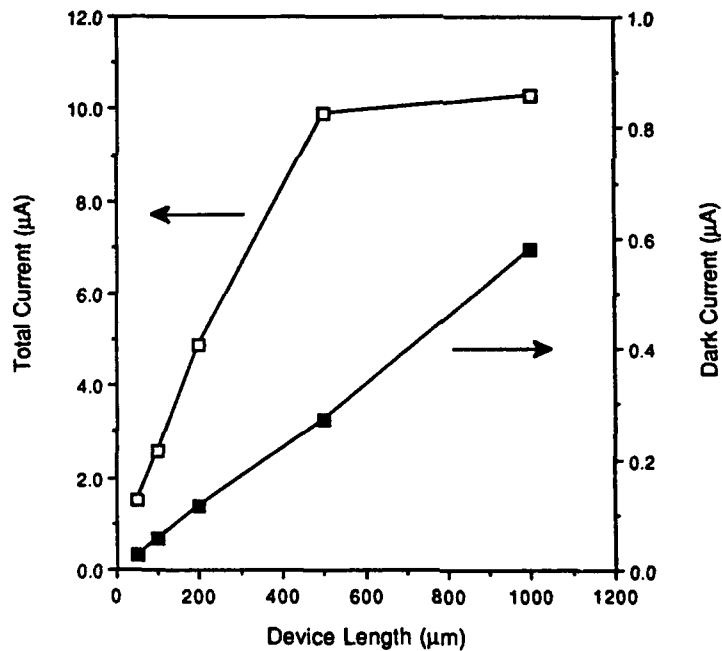


Fig. 6: External device current (photocurrent+dark) and dark current as a function of device length for a 20 μm wide device at 10V reverse bias at 1.3 μm.

impulse response time (full width half maximum) of the detector when illuminated by 70 ps pulses at 1.06 μm and 100 ps pulses at 1.3 μm by butt-coupling the fiber to the active region of the photodetector was 200 ps. The impulse response time when coupling evanescently through the Si waveguide at 1.3 μm was 250 ps (see Figs. 4 and 5). The speed of the detector appears to be limited by the RC time constant of the device. Fig. 6 shows the total current and dark current of the detector as a function of device length for a 20 μm wide device at 10 V reverse bias at 1.3 μm . The photodetector exhibited a peak spectral response at 1.06 μm at room temperature in good agreement with calculated transition energies between confined light hole valence band states to four fold electron conduction band states in the Si/SiGe multiple quantum well structure. The peak response of the detector is hence tunable by varying the physical parameters of the multiple quantum well structure. The dc electrical and optical characteristics, i.e., reverse leakage current, quantum efficiency, and speed are the best reported so far for Si/SiGe p-i-n detectors.

CONCLUSIONS

We have investigated the structural, electrical, and optical quality of epitaxial Si and $\text{Si}_{1-x}\text{Ge}_x$ films grown by MBE on SIMOX (Separation by IMplanted OXygen) silicon substrates. We have fabricated Si/Si $_{1-x}$ Ge $_x$ integrated rib waveguide-photodetectors for long wavelength applications. Low reverse leakage current densities were seen in these device structures. The detector exhibited 50% internal quantum efficiency at 1.1 μm with an impulse response time of 200 ps. Our results show promise for an integrated preamplifier/detector for an all Si-based long wavelength receiver.

ACKNOWLEDGEMENT

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SIMULATIONS OF Ge⁺ AND C⁺ IMPLANTATIONS TO FORM SiGe/Si HBT AND CHARACTERIZATION OF SiGe AND SiGeC DIODES

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ABSTRACT

Simulations of Ge⁺ and C⁺ implantations in Si were performed to study bandgap grading in the SiGeC/Si heterojunction bipolar transistor (HBT). Although no bandgap discontinuity was observed at the base-emitter junction, it was found that a wide-bandgap emitter and a narrow-bandgap base with proper bandgap grading were obtainable with implantation. Electrical characterization of SiGe and SiGeC diodes formed by Ge⁺ and C⁺ implantations in Si was carried out. Current-voltage (I-V) measurement results confirm that carbon doping improves the crystalline quality of the germanium-implanted layer. On the other hand, capacitance-voltage (C-V) measurements indicate that both germanium and carbon implantations result in considerable dopant deactivation.

INTRODUCTION

Recently, studies on the fabrication of SiGe/Si heterojunction bipolar transistors with epitaxially grown SiGe base have been reported [1-2]. Alternatively, SiGe can be formed by germanium ion implantation into silicon and subsequent solid phase epitaxy (SPE) [3]. Ion implantation is a technique convenient for selective SiGe growth, and is highly compatible with standard silicon technology. Hence it is advantageous over the various epitaxial processes. It has also been reported that carbon ion implantation into a germanium-implanted SiGe layer improves its crystallinity and the junction properties of p-n diodes fabricated in this layer [3]. The purpose of this study is to optimize the use of carbon for HBT fabrication and to perform additional electrical measurements on the p-n diodes fabricated in the SiGeC layer.

Being isoelectronic with both Si and Ge, substitutional C is not a dopant. Also, with a tetrahedral covalent radius of 0.77 Å, C is the only element in Group IV having a covalent radius smaller than that of Si (1.17 Å) [4]. This makes it ideal for the compensation of the lattice strain caused by the implanted Ge (1.22 Å) in Si. It follows from empirical consideration that an alloy consisting of Si, Ge, and C can be formed with the Si lattice parameter. This alloy has an approximate Ge to C ratio of 8:1 [4]. Furthermore, carbon in the diamond form has a much wider bandgap (5.6 eV) compared to both Si (1.12 eV) and Ge (0.66 eV). Thus it can be used to yield a wide-bandgap emitter in a HBT. To explore this possibility, simulations of Ge⁺ and C⁺ implantations into Si were performed and based on the results, bandgap profiles were obtained. Our results show that proper bandgap grading is obtainable in both the emitter and base regions but bandgap discontinuity at the base-emitter junction is not evident.

BANDGAP PROFILE SIMULATION

The aim of this study was to derive from simulations the implant parameters necessary to yield a bandgap versus depth profile as shown in Figure 1. Toward this end, different implant schemes, such as multiple Ge⁺ implants and implanting through a thick layer of oxide, were attempted. The simulation tool used was the commercially available program Profile Code [5]. The particle distributions in this code are calculated using up to 4 moments [6-8]. Based on empirical measurements, it also performs sputtering calculations for elemental solids [9]. To simulate solid phase epitaxy, the one-dimensional diffusion equation is solved assuming that the diffusion coefficient is temperature-dependent but independent of concentration [10]. To check the validity of this assumption, simulated and SIMS profiles of pre- and post-anneal Ge were compared and good agreements were obtained.

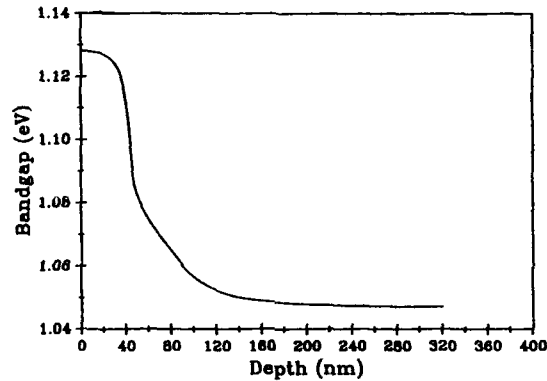


Figure 1. Desired bandgap profile.

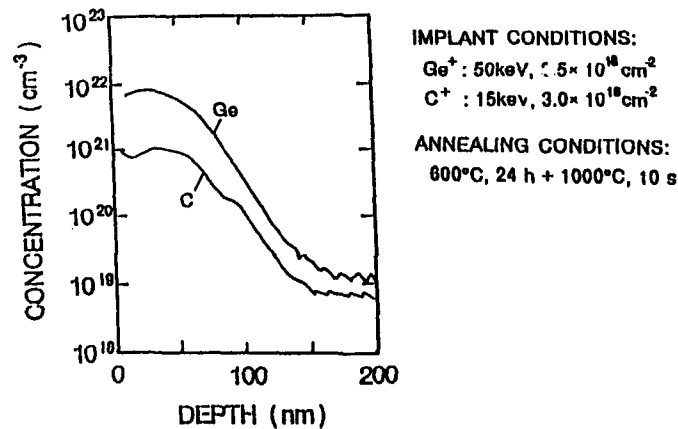


Figure 2. SIMS profiles of the implanted Ge and C concentrations in Si.

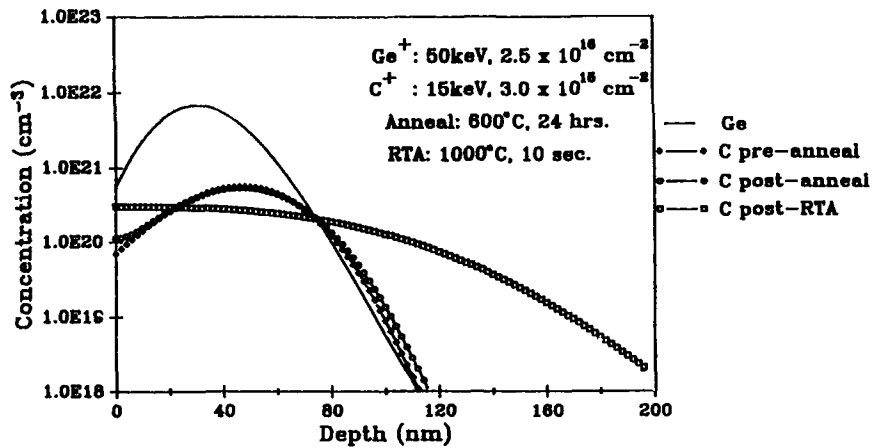


Figure 3. Simulated Ge and C profiles for comparison with the SIMS profiles.

Figure 2 shows the SIMS profiles of the implanted Ge and C concentrations in a Si (100) wafer [3]. Figure 3 shows the pre- and post-anneal simulated profiles using the same implant and anneal conditions. As seen from the simulated results, the Ge profile is unaffected by both the ordinary anneal and the rapid thermal anneal (RTA) conditions of 600°C, 24 hrs and 1000°C, 10 s respectively. The C profile shows little change after ordinary anneal but spreads out considerably upon RTA. The projected ranges and the peak concentrations for the Ge and pre-RTA C profiles are similar to the SIMS profiles. The difference between the SIMS and the simulated post-RTA C profiles can be attributed to cubic SiC island formation in the region near the projected range during the first anneal cycle [4]. These islands, being made up of tightly bound Si-C bonds, are not

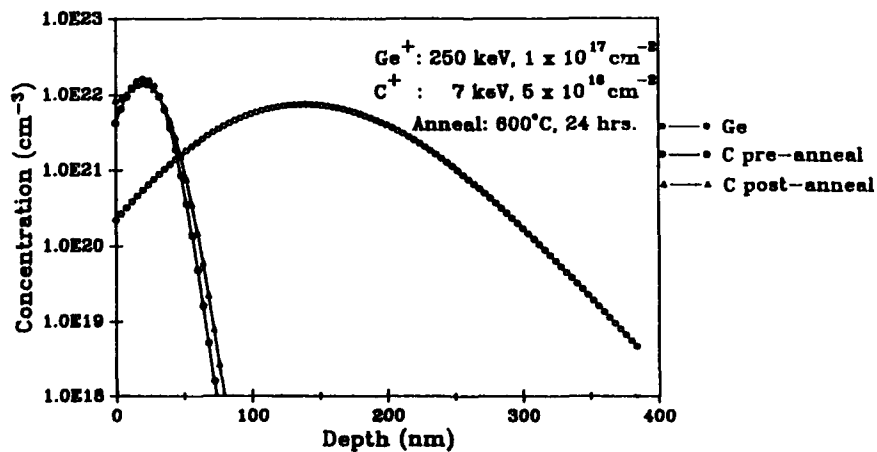


Figure 4. Optimized Simulated Ge and C profiles.

affected by the subsequent RTA.

Figure 4 shows the optimized simulated Ge and C profiles. These profiles were obtained from single energy Ge⁺ and C⁺ implants directly into Si as multiple Ge⁺ implantations resulted in a large sputtering of the Si substrate. The implant energy and doses are 250 keV and 1x10¹⁷ /cm² for Ge, and 7 keV and 5x10¹⁶ /cm² for C. Annealing is performed at 600°C for 24 hrs. Under these conditions, 563 Å of the Si substrate is sputtered off. Figure 5 summarizes results of bandgap calculations based on the simulated profiles, assuming that all implanted ions are substitutional. The bandgap is calculated using the linear relationship

$$E_g(\text{Si}_{1-a-b}\text{Ge}_a\text{C}_b) = aE_g(\text{Ge}) + bE_g(\beta\text{-SiC}) + (1-a-2b)E_g(\text{Si}) \quad (1)$$

For an emitter width of 40 nm and a base width of 60 nm, the E_g profile reveals that a desirable bandgap grading exists in the base region. However, no bandgap discontinuity results across the emitter-base junction.

ELECTRICAL CHARACTERIZATION OF DIODES

To elucidate the roles of Ge and C, electrical characterization of SiGe and SiGeC diodes formed by Ge⁺ and C⁺ implantations have been carried out. Figure 6 shows a schematic of the device geometry. Local or selective Ge⁺ implantation was performed at an energy of 120 keV with a dose of 5x10¹⁶ /cm² in a p-type Si (100) substrate. C⁺ implantation was subsequently carried out at 33 keV with 6.25x10¹⁵ ions/cm². These samples were then annealed in a N₂ ambient at 600°C for 16 hrs to grow the SiGeC layer. Boron ions were then implanted at 20 keV with 7x10¹³ /cm² followed by an arsenic ion implant through a 200 nm poly-Si layer at 80 keV with 1.5x10¹⁶ /cm². The samples were then annealed at 950°C for 10 minutes to yield planar n⁺-p⁺ diodes.

Current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed on samples fabricated with different anneal times and carbon doses. Measurements were also performed on diodes having different device areas. The I-V measurements reproduced the results of an earlier study [3], confirming that C doping improves the crystalline quality of the Ge⁺ implanted SiGe layer by reducing the surface defects. The

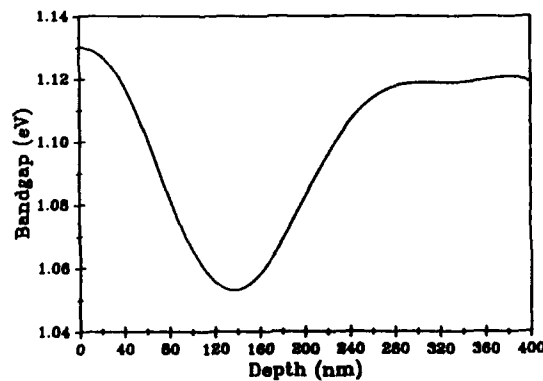


Figure 5. Bandgap profile obtained using simulation results.

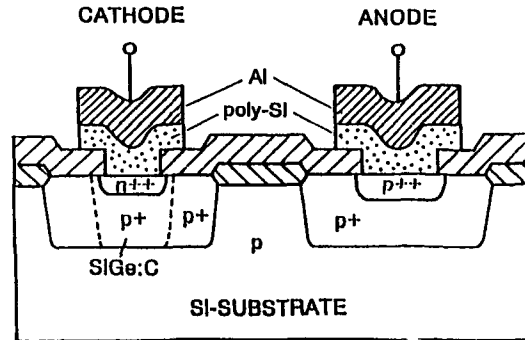


Figure 6. Schematic cross-section of the SiGe or SiGeC n^{++} - p^{+} junction.

C-V measurements indicated that there was no frequency dependence in the frequency range 10kHz - 1MHz. Figure 7 shows a comparison of the C-V results at 100 kHz for the Si, SiGe, and SiGeC devices. The Si diode is fabricated with the same process but without the Ge^{+} and C^{+} implantations. The reverse-biased characteristics of the SiGe and SiGeC diodes exhibit considerably smaller junction capacitances than that of the Si diode. Assuming that the differences in permittivities are small, the depletion widths of the SiGe and SiGeC diodes are therefore larger than that of the Si diode. This implies that the net doping is reduced by Ge^{+} and C^{+} implantations. This reduction can be attributed to the presence of large numbers of electrically inactive boron ions and/or dopant compensation created by defects related to Ge^{+} and C^{+} implantations. It can also be caused by defect-assisted out-diffusion of boron atoms into the n^{++} and poly regions. This net dopant reduction is particularly prominent in the SiGeC diode, where the capacitance at a reverse bias of 0.5 V is about 80% of that of the SiGe diode, and about 40% of the Si diode. At reverse biases larger than 1 V, the difference between SiGe and SiGeC diode capacitances is negligible. This behavior is consistent with the fact that the C concentration and range are considerably less than those of Ge (see Figure 2).

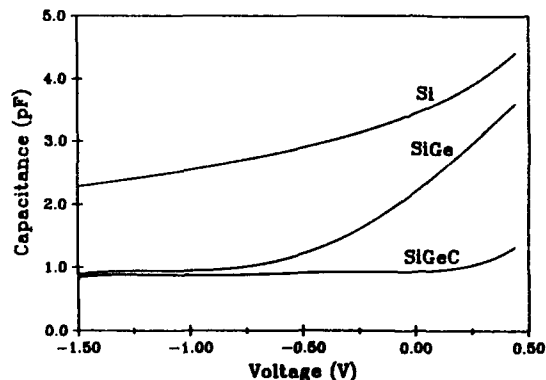


Figure 7. Comparison of diode capacitance-voltage characteristics at 100 kHz. Capacitor area = $30 \times 30 \mu m^2$.

CONCLUSION

It is found that the use of carbon in the fabrication of SiGe/Si heterojunction bipolar transistors has mixed blessings. On one hand, it is confirmed that carbon doping reduces surface defects caused by Ge^+ implantation into Si and that it can be used for bandgap engineering in the fabrication of HBTs. On the other hand, C-V data reveal that C^+ implantation results in further deactivation of boron in the base region.

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PART VII

Epitaxial Metals and Insulators

FABRICATION OF CoSi_2 GATE SI PERMEABLE BASE TRANSISTOR USING SI-MBE

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ABSTRACT

A permeable base transistor (PBT) with submicron grating is fabricated using a Si/ CoSi_2 /Si double heterostructure. The high-quality Si/ CoSi_2 /Si double heterostructure is formed by two-step molecular beam epitaxy (i.e. low-temperature MBE and successive high-temperature MBE). The Si and CoSi_2 interfaces observed by a cross-sectional transmission electron microscope are smooth and atomically abrupt. A new method of patterning CoSi_2 films is developed. This method uses the difference in surface energies between different crystal orientations. The mutual conductance and cutoff frequency of the PBT are 50 mS/mm and 6 GHz, respectively. These agree with the results of computer simulations. In addition, computer simulations indicate a potential of Si PBT for high frequency application, and a cutoff frequency as high as 90 GHz can be obtained by optimizing the device structure.

INTRODUCTION

In recent years, there has been considerable interest in introducing new heterostructures into Si transistors. This structure consists of a thin crystalline silicide gate embedded in Si. It is used in devices such as metal base transistors (MBT) [1] and permeable base transistors (PBT) [2]. MBT's and PBT's may offer important microwave applications, competitive with GaAs transistors, particularly because the fabrication of these devices is totally compatible with Si LSI technology. Si PBT's using a Si/ CoSi_2 /Si structure were realized [3,4]. However, problems originating from lattice mismatch between CoSi_2 and Si have remained. That is to say, pinholes are introduced into CoSi_2 films during high-temperature growth, and high-density defects are formed in the films during low-temperature growth [5]. In addition, fine patterning of CoSi_2 , which is crucial for device fabrication, cannot be carried out easily by conventional dry etching because the Co has no volatile compound at room temperature, as required with normal etching gases. Consequently, to realize a high-performance Si PBT, some improvements in crystal growth and fine patterning methods of CoSi_2 are necessary.

In line with this, the present paper describes a recently developed two-step molecular beam epitaxy (MBE) technique for obtaining high-quality Si/ CoSi_2 /Si double heterostructures and the method for fine patterning of CoSi_2 films. In addition, fabrication of a high-performance PBT is demonstrated.

EXPERIMENTAL

Etched grooves with 0.5- μm to 3- μm lines and spaces were made on a Si(111) substrate using conventional photolithography and dry etching techniques. Samples were chemically cleaned and finally a protective thin oxide was formed on them. They were loaded into an MBE chamber with a base pressure of 2×10^{-11} Torr. Prior to crystal growth, a thin surface oxide was sublimated by heating the substrate (800°C, 5 min)[6]. Next, the temperature was lowered and CoSi_2 films were grown on Si substrates using codeposition of Co and Si at various substrate temperatures. The ratio of the Co and Si fluxes was kept constant during growth. Next a Si overlayer was grown on the CoSi_2 in the same UHV chamber. The growth rates of both CoSi_2 and Si were about 0.1 nm/sec.

The crystallinity and interface structure of CoSi_2 and Si films were examined using reflection high-energy electron diffraction (RHEED) and cross-sectional transmission electron microscopy (cross-sectional TEM), respectively. The surface morphology was investigated using a Nomarsky microscope and scanning electron microscope (SEM). In addition, the

electrical property of the Si/CoSi₂/Si heterostructure was evaluated measuring the PBT's characteristics.

Formation of Si/CoSi₂/Si Double Heterostructure

To obtain a high-quality Si/CoSi₂/Si double heterostructure, single heteroepitaxial growth (CoSi₂/Si) was first investigated under the following conditions. The ratio of Co beam to Si beam fluxes was varied from 10 at.% Co-rich to 10 at.% Si-rich, growth temperatures were varied from 300°C to 700°C, and CoSi₂ film thickness was varied from 10 nm to 50 nm. The crystallinity and surface morphology of these films were examined. Figure 1 shows the Nomarsky micrographs of CoSi₂ surfaces for film thickness of 50 nm as a function of the growth temperature and beam intensity ratio. RHEED observation revealed that all the CoSi₂ films were single crystals. However, under non-stoichiometric conditions, the films had pinholes (a few percent Co-rich) or surface roughness (a few percent Si-rich) at 400°C. Si and/or Co atoms must move under non-stoichiometric conditions to form CoSi₂, and this may cause surface roughness. However, under stoichiometric conditions, pinhole-free CoSi₂ films without surface roughness were obtained at growth temperatures even around 400°C. Above 500°C, however, the films also had pinholes. Pinholes are thought to be introduced to reduce the interface energy between Si and CoSi₂. When the film thickness of CoSi₂ was decreased, the maximum growth temperature at which a smooth surface can be obtained became higher. For example, in the case of a 10-nm-thick film, no surface roughness was detected at growth temperatures up to 500°C. Strain energy accumulating in the CoSi₂ film caused by lattice mismatch between Si and CoSi₂ depends linearly on the CoSi₂ film thickness. Therefore, to reduce strain energy in thicker films, pinholes and/or surface roughness are introduced at lower temperatures. The resistivity of smooth CoSi₂ film grown at 500°C was typically 20 - 30 μ ohm-cm. This is almost the same as that of bulk CoSi₂.

The second step in the formation of a Si/CoSi₂/Si double heterostructure is Si overgrowth on a smooth CoSi₂/Si substrate. In the experiments, Si films (20 nm) were grown at different substrate temperatures (300 ~ 500°C). RHEED and XPS measurements confirmed that all Si films were grown epitaxially without any Co segregation. Nomarsky microscope observations, however, showed surface roughness above 500°C. Therefore, during overgrowth of Si, the growth temperature had to be below 500°C. In fact, a smooth surface was obtained at a growth temperature below 500°C. However, cross-sectional TEM reveals that the Si overlayer contains structural disorders due to low-temperature growth.

To solve this problem, two-step MBE growth was examined. First, a very thin Si layer (~ 2 nm) was grown at low temperatures (300 ~ 400°C) to stabilize the surface atoms of CoSi₂. Then, a thick Si layer was grown at a higher temperature (600°C) to obtain high-quality Si layers.

Results of SEM and RHEED observations after two-step MBE indicate that the surface morphology and crystallinity of the Si/CoSi₂/Si heterostructure were sufficiently good for device application. In addition, the XPS spectrum indicated that no surface segregation of Co occurred during Si MBE. The atomic structure of the hetero-interfaces was observed by cross-sectional TEM. The lattice image, as shown in Fig.2, indicates that the upper and lower hetero-interfaces between CoSi₂ and Si were atomically abrupt and smooth. In this way, a high-quality Si/CoSi₂/Si double heterostructure was realized using two-step MBE.

Surface cleaning of Si substrate and fine patterning of CoSi₂

As mentioned in a previous section, pinholes in CoSi₂ films are thought to be introduced to a lower interface and/or strain energy between CoSi₂ and Si [4]. It has been reported that the surface energy of Si(111) is smaller than that of Si(112) [6]. Therefore, when CoSi₂ film is grown in the etched grooves of a Si(111) surface, smooth CoSi₂ films are expected to grow on the top and bottom surfaces (Si(111) surfaces). On the other hand, CoSi₂ deposited on the side walls (Si(112) surfaces) agglomerates to reduce interface energy.

To confirm this idea, grooved patterns with different line and space widths (0.5 ~ 3 μm) were formed on a Si(111) substrate. However, we have observed deformation of cleaned Si grooves by heat treatments in UHV. Figure 3 shows a cross-sectional SEM view of Si grooves after heat treatments at several temperatures. Higher temperature and longer annealing time yielded stronger deformation. This phenomenon was measured on cleaned substrates at annealing temperatures higher than 650°C. Conversely, silicon grooves covered with SiO₂

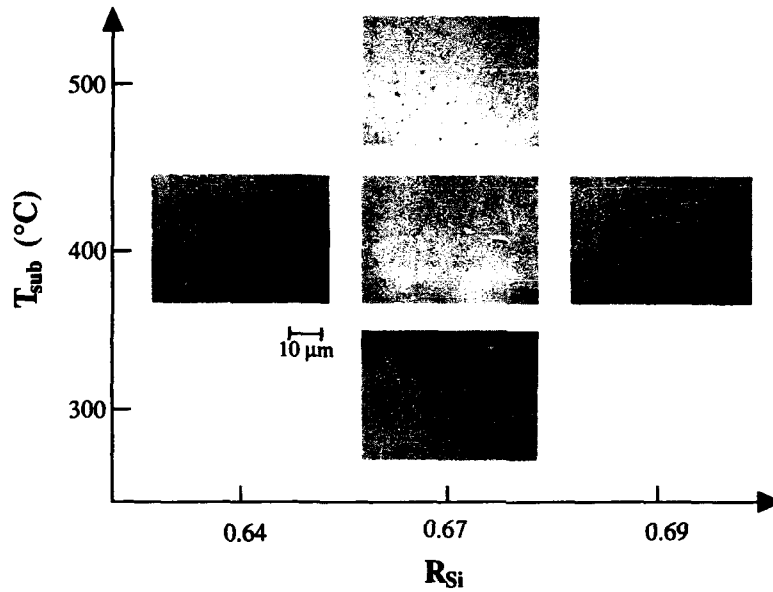


Fig.1 Influence of growth temperature (T_{sub}) and beam intensity ratio (R_{Si}) on surface morphology of CoSi_2 .

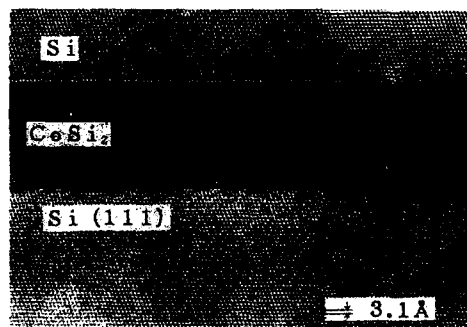


Fig.2 Cross-sectional lattice image of the $\text{Si}/\text{CoSi}_2/\text{Si}$ double heterostructure observed by TEM.

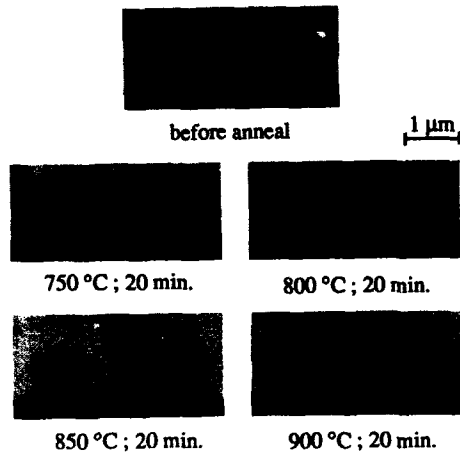


Fig.3 Cross-sectional SEM view of Si grooves after annealing in UHV.

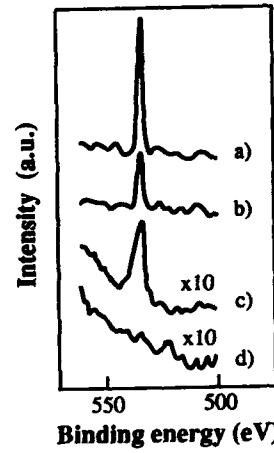


Fig.4 XPS spectra from Si wafers after each surface treatments. a), b) Oxidized wafer c), d) HF dipped wafer before and after annealing at 750 °C 5 min.

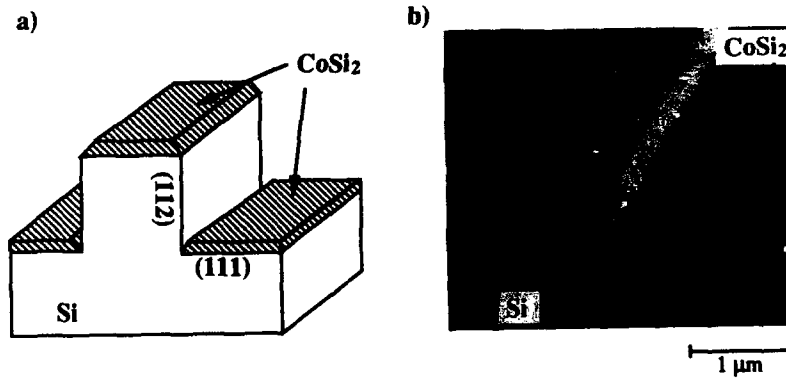


Fig.5 (a) Schematic illustration (b) SEM micrograph after CoSi₂ MBE growth on the etched grooves in Si the substrate.

films (10 nm thickness) showed no deformation. This deformation is relative to a clean Si surface and can be attributed to the surface atom migration of a large number of Si atoms and long migration distance[8].

In the pre-treatment (surface cleaning) of CoSi_2 MBE growth, thin oxide films which prevent both natural oxide formation and hydrocarbon adhesion were formed by chemical treatment (boiled in a $\text{HCl} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ mixture) on Si substrates. These films were removed by 20 minutes 780°C annealing in the MBE chamber (pressure $< 10^{-8}$ Pa) and a clean surface was obtained[6]. As a result of this procedure, Si grooves were deformed and other surfaces appeared on the sidewalls. CoSi_2 films deposited on these surfaces degraded device performance by increasing leakage current and gate capacitance. This effect was more critical for fine patterned gate.

To avoid deformation of the grooves, annealing temperatures lower than 750°C and annealing time less than 5 minutes are required. Results of X-ray photoelectron spectroscopy (XPS) measurement are shown in Fig.4a and b from the oxidized Si surface before and after annealing at 750°C , 5 min. Oxide still existed on the surface after annealing. In this process, the oxide layer had not been fully removed. Longer annealing time (20 minutes) decreased oxygen intensity, but the grooves were deformed. Therefore, in the refined process, oxide film was removed by HF solution before loading into the MBE chamber. To minimize both oxide film formation and hydrocarbon adhesion, a rapid water rinse was used after the HF dip for 2 seconds, and the Si wafer was saved in a box filled with pure N_2 gas immediately after being spun dry and loaded in the MBE chamber without air exposure. Figures 4c and d show the XPS spectra obtained before and after annealing. Before annealing, no carbon was measured, but a small amount of oxygen existed. After 750°C , 5 minutes annealing, the oxygen disappeared. In order to examine the cleanliness of this surface, CoSi_2 and Si films were grown by MBE on the surfaces obtained by this method and the low-temperature thermal etching method. There were no differences between the two methods in the crystallinity or surface morphology of grown layers. In this way, a clean surface was obtained without changing the shape of the Si grooves.

Then a 10-nm-thick film of CoSi_2 was grown at $300 \sim 600^\circ\text{C}$ on a grooved Si substrate cleaned using the above method under stoichiometric conditions. Current-voltage measurement showed that CoSi_2 films between the top and bottom surfaces were electrically connected to each other when the growth temperature was lower than 300°C . At growth temperatures higher than 400°C , they were electrically isolated from each other. This result means that CoSi_2 films were grown selectively on the top and bottom surfaces of the etched grooves. Figure 5 shows a schematic illustration and an SEM image after a CoSi_2 film was grown on the etched grooves. Thus, the patterning technique for CoSi_2 films in the submicron range was established.

Fabrication of PBT

PBTs were fabricated using the techniques described in the previous sections. In this work, n-type Si ($n=10^{16} \text{ cm}^{-3}$ and $2 \times 10^{16} \text{ cm}^{-3}$) n^+ type Si wafers were used as substrates. Here, the n^+ substrate was the drain region of the PBT. First, an n^+ -Si source region was formed by P^+ ion implantation (50 keV, $1 \times 10^{15} \text{ cm}^{-2}$) and annealing (900°C , 5 min.), (see Fig.6a). Next, grooves with $0.5 \mu\text{m}$ to $1 \mu\text{m}$ width and spacing were formed on the Si surface by dry etching (see Fig.6b). These Si grooves were cleaned by the method mentioned above, and then CoSi_2 was grown by MBE. As a result, a CoSi_2 gate electrode was formed on the bottom Si surface of the groove and a CoSi_2 source electrode was formed on the top n^+ -Si surface (see Fig.6c). Then these electrodes were buried in Si by 2-step Si MBE growth (see Fig.6d). Figures 7 and 8 show a plan view and cross-sectional SEM image of the sample, respectively. Afterwards, the Si overlayer was partially removed by dry etching to make contact regions of the gate and source CoSi_2 electrodes. Finally, Al electrodes for the gate and source were formed. The n^+ -Si substrate was used as a drain for the PBT.

The current-voltage characteristics in a common source mode shown in Fig.9 exhibited triode-like features. The highest transconductance (g_m) was 50 mS/mm. The highest unity current gain frequencies (f_T) were 4 and 6 GHz for $n=10^{16} \text{ cm}^{-3}$ and $2 \times 10^{16} \text{ cm}^{-3}$ substrates, respectively. Figure 10 shows the high-frequency response of the latter sample.

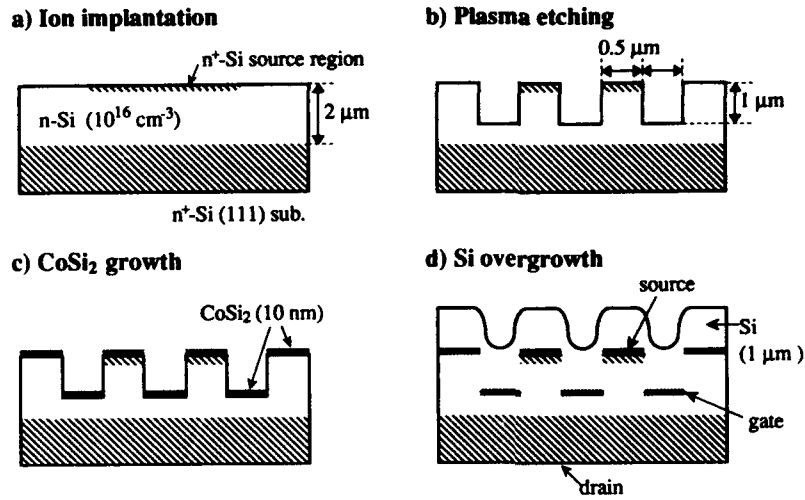


Fig.6 PBT fabrication process. Schematic cross-section of the active region.

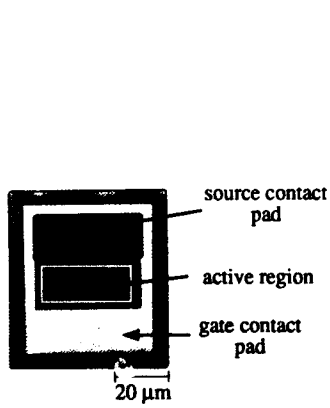


Fig.7 PBT plan view.

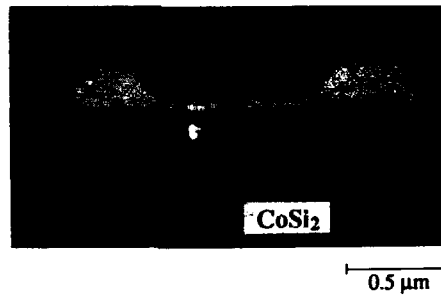
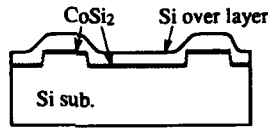


Fig.8 Cross-sectional SEM micrograph of buried CoSi₂ electrodes (10 nm) SEM observation was performed after Secco etching.

Numerical simulation

To evaluate the obtained result and to estimate the high-frequency performance of Si-PBT, 2-dimensional simulations were performed. The current flow was calculated according to the model shown in Fig. 11. The high-frequency performance was evaluated by the value of the cutoff frequency (f_T).

$$f_T = \frac{g_m}{2\pi C_{in}} \quad (1)$$

where V_G is the gate-to-source voltage. The transconductance (g_m) is calculated as

$$g_m = \frac{I(V_G+dV_G)-I(V_G)}{dV_G} \quad (2)$$

and the input capacitance (C_{in}) is calculated as

$$C_{in} = \frac{Q(V_G+dV_G)-Q(V_G)}{dV_G} \quad (3)$$

The total charge (Q), a function of gate voltage, is calculated as

$$Q(V_G) = \int n(V_G, v) dv \quad (4)$$

where n is the carrier density. Figure 12 shows the cutoff frequency dependence on the channel doping concentration. The source-to-gate distance (l_{sg}) and gate-to-drain distance (l_{gd}) were kept constant at $1 \mu\text{m}$. The channel width (d) was varied as a function of the doping concentration in order to keep the threshold voltage constant. The drain voltages were from 3 to 5 V, and the gate voltage was 0 V. The curve noted 'intrinsic' is the result from the net channel region. The cutoff frequency becomes higher at a higher doping concentration. This is because, as the doping concentration increases, the value of g_m increases due to higher channel conductivity, while the value of C_{in} does not increase due to a smaller gate region. The curve noted 'with pad' is the result for the actual device (shown in figure 7), where there is parasitic capacitance originating from the contact pad region.

Measured f_T 's of 4 GHz and 6 GHz agree with simulations at $n = 10^{16} \text{ cm}^{-3}$ and $2 \times 10^{16} \text{ cm}^{-3}$, respectively. These results indicate that the PBT fabricated here operates as well as expected, and that high-frequency performance can be improved. This improvement can be achieved by using a small parasitic capacitance structure and by using a higher doping concentration channel ($> 10^{17} \text{ cm}^{-3}$) and fine patterned gate ($< 0.3 \mu\text{m}$).

Next, the optimum source-to-gate distance (l_{sg}) and gate-to-drain distance (l_{gd}) were estimated. The channel doping concentration was kept constant at 10^{17} cm^{-3} throughout the calculations. The gate-to-drain distance (l_{gd}) was varied from $1 \mu\text{m}$ to $0.1 \mu\text{m}$. The source to gate distance (l_{sg}) was varied from $0.2 \mu\text{m}$ to $0.1 \mu\text{m}$ to obtain high g_m . In this range, l_{sg} showed little effect on the cutoff frequency. This is because, in smaller l_{sg} , g_m becomes larger since the source resistance becomes small. However, the capacitance between the gate and source becomes larger since it depends on l_{sg} . Conversely, the gate-to-drain distance (l_{gd}) showed a large effect on the cutoff frequency. This is because, as the l_{gd} becomes smaller ($< 0.2 \mu\text{m}$), the depletion region from the gate Schottky contact approaches the drain and the carrier injection effect takes place to enhance g_m . Figure 13 shows the cutoff frequency dependence on l_{gd} . As l_{gd} reaches $0.1 \mu\text{m}$, f_T becomes 60 GHz.

Smaller l_{gd} , less than $0.1 \mu\text{m}$, could result in higher f_T , however, leakage currents such as tunneling current will increase. In this dimension, the field intensity between the gate and drain approaches 10^6 V/cm which yields a soft breakdown, but the tunneling effect was not considered in these calculations. In the actual devices, a breakdown voltage is very important device parameter. Therefore, in order to estimate a very high frequency device with smaller dimensions, the breakdown voltage must be considered.

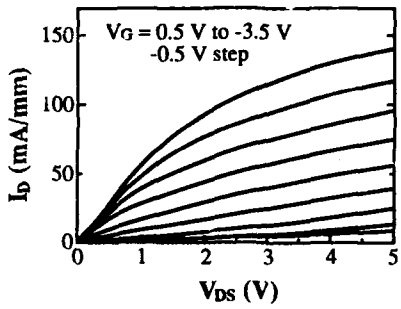


Fig.9 Current voltage characteristics of PBT. Highest g_m is 50 mS/mm.

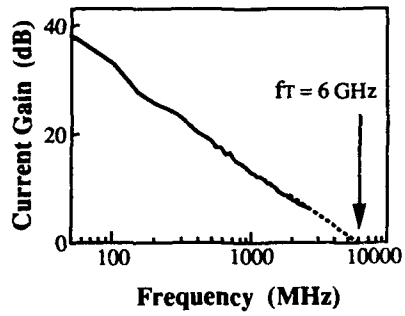


Fig.10 Current gain versus frequency.

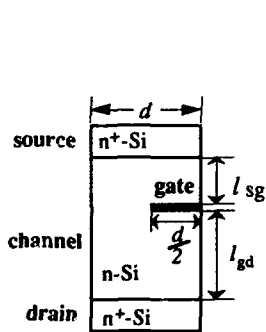


Fig.11 Model of PBT.

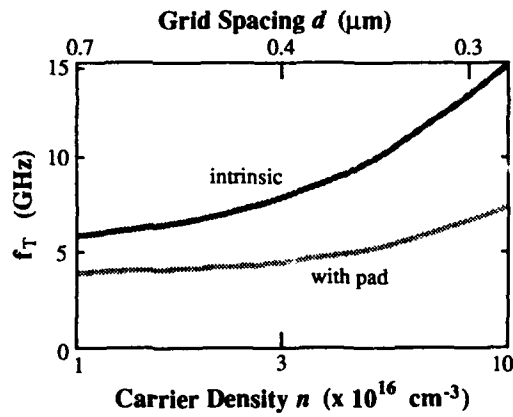


Fig.12 Cutoff frequency (f_T) dependance on Carrier Density (n).

In addition, at a very short channel length in the range of $0.1 \mu\text{m}$, the velocity overshoot effect can be expected. This effect is expected to cause a very high device performance of higher cutoff frequency. This is because, a higher electron velocity yields a larger g_m value without increasing the input capacitance. To estimate this effect, a study of the Monte Carlo simulation, where the current flow is calculated from the kinematics of electron particles, has been carried out. Also, the shown cutoff frequency can be increased from 60 to 90 GHz due to velocity overshoot.

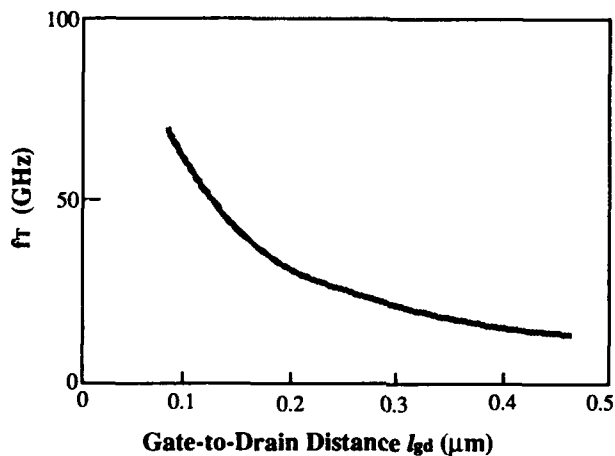


Fig. 13 Cutoff frequency (f_T) dependance on gate-to-drain distance (l_{gd}).

Conclusion

Silicon PBT's have been fabricated with a refined process. Here we have developed a two-step MBE method for formation of high-quality Si/CoSi₂/Si double heterostructures and a low-temperature surface cleaning method to solve the problem of obtaining a submicron CoSi₂ gate. Buried gate electrodes as small as $0.5 \mu\text{m}$ in width and spacing resulted in good device operation. The highest g_m was 50 mS/mm and the highest f_T was 6 GHz. Computer simulations indicate that more than one order of magnitude improvement of f_T (about 90 GHz) is possible by optimizing device structure. This can be realized by structural improvement in three areas. (1) Reduction of parasitic capacitance. This can be performed using a confined n⁺ drain region within the active region of the device. (2) Higher doping concentration channel ($1 \times 10^{17} \text{ cm}^{-3}$) and a submicron patterned gate ($< 0.3 \mu\text{m}$). (3) Short channel length, $0.1 \mu\text{m}$ of source-gate and gate-drain distance.

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SUBSURFACE GROWTH OF CoSi_2 BY DEPOSITION OF Co ON Si-CAPPED CoSi_2 SEED REGIONS

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ABSTRACT

At a growth temperature of 800°C , Co deposited on Si(111) diffuses through a Si cap and exhibits oriented growth on buried CoSi_2 grains, a process referred to as endotaxy. This occurs preferentially to surface nucleation of CoSi_2 provided the thickness of the Si cap is less than a critical value between 100 and 200 nm for a deposition rate of 0.01 nm/s. Steady-state endotaxy is modeled under the assumption that the process is controlled by Co diffusion.

INTRODUCTION

Epitaxy of CoSi_2 on Si has been actively studied for several years, and high-quality films have been grown on Si [1,2] and overgrown with epitaxial Si [3]. Several molecular beam epitaxy (MBE) techniques have been employed for the growth of CoSi_2 on Si surfaces. In addition to MBE growth of Si over CoSi_2 , ion implantation followed by annealing has been used for the growth of Si/ CoSi_2 /Si structures [4]. We have found that the growth of buried CoSi_2 is possible by deposition of Co at low rates on Si at high temperatures via diffusion of the Co through a Si cap to buried CoSi_2 seed regions. This process is referred to as "endotaxy" as it applies to oriented growth *within* a substrate rather than *upon* a substrate. A simple model of endotaxy is described in analogy to thermal oxidation of Si.

The disilicide phase of Co is stable to high temperatures and lattice matches Si to 1.2 % at room temperature. In addition, the Si sublattice of CoSi_2 occupies the same volume as the diamond Si lattice within the 1.2 % mismatch and is closely related in structure. Co diffuses interstitially in Si at very high rates, with a diffusion coefficient of $1.2 \times 10^{-5} \text{ cm}^2/\text{s}$ at 800°C [5]. The solid solubility of Co in Si at 800°C is $6.5 \times 10^{12} \text{ cm}^{-3}$ [5].

EXPERIMENTAL PROCEDURE

Two-inch diameter p-type (111)-oriented Si wafers cut on axis to within 0.5° were chemically cleaned *ex situ*, after which a protective chemical oxide was removed with an HF:ethanol solution in a dry-nitrogen glove box attached to the growth apparatus on the same

day as the growth [6]. A Riber EVA 320 molecular beam epitaxy (MBE) system equipped with separate electron-beam evaporation sources for Co and Si was used. On each sample, a 50-nm-thick silicon buffer layer was first grown at 800°C. This was followed by growth of CoSi_2 seed regions by columnar epitaxy at 800°C [7]. These seed regions consist of epitaxial silicide columns 50 nm thick and $\approx 150\text{--}200$ nm in diameter, surrounded by coplanar epitaxial Si, as seen in Fig. 1a. This seed layer was capped with continuous, single-crystal Si (Fig. 1b) of variable thickness at 650°C, leaving a 7×7 reconstructed surface. Co was deposited at 0.01 nm/s on these Si layers at 800°C. The 7×7 reconstruction largely disappears during endotaxy of Co in reflection high-energy electron diffraction patterns, though some faint indication of the reconstruction can still be seen. Substrate temperatures reported here are infrared pyrometry values.

RESULTS

For Si cap thicknesses of 40 and 100 nm, the deposited Co is observed to grow on the buried CoSi_2 columns, while for Si cap thicknesses of 200 and 400 nm large surface islands of CoSi_2 form (Fig. 2). Thus a critical thickness for endotaxy exists and under these growth conditions lies between 100 and 200 nm. The buried CoSi_2 regions grow primarily in the lateral direction. The structure of Fig. 1c and 2a consists of a nearly-continuous CoSi_2 layer

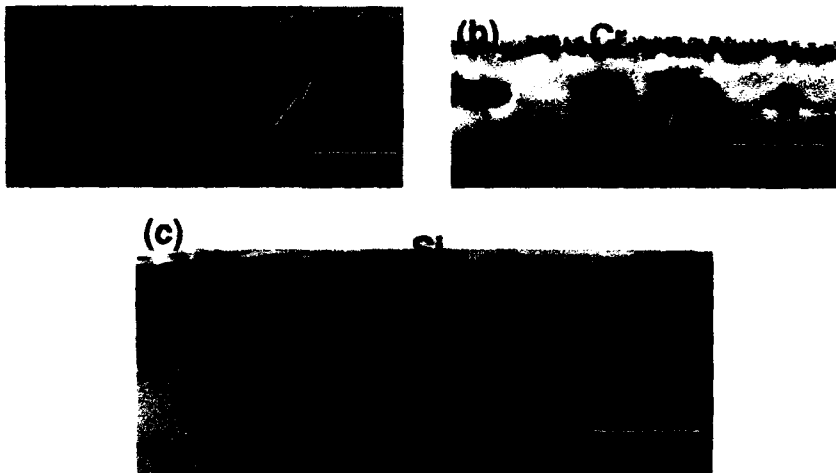


Fig. 1. Cross-sectional TEM micrographs of (a) 50-nm-thick columnar CoSi_2 seed regions grown by codeposition of 7:1 Si:Co at 800°C, (b) a "template" structure consisting of such seed regions capped with 40 nm of Si, and (c) the template structure, but with an additional 13.5 nm of Co deposited at 800°C on the Si cap. A Cr layer was deposited at room temperature on the samples shown in 1a and 1b to preserve the surface during TEM sample preparation.

capped with single-crystal silicon, though channels of silicon are still present. Note that the CoSi_2 has the usual type-B orientation with respect to the underlying Si; i.e., twinned with respect to the surface (111) plane. The Si cap orientation is the same as the substrate, since growth was seeded by the Si surrounding the columns. Thus the top CoSi_2/Si interface is also twinned, in contrast to the untwinned orientation more commonly observed for MBE growth of Si on planar CoSi_2 layers [3].

MODELING

The steady-state endotaxy process may be modeled analogously to thermal oxidation of Si [8]. In the present case, Co diffuses through Si to react with Si to form CoSi_2 , whereas in thermal oxidation O_2 (or another oxidizing species) diffuses through SiO_2 to react with the underlying Si to form SiO_2 . In steady state, the flux of Co to the wafer surface (F_1) must equal the flux of Co from the surface to the buried CoSi_2 (F_2), as shown schematically in Fig. 3a. The sticking coefficient of Co on Si is essentially unity, so the flux of Co to the wafer surface is simply the deposition rate $R = 0.01 \text{ nm/s} = 8.2 \times 10^{13} \text{ Co atoms/cm}^2/\text{s}$. The flux F_2 is that between a source and a sink of Co:

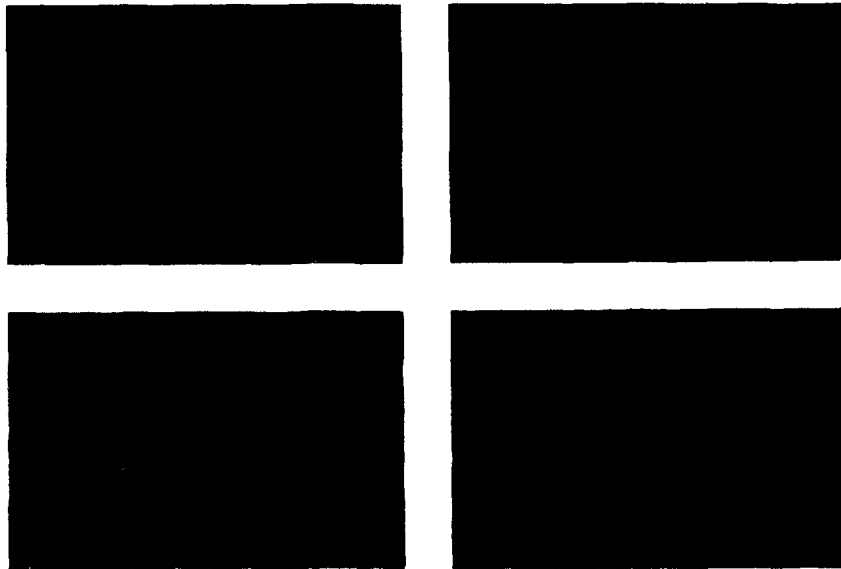


Fig. 2. SEM micrographs of samples with 13.5 nm of Co deposited at 800°C on a Si cap on a 50-nm-thick columnar CoSi_2 layer. The Si cap thicknesses were (a) 40 nm, (b) 100 nm, (c) 200 nm, and (d) 400 nm. The lighter grains in 2a (right edge) and 2b (center and top right) are surface CoSi_2 , while the medium contrast areas are buried CoSi_2 , and the darkest areas are Si.

$$F_2 = D(C_{bs} - C_{bi})/d, \quad (1)$$

where D is the bulk diffusion coefficient of Co in Si, C_{bs} is the bulk concentration of Co just below the surface, C_{bi} is the bulk concentration of Co just above the interface with the buried CoSi_2 , and d is the thickness of the Si cap. The Si just above the buried silicide grain must be supersaturated with Co for growth of CoSi_2 to occur. However, at 800°C the reaction between Si and Co proceeds very rapidly, so C_{bi} is not expected to rise much above the solid solubility limit of Co in Si (S) at 800°C . Replacing F_2 with the deposition rate R and rewriting eqn. 1 then gives

$$C_{bs} = Rd/D + S. \quad (2)$$

Since the critical value of d for endotaxy to dominate lies between 100 and 200 nm, a critical value of C_{bs} can be calculated to be $\approx 7.5 \times 10^{13}$ Co atoms/cm³. In a single monolayer, this corresponds to one Co atom every $100 \mu\text{m}^2$. This critical value comes about because C_{bs} is related to C_s , the surface concentration of Co. If C_s exceeds the critical concentration required for the formation of stable surface nuclei of CoSi_2 , endotaxy will not be the dominant process, as surface-diffusing species of Co will find attractive nucleation sites on the surface. The

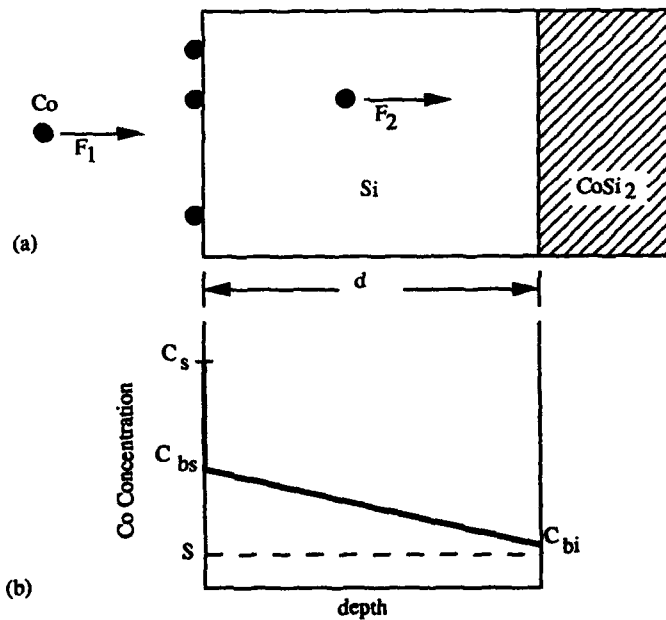


Fig. 3. Schematic diagrams showing (a) the endotaxy process, and (b) the Co concentration profile as a function of depth in the Si cap.

abrupt change in Co concentration between the surface and the bulk just under the surface is probably due to an activation energy for Co atoms to enter the bulk. The density of CoSi₂ columns in the seed region ($\approx 20/\mu\text{m}^2$) implies a much higher critical concentration of surface Co for nucleation of stable islands, suggesting a large difference between the concentration of Co on the surface and just below the surface.

The mobile Co surface species could be either Co atoms or CoSi₂ molecules (or clusters of these). If Co atoms were the migrating species, then they would react into the Si when they formed stable nuclei, leading to recessed islands. On the other hand, if Co atoms quickly pulled out Si to form molecules and migrated in this form, islands would sit on top of the Si. The latter is observed in epitaxy of CoSi₂ on Si at 800°C, suggesting that CoSi₂ molecules are the predominant mobile species [9]. The basic processes involved in endotaxy are formation and dissociation of CoSi₂ molecules on the surface, migration and formation of critical or subcritical surface nuclei, diffusion of Co in the Si capping layer, and growth of CoSi₂ on the buried CoSi₂ columns. Figure 2 shows that the transition between growth in which epitaxy is dominant versus growth in which endotaxy is dominant is quite abrupt. This is a consequence of the abruptness with which the formation of critical surface nuclei occurs.

Endotactic nucleation of CoSi₂ on CoSi₂ is similar to epitaxial nucleation of CoSi₂ on CoSi₂, differing primarily in the fact that the CoSi₂ "surface" is covered with single-crystal Si as opposed to vacuum. This changes the "surface" energy of the CoSi₂ "substrate", and also further restricts movements of the "surface" diffusing species. CoSi₂ is particularly well-suited to endotaxy because Si is not drastically displaced by growth of CoSi₂, but just shifts position slightly (as can be seen by examining the atomic structures). In the case discussed here, "homoendotaxy" of CoSi₂ on CoSi₂ has been demonstrated. "Heteroendotaxy" should also be possible, for example of NiSi₂ on CoSi₂, or between silicides with different structures.

SUMMARY

In summary, a new thin-film crystal growth mode referred to as "endotaxy" has been observed. In this process, Co deposited on a Si cap over CoSi₂ seed regions is observed to diffuse through the Si to grow on the seeds provided the cap is sufficiently thin. The process has been modeled in analogy to thermal oxidation of Si.

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OPTICAL PROPERTIES AND INTERNAL PHOTOEMISSION IN EPITAXIAL COMPOSITES OF CoSi_2 PARTICLES IN SILICON

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ABSTRACT

An analysis of optical absorption and internal photoemission in epitaxial CoSi_2 particles buried in silicon is carried out. The optical absorption is dominated by the well-known surface plasma resonance, and calculations of the surface plasma frequencies, using the previously measured dielectric constant of CoSi_2 , agree well with experiment. A model for the photoemission yield is presented which includes the effects of the surface plasmon excitation and decay. The model can reproduce the observed features of the yield in photoresponse experiments. A model for the replenishment of photoemitted carriers is also presented, in which the metal particles acquire a small steady-state charge under illumination.

INTRODUCTION

Recent work has demonstrated the fabrication of novel epitaxial structures consisting of metal silicide particles embedded in silicon[1]. One of the possible applications proposed for such structures is a Schottky-diode infrared detector employing internal photoemission out of the metal particles[2]. Such a detector is expected to have several advantages over standard infrared detectors employing metal films. One is that optical absorption can be enhanced at wavelengths of choice, through the particle-shape-dependence of the surface plasma absorption peak[2,3]. Another is that the emission of photoexcited carriers can also be increased because of the three-dimensionally confined nature of particles.[2] Several questions remain, however, about the mechanisms underlying the operation of such a detector. One is the mechanism by which charge emitted from the metal particle is replenished[2]. Another is the role played by the excitation of surface plasmons (which are collective excitations) in the emission of excited carriers (which are single-particle excitations).[2] In this paper, we present an analysis of these processes and the results of absorption and photoresponse measurements.

THE SURFACE-PLASMA RESONANCE

The dominant features in the optical absorption of small metal particles are the well-known surface-plasma-resonance peaks. These peaks occur when the frequency of light is equal to the frequency of the various surface plasma modes in the metal particle. This surface plasma frequency is strongly dependent on the shape of the particle. MBE growth techniques give precise control over the aspect ratio of the silicide particles, and therefore over the resonance peak position. If we model the silicide particles as spheroids, then the surface plasma frequencies ω_{lm} are determined by a relation of the form[4]

$$\epsilon_p(\omega_{lm}) = -\epsilon_h(\omega_{lm})F_{lm}(a_r), \quad (1)$$

where ϵ_p and ϵ_h are the dielectric constants of the metal particle and the host medium, respectively, l, m are the mode indices of the plasmon, and a_r is the aspect ratio of the particle. The factor $F_{lm}(a_r)$ can be expressed in terms of Legendre functions[4,5]. For small particles only the lowest plasmon mode will be appreciably excited. Figure 1a shows how the calculated function $F_{l=1,m=1}$ varies with the aspect ratio a_r of the spheroid, defined

as the ratio of the spheroid diameter to the spheroid height. Figure 1b illustrates how the frequency of this mode shifts downward as the aspect ratio increases. This behavior is observed in the experimental absorption curves for a series of samples of CoSi_2 particles in silicon with varying aspect ratio (Figure 1c). The absorption of the composite structure can be calculated with effective medium theories, and the results of such calculations [3,5] agree well with the observed absorption curves.

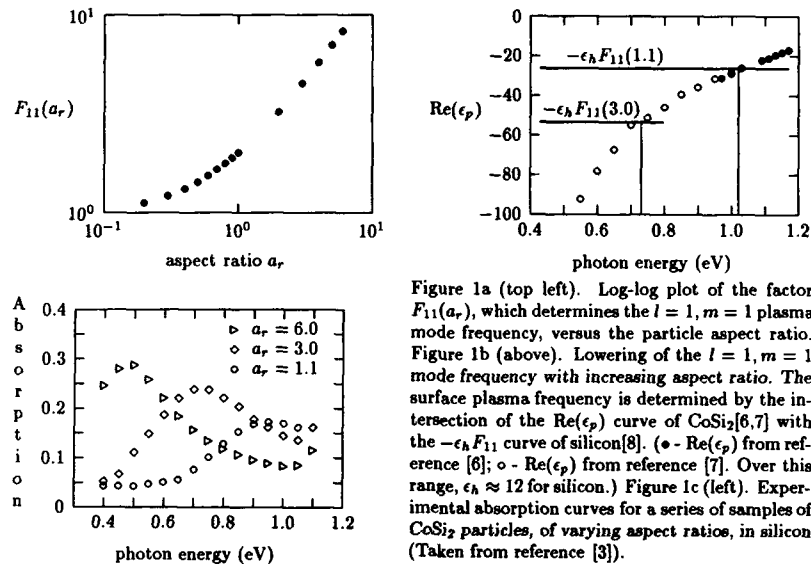


Figure 1a (top left). Log-log plot of the factor $F_{11}(a_r)$, which determines the $l = 1, m = 1$ plasma mode frequency, versus the particle aspect ratio. Figure 1b (above). Lowering of the $l = 1, m = 1$ mode frequency with increasing aspect ratio. The surface plasma frequency is determined by the intersection of the $\text{Re}(\epsilon_p)$ curve of CoSi_2 [6,7] with the $-\epsilon_h F_{11}$ curve of silicon [8]. (\bullet - $\text{Re}(\epsilon_p)$ from reference [6]; \circ - $\text{Re}(\epsilon_p)$ from reference [7]. Over this range, $\epsilon_h \approx 12$ for silicon.) Figure 1c (left). Experimental absorption curves for a series of samples of CoSi_2 particles, of varying aspect ratios, in silicon (Taken from reference [3]).

MODEL FOR THE PHOTOEMISSION YIELD

A simple relation that describes the essential behavior of the internal photoemission yield Y (the carrier emission probability per absorbed photon) is the modified Fowler equation [9]

$$Y = \frac{M}{8E_F} \frac{(h\nu - \psi)^2}{h\nu}, \quad (2)$$

where ψ is the Schottky barrier height, $h\nu$ is the photon energy, E_F is the metal Fermi energy, and M is the ratio of effective masses in the semiconductor and in the metal. A plot of $\sqrt{Y h\nu}$ versus $h\nu$ (a Fowler plot) therefore yields a straight line whose intercept gives the Schottky barrier height. In terms of the distribution $n(E)$ of excited carriers, the internal yield is $Y = \int n(E) y(E) dE / \int n(E) dE$, where $y(E)$ is the carrier-energy-dependent yield. Carrier scattering is neglected in equation (2). An analysis by Vickers [10], however, shows that scattering does not change the expression for $y(E)$, but only multiplies it by an enhancement factor U (dependent on the elastic and inelastic scattering lengths, and through these, on the carrier energy E).

Equation (2) was derived for a planar interface. For particles, we expect the yield to be enhanced because the three-dimensional confinement results in a greater probability that a carrier will be moving toward an interface. TEM observations [1,2,3] show that the epitaxial CoSi_2 particles are bounded by planar interfaces, two of which (the two ends of the particle) comprise a large percentage of the total interface. We therefore expect that this enhancement does not change the Fowler behavior of the yield $y(E)$ appreciably, and incorporate it into the enhancement factor U . (A more detailed analysis of this point will

be found in reference [5].)

In deriving an expression for the photoyield from metal particles, we must recognize that the excited carrier distribution in metal particles is different from that in films and bulk metal. In metal films, carriers are directly excited by photons, so that, if the carrier excitation probability is approximated to be independent of the initial energy of the carrier (as is done in deriving the modified Fowler equation) the distribution of excited carriers $n(E)$ is proportional to the density of initial states $g(E - h\nu)$. In particles, however, the creation of excited carriers can proceed through two processes. One is the normal process in which a photon directly excites an electron-hole pair. In the second process, which becomes increasingly important as the photon energy approaches the metal particle surface plasmon energy, the photon excites a surface plasmon, and the surface plasmon then decays into an electron-hole pair [11]. The distribution of excited carriers resulting from plasmon excitation and decay, $n_p(E)$, may be different from the distribution $n_e(E)$ resulting from direct photoexcitation. This is because the plasmon, as a discrete excited state with energy $\hbar\omega_{sp}$ and lifetime $1/\Gamma$, can decay into electron-hole pairs with a distribution of excitation energies $\hbar\omega$. Each pair excitation of given energy $\hbar\omega$ can have final electron energies ranging from E_F to $E_F + \hbar\omega$. The distribution $n_p(E)$ (in the normalized form $p_p(E) = n_p(E) / \int n_p(E) dE$) is therefore given by

$$p(E) = \int_{E-E_F}^E P(\hbar\omega, E) d(\hbar\omega) \quad (3)$$

where $P(\hbar\omega, E)$ is the distribution of decayed electron-hole pair excitations, of excitation energy $\hbar\omega$, and electron energy E . The distribution $P(\hbar\omega)$ is given (in first-order perturbation theory) by

$$P(\hbar\omega, E) = \frac{|\langle \hbar\omega, E | H_i | i m \rangle|^2 g(E) g(E - \hbar\omega)}{(\hbar\omega - \hbar\omega_{sp})^2 + (\hbar\Gamma/2)^2} \quad (4)$$

where H_i is the Hamiltonian term representing the interaction between the pair excitation and surface plasmons, $g(E)g(E - \hbar\omega)$ is the density of pair excitation states, and Γ is transition rate from the surface plasmon state to any of the final pair-excitation states.

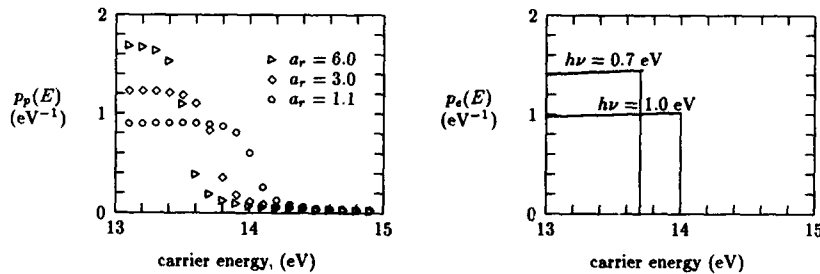


Figure 2a (left). Calculated distributions $p_p(E)$ of excited carriers resulting from the decay of surface plasmons, for various surface plasmon energies (or various aspect ratios) Figure 2b (right). Normalized distribution $p_e(E)$ of directly photoexcited carriers shown for two different photon energies. The plots start at the Fermi level of $E_F = 13$ eV for CoSi_2 .

The calculated distribution $n_p(E)$ is shown in Figure 2, together with the distribution $n_e(E)$ of directly photoexcited carriers. (Details of the calculation will be described in a later publication [5,12]) Because these two distributions are different, we write the quantum efficiency $\eta = AY$ for internal photoemission from a metal particle as the sum of two terms:

$$AY = A_p(h\nu)Y_p(\hbar\omega_{sp}) + A_e(h\nu)Y_e(h\nu), \quad (5)$$

where A_e is the absorption due to the direct excitation of electron-hole pairs, and A_p is the absorption in the metal particle due to the excitation and decay of plasmons.[14] The quantity Y_e is the probability that photon absorption excites a carrier into a state that will be emitted, and Y_p is the probability that plasmon decay results in an emitted carrier. In terms of the excited-carrier distributions, $Y_p = \int n_p(E)y(E)/\int n_p(E)dE$ and $Y_e = \int n_e(E)y(E)/\int n_e(E)dE$. The same enhancement factor U therefore appears in both Y_e and Y_p , and there is no room for the adjustment of their relative magnitudes. Integration yields the modified Fowler equation for Y_e , but results in a constant for Y_p , because $n_p(E)$ is independent of photon energy.

The total absorption, A , is the sum of a part due to the excitation of plasmons[13], A_p , and a part due to the direct excitation of electron-hole pairs, A_e . We write $A_p = fA$ and $A_e = (1-f)A$, where f will in general depend on photon energy. When written this way, the absorption falls out of equation (3), and the internal yield is therefore

$$Y(h\nu) = f(h\nu)Y_p(\hbar\omega_{sp}) + [1 - f(h\nu)]Y_e(h\nu). \quad (6)$$

Calculating $f(h\nu)$, the fraction of absorbed photons that excite plasmons, may be difficult. However, we do not need to calculate it in order to see how the yield predicted by this model will behave. We know that $0 < f(h\nu) < 1$, and because of the resonant nature of surface plasmon excitation, we expect that $f(h\nu)$ will be a peaked function with a maximum at the surface plasmon energy. Figure 3 shows theoretical Fowler plots of the yield Y , using the calculated values of Y_p and Y_e , and using Lorentzian curves of varying peak heights for $f(h\nu)$.

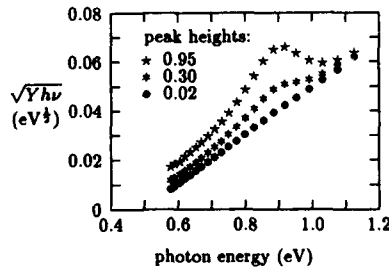


Figure 3. Theoretical curves for the internal yield Y from a metal particle, generated using Lorentzian curves $f(h\nu)$ of varying peak height, with a peak position of 0.9 eV (corresponding to $\alpha_s = 1.1$) and a halfwidth of 0.1 eV.

PHOTORESPONSE EXPERIMENTS

Photoresponse measurements were done at JPL on the series of samples of varying aspect ratio. A thin (1000 Å) film of cobalt was deposited onto the front side of the samples in order to make electrical contact. The results are shown in Figure 4 in the form of Fowler plots. It can be observed that the quantum efficiencies have peaks that correspond roughly to the plasma absorption peaks (Figure 1c) in the same samples. Because the absorption of metal films is approximately constant over this energy range, the cobalt film will make a linear contribution to the observed quantum efficiencies. Dividing out the absorption from the quantum efficiency data will give us the experimental yields, but the contribution of the cobalt film has to be removed first. Work on obtaining the experimental yields of the particles only, by experimentally determining the contribution of the cobalt film, are currently under way. Experiments with a p-i-n structure, with the particles in the intrinsic region[2], are also currently under way.

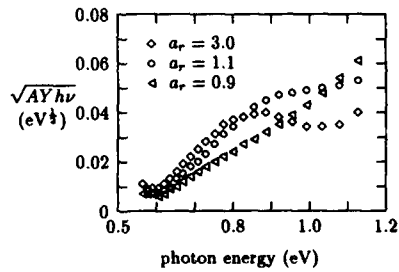


Figure 4. Experimental Fowler plots of the quantum efficiency AY for samples of CoSi_2 particles of varying aspect ratio (from reference [14]).

MODEL FOR REPLENISHMENT OF CARRIERS

An apparent problem that needs clarification is the replenishment of photoemitted carriers in the metal[2]. In normal, film-geometry Schottky-diode detectors, photoemitted carriers are replenished through the lead contact to the metal. For metal particles embedded in the semiconductor there is no such contact. It is clear, however, that photoemission, and the operation of the detector, cannot continue on indefinitely unless there is some mechanism by which charge can flow back into the particle. It might be possible to maintain charge neutrality by the emission of both holes and electrons, but this cannot occur for photon energies between the electron barrier height and the hole barrier height.

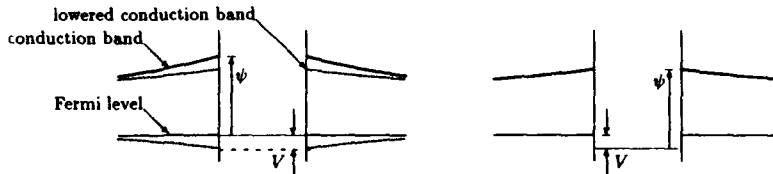


Figure 5a (left). Change in the curvature of the semiconductor conduction band caused by the electric field generated by accumulating charge on the metal particle. Continuous lines represent the bands before charging; discontinuous lines represent the situation after charging. Figure 5b (right). The potential gradient approximated as a potential step at the metal/semiconductor interface.

A model for the replenishment of charge is described as follows: as carriers are photoexcited out of the particle and swept away, the particle gets charged. There is therefore a potential due to the charged particle that varies approximately as r^{-1} . This lowers the Fermi level in the metal and modifies the band curvature in the semiconductor outside the metal, as shown in Figure 5a. To simplify matters, we can approximate the potential difference V between the particle and far away as occurring mostly near the interface (Fig 5b). The current flowing from the semiconductor into the metal increases with this potential difference. The current (photocurrent) out of the metal particle, on the other hand (the rate at which electrons are emitted) depends only on the Schottky barrier height ψ through the quantum efficiency η :

$$I_{out} = q \frac{I_{opt}}{h\nu} \eta. \quad (7)$$

This current therefore remains constant while causing V , and the current into the metal, to increase. The current into the metal will be an exponential function of the form $I_{in} = I_{in_0} \exp(qV/kT)$. Eventually, a steady-state situation $I_{out} = I_{in}$ will be reached at a

voltage V given by

$$qV = kT \ln \left(\frac{q I_{opt}}{h\nu I_{ino}} \eta \right), \quad (8)$$

The metal particles are therefore charged while the detector is illuminated. A simple calculation[5,12] using the thermionic emission theory for the current into the metal[15], shows that the steady-state voltage V is less than 0.1 volts, at $h\nu = 1$ eV, for a power density of 1 watt/cm² (assuming the worst case of $\eta = 1$). Furthermore, this charge, because of the logarithmic relationship (equation (8)), changes only slowly with the incident intensity.

SUMMARY

We have studied optical absorption and internal photoemission in epitaxially grown structures consisting of CoSi₂ particles embedded in silicon. The distribution of photoexcited carriers in the metal is found to be altered by excitation and decay of surface plasmons. This distribution has been calculated, and the resulting behavior of the photoemission yield has been obtained. The model is capable of accounting for the experimentally observed photoresponse. The replenishment of carriers during the photoemission process has been explained in a model in which the metal particles acquire a small ($qV \approx 0.1$ eV) steady-state charge.

ACKNOWLEDGEMENTS

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EPITAXIAL GROWTH OF SILICON ON $\text{CoSi}_2(001)/\text{Si}(001)$

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Abstract

Epitaxial Si layers have been grown under a variety of growth conditions on $\text{CoSi}_2(001)$ by molecular beam epitaxy (MBE). The structural properties of the Si overgrowth were studied by *in-situ* Reflection High Energy Electron Diffraction (RHEED), as well as *ex-situ* MeV $^4\text{He}^+$ ion channeling and High Resolution Transmission Electron Microscopy (HRTEM). Strong influences of the CoSi_2 surface reconstruction on the Si overgrowth have been observed. RHEED studies show islanding growth of Si on the $\text{CoSi}_2(001)$ $(3\sqrt{2} \times \sqrt{2})R45$ reconstructed surface, but smooth growth of Si on the $\text{CoSi}_2(001)$ $(\sqrt{2} \times \sqrt{2})R45$ reconstructed surface, under the same growth conditions. The growth of Si on thin layers of CoSi_2 (2nm-6nm) with $(\sqrt{2} \times \sqrt{2})R45$ reconstructed surface at 460°C results in high crystalline quality for the Si top layer, as indicated by good channeling minimum yield ($\chi_{\min} < 6\%$), but cross-sectional TEM shows that the CoSi_2 layers are discontinuous. We also report preliminary results on Si grown on a 2×2 reconstructed $\text{CoSi}_2(001)$ surface.

Introduction

Buried epitaxial metal silicide layers in Si have attracted great attention because of their potential application in high speed devices like the metal base transistor and the permeable base transistor, and also as buried epitaxial metal layers in three dimensional integrated circuits. The advantages of CoSi_2 are its excellent conductivity, its fluorite crystal structure (which is similar to the diamond structure of Si), and its small lattice mismatch with Si (1.2% at room temperature), which increase the possibility of growing high quality heteroepitaxial $\text{Si}/\text{CoSi}_2/\text{Si}$ structures. Despite great success in fabricating high quality CoSi_2 and Si/CoSi_2 multilayers on $\text{Si}(111)$ [1-4], a metal base transistor has been difficult to develop. This may be due to the absence of states in the silicide with the correct transverse momentum (near the Si conduction band minimum) for electron injection along the [111] direction [5]. Such states do exist in the silicide for electrons injection along [001] direction [5], so that the growth of epitaxial $\text{Si}/\text{CoSi}_2/\text{Si}(001)$ structures would have greater technological importance. Monocrystalline $\text{CoSi}_2(001)$ has been successfully grown on $\text{Si}(001)$ in recent years [6,7], which makes the studies of Si growth on $\text{CoSi}_2(001)/\text{Si}(001)$ possible.

Sample growth

In these experiments, four-inch p-type $\text{Si}(001)$ wafers with resistivity of 15-25 $\Omega\text{-cm}$ were used. The wafers were given a modified RCA clean before loading into the MBE system (VG Semicon, model V90S), which had a base pressure of 5×10^{-11} mbar.

Pressures during growth were in the middle of the 10^{-10} mbar range. Inside the MBE system, the wafers were heated to high temperature ($750^{\circ}\text{C} - 820^{\circ}\text{C}$) for 15 minutes in order to remove the protective oxide film. This annealing temperature was determined by obtaining a sharp RHEED 2×1 reconstructed streak pattern. RHEED, with 14 keV electrons, was used at every stage of deposition to monitor the surface. The cobalt and silicon were evaporated from two separate Temescal electron-beam evaporators. Evaporation rates were separately monitored by electron-impact emission spectroscopy and feedback controlled to within 5% by an Inficon Sentinel III deposition controller. The calibration of the evaporation rates was done by RBS. The temperature was measured by a thermocouple and calibrated by an optical pyrometer.

Results and Discussion

Epitaxial CoSi_2 layers of different thickness were grown using the direct codeposition [7], the template I [6,7], and what we call the template II, methods. For the direct codeposition method, the epitaxial CoSi_2 was grown at 550°C , at a Co:Si ratio of 1:1.8. The deposition rates for Co and Si were 0.021nm/s and 0.07nm/s, respectively. The CoSi_2 in this case displayed a $(\sqrt{2} \times \sqrt{2})R45$ reconstructed RHEED pattern. The template I growth of CoSi_2 involved depositing an initial 0.2nm of Co, then codepositing 0.2nm Co and 0.72nm Si, all at room temperature, followed by annealing at 460°C to form a 1.4nm CoSi_2 layer. Codepositing Co and Si in 1:2 ratio at 460°C was used to thicken the template to the desired CoSi_2 thickness. We have only observed the $(3\sqrt{2} \times \sqrt{2})R45$ reconstructed RHEED patterns for CoSi_2 grown by the template I method, although Yalisove et al. [8] reported observing both the $(\sqrt{2} \times \sqrt{2})R45$ and the $(3\sqrt{2} \times \sqrt{2})R45$ reconstructed CoSi_2 surfaces with this growth procedure. RBS channeling measurements on the CoSi_2 layers grown by both the direct codeposition and template I methods show good epitaxial quality ($\chi_{\text{min}} < 5\%$). This is also confirmed by the sharp RHEED patterns for both growth procedures. A second template technique (template II) for growth of CoSi_2 was used which involved sequential room temperature deposition of 0.26nm Co and 0.7nm Si, followed by annealing at 460°C to form 0.9nm CoSi_2 . The CoSi_2 layer grown by the template II method displays a 2×2 reconstructed RHEED pattern.

The RBS channeling studies of Si overgrowth on CoSi_2 layers of different thickness and at different temperatures, are shown in Figure 1. A deposition rate of 0.05nm/s was used for all Si overgrowth reported in this paper. RBS shows that Co diffuses to the surface when Si is deposited at 550°C . Room temperature deposition of a thin Si buffer layer (1nm and 2nm) before further Si growth at 550°C does not stop the diffusion of Co. The crystalline quality of the Si top layer, indicated by channeling minimum yield, improves at higher growth temperatures. Figure 1 also shows the dramatic improvement of Si crystalline quality for Si grown on thinner CoSi_2 layers. A growth temperature of 460°C was used for Si overgrowth on CoSi_2 with different surface reconstructions. The results are summarized in Table 1.

During Si growth on the $(3\sqrt{2} \times \sqrt{2})R45$ reconstructed surface, RHEED observations show that islanding takes place immediately after the start of Si deposition, and continues throughout the Si overgrowth. This is shown in Figure 2. Faceting of the overgrown Si layer can be seen in the RHEED pattern (Figure 2(b)). The crystalline quality of the CoSi_2 and the top Si layer is very poor, as indicated by the very high channeling minimum yields for both Si and Co. In contrast to the faceted growth of Si on the CoSi_2 $(3\sqrt{2} \times \sqrt{2})R45$ reconstructed surface, Si growth on the CoSi_2 $(\sqrt{2} \times \sqrt{2})R45$

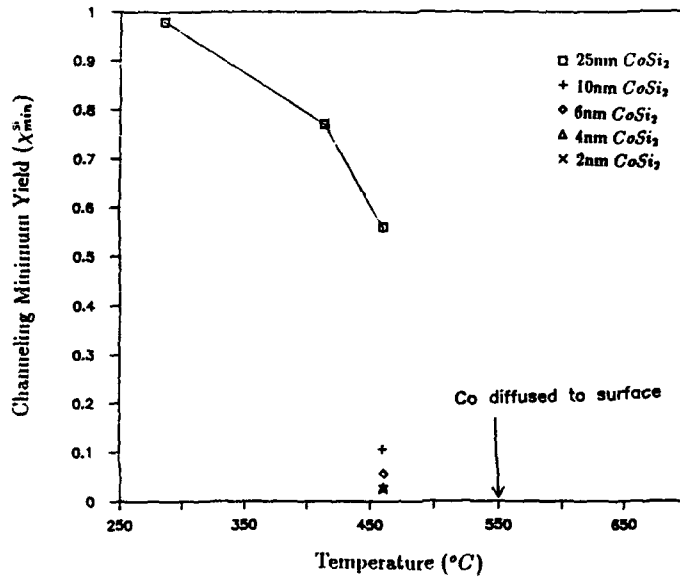


Figure 1. RBS channeling results of silicon overgrowth on CoSi_2 layers of different thicknesses at different temperatures.

Table 1. Summary of silicon overgrowth on $\text{CoSi}_2(001)$ at 460°C . The silicon deposition rate is 0.05nm/s for all the samples.

growth method	$\text{CoSi}_2/\text{Si}(001)$		$\text{Si}/\text{CoSi}_2/\text{Si}(001)$		
	RHEED	thickness (nm)	$\chi_{\text{min}}(\text{Si})$ (%)	$\chi_{\text{min}}(\text{Co})$ (%)	RHEED
codeposition	$(\sqrt{2} \times \sqrt{2})R45$	10	10.6	31.3	smooth growth
codeposition	$(\sqrt{2} \times \sqrt{2})R45$	6	5.6	36	smooth growth
codeposition	$(\sqrt{2} \times \sqrt{2})R45$	4	2.8	30	smooth growth
codeposition	$(\sqrt{2} \times \sqrt{2})R45$	2	2.4	28	smooth growth
template I	$(3\sqrt{2} \times \sqrt{2})R45$	6	52	77	faceted growth
template I	$(3\sqrt{2} \times \sqrt{2})R45$	2	62	73	faceted growth
template II	2×2	0.9	2.2	4.7	smooth growth

reconstructed surface is smooth, according to RHEED observations (Figure 3). Small modulations in the intensity along the main streak disappear as the Si grows thicker, giving way to a sharp $\text{Si } 2 \times 1$ reconstructed pattern. RBS channeling measurements show high crystalline quality for Si grown on thin CoSi_2 layers with the $(\sqrt{2} \times \sqrt{2})R45$ reconstructed surface, but relatively poor crystalline quality for the buried CoSi_2 layer (χ_{min} about 30% for the Co including the interfaces peaks).

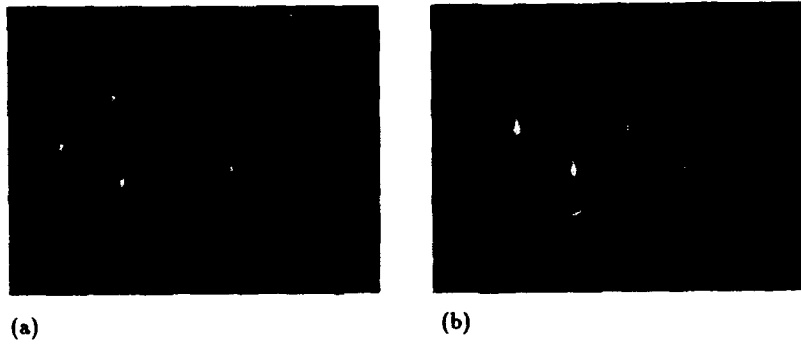


Figure 2. RHEED patterns (along the [001] azimuth) taken during Si growth on the 6 nm thick CoSi_2 film with a $(3\sqrt{2} \times \sqrt{2})R45$ reconstructed surface (a) at 6.5nm, and (b) at 100nm.

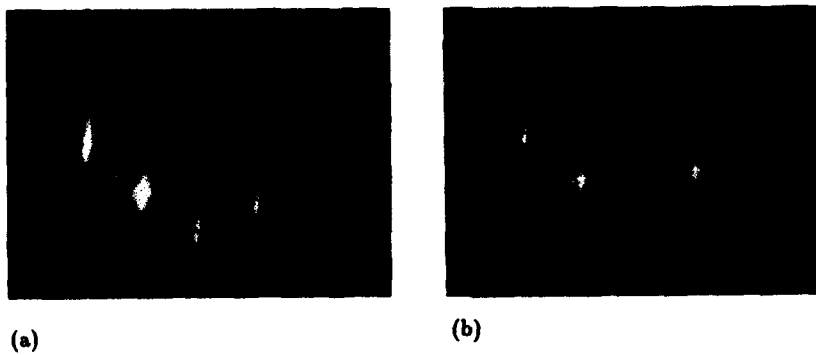


Figure 3. RHEED patterns (along the [001] azimuth) taken during Si growth on the 2 nm thick CoSi_2 film with a $(\sqrt{2} \times \sqrt{2})R45$ reconstructed surface (a) at 1.5nm, and (b) at 40nm.

HRTEM was used to study 100nm Si films grown on 6nm and 2nm CoSi_2 layers with the $(\sqrt{2} \times \sqrt{2})R45$ reconstructed surface. TEM shows that the CoSi_2 layers are not continuous in both samples (Figure 4). Increased CoSi_2 coverage and grain size were observed for the sample with the thicker CoSi_2 layer. The epitaxial Si layer on 6nm CoSi_2 contains a higher density of microtwins and stacking faults near the CoSi_2 layer. The tendency of CoSi_2 to facet along (111) planes is also observed, again indicating the relatively low Si(111)/ CoSi_2 (111) interface energy. The overall quality of the Si(111)/ CoSi_2 (111) and Si(001)/ CoSi_2 (001) interfaces is good.



Figure 4. A cross-sectional high-resolution TEM image of 100 nm Si grown on a 6 nm CoSi_2 (001) layer, imaged along the [110] direction.

Figure 5 shows RBS channeling spectra of 40nm of Si grown on a 0.9nm 2×2 surface reconstructed CoSi_2 layer grown by the template II method. It shows high crystalline quality for both the Si top layer and the buried CoSi_2 layer. The RHEED observations shows the smooth growth of Si on this 2×2 surface reconstructed CoSi_2 layer. The disordering of CoSi_2 layers, observed after Si growth on the previous two types of reconstructed CoSi_2 surfaces, was not observed for Si growth on the 2×2 surface reconstructed CoSi_2 layer. These results indicate a promising method of obtaining high quality epitaxial structures of Si/ CoSi_2 /Si(001), by depositing Si on a 2×2 surface reconstructed CoSi_2 layer.

Summary

Our results show that the CoSi_2 (001) surface reconstructions have strong influences on Si overgrowth at 460°C. Depositing Si on the $(3\sqrt{2} \times \sqrt{2})R45$ reconstructed CoSi_2 surface results in islanding growth, and the crystal quality of both the Si overlayer and the buried CoSi_2 layer is very poor. Si growth on the $(\sqrt{2} \times \sqrt{2})R45$ reconstructed CoSi_2 surface is smooth, and results in a high quality Si overlayer, but the buried CoSi_2 layer is slightly disordered. TEM also shows that the CoSi_2 layer is discontinuous. High crystalline quality is observed for both the buried CoSi_2 layer and the epitaxial Si overlayer grown by depositing Si on the 2×2 surface reconstructed CoSi_2 layer.

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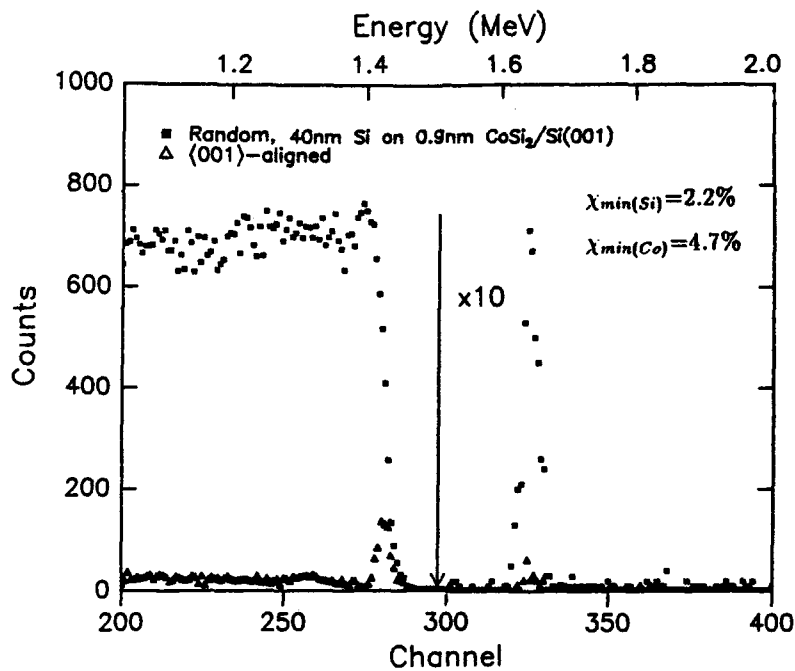


Figure 5. Random and channeling spectra of 40nm Si grown on 0.9nm CoSi₂ (grown by template II) with a 2×2 reconstructed surface.

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GROWTH OF CoSi_2 ON $\text{CaF}_2/\text{Si}(111)$ HETEROSTRUCTURES

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ABSTRACT

In order to produce an epitaxial metal/insulator/semiconductor structure we investigated the growth of CoSi_2 on $\text{CaF}_2/\text{Si}(111)$ heterostructures. We demonstrate the possibility to grow epitaxial CoSi_2 on CaF_2 films by utilization of the template technique. The fabrication of these structures will be presented. The properties of such heterostructures were determined by means of RHEED, LEED, AES, SIMS, RBS and resistivity measurements.

INTRODUCTION

For applications in 3-D integrated circuits it is important to study the heteroepitaxy of single crystal metal/ single crystal insulator structures. Calcium fluoride is a promising insulator for epitaxial growth on silicon. Successful growth of CaF_2 on Si substrates has been demonstrated by a number of groups [1],[2],[3]. Meanwhile backscattering yields (χ_{min}) of less than 6% have been achieved on both Si(111) and Si(100) substrates. On the other hand, CoSi_2 is an excellent choice for an epitaxial metal. The growth of high quality epitaxial silicide/Si and Si/silicide structures has already been demonstrated [4]. So the $\text{CoSi}_2/\text{CaF}_2/\text{Si}(111)$ heterostructure seems to be a promising candidate for a single crystal metal/ single crystal insulator structure, especially for 3-D integration. The growth of calcium fluoride on top of $\text{CoSi}_2/\text{Si}(111)$ heterostructures has already been reported by J.M. Phillip et.al. [5].

CoSi_2 has cubic fluorite structure with a lattice mismatch of 1.8% with CaF_2 at room temperature. Problems of the $\text{CoSi}_2/\text{CaF}_2$ system are:

- the great difference between the linear thermal expansion coefficients α ($\alpha_{\text{CaF}_2} = 19 \times 10^{-6} \text{ K}^{-1}$, $\alpha_{\text{CoSi}_2} = 10 \times 10^{-6} \text{ K}^{-1}$). This results in the build up of strain during thermal processing.
- the surface free energy F_{CaF_2} is about 5 times lower than F_{CoSi_2} ($F_{\text{CaF}_2} = 4.5 \times 10^{-5} \text{ J/cm}^2$ [6], $F_{\text{CoSi}_2} = 2.5 \times 10^{-4} \text{ J/cm}^2$ [7]). In this case island growth is the preferred growth mode at elevated temperatures [8].

In order to overcome the problem of island formation, the utilization of the template technique was investigated. For the first time the present work demonstrates the possibility to grow $\text{CoSi}_2/\text{CaF}_2/\text{Si}(111)$ heterostructures.

CaF_2 GROWTH ON Si(111)

To investigate the growth of CoSi_2 on $\text{CaF}_2/\text{Si}(111)$ heterostructures, 3" wafers were cleaned in situ by an annealing step at 850 °C for 10 minutes. After ramping down the substrate temperature to 700 °C, CaF_2 was evaporated with rates of 0.15 to 0.2 nm/s. The pressure during evaporation was below 3×10^{-7} Pa. After deposition of 140 nm CaF_2 , a sharp 1x1 structure with Kikuchi pattern could be observed with RHEED, which

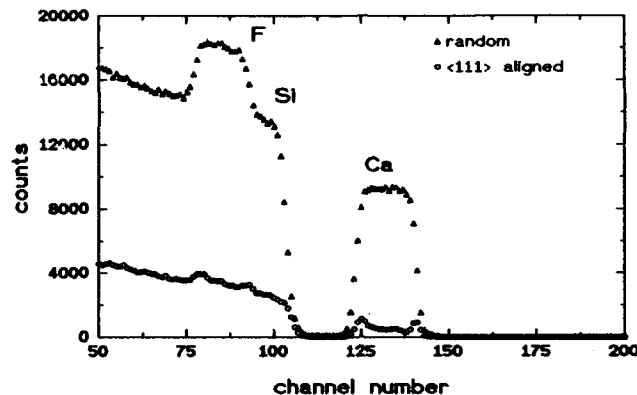


Fig. 1 RBS spectra of a 140nm CaF_2 layer on Si(111), $\chi_{\min} = 3.4\%$ for Ca.

demonstrates good crystal quality. For the determination of the crystal quality, RBS measurements were carried out. Fig. 1 shows the RBS channeling spectra of an epitaxial CaF_2 film with thickness of 140 nm. The backscattering yield was as low as 3.4% indicating excellent crystallinity.

$\text{CoSi}_2/\text{CaF}_2/\text{Si}(111)$ HETEROSTRUCTURES

To suppress island growth mode and pinhole formation of CoSi_2 on Si(111), codeposition of Co and Si in the correct stoichiometric ratio on substrates at room temperature to form a thin template layer is a successful technique [9]. Annealing of such templates at 380°C leads to epitaxial CoSi_2 -B-type films. On this template epitaxial CoSi_2 films of any thickness can be grown at substrate temperature of 380°C . A final anneal of 600°C is necessary to improve crystal quality and resistivity of these films. For example, CoSi_2 films of 100nm thickness with a RBS backscattering yield of 3.2% and a resistivity of $13\mu\Omega\text{cm}$ could be obtained [10].

We also used this technique for the growth of CoSi_2 on CaF_2 , but it turned out that there are some differences. The thickness of the template has to be increased from 7nm in the case of a Si substrate to 14nm in the case of CaF_2 . Thinner films with observable RHEED pattern turned out to be non-continuous. On Si substrates the templates showed a 1×1 RHEED pattern even at annealing temperatures as low as 150°C , whereas on CaF_2 first patterns were visible at 450°C . So a significant higher annealing temperature for the template is necessary to obtain a film with long range order. Annealing the templates at 500°C leads to continuous epitaxial films with a sheet resistance of $207\Omega/\square$. Increasing the temperature to 600°C results in non-continuous films with unmeasurable sheet resistance. So there is only a small temperature range for the production of suitable templates. Thicker films were grown on this templates by codeposition at substrate temperatures of 380°C . Finally the films were annealed at 650°C for 10 minutes to improve the crystal quality.

Depending on film thickness, different surface structures could be observed using LEED (Fig. 2). At 71nm a $\sqrt{12}\times\sqrt{12}R30^\circ$ structure was visible. In the range of 140nm-200nm a $\sqrt{3}\times\sqrt{3}R30^\circ$ could be observed. Above 280nm a 1×1 pattern with the typical

energy dependence of a CoSi_2 -S-surface was observed [11]. The CoSi_2 -S-surface is a $\text{CoSi}_2(111)$ plane with an additional Si double layer on top. This structure is found on all CoSi_2 -films, which were deposited on $\text{Si}(111)$ and annealed above 450°C . The observed 1×1 pattern has a remarkably good threefold point symmetry. This indicates that most parts of the film have a single orientation. AES measurements show a correlation between the amount of calcium and fluorine on the surface with the surface structure. The AES peak ratio of Ca to Si, respectively the surface structure in dependence of CoSi_2 thickness, is shown in table I. Because of the interference of the F_{KLL} -signal with the Co_{LVV} -signal the dependence of surface structure on the fluorine concentration is difficult to obtain and therefore not shown in the table.

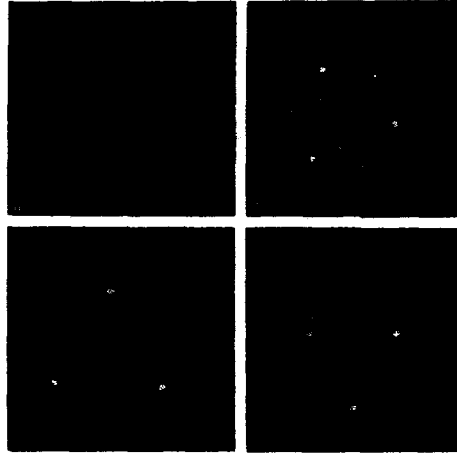


Fig. 2 a) $\sqrt{12}^\circ/\sqrt{12}R30^\circ$, 71nm CoSi_2 , b) $\sqrt{30}^\circ/\sqrt{30}R30^\circ$, 177nm CoSi_2 , c,d) CoSi_2 -S at $E_{\text{kin}} = 50\text{eV}$ and $E_{\text{kin}} = 80\text{eV}$, 283nm CoSi_2

Table I

CoSi_2 thickness [nm]	Surface structure	AES peak ratio $\frac{\text{Ca}_{\text{LMM}}}{[\text{Si}_{\text{LMM}} + \text{Ca}_{\text{LMM}}]}$	ρ_{CoSi_2} [$\mu\text{g}/\text{cm}^2$]
71	$\sqrt{12}^\circ/\sqrt{12}R30^\circ$	0.388	23.4
142	$\sqrt{30}^\circ/\sqrt{30}R30^\circ$	0.087	17.6
177	$\sqrt{30}^\circ/\sqrt{30}R30^\circ$	0.076	17.5
283	CoSi_2 -S	0.0	16.3

To determine the calcium and fluorine distribution in the CoSi_2 layer, SIMS depth profiles were taken (Fig. 3). Calcium tends to a strong surface segregation. This corroborates the AES measurements. There are also large amounts of Ca and F present in the CoSi_2 , but in a concentration more than one order of magnitude lower as at the surface. The relative large decay length of the Co and Si signal in the CaF_2 region can not only be explained by knock-on-effects and as an artifact of SIMS-measurements. A mixture of CoSi_2 and CaF_2 regions at the interface might also contribute to the measured depth profile.

For a 168nm thick silicide layer, RBS channeling spectra are shown in Fig. 4. The minimum backscattering yield χ_{min} for the Co signal was determined to be 34%. A film of 65nm thickness had a χ_{min} of 37%. For comparison, CoSi_2 films on $\text{Si}(111)$ have a typical χ_{min} of 3-4%. The films grown on CaF_2/Si heterostructures have a degraded

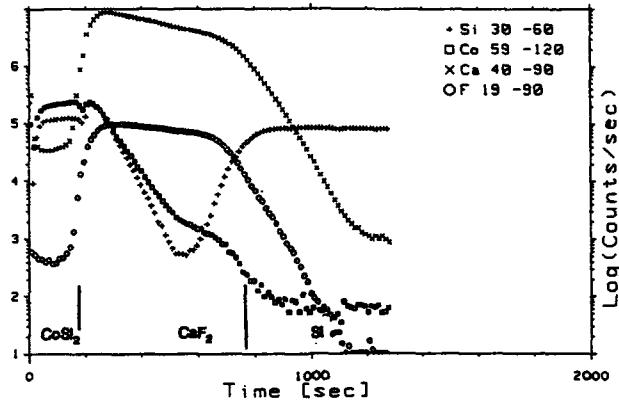


Fig. 3 SIMS depthprofile of a $\text{CoSi}_2/\text{CaF}_2/\text{Si}(111)$ heterostructure

crystal quality. The Co signals in the RBS spectra had smeared shoulders on the low energy side of the spectra. This indicates an inhomogeneous film thickness which could be caused by islands on the surface and a rough interface between CoSi_2 and CaF_2 .

In Fig. 5 the sheet conductance is plotted versus the cobalt disilicide thickness. Between 30nm and 280nm the graph shows a good linear dependence of sheet conductance on the film thickness following the equation $G = \sigma_B(d-d_0)$, where G is the sheet conductance, σ_B is the specific conductance of bulk CoSi_2 , d is the film thickness and d_0 is an offset in film thickness for $G=0$. The bulk resistivity calculated from the slope of the curve is $14\mu\Omega\text{cm}$. This is a remarkably good value. The resistivity of epitaxial CoSi_2 films on $\text{Si}(111)$ is about $13\mu\Omega\text{cm}$ [10]. The offset $d_0=14\text{nm}$ might be explained by a model in which most parts of the layer behave like good metallic CoSi_2 . But there exists also a high resistance layer at the interface $\text{CaF}_2/\text{CoSi}_2$ in which

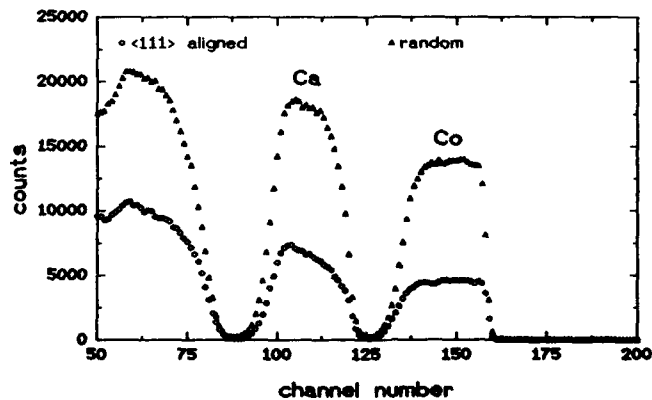


Fig. 4 RBS spectra of a CoSi_2 film of 168nm thickness. $\chi_{\text{min}} = 34\%$

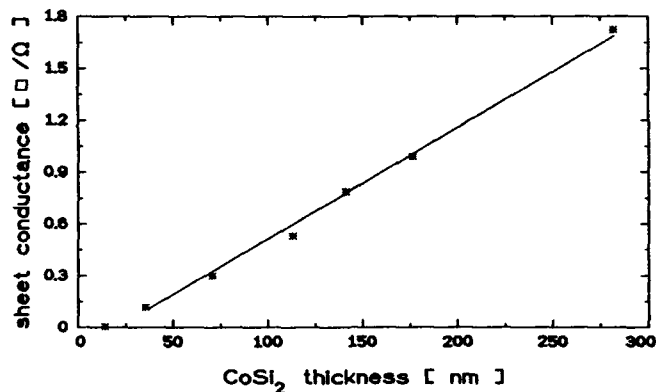


Fig. 5 CoSi₂ sheet conductance versus film thickness

epitaxial CoSi₂ is intermixed with the calcium fluoride. This assumption is supported by SIMS and RBS measurements, and the fact that below 14nm film thickness a continuous film was not obtainable. Table I shows the resistivity of each individual layer in relation to the film thickness.

The SEM micrograph (Fig. 6) of a 71nm film shows that island formation could not fully be suppressed by our growth technique. Some pinhole like features are also observable. Obviously, the difference in surface free energy is too large and the growth temperature which is necessary to get epitaxial growth is too high to avoid island growth successfully.

Although the electrical properties of the film structure were rather promising, the large difference of the linear thermal expansion coefficient results in large strain in the heterostructure. This leads to cracks in the heterostructure, or at thicker films, to peeling of the layers. It was not possible to grow a mechanically stable heterostructure.



Fig. 6 SEM micrograph of a 71nm CoSi₂ film

CONCLUSION

For the first time, epitaxial growth of cobalt disilicide on $\text{CaF}_2/\text{Si}(111)$ heterostructures is reported. It was found that Ca and F diffuses into the CoSi_2 layer and Ca tends to surface segregation. Only for very thick films of 280nm thickness a Ca and F free surface with a CoSi_2 -S-structure could be detected. In comparison to CoSi_2 grown on $\text{Si}(111)$ using the same technique these films showed a degraded crystal quality. The insufficient mechanical stability of the heterostructure is caused by the large difference of the linear thermal expansion coefficient of CoSi_2 and CaF_2 .

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LOW TEMPERATURE GROWTH OF GROUP II-A FLUORIDE LAYERS ON SILICON AS BUFFER FOR HETEROEPITAXIAL IV-VI AND II-VI COMPOUND SEMICONDUCTORS

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Abstract

We present our new development of low temperature (<450°C) MBE growth of group II-a fluorides on Si(111) and infrared sensor fabrication in $Pb_{1-x}Sn_xSe$ grown on such fluoride layers. The stacked CaF_2 - BaF_2 buffer helps to overcome the large lattice and thermal mismatch between the Si-substrate and the narrow gap chalcogenide. Despite a rather nominal quality of the low temperature grown CaF_2 layer, the 200nm thick epitaxial BaF_2 top layer is of good structural perfection as judged from RBS channelling yield, RHEED-patterns and microscopy. The fluoride buffers were successfully overgrown with $Pb_{1-x}Sn_xSe$ and small IR-sensor arrays with up to 10.5 μ m cut-off wavelength were fabricated in the layers. The performance of these sensors is as good as for sensors fabricated with the high temperature buffer layer growth process.

Introduction

Thin films of group II-a fluorides serve as buffers for heteroepitaxial growth of IV-VI compound semiconductors (lead chalcogenides) on silicon. Photovoltaic infrared sensors fabricated in such IV-VI-on-Si heterostructures have the potential for a low cost technique of large IR focal plane arrays for thermal imaging applications (For a review see Ref. 1). The signal processing can be performed in the Si-substrate using standard Si-technology, while the sensitivity and operating temperature is the same as in other narrow gap semiconductors like MCT or InSb. We also use such fluoride buffers to grow epitaxial II-VI material (CdTe) on Si substrates [2,3].

As is well known the optimal substrate temperature for epitaxial growth of CaF_2 on Si(111) lies around 700°C [4,5]. This is the highest temperature in the whole growth process if no high temperature Shiraki cleaning is used. The IV-VI layers do not need higher growth temperatures than 400°C, while the IR-sensor fabrication steps are performed at temperatures much below. However, 700°C is too high if one wishes to grow the whole heterostructure on active Si-substrates which already contain completely processed circuits for the read-out electronics. The limiting temperature is due to the Al-metallization, which can withstand temperatures up to 450°C-500°C for a short time only. From a practical point of view, it would be advantageous to deposit the fluoride layers directly on completely processed and already electrically tested Si devices.

We therefore developed a technique to grow the CaF_2 - BaF_2 layers at substrate temperatures never exceeding 450°C. The low temperature grown layers are of somewhat inferior quality compared to layers grown at high temperatures. But their quality suffices for subsequent IV-VI growth and realization of IR-sensors therein.

As in BaF₂ layers grown at high temperatures, mechanical strains due to thermal misfit also relax in BaF₂ grown at low temperatures [6]. This is a very important behaviour of the fluoride buffers and makes them useful for heteroepitaxy on silicon.

Experimental

We used (111)-oriented 3 inch silicon wafers as substrates. The wafers, as delivered from the manufacturer, were cleaned by spin cleaning in a N₂ atmosphere[7]. About 1.5ml Methanol followed by the same quantity of a 1:5 HF-Methanol mixture followed again by pure Methanol were dropped on the middle of the spinning wafer. After immediately inserting the wafer into UHV without exposure to laboratory air (the inserting procedure takes about 3 minutes), an Auger spectrum shows small amounts of C and very small amounts of O on the surface. By stepwise heating the wafer in 12min to 450°C the C surface contamination reduces further while the O contamination remains constant. The contamination of the Si surface by these two elements is in the range of some thousandths of a monolayer.

The base pressure of the self constructed UHV system is in the 2*10⁻⁹ mbar range. Growth by MBE is performed with solid source material and graphite covered pyrolytic boron nitride crucibles. Evaporation rates are between 150nm/hour and 700nm/hour for CaF₂ and between 500nm/hour and 1000nm/hour for BaF₂. Layer thicknesses for CaF₂ are around 2nm and for BaF₂ between 150 and 250nm.

The fluoride chamber is connected by a UHV tunnel (vacuum in the 10⁻⁸ mbar range) with the IV-VI growth chamber so that the fluoride covered Si wafers can be either transported directly in UHV or taken out of the vacuum for some observations or putting masks for further IV-VI growth. The Pb_{1-x}Sn_xSe was grown at typical growth rates of a few hundred nm per hour, substrate temperature was 400°C-450°C and 2-4μm thick layers were grown.

Results

The RHEED-pattern of the spin cleaned Si(111) surface after heating to 450°C is shown in Fig. 1a. In contrast to the RHEED-pattern of a Shiraki cleaned (heated to about 900°C in UHV) Si(111) wafer we observed no 7*7 surface reconstruction, but almost the same sharpness of the Kikuchi-bands and streaks.

After starting growth of CaF₂, the RHEED pattern get quite blurred as shown in Fig. 1b. Note that the rings observed in this pattern are not those usually observed for polycrystalline growth, as we obtained in our earlier work [8]. We found that a CaF₂ thickness of about 2nm is most favourable for further growth of BaF₂. For too thin CaF₂ layers we observed blisters and for too thick ones the BaF₂ layer cracks. The RHEED-pattern become sharper and sharper during BaF₂ growth. For a 200nm thick BaF₂ layer grown at low temperature (Fig. 1c) the RHEED-pattern is nearly as sharp as for layers grown at high temperature (Fig. 1d) [9].

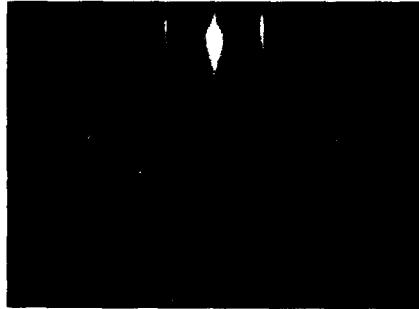


Fig. 1a:
RHEED-pattern of a spin-cleaned Si(111) wafer after heating to 450°C.



Fig. 1b:
RHEED-pattern of a 2nm thick CaF₂ layer grown at 450°C



Fig. 1c:
RHEED-pattern of a 200nm thick BaF₂ layer grown at 450°C.

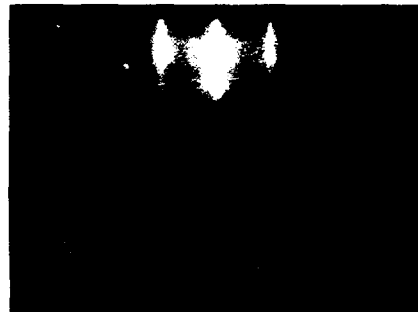


Fig. 1d:
RHEED-pattern of a 200nm thick BaF₂ layer grown at high temperatures (750/650)°C on Shiraki-cleaned Si(111).

Electron beam in [11-2] direction for all RHEED-patterns.

The crystalline quality of these layers was tested with Rutherford Backscattering Spectroscopy (RBS). As shown in Fig. 2a, the RBS-spectrum shows a minimum channelling yield of 11.7% for a 200nm thick BaF₂ layer grown at 450°C. This is somewhat higher than for the layers deposited with initial substrate temperature of 700°C (Fig. 2b), where the minimum channelling yield of a BaF₂ layer of the same thickness is 6.6% (still lower yields are found for thicker layers). The intensity of the BaF₂ signal increases towards the CaF₂-BaF₂ interface due to an increased number of lattice defects. This increase for the low temperature layer is much higher as in the case of high temperature growth, and indicates lower crystalline quality near the CaF₂-BaF₂ interface for layers grown at low temperatures.

The epitaxial relationship between Si and BaF₂ is predominantly type B (i.e. the BaF₂ lattice is rotated 180°

around the [111]-surface normal with respect to the Si). However we also achieved type A-oriented (i.e. the BaF_2 and Si lattice are of the same orientation) and mixed layers in some runs.

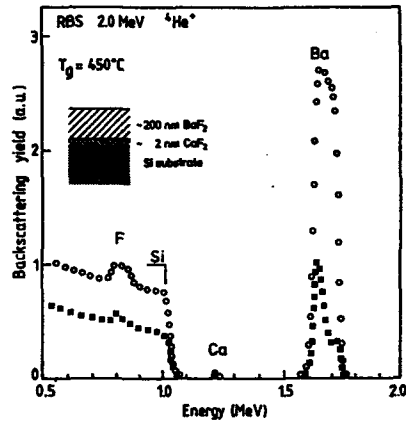


Fig. 2a:
RBS spectra of a 200nm thick BaF_2 - CaF_2 layer on Si(111) grown at substrate temperatures never exceeding 450°C.

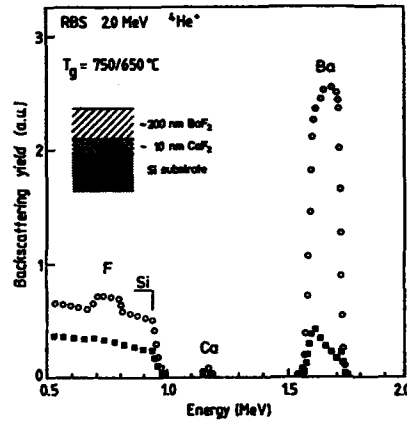


Fig. 2b:
RBS spectra of a 220nm thick BaF_2 - CaF_2 layer on Si(111) grown at substrate temperatures varying from 750°C-650°C.

The BaF_2 surfaces of the CaF_2 - BaF_2 layers grown at 450°C as described above are mirror-like, appear smooth in the optical microscope and show no cracks or blisters. Contrary to layers grown at high temperatures (Fig. 3), some roughness is revealed Fig. 4) with scanning electron microscopy (SEM) at high magnifications. This roughness is below a 100nm scale and does not hinder further epitaxial IV-VI growth.

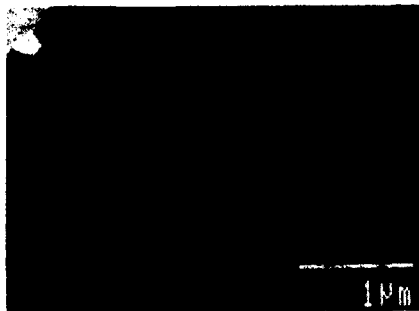


Fig. 3
SEM micrograph of a BaF_2 surface grown at 750/650°C

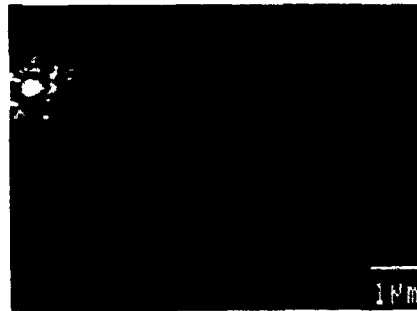


Fig. 4
SEM micrograph of a BaF_2 surface grown at 450°C

Mechanical strains in the layers are determined with x-ray diffraction [6]. As in the case of fluoride layers grown at high temperatures, the strains due to the thermal misfit are almost fully relaxed.

Infrared sensor array

The buffers were successfully overgrown with epitaxial $Pb_{1-x}Sn_xSe$. A linear photovoltaic IR-sensor array consisting of 66 sensors was fabricated in such a $Pb_{1-x}Sn_xSe$ layer [10]. The sensitivity of this array is similar compared to arrays fabricated with high temperature buffer layers. The uniformity of the array is excellent. The spread in 50% cut-off wavelength (nominal cut-off wavelength is $10.5\mu m$) is below $0.1\mu m$. The external quantum efficiencies are about 60% (without antireflection-coating) and with a standard deviation of 3% over the whole array.

Conclusion

We have grown for the first time epitaxial CaF_2 - BaF_2 stacks on Si substrates with reasonable epitaxial quality at temperatures never exceeding $450^\circ C$. Epitaxial $Pb_{1-x}Sn_xSe$ layers were grown on such stacks and photovoltaic IR-sensors with cut-off wavelength up to $10.5\mu m$ were fabricated in this IV-VI compound semiconductor. The sensitivity of these sensors is the same as that of sensors fabricated in layers grown on high temperature buffers.

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SUBSTRATE ENGINEERING WITH FLUORIDE BUFFER LAYERS ON Si

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ABSTRACT

Here, we report on our efforts to engineer Si substrates for growth of compound semiconductors through the use of suitable epitaxial buffer layers of CaF_2 , SrF_2 , and BaF_2 using a recently installed dual growth chamber MBE system. We have also developed new graphite-heater K-cells which have demonstrated reliable, high temperature deposition of the fluorides with excellent uniformity across substrates up to 6 inches in diameter. Excellent epitaxial quality ($\chi_{\text{min}} < 5.0\%$) and smooth surface morphologies have been achieved for epitaxial CaF_2 and SrF_2 grown directly on Si(111) and BaF_2 grown directly on Si(001). The BaF_2 is (111) oriented on the Si(001) substrates with one of the {110} planes of the BaF_2 aligned with the (110) plane in the Si(001). $\text{PbS}_{1-x}\text{Se}_x$ of excellent epitaxial quality has recently been demonstrated on the $\text{BaF}_2(111)/\text{Si}(001)$ films. Comparable epitaxial quality has been demonstrated for CaF_2 grown on Si(001) substrates using a two step growth method. We also report on preliminary results on epitaxial mixed fluoride growth on Si(111) and Si(001) substrates.

INTRODUCTION

It would be desirable for the semiconductor industry to have the ability to grow device quality epitaxial compound semiconductors onto Si substrates for VLSI applications. Due to the relatively small lattice parameter and thermal expansion coefficient of Si, heteroepitaxy of the most interesting semiconductors directly on Si substrates leads to insufficient quality. By using suitable buffer layers of CaF_2 , SrF_2 , and BaF_2 on Si substrates this problem could be overcome. The fluorides have the property of plastically deforming by the introduction of misfit dislocations when grown heteroepitaxially on lattice mismatched substrates [3]. Dislocations move freely in the fluorides removing any residual strain caused by lattice mismatch at temperatures as low as room temperature. The significant advantage in using the fluorides as buffer layers is due to their plastic properties. We have already demonstrated that GaAs, when grown on an epitaxial CaF_2 buffer layer results in over an order of magnitude reduction in residual strain [1,2]. However, the poor lattice match between GaAs and CaF_2 (4%) results in unacceptably high threading dislocation densities.

Recently we have installed a dual chamber MBE system whereby we can grow appropriate fluoride alloys in a Si MBE growth chamber and then transfer in UHV to a III-V MBE growth chamber. By lattice matching to GaAs or other compound semiconductors with fluoride buffer layers on Si substrates, we hope to alleviate the high dislocation densities observed for GaAs on CaF_2 . Here, we will report on our recent work on substrate engineering with epitaxial fluoride buffer layers on Si substrates.

PROCEDURES AND APPARATUS

The Si wafers were chemically cleaned using steps similar to those of Ishizaka, et al [4]. The wafers were then introduced into a VG Semicon VG90S silicon MBE system which was used to grow the fluoride layers. Typical base pressures were in the 10^{-11} mb range and during deposition in the 10^{-9} mb range. The majority of the layers were grown at a fixed substrate temperature in the range from 500°C to 800°C after the Si substrate had been thermally cleaned at 800°C for 10 min. Sometimes an intermediate Si buffer layer was grown but we have found that this is not generally necessary for obtaining high quality, epitaxial fluoride growth.

The Knudsen cells used to evaporate the fluorides were designed and built specifically for this purpose by us [5]. A pyrolytic-graphite-coated, graphite heating element is used which is capable of achieving crucible temperatures up to 1600°C . A tapered crucible design is used which allows deposition with excellent uniformity over a 6"-dia. wafer ($\pm 3\%$) with the crucible end approximately 34 cm away from the substrate. Graphite was chosen

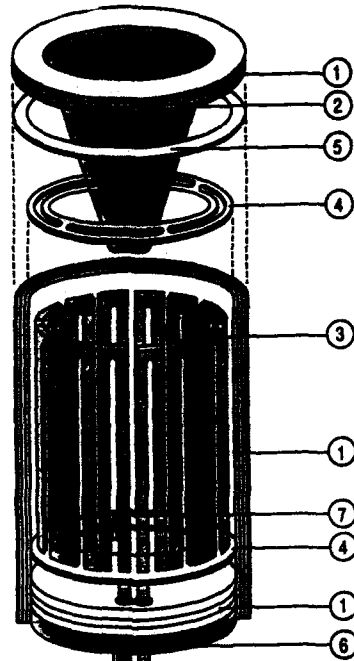


Fig. 1: Artist's rendition of the Knudsen cell with: 1) Ta radiation shielding; 2) pG crucible; 3) graphite heating element; 4) pBN rings; 5) Ta ring; 6) Mo base plate; and 7) W-Re thermocouple.

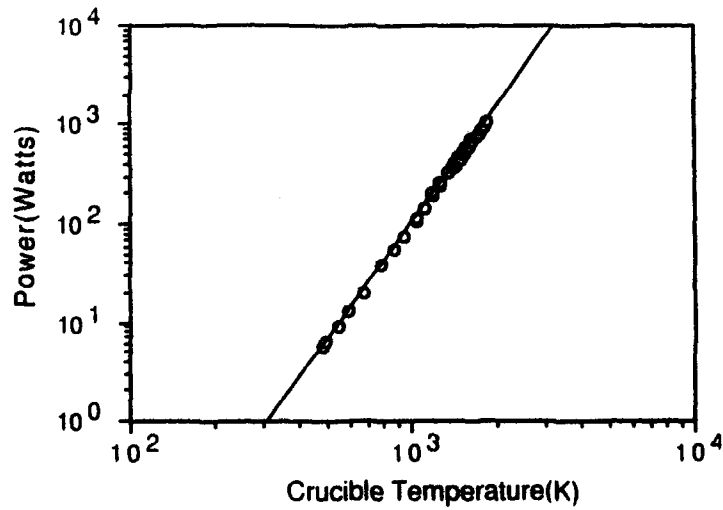


Fig. 2: Plot of power consumption versus crucible temperature.

for the heating element material due to low vapor pressure at high temperatures. High purity graphite was used in order to obtain cleanliness consistent with MBE growth of semiconductors.

The crucibles are made of pyrolytic graphite instead of the more common pyrolytic boron nitride (pBN) because it is well known that the fluorides react with the pBN [6]. Figure 1 is a partially exploded view of the K-cell with the major components identified. Power is supplied to the suspended heating element via Ta wire fastened to the element with Mo screws and nuts. A thermocouple is supported by the bottom pBN ring as shown. Both the power and thermocouple leads are insulated with alumina tubes that extend from the flange up to the base of the K-cell.

The power consumption of the K-cell was calculated from current and voltage measurements using a D.C. power supply over the crucible temperature range 200°C to 1550°C. Figure 2 is a plot of power (Watts) versus crucible temperature (K). The line fitted to the points has a slope of 3.9, close to the value of 4.0 expected for an ideal black body. An optical pyrometer (emissivity set at 0.8) was used at high temperatures to calibrate the thermocouple and this calibrated thermocouple was used.

Fluoride evaporant fluxes from 0.01 nm/s up to over 5 nm/s can be maintained with the K-cells. At a typical CaF_2 growth rate of 0.15 nm/s, 675W of heater power is supplied at 45V and 15A. From residual gas analysis the partial pressure of mass 28 species (primarily N_2 and CO) at these operating conditions is about 2×10^{-9} mb indicating that the level of the K-cell's pBN component disassociation is tolerable. This partial pressure is in the low 10^{-10} mb range during typical BaF_2 deposition.

RESULTS AND DISCUSSION

Fluoride films have been grown on both (111) and (001) oriented Si wafers. High crystalline quality CaF_2 and SrF_2 layers have been deposited on the (111) oriented wafers with layer thicknesses ranging from 0.2 to 1.0 microns. This work confirms similar earlier results [7]. A typical substrate temperature during growth was 550°C with growth rates of 0.2-0.3 nm/s. Ion channeling χ_{min} 's for these layers are below 5% and dark field optical microscopy revealed no signs of cracked layers. This is expected from previous studies where it was shown that the strain due to thermal and lattice mismatch is entirely taken up by dislocation motion (plastic deformation) [3]. RHEED indicated no surface reconstruction.

High crystalline quality CaF_2 and BaF_2 have also been grown on Si(001). The growth conditions for the BaF_2 layers were the same as those used for the CaF_2 and SrF_2 on Si(111) substrates. X-ray diffraction (XRD) confirmed that the BaF_2 layers are completely (111) oriented for thicknesses ranging from 0.2 to 1.25 microns. This phenomena has been reported by earlier workers [7]. RHEED patterns were streaky indicating 2-D growth and exhibited a "1/4x" reconstruction (Figure 3a). By using RBS channeling measurements to map the planar BaF_2 (111) channels on top of the planar Si(001) channels an alignment of one of the threefold symmetric {110} planes of the BaF_2 with one of the fourfold symmetric (110) and (110) planes of the Si was seen (Figure 3b). The central axial (111) and (001) channels of the BaF_2 and the Si, respectively, do not lie exactly on top of one another indicating slight orthogonal misalignment.

The χ_{min} 's of these layers were at best better than 4.0% for the Ba and dark field optical microscopy revealed fine irregularly cracked surfaces. The cracking probably occurs during cooling due to the large thermal expansion mismatch between BaF_2 and Si. This cracking behavior is quite different from previous results on CaF_2 (111) suggesting that the BaF_2 (111) layers, when grown directly on Si(001) are unable to allow dislocation motion to remove the thermal mismatch strain in the film.

Recently, excellent epitaxial quality $\text{PbS}_{1-x}\text{Se}_x$ has been deposited on our BaF_2 grown on Si(001) substrates [8]. The $\text{PbS}_{1-x}\text{Se}_x$ is (111) oriented when grown on top of the (111) BaF_2 . These $\text{PbS}_{1-x}\text{Se}_x$ layers were grown in a separate MBE system so the BaF_2 films were exposed to atmosphere prior to II-VI growth. The lattice mismatch between Si and $\text{PbS}_{1-x}\text{Se}_x$ is <11.3% at room temperature whereas BaF_2 has a 14% mismatch with Si.

It is much more difficult to obtain smooth, epitaxial growth of fluoride films along the (001) direction due to the high surface free energy of the bulk terminated fluoride in this direction [9,10]. Generally, (001) CaF_2 growth on Si(001) substrates proceeds with 111 facets. This growth preference can be overcome by employing a two step growth method



Fig. 3a: RHEED pattern of (111) oriented BaF_2 on $\text{Si}(001)$ exhibiting a smooth surface with a "1/4x" reconstruction.

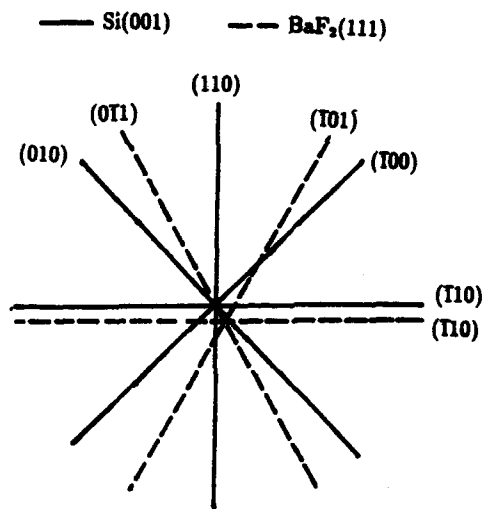


Fig. 3b: Representation of stereographic projections of the three {110} planes of (111) BaF_2 , aligned with either the (110) or the (110) plane of the (001) Si.

that results in smooth films [11]. The method used by us includes an initial nucleation stage at a substrate temperature of about 550°C where a 50-100 nm thick film is deposited followed by a ramp in substrate temperature up to about 750°C where a second, smooth layer is grown. Spotty RHEED patterns are observed during the nucleation stage exhibiting faceting along $\langle 111 \rangle$ directions. This is followed by streaky RHEED during and after the final growth step with only faint signs of faceting (Figure 4). The CaF_2 layers grown by this method are crack-free and of excellent crystalline quality ($\chi_{\text{min}} < 5.0\%$). They are (001) oriented as confirmed by XRD and were typically on the order of 100nm thick.

We have also done some preliminary work on alloyed fluoride layers. $\text{Ca}_{0.98}\text{Ba}_{0.02}\text{F}_2$ has been grown on both (001) and (111) oriented Si wafers. The films were grown at a fixed substrate temperature of 550°C at a growth rate of 0.2-0.3nm/s. The best χ_{min} 's of 7.6% for Ca and 53% for Ba of a film less than 100nm thick was achieved on the (111) substrates. These results indicate that the BaF_2 does not incorporate well within the CaF_2 lattice. Similar poor results were obtained for alloys with identical concentrations and similar growth procedures on (001) wafers.

RBS measurements made on these alloyed layers indicate nonuniform mixing of the BaF_2 and CaF_2 . The 5% value quoted for the BaF_2 concentration is only an average value that typically fluctuated from about 1.5% up to about 6.0%. It is known that BaF_2 and CaF_2 are not miscible for all concentrations which probably accounts for this behavior [12].

$\text{Ca}_{0.52}\text{Sr}_{0.48}\text{F}_2$ has also been grown directly on Si(001), on $\text{CaF}_2/\text{Si}(001)$ and on graded mixed fluoride layers on Si(001). CaF_2 and SrF_2 are miscible over the entire range of concentrations making it a more attractive candidate to use in lattice matching to GaAs which would require about a 50-50 mixture. The χ_{min} 's for these layers were approximately equivalent for both Ca and Sr at 25%. Presently we do not believe that optimal growth conditions for these alloys have been realized.



Fig. 4: RHEED pattern of (001) CaF_2 on (001) Si exhibiting a smooth surface with Kukuchi lines and faint signs of faceting.

SUMMARY AND CONCLUSIONS

Alloyed fluoride epitaxial layers can be used as lattice matched buffer layers for subsequent compound semiconductor growth on top. In particular, GaAs can be lattice matched with $\text{Ca}_{1-x}\text{Ba}_x\text{F}_2$ at an x value of about 0.25 or with $\text{Ca}_{1-x}\text{Sr}_x\text{F}_2$ at an x value of about 0.50. The $\text{CaF}_2/\text{SrF}_2$ alloys are more favorable candidates for these applications since they form a complete set of solid solutions whereas the $\text{CaF}_2/\text{BaF}_2$ alloys do not. The fluorides have the advantageous property of being able to plastically deform via dislocation motion even at room temperature. In our laboratory we are able to grow mixed fluorides in a Si MBE system and then transfer in UHV to a III-V MBE system for compound semiconductor growth. We have designed and built two high temperature Knudsen cells for fluoride evaporation that can achieve crucible temperatures up to 1600°C and film thickness uniformities of $\pm 3\%$ over a $6''$ wafer.

Excellent epitaxial quality CaF_2 and SrF_2 layers have been grown on Si(111) as well as CaF_2 and BaF_2 layers on Si(001). The BaF_2 layers on Si(001) were completely (111) oriented and aligned laterally with one planer direction in the Si(001) and slightly misaligned perpendicularly with the Si(001). Excellent epitaxial quality $\text{PbS}_{1-x}\text{Se}_x$ has been grown on these BaF_2 layers. Smooth CaF_2 layers were grown with a two step-growth process.

ACKNOWLEDGEMENTS

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PART VIII

**Novel Materials and
Growth Techniques**

Gas Source Silicon Molecular Beam Epitaxy

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Abstract

Gas source silicon molecular beam epitaxial (Si-MBE) growth is microscopically governed by a dissociative adsorption of silicon hydrides, such as Si_2H_6 source gas molecules on Si surface. The dissociative adsorption generates SiH species on the surface. From this hydride phase, hydrogen desorbs thermally. The temperature dependence of the growth rate indicated that the hydrogen desorption from the SiH is the rate limiting step. In HBO_2 Knudsen cell doping, B adsorbates block the surface migration. Such a blocking effect can be avoided by B_2H_6 gas dopant, because of the similar incorporation mechanism of B_2H_6 to that of Si_2H_6 . However, in PH_3 gas doping, a crystal quality degradation was observed at a high doping range due to the preferentially high sticking coefficient of PH_3 and the resulting surface dangling bond termination. The selective epitaxial growth of a B doped layer using Si_2H_6 and B_2H_6 was applied to a novel structured base fabrication for super self-aligned selectively grown base transistor (SSSBT). A successful achievement of the SSSBT fabrication indicates the high potentiality of gas source Si-MBE to the sub-micron size ultra-high speed bipolar large scale integrated (LSI) circuits.

Introduction

Si has superiority as an electronic material because of its manufacturability and a high quality and stable insulator of SiO_2 . This is the reason why Si is still a winner in large scale integrated circuits (LSI) technology, in spite of rapid progress in GaAs and related compound device technology. But, in Si LSI technology, the device size becomes small to a limit of the conventional technology. For a technical breakthrough, a new epitaxial growth technique for sub-micron size devices are strongly demanded. Si molecular beam epitaxy (Si-MBE) has a monoatomic layer thickness controllability [1]. It also enables an abrupt doping profile [2]. These advantages are attractive for high speed device fabrications. However, for advanced devices, not only the film thickness controllability but also the controllability in the lateral dimensions of the device active region are required. For the lateral size control, a selective epitaxial growth is favorable. Unfortunately, in the conventional e-gun evaporator type

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Si-MBE, the selective epitaxial growth is very difficult [3]. To include the advantageous selective growth to the Si-MBE technology, we have started the study on gas source Si-MBE.

At the start of our study, we have defined the gas source Si-MBE as the epitaxial growth technique governed by the surface reaction of gas molecules on Si surfaces. To realize this condition, the pressure during the growth should be low enough to avoid the contribution of the gas phase reaction (e.g. thermal decomposition of gas molecules) to the growth. By lowering the pressure, the gas molecule's behavior changes from the viscous flow to the molecular flow. In the molecular flow region, the above mentioned condition is achieved. In this region, the characteristic boundary region and the flow pattern problems [4] of chemical vapor deposition (CVD) can be avoided. Since the pioneering work of Joyce and Bradrey [5], silane (or disilane) molecular beam interactions with Si surfaces have been investigated by a few authors. [6-8] Their experimental conditions were similar to our gas source Si-MBE, though they have intended to clarify basic CVD reactions. However, a nozzle beam method in their experiments was unfavorable for the growth on a large wafer with an adequate film thickness uniformity. In our gas source Si-MBE, we have discarded the nozzle beam method and have adapted a large caliber gas cell. To obtain a reasonable growth rate, the pressure during the growth was set at around the upper limitation for the molecular flow region, where the mean free path of the gas molecule is equivalent to the representative length of the apparatus. With these premises, we have examined the potential of gas source Si-MBE as a new epitaxial growth method. In the following, first we explain our experimental apparatus. Next, we shed a light on the gas source Si-MBE growth mechanism with a viewpoint of the surface reaction. The dissociative adsorption and the surface migration of the Si_2H_6 gas molecules are discussed. Gas doping effect on the growth is also discussed. Finally, the selective epitaxial growth and its application to a novel-structured bipolar transistor are described. The results of $\text{Si}_{1-x}\text{Ge}_x$ alloy growth are also shown.

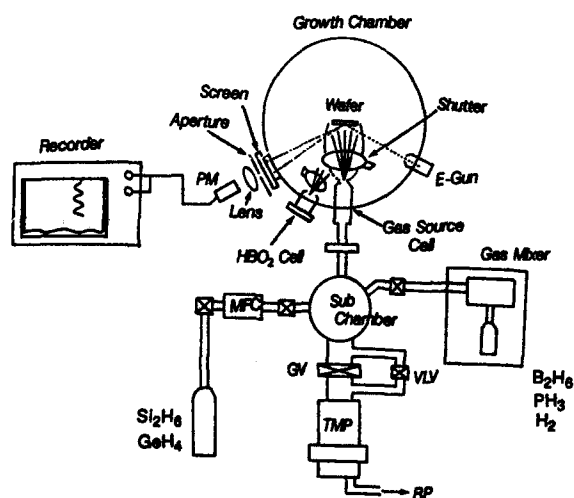


Fig.1 Gas source Si-MBE apparatus.

Experimental apparatus

The gas source Si-MBE apparatus is schematically shown in Fig.1. It consists of a main growth chamber, a subchamber (not shown in the figure), a sample exchange chamber and a gas mixing system. The base pressure of the main chamber was 10^{-10} Torr. For the growth, 100% Si_2H_6 was used as a source gas. B and P dopings were achieved with 5% B_2H_6 (diluted by H_2) and 5% PH_3 (diluted by SiH_4) gases, respectively. Pure GeH_4 was also combined for the $\text{Si}_{1-x}\text{Ge}_x$ alloy growth. Doping gas flow rates were controlled by the gas mixing system. The gas mixing system was designed to cover a wide doping range over 10^5 with one doping gas bomb, which was impossible in an usual single mass flow controller (MFC) method. The precise design of the mixing system has been described elsewhere [9]. During the growth, source gases were supplied toward the sample wafer through the gas cell. The gas cell has a 1cm diameter single-hole aperture. The pressure during the growth was less than 10^{-5} Torr. The wafer size was 4 inch.

In the main chamber, a reflection high energy electron diffraction (RHEED) system, a quadrupole mass spectrometer (QMS) for a residual gas analysis, a gas cell for the MBE growth, an electron cyclotron resonance (ECR) cell (not shown in the figure) for a source gas cracking [10], and a HBO_2 Knudsen cell (K-cell) for the B doping were equipped. In an usual growth, source gas was supplied through the gas cell. Only for a surface H-termination [10] and a low temperature surface cleaning by SiH_2 [11], the ECR cell was operated. B doping was possible both by the B_2H_6 gas doping and the HBO_2 K-cell doping. The difference between these two doping methods was discussed in the latter part. The intensity observation of the RHEED spots was also possible by an optical system [12].

The source gases of Si_2H_6 , GeH_4 , and the dopant gases of PH_3 , B_2H_6 are toxic and/or combustible. A special caution was paid to the evacuation system. The main, sub- and the exchange chambers are evacuated by chemical type turbo molecular pumps (TMP) and rotary pumps. Besides the TMP, the main chamber had an ion pump (IP), Ti getter pump and a liquid nitrogen shroud. During the growth, the main chamber was evacuated by the TMP and the liquid nitrogen shroud. All TMPs and rotary pumps were always purged by dry N_2 . The end of the evacuation pump was connected to a gas disposition system by stainless lines.

Gas Source Si-MBE Growth Mechanism

For the gas source Si-MBE growth, source gas molecules (Si_2H_6) should dissociatively adsorb on Si surfaces. This process is fundamental for the gas source Si-MBE growth. Hence, a basic understanding of this process is necessary. In the adsorption process, an initial sticking coefficient is an important parameter. For the gas source Si-MBE growth, SiH_4 , Si_2H_6 and Si_3H_8 are candidates for the source gas molecule. In recent series of works by Gates et. al. [13-15], the initial sticking coefficient of SiH_4 and Si_2H_6 have

been reported to be in the order of 10^{-5} and 10^{-1} , respectively. To obtain a reasonable growth rate, a large sticking coefficient is favorable. In fact, more than 10 times larger growth rate of Si_2H_6 gas source Si-MBE has been observed than that of SiH_4 one [16]. The superiority of Si_2H_6 as the source gas is clear. Hence, hereafter, we only discuss Si_2H_6 gas source Si-MBE in this article.

For the epitaxial growth, the dissociation after the adsorption is also indispensable [17]. The dissociation process of Si_2H_6 molecule on Si(100) [18] and Si(111) [19] surfaces have been reported recently. At $T=80\text{K}$, Si_2H_6 associatively adsorbs on both surfaces. This associative adsorption has been confirmed by observing the Si-Si bond related peak of Si_2H_6 in high resolution electron energy loss spectrum (EELS) and ultra-violet photoelectron spectrum (UPS). With the temperature raise, the Si-Si peak disappears at around 200K and the Si_2H_6 dissociates into SiH_3 species [15,19]. At $T>525\text{K}$ on Si(100) and $T>700\text{K}$ on Si(111) surfaces, SiH is generated after the thermal decomposition of SiH_3 species. However, on Si(111) surface, the decomposition path is expected to include SiH_2 [13] because the SiH_2 -related B_2 state has been reported in the H_2 temperature programmed desorption (TPD) on $\text{Si}_2\text{H}_6/\text{Si}(111)$ system. Kulkarni et al. have also indicated that a dynamical Si_2H_6 beam interaction with Si(111) surface generates a SiH_4 gas molecule and a SiH_2 adsorbate by modulated beam scattering experiments [20,21]. Two possible decomposition path for SiH_2 has also been pointed out [13].

But anyway, at gas source Si-MBE growth temperatures of 500-600C, all these studies showed that the surface was covered by SiH species as a results of Si_2H_6 dissociation. [18-20]. One cycle of a monolayer epitaxial growth is completed after the hydrogen desorption from this hydride surface. This hydrogen desorption process is an important one for gas source Si-MBE, because a drastic decrease of the Si_2H_6 sticking coefficient has been reported on the hydrogen covered Si surfaces [13,19]. Moreover, a slow time scale for the hydrogen desorption has been observed in the Si_2H_6 modulation beam scattering on Si(111) surface [20,21]. Therefore, in the gas source Si-MBE growth, the hydrogen desorption from SiH hydride phase is expect to limit the total growth rate.

The Si_2H_6 intensity and the substrate temperature dependences of the gas source Si-MBE growth rate on Si(100) surface are shown in Fig.2. As shown in the figure, the growth rate saturated at large flow rates. This tendency became obvious at low growth temperatures. The growth rate saturation indicates that the growth is governed by a surface thermal reaction. In fact, the Arrhenius plot of the saturated growth rate and the substrate temperature showed an activation energy of 46Kcal/mol, which agrees with a reported value for H_2 desorption from Si(100) monohydride phase [22]. Though the kinetic order of the H_2 desorption from the hydride surface [22], the H adsorption site (especially on the Si(111)7x7 DAS surface [23]), and the H adsorption form [24] are still controversial, this agreement gives a following basic understanding on the gas source Si-MBE growth mechanism. At a small Si_2H_6 intensity, the

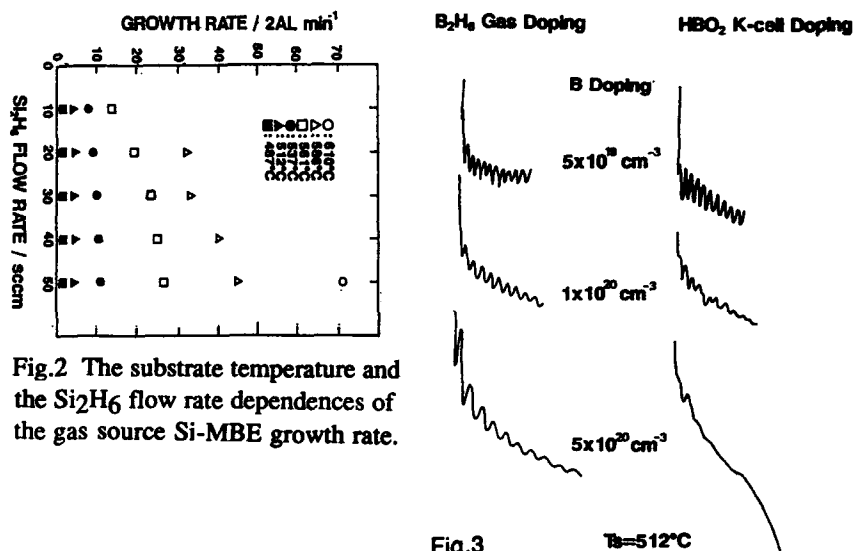


Fig.2 The substrate temperature and the Si_2H_6 flow rate dependences of the gas source Si-MBE growth rate.

Fig.3

Fig.3 RHEED intensity oscillation during gas source Si-MBE under HBO_2 K-cell doping (right side) and B_2H_6 gas doping (left side).

growth rate is proportional to the intensity (supply-limit region). But, at a large intensity, the incident rate of Si_2H_6 exceeds the thermal desorption rate of hydrogen from the growing surface. Hence, the growth rate saturates at the value which is governed by the H_2 desorption from SiH surface (reaction-limit region). The maximum growth rate is limited by the H_2 thermal desorption rate. This maximum rate is, of course, growth temperature-dependent. Judging from the onset of the H_2 TPD peak [13], a practical lowest growth temperature for gas source Si-MBE is thought to be around 400C.

Surface Migration and Dopant Incorporation

To obtain a high quality epitaxial film, a role of surface migration is important [25]. In the conventional e-gun evaporator type Si-MBE, the surface migration has been studied using RHEED intensity oscillation [26]. The intensity oscillation is attributed to the 2-dimensional nucleation and growth process [27] with the foreign Si atom's migration on the Si surface. During the gas source Si-MBE growth, the RHEED intensity oscillation has also been observed [12]. An example of RHEED intensity oscillations in gas source Si-MBE growth on Si(100) surface is shown in Fig.3. In our gas source Si-MBE, SiH species after Si_2H_6 dissociative adsorption is a candidate of the migration [20,21]. SiH is expected to be more mobile than the elementary Si, because of its weaker bonding energy to the surface. In Fig.3, an effect of B doping on the oscillation was also examined both in HBO_2 K-cell doping and B_2H_6 gas

doping. At high HBO₂ dopings above 10^{20} cm^{-3} , the oscillation disappeared. For this suppression of the oscillation, the following two reasons are mentioned. One is the dangling bond termination by adsorbed B dopant atoms. The other is the disturbance of the SiH surface migration by B dopant atoms on the surface. Judging from a large binding energy of B-Si bond, B atoms are thought to be less mobile than SiH and obstruct the surface migration. To determine the reason for the suppression of the RHEED intensity oscillation, we observed the RHEED oscillation on B-precovered Si(100) surfaces. The result indicated that the oscillation disappeared at the B precoverage above 0.2 monolayer. [28] This coverage is too small to terminate all the surface dangling bonds and, therefore, strongly suggests the latter phenomena; the disturbance of surface migration by B atoms. Moreover, a continuous RHEED intensity oscillation was observed on the Si(111) 3x 3-B surface, though the surface B coverage was 1/3 monolayer [29]. This is because the B atom on the 3 structure occupied the subsurface site [30] and does not disturb the surface migration. These results support the disturbance of the surface migration on Si(100) surface by B dopant atoms as a reason for the RHEED intensity oscillation's disappearance in HBO₂ K-cell high dopings.

On the contrary, in the B₂H₆ gas doping, RHEED intensity oscillation continued even at a high doping range. (left side of Fig.3) This is thought to be due to the dissociative adsorption kinetics of B₂H₆ on Si surfaces. For B₂H₆ doping, the dissociative adsorption is necessary to be incorporated into the epitaxial layer as a elementary B atom. In fact, the B carrier concentration was found to be proportional to the B₂H₆/Si₂H₆ flow rate ratio in B₂H₆ doping. This relationship holds even if we fixed the B₂H₆ flow rate and changed the Si₂H₆ flow rate from the supply-limit to the reaction-limit range. However, in the reaction-limited region, the sticking coefficient of Si₂H₆ is governed by the hydrogen coverage. Hence, the linearity of the doping concentration in the reaction-limited region strongly suggests the similar B₂H₆ dissociative adsorption process to the Si₂H₆ one. In this dissociative adsorption, B₂H₆ generate a mobile BH which is expected to be incorporated similar as SiH and, at least, not to disturb the surface migration of SiH. This is thought to be the reason for the continuous RHEED intensity oscillation even at a high doping range.

For n-type doping, PH₃ dopant gas was available in gas source Si-MBE. P is favorable for high n-type doping because of its high solubility limit above 10^{20} cm^{-3} in bulk Si. However in the conventional Si-MBE, most of all n-type doping have been achieved by Sb [31] because of the difficulty of P doping control due to its high vapor pressure. Hence, the PH₃ gas doping is one of advantages of gas source Si-MBE. In fact, a high doping above 10^{20} cm^{-3} has been achieved in the PH₃ gas doping. But, at a high doping, the growth rate decrease and the crystal quality degradation have been observed [32]. Recently, Bozso and Avouris have reported that PH₃ adsorption on Si(111) forms P:Si(111) 1x1 where all the surface dangling bonds are terminated [17]. This termination makes the Si surface chemically inert for gas source Si-MBE growth and causes the growth rate decrease and the crystal quality degradation.

With this respect, high n-type doping is still a problem of Si-MBE.

Selective Epitaxial Growth and Device Applications

As described above, the gas source MBE growth is governed by the dissociative adsorption. This enables the selective epitaxial growth of Si layer on SiO₂ patterned Si surfaces [33-35]. On the SiO₂, there are no chemically active dangling bond and the growth does not proceed, whereas the Si film epitaxially grows on Si surfaces. As stressed in the introduction, this selective epitaxial growth is indispensable for submicron size device fabrications. In this study, we examined the potentiality of gas source Si-MBE's selective epitaxial growth by applying it to the super self-align selectively grown base transistor (SSSBT). SSSBT is a prototype of submicron size bipolar LSIs. A cross sectional structure of SSSBT is shown in Fig.4. On this structure, an epitaxial base layer and a polycrystalline Si contact layer were grown at the same time by gas source Si-MBE. The B doping to the base and the contact layer was also automatically achieved by the B₂H₆ gas doping at the same time. The SSSBT growth procedure was briefly described below. Before loading to the MBE chamber, the SSSBT substrate was rinsed with a chemical solution (HCl:H₂O₂:H₂O=1:1:6) at 80C for 10 min. This solution removed surface contaminations and formed a protective thin oxide layer on the exposed Si area without etching Si and polycrystalline Si layers. (the usual NH₄OH:H₂O₂:H₂O=1:6:20 solution etches both Si and polycrystalline Si [36].) Because the etching is unfavorable for a fine device structure fabrication, the non-etching solution was used in this study. In the ultra-high vacuum MBE chamber, the protective oxide layer was removed by 850C, 15 min. annealing. Then, the 600A epitaxial Si base and the polycrystalline Si contact layers were grown by gas source Si-MBE at 561C with 70sccm Si₂H₆ flow rate. The growth rate was 70A/min. The B doping of $3 \times 10^{18} \text{ cm}^{-3}$ was achieved by B₂H₆ gas doping. To form the base contact automatically, the epitaxial base and the graft polycrystalline Si contact layers were grown even under the overhang structure till both layers touch each other.

The cross sectional scanning electron microscopy (SEM) photograph for the SSSBT before the growth (a), during the growth (b) and after the growth (c) are shown in Fig.4. As shown in Fig.4(c), the base and the contact layers were successfully grown by gas source Si-MBE. The growth under the overhang structure was achieved by obliquely incident molecules and scattered molecules at the SiO₂ side wall. The sticking coefficient of Si₂H₆ on Si(100) surface was in the order of 10^{-1} [13]. The value on polycrystalline Si was smaller than that on Si. Hence, under the overhang, the incident molecule is thought to contribute to the epitaxial growth after repeating billiard-like motions, which increase the effective flux intensity under the overhang. But, anyway, the effective incident flux under and around the overhang is different from that at the center part of the intrinsic base region. This ununiform flux distribution is a serious problem to obtain a flat base. However, this can be solved by the growth in the reaction-limited growth region. The flow rate for this SSSBT growth was larger enough than the critical value between the supply-limited and

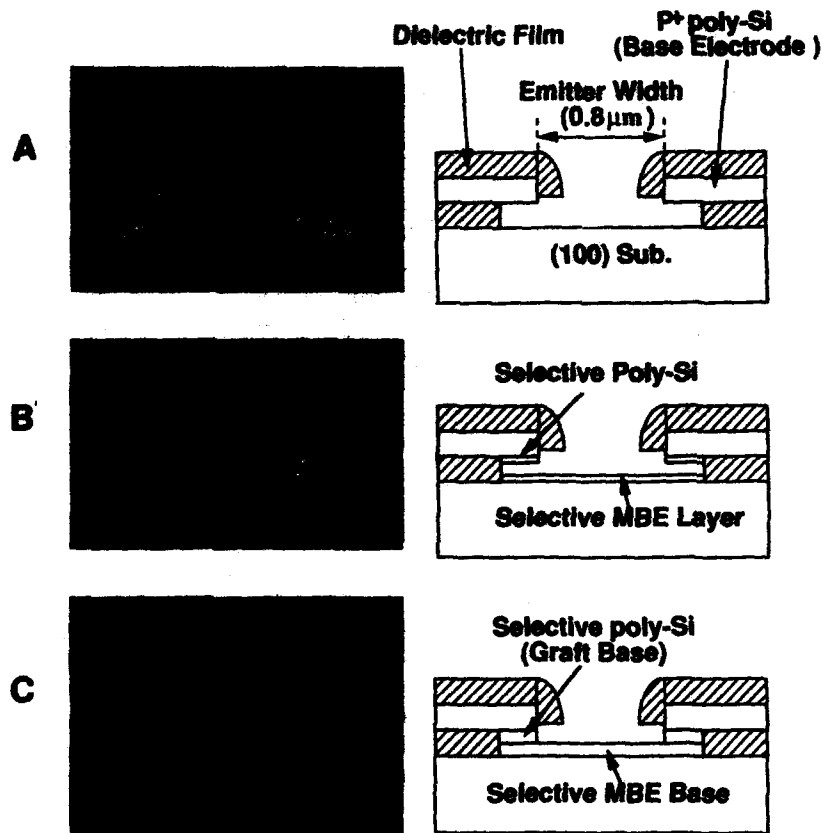


Fig.4 A cross sectional SEM images of the base and the contact layers growth for SSSBT. (a) before the growth, (b) during the growth and (c) after the growth.

the reaction-limited region. As described above, in the reaction-limited region, the growth rate was independent on the flow rate. This enables the same growth rate at the center and under the overhang in spite of the ununiform beam intensity. Moreover, a facet formation was found to be suppressed at a large flow rate growth [37]. Due to these reasons, a flat base layer of Fig.4(c) was obtained. Concerning the B doping, B_2H_6 is expected to be incorporated by the similar process to Si_2H_6 . This also worked effective to a uniform doping on the complicated SSSBT structure.

After the base layer growth, the transistor was fabricated by the following process. [38] On the base layer, a SiO_2 film was deposited by CVD. An emitter window was opened anisotropically by a reactive ion etching technique and the polycrystalline Si layer for the emitter electrode was deposited by CVD.

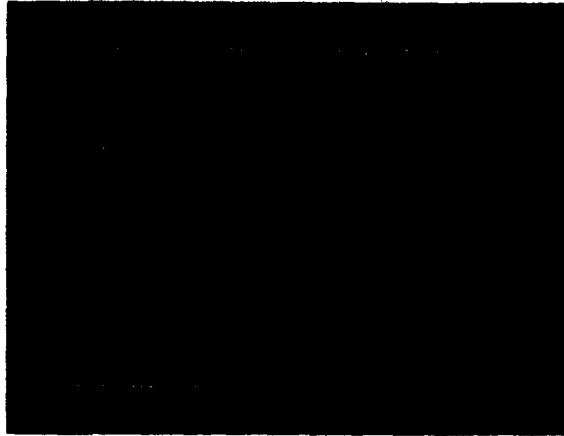


Fig.5 Common-emitter I-V characteristic of the fabricated SSSBT.

The doping for the emitter was achieved by $1 \times 10^{16} \text{ cm}^{-2}$ arsenic ion implantation (I/I) and the following rapid thermal annealing. The fabricated SSSBT showed a normal common-emitter current-voltage (I-V) characteristics as shown in Fig.5, the maximum current gain of which was 70. The normal I-V characteristic shows that gas source Si-MBE enables the simultaneous self-aligned base and the contact layer fabrications. This result indicates the high potentiality of gas source Si-MBE for its application to a sub-micron size self-aligned processing in ultra-high speed bipolar and BiCMOS LSIs.

Si_{1-x}Ge_x Alloy Growth

For a high performance bipolar device design, a heterojunction bipolar transistor (HBT) is promising. Especially, in the Si device technology, Si_{1-x}Ge_x alloy has been paid attention as a candidate of HBT material. In fact, very recently, an ultra-high speed performance of Si_{1-x}Ge_x based HBT ($f_T=90\text{GHz}$) has been demonstrated [39]. For a further development of Si_{1-x}Ge_x base HBT LSIs, the selective epitaxial growth of Si_{1-x}Ge_x alloy is desirable. With this respect, we have studied the gas source MBE growth of Si_{1-x}Ge_x alloy. As results, Si_{1-x}Ge_x selective epitaxial growth on a SiO₂ patterned Si(100) has been found to be possible [40]. This selective epitaxial growth has been applied to a primitive Si_{1-x}Ge_x based HBT fabrication [41,42]. However, in those studies, GeH₄ was used as a Ge source. In GeH₄ MBE, a high temperature about 600C is necessary to obtain a reasonable growth rate. This rather high temperature is due to the high kinetic barrier for GeH₄ dissociative adsorption. On the other hand, according to a multiple internal reflection infrared spectroscopy (MIRIRS) study on Ge₂H₆/Ge(111) surface, Ge₂H₆ has a similar dissociative adsorption process to Si₂H₆ [43]. The temperature range of the dissociation was also similar to Si₂H₆, that is

favorable for low temperature $\text{Si}_{1-x}\text{Ge}_x$ growth. Moreover, in a future gas source Si-MBE application to $\text{Si}_{1-x}\text{Ge}_x$ base SSSBT, the similar incorporation process is important to insure a Si/Ge ratio uniformity over the whole base region, just in the case of B_2H_6 doping. Hence, Ge_2H_6 gas source MBE study will be important, though the Ge_2H_6 adsorption process on $\text{Si}_{1-x}\text{Ge}_x$ alloy surface is still unknown.

Conclusion

Gas Source Si-MBE growth is governed by the dissociative adsorption of Si_2H_6 . At the growth temperature range, most of surface species was SiH. The hydrogen thermal desorption from this SiH phase limits the maximum growth rate. B doping by K-cell caused the suppression of the surface migration at high dopings. On the other hand, in B_2H_6 gas doping, the continuous RHEED intensity oscillation was observed. This is thought to reflect the similar dissociative incorporation process of B_2H_6 to Si_2H_6 . For n-type doping, PH_3 gas doping enables a high doping. But the crystal quality degradation was observed at high dopings due to the surface dangling bond termination by P during the PH_3 doping. With Si_2H_6 and B_2H_6 , the self-aligned base and the contact layers growth for SSSBT was achieved. The normal I-V characteristics of the fabricated SSSBT indicates the high potentiality of gas source Si-MBE for its application to a sub-micron size ultra-high speed bipolar and BiCMOS LSIs. The successful growth of the base and the contact layer even under the overhang structure of SSSBT is thought to be due to the proper sticking coefficient of Si_2H_6 and B_2H_6 , and the similar adsorption kinetics of both gas molecules. With this respect, a basic understanding of the adsorption dynamics becomes more important for a future advance of the gas source Si-MBE technology.

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RTP-CVD OF SI MATERIALS AND DEVICES FOR ULSI APPLICATIONS

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ABSTRACT

Rapid thermal processing chemical vapor deposition (RTP-CVD) has received considerable attention because of its ability to reduce many of the processing problems associated with thermal exposure in conventional chemical vapor deposition, while still retaining the ability to grow high quality epitaxial layers. In this paper, the principles of the RTP-CVD system are described, followed by results of experiments on *in-situ* cleaning, undoped Si epitaxy and *in-situ* doped Si epitaxy, and selective Si deposition using oxide masks. Our results show that RTP-CVD is capable of growing high quality, epitaxial layers with sharp dopant transition profiles. Selective deposition was achieved without the use of HCl. We also studied the growth and characterization of $\text{Ge}_x\text{Si}_{1-x}$ films for optical waveguiding.

INTRODUCTION

As device dimensions continue to shrink down into the submicron regime in pursuit of higher integration density and better circuit performance, dopant spreading becomes more and more intolerable and more stringent requirements are imposed on the deposition process. At conventional epitaxial growth temperatures, unintentional doping due to outdiffusion and autodoping may occur. Reducing dopant movement during processing is critical for bipolar and metal-oxide-semiconductor (MOS) device technologies. For future ultra-large scale integration (ULSI) and high-speed device applications, the capability of depositing thin Si epitaxial layers with an abrupt, well-controlled dopant transition profile is in increasing demand. The amount of thermal exposure to the Si wafer during the entire epitaxial growth procedure must be minimized. At the same time, high temperatures are needed to obtain high crystalline perfection. Therefore, exchanging temperature for time in an effort to reduce the thermal budget is not always possible, and short time, high temperature processing becomes increasingly important.

One method to limit thermal exposure time is rapid thermal processing (RTP). The properties of RTP prove to be particularly useful when combined with chemical vapor deposition (CVD) for growing high quality Si epitaxial films with precisely controlled dopant transition profiles. Limited reaction processing (LRP) [1] and the similar techniques of rapid thermal CVD (RTCVD) [2] and rapid thermal processing CVD (RTP-CVD) [3] are extremely attractive for the growth of ultra-thin Si epitaxial layers. Previous work has shown that these techniques are capable of growing high quality epitaxial Si [1-3] and $\text{Ge}_x\text{Si}_{1-x}$ layers [4,5], and selective epitaxial growth (SEG) [6] of Si.

RAPID THERMAL PROCESSING CHEMICAL VAPOR DEPOSITION

RTP-CVD has received considerable attention because of its ability to reduce many of the processing problems associated with thermal exposure in conventional CVD, while still retaining the ability to grow high quality epitaxial layers. RTP-CVD, as the name implies, is a combination of RTP and CVD. RTP-CVD utilizes rapid temperature cycling to start/stop the thermally-driven surface reactions of the CVD process. RTP-CVD is capable of ramping the temperature up to deposition temperatures in less than 3s. The wafer is capable of cooling down to below deposition temperatures in less than 2s. The large, quick, highly controllable temperature changes of RTP-CVD offer a viable means of growing precisely controlled, reproducible thin layers with low defect densities, while minimizing thermal exposure. Thus, RTP-CVD can provide sharp dopant transition profiles and a simple means of fabricating heavily-doped buried layer structures for bipolar junction transistor (BJT) and complementary

metal-oxide-semiconductor (CMOS) applications. As with conventional CVD, the actual growth rate can be controlled by a combination of source and carrier gas flow rates, deposition temperatures, and deposition pressures. RTP-CVD also offers the significant capability of *in-situ* multi-processing by rapidly changing the ambient between high temperature cycles, when the wafer is relatively cool and no deposition is occurring. Thus, RTP-CVD facilitates *in-situ* cleaning steps and deposition of multiple layers of different material compositions, such as layers of different dopants and doping levels and $\text{Ge}_x\text{Si}_{1-x}$ layers.

A schematic diagram of the RTP-CVD system is shown in Fig. 1. The RTP-CVD system is a single 4" wafer horizontal reactor consisting of a single-piece chamber made of high quality fused quartz specially designed to withstand external pressure during vacuum processing. The Si wafer is supported on three tapered quartz pins mounted on a quartz wafer holder which is attached to the water-cooled stainless steel door. The wafer is heated from above and below by radiant energy from two banks of nine nitrogen-cooled tungsten halogen lamps. The lamps and the quartz chamber are enclosed in a water-cooled stainless steel housing coated with highly reflective thin films to enhance the heating efficiency. The quartz chamber is highly transparent in the spectral range of the lamps, allowing the chamber to remain cool relative to the wafer and thereby embrace the advantages of a cold wall system. The cold wall design greatly minimizes chamber memory effects and reduces deposition on the reactor walls. The lamps can quickly heat up the wafer to 1200°C in less than 3s. The wafer temperature is monitored during the epitaxial growth by an optical pyrometer and is maintained according to the programmed time/temperature profile in a real-time closed-loop system by a microprocessor. Deposition is stopped by turning off power to the lamps, which allows the wafer to rapidly cool to room temperature, thereby stopping all thermally-driven surface reactions. All the process gases used are electronic grade and the gas flows are controlled by mass flow controllers. Chamber pressure is monitored and maintained in a closed-loop system consisting of a capacitance manometer, pressure controller, and throttle valve. Since the RTP-CVD system controls operate on a real-time closed-loop basis, very precise control over deposition parameters such as time/temperature profiles, gas flows, and chamber pressures can be achieved.

Epitaxial Si and $\text{Ge}_x\text{Si}_{1-x}$ films were deposited on (100)Si substrates in the RTP-CVD system. Substrate resistivities varied from 0.001 $\Omega\text{-cm}$ to 20 $\Omega\text{-cm}$ for n-type (Sb- or P-doped) and p-type (B-doped) substrates. Selective Si deposition experiments were performed on specially patterned wafers described below in the section on Selective Si deposition. Final *ex-situ* cleaning was performed by etching in dilute HF for 1 min, rinsing in deionized (DI) water, and blow drying with N_2 before being loaded into the chamber. The chamber was then pumped down to a base pressure of 1 mTorr or better. H_2 was used as the carrier gas. SiH_2Cl_2 and GeH_4 were used as source gases, while AsH_3 , B_2H_6 , and PH_3 were used as dopant gases.

IN-SITU CLEANING

A considerable amount of work has been done to minimize the contribution of the *in-situ* clean to the total process thermal exposure in order to reduce autodoping and broadening of an existing doping profiles. Numerous novel methods have been demonstrated for low temperature *in-situ* cleaning [7]. Recently, considerable interest has been directed toward utilization of a simple HF clean without rinsing with DI water. However, the most convenient and readily adaptable method is still a simple H_2 pre-bake. Therefore, we have examined the approach of reducing the processing temperature and time of the conventional H_2 pre-bake. Conventional H_2 pre-bakes are performed at temperatures $\geq 1000^\circ\text{C}$ at pressures on the order of Torr and higher. The primary function of the pre-bake is to remove any surface oxides prior to epitaxial growth. The reaction of O_2 and H_2O with the Si surface has been extensively studied [8,9]. At low O_2 and H_2O partial pressures and high substrate temperatures, the surface is free of SiO_2 due to the production of volatile SiO . The development of epitaxial reactors with low base pressures and low leak rates has resulted in lower background levels of impurities, allowing lower temperatures for *in-situ* cleaning and epitaxial growth. A H_2 pre-bake temperature as low as 850°C for 5 min at 10 Torr has been reported [10]. As long as the partial pressures of O_2 and H_2O are kept below the critical values for a given temperature, the fast oxide etching rates reported by Ghidini and Smith [8,9] should allow the pre-bake time to be reduced to the order of

seconds. The continued and nonuniform etching may cause surface damage in a prolonged and/or high temperature pre-bake process.

We studied the effects of the pre-clean using 60s bakes in H_2 at various base pressures and temperatures. The chamber pressure was held at 5 Torr during the pre-clean. Fig. 2 shows SEM micrographs of the sample surfaces after pre-cleans at different temperatures for a fixed base pressure. A high density of surface voids and a rough surface can be observed in Fig. 2(a) for the preclean at high temperature ($1000^\circ C$) and low base pressure (1.5×10^{-4} Torr). An interesting feature of the rectangular voids formed is that the sides are in $\langle 011 \rangle$ directions of the (100)Si substrate and are of different sizes. The surface is very rough in Fig. 2(b) for the preclean at high temperature ($1000^\circ C$) and high base pressure (7×10^{-4} Torr).

The defect densities in the subsequently grown Si layers are strongly dependent upon the H_2 pre-bake temperature and time. In general, lower chamber base pressures, higher pre-bake temperatures, and longer pre-bake times can introduce more surface damage, resulting in increased defects in the Si layer. Without lowering the chamber base pressure to the 10^{-4} Torr range, the lower temperature pre-bakes were ineffective in completely removing surface oxides. In our experiments, we observed that for chamber base pressures on the order of 10^{-4} Torr, a H_2 pre-bake at $800^\circ C$ for 15s gives satisfactory results in terms of both the quality of the resulting epilayer and the dopant transition profile. Nomarski micrographs of Schimmel-etched Si epilayers are essentially featureless.

UNDOPED Si EPITAXY

To become a commercially viable tool for Si epitaxy, RTP-CVD must provide sufficiently high growth rates to meet throughput goals. We have previously demonstrated that the growth rate remains constant for deposition times ≥ 10 s. The dependence of epitaxial growth rate on deposition temperature and SiH_2Cl_2 volume concentration for fixed deposition parameters of 1.2 lpm and 6 Torr is shown in Fig. 3. The transition between the mass transport limited and the reaction rate limited regions of growth occurs near $950^\circ C$. For temperatures below $950^\circ C$, the growth rate tends to saturate at a higher percentage of SiH_2Cl_2 due to the limited reduction rate for adsorbed $SiCl_2$ molecules at low temperatures [11]. When the deposition temperature is higher than $975^\circ C$, the growth rate increases linearly with the volume concentration of SiH_2Cl_2 . Under proper cleaning and deposition conditions, defect free epilayers have been easily grown by RTP-CVD at deposition temperatures $\geq 900^\circ C$. Below $900^\circ C$, a mixture of poly-Si and monocrystalline Si is often observed. Nomarski and TEM micrographs reveal defects, if any, consisted of isolated saucer pits, stacking faults, and interfacial precipitate-like defects.

Fig. 4 shows a secondary ion mass spectroscopy (SIMS) plot of B concentration as a function of depth and SiH_2Cl_2 volume concentration for undoped epilayers on heavily B-doped substrates and fixed deposition parameters of $1000^\circ C$, 750 sccm, and 10 Torr. The dopant concentrations abruptly drop three orders of magnitude in less than 400 Å, indicating minimal outdiffusion and autodoping occurred. Spreading resistance profiling (SRP) measurements verified the SIMS results. The SIMS profile in Fig. 5 shows that undoped epilayers deposited on heavily Sb-doped substrates show a sharp drop in Sb concentration of four orders of magnitude in less than 400 Å, while the C and O levels in the epilayer are comparable to the levels in the substrate. The deposition parameters were $1000^\circ C$, 90s, 10 sccm of SiH_2Cl_2 , 490 sccm of H_2 , and 6 Torr.

IN-SITU DOPED Si EPITAXY

In-situ doping allows almost any kind of dopant distribution profile to be realized, therefore precise control of the electrical characteristics of the epilayer can be achieved. Typical applications in CMOS involve growing a lightly-doped epilayer on a heavily-doped substrate. Bipolar applications commonly use a lightly-doped epilayer on a heavily-doped buried layer on a lightly-doped substrate. Recently, special interest has developed in epitaxial growth of thin heavily-doped buried layers for bipolar device applications. For a given base resistance and peak base doping, computer simulations have shown that a uniform base doping profile offers a

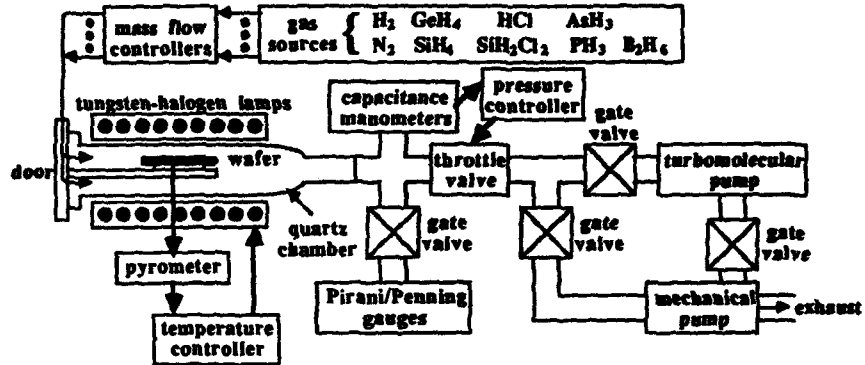


Fig. 1: A schematic diagram of the RTPCVD system.

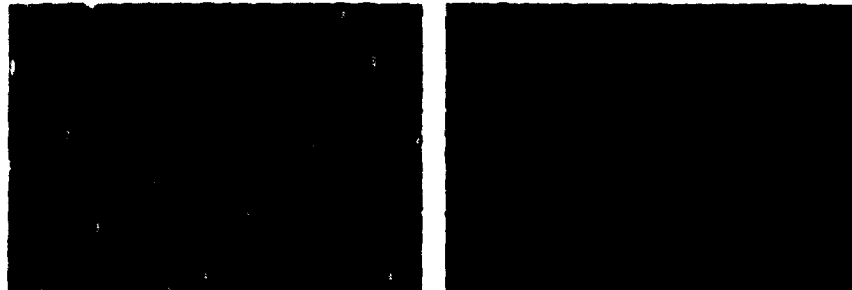


Fig. 2: SEM micrographs of sample surface after 60s preclean with base pressure and temperature of (a) 1.5×10^{-4} Torr and 1000°C , (b) 7×10^{-4} Torr and 1000°C .

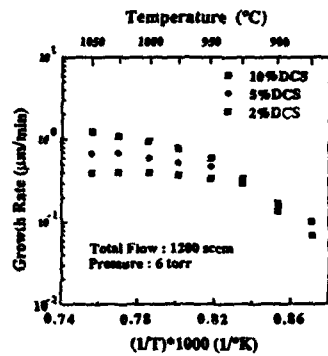


Fig. 3: Undoped Si epitaxial growth rates.

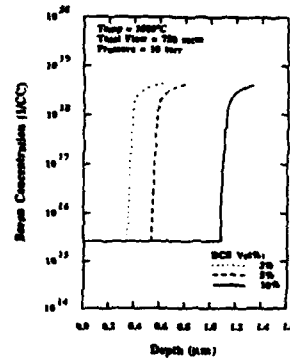


Fig. 4: SIMS depth profiles for undoped epilayers on heavily B-doped substrates.

higher cutoff frequency than a graded base doping profile [12]. Due to the B channeling effect, a thin base layer is difficult to obtain by implantation, even with low acceleration energies. Growing a thin heavily-doped epitaxial film for the base layer has been suggested as a solution.

N-type and p-type epilayers were grown at 1000°C with 250 ppm PH₃ and 5 ppm B₂H₆, respectively. A specular epitaxial surface can be reproducibly obtained by RTP-CVD for B and P doping. Nomarski micrographs of the as-deposited doped epilayers are featureless, but saucer pits could be observed after a dilute Schimmel etch. No stacking faults or dislocations were observed. Sharp, single crystal transmission electron diffraction (TED) patterns are obtained for B-doped epilayers for deposition temperatures between 950°C and 1000°C. However, polycrystalline rings can be observed in a few isolated areas of samples grown at 1050°C. The carrier concentration of the B-doped epilayers increases with deposition temperature, indicating that the B incorporation efficiency increases with temperature. Thus, the localized crystalline imperfections could be caused by B segregation in heavily-doped epilayers.

Carrier concentration profiles measured by SRP are shown in Figs. 6(a) and (b) for P- and B-doped epilayers, respectively. A nearly flat doping profile within the epilayers and a very abrupt transition at the epilayer/substrate interfaces are obtained for both P and B doping. The flat doping profiles and abrupt dopant transitions are significant in light of the fact the computer simulations have shown a uniform base profile is the optimum profile for high-speed BJT applications [12]. Change of carrier concentration from 10¹⁶ to 10¹⁸ cm⁻³ occurs within 300 Å. Fig. 7 shows SIMS depth profiles for a p⁺/p⁺/p⁻ buried layer structure grown on lightly B-doped substrates. The p⁺ buried layer and the p⁻ epilayer were grown at 1000°C with a SiH₂Cl₂ flow rate of 10 sccm and a total gas flow rate of 1 lpm for 10s and 90s, respectively. A B₂H₆ flow rate of 200 sccm was used to dope the buried layer. The SIMS profile shows the B concentration of 7×10¹⁹ cm⁻³ in the buried layer and a doping tail of less than 3×10¹⁶ cm⁻³ in the lightly-doped epilayer. The doping transitions are very abrupt, changing three orders of magnitude in less than 400 Å. The C and O levels in the epilayer are no higher than the levels in the substrate, even at the interfaces.

An interesting phenomenon we have observed with RTP-CVD is the ability of *in-situ* doping with As to reduce the minimum temperature at which epitaxial growth can be achieved. Our results strongly indicate that a basic physical mechanism similar to SPE enhancement still plays an important role in epitaxial growth by RTP-CVD. SPE studies have revealed that the SPE regrowth rate is enhanced by a high concentration of electrically active impurities (~0.1 at.%). Electrically active impurities are the dominant contributor to SPE enhancement [13]. Recrystallization of poly-Si can be enhanced by high concentration incorporation of impurities such as arsenic [14]. By SPE, epitaxial regrowth can be achieved at much lower temperatures (≤600°C) (66-67). These results suggest that the epitaxial growth temperature may be lowered by high concentration dopant incorporation.

Heavy doping with As and B has been reported to cause severe degradation of crystal quality using SiCl₄ as the Si source gas [15]. The observed degradations are believed to be due to particles falling from the reactor walls or generated by homogeneous nucleation. *In-situ* arsenic doping using AsH₃ in a conventional CVD reactor has been reported to cause significant film quality degradation at 800°C with SiH₄ as the Si source gas (68).

In our studies with RTP-CVD, we have observed that *in-situ* doping with As can reduce the minimum temperature at which epitaxial growth can be achieved. Our use of SiH₂Cl₂ as the Si source gas minimizes deposition on the reactor walls and homogeneous nucleation. TEM micrographs of undoped samples grown at 800°C with 5 vol.% SiH₂Cl₂ in H₂ reveal the films to be polycrystalline. Samples grown at a lower SiH₂Cl₂ concentration of 1 vol.% in H₂ at 800°C are still polycrystalline. We believe the poor film quality of undoped samples deposited at 800°C is mainly due to the background impurity level. Arsenic doping was obtained by adding dilute arsine (100 ppm AsH₃ in H₂) to the gas flow during the deposition. References below to the vol.% of arsine used are for the dilute arsine mixture and not pure arsine. Arsenic minimizes lattice stress compared to other dopants (*e. g.*, B and P) due to the small covalent radii difference (0.01Å), and thus reduces defect formation.

Fig. 8 shows TEM micrographs of *in-situ* doped epilayers grown at 800°C with 5 vol.% SiH₂Cl₂. The deposition parameters were identical for both samples with only the AsH₃ flow rate being varied. A significant reduction in defect densities can be observed in each successive micrograph. Fig. 8(a) shows the plan-view TEM micrograph and SAD pattern of a sample grown with 1 vol.% AsH₃. The film quality is monocrystalline with numerous defects such as

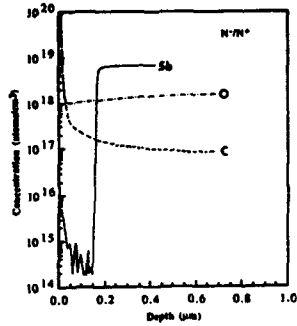


Fig. 5: SIMS depth profile for an undoped epilayer on a heavily Sb-doped substrate.

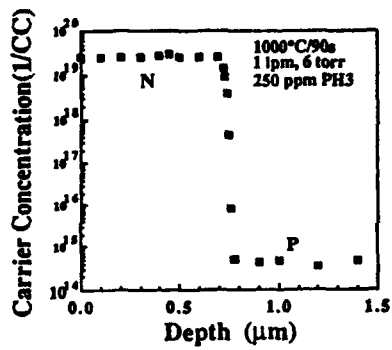


Fig. 6: SRP depth profiles for a P-doped epilayer.

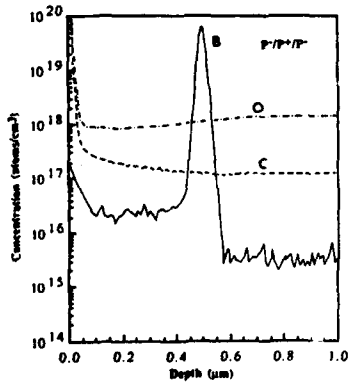


Fig. 7: SIMS depth profiles for a p⁻/p⁺/p⁻ buried layer structure.



Fig. 8: SAD and plan-view TEM micrographs of epilayers grown at 800°C with 5 vol.% SiH₂Cl₂ and with AsH₃ volume concentrations of (a) 1% and (b) 7.5%.

stacking faults and twinning planes. Some polycrystalline grains can be observed in the film. The SAD pattern taken in the area away from the polycrystalline grains also confirmed the monocrystalline structure with defects. A dramatic change of film quality is observed when the AsH_3 flow rate is increased. Shown in Fig. 8(b) are the plan-view TEM micrograph and SAD pattern of a sample grown with 7.5 vol.% AsH_3 . The film quality is perfect monocrystalline with no defects and SAD patterns also show an excellent monocrystalline structure. Since both samples were grown at the same temperature, the results suggest that dopant incorporation can directly enhance epitaxial growth.

SEM micrographs of the As-doped samples clearly show surface pits, which indicates growth defects. The surface pit density decreases with increasing doping levels, and the pits totally disappear for samples grown with 7.5 vol.% AsH_3 , resulting in a smooth surface and good film quality. Fig. 9 plots the defect density at the n^+ layer surface as a function of the electron concentration in the n^+ layer. The defect density decreased markedly with increasing electron concentration.

Fig. 10 shows carrier concentration profiles for samples grown at 800°C with 5 vol.% SiH_2Cl_2 and different AsH_3 flows. By comparing to SIMS results, the dopant activation ratio is determined to be about 100%, within experimental error. Relatively smooth carrier concentration profiles in the doped layer can be observed for all samples. The carrier concentration increased as AsH_3 flow increased. The carrier concentrations drop from 10^{18} cm^{-3} to 10^{15} cm^{-3} in 300 Å for all samples. The very abrupt transition profiles indicate the indiffusion effect is significantly reduced. The results are in good agreement with the SIMS data.

SELECTIVE Si DEPOSITION

Selective epitaxial growth (SEG) is emerging as a promising technology for future ULSI. The reduced thermal exposure of RTP-CVD eliminates undercutting, improves selectivity, and reduces sidewall defects. Lightly-doped, p-type (100)Si wafers covered with a 7000 Å thermal oxide patterned in $\langle 110 \rangle$ directions by RIE were used. An *in-situ* H_2 pre-clean at $1000\text{--}1150^\circ\text{C}$ for 10-60s completely eliminated oxide sidewall undercutting while still maintaining an effective clean. For SiH_2Cl_2 volume concentrations in H_2 below 2%, excellent selectivity was achieved without adding HCl. SEM micrographs of SEG samples grown at temperatures of 1050°C and 975°C are shown in Figs. 11(a) and (b), respectively. For deposition temperatures above 1000°C , almost no faceting can be observed and the epilayer surface appears very smooth. However, the interface between the oxide sidewall and the selectively grown Si appears slightly rough. Selected area diffraction (SAD) and cross-section TEM (XTEM) micrographs of the sample shown in Fig. 11(a) show a high density of epitaxial defects along the oxide sidewall, predominantly $\{111\}$ twinning planes. For SEG samples grown below 1000°C , the SiO_2/Si interface looks very sharp and clean with a smooth surface observed everywhere, suggesting very high crystalline perfection. However, distinct faceting of the epilayer can be observed along the sidewalls. In Fig. 11(b), epitaxial overgrowth was deliberately performed to visually enhance faceting. The XTEM micrograph in Fig. 12 corresponds to the sample in Fig. 11(b). No oxide sidewall undercutting was observed. Except for faceting, SEG samples grown below 1000°C are essentially defect free. The degree of faceting decreases with increasing deposition temperature. Facet formation occurs because the growth rate is different for different crystallographic orientations due to surface energy considerations [16]. The degree of faceting decreases with increasing growth temperature. We have identified $\{911\}$ and $\{111\}$ facet planes in addition to the common $\{311\}$ facet planes.

We have selectively deposited *in-situ* doped poly-Si as a diffusion source for ultra shallow junction formation. Excellent selectivity was achieved. Fig. 13 shows an SEM micrograph of a sample processed at 850°C . Growth rate decreases with increasing doping levels. The SIMS profiles show As pile-up at the surface and at the poly-Si/Si interface. The interface positions are consistent with XTEM results. The As pile-up at the interface indicates grain boundary segregation or impurity trapping of As near the interface. The As concentration increases with decreasing growth temperatures. SIMS profiles show the As concentration drops from 10^{19} cm^{-3} to 10^{17} cm^{-3} within 350 Å. Dopant drive-in was performed by RTP at 1000°C

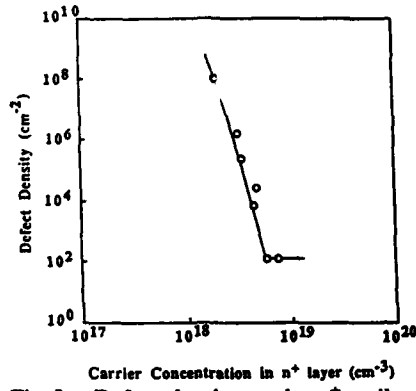


Fig. 9: Defect density at the n⁺ epilayer surface as a function of the carrier concentration at the n⁺ epilayer.

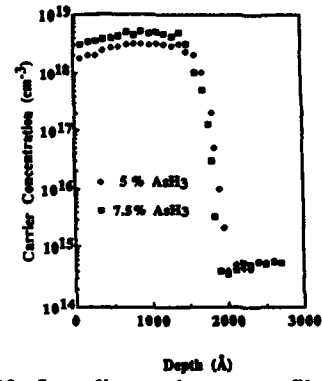


Fig. 10: Spreading resistance profiles for samples grown at 800°C with 5 vol.% SiH₂Cl₂ and different AsH₃ flows.

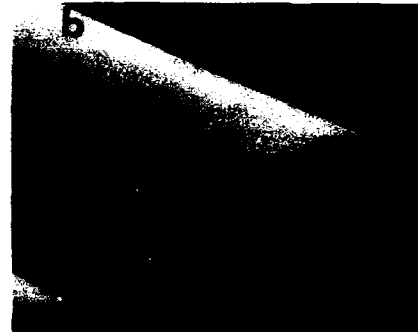
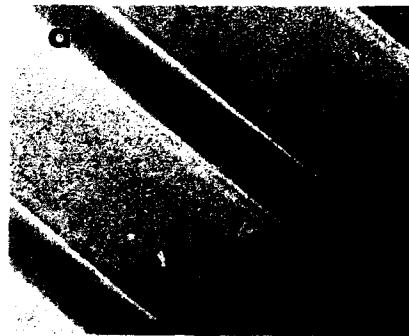


Fig. 11: SEM micrographs showing SEG of Si epilayers grown at (a) 1050°C and (b) 975°C.



Fig. 12: XTEM micrograph showing SEG of Si epilayer grown at 975°C.

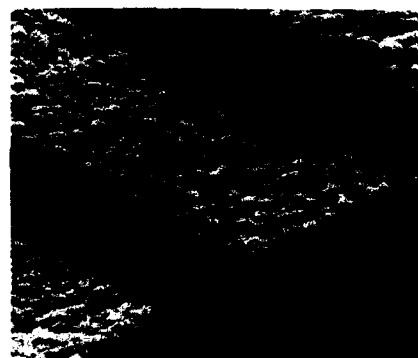


Fig. 13: SEM micrograph of polysilicon lines deposited at 850°C.

for 20s, resulting in partial alignment of the poly-Si and forming an ultra shallow, damage-free junction with uniform diffusion front.

Ge_xSi_{1-x} EPITAXY ON Si SUBSTRATES

Ge_xSi_{1-x} alloy layers have received considerable attention because of the numerous advantageous electrical, optical, and material properties afforded by the lattice mismatched binary system. The ability to tailor both the energy band gap and the band alignment, as well as the enhanced band gap reduction exhibited in strained Ge_xSi_{1-x} layers, has been utilized in fabricating photodetectors operating near 1.3 μm, modulation doped field-effect transistors (MODFETs), and heterojunction bipolar transistors (HBTs). We have previously reported the growth and characterization of single relaxed Ge_xSi_{1-x} layers by RTP-CVD [5]. Multi-layer epitaxy of Ge_xSi_{1-x} and Si films has numerous applications in the areas of relaxed buffer layers, strained layer superlattices, and for vertical device structures. We have grown multi-layer Ge_xSi_{1-x}/Si films consisting of alternating layers of Ge_xSi_{1-x} and Si on p-type Si substrates by RTP-CVD. An *in-situ* H₂ pre-bake of 1000°C for 45s in H₂ was followed by epitaxial growth at 900°C at a chamber pressure of 5 Torr and a total flow rate of 1 lpm.

The XTEM micrograph of a five layer Ge_xSi_{1-x}/Si structure is shown in Fig. 14. No Si capping layer was grown. Each Ge_xSi_{1-x} layer was grown for 15s while each Si layer was grown for 20s. The SiH₂Cl₂:GeH₄ ratios used in growing the Ge_xSi_{1-x} layers from top to bottom were 19:1, 38:1, and 95:1, yielding Ge fractions of 21% and 13% in the top and middle layers, respectively. All layers grew epitaxially. Twinning planes and a high density of dislocations threading through the higher Ge fraction top layer can be observed, while no threading dislocations or other defects can be observed in the underlying layers. In addition to a high density of threading dislocations, plan-view TEM micrographs of the top Ge_xSi_{1-x} layer and interface show that stacking faults, short misfit dislocations, and very small defects exhibiting dislocation loop type contrast can be observed. The misfit dislocations were confined near the interface and were aligned along <011> directions. The existence of the misfit dislocations indicates that relaxation has occurred in the top layer. The roughness of the top interface is believed to be due to the pile-up of Ge at the interface observed in the Auger depth profiles discussed below. The other interfaces were very planar, indicative of two-dimensional growth. Plan-view TEM micrographs of each successive underlying layer and interface reveal only small defects with dislocation loop type contrast confined near the interface. The dislocation loops varied from 2000 Å to less than 100 Å in diameter. Some of the dislocation loops were identified as hexagonal Frank loops with Burger's vectors of $\frac{1}{3}[111]$. Other dislocation loops were determined to be highly complex Frank loops. The final analysis indicated that the dislocation loops were Ge interstitial loops. No misfit dislocations or threading dislocations were observed in the underlying layers, indicating that the strain was preserved. Thus relaxation occurred in the top layer without relaxing the entire structure.

Fig. 15 shows the Auger depth profile for the top three layers of the five layer structure. The AES depth profile shows an accumulation of Ge at the surface and at the top interface. The same phenomenon was also observed in other multi-layer structures, but only in layers with high threading dislocation densities. The defects may provide pathways for enhancing the movement of Ge atoms toward more energetically favorable positions at the interface and possibly also at the surface, resulting in the observed pile-up peaks.

Ge_xSi_{1-x} WAVEGUIDES

Optoelectronics has been the subject of considerable research. Historically, III-V compounds have played the dominant role in optoelectronics. However, due to advances in growth technology and material understanding, the Ge_xSi_{1-x} materials system [17] has opened up numerous opportunities for Si-based optoelectronic applications such as photodetection, waveguiding, and optical modulation. Recently, interest has focused on Ge_xSi_{1-x} as a waveguiding material for Si-based optoelectronics [18,19]. The use of crystalline Ge_xSi_{1-x}

offers the prospects of further vertical device integration, hence incorporation into device structures is possible.

We have utilized the refractive index difference between $\text{Ge}_x\text{Si}_{1-x}$ and Si to fabricate $\text{Ge}_x\text{Si}_{1-x}$ waveguides on Si substrates. Both slab and rib waveguides were studied. The waveguide structures were patterned by conventional photolithography techniques and etched by reactive ion etching (RIE). Optical measurements were performed by end-fire coupling light into the edge of the polished rib structures with a microscope objective. The near field optical beam intensity was measured and recorded using a Ge photodiode, a lock-in amplifier, and a plotter. Optical losses were determined using the Fabry-Perot interference technique [20].

Single mode guiding was observed for rib widths of $\leq 5 \mu\text{m}$. Second order modes were observed for $10 \mu\text{m}$ widths. Fig. 16 shows a plot of waveguide loss as a function of waveguide length. An average waveguiding loss of as low as 3.3 dB/cm at $1.52 \mu\text{m}$ for TM polarization has been achieved for rib structures. Although our losses are not as low as for dielectric waveguides, the use of crystalline materials opens opportunities in device and circuit integration. Optimization of material quality and parameters (Ge fraction, film thickness, etc.) as well as waveguide dimensions and processing is expected to further decrease waveguide loss.

In addition, we have demonstrated coupling of light between waveguides. Fig. 17 is a semi-log plot of percentage of power coupled from one arm into another arm. Average coupling efficiencies ($P_2/[P_1+P_2]$) are 75% to 85%, depending on interwaveguide separation. The change in average coupling efficiency with interwaveguide spacing is approximately -8%/μm. An interwaveguide gap of $3 \mu\text{m}$ exhibits a transfer length of 0.46 cm and a coupling coefficient of 3.4 cm^{-1} . An interwaveguide gap of $1.5 \mu\text{m}$ exhibits a transfer length of 0.41 cm and a coupling coefficient of 3.9 cm^{-1} . Thus, the coupling coefficient changes by 0.17 cm^{-1} for each $0.5 \mu\text{m}$ change in interwaveguide spacing and the transfer length depends directly on interwaveguide spacing. The coupling coefficient and transfer length were calculated assuming identical waveguides and neglecting coupling near the Y-shaped bend region. Our results indicate that the waveguiding properties of $\text{Ge}_x\text{Si}_{1-x}$ are promising for further device and circuit integration. The $\text{Ge}_x\text{Si}_{1-x}$ layer can serve as the waveguiding structure in a $\text{Ge}_x\text{Si}_{1-x}$ modulator or as a waveguide for integration with a $\text{Ge}_x\text{Si}_{1-x}$ photodetector.

SUMMARY AND CONCLUSIONS

We have observed that the H_2 pre-clean is capable of causing a considerable amount of surface damage, depending strongly on process parameters such as system base pressure and temperature. A low thermal budget H_2 pre-bake at 800°C for 15s gives satisfactory results in terms of both the quality of the resulting epilayer and the dopant transition profile. The application of RTP-CVD to the growth of Si epitaxial films has been examined. The epitaxial growth kinetics have been determined by studying the dependence of growth rate on deposition temperature, volume percentage of SiH_2Cl_2 , and the total gas flow rate. Thin epilayers with hyper-abrupt dopant transition profiles can be easily produced by RTP-CVD due to the short thermal exposure during the RTP-CVD process. Through careful wafer pre-cleaning and proper deposition conditions, epitaxial layers free of stacking faults and dislocations can be reproducibly grown. Very high quality heavily-doped epilayers, both n-type and p-type, using B and P as dopants have been grown by RTP-CVD with flat and abrupt dopant transition profiles and the epilayers possess excellent crystalline quality. We have demonstrated, for the first time, that the epitaxial growth temperature can be lowered by *in-situ* dopant incorporation. Heavily arsenic-doped epitaxial layers with very abrupt dopant transition profiles and relative uniform carrier distribution have been achieved at 800°C . The defect formation is closely related to dopant concentration; the defect density as a function of carrier concentration shows a sharp transition at about $3 \times 10^{18} \text{ cm}^{-3}$.

We have demonstrated that RTP-CVD is capable of selectively growing very high quality epitaxial Si into openings of an oxide mask. Oxide undercutting is totally eliminated at temperatures below 1025°C during the H_2 bake, while still maintaining an effective clean. Growth temperatures below 1000°C appear to be favorable for producing defect-free SEG. However, higher growth temperatures tend to reduce faceting. The epitaxial growth proceeded with perfect selectivity, without the use of HCl.

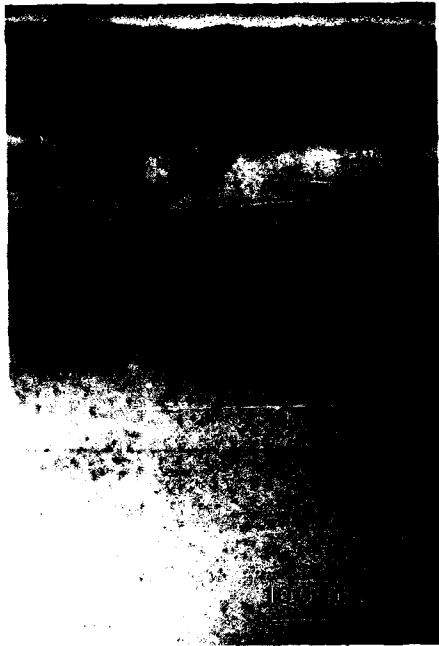


Fig. 14: XTEM micrograph of Ge_xSi_{1-x} structure.

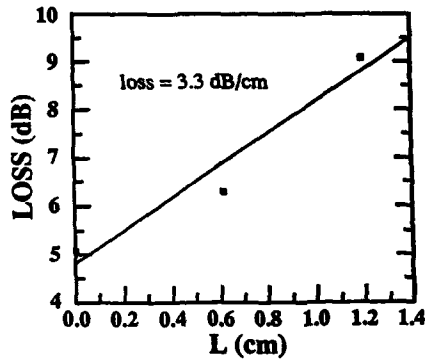


Fig. 16: Plot of loss as a function of waveguide length.

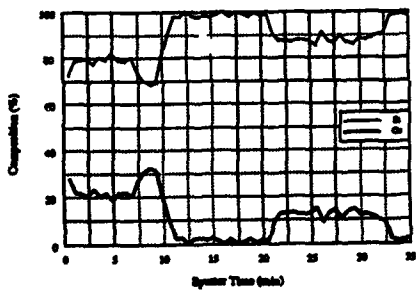


Fig. 15: AES depth profile of Ge_xSi_{1-x} structure.

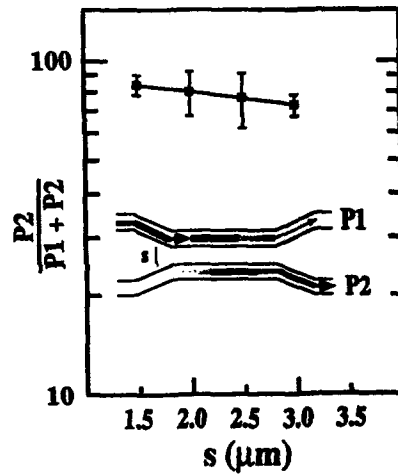


Fig. 17: Plot of coupling efficiency as a function of interwaveguide spacing.

We have grown multi-layer structures of alternating $\text{Ge}_x\text{Si}_{1-x}$ ($x < 0.21$) and pure Si layers on (100)Si substrates. In strained layers, the only defects were Ge interstitial loops confined near the interface. In layers that were partially relaxed, misfit dislocations, stacking faults, and threading dislocations were observed. Ge pile-up was also observed at the interface of relaxed layers containing high densities of threading dislocations. The pile-up is believed to be due primarily to defect-enhanced movement of Ge to more energetically favorable sites at the interface. In addition, we report the growth and characterization of $\text{Ge}_x\text{Si}_{1-x}$ films for optical waveguiding, and have demonstrated coupling of light between waveguides. An average attenuation of 3.3 dB/cm was achieved for a 1 μm thick $\text{Ge}_{0.04}\text{Si}_{0.96}$ layer patterned into rib waveguides 2000 \AA deep with widths of 5 μm . Average coupling efficiencies of as high as 85% for an interwaveguide spacing of 1.5 μm have been achieved. Our results indicate that the waveguiding properties of $\text{Ge}_x\text{Si}_{1-x}$ are promising for further device and circuit integration.

ACKNOWLEDGEMENTS

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GROWTH OF A β -SiC FILM ON A Si SUBSTRATE
BY A DIRECT CARBONIZATION METHOD

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Single crystal β -SiC films have been fabricated on (100)Si substrates through a thermal reaction between the substrate and carbon atoms sublimed from a high purity graphite source. The substrate temperature during the deposition ranged from 600 to 1100°C. The film properties were analyzed by RHEED and x-ray diffraction measurements. RBS measurements and TEM observations have also been made to investigate the film properties. The single crystal β -SiC films grow at and above 1000°C on (100) substrates. The activation energy is found to be around 1.1 eV for the crystallization process.

INTRODUCTION

Heteroepitaxial growth of a β -SiC film on a Si substrate is currently of considerable interest for various applications of the material to electronic devices. One of the interesting applications is that the β -SiC/Si structure is applicable to the emitter junction in a silicon hetero-bipolar junction transistor (HBT)⁽¹⁾. A large number of papers reporting the hetero-epitaxial growth of SiC films on Si substrates have been published. In most of these papers, they reported that β -SiC films have been formed when chemical vapor deposition (CVD) with substrate temperatures in the range of 1300 to 1400°C⁽²⁾⁻⁽⁴⁾. These temperatures are too high to be employed in a fabricating process for silicon devices such as HBTs.

Recently, low temperature epitaxial growth of β -SiC on Si substrates has been studied by many workers using different techniques. Chaudhry and Wright⁽⁵⁾ grew β -SiC films on (100)Si by low temperature CVD using a $\text{SiH}_4\text{-C}_2\text{H}_6\text{-H}_2\text{-Ar}$ gas system. They have reported that the β -SiC films grown at and above 1150°C are single crystals and that films grown below 1150°C are polycrystals as determined by TEM and x-ray diffraction observations. Low temperature growth of β -SiC on Si by reactive-ion-beam deposition has been reported by Yamada⁽⁶⁾. His data show that the heteroepitaxial growth of β -SiC film on (100)- and (111)-Si can be achieved at temperatures lower than 800°C using very thin (several nm in thickness) Si homo-epitaxial and SiC transition layers in the initial stage of the heteroepitaxial growth. Motoyama et al⁽⁷⁾ have reported that single crystal β -SiC films are formed on (111)Si at 1050°C using the molecular-beam epitaxial method. The present authors⁽⁸⁾ have shown that single crystal β -SiC films can be formed on (111)Si by the thermal reaction at and above 900°C between the substrate and C atoms.

We have studied the heteroepitaxial growth of the film on (100)Si using the same carbonization method as used in the previous work on the film growth on (111)Si. This paper reports the initial experimental results on crystal properties of β -SiC films grown on (100)Si by the carbonization method.

EXPERIMENTAL PROCEDURES

The substrates used in this experiment were commercially available, p-type, (100)Si wafers with a resistivity of 8-10 Ω -cm. For a comparison, (111)Si wafers were also used as the substrate. After surface cleaning by a chemical treatment, the substrate was heated at 950°C for 20 min in a vacuum chamber to remove the native oxide layer from the substrate. The chamber was evacuated initially with a turbo-molecular pump and then with an ion pump. The operating pressure in the heating treatment was less than 3×10^{-7} Torr. Carbon atoms were sublimed from a block of high purity (99.999%) polycrystal graphite and then were deposited on the heated substrate. The graphite block was heated above 2500°C by an electron beam accelerated at 4.2kV. The substrate temperature during the deposition ranged from 600 to 1100°C. The pressure in the carbonization was around 1×10^{-6} Torr.

The thermal reaction between heated substrate and C atoms proceeded during the deposition, resulting in the formation of a SiC film on the substrate. This reaction process and the atomic composition of the formed film were examined by Rutherford backscattering (RBS) and secondary ion mass spectroscopy (SIMS) measurements. The RBS measurements were carried out using 1.5 MeV He⁺ ion beam with a scattering angle of 150°. The crystal properties of the formed film were investigated by a high energy electron diffraction (RHEED) method. The crystallinity was additionally checked by x-ray diffraction and by transmission electron microscopic (TEM) observations. RBS/channeling measurements were also carried out to get some information on the crystallinity of the formed film and on the carbonization process.

RESULTS AND DISCUSSION

No thermal reaction between the substrate and deposited C atoms proceeded when the substrate was heated below 700°C, resulting in the formation of a polycrystal graphite layer on the substrate. When the substrate was heated at and above 800°C, the thermal reaction occurred and a SiC film grew on the substrate. The thickness of the film examined in this work was fixed at 200nm. RHEED observations showed that the crystallinity of the formed SiC film depended strongly upon the substrate temperature during the deposition. When the substrate was heated at a temperature between 800 and 900°C, polycrystal SiC films grew as shown in Fig.1(A). Single crystal β -SiC films grew if the carbonization was carried out at and above 1000°C. Fig.1(B) shows a typical RHEED pattern for a film grown at 1000°C. Our previous work has shown that

the critical temperature is 900°C, at and above which the single crystal β -SiC film is formed on the (111)Si substrate. These results indicated that single crystal β -SiC films grew more easily on (111)Si than on (100)Si. Liaw and Davies⁽³⁾ have reported that the epitaxial growth of (111) β -SiC films can

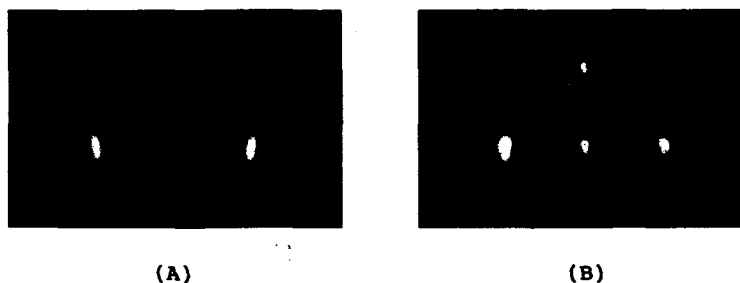


Fig.1 RHEED patterns for polycrystal and single crystal SiC films grown on (100)Si by the carbonization at 900°C(A) and at 1000°C(B), respectively.

be achieved at a relatively lower temperature than that required for the (100) films, where the epitaxial growth is carried out using a two-step process of surface conversion and subsequent film deposition. From the view point of Si device applications, the heteroepitaxial growth of β -SiC films on (100)Si is very much important. This is due to the fact that almost all Si devices are fabricated in (100)Si substrates.

Fig.2 shows x-ray diffraction spectra for three different films grown at 900, 1000 and 1100°C. The diffraction peak of the Si substrate appears in these spectra since the β -SiC films examined were thin; 200nm in thickness. As shown in the spectrum for the film grown at 900°C, two peaks at the diffraction angles (2θ) of 36.12° and 40.48° correspond to β -SiC(111) and (200) planes, respectively. These peaks were low in height and broad in width, indicating that the crystalline state of the film grown at 900 °C is imperfect. When the carbonization was carried out at 1000°C, the diffraction peak at 36.21° disappeared and the peak corresponding to the (200) plane was well defined. And the position of the diffraction peak was slightly shifted to 41.46°. From these results, it is noted that a single crystal β -SiC film grows on (100)Si by the carbonization at 1000°C.

The full width of half maximum (FWHM) for this β -SiC film, was found to be 0.475°. This FWHM is larger than that of the Si substrate (0.234°) which is a high quality single crystal. The diffraction peak increased in height and decreased in FWHM for a film grown at 1100°C. And its diffraction peak was located at 41.62° on the spectra and its FWHM was 0.30°. Note that this peak position is almost identical to that predicted

from the theoretical calculation for ideal single crystal β -SiC. Atomic compositions of grown films were examined by SIMS measurements. The SIMS data showed that uniformly distributed profiles for both of Si and C atoms were built in the SiC films grown at and above 1000°C. The concentration ratio of Si to C was unity throughout the film. Combining these SIMS results with RHEED and x-ray diffraction data, it is concluded that stoichiometric (100) β -SiC films can be formed by the carbonization method at and above 1000°C.

Fig.3 shows TEM photographs showing plan-view of two different β -SiC films grown at 1100°C on (100)- and (111)-Si. These TEM photographs show that both of the β -SiC films contain lattice defects which could not be well defined. The density of lattice defects in the (100) β -SiC films was higher than that in the (111) β -SiC films. In order to examine crystal properties of these films in further detail, cross-sectional TEM (XTEM) observations were made. A typical XTEM photograph for a (100) β -SiC film grown at 1100°C is shown in Fig.4. Rod-like defects originated from the SiC-Si interface and reached the surface of the film. In addition, the XTEM image indicates the existence of twins in the film.

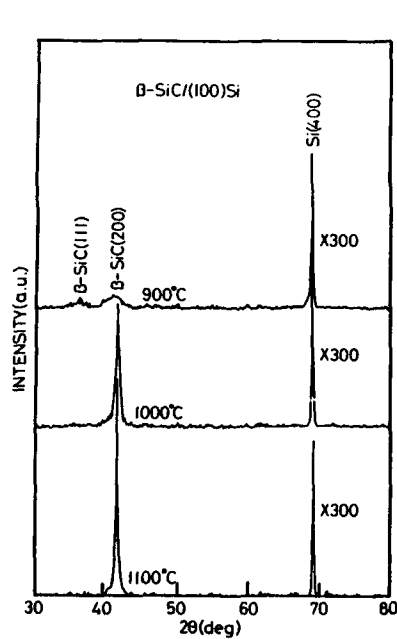


Fig.2 X-ray diffraction spectra for 200nm-thick β -SiC films grown on (100)Si at 900, 1000 and 1100°C by the carbonization method.

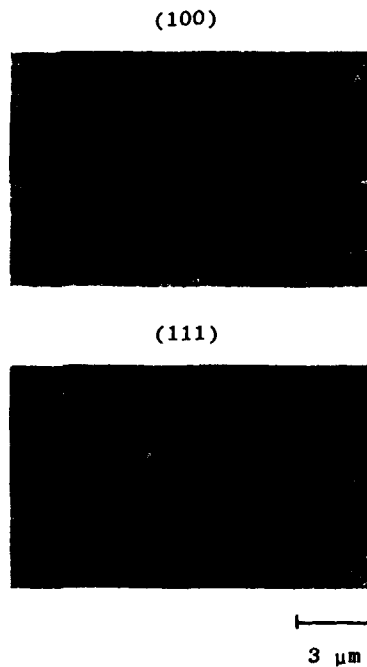


Fig.3 TEM photographs showing plan-view of β -SiC films grown at 1100°C on (100)- and (111)-Si by the carbonization method.

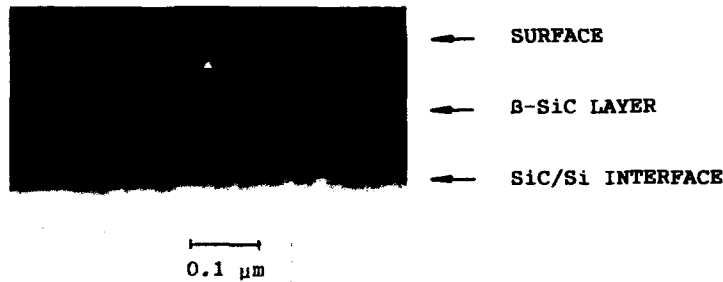


Fig.4 XTEM photograph for a B-SiC film grown on(100)Si at 1100°C by the carbonization method.

RBS/channeling measurements were carried out on films grown at temperatures in a range from 800 to 1100°C. Fig.5 shows an example of the angular dependence of the backscattering yield from a 200nm-thick SiC/Si structure. In evaluating an epitaxial layer by the RBS/channeling method, a ratio of minimum yield (H_A) to random yield (H_R), X_{min} , is widely used as a crystal quality factor of the epitaxial layer. The X_{min} expected for high quality single crystal B-SiC is less than 4%. The values of X_{min} were 19 and 54 % for B-SiC films grown on (111)- and (100)-Si at 1100°C, respectively. This result indicates these B-SiC films contained a high density of crystal defects, which well agrees with TEM data shown in Figs.3 and 4.

In order to study the mechanism of the carbonization process, a ratio of $H_R - H_A / H_R$ was defined in this work. This ratio indicates a degree of lattice ordering in the film. If a high quality, highly ordered, B-SiC film grows, this ratio becomes larger. And it is designated as a lattice ordering factor. Fig.6 shows the logarithm plots of the lattice ordering factor as a function of reciprocal growth temperature. The data points in Fig.6 can be fitted to an exponential function with an activation energy of 1.1 eV. There was no difference in value of the activation energy between the B-SiC growth on (100)- and (111)-Si. Note that

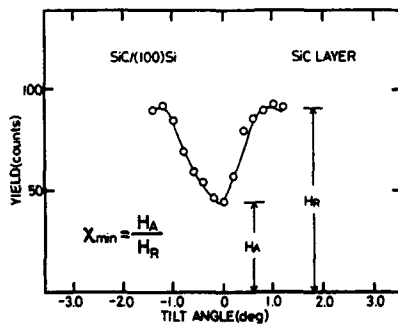


Fig.5 Angular dependence of backscattering yield of 1.5 MeV He^+ ions incident on a B-SiC film grown on (100)Si at 1100°C

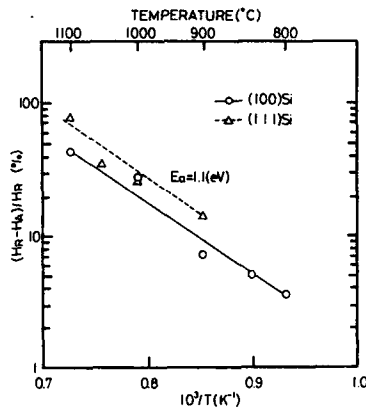


Fig.6 Logarithm plots of the lattice ordering factor, defined as a ratio of $(H_R - H_N)/H_R$ in the RBS spectrum, as a function of reciprocal growth temperature for β -SiC films formed on (100)- and (111)-Si by the carbonization method.

the value of the activation energy is close to that previously reported on the heteroepitaxial growth of β -SiC on Si by CVD.⁽²⁾

SUMMARY

In summary, we have studied heteroepitaxial growth of β -SiC films on (100)Si by the direct carbonization method. It is demonstrated that single crystal β -SiC films can be formed on (100)Si at and above 1000°C. The epitaxial temperature of 1000°C is 100°C higher than that for the growth on (111)Si. The carbonization process is characterized with an activation energy of approximately 1.1 eV for both (100)- and (111)-Si substrates, which is close to that previously reported on the β -SiC growth by different techniques. The crystal quality of β -SiC films grown in this work is incomplete and it should be improved before these films are applied to a wide-gap emitter in Si HBTs. The improvement in the crystallinity of the β -SiC film is now in progress and the results will be reported in the near future.

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CARBONIZATION DYNAMICS OF SILICON SURFACES
BY HYDROCARBON GAS MOLECULAR BEAMS

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ABSTRACT

Carbonization dynamics of Si surfaces using a hydrocarbon gas molecular beam was investigated. In case of carbonizing atomically clean Si surfaces with C_2H_2 , single crystalline 3C-SiC layers were obtained only in the narrow range of a substrate temperature near 780 °C. Control of surface reaction by a cap of very thin surface oxide layer and gradual increase of substrate temperature during carbonization were found to be effective in forming single crystalline 3C-SiC layers reproducibly.

INTRODUCTION

Silicon carbide (SiC) is a wide-gap semiconductor material with excellent physical stability and thermal conductivity which favors this material for applications to high-temperature, high-power and microwave devices. Among many polytypes of SiC, cubic SiC (3C-SiC; $E_g=2.3eV$) seems to be the most promising because of high electron mobility with values up to 1000 cm^2/Vs . A breakthrough in heteroepitaxy on Si substrates^{1,2} brought large area 3C-SiC wafers into existence and opened the door to device application. This method adopted a carbonization process preceding a chemical vapor deposition (CVD) process. In the carbonization process, the substrate surface is chemically converted to 3C-SiC using a hydrocarbon gas such as propane (C_3H_8). The carbonization process overcame the difficulties arising from the large lattice mismatch of 20% and the strong affinity of the Si surface to hydrocarbon species. The CVD method, however, requires growth temperatures as high as 1350 °C, and so, the reduction of growth temperature is desired.

Gas source molecular beam epitaxy (GSMBE) is a hopeful technique to realize low-temperature growth and high-purity epilayers. We already reported homoepitaxial growth of 3C-SiC at a substrate temperature as low as 1000 °C by an alternating supply of disilane (Si_2H_6) and acetylene (C_2H_2) gas molecular beams^{3,4}. In order to realize heteroepitaxial growth of 3C-SiC on Si by GSMBE, an adequate carbonization process in a high vacuum must be established.

In this study, carbonization processes using hydrocarbon gas molecular beams are investigated. Dynamics of carbonization is analyzed using in-situ reflection high energy electron diffraction (RHEED). First, experimental results on carbonization of clean Si surfaces are described together with some problems. Second, some different types of modified carbonization processes to get high-quality single crystalline 3C-SiC are discussed.

APPARATUS

Experiments were carried out in an ultra high-vacuum (UHV) chamber designed for GSMBE (Fig.1). The chamber is equipped with a sputter ion pump, by which an ultra high vacuum of 10^{-10} Torr range is achieved. The base pressure at an elevated temperature for carbonization is in a low 10^{-8} Torr range. During the carbonization process, a high vacuum of 10^{-6} Torr

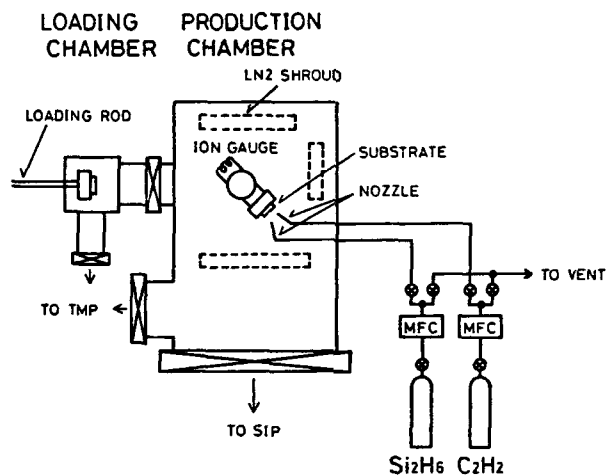


Fig.1. Gas source MBE apparatus.

range is maintained by a liquid nitrogen cold trap. The chamber is also equipped with a RHEED observation system for in-situ analysis of the specimen surface. The substrates are Si(001), and the hydrocarbon gas employed for carbonization is pure C_2H_2 , which is ejected from a nozzle located at a distance of 10 cm from the substrate. The substrate temperature is controlled within 1°C of fluctuation using a W-WRe thermocouple located between the substrate and the heater. The values of the substrate temperature in this report were measured by an optical pyrometer with a precision of 10°C .

CARBONIZATION OF BARE SI SURFACES

Carbonization of Si surfaces using hydrocarbon gases was investigated extensively in 1960-70's. It is known that carbonization of Si surfaces using C_2H_2 gas in a high vacuum produces epitaxial 3C-SiC layers at temperatures as low as 800°C ⁵⁻⁷). The carbonization reaction is considered to be due to outward diffusion of Si atoms from the interface to the surface. Mogab et al.⁷⁾ investigated the surface morphology of the carbonized layer and observed many defects through which Si atoms diffused outward. They concluded that these defects were intrinsic in carbonization of Si surfaces in a high vacuum.

In our study, carbonization of Si surfaces using hydrocarbon gas molecular beams in an ultra high vacuum (UHV) chamber was investigated. Si(001) substrates were first heated up to 900°C in a UHV ($< 3 \times 10^{-8}$ Torr) for oxide removal. The completion of oxide removal was verified by observation of (2x1) superstructure using in-situ RHEED. After the oxide removal, the substrate temperature was lowered to a desired value and an C_2H_2 beam (0.40 sccm) was introduced. A single crystalline 3C-SiC layer ($\sim 100\text{\AA}$) was obtained at 780°C , but not reproducibly. Even when a single crystalline layer was obtained, many defects, as described by Mogab et al.⁷⁾, were still observed. Another problem in this method is that a slightly higher temperature easily lead to polycrystalline SiC layers. Figure 2 shows the transition of the RHEED pattern in the case of carbonization at 900°C . Diffraction spots corresponding to 3C-SiC are

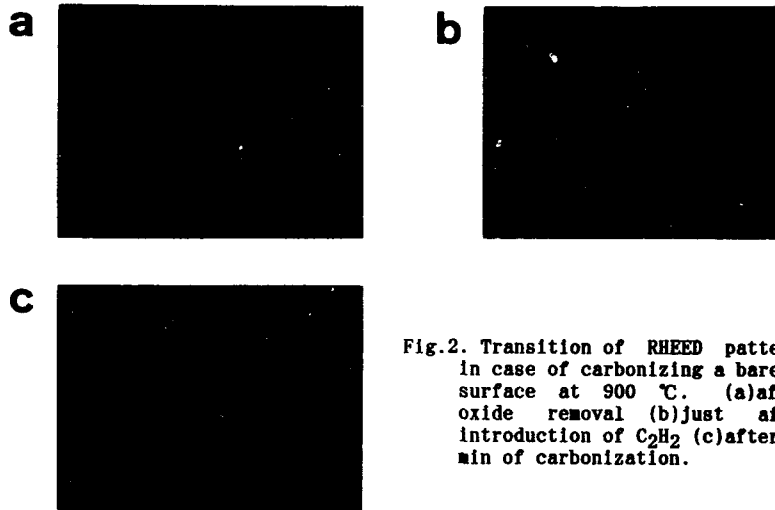


Fig.2. Transition of RHEED patterns in case of carbonizing a bare Si surface at 900 °C. (a) after oxide removal (b) just after introduction of C_2H_2 (c) after 60 min of carbonization.

observed just after the introduction of C_2H_2 (Fig.2(b)). A ring pattern was observed after 60 minutes of carbonization (Fig.2(c)). Carbonization reaction at the surface is discussed in more detail elsewhere⁸.

TEMPERATURE RISING DURING CARBONIZATION

As mentioned above, exposure of a Si surface to an C_2H_2 beam at higher temperatures brings about polycrystallization, which should be attributed to the strong affinity of the Si surface to C_2H_2 molecules. At lower temperatures (< 780 °C), however, carbonization does not occur, and the reproducibility of formation of single crystalline 3C-SiC is poor even at the critical temperature of 780 °C.

We tested a modified carbonization process in which the bare Si surface was not exposed to an C_2H_2 beam at a high temperature. The procedure is as follows. After the completion of oxide removal at 900 °C in a UHV, the substrate temperature was once lowered to 400 °C. Then, an C_2H_2 beam (0.40 sccm) was introduced and the temperature was gradually raised to 300 °C at a rate of 10 °C / min. The transition of the RHEED pattern is shown in Fig.3. After the oxide removal, 3C-SiC spot pattern was observed other than the Si (2x1) streaks as shown in Fig.3(a). This is probably due to formation of SiC particles caused by the residual hydrocarbon gases during the oxide removal. The Si (2x1) streaks were still observed at 600 °C (Fig.3(b)), but they disappeared at 700 °C (Fig.3(c)), which stands for the beginning of the reaction. The RHEED pattern of the obtained layer (Fig.3(d)) still contains some extra spots, but is much improved in comparison with Fig.2(c).

CARBONIZATION WITH CONTROLLED SURFACE REACTION

We tested another modified process in which the oxide removal was not performed prior to carbonization. The C_2H_2 beam (0.40 sccm) was introduced at 400 °C, and the substrate temperature was raised to 900 °C at a rate of

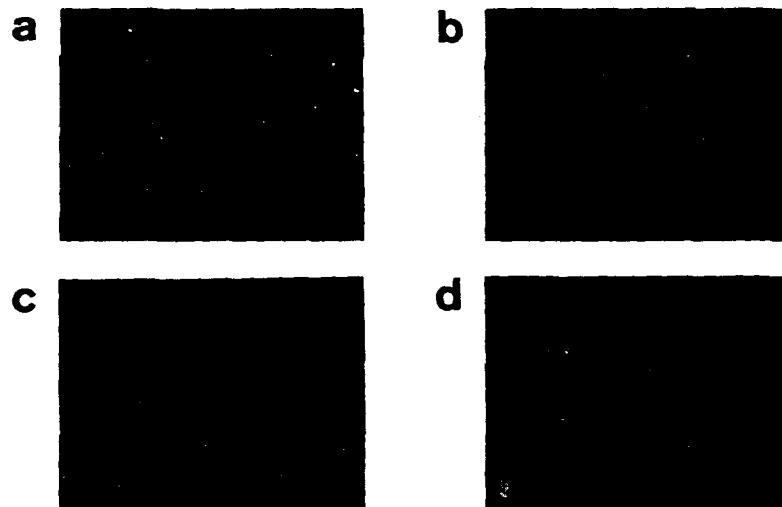


Fig.3. Transition of RHEED patterns in case of carbonization during temperature rising. (a)after oxide removal (b)at 600 °C (c)at 700 °C (d)after 60 min of carbonization.

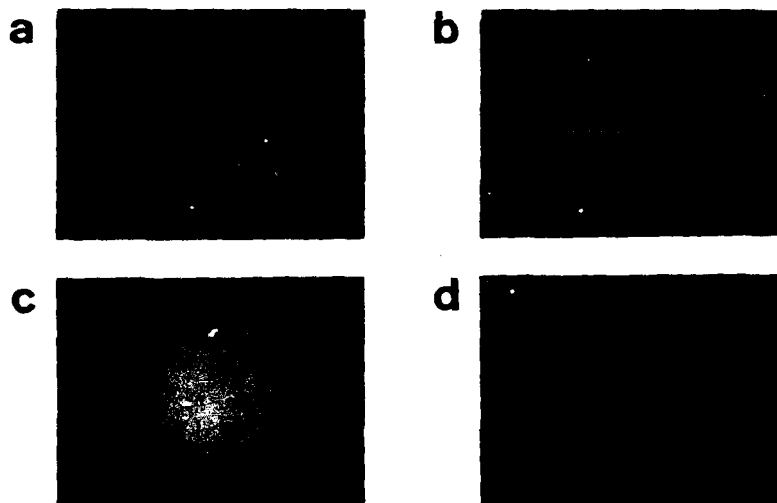


Fig.4. Transition of RHEED patterns in case of carbonization during temperature rising and under existence of surface oxide. (a)at 400 °C (b)3 min at 900 °C (c)40 min at 900 °C (d)after 180 min of carbonization.

10 °C/min. The transition of the RHEED pattern is shown in Fig.4. A streak pattern of Si was observed up to 870 °C (Fig.4(a)). Extra streaks related to the Si (2x1) superstructure were not observed because the surface was still covered with a thin oxide layer at this temperature. Then, at near 870 °C, the diffraction streaks disappeared and the pattern became halo, which implies the formation of an amorphous-like layer on the surface. Finally, a spot pattern of SiC appeared and became clear as the halo vanished gradually (Fig.4(b),(c) and (d)). This observation suggests that the reaction of Si and C₂H₂ was hindered by the existence of the amorphous-like (Si-C-O) layer, and carbonization took place very slowly with simultaneous removal of the oxide by evaporation.

Single crystalline SiC was reproducibly obtained in this method. The maximum temperature required for carbonization was 900 °C, which is 100 °C lower than that for epitaxial growth of SiC by GSMBE. It should be noted that the carbonized layer formed by this method exhibited no polycrystallization even when the temperature was raised up to 1100 °C. Thus, this method seems to be promising as a carbonization process preceding GSMBE growth of SiC.

SURFACE MORPHOLOGY

Nomarski surface microphotographs of the carbonized layers obtained in the above three methods are shown in Fig.5. In the first method, in which a bare Si surface is exposed to C₂H₂ at 900 °C, the obtained layer exhibits a very rough surface (Fig.5(a)). In the second method, in which a bare Si surface is carbonized during temperature rising, a relatively smooth surface is obtained, but many defects are still observed. These defects are probably related to the SiC particle formation during the oxide

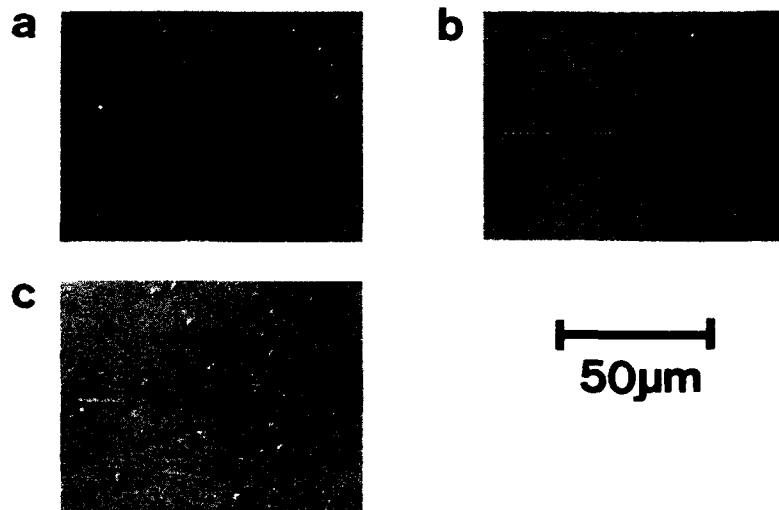


Fig.5. Nomarski surface microphotographs of obtained layers. (a)carbonization of bare Si surface at 900 °C (b)carbonization of bare Si surface during temperature rising (c)carbonization during temperature rising and under existence of surface oxide layer.

removal at a high temperature. In the third method, in which carbonization is done during temperature rising and under existence of the oxide layer, the defect density is much smaller, but the observed defects are larger in size. Their origin is not clear at present.

CONCLUSION

Carbonization dynamics of Si surfaces using a hydrocarbon gas molecular beam was investigated. In the case of carbonizing atomically clean Si surfaces with C_2H_2 , single crystalline 3C-SiC layers were obtained only in the narrow range of a substrate temperature near 780 °C. Control of surface reaction by a cap of very thin surface oxide layer and gradual increase of substrate temperature during carbonization were found to be effective in forming single crystalline 3C-SiC layers reproducibly.

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The Synthesis and Stability of $\text{Si}_{1-y}\text{C}_y$ Alloys and Strained Layer Superlattices

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ABSTRACT

We have synthesized $\text{Si}_{1-y}\text{C}_y$ layers and strained layer superlattices on Si (100) with C concentrations of up to a few percent using Solid Source Molecular Beam Epitaxy. The presence of C even in small quantities is known to disrupt the epitaxy of Si. We show that under conditions of high Si flux for a given C/Si flux ratio, defect-free epitaxy results. However, exceeding a critical C/Si flux ratio leads to disruption of epitaxy, initially via twinning and subsequently by amorphous growth. Growth temperature also plays a significant role in preventing twinning and islanding. Low growth temperature also suppresses the precipitation of β -SiC and leads to the formation of pseudomorphic $\text{Si}_{1-y}\text{C}_y$ random alloys. The layers are characterized by X-ray diffraction, Secondary Ion Mass spectroscopy, and Transmission Electron Microscopy. We have also studied the thermal stability of strained layer superlattices and find that the layers are stable to about 800°C (for $y=0.003$). Between 800°C and 1000°C, the layers relax by interdiffusion. Above 1000°C, silicon carbide precipitation occurs and the carbide layers nucleate and grow at high C content regions of the film.

Introduction

Heterostructures have been used to demonstrate significant leverage in a silicon-based technology. $\text{Si}_{1-x}\text{Ge}_x$ alloys and Strained Layer Superlattices (SLS), have been used to fabricate Heterojunction Bipolar Transistors (HBTs) [1], as well as other devices. The $\text{Si}_{1-x}\text{Ge}_x$ system allows one to integrate a smaller bandgap semiconductor with Si. In addition, one can engineer both Ge composition and strain independently to obtain a variety of bandgaps and band alignments. However, it is also very desirable to have a similar flexibility in integrating a Si-compatible wide bandgap semiconductor. A number of approaches have been attempted over the past few years: GaP [2], Semi-Insulating Polycrystalline-Silicon (SIPOS) [3-5], Oxygen-Doped Si Epitaxial Films (OXSEF) [6], β -SiC [7, 8], and amorphous and microcrystalline silicon (α -Si and μ -Si) [9, 10]. These approaches are severely limited because the material is not epitaxial and high quality Si can not be grown on these materials. In addition, many of these approaches require the use of high temperature growth techniques that may be incompatible with advanced VLSI processing trends.

The Si-C system offers the possibility of a widegap material compatible with Si. Fig. 1 shows the measured bandgap for $\text{Si}_{1-x}\text{Ge}_x$ alloys as a function of Ge content both for relaxed alloys and for alloys pseudomorphic to Si. Also shown is the projected bandgap for the Si-C system. Note that diamond has a bandgap of about 5.5 eV. However, unlike the Si-Ge system, Si and C are not miscible at all. In fact the solubility of C in Si even at the melting point of Si is barely 10^{-6} at. %. Furthermore, stoichiometric silicon carbide is a stable compound phase and exists in several phases and polytypes, the most notable being β -SiC (zinc blende structure) with

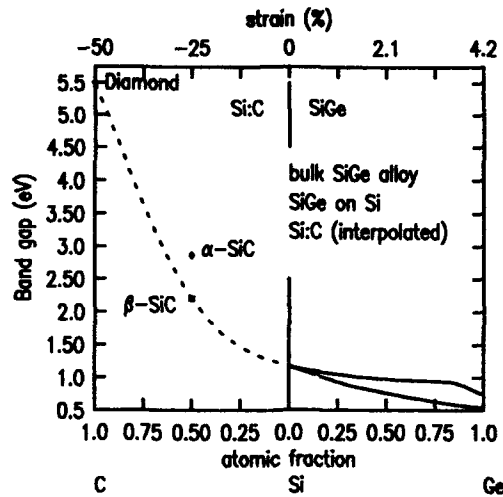


Fig. 1: Measured bandgap of $\text{Si}_{1-x}\text{Ge}_x$ alloys as a function of Ge content for bulk (upper curve) alloys and layers pseudomorphic to Si (lower curve), and the estimated bandgap of $\text{Si}_{1-y}\text{C}_y$ alloys as a function of C content. The estimate is based on a spline fit through the gaps for Si, β -Si and diamond. Also shown is the gap for α -SiC. The top scale shows the strain in the film for growth on Si.



Fig. 2: XTEM micrograph showing a highly twinned and islanded $\text{Si}_{1-y}\text{C}_y$ ($y=0.001$) layer grown at 550°C with a Si flux of 0.02 nm/sec . The layers are compensated for strain by addition of Ge ($x=0.01$). The layer is about 100 nm thick and has a 20 nm thick Si cap.

bandgap of about 2.2 eV and α -SiC (hexagonal structure) with bandgap of 2.9 eV. The dashed curve in Fig. 1 is a spline fit through the gaps of Si, β -SiC and diamond. In view of the lack of any band structure computations for $\text{Si}_{1-x}\text{C}_x$, this curve provides a crude estimate.

Also shown in Fig. 1 on the top abscissa scale is the misfit in percent. Note that while the misfit for pure Ge grown on Si is about 4.2 %, Diamond has a misfit of about 50%. Besides the obvious problem of growing a thermodynamically unstable alloy phase, one also has to contend with a highly mismatched system. Quite clearly we will be limited to relatively small percentages of C incorporation. In terms of strain, when grown pseudomorphic to silicon 1% C in Si produces comparable tensile strain to the compressive strain produced by about 12% Ge. We also expect the bandgap increase obtained for 1% C to be similar to the decrease produced by about 12% Ge i.e., about 100 meV, from our crude interpolated model.

To our knowledge the only published attempt grow $\text{Si}_{1-x}\text{C}_x$ alloys is by Posthill *et al.* [11] using Remote PECVD. They have reported a fairly thick alloy of over 7 μm with total C concentrations of about 3.5%. A $\text{Si}_{0.965}\text{C}_{0.035}$ alloy, with all the carbon on substitutional sites, grown on Si should have a lattice parameter perpendicular to the substrate, a_{perp} ranging from 0.5365 nm (fully relaxed) to 0.5315 (fully strained). However, the measured a_{perp} in that study was 0.5426 nm. This lattice constant contraction corresponds to a residual strain corresponding to 0.2 % C on substitutional sites. This suggests that there may be some carbide precipitation and / or strain relaxation in those films. The films were also highly dislocated. Nevertheless, their result is quite encouraging. Other attempts to grow such alloys from the gas phase invariably result in the deposition of the carbide phase, or very rough films, though very good morphology of β -SiC SLS have been reported by Sugii *et al.* [12] on Si (111) using gas source MBE at 900°C.

We have used solid source Molecular Beam Epitaxy (MBE) to synthesize $\text{Si}_{1-x}\text{C}_x$ layers and strained layer superlattices (SLS) with C concentrations of a few percent. We have used elemental C sources from resistively heated graphite filaments [13], or by electron beam evaporation. The growth of Si in the presence of C is a formidable challenge and strides in Si epitaxy have in fact been a consequence of the reduction of the C background in the reactor both for MBE and CVD techniques. Early work [14] shows that C on the surface especially at moderate to high temperature results in the formation of SiC particles that pin the motion of steps. This in turn leads to the disruption of epitaxy and in severe cases to 3-dimensional nucleation of Si on the growing surface. In fact reduction of C background in the reactor has been a prime consideration for growing high quality epitaxial films both by CVD and MBE.

Growth of $\text{Si}_{1-x}\text{C}_x$ alloys and SLS

The tendency to island or nucleate 3-dimensionally depends on several factors including interface and surface free-energy considerations and strain. The presence of nucleating centers such as C or SiC particles on the growing surface will enhance this tendency. Fig. 2 shows a cross-sectional Transmission Electron Micrograph (TEM) of a nominally 100 nm thick layer with about 0.1% C with a thin 20 nm Si Cap. (The layer also contains Ge of roughly 1% to compensate for strain effects.) This morphology of the film is very rough and highly islanded. The ratio of the C/Si flux was 0.001 and the Si growth rate was 0.02 nm/sec. The growth temperature was about 550°C. Besides being islanded, the layers are also highly twinned. Notice that the Si cap layer grown conforms to the islanded morphology.

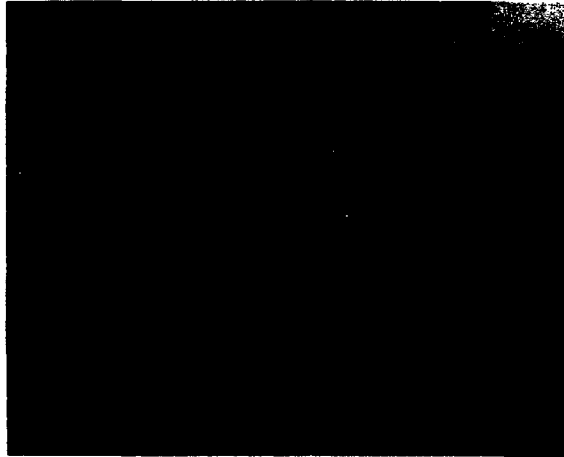


Fig. 3. Cross sectional TEM of a 20 period Si(26 nm)/Si_{1-y}C_y (y=0.015, 4 nm) strained layer superlattice grown on Si at 500°C.

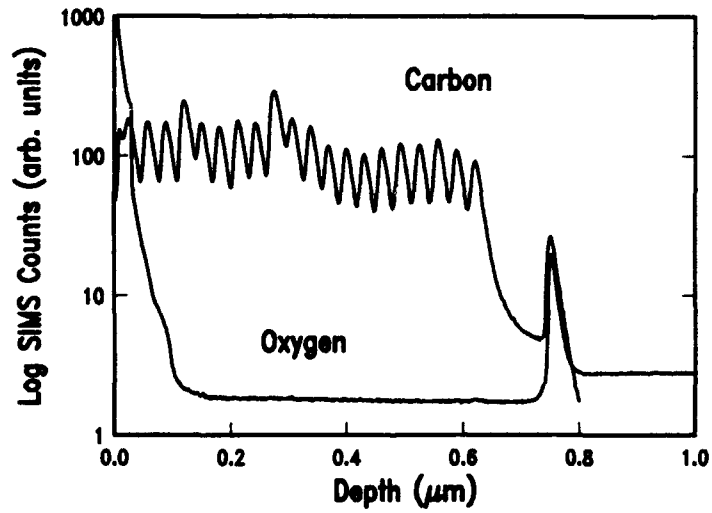


Fig. 4. SIMS profiles (C and O) for the superlattice in Fig. 3. The oxygen level in the epitaxial layers is below that in the substrate.

The morphology can be improved by lowering the growth temperature. This is seen in Fig. 3, which shows the cross sectional TEM for a $\text{Si}/\text{Si}_{1-y}\text{C}_y$ SLS. Fig. 4 shows the SIMS plot for the C and oxygen concentration in the film. Fig. 5 shows a double crystal X-ray rocking curve for the superlattice. Note that the first 10 layers were grown with $y=0.0086$ and the subsequent layers were grown with $y=0.015$. The X-ray diffraction also shows two peaks labelled a and b in Fig. 5 that correspond to these two concentrations. The contrast in the TEM follows the the C concentration profile obtained by SIMS. The $\text{Si}_{1-y}\text{C}_y$ layer is estimated to be about 4 nm and the Si layer about 26 nm. The oxygen concentration in the films is below that in the substrate and comparable to that in Si films grown under similar conditions. The defect density in the lower concentration part of the film is below TEM detection levels. Some threading dislocations have been observed to originate in the layer with the highest C concentration (layer 12) and these propagate to the surface. The key differences between this structure and the one in Fig. 2 is the increase of the Si flux to about 0.4 nm/sec. while increasing the C flux as well. The rationale here is to keep the Si growth rate sufficiently high so that the C flux does not disrupt epitaxy. The growth temperature in this case was about 500°C.

Increasing the C concentration to even higher levels results in a highly twinned crystal growth. We have found that if the C flux is increased beyond a critical value without increasing the Si flux a transition to amorphous growth can occur even at 500°C. Thus the Si flux, the C/Si flux ratio, and the growth temperature define an acceptable process window where good quality $\text{Si}_{1-y}\text{C}_y$ films may be grown. We also expect that this window is larger when single alloy layers rather than superlattices are to be grown.

Thermal stability of $\text{Si}/\text{Si}_{1-y}\text{C}_y$ SLS

Thermal stability of these layers is important especially for VLSI processing. We have annealed as-grown $\text{Si}/\text{Si}_{1-y}\text{C}_y$ SLS at temperatures from 600° C to 1100° C. We consider here the case of a 20 period $\text{Si}(25 \text{ nm})/\text{Si}_{1-y}\text{C}_y(5 \text{ nm})$ ($y=0.003$) SLS. Fig. 6 shows X-ray diffraction results for the as grown sample and those annealed at 900°C and 1100°C for one hour. Fig. 7 shows the SIMS profiles for these conditions. The x-ray results show both the (400) Si peak (mainly from the substrate) and the peak corresponding to the average strain in the SLS quite distinctly. Higher resolution scans over wider angle show well resolved higher order peaks with well defined pendellosung fringes for the as-grown SLS. This implies that the interfaces between the Si and $\text{Si}_{1-y}\text{C}_y$ layers are sharp and well defined, to a far better degree than can be ascertained by SIMS. Note also that we have intentionally put several marker layers of somewhat higher C layers, the purpose of which is to study the effect of increased C concentration on thermal stability. First we consider the 900°C results. X-Ray diffraction shows that the average level of strain has not changed. However, in wider angle high resolution scans (not shown here), the fringes disappear. This is consistent with the loss of the sharply defined $\text{Si}_{1-y}\text{C}_y$ layers mainly due to interdiffusion. This conclusion is also borne out from the SIMS results which show a smearing of the profiles especially for the lower C levels. At 1100° C, not only do the satellite peaks disappear, but the peak corresponding to the average strain in the layer moves towards the substrate peak. Since the SIMS profile shows that the carbon is segregating to the layers with high initial concentration, the loss of strain is most likely due to SiC precipitation, which represents the thermodynamically stable phase for this level of C in Si. TEM shows that large (100 nm) precipitates have formed around these layers. We conclude that the SiC relaxes by interdiffusion at temperatures $\leq 900^\circ\text{C}$. At temperatures $\geq 1000^\circ\text{C}$, precipitation presumably of SiC,

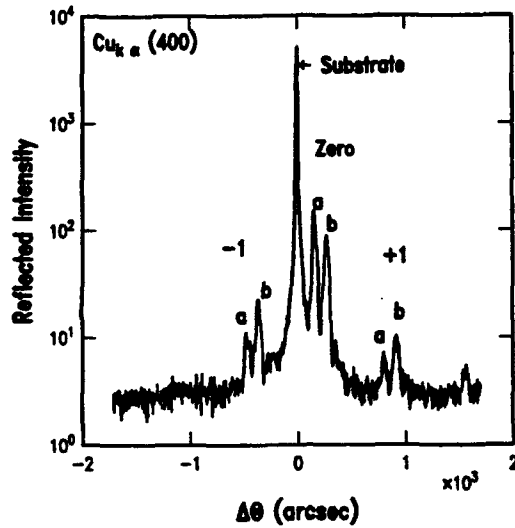


Fig. 5. Double crystal X-Ray diffraction (400) of the superlattice shown in Fig. 3. The peaks for the Si substrate (400) reflections and for the two distinct $\text{Si}_{1-y}\text{C}_y$ (a) $y=0.0086$ and (b) $y=0.015$ epitaxial layers corresponding to the SIMS plot of Fig. 4.

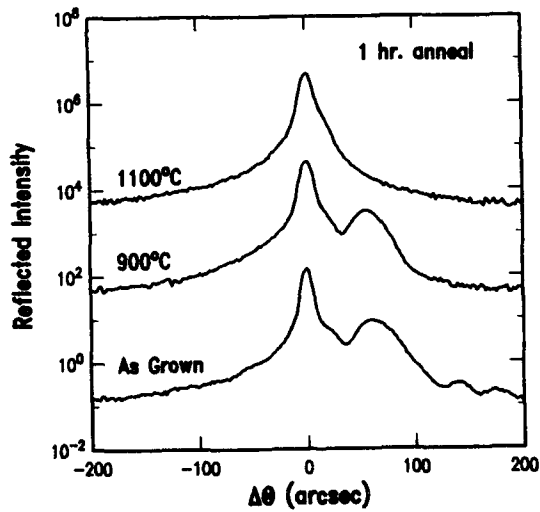


Fig. 6. X-ray rocking curves for a $\text{Si}(25 \text{ nm})/\text{Si}_{1-y}\text{C}_y$ ($y=0.003$, 5 nm) SLS as-grown and after annealing at 900°C and 1100°C .

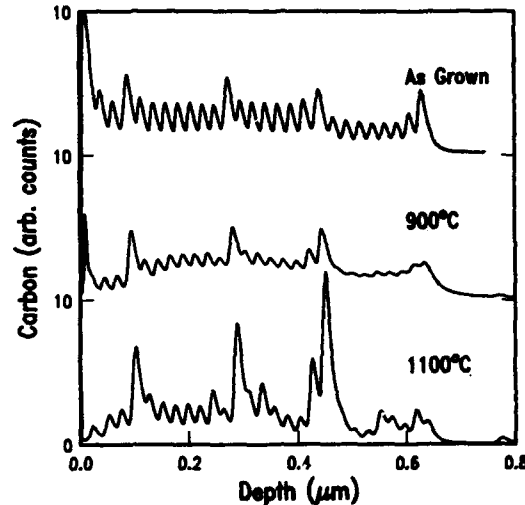


Fig. 7. SIMS profiles for C for the SLS of Fig. 6 showing breakdown by interdiffusion at 800°C and silicon carbide precipitation at 1100°C. The curves are offset for clarity.

is the preferred mode of relaxation. Interestingly, misfit dislocation generation is does not appear to be a preferred mode of relaxation.

Conclusions

Our ability to grow high quality $\text{Si}_{1-y}\text{C}_y$ alloy and SLS layers adds a new dimension Si-based bandgap engineering with the possibility for integration of a potential wide bandgap semiconductor with Si technology. The key features of our growth technique are the control of the C/Si flux ratio, the total Si flux and the growth temperature. Pseudomorphic $\text{Si}_{1-y}\text{C}_y$ layers with $y > 0.02$ can be grown under the right conditions. If the C flux is allowed to increase without corresponding increase in the Si flux, twinned or even amorphous growth can result. Also, at high temperatures there is a tendency of the films to island and form SiC precipitates. Our layers are stable to about 800°C (for $y=0.003$). Thereafter, breakdown occurs via two modes: interdiffusion at lower temperatures ($\leq 900^\circ\text{C}$) and silicon carbide precipitation at higher temperatures ($\geq 1000^\circ\text{C}$). The carbide precipitation process is nucleated at regions of pre-existing high C content and grow at the expense of the dissolved C.

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ELECTRONIC STRUCTURES FOR $(\text{Si})_m(\text{GaP})_n$ SUPERLATTICES

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ABSTRACT

This paper reports on a tight-binding calculation of the band structures of the Si-GaP superlattice (SL) systems with emphasis on the results of the band gap properties. This calculation finds that the SLs grown onto the [110] or [111] oriented substrate do not produce direct gap materials. On the other hand, some of the [001] oriented SLs become direct gap materials when either an interface (IF) state is created at the P and Si IF, or a confined state in the Si occurs with only Ga and Si atoms forming all the IF.

INTRODUCTION

The recent progress in the Molecular Beam Epitaxial (MBE) technology has created much interest in the fabrication of materials with alternate layers of elemental and compound semiconductors. These systems grown sequentially upon a suitable substrate offer possible new applications to optoelectronic devices because of their flexibility in "energy band tailoring" by changing the thickness and composition of each individual well and barrier, and by controlling the atomic layers at the IF.

The Si-GaP system under consideration is of particular importance in the extension of Si technology to luminescent devices. Unlike the Si-Ge system, the present system is lattice-matched and has large band offsets. Thus the complicate effects of strain can be avoided. This system is also different from the type I compound semiconductor SL, GaAs/AlAs, where both compounds have the same kind of anions. Therefore many new features appear in the energy band structures of this system. Both the Si and the GaP crystals have indirect energy gaps. The conduction band (CB) minima of Si and GaP are at $(0,0,0.85)$ and $(0, 0, 1)$ points of the Brillouin zone (BZ) respectively. Thus the zone folding effect along [001] direction for [001] and [110] SL systems brings the hope of generating new Si-related direct gap materials.

Theoretical work on the SL band structures determination has been carried out commonly in the past by two approaches. For very small period SL materials tight-binding approximation [1,2] or empirical pseudopotential method [3,4] were used to determine full three dimension band structures. For large period SL materials the envelope function approach in the framework of the k·p approximation [5,6] is used frequently to examine many interesting problems such as band mixing, doping and excitonic effects. In the present work a tight binding supercell method is used. For the [001] oriented substrate three types of SL are studied. We use m and n to denote the number of atomic layers in $(\text{Si})_m(\text{GaP})_n$. For n odd, the interface (IF) Si layer is next to the Ga layer in the $(\text{Si})_m(\text{GaP})_n$ system and to the P layer in the $(\text{Si})_m(\text{PGa})_n$ system whereas for n even, two types of IF exist in both systems; one IF has a Ga atom layer and the other IF has a P atom

layer. SLs along [110] and [111] directions are also studied.

METHOD

The energy bands of the SL are calculated here using the tight binding (TB) supercell method. The advantage of using this method to obtain a three dimensional band structure is that the size of the Hamiltonian matrix in the present representation is manageable even for larger period SLs. Thus consistently using the same method, we can examine the cases ranging from a few monolayer SL structures to thicker SL in the multiple quantum well limit. The physics of the evolution of each level is then easy to follow.

The TB matrix elements are constructed based upon the formalism of the two center integrals developed in [7,8]. The two center parameters for GaP are obtained from [8]. The parameters for Si are listed in Table I which differ from those in [7] but give better fit to the band structures of pure Si crystals.

Table I. Parameters for Si two center integrals.

(Notations follow those in ref.7, Table IV.)

A =3.6674eV	B=0.7252eV	C=0.
a _{ss} =15.4989eV	a _{pp} =16.0043eV	a _{sp} =14.9495eV
E _{ss} (000)=-3.9287eV		E _{ss} (000)=2.4449eV

The unit cell of [001]-(Si)_m(GaP)_n is simple tetragonal with m+n atoms per cell when m+n=4*integer. The [110] SL unit cell is also a simple tetragonal when m+n=even integers. It has 2(m+n) atoms per unit cell. The [111] SL on the other hand has hexagonal unit cell when m+n=6*integers. It has m+n atoms in a cell.

As the unit cell becomes larger for larger period SL the Brillouin zone (BZ) compresses along the SL axis and multiple zone folding results. For a [001] (m X n) SL the points (0, 0, 4N/(m+n)), with N equal to integers, fold onto the Γ point. For [110]-(m X n)SL the point (0,0,1) and the points (t, t, 0), with t=2N/(m+n), fold onto the Γ point of the BZ. Because the valence band (VB) edge for both Si and GaP occur at the Γ point but the conduction band (CB) minima are near and at the X point for the bulk materials, this zone folding property of the SL provides a possibility of getting direct gap materials if the X bands which fold onto the Γ point move to lower energy in comparison with the X bands perpendicular to the SL axis.

Band-edge discontinuity has been a concern in the band structure determination for SL. The Si-GaP system is known to have a large band offset. A prediction from measurements gives a VB discontinuity of 0.8eV.[9] A theoretical prediction which is based on the "universal theory", and which takes into account the tunneling current of the electronic states in the VB but ignores the defects or interface states, gives a value of 0.50eV.[10] In the present calculation we use the 0.8eV value. We found that changing this value does not alter the results qualitatively.

RESULTS

[001] (GaP)_n(Si)_m.

The results for the conduction band energy levels at symmetry points of a (2 X 2)SL are shown in fig. 1. (The zero energy is set at the valence band edge of Si throughout this work). The dashed lines lead to the states at (100) of the BZ. The CB minimum therefore occurs at the (100) point instead of the (001) point which folds onto the Γ point. Both levels are GaP-bulk like but extending to the P-Si IF. This indicates that the (2 X 2)SL is still an indirect gap material. However, increasing the thickness of the Si layer changes the ordering of the CB levels at different points of the BZ as given in fig. 2. For (2 X m)SL with $m > 22$, the CB minimum is located at the center of the BZ. The material then becomes direct gap. An examination of the wave function of this state reveals that this state localizes more at the P-Si IF just as the VB edge state localizes more at the Ga-Si IF as m increases. These two states rapidly converge to the energies of two IF states for large period SL and will not contribute to the transport property of the material along the SL axis direction.

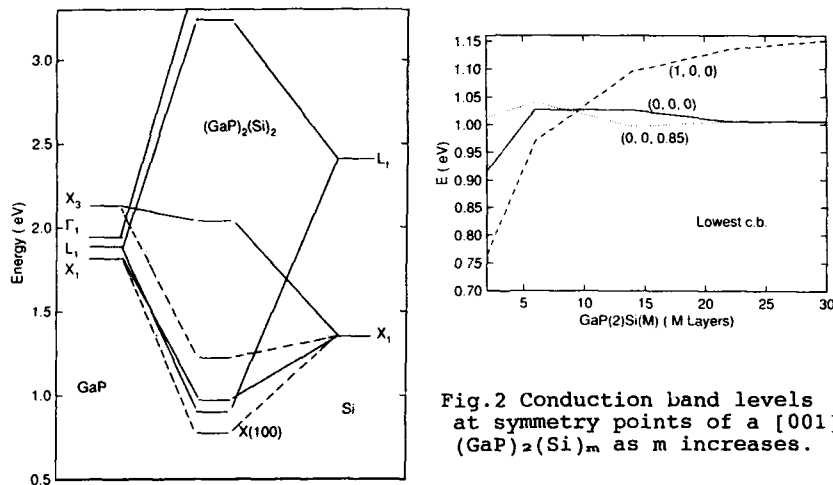


Fig.1 Conduction band energy levels at symmetry points for GaP, Si and the [001] (GaP)₂(Si)₂ SL.

Because the conduction band minimum is an IF state for large n or m , this state is very sensitive to the IF layer structure. For even number of n and m , the changes of the energy as functions of n and m are displayed in fig.3. It is found that this state converges to the IF state energy at $E_c=0.99\text{eV}$ (and the direct gap converges to 0.77eV) for large n and m . The wavefunction squares for this state in the case of $n=m=14$ SL is given in fig.4 where the dashed lines are the

locations of the IF Si layers. (The layer #11 is P layer and the layer #28 is Ga layer.) It can be seen that the CB min. state is localized near the P-Si IF. The degree of localization of both the CB min. and the VB max. states affects the oscillator strength of the direct optical transition and is strongly dependent upon the n and m . For large values of n and n/m the states immediately above the CB min. and below the VB max. at Γ become the confined quantum well states. Direct optical transition is allowed between these two states.

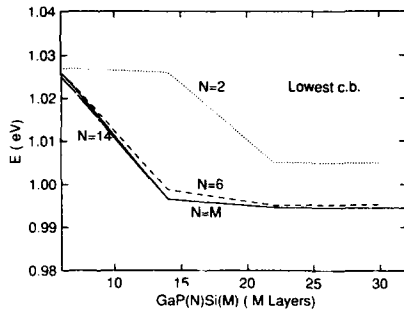


Fig.3 The lowest conduction band energy for even n, m in $(\text{GaP})_n(\text{Si})_m$ systems.

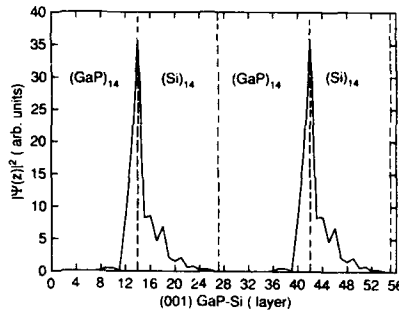


Fig.4 The wave function square of the CB minimum state in a $(\text{GaP})_{14}(\text{Si})_{14}$ SL.

For odd numbers of n and m the two IFs involved are identical. We denote $(\text{GaP})_n(\text{Si})_m$ when Ga atoms are at both IFs of the system, and $(\text{PGa})_n(\text{Si})_m$ when P atoms are at those IFs of the system. As displayed in fig.5 and fig.6 the CB min. state for these two cases appear quite differently from the case of even n and m in fig.4. In fig.5 when Ga layers are next to Si, the CB min. state becomes a confined well state whose energy increases to 1.429 eV as expected. The VB max. state is still a Ga-Si IF state. The direct transition then occurs at 1.2eV. Fig.6 shows a CB min. state being an IF state localized at both edges of the Si well when P layers are next to the Si well. In the latter case the VB max. becomes a confined quantum hole state and the direct gap at Γ is at 1.15eV.

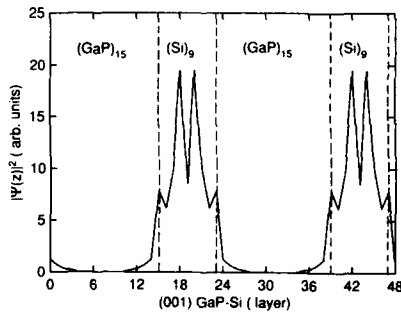


Fig.5 The wave function square of the CB min. state of a $(001) (\text{GaP})_{15}(\text{Si})_9$ SL.

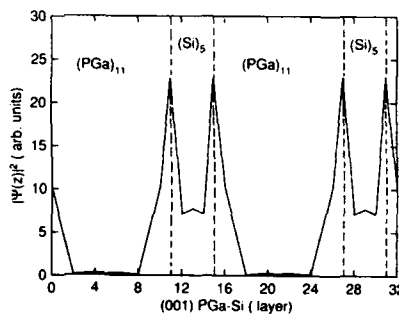


Fig.6 The wave function square of the CB min. state of a $(001) (\text{PGa})_{11}(\text{Si})_5$ SL.

Since this calculation is carried out for an ideal IF, the occurrence of the intrinsic IF states in this homopolar / heteropolar SL, but not in the III-V/III-V SL, suggests that the intrinsic IF states are primarily controlled by the different nature of the IF chemical bonds as compared to the bulk bonds. It does not arise from the possible change of IF geometry in the SL under consideration.

[110] (GaP)_n(Si)_m.

The [110] IF is nonpolar. No charge accumulation at the IF nor any electrostatic dipole layer is expected. Therefore ideal planar geometry and abrupt IFs are allowed for this SL system. Previously Madhukar and Delgado investigated the valence bands of this system. However, no result for the CB was presented.[11] In the present work we find that the CB state folded onto the Γ point is in higher energy than that at the (100) point in the BZ. The difference in energies is between 0.2eV and 0.4eV for a wide range of $n \times m$ SLs. Therefore no direct gap appears in any of the [110] SL considered here. This result is quite different from that for the Si/Ge [110] SL system which becomes direct gap.[12]

The two highest VB states are found to be confined hole states. As we change the band offset from 0.8eV to 0.5eV, the VB states shift more significantly than the CB states. The highest VB state moves up in energy and becomes an IF state. This agrees with the results reported in ref.11.

[111] (GaP)_n(Si)_m.

The separations of atomic layers in the [111] SL are not uniform. Many systems with different IF can be created. We have examined the [111]-(12 X 6)SL, (6 X 12)SL, (12 X 12)SL and (3 X 9)SL with different IF arrangements. The CB min. of all the SL considered are at the BZ boundary (001) point as expected. Because they remain indirect gap materials just as the Si/Ge [111]SL,[13] they generate no interest in the optoelectronic device application.

SUMMARY

Using a tight-binding supercell method we calculate the band structures for the Si-GaP SL in three different orientations, [001], [110], and [111]. For the [001] case we also consider three systems with different IF.

Intrinsic IF states and confined quantum states for both electrons and holes are found. No direct gap is found for the systems with [110] or [111] orientations. Direct gap is found for some systems with [001] orientation in the case when both the CB min. and the VB max. become IF states and in the case when both IFs are composed of Si and Ga atoms. The change of band discontinuity values does not affect the qualitative results of the present calculations.

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EPITAXIAL GROWTH OF PEROVSKITE TYPE OXIDE FILMS ON SI SUBSTRATES

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ABSTRACT

Epitaxial growth conditions of perovskite type oxide films on Si substrates are theoretically considered from a viewpoint of lattice matching. Then, epitaxial growth of SrTiO₃ films and BaTiO₃ films on Si(100) substrates has been tried, in which in order to deoxidize the SiO₂ layers on the substrates, thin Sr layers are deposited prior to deposition of the oxide films. It has been found from X-ray diffraction, reflection high energy diffraction, and Rutherford backscattering analyses that SrTiO₃ films grow epitaxially on Si(100) substrates under the optimum conditions of the Sr layer thickness, deposition temperature, and annealing temperature.

INTRODUCTION

Epitaxial growth of perovskite type oxide films on Si substrates will become important in fabrication of future functional LSIs, since these oxide films show such interesting properties as ferroelectric, piezoelectric, insulating, conducting, semiconducting, and superconducting properties. For example, heteroepitaxial structures composed of superconducting films and Si substrates are considered to be a basic structure to fabricate merged devices of semiconductor and superconductor. However, it is known to be difficult to grow oxide superconducting films on Si directly, because of interdiffusion of constitutional atoms. Even in the case of the more stable films, growth of oxide films on Si is not easy because of formation of interfacial SiO₂ layers.

So far, several methods to overcome the SiO₂ problem have been proposed and the growth of such oxide films as Al₂O₃MgO [1], YSZ [2], (Sr,Ba)O [3,4], Al₂O₃ [5], and CeO₂ [6] has been reported. However, no successful growth of perovskite type oxide films on Si has been reported, except our preliminary result on the oriented growth of SrTiO₃ films [7]. In this paper, we first discuss possibility of the epitaxial growth of perovskite type oxide films on Si from a viewpoint of lattice matching. Then, we present the experimental results on the growth of SrTiO₃ (STO) and BaTiO₃ (BTO) films on Si substrates.

LATTICE MATCHING BETWEEN PEROVSKITE TYPE OXIDES AND SI

The lattice constants of typical perovskite type oxides are shown in Table 1, together with their crystal structure and electrical properties. As can be seen from the Table, the lattice constant "a" is about 0.39 nm in all these cubic and tetragonal crystals. Since the lattice constant "a" of Si is about $\sqrt{2}$ times larger than these values, exact or approximate lattice matching can be expected between them, when the orientation of the oxide crystals is rotated around the surface normal axis by 45° on Si(100) or by 90° on Si(110). The epitaxial relations are schematically shown in Fig.1 for an STO/Si structure. It is interesting to note that the lattice mismatch between these oxides and Si is less than 4% when (100) and (110) substrates are used, and that it is independent of the electrical properties of the oxides.

EXPERIMENTAL PROCEDURE

In the experiment, epitaxial growth of both STO and BTO films on Si(100)

substrates was tried using a focused electron beam evaporation system shown in Fig.2. In this system, an electron beam generated in the gun room is transported to the deposition chamber using magnetic lenses and deflectors, and it can be scanned among various evaporation sources in the chamber. Typical voltage, current, and diameter of the beam used in this experiment are 12 kV, 8 mA, and 0.5 mm, respectively. The chamber was pumped with a turbomolecular pump down to a pressure lower than 1×10^{-5} Pa.

In the sample preparation, n-type Si(100) wafers were chemically cleaned in organic solvents, dipped in HF solution, and loaded in the chamber. First, in order to deoxidize the surface SiO₂ layers on Si, Sr layers about 10 nm thick were deposited on the Si substrates kept at 750°C with a typical growth rate of 1.5 nm/min. The pressure during film deposition was 2×10^{-4} Pa. It is expected that the Sr layers are changed to SrO during and after deposition, partially by deoxidizing the SiO₂ layers on Si and partially by reacting with residual oxidizing gases, and that the SrO layers grow epitaxially on the Si substrates at least in limited areas, as has been reported previously [3].

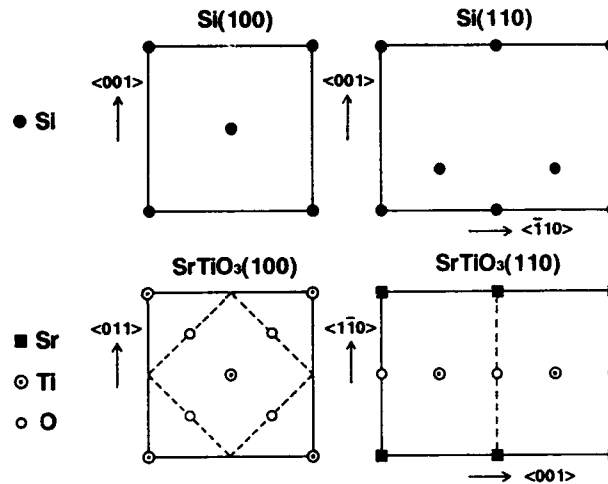


Fig.1 Lattice matching conditions between STO and Si

Materials	Crystal Structure	Lattice Constant (nm)	Electrical Properties	Mismatch to Si
SrTiO ₃	Cubic	0.391	Insulator	+1.8%
Sr ₂ TiO ₄	Tetragonal	a=0.388 c=1.260	Insulator	+1.1%
PbTiO ₃	Tetragonal	a=0.389 c=0.414	Insulator (Ferroelectric)	+1.3%
BaTiO ₃	Tetragonal	a=0.399 c=0.404	Insulator (Ferroelectric)	+3.9%
SrVO ₃	Cubic	0.384	Conductor	0%
YBa ₂ Cu ₃ O _{7-x}	Orthorhombic	a=0.389 b=0.383 c=1.168	Superconductor	+1.3%

Table 1 Lattice constants of typical perovskite type crystals

Then, STO or BTO films were deposited on the SrO layers at 750°C and 800°C, respectively. In the deposition of STO films, single crystalline STO grains were evaporated using a focused electron beam, while in the deposition of BTO, both polycrystalline BTO grains and TiO₂ pellets were alternately evaporated by scanning the beam to obtain the stoichiometric films. The thickness of the films ranged from 40 nm to 240 nm. In some cases, STO films were deposited onto Si substrates without depositing the Sr layers for comparison. During the deposition process, oxygen gas was not intentionally introduced in the chamber. The deposited samples were finally annealed in oxygen atmosphere at 800°C for 1 to 5 hours.

The crystalline quality and composition ratio of the films were characterized by Rutherford backscattering spectroscopy (RBS) with 1.5 MeV He⁺ ions. The crystalline quality and crystallographic orientation of the films were examined by X-ray diffraction analysis and reflection high energy electron diffraction (RHEED) with an energy of 10 keV.

EXPERIMENTAL RESULTS

Figure 3 shows X-ray diffraction patterns of STO films which were grown on Si(100) with SrO layers and annealed with various periods. We can see from the figure that the films have a cubic perovskite type crystal structure and they are strongly oriented along a (100) direction of the substrate. We can also see that the intensity of the diffraction peaks increases with increase of the annealing time at 800°C. It was found from the rocking curve measurement that the full width at half maximum (FWHM) value of the (200) reflection was 1.0°. On the other hand, the patterns for the STO films deposited without the interfacial SrO layers showed no peaks when their thickness was thinner than 100nm and showed weak polycrystalline peaks for the thicker cases.

The variation of the intensity of the (200) peaks with the annealing time is summarized in Fig.4 for the samples with different film thicknesses. As can be seen from the figure, increase of the intensity is pronounced in the initial 4 hours, which suggests that the annealing at 800°C is effective to improve the crystalline quality of the films. X-ray diffraction analysis was also done for BTO films grown on the interfacial SrO layers. A typical result is shown in Fig.5, in which a BTO film 65 nm thick was deposited at 800°C and

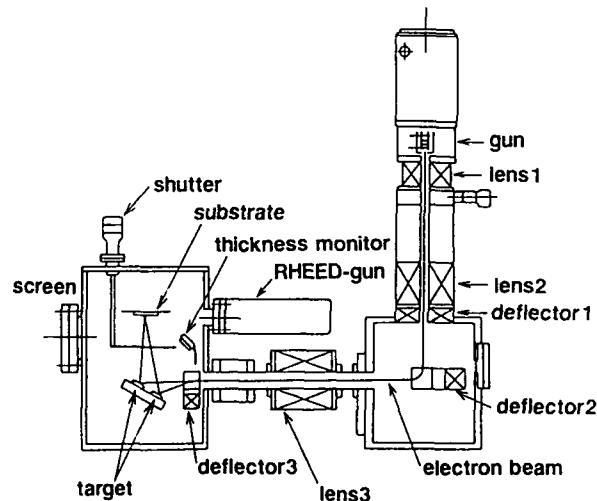


Fig.2 Schematic diagram of a focused electron beam evaporation system

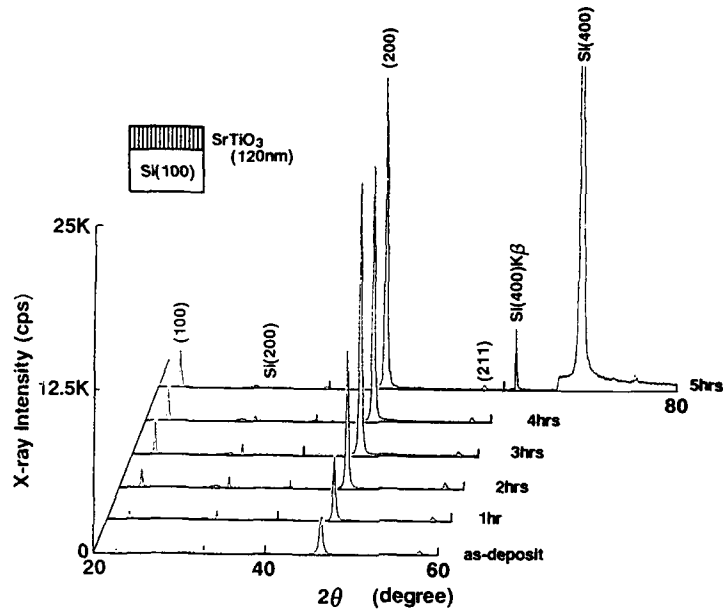


Fig.3 X-ray diffraction patters of STO/Si samples

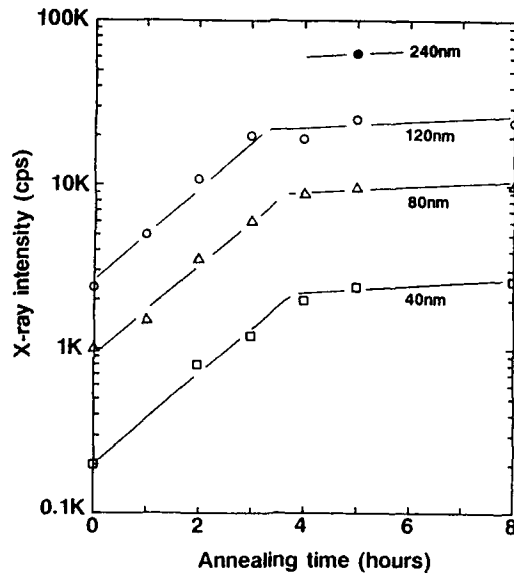


Fig.4 Variation of the Intensity of (200) peaks with annealing time

annealed at 800°C for 1 hour. We can see that the BTO film is oriented along a $\langle 100 \rangle$ axis of the substrate, but that the intensity of the peaks is much weaker than that of STO. This result indicates that the growth conditions of BTO films must be optimized in order to realize the epitaxial growth.

Figure 6 shows RHEED patterns along [010] and [011] azimuths of a 120-nm-thick STO film grown on Si(100). The film was deposited at 750°C and subsequently annealed at 800°C for 5 hours. These micrographs show clear streak patterns, indicating successful epitaxial growth of the film. Distances between two streaks in (a) are nearly equal to those along the [011] direction of Si substrate, while the distances in (b) are equal to those along the [001] direction. These relations show that the unit cell of STO is rotated by 45° on the Si substrate. On the other hand, the patterns for the samples without the interfacial SrO layers showed many rings and spots, which indicates that the films are polycrystalline.

Figure 7 shows random and aligned spectra of the same sample as shown in Fig. 6. We can see from the figure that composition of the film is about Sr:Ti = 1:0.98 except the interface region. The Ti composition near the interface is less than 10% and the thickness of the SrO-rich layer is about 20-40 nm. The channeling minimum yield which is defined as a ratio of the aligned yield to the random one is about 28% near the surface and about 55% near the interface. We conclude from this result that the STO film grows epitaxially on a Si(100) substrate, although the crystalline quality of the SrO-rich interface layer is relatively poor. We can also see from this figure that the film quality will be further improved by optimization of the deposition condition of the Sr layer.

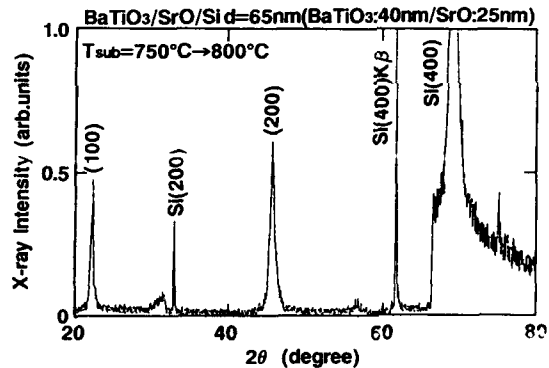


Fig.5 X-ray diffraction pattern of a BTO/Si sample

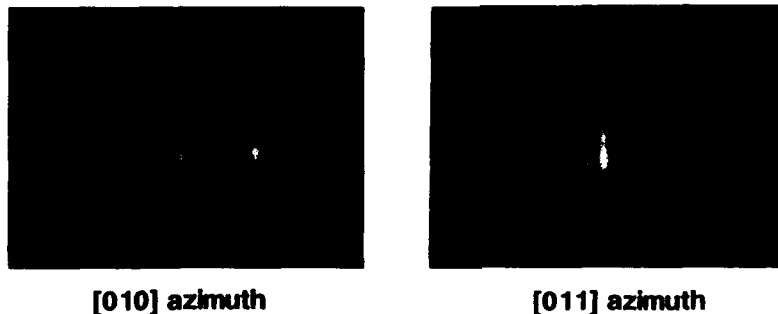


Fig.6 RHEED patterns for STO/Si structures. The incident directions of the beam are (a) STO[010]//Si[011] and (b) STO[011]//Si[001].

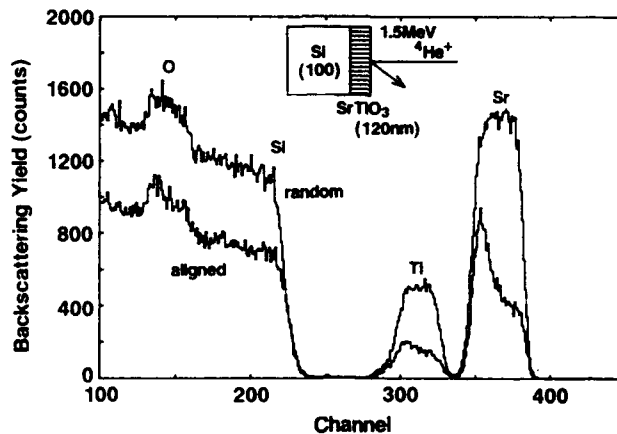


Fig.7 Rutherford backscattering spectra for an STO(120nm)/Si sample

CONCLUSIONS

Epitaxial growth conditions of perovskite type oxide films on Si substrates were investigated. Main results obtained are as follows.

- 1) Excellent lattice matching can be expected between the perovskite type oxide films and Si substrates when the orientation of the film is rotated around the surface normal axis by 45° on (100) and 90° on (110).
- 2) Deposition of thin Sr layers on Si substrates is effective to deoxidize the surface SiO_2 layers and to grow oxide films well.
- 3) SrTiO_3 films can be grown on Si(100) substrates by optimization of the Sr layer thickness, the deposition temperature, and the annealing temperature. The best value of the channeling minimum yield so far obtained is 28% near the surface.

ACKNOWLEDGMENT

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STUDIES OF $\text{SiH}_2\text{Cl}_2/\text{H}_2$ GAS PHASE CHEMISTRY FOR SELECTIVE THIN FILM GROWTH OF CRYSTALLINE SILICON, c-Si, USING REMOTE PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION

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ABSTRACT

Conventional high temperature, $>800^\circ\text{C}$, CVD processes, utilizing SiH_2Cl_2 promote selective deposition of c-Si onto c-Si, but not on SiO_2 surfaces. We show that low temperature, 300°C remote PECVD, with rf-excited He plasmas, and SiH_2Cl_2 and H_2 injected downstream, also selectively deposits c-Si on c-Si and not SiO_2 surfaces. This preliminary study employs *in-situ* mass spectrometry, MS, to determine the species responsible for selective deposition process reaction pathways. These MS studies suggest that species responsible for film deposition are Si-containing fragments of the SiH_2Cl_2 molecule, e.g., SiH_2Cl , SiCl_2H , etc., while the species responsible for inhibiting deposition on the SiO_2 surfaces are by-products of the break-up of the SiH_2Cl_2 molecule in the gas phase, e.g., H-atoms, HCl and H_2Cl^+ ions.

INTRODUCTION

Selective homoepitaxial growth of silicon is an important technique that creates unique opportunities for fabrication of high density circuits, and reduction of some photolithographic processing steps. For example, self-aligned techniques for polycrystalline silicon can eliminate the masking step sequence required for producing gate electrodes. A variety of thermal CVD techniques in the temperature range from 850 to 1100°C , based on various combinations of H_2 , HCl, and partially halogenated silane compounds, have been used for selective epitaxial growth of Si [1,2]. Much of the work on the chemistry of the Si/H/Cl system for thermal CVD processes show that there are competing deposition and etching reactions occurring simultaneously [3,4]. However, the high processing temperatures ($> 850^\circ\text{C}$) are undesirable for technologies where dopant diffusion and thermally induced stress must be minimized, or for heterojunction devices where compound semiconductors have already been incorporated into the structure [5,6]. There have been extensive studies of low temperature epitaxial growth of Si [7-9]. For example, by remotely exciting SiH_4 and H_2 with species extracted from a remote He plasma, Tasch et al. have deposited epitaxial Si on Si at temperatures as low as 150°C for thicknesses up to 100\AA , and significantly larger film thickness at temperatures of $\sim 300^\circ\text{C}$ [7]. There are two plasma techniques, other than what we discuss in this paper, by which Si has been selectively grown. Baert et al. have employed a glow discharge to deposit microcrystalline, high conductivity n^+ silicon gate electrodes for CMOS devices, utilizing an SiH_4 and SiF_4 source gas mixture, that also includes the dopant source gas, PH_3 [8]. Yew and Reif have used an H_2 plasma with an alternating SiH_4 flow cycle, to switch between Si deposition and etching, in order to obtain selective Si epitaxial films at 600°C [9]. There are two reasons why remote PECVD is being investigated for low temperature selective deposition studies: i) it intrinsically affords good control over gas phase reaction chemistries; and ii) it minimizes substrate damage associated with bombardment by energetic ions, as in conventional PECVD utilizing capacitively coupled reactors.

In order to understand how the selective process operates, it is necessary to understand and separate those chemical reactions that occur in the gas phase, e.g., the formation of deposition and etching precursors, and at the specific substrate surfaces, e.g., c-Si and SiO_2 . The primary goal of this work is to determine the species that contribute to selective silicon deposition using remote PECVD. We start by determining what the species are formed in the gas phase by the break-up of the SiH_2Cl_2 molecule in the presence of H_2 . By studying the effect of the H_2 flow rate for a constant flow rate of SiH_2Cl_2 , we can identify the way SiH_2Cl_2 is fragmented in the gas phase by interaction with plasma generated species from a H_2 and He discharge. We then discuss the way that these species can react at the respective Si and SiO_2 surfaces to either promote or inhibit Si deposition.

EXPERIMENTAL TECHNIQUES AND RESULTS

The chamber used for this study embodies all of the attributes of a remote PECVD system, and in addition it provides *in-situ* analysis of the gas species in the chamber by MS, and non-intrusive analysis of radiating species by optical emission spectroscopy, OES. The

inner diameter of the chamber is 14.9 cm, and the length is 56 cm (see Fig. 1). One end of the chamber is connected to a fused silica plasma generation tube with an inner diameter of 3.2 cm. This tube is positioned along the central axis of the chamber. Plasma excitation is

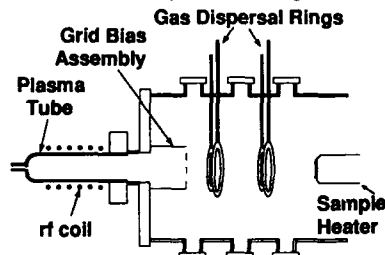


Figure 1: Schematic diagram of the Deposition/Analytical System

achieved at a frequency of 13.56 MHz. There is a grid assembly at the end of the plasma tube that connects to the deposition chamber region of the apparatus. A $4\text{ m}^3/\text{s}$ turbomolecular pump is used to attain a base pressure of $\sim 5 \times 10^{-8}$ Torr. A load-lock assembly located at the other end of the deposition chamber is designed to accommodate an electrically floating piston driven substrate holder/heater assembly. Inside the chamber, at 10.2 cm and 35.6 cm from the plasma tube flange, there are two sets of double gas rings for downstream injection of process gases. There are sampling stations located along the gas stream in three strategic locations: one between the plasma tube flange and the first gas ring, and the other two, 3.8 cm downstream from the each set of gas dispersal rings. These consist of two horizontally aligned pyrex windows for OES, and a vertical port to accommodate the sniffer tube for the MS. The mass spectrometer is an Extrel C-50 $3/8$ " quadrupole mass spectrometer with a mass range of 0-280 m/z, and an independently operated ionizer, so that both neutral and ionized species may be studied.

A series of films were grown on partially oxidized wafers to examine the selectivity of the deposition process. Each wafer is (100) oriented Si and was patterned with 1200Å of SiO_2 , grown by remote plasma CVD. The plasma power is 75W. 100 sccm He is injected through the plasma tube, and 10 sccm of 1% SiH_2Cl_2 in He, and between 0 to 50 sccm of H_2 are injected into the first set of downstream gas dispersal rings. The sample is mounted on a Si-coated copper block heater that is held at 300°C , and is kept 3.8 cm downstream from the first gas dispersal ring. The plasma grid assembly is kept electrically floating, and in this configuration does not block the plasma afterglow from extending into the deposition region of the chamber. After deposition, samples are examined under SEM to determine selectivity and growth morphology, and by RHEED to determine the degree of film crystallinity. Mass spectrometry is used to identify the gas phase species. We have used D_2 for H_2 substitutions in order to determine the parentage of the H-atoms in the various H-containing deposition and etching precursor species.

Figure 2 shows SEM micrographs of the boundaries between the oxide, and the grown c-Si layer. For the samples grown with less than 50 sccm of injected H_2 , there is no selectivity, while for the sample grown with 50 sccm of H_2 flow, selectivity is apparent. However, for this case there are a significant number of isolated Si nuclei on the oxide surface. Figure 3 shows RHEED patterns for the samples grown with 0, 20 and 50 sccm of injected H_2 . The rings of the 0 sccm sample indicate a microcrystalline Si, and a randomly oriented morphology, while the 20 and 50 sccm films, exhibit a spot pattern associated with a preferred orientation of polycrystalline film growth. At the present state of our research effort, film growth is limited by the low effective flow rate of the Si-source gas species, 1% SiH_2Cl_2 in He. To achieve selective film growth the films must be grown in a sequence that loads the chamber walls with active deposition, and also possible etchant species. This is accomplished by a 10 hour flow of sccm H_2 , 10 sccm 1% SiH_2Cl_2 + He, and 100 sccm He, with remote excitation of the He at 75 W. Using this pre-deposition process, we achieve reproducible selective film growth.

Figures 4 through 6 show the results of the MS in-situ monitoring. Figure 4 shows the cracking pattern of SiH_2Cl_2 in He, for masses 0-110, by a 70 eV electron beam energy in the MS ionizer. The electron-initiated cracking of SiH_2Cl_2 produces di- and mono-chlorosilane groups at 98-103, and 63-67 m/z, respectively, an HCl/Cl group with masses 35-38, and a silane group with masses 28-30. Mass 30, corresponding to SiH_2 is mostly absent, and the peaks above mass 31 are actually doubly ionized mono-chlorosilane fragments. Figure 5

shows the change in intensities for these peaks for mass 25 to 110, as the H_2 flow rate increases with the plasma power fixed at 75 W. As the H_2 flow increases, there is an

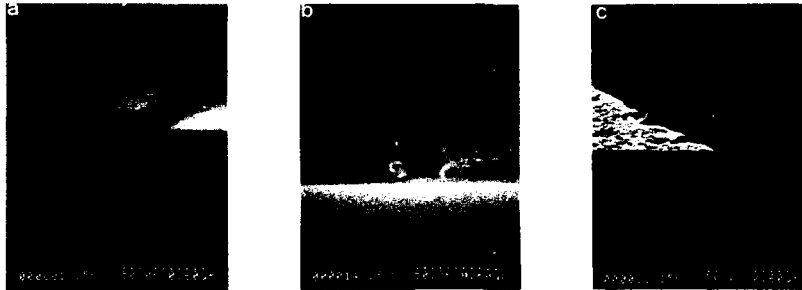


Figure 2: SEM Micrographs of Deposited Films a) 0 sccm H_2 , b) 20 sccm H_2 , c) 50 sccm H_2 . Deposited at 75W, 300°C, 100 sccm He in the plasma tube, 10 sccm 1% SiH_2Cl_2 + He downstream.



Figure 3: RHEED sample of films shown above, a) 0 sccm H_2 , b) 20 sccm H_2 , c) 50 sccm H_2 .

increase in the mono- and di-chlorosilane, silane, and hydrogen chloride peaks. Additional peaks at mass 31 and mass 39 appear, and the peak at mass 37 increases much more than the other HCl peaks. The major contribution to masses 31 (50%) and 37 (99%), and the only contribution to mass 39 are from ions generated externally to the mass spectrometer. This leads to the conclusion, that peaks 37 and 39 are caused by the formation of H_2Cl^+ , otherwise known as the chloronium ion, which has been well-documented as a species produced in

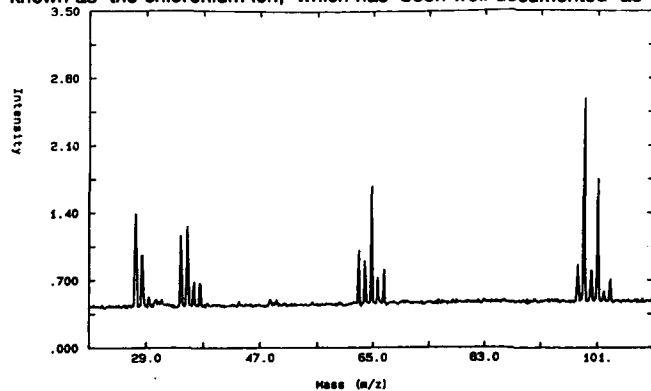


Figure 4: Mass spectrum showing the break-up pattern of SiH_2Cl_2 at 70 eV electron beam.

plasmas of HCl and hydrogen [10]. The mono- and di-chlorosilane peaks are also composed of almost entirely ions. The mono-chlorosilane peak intensities are about twice as large as the di-chlorosilane peaks with the plasma on, whereas in the SiH_2Cl_2 cracking pattern, the mono-chlorosilane peaks are only about half as intense. This is an indication that a Cl stripping reaction occurs under plasma excitation conditions. The silane peaks, particularly masses 30 and 31, associated with SiH_2 and SiH_3 , respectively, do not necessarily come

from the gas phase plasma excited reaction between H_2 and SiH_2Cl_2 . This is shown by striking a He plasma with only H_2 injected, and noting that the peaks associated with masses 30 and 31 are produced in the same proportional as when SiH_2Cl_2 is added. This is one indication that the chamber walls are a significant source of silane species *under these particular flow conditions*, which are lower than those generally used for film deposition. Note further that the relative peak intensities for masses 30 and 31 are not characteristic of the cracking pattern of silane by the MS ionizer, indicating that these species are generated by H-atom etching reactions at the chamber walls. Figure 6 shows results of the same experiment, in which deuterium, D_2 , was substituted for H_2 in order to tag the source of the hydrogen in the

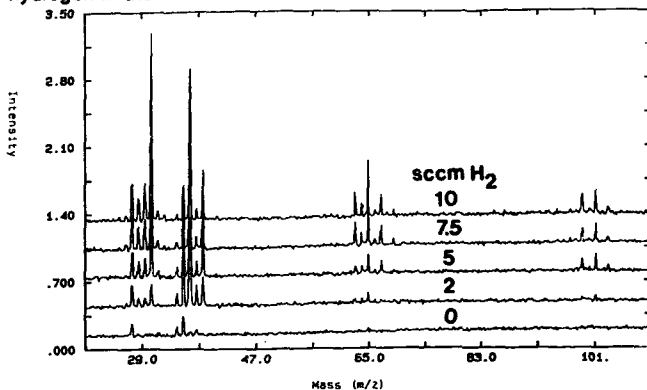


Figure 5: Mass spectra of SiH_2Cl_2 after 75W rf excitation as a function of H_2 flow rate.

same as the injection ratio of the gases, it is evidence that hydrogenation from injected sources is limited. For example, mass 64 can only be from $SiClH$, and mass 65 can be primarily from $SiClD$ and $SiClH_2$.

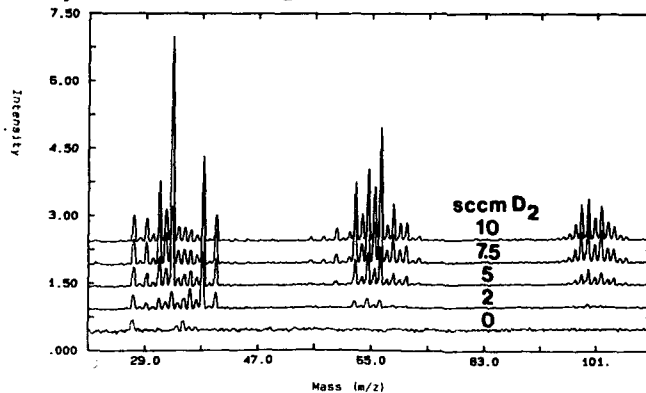


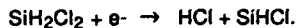
Figure 6: Mass spectra of SiH_2Cl_2 after 75W rf excitation as a function of D_2 flow rate.

larger than for the cracking of SiH_2Cl_2 without the plasma, this demonstrates conclusively that Cl is being stripped from SiH_2Cl_2 in the gas phase. There are two possible mechanisms that may perform the stripping, electron impact dissociation, and H stripping, followed by with ionization. With only SiH_2Cl_2 and a He plasma, or SiH_2Cl_2 in the 70 eV electron beam of the mass spectrometer HCl is formed, with the only source of hydrogen being SiH_2Cl_2 . Since virtually no gas phase collisions occur in the mass spectrometer, the HCl formed is a decomposition product of the reaction,

various species. The additional silane, and mono- and di-chlorosilane peak groups show that D-atoms are substituted for H-atoms. The mass intensities of the entirely deuterated species show the same relative intensities as the same protonated species. But, since the relative peak heights between deuterated and non-deuterated species are not the

DISCUSSION

From the data presented in Figs. 5 and 6, it is clear that the addition of increasing amounts of hydrogen into the chamber, along with its interaction with the plasma, strips Cl from SiH_2Cl_2 . The increase in the Cl and HCl peaks, and disproportionate increase in mass 37 show the production of H_2Cl^+ . Since these peaks are



A similar reaction may occur in the chamber, even though the average electron temperature is much lower than the mass spectrometer ionizing electron beam. In fact, the collision cross section is greatest at electron energies much less than 70 eV. The mechanism would at first seem counter-intuitive with the addition of the downstream H₂, but the electron temperature decrease in the plasma after-glow is offset by an increase in the electron current. This will increase the efficiency of SiH₂Cl₂ cracking, as long as the total number of electrons with energies over the threshold is high. Any hydrogenation of these cracking species apparently occurs afterwards. A hydrogen-ionization/hydrogenation mechanism appears less likely, since the deuterium substitution shows that the injected hydrogen attaches to stripped chlorosilanes and hydrogen chloride species at a much lower ratio of injected D₂ to SiH₂Cl₂, e.g. (3:1 for mass 65:mass 64, at a 20:1 D₂ to SiH₂Cl₂ injection ratio). If the injected hydrogen were performing the dissociations and ionizations, the ratio of peak heights would be expected to be more on the order of the ratio of total deuterium to total hydrogen content in the system.

As shown in Figs. 5 and 6, the concentration of monochloro- and silane species increases with the increasing H₂ injection. The largest change in the mass spectrometer signal is the increase in mass 31, which primarily consists of SiH₃ species. SiH₃ increases to a level that is about 5 times greater than SiH₂, whereas the intrinsic cracking pattern shows that SiH₂ is normally about 15% greater than SiH₃. The production of SiH₃ could be in the gas phase, but it is likely an etching product, associated with the walls of the chamber. When a discharge of He and H₂ is struck with no flow of SiH₂Cl₂, SiH₃ species are easily detected. The only source of Si in the system under these conditions are the fixtures and walls of the chamber. The mass 31 species is apparently formed in a surface etching reaction that directly produces SiH₃. If we assume that mass 30 is due from SiH₄ generation during etching, then at most 15-20% of the SiH₃ can also be attributed to wall-generated SiH₄ arriving unreacted at the mass spectrometer.

The fact that H₂Cl⁺ is found in the gas phase, is very interesting, from the standpoint of it being a possible process active species in inhibiting deposition of the SiO₂ surfaces. H₂Cl⁺ is designated among a group of chemical species known as superacids, which are known to be very strong proton donors. The formation of H₂Cl⁺ occurs in gaseous discharge systems of H₂ and HCl from the attraction of protons to HCl (proton affinity 6.1 eV) [10,11]. Due to the relatively strong dipole of the HCl molecule, it is easy to see that the proton will naturally be attracted to the net negative charge of the chlorine atom. Since HCl is a product of SiH₂Cl₂ decomposition by plasma excited H₂, it can clearly be a reaction intermediate in the process which generates H₂Cl⁺.

There are several possibilities through which H₂Cl⁺ ions may participate in the selective film deposition process. For example, they can hydrogenate the Si surface and promote etching. Protons are much more reactive than H atoms and H₂ molecules, thus more effective in promoting proton initiated surface reactions. Another possibility, is that the proton may be used to "dehalogenate" the Si surface, and promote crystalline rather than amorphous growth [12]. In addition, selectivity may be enhanced by the etching of Si species attached to the oxide preferentially to the Si species on Si. This can be accomplished by proton donation from the H₂Cl⁺ species as well. For example, it will take less energy for a proton to break the donor/acceptor bond between a surface O-atom of the oxide and a Si-atom of an attached silane or di-chlorosilane fragment, than a similar surface Si-atom associated bond on c-Si.

The surface morphology and RHEED patterns show, that at least the surface of the film is polycrystalline, which implicates a secondary etching mechanism, based on arguments of thin film nucleation and growth processes. Assume that both deposition and etching reactions occur on the oxide and the silicon surfaces. The deposition of Si atoms on the c-Si surface can come about in three ways: i) formation of additional nuclei through heterogeneous mechanisms; ii) bonding to existing nuclei; or iii) bonding directly to the substrate. In contrast bonding to the oxide to form a continuous Si layer can only be accomplished by i) and ii), thereby favoring nucleation and growth on the Si substrate over the oxide substrate. Due to the differences in growth morphology, shown in Fig. 2, atoms on the edges and corners of the crystallites on the oxide will be more susceptible to removal by hydrogenation, since they contain more reactive surface bonds. Even though the films shown here are polycrystalline surfaces, there is no reason inherent in this process that would prevent epitaxial film growth. The substrate is on an electrically floating sample stage, which inhibits the formation of a

sheath region about the wafer, thus minimizing any sort of damage that may be produced through ion acceleration. Hsu et. al. have shown that substrate damage sustained by the wafer is primarily from excited hydrogen creation of point defects, but that this technique can grow epitaxial films at 250°C anyway.[13]

As stated in the previous section, it is required that a sequence of "wall loading" depositions be performed in order to achieve selective film growth under these conditions. When this sequence is not followed, the conditions under which selective growth can be obtained, yield no significant film growth. It appears that residue from the previous runs is extracted from the surfaces of the chamber to assist in both growth and etching. However, when the H₂ flow rate is kept at less than 5 sccm, a crystalline film may be grown *uniformly* across the entire sample surface including the Si and oxide regions, and regardless of the previous deposition chamber history. By running a He/H₂ plasma, it is possible to remove all of the species that are apparently active in selective depositions. Since the wall loading plays a key role, it implies that the concentration of etchant and deposition species needs to be increased over what is currently available in our source gas mixtures, e.g., by increasing the effective flow rate of SiH₂Cl₂, or by using a source gas mixture with a higher concentration of SiH₂Cl₂. Independent of the deposition reactions studies at high H₂ flow rates, the mass spectrometry studies provide valuable insight into the breakup of di-chlorosilane in a remote plasma system, including the identification of probable deposition and etching precursors, such as mono- and di-chlorosilane ions and SiH₃, and H₂Cl⁺, respectively.

SUMMARY

This paper has demonstrated the effect of the relative H₂ flow rate on the gas phase species produced in the presence of downstream-injected SiH₂Cl₂/H₂ mixtures with respect to an rf-excited He discharge. The SiH₂Cl₂ is stripped of Cl, producing chlorinated silane ions, and H₂Cl⁺ ions. The H₂Cl⁺ ion is likely to be an etchant species, with the chlorinated silane being a possible deposition precursor. SiH₃ in this system is shown to be an etching product from wall interaction, but is none-the-less also a possible deposition precursor as well. It appears that the dissociation/ionization of SiH₂Cl₂ is caused by an electron impact mechanism, rather than proton attachment. It has been shown that this remotely excited process can produce selectively grown crystalline Si films at 300°C, but under special conditions of wall loading. This work raises several research issues as well. What is the effect of the Si:Cl ratio on the selectivity and deposition? Since H₂Cl⁺ is present, and it is known to be a super-acid, how will fluorine substitution affect the degree of selectivity? These questions are currently under investigation. In particular, we will study remote PECVD using: i) a significantly increased flow rate of SiH₂Cl₂; ii) mixtures of down-stream injected SiCl₄, SiH₄ and H₂; iii) mixtures of downstream injected SiH₄, HCl and H₂; and iv) fluorinated as well as chlorinated hydrides and substituted silanes.

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**GROWTH OF SILICON-GERMANIUM ALLOYS BY ATMOSPHERIC-PRESSURE
CHEMICAL VAPOR DEPOSITION AT LOW TEMPERATURES**

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ABSTRACT

Dichlorosilane and germane were used to grow silicon-germanium alloys at temperatures as low as 550°C at atmospheric pressure. Germanium mole fractions as high as 44% were obtained and the layers exhibit smooth surface morphology. Silicon-germanium/silicon multilayers with abrupt hetero-interfaces have been achieved. Cross Section Transmission Electron Microscopy, (XTEM) and High Resolution X-Ray Diffraction, (HRXRD) characterization of the hetero-interface abruptness will be presented. Recent results on two-dimensional (2-D) hole mobility structures grown by this technique will also be reported. Selective growth of silicon-germanium on oxide patterned silicon wafers was also demonstrated. A significant feature of the selective deposition is the lack of faceting at the oxide sidewall, which has been commonly observed in high temperature silicon growth.

INTRODUCTION

Since the fabrication of high performance SiGe heterojunction bipolar (HBT) devices [1] by Molecular Beam Epitaxy (MBE), there has been an incentive to explore alternative and simpler technologies for the growth of SiGe alloys. Ultra-High Vacuum Chemical Vapor Deposition (UHV/CVD) and Limited Reaction Processing (LRP) have emerged as candidates [2,3], however UHV/CVD is not necessarily less complicated than MBE and is incompatible with chlorosilane-based chemistry. LRP utilizes rapid and large temperature swings, thereby necessitating operation without a susceptor, and may not be practical for large wafers. In this study we have explored the feasibility of using a simpler atmospheric-pressure epitaxial reactor to deposit silicon-germanium alloys. In addition selective deposition was investigated. Abrupt compositional changes were achieved through gas switching, without rapid and large temperature changes.

EXPERIMENTAL

The reactor used in this study has been described earlier [4,5]. Briefly, it utilizes point of use gas purification, a load lock, and rigorously clean operating procedures to insure low levels of oxidizing impurities. Depositions were made from dichlorosilane and germane in H₂ carrier gas. The sample was placed on a SiC coated graphite susceptor and heated radiantly. Growth temperatures as low

as 550°C were used, however the typical growth temperature was 625°C. 125 mm diameter blank or oxide patterned wafers were pre-baked before deposition at 850°C for 10 min in hydrogen to remove native oxide.

RESULTS AND DISCUSSION

SiGe layers have been deposited with up to 44% Ge, as determined by RBS analysis. The growth rate of the Si component of the alloy is found to be enhanced by a factor of 3 to 5 for films containing 25% Ge. In contrast, other work at reduced pressure [6], shows a growth rate enhancement of two orders of magnitude for growth at 625°C and for films containing 25% Ge. In both cases the growth rate enhancement is observed to increase with decreasing temperature.

Figure 1a is a SIMS profile of the Ge content of a layer grown at 625°C. The layer consists of 60 nm of SiGe with a 20 nm Si cap. The Ge content of the film is very uniform at about 22% and exhibits abrupt turn-on and turn-off transients; the 90%-10% turn-off occurring in about 150Å, which may be attributed to the resolution of the SIMS measurement technique. Figure 1b shows the O profile in a SiGe film containing 33% Ge and deposited at 550°C. The film has a thick Si cap to obtain good SIMS sensitivity to O. The low level of O in the bulk of the layer is clearly observed. The out-diffusion of O from the substrate into the epitaxial layer is also observed and is indicative of the low level of O in the epitaxial layer. The absence of an impurity peak at the interface between the epitaxial layer and the substrate, indicates the effectiveness of the pre-clean and the general cleanliness of the system.

An XTEM of a 27 nm thick SiGe film containing 44% Ge and deposited at a temperature of 550°C is shown in Fig. 2. While strain related to a dislocation can be noted in the XTEM image, no stacking faults or twins, originating from the Si/SiGe interface, were observed for any of the SiGe layers grown in this study. A significant feature of the SiGe deposited by this technique is the abruptness of both the Si/SiGe interface and the top surface of the SiGe (<10Å). This is noteworthy in light of the observed surface roughening for growth from other techniques. In MBE growth, the onset of three dimensional growth has been attributed to the difference in surface free energy of the Si with respect to the SiGe and the strain in the structure [7]. It has recently been shown that a surfactant can suppress this tendency [8]. In the present growth system we speculate that the Cl present on the surface during growth may similarly suppress islanding. Alternatively, the possibility of a simultaneous etching reaction in a Cl-based growth system may lead to the removal of more weakly bound nuclei that might otherwise result in three dimensional growth.

Excellent selectivity of SiGe deposition is achieved without the addition of HCl gas. The selectivity of SiGe growth is superior to that of Si deposited from dichlorosilane in the same temperature range. Another significant result of the selective SiGe grown by this technique is the lack of faceting of the epitaxial layer at the <110> oriented oxide sidewall. Faceting has been observed for the deposition of selective silicon at higher temperatures [9,10] and limits the usefulness

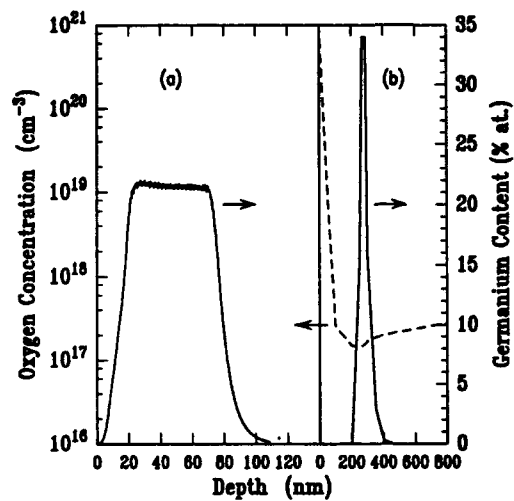


Figure 1: SIMS profiles for Ge and O from SiGe films with a Si capping layers grown at; a) 625°C, Ge profile only, b) 550°C, Ge and O profile.



Figure 2: Cross Section TEM image of a 27 nm thick SiGe film grown at 550°C and containing 44% Ge as determined by RBS.

of selective deposition in some applications. In the present work nodules of de-fected material formed where the oxide sidewall orientation passes through the $\langle 110 \rangle$ directions, similar to those observed for the selective growth of Si in this temperature range [11]. XTEM analysis of selective SiGe depositions confirms that while occasional defects originate from the oxide sidewall, no faceting is observed for growth adjacent to both $\langle 100 \rangle$ and $\langle 110 \rangle$ oriented sidewalls and for deposition in the field or in the well of such patterns, in marked contrast to other work [10].

A (400) HRXRD rocking curve, taken using Cu $K\alpha$ radiation, of a 26 nm thick SiGe layer containing 44% Ge and grown at 550°C is shown in Fig. 3 curve a). The layer thickness was determined independently by x-ray reflection measurements [12], while the Ge content was confirmed by RBS analysis. The observation of Pendullosung is indicative of high crystalline quality and smoothness of the growth front. An x-ray rocking curve simulation based upon the dynamical theory of x-ray diffraction [13] is plotted in curve b) for comparison. The simulated curve is for a 27 nm thick SiGe film containing 43.8% Ge. The simulation matches the observed substrate/epitaxial layer peak height ratio, peak breadth and peak intensity and position, and agrees with the independent determination of layer thickness and composition within experimental error. Additional simulations show that the Ge content of the film is constant to better than 1.0 atomic percent and exhibits a transition width of less than 30Å, in agreement with the XTEM observations.

Asymmetrical (440) reflections from this layer were also studied. The in-plane lattice constant of the SiGe film was determined to be the same as the substrate, to within 2×10^{-5} Å. This indicates that the film is pseudomorphic to within 0.1%, or a strain relaxation corresponding to less than 1×10^5 misfit dislocations/cm². The 26 nm film analyzed in Fig. 3 is metastable since the equilibrium critical layer thickness for a film containing 44% Ge is near 40Å [14].

Si/Si_{1-x}Ge_x ($0 \leq x \leq 0.3$) p-channel modulation-doped structures have been grown by AP-CVD at low temperatures. Temperature dependent Hall measurements show mobility enhancement with no carrier freeze-out at low temperatures clearly indicating the presence of a 2DHG in these structures. See table I. A sheet carrier concentration of 8×10^{12} /cm² and a mobility of 950 cm²/V-s at 12K was obtained using a 400Å Si_{0.8}Ge_{0.2} channel. By comparison, a degenerately p-doped Si layer has a temperature-independent mobility of around 50 cm²/V-s. The high sheet carrier concentrations obtained in this study suggest that structure optimization to yield higher mobilities is possible.

CONCLUSIONS

Rigorous exclusion of H₂O and O₂ from the growth ambient has enabled the growth of SiGe alloys at temperatures as low as 550°C by Atmospheric Pressure Chemical Vapor Deposition (AP-CVD) in a relatively simple reactor for which a commercial variant is available [15]. The films are pseudomorphic, exhibit ex-

Table I: AP-CVD Temperature dependent Hall effect measurements

Structure	%Ge	T(K)	N (cm ⁻²)	μ (cm ² /V-sec)
Double 2DIIIG	20	296	3.0E13	91
100 Å Spacer		77	9.6E12	258
400 Å SiGe		12	8.0E12	950

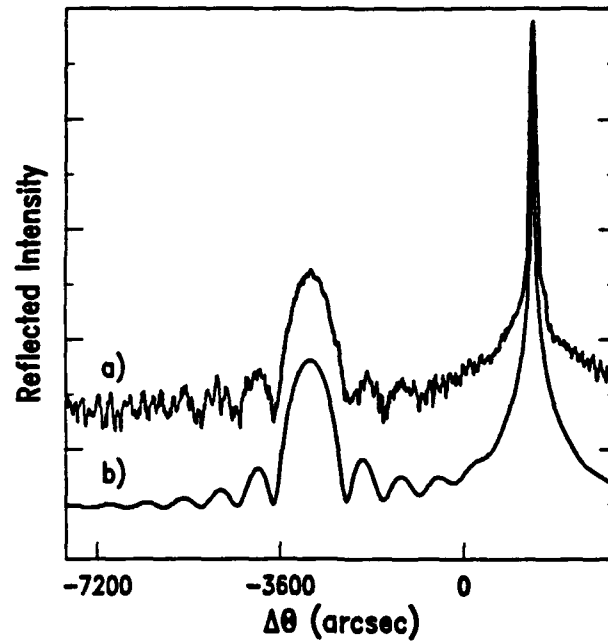


Figure 3: a) (400) x-ray rocking curve data from a SiGe film grown at 550°C. b) simulated curve assuming a SiGe film of 26 nm thickness and 43.8% Ge composition.

cellent crystal quality and contain extremely low levels of oxygen. Films containing as much as 44% Ge remained smooth as observed by high resolution TEM. The data presented in this letter demonstrate the excellent compositional control and the ability to abruptly change the Ge content of films grown by this technique, without the need for thermal switching. Metastable films, exceeding the equilibrium critical layer thickness, may be grown by this technique if low temperatures are employed. Selective growth has also been demonstrated and is facet free. AP-CVD shows great promise for realizing SiGe device structures with commercially available production epitaxy tools.

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ELECTRICAL AND OPTICAL PROPERTIES OF Si AND Si_{1-x}Ge_x ALLOY GROWN BY
THE ULTRA-HIGH VACUUM VAPOUR PHASE EPITAXY METHOD

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ABSTRACT

Epitaxial growth and p-type doping in Si and Si_{1-x}Ge_x alloy by the ultra-high vacuum vapour phase epitaxy (UHV-VPE) method using SiH₄/GeH₄/B₂H₆/H₂ mixture is reported. Growth temperatures as low as 610°C were studied for Ge contents between x=0 to 0.25. Secondary Ion Mass Spectroscopy (SIMS) data of boron dopant profiles in Si and Si_{1-x}Ge_x structures are presented. Strong luminescence attributed to the strained Si_{1-x}Ge_x alloy is obtained. The bandgap in the alloy layer obtained from our luminescence data is compared with published data. Unambiguous electroluminescence from a Si_{1-x}Ge_x multiple quantum well p-n structure grown by UHV-VPE, supported by the photoluminescence and photoconductivity measurement, is reported for the first time.

INTRODUCTION

Due to the potential application of strained SiGe alloy in both high speed heterojunction bipolar circuits and opto-electronics, considerable effort has been given to the study of the growth of this alloy on Si. Initial work had concentrated on the technique of Molecular Beam Epitaxy (MBE) which offers, in principle, the advantage of very low temperature growth and precise control over the layer thickness and composition. However, it is becoming increasingly evident that other growth techniques such as Low Pressure Chemical Vapour Deposition (LP-CVD), UHV-VPE[1], plasma-assisted CVD[2] and limited reaction CVD[3] are showing considerable promise and have produced material of equivalent, if not superior quality. These alternative growth techniques are also more amenable to scaling up for production. We have studied the epitaxial growth of and p-type doping in Si and SiGe alloy by the UHV-VPE technique at temperatures as low as 610°C. Single and multiple quantum well heterostructures were grown to assess their electrical and optical properties.

EXPERIMENTAL

The growth reactor consists of a stainless chamber bakeable to UHV and is primarily pumped by diffusion pumps with liquid nitrogen cold traps[4]. Recent alteration to the system included the use of turbo-molecular pumping in addition to the original Roots/rotary pumping during growth to minimise contamination and to offer the potential for growth studies at very low pressures. In-situ optical diagnostics were available to monitor the growth[5].

Both p- and n-type 4" diameter Si (100) wafers were used. The as-received wafers were given 1 minute exposure under UV-ozone prior to loading into the system. The native oxide was removed by heat-treating to 900-920°C for 8 minutes in 1.0 Torr H₂ ambient to suppress residual B contamination[6]. A SiH₄/GeH₄/H₂ mixture was used as the main source gas and the dopant gas was 1000ppm B₂H₆ in H₂. The gas flow of each gas was monitored by a mass flow controller. Each gas was injected into either the growth reactor or the exhaust via pneumatically controlled valves. Typically, the total pressure

during growth was maintained at 0.1 Torr.

Deep Level Transient Spectroscopy (DLTS) measurements were made using a Bio-Rad DL4600 instrument. Electrochemical CV profiling and SIMS were used to determine the carrier and impurity concentrations. Photoluminescence (PL) and electroluminescence (EL) measurements were carried out in an Oxford Instruments variable temperature cryostat and detected using a 0.75m monochromator and cooled Ge photodiode. In the PL measurement, an Ar ion laser with 514 nm line was used for excitation. Photoconductivity (PC) response was measured by exciting the diode under zero bias with near infrared radiation from a tungsten filament lamp dispersed through a band-pass filter and a 0.22m double monochromator.

P-TYPE DOPING IN Si AND $\text{Si}_{1-x}\text{Ge}_x$

Boron incorporation in Si and SiGe has been studied by growing a series of layers with dopant staircase or spike structures for growth temperatures ranging from 610 - 850°C. Fig.1 shows the SIMS profile of a boron dopant spike structure in Si grown at 610°C. Fig.2 shows the B incorporation in Si layers vs the injection ratio, $[\text{B}]/[\text{Si}]$ in the gas phase. It can be seen that the boron incorporation is controlled solely by the gas phase composition over the entire range of growth temperatures studied. B doping level of $3 \times 10^{19} \text{ cm}^{-3}$ could be achieved without reduction in the growth rate. The boron concentration transition on the leading edges of the dopant spikes were measured by SIMS to be about 90Å/decade. A similar SIMS transition gradient was obtained in Si-MBE grown samples using the same SIMS instrument. We believe our measurement is limited by the SIMS artifact.

Fig.3 shows the SIMS profile of a nominal 500Å Si/500Å $\text{Si}_{0.8}\text{Ge}_{0.2}$ heterostructure grown at 610°C with the SiH_4 , H_2 and 0.1% $\text{B}_2\text{H}_6/\text{H}_2$ flow rates kept constant at 20, 400 and 1.3 sccm respectively during growth. For the alloy layer, the GeH_4 flow rate was set at 1.5 sccm. It can be seen that the B incorporation remained unchanged across the heterojunction even though there was a reduction in the growth rates from $\text{Si}_{0.8}\text{Ge}_{0.2}$ to Si by a factor of 2[7]. This may be explained by the fact that the reaction probabilities for the hydrides are determined only by the H coverage of the surface.

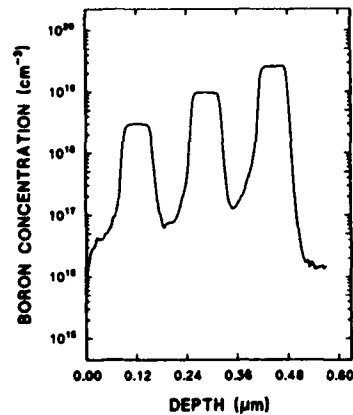


Fig.1 SIMS profile of a boron dopant spike structure in Si grown at 610°C. The SiH_4 flow was kept at 20 sccm whilst the $\text{B}_2\text{H}_6/\text{H}_2$ flow was set to 0.33, 1.0 and 3 sccm at the spikes respectively.

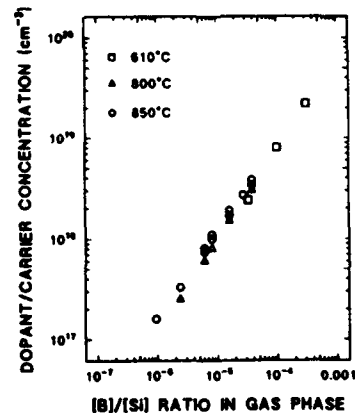


Fig.2 B incorporation efficiency plot for Si layers grown by UHV-VPE using $\text{B}_2\text{H}_6/\text{SiH}_4/\text{H}_2$ gas mixture. Total pressure during growth was typically 0.1 Torr.

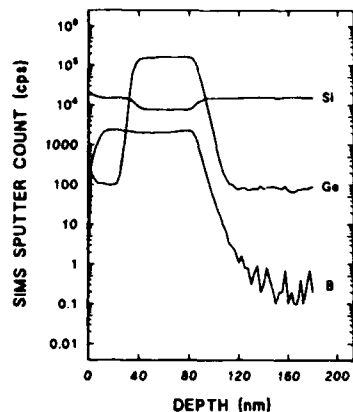


Fig.3 SIMS profile of a nominal 500Å Si/500Å $\text{Si}_{0.9}\text{Ge}_{0.1}$ heterostructure showing a constant boron concentration across the hetero-junction interface. Note that the growth rate in Si was almost reduced by a factor of 2 compared to $\text{Si}_{0.9}\text{Ge}_{0.2}$.

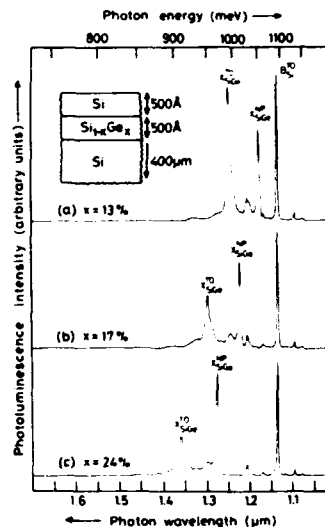


Fig.4 PL spectra of single $\text{Si}_{1-x}\text{Ge}_x$ quantum well heterostructures with different Ge fraction, x , measured at 4.2K.

OPTICAL PROPERTIES OF UHV-VPE $\text{Si}_{1-x}\text{Ge}_x$

Undoped single SiGe quantum well heterostructures with nominal well width of 500Å were grown on p-type Si substrates (1 ohm cm, B-doped) for PL studies. Fig.4 shows the PL spectra of three samples grown at 610°C with different Ge fraction, x , in the alloy. The Ge fractions were determined by X-ray diffraction and Rutherford back scattering[8]. No dislocation related luminescence was observed. Strong luminescence lines which shift towards lower energy with increase in the Ge content of the alloy are observed and are attributed to the excitonic recombination within the alloy layer itself. Our luminescence spectra are similar to those previously reported by Terashima *et al.*[9] and Sturm *et al.*[10]. The assignment of the $\text{Si}_{1-x}\text{Ge}_x$ related luminescence peaks, X^{NP} and X^{PO} , follow the work of Weber and Alonso[11]. The no-phonon (NP) peak energies, representing near bandgap recombination, are in good agreement with the bandgaps measured by Lang *et al.*[12] using absorption spectroscopy.

ELECTRICAL PROPERTIES OF UHV-VPE $\text{Si}_{1-x}\text{Ge}_x$

DLTS Measurement

SiGe alloy layers were accessed for electrically active deep centres using the DLTS technique on a p-n multiple quantum well (MQW) structure as shown in Fig.5. The alloy, Si spacer, and Si buffer layers were not intentionally doped. Background doping in our layers was typically n-type with a measured carrier concentration of $\sim 10^{15} \text{ cm}^{-3}$. Aluminium contacts were used for the top p-Si layer and n-Si substrate. In the measurement, the depleted region of the diode was first flooded with carriers by forward pulsing at +1V for 2 msec before detrapping under a reverse bias of -2V. The DLTS spectrum was taken over the temperature range of 100-350K. No identifiable trap was detected down to the detection limit of 10^{12} cm^{-3} .

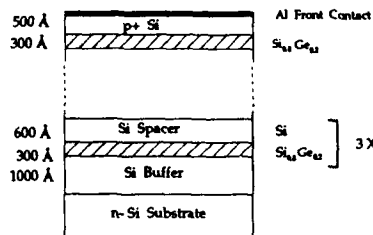


Fig.5 Schematic diagram of a p-n multiple $\text{Si}_{0.8}\text{Ge}_{0.2}$ quantum well structure used for the DLTS, electroluminescence and photoconductivity measurements. The p-Si cap was doped with B at $1 \times 10^{19} \text{ cm}^{-3}$. Contacts were made by Al evaporation.

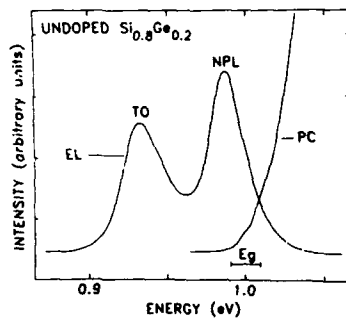


Fig.6 The EL spectrum and PC threshold response of a pn $\text{Si}_{0.8}\text{Ge}_{0.2}$ MQW diode measured at 77K. The current density used for EL was 22mA with diode area of $1 \times 2 \text{ mm}$. The PC threshold was measured at zero bias.

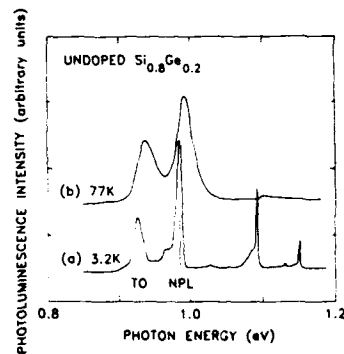


Fig.7 The PL spectra of the same SiGe MQW structure measured at 3.2 and 77K showing the corresponding NPL and TO peaks seen in the EL spectrum of Fig.6.

Electroluminescence and Photoconductivity Measurement

The same SiGe MQW structure was also used for electroluminescence and photoconductivity studies. The front Al contact of the mesa diode structure has been partially removed to allow the radiation to pass through the top surface. Fig.6 shows the EL spectrum and PC threshold response of the diode at 77K. Fig.7 shows the PL spectra of the same SiGe MQW structure obtained at 3.2 and 77K. We can clearly see that (a) the two EL peaks correspond to the NPL and TO peaks in the PL spectra, and (b) that the PC threshold occurred at the same energy position as the NPL EL peak suggesting that the NPL peak arises from near-bandgap exciton recombination in the alloy. The EL peaks remained detectable up to 220K.

The $\text{Si}_{1-x}\text{Ge}_x$ related electroluminescence reported by Rowell *et al.*[13] shows a very broad band (FWHM $\approx 75 \text{ meV}$) which is in sharp contrast to the double narrow peaks seen in our EL spectra. Furthermore, whereas the peak energy of their luminescence lies at about 120 meV below the published alloy bandgap energy, the NPL peak in our EL spectrum lies at the energy level as expected.

CONCLUSION

We have shown that good control of boron doping in Si and SiGe alloy layers can be achieved in UHV-VPE. The DLTS measurement showed that our layers have very low electrically active deep trap densities. The optical properties of the layers are indicated by the strong luminescence to be good. The observation of intense electroluminescence from the SiGe alloy layer supports this assessment.

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SELECTIVE GROWTH OF HETEROEPITAXIAL $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ LATERAL WELLS USING PULSED LASER INDUCED EPITAXY

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ABSTRACT

Patterned $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ wells are fabricated for the first time by pulsed laser induced epitaxy technique, employing two different semiconductor processing steps to grow these structures *selectively*. Two different dimensions of $\text{Ge}_{0.12}\text{Si}_{0.88}/\text{Si}$ wells are successfully formed, in which one is 3.5 μm wide and 1700Å deep while another is 6 μm wide and 1300Å deep. Transmission electron microscopy combined with energy-dispersive X-ray imaging reveals that the 2-D Ge redistribution profiles are well defined and no significant line or surface defects observed. The 2-D Ge well redistribution behavior, governed by heat and mass transport during laser processing, are also discussed.

INTRODUCTION

Strained $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heteroepitaxial layers provide a highly attractive, narrow bandgap material system for use, due to its valence band discontinuity, isoelectronic behavior and compatibility with Si integrated circuit processing technology, in the fabrication of high performance Si-based heterojunction bipolar transistors and circuits. Current efforts in the materials growth area toward making these layers are mainly based on either molecular beam epitaxy or chemical vapor deposition [1,2]. The selective nature of these growth techniques, however, is exploratory at best, with either redesign of device structures or improved growth techniques being pursued [3].

Recent reports have noted the fabrication of heteroepitaxial $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ large area single crystal layers using a pulsed XeCl excimer laser to melt through the deposited film and part of the substrate [4]. By combining this process with integrated circuit fabrication techniques and *in-situ* gas immersion laser doping [5], a pulsed laser induced epitaxy (PLIE) technique can be applied to selective processing on a die-by-die fashion, for example, in hybrid SiGe bipolar complementary metal-oxide-semiconductor (BiCMOS) circuits. Therefore, development of selective PLIE combined with *in-situ* doping is important for a host of possible applications for making very-shallow junction devices using selective heteroepitaxial layers. This could potentially allow for direct integration of a selective heteroepitaxial process into conventional semiconductor manufacturing technology.

In this report we demonstrate the integration of PLIE with conventional device processing for fabrication of patterned $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structures. In making these layers, we implement two different semiconductor patterning techniques in order to demonstrate the feasibility of developing the selective nature of this technology. The $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ well width is defined primarily by photolithography processing, while the layer depth is controlled by the deposited film thickness and laser parameters. Transmission electron microscopy (TEM) imaging and energy-dispersive X-ray (EDX) mapping are used to investigate the 2-D Ge profiles and to detect the existence of any significant line or surface defects in the layers. Successful demonstration of this process will allow fabrication of selectively isolated, thin base $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterojunction bipolar transistors and other structures such as electron or light waveguides by choosing the appropriate material systems.

EXPERIMENTAL

This study employs two different patterning techniques, Al/SiO₂-masking layers (Fig. 1) and liftoff (Fig. 2). For the patterned Al/SiO₂-mask processing sequences, shown in Fig. 1,

a 3-inch (100) *n*-type (0.1–0.9 Ω -cm) Si wafer is thermally oxidized to form a 500-nm SiO₂ layer. Then, a 1- μ m layer of pure Al is deposited, to serve as a highly reflective mask for the 308 nm XeCl laser. Following a standard photolithographic process, Al and SiO₂ are patterned to open the well region for the Ge_xSi_{1-x} layer growth. After removal of the photoresist, the wafer is loaded into an *e*-beam evaporator. Following the deposition of ~13 nm of amorphous Ge, the wafer is transferred to the pulsed laser system. For the liftoff process, a *p*-type (5X10¹⁴ cm⁻³) Si (100) wafer is used with the substrate axis 4° off toward the [110]. Following wafer cleaning, a 0.5 μ m thick photoresist is spun onto the substrate and then baked at 90°C for 20 min. Patterns of lines with various linewidths are photo-lithographically exposed in the resist. Just before loading into the *e*-beam evaporator, the wafer is dipped in BOE (6:1) for 10 sec and then rinsed in DI water for 30 sec. Then, a ~15 nm thick Ge film is evaporated onto the patterned substrate. Before loading into the laser system, the liftoff process is performed in acetone. In this experiment, only argon gas was used in the cell and no *in-situ* doping was incorporated.

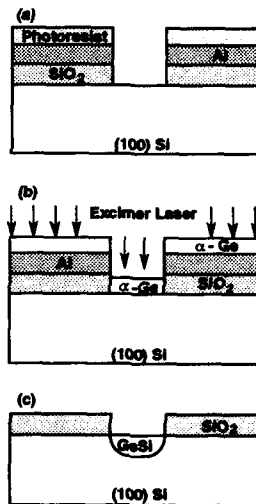
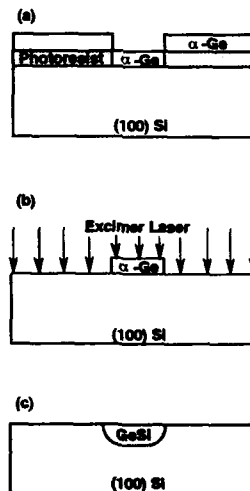
Fig. 1 Al/SiO₂ - mask Process

Fig. 2 Liftoff Process



Figs. 1 and 2 Schematic illustration of the processing steps for the Al/SiO₂-masking and liftoff patterning processes. For exact details see the discussion in the text. The dimensions shown here are not to scale.

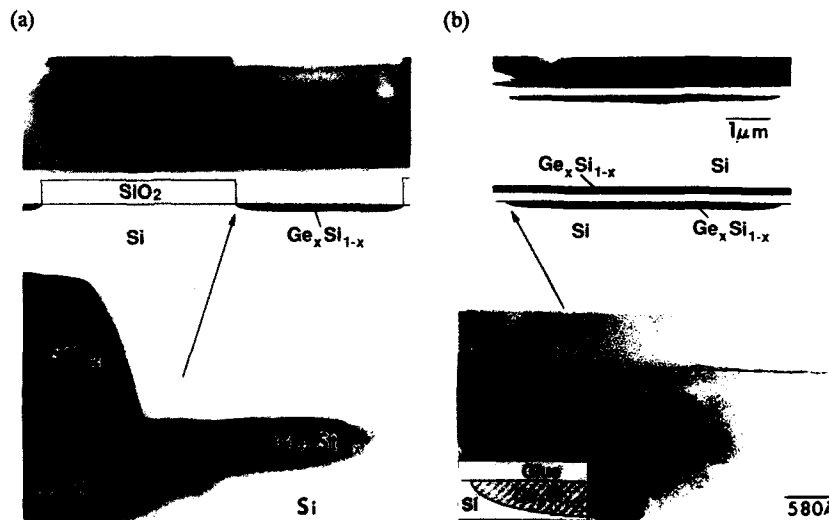
Two different lithography masks are used for this study. Each mask is essentially an array of open lines and oxide spacers which offer enough area for TEM sample preparation and investigation. The Al/SiO₂-mask consists of an array of closely spaced lines 1500 μ m long with 3 μ m openings and 5 μ m spacers [6]. For the liftoff array, the line widths and oxide spacers range from 2 μ m to 50 μ m with all lengths being 3 cm.

TEM is used to determine the Ge_xSi_{1-x} well configuration resulting from PLIE processing. The Ge and Si mass contrast, although low, is visible in the bright-field images if other contrast mechanisms, such as diffraction contrast due to thickness variations, are minimized. The Ge profile is also investigated *in-situ* in the TEM by EDX mapping. This is carried out in the scanning TEM mode by focusing the electron beam down to about 5 nm in diameter and scanning across the well. This mapping method is used to overcome the problem when the edge of the Ge_xSi_{1-x}/Si is difficult to define in the TEM image. The Ge concentrations in the Ge_xSi_{1-x}/Si wells are also determined by the EDX analysis. Features near the Ge_xSi_{1-x}/Si interface are examined in detail by lattice imaging to determine if any

defects exist. For the Al/SiO₂-mask process, regions available on the mask enable subsequent characterization of the layers using RBS. This allows exact determination of the Ge_xSi_{1-x}/Si layer depth and Ge composition which compare well with the TEM/EDX measurements.

RESULTS AND DISCUSSION

In Figure 3(a) we show Ge_{0.12}Si_{0.88} wells fabricated using the Al/SiO₂-mask process, while Fig. 3(b) presents the results using the liftoff process. The photos are arranged to allow easy comparison of the profile difference resulting from the two different processes. Fig. 3(a) clearly shows the 5 μm oxide spacers and 3 μm openings. Also, the 3 μm by 200 nm Ge_{0.12}Si_{0.88} well is clearly defined in the TEM photos from the Ge mass contrast. This is also seen in the higher magnification photo included at the bottom of Fig. 3(a). The laser parameters used for this sample are an energy fluence of 1.0 J/cm² resulting in a 70 nsec melt duration. The Ge redistribution profile starts from the edge of the Si/SiO₂/Ge_xSi_{1-x} corner and extends both vertically and laterally into the open channel. The oxide spacers have a rounded top corner which tapers down to the Si surface. This results in increased absorption of the laser light, causing a hot region at the Si/SiO₂/Ge_xSi_{1-x} corner since the Al will not reflect the incoming laser energy at this tapered edge. For this experiment, we employed only wet etching to remove the Al followed by a plasma etch to open the SiO₂ window. The SiO₂ edge could be improved by using plasma etching to remove both the Al and SiO₂ layers. In Fig. 3(b), a 6-μm wide 150-nm deep Ge_{0.12}Si_{0.88}/Si lateral well fabricated using the liftoff process is shown in the cross-sectional TEM micrograph. In order to investigate the Ge redistribution behavior at the sidewall, we also show the well picture at higher magnification, showing an abrupt Ge_xSi_{1-x}/Si junction. Even at the sidewall region, we can still see the Ge_xSi_{1-x}/Si interface. Furthermore, the very uniform image implies few if any defects in this structure. Fig. 4 shows a typical EDX mapping of the Ge_xSi_{1-x}/Si layers made by the liftoff process. The nearly abrupt Ge wells are clearly seen in the figure. We have also investigated lattice images (not shown here) in this region tracing along the Ge_xSi_{1-x}/Si interface. These structures exhibit no dislocations or stacking faults.



Figs. 3 (a) and (b). Cross-sectional TEM photographs of Ge_{0.12}Si_{0.88}/Si wells: (a) after Al/SiO₂-mask and (b) liftoff processing, respectively. The pictures shown at the bottom are the images viewed at a higher magnification.

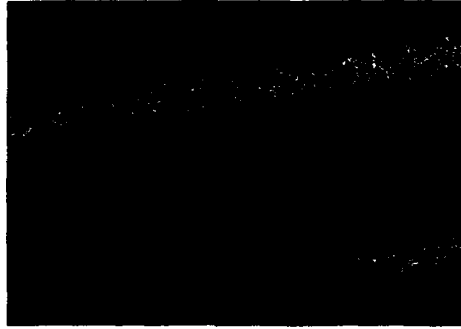


Fig. 4 EDX mapping of the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ layers made by the liftoff process in which white dots represent the signals from the Ge $K\alpha$ window.

In order to study the heat and mass transport behavior for the 2-D problem at hand, the Ge profiles, obtained from Figs. 3(a) and 3(b) for two different processing steps, are curve-fitted, with the results shown in Fig. 5. Since the Ge-Si mass contrast in the TEM bright field images serves as a good marker, these data can be provided as experimental results for verification using 2-D laser processing simulators. In Fig. 5, we are able to fit the curves with a simple logarithm relation rather than a more complicated polynomial fit. Although we do not presently understand the physical meaning of this logarithm relationship, it is particularly useful for providing a quantitative relation between the vertical and lateral melt lengths. The Ge profile for the liftoff process has a better fit to the logarithm relation than that of the Al/SiO₂-mask process, possibly due to the more complicated processes and geometry in the Al/SiO₂-mask process. The characteristic round sidewall shape, however, for both cases is indeed very similar. This nearly process-independent characteristic shape, which has a lateral diffusion length very nearly equal to the vertical transport depth, may eventually set limits on the smallest well width which can be fabricated.

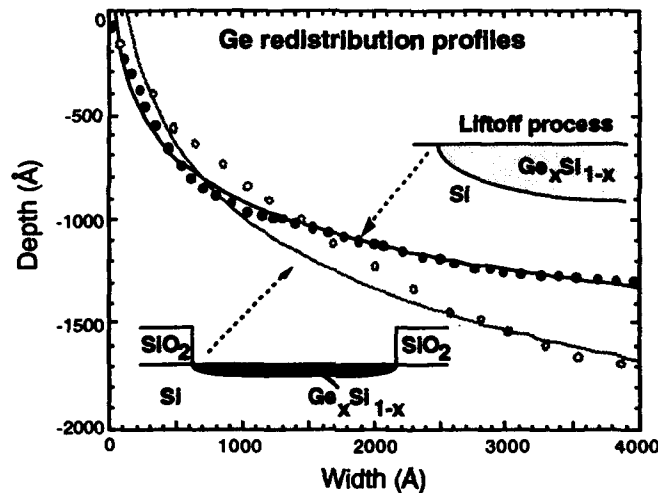


Fig. 5 Ge distribution profiles plotted and curve-fitted using the melt depth vs. lateral diffusion length. The schematic diagrams shown in the graphs are not to scale.

To summarize, we employ two different patterning processes to fabricate $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ lateral wells. The results indicate that laser-induced epitaxy techniques can be integrated into semiconductor processes for selective growth of patterned $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ wells.

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DOPANT ENHANCED LOW-TEMPERATURE EPITAXIAL GROWTH BY
RAPID THERMAL PROCESSING CHEMICAL VAPOR DEPOSITION

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ABSTRACT

We have demonstrated, for the first time, that the epitaxial growth temperature can be lowered by dopant incorporation using rapid thermal processing chemical vapor deposition (RTPCVD). Heavily arsenic-doped epitaxial layers with very abrupt dopant transition profiles and relative uniform carrier distribution have been achieved at 800°C. The defect formation is closely related to dopant concentration; the defect density as a function of carrier concentration shows a sharp transition at about $3 \times 10^{18} \text{ cm}^{-3}$.

INTRODUCTION

There has been significant interest in developing techniques capable of depositing thin Si epitaxial layers with abrupt, well-controlled dopant transition profiles for future ultra-large scale integration (ULSI) and high-speed device applications. Chemical vapor deposition (CVD) is currently the most mature technology for producing high quality Si epitaxial layers and has found widespread use in industry due to its enormous advantages over the other techniques in terms of film quality and throughput. However, obtaining a narrow dopant transition profile is also difficult by conventional CVD epitaxial techniques due to dopant autodoping and outdiffusion. Numerous techniques to reduce the amount of thermal exposure to the wafer during the epitaxial growth process through a reduction of process temperature [1-3] and/or process time have been studied in order to overcome some of the limitations of conventional CVD. In addition, Sedgwick *et al.* have lowered temperatures for undoped epitaxial growth down to 600°C at atmospheric pressure by using purified H_2 [4]. Rapid thermal processing CVD (RTPCVD[5], RTCVD[6], or limited reaction processing[7]) has also received considerable attention recently because of its ability to reduce many of the processing problems associated with thermal exposure in conventional CVD. RTPCVD can achieve high crystalline perfection and dopant activation while minimizing degradation of the dopant transition profile.

Studies on solid phase epitaxy (SPE) have revealed that the SPE regrowth rate is enhanced by high concentration electrically active impurities such as B, P, and As, but reduced by other impurities such as O[8]. By SPE, epitaxial regrowth can be achieved at much lower temperatures ($\leq 600^\circ\text{C}$)[8,9]. On the other hand, it has been demonstrated that a mono-Si substrate can act as a seed for epitaxial alignment of poly-Si deposited on Si and that recrystallization of poly-Si can be enhanced by high concentration impurity incorporation such as arsenic through ion implantation[10]. These results suggest that the epitaxial growth temperature may be lowered by high concentration dopant incorporation through *in-situ* doping.

This paper presents a new approach, based on the studies of SPE and poly-Si recrystallization, to lower epitaxial growth temperatures by high concentration dopant incorporation through *in-situ* doping. *In-situ* doped epitaxial growth has technological importance and has been studied extensively for conventional CVD[11]. Results show the addition of B_2H_6 enhances the deposition rate while the addition of AsH_3 and PH_3 reduces the deposition rate. Rai-Choudhury *et al.* reported that heavy doping of As and B caused severe degradation of crystal quality using SiCl_4 as Si source gas[12]. They attributed the observed degradations to particles falling from the reactor walls or generated by homogeneous nucleation when AsH_3 partial pressure was higher than 6.1×10^{-3} atm. Comfort *et al.* reported that the *in-situ* arsenic doping using AsH_3 in a conventional CVD reactor caused significant film quality degradation at 800°C with SiH_4 as Si source gas[13]. Meyerson *et al.* have demonstrated nonequilibrium boron doping effects in low temperature epitaxial growth using UHV/CVD[14]. In these studies, dopant incorporation was not used to lower the epitaxial growth temperature, and, as a result, the effect of dopant incorporation on the epitaxial growth temperature was not

discussed. The purpose of this work is to examine the effects of dopant incorporation and growth temperature on epitaxial film quality.

EXPERIMENTAL PROCEDURE

RTPCVD was carried out in a horizontal cold wall quartz reactor, the details of which have been reported elsewhere[5]. In this study, SiH_2Cl_2 was used as the Si source gas and H_2 was used as the carrier gas. Arsenic doping was obtained by adding dilute arsine (100 ppm AsH_3 in H_2) to the gas flow during the deposition. Compared to other dopants, arsenic can minimize the stress due to the small atomic size difference (0.01Å) and thus reduce the defect formation. The starting materials for epitaxial growth were B-doped (100)Si wafers with resistivities of 14-22 $\Omega\cdot\text{cm}$. They were chemically cleaned, etched in dilute HF, and rinsed in deionized water just prior loading into the chamber. The process gases are introduced to the reactor when the chamber pressure reached 1×10^{-3} Torr. The deposition pressure was 5 Torr. An *in-situ* hydrogen pre-bake was performed prior to deposition[5], followed by doped epitaxial layer growth.

RESULTS AND DISCUSSION

The Nomarski micrograph in Fig.1 of an undoped sample processed at 800°C with 5 vol.% SiH_2Cl_2 in H_2 shows roughness and a considerably grainy surface. The plan-view TEM micrograph reveals the existence of polycrystalline grains, also confirmed by the rings in the TED pattern. Undoped films deposited at 800°C are polycrystalline, possibly due to the surface cleaning and/or gas purity and background impurity level. *In-situ* cleaning of the substrate surface is critical for epitaxial growth. Meyerson has shown the effect of background impurity level on film quality[1]. Recently, Sedgwick *et al.* have also demonstrated the effect of gas purity on film quality[4]. We believe the poor film quality of undoped samples deposited at 800°C is mainly due to the background impurity level and gas purity.

Fig. 2 shows SEM micrographs of the surface morphology of *in-situ* doped epilayers grown at 800°C . The deposition parameters were identical for all three samples with only the AsH_3 flow rate being varied. A significant reduction in defect densities can be observed in each successive micrograph. Fig. 2(a) shows the surface morphology of the sample grown with 1 vol.% AsH_3 and clearly shows surface bump formation, which indicates growth defects. However, the film is not polycrystalline. Fig. 2(b) shows the surface morphology of the sample grown with 5 vol.% AsH_3 . The surface bumps can still be observed, but at a much lower density compared to Fig. 2(a). Fig. 2(c) shows a sample grown with 7.5 vol.% AsH_3 . The surface bumps totally disappear, resulting in a smooth surface and good film quality. The results strongly suggest that dopant incorporation has a significant impact on epitaxial defect densities and that higher dopant concentrations can improve surface morphology.



Fig. 1: Nomarski micrograph of sample surface morphology after 800°C deposition with 5 vol.% SiH_2Cl_2 .



Fig. 2: SEM micrographs of samples grown at 800°C with 5 vol.% SiH_2Cl_2 and with AsH_3 volume concentrations of (a) 1%, (b) 5%, and (c) 7.5%.

In our experimental conditions, the AsH_3 partial pressure was about 10^{-8} atm which was much lower than Rai-Choudhury's case[12]. In addition, SiH_2Cl_2 was used as the Si source gas which also minimized the deposition on the reactor walls and homogeneous nucleation. In Comfort's experiments[13], the base pressure was very low ($\sim 10^{-8}$ Torr) which was the main reason for obtaining good surface morphology when no AsH_3 was introduced. According to Rai-Choudhury's results[12], the addition of AsH_3 to SiCl_4 will enhance the gas phase nucleation or deposition on the reactor walls, or even on the wafers which enhance defect formation in the epilayer. It is suspected that this situation is even worse when SiH_4 is used as the Si source gas, since SiH_4 suffers from gas phase nucleation. Furthermore, no H_2 was used during the deposition, which further enhances homogeneous nucleation[13]. We believe these are the main reasons for the morphology degradation for arsenic doped samples in Comfort's case. In our case, SiH_2Cl_2 and H_2 were used, which can reduce defect formation.

TEM was used to characterize the detailed crystal structures. Fig. 3(a) shows the plan-view TEM micrograph and SAD pattern of the sample in Fig. 2(a). The film quality is monocrystalline with numerous defects such as stacking faults and twins. Some polycrystalline precipitates can be observed in the film. A dramatic change of film quality is observed when AsH_3 flow rate is increased. In Fig. 3(b), where the plan-view TEM micrograph and SAD pattern of the sample in Fig. 2(c), the film quality is perfect monocrystalline with no defects. SAD pattern also show an excellent monocrystalline structure. Since both samples were grown at the same temperature, the results suggest that dopant incorporation can directly enhance epitaxial growth.

Fig. 4 shows dopant concentration profiles and oxygen concentration profiles for samples grown at 800°C with 5 vol.% SiH_2Cl_2 and different AsH_3 flows. Very smooth doping profiles can be observed in the epilayers. The oxygen concentration in the epilayers is level with the substrate background concentration. Small oxygen peaks can be observed at the interface. The dopant concentration increased as AsH_3 flow increased. The dopant concentration drops from 10^{18} cm^{-3} to 10^{16} cm^{-3} in less than 500 Å for all samples. The very abrupt transition profiles indicate the indiffusion effect is significantly reduced.

Recently, continuous growth of n^+/p^+ and n^+/p^- structures using photoepitaxy has been studied by Yamazaki *et al.*[15]. In both n^+/p^+ and n^+/p^- structures, the phosphorus concentration in the n^+ photoepitaxial layer was $5 \times 10^{18} \text{ cm}^{-3}$. The surface bumps decreased markedly as boron concentration increased and completely disappeared at boron concentrations above $2 \times 10^{19} \text{ cm}^{-3}$. They studied the origin of the surface bumps and found that the surface bumps were caused by phosphorus precipitation in the initial stages of the n^+ layer growth, which was closely

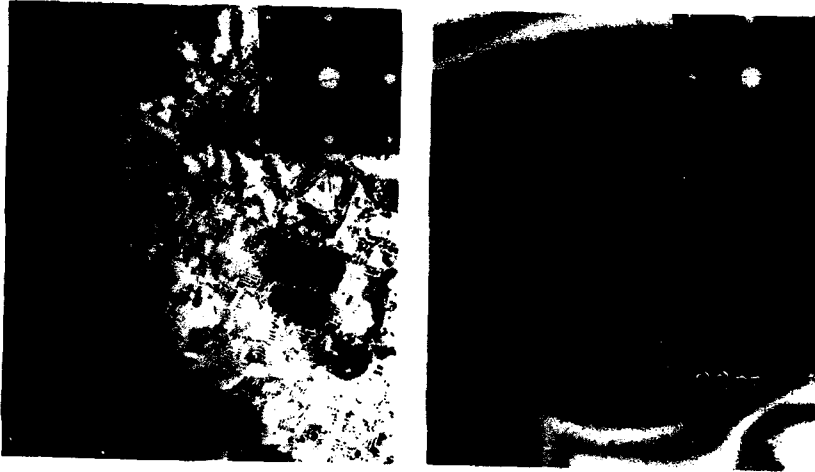


Fig. 3: SAD and plan-view TEM micrographs of epilayers grown at 800°C with 5 vol.% SiH_2Cl_2 and with AsH_3 volume concentrations of (a) 1% and (b) 7.5%.

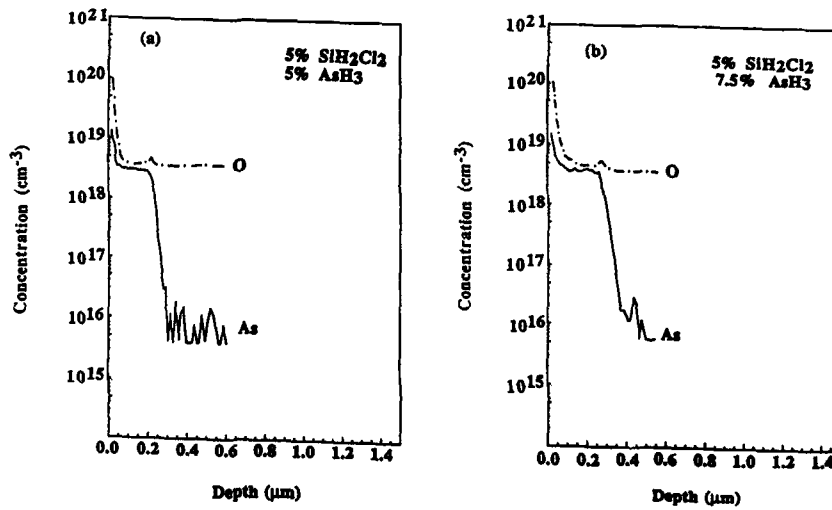


Fig. 4: SIMS profiles for samples grown at 800°C with 5 vol.% SiH_2Cl_2 and with AsH_3 volume concentrations of (a) 5% and (b) 7.5%.

related to the hole density at the surface. The results suggest that the carrier concentration is more important than the chemical dopant concentration in surface defect formation. On the other hand, the results of SPE also strongly suggest that the fractional ionization of impurities is the dominant contributor to the SPE enhancement[9]. Recently, Jeon *et al.* observed SPE enhancement with As concentrations higher than $3 \times 10^{18} \text{ cm}^{-3}$. Their results also show that B produces the greatest overall SPE regrowth rate enhancement when concentrations are higher than $1.1 \times 10^{19} \text{ cm}^{-3}$. Another very important effect observed in SPE studies is the compensation effect. Suni *et al.* have reported that compensated layers with equal concentrations of acceptors and donors showed a strong decrease in the SPE regrowth rate[16]. No compensation was observed in the SPE regrowth of layers with overlapping donor concentrations[16]. The results further suggest that both electron and hole (electrically active impurities) play an important role in the SPE growth kinetics.

Fig. 5 shows carrier concentration profiles for samples grown at 800°C with 5 vol.% SiH_2Cl_2 and different AsH_3 flows. SRP can only measure electrically active dopant concentrations. By comparing to SIMS results, the dopant activation ratio is about 100%, within experimental error. Relatively smooth carrier concentration profiles in the doped layer can be observed for all samples. The carrier concentration increased as AsH_3 flow increased. The carrier concentrations drop from 10^{18} cm^{-3} to 10^{15} cm^{-3} in 300 \AA for all samples. Again, the very abrupt transition profiles indicate the indiffusion effect is significantly reduced. The results are in good agreement with the SIMS data.

Fig. 6 shows the defect density at the n^+ layer surface as a function of the electron concentration at the n^+ layer. The defect density decreased markedly with increasing electron concentration. The transition occurred at the electron concentration $\sim 3 \times 10^{18} \text{ cm}^{-3}$. However, the transition is much sharper compared to Yamazaki's results[15]. The difference can be explained by SPE studies. The SPE process is thermally activated and the impurities present have significant effects on the kinetics. As a result, the carrier concentration for the transition should strongly depend on the impurity present. Our results show good agreement with SPE results. On the other hand, the sharpness of the transition should strongly depend on the temperature. In general, the SPE rate as a function of impurity concentration shows a much steeper slope at high temperatures than at low temperatures[8,9] and, as a result, a small change in concentration can cause a larger SPE rate change at high temperatures compared to low temperatures. Yamazaki's experiments[15] were performed at 650°C while our experiments were performed at 800°C . We believe that the temperature difference is the main reason for the difference in the transition sharpness. The electron concentration in their n^+ layer was $5 \times 10^{18} \text{ cm}^{-3}$, which is very close to our electron concentration. The hole concentration in their p^+ layer was above $1 \times 10^{19} \text{ cm}^{-3}$, which is more than three orders of magnitude higher than our hole concentration. But under proper deposition conditions, we observed no defects, even on n^+/p^+ structures. The difference can be explained as follows. In our case, electrically active arsenic is responsible for the SPE enhancement in the n^+/p^+ structure due to the higher fractional ionization in the low concentration range ($\sim 3 \times 10^{18} \text{ cm}^{-3}$). In their case, electrically active boron, after considering the compensation effect, is responsible for the SPE enhancement in n^+/p^+ and p^+/n^+ structures due to higher fractional ionization in the high concentration range ($\sim 2 \times 10^{19} \text{ cm}^{-3}$). Other minor differences might be due to the energy source and/or process gases.

CONCLUSION

In conclusion, we have demonstrated that the epitaxial growth temperature can be lowered utilizing dopant incorporation. Heavily arsenic-doped epitaxial layers with very abrupt transition profiles ($< 300 \text{ \AA}$) and relatively uniform carrier distributions can be grown at 800°C . The defect formation is closely related to the dopant concentration. The defect density as a function of carrier concentration shows a sharp transition at about $3 \times 10^{18} \text{ cm}^{-3}$. In addition, the results strongly indicate that a basic physical mechanism similar to SPE enhancement still plays an important role in several important solid phase processes such as epitaxial growth.

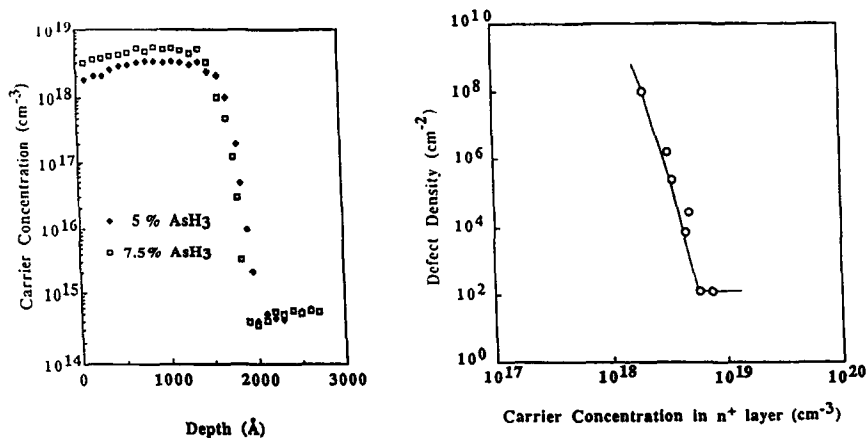


Fig. 5: Spreading resistance profiles for samples grown at 800°C with 5 vol.% SiH₂Cl₂ and different AsH₃ flows. Fig. 6: Defect density at the n⁺ epilayer surface as a function of the carrier concentration at the n⁺ epilayer.

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PART IX

Light From Porous Silicon

LAST DEVELOPMENTS IN LUMINESCENCE OF POROUS SILICON

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ABSTRACT

It is shown that visible photoluminescence and electroluminescence can be obtained from porous silicon layers. Room temperature photoluminescence is readily obtained from as-formed high porosity samples. Light emission at wavelengths as short as 560 nm can be observed after further thinning of the silicon pore walls by dissolution in HF under illumination. Silicon walls can also be thinned by an electrochemical oxidation process, this method allowing to use layers of rather low porosities (65%) which thus gives good mechanical properties to the samples. The thinning of the already very small size crystallites of porous silicon leads to quantum size effects which are at the origin of the light emission far above the band gap of silicon. Photoluminescence decay characteristics suggest that a tunnelling effect could be involved in the recombination mechanism of photogenerated charge carriers. Bright electroluminescence during anodic oxidation of porous silicon has been also evidenced. The influence of the porosity, of the layer thickness and of the anodic current density on the integrated electroluminescence intensity are described in detail.

Introduction

With an indirect energy gap of 1.1 eV, crystalline silicon is not expected to emit light in the visible. However, quantum confinement in crystallites of very small dimensions can increase the energy gap so that recombination can occur in the visible range. This was observed with electroluminescence of silicon precipitates in SiO₂ [1] or photoluminescence of ultrafine silicon particles[2]. More recently, a bright red emission at room temperature was reported for a layer of porous silicon thinned by dissolution in hydrofluoric acid [3].

The aim of this paper is to summarize the present state of our research in this new very promising domain. It will be shown that different methods can be used to obtain porous layers with quantum size silicon crystallites, which lead to improved luminescence characteristics and better control of the sample properties. A first approach consists in using different formation parameters in order to get as-formed porous layers of high porosity which exhibit strong photoluminescence without the need for subsequent chemical dissolution. The second approach is to decrease the silicon pore wall thickness by anodic oxidation of the porous layer and to reach, by

this mean, the quantum size range where silicon photoluminescence can be observed. It will be also shown that bright electroluminescence in the visible range is observed during anodic oxidation of porous films and the main characteristics of this new phenomenon will be described in some detail.

Main features of porous silicon.

Porous silicon is a material which is obtained by electrochemical attack of monocrystalline silicon in concentrated hydrofluoric acid solutions. In certain conditions of electrolysis, a localized anodic dissolution of the semiconductor is observed which leads to the formation of pores within the bulk of the silicon substrate. Any thickness can be obtained and controlled by the amount of charge exchanged during the electrochemical reaction. So-formed porous silicon films present a porosity, defined as the percentage of void volume in the material, which can vary between 20 and 85%, according to the anodization conditions. Pores are very small, with radii ranging from 1 to 100 nm, depending on the type and doping level of the silicon substrate and on the choice of the electrolysis parameters. Consequently, so-called porous silicon corresponds to a range of very different materials with different porous textures, but generally the as-formed porous layers exhibit a sharp pore size distribution and homogeneous porosity as a function of depth [4].

Because most applications of the material are related to the formation of silicon dioxide layers obtained by porous silicon oxidation and thus require initial porosities around 50% [5-6], the material characterizations have mainly concerned porous layers of such medium porosities, and up to now, there is some lack of informations about layers with porosities greater than 60%. The microstructure of 55% porosity layers formed on lightly doped p-type silicon has been previously studied [7], and consists of a nearly random network of small pores, highly interconnected, with diameters below 3 nm and with a very high specific surface of the order of $600 \text{ m}^2/\text{cm}^3$. Higher porosity values can be obtained by choosing properly the HF concentration in the electrolyte, and samples of 60% to 85% porosity are readily formed by decreasing the HF concentration from 35% to 15%. However, the pore size distribution and other characteristics of their microstructure are not known, and can only be assumed to be somewhat similar to that of 55% porosity layers, the difference in porosity likely resulting in thinner silicon walls.

Experimental

Substrates used were (100) oriented, 5 to 10 $\Omega\cdot\text{cm}$ resistivity boron doped silicon. An ohmic back-contact was achieved by aluminum vacuum deposition and subsequent annealing at 450°C. Anodization of silicon was performed in a single-tank Teflon cell, in the dark, at room temperature, with continuous stirring of the solution. Samples were anodized under galvanostatic conditions, using a potentiostat (PAR 273) and a three-electrode setup, potentials being measured versus an Ag/AgCl reference electrode (Orion 9001). The electrolyte used for porous silicon formation was a mixture of seven volumes of an aqueous solution of hydrofluoric acid (HF) and

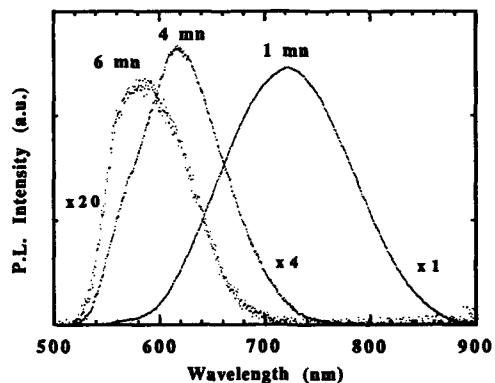


Figure 1 :
Time evolution of the photoluminescence spectra of 85% porosity samples upon dissolution in 15% HF solutions under illumination.

three volumes of absolute ethanol. Samples of different porosities, as determined by gravimetric measurements [7] were obtained by using solutions containing 15 to 35% of HF and current densities in the range 10 to 50 mA/cm². Samples of different thicknesses between 0.2 and 15 μm were obtained by varying the anodization time.

Electrochemical oxidation of porous silicon layers was performed with the same experimental setup using a different electrolytic solution composed of deionized water with 0.1 M KNO₃ or 1 M HCl as the supporting electrolyte. Anodic oxidation of porous films was carried out under galvanostatic conditions, with current densities in the range 0.1 - 50 mA/cm². The samples were carefully rinsed before anodic oxidation, by always keeping some liquid covering the sample in order to prevent native oxide growth upon exposure in air [8].

Luminescence was excited by the UV lines of a Hg arc and detected through a 20 cm monochromator by a GaAs photomultiplier with standard lock-in techniques. Electroluminescence was detected with a silicon photodiode located at 10 mm from the emitting sample.

Results

Photoluminescence characteristics of porous silicon have been so far reported for samples where the porosity was increased by chemical dissolution in aqueous HF solutions for several hours [3]. The slow dissolution rate of silicon in such solutions allows a progressive decrease in the pore wall dimensions, leading to a luminescence signal and to a shift of the luminescence spectra from the near infrared towards the visible wavelengths as porosity increases.

By choosing properly the formation parameters, and particularly the electrolyte concentration, it is possible to obtain as-formed porous layers of about 85% porosity which exhibit strong photoluminescence without the need for subsequent chemical dissolution [9]. The

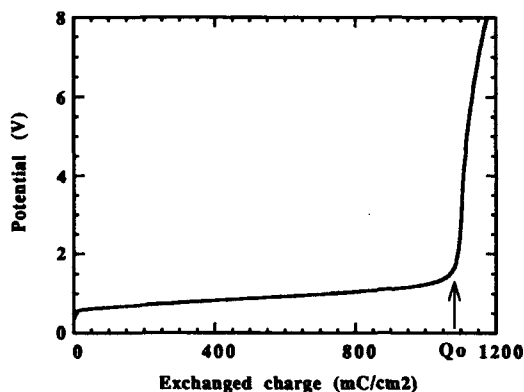


Figure 2 :
Variation of the
anodization potential as
a function of the
exchanged charge during
electrochemical
oxidation of a 75%
porosity layer under
galvanostatic conditions
(current density
 5 mA/cm^2 ,
thickness $4 \mu\text{m}$)

photoluminescence spectrum for the as-formed sample is very similar to that obtained by Canham [3] for porous layers submitted to a 6-hour chemical dissolution in HF concentrated solutions. Further thinning of these samples can also be achieved by chemical dissolution and it was observed that the silicon chemical dissolution was greatly enhanced in presence of light. Under these conditions, much smaller immersion times were required to produce noticeable shifts in the luminescence wavelengths. This behavior is demonstrated on figure 1, which shows the spectra obtained for different samples submitted to increasing dissolution times in HF under illumination. A noticeable blue shift of the whole luminescence spectrum is observed, and it appears that the wavelength of the maximum emission can be as short as 560 nm for a dissolution time of only 6 mn. Such a shift towards visible wavelength has not been observed before and indicates that silicon crystallites of much smaller dimensions can be obtained by starting with materials with higher porosities.

The silicon pore walls thinning down to quantum dimensions can also be achieved by silicon dioxide growth. However, uncomplete oxidation of high porosity layers by thermal treatment in an oxidizing ambient is quite difficult to control. On the contrary, the use of anodic oxidation which is always uncomplete [8] is particularly interesting as it can be quite easily controlled by the electrochemical parameters. The silicon potential during anodic oxidation of a porous layer at constant current density presents characteristic variations shown on figure 2. A slow potential increase is observed during the progressive oxidation of the porous layer, followed by a sharp increase resulting from the break of the electrical contact between the pore walls and the bulk and thus corresponding to the end of the oxidation process. At the current densities used in this work, pore walls are driven into charge carrier accumulation and oxidation proceeds quite homogeneously within the porous layer thickness. However, the total exchanged charge, Q_0 , obtained when the potential abruptly increases, does not correspond to complete oxidation of the porous layer. This is because a continuous oxide layer is formed at the interface by complete

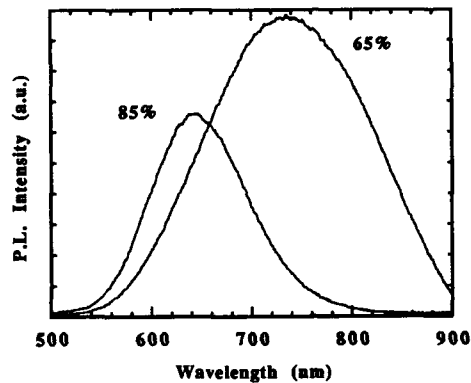


Figure 3 :
Photoluminescence
spectra of two porous
silicon layers of 65%
and 85% initial
porosities,
electrochemically
oxidized at Q_0

oxidation of the narrowest regions of the silicon walls, preventing then further oxidation of thicker regions which become electrically disconnected from the substrate.

Figure 3 shows the spectra of two samples of different initial porosities (65 and 85 %) oxidized up to Q_0 . The 65% porosity sample, which does not exhibit luminescence before anodic oxidation, presents after oxidation at Q_0 a luminescence spectrum which is very similar to that of the non-oxidized 85% porosity sample dissolved one minute in HF under illumination and shown on figure 1. A similar thinning effect is obtained on the other sample, for which the observed spectrum after anodic oxidation is to be compared to the spectrum of a 85% porosity sample which has been submitted during 6 minutes to chemical dissolution in presence of light (figure 1). These results confirm that anodic oxidation is an effective technique to obtain silicon thinning in porous layers, with the advantage that this method also gives good mechanical properties compared to the dissolution technique and provides some chemical passivation of the internal surface of the material leading to more stable luminescence characteristics.

The evolution of the luminescence spectrum of a porous layer has been studied for a given oxidation current density as a function of the exchanged charge below Q_0 . The spectra obtained for a 65% porosity sample oxidized in steps with a current density of 10 mA/cm^2 , show that there is no shift in the emitted light wavelength when oxidation is performed up to Q_0 . In fact, the emission spectrum is not modified upon oxidation, and remains similar to that obtained for as-formed 85% porosity layers. However, a large increase in the light intensity is obtained when the exchanged charge varies from $Q_0/4$ to Q_0 , as shown on figure 4. The variations of the photoluminescence maximum intensity as a function of the exchanged charge presented in figure 4 indicate that there is a threshold effect : no visible light emission can be detected for samples oxidized with an exchanged charge lower than $Q_0/4$. On further oxidation, the signal intensity shows a very sharp increase beyond $Q_0/4$ and is maximum for an exchanged charge of Q_0 . This behavior suggests that the oxidation process increases the number of silicon crystallites of appropriate dimensions which are able to emit visible light : below $Q_0/4$, the silicon walls are still

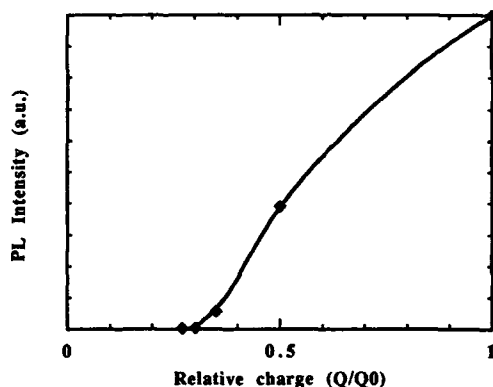
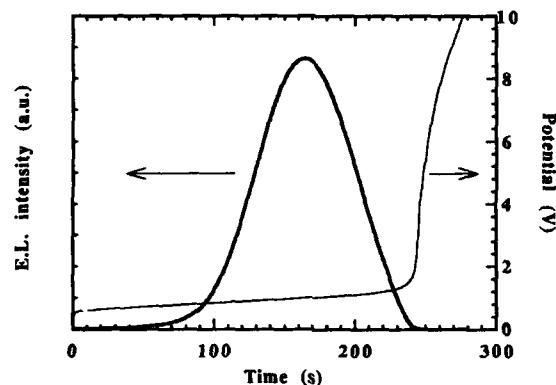


Figure 4 :
Variation of the
photoluminescence
intensity as a function
of the degree of anodic
oxidation Q/Q_0 at
constant current density
($i = 10 \text{ mA/cm}^2$,
porosity 75%)

too thick and no signal is detected. Under these conditions, the recombination is mostly non radiative, and occurs either in the silicon pore walls or in bulk silicon where photogenerated carriers can diffuse. For higher exchanged charge amounts, the critical silicon crystallite dimension to obtain emission is attained, and for further oxidation, the number of emitting crystallites increases sharply. However, no shift in the emitted wavelength is observed. This may indicate that there is no further variation in the silicon crystallite size when they have reached this critical value, possibly because at this stage they become electrically disconnected from the substrate. In this case, the emission spectra should be characteristic of the oxidation current density, which determines the thinning of the silicon walls, and not dependent on the oxidation level. However, further investigation is required in order to confirm these assumptions. Particularly, the determination of the crystallite size, and of their evolution upon anodic oxidation would be of great interest. Transmission Electron Microscopy (TEM) should be an appropriate technique for such investigations. Previously published TEM pictures, dealing with p-porous layers of porosity of about 60% [10] already indicate that crystallite sizes in such materials are far below 10 nanometers. Thus, it seems likely that the actual crystallite sizes in porous samples exhibiting luminescence is of the order of a few nanometers or less.

Far beyond the interest of being an effective thinning method, anodic oxidation also brings evidence that electroluminescence can be obtained from porous silicon layers. Indeed, a bright red-orange light emission is visible over the whole surface of porous layers submitted to anodic oxidation. Figure 5, which shows the potential variations and the integrated electroluminescence intensity as a function of time during anodic oxidation at 5 mA/cm^2 of a 75% porosity sample, allows to compare this visible light emission with the progression of the electrochemical oxidation. It first appears that there is a delay time for the electroluminescence onset. This delay depends on the sample porosity, it is longer for lower porosities, but it disappears for 85% porosity samples, for which light emission starts at the beginning of the anodic process. This delay is related to the



*Figure 5 :
Integrated electroluminescence intensity as a function of time
during anodic oxidation of a 75% porosity sample compared to
the variation of the anodic potential.*

actual sizes of the crystallites in the porous layer ; for lower porosity values, it is necessary to first thin down the pore wall sizes to a quantum range in order to obtain light emission. The electroluminescence intensity then increases sharply with the progression of the oxidation, reaches a maximum and finally decreases to zero, the emission vanishing when the electrochemical oxidation of the porous layer stops. These variations are also joined to a blue shift of the emitted spectra [11]. Consequently, such variations of the electroluminescence intensity during oxidation involve simultaneously several phenomena, including the increase of the number of the emitting crystallite (due to the pore wall thinning by anodic oxidation), the shift of the emitted wavelengths by the crystallites which vary in size, the variations in the emission efficiency with these sizes, and also the decrease of the number of the emitting crystallites as they become electrically disconnected from the substrate when the oxidation charge approaches the Q_0 value.

The electroluminescence intensity variations strongly depend upon the initial porosity of the sample, as shown on figure 6 where it appears that the emitted intensity decreases quite sharply with the porosity. It seems thus that the thinning by anodic oxidation of a porous structure remains largely dependent on the initial porosity of the sample. Figure 6 also shows the clear influence of the initial porosity on the delay before the electroluminescence onset which corresponds to the time necessary to get quantum size crystallites. This time decreases when the porosity is increased, confirming that the starting silicon particle sizes are smaller for higher porosity samples. On the other hand, the time during which emission is observed is longer for smaller porosities, as the quantity of silicon to be anodically oxidized in the layer is greater.

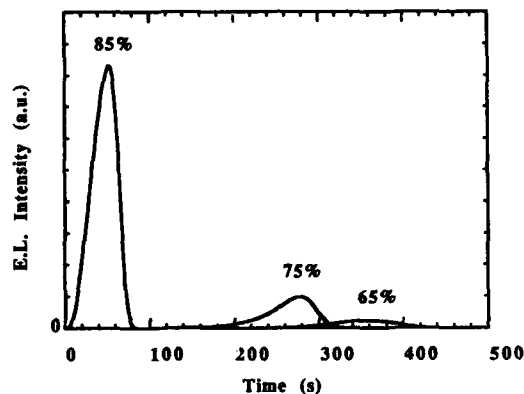


Figure 6 :
 Integrated electroluminescence intensity as a function of the anodic oxidation time for samples of different intensities : 85%, 75%, and 65%.

The electroluminescence intensity is found proportionnal to the thickness of the layer. Figure 7 shows the variations of the integrated emitted light intensity as a function of time during anodic oxidation of several samples of the same porosity (75%) of thicknesses between 0.5 and 10 μm . As the electrochemical oxidation proceeds homogeneously in the whole porous layer, the anodic current value is chosen proportionnal to the thickness of the porous layer in order to keep the local oxidizing current density constant for every sample. The exact proportionality of electroluminescence intensity with thickness proves that the emitting process does occur homogeneously within the sample thickness, and that light absorption by the material remains negligible in the emitted wavelength range.

There is also a strong influence of the oxidation current density on the observed electroluminescence. Figure 8 shows that the time variations of the emitted intensity of 75% porosity samples of the same thickness oxidized at different anodic current densities between 2 and 30 mA/cm^2 . A large influence of the current density on the emitted light intensity is observed. The luminescence duration is found mostly inversely proportionnal to the current density, as it could be expected from the fact that the Q_0 value does not depend upon the current density. However, if the emitted intensity is integrated during the whole anodic process, it is found that this integrated intensity decreases continuously with the anodic current density used (figure 9). This behavior is at present quite difficult to explain, and its interpretation requires that the different phenomena which occur during anodic oxidation should be more thoroughly analysed. There is a need for knowing how the crystallite sizes vary with the initial porosity and upon anodic oxidation, and also how the anodic current density influences these variations. It would be also necessary to obtain more details about the charge exchange mechanisms which are at the origin of this radiative

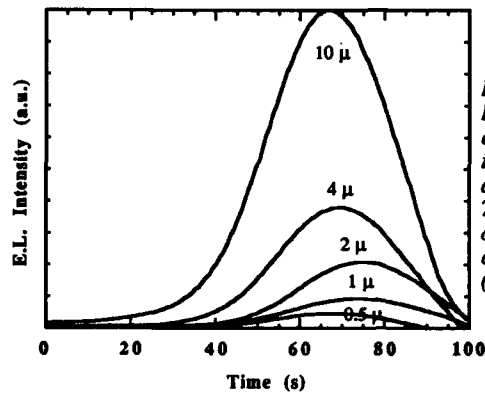


Figure 7.
Integrated
electroluminescence
intensity variation
as a function of time for
75% porosity samples
of different thickness
at constant local density
($I = 2.5 \text{ mA/cm}^2$)

recombination. If it is likely that holes are provided by the anodically polarized substrate, electrons must be injected from the electrolyte or the interface material-electrolyte within the silicon crystallites. The problem is to know what species is responsible for such injection, and also what is the energy of the injected charges and how it varies with the polarization.

Until now, the effect of confinement has been correlated with the energy of emission. Another aspect of this phenomenon is found in the dynamic. Emission decay has been measured following pulse excitation of 5 ns duration obtain with the third harmonic (355 nm) of a Q-switched Nd Yag laser. Measurements were performed on anodically oxidized 5 μm thick 65% porosity samples which present an emission spectrum peaking at 680 nm. The decays which are presented on figure 10 for various detection wavelengths show an extremely important increase of the decay rate with emission energy. As the observed regimes are strongly non exponential, an

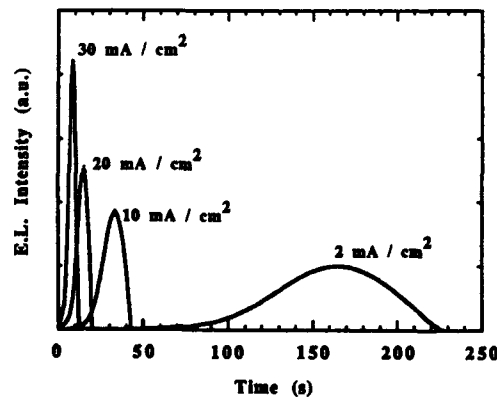


Figure 8 :
Integrated
Electroluminescence
intensity as a function of
time for 75% porosity
samples oxidized at
different current
densities.

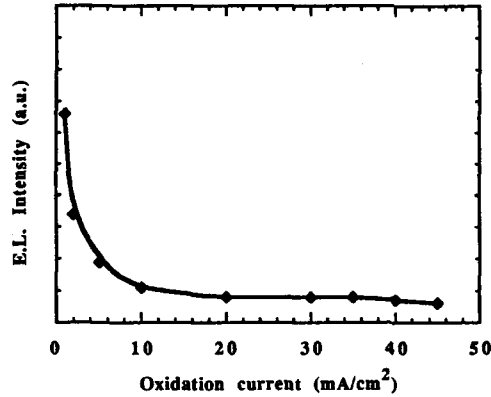


Figure 9.
Time and wavelength
integrated
Electroluminescence
intensity variation of
75% samples oxidized at
different current
densities.

average emission rate can be defined as the ratio :

$$W = \frac{I_{\max}}{\int_0^{\infty} I(t) dt} \quad (1)$$

The variations of W with the emitted energy E is represented on figure 11 which shows the exponential dependence of W with E . Such a dependence suggests a tunnelling effect. It could be that the electron or the hole escape the crystallite where it was photocreated by tunnelling through the barrier at the boundary, and then recombine non radiatively. Tunnelling will then depend exponentially on $k \cdot d$, with $k = \sqrt{E_B - E}$ where d and E_B are the barrier thickness and energy respectively. Assuming an energy barrier of about 3 eV, the measured dependence on E implies a tunneling through a barrier of 1 nm, which appears as a very reasonable order of magnitude for crystallite separation.

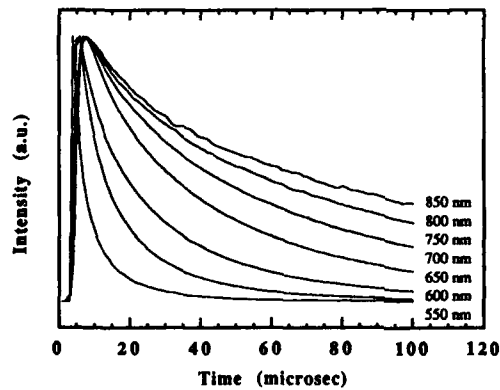


Figure 10.
Decay of the
luminescence detected at
different wavelengths
following pulsed
excitation. Sample is a
65% porous silicon,
anodically oxidized at
20.

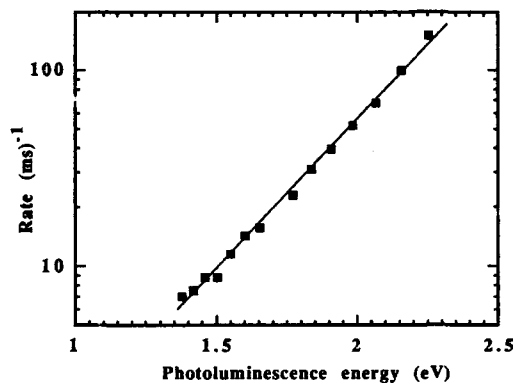


Figure 11.
Dependence of the decay rate with the energy of emission for the sample of figure 10.

Conclusion

This work shows that photoluminescence and electroluminescence can be obtained from porous silicon layers. Room temperature photoluminescence at visible wavelengths may be readily obtained from as-formed high porosity samples; further thinning of the silicon pore walls by dissolution in HF under illumination during a few minutes leads to emitted wavelengths as short as 560 nm. Silicon walls can also be thinned by an electrochemical oxidation process, this method allowing to use layers of rather low porosities (65%) which thus gives good mechanical properties to the samples. The thinning of the already very small size crystallites of porous silicon leads to quantum size effects which are at the origin of the light emission far above the band gap of silicon. Photoluminescence decay characteristics suggest that a tunnelling effect could be involved in the recombination mechanism of photogenerated charge carriers.

Bright electroluminescence during anodic oxidation of porous silicon has been also evidenced. The influence of the porosity, of the layer thickness and of the anodic current density on the integrated electroluminescence intensity have been described. Many aspects of these new promising effects are not clearly explained, and consequently, a large field of investigation is now opened in order to improve our understanding of the physics involved in these electroluminescence phenomena.

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