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MODELING OF RADIATION EFFECTS IN CMOS

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In this report, we present the basic analytical MOSFET model which describes both the below and above-threshold regimes of device operation. The description is based on a change control model which uses one unified expression for the effective differential channel capacitance. The model also accounts for series drain and source resistances, velocity saturation in the channel, finite output conductance in the saturation regime, and for the threshold voltage shift due to drain bias induced lowering of the injection barrier between the source and the channel (DIBL). The model parameters, such as the effective channel mobility, the saturation velocity, the source and drain resistances,etc. are extractable from experimental data. This makes the model very suitable for incirporation into our circuit simulator, AIM-Spice. We apply the characterization procedure based on this model to a MOSFET with a quarter micron gate length and obtain excellent agreement with experimental data. The approach developed in this report was also applied for modeling other field effect transistors, such as GaAs Metal Semiconductor Field Effect Transistors and Heterostructure Field Effect Transistors.

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MODELING OF RADIATION EFFECTS IN CMOS

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FOREWORD

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Modeling of Radiation Effects in CMOS

Technical report.

Table of Contents.

I. Abstract.

The objective of this program was to develop a model fo modeling radiation effects in CMOS. In this report, we describe a new MOSFET model suitable for modeling radiation effects and demonstrate the application of this model to commercial CMOS before and after radiation and after room temperature annealing.

II. Unified MOSFET model.

In this Report, we present the basic analytical MOSFET model which describes both the below and above-threshold regimes of device operation. The description is based on a charge control model which uses one unified expression for the effective differential channel capacitance. The model also accounts for series drain and source resistances, velocity saturation in the channel, finite output conductance in the saturation regime, and for the threshold voltage shift due to drain bias induced lowering of the injection barrier between the source and the channel (DIBL). The model parameters, such as the effective channel mobility, the saturation velocity, the source and drain resistances, etc. are extractable from experimental data. This makes the model very suitable for incorporation into our circuit simulator, AIM-Spice (see Ytterdal et al. (1991)). It is also quite useful for MOSFET design and characterization. We apply the characterization procedure based on this model to a MOSFET with a quarter micron gate length and obtain excellent agreement with experimental data.

The approach developed in this Report was also applied for modeling other field effect transistors, such as GaAs Metal Semiconductor Field Effect Transistors and Heterostructure Field Effect Transistors (see Fjeldly and Shur (1991)).

1. Unified Channel Capacitance

The charge control in the MOSFETs can be described in terms of a unified expression for the channel capacitance, valid for all bias voltages. As was discussed Jeng (1988), the differential gate-channel capacitance per unit area can be written as

$$C_{gc} = \frac{C_a C_b}{C_a + C_b} \tag{1}$$

where

$$c_a = \frac{\varepsilon_i}{d_i + \Delta d} \tag{2}$$

is the contribution from the strong inversion regime,

$$c_b = \frac{qn_o}{\eta V_{th}} \exp\left(\frac{V_{GT}}{\eta V_{th}}\right) \tag{3}$$

is the subthreshold contribution, and

$$n_o = \frac{\varepsilon_i \eta V_{th}}{2q(d_i + \Delta d)} \tag{4}$$

is the sheet density of inversion charge at threshold.

A unified carrier sheet charge density can now be expressed in terms of the effective, unified differential channel capacitance. For an *n*-channel MOSFET at very low drain-source bias (well below saturation), we find

$$qn_s = 2qn_o \ln\left[1 + \frac{1}{2}\exp\left(\frac{V_{GT}}{\eta V_{th}}\right)\right] \tag{5}$$

Since the drain current is assumed to be small, the intrinsic gate voltage swing, V_{GT}, in this expression can be replaced by its extrinsic counterpart, $V_{gt} = V_{GT} + I_d R_S$, where I_d is the drain current and R_S is the source series resistance.

The capacitance model described above can be used for calculating the channel contribution to the gate-source capacitance, C_{gs}, and the gate-drain capacitance, C_{gd}, by using an approximation similar to that used in the model by Meyer (1971):

$$C_{gs} = C_f + \frac{2}{3} C_{gc}\left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}}\right)^2\right] \tag{6}$$

$$C_{gd} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}} \right)^2 \right] \tag{7}$$

Here, $C_{gc} = c_{gc} LW$, $V_{sate} = I_{sat}/g_{ch}$ is the effective extrinsic saturation voltage, I_{sat} is the saturation drain current, g_{ch} is the extrinsic channel conductance at low drain-source bias, and V_{dse} is an effective extrinsic drain-source voltage. V_{dse} is equal to V_{ds} for $V_{ds} < V_{sat}$ and is equal to V_{sate} for $V_{ds} > V_{sate}$. In order to obtain a smooth transition between the two regimes, we interpolate V_{dse} by the following equation:

$$V_{dse} = V_{ds} \left[1 + \left(\frac{V_{ds}}{V_{sate}} \right)^{m_c} \right]^{-1/m_c} \tag{8}$$

where m_c is a constant determining the width of the transition region between the linear and the saturation regime. The capacitance C_f in eqs. (6) to (7) is the side wall and fringing capacitance which can be estimated, in terms of a metal line of the length W, as

$$C_f = \beta_c \, \varepsilon_s W \tag{9}$$

where β_c is on the order of 0.5 (see Gelmont et al. (1991)).

The source-substrate, drain-substrate, and gate-substrate capacitances also affect MOSFET performance in a circuit. Our model (implemented in AIM-Spice) uses standard expressions for these capacitances which can be found, for example, in Shur (1990), p. 393.

2. Current-Voltage Characteristics

At drain-source voltages well below the saturation voltage, the drain current can always (i.e., at both above and below threshold) be expressed as

$$I_{ds} = g_{chi} V_{DS} = g_{ch} V_{ds} \tag{10}$$

where the intrinsic channel conduction in the linear region, g_{chi}, is related to its extrinsic counterpart, g_{ch}, as follows:

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi} R_t} \tag{11}$$

Here, $R_t = R_S + R_d$ is the sum of the source and the drain series resistances. (In deriving eq. (11), we assumed that the drain current is so small that the transconductance is much less less than channel conductance). The intrinsic channel conductance can be written as

$$g_{chi} = \frac{q n_s W \mu_n}{L} \tag{12}$$

where n_S is the unified carrier sheet density at low drain-source voltage given by eq. (5) and μ_n is the low-field carrier mobility. In eq. (10), V_{DS} and V_{ds} are the intrinsic and extrinsic drain-source voltages, respectively, which are related by $V_{ds} = V_{DS} + I_d R_t$. We note that, in the subthreshold regime, the channel resistance will normally be much larger than the parasitic source and drain resistances such that $g_{ch} \approx g_{chi}$, $V_{ds} \approx V_{DS}$ and $V_{gt} \approx V_{GT}$.

The MOSFET drain saturation current for the above-threshold regime was derived for the two-piece velocity saturation model (see, for example, Shur (1990)). This current can be expressed as

$$I_{sat} = \frac{g_{chi} V_{gt}}{1 + g_{chi} R_s + \sqrt{1 + 2 g_{chi} R_s + \left(V_{gt}/V_L\right)^2}} \tag{13}$$

Here, $V_L = F_S L$ where F_S is the saturation field and L is the gate length.

In order to link the linear and the saturation regions by one single expression, we propose to use the following basic interpolation formula for our model:

$$I_{ds} = \frac{g_{ch} V_{ds}}{\left[1 + \left(g_{ch} V_{ds}/I_{sat}\right)^m\right]^{1/m}} \tag{14}$$

where m is a parameter that determines the shape of the characteristics in the knee region.

We should notice that this model can utilize different approximations for I_{sat}. For example, we can use the model proposed by Sodini et al. (1984) and utilized in the popular MOS model BSIM (see Jeng et al. (1987)). Still another alternative is to use the empirical model proposed by Sakurai et al. (1991) ($I_{sat} = BW(V_{gs} - V_T)^n/L$ where B and n are empirical fitting parameters). In this case, one can use the analytical equations for the propagation delays of logic gates by Sakurai et al.

We now want to improve this basic model to account for various non-ideal physical mechanisms such as subthreshold current, drain bias induced barrier lowering (DIBL), and other factors that contribute to a finite output conductance in saturation.

The subthreshold I-V characteristics of the MOSFET in the long channel limit, these characteristics can be expressed as

$$I_d \approx qWD_n \frac{n_s(0) - n_s(L)}{L}$$
$$= \frac{qWD_n n_o}{L} \exp\left(\frac{V_{gt}}{\eta V_{th}}\right)\left[1 - \exp\left(-\frac{V_{ds}}{V_{th}}\right)\right] \qquad (15)$$

where $D_n = \mu_n V_{th}$ is the carrier diffusion coefficient. From eq. (15), we find the following subthreshold saturation current:

$$I_{sat} = \frac{qW\mu_n V_{th} n_o}{L} \exp\left(\frac{V_{gt}}{\eta V_{th}}\right) \qquad (16)$$

(The corresponding saturation voltage is of the order of the thermal voltage, V_{th}.)

A unified expression for the saturation current, valid both above and below threshold, can be obtained by substituting the gate voltage swing V_{gt} in eq. (15) by an equivalent gate voltage swing which coincides with V_{gt} well above threshold and is equal to $2V_{th}$ below threshold:

$$V_{gte} = V_{th}\left[1 + \frac{V_{gt}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{gt}}{2V_{th}} - 1\right)^2}\right] \tag{17}$$

Here, δ determines the width of the transition region. Typically, $\delta = 3$ is a good choice. The unified saturation current

$$I_{sat} = \frac{g_{chi} V_{gte}}{1 + g_{chi} R_s + \sqrt{1 + 2 g_{chi} R_s + \left(V_{gte}/V_L\right)^2}} \tag{18}$$

reverts to eq. (13) above threshold and reduces to eq. (16) below threshold. Hence, using eq. (18) for the saturation current, eq. (14) becomes a unified expression for the *I-V* characteristics with the correct limiting behavior in both the above and below threshold regimes.

An important effect which must be taken into account for an adequate description of the MOSFET behavior is the dependence of the threshold voltage on the drain-source voltage. This dependence can be fairly accurately described by the equation

$$V_T = V_{To} - \sigma V_{ds} \tag{19}$$

where V_{To} is the threshold voltage at zero drain-source voltage and σ is a coefficient which may depend on the gate voltage swing. This translates into the following shift in V_{gt}:

$$V_{gt} = V_{gto} + \sigma V_{ds} \tag{20}$$

where V_{gto} is the gate voltage referred to threshold at zero drain-source bias. The effects of the drain bias induced threshold voltage shift can be accounted for in the *I-V* characteristics of eq. (14)) by using eq. (20) in the expressions for the the saturation current and the linear channel conductance. This will result in a finite output conductance in the saturation region. However, as discussed in by Klassen et al. (1988), σ will depend on the gate voltage swing since the effect of drain bias induced barrier lowering (DIBL) will vanish well above threshold.

Hence, for modeling purposes, we adopted the following empirical expression for σ

$$\sigma = \frac{\sigma_o}{1 + \exp\left(\dfrac{V_{gt} - V_{\sigma t}}{V_\sigma}\right)} \tag{21}$$

which gives $\sigma \rightarrow \sigma_o$ for $V_{gt} < V_{\sigma t}$ and $\sigma \rightarrow 0$ for $V_{gt} > V_{\sigma t}$. The voltage V_σ determines the width of the transition between the two regimes.

For a more accurate description of the saturation region, it is possible to include an additional empirical factor, $(1 + \lambda V_{ds})$, in the expression for the *I-V* characteristics (as usually done in SPICE FET models). The parameter λ is related to physical effects that are not explicitly included in our model, such as, for example, gate length modulation. It is important to emphasize that λ is a strong function of the gate length, the aspect ratio, the contact depth, and other factors. As a rule of thumb, we can assume $\lambda \approx k_o/L$ where k_o is a constant. Hence, our model *I-V* characteristics can finally be expressed as

$$I_d = \frac{g_{ch} V_{ds} \left(1 + \lambda V_{ds}\right)}{\left[1 + \left(V_{ds} / V_{sate}\right)^m\right]^{1/m}} \tag{22}$$

where

$$V_{sate} \approx I_{sat} / g_{ch} \tag{23}$$

is the effective, extrinsic saturation voltage (the same as used in eqs (6) - (8)). When the experimental *I-V* characteristics have a finite output conductance, g_{chs}, in saturation, the saturation current is conveniently defined, for the purpose of comparison with the present model, as the the interReport of the linear asymptotic behavior at small drain-source voltages ($I_d = g_{ch} V_{ds}$) and in deep saturation ($I_d = g_{ch} V_{sate} + g_{chs} V_{ds}$). Hence, we can express V_{sate} in terms of the saturation current as: $V_{sate} = (1 - g_{chs}/g_{ch}) I_{sat}/g_{ch}$. Normally, for well-behaved transistors, $g_{chs} << g_{ch}$ and we can use eq. (23). However, at sufficiently large gate voltage swing, i.e., for $V_{gt} > V_{\sigma t} + 3V_\sigma$, the effects of the drain voltage induced shift in the threshold voltage vanishes and we obtain $g_{chs} \approx \lambda g_{ch} V_{sate}$ in

deep saturation. This can be used to determine λ as part of the device characterization and to obtain the corrected relationship $V_{sate} = (g_{ch}/I_{sat} + \lambda)^{-1}$ to be used in eq. (22) well into strong inversion.

The quality of the present unified MOSFET model is illustrated in Figs. 1 and 2 for a deep submicrometer NMOS. Fig. 1 shows the above-threshold *I-V* characteristics and Fig. 2 shows the subthreshold characteristics in a semilog plot. As can be seen from the figures, our model quite accurately reproduces the experimental data in the entire range of bias voltages, over several decades of the current variation. A residual drain current at large negative gate-source voltages is not accounted for in our model. This current is caused by a small leakage of the reverse biased *p-n* drain-substrate junction. The parameters used in this calculation were obtained using the parameter extraction procedure described below (see Section 3).

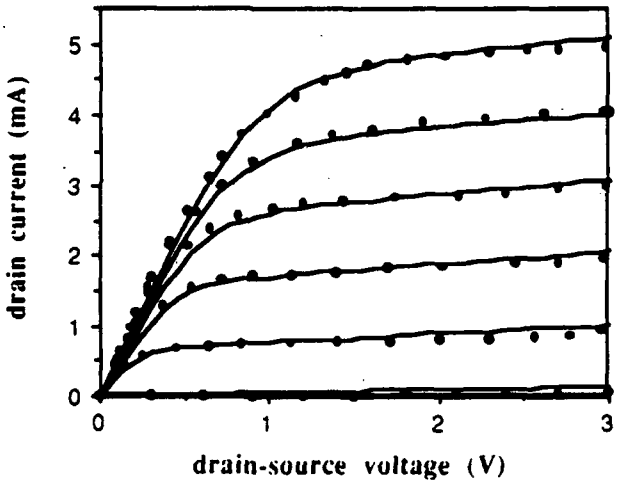

Fig. 1. *Above-threshold experimental (dots) and calculated (solid lines)* I-V *characteristics for a deep submicrometer NMOS with effective gate length* $L = 0.25\ \mu m$. *Device parameters are: effective gate width* $W = 10\ \mu m$, *oxide thickness* $d_i = 5.6\ nm$, *mobility* $\mu_n = 0.028\ m^2/Vs$, *saturation velocity* $v_s = 4x10^4\ m/s$, *saturation knee parameter* $m = 4.0$, *source and drain series resistances* $R_s = R_d = 75\ ohm$, *output conductance parameter* $\lambda = 0.048\ V^{-1}$, *subthreshold ideality factor* $\eta = 1.32$, *threshold voltage at zero drain-source bias* $V_{To} = 0.44\ V$, *threshold voltage parameters* $\sigma_0 = 0.048$, $V_\sigma = 0.2\ V$, $V_{\sigma t} = 1.7\ V$. *Substrate-source bias* $V_{bs} = 0\ V$. *Top curve:* $V_{gs} = 3.0\ V$, *step: -0.5 V. (Data from Chung et.al. (1991).)*

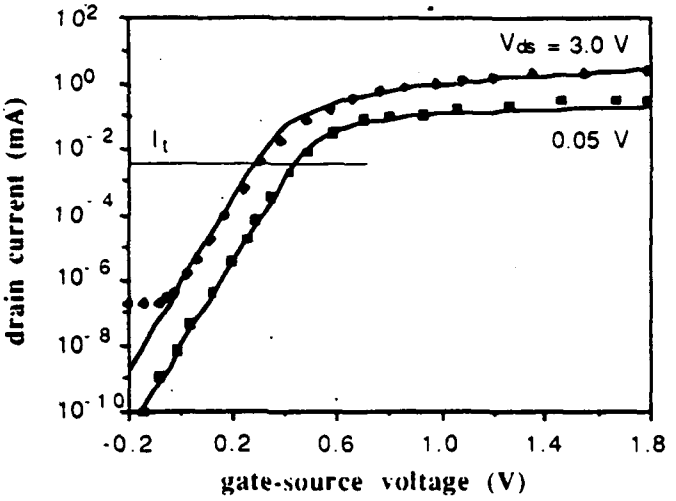

Fig. 2. *Subthreshold experimental (symbols) and calculated (solid lines)* I-V *characteristics for a deep submicrometer NMOS with effective gate length* L = *0.25 μm (the same as shown in Fig. 1).* I_t *denotes the threshold current.*

The advantage of the model described in this Report is its simplicity and applicability to short channel devices. However, it is also important to point out the limitations of this simple model. For example, the output conductance of long channel devices in the saturation regime is equal to zero (ideal saturation). The only way to approximate such an ideal saturation using eq. (14) (or eq. (22) with $\lambda = 0$) is to choose a large value of the shape parameter m. However, this leads to a very abrupt transition from the linear to the saturation regime in the computed current-voltage characteristics. In order to obtain a model which describes accurately devices with all channel lengths, we may choose to employ different equations for the linear and the saturation regimes while preserving the continuity of the drain current and its derivatives with respect to the terminal voltages. Such an approach was considered by Park et al. (1991) and Moon et al. (1991).

The dependence of the field effect mobility on the gate-source voltage can be accounted for within the framework of the model considered in this Report. However, the effective low field mobility may also depend on the drain-source voltage because the channel potential affects the surface electric field and, hence, the surface scattering. To some extent, these effects can be indirectly accounted for in the present model by adjusting the values of the parameters λ and m.

However, the ability of the model to reproduce these effects is limited. Here again, the more sophisticated models, such as the models developed by Park et al. (1991) and Moon et al. (1991). (These models have already been implemented in AIM-Spice. However, it is hard to compete with simplicity and with a set of equations that is easy to understand. Besides, for most practical modern day CMOS technologies, the model described in this Report is quite adequate.

The usefulness of the present unified MOSFET model is illustrated in the next Section where we describe the parameter extraction technique using this model.

3. Parameter Extraction

In order to apply the present model in circuit simulation, it is necessary to find a practical way of extracting the model parameters from experimental data. The accuracy of the parameter extraction depends on the accuracy of the model and on the accuracy and completeness of the experimental data.

In real life, there are usually problems with both the model and the experimental data. Even though the analytical model developed in this Reportreflect many important effects occurring in MOSFETs, such as velocity saturation, parasitic series resistances, the dependence of the threshold voltage on the drain voltage, and finite output conductance, many other important phenomena are included indirectly, at best. For example, our model treats the dependence of the mobility on the bias conditions only through effective values and, indirectly, through the fitting parameter λ. Furthermore, many complicated phenomena associated with the threshold voltage dependence on the drain-source voltage are accounted for in a set of simple, empirical formulae (see eqs. (19) to (21)).

Hence, our approach to the device characterization of MOSFETs is to extract effective device parameters, such as the threshold voltage, V_{TO}, the mobility, μ_n, the saturation velocity, v_s, the subthreshold ideality factor, η, the source and drain series resistances, R_S and R_d, the output conductance parameter, λ, the knee shape parameter m, the threshold voltage coefficient, σ_o, and the voltages $V_{\sigma t}$ and V_{σ} characterizing the dependence of parameter σ on the gate voltage swing. In other words, we describe a parameter extraction procedure which gives fairly reasonable results without parameter adjustment and which can produce a nearly perfect fit with some parameter adjustment. We should notice that, even without a precise knowledge of the device geometry and process

parameters, we can obtain a good fit to the device characteristics and, hence, predict the circuit performance fairly accurately using the AIM-Spice simulation program. Moreover, we still retain a limited ability to predict how device characteristics will scale with changes in the doping level and profile and device geometry. In other words, our model and parameter extraction procedure attempt to give the best possible answer based on the available information.

As an example, we perform the parameter extraction for the device with the characteristics shown in Fig. 1 and 2. We start by extracting the drain bias dependence of the threshold voltage from the measurements of the drain current versus gate-source voltage for different drain-source voltages. Plotting the results of these measurements in a semilog scale, as illustrated in Fig. 2, we can determine ηV_{th} from the slope of the characteristics in the subthreshold regime. We then estimate the threshold current in saturation, I_t, from eq. (16) using eq. (4) for electron sheet density at threshold, i.e.,

$$I_t = \frac{\varepsilon_i \mu_n W \eta V_{th}^2}{(d_i + \Delta d) L} \tag{24}$$

At this point, we do not need to know accurate values for the electron mobility, μ_n, the effective channel length, L, and the oxide thickness, d_i, because the threshold voltage is fairly insensitive to the exact value of I_t. (For our device, $I_t \approx 3\text{x}10^{-6}$ A.) The intercept of the measured curves with the line $I_d = I_t$ yields the values of the threshold voltage versus drain-source voltage (see Fig. 2). A linear interpolation of this dependence yields the parameter σ_o. For the present device, we find $V_{To} \approx 0.44$ V and $\sigma_o \approx 0.048$.

The next step is to find the shape parameter, m, for the knee region of the characteristics. For near ideal characteristics, with low output conductance in saturation, the extraction method is as indicated in Fig. 3. Each characteristic is approximated by two linear pieces, one describing correctly the linear region at small drain-source voltages (slope g_{ch}) and one approximating the characteristic in the saturated region (slope g_{chs}). The linear pieces intersect at the saturation current, I_{sat}, at the drain-source voltage voltage $V_{ds} = g_{ch}/I_{sat} \approx V_{sate}$ (see the discussion in Section 2). According to eq. (22), the real current at this drain-source voltage is $I_d = I_{sat} - \Delta I \approx I_{sat}/2^{1/m}$. Hence, by locating the interReport in the two-piece linear model applied to the experimental characteristic, as shown in

Fig. 3, and measuring the currents I_{sat} and $I_{sat} - \Delta I$, we can determine m as follows:

$$m \approx \frac{\ln(2)}{\ln[\, I_{sat} / (I_{sat} - \Delta I)\,]} \tag{25}$$

For the curve shown in Fig. 3, we obtain $m \approx 4$.

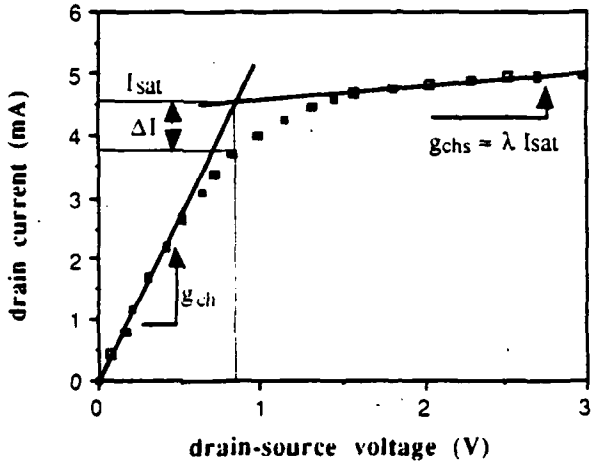

Fig. 3. *Method for extracting the shape parameter* m., *the saturation current,* I_{sat}, *and the parameter* λ. *The* I-V *characteristic is taken from Fig. 1* (V_{gs} = *3.0 V).*

From the output conductance in deep saturation, g_{chs}, for the largest value of V_{gs}, we also determine the value of parameter λ from the expression

$$\lambda = \frac{g_{chs}}{g_{ch} V_{sate}} \approx \frac{g_{chs}}{I_{sat}} \tag{26}$$

(see the discussion in Section 2). From Fig. 3, we find $\lambda \approx 0.048\ V^{-1}$.

The next step involves the determination of the total series resistance, $R_t = R_s + R_d$, and the transconductance parameter

$$\beta = \frac{\varepsilon_i\, \mu_n W}{L(d_i + \Delta d)} \tag{27}$$

In the above-threshold regime, the intrinsic, linear channel conductance can be expressed as follows in terms of β: $g_{chi} \approx \beta V_{GT} \approx \beta V_{gt}$. Hence, we can write

$$\frac{1}{g_{ch}} = \frac{1}{g_{chi}} + R_t \approx \frac{1}{\beta V_{gt}} + R_t \tag{28}$$

This allows β and R_t to be determined from the slope and the intercept with $1/g_{ch} = 0$ by plotting $1/g_{ch}$ versus V_{gt}. Such a plot is shown in Fig. 4 for the NMOS device under investigation, resulting in the following parameter values: $R_t \approx 150$ ohm and $\beta \approx 0.011$ A/V^2. However, we note that since the series resistance in this short channel MOSFET dominates the overall device resistivity in the linear regime, the determination of β by this method is somewhat uncertain. Besides, this technique of extracting β emphasizes the properties of the *I-V* characteristics in the linear regime while, in fact, the properties of saturation region are of greater interest in digital applications. Therefore, we return below with alternative ways of estimating β.

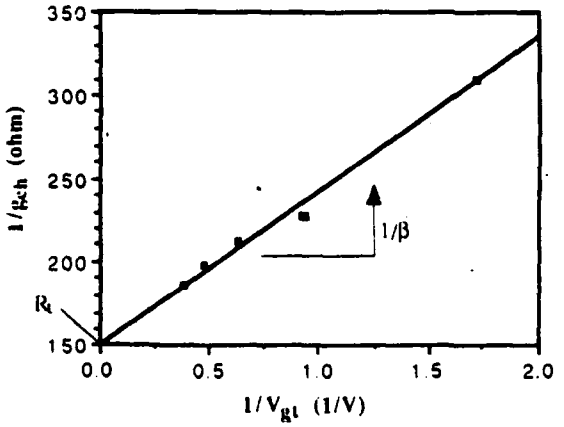

Fig. 4. *Plot of inverse channel conductance versus inverse gate voltage swing, used for the determination of the parameters* R_t *and* β.

For MOSFETs, we normally have $R_S \approx R_d \approx R_t/2$. If there is an asymmetry between the source and drain, an accurate estimate of the difference between R_S and R_d can be made by measuring the normal, extrinsic device transconductance in the saturation regime, g_m, and its counterpart, g_{mr}, with the source and drain interchanged (at constant drain current). Since the intrinsic transconductance is the same in both cases, we find

$$R_s - R_d = \frac{1}{g_m} - \frac{1}{g_{mr}} \tag{29}$$

In our our case, however, we used $R_s = R_d = R_t/2 = 75$ ohm.

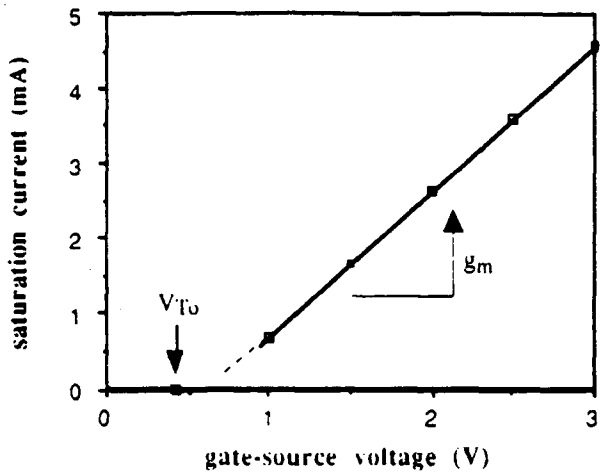

Fig. 5. *Measured saturation current (defined in Fig.3) versus gate-source voltage for the same device as in Fig. 1. This plot is used to determine the extrinsic transconductance in saturation*

Fig. 5 shows the dependence of the above-threshold saturation current, I_{sat}, on the gate-source voltage. From a suitable interpolation formula representing the experimental data, we can determine the extrinsic transconductance in saturation, g_m, as a function of V_{gs} by differentiation. The intrinsic transconductance is subsequently obtained as $g_{mi} = g_m/(1 - g_m R_s)$. According to our model, we can write

$$\frac{1}{g_{mi}^2} = \frac{1}{\beta^2 V_{GT}^2} + \frac{1}{\beta^2 V_L^2} \tag{30}$$

where $V_{GT} = V_{gt} - R_s I_{sat}$. Hence, by plotting $1/g_{mi}^2$ versus $1/V_{GT}^2$, we obtain β from the slope and βV_L from the intercept with the $1/g_{mi}^2$ axis (at $1/V_{GT}^2 = 0$). A plot based on eq. (30) and the data in Fig. 5 is shown in Fig. 6. As can be seen from this figure, the slope in this particular case is too small to serve as a reliable estimate for β. However, from the intercept, we find that $\beta V_L \approx 0.026$ A/V which corresponds to a saturation velocity $v_s \approx 4\text{x}10^4$ m/s. This value of v_s seems to be too low compared to the well established measured value of $v_s \approx 8\text{x}10^4$ m/s (see, for exaple, Chan et al. (1990)). However, we checked that the values of v_s extracted from these experimental data by other models, such as the model presented by Park et al. (1991) and the model by

Sodini et al. (1984), are quite similar. This may mean that there could be some uncertainty in the device parameters given by Chung et al. (1991).

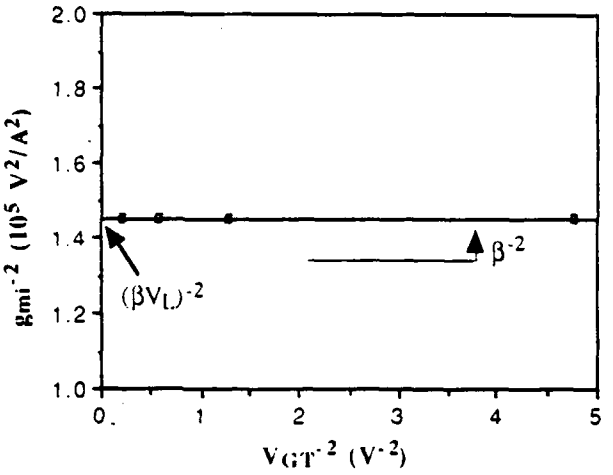

Fig. 6. Plot for the determination of the parameters β and V_L.

An alternative way to crudely estimate β from the experimental data (often used in literature) is to consider the saturation current slightly above threshold where $(V_{GT}/V_L)^2 << 1$. Then, the equation for the saturation current can be approximated by

$$I_{sat} = \beta V_L^2 \left[\sqrt{1 + \left(\frac{V_{GT}}{V_L} \right)^2} - 1 \right] \approx \frac{\beta}{2} V_{GT}^2 \tag{31}$$

and $(\beta/2)^{1/2}$ is found as the slope of the plot of $(I_{sat})^{1/2}$ versus V_{GT} ($\approx V_{gt}$ in this regime). (It may also suffice to measure I_{sat} for one value of V_{gt} sufficiently close to threshold). However, this technique is not very accurate in short channel devices where the region $V_{GT} << V_L$ is very narrow and may be affected by subthreshold current caused by short channel effects.

Using the various techniques described above, we arrive at the following parameter values used to fit the experimental *I-V* characteristics in Figs. 1 and 2: $\beta \approx 0.0067$ A/V^2 and $V_L \approx 0.36$ V, which correspond to $v_s \approx 4 \times 10^4$ m/s and $\mu_n \approx 0.028$ m^2/Vs. However, we note that a higher value of β (and μ_n), i.e., more in accordance with the values obtained from the slope in Fig. 4, would have

given a better fit in the linear part of the I-V characteristics, while the present values favour a good fit in the saturation region (which is of primary importance in digital applications).

Finally, we have to choose the voltages $V_{\sigma t}$ and V_{σ} which determine the dependence of the threshold voltage parameter σ on the gate-source voltage. Here, we have chosen $V_{\sigma} \approx 0.2$ V and $V_{\sigma t} = V_{To} + 0.5(V_{gt})_{max} \approx 1.7$ V. However, these parameter values can be slightly adjusted for a better fit.

4. Application of Model in AIM-Spice Simulation

The present model has been implemented in our circuit simulator, Automatic Integrated Circuit Modeling Spice (AIM-Spice). AIM-Spice runs under the WINDOWS™-3 environment on IBM PCs and compatible computers and takes full advantage of the resident graphics user interface and memory above the 640k DOS limit.

Fig. 7 is a screen-dump from the AIM-Spice post-processor showing a composite view of relevant voltages and currents from a turn-off transient analysis of a simple NMOS inverter circuit with an NMOS load at the output. The subthreshold regime is emphasized by showing the turn-off recovery of the drain current of the driver transistor in a semi-logarithmic scale. The inverter and load contain altogether three identical quarter micron transistors with the specifications corresponding to the transistors with characteristics shown in Fig. 1. The capacitances are calculated according to Meyer's expressions (see Section 2).

Fig. 7. *Transient analysis of an NMOS inverter with an NMOS load at the output. All transistors have the specifications given in Fig. 1. The trace in the background shows the input to the gate of the driver transistor (the gate of the inverter load transistor is fixed at 1.5 V and the voltage supply is $V_{DD} = 3.0$ V). The upper and lower traces on the right hand side show the drain-source voltage and the drain current for the driver transistor, respectively. (from Ytterdal et al. (1991).*

III. Modeling of Radiation Effects.

Fig. 8 shows typical experimental data for an unhardened CMOS process (from Baze et al. (1990)). As can be seen from the figure, the 60 krad dose leads to a considerable shift of the threshold voltage and to a drastic (over three orders of magnitude) increase in the leakage current. The device leakage current recovers after a long anneal. However, the threshold voltage shift remains.

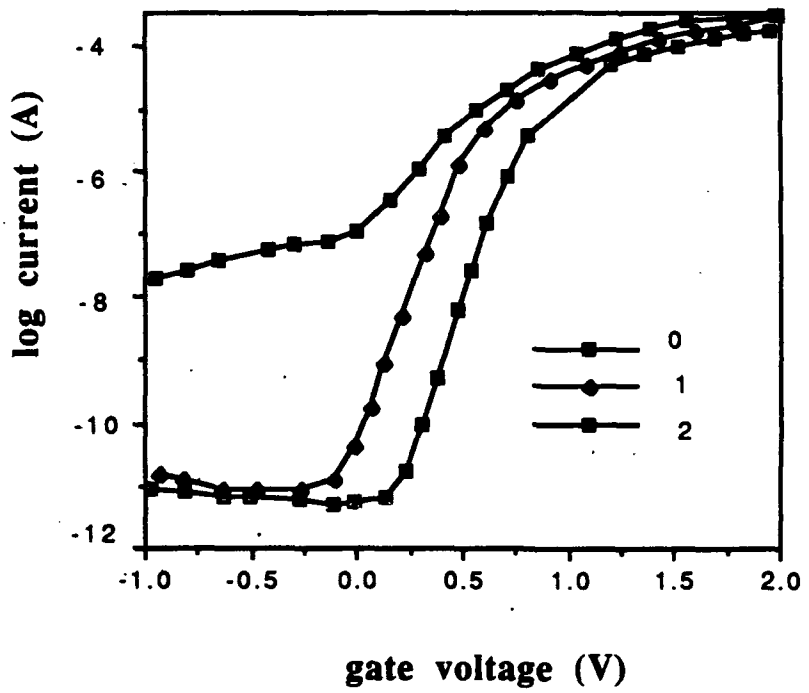

Fig. 8. Current-voltage characteristics for unhardened CMOS (after Baze et al. (1990)). n-channel device, V_{gs} = 5 V, Dose rate 167 rad/s. 0 - pretest, 2 - 60 krad (SiO_2), 1 60 krad and 107 sec anneal at 25 °C.

These characteristics can be readily modelled using our model when we include an additional leakage current

$$I_{leak} = \sigma_{leak} V_{ds} \tag{32}$$

The calculated curves are shown in Fig. 9.

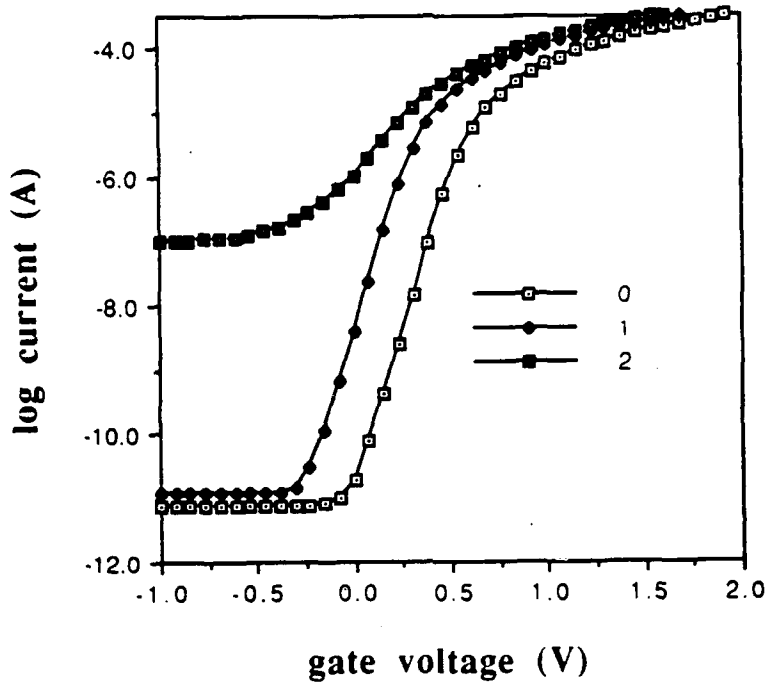

Fig. 9. Calculated current-voltage characteristics for unhardened CMOS. 0.. - pretest, 1. - 60 krad after anneal, 2. - 60 krad dose.

IV. Software listing.

```
REM
REM  Michael Shur (804)-924-6109
REM  fax (804)-924-8818
REM  e-mail ms8n@virginia.edu
REM
REM Program MOSFET.s
REM  version 1 5/2/91
REM pMOSFET.s calculates unified short-channel MOSFET I-Vs
REM
REM  The program is the subroutine of program PLOTII
REM which creates data files for Cricket graph
REM
REM
```

```
SetLimits:
REM x-axis variable limits
Xstart =-1:Xend=2
RETURN
ReadData:
Fpar%=1
A$="pMOSFET.s"
FL$="pMOSFET.s"
REM +++++ DATA SECTION ++++++
REM constants
REM +++++ DATA SECTION ++++++
REM constants
q=1.602E-19 'Coulomb
kb=1.38E-23'J/m
REM temperature
T=300' degree K
REM material parameters
eps=1.04E-10'F/m
epi = 3.44E-11'F/m
W = .00003
L = .0000007
di = .0000001
Nd = 4E+23
mob = .028
'm2/Vs mobility
vs = 40000!'m/s saturation velocity
m=4' saturation knee parameter
Vto = .44 'threshold voltage
Rsm = .75 'source series resist. ohm-mm
Rdm = .75 'drain series resist. ohm-mm
Rs=Rsm/(W*1000)
Rd=Rdm/(W*1000)
Rt = Rs + Rd
lambda=.044' output conductance parameter
sigmao=.048 'DIBL parameter
Vsigma = .2 'DIBL voltage parameter
Vst = 1.75 'DIBL transition parameter
eta=1.32 'subthreshold slope
sig=1E-11
Vds=1
GOSUB SetLimits
REM ****************************************
PRINT A$: PRINT
```

```
GOSUB PARDEF
RETURN
PARDEF:
Jpar%(1) = 3:par(1,1)=0:par(1,2)=1:par(1,3)=2
Rad = PARAMETER
RETURN
UPDATEPAR:
GOSUB PARDEF
RETURN
FirstFunction:
Vgs = xxx
IF Rad=0 THEN Vto=.5:sig=8E-12:eta=1.72
IF Rad=1 THEN Vto=.25:sig=1.2E-11:eta=1.72
IF Rad=2 THEN Vto=.1:sig=.0000001:eta=6
Vth = kb*T/q' thermal voltage
VL = vs*L/mob
no = epi*eta*Vth/(2*di*q)
Vgto = Vgs - Vto
sigma = sigmao/(1+EXP((Vgto-Vst)/Vsigma))
Vgt = Vgto + sigma*Vds
Vgho = .5*Vgt/Vth
Vgh=Vgt/(eta*Vth)
Vgte=Vth*(1+Vgho+(9+(Vgho-1)^2)^.5)
GOSUB nscalc:
'PRINT Vgs, Vgte, Vgh, ns
gchi =q*ns*W*mob/L
gch = gchi/(1+gchi*Rt)
gR=gchi*Rs
Isat = gchi*Vgte/(1+gR+SQR(1+2*gR+(Vgte/VL)^2))
zz=gch*Vds/Isat
Ids=gch*(1+lambda*Vds)*Vds/(1+zz^m)^(1/m)+sig*Vds
yyy = LOG(Ids)/LOG(10)
PRINT sig, Vto,eta
RETURN

REM subroutine nscalc
nscalc:
REM ns calculation
IF Vgh> 86 THEN ns = epi*Vgt/di
IF Vgh< -12 THEN ns = no*EXP(Vgh)
IF Vgh> -12 AND Vgh<86 THEN ns = 2*no*LOG(1 + .5*EXP(Vgh))
RETURN
```

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VII. Appendix. Device structure and equivalent circuit

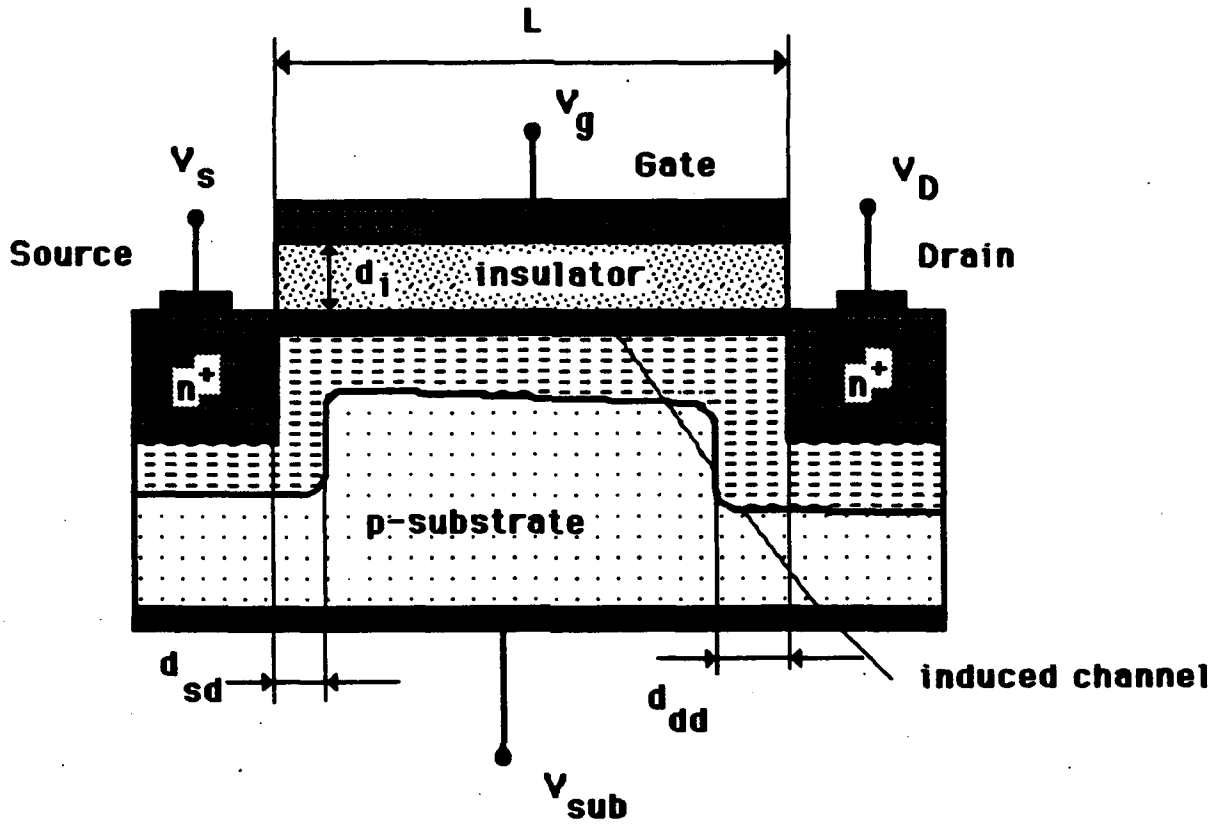

Fig. A1. Schematic device structure of NMOS.
Typical device dimensions: $W = 30$ μm, $L = 0.7$ μm, $d_i = 100$ Å

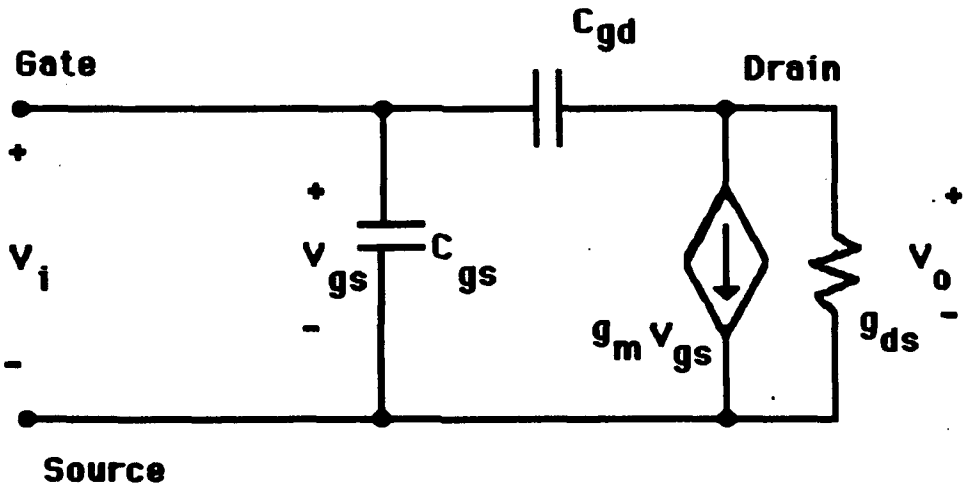

Fig. A2. Simplified equivalent circuit of NMOS.