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A NEW MULTIPLIER-FREE STRUCTURE FOR DFT BASED ON DELTA MODULATION

by

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A New Multiplier-Free Structure for DFT Based on Delta Modulation

Tang Kaijun, Siang Jingcheng, Huang Shunji
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Abstract A new implementation of the DFT based on delta modulation (DM) is proposed. It is different from the conventional implementation based on PCM. The hardware structure of the method is constructed without A/D converter and multiplier, so it is simpler and of lower cost. Its SNR can approach that of the conventional one, such as FFT. Computer simulations demonstrate that for deterministic signals, results obtained agree well with theoretical analyses, for band-limited Gaussian signals; if step size is suitably selected, results similar to the conventional DFT can still be obtained. Because of the limitation of the working speed of the device, this method will be suitable for processing speech and seismic signals. Finally, the hardware structure which simply consists of a ROM, an adder and some other auxiliary circuits is given.

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I. Introduction

Delta modulation (DM) is a simple coding method for various signals. In the past DM was mainly used in coding signals for transmission. Recently, application of DM has been extended to processing of digital signal and a family of DM wave filters[2-7] have been proposed. However, research aimed at applying DM to spectrum analysis is rare. The purpose of this paper is to utilize the relationship between DM serial spectrum and PCM serial spectrum to carry out spectrum analysis by DM method.

II. Delta Modulation Series Fourier Spectrum

Binary DM series is considered in this paper. Assuming that proper step size and sampling frequency were selected, the probability for the slope to be overload is very small and can be ignored.

A DM series is defined as:

$$dx(n) \triangleq \mathrm{sign}(x(n) - \hat{x}(n-1)), \tag{1}$$

where $\hat{x}(n-1)$ is the predicted value at n-1 instant. Because only linear DM system is studied in this work, the step size Δ is a constant. Figure 1 shows the delta modulator and figure 2 is the equivalent liberalized block diagram of figure 1.

Based on figure 2 we have:

$$\Delta dx(n) = x(n) - x(n-1) + e_q(n) - e_q(n-1), \tag{2}$$

where eq(n) is the quantified error series. Statistical analysis shows that it can be considered as the white noise homogeneously distributed between $[-\Delta, \Delta]$.

The DM series Fourier spectrum can be defined by:

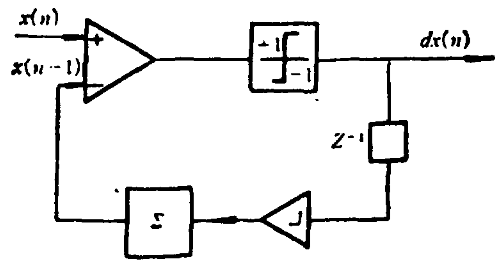


Fig. 1: Delta modulator

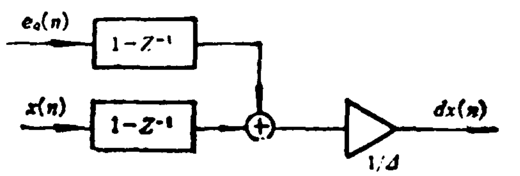


Fig. 2: Linear equivalent diagram of delta modulator

$$X_d(k) \triangleq \sum_{n=0}^{N-1} dx(n) W_N^{kn}, \quad k = 0, 1, \cdots, N-1; \tag{3}$$

or

$$X_d(k) = \sum_{n=0}^{N-1} dx(n) h(N-1-n, k), \quad k = 0, 1, \cdots, N-1; \tag{4}$$

where $h(n,k) = W_N^{-k(n+1)}$.

Figure 3 shows the circuit diagram of analyzed DM spectrum and figure 4 is the linear equivalent diagram of the entire system. Equation (4) is actually the roll product of the input series dx(n) and the pulse response function h(n,k) of FIR wave filter.

The relationship between the Fourier spectrum $X_q(k)$ of pulse coding modulation series and the Fourier spectrum $X_j(k)$ of DM series is:

$$X_{qn}(k) = X_{q,n-1}(k) + \Delta X_{\Delta n}(k), \tag{5}$$

where the definition of $X_{qn}(k)$ and $X_{jn}(k)$ are defined by:

$$X_{qn}(k) \triangleq \sum_{r=0}^{N-1} x_q(n+r) W_N^{kr}, \quad k = 0, 1, \cdots, N-1; \tag{6}$$

$$X_{\Delta n}(k) \triangleq \sum_{r=0}^{N-1} dx(n+r) W_N^{kr}, \quad k = 0, 1, \cdots, N-1. \tag{7}$$

and $x_q(n)$ in equation (6) is the quantitative magnitude of x(n).

Let $x_q(n) = \hat{x}(n)$ and from the relationship $\hat{x}(n) = \hat{x}(n-1) + \Delta dx(n)$ we can obtain equation (5). Equation (5) shows that the Fourier spectrum of PCM can be obtained by summing the Fourier spectra of DM.

The sampling rate parameter K is defined as $T/\Delta t$, where T is the Niquest sampling spacing and Δt is the DM sampling spacing and N=KM where M is the number of sampling points based on the

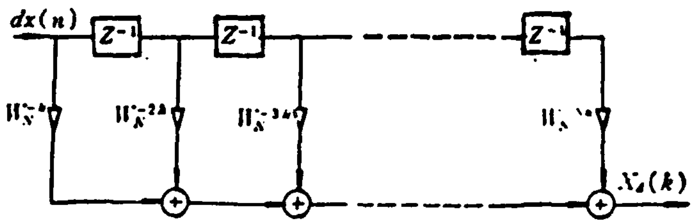


Fig. 3: DM spectrum analysis diagram

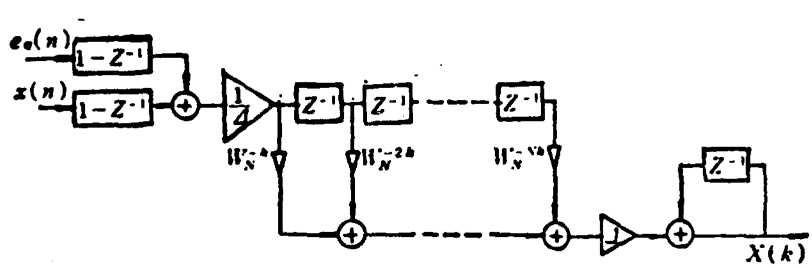


Fig. 4: Linear equivalent diagram of the entire system

Niquest sampling criterion. Because the signal band width is fixed, after adopting the DM system the sampling rate is enhanced by K times and X(k)=0 within one period of the cycle domain when M/2<=k<N-(M/2).

After adopting DM, the speed for the corresponding addition operation is improved by K times and the multiplication operation of the entire system are eliminated. For signals with narrow band width such as speech signals, the speed for addition operation will provide a healthy margin and this plan will work fine.

III. Quantitative Error Analysis of Delta Modulation

The transformation from the non-linear DM system to linear system is by the introduction of quantitative noise. It has been discussed above that the treatment of quantified noise as homogeneously distributed white noise is reasonable. This treatment also simplifies the system analysis.

Assuming the input is the white noise with power σ_x^2, then the power of the output signal, based on figure 4, is:

$$E[|X(k)|^2] = N\sigma_x^2, \qquad (8)$$

Similarly, the power of the output noise is:

$$E[|E(k)|^2] = N\sigma_{e_q}^2, \qquad (9)$$

Therefore, the output signal to noise ratio is:

$$\frac{E[|X(k)|^2]}{E[|E(k)|^2]} = \frac{\sigma_x^2}{\sigma_{e_q}^2} = CK^3, \qquad (10)$$

where $\sigma_x^2/\sigma_{e_q}^2 = CK^{3*}$, is the relationship between the input signal to noise ratio and the sampling rate coefficient K under the condition where there is no slope overload and maximum signal to noise ratio,[7] C is a proportionality constant. If the input is the band-limited Gaussian signal, then $C=6/(a\pi)^2$ and a should be determined by the probability of occurrence of slope overload.[7]

In PCM systems, the increase in the input signal-to-noise ratio is accomplished through extending the word length of A/D convertor, while in DM systems, it is accomplished through increasing the sampling coefficient. Therefore, in digital signal processing, DM method can be used to replace PCM methods and achieve the same result. Hence, DM method is an effective method in realizing digital signal processing.

(In reference [7], $\sigma_s^2/\sigma_{e_q}^2 = CK^3$, and the assumption $\sigma_{e_q}^2 = \frac{\Delta^2}{3}$. was made by its author. If the noise in the band width of the signal is considered we would obtain $\sigma_{e_q}^2 = \frac{\Delta^2}{3} \cdot \frac{2f_m}{f_s} = \frac{\Delta^2}{3K}$, and $\sigma_s^2/\sigma_{e_q}^2 = CK^3$.)

IV. Analysis of Limited Word Length Effect

There are two realization methods in digital signal processing; fixed point realization and floating point realization. Because of the limitation of word length of available hardware, only limited number of digits can be used and certain error is brought to the actual result. The following analysis shows the effect of these two realization methods on system function.

1. Fixed point realization limited word length effect

As shown in figure 4, because of the absence of multiplication operation there is only one kind of error; namely, the coefficient quantization error. As discussed in literature[4] this is a homogeneously distributed white noise.

However, in order to ensure no overflow when summation is taken, the summation was carried out in groups as shown in figure 5.

Based on equation (5), the relationship between X(k) (the subscripts q and n are deleted and X(k) is treated as the Fourier spectrum without coefficient quantization beginning with n=0) and $X_\Delta(k)$, note that $0<k<M/2$ and $K>=8$[9] and $|2\pi k/N|<\pi/K<1$ if the input signal-to-noise ratio is to be greater than 20dB, is

$$
\begin{aligned}
X(k) &\approx \frac{N\Delta}{j2\pi k} X_\Delta(k) \\
&= \sum_{n=0}^{N-1} dx(n)\left(\frac{N\Delta}{j2\pi k} W_N^{kn}\right), \quad k = 1, 2, \cdots, \frac{M}{2} - 1.
\end{aligned} \qquad (11)
$$

To ensure the absolute magnitude of the quantity in the bracket in equation (11) is smaller than 1, it is multiplied by a constant C and let

$$h_1(n, k) = \frac{N\Delta C}{j2\pi k} W_N^{-k(n+1)}.$$

with a suitably chosen constant C, $h_1(n,k)$ can be sufficiently expressed in terms of words with limited length as figure 5 shows.

Another error is introduced by this realization method; the digit-shifting operation error, which is treated again as a homogeneously distributed white noise and can be expressed by $\eta(p,n)$ ($p=1,2, \ldots, m=\log_2 N$; $n=0,1,\ldots,N-1$; where N is the powers of 2). Its real and imaginary parts are taken as $-2^{-(b+1)}$, 0, $2^{-(b+1)}$ with equal probability. From figure 5,

$$X(k) = \sum_{n=0}^{N-1} \left(\frac{1}{2}\right)^{\log_2 N} x(N-1-n)Ch(n, k), \qquad (12)$$

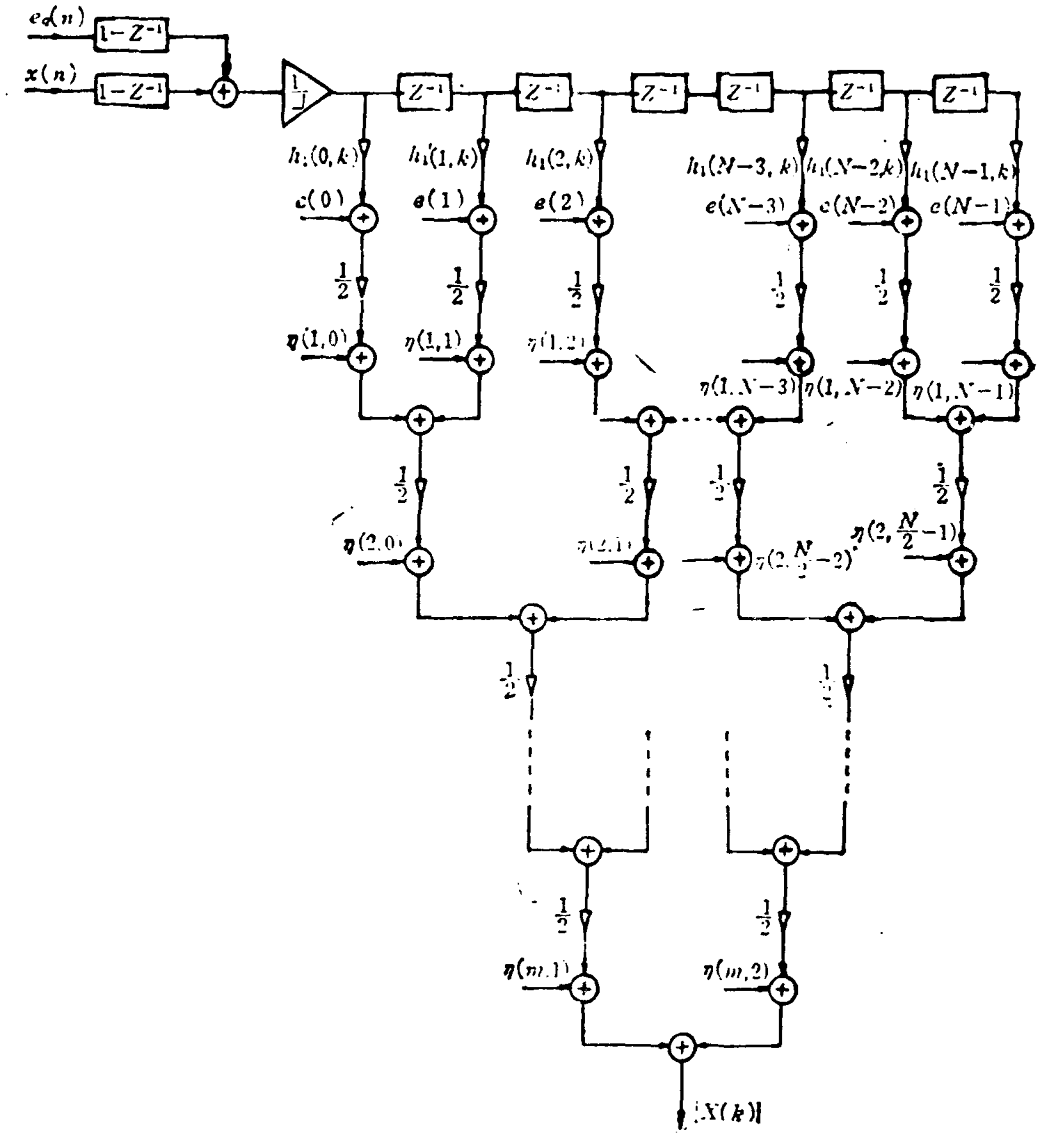


Fig. 5: Statistical analysis diagram of fixed point realization method

$$X_q(k) = \sum_{n=0}^{N-1} \left(\frac{1}{2}\right)^{\log_2 N} x(N-1-n)Ch_q(n,k), \qquad (13)$$

where Xq(k) is the Fourier spectrum with quantized coefficients.

The error of coefficient quantization is

$$\begin{aligned} E(k) &= X(k) - X_q(k) \\ &= \sum_{n=0}^{N-1} \left(\frac{1}{2}\right)^{\log_2 N} x(N-1-n)Ce(n,k) \\ &= \sum_{n=0}^{N-1} \frac{C}{N} x(N-1-n)e(n,k). \qquad (14) \end{aligned}$$

The power of the output noise is:

$$E[|E(k)|^2] = \frac{C^2\sigma_x^2\sigma_e^2}{N}, \qquad (15)$$

where $\sigma_C{}^2 = 2^{-2b}/6K$, and $\sigma_x{}^2$ is the power of input signal.

Similarly, if the input is the white noise signal, the output signal-to-noise ratio is

$$\frac{E[|E(k)|^2]}{E[|X(k)|^2]} = \sigma_e^2 = \frac{2^{-2b}}{6K}. \qquad (16)$$

Similar to the above analysis, the error corresponding to any digit-shifting of the s level is

$$\begin{aligned} E_s(k,s) &= \sum_{n=0}^{N/2^{s-1}-1} \left(\frac{1}{2}\right)^{\log_2 N - s} x(N-1-n)\eta(s,n) \\ &= \sum_{n=0}^{N/2^{s-1}-1} \frac{2^s}{N} x(N-1-n)\eta(s,n). \qquad (17) \end{aligned}$$

The total noise power

$$\begin{aligned} E[|E_s(k)|^2] &= E[|E_s(k,1)|^2] + E[|E_s(k,2)|^2] + \cdots + E[|E_s(k,s)|^2] \\ &= \frac{2^2}{N}\sigma_x^2\sigma_q^2 + \frac{2^3}{N}\sigma_x^2\sigma_q^2 + \cdots + 2\sigma_x^2\sigma_q^2 \\ &\approx 4\sigma_x^2\sigma_q^2. \qquad (18) \end{aligned}$$

and the output signal-to-noise ratio is

$$\frac{E[|E_s(k)|^2]}{E[|X(k)|^2]} = 4N\sigma_q^2 = \frac{4}{3}M2^{-2b}, \qquad (19)$$

where

$$\sigma_q^2 = 2\left(\frac{1}{3K}2^{-2(b+1)} + \frac{1}{3K}2^{-2(b+1)}\right) = \frac{1}{3K}2^{-2b}.$$

Comparing equations (19) and (20), it is obvious that the error from digit-shifting is greater than the input of coefficient. Therefore, digit-shifting noise is the major source of noise. This result is consistent with the noise signal of fixed point realization when FFT is calculated.

2. Floating point realization limited word length effect

Even though fixed point realization is easier, it requires longer word length and more adders. The floating point realization method discussed below will avoid this problem. Figure 6 is the equivalent statistical block diagram.

Similar to the above analysis, the coefficient quantization error e(n) and operation error ηi(n) are treated as homogeneously distributed white noise with a average value of 0 and square difference of $^2/_{3K}2^{-2bq}$ and $^2/_{3K}2^{-2br}$, where b_q and b_r are the coefficient quantization word length and operation round-off word length, respectively.

Similar to the analysis in reference [1], if the input were the white noise signal, then the output signal-to-noise ratio is

$$\frac{E[|E(k)|^2]}{E[|X(k)|^2]} \doteq \frac{2}{3K} 2^{-2b_q} + \frac{M}{3} 2^{-2b_r}. \qquad (20)$$

Computer simulation has shown that, if the input signal-to-noise ratio is 40dB then K has the value of 32.[9] If M is taken as 128, then N is 4096. Because generally $b_r >> b_q$ and if the latter is ignored, then the above equation can be approximated by

$$\frac{E[|E(k)|^2]}{E[|X(k)|^2]} \approx \frac{2}{3K} 2^{-2b_q}. \qquad (21)$$

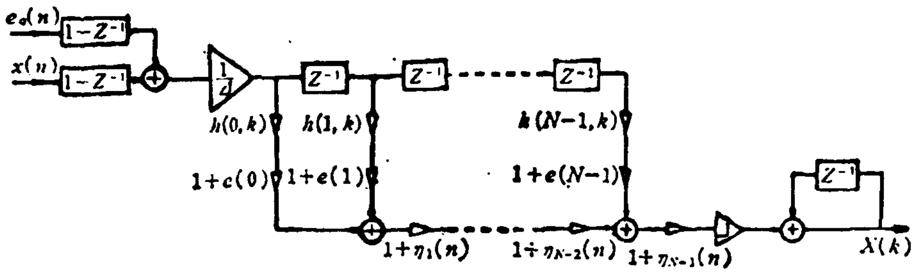


Fig. 6: Statistical analysis diagram of floating point realization method

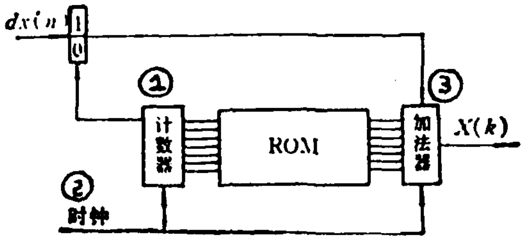
This result is better than the output signal-to-noise ratio based on the FFT fixed point realization and, indeed, this is because the operation error is ignored.

So far we have carried out a detailed analysis of the characteristics of DFT of DM and compared the result with that of FFT. In the course of our analysis all the inputs were assumed to be the white noise. In reality, delta modulation can not be carried using this type of signal. Computer simulation shows that if the input were the sinusoidal signal, under the condition that the minimum value is not lost when the summation is calculated; namely, when $b_q<-6$, $b_r>-18$, the increase in one digit of b_q will result in the increase of signal-to-noise ratio by 6dB. This is consistent with the theoretical analysis that when the decimal point of b_q in increased by one digit the signal-to-noise ratio will increase by 6dB.

V. Hardware Realization of Delta Modulation DFR

In the previous section, when the round-off effect of floating point realization was analyzed, a constant C was not used to prevent overflow of the coefficient. In the following analysis, the floating point realization is analyzed by equation (11), similar to the fixed point realization case. The discussion will be focused firstly on the hardware realization of floating point, then the determination of constant C, and finally the hardware realization of fixed point.

As shown in figure 7, the DM series (+1,-1) is first transformed to the binary coding (0,1) and then input to the



key: 1 - counter

2 - clock

3 - adder

Fig. 7: Hardware realization diagram of floating point calculation

controlling end of the adder for addition/subtraction operation. The clock is used as the counter input and the counting is used as the ROM address code. Each coefficient is stored in ROM sequentially. Addition/subtraction operation is executed if the binary code is 0/1. After N addition/subtraction operations, the output is X(k).

Equation (11) can be re-written as follows. Let

$g(n,k) = \frac{N\Delta C}{j2\pi k} W_N^{kn}$, (H)

$$X(k) = \sum_{n=0}^{N-1} dx(n) g(n,k). \quad (I)$$

According to the cyclic behavior of g(n,k), the above equation can be expressed as:

$$\begin{aligned} X(k) &= \sum_{n=0}^{N/2-1} dx(n)g(n,k) + \sum_{n=N/2}^{N-1} dx(n)g(n,k) \\ &= \sum_{n=0}^{N/2-1} dx(n)g(n,k) + (-1)^k \sum_{n=0}^{N/2-1} dx\left(n+\frac{N}{2}\right)g(n,k). \end{aligned} \quad (22)$$

The above equation has the property that if k=odd, then the N/2's dx(n) after n>=N/2 have opposite signs while the value of g(n,k) is unchanged; if k=even, then the N/2's dx(n) after n>=N/2 have their signs unchanged. Combining these two conditions, the ROM storage space can be reduced by half and only N/2 is needed for maximum counting. When n>=N/2, the counter will return to 0 and ROM will be re-read; only when k is odd a pulse will be output after the counter is full to control the input binary data to transform 0 to 1 and vice veers.

Similarly, if the value of k is taken to be a factor of N, equation (22) can be further decomposed to 2k terms and the ROM storage can be reduced to N/2k.

The determination of C of g(n,k) of equation (21) can be divided into the real and imaginary parts since g(n,k) is a complex function. Let

$$\max(|\mathrm{Re}(g(n,k))|,\ |\mathrm{Im}(g(n,k))|) = \frac{N\Delta C}{2\pi} = 2^{2^{b_c-1}}(1-2^{-b_m}), \qquad (23)$$

$$\min(|\mathrm{Re}(g(n,k))|,\ |\mathrm{Im}(g(n,k))|) = \Delta C = 2^{-(2^{b_c}-1)}2^{-1}(0\ \text{除外}), \qquad (24)$$

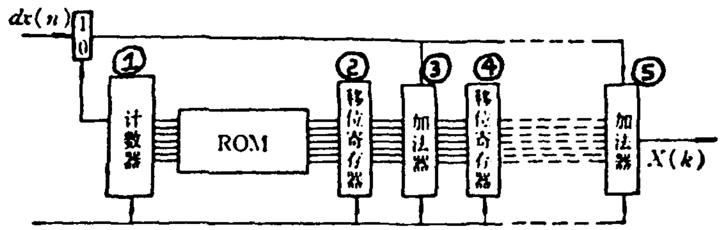
where b_c is the length of the valence code and b_m is the length of the tail number. Solving for the above two functions, one would obtain

$$C = \frac{1}{\Delta}\sqrt{\frac{\pi}{N}(1-2^{-b_m})}. \qquad (25)$$

The value of b_m can be determined if the signal-to-noise ratio is assigned. C can then be calculated using the above equation. As a result, b_c can be determined.

In the above analysis the word length of g(n,k) is determined. Actually, the word length of ROM is determined. Similarly, the word length of the adder can be determined. In order to ensure that the minimum quantity of g(n,k) will not be lost when summation is calculated, the word length should be determined based on the maximum value of X(k) and the minimum value of g(n,k). Because of the greater difference between the maximum value of X(k) and the minimum value of g(n,k), the required tail number is longer.

Figure 8 shows the hardware realization. Except for extra adders and digit-shifting temporary storers, the other parts are similar to the floating point hardware realization. If the summation is calculated by dividing the series not into pairs of numbers but into groups of 2^s numbers, then each number needs to



key: 1 - counter

2 - digit-shifting storer

3 - adder

4 - digit-shifting storer

5 - adder

Fig. 8: Hardware realization diagram of fixed point calculation

be shifted by s digits. If the maximum of s is taken as $\log_2 N$, only one adder is required. However, the digits of the adder is also increased correspondingly.

VI. Computer Simulation

In order to illustrate the feasibility of delta modulated DFT, we have chosen two different sinusoidal signals: (1) the input is the three sinusoidal signals with different frequencies, and (2) the input signal is the band-limited Gaussian signal, for simulation on VAX11/780 computers.

For the first kind of signals, three frequencies: 1kHz, 0.5kHz, 0.25kHz are assumed with magnitude of 5V, 1V, and 3V, respectively.

Based on the Niquest sampling criterion, 1/T=2kHz, if the required input signal-to-noise ratio is taken as 40dB then K has the value of 32 and the delta modulation sampling frequency $f_s=1/\Delta t=K/T=64$kHz. Therefore, let

$$x(t) = 10\sin 2\pi f_1 t + 5\sin 2\pi f_2 t + 3\sin 2\pi f_3 t, \tag{26}$$

where $f_1=0.5$kHz, $f_2=1$kHz, $f_3=0.25$kHz. In order to avoid slope overload, let

$$\frac{\Delta}{\Delta t} \geq x'_{max}(t), \tag{27}$$

then $\Delta>=1.055$ and Δ is taken as 1.055. Figure 9 shows the Fourier spectrum based on the delta modulation method. It can be seen from figure 9 that, because of the sinusoidal signal of limited length, the three partitions of the homogeneous wave of

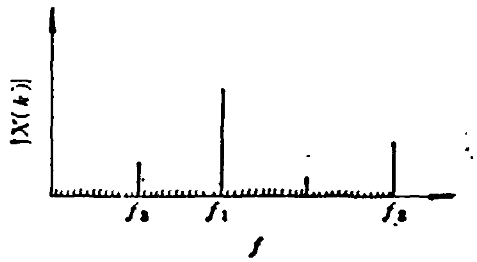


Fig. 9: Sinusoidal Fourier spectrum with three spectrum lines obtained through delta modulation DFT

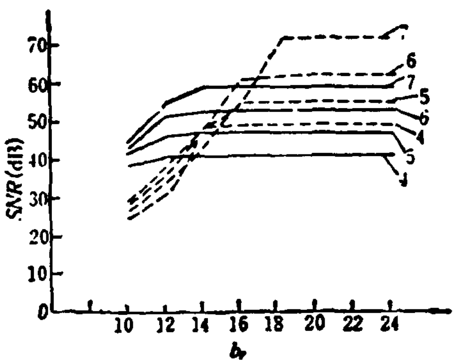


Fig. 10: Comparison of theoretical and simulated results of signal-to-noise ratio for b_q=4,5,6,7, and b_r>=10

f_s occurs at 0.75kHz. Figure 10 shows the effect on signal-to-noise ratio when b_q and b_r are with different word lengths. When, b_r>=18 and b_q=4, 5, 6, 7, the computer simulated result is greater than the theoretical predicted result by 10dB. This is because in the theoretical analysis, the input is assumed to be the white noise signal while in the simulation the input is the sinusoidal signal. However, we can also learn that when b_r>=18, each increment in b_q will result in the increase in signal-to-noise ratio by 6 to 10dB, which is very close to the theoretically predicted result.

When the input is Gaussian signal the optimal step size is difficult to determine. An empirical formulation for the determination of optimal step size is given in reference [8]. Figure 11(a) is the Gaussian signal spectrum of limit f_m=1kHz based on delta modulation DFT and 11(b) shows the Gaussian signal spectrum of limit f_m=1kHz based on ordinary DFT.

VII. Concluding Remark

The multiplier-free DFT based on DM proposed in this paper has similar characteristics as the FFT. Because of the major parts used are ROM and adder, the hardware realization is relatively easy. The theoretical analysis and computer simulation provided consistent results. Because of the limitation of ROM access speed, it can only be used in processing mainly speech and seismic signals.

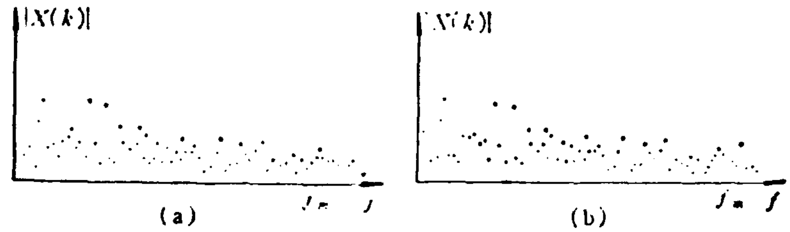


Fig. 11: (a) Limited 1kHz Gaussian signal obtained through delta modulation DFT and,

(b) Limited 1kHz Gaussian signal obtained through ordinary DFT

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