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Over the three-year course of this program, several issues in the device physics of resonant-tunneling diodes (RTDs) have been investigated, including the small-signal admittance, the shot noise, and the transport through multiple-quantum well structures. A large quantum-well inductance has been measured in the negative-differential-resistance region (NDR), but not in the positive-differential-resistance (PDR) region. The microwave shot-noise has been found to be suppressed relative to normal shot-noise in the PDR region, but enhanced in the NDR region. Triple-well RTDs have displayed a much wider NDR region in voltage than conventional single-well RTDs. Several new RTD material systems have been demonstrated including Type-II InAs/AlSb and Type-I GaSb/AlSb, the first of which has yielded excellent properties for high-speed device applications. Studies of highly lattice mismatched InAs/AlSb RTDs on GaAs substrates have proven that the RTD characteristics are insensitive to a high density of dislocations. Finally, these results have been incorporated into the design of RTDs in high-frequency oscillators and high-speed switches. The InGaAs/AlAs RTD has been optimized for application in a quasioptical fundamental-frequency oscillator operating above 200 GHz. The same material system has been used to make a low-power RTD load for heterojunction field-effect and bipolar transistors in high-performance digital integrated circuits.

14. SUBJECT TERMS

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1. INTRODUCTION

This is the final report for the program entitled "Physics and Technology of Resonant Tunneling," which was undertaken from May 1, 1989 through April 30, 1992. This program was designed to study the physics and technology of resonant-tunneling devices (RTDs) toward applications in high-frequency electronic circuits. When the program began, little was known about the ultimate frequency limits of these devices or their applicability in integrated circuits. Through the research carried out on this program, the RTD is now entering a stage of application in two key areas: (1) as a high-frequency fundamental oscillator, and (2) as a negative-resistance load in digital integrated circuits.

2. PROGRAM OBJECTIVES

The central objective of this program was to study the physics and to develop the technology of RTDs. In the three-year duration of the program, the plan was to investigate transport mechanisms and other issues relating to the device physics of the resonant-tunneling process, to develop new materials technology, and to incorporate the results into the design of RTDs. Significant progress has been made in each of these areas.

3. ACCOMPLISHMENTS

3.1. RESONANT-TUNNELING PHYSICS

In the area of resonant-tunneling physics, the small-signal admittance and microwave current fluctuations of double-barrier structures, as well as the transport properties of multiple-quantum-well (four-barrier) structures have been investigated.

3.1.1. Resonant-Tunneling Admittance

The small-signal admittance of an RTD has been measured in the negative-differential-resistance (NDR) and positive-differential-resistance (PDR) regions using a network analyzer. The measurements were carried out on specially designed double-barrier structures in the $In_{0.53}Ga_{0.47}As/AlAs$ materials system. This material system yields the highest room-temperature peak-to-valley current ratio (PVCR) of all known resonant-tunneling systems. The RTDs were grown with thick barriers so that the intrinsic time constants of the device - the quasibound-state lifetime and the RC time constant - were long enough to put the maximum oscillation frequency f_{max} well below the upper measurement limit of the network analyzer. However, the room-temperature PVCR (≈ 3.0) was sufficiently high that the electron transport through the structure was primarily by resonant tunneling. The cause of the low RC time constant is the low peak current density ($J_P \approx 100$ A cm^{-2}). The low J_P allowed the RTD to be stabilized against all oscillations in the NDR region, so that admittance measurement could be carried out in this region without confusion. A further discussion of the experimental technique is given in Appendix A.

To summarize the results, the admittance in the NDR region displayed an inductive nature consistent with the expression $L_{QW} \approx \tau_1/G$, where L_{QW} is the quantum-well inductance, G is the differential conductance, and τ_1 is the first quasibound-state lifetime. This expression was derived at Lincoln Laboratory in a previous program to explain anomalies in the RTD oscillator power. Surprisingly, the admittance in the PDR region did not display an inductive effect. This represents the first observation of the differing admittance characteristics in the NDR and PDR regions. A tentative explanation for this difference is as follows. In the PDR region below the current peak, the current arises from electrons that occupy traveling-wave states in the cathode region. Thus, the transmission probability for such electrons is described by the Breit-Wigner model, $T = [\Gamma^2/4]/[(E-E_1)^2 + \Gamma^2/4]$, where E is the electron longitudinal energy and E_1 is the first quasibound-state energy. Γ is the width factor given by $\Gamma_1 + \Gamma_S$, where Γ_1 is the intrinsic (or natural) width due to tunneling of the electron out of the quantum well, and Γ_S is the extrinsic width due to inelastic scattering. For the Breit-Wigner transmission probability the resonant-tunneling traversal time t_T is known to be $t_T \approx h/\pi(\Gamma_1 + \Gamma_S)$. In the present RTDs, $\Gamma_S >> \Gamma_1$, so that the traversal time is determined by the inelastic-scattering width. In contrast, the current in the NDR region arises from electrons emanating from occupied two-dimensional states in the accumulation layer on the cathode side. Because these states cannot form a wavepacket, the transmission from the accumulation layer through the quantum well is not given by the Breit-Wigner form. Instead, the experiments are consistent with a description by a resonant form that is much narrower in energy than Γ_S. The transmission width is probably much closer to Γ_1, so that the traversal time is of order $h/2\pi\Gamma_1$. The value of t_T deduced from the inductance measured in the NDR region is approximately 2 ns, compared to a theoretical value of 5 ns.

3.1.2. Current Fluctuations

In general, current fluctuations, or current noise, is of interest to device physicists for the following two reasons. First, the noise properties often reflect the underlying transport physics. Second, the noise properties often set absolute limits on the performance of devices such as amplifiers and oscillators. The research conducted on this program on the shot-noise of double-barrier RTDs has been illuminating in both respects. The measurements were carried out on oscillator-quality (f_{max} > 50 GHz) diodes at 1 GHz, which is well above the 1/f knee but well below f_{max}. The noise in the PDR region was measured by standard radiometric techniques. The noise in the NDR region was derived from the linewidth of the oscillating RTD. Measurements were made on several RTDs, including GaAs/AlGaAs and $In_{0.53}Ga_{0.47}As$/AlAs devices, and over a temperature range from 4.2 K to room temperature. The measurements are described further in Appendix B. All of the RTDs have shown shot-noise suppression in the PDR region and shot-noise enhancement in the NDR region. The enhancement in the NDR region is consistent with the relatively high noise figure, roughly 20 dB, that has been measured previously in RTD self-oscillating mixers. Fortunately, this noise is not so high as to hinder the application of RTDs as local oscillators for low-noise mixers, such as superconducting

tunnel junctions.

The shot-noise characteristics of RTDs are consistent with a mechanism called transmission modulation. The basis for this mechanism is that electrons stored in the quantum well during the resonant-tunneling process affect the potential drop across the RTD, thereby modulating the peak energy of the transmission function through the structure. The reason for the opposite shot-noise deviations in the PDR region (below the current peak) and the NDR region (above the current peak) is the sharply resonant nature of the transmission function. The theoretical analysis of these deviations is carried out in the accompanying manuscript of Appendix C.

3.1.3. Superlattice Resonant Tunneling

In the 1970s, interest in resonant-tunneling was driven by the desire to observe long-range coherent transport phenomena, such as Bloch oscillations in superlattice structures. In the interest of returning to this type of devices, a triple-quantum-well structure has been fabricated and tested. The idea behind this structure is to grade the width of the quantum wells between the cathode and anode side so that the first quasibound energy increases from well to well, as discussed in Appendix D. In this case the electron transmission at zero bias is very small because of misalignment of the energy levels. Under bias, the anode end of the structure drops in potential energy faster than the cathode end, so that the energy levels move towards coalignment. As this occurs, the electron transmission coefficient and the electrical current through the structure increase. When the levels approach a point of minimum separation (determined by the considerations of degenerate perturbation theory), the transmission coefficient and current will reach a maximum. At higher bias voltages, the transmission coefficient and current will both decrease leading to an NDR region.

The advantage of this type of RTD is that the NDR region is much broader in voltage than that of the conventional double-barrier RTDs. The double-barrier NDR region arises from the lowering of the transmission resonance below the occupied states on the cathode of the structure. Because the transmission resonance is always very sharp, the NDR region is narrow. The broader NDR voltage range of the graded quantum well yields a much higher oscillator power for a given load circuit. The graded quantum-well oscillator discussed in Appendix D has yielded five times the power of a double-barrier device.

3.2. DEVICE AND MATERIALS TECHNOLOCY

In the area of materials technology, advances have occurred in the understanding of existing resonant-tunneling materials and in the development of new material systems.

3.2.1. Type-II Resonant-Tunneling Diodes.

In work carried out in collaboration with Prof. Tom McGill's group at the California Institute of Technology (Caltech), RTDs were fabricated with InAs quantum well and cladding layers and AlSb barriers. InAs/AlSb has a type-II band offset, which means that the tunneling

electrons have an energy in the AlSb barriers that is much closer to the valence-band edge than to the conduction-band edge. As discussed in detail in Appendix E, this band alignment leads to an attenuation coefficient in the AlSb barrier that is about a factor of two smaller than in the AlAs barrier of a GaAs/AlAs structure. The result is a much higher peak current density for a given barrier thickness. For the barrier thicknesses of 1.5 and 1.8 nm that were tested, this leads to an increase in the peak current density by a factor of two or three. For example, the InAs/AlSb RTD having 1.5-nm-thick AlSb barriers displayed a J_P of 2.7×10^5 A cm^{-2} at room temperature. Because the PVCR of this diode is also very good, the available current density, ΔJ (the difference in the peak and valley current densities) was comparable to that of the best $In_{0.53}Ga_{0.47}As$/AlAs devices and far superior to the best GaAs/AlAs devices. The above InAs/AlSb RTD yielded $\Delta J \approx 2.1\times10^5$ A cm^{-2}, compared to about 0.5×10^5 A cm^{-2} in high-J_P GaAs/AlAs RTDs.

Further advantages of the InAs/AlSb material system are the low resistance and the favorable high-field transport properties of the InAs. The lower series resistance is due in part to the nearly ideal ohmic contact that can be formed to InAs. By transmission-line methods, the value of the specific contact resistance was estimated to be about 1×10^{-7} Ω cm^2. The high-field transport is far superior to that of GaAs or even $In_{0.53}Ga_{0.47}As$ because of the lower electronic effective mass in the Γ valley and because of the large energy separation ($\approx$ 1 eV) between the Γ valley and the next higher valley at the X point. The combination of these factors leads to a much higher electronic drift velocity across the depletion region of the RTD. For a given potential profile, the electronic drift velocity in a 50-nm-long depletion region is approximately 7×10^7 cm s^{-1} for InAs and 2×10^7 cm s^{-1} for GaAs.

3.2.2. Lattice-Mismatched Growth

A detailed study has been carried out of nominally identical InAs/AlSb double-barrier structures grown on InAs and GaAs substrates. The lattice mismatch between InAs and GaAs is 8%. The materials growths were carried out at Lincoln Laboratory following the initial demonstration of InAs/AlSb RTDs on GaAs substrates at Caltech. Details regarding the growth and characterization of the materials are given in the enclosed abstract and figures in Appendix F. X-ray diffraction and photoluminescence experiments indicated that the crystalline quality of the lattice-mismatched sample was far inferior to that of the lattice-matched sample. It was estimated that a large concentration of threading dislocations, $\sigma_D > 10^9$ cm^{-2}, permeated the double-barrier structure grown on the GaAs. However, dc electrical characterization showed little difference between the two samples. The peak current of the two samples was nearly identical, and the valley current of the lattice-mismatched sample was greater by only 20%.

The conclusion of the study was that a large concentration of threading dislocations does not significantly affect the peak current and only causes a small increase in the nonresonant excess current through these diodes. This opens up the possibility of fabricating narrow-bandgap, ultrahigh-speed, indium-bearing RTDs (and perhaps other unipolar devices, such as hot electron transistors) on GaAs substrates in integrated circuits. The difference in the valley

current of RTDs has little effect on the device performance, especially in oscillator applications. In fact, the InAs/AlSb oscillator results at 360 and 712 GHz that are discussed below were obtained with RTDs grown on GaAs substrates.

3.2.3. Low-Current-Density GaAs/$Al_xGa_{1-x}As$ RTDs

A detailed study has been carried out on the dc characteristics of GaAs/$Al_xGa_{1-x}As$ RTDs as a function of Al fraction x for x = 0.4 to 1.0 with increments of 0.1. The samples were grown using the most up-to-date MBE system at Lincoln Laboratory to ensure good control of Al fraction and the epitaxial growth rate (Varian Gen II with gas sources). The dc characterization indicated that for any given barrier thickness, a maximum PVCR occurs near x = 0.70. Preliminary theoretical analysis shows that the optimum Al fraction results from a competition between two excess current mechanisms. At low Al fractions, thermionic emission over the Γ-valley barriers dominates. At higher Al fractions, nonresonant tunneling proceeds via the X-point profile of the double-barrier structure.

In thin-barrier RTDs, the maximum PVCR at x = 0.70 is only marginally better than that at x = 1.0. However in thick barrier RTDs, the maximum at x = 0.70 is substantially greater than the PVCR at x = 1.0. In fact, for AlAs barrier thicknesses greater than about 3.0 nm, the PVCR vanishes completely. Thick-barrier RTDs are useful in applications that require low current density but do not require high speed. One such application is in a device developed recently at Lincoln Laboratory - the monolithic optoelectronic transistor. This device is the subject of Appendix G.

3.2.4. AlAs Barriers Beyond the Pseudomorphic Limit

Following the work in Sec. 3.2.3, it became apparent that dislocations arising from lattice mismatch between the barriers and cladding layers may not significantly degrade performance, just as is the case with dislocations arising from lattice mismatch to the substrate. To investigate barrier mismatch, two RTD samples were grown using $In_{0.53}Ga_{0.47}As$/AlAs, the combination of quantum well and barriers that has yielded superior performance. In this case, the AlAs barriers are approximately 4% mismatched to the $In_{0.53}Ga_{0.47}As$ cladding layers. With this mismatch, a single barrier should remain pseudomorphic up to a thickness of only about 3.5 nm. With this in mind, the barrier thicknesses of the two samples were chosen to be 4.4 and 5.5 nm, respectively. The room-temperature J_P of the two samples was approximately 150 A cm^{-2} and 1 A cm^{-2}, respectively. The PVCR of the two samples was approximately 3.0 and 1.5, respectively. The results support the conclusion that an increase in barrier thickness beyond the pseudomorphic limit causes a gradual but not critical degradation in the RTD characteristics. The reason for the gradual, rather than critical, degradation of RTD characteristics beyond the pseudomorphic limit is probably that dislocations in the barriers do not significantly affect the resonant-tunneling process. However, it is possible that the pseudomorphic limit as calculated for thick lattice-mismatched layers does not apply to thin hetero-barriers. This issue is presently under investigation.

3.2.5. GaSb-Based Resonant-Tunneling Structures

An RTD has been demonstrated for the first time in the GaSb/AlSb material system. An NDR effect was observed only at temperatures of 77 K and lower. It is thought that the absence of NDR at room temperature is caused by mixing between the Γ- and L-valley envelope states in the quantum well. With the application of uniaxial pressure, the two states separate, and a PVCR of approximately 2 is observed at 77 K. Theoretical models are presently being developed for multiple-valley resonant-tunneling structures. The understanding of these structures will be important for wide GaAs quantum-wells and for optoelectronic RTDs presently being designed in the GaSb/AlSb system.

3.3. RESONANT-TUNNELING DEVICES

In the area of RTD applications, progress has been made in the performance of RTD oscillators, and a useful application has been identified with the RTD used as the negative-resistance load to a high-speed transistor.

3.3.1. InAs/AlSb RTD Oscillators

The properties of the InAs/AlSb material system discussed in Sec. 3.2.1 are very beneficial in improving the performance of RTD oscillators. To demonstrate this, four waveguide oscillator circuits were constructed spanning the frequency range between 100 and 750 GHz. The experimental results are discussed fully in Appendix H. In the highest frequency waveguide circuit, the InAs/AlSb RTDs achieved room-temperature oscillations up to a frequency of 712 GHz, which is the highest oscillation frequency for any solid-state device at room temperature. The power at this frequency was roughly 0.2 μW. At a lower frequency of 370 GHz the power was approximately 3 μW and the power density was 80 W cm^{-2}, which is approximately 50 times that of GaAs/AlAs RTDs at the same frequency. These results were achieved with a 1.5-μm-diameter diode operating at room temperature. The power levels could be increased roughly 10 fold in the existing resonator by increasing the diameter of the diode to about 5 μm. The rolloff in power shown in Appendix H is consistent with the theoretical f_{max} of 1.3 THz calculated for this RTD using a generalized impedance model developed in a previous program.

3.3.2. $In_{0.53}Ga_{0.47}As/AlAs$ *RTD Switches*

At any given peak current density, the resonant-tunneling material system that displays the best PVCR is $In_{0.53}Ga_{0.47}As/AlAs$. $In_{0.53}Ga_{0.47}As/AlAs$ RTDs developed for this program typically have eight times higher PVCR than GaAs/AlAs RTDs and about three times higher PVCR than InAs/AlSb RTDs. This advantage is very important in the application of RTDs as switches in logic and memory circuits since low valley current corresponds to low static power dissipation. Analytic and numerical techniques have been used to calculate the switching speed of the $In_{0.53}Ga_{0.47}As/AlAs$ RTDs. The simplest technique is described in Appendix I. The conclusion of this analysis, as well as the more complex analyses, is that the fastest $In_{0.53}Ga_{0.47}As/AlAs$ RTDs will switch between the peak and valley points in less than 1 ps.

By comparison the best GaAs/AlAs diodes reported to date are limited to switching times of about 3 ps or higher when they are triggered without overdrive.

3.3.3. Quasioptical RTD Oscillator

A quasioptical oscillator has been developed to operate at frequencies above 100 GHz using the improved RTDs developed during this program. It is well known that conventional microwave resonators have a relatively low quality factor in this frequency region, which causes the FM-noise of any oscillator to become progressively higher with frequency. To solve this problem, the low-Q waveguide resonator used for the RTD demonstrations has been coupled to a very high-Q semi-confocal open resonator like those used in lasers. The quasi-optical oscillator was demonstrated in the frequency range 100 to 110 GHz using the most powerful $In_{0.53}Ga_{0.47}As$/AlAs RTDs. These results are discussed in detail in Appendix J. The major benefit is a reduction in the overall oscillator FM-noise linewidth by a factor of over 100 from approximately 1 MHz (for the waveguide oscillator alone) to 10 kHz (for the waveguide resonator coupled to the semi-confocal resonator). In addition, the oscillator is easily and precisely tuned by varying the length of the semi-confocal resonator. The oscillator output power is not significantly affected by coupling to the quasioptical resonator.

3.3.3. Planar RTD Slot Oscillator

A planar quasioptical oscillator has been demonstrated using the same operating principles as in the waveguide quasioptical oscillator discussed above. In the planar design, discussed in Appendix K, the RTD is part of a monolithic integrated circuit in which a low-Q slot resonator plays the role of the waveguide resonator. In principle the low-Q slot resonator, like the waveguide resonator, facilitates the start up of the oscillations. However, it yields a relatively noisy oscillator power spectrum and a broad antenna pattern. In the quasioptical oscillator, the slot resonator is locked on to the TEM_{00N} mode of the high-Q quasioptical resonator, thereby narrowing the line. The antenna pattern is also improved. This design was demonstrated in a 10-GHz scale model, and the desired frequency narrowing properties were observed. The key advantage of the planar approach over the waveguide is that it allows for a vast increase in the oscillator power by combining many RTD-slot N elements in a two-dimensional planar array. In this case, the frequency narrowing property of the high-Q resonator will act to synchronize all of the elements in the array and will thus provide an output power roughly N times that of a single element. In addition, the dc power will be distributed across the elements of the array, avoiding the thermal problems that have plagued high-power solid-state sources in the millimeter-wave region.

3.3.4. RTD Parallel Arrays

Another way to increase the power from the standard double-barrier RTD oscillator is to combine many diodes in parallel on chip to create an overall I-V characteristic with much higher peak current. This cannot be done with a single device because of destructive heating caused by the high current. The successful combination of 25 parallel diodes is discussed in Appendix L. This parallel array was used to obtain an output power of 5 mW at a frequency above 1 GHz.

3.3.5. RTDs as Loads in Digital Circuits

At the beginning of this program, there was a high level of interest in the resonant-tunneling transistor (RTT). Work at AT&T and Texas Instruments had led to a bipolar RTT showing the attractive property of negative transconductance. In previous programs, the effort at Lincoln Laboratory had been directed toward a unipolar RTT. The results were not encouraging. The first version of the unipolar RTT consisted of a standard double-barrier structure with an ohmic contact on the quantum well to form the base. This version proved very difficult to fabricate and was abandoned. The second version consisted of two double-barrier structures separated by a wide quantum well. The added width of the quantum well was thought to facilitate the formation of the base ohmic contact. However, it greatly hindered the transport between the emitter and the collector, resulting in poor current gain.

An alternative approach is to separate the double-barrier structure from the transistor and use it as a load for more conventional high-performance transistors. One advantage of this approach is that it allows the RTD to be used with either vertical or lateral transistors. In either case, it can operate with comparable speed but much lower static power than conventional (transistor-load) approaches. This approach also provides much greater noise margins. Numerical simulations have been carried out with the RTD acting as a load element for heterostructure field-effect transistors (HFETs) and heterojunction bipolar transistors (HBTs). The HFET results are summarized in Appendix M, and the HBT results are given in Appendix N. For the HFET/RTD configuration, the static power is approximately six times lower, the static noise margins are approximately three times higher, and the propagation delay is approximately twice that of conventional direct-coupled FET logic.

4. REVIEW ARTICLES

During the course of this program, several review articles have been written. The first, entitled "High-Frequency Applications of Resonant-Tunneling Devices", appears as Appendix O and concentrates on the microwave and millimeter-wave applications of RTDs. It includes several results not published anywhere else, such as experimental results of the RTD as a self-oscillating mixer. The second article, entitled "High-Frequency Resonant-Tunneling Oscillators," appears as Appendix P and focuses on the millimeter- and submillimeter-wave oscillator results. The third article, entitled "Resonant-Tunneling in High-Speed Double-Barrier Diodes," appears as Appendix Q. It emphasizes the physical principles of resonant tunneling and is designed to serve as a useful pedagogical introduction to resonant tunneling at the advanced-undergraduate or first-year-graduate level. The fourth article, entitled "High-speed resonant-tunneling diodes," appears as Appendix R. This article concentrates on device physics, particularly high-frequency effects. It includes several previously unpublished discussions of the effects of resonant-tunneling traversal time and depletion-layer transit time on the high-frequency performance of RTDs.

5. PROFESSIONAL PERSONNEL

Over the course of this program, the following personnel were involved to some degree in the research effort:

Name	Contribution
E.R. Brown	Resonant-tunneling device design, testing, and analysis.
T.C.L.G. Sollner	Device design and analysis.
C.D. Parker	Device packaging and high-frequency testing.
A.R. Calawa	Materials science and MBE growth.
M.J. Manfra	MBE growth.
W.D. Goodhue	MBE growth and fabrication.
S.J. Eglash	Materials science and Sb-based MBE growth.
C.L. Chen	RTD device fabrication.
K.M. Molvar	Device fabrication.

In addition, an MIT student, John Paul Mattia, carried out the research for a Master's thesis, entitled "AC Characterization and Modeling of Resonant-Tunneling Diodes," between the period December 1990 and September 1991. In June 1992, he was awarded an MIT Master of Science degree for this work.

6. INTERACTIONS

6.1. CONFERENCE PAPERS

The following is a list of papers given by the above personnel in the period 1 May 1989 through 30 April 1992 on subjects relevant to this program:

Authors	Meeting (Location, Date)	Title
Brown	Hot Electrons in Semiconductors (Tempe, AZ, July 1989)	"High-speed resonant tunneling"
Sollner, Brown, Parker, Goodhue	NATO Advanced Study Institute (Castera, France, Sept. 1989)	"High-frequency applications of resonant tunneling devices"
Brown, Parker, Calawa, Manfra, Sollner, Chen, Pang, Molvar	SPIE Symposium on High-Speed Electronics and Device Scaling (Newport Beach, CA, March 1990)	"High-speed resonant-tunneling diodes made from the $In_{0.53}Ga_{0.47}As$/AlAs material system"
Sollner, Brown, Parker, Goodhue	NATO Workshop on Resonant Tunneling (El Escorial, Spain, May 1990)	"High-frequency oscillators based on resonant tunneling"
Brown, Parker, Mahoney, Soderstrom, McGill	Device Research Conference (Santa Barbara, CA, June 1990)	"Room-temperature oscillations up to 675 GHz in InAs/AlSb resonant-tunneling diodes"
Sollner	GaAs IC Symposium (New Orleans, LA, Oct. 1990)	"Resonant-tunneling devices and circuits"
Sollner	Advanced Heterostructure Transistors (Kona, Hawaii, Dec. 1990)	"Resonant-tunneling devices and circuits"
Brown, Parker, Calawa, Manfra	Device Research Conference (Boulder, CO, June 1991)	"Low shot noise in high-speed resonant-tunneling diodes"
Brown, Hollis, Smith, Wang, Asbeck	International Solid-State Circuits Conference	"Resonant-tunneling-diode loads: speed limit

	(San Francisco, CA, Jan. 1992)	and applications in fast logic"
Sollner, Brown, Calawa, Chen, Fonstad, Goodhue, Mathews, Sage, Smith	Workshop on Quantum-Effect Physics (Cairo, Egypt, Jan. 1992)	"Resonant-tunneling diode circuits"
Brown, Parker, Molvar, Calawa, Manfra	NASA Space Terahertz Symposium (Ann Arbor, MI, March 1992)	"A quasioptical resonant-tunneling oscillator operating above 200 GHz"

6.2. UNIVERSITY AND INDUSTRIAL SEMINARS

Several university and industrial seminars have been given under the support of this program. All were on the subject of either high-speed resonant-tunneling diodes or the physics and technology of resonant tunneling. In each case, the host organization requested that the speaker emphasize specific technical aspects of resonant tunneling.

Speaker	Host Organization (Location, Date)	Technical Emphasis
Brown	AT&T Bell Labs (Murray Hill, NJ, June 1989)	Quantum-transport effects
Sollner	Caltech (Pasadena, CA, Feb. 1990)	RTD applications
Brown	Purdue University (Lafayette, IN, Nov. 1990)	In-bearing RTD structures
Sollner	Georgia Tech Univ. (Atlanta, GA, Nov. 1990)	RTD applications
Brown	Cornell University (Ithaca, NY, Jan. 1991)	Resonant-tunneling physics
Sollner	MIT (Cambridge, MA, Jan. 1991)	RTD applications
Sollner	Univ. of Illinois (Champaign, IL, April 1991)	RTD applications
Brown	Univ. Connecticut (Storrs, CT, Oct. 1991)	Resonant-tunneling noise
Brown	Tektronix (Beaverton, OR, Nov. 1991)	Resonant-tunneling switches
Brown	Univ. of Virginia (Charlottesville, VA, April 1992)	Resonant-tunneling transistors

6.3. COLLABORATIONS

Over the course of this program, the following collaborations have been established with organizations outside of MIT and Lincoln Laboratory:

Organization	Investigator	Research Project
Stanford Univ.	Prof. Jim Harris Dr. Edmund Wolak	RTD Modeling
Caltech	Prof. Tom McGill Dr. Jan Soderstrom	InAs/AlSb RTDs
Univ. of Massachusetts	Prof. Karl Stephan	Planar and high-power RTDs
Purdue University	Prof. Robert Gunshor	InSb/MnTe heterostructures
Rockwell Science Center	Dr. Peter Asbeck Dr. K.C. Wang	RTD loads for HFET and HBT integrated circuits
Northeastern University	Prof. Charles Surya	1/f noise in RTDs
U.C. Santa Barbara	Prof. Jim Allen	High-frequency planar RTDs
University of Virginia	Prof. Michael Shur Prof. Bill Peatman	A new approach to resonant-tunneling transistors

APPENDIX A

Draft

Small-Signal Admittance Measurement and Modeling of the Resonant-Tunneling Diode

J. P. Mattia, E. R. Brown, A. R. Calawa, and M. J. Manfra.

Abstract

An admittance measurement of a resonant-tunneling diode made from the $In_{0.53}Ga_{0.47}As/AlAs$ material system is presented. The admittance in the positive differential resistance (PDR) region is found to be only a weak function of frequency. In contrast, the admittance in the negative differential resistance (NDR) region is a strong function of frequency and is consistent with the presence of a quantum-well inductance. A coupled-quantum-well model is proposed to explain the difference between the behavior in the NDR and PDR regions.

Resonant-tunneling diodes (RTDs) have shown great promise in both high-speed switching [1] and high-frequency oscillator applications [2]. However, the speed of the RTD has made its small-signal characterization more difficult. In devices that are designed for high-frequency operation, significantly reduced values of peak-to-valley current ratio (PVCR) must be accepted in order to obtain stability in the NDR region. Previously reported admittance measurements have been taken from devices manufactured from the GaAs/AlGaAs material system. These devices have been either unstable in the NDR region with a high PVCR [3, 4, 5], or stable with no NDR [6]. In order to obtain stability with a high PVCR, we have fabricated low-current-density double-barrier RTDs made from the $In_{0.53}Ga_{0.47}As$/AlAs material system.

The $In_{0.53}Ga_{0.47}As$/AlAs RTDs were fabricated using molecular beam epitaxy on n^+-InP substrates. A 5000-Å-thick heavily doped (n-type, 2×10^{18} cm^{-3} Si) $In_{0.53}Ga_{0.47}As$ layer was grown first, followed by a 1000-Å-thick lightly doped (n-type, 2×10^{16} cm^{-3}) $In_{0.53}Ga_{0.47}As$ spacer layer. This spacer layer, which is on the anode side of the RTD, is designed to have a depletion-layer capacitance that is much smaller than the parallel-plate capacitance of the double-barrier structure. The double-barrier structure was then grown and consisted of undoped 45-Å-thick AlAs barriers and a 55-Å-thick $In_{0.53}Ga_{0.47}As$ quantum well. Above the double-barrier structure, a 100-Å-thick lightly doped (n-type, 2×10^{16} cm^{-3} Si) $In_{0.53}Ga_{0.47}As$ spacer layer was deposited followed by a final 4000-Å-thick layer of heavily doped (n-type, 2×10^{18} cm^{-3} Si) $In_{0.53}Ga_{0.47}As$ constituting the cathode of the device. Ohmic contact was made with a Pd/Ge/Au metallization sintered at 400°C for 30 s, and square mesas having an area of 64 μm^2 were defined by wet etching using the metal as a self-aligned mask. After fabrication, 250×250 μm dies were mounted in a

microwave coaxial package, and a mesa was contacted by a fine wire.

The admittance was obtained from one-port measurements of the reflection coefficient S_{11} using a network analyzer. Although data were obtained up to 10 GHz, all of the interesting features in the data occur below 900 MHz. S_{11} was measured with -30 dBm incident power (corresponding to a rf voltage amplitude of approximately 7 mV) and was converted into an equivalent admittance. An important aspect of the measurement is establishing the reference plane of the network analyzer. This calibration was carried out by using an $In_{0.53}Ga_{0.47}As/AlAs$ RTD from a separate wafer, identical in all respects to the device described above except that it had 55-Å-thick barriers. The lower conductance resulting from the thicker barriers of the device enabled the direct measurement of capacitance by a conventional LCR impedance bridge (HP 4275). At low biases, the capacitance of both the 45-Å- and 55-Å-barrier devices is nearly identical because it is primarily determined by the depletion-layer capacitances. Therefore, we chose the reference plane so that the high-frequency susceptance measured on the 45-Å-barrier devices at low bias was identical to that inferred from the impedance-bridge measurements of the 55-Å-barrier devices.

The current-voltage (I-V) curve of the 45-Å-barrier device at 300 K is shown in Fig. 1. The PVCR is 3.45, and the device is stable in the NDR region. In Fig. 2(a), the admittance is shown as a function of frequency for a bias voltage $V_T = 1.4$ V in the PDR region. The ac conductance agrees with the dc differential conductance from the I-V data to within a few percent. The conductance is practically independent of frequency up to 900 MHz, and this behavior was characteristic of all biases in the PDR region. The ac susceptance in Fig. 2(a) is linear with frequency and is equal to ωC_D, where $C_D = 0.19 \mu F\ cm^{-2}$ is the expected depletion-layer capacitance. From these plots, we conclude that the device admittance in

the PDR region is modeled quite well by a parallel connection of a resistor and capacitor.

The admittance in the NDR region is remarkably different. Figure 2(b) shows the admittance for V_T = 1.72 V. Below roughly 150 MHz, both the conductance and the susceptance increase rapidly with frequency. Above 150-200 MHz, the conductance and susceptance continue to increase, but much less rapidly. This behavior is consistent with the model of Brown *et al.* [7], shown in the inset of Fig. 2(b), in which a "quantum-well inductance" $L_{QW} = \tau/G$ is placed in series with the dc differential conductance G. Using the depletion approximation, the depletion-layer susceptance ωC_D in the NDR region is obtained by extrapolating the capacitive susceptance measured in the PDR region. This component is subtracted from the data in Fig. 2(b) and the remaining admittance is given by the solid curve in Fig. 3. Since this curve represents the series combination of L_{QW} and G as shown in the Fig. 3 inset, we compare the data to the expected admittance

$$Y_{QW} = \frac{G}{1 + i\omega\tau} = \frac{G}{1 + (\omega\tau)^2} + i\omega\frac{G\tau}{1 + (\omega\tau)^2}. \qquad (1)$$

The susceptance in this expression has a maximum at the frequency $\omega = 1/\tau$, which implies that τ = 1.6 ns for the solid curve in Fig. 3. This value of τ is comparable to the τ of 5 ns estimated from the coherent theory of resonant tunneling. Using τ = 1.6 ns and G as inferred from the I-V characteristic of Fig. 1, we obtain the dashed curve in Fig. 3. If we instead use a lower value of G that provides agreement between the maximum susceptance in (1) and the maximum measured susceptance, we find the dotted curve in Fig. 3. The discrepancy between the dashed and experimental curves is likely caused by the excess conductance from a leakage current mechanism in the diode, which is not accounted for in

the model described below.

In Fig. 4 we plot the susceptance for several biases around the peak voltage of 1.70 V. The capacitive susceptance has again been subtracted from the measured admittance for each curve. For each bias, the vertical scale is the same but the origin has been offset for clarity. Since the frequency of the susceptance peak occurs at $1/(2\pi\tau)$, we can conclude from the data in Fig. 4 that the effective lifetime is changing rapidly with bias in the NDR region.

We can qualitatively explain the dramatic difference between the PDR and NDR regions. Under large applied bias, there are two quantum wells present in the active region of the device. One is the double-barrier quantum well (DBQW). The other is an accumulation-layer quantum well (ALQW) that exists on the cathode side. Though separated by a thick barrier, the two wells are coupled, and we must consider the quasibound-state energy and probability density in both wells to understand the electron transport. Shown in Fig. 5 is a model of the coupled quantum wells with a bias in the NDR region. For simplicity, we have assumed that there is only one quasibound state associated with each quantum well. The two lowest states have energies E_1 and E_2 and associated wavefunctions ψ_1 and ψ_2. The conduction-band edge in the neutral cathode and neutral anode are denoted by E_C and E_A respectively. Not depicted in the figure are the extended states in the cathode, which we denote by ψ_C.

In the PDR region, $E_2 > E_C$ and $E_1 < E_C$. The state with energy E_1 roughly corresponds to an accumulation-layer state that would occur in the presence of a thick single barrier. A numerical calculation of ψ_1 [8] indicates that this state has a high amplitude in the ALQW but practically no amplitude in the anode region, so that electrons occupying E_1 have a

low probability of tunneling out. The next state, ψ_2, is a traveling wave in the cathode and anode, although most of its probability density concentrated in the DBQW. In the PDR region, resonant tunneling proceeds through this level and is directly affected by scattering. If we assume that the scattering is characterized by a perturbation Hamiltonian H', then the transition rate from ψ_C to ψ_2 is proportional to $|\langle\psi_2|H'|\psi_C\rangle|^2$ according to Fermi's Golden Rule. This rate is potentially very fast, since both ψ_C and ψ_2 have significant amplitude over the entire cathode region. Thus, electrons in states that only had a small probability of transmission in the absence of scattering can have a large probability in the presence of scattering. As a result, the transmission function is broadened in energy, which is consistent with previous models of incoherent resonant tunneling [9, 10]. From the uncertainty principle, the lifetime of the state, τ, is inversely related to the width of the transmission resonance. Therefore, the inductive component is greatly diminished in the PDR region, assuming that L_{QW} remains proportional to τ.

In the NDR region E_2 drops below E_C, and ψ_1 and ψ_2 interchange character, as depicted in Fig. 5. In this case, ψ_1 is localized in the DBQW and ψ_2 is localized in the ALQW. For this bias, ψ_1 has some probability of tunneling into the anode, while ψ_2 has practically no probability. The matrix element $\langle\psi_1|H'|\psi_C\rangle$ will be fairly small, since the two wavefunctions are localized in different regions. The small matrix element implies that the $\psi_C \rightarrow \psi_1$ transition is relatively slow. There is an alternative mechanism that involves two transitions. Since ψ_2 has a higher probability density in the accumulation layer, the $\psi_C \rightarrow \psi_2$ transition is faster than the $\psi_C \rightarrow \psi_1$ transition. However, since ψ_2 has a small probability density in the anode, electrons must make another transition to ψ_1 before tunneling into the anode. The rate of the second transition is proportional to $|\langle\psi_1|H'|\psi_2\rangle|^2$. Since the matrix elements

for both the one- and two- step processes are likely to be less than the matrix element of the dominant transition in the PDR region, $|\langle\psi_2|H'|\psi_C\rangle|^2$, we expect that the effective lifetime should be much longer in the NDR region. The change in the time constant observed in Fig. 4 could be explained either by the voltage dependence of the wavefunctions or by a voltage dependence of a perturbation Hamiltonian.

In conclusion, we have measured the small-signal admittance of a thick-barrier $In_{0.53}Ga_{0.47}As/AlAs$ RTD. We found that the admittance of the RTD in the PDR region has only a weak dependence on frequency. In contrast, the admittance in the NDR region has a strong frequency dependence and was accurately modeled by a series combination of an inductance and conductance, both in parallel with a capacitance. We have qualitatively explained these results in terms of a coupled-quantum-well model.

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References

[1] J. F. Whitaker, G. A. Mourou, T. C. L. G. Sollner, and W. D. Goodhue, "Picosecond switching time measurement of a resonant tunneling diode," *Appl. Phys. Lett.*, vol. 53, p. 385, 1988.

[2] E. R. Brown, J. R. Söderström, C. D. Parker, L. J. Mahoney, K. M. Molvar, and T. C. McGill *Appl. Phys. Lett.*, vol. 58, p. 2291, 1991.

[3] J. M. Gering, D. A. Crim, D. G. Morgan, P. D. Coleman, W. Kopp, and H. Morkoç *J. Appl. Phys.*, vol. 61, p. 271, 1987.

[4] D. Lippens and P. Mounaix, "Small-signal impedance of GaAs-$Al_xGa_{1-x}As$ resonant tunnelling heterostructures at microwave frequency," *Electron Lett.*, vol. 24, p. 1180, 1988.

[5] R. E. Miles, G. Millington, R. D. Pollard, D. P. Steenson, J. M. Chamberlain, and M. Henini, "Accurate equivalent circuit model of resonant tunneling diodes," *Electron Lett.*, vol. 27, p. 427, 1991.

[6] J. Genoe, C. V. Hoof, W. V. Roy, J. H. Smet, K. Fobelets, R. P. Mertens, and G. Borghs, "Capacitances in double-barrier tunneling structures," *IEEE Transactions on Electron Devices*, vol. 38, p. 2006, 1991.

[7] E. R. Brown, C. D. Parker, and T. C. L. G. Sollner, "Effect of quasibound-state lifetime on the oscillation power of resonant tunneling diodes," *Appl. Phys. Lett.*, vol. 54, p. 934, 1989.

[8] J. P. Mattia, "Sm thesis, mit, department of eecs,"

[9] A. D. Stone and P. A. Lee, "Effect of inelastic processes on resonant tunneling in one dimension," *Phys. Rev. Lett.*, vol. 54, p. 1196, 1985.

[10] M. Jonson and A. Grincwajg, "Effect of inelastic scattering on resonant and sequential tunneling in double barrier heterostructures.," *Appl. Phys. Lett.*, vol. 51, p. 1729, 1987.

Figure Captions.

Figure 1. Current density (solid-curve) and dc conductance (dashed curve) as a function of bias voltage. The two dots on the solid curve at 1.4 V and 1.72 V illustrate the bias points for the measurements of Fig. 2.

Figure 2. Conductance (solid) and susceptance (dashed) as a function of frequency. (a) PDR, bias voltage = 1.4 V. (b) bias voltage = 1.72 V. The complete equivalent circuit model is shown in the inset.

Figure 3. Susceptance curves for a bias voltage of 1.72 V. The solid line is the measured data of Fig. 2(b) after subtraction of the depletion-layer susceptance. The equivalent circuit model is shown in the inset. The dashed line uses the dc conductance in the model, and the dotted line uses a conductance which results in a modeled maximum susceptance value equal to the measured value.

Figure 4. Measured susceptance curves after subtraction of the depletion-layer susceptance for several biases around the peak voltage 1.70 V.

Figure 5. Coupled-quantum-well model for the RTD biased in the NDR region. E_1 and E_2 are the two lowest quasibound levels. E_C and E_A are the conduction-band edges in the neutral cathode and anode regions respectively.

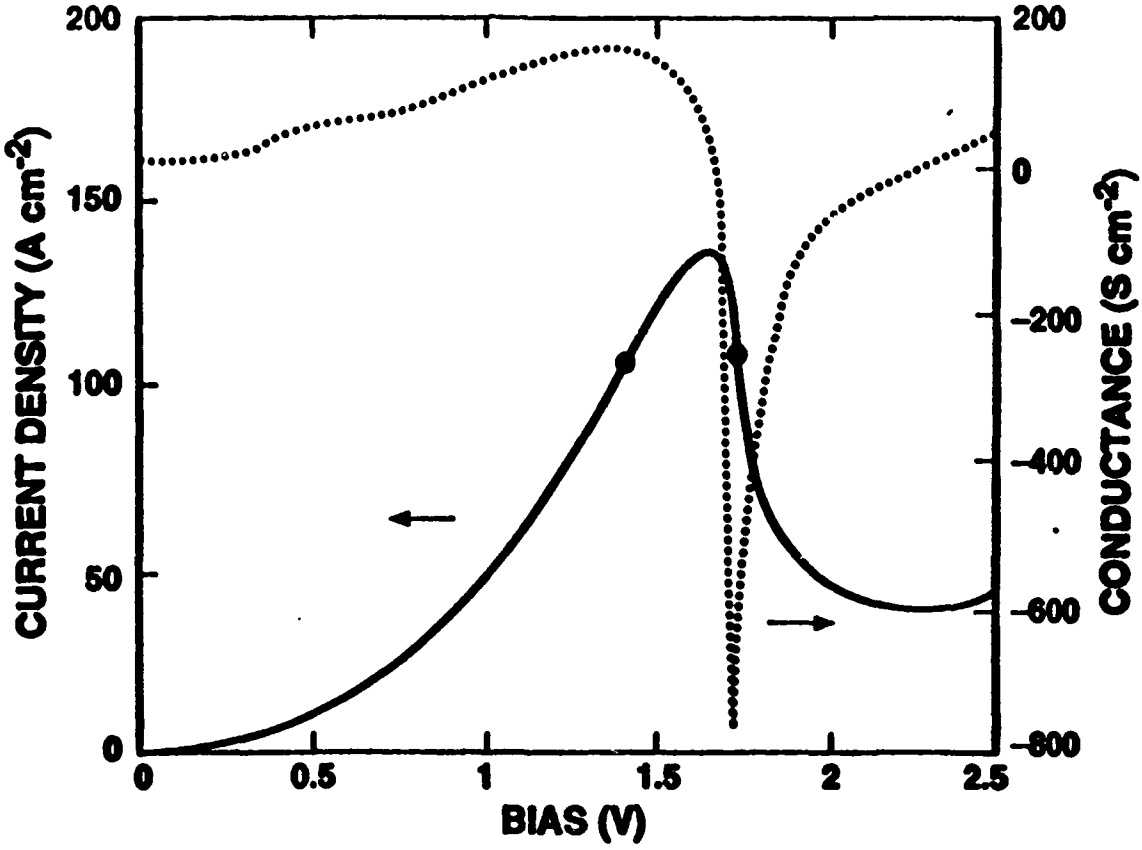
200
150
100
50
0
CURRENT DENSITY (A cm-2)
200
0
-200
-400
-600
-800
CONDUCTANCE (S cm-2)
0
0.5
1
1.5
2
2.5
BIAS (V)

FIG. 1

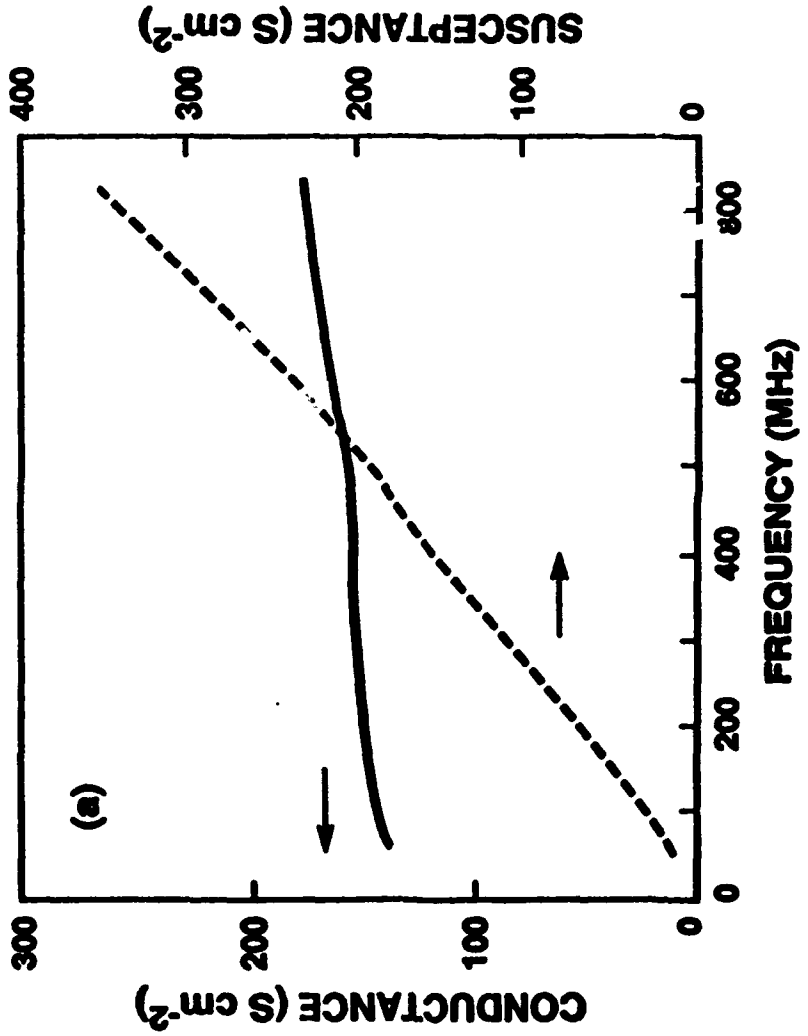
SUSCEPTANCE (S cm⁻²)
400
300
200
100
0
800
600
400
200
0
FREQUENCY (MHz)
(a)
300
200
100
0
CONDUCTANCE (S cm⁻²)

FIG. 2(a)

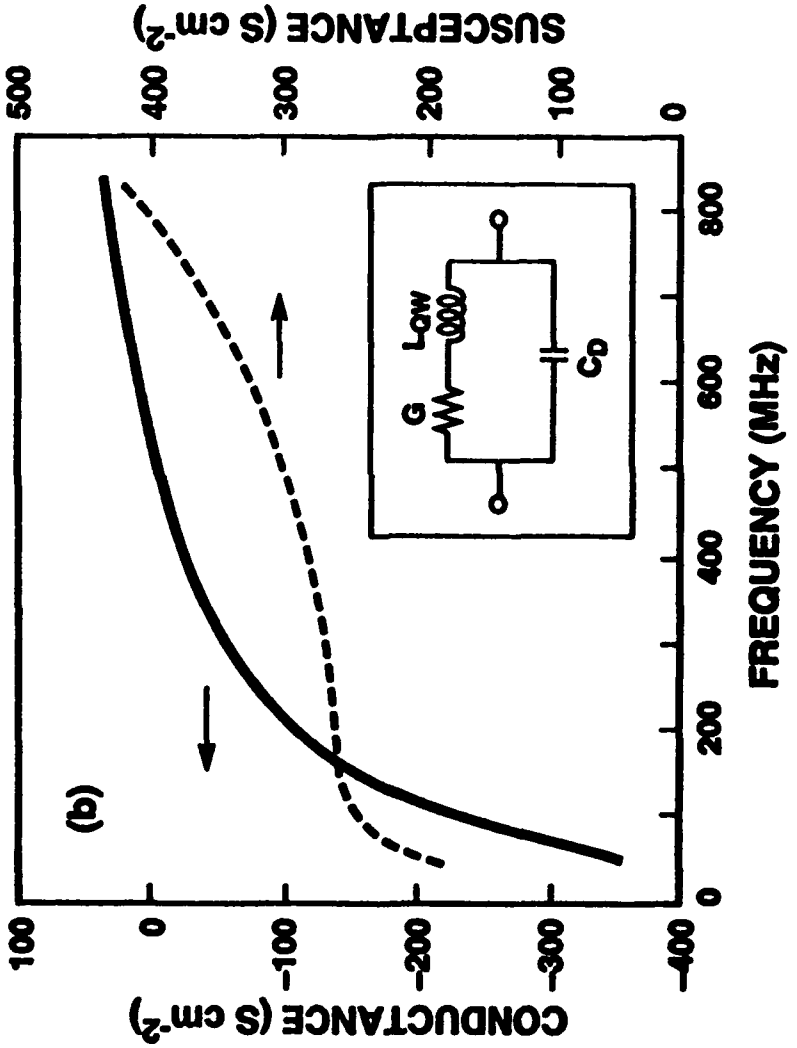
SUSCEPTANCE (S cm⁻²)
500
400
300
200
100
0
800
600
400
200
0
FREQUENCY (MHz)
100
0
-100
-200
-300
-400
CONDUCTANCE (S cm⁻²)
(b)
G
L_GW
C_D

FIG. 2(b)

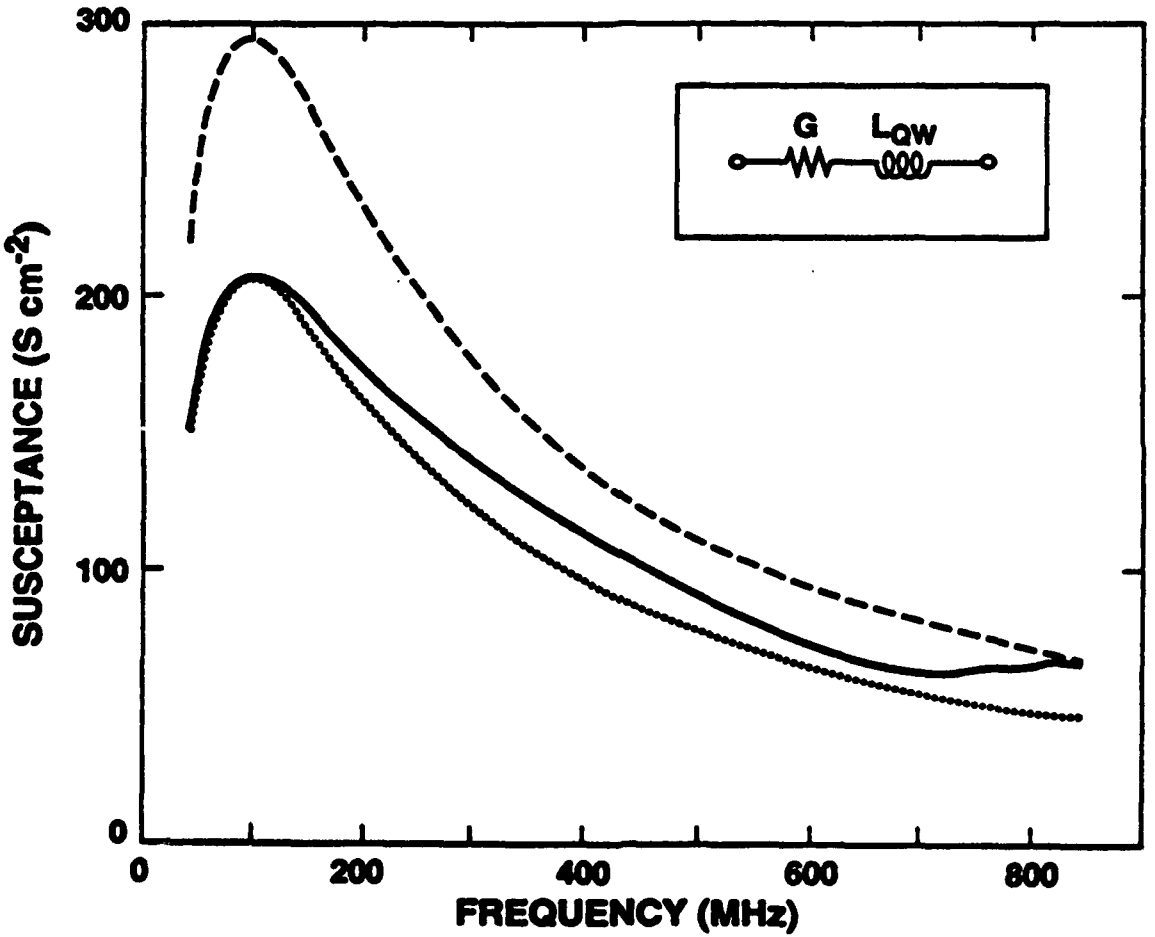
300
200
100
0
SUSCEPTANCE (S cm^{-2})
0
200
400
600
800
FREQUENCY (MHz)
G
L_{QW}

FIG. 3

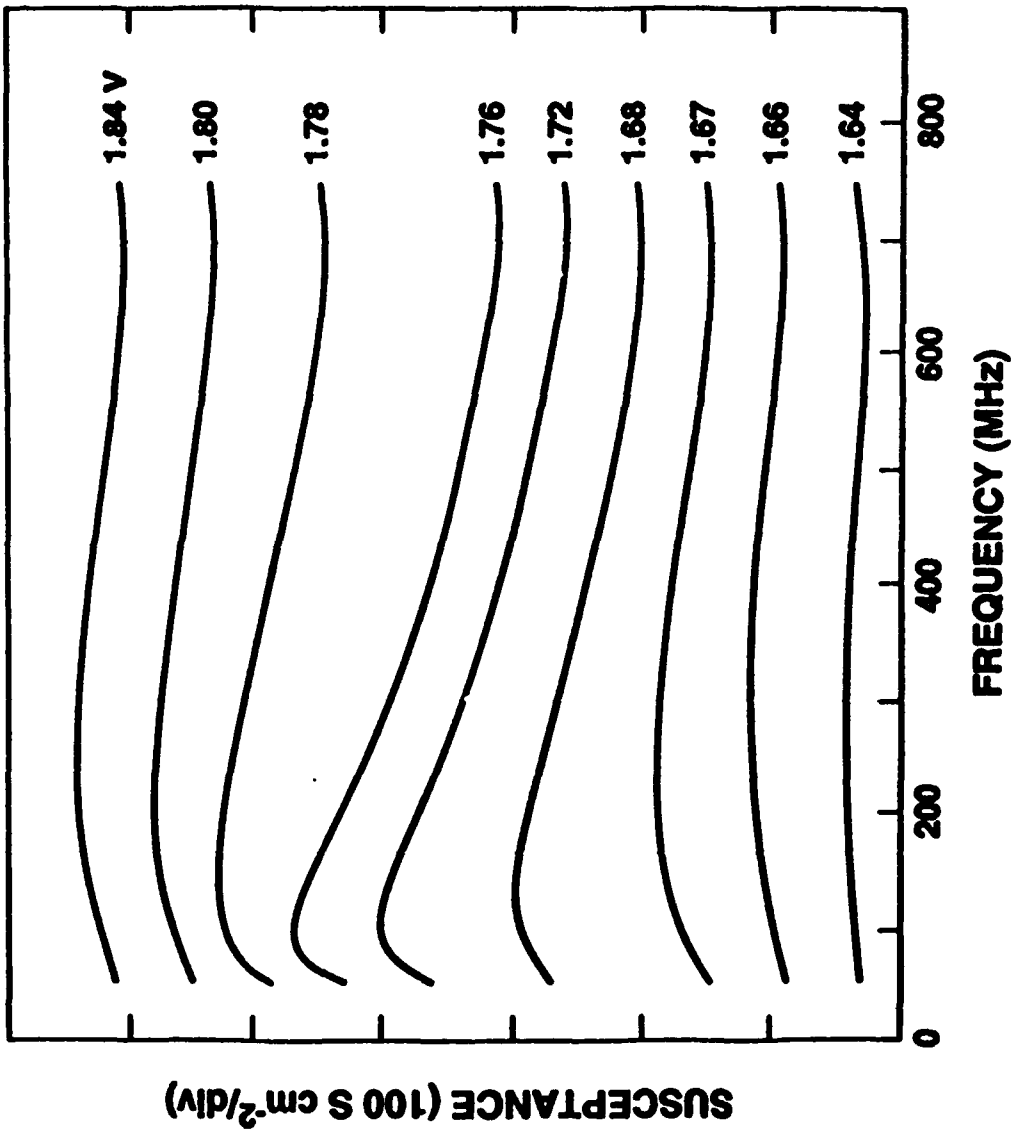
1.84 V
1.80
1.78
1.76
1.72
1.68
1.67
1.66
1.64
0
200
400
600
800
FREQUENCY (MHz)
SUSCEPTANCE (100 S cm⁻²/div)

FIG. 4

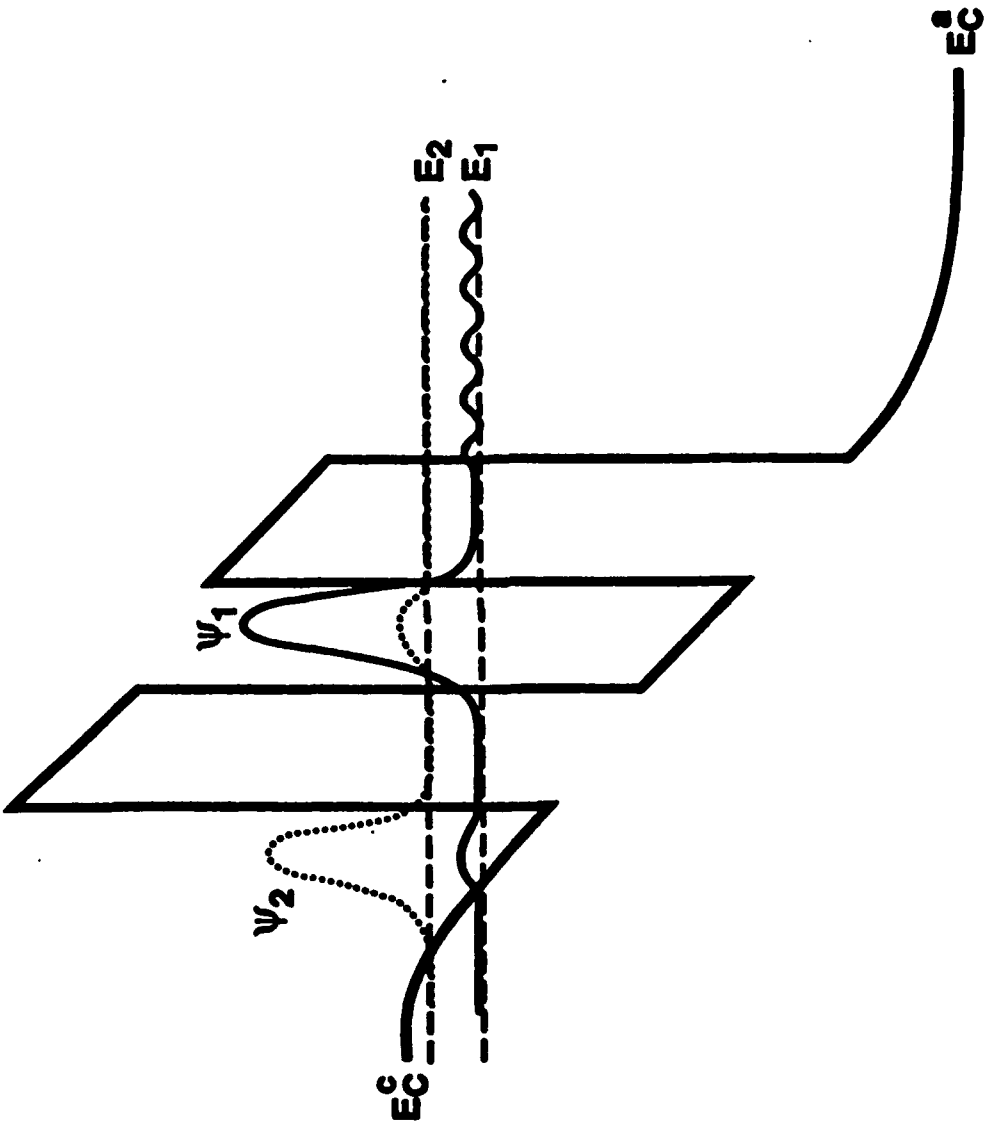

FIG. 5

We have fabricated a variety of planar coupled quantum wires with different lengths and widths using electron-beam lithography on a AlGaAs/GaAs MODFET structure ($N_s \approx 7 \times 10^{11}$ cm^{-2} and $\mu \approx 170{,}000$ cm^2/V · s at 4 K). The key feature in these devices is the 30-nm-wide middle gate fabricated using a single-pass e-beam lithography technique. The middle gate is widened outside of the coupled region to prevent interaction in the extrinsic device. Device processing consists of mesa isolation, ohmic contact formation to allow individual access to the input and output of each wire, and a combination of UV and e-beam lithography for gate formation.

The coupled quantum wires have been characterized at 300 and 4 K. By monitoring the current through the various terminals, we have identified the regime in which two quantum wires are formed. Controlling the middle gate voltage, we can vary the level of interaction of the two wires, from complete isolation to merging into a very wide wire whose boundaries are the side gates. At low temperatures, we observed conductance steps in each wire separately at $T = 1.7$ K, confirming quasi-ballistic 1D transport ($L = 0.5$ μm). We then biased the middle gate so as having the two quantum wires separated by a narrow tunneling barrier. Current from one wire to the other was studied in a configuration in which the device is essentially an FET with a quantized 1D source and drain. We observed strong oscillations in the current transversing the middle gate as a function of the drain wire. The oscillations disappeared at high V_{DS} ($\cong 1$ mV), high temperatures ($\cong 10$ K), and for very negative middle gate biases, indicating that this is a tunneling current whose features might derive from the 1D density of states structure of the drain.

In summary, we have fabricated for the first time two planar quantum wires, whose coupling can be controlled through the field-effect action of a gate. Our split-gate coupled wire scheme provides a new architecture to study electron interaction in low-dimensionality systems. This work might lead to the conception of new electron devices with enhanced functionality.

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[1] van Wees *et al.*, *Phys. Rev. B*, vol. 60, p. 848, 1988.
[2] Wharam *et al.*, *J. Phys. C*, vol. 21, p. L209, 1988.
[3] Eugster *et al.*, in *DRC 1990*.
[4] del Alamo *et al.*, *Appl. Phys. Lett.*, vol. 56, p. 78, 1990.

VB-2 Avalanche Electron Emitter Arrays Using Si Ultra-Shallow p-n Junctions—Jung Y. Ea*, Yicheng Lu, Dazhong Zhu**, and B. Lalevic, Department of Electrical and Computer Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855; Robert J. Zeto, U.S. Army, Electronics Technology and Devices Laboratory, Fort Mommouth, NJ 07703.

Recently, vacuum microelectronic devices have been studied intensively in order to overcome the transit-time limitations while keeping all the advantages of silicon integrated circuits. In this abstract we report a silicon avalanche electron emitter array using ultra-shallow p-n junctions biased in the avalanche region.

The devices were fabricated on a p^- epilayer grown on p^+ substrates. The p^+ region formed in the top of the p^- epilayer defines the cold-cathode pattern. The ultrathin n^{++} layer forms a shallow p-n junction and a current channel connecting the cathode and the contact. Different size's cathodes with diameters ranging from 5-40 μm and different shapes of single cathodes and arrayed cathodes were fabricated. Under a vacuum of 3×10^{-9} torr the emission current was collected by applying positive voltage to the external anode which was located about 1 mm above the cathode. With larger area cathodes the emission current is confined to the perimeter region of the cathodes. As the diameter decreases to 5 μm, the emission approached uniformity. The emission current was investigated as a function of reverse bias, anode collecting voltage, cathode diameter, and number of arrayed single cathodes simultaneously biased. The electron emission starts with the onset of avalanche breakdown. At the fixed anode voltage, the emission current increases linearly with increasing reverse-bias voltage of the diode until it reaches the peak. With further increase in the bias voltage, emission current decreases. This can be attributed to the current-crowding effect. The emission current initially increases with increasing anode voltage, in agreement with the Langmuir-Child Law. It saturates at higher anode voltages, corresponding to the electric field intensity of $\sim 2 \times 10^5$ V/cm for the 40-μm-diameter cathode. Without optimization of the device parameters, an emission current of 0.7 μA was obtained from a single cathode with a 40-μm diameter. The emission current from eight, 5-μm diameter, arrayed cathodes shows a peak emission current of ~ 230 nA, while the magnitude of the emission current for a single cathode at the same reverse-biased condition is about 30 nA. Therefore, the emission current was multiplied by the number of single cathodes arrayed together.

We have demonstrated the prototype of silicon cold cathodes for vacuum microelectronics, which contains the following features: i) fabrication is compatible with IC technology; ii) it can be integrated and arrayed to produce large current from a small chip area without the cesiation of the cathode; iii) by using on-chip polysilicon cantilever beam anode, the device shall be able to operate at low voltages (~ 5 V). The most promising applications include flat panel displays with high current density and brightness; as an electron source for scientific instrumentation; as an electron source in microwave applications, which requires a long and thin rectilinear electron beam. The fabrication of the complete device, including vacuum microelectonic diodes and triodes, is in progress. The results will be reported at the conference.

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VB-3 Low Shot Noise in High-Speed Resonant-Tunneling Diodes—E. R. Brown, C. D. Parker, A. R. Calawa, and M. J. Manfra, Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173-9108.

Resonant-tunneling devices provide benefits in performance and functionality. For example, the resonant-tunneling diode (RTD) has provided an oscillation frequency above 700 GHz, the bipolar resonant-tunneling transistor has demonstrated negative transconductance, the resonant-tunneling hot-electron transistor has demonstrated a unity-current-gain cutoff frequency f_T over 100 GHz, and the quantum-well injection and transit-time (QWITT) diode offers the capability for much higher power than the RTD oscillator. The building block of each of these devices is the double-barrier heterostructure. This paper presents experimental and theoretical results on microwave shot noise in high-speed double-barrier RTD's. We find that the room-temperature shot noise per unit current can be more than a factor of two lower than in single-barrier structures (e.g., p-n junctions) when the RTD is biased into the positive differential resistance (PDR) region below the current peak, but is increased when biased into the negative differential resistance (NDR) region. The analysis suggests that the reduced shot noise could also be obtained in other double-barrier resonant-tunneling

devices that operate in the PDR region, such as the resonant-tunneling transistors and the QWITT oscillator. Reduced shot noise can lower the noise figure of amplifiers, narrow the linewidth of oscillators, and decrease the error rate in logic circuits.

In general, shot noise is characterized by the power spectral density $S_I = 2\Gamma e I_0$, where I_0 is the dc bias current and Γ is the shot-noise factor. For single-barrier devices, $\Gamma = 1.0$. We have carried out shot-noise measurements to determine Γ in three different RTD structures. The first is a GaAs/$Al_{0.42}Ga_{0.58}As$ RTD having a room-temperature peak current density J_p and peak-to-valley current ratio (PVCR) of 1×10^4 A cm^{-2} and 3.8, respectively. The remaining two are $In_{0.53}Ga_{0.47}As$/AlAs RTD's having a room-temperature J_p of 3×10^4 and 2×10^5 A · cm^{-2}, and a PVCR of 12 and 5, respectively. In the PDR region, the noise spectral density was measured by radiometric techniques at a frequency of 1.0 GHz. This frequency was far above the $1/f$ knee and far below the RC cutoff frequency. In all three devices, $\Gamma < 1.0$ in the PDR region below the current peak. The GaAs/AlGaAs and the high-J_p InGaAs/AlAs RTD's displayed a minimum Γ of approximately 0.45 at room temperature. The low-J_p InGaAs/AlAs RTD displayed a minimum Γ of 0.73 at room temperature. In the NDR region, the shot noise was determined indirectly from the phase-noise linewidth of the RTD operating as a microwave oscillator. At one point in the NDR region of the GaAs/AlGaAs RTD, $\Gamma = 5$ was measured at room temperature. In spite of this fact, the linewidth of the RTD oscillator at a given frequency is less than that of a Gunn-diode oscillator and much less than that of an IMPATT-diode oscillator.

The deviations from $\Gamma = 1.0$ occur because the resonant-tunneling current in a double-barrier structure is self-modulated. By this mechanism, sheet charge accumulates in the quantum well in proportion ot the current density. The sheet charge affects the potential across the double-barrier structure and shifts the transmission function, thereby modulating the RTD current. A theoretical model will be presented that agrees with the experimentally observed short-noise effects, and predicts that RTD's can be designed with further reduced Γ in the PDR region. This is the first study of microwave shot noise in RTD's.

*This work was sponsored by the Air Force Office of Scientific Research.

VB-4 RF Response of High RF-T_C SNS Josephson Microbridges Suitable for Integrated Circuit Applications—R. H. Ono, J. A. Beall, M. W. Cromar, T. E. Harvey, M. E. Johansson, C. D. Reintsema, and D. A. Rudman, Electromagnetic Technology Division, National Institute of Standards and Technology, Boulder, CO 80303.

We have developed a simple process for microfabricating high transition temperature superconductor-normal metal-superconductor (SNS) Josephson devices which operate up to 80 K, and are reasonably ideal at 43 K. Bridge resistances greater than 10 Ω and critical current-normal state resistance (I_CR_N) products greater than 1 mV have been achieved. Clearly defined RF steps have been observed, with power dependence qualitatively similar to theoretical predictions. The fabrication process and the device characteristics are suitable for superconducting integrated circuit applications such as millimeter-wave Josephson oscillators, parametric amplifiers, and single-flux quantum digital logic.

We have used a step-edge technique with *in situ* deposition of both the superconductor and normal metal to make very short SNS microbridges. The superconductor, $YBa_2Cu_3O_{7-\delta}$, is deposited by pulsed laser ablation at an angle onto a substrate which has a nearly vertical step, allowing shadowing from the step edge to create a break in the superconductor. The normal metal is then deposited from the other direction so as to cover the step and bridge the superconducting banks. The length of the bridge is defined by the step height and thus can be made very short. To ensure the lowest possible contact resitance between the superconducting and normal metal films, we deposit the normal metal without exposure to air (*in situ*). This technique also allows the normal metal to contact the exposed edges of the c-axis-oriented films, producing a low boundary resistance a–b plane contact. Once the YBCO-normal metal bilayer is completed, the lateral device dimensions are patterned using a positive photoresist and ion milling.

We have used both pure Ag and a Ag–Au alloy as the normal metal link. The alloy typically had a low-temperature resistivity 5–10 times higher than the pure noble metal. The resistances of the Ag bridges were typically 1 Ω or less, whereas those of the alloy bridges were usually over 10 Ω. As predicted by boundary conditions from the standard SNS model [1], the high-resistance alloy bridges showed a higher I_CR_N than the pure Ag bridges.

The voltage-current (V-I) characteristics of these devices are similar to those predicted by the resistively shunted junction (RSJ) model [2], as opposed to the rounded, nonlinear V-I curve due to flux flow resistance. We also observe RF-induced steps at voltages of $nh\nu/2e$ to beyond $n = 20$, even at 43 K, and steps are still clearly defined at 78 K. The amplitude of the step size modulates with increasing RF power, as predicted by the RSJ model. The RF power modulates the zeroth and first steps over more than six periods, with the interval between zeros found to agree with RSJ-based predictions [3] within a factor of 2.

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[1] M. Yu. Kupriyanov, and K. K. Likharev, *IEEE Trans. Magn.*, vol. 27, p. 2460, 1991.
[2] K. K. Likharev, *Rev. Mod. Phys.*, vol. 51, p. 101, 1979.
[3] K. K. Likharev and V. K. Semenov, *Radio Eng. Electron. Phy.*, vol. 16, p. 1917, 1971.

VIA-1 Effects of Substrate Tilting in Substantial Improvement of DC Performance of AlGaAs/GaAs n-p-n DHBT's Grown by MBE—Naresh Chand, Paul R. Berger, and Niloy K. Dutta, AT&T Bell Laboratories, Murray Hill, NJ 07974.

We observe a marked improvement in the dc performance of $Al_{0.3}Ga_{0.7}As/GaAs/Al_{0.3}Ga_{0.7}As$ double heterojunction bipolar transistors (DHBT's) by tilting the (100) GaAs substrates 3° towards ⟨111⟩A. On the tilted substrate, the surface, space charge and bulk recombination currents are reduced, and the quality of AlGaAs/GaAs heterointerfaces is improved. As a result, both the emitter injection efficiency (η) and base transport factor are increased leading to a substantial increase in current gain with a marked reduction of its current and junction geometry dependence, as shown in Table I.

The structures studied were grown simultaneously at 580°C on Si-doped n^+-GaAs flat (100) and misoriented substrates. A compositional grading of 300 Å was employed at the emitter-base (e-b) junction. The base-collector (b-c) junction was not graded to see the effect of an abrupt junction on the offset voltage and gain. The

APPENDIX C

Analytic model of shot noise in double-barrier resonant-tunneling diodes

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ABSTRACT

The shot noise in double-barrier diodes is analyzed using the stationary-state approach to resonant tunneling through the first quasibound level. Significant deviations from full shot noise are predicted. Shot-noise suppression occurs in the entire positive differential resistance region below the current peak, and shot-noise enhancement occurs in the negative differential resistance region above the peak. The physical basis for these effects is assumed to be the modulation of the double-barrier transmission probability by charge stored in the first quasi-bound level in the quantum well. The analysis confirms recent microwave noise measurements of high-speed double-barrier diodes.

I. INTRODUCTION

Shot noise is a type of fluctuation in the electrical current that is observed in many electronic devices operating out of thermodynamic equilibrium. In most cases it is associated with randomness in the flux of carriers crossing the depletion layer of a device. The source of this randomness is thermal fluctuations in the rate of carrier injection into the depletion layer. At frequencies small compared to the reciprocal of the transit time through the depletion layer, the power spectral density of such shot noise is given by $S_I = 2e\gamma I$, where I is the dc current, e is the magnitude of the electronic charge, and γ is the shot-noise factor [1]. In the majority of devices it is found that $\gamma = 1.0$, which is the condition of normal, or full, shot noise. Some examples are p-n diodes, metal-semiconductor (Schottky) diodes, and semiconductor heterobarrier diodes. In all of these devices the electrical current is limited by a potential energy barrier whose transmission characteristics are independent of the current magnitude. In devices having a barrier whose transmission depends on the current, significant deviations from full shot noise can occur. The classic example is the space-charge-limited vacuum diode in which the barrier consists of a spatial distribution of electrons located near the cathode [2]. A more recent example is the resonant-tunneling diode (RTD), in which significant shot-noise suppression [3,4,5,6] and shot-noise enhancement [6] have been observed.

The purpose of this paper is to demonstrate analytically how the quantum-well charge storage can lead to shot-noise suppression in the PDR region below the current peak. The analysis also predicts shot-noise enhancement in the negative differential resistance (NDR) region, consistent with recent experimental results [6]. The analysis will include the following steps. First, a formalism for shot noise in the presence of a current-dependent transmission probability will be developed. This entails the introduction of a matrix that couples fluctuations in the transmission probability in any longitudinal-energy interval to fluctuations in the incident current in all other intervals. Next the transmission probability and the incident current will be related through the charge stored in the quantum well. This relationship leads to the definition of a quantity called the transmission modulation function. Finally, the modulation function is used to derive a closed-form expression for the shot-noise factor under short-circuit load conditions. The analysis is based on the stationary-state approach to resonant tunneling. The results apply to any resonant-tunneling process (coherent or sequential) described by the Breit-Wigner form of transmission probability.

II. CURRENT FLUCTUATIONS IN A DOUBLE-BARRIER DIODE

Current fluctuations through the double-barrier diode will be analyzed for an n-type device with a current consisting entirely of mobile electrons. The diode is biased with a large

enough voltage that a wide depleted space-charge region forms on one (anode) side of the double-barrier structure and excess electrons collect on the opposite (cathode) side. The actual band bending is represented by the solid conduction band edge in Fig. 1, but the analysis will carried out with the simplified band bending given by the dashed band edge. Under these conditions, the current through the diode consists of electrons that are incident on the double-barrier structure from the cathode side and are transmitted through the structure by resonant tunneling through the first quasibound level in the quantum well. The total time-averaged electronic flux incident on the double-barrier structure from the cathode side is denoted by J^i, and the transmitted flux is denoted by J^t. These fluxes can be decomposed into components J_n^i and J_n^t contained within specified intervals of energy, ΔE_n, along the tunneling direction (i.e., perpendicular to the heterobarriers). The energy is referenced to the conduction band edge on the cathode side. The magnitude of the time-averaged electrical current through the diode is related to the incident flux by

$$I = \sum_n eJ_n^t = \sum_{n,m} eT_{nm}J_m^i \equiv \sum_m eT_mJ_m^i = \sum_m I_m^c , \tag{1}$$

where T_{nm} is the transmission probability through the double-barrier structure of an electron incident in the *m*th energy interval and transmitted to the *n*th interval, and I_m^c is the electrical current flowing in the *m*th interval on the cathode side. This expression is valid independent of the coherent or sequential nature of the resonant tunneling [7]. For the purpose of analyzing the shot noise, fluctuations in the current and the fluxes are defined in the usual sense as the difference between the instantaneous and the average value of each of these quantities. For example, fluctuations in the *n*th component of the transmitted flux are denoted by $\Delta J_n^t = j_n^t(t) - J_n^t$. All of the fluctuations are assumed to occur under the condition of an ac short circuit across the diode.

The source of the shot noise is the fluctuations of the incident flux in each energy interval. A given component ΔJ_n^i has two effects on the transmitted current. First, it contributes directly to the transmitted current through the term $T_n\Delta J_n^i$. Second, it modulates the transmission probability in other energy intervals by varying the charge density, and hence the potential drop, in the double-barrier structure. To first order, the fluctuation in the diode current due to the fluctuations in all intervals is

$$\Delta I = \sum_n eT_n\Delta J_n^i + \sum_{n,m} eJ_n^i\frac{\partial T_n}{\partial J_m^i}\Delta J_m^i . \tag{2}$$

Since the fluctuation ΔJ_n^i occurs independently of T_n, one can write $\Delta I_n^c = eT_n\Delta J_n^i$ and

$$\Delta I = \sum_n \Delta I_n^c + \sum_{n,m} C_{nm}\Delta I_m^c , \tag{3}$$

where $C_{nm} = J_n^1(\partial T_n/\partial J_m^1)T_m^{-1}$. The quantity C_{nm} is an element of a matrix that represents the modulation of the transmission at each energy by fluctuations of the incident current at other energies.

From Eq. (3) the low-frequency power spectrum is found to be

$$S_I \equiv \frac{\overline{(\Delta I)^2}}{\delta f} = \frac{1}{\delta f}\left[\overline{(\sum_n \Delta I_n^c)^2} + \overline{2\sum_k \Delta I_k^c \sum_{n,m} C_{nm}\Delta I_m^c} + \overline{(\sum_{n,m} C_{nm}\Delta I_m^c)^2}\right]. \quad (4)$$

This expression is simplified with the assumption that the region on the cathode side of the double-barrier structure is in a state of thermodynamic quasi-equilibrium. In this case, there is a net electrical current through the region but the magnitude of the current is small enough that the following equilibrium properties are maintained. First, current fluctuations in different longitudinal energy intervals are uncorrelated [2],

$$\overline{\Delta I_n^c \Delta I_m^c} = \delta_{nm}\,\overline{[\Delta I_n^c]^2}\,, \quad (5)$$

where δ_{nm} is the Kronecker delta function. Second, the current component fluctuations are Poisson distributed and are thus related to the dc component by the well-known Schottky relation [1],

$$\overline{[\Delta I_n^c]^2} = 2eI_n^c\,\delta f\,. \quad (6)$$

The application of these relations in Eq. (4) leads to the result

$$S_I = 2eI\left[1 + 2I^{-1}\sum_{n,m} C_{nm}I_m^c + I^{-1}\sum_m(\sum_n C_{nm})^2 I_m^c\right] \equiv 2eI\gamma\,, \quad (7)$$

where the identity $I = \sum_m I_m^c$ has been applied. In the limit that $\Delta E_n \to 0$ for all n, γ can be written in integral form as

$$\gamma = 1 + 2I^{-1}\int_{E'}\left[\int_E dC(E,E')\right] dI^c(E') + I^{-1}\int_{E'}\left[\int_E dC(E,E')\right]^2 dI^c(E')\,, \quad (8)$$

where $dC(E,E') = dJ^1(E)[\partial T(E)/\partial J^1(E')]T^{-1}(E')$.

III. DERIVATION OF THE SHOT-NOISE FACTOR

Up to this point the discussion has been rather general in scope, relying only on the validity of the stationary-state approach and the presence of quasi-equilibrium on the cathode side of the double-barrier structure. To evaluate $dC(E,E')$ analytically, several assumptions regarding the nature of the resonant tunneling and the electrostatics of the double-barrier structure are required. First, the resonant-tunneling process is assumed to be consistent with the single-particle Breit-Wigner transmission probability [8,9],

$$T(E) = \frac{\Gamma_T}{\Gamma_1^L + \Gamma_1^R}\left[\frac{\Gamma_1^L\Gamma_1^R}{(E - E_1)^2 + \Gamma_1^2/4}\right], \tag{9}$$

where E_1 is the energy of the first quasibound state in the quantum well referenced to the neutral conduction-band edge on the cathode side, Γ_1^L and Γ_1^R are the partial-width factors for the left and right barriers, respectively, and $\Gamma_T = \Gamma_1^L + \Gamma_1^R + \Gamma_S$ with Γ_S being a phenomenological scattering parameter representing the effect of inelastic scattering events that occur in the double-barrier structure [10]. The partial-width factors are a measure of the transparency of the barriers, and depend on the bias voltage in a rather complicated manner. However, it is generally true that in double-barrier structures having Type I band offsets (the wider bandgap material acts as a barrier to both electrons and holes), Γ_1^L decreases monotonically with increasing bias voltage and Γ_1^R increases monotonically. Therefore, as a first approximation one can assume that the product and the sum of Γ_1^R and Γ_1^L are both constant with respect to bias voltage. This approximation will be addressed further in Appendix A.

The next assumption is that E_1 depends only on the electrostatic potential drop across the double-barrier structure, ψ_S, and is not affected by electron-electron interactions (i.e., direct and exchange forces), band mixing, or other effects in the quantum well. A useful approximation is that E_1 decreases with bias voltage as

$$E_1 = E_1^0 - \frac{1}{2}e\psi_S , \tag{10}$$

where E_1^0 is the energy of the first state at zero bias. In double-barrier structures biased so that a large electrical current flows, the many-body potentials are usually much smaller than the potential energy term $e\psi_S/2$ [11].

The next three assumptions concern the distribution of charge and the band bending in the double-barrier diode. First, the magnitude of the electron sheet charge density, σ_w, stored in the double-barrier structure is distributed as a delta function at the center of the quantum well [12]. Then, ψ_S can be written

$$\psi_S = F_D L_S - \frac{\sigma_w}{\varepsilon}(L_B^L + L_W/2) , \tag{11}$$

where F_D is the magnitude of electric field at the depletion end of the double-barrier structure, ε is the permittivity which is assumed to be uniform throughout the structure, L_B^L is the thickness of the left-hand barrier (adjacent to the cathode side), L_W is the width of the quantum well, and L_S is the total thickness of the double-barrier structure given by $L_B^L + L_W + L_B^R$, where L_B^R is the thickness of the right-hand barrier. Second, the electron density on the cathode side is so high that no potential drop occurs across this region. Third, the depletion

region has a uniform background donor doping N_D and a potential drop ψ_D consistent with the depletion approximation. With these assumptions one can derive the expression

$$\psi_S \approx L_S[2N_D(eV_T + E_F^a - E_F^c - e\psi_S)/\varepsilon]^{1/2} - \frac{\sigma_w}{\varepsilon}(L_B^L + L_W/2)\,, \tag{12}$$

where V_T is the bias voltage applied across the device. The combination of zero potential drop and quasi-equilibrium on the cathode side allows one to write [13]

$$dJ^i(E) = \frac{m^*kTA}{2\pi^2\hbar^3}\log[1 + \exp(E_F^c - E)/kT]dE\,, \tag{13}$$

where A is the diode area.

The last assumption is that the sheet charge density is given by the expression resulting from the dwell-time theory of double-barrier traversal [14]:

$$\sigma_w = \frac{\hbar I}{A\Gamma_I^R}\,. \tag{14}$$

This expression assumes that electrons traverse the structure only from cathode to anode, and are prohibited by Pauli exclusion from traversing the structure in the opposite sense. Substitution of the integral form of Eq. (1) yields

$$\sigma_w = \frac{e\hbar}{A\Gamma_I^R}\int T(E)dJ^i(E)\,. \tag{15}$$

The above set of assumptions facilitate an evaluation of $dC(E,E')$ using the following expansion by the chain rule:

$$dC(E,E') = dJ^i(E)\,\frac{\partial T(E)}{\partial \psi_S}\,\frac{\partial \psi_S}{\partial \sigma_w}\,\frac{\partial \sigma_w}{\partial J^i(E')}T^{-1}(E')\,. \tag{16}$$

This expansion is analyzed in Appendix B, where it is found that $dC(E,E')$ is independent of E'. This means that Eq. (8) can be reformulated as

$$\gamma = 1 + 2M + M^2\,, \tag{17}$$

where $M \equiv \int dC(E)$ will be called the transmission modulation function. Note that γ has a minimum value of zero at $M = -1$, approaches 1 at $M = 0$, and exceeds 1 for $M > 0$. That is, the shot noise is *suppressed* for $-1 < M < 0$ and is *enhanced* for $M > 0$.

A closed form expression for M is obtained from Eq. (B.5) in the limit

$$E_F^c - E_1^0 + e\psi_S/2 \gg kT\,, \tag{18}$$

which corresponds to either low temperatures or bias voltages well above the current turn-on (i.e., the voltage at which a sizable current begins to flow). Evaluation of the integral over

the range from 0 to E_F^ξ leads to the result

$$M = \lambda \left[\frac{E_F^\xi \Gamma_T/2}{(\xi - E_F^\xi)^2 + \Gamma_T^2/4} + \left[\tan^{-1}[(2(\xi - E_F^\xi)/\Gamma_T] - \tan^{-1}[2\xi/\Gamma_T] \right] \right], \qquad (19)$$

where $\lambda = e^2\hbar\beta(\Gamma_1^L\Gamma_1^R)(L_B^L + L_W/2)[\epsilon(\Gamma_1^L+\Gamma_1^R)\Gamma_1^R(1 + L_S/L_D)]^{-1}$, $\beta = m^*/2\pi^2\hbar^3$, $\xi = E_F^\xi - E_1^0 + e\psi_S/2$, and L_D is the depletion length given by $\epsilon F_D/eN_D$ in the depletion approximation. This expression has the desired property that $M \to 0$ as $\Gamma_1^L \to 0$ or as $\Gamma_1^R \to \infty$. Both of these limits describe a situation where no charge is stored in the quantum well during resonant tunneling and thus no modulation of the transmission probability is possible.

IV. CURRENT-VOLTAGE CHARACTERISTIC

To obtain the shot-noise factor it is necessary to obtain the current-voltage (I-V) curve since through Eq. (14) the current determines the sheet charge in the well, and the sheet charge in the well determines the voltage drop ψ_S and the partial-width factors. The I-V curve follows directly from the integral form of Eq. (1), Eq. (13), and the assumptions stated in Sec. III:

$$I = \beta AkT \int_0^{E_F^\xi} T(E,\sigma_w) \log[1 + \exp(E_F^\xi - E)/kT]dE . \qquad (20)$$

The transmission probability is written explicitly as a function of σ_w to emphasize the fact that the sheet charge density in the quantum well could be high enough to affect the I-V curve as well as the shot noise. In the limit of low temperatures or high bias voltages defined by Eq. (18), the current is given by

$$I = \frac{\beta A \Gamma_T(\Gamma_1^L\Gamma_1^R)}{(\Gamma_1^L + \Gamma_1^R)} \left[\frac{2\xi}{\Gamma_T} \left[\tan^{-1}\frac{2\xi}{\Gamma_T} - \tan^{-1}\frac{2(\xi - E_F^\xi)}{\Gamma_T} \right] + \frac{1}{2}\log\left[\frac{\Gamma_1^2/4 + (\xi - E_F^\xi)^2}{\Gamma_1^2/4 + \xi^2} \right] \right]. \qquad (21)$$

Using Eqs. (11) and (14), one can write

$$\xi = E_F^\xi - E_1^0 + \frac{eL_S}{2}(F_D - \sigma_w/2\epsilon) . \qquad (22)$$

For each value of F_D, one can obtain the current and the sheet-charge density by iteration. In the first pass, a value of F_D is chosen that is large enough to neglect right to left going currents, σ_w is assumed to be zero, and ξ, Γ_1^L, and Γ_1^R are calculated from Eqs. (22) and (A.1) - (A.3). The current is then obtained from Eq. (21) and used as input to the second pass. The first step of the second pass is computing σ_w using values of I and Γ_1^R obtained

from the first pass. Then ξ and I are re-computed with $\Gamma_1^L\Gamma_1^R$ and $\Gamma_1^L + \Gamma_1^R$ held fixed. The process is repeated until convergence is achieved. The final values of σ_w, ξ, and Γ_1^R are inserted into Eq. (19) to obtain the shot-noise factor.

V. COMPARISON WITH EXPERIMENT

The experimental I-V curve and shot-noise factor are given in Figs. 2(a) and 2(b), respectively, for an RTD consisting of two 5.0-nm-thick undoped $Al_{0.42}Ga_{0.58}As$ barriers separated by a 5.0-nm-thick GaAs quantum well. Outside of each barrier is a 50-nm-thick buffer layer that is doped $N_D = 2\times10^{16}$ cm^{-3}, and outside of each buffer layer are n^+ epilayers that extend to the substrate and the top contact region. Other details regarding the growth and material quality of this structure are given elsewhere [15]. The experiments were conducted on an 8-μm-diameter diode mounted and whisker contacted in a cartridge and cooled to 77 K by immersion in liquid nitrogen. The shot-noise factor in the PDR region below the current peak was measured by microwave radiometric techniques [6]. The shot-noise factor in the NDR region was determined by measuring the linewidth of the RTD functioning as a microwave oscillator and relating this linewidth to the phase noise expected from a shot-noise process. The resulting value of γ is a crude upper limit since other mechanisms such as 1/f noise from the ohmic contacts contribute to the linewidth but are not subtracted out in the derivation.

The I-V curve in Fig. 2(a) displays a current turn-on near 0.3 V, a current peak at approximately 0.6 V, and a current valley at 0.85 V. The peak-to-valley current ratio is 8. Between the peak and valley points is an NDR region characterized by several discontinuities in the current. These discontinuities are a result of oscillations in the diode and the measurement circuit. The vertical segments with arrows denote the *extrinsic* bistability associated with the oscillations. At voltages above the valley point, the current increases rapidly. This is caused at least in part by the turn-on of current through the second quasibound level in the quantum well.

The experimental 77-K shot-noise factor in Fig. 2(b) is suppressed throughout the PDR region below the current peak and is enhanced at the only measurement point in the NDR region. In the PDR region, γ is nearly constant with bias voltage, ranging from 0.5 just above the current turn-on to 0.35 just below the current peak. In the NDR region, a shot-noise factor of 8.0 is obtained at a bias point in the discontinuous region just above the peak. Beyond the valley point, the shot-noise factor asymptotically approaches unity. The measured I-V curve and shot-noise characteristics at 77 K are practically identical to those obtained in separate measurements at a bath temperature of 4.2 K. In room temperature measurements, the I-V curve had about 1 mA less peak current and a current peak-to-valley ratio of

approximately 4. The shot-noise factor was similar to the results at 77 K except that the minimum γ in the PDR region was about 30% less than that measured at room temperature, and the value of γ at the one bias point in the NDR region was 5.0.

Theoretical I-V and shot-noise-factor curves are given in Figs. 3, 4, and 5. The physical parameters used in each of the curves are $E_1^0 = 89$ meV, $E_F^S = 40$ meV, $\phi_{B,0}^L = \phi_{B,0}^R = 0.31$ eV, and $m^* = 0.067m_0$. Using Eq. (A.1), one finds $\Gamma_1^L = \Gamma_1^R = 0.10$ meV at zero bias so that $\Gamma_1^L\Gamma_1^R = 1\times10^{-8}$ eV^2 and $\Gamma_1^L + \Gamma_1^R = 0.2$ meV. The area of the RTD is 50 μm^2. Because the scattering parameter Γ_S is not known *a priori*, it was determined by the requirement that the theoretical I-V curve match the experimental curve qualitatively. In Fig. 3(a) with $\Gamma_S = 0.8$ meV, the I-V curve displays a voltage range of *intrinsic* bistability or, more properly, tristability (i.e., three different currents for the same voltage), which is associated with charge storage in the quantum well [16,17]. Since this behavior is not observed experimentally, one must consider a larger Γ_S, such as the value 4.0 meV. In this case, the *intrinsic* bistability does not appear in the I-V curve and the NDR region is characterized by a nearly vertical drop in current at voltages just above the peak point. The largest Γ_S assumed in Fig. 3(a) is 20 meV. The resulting I-V curve is qualitatively similar to the curve for $\Gamma_S = 4.0$ meV except that the peak current is significantly reduced. This is a result the fact that Γ_S is approaching E_F^S. In other words, the area under the T(E) vs E curve is no longer contained entirely within the occupied Fermi sea of electrons on the cathode side. None of the theoretical I-V curves displays a valley point since the present model does not account for current flow through the second quasibound level in the quantum well.

The theoretical I-V curve that most resembles the experimental curve is that in Fig. 3(a) for $\Gamma_S = 4$ meV. In this case, the shot-noise factor shown in Fig. 3(b) starts out at unity at voltages below the current turn-on, decreases rapidly to 0.58 just above this point, and then increases gradually to 1.0 at the current peak. At voltages above the peak, γ rises to a maximum of approximately 4.3 in the steepest part of the NDR region, and then falls rapidly to unity at higher voltages. The theoretical γ is in qualitative agreement with the experimental curve except at voltages below the current turn-on and at voltages in the PDR region beyond the valley point. In the former region, the theoretical γ approaches unity but the experimental value does not. In the latter region, the theoretical γ approaches unity from above whereas the experimental value approaches unity from below. The first discrepancy is thought to result from a breakdown of the assumption given by Eq. (18) at low bias voltages. The second discrepancy is not presently understood. The less significant discrepancy between the minimum experimental (0.35) and theoretical (0.58) γ values in the PDR region is also unexplained, but it is not related to the magnitude of Γ_S. Fig. 3(b) illustrates that a much smaller Γ_S of 0.8 meV still yields a minimum γ (0.52) greater than the experimental minimum. The

difference between the maximum theoretical (4.3) and experimental (8.0) values of γ in the NDR region may reflect the fact that the experimentally determined shot-noise factor is just an upper limit, as mentioned above. Note that the theoretical shot-noise factor in the NDR region is very sensitive to Γ_S in contrast to its behavior in the PDR region. This results from a weakening of the transmission modulation mechanism in the NDR region with increasing breadth of T(E).

A broadening parameter of 4 meV corresponds to a scattering or dephasing time of $\tau_s = \hbar/\Gamma_S = 0.16$ ps, which is a plausible value in this type of double-barrier structure. It easily satisfies the condition for spatial quantization in the quantum well, which is given by $E_1\tau_s \gg \hbar$ or $\tau_s >> 7$ fs. It is consistent with a sequential rather than a coherent resonant tunneling process in the sense that $\tau_S < \tau_1$, where $\tau_1 = \hbar/(\Gamma_1^L+\Gamma_1^R) = 3$ ps is the quasibound-state lifetime. However, the present analysis suggests that the shot-noise suppression and enhancement effects are not critically sensitive to which process prevails. Rather, the analysis suggests that the deviations from normal shot noise are greatest in the fully coherent limit (i.e., $\Gamma_S = 0$) and gradually disappear as Γ_S increases.

VI. DISCUSSION

An important question is whether or not the shot-noise characteristics observed in the above diode are to be expected in other RTDs, especially the high-current-density diodes used in high-speed oscillation and switching applications. This can be addressed by analyzing Eq. (19) as a function of bias voltage. The PDR region of RTDs biased well above the current turn-on is defined approximately by $\Gamma_T \ll \xi < E_F^E$. In this range one finds $M \approx -\lambda\pi$, where λ is the positive unitless quantity defined after Eq. (19). Thus, one expects shot-noise suppression to occur in the PDR region of all RTDs. To obtain the greatest shot-noise suppression, the sum $L_B^L + L_W/2$ and the ratio $\Gamma_1^L/(\Gamma_1^L + \Gamma_1^R)$ should be as large as possible. This ratio approaches a maximum value of unity in the limit where the second barrier is much less transparent than the first. For barriers made of the same material, this limit means that the second barrier is much thicker than the first. Intuitively, it makes sense that such a double-barrier structure would display large shot-noise suppression since, according to Eq. (14), the sheet-charge density in the quantum well is high when Γ_1^R is small, and high sheet-charge density makes the transmission modulation mechanism more effective. In addition, the ratio of L_D to L_S should be as large as possible. This is realized in diodes containing wide, lightly doped spacer layers on the anode side. Nearly all high-speed RTDs have this feature.

As discussed above, a significant shot-noise enhancement occurs in the NDR bias-voltage region, which is defined approximately by $E_F^E - \Gamma_T < \xi < E_F^E + \Gamma_T$. It is is a region where RTD oscillators are often biased for high-frequency operation. From Eq. (19), one finds a

maximum theoretical M of approximately $2\lambda E_F^c/\Gamma_T$ in this range. In most high-speed RTDs E_F^c probably exceeds Γ_T by a sizable margin (since E_F^c is made large to achieve high current density), so that one expects significant shot-noise enhancement to occur. To minimize the shot-noise enhancement, the double-barrier structure should be thin and the ratio $\Gamma_1^L/(\Gamma_1^L+\Gamma_1^R)$ should be as small as possible. Most high-speed RTDs have these features since they typically have a narrow quantum well and very thin, nominally identical barriers. The thin barriers cause Γ_1^R to be comparable in value to Γ_1^L even at bias voltages in the NDR region, so that $\Gamma_1^L/(\Gamma_1^L+\Gamma_1^R) \approx 0.5$. Unfortunately, high-speed RTDs usually have a large E_F^c to produce high current density. Consequently, a tradeoff between shot-noise enhancement and current density exists in RTDs operating in the NDR region.

The bias region far beyond the current peak is defined by $\xi \gg E_F^c$. In this region one finds $M \approx \lambda E_F^c \Gamma_T/2(\xi - E_F^c)^2$. In most RTDs this is positive and substantially smaller in magnitude than M in the aforementioned bias regions. It also decays very rapidly with bias voltage beyond the current peak. Thus, one expects that the shot-noise enhancement observed just beyond the current peak will diminish rapidly with increasing voltage.

CONCLUSION

An analytic model has been developed to explain the shot noise associated with current flow through the first quasibound level of a double-barrier resonant-tunneling diode. The model explains the shot-noise suppression and enhancement effects that have been measured in double-barrier RTDs biased into the PDR and NDR regions, respectively, of the first current peak. The physical basis for the model is the modulation of the transmission probability by electrons stored in the quantum well during the resonant-tunneling process. It is instructive to point out a physical characteristic of the model that is responsible for the opposing shot-noise effects. This characteristic is given by the relation $\partial\psi_S/\partial\sigma_w < 0$ used in the derivation of Eq. (B.5). This relation implies that a fluctuation associated with increasing incident current (and hence σ_w) decreases ψ_S. This should lead to a decrease in the total current if the device is biased in the PDR region below the current peak, because a drop in ψ_S moves the quasibound level up to an energy at which there are fewer electrons to tunnel from the cathode side. In the NDR region, it causes an increase in the total current because a drop in ψ_S moves the quasibound level to an energy at which there are more electrons to tunnel. In this sense, the shot-noise suppression in the PDR region below the current peak is similar in nature to that of a space-charge-limited vacuum diode. The novel feature of the RTD is the shot-noise enhancement, which relies on the existence of a resonant transmission probability.

ACKNOWLEDGMENTS

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APPENDIX A: PARTIAL WIDTHS OF THE TRANSMISSION PROBABILITY

Under the assumption that the potential profile across the double-barrier structure is piecewise flat, the following expression for the partial widths of T(E) in Eq. (9) have been derived [19]:

$$\Gamma_1^{L,R} = \left. \frac{8\hbar^2 k_1^2 k_{L,R} \alpha_{L,R}^2}{m^*} \frac{\exp(-2\alpha_{L,R} L_B^{L,R})}{(L_S + \alpha_L^{-1} + \alpha_R^{-1}) K_{L,R}^4} \right|_{E_1} . \qquad (A.1)$$

In this equation k_1 is the quasibound-state wavevector, k_L and k_R are the wavevectors in the left and right cladding layers, respectively, and α_L and α_R are the attenuation coefficients in the left and right barriers, respectively, measured at energy E_1. The quantities K_L and K_R are given by $(2m^*\phi_{B,0}^L)^{1/2}/\hbar$ and $(2m^*\phi_{B,0}^R)^{1/2}/\hbar$, respectively, where $\phi_{B,0}^L$ and $\phi_{B,0}^R$ are zero-bias barrier heights referenced to the conduction band edge on the cathode side. The validity of Eq. (A.1) requires that the quasibound level is always aligned with traveling-wave states on the cathode and anode sides, respectively. A second requirement is that the effective mass m^* is uniform throughout the double-barrier structure and cladding layers. The former requirement is not satisfied in the present electrostatic model at bias voltages that lower the first quasibound level below the occupied states on the cathode side. This precludes the application of Eq. (A.1) for Γ_1^L at bias voltages in the NDR region and beyond, and is a further motivation for adopting the simplifying assumptions in Sec. III concerning the constancy of the product $\Gamma_1^L\Gamma_1^R$ and the sum $\Gamma_1^L + \Gamma_1^R$. The second requirement concerning the effective mass is reasonably satisfied for a GaAs/$Al_{0.42}Ga_{0.58}As$ structure [$m^*(GaAs) = 0.067\ m_0$, and $m^*(Al_{0.42}Ga_{0.58}As) \approx 0.09\ m_0$], but may not be satisfied in a GaAs/AlAs structure [$m^*(AlAs) = 0.15\ m_0$].

To apply Eq. (A.1), the expected band bending (solid line) given in Fig. 1 must be replaced by the piecewise-flat profile (dashed line) that is superimposed in the same figure. From this profile and the electrostatic assumptions stated in Sec. III, the partial-width parameters are expressed by $k_L = [(2m^*(E_1^0 - e\psi_S/2)]^{1/2}/\hbar$ (since there is no potential drop on the cathode side), $k_1 = (2m^*E_1^0)^{1/2}/\hbar$, and $k_R = [(2m^*(E_1^0 + e\psi_S/2)]^{1/2}/\hbar$. For the attenuation

coefficients, the following bias-dependent barrier heights are introduced: $\phi_B^L = \phi_{B,0}^L - (F_D - \sigma_w/\varepsilon)eL_B^L/2$, and $\phi_B^R = \phi_{B,0}^R - e\psi_S + eF_DL_B^R/2$. These barrier heights are again referenced to the conduction band edge on the cathode side, as shown diagrammatically in Fig. 1. With these parameters one can write the following expressions for the attenuation coefficients:

$$\alpha_L = \frac{1}{\hbar}[2m^*(\phi_B^L - E_1^0 + \tfrac{1}{2}eF_D(L_S - L_B^L) - e\sigma_w(L_S/2 - L_B^L)/2\varepsilon)]^{1/2} \qquad (A.2)$$

$$\alpha_R = \frac{1}{\hbar}[2m^*(\phi_B^R - E_1^0 - \tfrac{1}{2}eF_D(L_S - L_B^R) + e\sigma_wL_S/4\varepsilon)]^{1/2}\,. \qquad (A.3)$$

APPENDIX B: DERIVATION OF THE TRANSMISSION MODULATION FUNCTION

The derivation of the shot-noise factor starts with an evaluation of the function $dC(E,E')$ given by Eq. (16). The first partial derivative in this expression can be derived directly from the Breit-Wigner form in Eq. (9). Three quantities in Eq. (9), E_1, Γ_1^L, and Γ_1^R, vary with ψ_S. The strongest dependence occurs through E_1, which yields

$$\frac{\partial T(E)}{\partial \psi_S} = -\frac{eT(E)(E - E_1^0 + e\psi_S/2)}{(E - E_1^0 + e\psi_S/2)^2 + \Gamma_1^2/4}\,. \qquad (B.1)$$

The dependence of $T(E)$ on ψ_S through Γ_1^L and Γ_1^R is relatively weak because these quantities have an opposing variation with ψ_S and because $T(E)$ in Eq. (9) depends on these quantities either as the sum or product. The opposing variation of Γ_1^L and Γ_1^R stems from the following properties. From Eqs. (A.2) and (A.3) one observes that α_L increases with ψ_S and α_R decreases with ψ_S at nearly the same rate. This requires that $|F_D| \gg \sigma_w/\varepsilon$, which is generally true in double-barrier structures. Typical double-barrier structures also satisfy the thick-barrier criterion, $2\alpha_{L,R}L_B^{L,R} > 1$. From Eq. (A.1) this means that Γ_1^L decreases with increasing α_L and Γ_1^R increases with decreasing α_R.

The next partial derivative is found by imposing the short-circuit condition on Eq. (12). The short-circuit condition means that V_T remains fixed for all current fluctuations. Thus, one can write

$$\left.\frac{\partial \psi_S}{\partial \sigma_w}\right|_{V_T} = -\frac{(L_B^L + L_W/2)[\psi_S + \sigma_w(L_B^L + L_W/2)/\varepsilon]}{\varepsilon[\psi_S + \sigma_w(L_B^L + L_W/2)/\varepsilon + eN_DL_S^2/\varepsilon]} = -\frac{(L_B^L + L_W/2)}{\varepsilon(1 + L_S/L_D)}\,. \qquad (B.2)$$

The last partial derivative is found from Eq. (15) as $\partial\sigma_w/\partial J^i(E') = e\hbar T(E')/\Gamma_1^RA$. When this is combined with Eqs. (B.1) through (B.3) and inserted into Eq. (16), one obtains

$$dC(E,E') = \frac{dJ^i(E)e^2\hbar}{\Gamma_1^RA}\,\frac{(E - E_1^0 + e\psi_S/2)T(E)}{(E - E_1^0 + e\psi_S/2)^2 + \Gamma_1^2/4}\,\frac{L_B^L + L_W/2}{\varepsilon(1 + L_S/L_D)}\,. \qquad (B.3)$$

REFERENCES

[1] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986, Chap. 3.

[2] F. N. H. Robinson, *Noise and Fluctuations in Electronic Devices and Circuits*. Oxford: Clarendon, 1974, Sec. 5.4.

[3] E. R. Brown, T. C. L. G. Sollner, and W. D. Goodhue, "Noise properties of quantum well structures," in *Solid State Research Report*. Lexington, MA: MIT Lincoln Laboratory, 1986:1, pp. 37-40.

[4] Y. P. Li, A. Zaslavsky, D. C. Tsui, M. Santos, and M. Shayegan, "Noise characteristics of double-barrier resonant-tunneling structures below 10 kHz," *Phys. Rev. B*, vol. 41, pp. 8388-8391, 1990.

[5] J. Han and F. S. Barnes, "A theory of shot noise in quantum wells and applications in resonant tunneling heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 38, pp. 237-241, 1991.

[6] E. R. Brown, C. D. Parker, A. R. Calawa, and M. J. Manfra, in "1991 Device Research Conference Abstracts," to be published in *IEEE Trans. Electron Devices*.

[7] For the coherent case, one can write $J_n^{(t)} = T_n J_n^{(i)}$. In the sequential case where longitudinal energy is not conserved, $J_n^{(t)}$ and $J_n^{(i)}$ are no longer directly related, but the sum in Eq. (1) remains valid.

[8] A. D. Stone and P. A. Lee, "Effect of inelastic processes on resonant tunneling in one dimension," *Phys. Rev. Lett.*, vol. 54, pp. 1196-1199, 1985.

[9] M. Büttiker, "Coherent and sequential tunneling in series barriers," *IBM J. Res. Dev.*, vol. 32, pp. 63-75, 1988.

[10] The ratio $\Gamma_S / \left(\Gamma_1^L + \Gamma_1^R\right)$ is a measure of the nature of the resonant tunneling. For $\Gamma_S << \Gamma_1^L + \Gamma_1^R$, the resonant tunneling is coherent. In the opposite limit, it is sequential.

[11] K. M. S. V. Bandara and D. D. Coon, "Electron-electron interactions and resonant tunneling in heterostructures," *Appl. Phys. Lett.*, vol. 53, pp. 1865-1867, 1988.

[12] This approximation for the charge distribution causes very little error in double-barrier structures having thin quantum wells, which include most high-speed RTDs.

[13] C. B. Duke, "Tunneling in Solids," in *Solid State Physics*, F. Seitz, D. Turnbull, and H. Ehrenreich, Eds., Suppl. 10. New York: Academic, 1969, Sec. 5.

[14] K. M. S. V. Bandara, D. D. Coon, and H. Zhao, "Resonant tunneling time delay and quantum well sheet density," *J. Appl. Phys.*, vol. 66, pp. 1227-1230, 1989.

[15] C. I. Huang, M. J. Paulus, C. A. Bozada, S. C. Dudley, K. R. Evans, C. E. Stutz, R. L. Jones, and M. E. Cheney, "AlGaAs/GaAs double barrier diodes with high peak-to-valley current ratio," *Appl. Phys. Lett.*, vol. 51, pp. 121-123, 1987.

[16] V. J. Goldman, D. C. Tsui, and J. E. Cunningham, "Observation of intrinsic bistability in resonant-tunneling structures," *Phys. Rev. Lett.*, vol. 58, pp. 1256-1259, 1987.

[17] F. W. Sheard and G. A. Toombs, "Space-charge buildup and bistability in resonant-tunneling double-barrier structures," *Appl. Phys. Lett.*, vol. 52, pp. 1228-1230, 1988.

[18] E. T. Koenig, B. Jogai, M. J. Paulus, C. I. Huang, and C. A. Bozada, "Charge-quantization effects on current-voltage characteristics of AlGaAs/GaAs resonant tunneling diodes with spacer layers," *J. Appl. Phys.*, vol. 68, pp. 3425-3430, 1990.

[19] E. Gerjuoy and D. D. Coon, "Analytic S-matrix considerations and time delay in resonant tunneling," *Supperlatt. Microstruct.*, vol. 5, pp. 305-315, 1989.

FIGURE CAPTIONS

Fig. 1. Band bending model of double-barrier structure. ψ_S is the electrostatic potential drop across the double-barrier structure and V_T the voltage drop across the total active region. F_D is the magnitude of the electric field at the depletion-region boundary, E_1 is the energy of the quasibound state under bias, and E_F^c and E_F^a are the quasi-Fermi levels on the cathode and anode sides of the structure, respectively. This model assumes that the charge is distributed as a delta function in the center of the quantum well. The dashed lines in the double-barrier structure represent the piecewise-flat approximation to the above band-bending model, which is used for calculating the partial-width factors of the transmission probability.

Fig. 2. (a) Experimental I-V curve showing hysteresis in the NDR region and (b) shot-noise factor for a GaAs/$Al_{0.42}Ga_{0.58}As$ RTD at 77 K.

Fig. 3. (a) Theoretical I-V curve and (b) shot-noise factor for the RTD in Fig. 2 computed with Γ_S = 0.8 meV, 4.0 meV, and 20.0 meV. The other physical parameters are defined in the text. For Γ_S = 4.0 meV, the minimum shot-noise factor is 0.58 at a bias voltage just above the current turn-on, and the maximum shot-noise factor is 4.2 at a voltage in the NDR region above the peak.

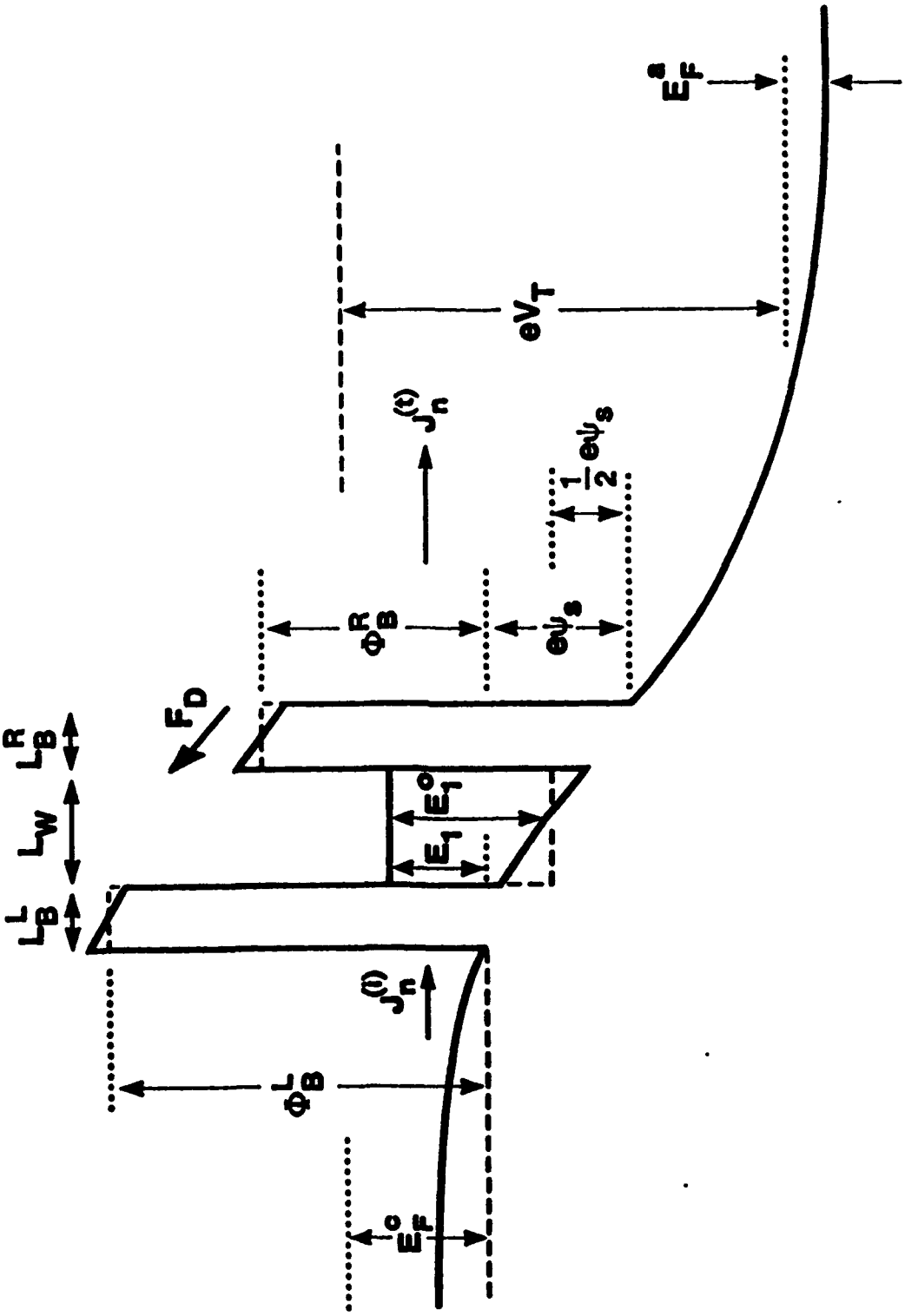
E_F^a
eV_T
$J_n^{(t)}$
$\frac{1}{2}e\psi_s$
Φ_B^R
$e\psi_s$
F_D
L_B^R
L_W
L_B^L
E_1^o
E_1
$J_n^{(i)}$
Φ_B^L
E_F^o

FIGURE 1

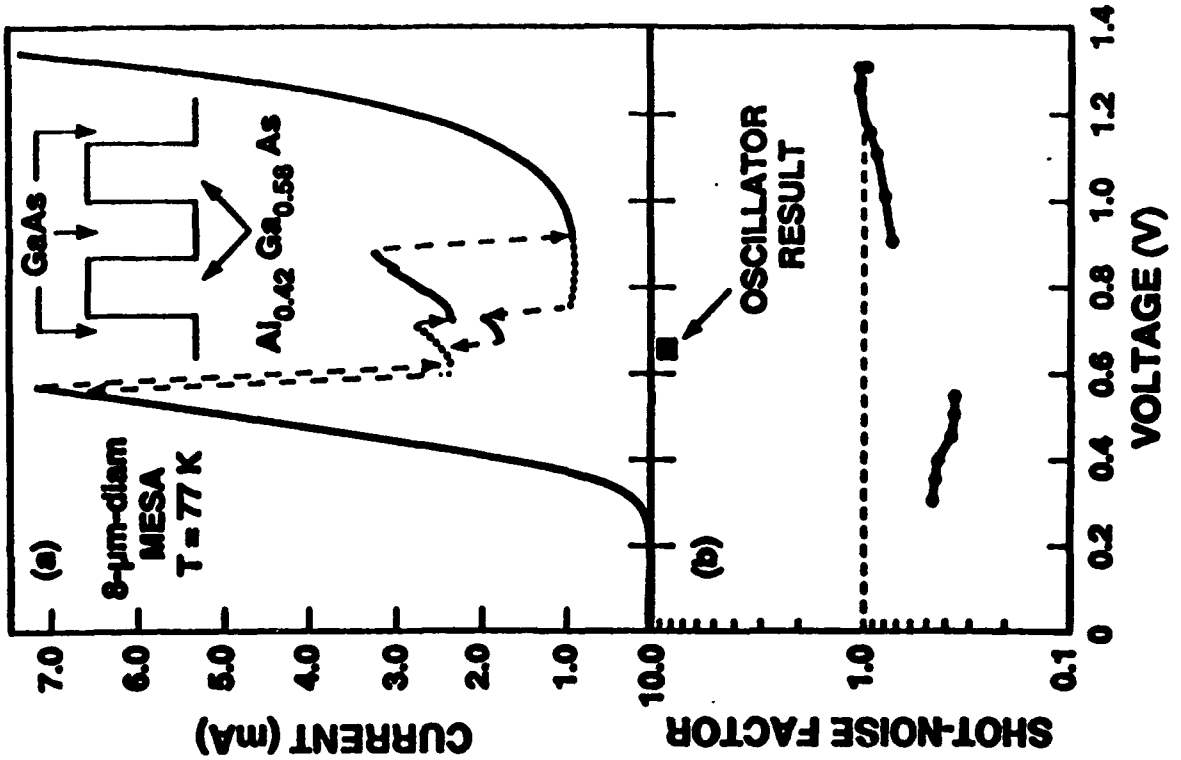
(a)
8-μm-diam MESA T = 77 K
GaAs
$Al_{0.42}Ga_{0.58}As$
CURRENT (mA)
7.0
6.0
5.0
4.0
3.0
2.0
1.0
(b)
OSCILLATOR RESULT
SHOT-NOISE FACTOR
10.0
1.0
0.1
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
VOLTAGE (V)

FIGURE 2

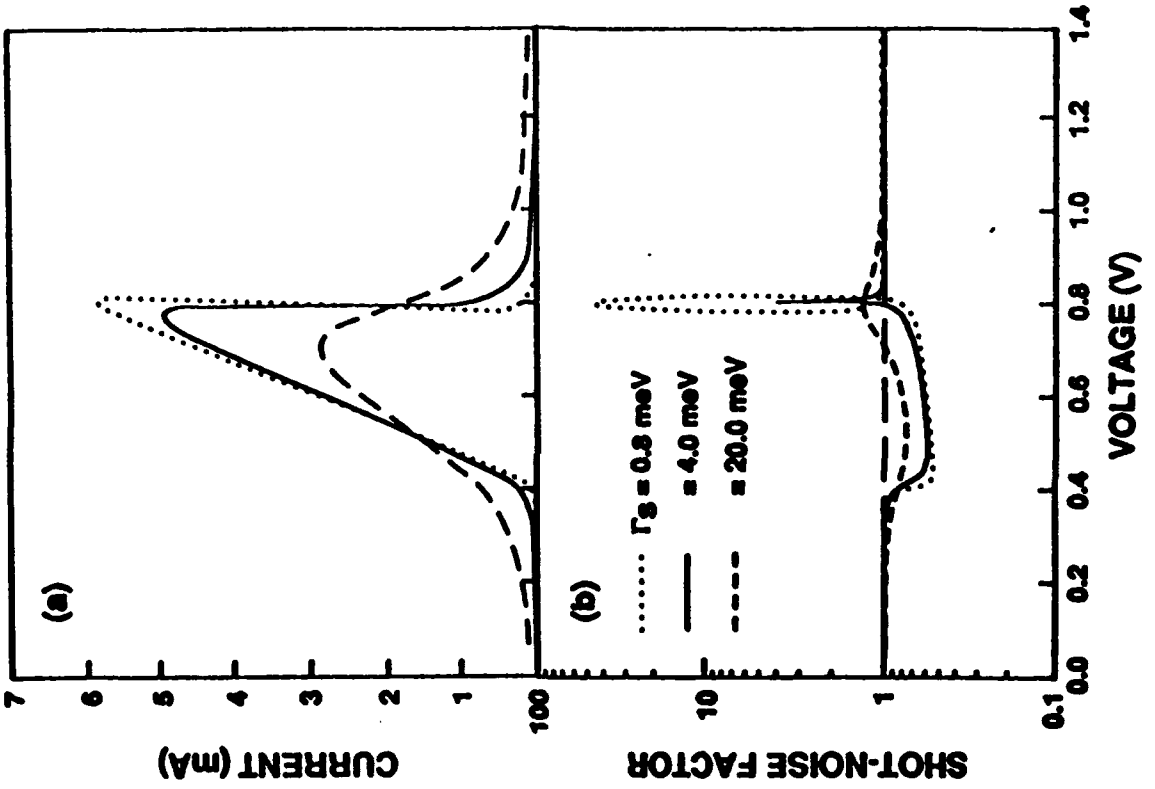
(a)
(b)
CURRENT (mA)
SHOT-NOISE FACTOR
VOLTAGE (V)
Γ_S = 0.8 meV
= 4.0 meV
= 20.0 meV
7
6
5
4
3
2
1
100
10
1
0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4

FIGURE 3

APPENDIX D

Enhanced negative differential resistance in a resonant-tunneling structure

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Abstract

A triple-well resonant-tunneling structure made from the $In_{0.53}Ga_{0.47}As$/AlAs material system is shown to have a 1.3-V-wide negative differential resistance (NDR) region, as compared to approximately 0.4 V for a typical single-well resonant-tunneling diode. A diode made from this structure is used to generate a nearly constant power of 0.5 mW up to 16 GHz. The broad NDR region is attributed to resonant tunneling through two closely spaced quasibound levels.

Resonant tunneling continues to attract interest for electronic applications since it is a transport process that provides a high-speed negative differential resistance (NDR) characteristic with very high peak current density and useful peak-to-valley current ratio at room temperature. The device used for the majority of applications has been the single-well (double-barrier) resonant-tunneling diode (RTD). For example, a single-well RTD fabricated from the InAs/AlSb material system has recently produced oscillations up to 712 GHz [1]. A characteristic shared by the current-voltage (I-V) curves of all single-well RTDs is the precipitous drop of the current in the NDR region between the peak and valley voltages. While this characteristic is ideally suited to switching applications [2], it is often detrimental in analog applications such as oscillators. In this letter, we demonstrate a diode having a much broader NDR region than the typical single-well RTD, and we show that the oscillator power can be increased by the broad NDR region.

The diode in the present study was originally designed to see if high peak current density J_P could be achieved in multiple-well structures and to search for new resonant-tunneling effects associated with the distribution of electrons over several quantum wells. Our numerical simulations showed that high J_P was possible by successively decreasing the well widths between the cathode and anode sides of the structure. This approach was proposed several years ago by Summers and Brennan under the title variably spaced superlattice energy filters [3]. In their structures the width of adjacent quantum wells was substantially different, which resulted in a distinct peak in the I-V curve for each quasibound level in the structure. In the present structure adjacent wells have a much smaller difference in width, leading to a strong interaction between nearest quasibound levels and giving the broad NDR region that we observe.

The diodes were fabricated from a wafer containing epitaxial layers of $In_{0.53}Ga_{0.47}As$ and AlAs on an n^+-InP substrate. The layers were grown by molecular beam epitaxy at 500°C. The $In_{0.53}Ga_{0.47}As$/AlAs material system was chosen in lieu of the more common GaAs/$Al_xGa_{1-x}As$ system because of its superior resonant-tunneling properties. The tunneling structure consists of four undoped, 1.4-nm-thick AlAs barriers separated by three undoped $In_{0.53}Ga_{0.47}As$ quantum wells of graded width. Starting from the bottom (or substrate) side, the widths of the quantum wells are 4.0, 4.6, and 5.2 nm. Outside of the tunneling structure are lightly doped ($N_D = 2\times10^{16}$ cm^{-3}) spacer layers of thickness 50 and 10 nm on the bottom and top sides, respectively. Outside of the spacer layers are thick n^+ regions doped to $N_D = 1\times10^{18}$ cm^{-3}. The latter regions serve as the top and bottom contacts. Mesas were fabricated by defining 8-μm-square metal pads on the top surface and wet etching to approximately

0.1 nm below the tunnel structure using a H_3PO_4-based wet-etch solution. Electrical contact was made to the top pad by a fine wire and to the bottom of the wafer by soldering.

The experimental room-temperature I-V curve obtained by conventional wafer probing is shown in Fig. 1(a). Negative bias was applied to the top contact, and the solid and dashed lines represent dc-stable and dc-unstable regions, respectively. The I-V curve has three current peaks near bias-voltage magnitudes V_B of 1.6, 2.6, and 3.5 V, and labeled A, B, and C, respectively. The current density at peak A is 1.1×10^4 A cm^{-2}, which is very close to the theoretical value calculated below. At least two closely spaced NDR regions are apparent, containing broad plateaus centered at approximately 1.8 and 2.7 V, and a dc stable positive-resistance region [labeled D in Fig. 1(a)] appears between the current peaks. With positive bias applied to the top contact, the I-V curve displays three well separated current peaks with only the second peak having a substantial NDR region. The positive-biased I-V curve is less interesting than the negative-biased curve and thus will not be discussed further.

In double-barrier RTDs, a plateau-like structure in an NDR region is usually indicative of oscillations occurring between the diode and the measurement circuit. To ascertain the nature of the NDR plateaus in the present diode, we mounted an 8×8-μm device in a coaxial package and induced oscillations with a double-stub tuner connected between the diode package and a microwave spectrum analyzer. Oscillations were observed in the NDR plateaus above current peaks A and B that were similar to the oscillations in single-well RTDs, having a power of a few μW and a frequency that varied greatly with the adjustment of the tuner. However, much more powerful oscillations were observed in the intermediate region D. The most powerful oscillations in this region were 0.44 mW at 4.92 GHz, 0.53 mW at 12.2 GHz, and 0.46 mW at 16.3 GHz. The small change of power with frequency suggests that the maximum frequency at which these oscillations can occur is very high.

The fact that the device oscillates at all values of V_B between 1.6 and 2.9 V indicates that the intrinsic I-V curve (i.e., the I-V curve measured in the absence of oscillation) of this device may contain an NDR region over this entire range. To investigate this possibility, we replaced the coaxial tuner with an attenuator mounted in close proximity to the device to eliminate the circuit resonances. The resulting I-V curve is shown in Fig. 1(b) and displays a nearly continuous NDR region between 1.6 and 2.9 V. The roughness just above the current peak at 1.6 V is thought to be caused by oscillations occurring at frequencies well above the 22-GHz frequency limit of the spectrum analyzer. The 1.3-V width of the NDR region in Fig. 1(b) is much greater than the approximately 0.4-V width of the NDR region in typical single-well RTDs. For comparison, the I-V curve of a single-well $In_{0.53}Ga_{0.47}As/AlAs$ RTD having nearly the

same peak current and cladding-layer doping profile as the present device is shown in Fig. 1(b).

To understand the physical cause of the broad NDR region, we have simulated the electrical current through the triple-well structure using a stationary-state model. In this model the current in each longitudinal energy interval is the product of the quantum-mechanical coherent transmission probability T*T through the structure and the supply function $S(E_L)$ [4] of electrons on the cathode side [5]. The resulting I-V curve for the triple-well structure with negative bias applied to the top contact is shown in Fig. 2. A prominent feature of this curve is the chair-like structure extending between 1.0 and 1.5 V. This behavior is quite unlike anything seen in the theoretical I-V curves of single-well RTDs. As discussed below, it can be explained by the effect of resonant tunneling through two closely spaced levels.

The chair structure in the theoretical I-V curve can be explained by examining separately computed curves of T*T and $S(E_L)$ vs bias voltage. In computing T*T, we assumed that the electric field across the tunnel structure is uniform and took the zero of energy as the conduction band edge on the cathode side. The dependence of T*T and $S(E_L)$ upon energy for several values of V_B is shown in Fig. 3. At zero bias [Fig. 3(a)], T*T displays a triplet of peaks corresponding to the quasibound-state energies for the 4.0-, 4.6-, and 5.2-nm wells of $E_{1,1}$ = 0.143 eV, $E_{1,2}$ = 0.170 eV, and $E_{1,3}$ = 0.204 eV, respectively (the symbol $E_{m,n}$ denotes the mth quasibound level in the nth quantum well from the cathode side). With increasing bias, $E_{1,3}$ drops most rapidly, followed by $E_{1,2}$ and $E_{1,1}$. With just a small bias of V_B = 0.39 V [Fig. 3(b)], the three states approach a point of minimum energy separation and high combined transmission probability. However, practically no current flows at this bias because of the small overlap between T*T and $S(E_L)$.

At V_B = 0.96 V [Fig. 3(c)], corresponding to the current peak in Fig. 2, the overlap between T*T and $S(E_L)$ is large, and the separation between transmission peaks is much greater than at lower voltages because the bias electric field has caused the levels to interchange their order in energy. The dominant transmission peak associated with $E_{1,2}$ is approaching the lower edge of the supply function, which explains the sharp drop at 1.1 V in Fig. 2. Between 1.1 and 1.6 V, the transmission through the structure acquires a mixed nature as the probability of resonant tunneling through $E_{1,2}$ decreases and the probability through $E_{1,1}$ increases. The same type of mixing occurs between $E_{1,2}$ and $E_{1,3}$ at a lower bias field [c.f., Fig. 3(b)], but the overlap between T*T and $S(E_L)$ is so slight that there is no discernable effect in the I-V curve. At the highest V_B of 1.41 V [Fig. 3(d)], the only transmission peak of the triplet that remains within the supply function is $E_{1,1}$. With a further increase in bias, this peak drops below the supply function giving rise to the sharp drop in Fig. 2 at 1.6 V. The sharpness of both drops

results from the narrowness of the quasibound-state transmission resonances for the two levels in the coherent model. Experimentally these resonances are greatly broadened by scattering processes in the structure. The broadening has the effect of smearing out the sharp transitions and rendering a smoother I-V curve like the experimental one in Fig. 1(b).

Two other essential features of the theoretical I-V curve are explained by the behavior of T*T, but are not examined by the graphs presented here for brevity. The small undulation in Fig. 2 just below 0.5 V is caused by the drop of $E_{1,3}$ below the supply function. An NDR region region is not observed because of the small peak magnitude of T*T through $E_{1,3}$ at this bias. The NDR region between 3.4 and 3.6 V in Figs. 1 and 2 is caused by resonant tunneling through $E_{2,3}$. Although the peak transmission through this level is small, the NDR region is substantial because of the large transmission width.

An interesting by-product of the analysis is the close agreement between the experimental and theoretical peak currents in Figs. 1 and 2. This is reminiscent of the favorable comparison of these quantities in single-well RTDs. In the single-well case, it was argued that the inelastic scattering neglected by the coherent model greatly reduces the peak transmission but leaves the integrated transmission unchanged [6,7]. This means that the peak current is also unchanged if the range of high transmission probability in the presence of scattering remains less than the Fermi energy on the cathode side of the structure. The same argument carries over to the multiple-well structures since the physical basis for the argument – the Breit-Wigner formalism of inelastic scattering – also applies to these structures. However, as in the single-well case, the neglect of scattering in the coherent model leads to an underestimation of the current at any of the valley points. For example, the theoretical valley current at 2.1 V in Fig. 2 is approximately three orders of magnitude lower than the corresponding experimental valley current at 2.8 V in Fig. 1(b). This is far greater than the discrepancy that occurs with typical single-well $In_{0.53}Ga_{0.47}As$/AlAs RTDs and is probably caused by a rapid increase in the inelastic scattering probability with the number of quantum wells in the resonant-tunneling structure.

The broadened NDR region of the triple-well RTD should provide a significant advantage over the single-well RTD in terms of oscillator power. To demonstrate this, we compared the oscillator performance of the triple-well RTD with that of the single-well RTD of Fig. 1(b). The results are shown in Fig. 4. Both devices were mounted in the same 50-Ω coaxial resonator for oscillations up to 20 GHz, and the results shown for the single-well RTD at higher frequencies were obtained separately in a waveguide resonator. Near 10 GHz the triple-well RTD generates an output power that is nearly 4 times greater. Further tests of the triple-well RTD are underway at frequencies above 20 GHz. We are also investigating parallel arrays of these

diodes to increase the output power to values well above 1 mW. To date, the highest power obtained from such an array is 5 mW near 1.2 GHz [8].

In conclusion, we have demonstrated an enhanced NDR effect in a triple-well RTD that we attribute to mixed resonant-tunneling through adjacent quasibound levels. This new effect is characterized by a much broader NDR region than occurs in single-well RTDs, which is useful for oscillators and other analog devices. The triple-well diode also represents a return to the superlattice-like structures that promised exciting transport phenomena, such as Bloch oscillations, but never performed as expected. The improved understanding of resonant tunneling acquired through research on single-well structures combined with the steady improvement in heterostructure materials now make such devices realizable.

The authors acknowledge K.M. Molvar for assistance in fabrication, D.L. Landers for help in dicing and bonding, R.A. Murphy for helpful comments, and A.L. McWhorter for a thorough critique of the manuscript. This work was sponsored by the Air Force Office of Scientific Research, the Army Research Office, and NASA.

References

[1] E.R. Brown, J.R. Söderström, C.D. Parker, L.J. Mahoney, K.M. Molvar, and T.C. McGill, Appl. Phys. Lett. 58, 2291 (1991).

[2] E. Ozbay and D.M. Bloom, IEEE Electron Dev. Lett. 12, 480 (1991).

[3] C.J. Summers and K.F. Brennan, Appl. Phys. Lett. 48, 806 (1986).

[4] C.B. Duke, *Tunneling in Solids*, Solid State Physics (Academic, New York, 1969).

[5] R. Tsu and L. Esaki, Appl. Phys. Lett. 22, 562 (1973).

[6] T. Weil and B. Vinter, Appl. Phys. Lett. 50, 1281 (1987).

[7] M. Büttiker, IBM J. Res. Dev. 32, 63 (1988).

[8] K.D. Stephan, E.R. Brown, S.C. Wong, K.M. Molvar, A.R. Calawa, and M.J. Manfra, to be published.

Figure Captions

Fig. 1. (a) Room-temperature I-V curves of triple-well RTD. The dashed regions represent discontinuous transitions resulting from self-rectification of oscillations occurring in NDR regions. (b) I-V curve of the same triple-well RTD as in (a) but mounted in a coaxial package configured to suppress oscillations up to at least 22 GHz. The I-V curve of a single-well RTD having nearly the same peak current is also shown for comparison.

Fig. 2. Theoretical I-V curve of a triple-well RTD, as computed from a stationary-state model of resonant tunneling. The chair-like structure between 1.1 and 1.5 V is caused by mixed resonant tunneling through two adjacent levels of the structure.

Fig. 3. Transmission probability (solid curve) and supply function (dashed curve) for the triple-well RTD at specific bias voltages across the active region of the device. (a) $V_B = 0.0$, (b) $V_B = 0.39$ V, (c) $V_B = 0.96$ V, and (d) $V_B = 1.41$ V. A uniform electric field E_W was assumed to exist across the triple-well structure.

Fig. 4. Oscillation power of the triple-well and single-well RTDs having the I-V curves in Fig. 1(b).

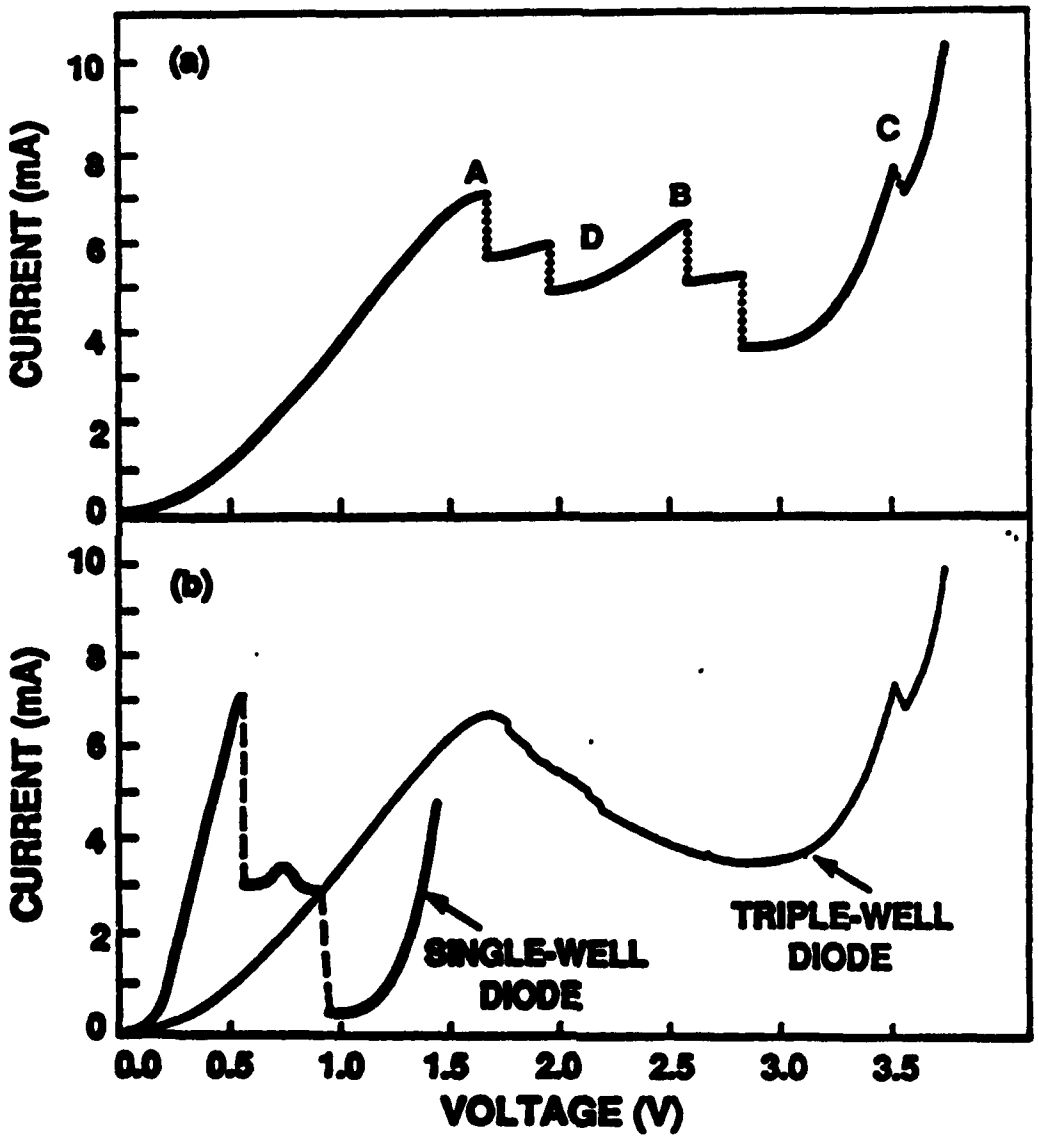
(a)
CURRENT (mA)
10
8
6
4
2
0
A
B
C
D
(b)
CURRENT (mA)
SINGLE-WELL DIODE
TRIPLE-WELL DIODE
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
VOLTAGE (V)

FIGURE 1

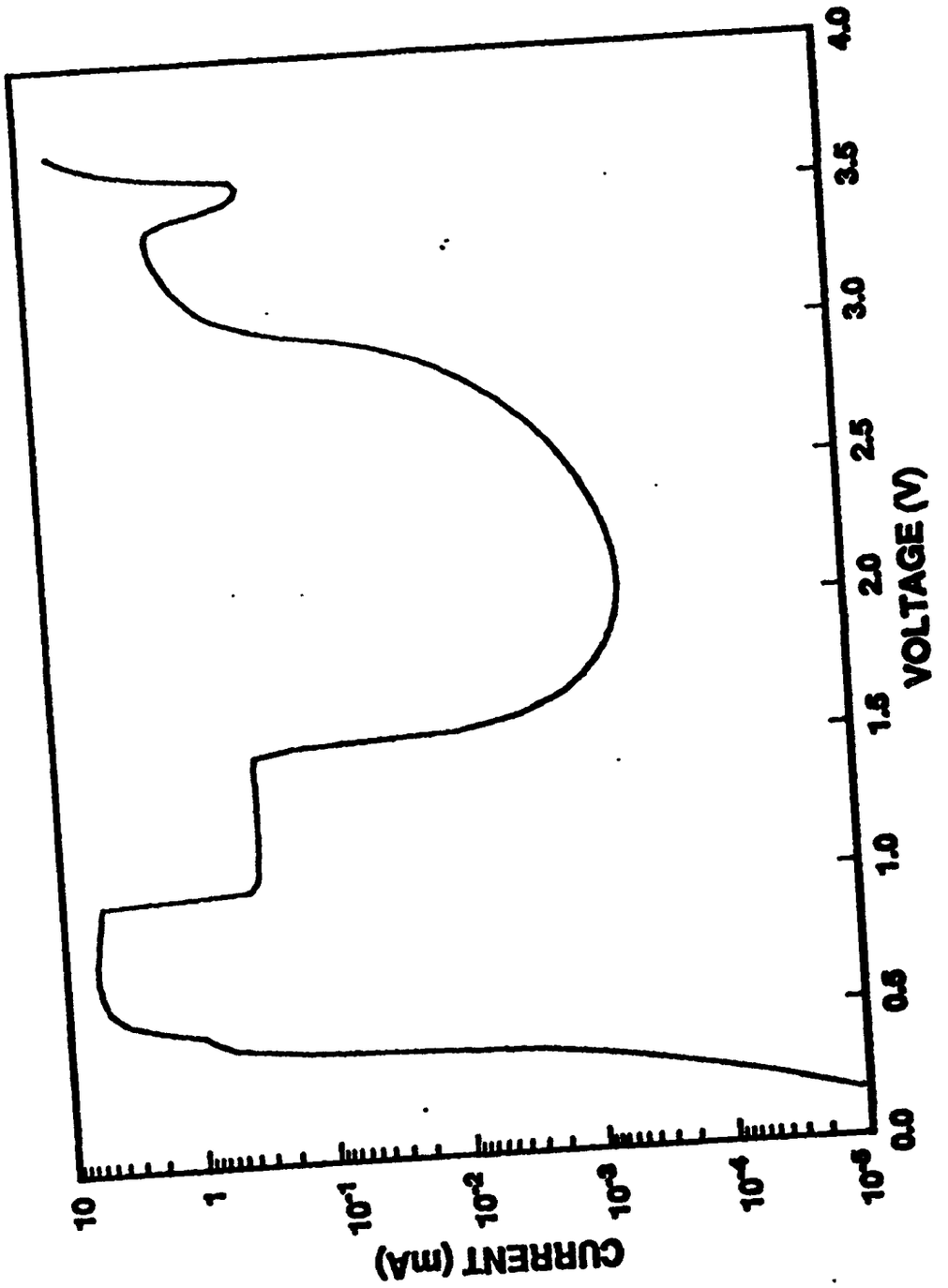
CURRENT (mA)
10
1
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
VOLTAGE (V)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0

FIGURE 2

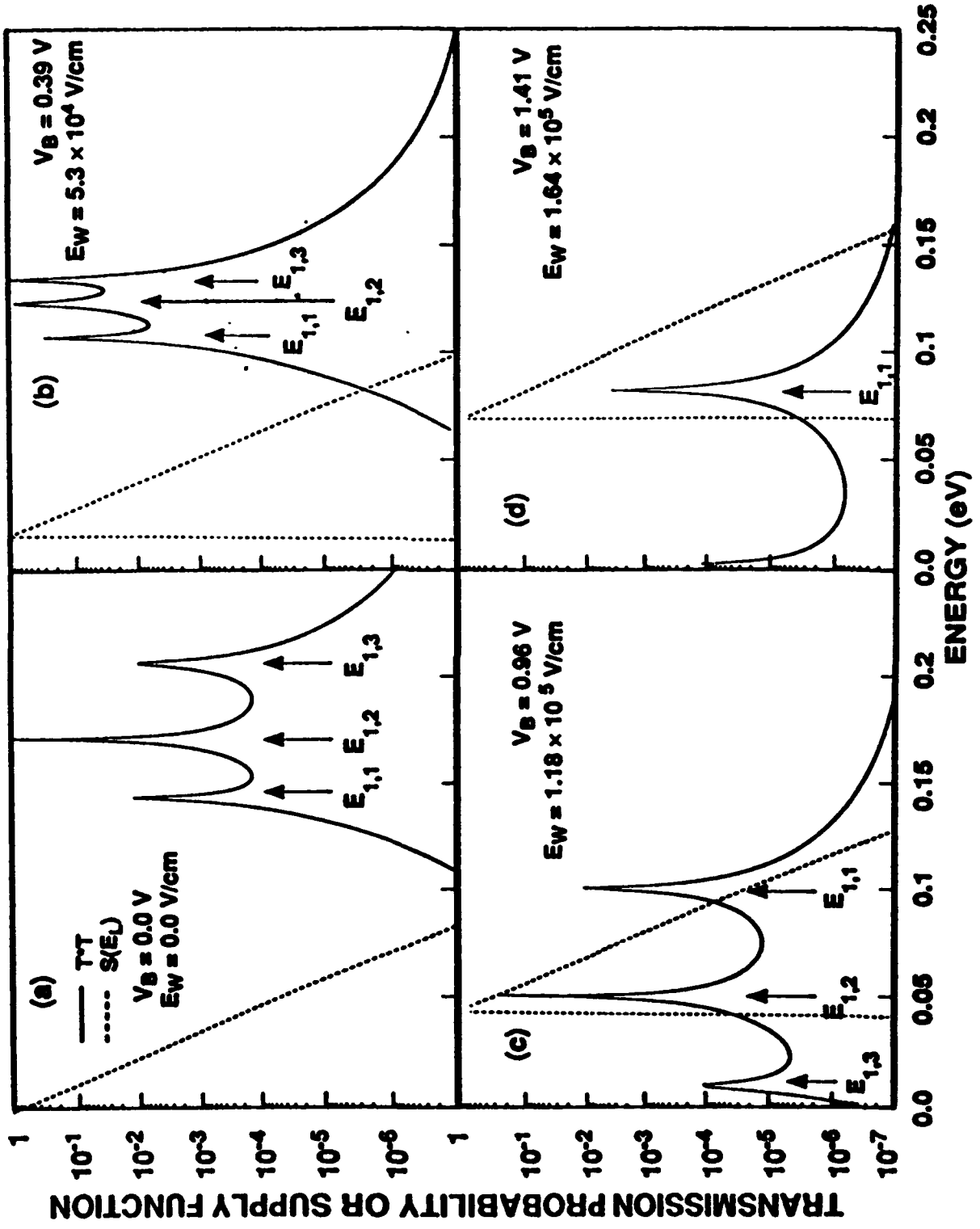
(a)
TT
S(E_L)
V_B = 0.0 V
E_W = 0.0 V/cm
E_1,1
E_1,2
E_1,3
(b)
V_B = 0.39 V
E_W = 5.3 x 10^4 V/cm
E_1,1
E_1,2
E_1,3
(c)
V_B = 0.96 V
E_W = 1.18 x 10^5 V/cm
E_1,1
E_1,2
E_1,3
(d)
V_B = 1.41 V
E_W = 1.64 x 10^5 V/cm
E_1,1
TRANSMISSION PROBABILITY OR SUPPLY FUNCTION
ENERGY (eV)
1
10^-1
10^-2
10^-3
10^-4
10^-5
10^-6
10^-7
0.0
0.05
0.1
0.15
0.2
0.25

FIGURE 3

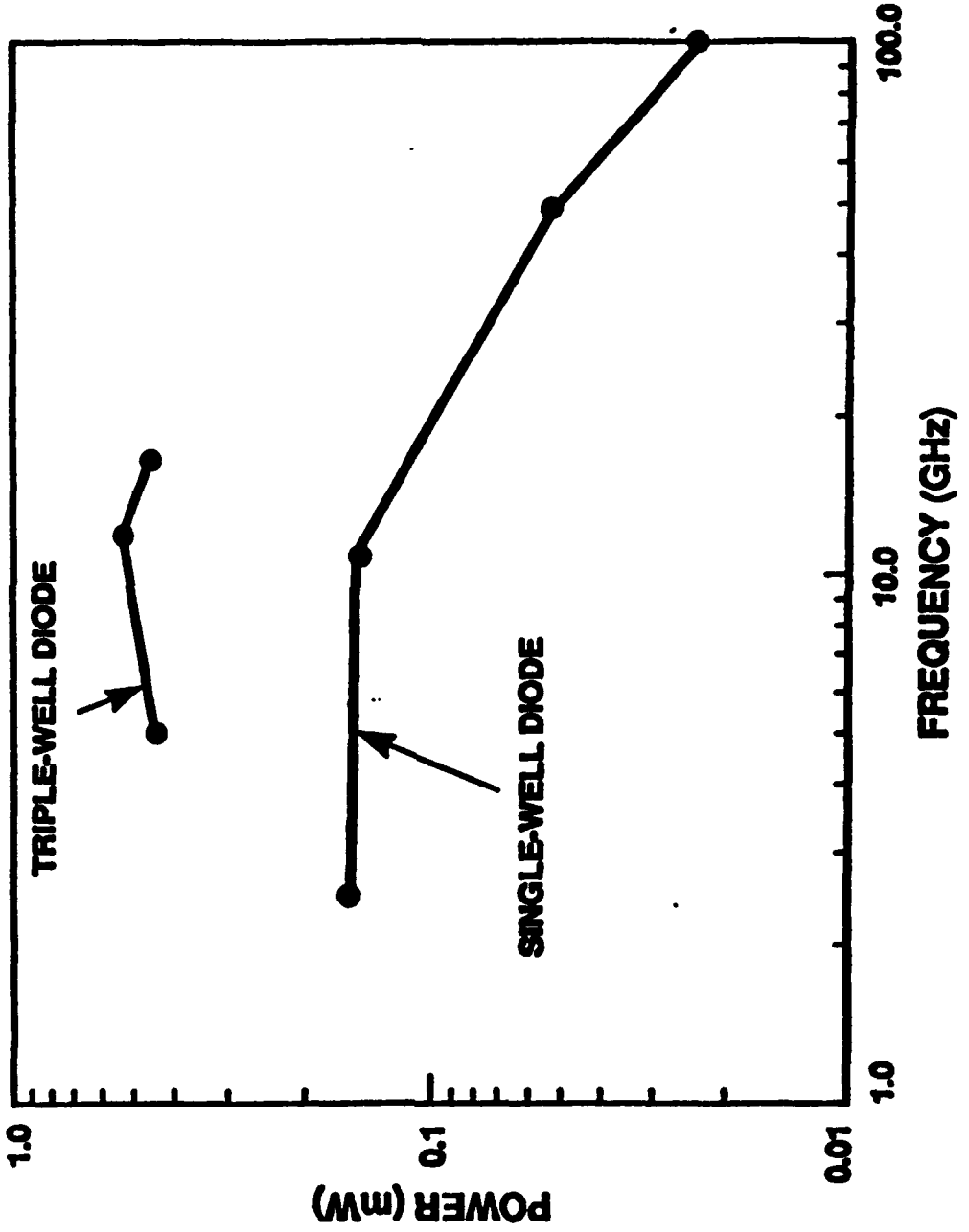
TRIPLE-WELL DIODE
SINGLE-WELL DIODE
POWER (mW)
1.0
0.1
0.01
1.0
10.0
100.0
FREQUENCY (GHz)

FIGURE 4

Growth and characterization of high current density, high-speed InAs/AlSb resonant tunneling diodes

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High quality resonant tunneling diodes have been fabricated from the InAs/AlSb material system (InAs quantum well and cladding layers, AlSb barriers) on (100)GaAs substrates. A diode with a 6.4-nm-thick InAs quantum well and 1.5-nm-thick AlSb barriers yielded a room-temperature peak current density of 3.7×10^5 A cm^{-2} and peak-to-valley current ratio of 3.2. This corresponds to an available current density of 2.6×10^5 A cm^{-2}, which is comparable to that of the best $In_{0.53}Ga_{0.47}As$/AlAs diodes grown on lattice-matched substrates and is three times higher than that of the best GaAs/AlAs diode reported to date. These results were obtained in spite of a 7.2% lattice mismatch between the InAs epilayers and the GaAs substrates, which leads to a measured threading dislocation density of roughly 10^9 cm^{-2}. The experimental peak voltage and current density are in good agreement with theoretical calculations based on a stationary-state transport model with a two-band envelope function approximation.

Since the first observation of negative differential resistance (NDR) in semiconductor resonant tunneling diodes (RTDs),[1] there has been great interest in using these devices in high-speed analog and digital applications. The most promising analog application is oscillators for the terahertz frequency range. RTDs made from the GaAs/AlAs material system (GaAs quantum wells and cladding layers, AlAs barriers) have previously yielded oscillations up to 420 GHz, but various materials parameters presently preclude operation at higher frequencies.[2] In order to circumvent there problems, other material systems such as InGaAs/AlAs (Ref. 3) and InAs/AlSb,[4-7] have been investigated.

In this study we have fabricated three wafers, each containing an InAs/AlSb double-barrier structure designed for high current density and high speed. One of the wafers has yielded RTDs that have oscillated up to about 700 GHz, which is the highest frequency obtained in any solid-state oscillator at room temperatures.[8] The results of the microwave measurements will be presented elsewhere. This letter reports on the epitaxial growth of these devices, the study of their structural properties by transmission electron microscopy (TEM), the measurement of current density versus voltage (J-V) curves of high current density diodes, and the calculation of theoretical J-V curves using a two-band envelope function model.

The epitaxial layers of the three wafers were grown using an MBE system equipped with As and Sb-cracker sources. The InAs and AlSb layers were all grown at 500 °C on (100)GaAs substrates. The active region of each sample consists of an AlSb-InAs-AlSb double-barrier heterostructure, lightly doped InAs spacer layer immediately outside of the barriers, and heavily doped InAs contact layers outside of the spacer layers. In each sample, the InAs/AlSb heterojunctions were grown to be InSb-like in accordance with the suggestion that this leads to fewer surface states than the AlAs-like interface.[9] To achieve the InSb interface at an InAs/AlSb heterojunction, the effusion-cell shutter sequence was to close the In and As shutters and open the Sb shutter simultaneously, wait five seconds, and then open the Al shutter. The inverse sequence was used at the AlSb/InAs heterojunctions.

The epitaxial layers between the substrate and the double-barrier structure are the same in each sample. The bottom buffer layer consists of 500 nm of undoped GaAs. The next layer consists of a five-period $In_{0.7}Ga_{0.3}As$/GaAs (2 monolayers/2 monolayers) superlattice grown at 520 °C. This layer is an attempt to accomodate the $\cong$7.2% lattice mismatch between InAs and GaAs. The following layer is a 1.0-μm-thick InAs buffer that is Si doped to a concentration of $N_D \gtrsim 5\times10^{18}$ cm^{-3}. The InAs layer on top of the buffer is 200 nm thick and is doped n type to $N_D = 2\times10^{18}$ cm^{-3}. This layer is designed to form the anode, or collector region of the biased device. The following InAs spacer layer, which comes directly below the double-barrier structure, is 75 nm thick and is doped to $N_D \cong 2\times10^{17}$ cm^{-3}. This spacer layer is designed to be fully depleted at a bias voltage in the NDR region, so

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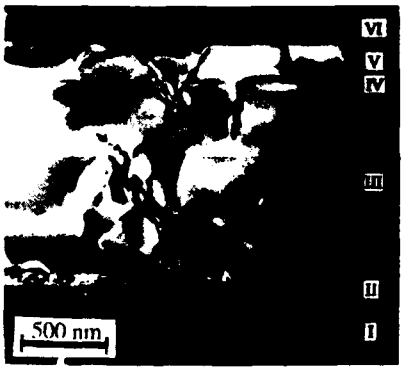

FIG. 1. TEM micrograph of sample B displaying the structural quality of the InAs/AlSb structure grown on GaAs substrates. Label key: (I) GaAs, (II) InGaAs/GaAs superlattice, (III) InAs buffer layer, (IV) InAs/AlSb double-barrier structure, (V) InAs cap layer, and (VI) amorphous silicon from the TEM sample preparation. The lattice mismatch between GaAs and InAs results in a threading dislocation density of about 10^{9} cm^{-2} at the surface of the wafer.

that the specific capacitance of these diodes is low enough for high-speed operation.

The active regions of the three samples differ only in the barrier thickness and in the thickness of the spacer layer above (i.e., opposite to the substrate) the double-barrier structure. In samples A, B, and C, the AlSb barrier thickness is nominally 1.8 nm (6 monolayers), 1.5 nm (5 monolayers), and 1.5 nm, respectively, and the top spacer thickness is 20 nm, 20 nm, and 10 nm, respectively. The InAs quantum well of each sample is 6.4 nm thick and is undoped, and the top spacer layer is doped n type to 2×10^{16} cm^{-3}. From the top of the spacer layer to the surface of the wafer, the epilayers are again the same in each wafer. Immediately above the spacer is a 100-nm-thick layer of InAs doped n type to $N_D = 2\times10^{18}$ cm^{-3}, which corresponds to a Fermi energy of 0.21 eV at room temperature. This is the intended injection layer (i.e., the layer where the band bending across the active region starts). The next epilayer consists of 100 nm of InAs that is heavily doped ($N_D \gtrsim 5\times10^{18}$ cm^{-3}) to improve the quality of the ohmic contact. The ohmic contact is produced *in situ* by depositing 20 nm of indium in the MBE machine before exposing the device to atmosphere.

To determine the material quality of the samples, we carried out TEM measurements in a manner described in Ref. 10. Figure 1 shows a TEM cross-section dark field image ($g = 200$) of sample B. The 7.2% lattice mismatch causes the formation of misfit dislocations in the interface that transform into threading dislocations propagating through the epitaxial film. From Fig. 1, we see that the dislocations penetrate through the InAs/AlSb double-barrier structure without forming any misfit dislocations at the heterointerfaces. A plan-view specimen was also prepared from sample B and the dislocation density at the top of the wafer was measured to be approximately 1×10^{9} cm^{-2}.

The processing of the wafers into diodes was completed by standard fabrication steps, starting with the deposition of 400 nm of gold on top of the 20-nm-thick *in situ* indium layer. Round contacts ranging in diameter from 1 to 8 μm were then patterned, and diodes were isolated by

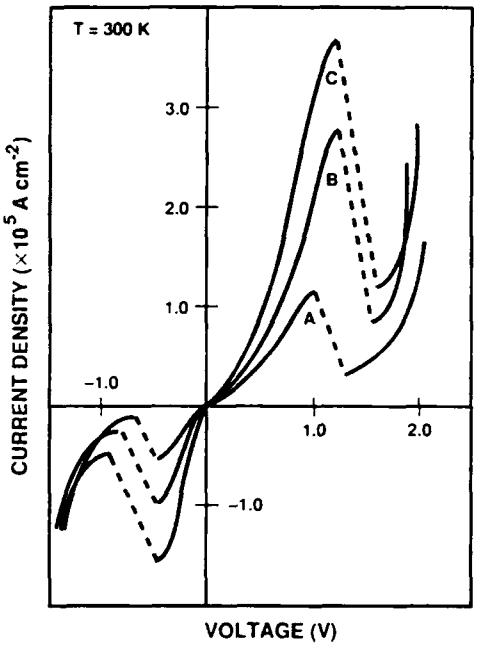

FIG. 2. Experimental current density vs voltage characteristics at room temperature for the three samples studied. At positive bias the peak current densities are 1.1×10^{5}, 2.7×10^{5}, and 3.7×10^{5} A cm^{-2}, and the best peak-to-valley current ratios were 3.5, 3.3, and 3.2 for samples A, B, and C, respectively.

wet chemical etching. The gold-indium contacts were not annealed or alloyed in any way. The experimental room-temperature J-V curves of the three samples are shown in Fig. 2. The polarity of the voltage in Fig. 2 corresponds to the polarity of the voltage applied to the substrate side of the diodes. For each sample the current density is much smaller with negative voltage consistent with the asymmetric doping profile. The 75-nm-thick spacer layer forms a large potential barrier to electrons emanating from the heavily doped contact layer. We will henceforth concentrate on the positive polarity in Fig. 2 since high current density is desirable for high-speed operation. Sample A has a peak current density J_p of about 1.1×10^{5} A cm^{-2} and a peak-to-valley current ratio (PVCR) ranging from 2.7 to 3.5 in diodes measured across the wafer. Sample B has a much larger J_p of 2.7×10^{5} A cm^{-2} with only a slight reduction of the PVCR in the range 2.5 to 3.3. The increased current density reflects the smaller AlSb barrier thickness (1.5 nm) of sample B compared to sample A (1.8 nm). Sample C had the highest J_p of all, $\cong 3.7\times10^{5}$ A cm^{-2}, and a PVCR range of 2.2 to 3.2. The increase in J_p over sample B reflects the reduction in spacer-layer thickness on the top side to 10 nm. These results represent a great improvement over GaAs/AlAs diodes in terms of the available current density, $\Delta J = J_p - J_v$, where J_v is the valley current density. ΔJ is an important figure of merit for RTDs in most applications. For example, sample C yields $\Delta J \lesssim 2.6\times10^{5}$ A cm^{-2}, compared to the best reported value of $\Delta J = 7.8\times10^{4}$ A cm^{-2} GaAs/AlAs diodes.[11] Our ΔJ result is comparable to the best reported value, $\Delta J = 3.2\times10^{5}$ A cm^{-2}, for $In_{0.53}Ga_{0.47}As$/AsAs diodes, which were fabricated on lattice-matched InP substrates.[12]

A comparison of the experimental J-V curves to theoretical prediction has been carried out. The traditional way

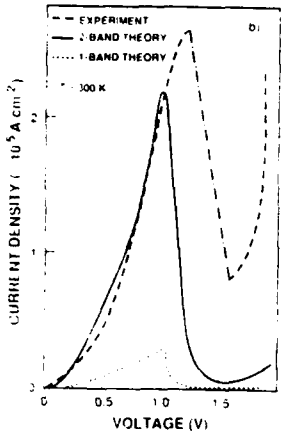

FIG. 3. Comparison of the experimental (dashed line) and theoretical J-V curves for sample B at room temperature. The dash-dot segment of the experimental curve connects the peak point to a bias point lying just above the valley, and is unrelated to the intrinsic J-V curve in the NDR region.

to compute J-V curves for the RTDs is to use the stationary-state method in conjunction with the one-band envelope function (or effective mass) approximation.[13] This method has been used successfully in predicting peak currents and peak voltages, but is likely to fail in InAs/AlSb RTDs because of the small band gap of InAs and because of the type-II (staggered) band offset of the InAs/AlSb heterojunction. This band offset causes the electrons to tunnel through the barriers close to the valence-band edge of the AlSb and requires that the valence band be included to obtain an accurate calculation of the tunneling properties.[14] We have recently developed a stationary-state model with a two-band envelope-function approximation that includes the conduction and light hole valence bands, and incorporates a detailed accounting for the band bending in the tunnel structure.[15]

Theoretical J-V curves for sample B are shown in Fig. 3 along with the experimental J-V curve at room temperature. It is evident that the two-band model provides good agreement with the peak current density and peak voltage, and this is achieved without the use of any fitting parameters. The corresponding theoretical values are both within about 20% of the experimental ones. However, the theory underestimates the valley current by about a factor of twelve. To show the importance of the two-band envelope function model in the present structure, we also plot in Fig. 3 the theoretical J-V curve assuming a one-band model. The one-band model underestimates the peak current by approximately a factor of five. This difference stems largely from the fact that the electrons tunnel from the InAs through the AlSb barrier close to the valence-band edge of the AlSb.

A surprising result of this work is that diodes with such high dislocations densities of 10^9 cm^{-2}, corresponding to about 30 dislocations per 2-μm-diam device, can display excellent resonant tunneling characteristics. Our explanation is that the dislocations are relatively inactive in the tunneling process. We surmise that the dislocations do not provide a low-impedance (i.e., short-circuit) path for electrons, and do not scatter the electrons significantly. The first point is supported by the fact that the experimental peak current density is accurately predicted by theory, and the second point is supported by the fact that the valley current density of our devices is similar to that of lattice-matched GaAs/AlAs or InGaAs/AlAs diodes having comparable peak current density.

In summary, we have fabricated InAs/AlSb double-barrier resonant tunneling diodes with peak current densities up to 3.7×10^5 A cm^{-2} and high peak-to-valley current ratios of 3.2 at room temperature. Because of the 7.2% lattice mismatch between the GaAs substrate and the InAs epilayers, the dislocation density in our diodes is about 1×10^9 cm^{-2}. In spite of this, the peak current density is well explained by a stationary-state transport model with the two-band envelope function approximation. The valley current density predicted by this model is less than the experimental value by a factor that is typical of the discrepancy found in other double-barrier structures such as GaAs/AlAs or $In_{0.53}Ga_{0.47}As$/AlAs. These facts lead us to conclude that threading dislocations are largely inactive in the resonant tunneling process. This is an important conclusion from a technological point of view, since GaAs substrates are much more desirable than the two lattice-matched substrates, InAs or GaSb, for making monolithic integrated circuits.

We wish to thank E. T. Yu of the California Institute of Technology for assistance in the band bending and current density calculations, K. M. Molvar of Lincoln Laboratory for assistance in the fabrication, S. J. Eglash for useful discussions regarding the materials growth, and R. A. Murphy and A. L. McWhorter for important comments on the manuscript. This work was sponsored by the Air Force Office of Scientific Research, the Defense Advanced Research Projects Agency, and NASA.

[1] L. L. Chang, L. Esaki, and R. Tsu, Appl. Phys. Lett. **24**, 593 (1974).
[2] E. R. Brown, T. C. L. G. Sollner, C. D. Parker, W. D. Goodhue, and C. L. Chen, Appl. Phys. Lett. **55**, 1777 (1989).
[3] T. P. E. Broeckaert, W. Lee, and C. G. Fonstad, Appl. Phys. Lett. **53**, 1545 (1988).
[4] L. F. Luo, R. Beresford, and W. I. Wang, Appl. Phys. Lett. **53**, 2320 (1988).
[5] J. R. Söderstrom, D. H. Chow, and T. C. McGill, IEEE Electron Device Lett. **11**, 27 (1990).
[6] C. J. Gulatieri, C. D. Schwarz, R. G. Nuzzo, R. J. Malik, and J. P. Walker, J. Appl. Phys. **61**, 5337 (1987).
[7] C. J. Gulatieri, C. D. Schwarz, R. G. Nuzzo, and W. A. Sunder, Appl. Phys. Lett. **49**, 1037 (1986).
[8] E. R. Brown, C. D. Parker, L. J. Mahoney, J. R. Söderstrom, and T. C. McGill, Abstracts of the 48th Annual IEEE Device Research Conference, June 1990.
[9] G. Tuttle, H. Kroemer, and J. H. English, Mater. Res. Soc. Symp. Proceed. **145**, 415 (1989).
[10] J. Y. Yao and G. L. Dunlop, Inst. Phys. Conf. Ser. No. 93 **2**, 93 (1988).
[11] S. K. Diamond, E. Ozbay, M. J. W. Rodwell, D. M. Bloom, Y. C. Pao, E. Wolak, and J. S. Harris, IEEE Electron Device Lett. **10**, 104 (1989).
[12] T. P. E. Broeckaert and C. G. Fonstad, IEDM Tech. Dig. Washington D. C., December, 559 (1989).
[13] R. Tsu and L. Esaki, Appl. Phys. Lett. **22**, 562 (1973).
[14] G. Bastard, Phys. Rev. B **25**, 7584 (1982).
[15] J. R. Söderstrom, E. T. Yu, M. K. Jackson, Y. Rajakarunanayake, and T. C. McGill, J. Appl. Phys. **68**, 1372 (1990).

APPENDIX F

Effects of Lattice Mismatch on InAs/AlSb Resonant-Tunneling Diodes

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Excellent dc and microwave characteristics have been reported for resonant-tunneling diodes (RTDs) incorporating InAs/AlSb double-barrier structures grown by MBE on GaAs substrates [1,2], even though such structures contain about 10^9 cm^{-2} threading dislocations formed because of the 7% lattice mismatch between InAs and GaAs (Figs. 1 and 2). With the objective of improving device performance by using a lattice-matched substrate, we have fabricated RTDs incorporating an InAs/AlSb double-barrier structure grown on an InAs substrate. This structure has a much lower defect density than a control structure grown on a GaAs substrate, as evidenced by x-ray diffraction and photoluminescence data. However, the decrease in defect density produces only a modest improvement in the dc characteristics of the RTDs on the InAs substrate.

The epilayers grown by MBE include an InAs buffer layer as well as the double-barrier structure. For the epilayers on the InAs substrate, the x-ray rocking curve has a narrow central peak only 14 arc-sec wide (FWHM) and exhibits extensive oscillations that arise from scattering within the double-barrier structure, in good agreement with the simulated curve for a perfect lattice (Fig. 3). In contrast, the epilayers on the GaAs substrate exhibit a rocking curve with only a single broad peak 545 arc-sec wide. For the epilayers on the GaAs substrate, the high density of dislocations broadens the rocking curve and the oscillations are not visible. The band-edge photoluminescence peak at 4.5 K is considerably narrower and about ten times more intense for the sample on InAs than for the one on GaAs (Fig. 4), presumably because the defects in the latter sample act as centers for nonradiative recombination.

Current-voltage characteristics were measured at room temperature for ten RTDs fabricated on each of the two substrates. In all cases the peak current density exceeded 1×10^5 A cm^{-2}. For the devices on the InAs substrate, the average peak-to-valley current ratio is 4.66, compared with an average of 3.50 for the devices on the GaAs substrate (Fig. 5). The peak-to-valley ratios observed for the devices on the InAs substrate are the highest ratios reported for such high-current-density InAs/AlSb RTDs. The improvement observed for the InAs devices results primarily from a reduction in non-resonant current at the valley voltage. Apparently the high dislocation density of the GaAs devices permits the flow of additional non-resonant current, but the magnitude of this excess current is quite small. Since only a small penalty in performance results from using a GaAs substrate, InAs/AlSb RTDs could find application in a number of GaAs-based monolithic integrated circuits.

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References

[1] J.R. Söderström *et al.*, *Appl. Phys. Lett.* 58, 275 (1991).
[2] E.R. Brown *et al.*, *Appl. Phys. Lett.* 58, 2291 (1991).

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Tel: (617) 981-4472; Fax: (617) 981-0122

Suggested Area: Quantum Electronics and Compound Semiconductor Devices

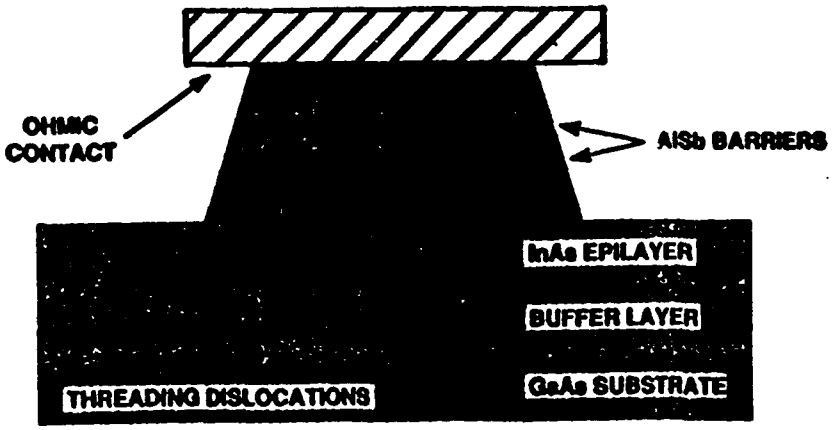

Figure 1. Schematic cross section showing a resonant-tunneling diode mesa on a GaAs substrate. The resonant-tunneling diodes fabricated for this study consist of 1.5-nm-thick AlSb barriers, a 7-nm-thick InAs well, and InAs anode and cathode layers. Samples were grown on InAs and GaAs substrates to investigate the effects of lattice mismatch.

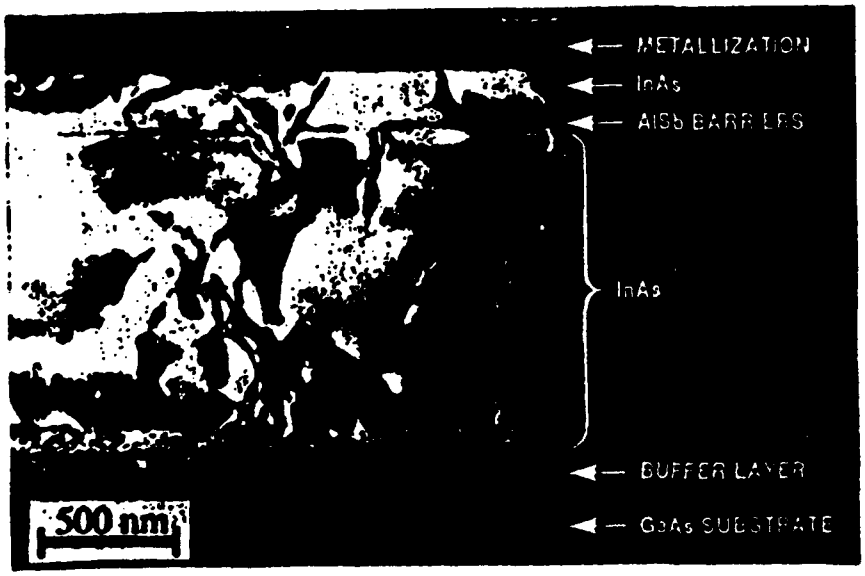

Figure 2. Transmission electron microscopy cross-sectional image of an InAs/AlSb double-barrier structure on a GaAs substrate, nominally identical to the one grown for the present study. Such images show a threading dislocation density of ~ 10^9 cm^{-2} [J.R. Söderström *et al.*, *Appl. Phys. Lett.* 58, 275 (1991)].

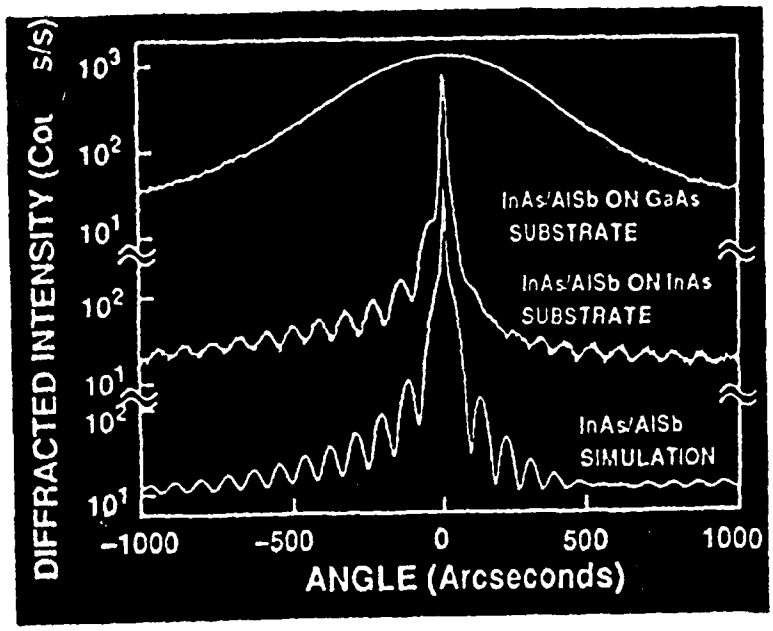

Figure 3. Measured and simulated double-crystal x-ray rocking curves. The lattice-matched sample (InAs substrate) exhibits a rocking curve that is considerably narrower than the mismatched sample (GaAs substrate). The rocking curve from the lattice-matched sample is in good agreement with the simulated curve for a perfect InAs/AlSb double-barrier structure.

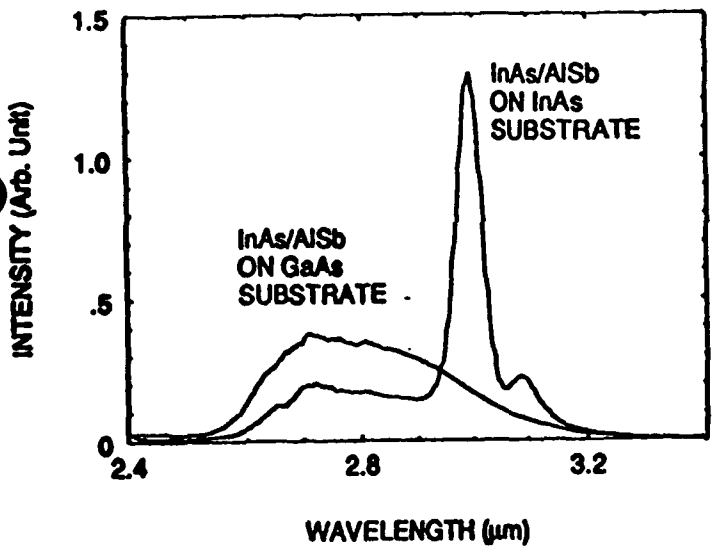

Figure 4. Photoluminescence spectra. The InAs band-edge photoluminescence peak is narrower and more intense for the lattice-matched sample than for the mismatched sample.

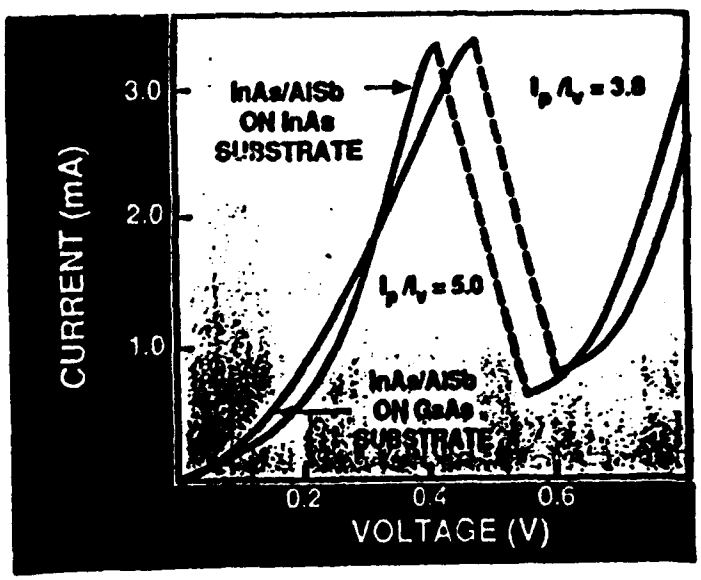

Figure 5. Room-temperature current-voltage characteristics. The lattice-matched sample exhibits a peak-to-valley current ratio 33 percent larger than the mismatched sample. Both diodes display peak current densities in excess of 1×10^5 A cm^{-2}.

APPENDIX G

The Monolithic Optoelectronic Transistor

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Abstract

The monolithic optoelectronic transistor (MOET) is a smart pixel device that uses multiple-quantum-well detectors and modulators, resonant tunneling diodes, and FETs. The growth and fabrication of monolithic arrays of MOETs is discussed.

This work was sponsored by the Defense Advanced Research Projects Agency and the Department of the Air Force.

The Monolithic Optoelectronic Transistor

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The monolithic optoelectronic transistor (MOET) is a smart pixel device that performs thresholding and logic operations and can be tailored either for optical logic applications or for optoelectronically implemented neural networks. It displays optical gain, is cascadable, and has an abrupt switching threshold and saturated "on" and "off" output states.

The circuit of figure 1 shows the operation of the most rudimentary version of the MOET, which performs optical inversion. A p-i-n diode with a multiple-quantum-well (MQW) intrinsic region serves as an input photodetector and a separate one serves as an output modulator. The photocurrent from the input detector flows through a double-barrier resonant tunneling diode (RTD), which has a region of negative differential resistance in its I-V characteristic. When the photocurrent exceeds the peak current of the RTD, the RTD abruptly switches to a higher voltage operating point and this voltage change is amplified by a JFET to drive the output modulator. Since the modulator can be illuminated at much higher optical power than required for switching at the input, the MOET displays optical gain. We project that the MOET will switch in 10 ns with 10 μW of input power, or a switching energy of 100 fJ.

The p-i-n detector/modulator structure uses an asymmetric Fabry-Perot to achieve a high contrast reflection modulator and a highly efficient photodetector. This structure requires high purity and low background doping in the MQW, good control of layer thicknesses, and very high uniformity in layer thickness (<0.1%) over the area of an array. Using gas-source MBE, we have grown a detector/modulator structure with 65:1 contrast at 8 V, high quantum efficiency as a photodetector, and high thickness uniformity (0.3% over a 2-inch wafer).

The RTD peak current determines the input optical power required for switching. Therefore, high optical gain requires an RTD with low peak current. A systematic study to optimize barrier composition has yielded RTDs with peak current densities under 100 A/cm^2 with peak-to-valley current ratios of more than 2.

We discuss the growth and fabrication of the MOET structure and the successful achievement of high performance in each of its critical components. Alternative versions of the MOET will be described.

This work was sponsored by the Defense Advanced Research Projects Agency and the Department of the Air Force.

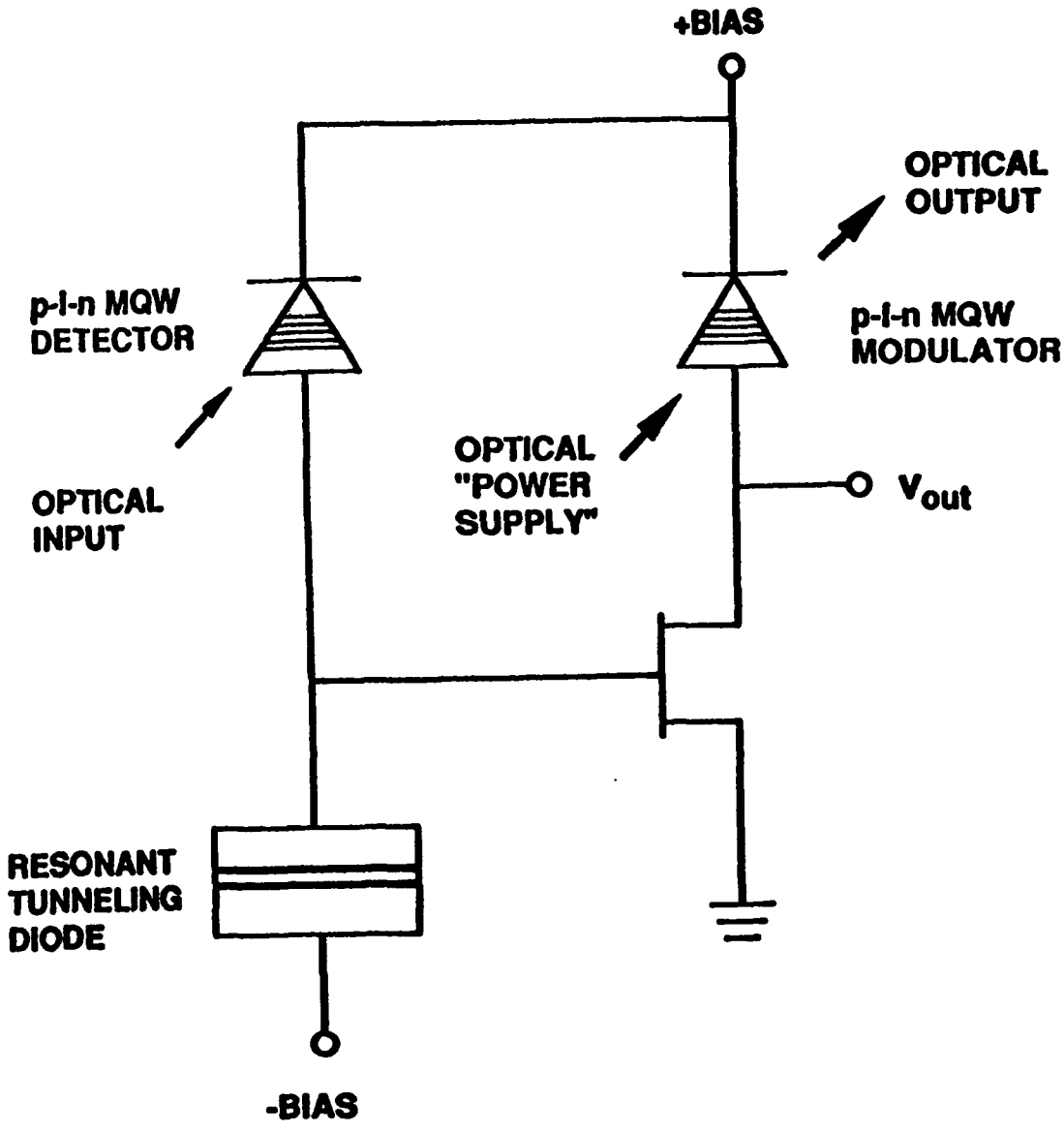

Figure 1 The circuit of the monolithic optoelectronic transistor

APPENDIX H

Oscillations up to 712 GHz in InAs/AlSb resonant-tunneling diodes

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Oscillations have been obtained at frequencies from 100 to 712 GHz in InAs/AlSb double-barrier resonant-tunneling diodes at room temperature. The measured power density at 360 GHz was 90 W cm^{-2}, which is 50 times that generated by GaAs/AlAs diodes at essentially the same frequency. The oscillation at 712 GHz represents the highest frequency reported to date from a solid-state electronic oscillator at room temperature.

The double-barrier resonant-tunneling diode (RTD) has demonstrated useful high-speed characteristics as an oscillator and a switch. Until recently most of the high-speed experiments have been conducted with RTDs made from the GaAs/AlAs material system (GaAs quantum well and cladding layers, AlAs barriers). Oscillators made from such diodes have operated at room temperature up to 420 GHz.[1] Switches have been demonstrated with peak-to-valley switching times of 2 ps,[2] and 6–10 ps.[3] It has been argued that the oscillator frequency and the switching speed of GaAs/AlAs RTDs are limited primarily by the *RC* time delay in the negative-differential conductance (NDC) region of the current-voltage (*I-V*) curve.[1,4] In this letter, we present experimental oscillations from InAs/AlSb RTDs at frequencies up to 712 GHz. These results are consistent with a theoretical maximum frequency of oscillation f_{max} of 1.24 THz. According to our estimates, this f_{max} is limited more by the resonant-tunneling traversal and depletion-layer transit times than by the fundamental *RC* time delay of the device.

The InAs/AlSb materials system has several advantages over GaAs/AlAs for making high-speed RTDs.[5] First, the InAs/AlSb band offset (staggered type II at the Γ point) allows an electron to tunnel through an AlSb barrier with a smaller attenuation coefficient than it would have at the same energy in the AlAs barrier of a GaAs/AlAs structure (type-I band offset). This leads to a higher available current density ΔJ for a given barrier thickness, where $\Delta J = J_P - J_V$, and J_P and J_V are the peak and valley current densities, respectively. A higher ΔJ usually leads to a reduced *RC* time delay in RTDs. A second advantage is that electrons will drift across a given depletion layer much more rapidly in InAs than in GaAs provided that this layer is narrow enough ($\lesssim 0.1$ μm) or the voltage drop is small enough to maintain a low probability of impact ionization.[6] A shorter depletion-layer transit time in RTDs generally raises the f_{max}, as expected intuitively.[1] A third advantage is that InAs RTDs have a lower total series resistance R_s, which always increases the f_{max}. The lower R_S follows from the higher mobility of electrons in InAs (for any fixed *n*-type doping concentration) and the lower specific resistance of ohmic contacts.

One InAs/AlSb wafer (referred to as wafer B in Ref. 5) was used to make RTDs for the present work. It was grown by molecular beam epitaxy on semi-insulating (100)GaAs substrates at 500 °C. The double-barrier structure consists of two 1.5-nm-thick undoped AlSb barriers separated by a 6.4-nm-thick undoped InAs quantum well. Diode mesas are fabricated by first defining gold pads on top of the wafer by a photoresist liftoff technique. Approximately 500 nm of the epilayer material is then removed by wet chemical etching using the gold pad as a mask. The exposed surface of the etched wafer is a 1.0-μm-thick InAs epilayer doped to $N_D = 5\times10^{18}$ cm^{-3}. Further details regarding the fabrication are given in Ref. 5.

In preparation for high-frequency experiments, the fabricated wafer was diced into 100×100 μm chips and the sidewalls of the chips were plated with palladium and gold. This procedure creates a very low resistance current path between the diode mesas and the ground plane, which is the bottom surface of the chip. Between a mesa and the top edge of the chip, the current flows in the $N_D = 5\times10^{18}$ cm^{-3} InAs layer. From the top edge to the bottom edge, the current flows in the sidewall metalization. The dc current-voltage (*I-V*) characteristic of a 1.8-μm-diam diode is given in Fig. 1 with negative voltage applied to the top contact. The *I-V* curve shows a peak-to-valley current ratio of about 3.4 at room temperature, and a peak current density of 2.8×10^5 A cm^{-2}, corresponding to $\Delta J \cong 2.0\times10^5$ A cm^{-2}. The discontinuous nature of the experimental *I-V* curve in the NDC region is caused by self-rectification of the oscillations.[7]

To study these diodes as oscillators, the chips were mounted in one of four full-height rectangular waveguide resonators operating in frequency bands around 100, 200, 400, and 650 GHz, respectively. The design of the first three resonators and the techniques used to measure power and frequency in these bands are the same as used in previous experiments.[1] The highest power density obtained by

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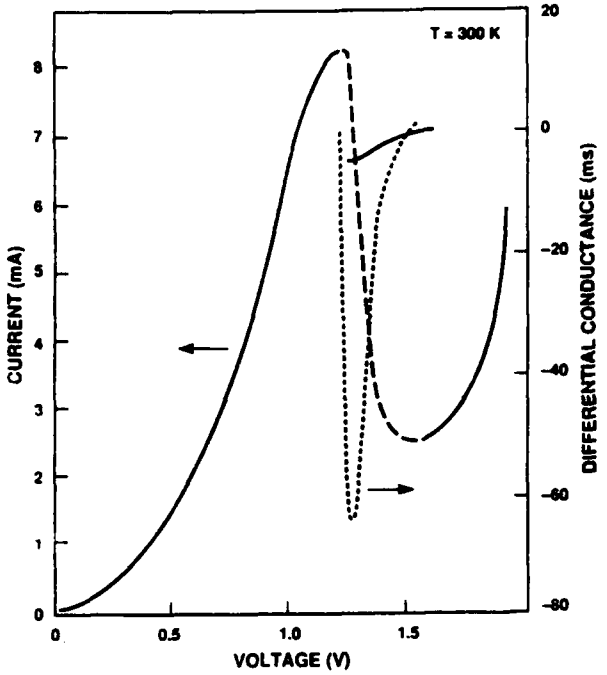

FIG. 1. Room-temperature I-V curve (solid line) of a 1.8-μm-diam InAs/AlSb RTD measured while the diode was oscillating near 360 GHz. The step structure spanning the NDC region is caused by rectification of the oscillations. The long-dashed curve connecting the peak and valley points is a physical model of the (stable) I-V curve that would be measured in the absence of oscillations. The short-dashed line is the G-V curve (right-hand scale) derived from the model I-V curve.

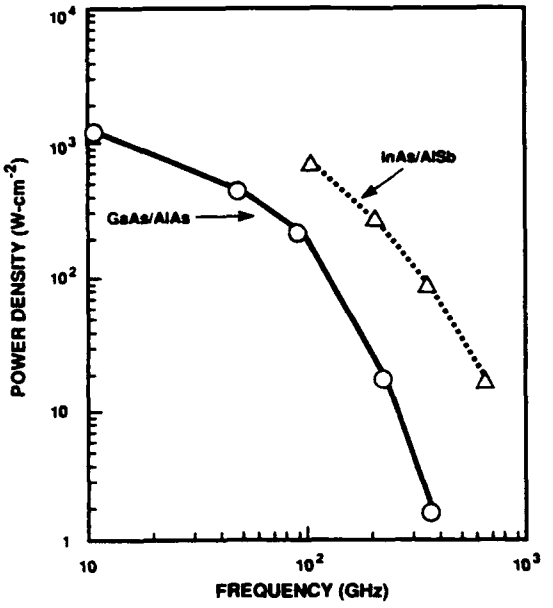

FIG. 2. Experimental oscillator results for the InAs/AlSb RTD (solid line) and the best GaAs/AlAs (dashed line) tested to date. All of the oscillations were obtained at room temperature.

1.8-μm-diam diodes in each of the resonators is shown in Fig. 2. At 360 GHz an absolute power of 3 μW was obtained, corresponding to a power density of 90 W cm^{-2}. This is 50 times the power density obtained previously from GaAs/AlAs RTDs at 370 GHz, and is indicative of a very high f_{max}, as discussed later.

The highest frequency oscillations were obtained in a 0.030×0.015 cm rectangular waveguide resonator designed to operate between roughly 600 and 750 GHz. The highest power obtained in this resonator was 0.3 μW from a 1.8-μm-diam InAs/AlSb RTD oscillating at 712 GHz. This corresponds to a power density of 15 W cm^{-2}. Our uncertainty in these values is about 50%, reflecting the difficulty in calibrating the power measurements in this frequency region. The power was measured by coupling the radiation out of the waveguide with a pyramidal feedhorn and focusing it onto a composite bolometer. The oscillation frequency was measured by placing a scanning Fabry–Perot spectrometer in the path between the waveguide oscillator and the bolometer. By scanning one mirror of the spectrometer over a distance of about 5 cm, we were able to determine the wavelength to an accuracy of 0.1 %. Using the spectrometer, we looked for changes in the oscillation frequency with variations in the position of the waveguide backshort. We found that the backshort tuned the output frequency by about 2 GHz. This tuning would probably not be observed if the oscillation was a second or higher harmonic since propagation at the fundamental frequency would not occur in the waveguide, and thus the oscillation frequency would not depend on the backshort position. However, second (or higher) harmonic tuning effects cannot be ruled out, and better techniques are needed for this determination.

We estimate the f_{max} of the present diodes by applying a small-signal electrical model recently developed for the RTD.[1] The basis for the model is a lumped-element equivalent circuit consisting of the parallel combination of a conductance G and a capacitance C, in series with R_S. The quantity G is the differential conductance across the active region of the device, C accounts for the accumulation and depletion space-charge layers on the cathode and anode sides, respectively, of the double-barrier structure, and R_S is the sum of the ohmic-contact resistance and the spreading resistance from the RTD mesa to the ground plane of the chip. At high frequencies or short time scales, this circuit must be generalized to account for several time-delay mechanisms. The resonant-tunneling traversal time is included by replacing G with a resonant-tunneling admittance, $G(1 + i\omega\tau_1)^{-1}$, where τ_1 is the quasibound-state lifetime. This is equivalent to adding an inductance, $L_{QW} = \tau_1/G$, into the basic circuit. The effect of the depletion-layer transit time is included through an ac analysis in which the electron is assumed to cross the depletion layer with a uniform drift velocity v_D, but the double-barrier structure remains as a lumped-element (injection admittance) proportional to $G(1 + i\omega\tau_1)^{-1}$. The classical skin effect confines the ac current to a surface layer having a thickness roughly equal to the skin depth, and thus it causes R_S to increase slowly with frequency. All parameters in the model other than G depend weakly on bias voltage and thus are assumed to be constant throughout the NDC region.

We estimate G from a theoretical model of the (stable) I-V curve in the NDC region. The theoretical NDC region shown in Fig. 1, is the sum of a resonant-tunneling and an

excess-current component. The resonant-tunneling component is based on the stationary-state tunneling integral with a Breit–Wigner form for the transmission probability.[8] The excess-current component is a second-order polynomial in V. It is not possible to estimate G from the experimental I-V curve since this curve is highly distorted by the oscillation. We determine τ_1 from separate numerical calculations of the full width at half maximum, Γ_1, of the transmission probability T^*T, using a two-band model for the tunneling dispersion relation in the barriers. The result is $\tau_1 = \hbar/\Gamma_1 = 90$ fs. The capacitance is approximated by $C = \epsilon a(L_D + L_W + L_A)^{-1} = 2.8$ fF, where a is the RTD area (2.5×10^{-8} cm^2), L_W is the width of the double-barrier structure (9.4 nm), L_D is the width of the depletion layer ($\simeq$75 nm), and L_A is the width of the accumulation layer ($\sim$20 nm). The values of L_D and L_A are taken from the solution to Poisson's equation with the peak voltage applied across the device. The drift velocity across the depletion layer, $v_D = 8\times10^7$ cm s^{-1}, is obtained from the results of Monte Carlo simulations of electron transport in InAs under conditions similar to those in the depletion layer at the peak voltage.[6] The ohmic contact resistance is assumed to be 2 Ω in accordance with a specific contact resistance of $\rho_C = 5\times10^{-8}$ Ω cm^2. This ρ_C was estimated from transmission-line-model (TLM) measurements made on separate InAs ohmic contacts.[9] The frequency-dependent spreading resistance is approximated as 1.0 Ω at dc and 1.5 Ω at 600 GHz, based on a resistivity of 0.0003 Ω cm in the InAs epilayer doped to $N_D = 5\times10^{18}$ cm^{-3}.

The small-signal model yields a quantity, called the resistive cutoff frequency f_R, at which the real part of the terminal impedance equals zero. This is a frequency above which oscillation cannot occur. We plot f_R in Fig. 3 as a function of G with the other parameters held constant. This curve displays a peak value of 1.24 THz at $G = -20$ mS. This is a realizable G since it is less in magnitude than the minimum G (-64 mS) in the theoretical NDC region in Fig. 1. Thus, 1.24 THz is the f_{max} of this RTD.

The presence of the peak in the f_R vs G curve is a consequence of the series resistance in the model. To understand this, note that the basic G-C-R_S circuit yields $f_R = (2\pi C)^{-1}(-G/R_S - G^2)^{1/2}$. This expression displays a peak value of $(4\pi CR_S)^{-1}$ at $G = (2R_S)^{-1}$. The addition of the lifetime and transit time delays leads to a reduction in the f_{max} (and a reduction in the G at which the f_{max} occurs), but it does not change the peaked nature of the f_R vs G curve. The basic circuit can also be described by an RC time constant, $\tau_{RC} = C(-G/R_S - G^2)^{-1/2}$. Over the range of the G-V curve in Fig. 1 (and assuming $R_S = 3$ Ω and $C = 2.8$ fF) this expression yields a minimum value of $\tau_{RC} = 21$ fs at $G = -64$ mS. This is much less than τ_1 (90 fs) or the depletion-layer transit time ($L_D/v_D = 94$ fs). Therefore, we believe that the speed of this RTD is not limited by the fundamental RC time delay, and that changes in the materials parameters (such as thinner AlSb barriers to decrease τ_1 or optimization of the InAs depletion layer to reduce the effect of transit time) could further increase the f_{max}. The difference between the present τ_{RC} and that of the best GaAs/AlAs RTDs ($\tau_{RC} > 100$ fs) is attributed in part to the four times larger ΔJ of the InAs/AlSb RTD, and in part to the lower series resistance (at least three times lower specific contact and spreading resistances). The larger ΔJ is responsible for the fact that the minimum G in Fig. 1 is about ten times larger in magnitude than the minimum G of a GaAs/AlAs RTD having the same area.

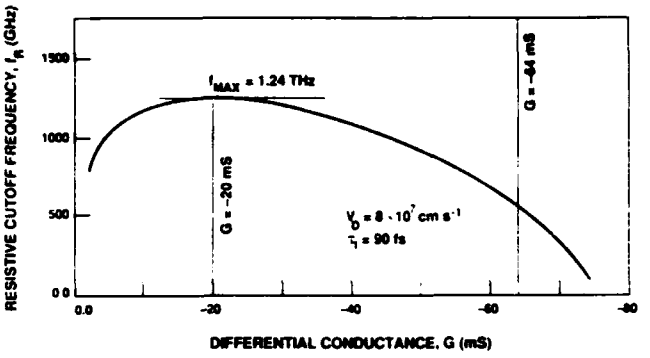

FIG. 3. Theoretical resistive cutoff frequency vs differential conductance for a 1.8-μm diam InAs/AlSb RTD obtained from the small-signal impedance model of the device.

In summary, an InAs/AlSb RTD has oscillated up to 712 GHz at room temperature, and has generated a 50 times higher power density at 360 GHz than GaAs/AlAs RTDs operating near the same frequency. We emphasize that these results were obtained with RTDs containing a 7% lattice mismatch between the active epitaxial layers and the semi-insulating GaAs substrate.[5] This suggests that InAs/AlSb RTDs could find application in a number of monolithic integrated circuits, such as planar oscillator arrays and signal-processing circuits, for which semi-insulating GaAs is the most desirable III-V substrate material.

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[1] E. R. Brown, T. C. L. G. Sollner, C. D. Parker, W. D. Goodhue, and C. L. Chen, Appl. Phys. Lett. **55**, 1777 (1989).
[2] J. F. Whitaker, G. A. Mourou, T. C. L. G. Sollner, and W. D. Goodhue, Appl. Phys. Lett. **53**, 385 (1988).
[3] S. K. Diamond, E. Ozbay, M. J. W. Rodwell, D. M. Bloom, Y. C. Pao, E. Wolak, and J. S. Harris, Jr., in *OSA Proceedings on Picosecond Electronics and Optoelectronics* (Optical Society of America, Washington, D.C., 1989), Vol. 4, pp. 101, 105.
[4] S. K. Diamond, E. Ozbay, M. J. W. Rodwell, D. M. Bloom, Y. C. Pao, and J. S. Harris, Jr., Appl. Phys. Lett. **54**, 153 (1989).
[5] J. R. Söderström, E. R. Brown, C. D. Parker, L. J. Mahoney, and T. C. McGill, Appl. Phys. Lett. **58**, 275 (1991).
[6] K. Brennan and K. Hess, Solid-State Electron. **27**, 347 (1984).
[7] H. C. Liu, Appl. Phys. Lett. **53**, 485 (1988).
[8] E. R. Brown, W. D. Goodhue, and T. C. L. G. Sollner, J. Appl. Phys. **64**, 1519 (1988).
[9] E. R. Brown, S. J. Eglash, and C. L. Chen (unpublished).

APPENDIX I

High-speed resonant-tunneling diodes made from the $In_{0.53}Ga_{0.47}As$/AlAs material system

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ABSTRACT

New double-barrier resonant-tunneling diodes have been fabricated in the pseudomorphic $In_{0.53}Ga_{0.47}As$/AlAs material system that have peak current densities exceeding 1×10^5 A cm^{-2} and peak-to-valley current ratios of approximately 10 at room temperature. One of these diodes yielded oscillations up to 125 GHz, but did not oscillate at higher frequencies because of a large device capacitance. A device with a much lower capacitance is estimated to have a maximum oscillation frequency of 932 GHz and a voltage rise time of 1.5 ps in switching from the peak bias point to the valley bias point. Other reported $In_{0.53}Ga_{0.47}As$/AlAs diodes are analyzed and yield theoretical maximum oscillation frequencies over 1 THz and rise times as low as 0.3 ps.

1. INTRODUCTION

Resonant tunneling continues to draw the interest of physicists and device engineers alike because it is one of the few solid-state transport processes that can provide a fast negative differential resistance (NDR). The most studied resonant-tunneling device to date is the double-barrier diode (DBD), which consists essentially of two layers of a semiconductor material embedded in another semiconductor of smaller bandgap. The wider-bandgap layers act as barriers to electrons and are separated by a distance sufficiently small to allow spatial quantization to occur in the quantum-well region between them. Electrons can transit the double-barrier structure with high probability if they have a longitudinal energy equal to the energy E_n of one of the quasibound states. If the quantization is strong (i.e., $E_1\tau_s/\hbar \gg 1$, where τ_s is the scattering time), then the current-voltage (I-V) characteristic will display an NDR region, as first observed by Chang, Esaki, and Tsu [1]. The requirement of spatial quantization imposes limits on the overall size of the double-barrier structure. It is found empirically that the thickness of the GaAs quantum well and AlAs barriers of a GaAs/AlAs structure must be less than about 6 nm and 3 nm, respectively, in order to observe NDR at room temperature. In addition, the heterojunctions forming each face of the barrier must be smooth on an atomic scale so that transverse crystal momentum is conserved while electrons tunnel through. Fortunately, barriers as thin as three or four monolayers and as smooth as one monolayer (i.e., the thickness fluctuates by only one monolayer) can be obtained by modern crystal growth techniques, such as molecular-beam epitaxy.

The NDR region of the DBD has been used for high-frequency oscillations and high-speed switching. For example, DBDs made in the GaAs/AlAs system have demonstrated

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room-temperature oscillations up to 420 GHz [2] and a switching time from the peak to the valley points of 2 ps [3]. These results are impressive, but they fall short of practical performance requirements in some important respects. For the oscillator, the power and power density (output power per unit diode area) obtained around 400 GHz were only about 0.2 μW and 2 W cm^{-2}, respectively. Most applications in this frequency range, such as local oscillators for superconducting tunnel-junction mixers, require power levels of at least 1 μW [4]. For the switch, the 2-ps result was obtained in an electro-optic sampling experiment using significant overdrive (i.e., driving a switch beyond threshold in a time of the order of the switching time). Circuits employing less overdrive have yielded switching times of 6 ps or longer [5]. Overdrive requirements decrease the allowable device variability in a circuit, so higher speed with reduced overdrive is highly desirable for circuit applications.

In this study, we show that the oscillator and switch performance are significantly improved in DBDs made from the $In_{0.53}Ga_{0.47}As$/AlAs material system. This is largely because InGaAs/AlAs diodes provide a very high peak-to-valley current ratio (PVCR) compared to GaAs/AlAs diodes with the same peak current density J_P. As a result the InGaAs diodes have a significantly higher available current density ΔJ, which is defined as the difference between the peak and valley current densities, $J_P - J_V$, and is an important parameter for all high-speed applications.

2. DEVELOPMENT OF InGaAs/InAlAs DOUBLE-BARRIER DIODES

The first demonstration of DBDs in the $In_{0.53}Ga_{0.47}As$/InAlAs material system was carried out at Fujitsu [6,7]. The $In_{0.53}Ga_{0.47}As$ alloy was chosen for the quantum well and cladding layers because it is lattice matched to InP, which is available in high-quality substrates. Two different barrier compositions were used: (1) $In_{0.52}Al_{0.48}As$, which is lattice matched to $In_{0.53}Ga_{0.47}As$, and (2) AlAs, which has a 3.5% smaller lattice constant than $In_{0.53}Ga_{0.47}As$. The $In_{0.52}Al_{0.48}As$- and AlAs-barrier diodes yielded PVCRs of 2.3 and 14, respectively, at room temperature. Subsequent progress has been made with both barrier compositions [8,9], but the $In_{0.53}Ga_{0.47}As$/AlAs diodes maintain a big advantage. The highest PVCR and ΔJ reported for these diodes to date is 30 [9] and 3.2×10^5 A cm^{-2} [10], respectively, at room temperature. The reason for this advantage is presumably that an AlAs barrier causes little or no alloy-related scattering compared to a ternary InAlAs barrier. This assumes that the thickness of the barrier is small enough ($\lesssim$ 3 nm) so that the AlAs material is pseudomorphic to $In_{0.53}Ga_{0.47}As$, and thus has a negligible concentration of misfit dislocations.

The $In_{0.53}Ga_{0.47}As$/AlAs DBDs provide a significantly higher PVCR than the best GaAs/AlGaAs diodes. Extensive development of GaAs/AlGaAs DBDs has resulted in maximum room-temperature PVCRs of only 4 in diodes having low J_P, and about 2 or less in diodes having a J_P over 1×10^5 A cm^{-2}. Initially, the superiority of the $In_{0.53}Ga_{0.47}As$/AlAs diodes was attributed to the large energy separation, ~ 0.65 eV, between the Γ conduction-band minimum in the $In_{0.53}Ga_{0.47}As$ and the X conduction-band minimum in the AlAs barrier [7]. This quantity is estimated to be 0.13 eV in the GaAs/AlAs, and has been correlated to the excess valley current in those diodes [11]. More recently, it has been realized that the lower effective mass ($m^* = 0.042\ m_0$) of the $In_{0.53}Ga_{0.47}As$ compared to GaAs ($m^* = 0.067\ m_0$) also contributes to the difference since a lower effective mass is consistent with a weaker interaction between electrons and longitudinal optical phonons, and between electrons and acoustical phonons. These scattering mechanisms can induce significant excess

current at the valley voltage and beyond when they occur in the accumulation region adjacent to the double-barrier structure [12]. We also believe that polar-mode acoustical-phonon (i.e., piezoelectric) scattering plays an important role, but to our knowledge this mechanism has not been analyzed for DBDs. Other advantages of the $In_{0.53}Ga_{0.47}As$ over the GaAs include a much lower Schottky-barrier height ($\cong$ 0.2 eV for common metals compared to $\cong$ 0.8 eV for GaAs), and a greater solid-state solubility for n-type dopants. Both of these factors lead to a much lower series resistance for the InGaAs diodes, which is very important in high-speed devices.

3. NEW $In_{0.53}Ga_{0.47}As$/AlAs DOUBLE-BARRIER DIODES

Three different $In_{0.53}Ga_{0.47}As$/AlAs DBD structures, henceforth called devices 1, 2, and 3, were fabricated for the present study. Pseudomorphic AlAs barriers were chosen over lattice-matched $In_{0.52}Al_{0.48}As$ ones because of their superior performance discussed above. All of the structures were grown by molecular-beam epitaxy on n^+-InP substrates at a temperature of 470°C. After completing the epitaxial growth, round Ni/Ge/Au contacts ranging in diameter from 1 to 8 μm were patterned on the top surface of the wafer by photoresist liftoff techniques. Mesa diodes were then defined by either wet-chemical etching or reactive ion etching using CH_4:H_2. In both cases the top metallization was used as an etch mask. The final fabrication step was to dice the wafer into roughly 0.02 cm square chips suitable for packaging into high-frequency oscillator circuits.

Device 1 is composed of 6-monolayer-thick (~ 1.7 nm) AlAs barriers separated by a 16-monolayer-thick (~ 4.7 nm) quantum well. The I-V curve for this device has a PVCR of about 28 at room temperature, as shown in Fig. 1, and 70 at 77 K. This room-temperature PVCR is about a factor of eight higher than achieved with the best GaAs/AlAs or GaAs/AlGaAs structures and is two times higher than the best p-n junction tunnel (Esaki) diodes made from GaSb or GaAs [13]. The current density at the peak is limited to 1×10^4 A cm^{-2} because of the relatively thick (50 nm), unintentionally doped ($N_D = 2\times10^{16}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ buffer layers outside of each barrier. These layers are added to minimize the impurity concentration in the double-barrier structure. Nearly identical values of PVCR have been obtained at a higher peak current density, $J_P \cong 4\times10^4$ A cm^{-2}, in a different $In_{0.53}Ga_{0.47}As$/AlAs structure described in Ref. [9].

To obtain a higher current density, device 2 is designed to have the same quantum-well thickness (4.6 nm) as device 1, but to have thinner AlAs barriers (1.4 nm), a thinner (10 nm) buffer layer on one side (the intended cathode) of the double-barrier structure to increase the quasi-Fermi energy, and a thicker (75 nm) buffer layer on the opposite side to reduce the device capacitance. With negative bias applied to the thin-buffer-layer side, 2-μm-diameter diodes broke down at voltages less than required to observe a NDR region. With the opposite bias polarity, a stable NDR region was observed and is shown in the current density vs voltage curve in Fig. 2. The measured J_P is 1.7×10^5 A cm^{-2} and the PVCR is about 12 at room temperature. A comparison is made in Fig. 2 with a GaAs/AlAs diode [2] having nearly the same J_P. The difference in PVCRs is almost identical to what was observed above at much lower J_P, and leads to the following useful rule of thumb. That is, $In_{0.53}Ga_{0.47}As$/AlAs and GaAs/AlAs having the same J_P differ in PVCR by about a factor of 8.

Device 3 differs from device 2 only by the presence of a wider (5.5 nm) quantum well. The wider well reduces the voltage required for peak current and allows the NDR region to be

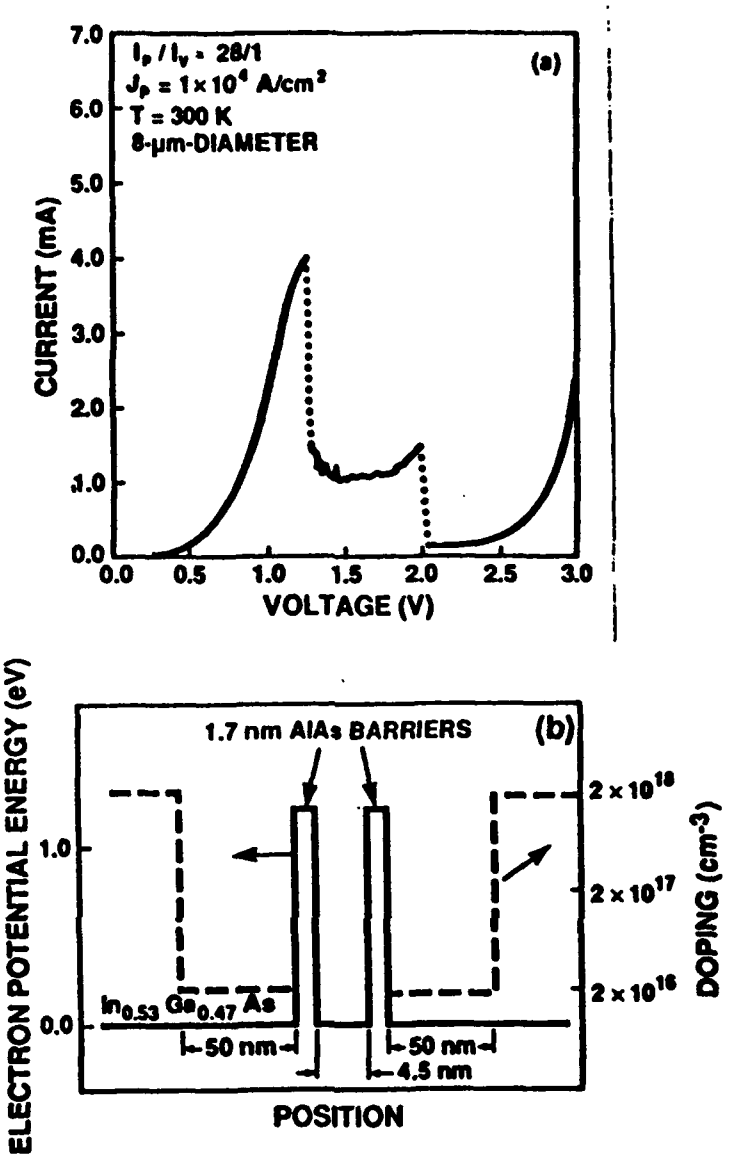

Fig. 1. (a) Current-voltage characteristic of device 1 at room temperature. (b) Compositional and doping profiles of device 1.

observed with the desired bias polarity. The curve of room-temperature current density vs voltage is shown for both polarities in Fig. 3. For positive bias applied to the thin-buffer-layer side (positive voltage in Fig. 3), the J_p and PVCR are similar to what was measured in device 2. For negative bias a larger J_p of about 2.5×10^5 A cm^{-2}, and a PVCR of about 8.5 were measured at room temperature. The asymmetry in the current-density vs voltage curve is an expected consequence of the asymmetric doping profile in the buffer layers. The NDR region at negative bias voltage is very promising for high-speed applications, as will be discussed below.

The I-V curves in Figs. 1, 2, and 3 are discontinuous because the current switches into the middle of the NDR region when the voltage is increased just above the peak point or just

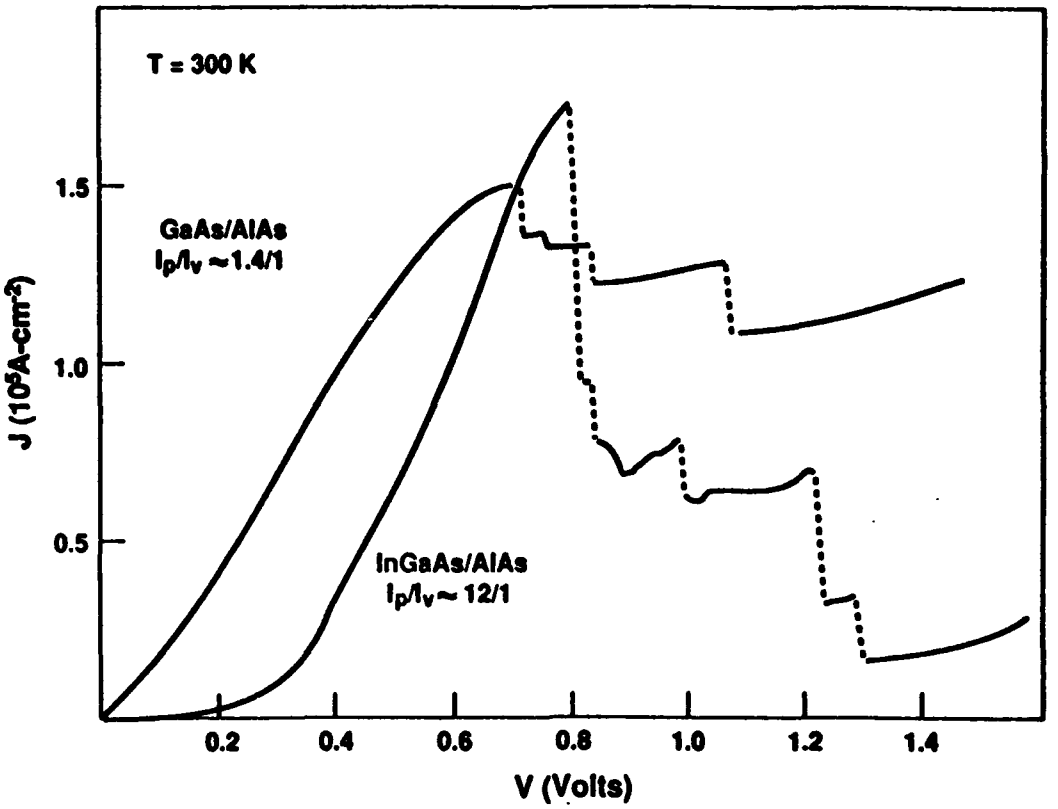

Fig. 2. Room-temperature current-voltage characteristics of device 2 and of a high-current density GaAs/AlAs diode.

below the valley point. At the bias voltages in the NDR region, low-frequency oscillations occur in the circuit used to measure the I-V curve. These oscillations are rectified by the diode, resulting in the characteristic current plateau(s) of the NDR region. The I-V curves would be much steeper in the NDR region if the device was electrically stable such that no switches or oscillations occurred. The circuits used to test the DBDs at high frequencies are designed to support only the desired oscillation, and suppress low frequency oscillations in the bias circuit.

4. EXPERIMENTAL OSCILLATOR RESULTS

The oscillation power and frequency of device 2 were measured at room temperature in a series of microwave and millimeter-wave resonators operating between 1 and 200 GHz. The results for a 2-μm-diameter diode, plotted in Fig. 4, include a maximum oscillation power of 280 μW at 1.1 GHz, This corresponds to a dc-to-rf efficiency of 11% and a power density of 0.9×10^4 W cm^{-2}. Similar results were obtained up to frequencies of about 20 GHz. We also tested a 4-μm-diameter diode at low frequencies and measured an absolute power of about 0.9 mW (7.2×10^3 W cm^{-2}) near 1 GHz. A comparison with the oscillation results of the fastest GaAs/AlAs DBD is also made in Fig. 4, where we see a factor of 8 difference in the power density at the low-frequency end. This difference is due in large part to the difference in ΔJ, which is 1.6×10^5 A cm^{-2} for device 2 and 4.3×10^4 A cm^{-2} for the GaAs/AlAs device.

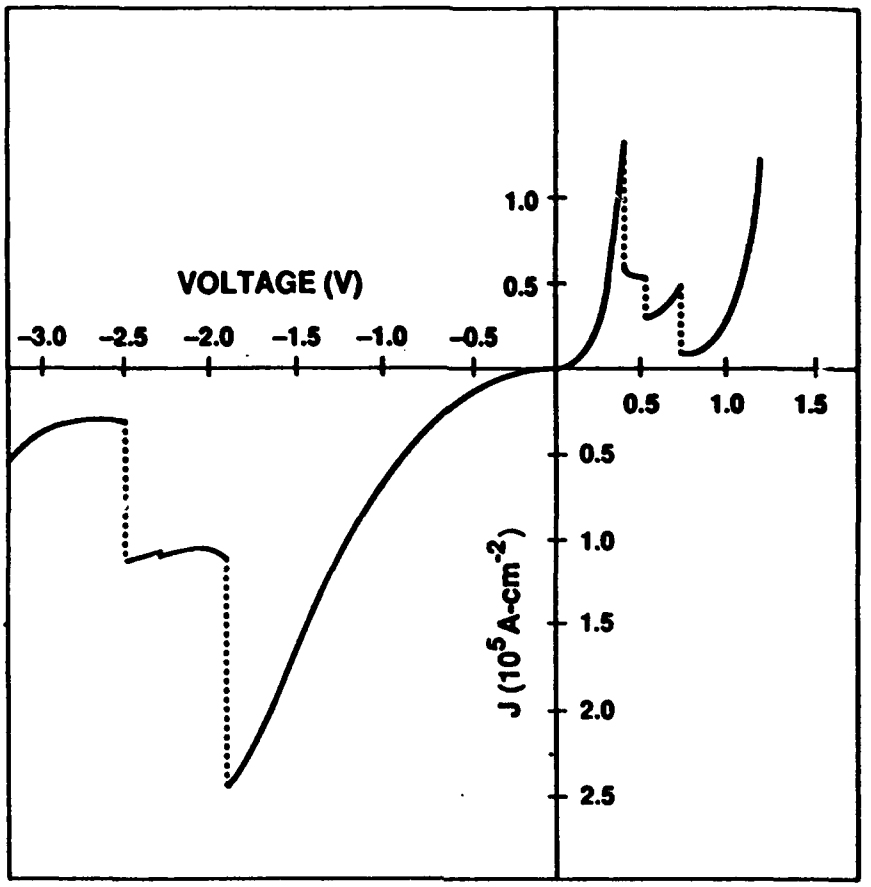

Fig. 3. Current-voltage characteristic of device 3 at room temperature.

At frequencies above 20 GHz, the power of the InGaAs diode decreased rapidly such that the measured power at 125 GHz was 5 μW. This roll-off behavior is quite different from that displayed by the GaAs/AlAs diode, which shows no obvious break point between slow and rapid power decrease. We attribute the roll-off behavior of the InGaAs diode to a high specific capacitance, which is calculated to be about 3.8 fF μm^{-2}. The capacitance is high because the narrow-buffer-layer side depletes over a distance of only 20 nm or so with positive voltage applied to this side, which is about three times less than the depletion length in the GaAs/AlAs diode.

5. THEORETICAL OSCILLATION CHARACTERISTICS

It is informative to calculate the theoretical oscillator performance since the most promising $In_{0.53}Ga_{0.47}As$/AlAs DBDs (e.g., device 3) have yet to be tested as oscillators. The important figures of merit for DBD oscillators are the maximum oscillation frequency f_{MAX} and the maximum power density P_{MAX}. The f_{MAX} of a DBD must be very high (~ 1 THz) to be useful, because DBD oscillators will probably be implemented only at frequencies where other solid-state devices cannot oscillate ($f \gtrsim 200$ GHz). At lower frequencies single DBDs cannot presently generate power levels that are competitive with those from standard solid-state oscillators because the DBDs cannot be operated with comparable device area. This limitation stems from the fact that the negative differential conductance of DBDs is practically

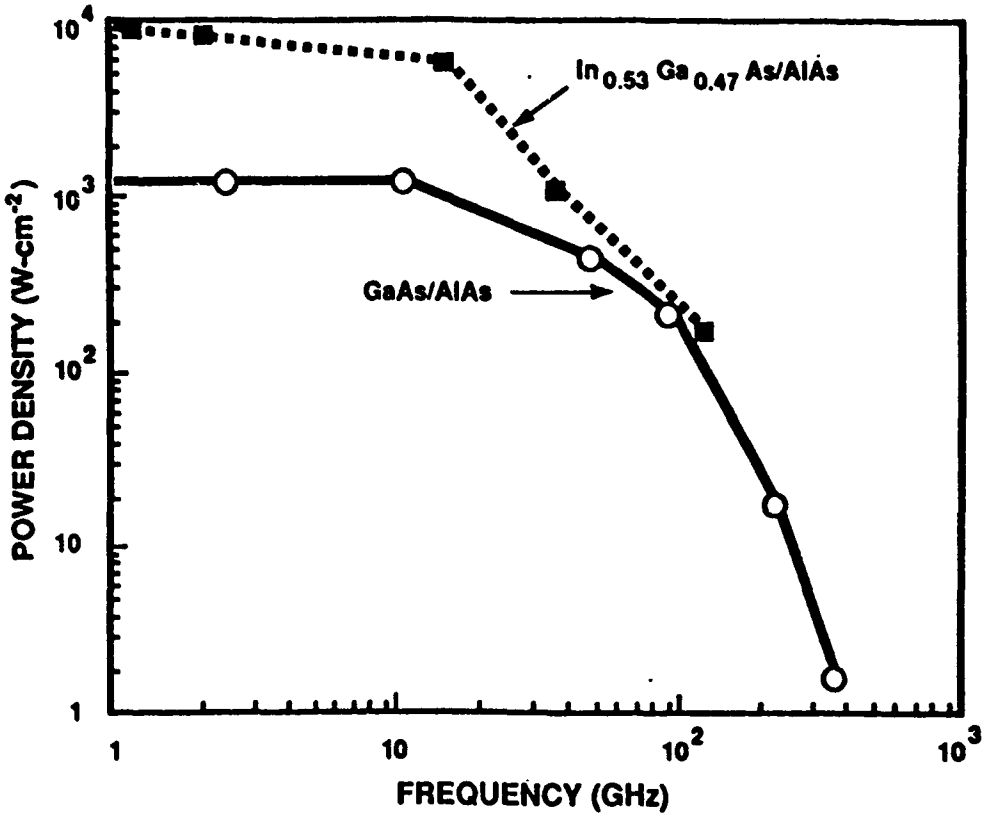

Fig. 4. Experimental oscillation results for device 2 in comparison with results for the fastest GaAs/AlAs device tested to date.

constant from dc up to the operating frequency. Thus, large-area DBDs present a very large magnitude of negative conductance at low frequencies, which makes it difficult to achieve dc-bias stability. This is the same problem that arose with Esaki tunnel diodes [14].

We have found that f_{MAX} of DBDs is adequately predicted by a lumped-element RCL equivalent-circuit model [15]. The equivalent circuit includes the intrinsic differential conductance G, the diode capacitance C, the series resistance R_S, and the "quantum-well inductance" L_{QW}, which is given approximately by $L_{QW} = \tau_1/G$ where τ_1 is the first quasibound-state lifetime. The intrinsic G would be the slope of the I-V curve for a device that was perfectly stable (i.e., no switching or oscillations) and had no series resistance. The condition that the real part of the terminal impedance of this circuit vanish determines a frequency f_{RCL} that is the upper limit for oscillation as a function of the circuit elements. Over the range of the NDR region, the element that varies the most is G. The expression for f_{RCL}, given in Table I, displays a maximum with respect to G at a value G_{MAX} that is usually close to $(2R_S)^{-1}$. This value, f_{MAX}, is given in Table I for the present InGaAs diodes and for other high-current-density InGaAs/AlAs and GaAs/AlAs diodes reported in the literature. To make the comparison tractable, we make two simplifying assumptions. First, each of the circuit elements in the model scales linearly (or inversely) with area. This is a very good assumption for all of the elements except the series resistance, which usually has a component that depends

TABLE I - Comparison of DBD oscillator characteristics

J_P (A cm^{-2})	G_{MAX} (mS μm^{-2})	C (fF μm^{-2})	τ_1 (ps)	f_{MAX} (GHz)	Reference
		$In_{0.53}Ga_{0.47}As$/AlAs Diodes			
1.7×10^5	-15	3.8	0.4	418	device 2
2.5×10^5	-11	1.3	0.2	932	device 3
4.5×10^5	-15	1.5	0.1	1280	[12]
5.0×10^5	-15	1.5	0.1	1280	[12]
		GaAs/AlAs Diodes			
1.5×10^5	-6	1.5	0.1	555	[2]
1.3×10^5	-5	1.3	0.3	468	[18]

$$f_{RCL} = \frac{1}{2\pi}\left[\left(\frac{1}{LC}(1 - C/2LG^2)\right)\left(1 - \sqrt{1 - \frac{(GR_S+1)/GR_S}{(C/2LG^2 - 1)^2}}\right)\right]^{1/2}$$

$$L = \frac{\tau_1}{G} \qquad f_{MAX} = f_{RCL}(G_{MAX})$$

sublinearly on area because of current-spreading effects [16]. As a result of this assumption, each of the element values listed in Table I and hereafter are area specific. The second simplifying assumption is that all of the InGaAs diodes have the same total specific series resistance of $R_S = 2\times10^{-7}\ \Omega\ cm^2$, and that the GaAs diodes have a common value $R_S = 6\times10^{-7}\ \Omega\ cm^2$. These are considered to be approximate values for the room-temperature R_S that can be obtained in these materials with present technology. This resistance includes ohmic-contact and undepleted-epilayer contributions.

We estimate an f_{MAX} of 932 GHz for device 3. This assumes that a negative bias voltage is applied to the thin-buffer-layer side (negative voltage in Fig. 3). Under this condition, C and τ_1 are found to be 1.3 fF μm^{-2} and 0.2 ps from separate numerical solutions to Poisson's and Schrödinger's equations, respectively. The resulting f_{MAX} is about 70% higher than the value for the fastest GaAs/AlAs oscillator diode fabricated to date and is limited largely by τ_1. The InGaAs/AlAs diodes listed below device 3 in Table I have about a factor of two smaller τ_1 because of the thinner barriers, and thus yield a higher f_{MAX} of 1.28 THz.

The maximum power density of DBDs measured at the fundamental oscillation frequency is usually very close to the theoretical value predicted for Esaki diodes [17], $P_{MAX} = (3/16)\Delta J\ \Delta V$, where ΔV is the difference between the valley voltage V_V and the peak

TABLE II - Comparison of DBD oscillator power

J_P (A cm^{-2})	J_P/J_V	$J_P - J_V$ (A cm^{-2})	$V_V - V_P$ (V)	P_{MAX} (W cm^{-2})
		$In_{0.53}Ga_{0.47}As$/AlAs Diodes		
1.7×10^5	12	1.6×10^5	0.43	1.3×10^4
2.5×10^5	8.5	2.2×10^5	0.60	2.5×10^4
4.5×10^5	3.6	3.2×10^5	0.15	9.0×10^3
5.0×10^5	3.0	3.3×10^5	0.25	1.6×10^4
		GaAs/AlAs Diodes		
1.5×10^5	1.4	4.3×10^4	0.30	2.4×10^3
1.3×10^5	2.5	7.8×10^4	0.4	5.8×10^3

$$P_{MAX} = \frac{3}{16}(J_P - J_V)(V_V - V_P).$$

voltage V_P. For example, this expression yields 1.25×10^4 W cm^{-2} for device 2, consistent with the low-frequency experimental results. Maximum power densities are given in Table II for each of the InGaAs/AlAs and GaAs/AlAs diodes listed in Table I. According to these estimates, device 3 should generate a power density of 2.5×10^4 W cm^{-2}, corresponding to an absolute power of 0.9 mW from a 2-μm-diameter diode. This exceeds the power density estimated for the best GaAs/AlAs diode reported to date [18] by over a factor of four. This improvement reflects the high ΔJ and relatively large ΔV that device 3 provides. The next highest power density, 1.6×10^4 W cm^{-2}, is predicted for an $In_{0.53}Ga_{0.47}As$/AlAs device having a record high J_P of 5×10^5 A cm^{-2} [10]. This remarkable device has very thin (1.1 nm) AlAs barriers and a thin InAs layer in the middle of the $In_{0.53}Ga_{0.47}As$ quantum well to help reduce the peak voltage.

Our expression for f_{MAX} should be considered as an upper limit on the actual maximum oscillation frequency for the following reasons. First, the lumped-element RCL model neglects the transit-time delay across the depletion layer. This effect is very difficult to model properly because of the velocity overshoot effect, but a constant drift-velocity approximation leads to a reduction in f_{MAX} for any finite velocity and depletion length [2]. Second, the G_{MAX} used to compute f_{MAX} may not be realizable in DBDs with low PVCR. This is a difficult issue to address in high-speed DBDs because the I-V curves of these devices are usually distorted by oscillations. This makes it impossible to determine the intrinsic G of the DBD from the measured I-V curve.

TABLE III - Comparison of DBD switching characteristics

J_P (A cm^{-2})	$J_P - J_V$ (A cm^{-2})	$V_V - V_P$ (V)	S (10^{12} V s^{-1})	t_R (ps)	Reference
		$In_{0.53}Ga_{0.47}As$/AlAs Diodes			
2.5×10^5	2.2×10^5	0.60	1.7	1.5	device 3
4.5×10^5	3.2×10^5	0.15	2.2	0.3	[10]
5.0×10^5	3.3×10^5	0.25	2.2	0.5	[10]
		GaAs/AlAs Diodes			
4.0×10^4	3.0×10^4	0.40	0.20	8.8	[3]
1.5×10^5	4.3×10^4	0.30	0.29	4.5	[2]
1.3×10^5	7.8×10^4	0.40	0.60	2.9	[18]

$$S = (J_P - J_V)/C \qquad t_R = 4.4(V_V - V_P)/S$$

6. THEORETICAL SWITCHING PERFORMANCE

Although $In_{0.53}Ga_{0.47}As$/AlAs diodes have been tested only as oscillators, it is important to estimate their switching speed since there is great interest in using them in various pulse, trigger, and logic circuits. A useful figure of merit for switches is the speed index [13], $S = (J_P - J_V)/C$. This quantity enters into an estimate of the time required for the diode to switch from a voltage bias point below the peak to a point above the valley point, or vice versa. This is a more difficult quantity to calculate than f_{MAX} since it necessarily depends on the large-signal characteristics of the double-barrier diode. To estimate the switching time, we model the I-V curve in the NDR region by the following parabolic form,

$$I = \frac{\Delta I}{\Delta V^2}(V - V_V)^2 + I_V \,. \qquad (1)$$

This expression increases in slope monotonically as the voltage is decreased from the valley point to the peak point. This is a good approximation to the stable I-V curve at all voltages except those just above the peak. We assume that the diode is biased at the peak point through a load resistance R_L that is consistent with dc bistability (i.e., two possible dc bias points exist, one above and one below the NDR region). This resistance must satisfy $R_L > \Delta V/\Delta I$. A slight increase in the bias voltage will then eliminate the stable operating point at the peak, and cause a switch to the stable point at the valley point or beyond. We assume that the diode capacitance is a constant equal to the value at the peak voltage, and we ignore the quantum-well inductance and series resistance for the moment. For a load

resistance equal to $\Delta V/\Delta I$, the time required for the diode voltage to increase from a value 10% above the peak voltage to a value 10% below the valley voltage is given by,

$$t_R = \int_{V_P+0.1\Delta V}^{V_V-0.1\Delta V} \frac{CdV}{-\Delta I/\Delta V(V - V_V) - \Delta I/\Delta V^2(V - V_V)^2} . \quad (2)$$

Evaluation of this "rise-time" integral yields $t_R \cong 4.4\Delta V/S$.

This expression can be tested on the GaAs/AlAs DBD that was measured to switch in 2.1 ps [3]. The speed index for this diode is computed from the device characteristics to be 0.20×10^{12} V s^{-1}, and ΔV is about 0.4 V, so that the switching time is estimated to be 8.8 ps. The discrepancy between experiment and the estimation is due in large part to the fact that the experiment was conducted under overdrive conditions whereby the voltage pulse that initiated the switch was a significant fraction of ΔV in magnitude and comparable to t_R in rise time. Our estimate, as well as the 12 ps estimate reported recently by Diamond et al. [19] for the same device, assumes no overdrive.

Using the NDR measured at negative bias in Fig. 3 and a specific capacitance value of 1.3 fF μm^{-2}, we calculate a speed index for device 3 of 1.7×10^{12} V s^{-1}. This leads to an estimate of t_R = 1.5 ps, which is less than the value for any GaAs/AlAs diode fabricated to date. For example, we calculate t_R = 4.5 ps for our fastest GaAs/AlAs oscillator diode ($\Delta J = 4.3\times10^4$ A cm^{-2}) based on $S = 0.29\times10^{12}$ V s^{-1} and ΔV = 0.3 V for that device [2]. An improved GaAs/AlAs device having $\Delta J = 7.8\times10^4$ A cm^{-2} [18] yields t_R = 2.9 ps. The primary reason for the greater speed of device 3 is the larger ΔJ at high J_P. Note that the best reported speed index for Esaki diodes is 0.07×10^{12} V s^{-1}, or 70 mA pF^{-1} [20], so that the $In_{0.53}Ga_{0.47}As$/AlAs diode offers an improvement by a factor of 24. This difference is a result of a much lower specific capacitance as well as a larger ΔJ for the DBD compared to the Esaki diode.

The estimated switching times for the best $In_{0.53}Ga_{0.47}As$/AlAs and GaAs/AlAs diodes fabricated to date are compiled in Table III. The highest speed index and the lowest switching time, by far, are given for the very high current density diodes demonstrated recently by Broekaert et al. [10]. This results in part from a high $\Delta J \sim 3.2\times10^5$ A cm^{-2}, and in part from a small ΔV. A comparison with the oscillator characteristics in Table II leads to the following important point regarding DBDs. The best oscillator diodes are not necessarily the best switch diodes, and vice versa. Increasing ΔJ tends to increase oscillator power and decrease switching time in the same manner. Increasing ΔV also enhances oscillator power, but it increases the switching time since a greater ΔV requires a greater change of charge across the DBD capacitor.

We have carried out more detailed calculations of the rise-time to investigate the effect of other parameters in the device or circuit. The effect of varying the load resistance was determined by fitting the I-V curve of the diode beyond the valley voltage with a parabola, and then deriving an expression analogous to Eq. (2) for the rise time as a function of $R_L \geq \Delta V/\Delta I$. This procedure yields a minimum value of t_R that depends on the detailed form of the current-voltage curve, but typically is about 10% less than $4.4\Delta V/S$ and occurs at an R_L roughly two times $\Delta V/\Delta I$. The effects of the diode series resistance and the quantum-well inductance were determined by assuming a piecewise-linear fit to the I-V curve and solving the differential equations governing the dynamic current and voltage. The series resistance is found to increase t_R by an amount that becomes negligible when $R_S \ll \Delta V/\Delta I$. In contrast,

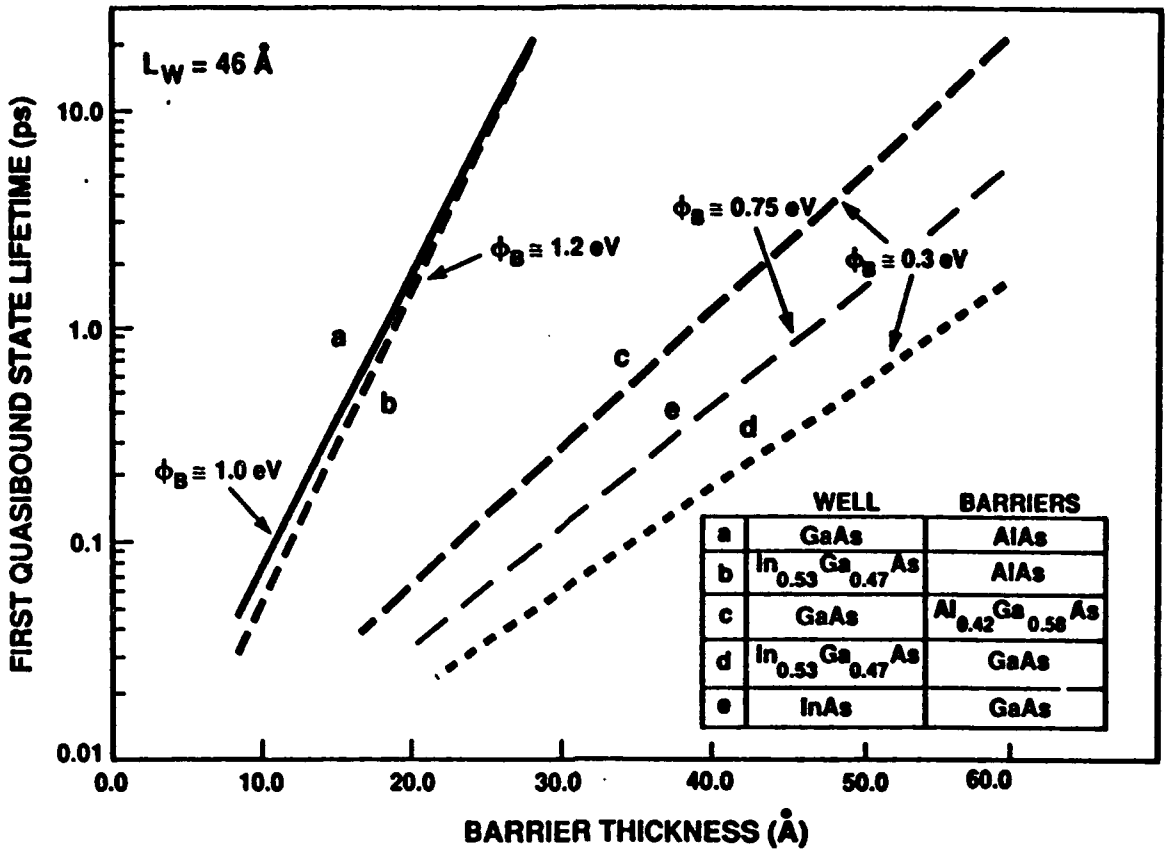

Fig. 5. Lifetime of the first quasibound state as a function of barrier thickness for double-barrier structures made from five different InGaAs/AlGaAs material systems. The quantum-well width is fixed at 4.6 nm.

the quantum-well inductance decreases t_R somewhat, but the decrease is quite small if τ_1 is less than the t_R given by Eq. (2). Inspection of Tables I and III shows that $\tau_1 < t_R$ for all of the diodes considered here. There are other effects that could increase the rise time, particularly in the diodes having sub-picosecond values for t_R in Table III. For example, the depletion-layer transit time will increase t_R, as will the parasitic capacitances and inductances of most device-connection designs that are commonly used.

7. ALTERNATIVE InGaAs MATERIAL SYSTEMS

An important quantity in predicting the performance of double-barrier structures as high-speed devices is the quasibound-state lifetime τ_1. The peak current density is inversely proportional to τ_1, and the intrinsic time delay of the resonant-tunneling process (represented in the circuit model by L_{QW}) is directly proportional to τ_1. Shown in Fig. 5 is the theoretical τ_1 as a function of barrier thicknesses for five different material systems, all containing some alloy of $In_xGa_{1-x}As$ for the quantum well and cladding layers, and some alloy of $Al_xGa_{1-x}As$

for the barriers. The quantum-well thickness in all cases is assumed to be 4.6 nm. Notice that the GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs systems yield nearly the same curve, despite the fact that the $In_{0.53}Ga_{0.47}As$ effective mass (0.042 m_0) is less than that of GaAs. This reflects the fact that the lifetime depends strongly on the attenuation coefficient (complex wavevector) in the barriers but depends rather weakly on the real wavevector in the quantum well and cladding layers. In all regions, the attenuation coefficient has roughly a square-root dependence on the effective mass. Although the $In_{0.53}Ga_{0.47}As$/AlAs system does not exhibit the severe degradation of PVCR that is observed in the GaAs/AlAs system with thin barriers, thin barriers remain a necessity for the InGaAs/AlAs system.

The most obvious way to eliminate the need for thin barriers is to use a material system with low barrier height. The GaAs/AlGaAs system is the most obvious choice, but the PVCR of diodes made from this system is generally worse than that of GaAs/AlAs diodes because of excess current resulting from alloy scattering in the barriers and from thermionic emission over the top of the barriers. Another choice of material is the $In_{0.53}Ga_{0.47}As$/GaAs. This system yields a somewhat lower barrier height ($\phi_B \cong 0.3$ eV) and thus more thermionic current than GaAs/AlGaAs, but should have no leakage current due to alloy scattering. As shown in Fig. 5, this system has a much smaller quasibound-state lifetime for a given barrier thickness than any of the AlAs-barrier systems. This should allow for high current densities ($J_P \geq 1\times10^5$ A cm^{-2}) and small lifetimes in structures with relatively thick barriers, e.g., in the range of 4 to 5 nm. Recently, this system has been implemented to make a planar DBD with a J_P of 1.0×10^5 A cm^{-2} and a PVCR of 8 at 77 K [21]. The last system we consider here is InAs/GaAs with the GaAs barriers kept thin enough to be pseudomorphic. The barrier height for this system is estimated to be 0.7 eV, which should allow for excellent PVCR at room temperature. In addition, the InAs is a superior material for the cladding regions outside the barriers since it will have low series resistance, and a much lower specific contact resistance than GaAs or $In_{0.53}Ga_{0.47}As$.

8. CONCLUSION

For both oscillator and switch applications, the device performance of pseudomorphic $In_{0.53}Ga_{0.47}As$/AlAs DBDs is superior to that of GaAs/AlGaAs diodes. The difference in f_{MAX} is estimated to be about a factor of two, and the difference in switching speed is at least a factor of four. The switching speed advantage results from the fact that the available current density in the best InGaAs devices is approximately four times higher than in the best GaAs devices. Thus we anticipate that the $In_{0.53}Ga_{0.47}As$/AlAs device will be the most likely candidate to be used in the high-speed pulse, trigger and logic applications that are presently proposed for DBDs.

9. ACKNOWLEDGMENTS

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10. REFERENCES

[1] L.L. Chang, L. Esaki, and R. Tsu, Appl. Phys. Lett. 24, 593 (1974).

[2] E.R. Brown, T.C.L.G. Sollner, C.D. Parker, W.D. Goodhue, and C.L. Chen, Appl. Phys. Lett. 55, 1777 (1989).

[3] J.F. Whitaker, G.A. Mourou, T.C.L.G. Sollner, and W.D. Goodhue, Appl. Phys. Lett. 53, 385 (1988).

[4] E.C. Sutton, IEEE Trans. Microwave Theory Tech. MTT-31, 589 (1983).

[5] S.K. Diamond, E. Ozbay, M.J.W. Rodwell, D.M. Bloom, Y.C. Pao, E. Wolak, and J.S. Harris, in OSA Proceedings on Picosecond Electronics and Optoelectronics, Vol. 4 of the OSA Proceeding Series, T.C.L.G. Sollner and D.M. Bloom, eds. (Optical Society of America, Washington, D.C., 1989), pp. 101-105.

[6] T. Inata, S. Muto, Y. Nakata, T. Fujii, H. Ohnishi, and S. Hiyamizu, Japan. J. Appl. Phys. 25, L983 (1986).

[7] T. Inata, S. Muto, Y. Nakata, S. Sasa, T. Fujii, and S. Hiyamizu, Japan. J. Appl. Phys. 26, L1332 (1987).

[8] S. Sen, F. Capasso, A.L. Hutchinson, A.Y. Cho, Electron. Lett. 23, 1229 (1987).

[9] T.P.E. Broekaert, W. Lee, and C.G. Fonstad, Appl. Phys. Lett. 53, 1545 (1988).

[10] T.P.E. Broekaert and C.G. Fonstad, IEDM Technical Digest, Washington D.C., Dec. 1989, p. 559.

[11] E.E. Mendez, W.I. Wang, E. Calleja, and C.E.T. Goncalves da Silva, Appl. Phys. Lett. 50, 1263 (1987).

[12] F. Chevoir and B.Vinter, Appl. Phys. Lett. 55, 1859 (1989).

[13] S.M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981), Sec. 9.2.

[14] M.E. Hines, Bell Syst. Tech. J. 39, 485 (1960).

[15] E.R. Brown, C.D. Parker, and T.C.L.G. Sollner, Appl. Phys. Lett. 54, 934 (1989).

[16] E.R. Brown, W.D. Goodhue, and T.C.L.G. Sollner, J. Appl. Phys. 64, 1519 (1988).

[17] C.S. Kim and A. Brandli, I.R.E. Trans. Circuit Theory CT-8, 416 (1961).

[18] S.K. Diamond, E. Ozbay, M.J.W. Rodwell, D.M. Bloom, Y.C. Pao, E. Wolak, and J.S. Harris, IEEE Electron Device Lett. 10, 104 (1989).

[19] S.K. Diamond, E. Ozbay, M.J.W. Rodwell, D.M. Bloom, Y.C. Pao, and J.S. Harris, Appl. Phys. Lett. 54, 153 (1989).

[20] D.T. Young, C.A. Burrus and R.C. Shaw, Proc. IEEE 52, 1260 (1964).

[21] X.J. Song, J.B. Kuang, W.J. Schaff, P.J. Tasker, K. Yamasaki, and L.F. Eastman, SPIE Proceedings on High Speed Electronics and Device Scaling, 17-21 March, 1990.

A Quasioptically Stabilized Resonant-Tunneling-Diode Oscillator for the Millimeter- and Submillimeter-Wave Regions

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***Abstract*—A semiconfocal open-cavity resonator has been used to stabilize a resonant-tunneling-diode waveguide oscillator at frequencies near 100 GHz. The high quality factor of the open cavity resulted in a linewidth of approximately 10 kHz at 10 dB below the peak, which is about 100 times narrower than the linewidth of an unstabilized waveguide oscillator. This technique is well suited for resonant-tunneling-diode oscillators in the submillimeter-wave region.**

I. Introduction

THE OSCILLATION frequency of the double-barrier resonant-tunneling diode (RTD) has recently been extended up to 712 GHz [1], which makes it the fastest solid-state electronic oscillator demonstrated to date at room temperature. A major challenge in operating solid-state oscillators at frequencies above 100 GHz is the design of the resonator. Conventional resonators, such as those based on closed cavities or radial transmission lines, exhibit an unloaded quality factor Q_u that decreases with increasing frequency because of increases in the ohmic losses of metallic surfaces. Open resonators, such as those used in lasers, provide a much higher Q_u but are difficult to integrate with lumped-element, solid-state oscillators. We have combined a waveguide RTD oscillator and a high-Q_u semiconfocal cavity to form a quasioptical oscillator operating at frequencies near 100 GHz.

At present, the primary application of the RTD oscillator is a low-noise local oscillator (LO) for high-sensitivity radiometers operating in the submillimeter-wave region ($f \gtrsim 300$ GHz). In this application the linewidth must be less than about 100 kHz and the oscillator should be frequency tunable by at least $\pm 1\%$ of the nominal center frequency. The quasioptical oscillator demonstrated here provides the required narrow linewidth, and can be easily scaled down in size for operation at higher frequencies.

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II. Quasioptical Oscillator Design

The schematic diagram of our quasioptical oscillator designed for the 100 GHz region is shown in Fig. 1. The RTD is mounted in a standard-height WR-6 (0.065 × 0.0325 in) rectangular waveguide that opens abruptly to a round 0.075-in-diameter coupling hole within the middle of a flat metallic plate. This plate forms one reflector of a semiconfocal open resonator. The TEM_{00N} modes of this resonator have a Gaussian transverse intensity profile with 1/e-point loci as shown in Fig. 1. The spot diameter of these modes at the flat reflector is designed to be larger than the diameter of the coupling hole. This makes the coupling between the waveguide and the open cavity fairly weak, which is necessary to realize a large loaded quality factor Q_l for the open resonator.

In our first implementation of the open resonator, the flat mirror was an aluminum plate, and the spherical mirror was made from stainless steel and had a radius of curvature of 3.0 cm. The length of the cavity, D, was mechanically adjustable about the semiconfocal value of 1.5 cm. The upper limit of Q_l for this cavity is the unloaded quality factor Q_u. This can be estimated by assuming that the only power loss suffered by the Gaussian beam is the ohmic loss in the stainless steel mirror, which is much greater than the loss in the aluminum mirror. For a resonator in which the loss of one mirror dominates, a useful expression is $Q_u = D/\delta$ [2], where δ is the skin depth given by $\delta = (\rho/\mu\pi f)^{1/2}$ (MKSA units) ρ is the resistivity, μ is the permeability, and f is the frequency. Taking $D = 1.5$ cm, $f = 103$ GHz, and $\rho = 72 \times 10^{-6}$ Ω-cm (the dc resistivity of stainless steel [3]), we find $\delta = 1.3$ μm and $Q_u = 1.2 \times 10^4$.

The waveguide portion of the oscillator, shown in cross section in Fig. 2(a), is similar to the circuit used in all of our previous RTD oscillators operating above 100 GHz. The diode is dc biased by a coaxial circuit that suppresses spurious oscillations by means of a very lossy section of transmission line placed in close proximity to the diode chip. The lossy material is an iron-loaded epoxy. The equivalent circuit is given in Fig. 2(b). The active region of the RTD is represented by a large-signal conductance G in series with an inductance L_{QW}, both in parallel with a capacitance C_D. The capacitance is attributed primarily to the depletion region of the RTD. The inductance is

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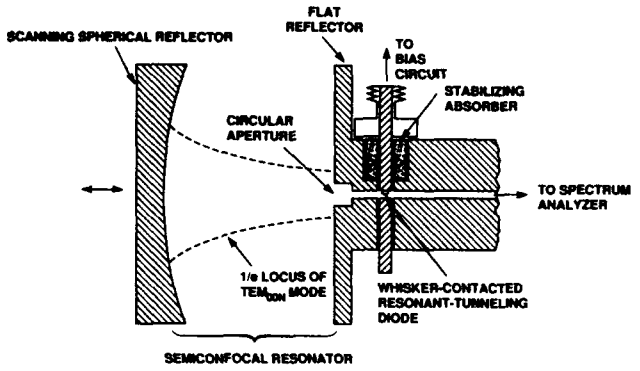

Fig. 1. Schematic cross-sectional diagram of quasioptical resonant-tunneling-diode oscillator designed to operate in the 100 GHz region.

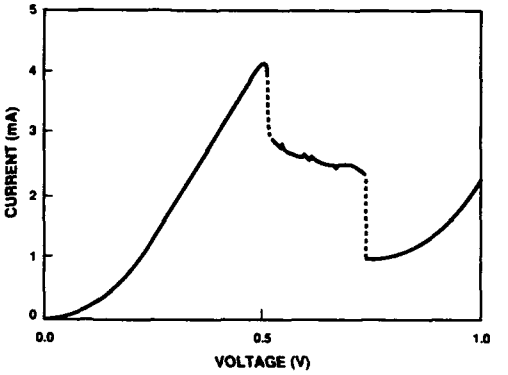

Fig. 3. Current-voltage curve of an $In_{0.53}Ga_{0.47}As/AlAs$ RTD mounted in the WR-6 waveguide at room temperature.

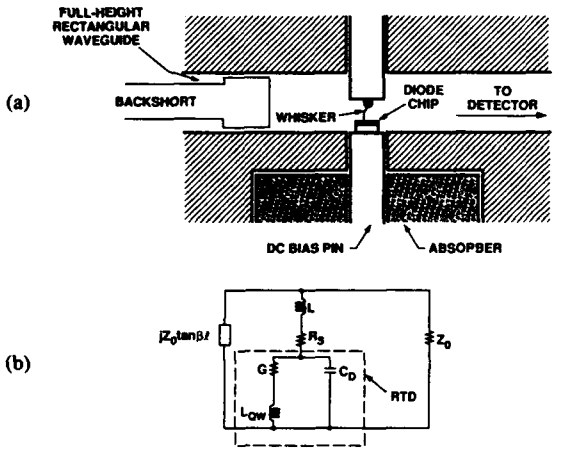

Fig. 2. (a) Cross-sectional diagram of the waveguide part of the quasioptical oscillator with a tunable backshort replacing the open cavity. (b) Equivalent circuit of the waveguide oscillator.

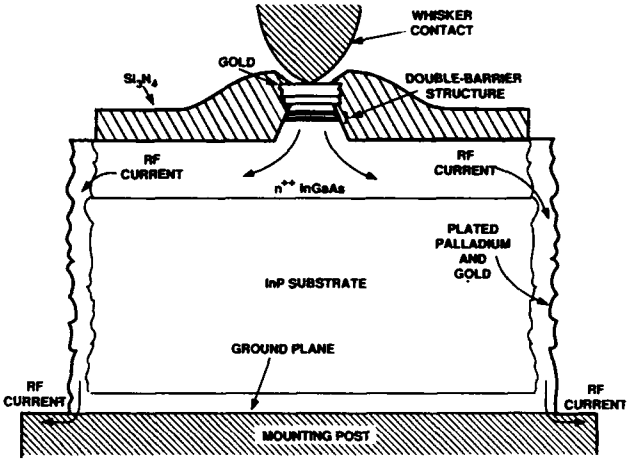

Fig. 4. Cross section of RTD chip showing Si_3N_4 hole for whisker contact. The figure also shows the path followed by the RF current between the top contact and the ground plane.

attributed to the time delay of resonant tunneling [4], but is not important in the present experiment because this time delay is much less than the period of an oscillator operating near 100 GHz. The elements representing the active region are in series with a parasitic resistance R_S that is composed of a number of ohmic-loss mechanisms in the RTD chip. Each chip contains several mesa-geometry RTD's, one of which is contacted by a whisker. The whisker is mounted on a post that penetrates somewhat into the waveguide, and the electrical effect of the whisker is represented by the inductance L. The effect of the backshort is represented by the reactive element $jZ_0 \tan \beta l$, where Z_0 is the characteristic impedance, β is the propagation constant for the fundamental TE_{10} mode, and l is the separation between the backshort and the whisker. The parallel combination of Z_0 and $jZ_0 \tan \beta_l$ yields a series impedance $Z_L = Z_0 \sin^2 \beta l + j(Z_0/2) \sin 2\beta l$. The elements Z_L, C_D, and L form a low-Q series resonance that supports oscillations when G is sufficiently negative.

III. High-Speed Resonant-Tunneling Diode

The RTD used in the present experiment was made from the InGaAs/AlAs materials system. It has a theoretical maximum oscillation frequency of 900 GHz, and has previously demonstrated the most powerful oscillations we have observed to date above 100 GHz [5]. It consists of two 1.4-nm-thick undoped AlAs barriers separated by a 5.5-nm-thick undoped $In_{0.53}Ga_{0.47}As$ quantum well. It was grown by molecular beam epitaxy on an n^+ InP substrate. The room-temperature current-voltage (I–V) curve of a diode having an active area of 4 μm^2 is shown in Fig. 3. It has a peak-to-valley current ratio of approximately 4.2, and a peak current density of 1.0×10^5 A cm^{-2}. The plateau in the I–V curve between the peak and valley voltages is the region of oscillation. The discontinuities (shown in Fig. 3 as dashed lines) connecting the plateau to the peak and valley points are a result of self-rectification of the oscillation by the RTD.

In RTD's intended for stable high frequency oscillators, it is important to achieve a robust whisker contact and a low-resistance current path from the active region of the device to the ground plane. The robust contact is obtained by entrapping the whisker in a hole in a Si_3N_4 layer which covers the RTD, as shown in Fig. 4. The Si_3N_4 layer is deposited after the RTD mesas are fabricated on the wafer. The holes are defined by photolithog-

raphy and reactive-ion etching. An additional benefit of the Si_3N_4 layer is that it acts to passivate the $In_{0.53}Ga_{0.47}As$ sidewalls of the RTD mesa [6]. The low-resistance current path is achieved in the manner shown in Fig. 4. Between the RTD mesa and the edges of the chip, the RF current flows in a heavily doped n^{++} epitaxial layer grown on top of the InP substrate. The ac conductivity of this layer is roughly 10 times that of the substrate. From the edge of the chip down to the post (ground plane), the current flows through a palladium/gold layer plated on the sidewalls of the chip. The overall series resistance from the double-barrier structure to the bottom of the chip is approximately 0.5 Ω at dc, increasing to about 1.0 Ω at 600 GHz.

IV. Experimental Results

The output radiation of the quasioptical oscillator propagates down the waveguide to a Schottky-diode mixer where it is down converted to the frequency range of a microwave spectrum analyzer. Experimental power spectra are shown in Fig. 5 for an RTD oscillator operating near 103 GHz. The broad spectrum in Fig. 5(a) results from inserting a backshort into the waveguide at the open end. In this case, the oscillator operates with the waveguide resonator shown in Fig. 2. The width of the spectrum 10 dB below the peak is approximately 1 MHz, which is unsuitable for most applications.

Upon removing the short and exposing the open cavity, the spectrum shifts and becomes much narrower. The expansion of this spectrum, shown in Fig. 5(b), yields a linewidth of approximately 10 kHz at 10 dB below the peak. This is 100 times narrower than the waveguide-oscillator linewidth. The center frequency of the cavity resonance is determined, as in all open resonators, by the spatial separation of the reflectors. By varying this separation, we were able to tune the stabilized power spectrum over a range of about 0.3 GHz at a fixed RTD bias voltage. A greater tuning range of approximately 5 GHz was obtained by varying the bias voltage. With each change of bias, the open cavity had to be adjusted to establish a new oscillation frequency.

The average power of the waveguide and quasioptical oscillators corresponding to the spectra in Fig. 5(a) and (b) was found to be approximately −17 and −19 dBm, respectively. The lower power of the quasioptical resonator may be a result of some diffraction loss to free space by the semiconfocal cavity. Because the RTD is a negative resistance oscillator, its theoretical maximum power P_{max} can be estimated directly from the I–V curve. A useful estimate, first derived for p-n Esaki tunnel diodes [7], is $P_{max} = (3/16)\ \Delta I \cdot \Delta V$, where ΔI and ΔV are the differences between peak and valley currents and between valley and peak voltages, respectively. For the present diode, we find $\Delta I = 3.1$ mA and $\Delta V = 0.22$ V, so that $P_{max} = -9$ dBm. The discrepancy between this and our measured powers is typical for the best RTD oscillators operating near 100 GHz.

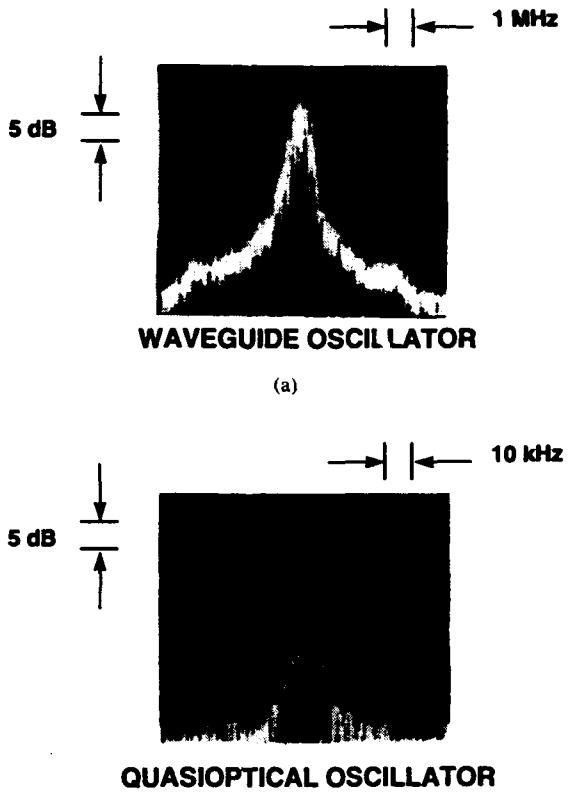

Fig. 5. (a) Power spectrum of the waveguide oscillator without the semiconfocal open cavity. (b) Power spectrum of the quasioptical oscillator with the semiconfocal cavity.

V. Analysis

The nonzero linewidth of an RTD oscillator is attributed to phase fluctuations caused by noise processes in the RTD. In this case, one expects that the linewidth should depend directly on the RTD noise power and reciprocally on the loaded quality factor. The dc bias conditions were the same for both spectra in Fig. 5, and hence the intrinsic RTD noise characteristics should have been the same for both cases. The factor of 100 difference in linewidth is therefore attributed to a difference in the Q_l of the two oscillators.

The Q_l of the quasioptical oscillator is estimated by assuming that it is approximately equal to the Q_l of the semiconfocal cavity coupled to the waveguide. Thus we can apply the general expression $Q_l^{-1} = Q_u^{-1} + Q_e^{-1}$, where Q_e is the (external) quality factor for the reactive part of the open cavity plus the load circuit. An expression applicable to the semiconfocal resonator is $Q_e = 4\pi f_0 D/Tv_g$ [8], where f_0 is the resonant frequency, v_g is the group velocity of the radiation in the cavity, and T is the net coupling transmissivity. We estimate T by assuming that the power coupled from the open cavity to the waveguide is given by the ratio of the power contained within the area (πR^2) of the coupling hole to the total power in the TEM_{00N} Gaussian mode. This leads to $T = 1.0 - \exp(-2R^2/\omega_0^2)$, where ω_0 is the characteristic width of the

Gaussian beam at the flat mirror.† For our semiconfocal cavity, the expression $\omega_0 = (\lambda D/\pi)^{1/2}$ applies [9], which yields $\omega_0 = 0.4$ cm. From this we find $T \cong 0.1$, which results in $Q_e = 1.3 \times 10^3$ for our open cavity. Combining this with the value of Q_u derived in Section II yields $Q_l \cong 1.2 \times 10^3$.

The Q_l of the waveguide oscillator is estimated from the equivalent circuit of Fig. 2. Experience has shown that this circuit oscillates with greatest power when Im $[Z_L]$ is inductive and Re $[Z_L]$ is fairly small, i.e., when $n\pi \lesssim \beta l \lesssim (n + 1/4)\pi$, where n is an integer. In this case the quality factor (for a series resonance) is $Q_l \cong X_c/(\text{Re}\ [Z_L] + R_s)$, where $X_c = (2\pi f_0 C)^{-1}$ is the capacitive reactance at resonance. In the experiment reported here, we used a 4 μm^2 RTD having $R_s \cong 12\ \Omega$ and $C \cong 5$ fF, and the backshort was adjusted so that Re $[Z_L] \sim 60\ \Omega$. Thus we estimate $Q_l \sim 5$ for the waveguide oscillator. The ratio of the theoretical loaded quality factors of the two oscillators is 240, which is of the same order as the inverse ratio of the linewidths.

VI. Increased Frequency and Power

The quasioptical oscillator is ideally suited to operate far into the submillimeter-wave region where the RTD is currently the only solid-state source that operates at room temperature. The unloaded quality factor of the resonator will certainly increase with frequency as the skin depth in the mirrors decreases. Values of Q_u over 10^6 are routinely available from semiconfocal resonators in the infrared region of the spectrum.

One could obtain significantly more power and maintain the advantage of quasioptical stabilization by properly implementing an array of RTD oscillators rather than the single-element oscillator demonstrated here. In principle, one could configure many waveguide-mounted RTD's with a single semiconfocal resonator. However, a more practical approach for very high frequencies is a planar RTD array based on microstrip-circuit techniques. The key point in either approach is that the oscillators all lie in an equiphase plane of the open-cavity mode and are thus synchronized by the high-Q_l resonance. This method of power combining has been used to obtain CW power levels up to 0.32 W from both planar FET oscillator arrays and Gunn diode oscillator arrays operating near 10 GHz [10]. It should be a useful technique for obtaining milliwatt levels of power from RTD oscillators in the submillimeter-wave region. A prototype planar RTD quasioptical oscillator having a single element has recently been demonstrated near 10 GHz [11].

VII. Summary

A semiconfocal resonator has been used to stabilize a waveguide-based RTD oscillator at a frequency of 103 GHz. The stabilized oscillator linewidth was approximately 10 kHz, which is about 100 times narrower than the linewidth of the waveguide oscillator alone. The quasioptical RTD oscillator should be suitable as a local oscillator for superconducting tunnel-junction mixers up to frequencies of at least 400 GHz.

†The quantity ω_0 is the distance from the center of the Gaussian beam to the point where the electric field is down by 1/e.

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References

[1] E. R. Brown, J. R. Söderström, C. D. Parker, L. J. Mahoney, K. M. Molvar, and T. C. McGill, "Oscillations up to 712 GHz in InAs/AlSb resonant-tunneling diodes," *Appl. Phys. Lett.*, vol. 58, pp. 2291–2293, 1991.

[2] R. G. Jones, "Precise dielectric measurements at 35 GHz using an open microwave resonator," *Proc. IEE*, vol. 123, pp. 285–290, 1976.

[3] *CRC Handbook of Chemistry and Physics*, 61st ed. Boca Raton, FL: CRC Press, 1980–1981, p. D-187.

[4] E. R. Brown, C. D. Parker, and T. C. L. G. Sollner, "Effect of quasibound-state lifetime on the oscillation power of resonant tunneling diodes," *Appl. Phys. Lett.*, vol. 54, pp. 934–937, 1989.

[5] E. R. Brown, C. D. Parker, A. R. Calawa, M. J. Manfra, C. L. Chen, L. J. Mahoney, W. D. Goodhue, J. R. Söderström, and T. C. McGill, "High-frequency resonant-tunneling oscillators," *Microwave Optical Tech. Lett.*, vol. 4, pp. 19–23, 1991.

[6] P. Boher, M. Renaud, J. M. Lopez-Villegas, J. Schneider, and J. P. Chane, "InGaAs/Si_3N_4 interface obtained in ultrahigh vacuum multipolar plasma: in-situ control by ellipsometry and electrical characterization," *Appl. Surf. Sci.*, vol. 30, pp. 100–103, 1987.

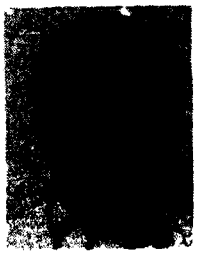
[7] C. S. Kim and A. Brandli, "High frequency high power operation of tunnel diodes," *IRE Trans. Circuit Theory*, vol. CT8, pp. 416–418, 1961.

[8] H. A. Haus, *Waves and Fields in Optoelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1985, p. 208.

[9] A. Yariv, *Quantum Electronics*, 2nd ed. New York: Wiley, 1975, p. 134.

[10] D. B. Rutledge, Z. B. Popovic, R. M. Weikle, M. Kim, K. A. Potter, R. C. Compton, and R. A. York, "Quasioptical power-combining arrays," in *1990 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1201–1204.

[11] K. D. Stephan, E. R. Brown, C. D. Parker, W. D. Goodhue, C. L. Chen, and T. C. L. G. Sollner, "Resonant-tunneling diode oscillator using a slot-coupled quasioptical open resonator," *Electron. Lett.*, vol. 27, pp. 647–649, 1991.



Elliott R. Brown obtained the Bachelor of Science degree (Summa Cum Laude) in physics from U.C.L.A. in 1979. In 1985 he was granted the Ph.D. in applied physics from the California Institute of Technology. His thesis concerned the application of cyclotron resonance in InSb for heterodyne conversion in the submillimeter-wavelength region.

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Christopher D. Parker was born in Boston, MA, on September 17, 1931. He attended the University of Maine, Orono, majoring in engineering physics.

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Karen M. Molvar received the B.S. degree in Textile Science from the University of Wisconsin-Madison in December 1978.

She joined MIT Lincoln Laboratory in 1980, where she has worked on the fabrication of a number of microwave devices, including surface-oriented mixer diodes, frequency doublers, and FET's. She is currently a Project Technician in the High-Speed Electronics Group working on process development and fabrication of III-V compound high-frequency devices.

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In 1977, he joined Motorola, Inc. From 1979 to 1981, he was with Scientific-Atlanta, where he engaged in research and development pertaining to cable television systems. In September 1983, he joined the faculty of the University of Massachusetts at Amherst, where he is presently Associate Professor of Electrical Engineering. His current research interests include the application of quasi-optical techniques to millimeter-wave circuits and subsystems.

Summary: We have reported the fabrication and the performance characteristics of 1·5 μm strained-layer MQW-DFB lasers. These lasers have narrower linewidth and lower chirp width than that of bulk-active DFB lasers. However, they are only comparable with unstrained MQW-DFB lasers, probably because of their positive detuning. A linewidth as low as 3·5 MHz was observed for one laser at 14·4 mW output. A 1·7 Gbit/s ASK transmission experiment using the strained MQW-DFB laser has been demonstrated with a receiver sensitivity of −37 dBm at BER = 10^{-9} and with 0·3 dB and 0·8 dB power penalty due to dispersion of 40 km and 60 km standard fibre, respectively.

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References

1 ADAMS, A. R.: 'Band-structure engineering for low-threshold high-efficiency semiconductor lasers', *Electron. Lett.*, 1986, 22, pp. 249–250
2 TANBUN-EK, T., LOGAN, R. A., OLSSON, N. A., TEMKIN, H., SERGENT, A. M., and WECHT, K. W.: 'High power output 1·48–1·51 μm continuously graded index separate confinement strained quantum well lasers', *Appl. Phys. Lett.*, 1990, 57, pp. 224–226
3 LAU, K. Y., XIN, S., WANG, W. I., BAR-CHAIM, N., and MITTELSTEIN, M.: 'Enhancement of modulation bandwidth in InGaAs strained-layer single quantum well lasers', *Appl. Phys. Lett.*, 1989, 55, pp. 1173–1175
4 SUEMUNE, I., COLDREN, L. A., YAMANISHI, M., and KAN, Y.: 'Extremely wide modulation bandwidth in a low threshold current strained quantum well laser', *Appl. Phys. Lett.*, 1988, 53, pp. 1378–1380
5 OHTOSHI, T., and CHINONE, N.: 'Linewidth enhancement factor in strained quantum well lasers', *IEEE Photon. Technol. Lett.*, 1989, 1, pp. 117–119
6 YABLONOVITCH, E., and KANE, E. O.: 'Reduction of lasing threshold current density by the lowering of valence band effective mass', *IEEE J. Lightwave Technol.*, 1986, LT-4, pp. 504–506
7 TEMKIN, H., TANBUN-EK, T., and LOGAN, R. A.: 'Strained InGaAs/InP quantum well lasers', *Appl. Phys. Lett.*, 1990, 56, pp. 1210–1212
8 TEMKIN, H., TANBUN-EK, T., LOGAN, R. A., LEWIS, J. A., and DUTTA, N. K.: 'InGaAs/InP graded index quantum well lasers with nearly ideal static characteristics', *Appl. Phys. Lett.*, 1990, 56, pp. 1222–1224
9 DUTTA, N. K., TEMKIN, H., TANBUN-EK, T., and LOGAN, R. A.: 'Linewidth enhancement factor for InGaAs/InP strained quantum well lasers', *Appl. Phys. Lett.*, 1990, 57, p. 1390
10 WANG, S. J., DUTTA, N. K., and GNAUCK, A. H.: 'Dynamic and CW linewidth measurements of buried heterostructure distributed feedback lasers', *IEEE Photon. Technol. Lett.*, 1989, 1, pp. 215–217
11 WANG, S. J., KETELSEN, L. J. P., MCCRARY, V. R., TWU, Y., NAPHOLTZ, S. G., and WERNER, W. V.: 'Dynamic and CW linewidth measurements of 1·55-μm InGaAs/InGaAsP multiquantum well distributed feedback lasers', *IEEE Photon. Technol. Lett.*, 1990, 2, pp. 775–777
12 WANG, S. J., KUO, C. Y., PARAYANTHAL, P., SHEN, T. M., MILLEV, M. P., and HARTMAN, R. L.: 'A 1·7 Gbit/s ASK and A 622 Mb/s incoherent FSK transmission experiment using a 1·55-μm multiquantum well distributed feedback laser', *IEEE Photon. Technol. Lett.*, to be published

APPENDIX K RESONANT-TUNNELLING DIODE OSCILLATOR USING A SLOT-COUPLED QUASIOPTICAL OPEN RESONATOR

Indexing terms: Tunnel diodes, Oscillators, Microwave oscillation

A resonant-tunnelling diode has oscillated at X-band frequencies in a microwave circuit consisting of a slot antenna coupled to a semiconfocal open resonator. Coupling between the open resonator and the slot oscillator improves the noise-to-carrier ratio by about 36 dB relative to that of the slot oscillator alone in the 100–200 kHz range. A circuit operating near 10 GHz has been designed as a scale model for millimetre- and submillimetre-wave applications.

The resonant-tunnelling diode (RTD) is a quantum-well structure which exhibits negative resistance that extends into the submillimetre-wave range. Fundamental-frequency oscillations at 675 GHz have recently been obtained from RTDs,[1] and detection experiments have demonstrated that the negative resistance responsible for these oscillators may persist to frequencies as high as 2·5 THz.[2] Planar circuits are more easily fabricated than waveguide circuits above 100 GHz, so a hybrid, planar, quasioptical RTD oscillator circuit whose essential features can be scaled for use at millimetre wavelengths have been developed. Instead of the customary reactive-network lowpass filter for biasing, a unique low-impedance, lossy transmission line has been used to isolate the RTD from external bias circuitry. A semiconfocal open cavity has also been used as a resonator, which allows very high quality factor Q and improves the spectral purity of the oscillator. Coupling of a microstrip line to an open resonator has been demonstrated.[3] This is the first time a planar oscillator has been coupled to an open resonator with a slot antenna.

The oscillator is illustrated in Fig. 1. A concave brass reflector faces a microwave circuit substrate that is clad with copper on the side facing away from the concave reflector. The separation distance, D, between the circuit and reflector is adjustable in the 15–20 mm range. The lowest-order (TEM_{00q}) mode of the open resonator thus formed[4] is in the 8–10 GHz range. The Gaussian beam waist radius is 28 mm and lies well within the area of the 10 cm by 10 cm-square flat reflector as well as the larger spherical reflector, so diffraction losses are negligible. An unloaded Q of 3500 was measured for the TEM_{009} mode. This is a reasonable Q for a short open resonator.

The RTD was fabricated by molecular-beam epitaxy and has the material parameters, current–voltage characteristics, and the waveguide-oscillator performance described by Brown *et al.*[5] The resonant-tunnelling structure in the diode consists of two 1·5 nm-thick undoped AlAs barriers separated by a 4·5 nm-thick undoped GaAs quantum well. The GaAs regions outside each barrier were uniformly doped n-type with a concentration of $N_D = 2 \times 10^{17}$ cm^{-3}. The current density and specific capacitance of this device are known from previous

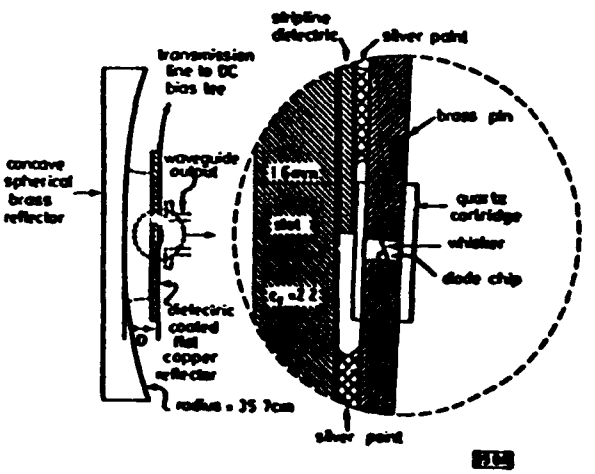

Fig. 1 *Quasioptical RTD oscillator with enlarged view of diode area*

measurements[5] to be 4.5×10^4 A cm^{-2} and about 1.6 fF μm^{-2}, respectively, at the bias voltage for peak current (i.e. the low-voltage end of the negative-resistance region). The diode used in the present experiment was a 4 μm-diameter mesa with a peak current of 3.3 mA at a peak voltage of 0.7 V, and a peak-to-valley current ratio of about two at room temperature. The diode chip was mounted on a 0.6 mm-diameter post and inserted into a 2.5 mm-long quartz tube, where a tungsten whisker mounted on a similar post contacted the device (Fig. 1). Cyanoacrylate fixes the posts in the quartz tube. Although this package provides great convenience in handling, it has parasitic reactances that preclude its use above 30 GHz.

RTDs show negative resistance at all frequencies from DC up to the oscillation frequency. A bias circuit that suppresses undesired oscillations over such a broad frequency range presents a formidable challenge. The solution to this problem uses a lossy distributed element, rather than a low-loss reactive filter. Leading from the external low-frequency bias network to the diode circuit was a 6.3 mm-wide parallel-plate transmission line made from 0.25 mm-thick fibreglass circuit board material with copper cladding on both sides. The bias line accomplishes two things. It has a low characteristic impedance, $Z_0 \simeq 7.5\,\Omega$, which provides for DC stability of the oscillator. It also presents a high loss (metallic and dielectric) per unit length, which significantly lowers the Q of all resonances in the bias circuit and thus prevents the occurrence of spurious oscillations in this circuit at frequencies below those of interest. The transmission line was 27 cm long, a length that approaches the ideal situation of an infinite line whose input impedance is Z_0, regardless of how the external bias circuit terminates the far end. At low frequencies, the transmission-line attenuation was insufficient for effective isolation, but normal termination and bypass measures with lumped-element networks at the bias end of the line prevented oscillations in that range of frequencies. In a monolithic version of this circuit, highly doped GaAs beneath a thin insulating layer could be used for the lossy dielectric. Metal-insulator-semiconductor slow-wave transmission lines have shown losses as high as 17.5 dB/cm at 5 GHz,[6] and this loss could easily be increased.

The diode package was placed in a circuit consisting of the diode, the parallel-plate bias line, and a slot in the single copper cladding of the resonator's flat reflector. The narrow dimension of the slot is shown in Fig. 1 and is approximately 0.13 mm. The wide dimension l runs perpendicular to the Figure and was about 6.3 mm. The equivalent circuit that best models the oscillator is shown in Fig. 2. At 8.9 GHz, the slot can be represented as an inductance L_s that is calculated to be about 1 nH. The semiconfocal cavity resonance occurs at a radian frequency $\omega_r = [L_r C_r]^{-1/2}$ and is represented by a series resonant circuit in which the energy storage is modelled by L_r and C_r, and the power losses are represented by R_r. The overall circuit resonance occurs at a frequency just below ω_r where the capacitive susceptance of the series resonant circuit cancels the inductive susceptance of the slot. At resonance, the cavity-slot circuit acts as an impedance inverter, transforming the resistance R_r into a higher resistance $R_s = (\omega L_s)^2/R_r$. For sufficiently high Q, R_s is large compared with the lossy line Z_0 at resonance, so that most of the current generated by the RTD is coupled to the external RF load, leading to smaller losses in the bias network.

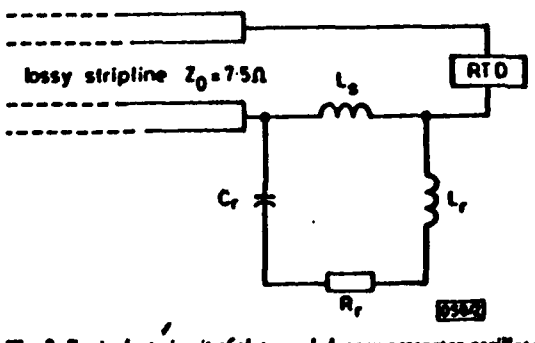

Fig. 2 Equivalent circuit of slot-coupled, open-resonator oscillator

Measurements were performed on the oscillator both with and without the open resonator in place. In both cases the output was monitored by means of an X-band waveguide flange that was placed as close as possible to the diode side of the slot. Although this coupling was rather inefficient, it was sufficient to permit spectral measurements.

The diode, its package parasitics, and the slot inductance form a low-Q resonant circuit that allows oscillation in the 8 GHz range in the absence of the spherical reflector. The spectrum is very broad, as the data for the no-resonator case in Fig. 3 shows. When the spherical reflector is moved into

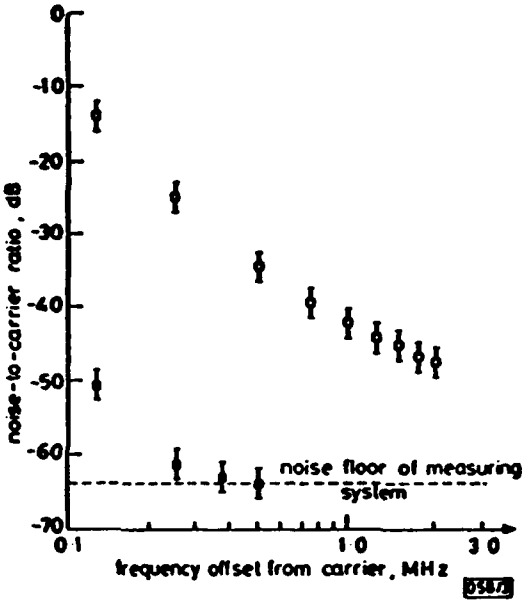

Fig. 3 Noise-to-carrier ratio $\mathcal{L}(f)$ for RTD oscillator
no open resonator; open resonator

position and D is slowly varied so that the resonant frequency of the TEM_{00q} mode sweeps past the free-running oscillator frequency, the oscillator locks onto the cavity mode. When locked, the noise-to-carrier ratio $\mathcal{L}(f)$ in the 100–200 kHz offset range decreases by about 36 dB, and the oscillator can be tuned over a 2.5% range by adjusting D. According to the elementary oscillator noise theory of Vendelin,[7] the value of $\mathcal{L}(f)$ (in the sideband frequency ranges not dominated by $1/f$ device noise) goes as Q_e^{-2} where Q_e is the unloaded quality factor of the resonant circuit. If Q_e with the open resonator is assumed to be 3500, the observed 36 dB decrease in noise would result if the slot-oscillator circuit Q_e was about 55. This value of Q_e is in the range to be expected from a planar-circuit oscillator. Although diodes of this type have produced as much as 150 μW in waveguide cavities, the unoptimised output power of this oscillator into the waveguide flange was only about 10 μW. This could be improved by a more sophisticated output coupling method such as the partially reflecting dielectric plate used by Popovic *et al.*[8] in their quasioptical grid oscillator.

The quasioptical oscillator demonstrated can be scaled down in size for operation at millimetre and submillimetre wavelengths and could generate much higher power by incorporating many RTD slot-oscillators in a planar array. Fig. 4 shows a planar array of RTD slot oscillators in which the open resonator both synchronises the oscillator elements and narrows the linewidth. The lossy bias line feeds an entire row of such oscillators. In contrast to waveguide resonators, the Q of an open resonator of fixed size increases with frequency, so that this design should be very useful for the submillimetre-wavelength region.

The use of a quasioptical cavity and slot antenna as a resonator for an RTD oscillator has been demonstrated. The quasioptical cavity reduces the noise-to-carrier ratio by about 36 dB compared with the slot oscillator alone in the 100–200 kHz range. Variation of the cavity length leads to a 2.5% tunability of the oscillation frequency. This oscillator design is expected to be useful in the submillimetre-wavelength region

where the RTD has shown great promise as a fundamental solid-state oscillator.

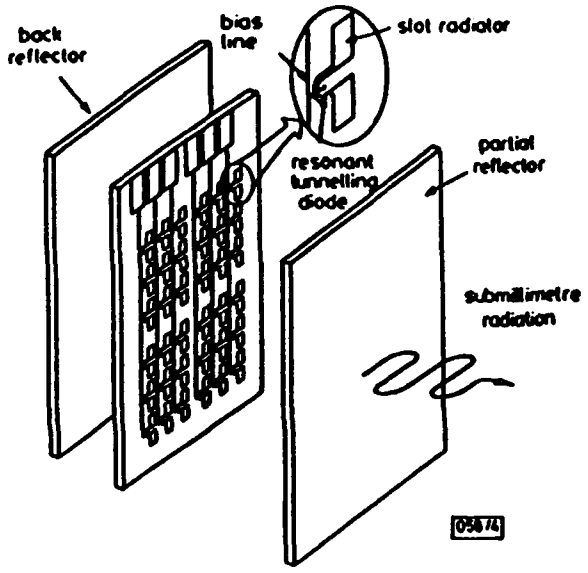

Fig. 4 *Planar-monolithic array of RTD oscillators synchronized by quasioptical cavity*

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References

1 BROWN, E. R., PARKER, C. D., MAHONEY, L. J., SÖDERSTRÖM, J. R., and MCGILL, T. C.: 'Room-temperature oscillations up to 675GHz in InAs/AlSb resonant-tunneling diodes'. 1990 Device Research Conference, Santa Barbara, USA

2 SOLLNER, T. C. L. G., GOODHUE, W. D., TANNENWALD, P. E., PARKER, C. D., and PECK, D. D.: 'Resonant tunneling through quantum wells at frequencies up to 2·5 THz', *Appl. Phys. Lett.*, 1983, 43, pp. 588–590

3 STEPHAN, K. D., YOUNG, S. L., and WONG, S. C.: 'Microstrip circuit applications of high-Q open microwave resonators', *IEEE Trans.*, 1988, MTT-36, pp. 1319–1327

4 JONES, R. G.: 'Precise dielectric measurements at 35GHz using an open microwave resonator', *Proc. IEE*, 1976, 123, pp. 285–290

5 BROWN, E. R., GOODHUE, W. D., and SOLLNER, T. C. L. G.: 'Fundamental oscillations up to 200GHz in resonant tunneling diodes and new estimates of their maximum oscillation frequency from stationary-state tunneling theory', *J. Appl. Phys.*, 1988, 64, pp. 1519–1529

6 HASEGAWA, H., and OKIZAKI, H.: 'M.I.S. and Schottky slow-wave coplanar striplines on GaAs substrates', *Electron. Lett.*, 1977, 13, pp. 663–664

7 VENDELIN, G. D., PAVIO, A. M., and ROHDE, U. L.: 'Microwave circuit design, using linear and nonlinear techniques' (Wiley, New York, 1990)

8 POPOVIC, Z. B., KIM, M., and RUTLEDGE, D. B.: 'Grid oscillators', *Int. J. Infrared Millimetre Waves*, 1989, 10, pp. 1003–1010

CHIRP COMPENSATION CAPABILITY OF A SEMICONDUCTOR LASER AMPLIFIER

Indexing terms: Lasers and laser applications, Semiconductor lasers, Amplifiers

Performance improvement is reported resulting from incorporating a semiconductor laser amplifier (SLA) as a post-transmitter-amplifier in long-haul directly modulated optical systems operating in the 1·5 μm region. This improvement arises from reduction of the chirp produced by the semiconductor laser as the signal passes through the SLA. Eye closure penalty improvements in excess of 5 dB are observed for an illustrative long-haul 4·8 Gbit/s system.

Introduction: Long-haul high-data-rate direct-modulation optical-fibre communication systems, operating in the 1·5 μm wavelength region with conventional single-mode optical fibre, can be seriously impaired by interactions between laser dynamic frequency chirp and fibre chromatic dispersion. Insertion of a semiconductor laser amplifier as a post-transmitter amplifier enables the source laser to be operated at reduced power levels. This can help alleviate several problems associated with direct modulation of the semiconductor laser at high output powers, such as large chirp and the difficulty of implementing suitable drive circuits.[1] We show here that this configuration can also compensate for the frequency chirp of directly modulated lasers, thus improving the performance of long-haul systems. This happens because even with the modest peak power available from semiconductor lasers, the nonlinear properties of the SLA can be significant, yielding an amplified signal with an imposed frequency chirp, which counteracts the chirping of the directly modulated laser.[2]

System model and analysis: The block diagram of Fig. 1 shows the functional elements of a fibre-optic system using direct intensity modulation and post amplification. The optical source is assumed to be a DFB laser that is directly modulated by its drive current. The data patterns used are pseudo-

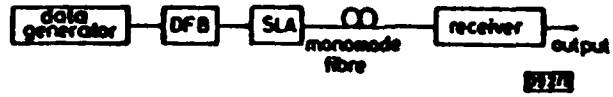

Fig. 1 *Block diagram of direct-detection optical communication system incorporating SLA as post-transmitter amplifier*

random sequences of length $2^5 - 1$. The response of the semiconductor laser in terms of optical power $P(t)$ and phase $\phi(t)$ is determined by solving the large-signal rate equations. The complex envelope of the electromagnetic field of the laser output can be represented by $E(t) = \sqrt{[P(t)]} \exp[j\phi(t)]$. The output field of the SLA, $E_{out}(t)$, taking into account the effect of facet reflectivities and gain saturation can be expressed in terms of the input optical field $E_{in}(t)$ and the physical parameters of the SLA:[3]

$$E_{out}(t) = t_2 t_1 E_{in}(t-\tau) \times \exp\left\{\tfrac{1}{2}G(t) - j\left[\frac{\alpha}{2}G(t) + KL\right]\right\} + r_1 r_2 E_{out}(t-2\tau) \times \exp\left\{\frac{G(t)+G(t-\tau)}{2} - j\left\langle\frac{\alpha[G(t)+G(t-\tau)]}{2} + 2KL\right\rangle\right\} \quad (1)$$

$$\frac{dG(t)}{dt} = \frac{G_0 - G(t)}{\tau_c} - \frac{t_2^{-2}|E_{out}(t)|^2}{E_{sat}}[1 - \exp(-G(t))] - \frac{r_2^2 t_2^{-2}|E_{out}(t-\tau)|^2}{E_{sat}}[\exp G(t) - 1] \quad (2)$$

APPENDIX L

5-mW Parallel-Connected Resonant-Tunneling-Diode Oscillator

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5-mW Parallel-Connected Resonant-Tunneling-Diode Oscillator

Abstract: A novel oscillator using an array of 25 resonant-tunneling diodes connected in parallel has delivered an output power of 5 mW at 1.18 GHz, which is the highest microwave power ever obtained from a resonant-tunneling quantum-well device. Details of the device design and the oscillator circuit are given.

Introduction: We report a new type of resonant-tunneling-diode (RTD) oscillator that generates 5 mW at 1.18 GHz. This was obtained by paralleling 25 individual diodes designed for such a connection. Since RTD oscillators have generated power at fundamental frequencies as high as 712 GHz,[1] advances in device power output have important implications for millimeter-wave and submillimeter-wave power generation.

Device: The diode used in these experiments is an RTD containing four barriers instead of the usual two. The quantum wells and cladding layers are made from $In_{0.53}Ga_{0.47}As$ (lattice matched to InP), and the barriers are made from AlAs. The advantage of the new device is that the voltage range of the negative differential resistance (NDR) region, ΔV, is approximately three times that of a typical double-barrier device.[2] Since the power delivered to the load is proportional to $(\Delta V)^2$ for a given resonator circuit, this increases the available oscillator power by approximately nine times. To achieve this level of power, the total area of the diode must be such that the average negative resistance of the diode, $|R|$, is matched to load resistance R_L.

In the present experiment, we designed R_L to be approximately 5 Ω. This resistance required a relatively large total diode area (roughly 1000 μm^2) to achieve the matched condition. A single diode having this area would be destroyed by overheating if biased anywhere in the NDR region. To reduce the device heating, we fabricated an array of 25 diodes in parallel using planar fabrication techniques. Each diode had an area of approximately 60 μm^2 and was positioned on a square grid with 24 μm between the centers of nearest neighbors. The connection between

elements of the array was accomplished by a central contact pad deposited on top of a silicon nitride planarizing layer. We estimate the maximum frequency of oscillation of a single diode to be 120 GHz.

Experiment and results: The test circuit is shown in Fig. 1. The 25-diode chip was packaged on a standard TO5 header whose parasitic inductance limited the frequency of oscillation in the circuit. The TO5 header was connected to one end of a resonator loop fabricated from a 8-mm-wide, 6-mm-long piece of thin brass sheet. The loop extended away from the header ground plane in the shape of an upside-down "U" with the other end going to the bias circuit. The output coupling was achieved by a copper strip that fitted over the resonator and was separated from it by a thin plastic insulating sheet. The resonator and coupling loop are shown as transformer T_1 in Fig. 1. Because the NDR of an RTD extends in frequency down to DC, they are prone to bias-circuit oscillations. For these devices, we found that a technique similar to that used by us in a previous 10-GHz RTD oscillator[3] was effective in eliminating oscillation below the desired frequency. The low-impedance microstrip transmission line shown in Fig. 1 presented nearly a short circuit to the diode at low frequencies, stabilizing it outside the frequency range of oscillation.

The current-voltage (I-V) characteristic of the 25 parallel-connected diodes is given in Fig. 2 for a negative voltage applied to the top contact and the substrate at ground. Estimating the maximum theoretical power by the formula $(3/16)(\Delta V)(\Delta I)$ [4] we predicted about 20 mW based upon this I-V curve. The highest power we have obtained from this circuit in preliminary experiments is 5 mW at the output of a three-stub tuner, measured with a power sensor. The corresponding bias was -1.949 V at -131 mA, and the spectrum of this output is shown in Fig. 3. All harmonics were at least 23 dB down from the fundamental.

Conclusions: We have obtained a power of 5 mW at 1.18 GHz from a parallel combination of 25 RTDs. In addition to demonstrating a new type of RTD oscillator, this experiment demonstrates that RTDs can successfully be used in a chip-level power-combining circuit.

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References

[1] BROWN, E. R., PARKER, C. D., MOLVAR, K. M., CONNORS, M. K., and STEPHAN, K. D.: 'Recent advances in resonant-tunneling diode oscillators', *Proc. of Second Int'l. Symp. on Space Terahertz Technology*, 1991, Pasadena, CA, pp. 133-144

[2] BROWN, E. R., CALAWA, A. R., MANFRA, M. J., and PARKER, C. D.: 'Enhanced negative differential resistance in a resonant tunneling structure', submitted to *Appl. Phys. Lett.*

[3] STEPHAN, K. D., BROWN, E. R., PARKER, C. D., GOODHUE, W. D., CHEN, C.-L., SOLLNER, T. C. L. G.: 'Resonant-tunneling diode oscillator using a slot-coupled quasioptical open resonator', *Electron. Lett.*, 1991, 27, pp. 647-649

[4] BROWN, E. R., SOLLNER, T. C. L. G., GOODHUE, W. D., and PARKER, C. D., 'Millimeter-band oscillations based on resonant tunneling in a double-barrier diode at room temperature', *Appl. Phys. Lett.*, 1987, 50, pp. 83-85

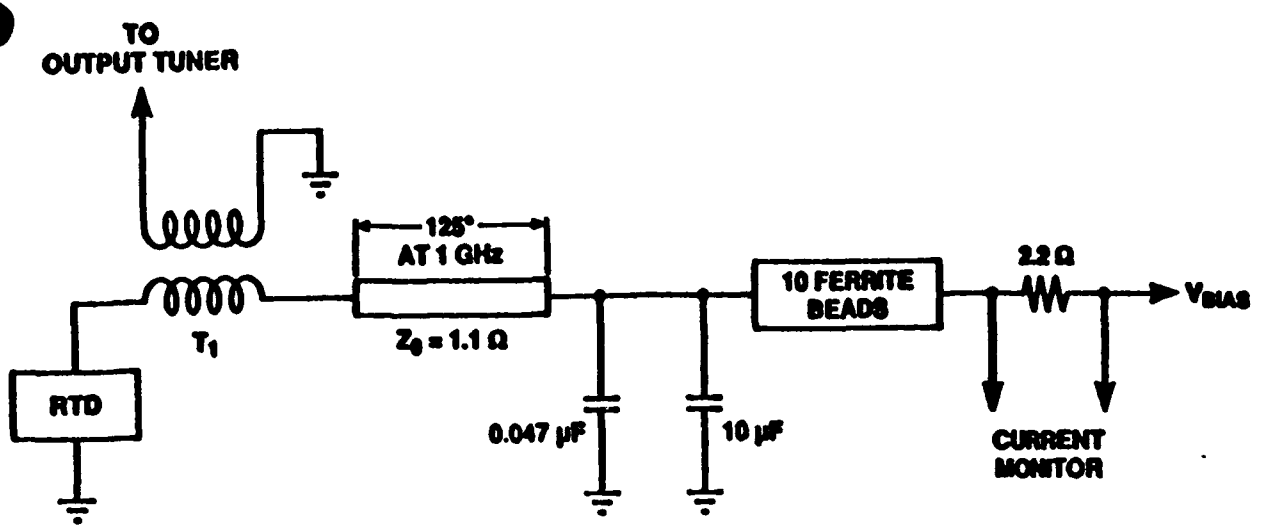

Fig. 1. Oscillator circuit using 25 parallel-connected RTDs

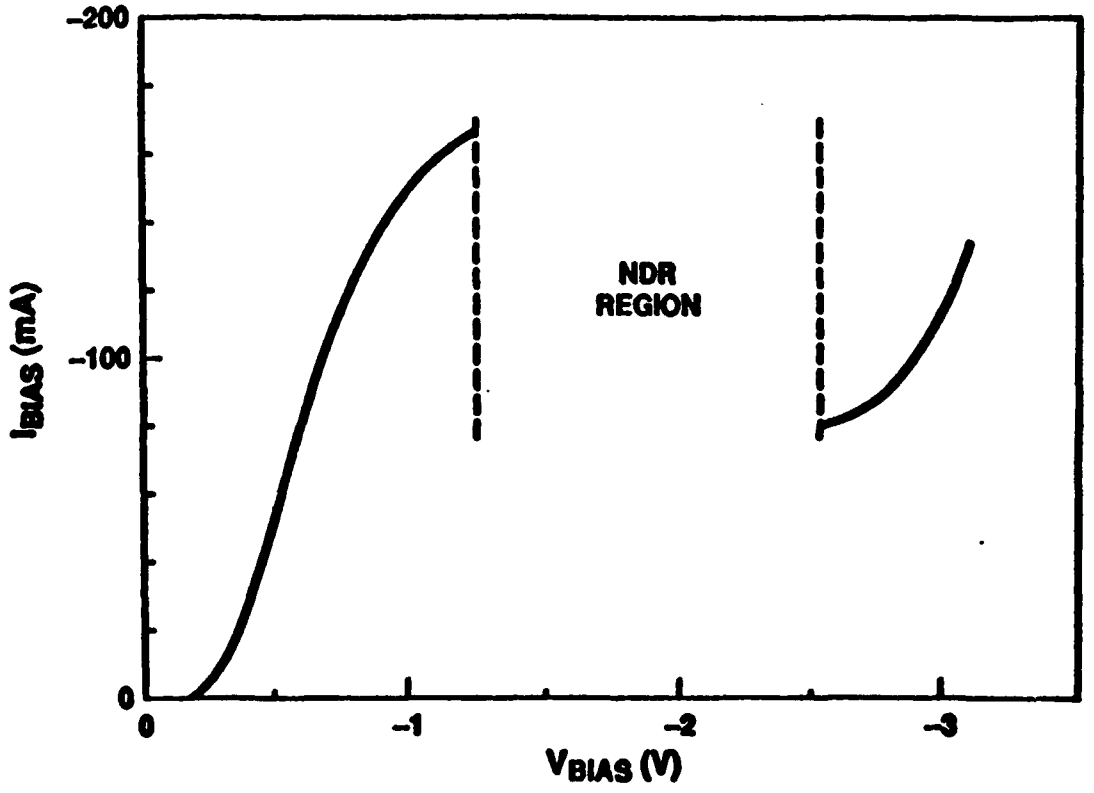

Fig. 2. I-V characteristic of 25 parallel-connected RTDs.

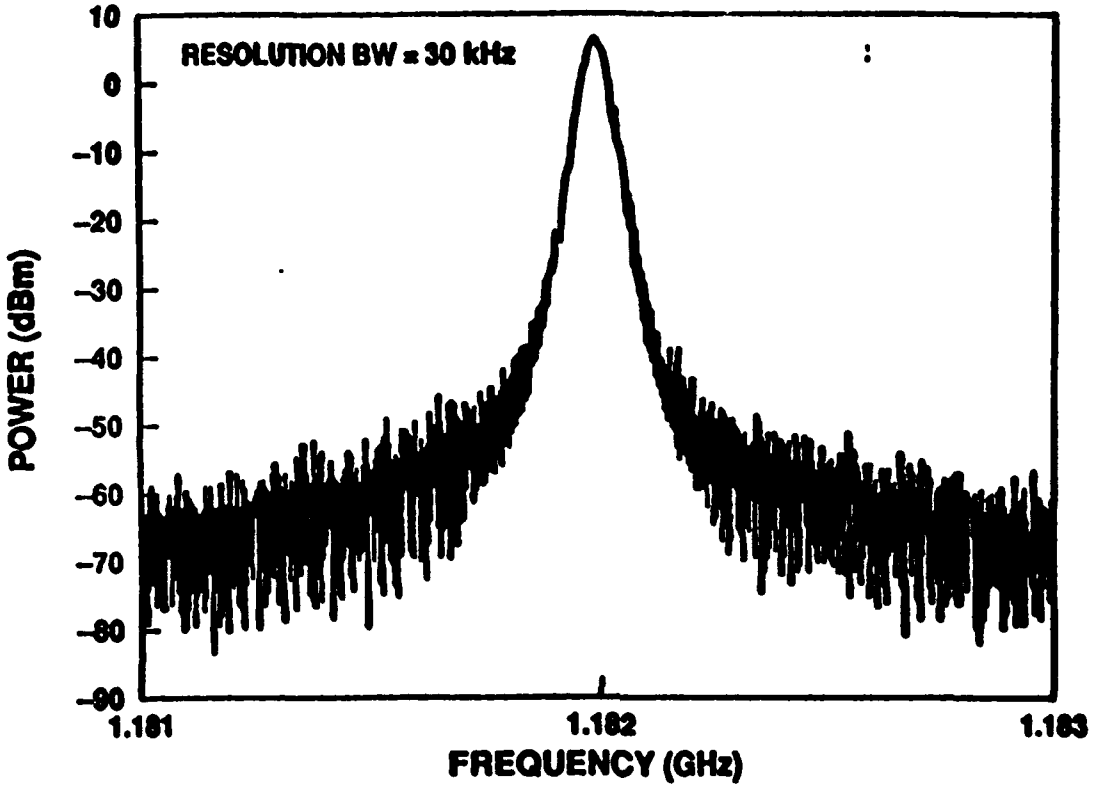

Fig. 3. Spectrum of oscillator output.

APPENDIX M

Resonant-tunneling-diode loads: speed limits and applications in fast logic circuits

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There is a need for low-power, high-speed digital devices in a wide array of applications including logic, static memory, and signal processing. In this paper we show that the high-speed and negative-resistance properties of the resonant-tunneling diode (RTD) can improve the performance of some common inverters by greatly reducing the static power dissipation while affecting the dynamic properties to a much lesser extent. We examine the RTD used as a load for: (1) the heterostructure field-effect transistor (HFET) in a direct-coupled FET logic (DCFL) configuration like that in [1], and (2) the heterojunction bipolar transistor (HBT) in an integrated-injection logic (I^2L) configuration [2].

The resonant-tunneling diode (RTD) is a quantum-transport device that has attracted much attention in recent years because of the high-speed negative differential resistance (NDR) region in its current-voltage (I-V) curve. Fundamental oscillations in the NDR region have been obtained up to 712 GHz [3] in the highest-quality diodes. Shown in Fig. 1 is the current density vs voltage (J-V) curve of a candidate RTD for high-speed low-power digital applications. It consists two 1.4-nm-thick AlAs barriers separated by a 5.9-nm-thick $In_{0.53}Ga_{0.47}As$ quantum well. The peak current density J_P is 1.4×10^5 A cm^{-2} and the peak-to-valley current ratio (PVCR) of this device is 12. At the peak voltage the specific capacitance C_S is approximately 1.5 fF μm^{-2}. The theoretical RC-limited switching time t_{RC} from the peak to the valley point is approximately 2 ps. This is roughly ten times shorter than the switching time of the p-n (Esaki) tunnel diode, a negative resistance device that can also function as a load element for transistors [4].

In the HFET-RTD inverter configuration, the RTD presents the load line shown in Fig. 2. The static transfer characteristic of the inverter computed by using SPICE 2G is given in Fig. 3. The RTD I-V curve used is a polynomial representation of a 1.5-μm^2-area InGaAs diode. The HFET I-V characteristics used are those of a SPICE model representing a 1.0-μm-gate-length, 10-μm-wide InGaAs enhancement-mode (E)-HFET having a channel sheet density of approximately 2×10^{12} cm^{-2}. The unity-current-gain cutoff frequency of this HFET is 22 GHz. The low static power P_S in the low-output-voltage (V_{OUT}^{LO}) state is an attractive feature, similar to that displayed by the MESFET Esaki-diode inverter in [4]. From Table I, we see that the static power can be as low as 24 μW but increases rapidly as V_{DD} goes from 0.75 to 0.9 V. The sensitivity of the inverter characteristics to V_{DD} as well as the effect of RTD and HFET device variations on logic performance will be discussed.

The dynamic properties of this HFET-RTD inverter were determined by SPICE simulations of ring oscillators. The gate capacitance of the HFET was assumed to be 2 fF per micrometer of gate length per micrometer of gate width. An additional 10 fF is connected between the output node and ground to simulate interconnect capacitance. The switching delay time t_d is 62 ps when P_S = 24 μW and decreases slowly with V_{DD}, as does the dynamic

power P_D. The switching energy $E = P_D \times t_d$ is 3.6 fJ for $V_{DD} = 0.75$ V. For comparison, Table I shows the simulated result for a conventional DCFL inverter consisting of the same (E)-HFET InGaAs inverter as above but with a depletion-mode (D)-InGaAs HFET load. The E-D HFET inverter operates with less than half the switching delay but nearly 5 times the static power and 80% higher power-delay product compared to the inverter above. The longer t_d of the HFET-RTD inverter stems from a slow V_{OUT}^{LO} to V_{OUT}^{HI} transition. The higher power-delay product of the E-D HFET is caused by the nearly two-times greater output node capacitance of the D-HFET load compared to the RTD load. Table I also shows the effect of varying the HFET size. Reducing the gate length to 0.5 μm does not change P_S but decreases t_d and E by just over a factor of two. This demonstrates that the driver HFET is limiting the speed of the HFET-RTD inverter.

A bipolar analog of the HFET-RTD inverter can be made with the RTD as the load element and an HBT as the driver. In this configuration, HBTs can potentially provide higher transconductance than the FETs, leading to higher fan-out capability. The uniformity of the turn-on voltage of HBTs is better than that of FETs, potentially leading to greater manufacturability. With HBTs it is also easier to ensure that the transistor peak current is greater than the peak current of the RTD load. A problem associated with HBT use, however, is the fact that with the collector current limited by the RTD, the device enters the saturation regime, which can result in excess base current and excess charge storage. These adverse effects can be alleviated with proper current limiting in the base circuit. A candidate logic circuit is shown in Fig. 4. Preliminary simulations indicate a dramatic reduction in static power dissipation compared to conventional I^2L [2].

In summary, we have shown that InGaAs RTDs having a peak-to-valley ratio of 12 at room temperature can switch in approximately 2 ps and, therefore, are useful as negative resistance loads for heterostructure transistors in digital circuits. We have simulated HFET-RTD and HBT-RTD inverters using SPICE. We have found that t_d of the 1.0-μm-gate-length HFET-RTD inverter is greater than that of the E-D HFET inverter by over a factor of two, the power-delay product is lower by nearly a factor of two, and P_S is lower by a factor of five. A similar contrast is found between HBT-RTD and conventional HBT-I^2L inverters.

Acknowledgments:

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References:

[1] K. L. Lear, K. Yoh, and J. S. Harris, Int. Symp. GaAs and Related Compounds, Atlanta, GA, 1989, p. 593.

[2] C. E. Chang, P. M. Asbeck, K. C. Wang, and E. R. Brown (to be published)

[3] E. R. Brown, J. R. Söderström, C. D. Parker, L. J. Mahoney, K. M. Molvar, and T. C. McGill, Appl. Phys. Lett., vol. 58, pp. 2291-2293, 1991.

[4] K. Lehovec, IEEE J. Solid-State Circuits, vol. 14, pp. 797-800, 1979.

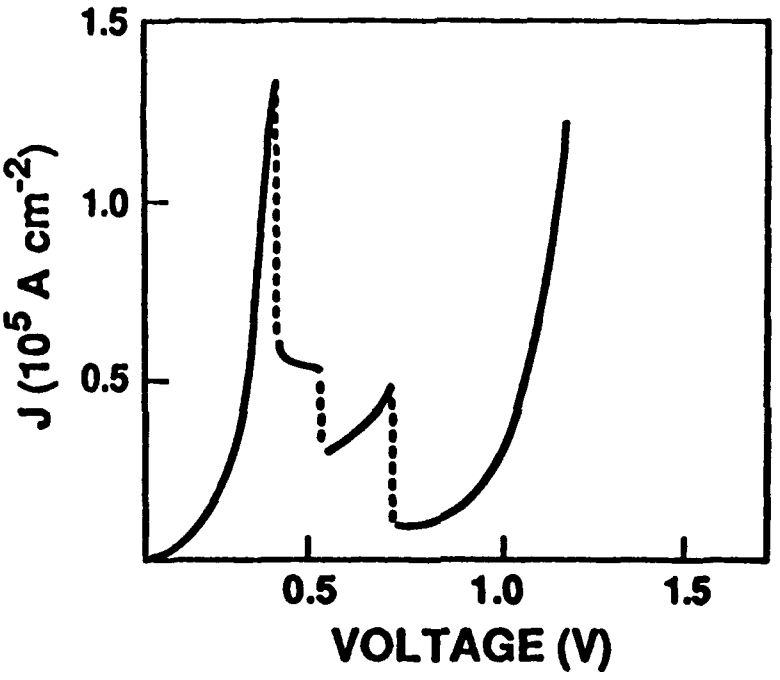

Fig. 1: Current density vs voltage for a low-power high-speed RTD made from the InGaAs/AlAs materials system.

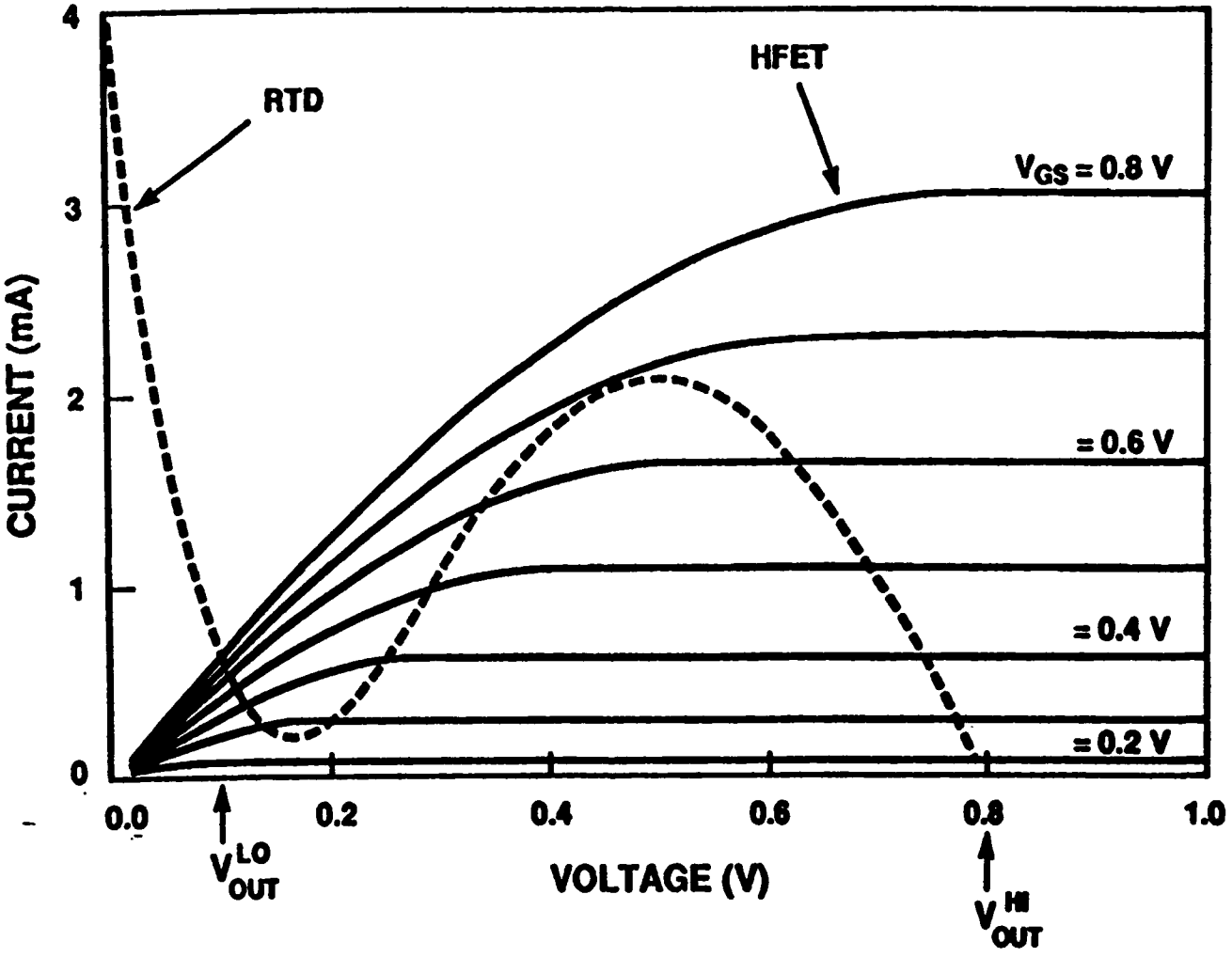

Fig. 2: Current-voltage curves for 1.5-μm^2-area InGaAs/AlAs RTD and 1.0-μm-gate-length InGaAs HFET at room temperature. Both curves are derived from SPICE 2G models.

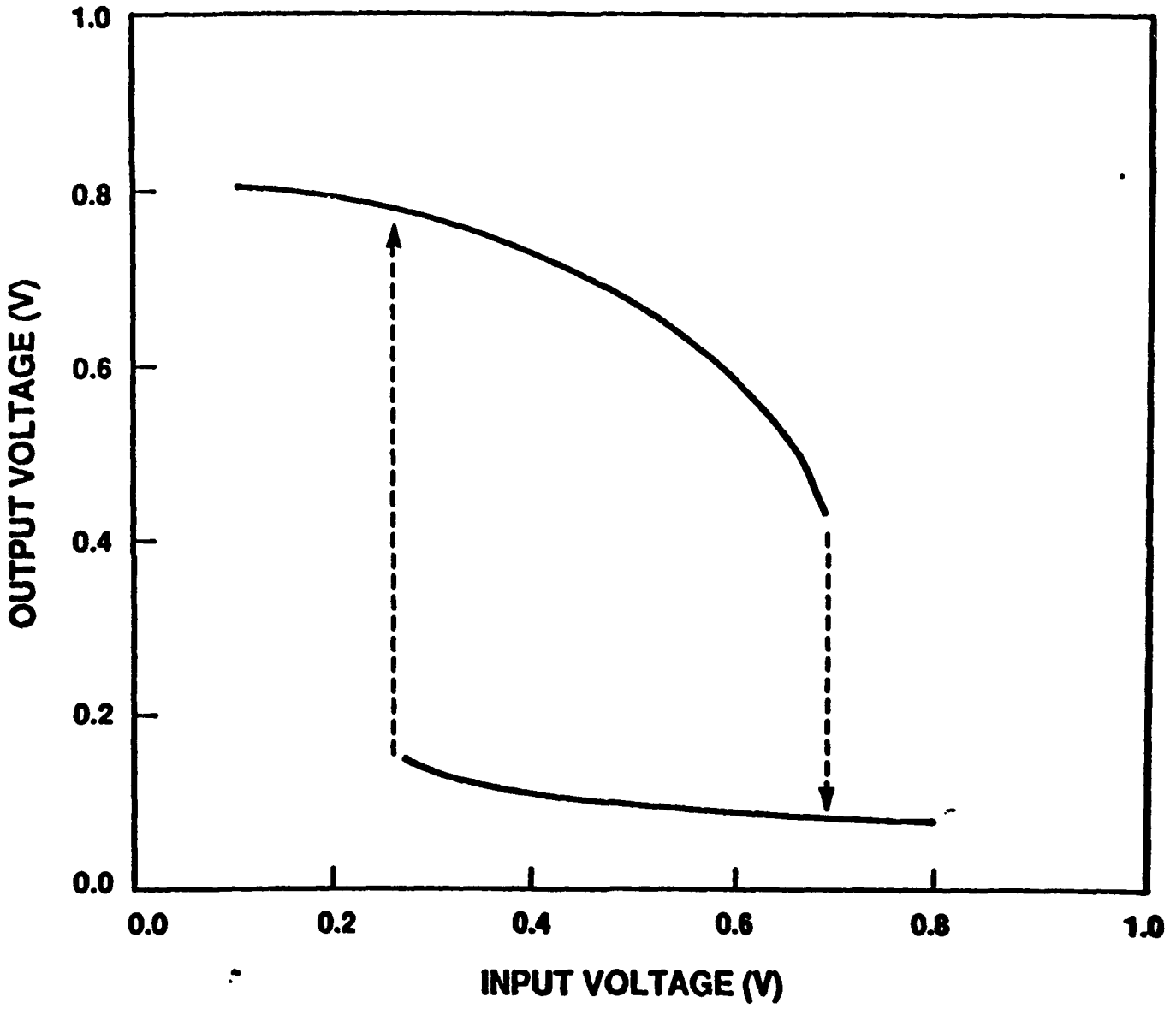

Fig. 3: Transfer characteristic of HFET-RTD inverter of Fig. 2.

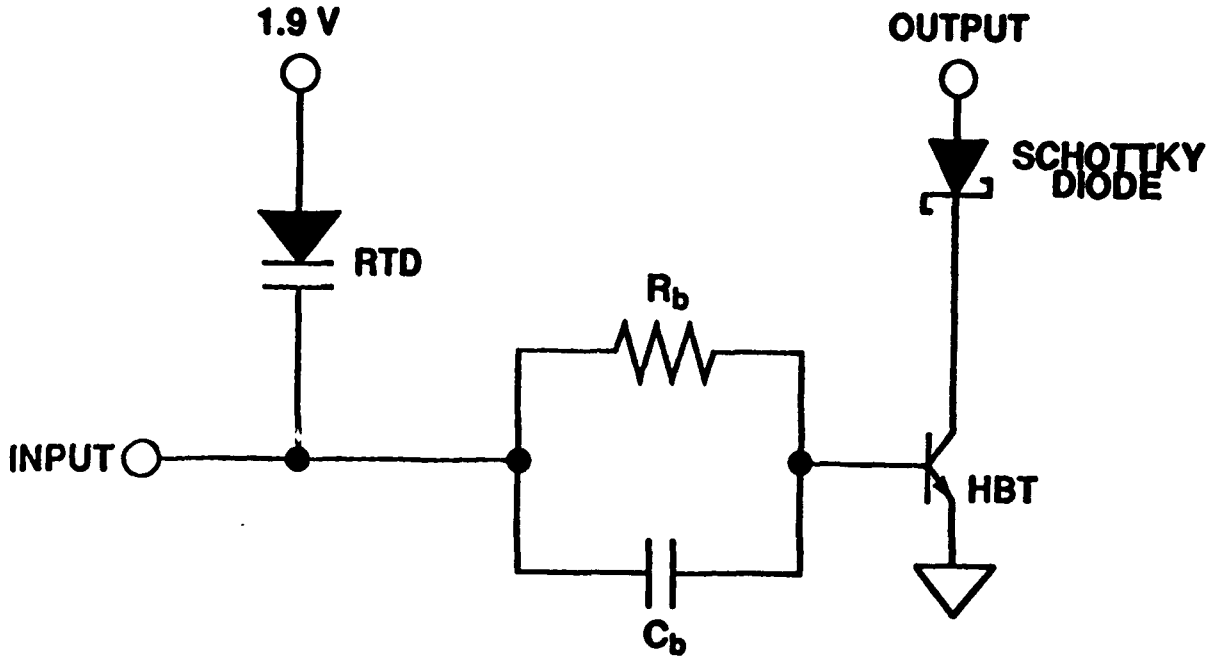

Fig. 4: Circuit diagram for inverter element containing an RTD and an npn HBT.

TABLE I. HFET-RTD INVERTER RESULTS

INVERTER CONFIGURATION	V_{DD} (V)	P_S (μW)	td (ps)	P_D(μW)	E (fJ)
1.0 μm-GATE InGaAs E-HFET 1.5 μm^2 InGaAs RTD	0.75	24	62	58	3.6
1.0 μm-GATE InGaAs E-HFET 1.5 μm^2 InGaAs RTD	0.9	250	55	52	2.9
0.5 μm-GATE InGaAs E-HFET 1.5 μm^2 InGaAs RTD	0.75	23	28	50	1.4
1.0 μm-GATE InGaAs E-HFET 1.0 μm-GATE InGaAs D-HFET	0.75	117	27	243	6.6

APPENDIX N

Analysis of Heterojunction Bipolar Transistor/ Resonant-Tunneling-Diode Logic for Low-Power and High-Speed Digital Applications*

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Abstract

A new high-speed digital logic family based on heterojunction bipolar transistors (HBTs) and resonant tunneling diodes (RTDs) is proposed. The negative differential resistance of an RTD is used to significantly decrease the static power dissipation. SPICE simulations indicate that a switching speed below 150 ps at 0.09-mW static power dissipation per gate should be obtainable.

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I. Introduction

Many present and future digital systems demand ultrahigh-speed operation, high levels of integration, and low power dissipation. These three requirements often conflict, and therefore the design of practical logic families reflects application-specific compromises. For ultrahigh speed, the heterojunction bipolar transistor (HBT) provides significant advantages over competing transistor technology. HBT-based ECL frequency dividers have operated up to 36 GHz [1], but the high speed comes at the cost of high power consumption. Power dissipation comprises the dynamic power dissipation (while gates are switching) and the static power dissipation (consumed even without switching operations). The dynamic power dissipation is determined by the need to charge output capacitances. However, in most circuits the majority of the power dissipation is static power. It is of significant interest to develop logic approaches with HBTs and other high-speed devices that minimize static power, as occurs in CMOS. In this paper, a novel logic approach is proposed and analyzed that employs the negative differential resistance (NDR) of RTDs to reduce static power dissipation.

The use of NDR loads in logic circuits has been previously discussed. Lehovec [2] proposed the application of Esaki tunnel diodes as load devices for GaAs MESFET-based circuits. Later, a related logic family combining RTDs and HFETs was analyzed by Lear [3]. The RTDs provide a significant improvement in performance as compared with Esaki tunnel diodes. In particular, the device capacitance, which is high in Esaki tunnel diodes because of the required high doping densities, can be reduced roughly tenfold. Furthermore, the output current vs voltage (I-V) characteristics can be tailored by appropriate bandgap engineering to provide the desired shape. In recent years, RTDs have been demonstrated in high-performance oscillators operating up to 712 GHz [4] with typical current densities greater than 1×10^5 A cm^{-2} [5].

This paper discusses a logic family that combines RTD loads with HBTs. The use of HBTs rather than FETs provides a number of advantages. As discussed below, the high transconductance of HBTs allows the devices to operate at high speed with relatively low voltage swings. The high transconductance also minimizes the hysteresis in the static transfer characteristic, which is a natural consequence of the RTD I-V curve. Not only do HBTs naturally provide the threshold voltage control necessary for logic with

low voltage swings, but they also are compact devices with very high unity-current-gain frequency f_T (above 50 GHz) that permits the realization of high-speed circuits. Moreover, fabrication approaches for RTDs and HBTs appear to be compatible. In principle, the logic family discussed here could be realized with either silicon or heterojunction bipolar technology.

The use of bipolar transistors in conjunction with RTDs also has a disadvantage compared to FET approaches. In the circuit described below, the saturation of the bipolar transistor in one of the logic states results in excess current and minority-carrier charge storage in the base. A novel approach to alleviating these problems is discussed here.

The paper first presents a description of the proposed HBT/RTD circuit topology. This is followed by a discussion of the SPICE models and the simulated performance of a few specific circuits. Last, future prospects for realization are discussed.

II. Circuit Description

A schematic diagram of the HBT/RTD inverter is presented in Fig. 1. In this configuration, the RTD functions as a source of current for the base as well as a pull-up load for the previous stage (not shown in Fig. 1). Schottky barrier diodes (D1-D3) shift the output voltage to allow compatibility between input and output voltages. The same Schottky barrier diodes also function as "logic diodes" that enable the outputs of various gates to be wired in AND configurations, as in I^2L. The resistor R_b is chosen to minimize the base current, while the bypass capacitor C_b maintains fast transient response. Together, these elements alleviate the problems associated with HBT saturation. As one might observe from Fig. 1, the proposed HBT/RTD logic family is similar to I^2L logic. This similarity allows HBT/RTD logic to implement the myriad of circuits already designed for I^2L.

Illustrated in Fig. 2 is the I-V curve of the RTD pull-up load superimposed on the I-V characteristic of the driver device (an HBT in series with a Schottky diode) for analyzing the logic levels. The stable intersections of the I-V curves are labeled A and B. Typical high and low logic levels are 1.75 and 0.98 V, respectively. By neglecting base currents, the intersection of the pull-up device curve with the driver device determines the collector current I_c. For high output voltage the HBT is off, and power dissipation is minimal. For low output voltage

the RTD is biased near the valley point, which constrains I_c and the power dissipation to a low (although nonzero) value.

The application of a high logic level on the input of the inverter causes the HBT to saturate. It is necessary to limit the current flow into the collector in this state. This limitation is accomplished by R_b, which suppresses the base current and charge storage in the base-collector junction. To minimize the static power dissipation in this state, the voltage drop across the RTD should correspond closely to the valley voltage. This can be arranged by proper choice of power-supply voltage V_{cc}. Temperature variations in the saturation voltage of the HBT and in the turn-on voltage of the Schottky diode cause relatively small excursions of the bias point around the preferred design point.

With V_{cc} adjusted for minimum static power dissipation, the logic swing of the HBT/RTD circuit is around 0.8 V. The turn-on voltage for the typical GaAs/AlGaAs HBT is approximately 1.3 V. Without the shift in voltage level due to the Schottky diode, an incompatibility exists between the input and output logic levels. With the Schottky diode, the output swing is between 1.75 and 0.98 V. Unlike the case for CMOS, the low output-logic level of the HBT/RTD inverter does not approach ground because of both the level-shift diode and the saturation voltage of the HBT. However, as shown later, the static power dissipation is still low compared to that of conventional I^2L inverters.

In order for the output to make a transition from the high to the low logic level, it is necessary that the transistor collector current momentarily exceed the peak current of the RTD. That is, the transistor base current must rise so that the operating collector current curve is the curve labeled C in Fig. 2 (or a higher curve). In order for the output to make a transition from the low to the high logic level, it is necessary that the transistor collector current momentarily be lower than the valley current of the RTD. For this to occur, the transistor base current must be just lower than the base current corresponding to curve D in Fig. 2. This assumes that the base of the HBT in the next stage draws negligible current due to R_b. Our simulations show, in addition, that proper operation of the circuit depends on having adequately low values of the HBT parasitic emitter and collector resistances R_e and R_c, so that the peak HBT collector current achievable during an input low-to-high transition exceeds the peak RTD current.

The inverter static transfer characteristic is shown in Fig. 3. The nonlinear I-V curve of the RTD load causes a hysteresis in the transfer

characteristic. The vertical transitions (dashed lines in Fig. 3) represent unstable regions and correspond to abrupt changes in the stable operating points of the HBT/RTD combination. The noise margins NM^0 and NM^1 are defined in Fig. 3 as the separations between the stable logic voltages and the nearest respective points having unity gain. The presence of hysteresis can actually enhance noise margins, increasing the circuit tolerance to noise pulses [2]. The magnitude of the hysteresis of HBT/RTD inverters is relatively small compared to FET/RTD inverters because of the larger transconductance of the HBTs.

During transient operation, the rate at which a logic gate can charge and discharge the output node capacitance determines the switching speed. In pulling the output from high to low, the high transconductance of the HBT enables it to swiftly sink the current from both the load RTD and the next stage. In pulling the output from low to high, on the other hand, the current is provided by the RTD. If the peak-to-valley current ratio (PVCR) (point E/point B, Fig. 2) is high, then the switching time from output low to output high is limited primarily by the valley point, and the switching time decreases rapidly with the magnitude of the valley current. Since the static power increases with valley current, a trade-off exists between these two factors. Thus, the PVCR plays an instrumental role in both the switching time and the power consumption. A high value of PVCR of 10 is assumed in the present work. Experimental values of PVCR in excess of 10 have been reported for RTDs, even in conjunction with high current density [6].

In order that R_b not limit the switching speed of the circuit, it is bypassed with a capacitor. The value of the capacitor is chosen to be large enough to provide the base charge required to switch the HBT while small enough to minimize excess charge storage in the saturation region. With the high f_T and small size of present HBTs, the value of C_b need not be very large. A value of 0.25 pF is chosen for our simulations.

III. Device Modeling

Modeling using the SPICE 3D2 circuit simulation program has been carried out to determine the performance of the proposed logic family. For meaningful circuit simulations, accurate models for the RTDs and HBTs were required.

SPICE models of RTDs have been introduced and have been used to simulate integrated circuits. All of the models have been based on simplified representations of the I-V curve, such as piecewise linear [7] or polynomial fits. The present simulations employ a more physical representation, taking advantage of the option in SPICE 3D for transcendental forms for voltage-controlled current sources. The RTD I-V curve has the form

$$I = f\left\{c_1 V\left[\tan^{-1}(c_2 V + c_3) - \tan^{-1}(c_2 V + c_4)\right] + c_5 V^m + c_6 V^n\right\} \quad , \qquad (1)$$

where f is a scale factor used to vary the RTD area. Constants c_1 through c_4 are determined by the peak voltage, the peak current, and the turn-on voltage. Constants c_5 and c_6 are determined by the valley voltage and current. The exponents m and n (n > m) are chosen to get a satisfactory fit to the I-V curve beyond the valley point. The two $\tan^{-1}$ terms arise from the degenerate stationary-state tunneling theory of the I-V curve, with a Lorentzian form used for the transmission probability [8]. The two polynomial terms account for the excess (*i.e.*, inelastic) current, which is the predominant current component at the valley point and beyond.

The parameters in the SPICE 3D RTD model are determined from the experimental room temperature I-V curve of an RTD having an area of 14 μm^2, a 5.5-nm-thick $In_{0.53}Ga_{0.47}As$ quantum well, 1.5-nm-thick AlAs barriers, and $In_{0.53}Ga_{0.47}As$ cladding layers, all grown lattice matched on an InP substrate. The experimental curve in Fig. 4 has a peak current density of 6×10^4 A cm^{-2} and a PVCR of 10. The SPICE model I-V curve has $c_1 = 0.0021$ A V^{-1}, $c_2 = 24.5$ V^{-1}, $c_3 = -5.0$, $c_4 = -15.0$, $c_5 = 0.000035$ A V^{-1}, $c_6 = 0.000056$ A V^{-5}, $m = 1$, and $n = 5$. The model I-V curve overestimates the current somewhat at voltages just below the peak, and deviates significantly at voltages well beyond the valley, but it agrees very well at the crucial peak and valley points and near zero bias. To account for displacement current in the RTD, the SPICE model also incorporates a reverse-biased junction diode in parallel with the current source. The capacitance is chosen as $C_{jo} = 2.5$ fF μm^{-2} at zero bias and has a voltage dependence of $(1+V/V_{bi})^{-1/2}$, where $V_{bi} = 0.1$ V. This form of capacitance is suitable for RTDs having a lightly doped spacer layer on the anode side of the double-barrier structure that is much wider than the double-barrier structure itself. The effect of the double-barrier traversal time, which can be represented

by a quantum-well inductance [9], is neglected in the present simulations since in a device with 1.5-nm-thick barriers it is thought to be important only at much shorter time scales (< 1 ps).

SPICE models for HBTs are relatively well established. In this work, the model corresponds to HBTs in routine fabrication at Rockwell International Science Center. The fabricated HBTs have an emitter mesa measuring 1.4 x 3 μm, an f_T of nearly 60 GHz, and a maximum oscillation frequency f_{max} of 70 GHz [10]. The Schottky diodes in this work were modeled using the SPICE diode model with the zero-bias junction capacitance set to 12 fF. The other model parameters were chosen to be consistent with a 2x4-μm Schottky contact on GaAs.

IV. HBT/RTD Simulation Results

A variety of circuits based on the proposed inverter have been simulated, including other logic gates, "delay chains" based on sequences of inverters with varying fan-out, flip-flops, and flip-flop-based static frequency dividers. For all circuits the input and output are buffered by at least one inverter, and the last inverter was terminated by an RTD in order to maintain the node voltages that would exist in a very large gate array.

A six-inverter chain circuit having one Schottky diode per gate was used to determine the transient characteristics of this logic family. The input voltage waveform to the chain consists of a periodic pulse that approximates the typical HBT/RTD switching characteristics. The slew rate and amplitude were chosen in a self-consistent manner. The third gate of the inverter chain was used to determine the propagation delay time (measured between the 50% points on the input and output waveform) and the static power dissipation. The results of the simulations are listed in Table I. Fig. 5 illustrates the typical switching voltage and current characteristics. The output current waveform shows significant peaking during the switching transients, while the steady state values of current are small, as desired for low static power dissipation.

In order to quantify the power dissipation, both dynamic and static power components must be accounted for. The total power dissipation P_{tot} can be expressed in the form

$$P_{tot} = P_{ave} + E_o f \ , \qquad (2)$$

where P_{ave} is the static power dissipation averaged over the low and high states, E_o is the dynamic switching energy, and f is the frequency of switching of the gate. Values of P_{ave} were determined from the transient analysis by using an input waveform with a large period. The value of E_o was determined by integrating the current passing through the gate from the power supply during transient analysis. This is accomplished by measuring the voltage across a dummy capacitor that is coupled to the gate by a current-controlled current source.

To gain further insight into the operation of the HBT/RTD inverter, the effect of varying a number of relevant device parameters was investigated. These parameters included a parasitic load capacitance C_L and the external resistor R_b as well as the areas of the HBT, the Schottky diode, and the RTD. In Table I, a scale factor of 1 for the HBT/diode combination denotes that the areas of the standard HBT and Schottky-diode designs described in Sec. III were used. The RTD scale factor is normalized to the area of the RTD design described in Sec. III. Table I contains the resulting values of delay time $\langle t_d \rangle$, speed-power product $P_{ave} * \langle t_d \rangle$, P_{ave}, and E_o for the various circuits. The quantity $\langle t_d \rangle$ is obtained by averaging the output low-to-high propagation delay time with the output high-to-low propagation delay time. The lowest delay time in Table I is 39 ps, but the P_{ave} in this case is 0.4 mW. If power considerations are more important, the HBT/RTD logic can be designed to dissipate 0.09 mW with an average delay of 148 ps by using an RTD scale factor of 0.1 and an R_b of 10 kΩ. A comparison between the output-voltage rise and fall times reveals that the rise time is significantly larger than the fall time and is limited by the current supplied to the node capacitance by the RTD. Further studies also reveal that the intrinsic base-collector capacitance C_{bc} of the HBT limits the switching time. Reductions in C_{bc} will significantly improve the switching speed of the inverter.

For comparative purposes, an I^2L logic inverter chain with the same HBT transistor was simulated. The logic swing was set to be around 0.4 V [11]. A 2-kΩ base pull-up resistor yields a static power dissipation of 0.9 mW, a 45-fJ static power-delay product, and a 54-ps time delay. This power-delay product is 3.5 times larger than the best result of 15 fJ shown in Table I. This is a good measure of the improvement offered by the HBT/RTD logic over existing HBT I^2L logic.

Additional simulated circuits verified the wired AND function of the HBT/RTD logic family. Simulations of circuits designed to evaluate the fan-out characteristics of the gate uncovered several important device design criteria. The current supplied by the HBT must exceed the fan-out number times the RTD peak current. This requires adequately high input base current, as well as controlled transistor saturation voltage, which depends on having uniform and low R_e and R_c values in the transistors involved. If R_e and R_c are too high, the circuit will have reduced logic swing and high static power dissipation. However, the logic functions will still be correct in spite of the reduced logic levels. One possible approach for reducing R_e and R_c for increased fan-out is to scale the area of the HBT and the Schottky diode. The penalty of this approach is that it increases the overall capacitance.

Frequency dividers are often used to determine the high-speed characteristics of a logic family. The frequency divider requires a fan-out of three for certain gates in the circuit. A divide-by-two frequency divider consisting of six NAND gates was simulated. The maximum frequency of operation for this circuit is the inverse of four times the average time delay of a single gate. In the first simulation, the same optimized HBTs (reduced R_e and R_c without area scaling) are used throughout the circuit. A maximum operating frequency of 5.25 GHz with an average P_{tot} of 1.4 mW per gate was calculated. For the second simulation, area scaling is used to reduce R_e and R_c. Since fan-outs of one, two, and three are used in the frequency divider circuit, it is possible to optimize performance by increasing the device area selectively. In a design with scaling commensurate with actual fan-out, an f_{max} of 2.4 GHz with a P_{tot} of 1.1 mW (0.4-mW static power plus 0.7-mW dynamic power) per gate is demonstrated. Fig. 6 contains a plot of the frequency divider operating at 2.375 GHz. The values of power and speed for these simulated dividers compare favorably with those for other HBT-based technologies. For example, we have simulated a divide-by-two frequency divider comprising standard HBT I^2L logic and have found the total power to be roughly twice that of an equivalent HBT/RTD divider operating at the same frequency.

V. Prospects for Realization

GaAs/AlGaAs HBT-based integrated circuits made using molecular beam epitaxy (MBE) or organometallic vapor phase epitaxy have been widely

produced in research laboratories, and pilot production has recently begun at several companies. Also, RTDs made from several materials systems have been demonstrated using MBE growth. In both cases, the key device dimensions are defined during epitaxy rather than by post-growth lateral patterning. In principal, the layer structures for both devices could be defined monolithically by a single MBE growth with the RTD epilayers lying on top of the HBT epilayers. This is particularly easy because the RTD layers are very thin and can be readily removed from the wafer where not needed. However, the highest-performance RTDs (*e.g.*, with high PVCR at room temperature and high peak current density) have been fabricated with materials systems other than GaAs/AlGaAs and thus will not be lattice matched to GaAs substrates. The requirements for the present circuits can be met by RTDs made from InGaAs/AlAs (which has been assumed as the basis for the simulations) or InAs/GaSb/AlSb. It is noteworthy that Brown *et al.* have demonstrated high-speed operation of InAs/AlSb RTDs deposited on GaAs substrates, despite the presence of misfit dislocations caused by the large lattice mismatch [4]. The ability to produce useful devices without lattice matching suggests that it may also be possible to combine III-V RTDs with Si bipolar transistors to form a logic family with even lower power dissipation but lower speed than the one described here.

VI. Summary

An HBT/RTD logic family has been proposed that, according to SPICE computer simulations, offers high-speed switching with low static power dissipation. Although not the fastest logic family, it offers considerable reduction in static power for applications requiring high-speed digital logic. Furthermore, it should be possible to combine both HBT/RTD logic and HBT-based ECL logic in the same integrated circuit through appropriate matching circuitry. The HBT/RTD logic family would take care of the slower functions and offer reduced power dissipation and high packing density, while the ECL-logic-based circuits would be employed in the core high-speed circuits.

References

[1] M. F. Chang and P. M. Asbeck, "III-V heterojunction bipolar transistors for high-speed applications," *Int. J. High Speed Electron.*, vol. 1, pp. 245-1990.

[2] K. Lehovec, "GaAs enhancement mode FET-tunnel diode ultra-fast low power inverter and memory cell," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 787-800, Oct. 1979.

[3] K. L. Lear, K. Yoh, and J. S. Harris, Jr., "Monolithic integration of GaAs/AlGaAs resonant tunnel diode load and GaAs enhancement-mode MESFET drivers for tunnel diode FET logic gates," in *Gallium Arsenide and Related Compounds 1988.* IOP Publishing: Bristol, England, 1989, pp. 593-598.

[4] E. R. Brown, J. R. Söderström, C. D. Parker, L. J. Mahoney, K. M. Molvar, and T. C. McGill, "Oscillations up to 712 GHz in InAs/AlSb resonant tunneling diodes," *Appl. Phys Lett.*, vol. 58, pp. 2291-2293, 20 May 1991.

[5] T. P. E. Broekaert and C. G. Fonstad, "Extremely high current density, low peak voltage, pseudomorphic $In_{0.53}Ga_{0.47}As$/AlAs/InAs resonant tunneling diodes," in *Int. Electron Devices Mtg. Tech. Dig.*, 1989, pp. 559-562.

[6] J. R. Söderström, D. H. Chow, and T. C. McGill, "InAs/AlSb double-barrier structure with large peak-to-valley current ratio: A candidate for high-frequency microwave devices," *IEEE Electron Device Lett.*, vol. 11, pp. 27-29, Jan. 1990.

[7] T.-H. Kuo, H. C. Lin, U. Anandakrishnan, R. C. Potter, and D. Shupe, "Large-signal resonant tunneling diode model for SPICE3 simulation," in *Int. Electron Devices Mtg. Tech. Dig.*, 1989, pp. 567-570.

[8] D. D. Coon and H. C. Liu, "Frequency limit of double barrier resonant tunneling oscillators," *Appl. Phys. Lett.*, vol. 49, pp. 94-96, 14 July 1986.

[9] E. R. Brown, C. D. Parker, and T. C. L. G. Sollner, "Effect of quasibound-state lifetime on the oscillation power of resonant tunneling diodes," *Appl. Phys. Lett.*, vol. 54, pp. 934-936, 6 March 1989.

[10] K. D. Pedrotti, N. H. Sheng, et al., "Monolithic ultrahigh-speed GaAs HBT optical integrated receivers," in *IEEE Gallium Arsenide Integrated Circuit Symp. Tech. Dig.*, 1991, pp..

[11] H.-T. Yuan, H.-D. Shih, J. Delaney, and C. Fuller, "The development of heterojunction integrated injection logic," *IEEE Trans. Electron Devices*, vol. 36, pp. 2083-2092, Oct. 1989.

Figure Captions

Fig. 1. Schematic of HBT/RTD inverter capable of driving a fan-out of three.

Fig. 2. Inverter characteristic consisting of the HBT driver curves superimposed on the curve for the RTD pull-up load.

Fig. 3. Voltage transfer characteristic of the HBT/RTD inverter showing hysteresis. The dashed segments represent switching through the NDR region of the RTD and are not stable at dc.

Fig. 4. Comparison of experiment (solid and dashed) and SPICE model (dotted) for the I-V curve of a high-current-density RTD made from the $In_{0.53}Ga_{0.47}As$/AlAs material system. The dashed portion of the experimental I-V curve represents discontinuous switching into the middle portion of the NDR region (also shown solid) in which the RTD is oscillating in the measurement circuit.

Fig. 5. Simulated voltage and current transient results of HBT/RTD inverter.

Fig. 6. Simulated results of a divide-by-two frequency divider at 2.375 GHz (scaled by fan-out). This frequency is close to the maximum operation frequency $f_{max} = 1/(4\ t_d)$.

Table I
Numerical results of SPICE 3D2 simulations of the HBT/RTD inverter*

HBT/ Diode Scale Factor	RTD Scale Factor	R_b (kΩ)	C_L (fF)	I_{ave} (mA)	P_{ave} (mW)	$\langle t_d \rangle$ (ps)	$P_{ave} * \langle t_d \rangle$ (fJ)	E_o (fJ)
3	0.4	2	0	0.22	0.42	99.1	41.2	202
3	0.4	2	100	0.22	0.42	154.5	64.2	285
3	0.4	4	0	0.17	0.32	102.7	33.0	177
3	0.4	4	100	0.17	0.32	148.0	47.6	253
3	0.2	2	0	0.16	0.31	203.1	62.0	139
3	0.2	2	100	0.16	0.31	323.8	99.2	203
3	0.2	4	0	0.11	0.21	191.8	40.3	177
3	0.2	4	100	0.11	0.21	307.2	65.4	215
2	0.4	2	0	0.21	0.41	78.7	32.1	152
2	0.4	2	100	0.21	0.41	127.9	52.1	228
2	0.2	2	0	0.16	0.31	144.9	45.5	120
2	0.2	2	100	0.16	0.30	261.2	78.4	193
1	0.4	2	0	0.21	0.40	38.6	15.4	165
1	0.4	2	100	0.21	0.40	88.7	35.5	253
1	0.2	2	0	0.15	0.29	78.9	22.5	127
1	0.2	2	100	0.15	0.29	195.6	56.2	165
1	0.1	10	0	0.05	0.09	148.0	13.9	82

*Inverter chain used with V_{cc} = 1.9 V and C_b = 0.25 pF; typical magnitude of logic swing is 0.8 V.

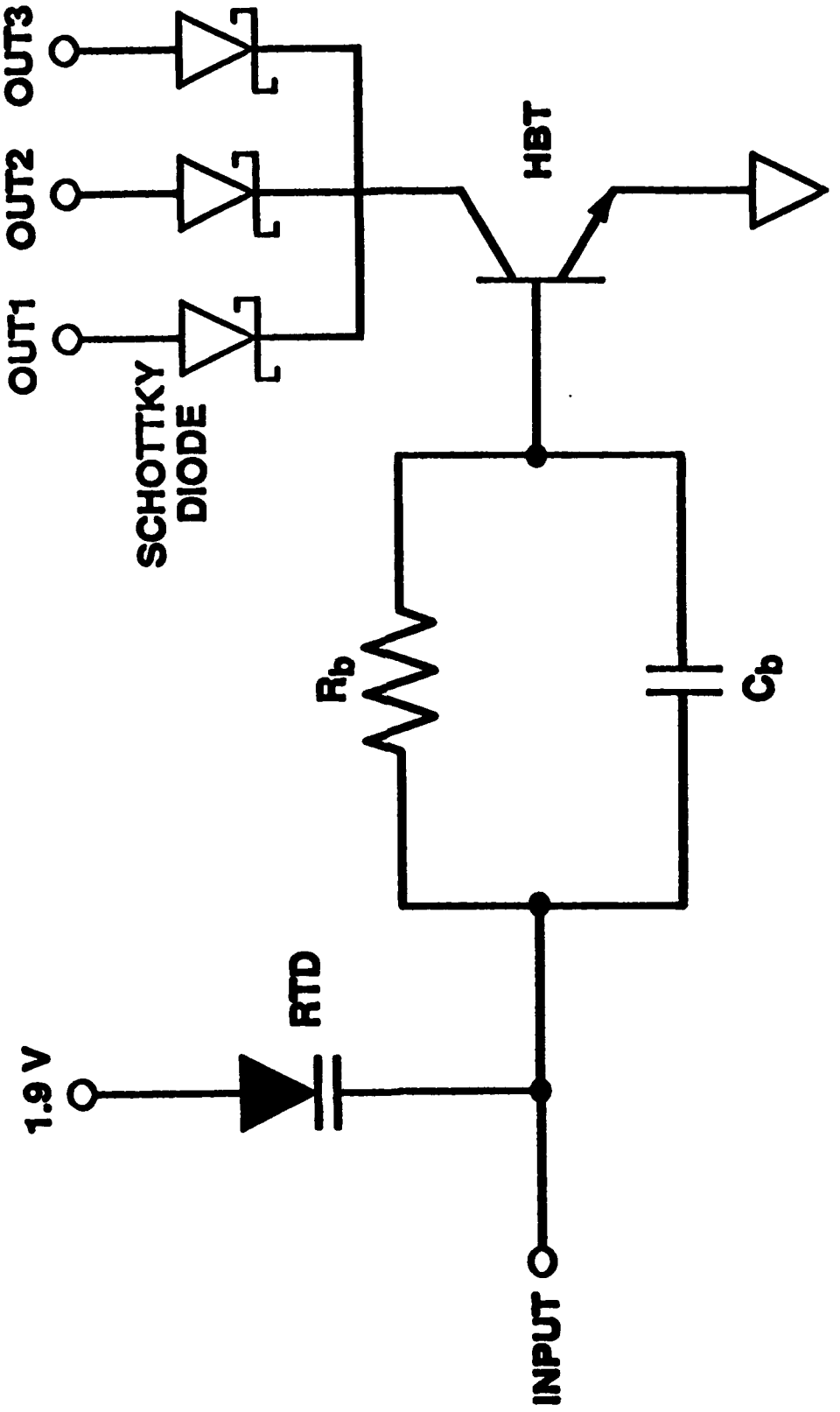

FIGURE 1

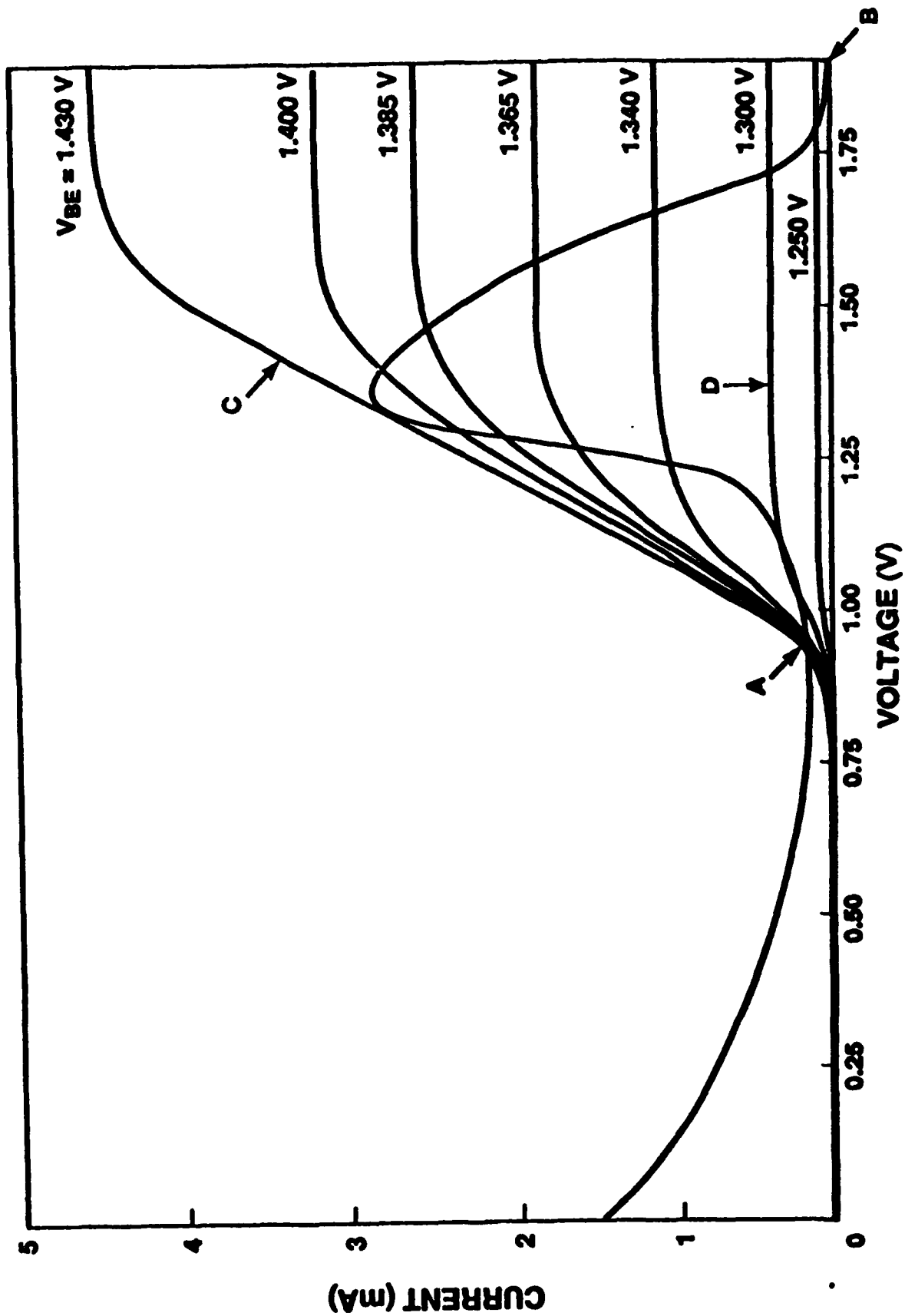
V_{BE} = 1.430 V
1.400 V
1.385 V
1.365 V
1.340 V
1.300 V
1.250 V
A
B
C
D
CURRENT (mA)
VOLTAGE (V)
0
1
2
3
4
5
0.25
0.50
0.75
1.00
1.25
1.50
1.75

FIGURE 2

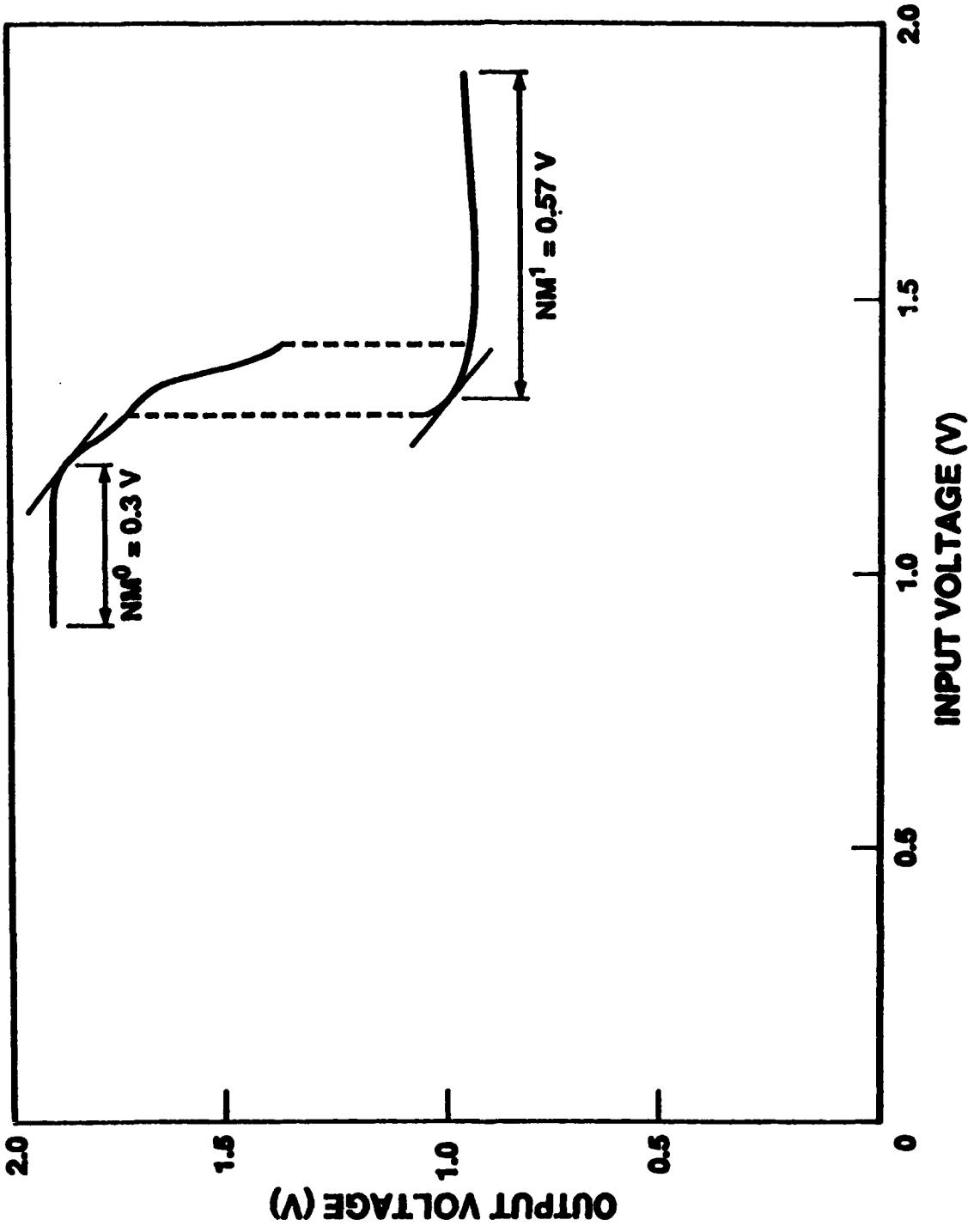
OUTPUT VOLTAGE (V)
2.0
1.5
1.0
0.5
0
0.5
1.0
1.5
2.0
INPUT VOLTAGE (V)
NM^0 = 0.3 V
NM^1 = 0.57 V

FIGURE 3

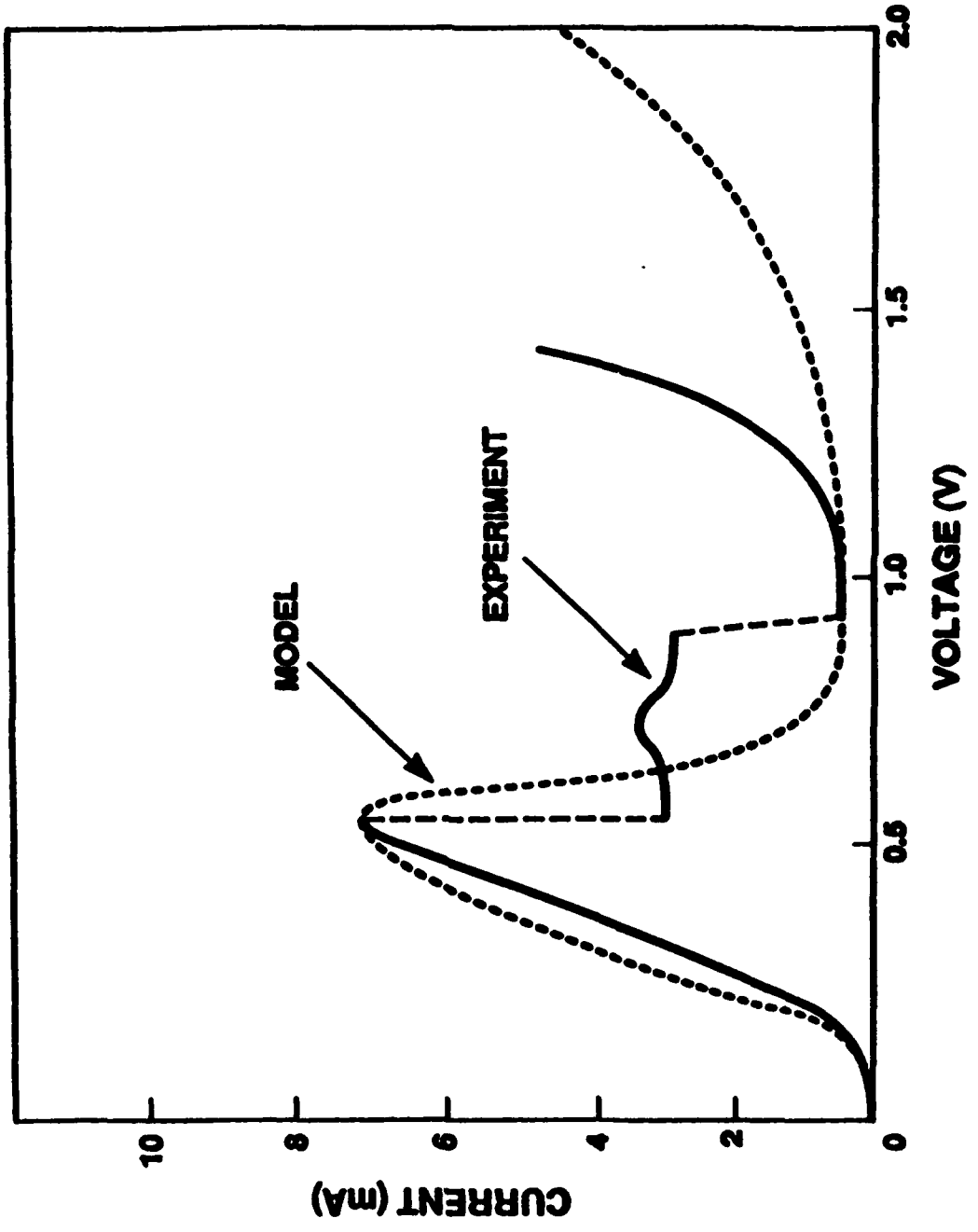

FIGURE 4

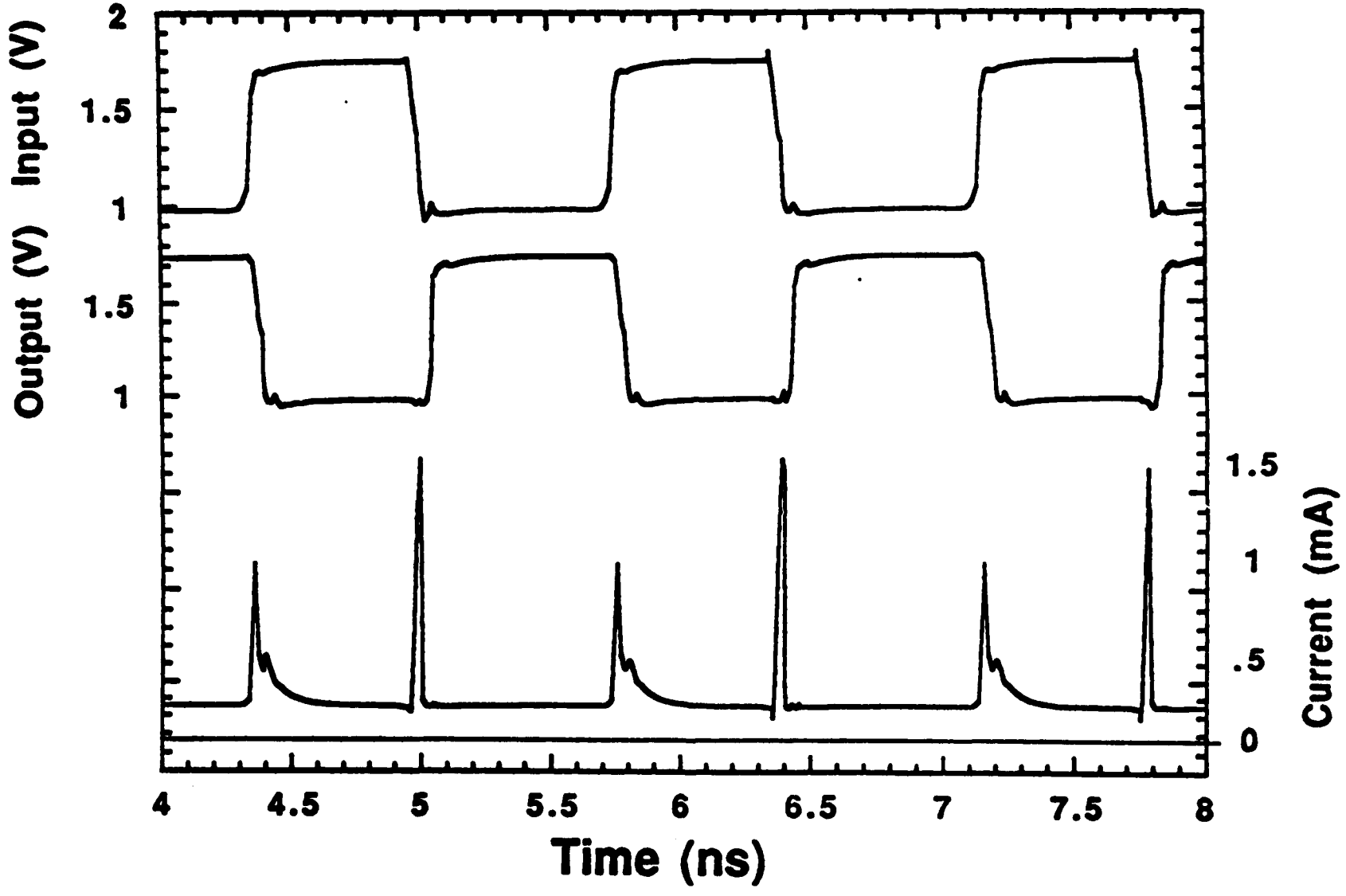

FIGURE 5

FIG. 5

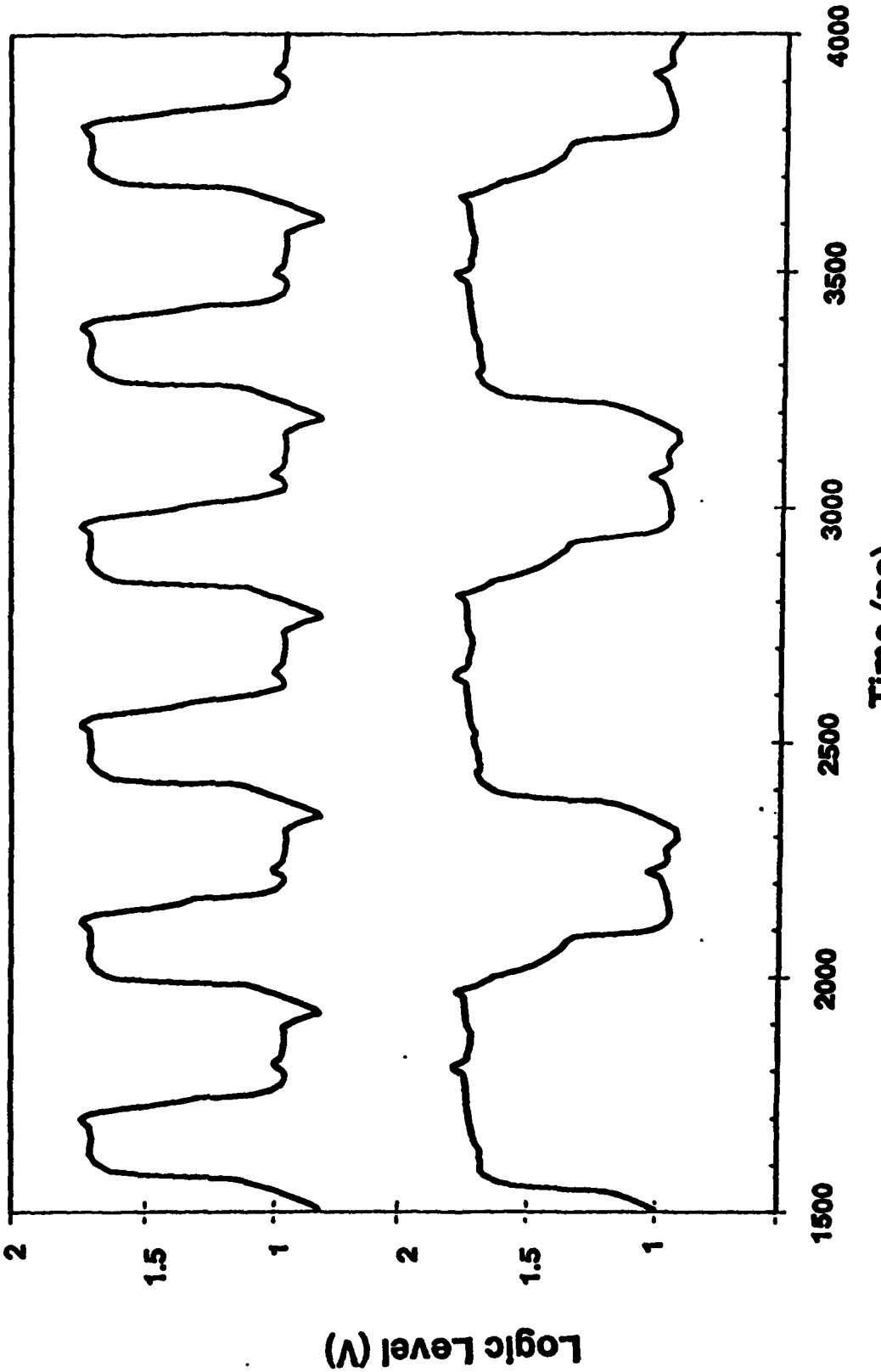

FIG. 6

FIGURE 6

APPENDIX R

High-Speed Resonant-Tunneling Diodes†

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High-speed resonant-tunneling diodes

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1. Introduction

1.1. Overview

Tunneling is a strictly quantum-mechanical process that entails the passage of a particle from one classically allowed region to another through a classically forbidden, or tunneling, region. Resonant tunneling is distinguished by the presence within the clasically forbidden region of quasibound, or metastable, states of the tunneling particle. In solid-state resonant tunneling, the quasibound states are usually associated with impurities in the tunneling region or with narrow classically allowed regions (i.e., quantum wells) contained within semiconductor heterostructures. The present chapter is concerned with resonant tunneling in the double-barrier heterostructure, which is composed of two layers of a semiconductor material, such as AlAs, embedded in another semiconductor having a smaller bandgap, such as GaAs.

Double-barrier resonant tunneling has attracted considerable attention because it is one of the few solid-state transport phenomena that can provide a fast negative differential resistance (NDR) at room temperature. The NDR region has been used as the basis for high-frequency oscillations and high-speed switching. For example, double-barrier resonant-tunneling diodes (DBRTDs) made from the InAs/AlSb material system have oscillated up to to 712 GHz, and DBRTDs made from the GaAs/AlAs system have switched from the peak-current point to the valley-current region in a time near 2 ps. Much of the interest in resonant-tunneling devices stems from the fact that these results are among the highest oscillation frequencies and the lowest switching times reported to date for electronic devices. This has led to the development of DBRTD oscillators for the terahertz region and DBRTD switches for signal processing and digital applications.

The outline of this chapter is as follows. Section 2 reviews the fundamental physical characteristics of resonant tunneling. Section 3 deals with the various resonant-tunneling material systems and the dc I-V characteristics obtained from DBRTDs in these systems. These include III-V material systems having type-I band offsets, such as the common GaAs/AlAs (GaAs quantum well and AlAs barriers); those having type-II offset, such as InAs/AlSb; pseudomorphic systems, such as $In_xGa_{1-x}As/AlAs$; and column-IV systems, such as Si_xGe_{1-x}/Si. Section 4 covers some of the key issues in the device physics such as the current density, charge storage in the quantum well, current fluctuations, and excess current mechanisms. Section 5 analyzes the important time-delay mechanisms operative in high-speed diodes, including the fundamental RC time, resonant-tunneling traversal time, and semiclassical transit time across the depletion region. In Sec. 6, these time delays are combined to yield the two most important theoretical measures of device performance: the maximum oscillation frequency f_{max} and the switching risetime t_R. Section 7 summarizes some of the experimental methods, both electronic and optoelectronic, that have been employed to characterize the speed of the DBRTD. Among these methods are oscillator-frequency measurement and switching-time measurement by electrooptic sampling. The last section surveys some promising analog and digital applications of DBRTDs. Each of the applications utilizes the DBRTD as an independent device. The chapter does not address the integration of double-barrier structures into transistors, such as the resonant-tunneling bipolar transistor,[1] the resonant-tunneling hot electron transistor,[2] or the quantum-well resonant-tunneling transistor.[3]

1.2. Historical background

In a sense the double-barrier structure represented a retreat from more complicated multiple-barrier, or superlattice, structures that initially promised new electronic functions, such as Bloch oscillations, but did not perform as expected.[4,5] The first realization of the double-barrier structure occurred in 1974 with the observation of NDR in a GaAs/AlGaAs DBRTD at low temperatures.[6] Following this pioneering result, most of the work in heterostructures centered around the development of molecular beam epitaxy (MBE), since it was clear that the quality of the materials in these structures would have to be improved in order to observe the NDR or any other quantum-transport effect at room temperature. The primary structures studied during this time were single- or double-heterojunction quantum wells rather than resonant-tunneling structures. The subsequent improvements in materials growth led to the advent of two very important devices: the heterojunction diode laser and the

heterostructure field-effect transistor. However, the resonant-tunneling structure went relatively unstudied until 1983. At that time, a cooled GaAs/AlGaAs double-barrier structure was used to rectify 2.5-THz laser radiation.[7] This pivotal experiment demonstrated that resonant tunneling was a very fast process, and it spurred the development of improved materials. Within three years, several groups had achieved a large room-temperature NDR effect, first in the $GaAs/Al_{0.25}Ga_{0.75}As$ material system,[8] and shortly thereafter in the GaAs/AlAs system.[9, 10]

In the ensuing years, the research has branched in different directions, with much of the effort aimed at developing new material systems or at understanding the dynamic characteristics of resonant tunneling. A key advance in material systems was the development of indium-bearing heterostructures, as discussed in Secs. 3.3 and 3.4. The research on the dynamic characteristics has centered around a set of oscillation and switching experiments, described in Sec. 7, and around the quantum-transport theory, described in Chapter 9.

2. Physical concepts in resonant tunneling

2.1. Resonant-tunneling characteristics

The fundamental requirement for resonant tunneling in any structure is spatial quantization. This entails the formation of quasibound states whose energy can be found by solving the time-independent Schrödinger equation for the structure. As an example, the lowest three quasibound states of a double-barrier structure are depicted in Fig. 1. Each state is characterized by a quasibound energy E_n and a lifetime τ_n. These quantities are related to the tunneling process in that E_n is the peak of the transmission probability T*T vs longitudinal energy E_Z (the energy along the direction perpendicular to the barrier layers), $\tau_n \approx \hbar/\Gamma_n$ where Γ_n is the full width at half-maximum of the nth peak of the T*T curve. The requirement for spatial quantization is $E_n \gtrsim \hbar/\tau_s$, where τ_s is the inelastic scattering time for an electron occupying the nth state. In the limit of an infinitely deep quantum well where $E_n = (\hbar k_n)^2/2m^* = (n\pi\hbar)^2/2m^*L_W^2$, this inequality becomes $\tau_s \gtrsim 2L_W/n\pi v_g \equiv 2t_w/n\pi$, where L_W is the quantum-well width, $v_g = \hbar k_n/m^*$ is the group velocity, m^* is the effective mass, and t_w is the semiclassical quantum-well traversal time. That is, spatial quantization requires that the electron traverse the quantum well at least once without scattering.

Resonant tunneling is also characterized by the relative magnitudes of τ_n and τ_s. If $\tau_n < \tau_s$, the resonant tunneling through the nth state is said to be coherent, since under this condition the electron does not scatter during the process and thus the phase of the wavefunction at each point in space is continuous in time. If $\tau_n \gg \tau_s$, the resonant tunneling is said to be sequential. In this case, the wavefunction is partially randomized by scattering events that occur in or near the double-barrier structure. Thus, resonant tunneling can be neatly classified by the three characteristic times, τ_n, t_w, and τ_s.[11, 12] Coherent resonant tunneling satisfies $\tau_n < \tau_s > t_w$, and sequential resonant tunneling satisfies $\tau_n > \tau_s > t_w$.

2.2. Transmission probability

Coherent and sequential resonant tunneling can be analyzed within the stationary-state formalism of quantum mechanics. One can represent a particle incident on the double-barrier structure as a plane wave having a wavevector $k_z = (2m^*E_Z)^{1/2}/\hbar$ along the direction (z) perpendicular to the plane of the barriers. The interaction of the particle with the double-barrier structure is described entirely by the transmission probability $T^*T(E_Z)$. In the situation where the energy in the lateral plane is conserved throughout the resonant-tunneling process, only those particles having E_Z nearly equal to E_n can traverse the structure with high probability. For these particles the transmission probability is well approximated by the following Lorentzian form[12, 13]

$$T^*T = \frac{\Gamma_n^L \Gamma_n^R}{(E_Z - E_n)^2 + \Gamma_n^2/4}, \tag{2.1}$$

where Γ_n^L and Γ_n^R are the partial-width, or transparency, factors for the left and right barriers, respectively. In the presence of certain types of scattering, this expression can be generalized to the form

$$T^*T = \left[\frac{\Gamma_n^L \Gamma_n^R}{\Gamma_n^L + \Gamma_n^R}\right] \frac{\Gamma_T}{(E_Z - E_n)^2 + \Gamma_T^2/4}, \tag{2.2}$$

where $\Gamma_T = \Gamma_n^L + \Gamma_n^R + \Gamma_S$, and Γ_S is a scattering parameter. In this case, T^*T represents the probability for an electron to enter the structure at E_Z and to exit at any energy. The scattering causes the energy of the particle to be uncertain after entering the structure. However, the integrated probability, $\int_0^\infty T^*T(E_Z)dE_Z$, is independent of Γ_S. This is analogous to the sum rule

for oscillator strengths in the quantum theory of radiative transitions. Analytic expressions have been derived for the first-quasibound-state partial widths, Γ_1^R and Γ_1^L, under the following conditions:[13] (1) the potential energy is everywhere flat except for the step discontinuities at the heterojunctions, and (2) the dispersion relations for the particle are parabolic in all regions, including the barriers.

In many practical situations, such as double-barrier structures under large bias, the analytic expressions for T*T are inadequate and one must rely on numerical solutions. Under the condition of lateral momentum conservation, one solves the longitudinal effective-mass Schrödinger equation,

$$E(P_z/\hbar)F(z) + V(z)F(z) = EF(z) , \tag{2.3}$$

where P_z is the longitudinal momentum operator, $E(P_z/\hbar)$ is the energy-dispersion functional, $V(z)$ is the electron potential energy including both compositional and electrostatic contributions, $F(z)$ is the envelope function, and E is the energy eigenvalue. Near the conduction-band edge of any semiconductor, the dispersion relation along a given direction of momentum space is parabolic, so that $E(P_z/\hbar) = P_z^2/2m^*$ where m^* is the local effective mass. In this case, Eq. (2.3) is a second-order linear differential equation, called the effective-mass equation, that is solved uniquely by applying the boundary conditions of the continuity of F and the continuity of the electron flux $(1/m^*)dF/dz$ at each heterojunction in the structure.[14] T*T through the structure is obtained by connecting the solutions across the heterojunctions using the transfer-matrix technique.[15]

If the particle energy is not near a band edge or is near the edge of degenerate bands, then the effective-mass equation does not apply straightforwardly. The common approach in this case is to employ the so-called envelope-function formalism.[16] The tunneling wavefunction is represented as an admixture of conduction- and valence-band envelope functions, and the dispersion relations are everywhere formulated within the context of multiple bands. For example, two-band models (Γ electron and light hole) have been successful in describing energy levels in type-II band structures (defined in Sec. 4.1).[16] Two-band models have also been applied in tunneling problems.[17] A useful simplification of this formalism for electron tunneling results from assuming that the wavevectors and effective masses are everywhere determined by non parabolic dispersion, but that the wavefunction has only a conduction-band component. The barrier dispersion is determined by connecting the conduction band to the light-hole band.[18] This results in an analytic expression of E vs K where K is the attenuation

coefficient, or the modulus, of the imaginary wavevector. Associated with this expression is a branch point where the K reaches a maximum value in the bandgap. In the classically allowed regions, it often suffices to model the electron dispersion relation by the expression obtained from two-band $\mathbf{k}\cdot\mathbf{p}$ perturbation theory,[19] $E(k) = (\hbar k)^2(1 - Ak^2)/2m^*$, where A is a constant that depends on the band structure.

Some questions arise regarding the validity of the effective-mass equation, or envelope-function approximation, in problems of heterobarrier tunneling. It is often asked, for example, how effectively a heterojunction couples the envelope function of an incident electron to components of the wavefunction in the barrier at different points in the Brillouin zone. One study of this issue has shown that when the barriers are sufficiently thin, the coupling is weak.[20] This situation applies to at least the lower end of the range of barrier thicknesses used in high-speed DBRTDs, which is approximately 1.0 to 5.0 nm. Thus, one can assume that the Brillouin-zone symmetry of the envelope function is preserved upon tunneling through thin barriers. Another question is whether or not it is valid to neglect the cell-periodic part of the wavefunction in the presence of the abrupt change of potential at a heterojunction. The answer is that the envelope function alone is adequate if it varies slowly over a unit cell.[21] This is generally true in semiconductor heterostructures, where the electron energy usually lies within 1 eV or so of the closest band edge and thus the de Broglie wavelength (i.e., the inverse crystal wavevector) is much larger than a unit cell.

2.3. Electrical current and NDR

The electrical current through the first quasibound state of a double-barrier structure is understood from the diagram given in Fig. 1. As the bias voltage is increased from zero, the quasibound level in the quantum well drops relative to the band edge on the cathode side. When the quasibound level approaches alignment with the quasi-Fermi level E_F^c, the electron current begins to increase rapidly. This rise can be explained in terms of an increase in the number of electrons in the cathode Fermi sphere that have $E_Z = E_1$.[22] The current eventually approaches a peak near the voltage that aligns the quasibound level with the conduction band edge in the neutral region on the cathode side. This is the bias voltage depicted in Fig. 1. At higher voltages there are no electrons with $E_Z = E_1$, so that the current decreases precipitously, and an NDR region occurs. This NDR region is the basis for all of the high-speed

oscillations and switching observed to date in DBRTDs.

The quality of a DBRTD is usually given by the peak current density J_P and the peak-to-valley current ratio, PVCR $\equiv I_P/I_V$, where I_P and I_V are the peak and valley currents, respectively, associated with the NDR region. A quantity of secondary importance is the peak-to-valley voltage ratio PVVR $\equiv V_V/V_P$, where V_V and V_P are the valley and peak voltages, respectively. For high-speed operation the current density should be relatively large ($J_P \gtrsim 1\times10^4$ A cm^{-2}) for the same reason as in any other high-speed electronic device: high current density is required for fast charging and discharging of the device and circuit capacitance. The relationship between current density and device speed is addressed in Sec. 6.

3. Resonant-tunneling materials

3.1. Material-system properties

It is a testament to the resonant-tunneling phenomenon that its trademark, the NDR region, has been observed at room temperature in several different material systems under a variety of crystalline conditions. In this section the constitutive properties of these material systems are summarized. One such property is the nature of the band alignment that occurs at a heterojunction between two materials of different bandgap. The well-known type-I alignment is one in which the bandgap of the narrower gap material is contained entirely within the bandgap of the other on an energy diagram. In type-II alignments, the bandgap of the narrower-gap material does not overlap the gap of the other material at all, and usually lies well below it. In type-II-staggered systems, the bandgap of the narrower-gap material intersects the wider gap partially, usually in the bottom portion of the wider bandgap. Thus the wider-gap material appears as a barrier to electrons but a well to holes. Independent of band alignment, each of the systems is designated by A/B, where A and B are the two constituent materials, and B is the material with the wider bandgap.

A second constitutive property is the crystalline state of the semiconductor layers in and around the double-barrier structure. In the most desirable case, all layers are lattice matched to the substrate material. One variation is to lattice match the quantum well and cladding layers but use lattice-mismatched barriers. If they are suitably thin, the lattice constant of the barriers will conform to that of the cladding layers, creating what is called a *pseudomorphic*

match. Another variation is to lattice match the barriers but mismatch all or part of the quantum well, or some part of the cladding layers. Again, if the mismatched layer is kept suitably thin, a pseudomorphic match results. Finally, one can mismatch all of the cladding material and, possibly, the barrier material with respect to the substrate, creating what is called a lattice-mismatched structure.

The diversity introduced by the different resonant-tunneling material systems is exemplified in Fig. 2, which shows the theoretical first-quasibound-state electron lifetime, $\tau_1 = \hbar/\Gamma_1$, as a function of barrier thickness for a fixed quantum-well thickness of 4.6 nm. Non-parabolic effects are included. All of the materials represented in Fig. 2 have type-I band offsets except InAs/AlSb, which is type II staggered. The important aspect of this plot is the broad range of lifetimes offered by different material systems at a given barrier thickness. This is a result of the strong dependence of the lifetime on the barrier attenuation coefficient, $\tau \approx \hbar/\Gamma_1 \propto \exp(KL_B)$, where L_B is the barrier thickness. The difference in K between the material systems arises from differences in the band gap or band alignment. For example, the smaller lifetimes of the GaAs/$Al_{0.42}Ga_{0.58}As$ structure compared to those of the GaAs/AlAs structure are caused primarily by the smaller bandgap, and hence barrier height, of the $Al_{0.42}Ga_{0.58}As$. In contrast, the much smaller lifetimes of the InAs/AlSb structure compared to the InAs/AlAs structure are caused by the type-II-staggered band alignment of InAs/AlSb, which is discussed in Sec. 3.4.

3.2. GaAs-based structures

The GaAs quantum well with $Al_xGa_{1-x}As$ barriers is the most venerable of the resonant-tunneling material systems, since it was the first system to yield an NDR effect at low temperatures[6] and at room temperature.[8] With $x \approx 0.4$, this system provides useful PVCR at values of J_P up to about 1×10^4 A cm^{-2}.[23] At higher values of J_P the PVCR is usually degraded by large thermionic current over the top of the barriers. Consequently, much better PVCR at high J_P is obtained from GaAs/AlAs structures. In GaAs/AlAs DBRTDs having J_P in the range from 10^4 to 10^5 A cm^{-2}, the best observed room-temperature PVCRs are about 4. Above this range, the PVCR degrades significantly. For example, PVCRs of 1.4 and 2.5 have been achieved in DBRTDs having J_P of 1.5×10^5 A cm^{-2},[24] and 1.3×10^5 A cm^{-2},[25] respectively. The best reported PVCR with $J_P \geq 10^5$ A cm^{-2} is 3.0 at $J_P \approx 1.2\times10^5$ A cm^{-2}.[26] This degradation is a drawback of GaAs/AlAs DBRTDs for high-speed applications, which usually

require $J_P \geq 10^5$ A cm^{-2}. The J-V curve of a high-J_P GaAs/AlAs DBRTD is shown in Fig. 3 in comparison with the curves for DBRTDs made from alternative material systems.

Several clever structures have been implemented to improve the PVCR of lattice-matched GaAs DBRTDs, at least at low current densities. For example, anode- and cathode-side AlAs barriers have been grown with $Al_xGa_{1-x}As$ layers just outside to form "chair barriers."[27] This has resulted in a DBRTD having a PVCR of 6.3 at room temperature.[28] Another structure contained an $In_xGa_{1-x}As$ layer either as a pre-well on the cathode side,[29] or in place of the GaAs quantum well.[30] An improved PVCR resulted in both cases.

3.3. $In_{0.53}Ga_{0.47}As$-based structures

The first DBRTDs fabricated in a system other than GaAs/$Al_xGa_{1-x}As$ were made from the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ system.[31] Both of these ternary alloys are lattice matched to InP substrates. The initial $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ DBRTDs yielded a PVCR of 2.3 at room temperature. This was subsequently improved to about 7 at room temperature and 40 at 77 K.[32,33] Shortly thereafter, superior results were obtained by replacing the $In_{0.52}Al_{0.48}As$ barriers with AlAs, which in the relaxed state has a 3.5% smaller lattice constant than $In_{0.53}Ga_{0.47}As$. In spite of this mismatch, the AlAs is pseudomorphic if the barrier thickness is limited to approximately 3.0 nm or less. The resulting DBRTDs yielded unprecedented PVCRs of 14 at room temperature.[34] Further improvement followed with the achievement of a PVCR of 30 at room temperature in a DBRTD having a thin InAs layer embedded in the $In_{0.53}Ga_{0.47}As$ quantum well.[35]

A second $In_{0.53}Ga_{0.47}As$-based system of interest contains GaAs rather than AlAs barriers. Because of its low electronic and light-hole effective masses, the GaAs barrier has a maximum attenuation coefficient in the gap that is about a factor-of-two smaller. However, the bandgap difference between the constituent materials is small, so that a low barrier height (~0.3 eV) is obtained. Consequently, the NDR region is observed only at 77 K or lower operating temperatures.[36]

A third $In_{0.53}Ga_{0.47}As$-based DBRTD has been fabricated with InP barriers by low-pressure metallorganic chemical vapor deposition (MOCVD).[37] The structure contained a 10-nm-thick $In_{0.53}Ga_{0.47}As$ quantum well and 10-nm-thick InP barriers. It displayed a 77-K PVCR of 1.2 for resonant tunneling through the first quasibound level and a PVCR of 3.0 through the second level. Although these results are inferior to those discussed above, the

thick barriers of the $In_{0.53}Ga_{0.47}As$/InP sample probably hindered the performance greatly, just as they do in other material systems. This DBRTD with much thinner InP barriers could ultimately provide competitive performance with the other $In_{0.53}Ga_{0.47}As$-based DBRTDs, since it has the advantage over $In_{0.53}Ga_{0.47}As$/AlAs of lattice matching and the advantage over $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ of no alloy scattering in the barriers.

3.4. InAs-based structures

High-quality DBRTDs have recently been fabricated from the InAs/AlSb material system, whose band offset is shown in Fig. 4. This is a type-II-staggered offset in which the valence-band edge of the AlSb lines up in the band gap of the InAs. Consequently, an electron tunnels into the AlSb from the InAs at an energy well below the branch point, and K is approximately 0.6 times the maximum value. In contrast, an electron tunnels into a type-I offset barrier, such as the AlAs barrier depicted in Fig. 4, much closer to the branch point. Since Γ_1 and J_P both depend on this attenuation coefficient roughly as $\exp(-KL_B)$, the difference in K corresponds to a difference of approximately five times in J_P at the typical barrier thickness of 1.5 nm. The superior current capability of the InAs/AlSb structure is displayed in Fig. 3. The J-V curve was obtained on a diode having 1.5-nm-thick AlSb barriers and a 6.4-nm-thick InAs quantum well.[38] The measured values of $J_P = 3.7\times10^5$ A cm^{-2} and $\Delta J = 2\times10^5$ A cm^{-2} are comparable to the best results achieved in the $In_{0.53}Ga_{0.47}As$/AlAs system, and are considerably better than those of GaAs/AlAs DBRTDs.

In addition to the superior current density, the InAs-based material systems have two advantages over GaAs-based material systems for high-speed device performance.[38] First, electrons will drift across a given depletion layer in InAs much more rapidly than in GaAs provided that this layer is sufficiently thin ($\lesssim 0.1$ μm) or the voltage drop is sufficiently small that there is little probability of impact ionization.[39] The higher drift velocities compared with GaAs are due to the weaker electron LO-phonon interaction strength in InAs and the much larger separation in energy between the conduction-band edge and the first upper valley. A short depletion-layer transit time is necessary to maximize the device speed, as discussed in Sec. 5. A second advantage is that InAs DBRTDs have a significantly lower series resistance R_S. This stems primarily from the ultra low specific resistance R_C of ohmic contacts to InAs. Values of R_C as low as 5×10^{-8} Ω cm^2 have been measured by transmission-line model measurements made on non-alloyed InAs ohmic contacts.[40] The R_S is further reduced by the

higher mobility of electrons in InAs than in GaAs at all practical n-type doping concentrations. Each of these advantages of InAs relative to GaAs also applies to a lesser extent in comparing $In_{0.53}Ga_{0.47}As$ to GaAs.

3.5. GaSb and InSb structures

A type-II DBRTD is obtained by replacing the InAs quantum well in the above structure by GaSb. This is the basis for a type of resonant tunneling through quasibound levels in the valence band, which is called resonant interband tunneling (RIT).[41] The RIT structure has demonstrated a very high PVCR of approximately 20 at room temperature. A complementary structure having an InAs quantum well and GaSb cladding layers has also been demonstrated.[42,43] Unfortunately, in both types of structures the peak current density is not yet sufficient to be useful in high-speed circuits. However, the type-II alignment between GaSb and InAs allows for new types of vertical transistor structures.[44,45]

Very recently a DBRTD has been fabricated in the InSb/InAlSb system.[46] The PVCRs measured at room temperature and 77 K were 1.4 and 3.9, respectively. The appeal of this material system is that InSb has the excellent transport properties of very low electronic effective mass ($m^* = 0.0139m_0$) and high mobility resulting from a low electron-phonon scattering cross section. A disadvantage is the narrow bandgap ($E_G = 0.16$ eV at T = 300 K), which magnifies the effects of impact ionization and Zener (i.e., cross-gap) tunneling.

3.6. Column-IV material systems

In the preceding sections, the material systems have consisted of some combination of column-III (Ga, Al, or In) and column-V (As, Sb, or P) constituent materials. All high-speed DBRTDs have been made from one of these combinations. However, because of the success and pervasiveness of silicon in electronic devices, efforts have been expended to develop Si-based resonant-tunneling structures. The most studied material systems are Si_xGe_{1-x}/Si and Si/SiC. Although the band alignment in Si_xGe_{1-x}/Si is type I, most of the bandgap difference appears in the valence band of the SiGe. This results in a Si barrier in SiGe that is too small to allow strong electronic resonant tunneling. Therefore, researchers have studied hole resonant tunneling.[47,48] The best result reported to date is a PVCR of 2.0 at 77 K.[49] NDR has not yet been observed at room temperature. The relatively poor performance of Si_xGe_{1-x}/Si DBRTDs is apparently not caused by lattice mismatch, but instead is the

consequence of the undesirable transmission characteristics associated with resonant tunneling through quasibound levels in the valence band. The mixing that occurs between the light- and heavy-hole subbands smears out the transmission probability such that the ground state resonance is not well isolated from the next higher resonance, and hence the PVCR is degraded.

The Si/SiC system alleviates the difficulties of SiGe/Si by offering a much larger conduction-band offset and thus the possibility of strong electronic resonant tunneling.[50] Unfortunately, the poor crystalline quality of epitaxial SiC has precluded good experimental results. However, if SiC epitaxial growth techniques were to advance significantly, Si/SiC could become the material system of choice, particularly for applications of DBRTDs in large-scale Si integrated circuits.

4. DBRTD device physics

4.1. Band bending and diode capacitance

An external bias voltage applied across a DBRTD modifies the equilibrium band profile in the active region. In order to analyze the current density, one must determine the modified band profile, or band bending, to a satisfactory degree of accuracy. A first estimate is obtained by modeling the device as a semiconductor-insulator-semiconductor (SIS) diode. Unless the current density is very high, one can then assume that the diode is in a condition of quasi-equilibrium. Under this condition, the electron concentration on each side is characterized by a uniform quasi-Fermi level [i.e., E_F^c on the cathode (or emitter) side and E_F^a on the anode (or collector) side], as shown in Fig. 1. The band bending is obtained by solving Poisson's equation on each side and connecting the solutions with a uniform field across the double-barrier structure. Shown in Fig. 5 is the band bending obtained by this method for a DBRTD containing 5.0-nm-thick $Al_{0.42}Ga_{0.58}As$ barriers, a 5.0-nm-thick GaAs quantum well, and 50-nm-thick lightly doped spacer layers on either side.

The capacitance of the DBRTD in this model is what one expects from an analogous SIS diode. That is, $C \approx \varepsilon A(L_D + L_W + 2L_B + L_A)^{-1}$, where A is the area, L_D is the width of the depletion region, and L_A is the width of the accumulation region (i.e., the distance over which band bending occurs) on the cathode side. For the device in Fig. 5, $L_D \approx 60$ nm, $L_W + 2L_B = 15$ nm, and $L_A \approx 25$ nm, leading to $C/A \approx 1.1$ fF μm^{-2}. This is a typical specific capacitance

for high-speed DBRTDs, and is considerably lower than that of most other tunneling devices such as p-n (Esaki) diodes or Josephson-junction devices. The latter two devices require degenerate electron concentrations on both sides of the junction in order to achieve high current densities. In that case both L_D and L_A are roughly equal to 10 nm, and the specific capacitance is roughly five times that of the DBRTD.

A more accurate estimate of the band bending maintains the assumption of quasi-equilibrium in the cladding layers but accounts for at least one of the following effects: (1) spatial quantization in the accumulation layer, or (2) charge storage in the quantum well. To properly deal with the first effect, one must carry out self-consistent calculations of the Poisson and Schrödinger equations such as those discussed in Chapter 1. Such calculations made on DBRTDs indicate that the electron states in the accumulation layer consist of a continuum at energies above the neutral band edge on the cathode side and quasibound states at lower energies.[51] In the majority of DBRTD structures, the binding energy of the lowest quasibound state (relative to the neutral band edge) is only a small fraction of the total potential drop across the accumulation layer, V_A. The presence of these quasibound levels has been correlated experimentally with undulations in the I-V curve at voltages below the first peak.[52] The charge storage in the quantum well can have a profound effect on the I-V curve and is addressed in Sec. 4.3.

4.2. Current density

The current density J is estimated quantitatively by employing the well-known stationary-state transport model in which the traversal through the double-barrier structure is analyzed by the stationary-state formulation discussed in Sec. 2.2, and the transport in the cladding layers is analyzed with semiclassical theory.[53] The magnitude of J in a given longitudinal energy interval is thus the product of the density of electrons incident, the group velocity, and the transmission probability in this interval. The magnitude of current density is the difference between the left-hand-going and right-hand-going fluxes, integrated over all energy,[15]

$$J = \beta kT \int_0^\infty dE_Z T^* T \log \left[\frac{1 + \exp(E_F^c + eV_A - E_Z)/kT}{1 + \exp(E_F^c + eV_A - eV_T - E_Z)/kT} \right], \tag{4.1}$$

where $\beta = em^*/2\pi^2\hbar^3$, and V_T is the total applied voltage across the device defined in Fig. 1. It is useful to evaluate this integral in conjunction with the Breit-Wigner form for T*T in Sec. 2.1. When the temperature is low enough that the Fermi distribution on the cathode side is degenerate and the bias voltage is high enough that the anode-to-cathode current can be ignored, one obtains

$$J \approx \frac{2\beta\Gamma_1^L\Gamma_1^R}{\Gamma_1}(E_F^c + eV_A - E_P)\left[\tan^{-1}\left[\frac{2(E_F^c + eV_A - E_P)}{\Gamma_T}\right] - \tan^{-1}\left[\frac{2(eV_A - E_P)}{\Gamma_T}\right]\right] \quad (4.2)$$

$$+ \frac{\beta\Gamma_1^L\Gamma_1^R\Gamma_T}{2\Gamma_1}\log\left[\frac{\Gamma_T^2/4 + (eV_A - E_P)^2}{\Gamma_T^2/4 + (eV_A + E_F^c - E_P)^2}\right],$$

where E_P peak energy of T*T relative to the conduction band edge on the cathode side. The minimum limit of integration has been taken as V_A based on the assumption that a negligible fraction of the electrons occupy spatially quantized states in the accumulation layer. In DBRTDs containing thin barriers, the major effect of the bias voltage on T*T is to displace E_P downward relative to the band edge on the cathode side. At low bias voltages satisfying $E_F^c + eV_A < E_P$, *both* $\tan^{-1}$ *factors are approximately* $-\pi/2$, and the current is cathode-to-anode current is determined largely by the second term (with the logarithmic factor). At bias voltages satisfying $eV_A < E_P < eV_A + E_F^c$, the two $\tan^{-1}$ factors sum to approximately π and the second term (with the logarithmic factor) is negligible provided that $E_F^c > \Gamma_T$. From the prefactor for the first term, the current increases monotonically with bias voltage in this range up to the point $eV_A \approx E_P$ where the second $\tan^{-1}$ factor changes sign to positive. For just a small variation in bias voltage about this point, the two $\tan^{-1}$ terms go from π to 0. This rapid change defines the precipitous drop in current associated with the NDR region. For a bias voltage slightly less than that yielding $eV_A = E_P$, the current density reaches its peak value. Under the condition $E_F^c \gg \Gamma_T$, one finds $J_P \approx 2\pi\beta\Gamma_1^L\Gamma_1^R E_F^c/\Gamma_1$. The fact that Γ_S does not appear in this expression illustrates the important point that J_P is independent of scattering processes in the double-barrier structure that can be represented by the Breit-Wigner formalism and are weak enough to satisfy $E_F^c \gg \Gamma_S$. This conclusion was first drawn by Weil and Vinter in the case of sequential resonant tunneling.[54]

Figure 6 compares the theoretical and experimental current density for one of the best DBRTDs (in terms of room-temperature PVCR) fabricated in the GaAs/AlGaAs material

system. It is the same diode whose band bending appears in Fig. 5. The peak currents agree within a factor of two, but the valley currents differ by about a factor of 100. The discrepancy in valley currents reflects the predominance of excess-current mechanisms not addressed by the stationary-state model. Several of these mechanisms are discussed in Sec. 4.5. Another experimental aspect not explained by the model is the small undulation in the experimental I-V curve at approximately 0.3 V. This is an indicator of quantum-size effects in the accumulation layer on the cathode side. The distorted nature of the experimental I-V curve in the NDR region is attributed to the rectification by the DBRTD of its own electrical oscillations with the measurement circuit. The rectification results in a hysteresis loop in the I-V curve (denoted by arrows in Fig. 6), which is known as *extrinsic bistability*.[55]

Although there are several shortcomings with the stationary-state model, the fact remains that in high-quality structures it does a good job of predicting J_P. Thus, it is useful in designing DBRTDs for high-speed applications, where J_P is one of the most important device specifications.

4.3. Quantum-well charge storage

Like any quasi-two-dimensional system, the double-barrier structure can harbor mobile sheet charge. Intuitively, one expects that the sheet charge density σ_w is proportional to the product of the current density and the lifetime (i.e., $\sigma_w = J\tau$). Detailed treatments of this effect in the sequential[56] and coherent[57] limits have resulted in the following expression for σ_w in the first quasibound level:

$$\sigma_{w,1} = \frac{J\hbar}{\Gamma_1^R} \,. \tag{4.3}$$

An important assumption made in deriving this expression is that the escape of an electron from the quantum well to the cathode side is prohibited by Pauli exclusion of occupied states on that side. Thus one expects the expression for $\sigma_{w,1}$ to be most applicable at low temperatures where the charge in the well is fed only by electron states on the cathode side that have a Fermi occupancy factor near unity.

An important effect of the sheet charge is to alter the electrostatic potential across the double-barrier structure from the linear form assumed in Secs. 4.1 and 4.2. The altered potential modulates the resonant-tunneling current because of the strong dependence of this current on the position of the quasibound level in the well. Because the sheet charge is proportional

to the current density by Eq. (4.3), the net current density becomes self-dependent. This mechanism is known as *electrostatic feedback*.[58, 59] Shown in Fig. 7 are I-V curves for a typical double-barrier structure computed by demanding self-consistency between Eqs. (4.2) and (4.3). With Γ_S set equal to zero, the current is multiple valued between the peak and valley voltages, an effect known as *intrinsic bistability*.[58] This effect has not been observed unambiguously in any double-barrier structures containing symmetric barriers (i.e., the same barrier materials and thicknesses). Instead, such structures typically display *extrinsic* bistability as defined in Sec. 4.2. Intrinsic bistability has been observed clearly only in a highly asymmetric structure biased so that the more transparent barrier is adjacent to the cathode (i.e., $\Gamma_1^L \gg \Gamma_1^R$).[59, 60]

One possible reason for the lack of experimental intrinsic bistability is the broadening of T*T by scattering. This effect can be modeled by making Γ_S non-zero in the self-consistent I-V calculations. For example, when Γ_S = 4.0 meV, the bistability in Fig. 7 disappears. At a much larger Γ_S of 20 meV, which is approaching E_F^c in the device of Fig. 7, the peak current decreases and the peak region broadens. A Γ_S of 4 meV is consistent with the results of a recent experimental study on a variety of double-barrier structures.[61] Another reason for the lack of bistability may be quantum-size effects in the accumulation layer. Self-consistent calculations of the I-V curve in symmetric DBRTDs generally do not display intrinsic bistability if spatial quantization is accounted for in both the quantum well and accumulation layer.[62, 63]

4.4. Current fluctuations

As in all electronic devices, the fluctuations of current in DBRTDs arise from fluctuations in the population of electronic states or, equivalently, fluctuations in the energy and momentum of electrons in specific regions of the device. These fluctuations give rise to electrical noise in either the current or voltage at the terminals of the device, and are important in DBRTDs for the following reasons. First, in a practical sense the electrical noise sets the limit on the peformance of the DBRTD in certain device applications such as oscillators. Second, the measured noise can reflect underlying physical processes that are difficult to detect by other experimental techniques.

The current fluctuations in a DBRTD are quantified in the standard way by a power spectrum $S_I(f)$, which represents the mean-square current measured per hertz of bandwidth by an ideal current meter connected across the terminals of the device. At low frequencies, the

power spectrum has a 1/f-type behavior arising from a number of mechanisms, such as trap states in the barriers. Well above the 1/f knee and up to frequencies approaching the speed limits of the device, the current fluctuations are dominated by thermal and shot-noise mechanisms. The thermal noise is dominant when little or no bias voltage is applied, so that the device is near thermal equilibrium. The shot noise dominates at high bias voltages, where the current is large and is limited by the double-barrier structure. The shot-noise power spectrum measured between the anode and cathode contacts is expressed by $S_I = 2\gamma eI$, where γ is the shot-noise factor.[64] For devices containing single barriers whose transmission properties do not depend on the current density (e.g., p-n, Schottky, and single-heterobarrier diodes), it is generally found that $\gamma = 1.0$. The DBRTD can display deviations from $\gamma = 1.0$ because T*T is a function of the current through the electrostatic feedback mechanism.

To model the shot-noise mechanism in DBRTDs, one supposes that the total current arises from a superposition of electron fluxes incident on the double-barrier structure in all longitudinal energy intervals. Fluctuations occur in each flux because of thermalization processes on the cathode side. These fluctuations have two effects on the total current. First, they contribute directly to a fluctuation in the transmitted flux on the anode side. Second, they vary the charge in the quantum well, which alters the energy of the quasibound state electrostatically. This process modulates the transmission in other energy intervals, thereby decreasing or increasing the current in those intervals. A detailed calculation of the shot-noise factor based on these consideratons has been carried out in the limit of degenerate Fermi statistics on the cathode side.[65] The theoretical results are shown in Fig. 8 for the same DBRTD as in Figs. 5 and 6. At bias voltages below the current peak, the shot noise is suppressed, the γ being roughly 0.3. At the peak voltage, γ crosses unity and stays greater than 1.0 throughout the NDR region, representing shot-noise enhancement. Both of these predictions are in good agreement with the experimental results described in Sec. 7.

4.5. Excess current

Excess current is defined as the current measured through the RTD, at the valley point and beyond, that is not explained by elastic tunneling theory. It does not include the potentially large elastic current components that pass through the double-barrier structure at upper quasibound levels or thermionically over the tops of the barriers. The latter two components are properly predicted by the coherent theory, Eq. (4.1), provided that an accurate form of the transmission probability is obtained for all longitudinal energies.

One of the most important sources of excess current in RTDs is transport associated with upper valleys, particularly the X-valley in AlAs barriers. Early on, the vast superiority of the $In_{0.53}Ga_{0.47}As$/AlAs diodes over GaAs/AlAs diodes was attributed in large part to the larger energy separation, ~ 0.65 eV, between the Γ conduction-band minimum in the $In_{0.53}Ga_{0.47}As$ and the X conduction-band minimum in the AlAs barrier.[34] In contrast, this separation is estimated to be 0.13 eV in the GaAs/AlAs system, and has been experimentally correlated to the excess valley current in these devices through hydrostatic pressure experiments.[66]

The X-valley-related excess current in both single- and double-barrier structures has been studied theoretically by a number of techniques including Fowler-Nordheim models,[67] transfer-matrix techniques,[68] pseudopotential methods,[69] and empirical tight-binding formalisms.[70] Although there is not a consensus, a commonly described transport mechanism in double-barrier structures is one whereby the incident Γ electron transfers to X at the first heterojunction, maintains an X character throughout the double-barrier structure, and subsequently transfers from X back to Γ at the last heterojunction. The materials having a large Γ–X offset greatly suppress this mechanism by making the initial and final Γ–X transfers much less probable.

Another important source of excess current, inherent to all RTD materials, is LO-phonon scattering. In the sequential picture, this scattering allows electrons to transfer from the cathode side into the quantum well at bias voltages past the point of alignment between the quasibound level and occupied states on the cathode side.[71] Once in the quantum well, the electrons can tunnel to the anode side by elastic means. In the coherent picture, the LO-phonon scattering introduces sidebands on the transmission probability curve separated by an integral number of phonon quanta, $\pm n\hbar\omega_{LO}$, from the central peak.[72] In either picture, a large excess current arises in the vicinity of the valley voltage in most RTDs. Materials having lower effective mass tend to have a relatively smaller amount of this scattering, which is another advantage of the indium-bearing materials, $In_{0.53}Ga_{0.47}As$ and especially InAs, over GaAs.

Acoustic-phonon and alloy scattering have been analyzed by the same sequential mechanism as used for the LO phonons.[71] The conclusion reached for acoustic phonons is that they play a much smaller role than optical phonons in generating excess current. However, the analysis was not carried out for polar-mode (i.e., piezoelectric) acoustic-phonon scattering which is known to be very strong in narrow-band, low-effective-mass materials.

Alloy scattering in ternary compound barriers can give rise to a more significant excess current component that is approximately independent of temperature. This component can explain the inferior PVCR of the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ RTDs relative to those made from $In_{0.53}Ga_{0.47}As$/AlAs, since the AlAs barriers are presumably pseudomorphic and therefore introduce neither alloy nor dislocation scattering.

More recently, the excess current due to scattering off of interface defects has been studied. [73] This is an important mechanism because it is generally believed that the heterointerfaces in all heterojunction devices, including RTDs, are rough in the lateral plane by at least one monolayer. This imperfection breaks down the conservation of lateral momentum, leading to a scattering mechansim that, like alloy scattering, has a very broad transmission characteristic. An interesting prediction is that the strength of this scattering mechanism depends heavily on which interfaces in the RTD are assumed to be rough.

A final-excess current mechanism inherent to all RTDs arises from scattering in the cladding layers. This is, perhaps, the most fundamental of all scattering mechanisms, but one of the most difficult to deal with, since it transcends the stationary-state model outlined in Sec. 4.2. The stationary-state model separates the quantum-mechanical transport in the barrier structure from the semiclassical transport in the cladding layers. A proper description requires the quantum-transport theory discussed in Chapter 9. The latter theory has yielded excellent agreement with experiment at the valley point of GaAs/AlAs RTDs.[63]

5. Time-delay mechanisms

5.1. Fundamental RC limit

Like any electronic device in which the current flow is limited by a barrier, a fundamental speed limit of the DBRTD is set by the time required to charge or discharge the space-charge regions in the active region of the device. This is known as the RC limit, where R and C are the differential resistance and capacitance, respectively, associated with the active region. A great advantage of the DBRTD over most other tunneling devices is that the intrinsic RC time constant can be made very small, with values below 1 ps being possible in optimized devices. This is because R and C are determined by different factors, so that they are essentially independent quantities. R is inversely related to J_P, which depends on the

carrier concentration on the cathode side (through the quasi-Fermi level E_F^c) and on the area (in energy space) under the transmission resonance (see Sec. 4.2). C is inversely related to the depletion length on the anode side, which depends on the doping distribution on this side. Two mechanisms that reduce the speed of the DBRTD below that defined by the RC time are the finite resonant-tunneling traversal time and the finite transit time across the depletion layer.

5.2. Resonant-tunneling traversal time

The effect of the resonant-tunneling traversal time can be analyzed by a number of techniques with widely varying degrees of sophistication. One analysis has applied linear-response theory to determine the equivalent electrical admittance of the double-barrier structure.[74] The analysis starts by determining the response of the conduction current, $i(t)$, to an applied voltage step ΔV. It is reasonable to assume that the step response is exponential in time with time constant τ_n.[74]

$$i(t) = I_1\theta(-t) + \left[I_2 + [I_1 - I_2]\exp(-t/\tau_n)\right]\theta(t)\,, \tag{5.1}$$

where I_1 and I_2 are the initial and final dc currents, respectively, and $\theta(t)$ is the unit step function. In the small-signal limit where $I_2 = I_1 + G_S\Delta V$ and G_S is the differential conductance of the double-barrier structure, the impulse response function is given by $h(t) = (\Delta V)^{-1}di(t)/dt = [1 - \exp(-t/\tau_n)]\delta(t)G_S + \exp(-t/\tau_n)\,\theta(t)G_S/\tau_n$. Finally, the admittance is obtained by Fourier transformation,

$$Y_S(\omega) = \int_{-\infty}^{\infty} h(t)\exp(-i\omega t)\,dt = \frac{G_S}{1 + i\omega\tau_n}. \tag{5.2}$$

The reciprocal impedance function, $Z_S(\omega) = Y_S^{-1}(\omega)$, has the form $G_S^{-1} + i\omega L_S$ where $L_S = \tau_n/G_S$ is the tunneling inductance. Intuitively, an inductive reactance might be expected in any model of resonant tunneling since the time required for the build up or decay of the wavefunction in the quantum well leads to a delay of current with respect to voltage.

An inductive character of the resonant-tunneling admittance has also been predicted by more rigorous quantum-transport treatments.[63,75] In at least two such treatments the magnitude of the inductance was similar to that derived here, but the sign was opposite, that is, $L_S = -\tau_n/G_S$. The sign is important since the high-frequency admittance behaves very differently when the inductance is negative than when it is positive. The result derived here would change sign if in Eq. (5.2) the argument of the exponential was positive. However, $\exp(-i\omega t)$ is the correct form, since the Fourier transform is a special case of the Laplace transform, and to obtain a bounded result the Laplace transform must weight the time-varying waveform by $\exp(-st)$ where s is the complex frequency.

One shortcoming of the analysis is the assumption of an exponential approach to steady state. It is thought that the actual conduction current displays a much richer behavior on short time scales. Time-dependent quantum-mechanical solutions yield an oscillatory component

with an exponentially decaying envelope.[75] This is indicative of the well-known *ringing* phenomenon of resonant systems. For resonant tunneling through the first quasibound level, the oscillatory component has a period very close to the traversal time t_w across the quantum well of a wave packet centered at energy E_1. The effect of the ringing on the admittance is to cause the imaginary part to increase as ω approaches t_w^{-1}. This increase will be most observable experimentally in structures designed with very thin barriers so that $\tau_1 \approx t_w$.

5.3. Depletion-layer transit time

The effect of a finite depletion-layer transit time can be understood by thinking of the double-barrier structure as an electron injector. As such, the electrons will have an initial kinetic energy that is close to E_1 in the quantum well. Most double-barrier structures have $E_1 \gtrsim 100$ meV to satisfy the spatial-quantization condition given in Sec. 2.1. Such a kinetic energy corresponds to a very high group velocity v_g in the common III-V materials. For example, a 0.1 eV kinetic energy in GaAs corresponds to $v_g \approx 7\times10^7$ cm^{-1} according to the theoretical Γ-valley dispersion curve. The theoretical v_g derived from this curve is shown in Fig. 9.[76] One expects this velocity to be maintained over some distance approximately equal to the ballistic mean free path, which depends critically on the applied electric field, the upper-valley separation, and the strength of the optical-phonon interaction. After drifting this distance, the electron is rapidly decelerated, and then crosses the remaining depletion region at a velocity much closer to the saturated value. For example, in GaAs the small upper-valley separation of 0.28 eV limits the ballistic mean free path to about 20 to 30 nm. In the indium-bearing materials, $In_{0.53}Ga_{0.47}As$ and InAs, the ballistic mean free path is significantly higher because of the larger upper-valley separations, ~ 0.5 and 0.9 eV, respectively, in these materials.

In a DBRTD having a very large depletion length, one expects the transit time to be given by $t_T \approx L_D/v_s$, where v_s is the saturation velocity in the depletion-layer material. In GaAs, $v_s \approx 1\times10^7$ cm s^{-1}, so that an electron suffers a delay of 1 ps in a distance of only 100 nm. Because of this fact, DBRTDs have usually been designed with L_D somewhat less than 100 nm to maintain a short transit time. However, a long L_D can lead to an enhancement in the magnitude of the terminal NDR, which is the basis for a device called the quantum-well injection and transit time diode.[77]

6. High-speed performance characteristics

6.1. Small-signal impedance model

The fundamental RC time constant, the resonant-tunneling time and the transit time can be combined into a small-signal impedance model of the DBRTD that is very useful in characterizing high-speed devices. To construct this model, one starts with the double-barrier structure alone, noting that a time-varying potential induces a displacement current in addition to the resonant-tunneling conduction current analyzed in Sec 5.2. The time-varying potential is assumed to be unaffected by the charge storage in the quantum well. This assumption allows one to neglect the contribution to the impedance of the so-called quantum-well capacitance,[78] which has a significant effect only in relatively wide quantum wells.[79,80] The displacement current through the double-barrier structure is represented by a capacitance $C_S = \varepsilon A/(L_W + 2L_B)$ in shunt with the complex tunnel admittance $Y_S(\omega)$ of Eq. (5.2), where ε is the permittivity and A is the lateral area of the diode. To include the additional potential drop in the space-charge regions outside of the double-barrier structure, it is assumed for the moment that the conduction current traverses these regions with no transit-time delay. The circuit elements G_S and C_S are then simply scaled by the factor dV_S/dV_D and L_S by the inverse to form the lumped-element circuit shown in Fig. 10. The series resistance R_S in Fig. 10 arises from ohmic dissipation outside the active region of the device, so that it is not involved in the scaling. The element G is the differential conductance measured across the terminals of the diode, C is the total space charge capacitance, and L_{QW} is called the "quantum-well inductance" because of its physical origin - the quantum-well quasibound-state lifetime. The validity of this circuit has been confirmed by two separate theoretical treatments.[81,82]

To include the effect of the depletion-layer transit time, the electron is assumed to have a constant drift velocity v_d that is an average between the high initial velocity and a saturated terminal velocity. This assumption allows one to apply the small-signal transit time theory that has been successful in describing a variety of fast devices such as IMPATT diodes.[83] In this theory the real part of the admittance of the double-barrier structure is represented as an injection conductance, $\sigma = dJ/dF_W \approx (L_D + L_W + 2L_B + L_A)A^{-1}G(1 + i\omega\tau_1)^{-1}$, where F_W is the electric field (implicitly uniform) across the double-barrier structure, and $G = dI/dV$ is the differential conductance associated with the entire active region. This leads to a total

impedance of [24,77]

$$Z_{TT} = \frac{L_D}{i\omega\varepsilon A}\left[1 - \frac{\sigma}{\sigma + i\omega\varepsilon}\frac{1-\exp(-i\theta_d)}{i\theta_d}\right]\sigma + i\omega\varepsilon + R_S(\omega)\,, \qquad (6.1)$$

where ε is the permittivity of the double-barrier region, and $\theta_d = \omega L_D/v_d$ is the transit angle. The first term is the component arising from the finite transit time. In the limit of infinitesimal transit time or zero frequency, this term reduces to the sum of the space charge resistance $R_{SC} \simeq L_D^2/2A\varepsilon v_d$, and the depletion-layer capacitance $C = \varepsilon A/L_D$. The space-charge resistance arises from mobile charge storage in the depletion layer. In the limit of zero frequency, the second term reduces to the differential resistance and the quantum-well inductance, so that the total expression reduces to the lumped-element RCL model shown in Fig. 10.

6.2. Maximum oscillation frequency

Provided that it can be stably dc biased in the NDR region, the DBRTD is capable of oscillating up to a frequency f_{max} at which the real part of the terminal impedance vanishes. In the limit of infinitesimal transit angle, this frequency reduces to that predicted from Fig. 10, namely

$$f_{max}^{RCL} = \frac{1}{2\pi}\left[\left[\frac{1}{L_{QW}}C(1 - C/2L_{QW}G^2)\right]\left[1 - \sqrt{1 - \frac{(GR_S + 1)/GR_S}{(C/2L_{QW}G^2 - 1)^2}}\right]\right]^{1/2}. \qquad (6.2)$$

In the limit that $L_{QW}\to 0$ or equivalently $\tau_n\to 0$, this solution reduces further to the RC-limited result $f_{max}^{RC} = (2\pi C)^{-1}\sqrt{-G/R_S - G^2}$. A solution to the above equation always exists provided that $|G|R_S < 1$, $G < 0$, and $L_{QW} < 0$. The first condition defines the dc-bias stability mentioned above, and the next two are automatically satisfied in the NDR region. Also note that in the NDR region the imaginary part of the impedance of this circuit is always less than zero because L_{QW} is negative. This means that the equivalent circuit in Fig. 10 cannot self-oscillate, i.e., it cannot oscillate by an internal resonance.

Listed in Table I are the theoretical values of f_{max}^{RCL} for the fastest DBRTDs fabricated to date. The highest f_{max} values for GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs diodes are 555 and 1280 GHz, respectively. The superiority of the $In_{0.53}Ga_{0.47}As$/AlAs diode is attributable to a lower magnitude of NDR per unit device area and to a lower specific series resistance.

6.3. Switching time

The NDR region is also the basis for switching from the peak to the valley region of the DBRTD, and vice versa. The switching process occurs by dc biasing the device near the peak point through a load resistance R_L that is consistent with dc bistability (i.e., two possible dc bias points exist, one above and one below the NDR region). This resistance must satisfy $R_L > \Delta V/\Delta I$. A slight increase in the bias voltage will then eliminate the stable operating point at the peak and cause a switch to the stable point at the valley point or beyond. The separation in voltage between the initial stable point and the final one is assumed to be small enough that the diode capacitance is constant at the peak-voltage value.

A useful estimate of the switching time is obtained by analyzing only the RC components without accounting for the resonant-tunneling traversal or transit-time delays. The I-V curve in the NDR region is represented by the following parabolic form:

$$I = \frac{\Delta I}{\Delta V^2}(V - V_V)^2 + I_V \, . \tag{6.3}$$

This expression increases in slope monotonically as the voltage is decreased from the valley point to the peak point. It is thought to be a good approximation to the stable I-V curve at all voltages except those just above the peak. For a load resistance equal to $\Delta V/\Delta I$, as shown in Fig. 11, the time required for the diode voltage to increase from a value 10% above the peak voltage to a value 10% below the valley voltage is given by

$$t_R = \int_{V_P+0.1\Delta V}^{V_V-0.1\Delta V} \frac{C dV}{-\Delta I/\Delta V(V - V_V) - \Delta I/\Delta V^2(V - V_V)^2} \, . \tag{6.4}$$

Evaluation of this "rise time" integral yields $t_R \approx 4.4\Delta V/S$, where $S = (J_P - J_V)/C$ is called the speed index.[84]

Theoretical results for the fastest GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs DBRTDs are given in Table II. The highest S and lowest t_R values, by far, are predicted for the diodes having the highest current density.[85] This results in part from a high ΔJ of $\approx 3.2\times10^5$ A cm^{-2}, and in part from a small ΔV. A comparison with the oscillator characteristics in Table I leads to the following important point regarding DBRTDs. The best oscillator diodes are not necessarily the best switching diodes, and vice versa. Increasing ΔJ tends to increase oscillator power and decrease switching time in the same manner. Increasing ΔV also enhances oscillator power, but it increases the switching time since a greater ΔV requires a greater change of

charge stored in C.

In considering the subpicosecond values given in Table II, it is important to realize that the neglected resonant-tunneling traversal and transit-time delays could significantly affect the switching time on the given time scale. It is expected that the depletion-layer transit time will increase t_R, but the[86] effect of the quantum-well traversal time is not yet clear.

7. High-speed experimental results

7.1. Oscillations

Oscillations can be made to occur in the NDR region at any frequency from dc up to f_{max}. One requirement for oscillation is that the device be dc stable in the NDR region so that $R_L < \Delta V/\Delta I$, where R_L is the real part of the dc load impedance, $\Delta V = V_V - V_P$, and $\Delta I = I_P - I_V$. Another requirement for oscillation is that the total impedance be resonant in the sense that the imaginary part is zero. A variety of resonant circuits have been made with DBRTDs, but the waveguide resonator shown in Fig. 12 has been the most useful and has yielded the highest-frequency results to date. Oscillators operating around 50, 100, 200, 350, and 650 GHz have been studied extensively.[24]

One of the useful results of oscillator measurements is the determination of f_{max}. The comparison between experiment and theory for two diodes is given in Fig. 13. The lower-frequency results are for a diode having thick (4.8 nm) $Al_{0.42}Ga_{0.58}As$ barriers, so that $\tau_1 >> \tau_{RC}$ and $\tau_1 >> t_T$. This allows one to observe the effect of the quantum-well inductance. It is clear from the results that the f_{max} with the quantum-well inductance included provides a better agreement with the observed rolloff of oscillation power of this device. The f_{max}^{RCL} of this device is calculated to be 50 GHz, while f_{max}^{RC} is 180 GHz. Figure 13 also compares the experiment and theory of the fastest GaAs/AlAs oscllator tested to date. The results are, again, consistent with theory in that the maximum measured oscillation frequency of 420 GHz is below f_{max}^{RCL}, which is 468 GHz. The theoretical calculation uses a G equal to the maximum slope in the NDR region. A more detailed analysis shows that a threefold reduction in R_S with the same G would increase f_{max}^{RCL} to approximately 900 GHz.[24]

The oscillation results for the fastest diodes made to date in all three material systems are presented in Fig 14. The relatively poor PVCR of the GaAs/AlAs diode limits the power

density to a maximum low-frequency value just over 1×10^3 W cm^{-2}. The typical absolute power obtained from a 4-μm-diameter diode of our fastest GaAs/AlAs material is 15 μW at 112 GHz and 0.2 μW at 360 GHz. The superior PVCR of the $In_{0.53}Ga_{0.47}As$/AlAs diodes provides a low-frequency power density of 1×10^4 W cm^{-2}, which is comparable to that generated by microwave IMPATT diodes. For the $In_{0.53}Ga_{0.47}As$/AlAs results labeled (A) in Fig. 14, such power densities were maintained up to only 10 GHz because of high device capacitance. Recently, a superior $In_{0.53}Ga_{0.47}As$/AlAs diode, labeled (B) in Fig. 14, has been demonstrated with a power density of 1.2×10^3 W cm^{-2} and absolute power of 50 μW at 110 GHz. This is the highest oscillation power obtained from a DBRTD to date above 100 GHz.

DBRTDs made from InAs/AlSb are very promising for submillimeter-wave oscillator applications. The power density of the InAs/AlSb RTD at 360 GHz is about 50-times greater than that of the GaAs/AlAs RTD at the same frequency. The absolute power of a 2-μm-diameter InAs/AlSb diode at 360 GHz was measured to be 3 μW, which is about 12-fold more power than obtained from a GaAs/AlAs diode having four times the area. The highest frequency measured to date from InAs/AlSb diodes is 712 GHz.[87] The power density and absolute power at this frequency were measured to be 20 W cm^{-2} and 0.5 μW, respectively. The InAs/AlSb DBRTD should be capable of oscillating up to about 1 THz.

7.2. Small-signal impedance

Network analysis entails the measurement of the small-signal impedance or admittance of the DBRTD, and is most easily done in the positive differential resistance (PDR) region where the device is inherently dc stable. The first network analysis measurements found that the imaginary part of the impedance contained an inductive component that was practically independent of bias voltage.[88] The physical origin of this inductance was not clear. A second study also found an inductive component in the DBRTD impedance and has shown qualitative agreement between experiment and the small-signal impedance model derived in Sec. 6.1.[89]

More recently, small-signal impedance measurements have been carried out in both the PDR and a stable NDR region by a network analysis.[80] The measurements were conducted on a specially designed DBRTD in the $In_{0.53}Ga_{0.47}As$/AlAs material system, which had a very low J_p ($\approx$ 100 A cm^{-2}) and a sufficiently high PVCR ($\approx$ 3.0) at room temperature that the electron transport through the structure was primarily resonant tunneling through the first quasibound state. The experimental I-V and G-V curves are shown in Fig. 15(a). The low J_p

allowed the DBRTD to be stablized against all oscillations in the NDR region, so that an accurate admittance measurement could be made in this region. The results are summarized in Fig. 15(b) and (c) for bias voltages of 1.40 and 1.72 V, respectively. In the PDR region at 1.40 V, the conductance is practically independent of frequency, and the susceptance is nearly linear, consistent with a simple RC model of the device. In the NDR region at 1.72 V, the conductance displayed a strong frequency dependence and the susceptance showed an obvious inductive character consistent with with $L_{QW} = \tau_1/G$ and τ_1 = 1.6 ns. One possible explanation for the absence of inductance in the PDR region is that the resonant-tunneling traversal time is much shorter than it is in the NDR region because inelastic scattering significantly reduces the quasibound-state lifetime. This is presently an active area of research.

7.3. Electrooptic measurements of switching time

A technique that has measured DBRTD switching with high resolution in the time domain is electrooptic sampling. In one version of this technique, switching is induced by a fast photoconductive gap in a transmission line,[90] and in another version it is induced by electronic means (a pulse-forming circuit).[91] The version with photoconductive-switch excitation is shown schematically in Fig. 16(a). A DBRTD chip is mounted on one conductor of a heterogeneous coupled stripline in such a way that the n^+ GaAs substrate makes contact to the stripline conductor on a $LiTaO_3$ substrate, and the top mesa is connected (by a whisker) to the conductor on a GaAs substrate. Synchronous pulses from a short-duration (~ 80 fs) dye laser are used to activate a photoconductive gap in the conductor on the GaAs side of the transmission line and to measure the electric field between the conductors by probing the change of refractive index in the $LiTaO_3$ induced by the switching action of the diode. The experimental results for this technique are shown in Fig. 16(b). The elapsed time between the 90 and 10% points is found to be 2.1 ps. The DBRTD structure used from this test consisted of two 1.7-nm-thick AlAs barriers separated by a 4.5-nm-thick GaAs quantum well. It is the same DBRTD structure that oscillated up to approximately 200 GHz.[92]

The electrooptic sampling technique with electrical excitation has yielded somewhat longer switching risetimes, in the range of 6 to 10 ps.[91] These results were obtained on DBRTDs that, in theory, were at least as fast as the one tested above. The discrepancy between the two results has been attributed to the fact that the photoconductive switch generates a very fast pulse across the DBRTD that is larger than ΔV in amplitude. Such a pulse

can accelerate the switching process of the DBRTD by the effect known in switching theory as *overdrive.*

7.4. Microwave noise power spectrum

The noise power of high-speed DBRTDs has been measured by a radiometric technique in the PDR region and by an oscillator FM-noise technique in the NDR region. In the radiometric technique outlined schematically in Fig. 17, the noise power generated by the DBRTD enters a circulator designed for operation around 1 GHz. The circulator feeds the power to a low-noise amplifier chain, and the output power of the amplifiers is measured with a spectrum analyzer in a narrow bandwidth Δf centered at 1 GHz. The purpose of the circulator is to make the noise component of the amplifier, which is roughly 50% of the total noise, independent of the impedance of the DBRTD. From the noise power at the analyzer, an equivalent shot-noise current I_{eq} is derived using the circuit model of Fig. 17. This is a version of Fig. 10 in which L_{QW} can be neglected because of the low frequency. The thermal noise associated with the R_S is represented by a current generator $i_n = (4kT\Delta f/R_S)^{1/2}$, and is subtracted from the total noise in the process of deriving I_{eq} at each bias point.

The measurement of noise power in the NDR region is much more difficult because of the strong tendency for high-speed DBRTDs to oscillate in this region. With this fact in mind, a pragmatic approach is to force the DBRTD to oscillate at a suitably low frequency and deduce the noise properties from the FM characteristics of the oscillator power spectrum.[93] This technique provides only an upper limit since other mechanisms, such as 1/f noise in the contacts, can contribute significantly to the microwave power spectrum, but are not accounted for in the analysis.

Shown in Fig. 18 are the experimental results at 77 K for the same GaAs/AlGaAs DBRTD as in Figs. 5 and 6. The device exhibits obvious shot-noise suppression in the PDR region with a minimum γ of approximately 0.35 at a bias voltage just below the current peak. At the only bias point in the NDR region, the shot noise is enhanced by a factor of eight, in qualitative agreement with the theory derived in Sec. 4.6. The results at room temperature were similar except that less suppression and enhancement were measured in the PDR and NDR regions, respectively. In addition, shot-noise measurements have been carried out on an $In_{0.53}Ga_{0.47}As$/AlAs DBRTD having much thinner barriers, and a much higher J_P, than the GaAs/AlGaAs device.[93] This device also had a superior PVCR of 12 at room temperature.

The experimental shot-noise factor for this diode in the PDR region was qualitatively similar to that of the GaAs/AlGaAs diode, supporting the conclusion that the shot-noise suppression mechanism is inherent to all symmetric DBRTDs. Unfortunately, results were not obtained in the NDR region because of the difficulty in making this diode oscillate at low frequencies.

8. Survey of high-speed applications

8.1. Device qualifications

Many of the DBRTD applications investigated up to the present time are analogous to p-n (Esaki) tunnel-diode applications of the 1960s.[94] Most of the Esaki-diode applications were abandoned with the advent of fast transistors because of the difficulty in designing satisfactory circuits using only two-terminal devices. The DBRTD has three advantages over Esaki diodes that compensate for this shortcoming. First, the DBRTD is roughly ten times faster than the Esaki diode in both oscillations and switching. This allows the DBRTD to operate in the terahertz/picosecond regions that are presently the frontiers of high-speed electronics. Second, the I-V characteristics of DBRTDs can be tailored by *bandgap engineering* over a very large range. For example, peak current densities can be designed to occur from roughly 10^3 to 5×10^5 A cm^{-2} and peak voltages from roughly 0.3 to 3 V, both in the presence of a useful PVCR. Third, DBRTDs are compatible with modern heterostructure transistor devices since they are grown monolithically by the same epitaxial techniques and fabricated by very similar methods. This opens up many possibilities of high-speed DBRTDs used in conjunction with heterostructure transistors to make integrated circuits having superior performance or functionality[95] compared to existing circuits.

Presently dozens of applications of DBRTDs are under development or being proposed. Some of the more promising applications are summarized below. For a more complete discussion of the applications, the reader is referred to one of the review articles on the subject.[1,96]

8.2. DBRTD quasioptical oscillator

The oscillation of the DBRTD at 712 GHz establishes it as the fastest solid-state electronic oscillator demonstrated to date at room temperature. As such, it has the potential to fill

the need for coherent power in the region between 100 GHz and 1 THz where fundamental-frequency solid-state sources are lacking. In this region the primary application of the DBRTD is a low-noise local oscillator for high-sensitivity coherent radiometers. In this application the instantaneous linewidth must be less than about 100 kHz, and the oscillator should be frequency tunable by at least ± 1% of the nominal center frequency. A DBRTD oscillator satisfying these requirements is the quasioptical design represented in Fig. 19(a).[97]

Shown in Fig. 19(b) is the experimental power spectrum of the quasioptical oscillator operating near 210 GHz. This particular oscillator contains a DBRTD made from the $In_{0.53}Ga_{0.47}As$/AlAs material system and having an f_{max} of approximately 900 GHz. The oscillator power spectrum has a linewidth of approximately 20 kHz at 10 dB below the peak. The measured power was approximately 50 μW, which is sufficient to drive the superconducting quasiparticle mixers that operate in this frequency range, and is probably high enough to drive the next generation of cooled Schottky diode mixers made from InGaAs. Future versions of the quasioptical oscillator will operate up to frequencies of at least 400 GHz.

8.3. DBRTD pulse forming and trigger circuits

The fast switching behavior described in Sec. 6.3 makes the DBRTD ideally suited for generating sharp edges in response to a slowly varying input waveform. The basic idea is to take the dc load line in Fig. 11 and superimpose on it an ac drive waveform of arbitrary period. The amplitude of the drive is chosen such that the stable operating point switches from the peak to the valley region as the drive increases from minimum to maximum voltage, and the stable point switches from the valley to the peak region as the drive decreases from maximum to minimum. The resulting current waveform through the DBRTD can be much faster than the drive, and if fed into a separate circuit from the drive circuit (by frequency separation techniques) should have the form of a square pulse with sharp leading and lagging edges. With proper design the current pulse can be induced with a relatively small amplitude drive waveform, which means that the pulse generator has high sensitivity. Another benefit is that the switching thresholds are well defined by the peak and valley points, so that the sharp edges of the pulse always occur at the same phase of the drive voltage. This is the required characteristic of a trigger. These characteristics have been utilized recently in the demonstration of some monolithic DBRTD-based circuits, including a complete sampling head operating up to 26 GHz[98] and a trigger circuit operating up to 110 GHz.[26]

8.4. DBRTD-based signal-processing circuits

The flexibility in design of the DBRTD I-V characteristics can be utilized to perform various specialized signal-processing functions. For example, if a DBRTD is grown with compositional and doping profiles that are perfectly symmetrical about the center of the quantum well, then the I-V curve will be antisymmetrical about the origin. When such an I-V curve is driven with a sinusoidal voltage waveform, the current spectrum flowing through the diode will contain only odd harmonics of the drive waveform.[99] If the amplitude of the voltage waveform is close to the magnitude of the valley voltage of the DBRTD and if the PVCR of the DBRTD is sufficiently high, then the power contained in the fifth harmonic can exceed the power in the third. This property is demonstrated diagrammatically in Fig. 20(a). The performance of a prototype microwave fifth-harmonic multiplier is displayed in Fig. 20(b). The conversion efficiency to the fifth harmonic is approximately 0.3%.

If two or more double-barrier structures are grown in tandem, the overall I-V curve will have a sawtooth-like characteristic, similar to that observed with two or more Esaki diodes in series, but without the parasitic impedance of the interconnection. By designing the DBRTDs properly, the successive peaks in the sawtooth can be separated by equal voltage. This leads to the possibility of multibit analog-to-digital (A/D) conversion. Simulations on such a device have predicted that a 4-bit A/D converter made by this technique should operate up 30 GHz.[100]

8.5. DBRTDs in memory and logic circuits

When a single DBRTD is connected to the source terminal of a field-effect transistor (FET),[101] or to the emitter terminal of a bipolar junction transistor (BJT),[102] a negative transconductance region is introduced into the I-V curves of the transistor-DBRTD combination. When the FET (BJT) transistor is loaded by a suitable resistive load at the drain (collector) terminal, the output at this terminal will then be bistable in the sense that two different output states will be possible for the same input gate-voltage (base-current) level. Which output state results from a given input depends on how that input level was reached. This is the basis for a latch, or flip-flop, which is the building block of sequential (i.e., memory-containing) logic. When either transistor is loaded by a structure containing several DBRTDs in tandem, more than two possible output levels are obtained. This raises the possibility of multivalued (i.e., trinary or higher) logic families based on these devices.[95]

Improved performance (in terms of static power dissipation) with similar functionality can be obtained by using the DBRTD as the transistor load at the drain (collector) terminal and grounding the source (emitter). The analogous configuration of an FET and an Esaki-diode load was originally proposed by Lehovec as a low-power static RAM cell.[103] It can also function as a low-power inverter for combinational logic. The simulated load line of a heterostructure FET transistor loaded by a DBRTD is shown in Fig. 21(a). Clearly, the low static power is achieved by choosing a bias voltage V_{DD} so that the low-output (V_{OUT}^{LOW}) logic state is just above the valley point of the DBRTD. The resulting static transfer characteristic is shown in Fig. 21(b). The large hysteresis in this curve may enhance the logic noise margins, and is also the basis for static-RAM applications of this configuration. Such a circuit has been fabricated monolithically and shown to have the desired static properties.[104] Recently, this configuration has been demonstrated by numerical simulation to have a speed competitive with the fastest direct-coupled-transistor logic families presently available.[105]

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References

1. F. Capasso, S. Sen, and F. Beltram, "Quantum-effect devices," *High-Speed Semiconductor Devices*, (Wiley, New York, 1990).
2. N. Yokoyama et al., in, *Hot Electrons in Semiconductor Nanostructures*, ed. J. Shah, (Academic, Orlando, 1991).

3. see Chapter 11 by M. Reed and A. Seabaugh.

4. L. Esaki and R. Tsu, *IBM J. Res. Dev.* **14**, 61 (1970).

5. R.F. Kazarinov and R.A. Suris, *Sov. Phys. Semicond.* **6**, 120 (1972).

6. L.L. Chang, L. Esaki, and R. Tsu, *Appl. Phys. Lett.* **24**, 593 (1974).

7. T.C.L.G. Sollner, W.D. Goodhue, P.E. Tannenwald, C.D. Parker, and D.D. Peck, *Appl. Phys. Lett.* **43**, 588 (1983).

8. T.J. Shewchuk, P.C. Chapin, P.D. Coleman, W. Kopp, R. Fischer, and H. Morkoc, *Appl. Phys. Lett.* **46**, 508 (1985).

9. M. Tsuchiya, H. Sakaki, and J. Yoshino, *Jpn. J. Appl. Phys.* **24**, L466 (1985).

10. W.D. Goodhue, T.C.L.G. Sollner, H.Q. Le, E.R. Brown, and B.A. Vojak, *Appl. Phys. Lett.* **49**, 1086 (1986).

11. P.J. Price, *Phys. Rev. B* **36**, 1314 (1987).

12. M. Büttiker, *IBM J. Res. Dev.* **32**, 63 (1988).

13. E. Gerjuoy and D.D. Coon, *Superlatt. Microstruct.* **5**, 305 (1989).

14. D.J. BenDaniel and C.B. Duke, *Phys. Rev.* **152**, 683 (1966).

15. R. Tsu and L. Esaki, *Appl. Phys. Lett.* **22**, 562 (1973).

16. G. Bastard, *Phys. Rev. B* **24**, 5693 (1981).

17. J.R. Söderström, E.T. Yu, M.K. Jackson, Y. Rajakarunanayake, and T.C. McGill, *J. Appl. Phys.* **68**, 1372 (1990).

18. J.N. Schulman and T.C. McGill, *Phys. Rev. B* **23**, 4149 (1981).

19. E.O. Kane, *J. Phys. Chem. Solids* **8**, 38 (1959).

20. C. Mailhiot, T.C. McGill, and J.N. Schulman, *J. Vac. Sci. Technol. B* **1**, 439 (1983).

21. J.M. Ziman, *Principles of the Theory of Solids*, 2nd ed (Cambridge, London, 1972).

22. S. Luryi, *Appl. Phys. Lett.* **47**, 490 (1985).

23. C.I. Huang, M.J. Paulus, C.A. Bozada, S.C. Dudley, K.R. Evans, C.E. Stutz, R.L. Jones, and M.E. Chaney, *Appl. Phys. Lett.* **51**, 121 (1987).

24. E.R. Brown, T.C.L.G. Sollner, C.D. Parker, W.D. Goodhue, and C.L. Chen, *Appl. Phys. Lett.* **55**, 1777 (1989).

25. S.K. Diamond, E. Ozbay, M.J.W. Rodwell, D.M. Bloom, Y.C. Pao, E. Wolak, and J.S. Harris, Jr., *IEEE Electron Devices Lett.* **10**, 104 (1989).

26. E. Ozbay and D.M. Bloom, *IEEE Electron Devices Lett.* **12**, 480 (1991).

27. P. Cheng and J.S. Harris, *Appl. Phys. Lett.* **56**, 1676 (1990).

28. V.K. Reddy, A.J. Tsao, and D.P. Neikirk, *Electron. Lett.* **26**, 1742 (1990).

29. K.L. Lear, W.S. Lee, and J.S. Harris, *IEEE Trans. Electron Devices* **36**, 2619 (1989).

30. H.M. Yoo, S.M. Goodnick, and J.R. Arthur, *Appl. Phys. Lett.* **56**, 84 (1990).

31. T. Inata, S. Muto, Y. Nakata, T. Fujii, H. Ohnishi, and S. Hiyamizu, *Jpn. J. Appl. Phys.* **25**, L983 (1986).

32. S. Sen, F. Capasso, A.L. Hutchinson, and A.Y. Cho, *Electron. Lett.* **23**, 1229 (1987).

33. A.A. Lakhani, R.C. Potter, D. Beyea, H.H. Hier, E. Hempfling, L. Aina, and J.M. O'Connor, *Electron. Lett.* **24**, 153 (1988).

34. T. Inata, S. Muto, Y. Nakata, T. Fujii, H. Ohnishi, and S. Hiyamizu, *Jpn. J. Appl. Phys.* **26**, L1332 (1987).

35. T.P.E. Broekaert, W. Lee, and C.G. Fonstad, *Appl. Phys. Lett.* **53**, 1545 (1988).

36. X.J. Song, J.B. Kuang, W.J. Schaff, P.J. Tasker, K. Yamasaki, and L.F. Eastman, *Proc. SPIE* **1288**, 136 (1990).

37. A.W. Higgs, L.L. Taylor, N. Apsley, S.J. Bass, and H.J. Hutchinson, *Electron. Lett.* **24**, 322 (1988).

38. J.R. Söderström, E.R. Brown, C.D. Parker, L.J. Mahoney, and T.C. McGill, *Appl. Phys. Lett.* **58**, 275 (1991).

39. K. Brennan and K. Hess, *Solid-State Electron.* **27**, 347 (1984).

40. E.R. Brown, S.J. Eglash, and C.L. Chen, unpublished.

41. J.R. Söderström, D.H. Chow, and T.C. McGill, *Appl. Phys. Lett.* **55**, 1094 (1989).

42. D.H. Chow, J.R. Söderström, D.A. Collins, D.Z.-Y. Ting, E.T. Yu, and T.C. McGill, *Proc. SPIE* **1283**, 2 (1990).

43. R. Beresford, L. Luo, K.F. Longenbach, and W.I. Wang, *Appl. Phys. Lett.* **56**, 551 (1990).

44. D.A. Collins, D.H. Chow, and T.C. McGill, *Appl. Phys. Lett.* **58**, 1673 (1991).

45. R. Beresford, L. Luo, and W.I. Wang, *J. Cryst. Growth* **111**, 651 (1991).

46. J.R. Söderström, J.Y. Yao, and T.G. Andersson, *Appl. Phys. Lett.* **58**, 708 (1991).

47. D.C. Houghton, H.C. Liu, D. Landheer, M. Buchanan, and M. D'Iorio, *Proc. SPIE* **943**,, 65 (1988).

48. H.C. Liu, D. Landheer, M. Buchanan, D.C. Houghton, M. D'Iorio, and S. Kechang, *Superlatt. Microstruct.* **5**, 213 (1989).

49. U. Gennser, V.P. Kesan, S.S. Iyer, T.J. Bucelot, and E.S. Yang, *J. Vac. Sci. Technol. B* **8**, 210 (1990).

50. I. Pereyra, M.P. Carreno, and F. Alvarez, *J. Non-Crystalline Solids* **110**, 175 (1989).

51. E.T. Koenig, B. Jogai, M.J. Paulus, C.I. Huang, and C.A. Bozada, *J. Appl. Phys.* **68**, 3525 (1990).

52. J.S. Wu, C.Y. Chang, C.P. Lee, K.H. Chang, and D.G. Liu, *Solid-State Electron.* **34**, 403 (1991).

53. C.B. Duke, "Tunneling in Solids," *Solid State Physics*, Suppl. to vol. 10 (Academic, New York, 1969).

54. T. Weil and B. Vinter, *Appl. Phys. Lett.* **50**, 1281 (1987).

55. T.C.L.G. Sollner, *Phys. Rev. Lett.* **59**, 1622 (1987).

56. F.W. Sheard and G.A. Toombs, *Appl. Phys. Lett.* **52**, 1228 (1988).

57. K.M.S.V. Bandara, D.D. Coon, and H. Zhao, *J. Appl. Phys.* **66**, 1227 (1989).

58. V.J. Goldman, D.C. Tsui, and J.E. Cunningham, *Phys. Rev. Lett.* **58**, 1256 (1987).

59. E.S. Alves, L. Eaves, M. Henini, O.H. Hughes, M.L. Leadbeater, F.W. Sheard, G.A. Toombs, G. Hill, and M.A. Pate, *Electron. Lett.* **24**, 1190 (1988).

60. A.V. Zaslavsky, V.J. Goldman, D.C. Tsui, and J.E. Cunningham, *Appl. Phys. Lett.* **53**, 1408 (1988).

61. H.C. Liu, M. Buchanan, G.C. Aers, Z.R. Wasilewski, W.T. Moore, R.L.S. Devine, and D. Landheer, *Phys. Rev. B* **43**, 7086 (1991).

62. M. Cahay, M. McLennan, S. Datta, and M.S. Lundstrom, *Appl. Phys. Lett.* **50**, 612 (1987).

63. W.R. Frensley, *Phys. Rev. B* **36**, 1570 (1987).

64. A. van der Ziel, *Noise in Solid State Devices and Circuits*, (Wiley, New York, 1986), Chap. 3.

65. E.R. Brown, *IEEE Trans. Electron Devices*, to be published.

66. E.E. Mendez, W.I. Wang, E. Calleja, and C.E.T. Goncalves da Silva, *Appl. Phys. Lett.* **50**, 1263 (1987).

67. P.J. Price, *Surf. Sci.* **196**, 394 (1988).

68. D. Landheer, H.C. Liu, M. Buchanan, and R. Stoner, *Appl. Phys. Lett.* **54**, 1784 (1989).

69. A.C. Marsh, *IEEE J. Quantum Electron.* **23**, 371 (1987).

70. K.V. Rousseau, K.L. Wang, and J.N. Schulman, *Appl. Phys. Lett.* **54**, 1341 (1989).

71. F. Chevoir and B. Vinter, *Appl. Phys. Lett.* **55**, 1859 (1989).

72. N.S. Wingreen, K.W. Jacobsen, and J.W. Wilkins, *Phys. Rev. Lett.* **61**, 1396 (1988).

73. J. Leo and A.H. McDonald, *Phys. Rev. Lett.* **64**, 817 (1990).

74. E.R. Brown, C.D. Parker, and T.C.L.G. Sollner, *Appl. Phys. Lett.* **54**, 934 (1989).

75. R.K. Mains and G.I. Haddad, *J. Appl. Phys.* **64**, 3564 (1988).

76. L.F. Eastman, Cornell University, private correspondence.

77. V.P. Kesan, D.P. Neikirk, B.G. Streetman, and P.A. Blakey, *IEEE Trans. Electron Devices* **35**, 405 (1988).

78. S. Luryi, *Appl. Phys. Lett.* **52**, 501 (1988).

79. E.F. Schubert, F. Capasso, A.L. Hutchinson, S. Sen, and A. Gossard, *Appl. Phys. Lett.* **57**, 2820 (1991).

80. J.P. Mattia, Master's thesis, Massachusetts Institute of Technology, 1991.

81. H.C. Liu, *Phys. Rev. B* **43**, 12538 (1991).

82. H.Y. Sheng and J. Sinkkonen, *Superlatt. Microstruct.* **9**, 537 (1991).

83. D.J. Coleman, Jr. and S.M. Sze, *Bell Syst. Tech. J.* **50**, 1695 (1971).

84. S. Sze, *Physics of Semiconductor Devices*, (Wiley, New York, 1981).

85. T.P.E. Broekaert and C.G. Fonstad, *International Electron Devices Meeting Technical Digest*, (IEEE, New York, 1989), p. 559.

86. S.K. Diamond, E. Ozbay, M.J.W. Rodwell, D.M. Bloom, Y.C. Pao, and J.S. Harris, Jr., *Appl. Phys. Lett.* **54**, 153 (1989).

87. E.R. Brown, J.R. Söderström, C.D. Parker, L.J. Mahoney, K.M. Molvar, and T.C. McGill, *Appl. Phys. Lett.* **58**, 2291 (1991).

88. J.M. Gering, D.A. Crim, D.G. Morgan, and P.D. Coleman, *J. Appl. Phys.* **61**, 271 (1987).

89. D.W. Whitson, M.J. Paulus, C.E. Stutz, E. Koenig, R. Neidhard, and K.R. Evans, *Proceedings of the IEEE/Cornell Conference*, (IEEE, New York, 1989), p. 301.

90. J.F. Whitaker, G.A. Mourou, T.C.L.G. Sollner, and W.D. Goodhue, *Appl. Phys. Lett.* **53**, 385 (1988).

91. S.K. Diamond, E. Ozbay, M.J.W. Rodwell, D.M. Bloom, Y.C. Pao, E. Wolak, and J.S. Harris, Jr., *OSA Proceedings on Picosecond Electronics and Optoelectronics*, Vol. 4 (Optical Society of America, Washington, D.C., 1989), p. 101.

92. E.R. Brown, W.D. Goodhue, and T.C.L.G. Sollner, *J. Appl. Phys.* **64**, 1519 (1988).

93. E.R. Brown, C.D. Parker, A.R Calawa, and M.J. Manfra, *IEEE Trans. Electron Devices* **38**, 2716 (1991).

94. J.M. Carroll, *Tunnel-Diode and Semiconductor Circuits*, (McGraw-Hill, New York, 1963).

95. F. Capasso, S. Sen, F. Beltram, L. Lunardi, A. Vengurlekar, P. Smith, N. Shah, R. Malik, and A. Choh, *IEEE Trans. Electron Devices* **36**, 2065 (1989).

96. T.C.L.G. Sollner, E.R. Brown, W.D. Goodhue, and H.Q. Le, *in Physics of Quantum Electron Devices*, ed. F. Capasso (Springer, New York, 1990), p. 147.

97. E.R. Brown, C.D. Parker, K.M. Molvar, and K.D. Stephan, to appear in special issue of IEEE Trans. Microwave Theory Tech. (1991).

98. A. Miura, S. Kobayashi, T. Yakihara, S. Uchida, H. Kamada, and S. Oka, *International Microwave Symposium Digest*, (IEEE, New York, 1990), p. 1845.

99. T.C.L.G. Sollner, E.R. Brown, W.D. Goodhue, and C.A. Correa, *J. Appl. Phys.* **64**, L4248 (1988).

100. R.C. Potter, D. Shupe, T.H. Kuo, and H.C. Lin, *IEEE International Symposium on Circuits and Systems*, (IEEE, New York, 1990), p. 2557.

101. T.K. Woodward and T.C. McGill, *Superlatt. Microstruct.* **4**, 1 (1988).

102. S. Sen, F. Capasso, A.Y. Cho, and D.L. Sivco, *IEEE Electron Devices Lett.* **9**, 533 (1988).

103. K. Lehovec, *IEEE J. Solid-State Circuits* **14**, 797 (1979).

104. K.L. Lear, K. Yoh, and J.S. Harris, *Proc. International Symposium GaAs and Related Compounds*, (IEEE, New York, 1989), p. 593.

105. E.R. Brown, M.A. Hollis, F.W. Smith, K.C. Wang, and P.M. Asbeck, *Proc. International Solid-State Circuits Conference*, (IEEE, New York, 1992), p. 142.

106. E.R. Brown, C.D. Parker, A.R. Calawa, M.J. Manfra, T.C.L.G. Sollner, C.L. Chen, S.W. Pang, and K.M. Molvar, Proc. SPIE **1288**, 122 (1990).

FIGURE CAPTIONS

Fig. 1. Conduction-band-bending diagram of a GaAs/AlAs DBRTD at a bias voltage corresponding to the peak of the resonant-tunneling current through the first quasibound state.

Fig. 2. First-quasibound-state lifetime in double-barrier structures made from five of the material systems discussed in the text. In each structure the quantum-well width is fixed at 4.6 nm.

Fig. 3. Room-temperature current density vs voltage curves for high-speed DBRTDs made from three different material systems.

Fig. 4. Band alignment of the type-II-staggered InAs/AlSb material system in contrast to that of the type-I InAs/AlAs system. It is assumed for simplicity that the latter system is lattice matched and that 65% of the difference between the AlAs and InAs Γ-point bandgap appears as a barrier in the conduction band.

Fig. 5. Solution to Poisson's equation in a GaAs/$Al_{0.42}Ga_{0.58}As$ DBRTD at room temperature assuming that no charge is stored in the quantum well and that there is no spatial quantization outside of the double-barrier structure.

Fig. 6. Comparison of the room-temperature experimental and theoretical I-V curves for the DBRTD in Fig. 5. The dotted lines in the NDR region represent discontinuous jumps in the current caused by switching into or out of the oscillation region shown by the solid line in the middle of the NDR region. The dashed line is a phenomenological fit that represents the expected form of the I-V curve in the absence of oscillations. The theoretical curve is based on the stationary-state model of Sec. 4.2.

Fig. 7. Theoretical I-V curves for a GaAs/$Al_{0.42}Ga_{0.58}As$ DBRTD at 77 K based on the stationary-state model with three different scattering parameters: Γ_S = 0.0, 4.0, and 20.0 meV.

Fig. 8. (a) 77-K I-V curve for the GaAs/$Al_{0.42}Ga_{0.58}As$ DBRTD having Γ_S = 4 meV.

Fig. 9. Group velocity of an electron in the Γ-valley of GaAs as computed from the theoretical band structure.

Fig. 10. Small-signal equivalent circuit of the DBRTD.

Fig. 11. Load-line diagram of a DBRTD used to compute the 10 to 90% risetime for switching from the peak point to the valley point.

Fig. 12. Cross-sectional diagram of rectangular waveguide circuit used to generate oscillations with the DBRTD up to frequencies of 712 GHz. The blowup shows a side view of a DBRTD mesa with top whisker contact.

Fig. 13. Comparison of experimental and theoretical oscillation results for two DBRTDs. The thick-barrier device has two 5.0-nm-thick $Al_{0.42}Ga_{0.58}As$ barriers and a 5.0-nm-thick GaAs quantum well. The thin barrier device has two 1.4-nm-thick AlAs barriers and a 4.5-nm-thick GaAs quantum well.

Fig. 14. Experimental oscillation results for some of the fastest DBRTDs fabricated from three different material systems.

Fig. 15. (a) Experimental I-V curve of a low-current-density DBRTD containing two 4.4-nm-thick AlAs barriers and a 5.5-nm-thick $In_{0.53}Ga_{0.47}As$ quantum well. (b) Experimental differential conductance and susceptance (imaginary part of the admittance) vs frequency for the device in (a) at a bias voltage in the PDR regoin at 1.40 V. (b) Experimental conductance and susceptance at a bias voltage in the NDR region at 1.72 V.

Fig. 16. (a) Experimental setup for electrooptically driven DBRTD switch with electooptical sampling of the resulting waveform. (b) DBRTD switching waveform measured by electrooptical sampling.

Fig. 17. Schematic diagram of technique used to measure microwave noise power of DBRTD. The dashed box contains the equivalent noise circuit.

Fig. 18. (a) Experimental 77-K I-V curve of a $GaAs/Al_{0.42}Ga_{0.58}As$ DBRTD having a 5.0-nm-thick quantum well and 5.0-nm-thick barriers. (b) Experimental shot-noise factor of DBRTD in (a) measured at a frequency of 1.0 GHz.

Fig. 19. (a) Cross-sectional view of a quasioptically stabilized DBRTD oscillator for operation in the millimeter- and submillimeter-wave regions. (b) Experimental power spectrum of quasioptically stabilized DBRTD oscillator operating at 210 GHz.

Fig. 20. (a) Simulated current waveform through a DBRTD having a perfectly antisymmetric I-V curve and driven by a sinusoidal voltage having amplitude greater than V_P. (b) Power spectrum of the current in (a) for a voltage-waveform frequency of 4.25 GHz.

Fig. 21. (a) Load line presented by a DBRTD to a heterostructure field-effect transistor. (b) Transfer characteristic of the logic-level inverter based on the load line in (a).

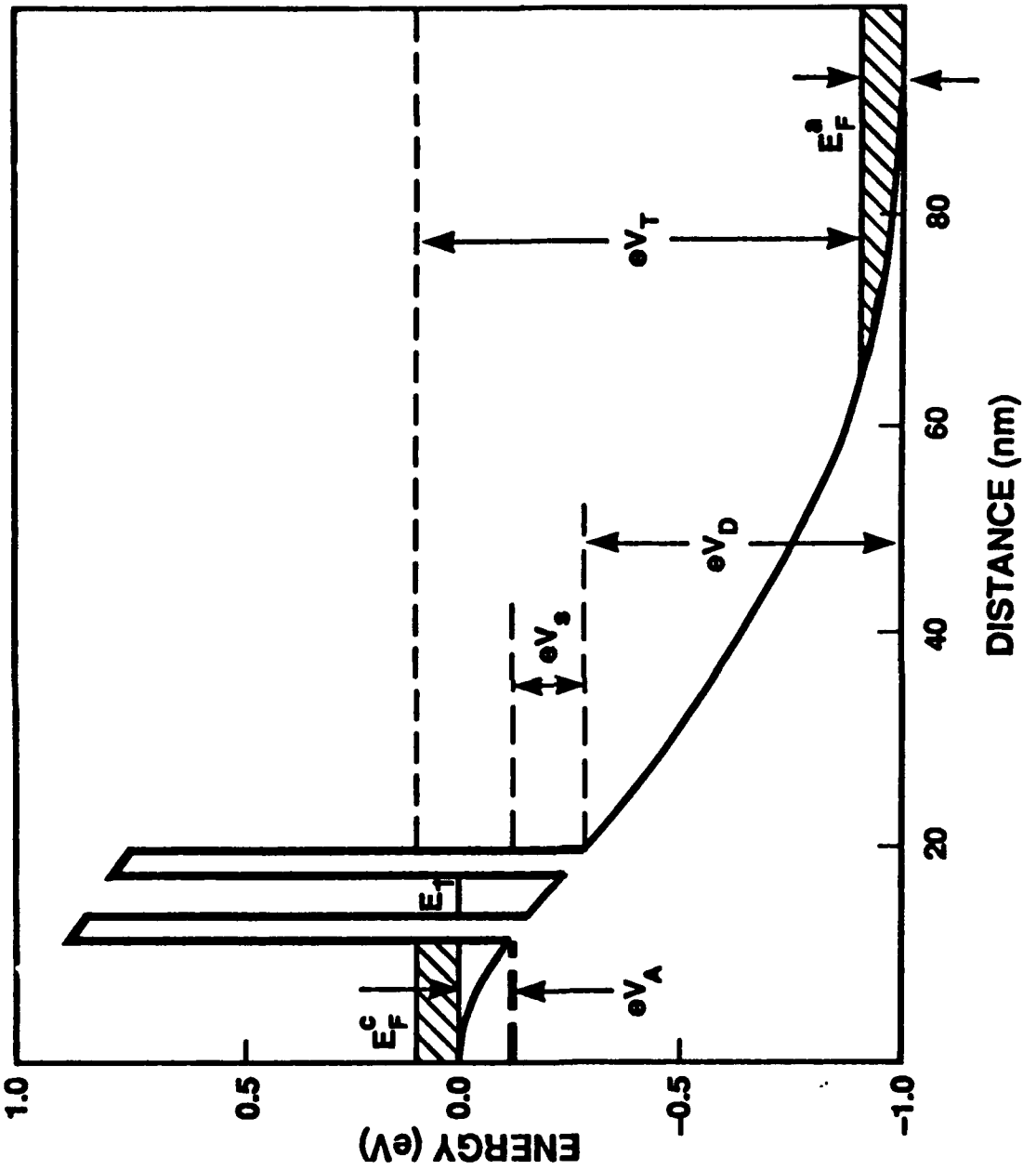

ENERGY (eV)
1.0
0.5
0.0
-0.5
-1.0
DISTANCE (nm)
20
40
60
80
E_F^a
eV_T
eV_D
eV_s
E_T
eV_A
E_F^c

FIG. 1

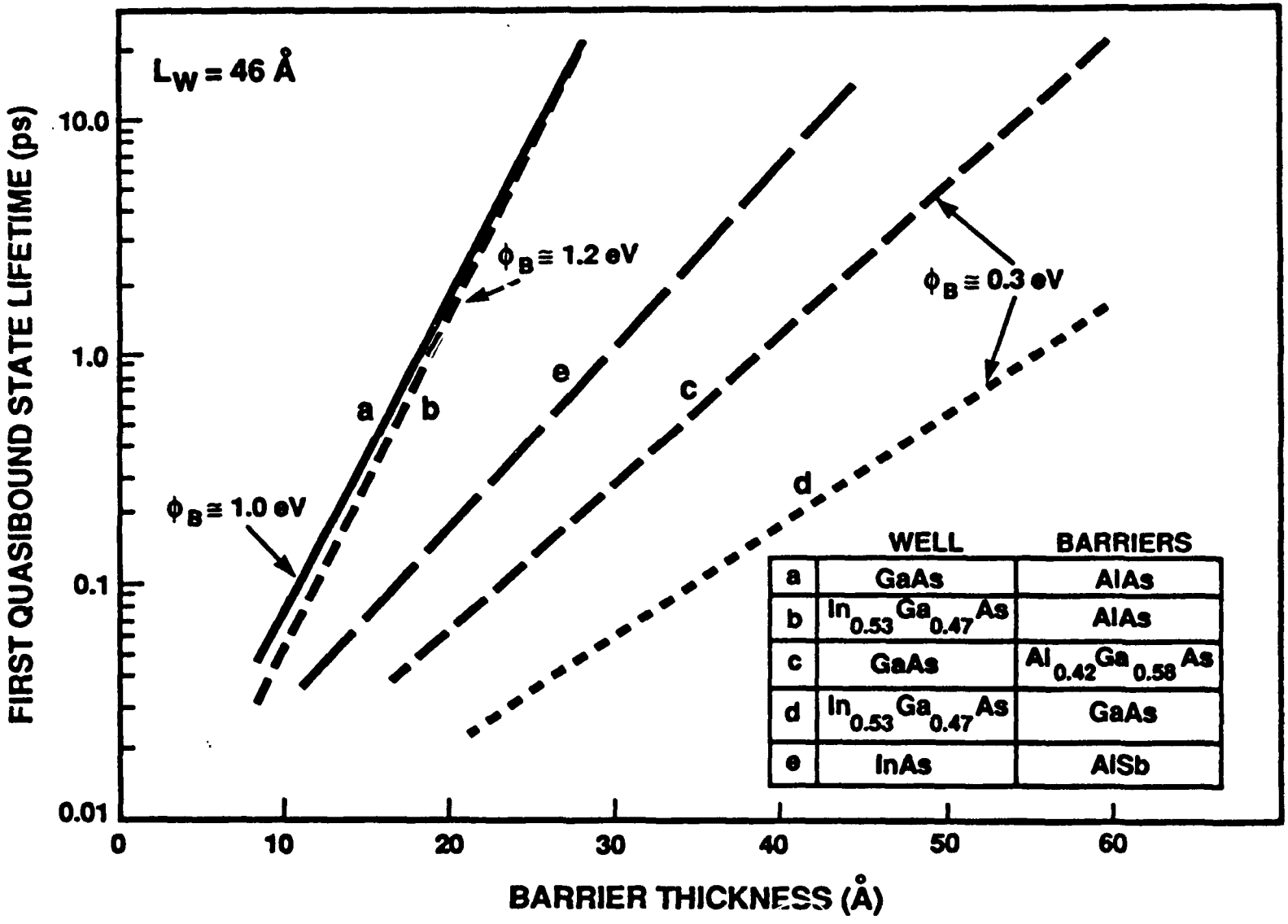

L_W = 46 Å
FIRST QUASIBOUND STATE LIFETIME (ps)
10.0
1.0
0.1
0.01
0
10
20
30
40
50
60
BARRIER THICKNESS (Å)
$\phi_B \cong 1.2$ eV
$\phi_B \cong 1.0$ eV
$\phi_B \cong 0.3$ eV
a
b
c
d
e
WELL
BARRIERS
a GaAs AlAs
b $In_{0.53}Ga_{0.47}As$ AlAs
c GaAs $Al_{0.42}Ga_{0.58}As$
d $In_{0.53}Ga_{0.47}As$ GaAs
e InAs AlSb

FIG. 2

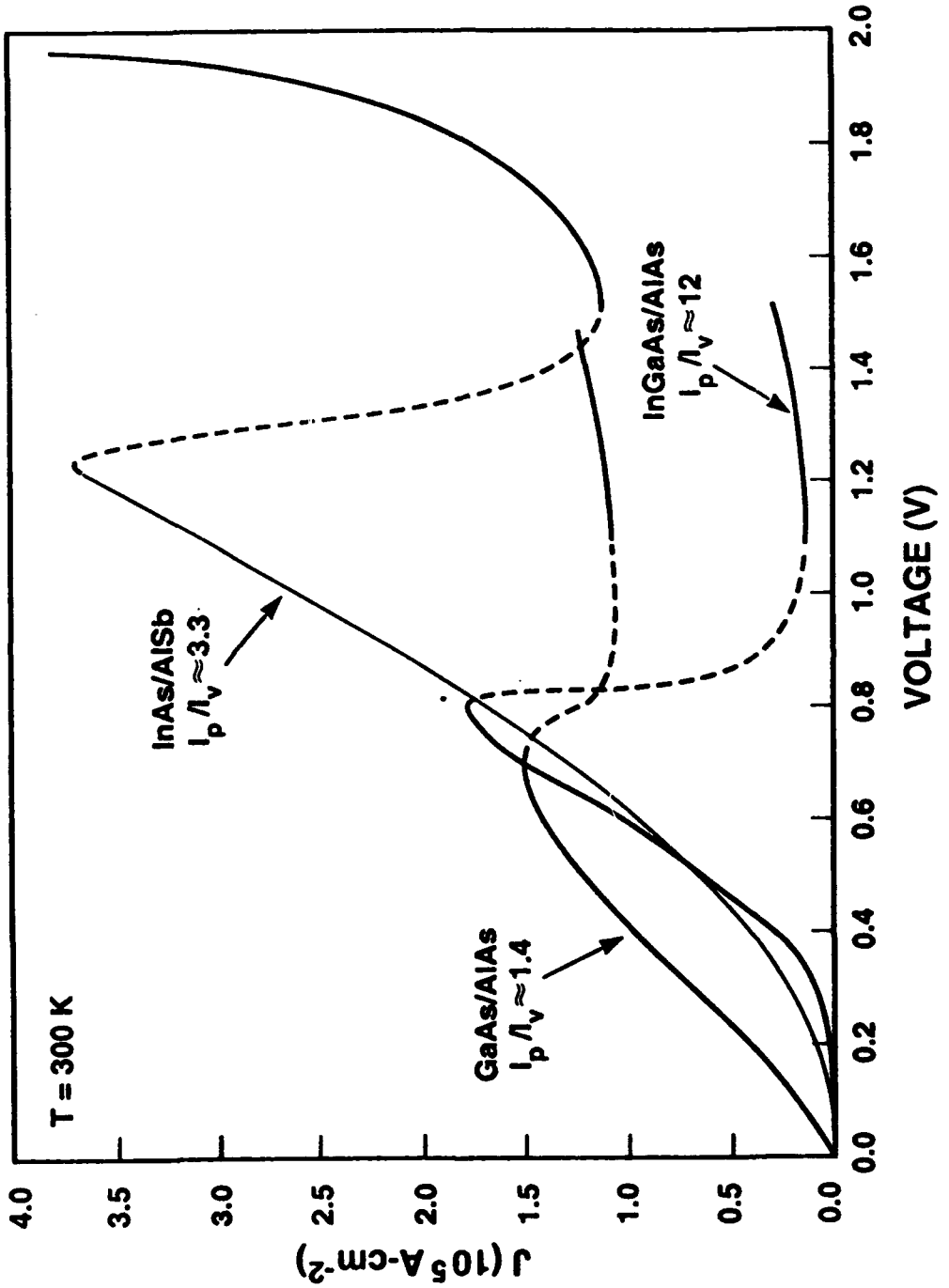

T = 300 K
InAs/AlSb
$I_p/I_v \approx 3.3$
GaAs/AlAs
$I_p/I_v \approx 1.4$
InGaAs/AlAs
$I_p/I_v \approx 12$
J (10^5 A-cm^{-2})
VOLTAGE (V)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

FIG. 3

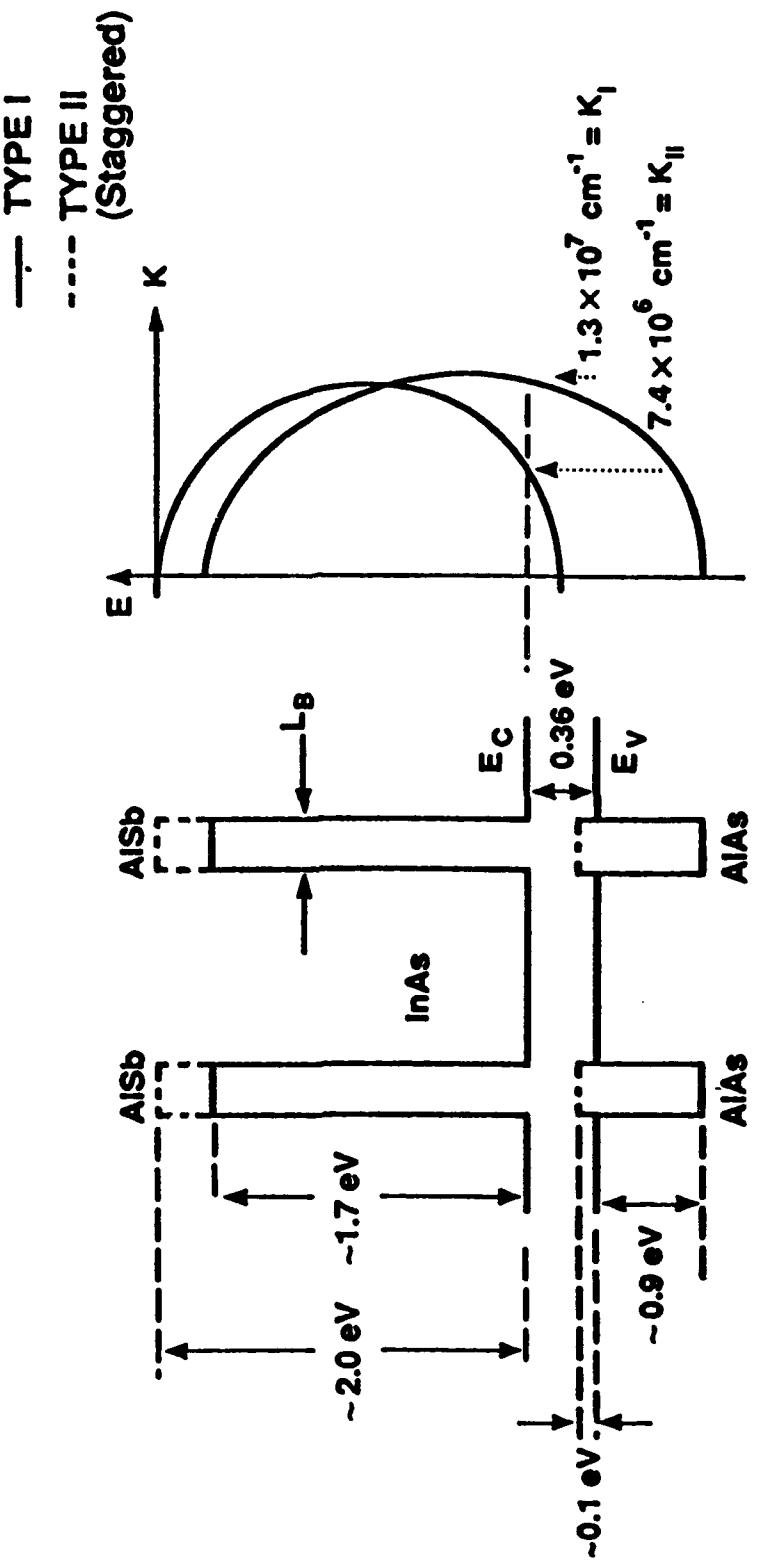

TYPE I
TYPE II
(Staggered)
K
E
1.3×10^7 cm^{-1} = K_I
7.4×10^6 cm^{-1} = K_{II}
L_B
E_C
0.36 eV
E_V
AlSb
AlAs
InAs
AlSb
AlAs
~1.7 eV
~2.0 eV
~0.9 eV
~0.1 eV

FIG. 4

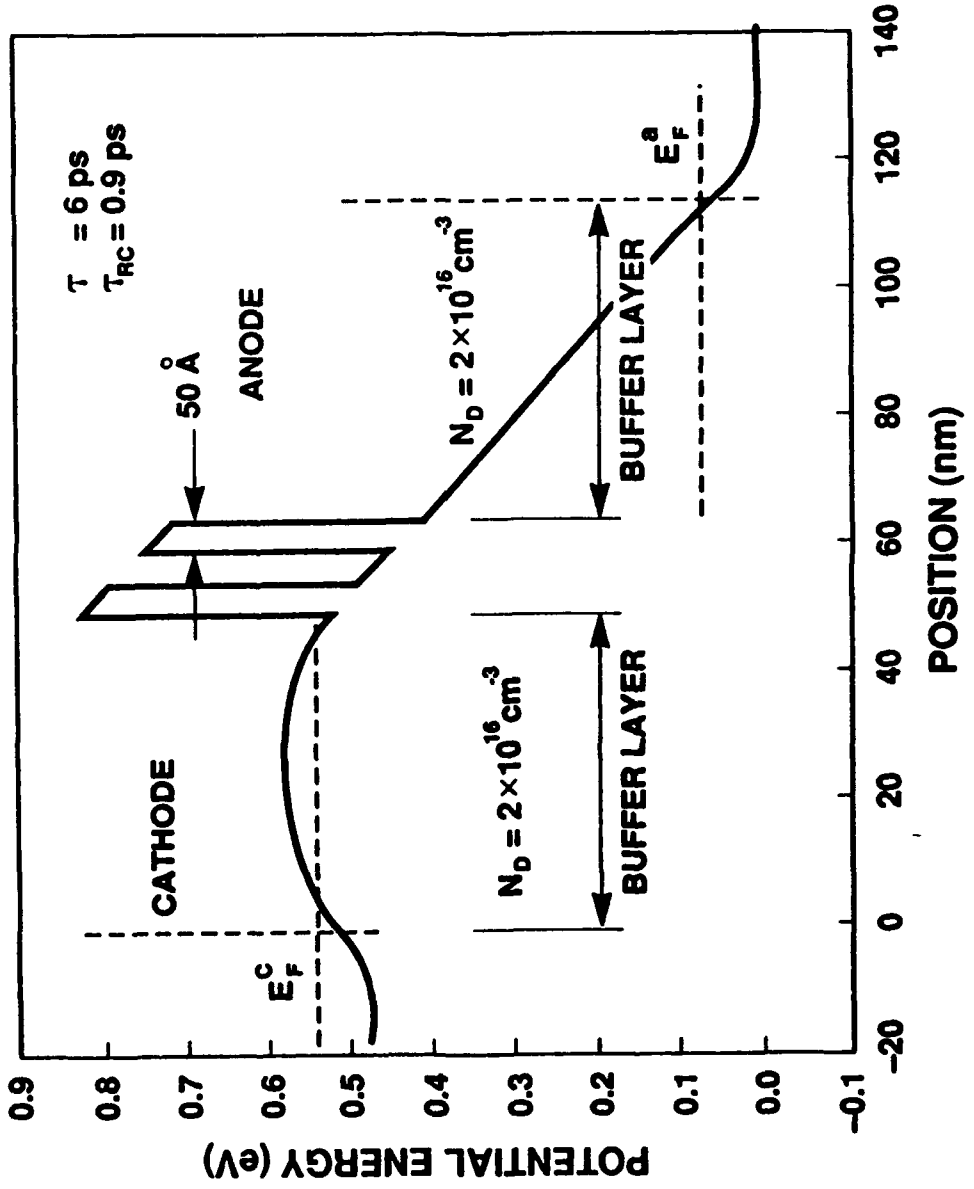

POTENTIAL ENERGY (eV)
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
POSITION (nm)
-20
0
20
40
60
80
100
120
140
CATHODE
E_F^c
$N_D = 2\times10^{16}cm^{-3}$
BUFFER LAYER
50 Å
ANODE
$N_D = 2\times10^{16}cm^{-3}$
BUFFER LAYER
E_F^a
$T = 6$ ps
$T_{RC} = 0.9$ ps

FIG. 5

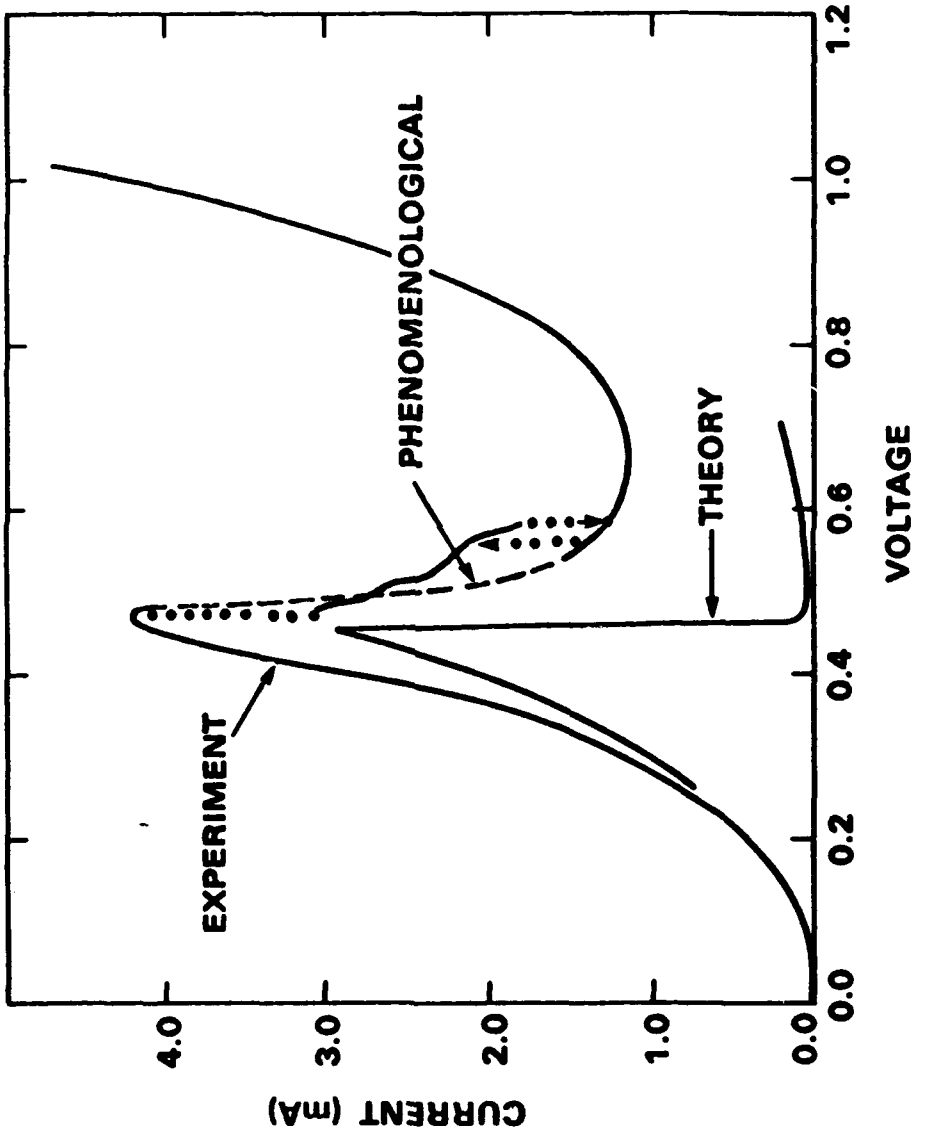

CURRENT (mA)
4.0
3.0
2.0
1.0
0.0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
VOLTAGE
EXPERIMENT
PHENOMENOLOGICAL
THEORY

FIG. 6

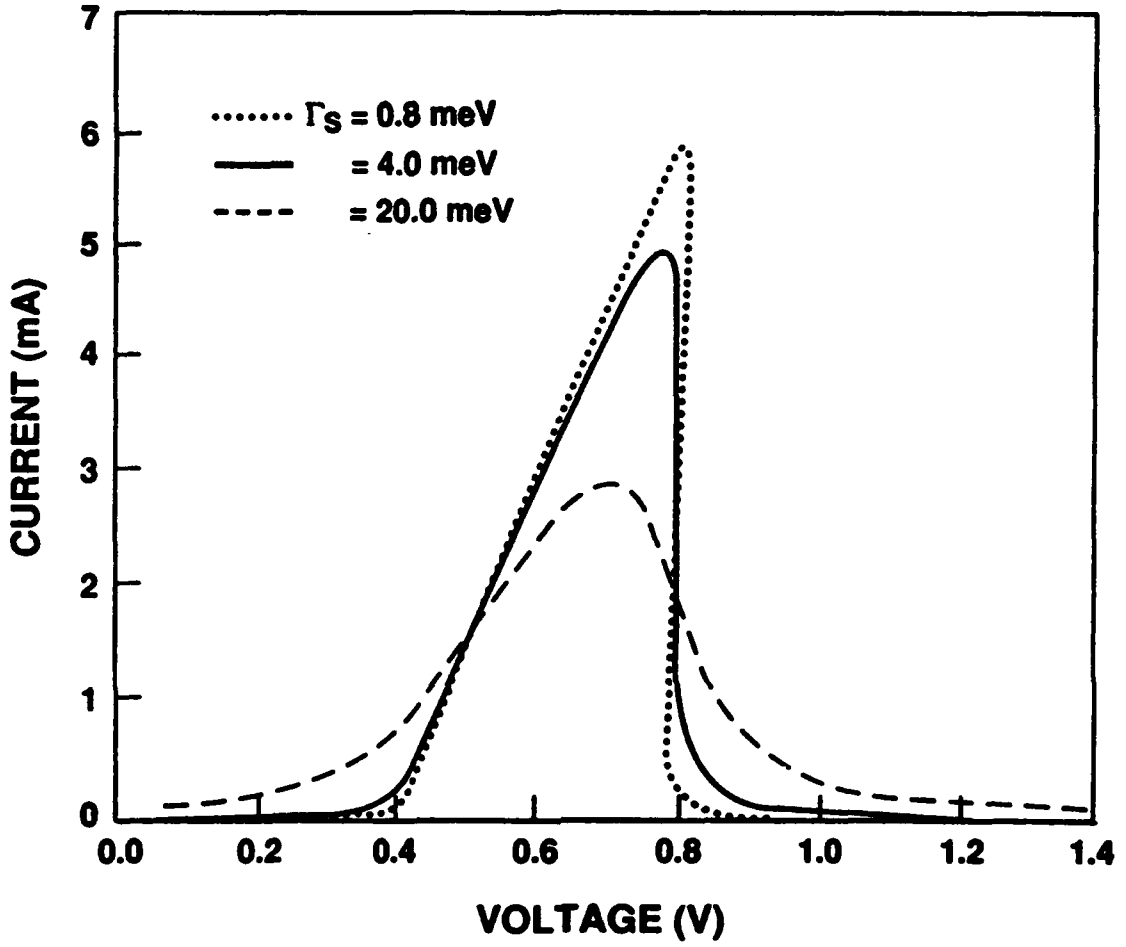

7
6
5
4
3
2
1
0
CURRENT (mA)
Γ_S = 0.8 meV
= 4.0 meV
= 20.0 meV
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
VOLTAGE (V)

FIG. 7

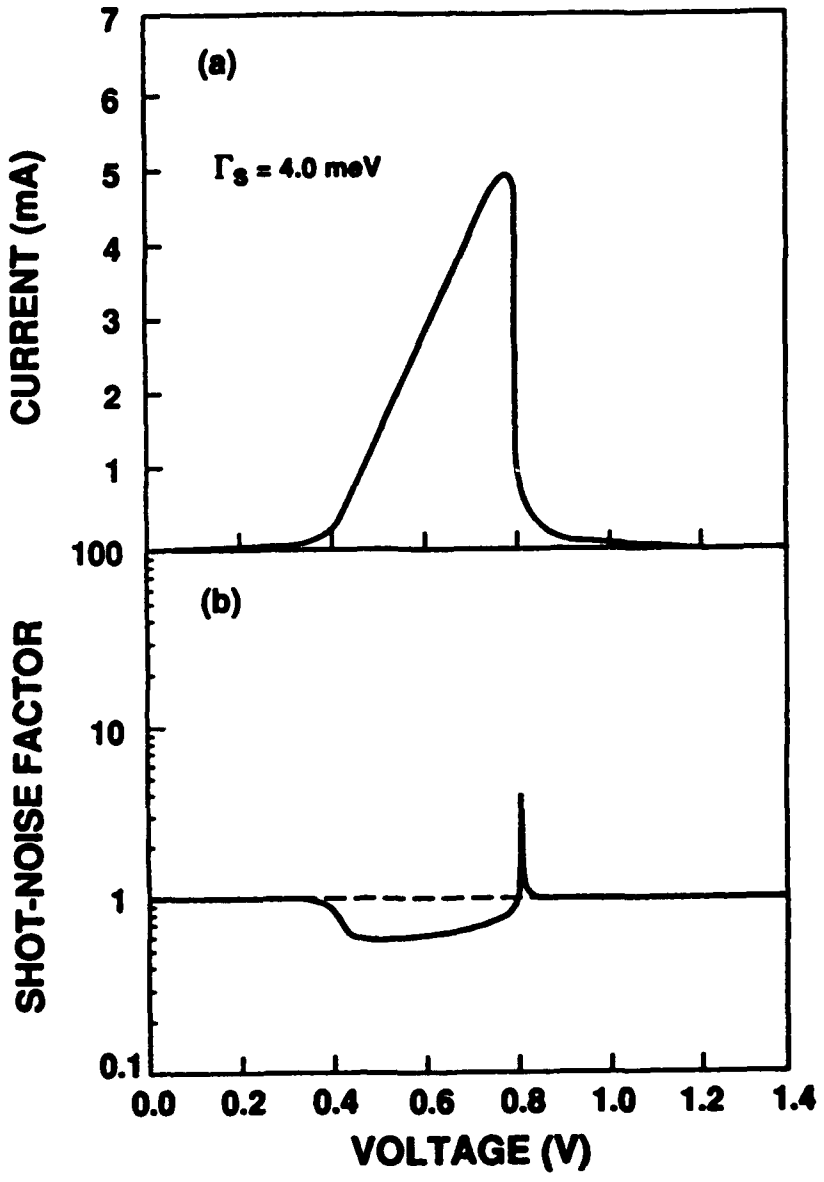

(a)
Γ_s = 4.0 meV
CURRENT (mA)
7
6
5
4
3
2
1
100
(b)
SHOT-NOISE FACTOR
10
1
0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
VOLTAGE (V)

FIG. 8

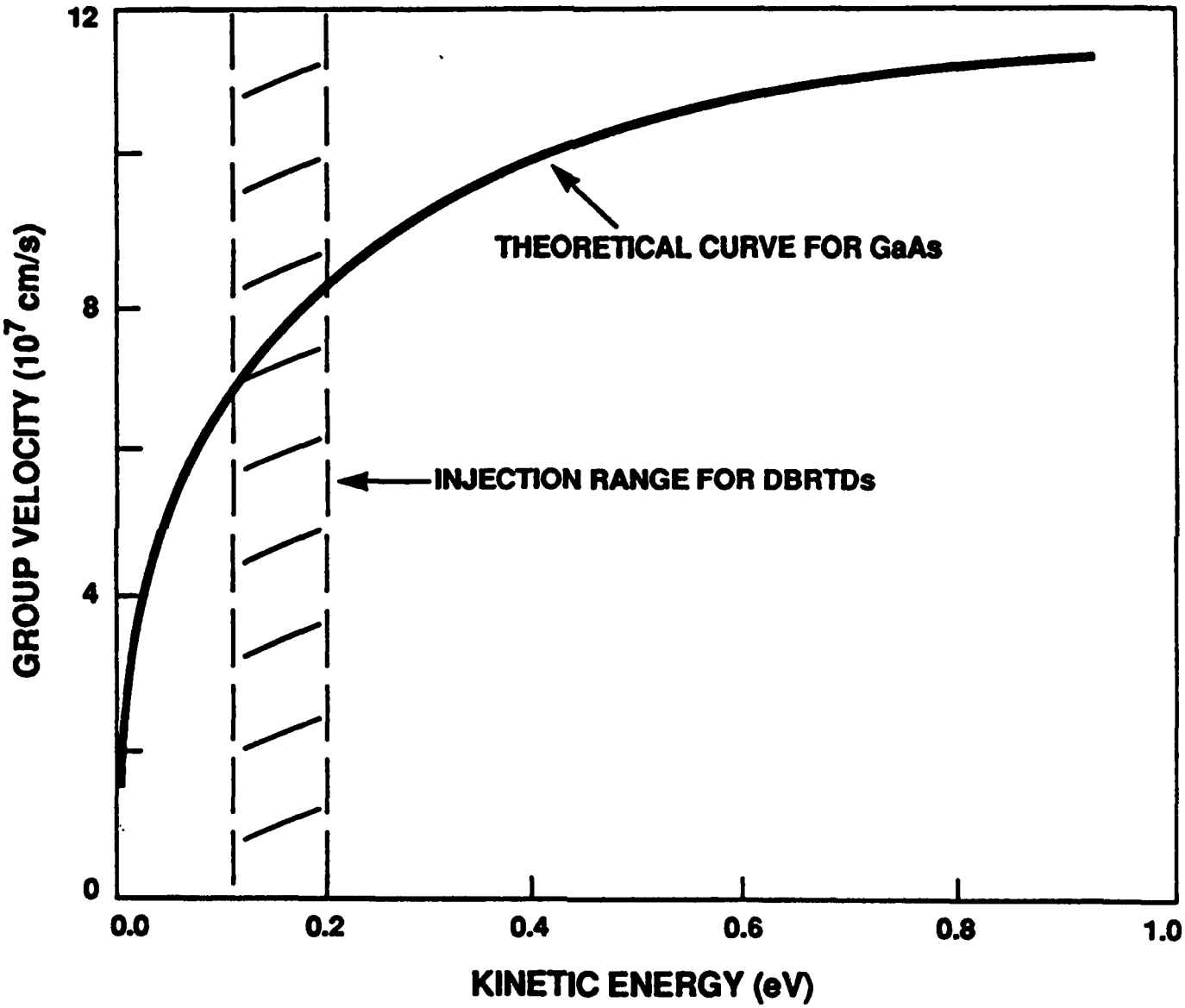

12
8
4
0
GROUP VELOCITY (10^7 cm/s)
THEORETICAL CURVE FOR GaAs
INJECTION RANGE FOR DBRTDs
0.0
0.2
0.4
0.6
0.8
1.0
KINETIC ENERGY (eV)

FIG. 9

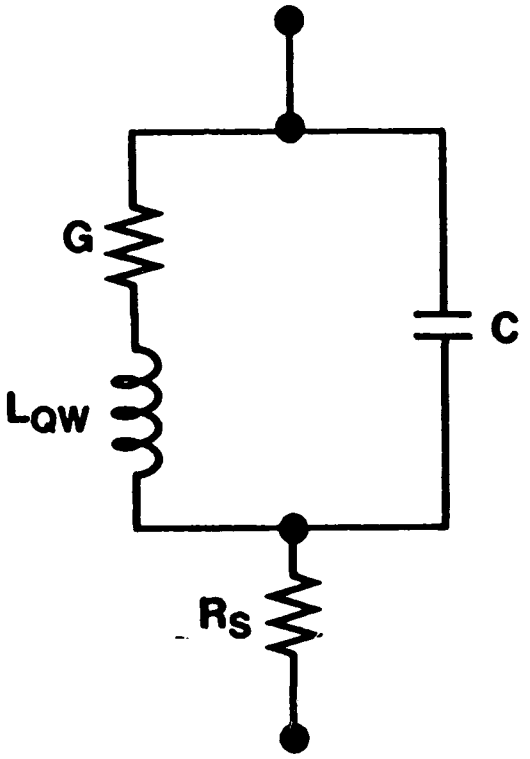


FIG. 10

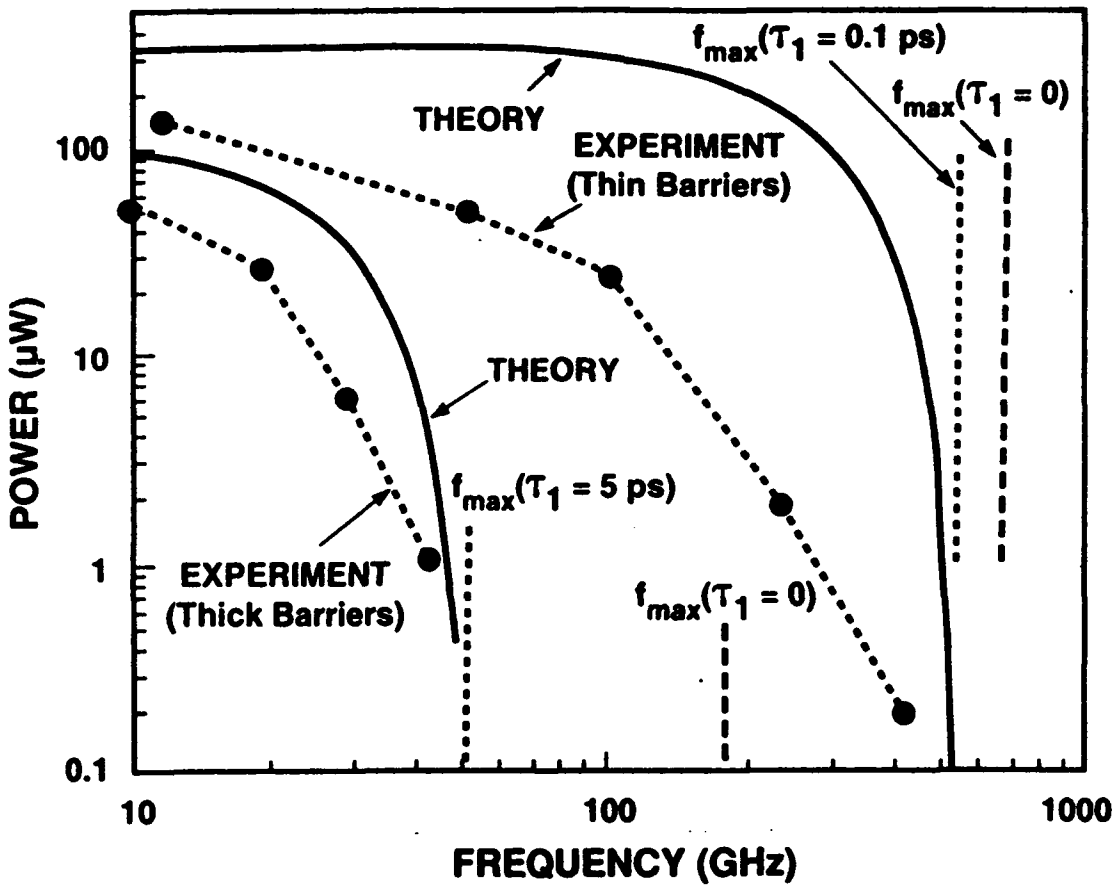

$f_{max}(\tau_1 = 0.1\ ps)$
$f_{max}(\tau_1 = 0)$
THEORY
EXPERIMENT
(Thin Barriers)
100
10
1
0.1
POWER (μW)
THEORY
$f_{max}(\tau_1 = 5\ ps)$
EXPERIMENT
(Thick Barriers)
$f_{max}(\tau_1 = 0)$
10
100
1000
FREQUENCY (GHz)

FIG. 11

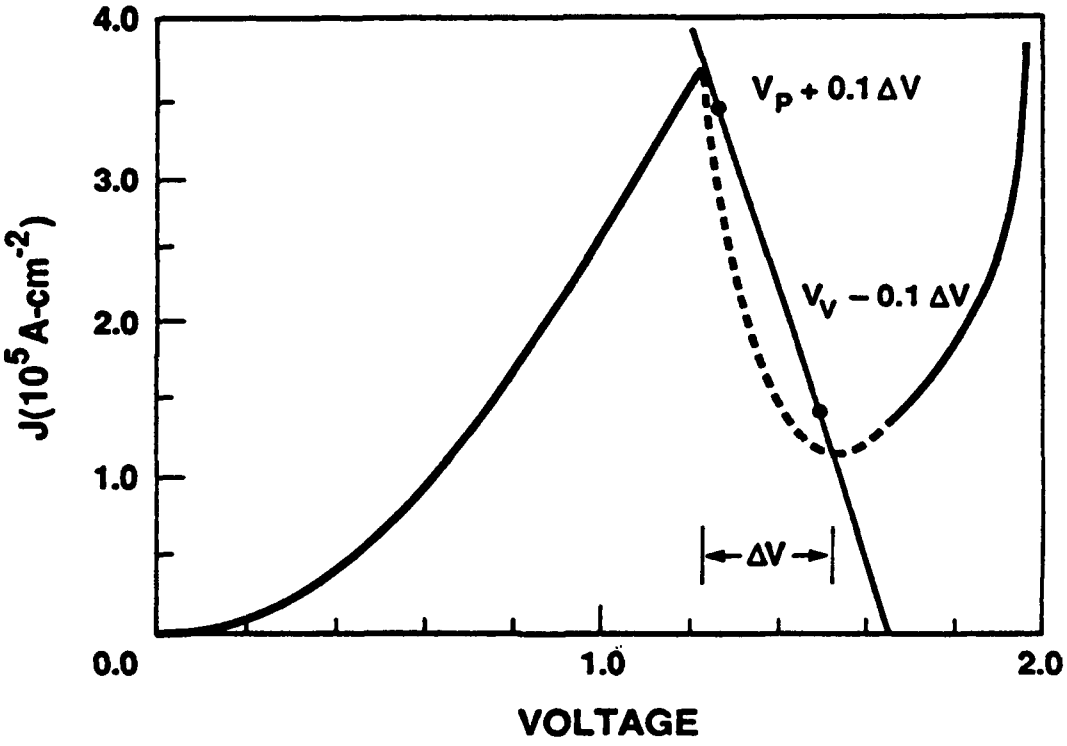


FIG. 12

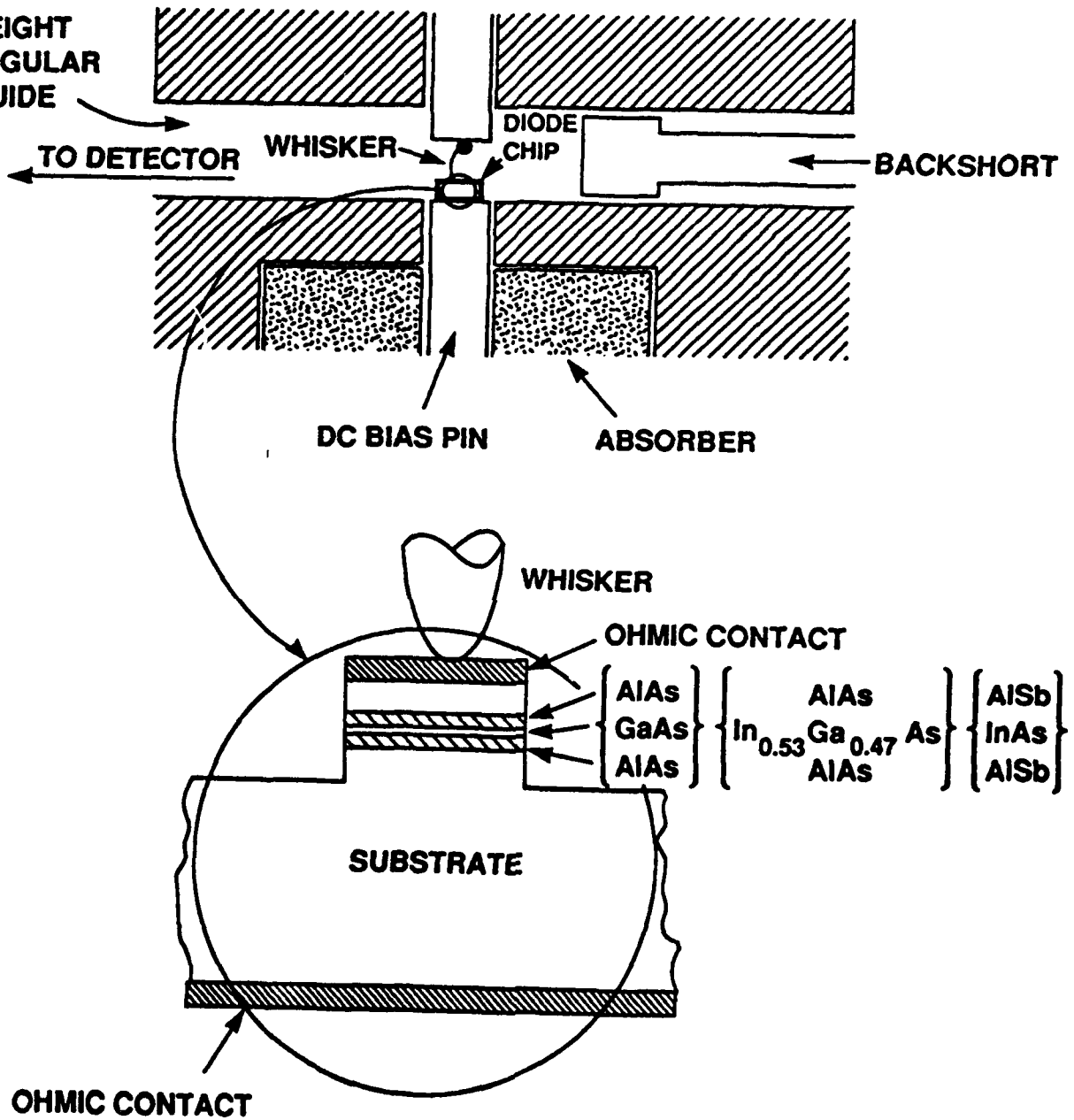

FULL-HEIGHT
RECTANGULAR
WAVEGUIDE
TO DETECTOR
WHISKER
DIODE
CHIP
BACKSHORT
DC BIAS PIN
ABSORBER
WHISKER
OHMIC CONTACT
AlAs
GaAs
AlAs
AlAs
$In_{0.53}Ga_{0.47}As$
AlAs
AlSb
InAs
AlSb
SUBSTRATE
OHMIC CONTACT

FIG. 13

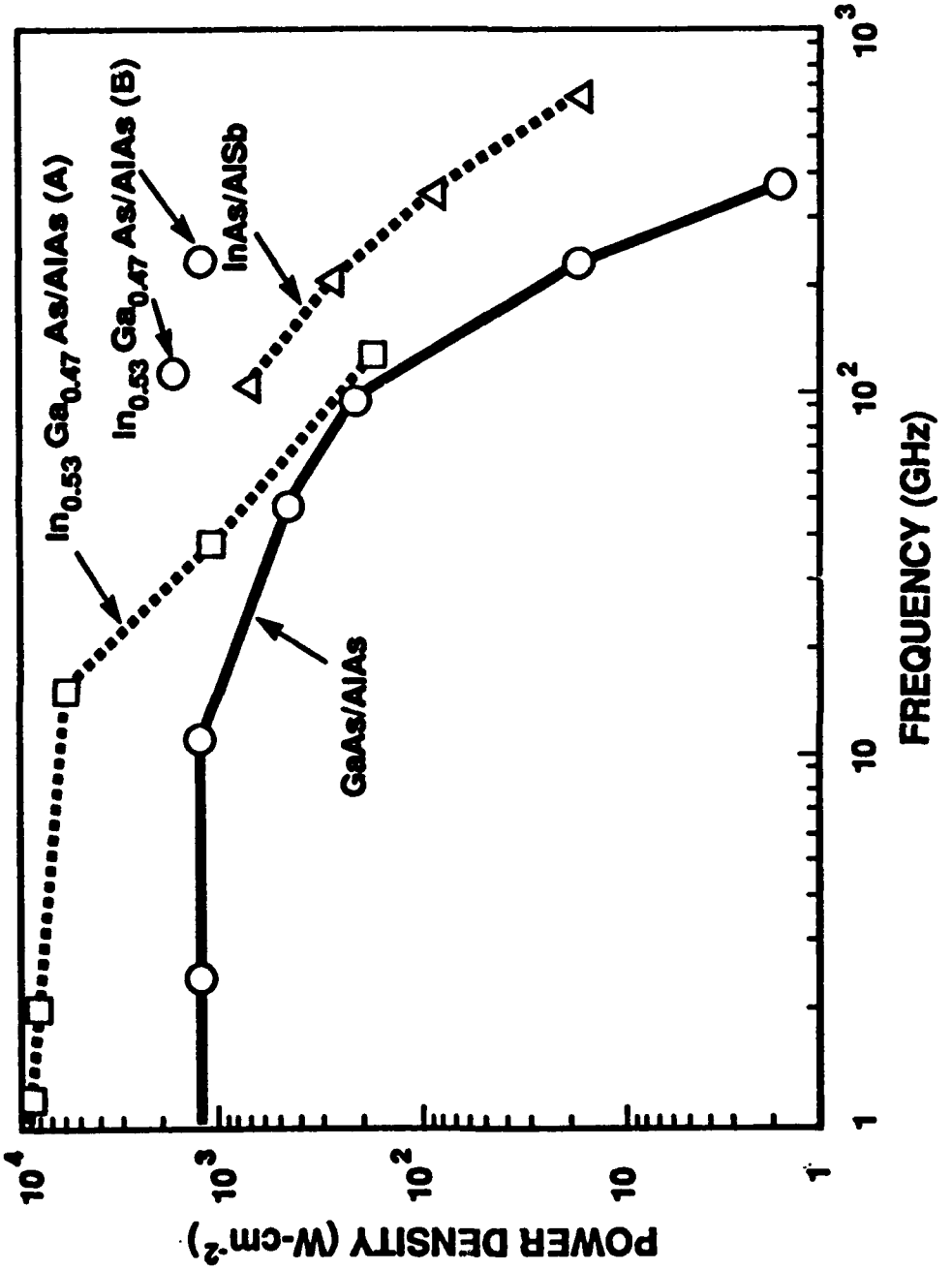
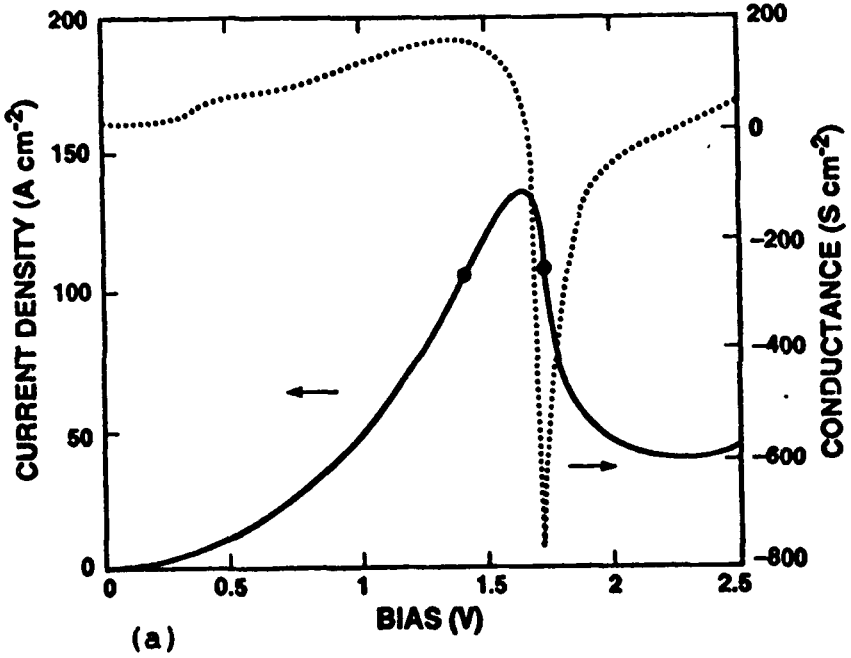

$In_{0.53}Ga_{0.47}As/AlAs$ (A)
$In_{0.53}Ga_{0.47}As/AlAs$ (B)
InAs/AlSb
GaAs/AlAs
POWER DENSITY (W-cm^{-2})
FREQUENCY (GHz)
10^4
10^3
10^2
10
1
10^3
10^2
10
1

FIG. 14


CURRENT DENSITY (A cm-2)
CONDUCTANCE (S cm-2)
BIAS (V)
(a)

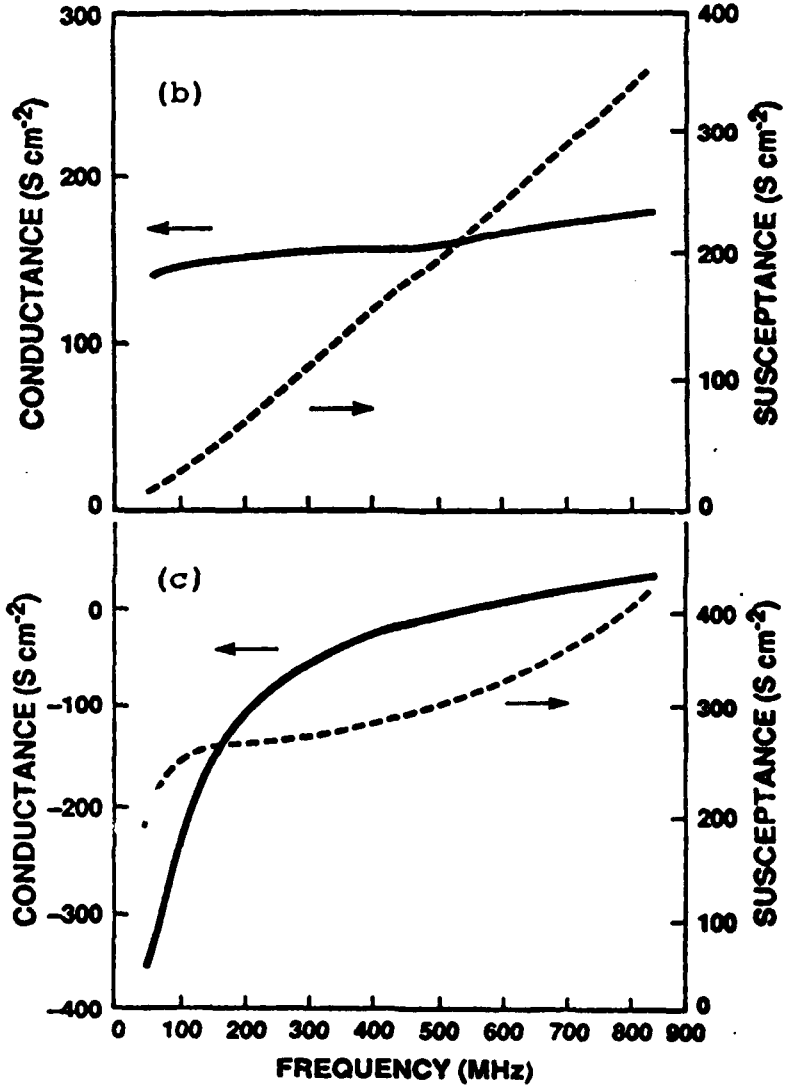
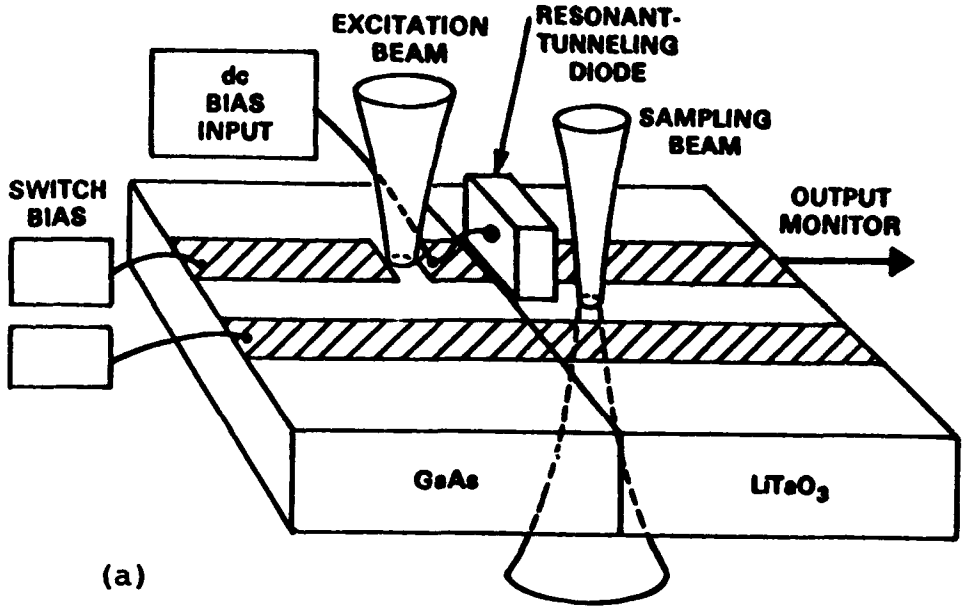
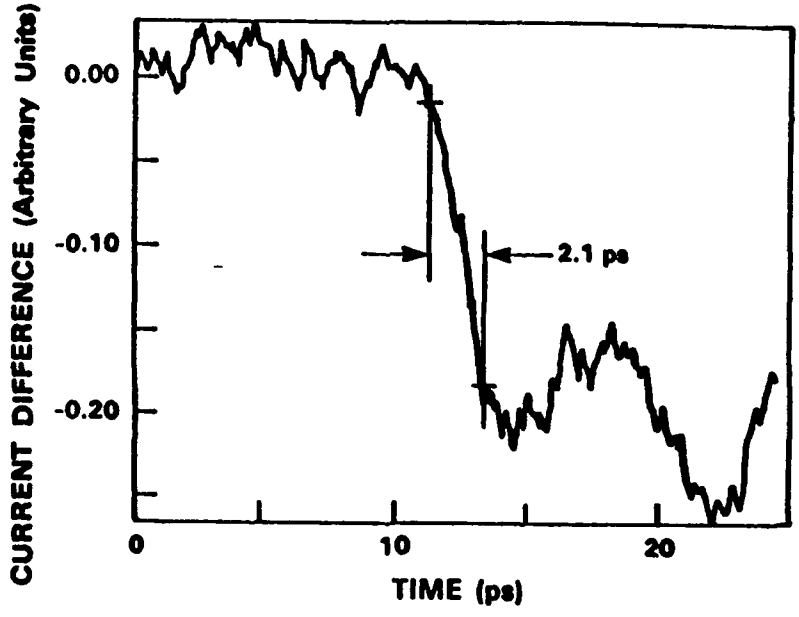

(b)
(c)
CONDUCTANCE (S cm-2)
SUSCEPTANCE (S cm-2)
FREQUENCY (MHz)

FIG. 15


EXCITATION BEAM
RESONANT-TUNNELING DIODE
dc BIAS INPUT
SAMPLING BEAM
SWITCH BIAS
OUTPUT MONITOR
GaAs
$LiTaO_3$

(a)


CURRENT DIFFERENCE (Arbitrary Units)
0.00
-0.10
-0.20
2.1 ps
0
10
20
TIME (ps)

(b)

FIG. 16

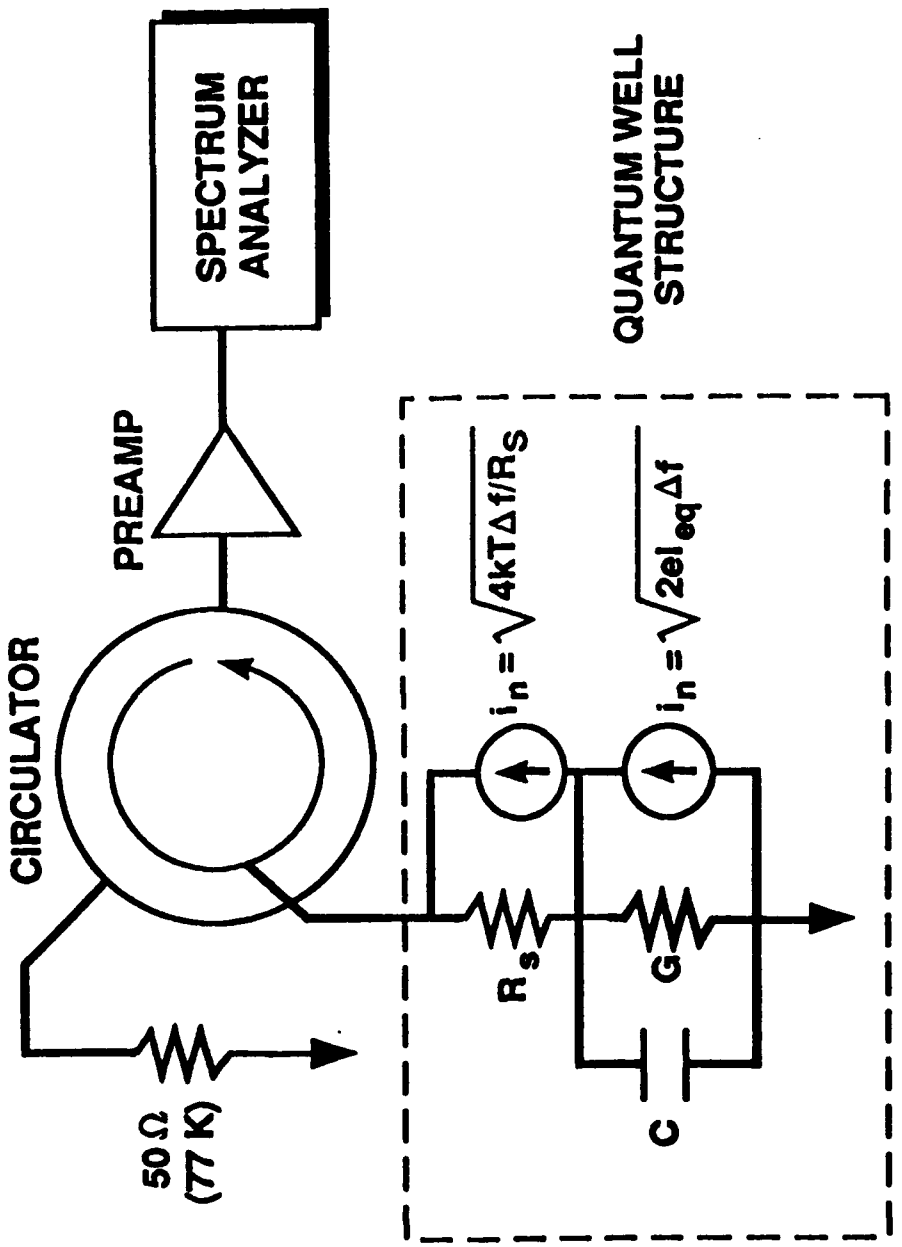

SPECTRUM ANALYZER
PREAMP
CIRCULATOR
50 Ω (77 K)
QUANTUM WELL STRUCTURE
$i_n = \sqrt{4kT\Delta f/R_S}$
$i_n = \sqrt{2eI_{eq}\Delta f}$
R_s
G
C

FIG. 17

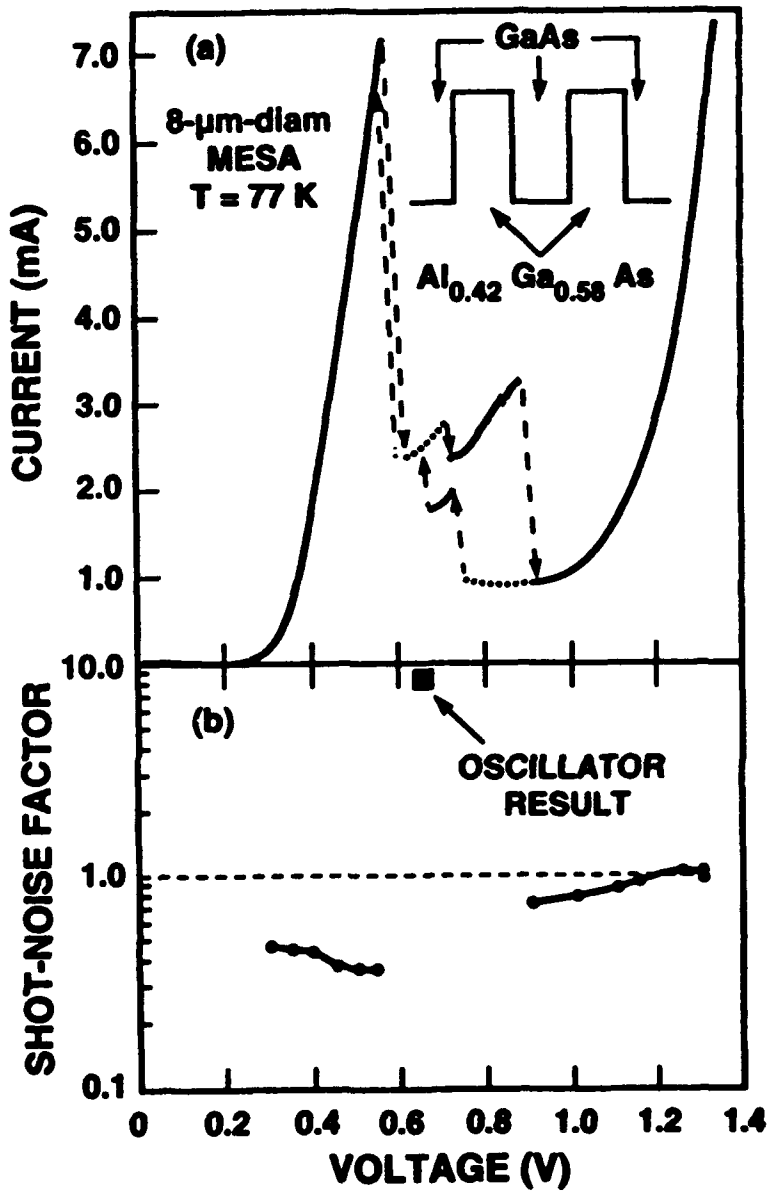
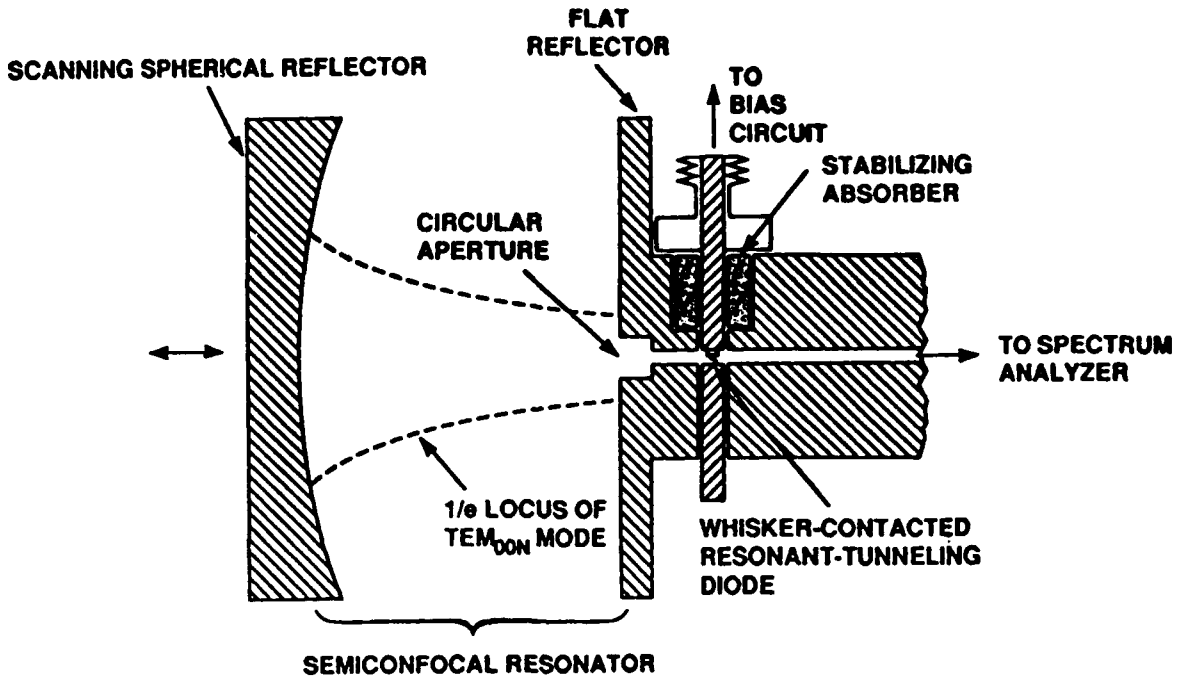
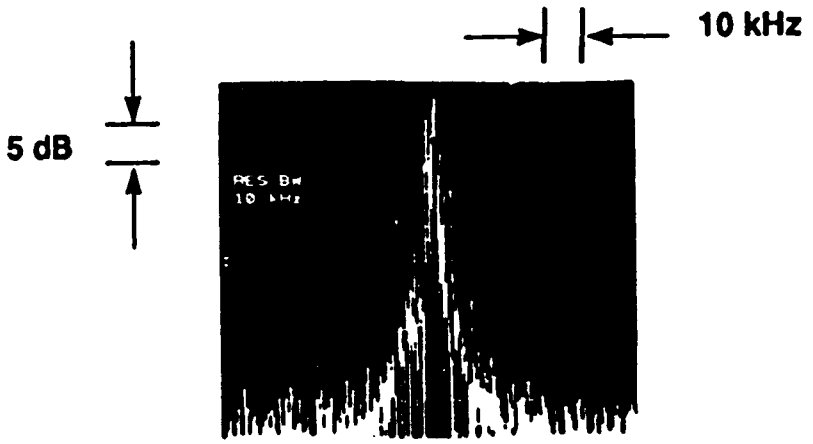

(a)
8-μm-diam
MESA
T = 77 K
GaAs
$Al_{0.42}Ga_{0.58}As$
CURRENT (mA)
7.0
6.0
5.0
4.0
3.0
2.0
1.0
(b)
OSCILLATOR
RESULT
SHOT-NOISE FACTOR
10.0
1.0
0.1
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
VOLTAGE (V)

FIG. 18

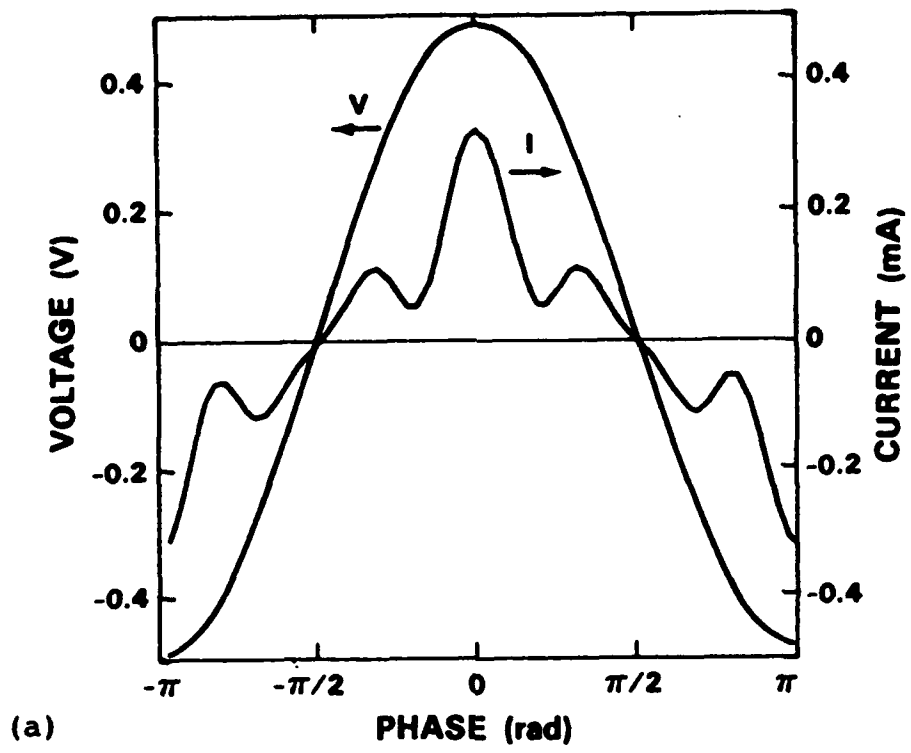

SCANNING SPHERICAL REFLECTOR
FLAT REFLECTOR
TO BIAS CIRCUIT
STABILIZING ABSORBER
CIRCULAR APERTURE
TO SPECTRUM ANALYZER
1/e LOCUS OF TEM00N MODE
WHISKER-CONTACTED RESONANT-TUNNELING DIODE
SEMICONFOCAL RESONATOR

(a)

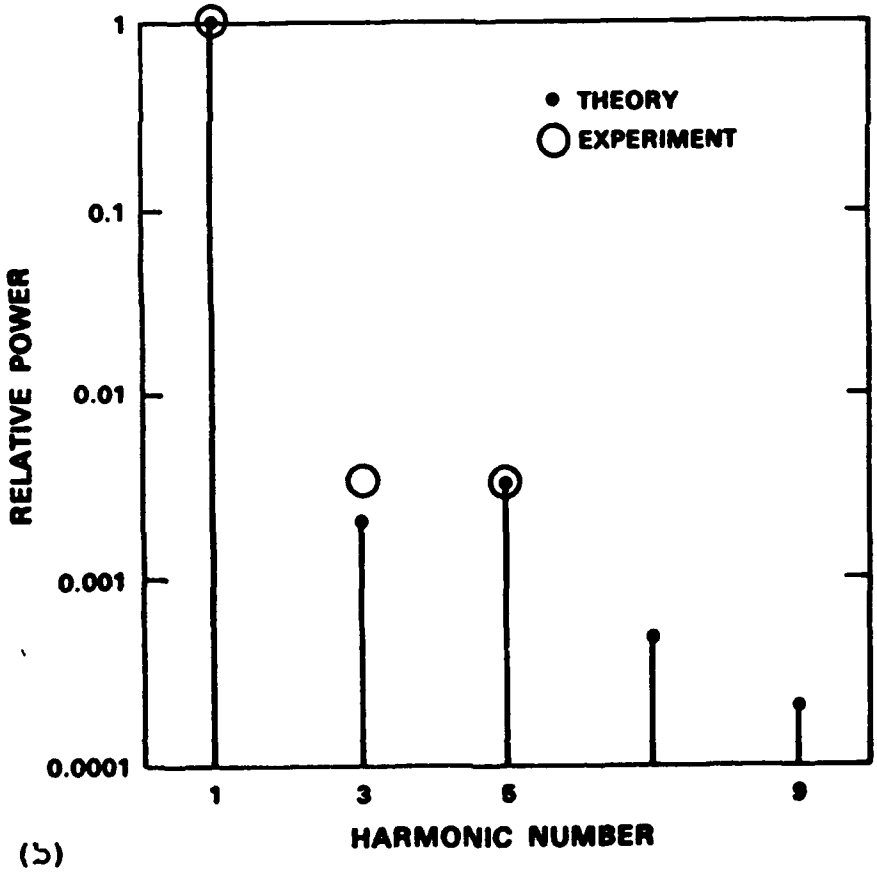

10 kHz
5 dB
RES BW
10 kHz

(b)

FIG. 19

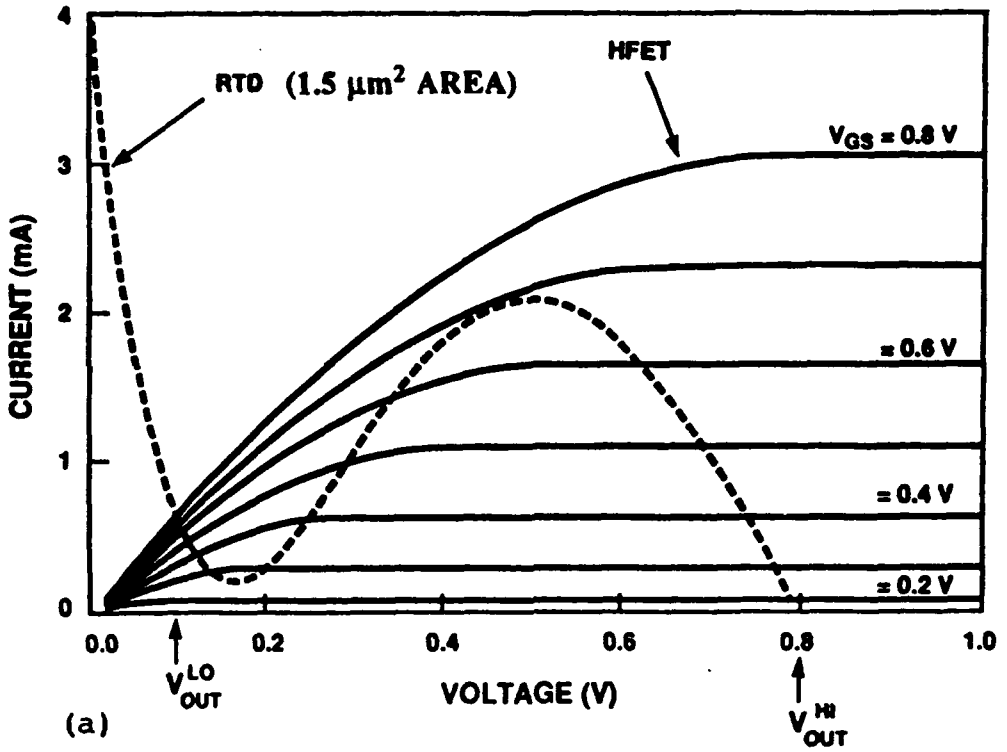

0.4
0.2
0
-0.2
-0.4
V
I
VOLTAGE (V)
CURRENT (mA)
-π
-π/2
0
π/2
π
PHASE (rad)

(a)

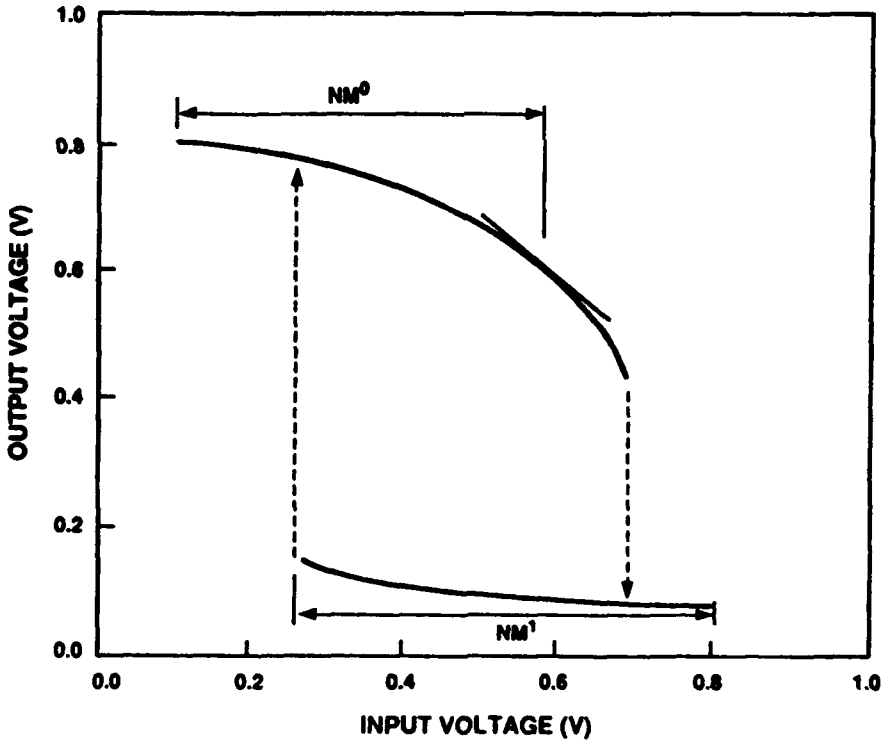

1
0.1
0.01
0.001
0.0001
RELATIVE POWER
THEORY
EXPERIMENT
1
3
5
9
HARMONIC NUMBER

(b)

FIG. 20


RTD (1.5 μm² AREA)
HFET
V_{GS} = 0.8 V
= 0.6 V
= 0.4 V
= 0.2 V
CURRENT (mA)
VOLTAGE (V)
V_{OUT}^{LO}
V_{OUT}^{HI}
0
1
2
3
4
0.0
0.2
0.4
0.6
0.8
1.0

(a)


NM^0
NM^1
OUTPUT VOLTAGE (V)
INPUT VOLTAGE (V)
0.0
0.2
0.4
0.6
0.8
1.0

(b)

FIG. 21

TABLE I. Theoretical oscillator characteristics for DBRTDs

J_p (A cm^{-2})	G/A (mS μm^{-2})	C/A (fF μm^{-2})	τ_1 (ps)	f_{max} (GHz)	Reference
		$In_{0.53}Ga_{0.47}As/AlAs$			
2.5×10^5	-11	1.3	0.2	932	[106]
5.0×10^5	-15	1.5	0.1	1280	[85]
		GaAs/AlAs			
1.5×10^5	-6	1.5	0.1	555	[24]
1.3×10^5	-5	1.3	0.3	468	[25]

TABLE II. Theoretical Switching Time for DBRTDs

J_P (A cm^{-2})	$J_P - J_V$ (A cm^{-2})	$V_V - V_P$ (V)	S (10^{12} V s^{-1})	t_R (ps)	Reference
		$In_{0.53}Ga_{0.47}As/AlAs$			
2.5×10^5	2.2×10^5	0.60	1.7	1.5	[106]
5.0×10^5	3.3×10^5	0.25	2.2	0.5	[85]
		GaAs/AlAs			
1.5×10^5	4.3×10^4	0.30	0.29	4.5	[24]
1.3×10^5	7.8×10^4	0.40	0.60	2.9	[25]