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SILICON NEURON

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Many researchers have developed neural architectures based on extremely simplified models of neurons. Recently, researchers have developed an analog electronic model of a neuron that more accurately reproduces its biological counterpart. This electronic neuron was designed to emulate the ionic currents present in biological neurons. Based on this neural model, we designed and fabricated an eight input neuron on a 2mm by 2mm 40 pin VLSI (very large scale integrated) chip. This neuron had four excitatory and four inhibitory inputs and was approximately 330 microns by 330 microns in size. In this report I describe how the neuron operates, some of the specifics of our design, our testing procedures, and the results of our tests.

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PREFACE

The work described in this report was authorized under Contract No. DAAD05-91-P6564, Silicon Neuron. This work was started in September 1991 and completed in June 1992.

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1. INTRODUCTION

Many researchers have developed neural architectures based on extremely simplified models of neurons. Recently, researchers have developed an analog electronic model of a neuron that more accurately reproduces its biological counterpart[1]. This electronic neuron was designed to emulate the ionic currents present in biological neurons. Based on this neural model we designed and fabricated an eight input neuron on a 2mm by 2mm 40 pin VLSI (very large scale integrated) chip. This neuron had four excitatory and four inhibitory inputs and was approximately 330 microns by 330 microns in size. In this paper I will describe how the neuron operates, some of the specifics of our design, our testing procedures, and the results of our tests. I will then conclude by describing some future directions of this research.

2. BIOLOGICAL NEURONS

In order to understand how the electronic neuron operates you must first understand some of the basic mechanisms involved in the operation of biological neurons[2]. The most basic components of a neuron are the dendrites, soma, and axon (see Figure 1). Neural structures often exist as layers of interconnected neurons. The dendrites of the neurons in layer i are normally connected to the axons of the neurons in layer i-1 and the axon of the neurons in layer i are normally connected to the dendrites of the neurons in layer i+1. The dendrites are the inputs to the neuron and the axon is the output. Interconnections between neurons are called synapses and can either be excitatory or inhibitory. The axon and dendrites are essentially tubes made out of phospholipids and proteins (just like any other cell wall). The signals carried by the axon and dendrites are represented by ionic currents flowing through the tubes. The soma is the body of the neuron and is the location where all the excitatory and inhibitory currents are summed. Along the wall of the axon are voltage controlled sodium (Na^+) and potassium (K^+) gates. These gates act in combination to produce a voltage spike which travels down the axon to excite or inhibit other neurons. The frequency with which these action potentials are created is related to the intensity of the input signals.

As I alluded to above, the action potential, i.e. the output signal, is formed by a combination of voltage controlled Na^+ and K^+ gates. In order to understand there effect you must first realize that all cells, including neurons, are bathed in a sea of salt water. This water, or extracellular fluid, has a Na^+ concentration that is higher than the intracellular fluid (water inside the cell) but a K^+ concentration that is lower. Nature has miraculously managed to exploit this fact by "designing" the following system of Na^+ and K^+ gates (which are made out of protein). As the voltage in the soma increases above threshold, where the threshold voltage is that voltage required to open the Na^+ gates, the Na^+ gates begin to open. As these gates open Na^+ starts to enter the axon (via its electro-chemical gradient) thus further increasing the voltage. This process continues until the voltage inside the cell reaches the upper threshold and the Na^+ gates close. Meanwhile, the slower acting K^+ gates are beginning to open and K^+ is starting to leave the cell (via its electro-chemical gradient). This causes the potential to decrease until it is again below threshold and at its original resting level. As the Na^+ ions, which are now inside the cell, diffuse down the

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1 Mahowald, M., Douglas, R., "A Silicon Neuron," Nature Vol. 354, pp 515-518 (1991).

2 Patton, H.D., Fuchs, A.F., Hille, B., Scher, A.M., Steiner, R., Textbook of Physiology, Vol. 1, 21st ed.,W.B. Saunders Company, Philadelphia, PA, 1989.

length of the axon they increase the potential at this new location thus causing the same reaction to occur there. It is in this way that the action potential is propagated along the axon. This process will repeat so long as the net input increases the potential inside the soma.

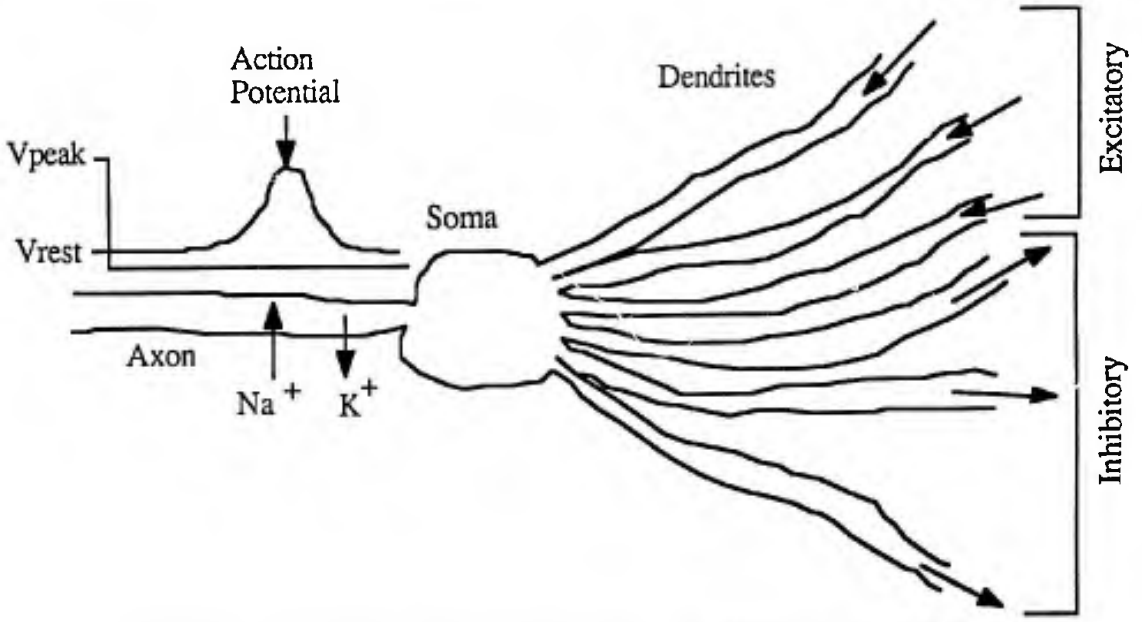

Figure 1. Diagrammatic representation of a neuron. The arrows to the right of the dendrites represent the flow of ions in the dendrites. The dendrites and axon are normally connected to other neurons. The graph above the axon shows the voltage along the axon.

3. BASIC TRANSISTOR OPERATION

There are many types of transistors but the type most often used today are complimentary metal-oxide semiconductor field effect transistors (CMOS FET's). In this paper, unless otherwise stated, when I refer to transistors I am specifically referring to CMOS FET's. CMOS FET's come in two varieties, p-channel and n-channel (see Figure 2). On any given chip, both types are usually used. The difference between the two is a matter of how they are fabricated and, for normal transistor operation, Vgs and Vds are negative for the p-channel transistor and positive for the n-channel. Both types are used because the p-channel is a good current source and the n-channel in a good current sink.

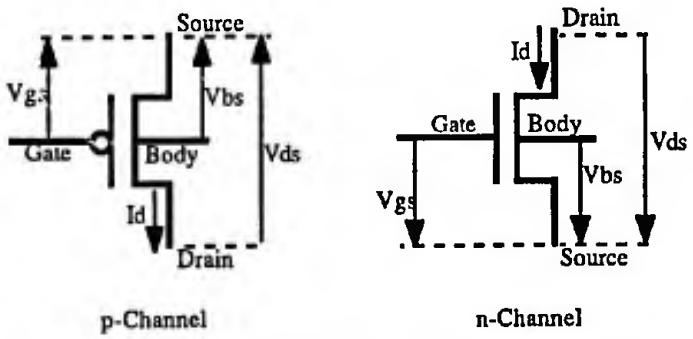

Figure 2. Schematic diagrams of p- and n-channel transistors. The source and drain assignments follow the convention that voltages decrease from top to bottom.

The current / voltage characteristics of both the n- and p-channel devices are qualitatively the same and will only be discussed for the n-channel device. For analog VLSI implementations the transistors are operated subthreshold in the saturation region (see Figure 3).The current / voltage characteristics of transistors operated in this region are remarkably analogous to those of biological neurons[3].

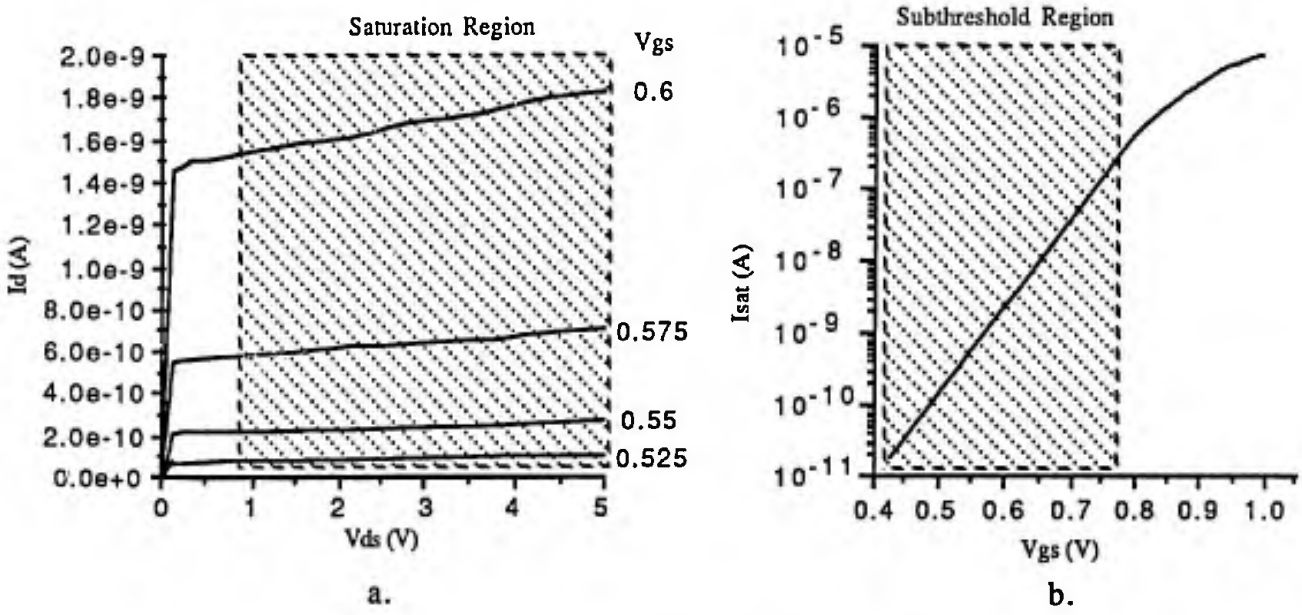

Figure 3. a) Plot showing the effects of Vds and Vgs on the current (Id) through the transistor. It also clearly labels the saturation region. b) Plot showing the exponential relationship between Vgs and Isat. Isat is the saturation value of the current Id as seen in Figure 3a. It also shows where the subthreshold region is. Above threshold Isat is proportional to Vgs^2.

The equation describing the characteristics of a transistor in the subthreshold region is

$$I = I_0\, e^{-\{(1-k)/V_T\}V_{bs}}\, e^{(k/V_t)V_{gs}}\left(1 - e^{-(1/V_T)V_{ds}} + V_{ds}/V_o\right)$$

Leakage Current | Body Effect | Subthreshold Control | Saturation Control | Early Effect

where k = the effectiveness of the gate voltage in determining the surface potential
I_0 = the zero bias current or leakage current
V_0 = a measure of the drain resistance or early voltage
V_T = the thermal voltage

The values k, I_0, and V_0 are constants of the fabrication process and V_T is a constant equal to Boltzmann's constant times absolute temperature divided by the charge of an electron. The various portions of the equation are labeled underneath. The leakage current is due to the fact that the

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[3] Mead, C., Analog VLSI and Neural Systems, Addison-Wesley Publishing Company, New York, NY, 1989.

transistor does not have infinite resistance when Vgs equals zero. Io is usually on the order of 10^{-18} amps but it can vary several orders of magnitude depending on the temperature and size of the transistor. The body effect is a measure of how much the body voltage (Vbs) controls the conductance of the transistor. Ideally, only the gate voltage (Vgs) would change the conductance but in the real world you typically find values of k equal to about 0.7. The subthreshold and saturation control portions of the equation effect the regions of operation of the transistor as demonstrated in Figure 3. The early effect is caused by the fact that the resistance of the transistor is greater than zero in the saturation region and is what causes the slight positive slope in the saturation region.

If the transistor is confined to the saturation region as well as the subthreshold region and if the early effect and body effect are small, the equation reduces to

$$I_{sat} = I_o e^{(k/V_t)V_{gs}}$$

A plot of this equation can be seen in the subthreshold region of Figure 3b. Above threshold in Figure 3b Isat is proportional to Vgs^2. It is important to note that the assumptions used in deriving the above simplified version of the equation are often not valid. This simplified version is often useful in a qualitative sense but the more complete version is usually used for any real circuit analysis. For the purposes of understanding how the electronic neuron operates the reduced form of the equation is sufficient. The important thing to remember is that Isat, which is the drain current through the transistor (Id in Figure 2), is directly related to the exponential of Vgs. In other words, as Vgs increases, the resistance across the transistor decreases exponentially, and therefore the drain current through the transistor increases exponentially.

4. ELECTRONIC NEURON

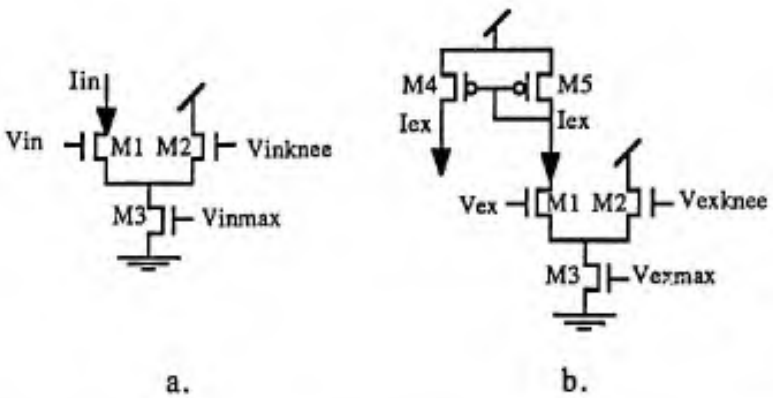
4.1 The Dendrites.

In this section of the paper, when I use the word neuron I am specifically referring to the electronic neuron we developed. The neuron has eight inputs or dendrites, four excitatory and four inhibitory. The input circuits consist of a differential pair for the inhibitory and a mirrored differential pair for the excitatory (see Figure 4). A differential pair is a common circuit which converts a ΔV into a ΔI. In the case of the input circuits below the ΔV = Vin - Vinknee for the inhibitory and ΔV = Vex - Vexknee for excitatory. It essentially operates as a resistive current divider. Transistor M3 establishes the maximum current as set by Vinmax (Vexmax). The current is comprised of the sum of the drain currents through transistors M1 and M2, which is controlled by there respective gate voltages. When the Vin (Vex) is less than Vinknee (Vexknee) by a few thermal voltages most of the current will go through transistor M2 because it is the path of least resistance. This results in little to no Iin (Iex), i.e. no output current. However, when Vin (Vex) is greater than Vinknee (Vexknee) by a few thermal voltages, most of the current will go through transistor M1 resulting in a significant Iin (Iex). The equation for a differential pair is

$$I = Ib \frac{e^{kV1}}{e^{kV1} + e^{kV2}} \qquad (1)$$

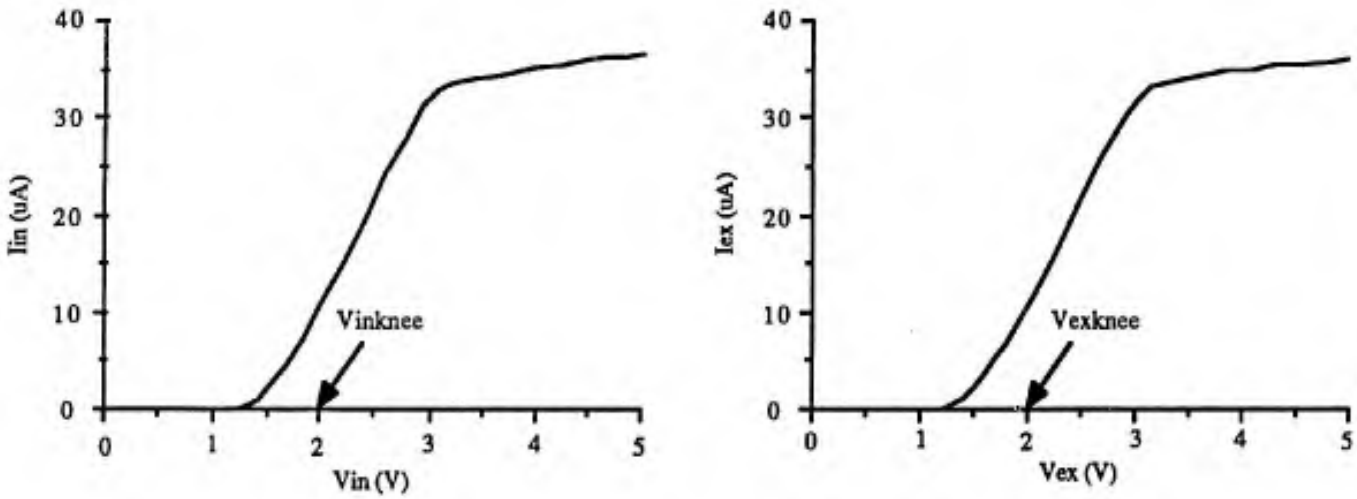
where k = the effectiveness of the gate voltage in regulating the drain current
V1 = Vin or Vex depending on the circuit
V2 = Vinknee or Vexknee depending on the circuit
Ib = the drain current through transistor M3 and is set by Vinmax or Vexmax depending on the circuit

A current mirror is, as its name suggests, a circuit which causes a current in one location to be reflected, almost unchanged, to another location. Referring to Figure 4b, since transistor M4 and M5 have common gate and source connections and assuming they have approximately equal values of Io, then the current through each will be approximately the same. Also, Iex is still controlled by Vex because the transistor M5 is diode connected (its gate is connected to its drain), thus the drain current through it sets its gate voltage. In the case of the excitatory input, the drain current through transistor M1 is reflected over to act as an excitatory input. Refer to Figure 5 for a plot of the input / output characteristics of the inhibitory and excitatory input circuits.



a. b.

Figure 4. a) Schematic diagram of an inhibitory input. b) Schematic diagram of an excitatory input. The arrows show the direction of the injection current.



a. b.

Figure 5. a) Plot of the input / output characteristics of the inhibitory circuit. b) Plot of the input / output characteristics of the excitatory circuit.

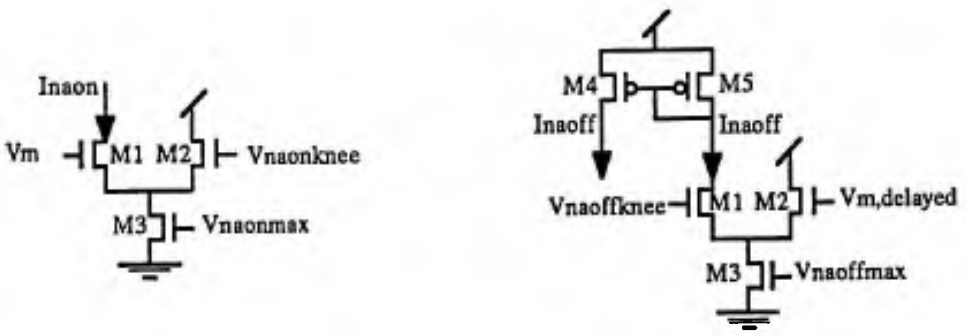
4.2 The Soma.

4.2.1 The Membrane Capacitance.

The soma is modeled as a capacitor. Just as the soma's voltage changes according to the summation of the currents coming from the dendrites, the capacitors voltage also changes according to the summation of the input currents. The voltage of the capacitor, in a manner similar to that of the soma, initiates a series of reactions resulting in the formation of an action potential or voltage spike.

4.2.2 The Sodium Current.

The sodium current is broken down into the sodium activation (Inaon) and sodium inactivation (Inaoff) currents. Inaon models the opening of the voltage controlled sodium gates and Inaoff models the closing of these gates. Inaon is generated using a differential pair where the voltage on the capacitor (Vm) is the input signal (see Figure 6a). Inaoff is generated using a mirrored differential pair where a delayed version of Vm is used as the input signal (see Figure 6b). Vnaonknee and Vnaoffknee model the threshold voltages for the opening and closing of the sodium gates respectively. It is necessary to delay the signal to the sodium inactivation circuit to allow time for Inaon to charge the capacitor sufficiently to generate an action potential and is consistent with the delay between the opening and closing of the sodium gates.



a. b.

Figure 6. a) Schematic diagram of the sodium activation current. b) Schematic diagram of the sodium inactivation current. The summation of these two currents is mirrored onto the membrane capacitor.

The delay circuit used to generate Vm,delayed is a low pass filter (see Figure 7). Essentially it is a differential pair with a current mirror connecting the ends and a capacitor connected to the output. In order to explain the operation of this circuit let us assume that Vm is initially 0 volts and takes a step increase to 2 volts. Vm establishes a drain current through transistor M2, this current is mirrored to the other side of the differential pair. This current will then be divided into a drain current through transistor M1 and a current to charge the capacitor. Initially, most of the current will be used to charge the capacitor because the resistance through transistor M1 will be large. As the capacitor is charged, however, the gate to source voltage on transistor M1 will increase, thus decreasing its resistance and more of the current will go through it. Once Vm,delayed reaches Vm it will remain at equilibrium until Vm changes. The parameter Vnaofftau establishes the maximum current that can pass through transistors M1 and M2. In this way it limits how fast the capacitor can charge, thus it can control the delay of the circuit. The

smaller Vnaofftau is the larger the delay will be. Figure 8 shows a plot of the input / output characteristics of this circuit.

The sodium current, which is a summation of Inaon and Inaoff, is mirrored onto the membrane capacitor and is used to charge the capacitor (i.e. increase the voltage in the soma). The mirror is sourced at a voltage Ena. Ena is the limit to which the membrane capacitor can be charged and is analogous to the potential of the electro-chemical gradient (reversal potential) in biological neurons. When Vm is increased due to the excitatory inputs Inaon will increase thus further increasing Vm. After a time delay, Inaoff will begin to increase until it completely cancels Inaon and Vm will stop increasing. At this point in the biological neuron potassium gates open and decrease the voltage in the soma. Likewise, in the electronic neuron, there is a potassium current which will now be described.

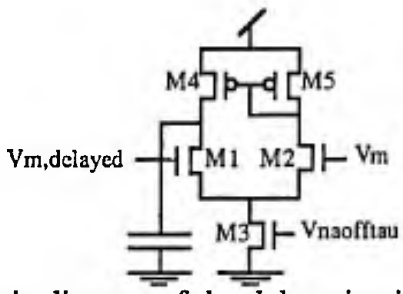


Figure 7. Schematic diagram of the delay circuit used to generate Vm, delayed from Vm.

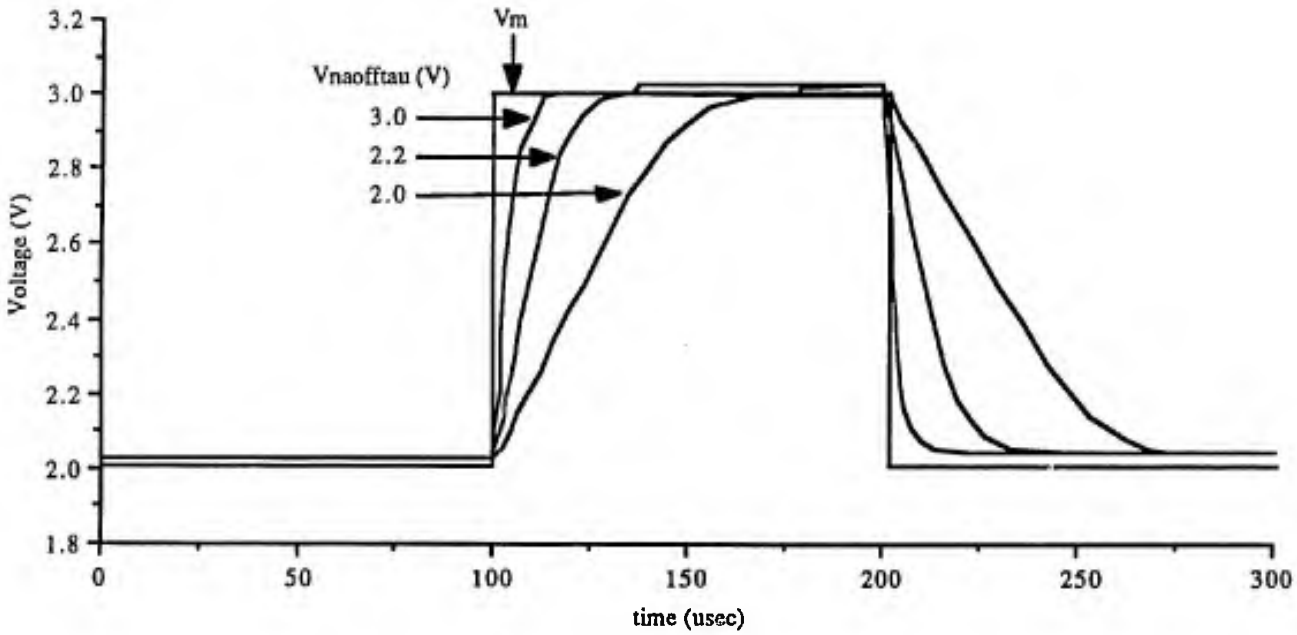


Figure 8. Plot of the input/output characteristics of the delay circuit for various values of Vnaofftau. This simulation was performed with Vm stepping up and down between 2 to 3 volts.

4.2.3 The Potassium Current.

The potassium current (Ik) is formed the same way as Inaoff. Referring to Fig's 4b and 5, simply substitute Vktau, Vkmax, and Vkknee for Vnaofftau, Vnaoffmax, and Vnaoffknee and you have the circuit for Ik. The output of this circuit is mirrored onto the membrane capacitor with a n-type mirror sourced at Ek. Ek is analogous to the reversal potential of potassium in biological neurons and controls the minimum voltage to which Ik can bring Vm.

4.3 The Axon.

The axon in biological neurons transmits the action potential to its destinations. In the electronic neuron an analogous device would simply be a voltage tap off the capacitor to transmit Vm. The line could then be connected to the inhibitory or excitatory inputs (dendrites) of other neurons or it could be used to drive electric motors (muscles). Depending on the size of the motor, however, you might want to amplify the signal first. See appendix A for a complete schematic of the neuron.

5. LAYOUT CONSIDERATIONS

The chief objective in the layout was to achieve the minimum possible size. The overall neuron size came to about 330 microns by 330 microns. The capacitors were made by laying poly2 on top of poly with a layer oxide between them. This achieves a capacitance of about 0.5 ff per square micron. The membrane capacitor is 10 microns by 20 microns for a value of 100ff and the capacitors in the delay circuits are 4 microns by 80 microns for a value of 160ff. Appendix A shows the sizes of all the transistors but, essentially, all the transistors were sized 4 microns by 4 microns except the bias transistors for the differential pairs which were sized 4 microns wide by 12 microns long and the transistors that mirror Ina and Ik onto the membrane capacitance which were 4 microns wide by 2 microns long. See appendix B for a diagram of the pinout used.

6. TESTING PROCEDURES

6.1 Testing for Proper Functionality.

As an initial guess we initialized all the voltages to those used in the SPICE simulation and powered up the circuit. This resulted in Vm rising to a constant value. We then varied each parameter to see if it had the expected effect on Vm. As an example, increasing Vnaoffmax decreased Vm because it caused more current to be pulled away from the capacitor, increasing Vnaonmax increased Vm because it caused more current to be dumped onto the capacitor. This process continued until all the parameters had been tested and we felt that all the circuit elements were functioning properly. After adjusting Vnaoffknee and Vnaonknee the neuron began spiking.

Once the neuron was spiking we continued adjusting the parameters to get the spike shape seen in the SPICE simulations. We found that the circuit was extremely sensitive to the knee voltages (see the results section for the voltages used). We then gradually increased the excitatory input and observed an increase in the spiking frequency and then increased an inhibitory input and saw a corresponding decrease in the frequency until it completely nulled the output. We tested each input circuit in a similar manner to ensure that they were all working properly.

The next step was to see if there was good matching between the chips. To test this we pulled the chip we were presently using and put in another chip, keeping all the voltages the same, and powered up the circuit. We found that three out of the four chips fired properly under these conditions.

6.2 Cascading Neurons.

As our end goal in fabricating these chips is to build a system of neurons with one neuron exciting or inhibiting the next we decided to test if a pulsating input could excite the neuron. To test this we used a square wave as input to one of the excitatory circuits. At first we used a square wave with a 50 percent duty cycle (the duty cycle is the percentage of the period that the signal is high) at a frequency of 1 kHz, this input was sufficient to excite the neuron but was not a realistic model of the neuron spikes we intended to use. We then decreased the duty cycle to 0.5 percent and the neuron stopped firing. It was found that at 1 kHz, a duty cycle of 5 percent was the minimum required to elicit a response. At that level, each input pulse elicited a single spike. As the 0.5 percent duty cycle was the most realistic model we brought the duty cycle back down to that level and increased the frequency until the neuron would fire. The minimum frequency was found to be 2 kHz.

The next step was to hook the output of one neuron into the excitatory input of the next to see if the neuron would fire in cascade. With the first neuron spiking at about 2 kHz the second neuron was sufficiently excited and fired at about 1 kHz. We then tried a feedback loop where the first neuron excited the second and the output of the second was fed back to inhibit the first. As a result, every time the second neuron fired it inhibited the first causing it to miss a spike. Finally, we had the same feedback set-up as above except the output of the second neuron was fed into the excitatory input of the first. In this case, every time the second neuron fired it excited the first, thus causing an additional spike.

7. RESULTS

7.1 Results of the SPICE Simulation.

A SPICE simulation of the spike shapes is shown in Figure 9. Figure 10 shows the effect of the excitatory input intensity on the spiking frequency. The values used in the SPICE simulation are given in Table 1. The SPICE simulations results were similar to those obtained experimentally. The initial rising hump in the spikes is due to the charging of the membrane capacitor. Once the membrane capacitor is charged high enough to surpass the threshold voltage (i.e. above Vnaonknee) then Inaon increases and quickly spikes the neuron up to approximately Ena (Ena = 3V). Shortly thereafter Inaoff and Ik turn on and the voltage is quickly brought back down to its base value which is moderately higher than Ek (Ek = 1V). This process is repeated so long as there is a net excitatory input feeding current to the membrane capacitor

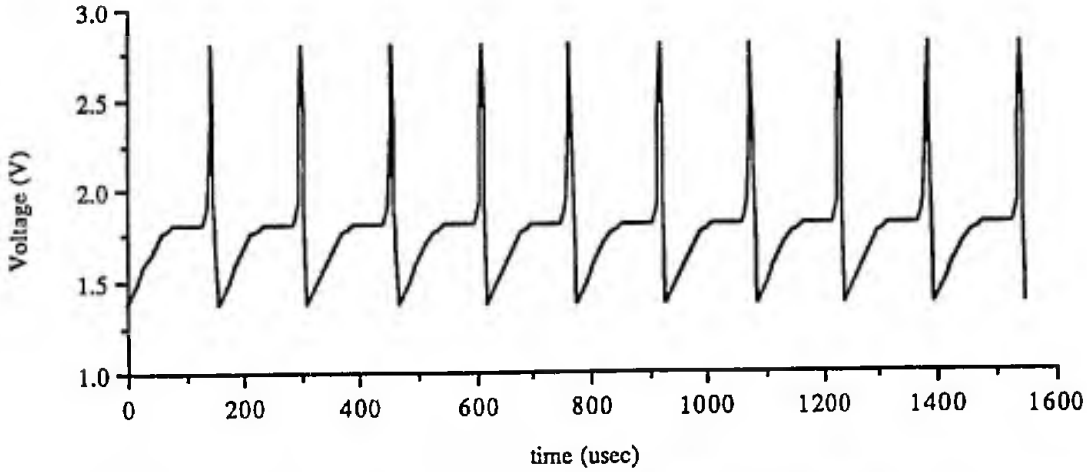


Figure 9. Plot of the peak shapes from the SPICE simulation. The transistor model used was that provided by the MOSIS Foundation for the simulation of circuits fabricated through them.

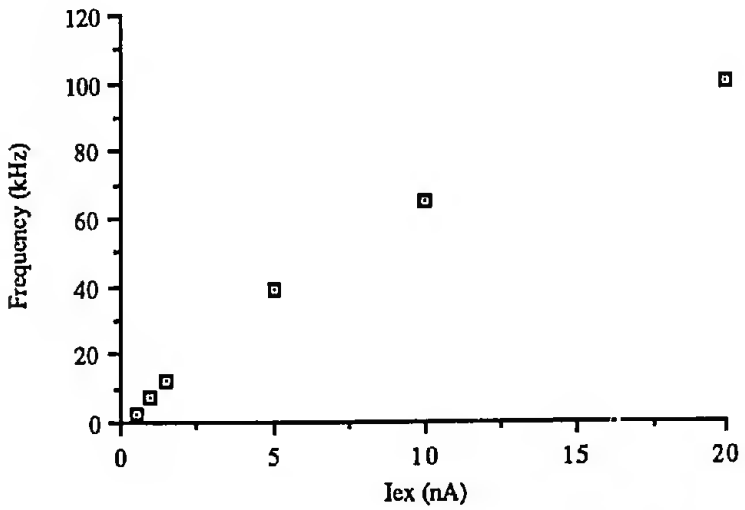


Figure 10. Plot of the spike frequency versus the input current obtained from the results of the SPICE simulations. Iex is related to Vex by equation (1) for the differential pair given above.

As the input current to the membrane capacitor is increased the spiking frequency will also increase. The input current, as described above, is related to the input voltage and the knee voltage by equation (1). This relationship is plotted in Figure 5b. The spiking frequency plateaus at about 100 kHz. The plateau level is controlled in part by Vnaonmax, Vnaoffmax, and Vkmax because they control how much current can be used to increase or decrease the voltage on the membrane capacitor. It is also controlled by Vnaofftau and Vktau because they control the delay between charging and discharging the membrane capacitor, thereby controlling the pulse width and frequency.

7.2 Results of the Experimental Tests.

Table 1 shows the values used in the experimental portion. The first attempt at generating a signal with a pulsed input was to use a square wave with a 50 percent duty cycle at frequency of 1 kHz. When the excitation input is high the neuron spikes but when it is low it does not (see Figure 11). There is a short delay between the input square wave going high and the neuron's spike, this is caused by the time delay in charging the membrane capacitor above the threshold voltage. The last spike in each packet occurs just after the input voltage goes low. This is because the membrane capacitor was still charged and the sodium circuit was already starting to turn on, therefore it completed the cycle and spiked while the input was zero.

An attempt was made to more accurately model the spiking of neuron by reducing the duty cycle to 0.5 percent at a frequency of 1 kHz. This set-up generated only random spikes. The duty cycle was raised until the neuron would start firing again. This occurred at a duty cycle of 5 percent with a frequency of 1 kHz. This set-up generated a single spike for every input pulse.

TABLE 1 - PARAMETER VALUES USED

Parameter	SPICE	Experimental
Ena	3	4
Vktau	0.67	.74
Vkknee	2.2	1.8
Vkmax	0.75	1.48
Vnatau	0.67	.73
Vnaoffknee	2.2	1.9
Vnaoffmax	0.79	1.25
Vnaonknee	2.0	1.64
Vnaonmax	0.79	1.08
Vexknee	2.0	2.05
Vex1	2.0	2.04
Vexmax1	0.65	.66
Vinknee	2.0	2.03
Vin1	0.0	0
Vinmax1	0.65	.66
Vek	1.0	.996
All Others	0.0	0

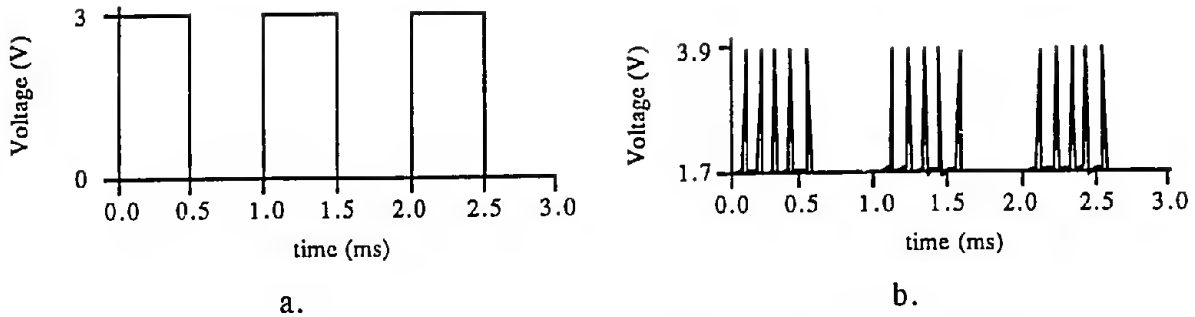


Figure 11. a) Plot of the square wave excitatory input signal. The duty cycle is 50 percent. b) Plot of the resulting output signal from the neuron. The neuron spikes only when the input signal is high.

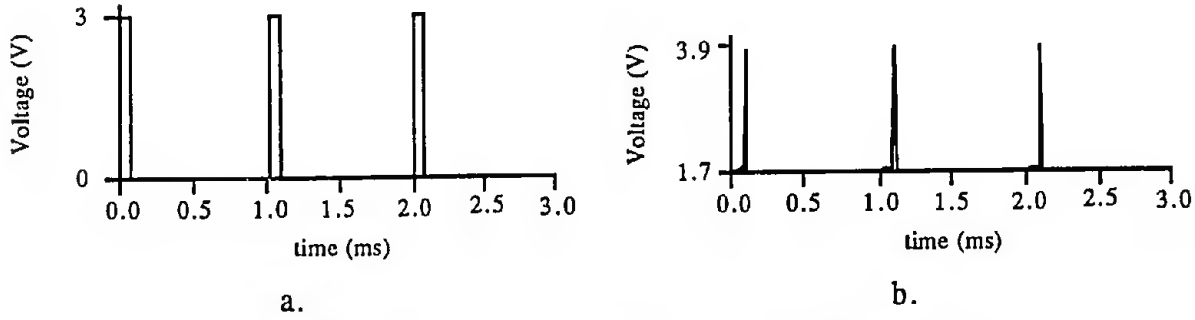


Figure 12. a) Plot of the square wave excitatory input signal. The duty cycle is 5 percent. b) Plot of the resulting output signal from the neuron. The input square wave elicits only a single spike from the neuron. A shorter duty cycle can be used if you increase the frequency of the input signal.

A more realistic model of a neuron spike would be obtained with a shorter duty cycle, therefore we increased the frequency of the input, keeping the duty cycle at 1 percent, until a spike occurred. This was achieved at a frequency of 2 kHz. The duty cycle was further reduced to 0.5 percent and the neuron still spiked but at a significantly lower rate. This showed that the neuron could be excited with another neuron. We then cascaded two neurons as shown in Figure 13. This was the crucial test to prove that one neuron's output could excite another neuron. Neuron A was spiking at about 2 kHz and neuron B was spiking at about 1 kHz (see Figure 14). The first spike of neuron A raises the voltage on the membrane capacitor but not above the threshold voltage. The second spike brings it over the threshold and elicits a spike in neuron B.

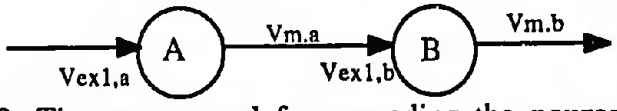
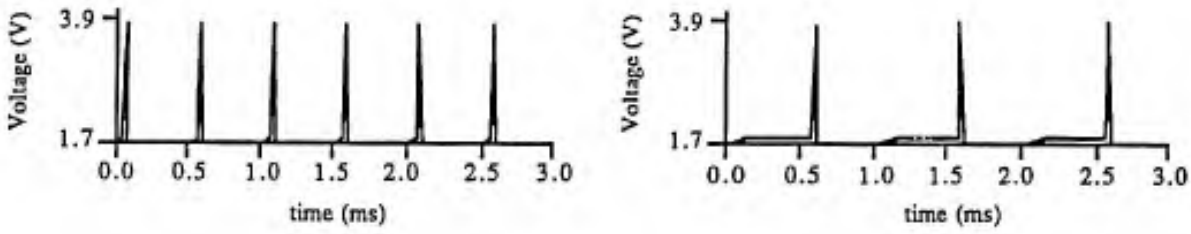


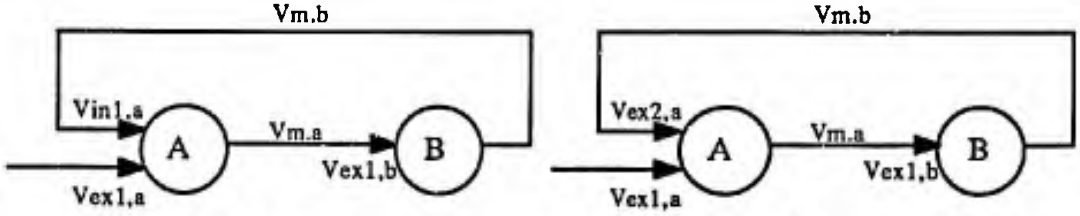
Figure 13. The set-up used for cascading the neurons. Both neurons are receiving there signals through excitatory input circuits.



a. b.

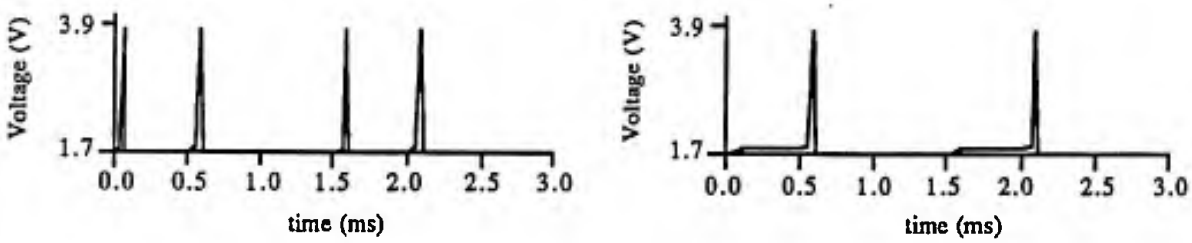
Figure 14. a) Plot of the output of neuron A. b) Plot of the output of neuron B. The first spike of neuron A raises the voltage on the membrane capacitor but not above the threshold voltage. The second spike brings it over the threshold and elicits a spike in neuron B.

The next step was to test the inhibitory capability of the neuron as well as to see if the neuron could be used in a feedback type structure. To test this the negative feedback architecture of Figure 15a was used. As expected neuron A excited neuron B and every time neuron B spiked it inhibited neuron A and a spike was skipped (see Figure 16). This sort of feedback architecture is used quite commonly in biological systems. This also demonstrated the inhibitory capability of the neurons. Finally, we tested the neuron in a positive feedback architecture (see Figure 15b). Using this architecture neuron A excited neuron B and every time neuron B spiked it excited neuron A and an extra spike was elicited (see Figure 17).



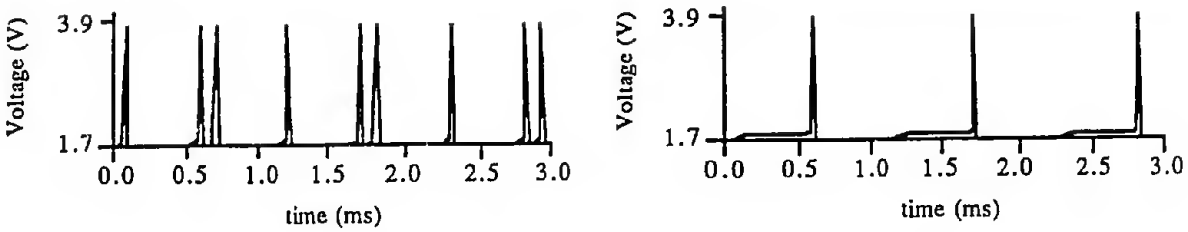
a. b.

Figure 15. a) Negative feedback loop b) Positive feedback loop.



a. b.

Figure 16. a) Plot of the output of neuron A connected in the negative feedback architecture. b) Plot of the output of neuron B. Just as with Figure 14, it takes two spikes from neuron A to elicit a spike from neuron B. When neuron B spikes it successfully manages to inhibit neuron A and neuron A skips a spike.



a. b.

Figure 17. a) Plot of the output of neuron A connected in the positive feedback architecture. b) Plot of the output of neuron B. Just as with Figure 14, it takes two spikes from neuron A to elicit a spike from neuron B. When neuron B spikes it successfully manages to excite neuron A.

8. CONCLUSIONS

The results of these tests are quite promising. They show both the ability of the neuron to accurately model its biological counterpart and its ability to be used in some neural architecture where neurons are exciting and inhibiting other neurons. Most neural network architectures use extremely simplified models of neurons as their base component. This is mostly due to the fact that these architectures are usually implemented in software and computational efficiency is a very high priority. With this analog VLSI neuron, however, a more sophisticated model can be used without sacrificing time. In fact, the computational speed of an analog VLSI chip will be several orders of magnitude faster than using desk top computers. Using this neuron as the basic building block it should be possible to build more complex networks that display many of the characteristics of human intelligence. In order to test the ability of this model in simulating more complex neural architectures we will attempt to recreate the neural motor control system of an insect, specifically a cockroach, using this neuron as a building block. The neural architecture of a cockroach was successfully modeled in software previously by other researchers[4]. This model will be the basis of our hardware implementation.

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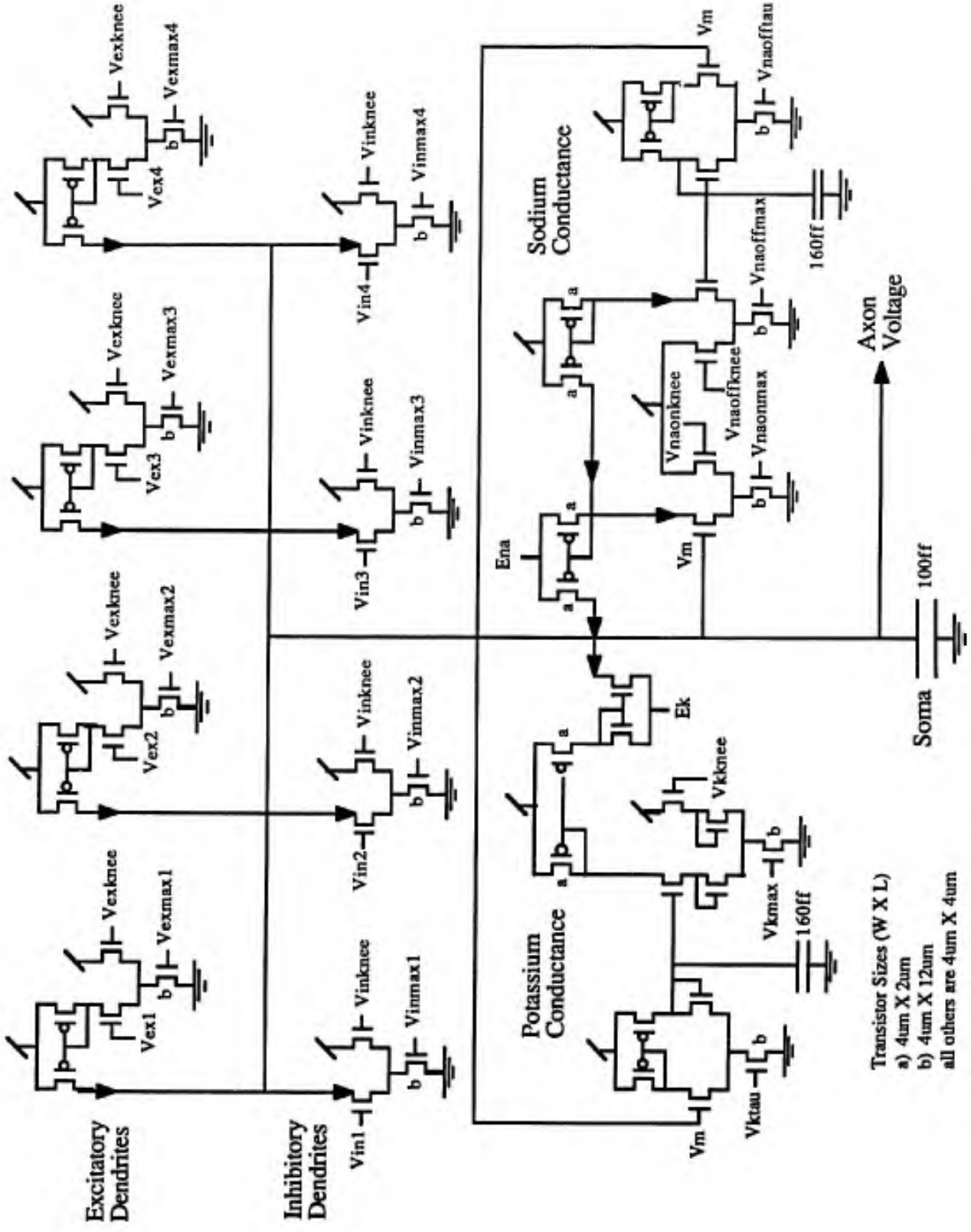
4 Beer, R.D., Chiel, H.J., Sterling, L.S., "An Artificial Insect," American Scientist Vol. 79, pp 444-452 (1991).

APPENDIX A

SCHEMATIC DIAGRAM OF THE SILICON NEURON



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APPENDIX B
CHIP PINOUT ARRANGEMENT