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QUARTERLY TECHNICAL REPORT #1
(4/20/92 - 6/30/92)

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Title of Work:

RF VACUUM MICROELECTRONICS

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REVIEW

Since this is the first quarterly progress report, a brief review will be given of the basic Hughes process as developed up through 1990 to create FEAs. Uniform pyramidal tips are defined when a <100> Si substrate is etched through a Si_3N_4 mask using KOH. The width of the opening determines the depth of this self-limiting etch. The result is a crystallographically sharp pyramidal hole formed by the <111> planes. Any desired array pattern of these holes can be formed. These holes are subsequently thermally oxidized to produce a thin oxide etch barrier, and this etched Si wafer then becomes a "mold" or negative of the desired array of tips. Polysilicon is deposited into the mold and built up to a self-supporting thickness. The mold is then etched away leaving a array of uniform polysilicon tips on a self-supporting polysilicon substrate.

FEAs are then formed by coating the tips with a thin layer of molybdenum. The emitter-to-gate insulator of SiO_2 is applied by CVD, and then the gate metal is laid down. The next step, the key to the process, employs a self-aligned planarization technique. A thin layer of photoresist is spun on and becomes "planarized." The resist is then dry etched in an oxygen plasma to reveal only the tips of the coated pyramids. Reactive ion etching of both the gate metal and the SiO_2 insulator results in submicron openings in the gate layer centered on the emitter tips and the FEAs are complete. Note only one mask layer was needed for the process.

1.0 Emitter Fabrication

1.1 Mask Design and Procurement

1.1.1 Mask Set #1

The first multi-layer mask set has been designed and ordered. This set will allow us to fabricate pyramidal FEA structures with tip base sizes of 1.0, 1.5, 2.0, and 2.5 micrometers. The set includes tip arrays of 1 X 1, 3 X 3, 4 X 4, 6 X 6, 10 X 10, 20 X 20, 100 X 100, and a hexagonal 100 X 100 array with two tips per unit cell or 20,000 tips total. Most combinations of tip size and array size are available. The mask set consists of five layers. The main layer, the tip mask, creates the basic FEA pattern. Two additional layers allow us to pattern both the emitter structures as well as the gate structures to reduce gate-to-emitter capacitance. Another layer allows us to deposit additional metal in the array "streets" between the tips. This should help to localize damage to the array in the event of an arc. The last layer allows us to etch back down to the emitter layer from the front to make contact with the tips if we decide to isolate the tips from the header.

Four of the five layers arrived in June. Unfortunately, the mask house had to remake the main layer which is due near the end of July.

1.2 Process Optimization Experiments

1.2.1 Process #1.1

While the main mask layer did not arrive in June, we did have some Si molds left over from our previous IR&D program, so we began process design experiments using these molds and plain Si wafers. Although polysilicon was previously used as the tip material, we wanted to see if the tips could be formed of solid

metal. To this end we began a series of experiments whereby first a 200 A layer of titanium was deposited onto a Si wafer followed by 1 micron of gold. We then electrodeposited .007" of silver to form a self-supporting substrate, silver being chosen since it was the most convenient plating bath available. The Si was then etched away, and the Ti/Au was unaffected and the substrate flat.

We then repeated the process using some of the left-over molds, and the process proved perfectly suitable. Figures 1 and 2 show Ti/Au tips on a silver substrate. We next continued processing these tips into FEAs. 300 A of Mo was deposited onto the tips without any noticeable reduction of tip sharpness as shown in Figure 3. The rest of the process was performed as described above with the resulting FEAs shown in Figures 4 and 5.

Concurrently, we have also been experimenting with electodeposited nickel and copper. We believe that nickel would be a more suitable substrate than silver due to the former's higher tensile strength and melting point. Further experiments will continue during the next quarter.

2.0 Emitter Testing

2.1 Design and Fabrication of Test Chamber

Fabrication of the test chamber began this quarter. The chamber is a horizontal cylinder with a test volume 11" in diameter and 24" long. The vacuum is produced by a 6" turbopump. One end of the chamber is a 14" Conflat flange. This flange carries 48 MHV electrical feedthroughs to allow 16 FEAs to be tested per loading. Also attached to this flange will be the fixturing to hold the FEAs. Thus each loading will only require the removal of this one flange and good access to the FEAs will be obtained.

The chamber also has feedthroughs for possible plasma cleaning of the FEAs, internal quartz bakeout lamps, and thermocouples. An RGA will also be attached.

Currently only the FEA fixturing remains to be completed. The 14" end flange is complete. The chamber has been pumped down, and a pressure in the low 10^{-9} Torr range is easily achieved.

2.2 Create Test Plan

We intend to test each FEA using three Keithly Source Measurement Units. To this end two Keithly Model 237 SMUs and one Keithly Model 236 were purchased and received. We are presently writing the software to measure the I-V curves of the FEAs.

3.0 Low Work Function Materials

3.1 Identify Candidate Materials

Candidate materials are currently under study at the Hughes Research Laboratories at Malibu. No significant progress to report at this time.

4.0 FEA Equivalent Model

4.1 Develop Model

An equivalent circuit model of the FEA is currently in work and an initial model will be completed in the next quarter.

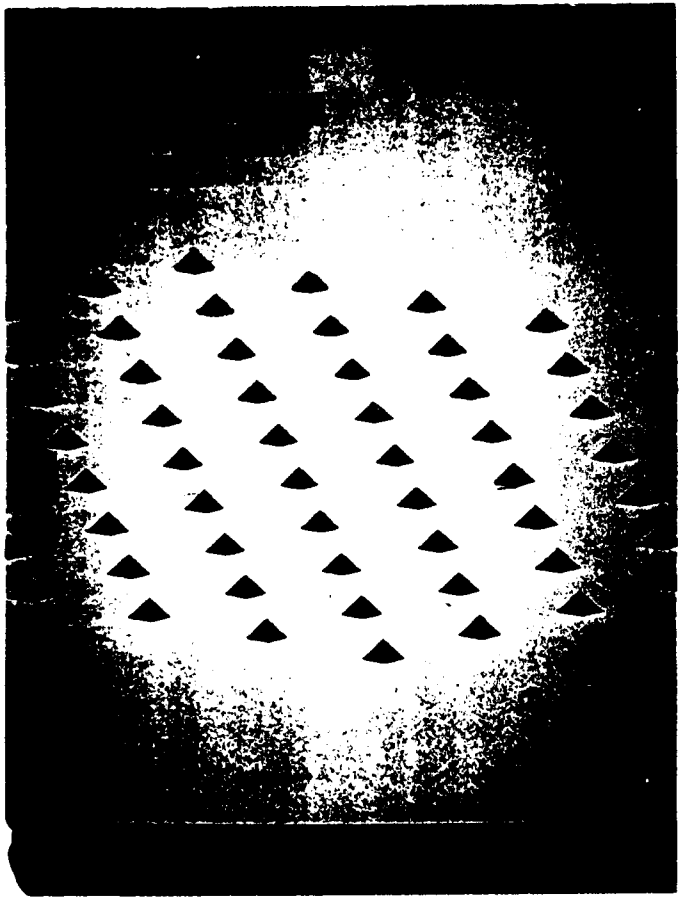

Figure 1
FEA Fabricated on
Silver Substrate

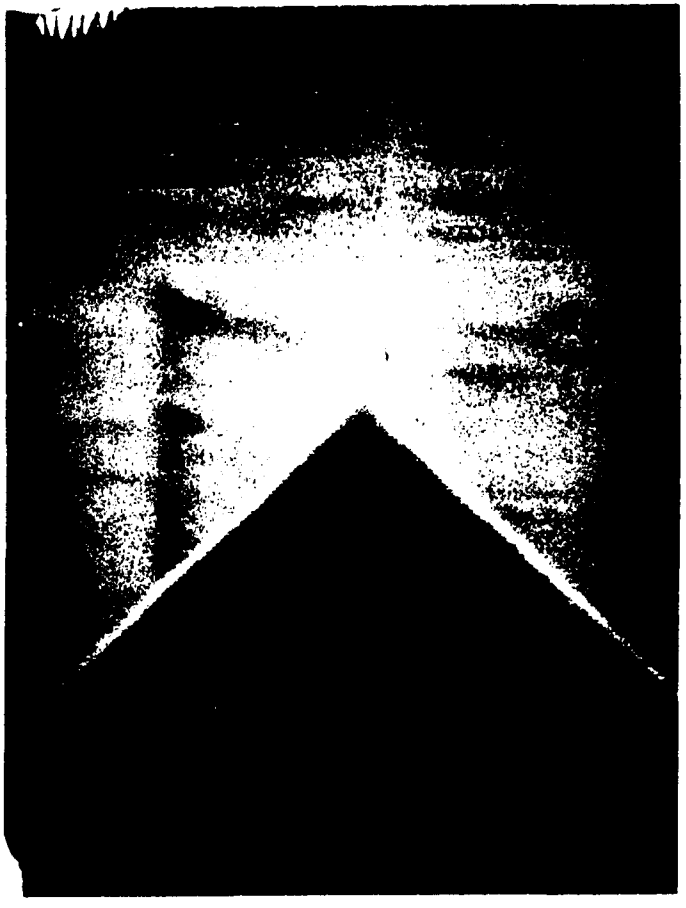

Figure 2
Individual Tip

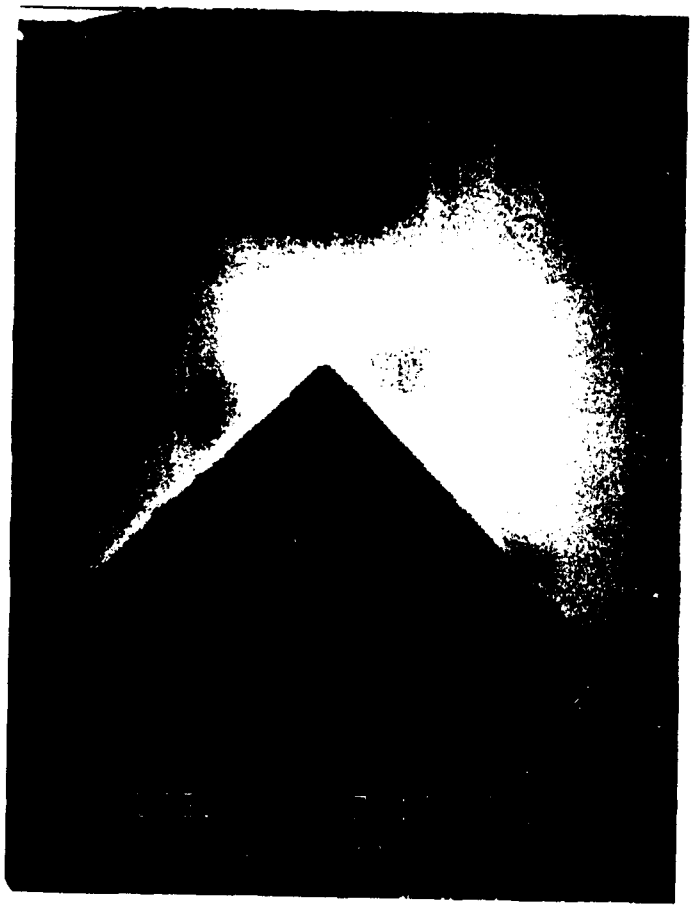

Figure 3
FEA Tip Coated with
300 A of Molybdenum

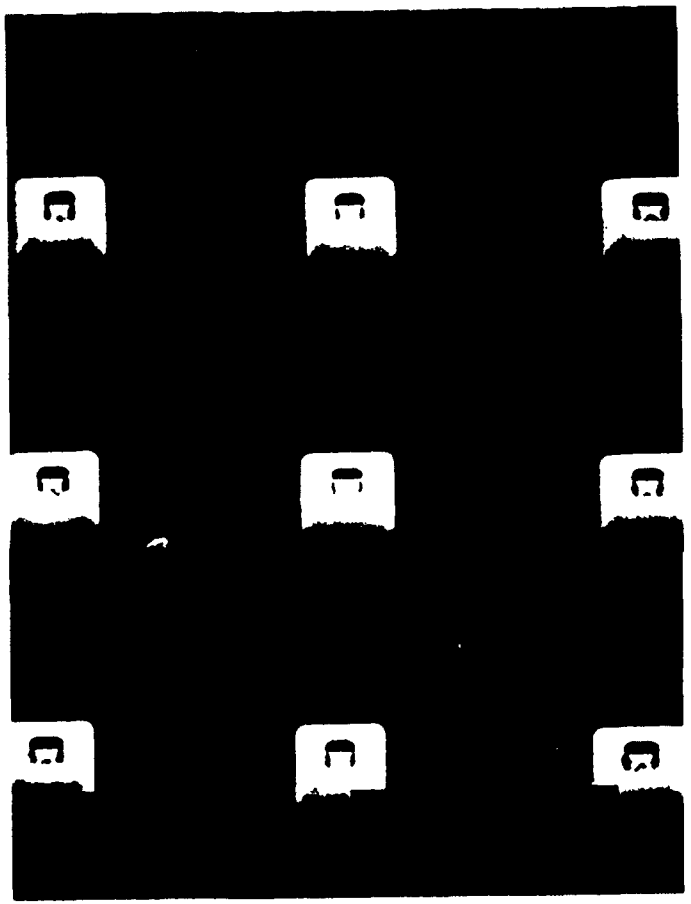

Figure 4
Fabricated FEA Structures

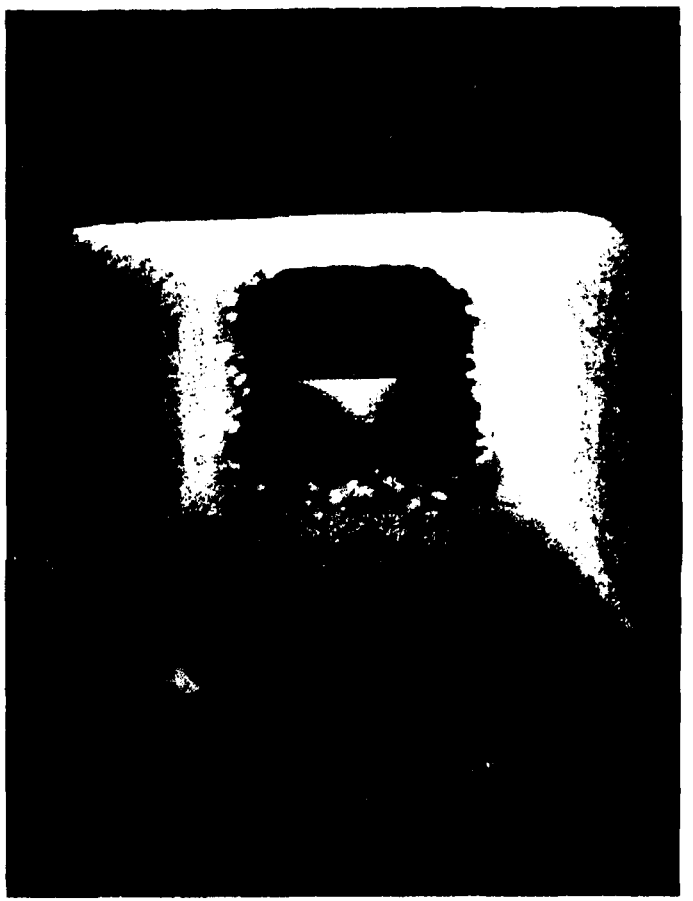

Figure 5
Individual Gated Structure