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Final Technical Report

VLSI Reliability Research

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Abstract

Aggressive scaling toward submicron VLSI technologies has greatly heightened the need for a better basic understanding of the reliability failure mechanisms and the need for better testing methods and technological solutions. This project researched these issues for the four leading failure modes of VLSI systems: oxide wearout, radiation effects, hot-electron-induced degradation, and interconnect and contact electromigration. We have developed quantitative physical (not simply empirical) models for the failure mechanisms, more accurate methods for testing, screening and reliability prediction, and explored promising new technologies for improved VLSI reliability. Many of the research results have already been accepted and used by the semiconductor industry.

Research in VLSI Reliability

I. Introduction

In order to increase the circuit density and speed of VLSI systems, microelectronic device geometry is shrinking from a few microns to submicron and beyond. This scaling has greatly heightened the need for a better understanding of the failure mechanisms affecting the long-term reliability of VLSI system and for improved methods of designing and testing for reliability. In contrast to production technologies and circuit performances, whose failures to meet specifications will be either obvious or relatively easily discovered before the circuits are incorporated into complex systems or missions, reliability failures cannot be easily or completely eliminated. When they do occur, reliability failures can be costly in many ways. Yet, until recently, reliability issues have been given little systematic scientific research. They are relegated to empirical burn-in screening and costly design bandaids.

Analysis of field failures and laboratory test have identified three failure mechanisms as being the most important for VLSI systems. They are oxide wearout, hot-electron failures and contact and interconnect failures. We have investigated all these three failure mechanisms.

Due to aggressive scaling, the nature of reliability failures is undergoing a subtle change. Gross extrinsic defects used to be the main cause of, for example, oxide and contact failures. Now, the lifetime of a normally good oxide and contact becomes the issue. On the negative side, this has made reliability a more urgent issue, one that must be considered at the design stage. On the positive side, this has made some of the reliability failures more predictable and allowed reliability research to be performed on a larger group of samples. Interestingly, insights gained from studying these "predictable" failures will also help us to deal with the gross-defect failures, which remain important and significant.

The goal of this research was to perform basic scientific research into the mechanisms of the three leading hard failure modes: hot-electron-induced degradations, and contact and metal failures. Failure models have been developed and methods to improve reliability assurance through design, processing, and testing techniques have been invented and developed.

III. *List of Publications*

1. J. Lee, I.C. Chen, S. Holland, Y. Fong, C. Hu, "Oxide Defect Density, Failure Rate and Screen Yield," Digest of Technical Papers, *1986 IEEE Symposium on VLSI Technology*, San Diego, CA., May 1986, pp. 69-70.
2. J.Y. Choi, P.K. Ko, and C. Hu, "Effect of Oxide Field on Hot-Carrier-Induced Metal-Oxide-Semiconductor Field-Effect Transistor Degradation," *Applied Physics Letters*, Vol. 50, No. 17, Apr. 27, 1987, pp. 1188-1190.
3. I.C. Chen and C. Hu, "Accelerated Testing of Time-Dependent Breakdown of SiO_2," *IEEE Electron Device Letters*, EDL-8, No. 4, Apr. 1987, pp. 140-142.
4. I.C. Chen, S. Holland, and C. Hu, "Electron Trap Generation and Defect in SiO_2," *Proceedings of 1987 International Symposium on VLSI Technology, Systems and Applications*, Taipei, Taiwan, May 1987, pp. 85-86.
5. I.C. Chen, S. Holland, and C. Hu, "Electron Trap Generation by Recombination of Electrons and Holes in SiO_2," *Journal of Applied Physics*, Vol. 61, No. 9, 1 May 1987, pp. 4544-4548.
6. S. Holland, I.C. Chen, and C. Hu, "Ultra-Thin Silicon-Dioxide Breakdown Characteristics of MOS Devices with n^+ and p^+ Polysilicon Gates," *IEEE Electron Device Letters*, Vol. EDL-8, No. 12, Dec. 1987, pp. 572-575.
7. I.C. Chen, J.Y. Choi, T.Y. Chan, T.C. Ong, and C. Hu, "The Effect of Channel Hot-Carrier Stressing on Gate Oxide Integrity in MOSFET," *Proceedings of IEEE International Reliability Physics Symposium*, Monterey, CA., Apr. 1988, pp. 1-7.

8. J. Lee, I.C. Chen, and C. Hu, "Statistical Modeling of Silicon Dioxide Reliability," *Proceedings of IEEE International Reliability Physics Symposium*, Monterey, California, April 1988, pp. 131-138.

9. Y. Fong, A.T. Wu, P.K. Ko, and C. Hu, "Oxides Grown on Textured Single-Crystal Silicon for Enhanced Conduction," *Applied Physics Letters*, Vol. 52, No. 14, April 1988, pp. 1139-1141.

10. B-K. Liew, N.W. Cheung, and C. Hu, "Effects of High Current Pulses on Integrated Circuit Metallization Reliability," *IEEE Intersociety Conference on Thermal Phenomena in the Fabrication and Operation of Electronic Components*, Los Angeles, May 1988, pp. 3-6.

11. J. Lee and C. Hu, "LPCVD Thin Oxide Process," *Digest of 1988 VLSI Technology Symposium*, San Diego, May 1988, pp. 49-50.

11. B-K Liew, N.W. Cheung and C. Hu, "Electromigration Interconnect Failure Under Pulse Test Conditions," *Digest of 1988 Symposium on VLSI Technology*, San Diego, May 1988, pp. 59-60.

12. T.C. Ong, K. Seki, P.K. Ko, and C. Hu, "Hot-Carrier Induced Degradation in P-MOSFET's Under AC Stress," *IEEE Electron Device Letters*, Vol. 9, No. 5, May 1988, pp. 211-213.

13. M.M. Kuo, M. Seki, P. Lee, J.Y. Choi, P.K. Ko, and C. Hu, "Simulation of MOSFET Lifetime Under AC Hot Electron Stress," *IEEE Transaction on Electron Devices*, Vol. ED-35, No. 7, July 1988, pp. 1004-1011.

14. J. Lee, C. Hegarty, and C. Hu, "Electrical Characteristics of MOSFETs Using Low-Pressure Chemical Vapor Deposited Oxide," *IEEE Electron Device Lett.*, Vol. EDL-9, No. 7, July 1988, pp. 324-327.

15. C. Hu, P.K. Ko, P. Lee, J. Lee, N. Cheung, and B.K. Liew, "IC Reliability Prediction," *Abstracts of Semiconductor Research Council (SRC) TECHCON '88*, October 1988, Dallas, Texas, pp. 240-243.

16. C. Hu, "Reliability by Design," *Digest of Government Microcircuit Applications Conference*, Las Vegas, Nevada, November 1988, pp. 381-384.

17. I.C. Chen, J.Y. Choi, T.Y. Chan, and C. Hu, "The Effect of Channel Hot Carrier Stressing on Gate Oxide Integrity in MOSFET," *IEEE Transaction on Electron Devices*, Vol. 35, No. 12, December 1988, pp. 2253-2258.

18. J. Lee, I.C. Chen, and C. Hu, "Modeling and Characterization of Oxide Reliability," *IEEE Trans. on Electron Devices*, Vol. 35, No. 12, December 1988, pp. 2268-2278.

19. J. Chung, M.C. Jeng, G. May, P.K. Ko, and C. Hu, "Hot Electron Currents in Deep Submicron MOSFETs," *Technical Digest of International Electron Devices Meeting (IEDM)*, San Francisco, December 1988, pp. 200-203.

20. M. Jeng, J. Chung, G. May, P. Ko, and C. Hu, "Design Guidelines for Deep-Submicron MOSFETs," *Technical Digest of International Electron Devices Meeting (IEDM)*, San Francisco, December 1988, pp. 386-389.

21. M.C. Jeng, J. Chung, A.T. Wu, T.Y. Chan, J. Moon, G. May, P.K. Ko, and C. Hu, "Performance and Hot-Electron Reliability of Deep-Submicron MOSFET's," *Technical Digest of International Electron Devices Meeting (IEDM)*, Washington, D.C., Dec. 1987, pp. 710-713.

22. R. Moazzami, J. Lee, I. Chen, and C. Hu, "Projecting the Minimum Acceptable Oxide Thickness for Time Dependent Dielectric Breakdown," *Technical Digest of International Electron Devices Meeting (IEDM)*, San Francisco, CA, December 1988, pp. 710-713.

23. J.Y. Choi, P.K. Ko, C. Hu, and W. Scott, "Hot-Carrier Induced MOSFET Degradation -- Oxide Charge versus Interface Traps," *Journal of Applied Physics*, Vol. 65, No. 1, 1 January 1989, pp. 354-360.

24. T.C. Ong, K. Seki, P.K. Ko, and C. Hu, "P-MOSFET Gate Current and Device Degradation," *1989 International Reliability Physics Symposium Proceedings*, Phoenix, AZ, April 1989, pp. 178-182.

25. J. Chung, M.C. Jeng, J.E. Moon, P.K. Ko, and C. Hu, "Low-Voltage Hot Electron Degradation in Deep Submicrometer MOSFETs," *1989 International Reliability Physics Symposium Proceedings*, Phoenix, AZ, April 1989, pp. 92-97.

26. B.K. Liew, N.W. Cheung, and C. Hu, "Electromigration Interconnect Lifetime Under AC and Pulse DC Stress," *1989 International Reliability Physics Symposium Proceedings*, Phoenix, AZ, April 1989, pp. 215-219.

27. R. Moazzami and C. Hu, "An Oxide Burn-In Model," *Digest of 1989 VLSI Technology Symposium*, Kyoto, Japan, May 1989, pp. 77-78.

28. T.C. Ong, P.K. Ko, and C. Hu, "P-MOSFET Gate Current and Device Degradation," *Proceedings of 1989 International Symposium on VLSI Technology, Systems and Applications*, Taipei, Taiwan, May 1989, pp. 193-196.

29. **Keynote Address,** C. Hu, "Submicron IC Reliability Research at Berkeley," *Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, New Orleans, Louisiana, September 1989, pp. 1-6.

30. **Invited Paper,** C. Hu, "Reliability Issues of MOS and Bipolar IC's," *Proceedings of 1989 IEEE International Conference on Computer Design (ICCD '89)*, Cambridge, Massachusetts, October 1989, pp. 438-442.

31. **Invited Paper,** C. Hu, "Submicron Device Reliability Research," *Technical Digest of 1989 International Conference on VLSI and CAD (ICVC '89)*, Seoul, Korea, October 1989, pp. 425-429.

32. R. Moazzami, J. Lee, and C. Hu, "Temperature Acceleration of Time-Dependent Dielectric Breakdown," *IEEE Trans. on Electron Devices.*, Vol. 36, No. 11, November 1989, pp. 2462-2465.

33. B.K. Liew, N.W. Cheung, and C. Hu, "Effects of Self-Heating on Integrated Circuit Metallization Lifetimes," *Technical Digest of International Electron Devices Meeting (IEDM)*, Washington, D.C., December 1989, pp. 323-326.

34. E. Rosenbaum, P.M. Lee, R. Moazzami, P.K. Ko, and C. Hu, "Circuit Reliability Simulator -- Oxide Reliability Module," *Technical Digest of International Electron Devices Meeting (IEDM)*, Washington, D.C., December 1989, pp. 331-334.

35. J. Chung, J. Chen, M. Levi, P.K. Ko, and C. Hu, "The Effects of Off-Axis Substrate Orientation on MOSFET Characteristics," *Technical Digest of International Electron Devices Meeting (IEDM)*, Washington, D.C., December 1989, pp. 633-636.

36. C. Lau, C. Hu, and E.J. McCluskey, "Research in Advanced Electronic System Reliability," *Naval Review*, Vol. XLI, Three/1989, pp. 9-19.

37. P.M. Lee, P.K. Ko, and C. Hu, "Relating CMOS Inverter Lifetime to DC Hot-Carrier Lifetime of NMOSFETs," *IEEE Electron Device Letts.*, Vol. 11, No. 1, January 1990, pp. 39-41.

38. Y. Fong, A.T. Wu, and C. Hu, "Oxides Grown on Textured Single-Crystal Silicon -- Dependence on Process and Application of EEPROMs," *IEEE Trans. on Electron Devices*, Vol. 37, No. 3, March 1990, pp. 583-590.

39. B.K. Liew, P. Fang, N.W. Cheung, and C. Hu, "Reliability Simulator for Interconnect and Intermetallic Contact Electromigration," *1990 International Reliability Physics Symposium Proceedings*, New Orleans, LA, March 1990, pp. 111-118.

40. B. Liew, N. Cheung, and C. Hu, "Projecting Interconnect Electromigration Lifetime for Arbitrary Current Waveforms," *IEEE Trans. on Electron Devices*, Vol. 37, No. 5, May 1990, pp. 1343-1351.

41. J.E. Moon, T. Garfinkel, J. Chung, M. Wong, P.K. Ko, and C. Hu, "A New LDD Structure: Total Overlap with Polysilicon Spacer (TOPS)," *IEEE Electron Device Letters*, Vol. 11, No. 5, May 1990, pp. 221-223.

42. P. Fang, K.K. Hung, P.K. Ko, and C. Hu, "Characterizing a Single Hot-Electron-Induced Trap in Submicron MOSFET Using Random Telegraph Noise," *Digest of Technical Papers of Symposium on VLSI Technology*, Honolulu, Hawaii, June 1990, pp. 37-38.

43. R. Moazzami and C. Hu, "Projecting Gate Oxide Reliability and Optimizing Burn-in," *IEEE Trans. on Electron Devices*, Vol. 37, No. 7, July 1990, pp. 1643-1650.

44. J. Chung, M-C. Jeng, J. Moon, P.K. Ko, and C. Hu, "Low Voltage Hot Electron Degradation in Deep Submicron MOSFETs," *IEEE Trans. on Electron Devices*, Vol. 37, No. 7, July 1990, pp. 1651-1657.

45. T.C. Ong, P.K. Ko, and C. Hu, "Hot-Carrier Current Modeling and Device Degradation in Surface Channel P-MOSFET," *IEEE Trans. on Electron Devices*, Vol. 37, No. 7, July 1990, pp. 1658-1666.

46. Y. Fong and C. Hu, "High-Current Snapback Characteristics of MOSFETs," *IEEE Trans. on Electron Devices*, Vol. 37, No. 9, September 1990, pp. 2101-2103.

47. J.E. Chung, K.N. Quader, C.G. Sodini, P.K. Ko, and C. Hu, "The Effects of Hot-Electron Degradation on Analog MOSFET Performance," *Technical Digest of IEEE International Electron Devices Meeting*, December 1990, pp. 553-556.

48. *Book Chapter*

C. Hu, "Hot Carrier Effects," Chapter 3 of *Advanced MOS Device Physics*, N.G. Einspruch, Editor, Academic Press, 1989, pp. 119-160.

IV. *Ph.D. Students Graduated*

Nine. Presently employed at MIT, University of Texas (Austin), Intel, TI, Motorola, Cyress Semiconductor, and Lawrence Berkeley Laboratory.

V. *Best Paper Awards*

1. Y. Fong and C. Hu, "The Effects of High Electric Field Transients on Thin Gate Oxide MOSFETs," *1987 Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, Orlando, Florida, Oct. 1987, pp. 252-257.

2. J. Lee, I.C. Chen, and C. Hu, "Statistical Modeling of Silicon Dioxide Reliability," *Proceedings of IEEE International Reliability Physics Symposium*, Monterey, CA., Apr. 1988, pp. 131-138.

3. C. Hu, P.K. Ko, P. Lee, J. Lee, N. Cheung, and B.K. Liew, "IC Reliability Prediction," *Abstracts of Semiconductor Research Council (SRC) TECHCON '88*, October 1988, Dallas, Texas, pp. 240-243.

4. J. Chung, M.C. Jeng, J.E. Moon, P.K. Ko, and C. Hu, "Low-Voltage Hot Electron Degradation in Deep Submicrometer MOSFETs," *1989 International Reliability Physics Symposium Proceedings*, Phoenix, AZ, April 1989, pp. 92-97.

VI. *Keynote Address and Invited Papers*

1. C. Hu (Invited Paper), "Thin Oxide Reliability," 1985 IEDM, Washington, DC, December 1985.

2. C. Hu (Invited Paper), "IC Reliability Prediction," *SRC TECHCON'88*, Dallas, Texas, October 1988.

3. **Keynote Address**, C. Hu, "Submicron IC Reliability Research at Berkeley," *Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, New Orleans, Louisiana, September 1989, pp. 1-6.

4. **Invited Paper,** C. Hu, "Reliability Issues of MOS and Bipolar IC's," *Proceedings of 1989 IEEE International Conference on Computer Design (ICCD '89),* Cambridge, Massachusetts, October 1989, pp. 438-442.

5. **Invited Paper,** C. Hu, "Submicron Device Reliability Research," *Technical Digest of 1989 International Conference on VLSI and CAD (ICVC '89),* Seoul, Korea, October 1989, pp. 425-429.

6. B.K. Liew (Invited Paper), "Electromigration Reliability," *Wafer Level Reliability Workshop,* Lake Tahoe, CA, October 1990.

VII. *Summary of Work Accomplished*

The numbers in parentheses () refer to the publications in Sec. III.

- Showed that hot-electron stress has no significant impact on oxide integrity, but hot hole injection significantly accelerates oxide wearout (7,18). This additional "worst case" for MOSFET oxide reliability has attracted two followup studies by DEC and Hitachi, both published in 1990.
- An "effective thinning" model is proposed so that oxide reliability can be quantified from ramp breakdown data (8,19,32)
- The first oxide burn-in model was developed (27) and a comprehensive approach to oxide reliability prediction was introduced (43). The theoretical minimum oxide thickness for 20 year operation at 5.5 V was determined to be 80 Å.
- A method for making 230 Å oxide behave as a 60 Å tunneling oxide for EEPROM without the defect and reliability problem fo the very thin oxide was proposed and demonstrated (9,38).
- An AC electromigration model was developed (12, 26, 40) and the self heating effect characterized (12,33). Electromigration data at up to 20 MHz was collected (40) while previous studies never could exceed 0.5 MHz.
- World record of MOSFET speed (22ps) was set and the reliability and performance constraints of highly scaled devices were determined (20, 21, 25)
- It was shown that no threshold (power supply) voltage exists for hot electron effects, contrary to previous optimistic suggestion (25,44)
- A new total-overlap LDD structure was proposed (41).
- For the first time, an individual hot-electron-generated interface trap was observed and characterized. The technique was the random telegraphic noise (42).
- Preliminary reliability simulator development ws carried out (34,37,39).

VIII. *Interaction with Industry*

The IC industry, in general, has considered our research highly relevant to the development of high density reliable IC's. Besides the awards and honors listed above, industry interest may be evidenced by the fact that supplementary funding for our reliability research has been provided by TI, GE, Rockwell International, Hughes, AMD, Signetics, and Sandia National Laboratory.

We were diligent in transferring knowledge generated by this research contract. Means for knowledge transfer included publication in journals and conferences, participation in industry workshops and standard committee (JDEC), career and summer student employment, visits and seminars at company sites, informal and organized visits by industry personnel to our laboratory, etc. Our new emphasis on reliability simulation, in our opinion, will be a major boost for knowledge transfer—it is considerably easier and more convenient for a large segment of IC engineers to use knowledge embedded in a turn-key software then to use the knowledge in a hundred journal articles. Developing improved device and process on the base of reliability physics knowledge is another form of knowledge transfer.