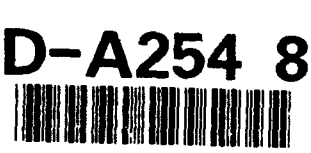

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# GaAs Gate Dynamic Memory Technology

## Final Report for
## ONR Contract N00014-89-J-1864

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During the course of this work the charge storage times of isolated GaAs pn-junction storage capacitors was increased from 20 minutes to over 10 hours at room temperature. This was accomplished through a combination of improved epitaxy, device processing, and device structure. Furthermore complete DRAM cells were demonstrated using JFET-, MESFET-, MODFET-, and HBT-access transistors.

The research supported by this contract has resulted in 21 journal publications and 18 conference papers.

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GaAs digital circuits are of interest because of their higher speed and lower power dissipation relative to silicon, their broader temperature range of operation, and their greater radiation tolerance. These factors make GaAs circuits very attractive for many military applications. There is a growing commercial market for digital GaAs as well, mainly in the area of high speed supercomputers. Future applications will develop around the basic compatibility of GaAs with MMIC and optoelectronic devices.

Digital systems invariably require large amounts of memory, preferably integrated on the same chip with the processing elements. Recent studies of computer architecture for GaAs show that the speed advantage of GaAs microprocessors is severely compromised by the need to go off-chip for memory access. This is especially true since the off-chip/on-chip cycle time ratio is larger for GaAs circuits than for silicon (in other words since GaAs systems are running faster than silicon, a long wait for off-chip access wastes more cycles in a GaAs system than a silicon system). This intensifies the need for fast , dense on-chip memory for GaAs digital systems. The one transistor dynamic RAM (DRAM) is the smallest, most dense semiconductor memory available. The availability of high density DRAM arrays in GaAs will have an enormous impact on the performance of GaAs digital systems by reducing the need for off-chip access, thereby directly improving the performance of the system as a whole.

We have investigated use of pn-junctions as the storage capacitor for GaAs DRAMs. During the course of this work the charge storage times of isolated GaAs pn-junction storage capacitors was increased from 20 minutes to over 10 hours at room temperature. This was accomplished through a combination of improved epitaxy, device processing, and device structure. Furthermore complete DRAM cells were demonstrated using JFET-, MESFET-, MODFET-, and HBT-access transistors. The details of the charge storage pn-junction capacitor and the transistor-accessed DRAM cells are discussed in the attached publications which are listed below.

**Thesis Supervision Completed Under This Contract**

| Name | date | Thesis Title |
|---|---|---|
| Scott T. Sheppard | MSEE, August 1991 | "Characterization of Generation Mechanisms in Gallium Arsenide PIN Diodes" |
| Chester Thad Gardner | MSEE, December 1991 | "Electrical-Characterization of NIPIN Structures in 6H-SiC" |
| John Kleine | Ph.D., May 1992 | "Characterization of MODFET Dynamic Memory Cells" |

**Publications in Scientific Journals Under This Contract**


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# Molecular beam epitaxy regrowth by use of ammonium sulfide chemical treatments

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The application of ammonium sulfide chemical treatments for molecular beam epitaxy regrowth is examined. Reflection high-energy electron diffraction, transmission electron microscopy, and capacitance-voltage profiling techniques are used to investigate the regrown interface. A slight enhancement of the electron concentration is seen at the regrown interface due to the incorporation of residual sulfur atoms as donors. The amount of residual sulfur donors is a strong function of the substrate temperature at which regrowth is initiated.

Several molecular beam epitaxy (MBE) regrowth techniques have been investigated during the past few years.[1-9] The major difficulty encountered in (MBE) regrowth is that GaAs surfaces exposed to atmosphere oxidize. This oxidation of the surface of a MBE-grown film results in a high density of interface states upon MBE regrowth even though the surface oxide is thermally desorbed before initializing growth. The regrowth technique which has met with the most success consists of deposition of an arsenic layer as passivation before removal of the sample from the MBE system.[1-5] However, the arsenic layers are not adequate for performing processing steps but only as protection when transferring samples between vacuum systems.[10] The arsenic can then be thermally removed leaving an as-grown surface.[4,5,11] Also, no matter how robust the passivation layer, if the processing step between growths exposes material below the passivation layer, some treatment of the exposed material is required to allow for the formation of an adequate electrical interface upon regrowth. A versatile regrowth procedure would allow growth of a MBE film structure, removal of the wafer from the vacuum system for an intermediate processing step such as patterning of the film, and then regrowth of MBE layers on the patterned lower MBE layers. Such a regrowth process would open the possibilities for many new device structures[12] if the regrown interface was of adequate electrical quality.

A number of chemical treatments have been demonstrated which remove surface oxides while at the same time reduce the surface state density of an exposed GaAs surface.[13-29] X-ray photoelectron spectroscopy (XPS) has shown that two of these chemical treatments, with ammonium sulfide or selenium reactions, result in a removal of surface oxides with at most a monolayer of sulfur or selenium remaining on the surface.[21-28] With a complete removal of the surface oxides, a reduction in surface state densities, and at most a monolayer of sulfur or selenium on the surface, these two chemical treatments are promising candidates for MBE regrowth. Recently Carpenter *et al.*[24] have demonstrated MBE regrowth on ammonium-sulfide-treated GaAs surfaces and Turco *et al.*[29] have demonstrated MBE regrowth on GaAs surfaces which have undergone selenium reactions. In this letter we present reflection high-energy electron diffraction (RHEED), transmission electron microscopy (TEM), and capacitance-voltage ($C$-$V$) profiling characterization of the regrown interface which results when the ammonium sulfide chemical treatment is utilized.

The MBE regrowth experiments were performed in a Varian Gen II MBE with 2 in. $n$-type GaAs substrates. Nonindium mounting was used for ease of remounting of the substrates and also so the samples would not need to be heated before reinsertion into the MBE system. Initially 1.5 $\mu$m of $n$-type GaAs doped $2\times10^{16}$ cm$^{-3}$ was grown. The sample was then removed from the MBE system and placed in a laminar flow hood for 1 h to insure oxidation and degradation of the surface. Next, the sample was placed in de-ionized water while an etch of 1:1:250 $H_2SO_4$:$H_2O_2$:$H_2O$ was prepared. The sample was then etched for 30 s followed by a de-ionized water rinse for 30 s. The sample was then placed in ammonium sulfide for 20 min. Following this soak, the ammonium sulfide solution was diluted with de-ionized water and the sample rinsed thoroughly. The sample was then blown dry and reinserted into the MBE system.

Since XPS measurements indicate less than a monolayer of sulfur coverage and no other contaminants, no contamination of the MBE growth chamber was expected. However, we outgassed the sample at 350 °C for 1 h in a high vacuum buffer chamber before insertion in the growth chamber of the MBE system.

The reflection high-energy electron diffraction (RHEED) pattern of the ammonium-sulfide-treated GaAs samples observed as the sample was heated to growth temperatures is displayed in Fig. 1. (The sample was under an arsenic flux during the RHEED observations.) Initially the RHEED pattern was somewhat spotty with only a hint of surface reconstruction. At 530 °C there was a dramatic change in the RHEED pattern. The main RHEED lines became streaks followed by an appearance of a twofold reconstruction in the [110] azimuth. It is possible the submonolayer of sulfur was starting to evaporate at this temperature, allowing the GaAs surface to reconstruct. [This interpretation is consistent with the low-energy electron energy loss spectroscopy (LEELS) observations of Oigawa *et al.*[30] who determined that the sulfur atoms are removed by heat treatments above 530 °C.] Above 580 °C the fourfold reconstruc-

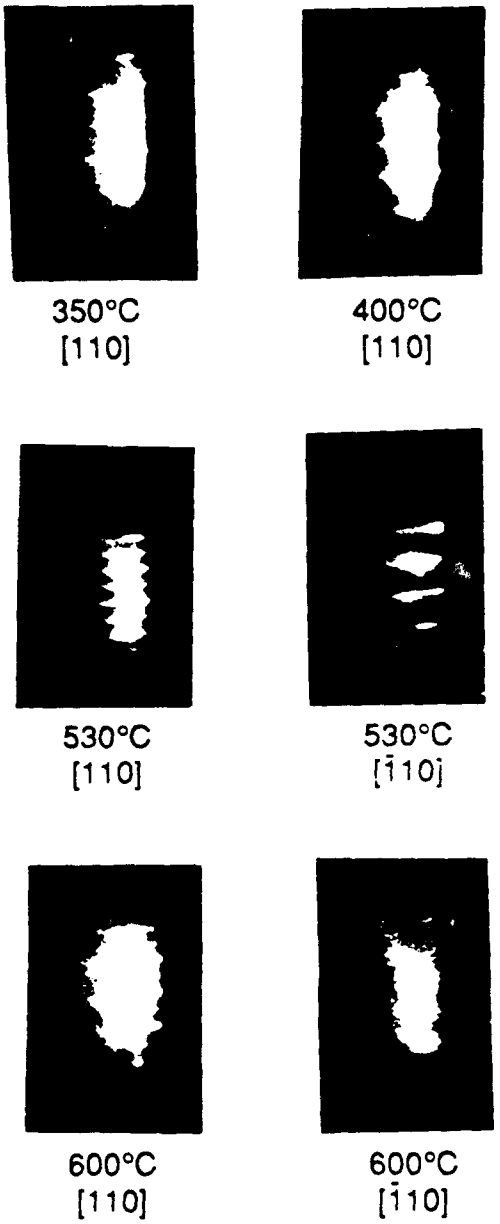


FIG. 1. Reflection high-energy diffraction pattern of a GaAs surface treated with ammonium sulfide as the sample is heated under an arsenic flux.

tion lines in the [$\bar{1}$10] azimuth became clearly visible, with the twofold reconstruction lines in the [110] azimuth dimming somewhat in comparison to the main lines. This RHEED behavior was observed on three separate wafers which were treated with the ammonium sulfide.

Upon initating growth of GaAs on the ammonium-sulfide-treated GaAs samples at a substrate temperature of 600 °C, the reconstruction lines in the [110] azimuth brightened, but the pattern was not unlike the pattern of the ammonium-sulfide-treated surface at a substrate temperature near or slightly higher than 540 °C. Also, oscillations were observed in the specular spot of the RHEED pattern upon initiating growth, indicating two-dimensional nucleation of the GaAs on the ammonium-sulfide-treated GaAs surface. The regrown GaAs layer was 0.5 $\mu$m thick and doped $n$ type at a concentration of $\sim 2\times 10^{16}$ cm

Using a mercury probe, the samples were $C$-$V$ profiled. From the $C$-$V$ data, the apparent carrier concentration as a function of distance from the surface was determined as displayed in Fig. 2. The measured carrier concentrations in the epilayers of $2.5\times 10^{16}$ cm$^{-3}$ are very close to the targeted value. However, there is a slight accumulation of electrons near the interrupted growth interface with a peak concentration of $5.7\times 10^{16}$ cm$^{-3}$. The accumulation of electrons at the interface may be due to residual sulfur atoms which did not evaporate and were incorporated into the film as donors. (The peak concentration appears to be shifted slightly into the regrown layer possibly due to outdiffusion of the sulfur ions.) This interpretation is further substantiated by measured carrier concentration as a function of position across our 2 in. sample. At the substrate temperatures used during MBE growth, there is a 10 °C increase in temperature from the center to the edge of our 2 in. sample as measured with an optical pyrometer. The carrier concentration displayed in Fig. 2 was measured $\sim$0.5 in. from the center of the 2 in. sample. As one moves towards the center of the sample, the peak of the electron concentration increases in magnitude. With the center of the wafer at a lower temperature, it is plausible that there is a larger concentration of residual sulfur atoms present which can incorporate in the film as donors and lead to the observed larger electron concentration at the interface.

The regrowth structures were also examined by cross-sectional transmission electron microscopy (TEM). The cross-sectional samples were prepared by mechanical grinding and argon ion thinning. A JEM 2000EX electron microscope was used for the observations. Figure 3 is a bright field image of a thin area of a cross-sectional sample, which exhibits a typical microstructure of the examined samples. In the lower part of the image, the interface between the substrate and the $n^+$-GaAs epilayer is seen as a low contrast dark line.

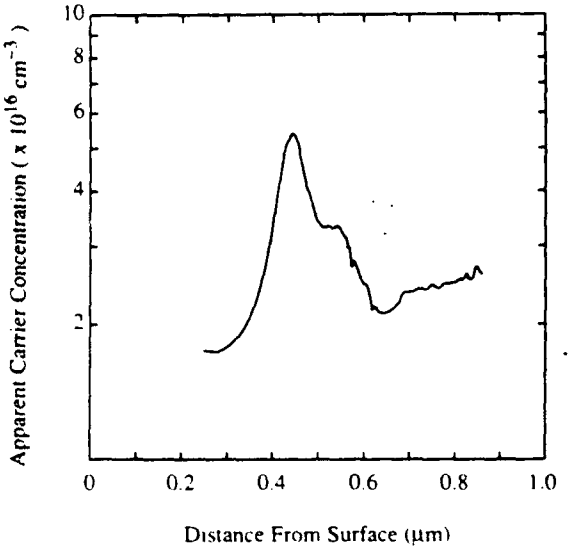


FIG. 2. Apparent electron concentration as a function of distance from the surface as determined from capacitance-voltage profiling. A slight accumulation of electrons is observed at the interrupted growth interface which was treated with ammonium sulfide.


FIG. 3. Cross-sectional transmission electron micrograph bright-field image in the area of MBE regrowth on an ammonium-sulfide-treated MBE-grown GaAs epilayer.

The appearance of the dark line suggests the existence of residual materials resulting from the substrate surface preparation. No contrast, however, is observed from the interface between the regrown epilayer and the buffer epilayer. In the image, the location of this interface, which is determined by the distance from the free surface of the regrown epilayer, is marked by arrows. All observed areas show similar bright-field images of the regrown interface, which are free of defects or clusters.

In summary, we have investigated the regrowth of GaAs on ammonium-sulfide-treated MBE-grown GaAs epilayers. Reflection high-energy electron diffraction, transmission electron microscopy, and capacitance-voltage profiling techniques were used. There appears to be a slight enhancement of electron concentration at the regrown interface due to residual sulfur atoms which incorporate in the film as donors. The amount of residual sulfur donors is a strong function of the substrate temperature at which regrowth is initiated. Ammonium sulfide chemical treatments appear to be a promising approach to a versatile regrowth procedure.

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# Ion-Implanted p-n Junction Capacitors for GaAs DRAM's

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# Briefs

## Ion-Implanted p-n Junction Capacitors for GaAs DRAM's

J. W. PABST, T. E. DUNGAN, J. A. COOPER, JR., AND M. R. MELLOCH

***Abstract*—The generation-limited storage time of ion-implanted GaAs p-n junction capacitors is reported. Deep n-type potential wells were formed in a lightly p-doped epitaxial layer with 150-keV $Si^{++}$ doses of $5 \times 10^{13}$ cm$^{-2}$ and $1 \times 10^{14}$ cm$^{-2}$. $Mg^{+}$ doses of $5 \times 10^{14}$ cm$^{-2}$ were implanted through a thin SiON cap at 40 and 60 keV to form shallow $p^{+}$-regions within the n-wells. Storage times obtained from capacitance transient measurements of the p-n-p structures indicate the possibility of planar ion-implanted GaAs dynamic memory cells at room temperature.**

### I. Introduction

GaAs memories are attractive for cache applications demanding very high speed and moderate capacity. Without a complementary MESFET technology, most GaAs SRAM's are fabricated with six-transistor E-D DCFL cells or with cells using four enhancement-mode transistors and two high-resistance load elements. To achieve high-speed operation, such cells are operated in overdrive [1], resulting in significant power dissipation in the storage state. A one-transistor GaAs dynamic memory cell could provide higher integration density and better speed/power performance than static memory cell designs.

The essential qualities of a DRAM storage capacitor are long storage time and large capacitance per unit area. Carrier confinement must be sufficient to insure storage times longer than the DRAM refresh period over the entire range of operating temperatures. For the down-scaling necessary for the desired high density of a DRAM design, the storage cell should also exhibit a large capacitance per unit area. The capacitance of a GaAs p-n junction grown by molecular-beam epitaxy (MBE) has demonstrated both attributes [2], [3].

Ion-implantation technology offers a proven processing strategy for fabricating high-yield planar devices. Demonstration of a storage capacitor fabricated by ion implantation is a first step toward achieving a one-transistor dynamic memory cell compatible with standard MESFET technology [4]. Fig. 1 shows such a fully ion-implanted GaAs MESFET DRAM cell, as proposed by Dungan *et al.* [2]. Although MBE-grown GaAs p-n junctions have demonstrated sufficient storage characteristics for DRAM applications, it is not apparent that the same qualities can be obtained with implanted p-n junctions. In this brief we report our investigations into ion-implanted GaAs p-n junctions for use as DRAM storage capacitors.

### II. Device Fabrication

To investigate the charge storage potential of ion-implanted p-n junctions, the structure of Fig. 2 was fabricated and tested. The storage cell is an ion-implanted version of the MBE-grown symmetric p-n-p buried-well structure reported from earlier experiments [2], [3]. The p-n-p capacitors were fabricated on four GaAs samples by ion-implanting Si and Mg into a 3-$\mu$m MBE-grown $p^{-}$-layer doped at $2 \times 10^{15}$ cm$^{-3}$. The samples and respective implants are listed in Table I. Using a 7-$\mu$m AZ-4620 photoresist mask on the bare GaAs, deep n-wells were selectively implanted with $Si^{++}$ ions at 150 keV. Si doses of $5 \times 10^{13}$ cm$^{-2}$ and $1 \times 10^{14}$ cm$^{-2}$ were used in two samples each, to form n-wells of differing donor density. After stripping the Si implant mask, 300 Å of $SiO_xN_y$ was deposited by PECVD with a flow ratio of 5 $SiH_4$ : 7 $NH_3$ : 3 $N_2O$. The SiON cap served several purposes. As reported in other papers [5], [6], this SiON film was found to minimize surface degradation of encapsulated semi-insulating GaAs substrates in furnace anneals. The amorphous capping layer reduced channeling of $Mg^{+}$ ions, which could spread the shallow $p^{+}$-regions to undesired depths. Mg lodged in the encapsulant above implanted regions also retarded the significant outdiffusion of Mg from the shallow $p^{+}$-regions into the SiON, which can occur during a furnace anneal [7]. An AZ-4620 photoresist layer was patterned to mask two $p^{+}$-regions within each n-well. A heavy dose of $5 \times 10^{14}$ cm$^{-2}$ of $Mg^{+}$ was implanted at either 40 or 60 keV to form the shallow $p^{+}$-surface regions. Following photoresist removal, the samples were rinsed in HCl acid and cleaned with solvents before furnace annealing for 15 min in an 850°C $N_2$ ambient. Proximity caps of semi-insulating GaAs placed face-to-face on each of the four sam-

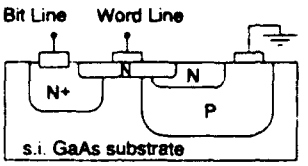


Fig. 1. Fully ion-implanted MESFET DRAM cell.

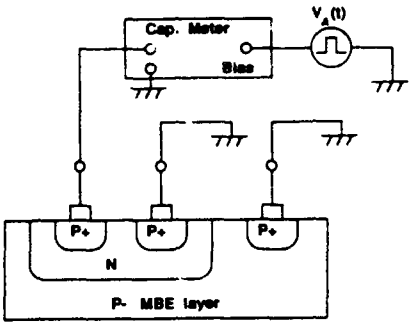


Fig. 2. Storage time test circuit and $p^{+}$-n-$p^{-}$ capacitor structure.

TABLE I
SAMPLES AND ION IMPLANTS

| sample | $Si^{++}$ implant | | $Mg^{+}$ implant | |
|---|---|---|---|---|
| | energy (keV) | dose (cm$^{-2}$) | energy (keV) | dose (cm$^{-2}$) |
| #P2A | 150 | $5 \times 10^{13}$ | 40 | $5 \times 10^{14}$ |
| #P2B | 150 | $5 \times 10^{13}$ | 60 | $5 \times 10^{14}$ |
| #P3A | 150 | $1 \times 10^{14}$ | 40 | $5 \times 10^{14}$ |
| #P3B | 150 | $1 \times 10^{14}$ | 60 | $5 \times 10^{14}$ |

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ples provided As (and Ga) overpressure to adequately reduce surface evaporation damage. A 5-min etch in HF acid and a 5-min boil in $H_3PO_4$ acid (140–150°C) removed all oxi-nitride from the GaAs samples. Contacts were fabricated with an evaporation and lift-off procedure. The surface acceptor density of the Mg-implanted regions was sufficient for ohmic response from the unannealed AuZn (99:1) p-contacts.

## III. Experiment

An n-layer sandwiched between two p-regions can be depleted of majority carriers for storage of positive charge. To deplete the n-well for storage time measurements, a voltage pulse is applied to the top $p^+$-contacts within the n-well, while the $p^-$-substrate is grounded. The capacitance transient following the voltage pulse shows the storage time constant, defined as the time needed for the capacitance of the depleted p-n-p structure to recover 63.2 percent of the difference between its initial and final values at zero bias.

In testing ion-implanted structures, it is important to understand the effects of assymetric doping levels on the capacitance transients. Fig. 3 is a typical capacitance transient observed in testing an ion-implanted $p^+$-n-$p^-$ storage cell by applying a voltage pulse $V_A$ as illustrated in Fig. 2. Consider the instant immediately after the leading edge of the positive pulse. Before any current flows from the n-well, electrons in the well redistribute towards the $p^+$-region. The $p^-$-n-depletion region widens more than the $p^+$-n depletion region contracts. The result is an immediate drop in the total capacitance.

The net effect of the forward- and reverse-bias currents across the $p^+$-n and $p^-$-n junctions, respectively, is a positive charging of the n-well. As the well charges, the $p^+$-n depletion region widens slightly, as its forward bias is reduced. The $p^-$-n depletion width also widens, as its reverse-bias is increased. The widening depletion regions cause the total capacitance to drop as the forward- and reverse-bias junction currents settle. When the two junction currents are equal, the total device capacitance reaches a steady-state value.

At the trailing edge of the voltage pulse, the electrons in the charged well are no longer drawn toward the $p^+$-region. The carriers shift back toward the $p^-$n junction, shrinking its depletion width and slightly widening the $p^+$-n depletion region. The total device capacitance, dominated by the wider $p^-$-n depletion width, instantaneously rises in response to the charge redistribution. Because electrons have been removed from the n-well, the n-region retains a positive charge. The capacitance is lower than the initial equilibrium zero-bias capacitance due to the enlarged depletion widths. Thermal generation in the depletion regions slowly repopulates the n-well to restore the depletion widths and the device capacitance to equilibrium. Analysis of the final rising capacitance transient yields the storage time constant.

The thermal generation rate is exponentially dependent on the operating temperature. Equation (1) follows from the inverse relationship between the generation rate and the storage time constant.

$$r_{gen} = \frac{C_1}{\tau_{st}} = C_2 e^{-E_A/kT} \qquad (1)$$

where

- $r_{gen}$ is the thermal generation rate (in ehp per second times cubic centimeters);
- $C_1$ is the proportionality (in ehp per cubic centimeter);
- $\tau_{st}$ is the storage constant (in seconds);
- $C_2$ is the rate constant (in ehp per second times cubic centimeter);
- $E_A$ is the activation energy of the generation mechanism (in electronvolts);
- $k$ is Boltzmann's constant (in electronvolts per degree Kelvin);
- $T$ is the abolute temperature of the device (in degrees Kelvin).

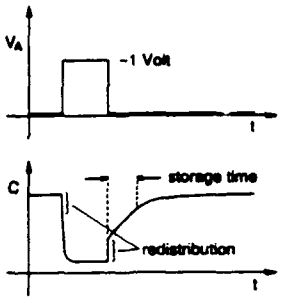


Fig. 3. Capacitance transient of $p^+$-n-$p^-$ structure during storage time test.

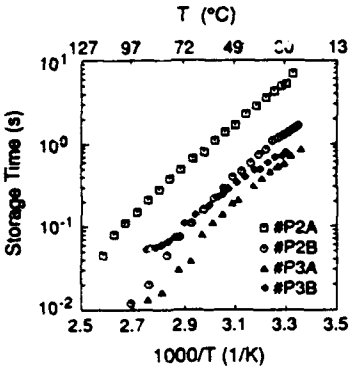


Fig. 4. Storage times versus temperature.

TABLE II
Storage Times and Activation Energies

| sample | $\tau_{st}$ at 27°C (s) | | | $E_A$ |
|---|---|---|---|---|
| | ave. | # tested | best | (eV) |
| #P2A | 2.00 | 24 | 8.00 | 0.516 |
| #P2B | 0.69 | 11 | 1.10 | 0.590 |
| #P3A | 0.64 | 29 | 2.50 | 0.539 |
| #P3B | 0.77 | 26 | 1.80 | 0.455 |
| ave. | — | — | — | 0.525 |

The activation energy $E_A$ can be found from the slope of a plot of $\ln(\tau_{st})$ versus $1/T$.

Table II summarizes the storage time data measured from the capacitance transients. Two $p^+$-regions were implemented within each n-region to allow surface-to-surface ($p^+$-n-$p^+$) or surface-to-substrate ($p^+$-n-$p^-$) capacitance tests. In measuring the storage times, the voltage pulse was applied to one $p^+$-surface region, while the other $p^+$-region and the $p^-$-bulk were grounded as illustrated in Fig. 2. This test configuration reduced noise in the capacitance meter output signal. Storage time constants $\geq 1$ s were typical at room temperature. Devices on sample #P2A held the positive charge for the longest time, averaging 2 s at room temperature. The superior storage times of sample #P2A devices can be related to the quantity of ion-implant damage to the substrate. Lighter doses and lower implant energies cause less lattice damage. The lighter dose of $Si^{++}$ and the lower energy of the $Mg^+$ implant in sample #P2A produce the least lattice damage, resulting in the longest storage times. The charge regeneration rate of the other three samples appears to be accelerated by the increased dose of $Si^{++}$ ions and/or the higher energy of the $Mg^+$ ions.

Fig. 4 shows the expected linear relationship between $\ln(\tau_{st})$ and $1/T$. The data were obtained by testing the best device on each of the four samples. The average activation energy of the thermal generation was found to be 0.53 eV. Half-bandgap activation energy is expected for bulk generation in most cases, but in an im-

planted region this assumption is questionable. The quantity and distribution of traps caused by the ion-implant damage may significantly increase the probability of multiple trap generation mechanisms.

## IV. Conclusion

The activation energies and time constants of the ion-implanted GaAs p-n junction storage capacitors are lower than previously repeated measurements of comparable devices constructed with MBE [2], [3] but sufficient for DRAM applications. The best ion-implanted device exhibited a storage time of 8 s at 27°C, decreasing to 110 ms at 101°C. Using such p-n junction capacitors in a GaAs DRAM with a refresh period of 1 kHz, commercial operating temperatures are attainable with a safety margin of two orders of magnitude in storage times. Shorter storage times corresponded to higher ion-implant doses and energies, suggesting that lattice damage is the limiting factor in the generation rate. Continuing improvements in ion-implantation technology will enable high-density high-yield radiation-resistant GaAs DRAM circuits for high-speed low-power digital signal processing applications.

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# One-Transistor GaAs MESFET- and JFET-Accessed Dynamic RAM Cells for High-Speed Medium Density Applications

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*Abstract*—**The introduction of digital GaAs into modern computing systems has lead to increasing demand for high-density memory in these GaAs technologies. To date, most of the memory development efforts in GaAs have been directed toward four- and six-transistor static RAM's, which consume substantial chip area and dissipate much static power. This paper discusses theoretical and experimental work that presents the possibility for a high-speed, low-power one-transistor room-temperature dynamic RAM technology in GaAs. Isolated storage capacitors have demonstrated over 20 min of storage time at room temperature with charge densities comparable to that obtained with planar silicon technology. One-transistor MESFET- and JFET-accessed DRAM cells have been fabricated and operated at room temperature and above. The standby power dissipation of these first cells is only a small fraction of the power dissipated by the best commercial GaAs SRAM cells.**

## I. Introduction

IN SILICON integrated circuits, dynamic and static memories have traditionally been targeted at different applications because of their differing capacities, speeds, and complexities. Dynamic memories achieve extremely high single-chip capacities which translate into excellent cost per bit and produce reliable, compact system designs. Static memories are used in applications requiring smaller single-chip capacity because of the design-simplicity advantage derived from eliminating the need for periodic refresh of the contents of the memory. Any memory technology will experience a reduction in speed performance as single-chip capacity is increased. Because dynamic memories are designed for higher densities, the access times of dynamic circuits are typically considerably longer than those achieved in static designs. For example, if the technology used is the same (e.g., 1-$\mu$m CMOS), then the access-time advantage of a 256-kb static memory over a 1-Mb dynamic chip is essentially attributable to the difference in capacity, rather than to an inherent speed advantage of one design approach over the other.

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Hierarchical memory designs combine the advantages of both static and dynamic memories by using small, fast static caches backed by large, efficient dynamic main memories. As processor speeds increase, the importance of inter-chip delays increases and the consequences of cache misses become more severe. The need for larger caches requires development of very fast memories of intermediate single-chip capacity in the 16- to 256-kb range. Because of power dissipation limitations, this capacity range is difficult to achieve with the static Si ECL designs presently used for high-speed caches. This paper reports initial progress in the development of low-power GaAs dynamic memories for this high-speed intermediate-capacity performance area.

MESFET-based static GaAs memories have been available for some time, but their single-chip capacity is limited both because of power dissipation and because of die-size restrictions in GaAs. Without an effective complementary-MESFET technology, GaAs static memory cells consume a significant amount of power in the storage state. This power dissipation can be largely eliminated in dynamic cell designs. It is this possible reduction in power dissipation without corresponding loss of speed that primarily motivates the consideration of dynamic memories in GaAs. The cell-area reduction associated with switching from static to dynamic cells is expected to be less significant in GaAs than in Si, as will be discussed later.

The lack of a native oxide with the excellent electrical characteristics of the $Si/SiO_2$ system complicates the design of both the access transistor and the storage capacitor for a one-transistor dynamic memory cell in GaAs. Section II describes the performance of generation-limited p-n junction capacitors as an alternative to MIS structures. Section III considers operating voltages for FET-accessed cells. Section IV discusses possible complete-cell configurations. Section V reports preliminary results from complete MESFET- and JFET-accessed memory cells. The concluding section summarizes the present state of the research.

## II. Design Considerations for p-n Junction Capacitors

Without a high-quality insulator with very low interface state density, it is not possible to construct the charge-

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coupled memory cells used in early silicon dynamic memory designs. The capacitance of a simple reverse-biased p-n homojunction has been suggested as an alternative for the storage element of GaAs dynamic memory cells [1]. The two critical requirements for the dynamic storage element are sufficient charge-storage density and low enough leakage to allow an acceptable refresh rate over the intended operating temperature range. In the optimization of p-n junction capacitors, a design tradeoff is encountered between maximum charge density and maximum storage time, as described below.

The charge per unit area stored on an abrupt p-n junction at reverse-bias voltage $V$ can be written as

$$Q = \left[ 2\epsilon q \frac{N_A N_D}{N_A + N_D} \right]^{1/2} [\sqrt{V_{bi} + V} - \sqrt{V_{bi}}] \quad (1)$$

where $\epsilon$ is the dielectric constant, $q$ is the electronic charge, $N_A$ and $N_D$ are the acceptor and donor densities, and $V_{bi}$ is the built-in potential. Increasing the doping density on both sides of the junction narrows the depletion width and increases the charge-storage density. The maximum charge-storage density at a given voltage would be obtained by increasing the doping levels until the breakdown limit due to avalanching or tunneling was only slightly larger than the applied bias. However, at the small logic-level voltages used in digital GaAs circuits, the material limits on doping density ($\sim 10^{18}$ cm$^{-3}$) will be reached before the breakdown limits of an ideal planar diode. At 1 V reverse bias, the charge-storage density on a GaAs diode doped near the material limits will be between 2 and 3 fC/$\mu$m$^2$. This is an order of magnitude lower than the theoretical maximum charge density achievable in silicon capacitors [2], but it is comparable to charge densities actually obtained in planar Si designs [3].

The storage time in a p-n junction capacitor with the p region grounded and the n region floating is determined by the rate at which thermal generation replenishes electrons removed from the n region. The generation current will have components due to the bulk and the perimeter of the device, and generation will occur both inside the depletion width and outside within a minority-carrier diffusion length. In GaAs the extremely low equilibrium minority-carrier concentrations result in a vanishingly small concentration gradient in the neutral regions under reverse bias, and bulk diffusion currents can be ignored. In regions where the junction intersects a surface, the surface diffusion current is enhanced because Fermi-level pinning results in increased equilibrium minority-carrier concentrations at the surface. However, calculation of the surface diffusion component by a method similar to that used in [4] for forward-biased diodes indicates that the generation within the surface depletion region will dominate surface diffusion current for biases greater than a few tens of millivolts, using reasonable assumptions for the surface-state parameters in GaAs [5].

If the generation lifetime were independent of the doping, then increasing the doping would be beneficial to the storage time. Increasing doping reduces the depletion width, and thus the generation volume. Heavier doping also raises the built-in potential of the junction, resulting in reduced bulk generation lifetimes due to field-enhanced generation [6]. The competing effects of smaller generation volume and shorter lifetimes result in a maximum in the storage time performance as the doping in abrupt GaAs p-n junction capacitors is increased.

The effect of doping on storage time has been investigated experimentally using buried-well test structures and the capacitance-transient storage time measurement technique described in [1]. The MBE-grown test structures consist of an n region between two p layers, forming back-to-back diodes which are defined by wet chemical etching. Ohmic contacts are made to the upper and lower p regions while the n region is left floating. The storage time is measured by using a momentary bias pulse to withdraw electrons from the n region and observing the resulting transient in the capacitance as thermal generation refills the well. Devices which are otherwise identical except for the doping in the p regions surrounding the n layer have been examined. Fig. 1 plots the $1/e$ capacitance-recovery time constant versus inverse temperature for devices having p region dopings of $7 \times 10^{15}$ cm$^{-3}$, $10^{17}$ cm$^{-3}$, and $10^{19}$ cm$^{-3}$. In all three samples, the n region was doped at approximately $10^{18}$ cm$^{-3}$, and the n and p regions were made thick enough so that they were never completely depleted at the 2 V bias pulse used in the measurement.

The maximum in the storage time performance as the doping is increased is evident in Fig. 1. The shortest storage times come from the most lightly doped sample. The sample with intermediate doping shows the longest storage times, and the performance of the heavily doped sample is reduced. Also apparent in Fig. 1 is the effect of field-enhanced generation on the activation energies of the samples. Least squares fits to the data show activation energies of 0.79, 0.62, and 0.51 eV for the light, intermediate, and heavy dopings, respectively. The differences in the activation energies agree fairly well with Frenkel's simple one-dimensional model of field-enhanced barrier reduction [6], which is somewhat surprising, because measurements of field-enhanced generation in Si have found the simple theory to predict a much larger effect on activation energy than is actually observed [7]-[9]. The tradeoff between storage time and charge density can be seen in the performance of the two more heavily doped samples of Fig. 1. The individual junctions in the structure with $N_A = 10^{17}$ cm$^{-3}$ have charge densities of 0.68 fC/$\mu$m$^2$ at 1 V reverse bias, while the charge density at the same bias on the junctions of the degenerately doped sample is 2.1 fC/$\mu$m$^2$.

It is possible to retain the long storage times of the sample with the intermediate doping while achieving a charge storage density almost as high as in the degenerately doped sample by inserting a thin undoped layer between the n and p regions. Fig. 2 compares the storage time performance of the degenerately doped sample from Fig. 1 to

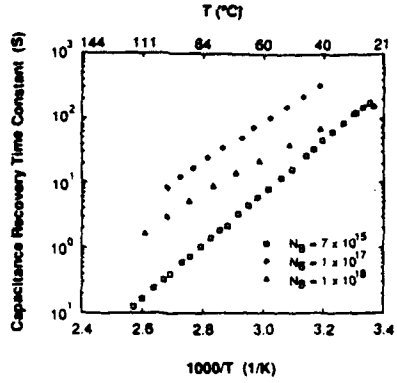


Fig. 1. $1/e$ capacitance recovery time constant of p-n-p storage capacitors for various lighter doped side doping concentrations. In all cases a 1.0 V bias pulse was used to remove electrons from the floating n region.

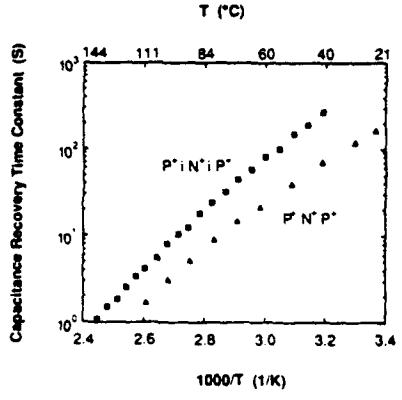


Fig. 2. Storage time performance of heavily doped $p^+$-i-$n^+$-i-$p^+$ and $p^+$-$n^+$-$p^+$ capacitors versus temperature. The reduction of junction electric field through the addition of a thin intrinsic layer increases the capacitor storage time.

that of a device which is identical except for the addition of 300 Å undoped layers between the $p^+$ and $n^+$ regions. The intrinsic region reduces the built-in fields, resulting in improved storage times and a higher activation energy. The storage time of the $p^+$-i-$n^+$ diodes is almost identical to that of the intermediately doped sample from Fig. 1, while the charge storage density at 1 V reverse bias in the $p^+$-i-$n^+$ junction is more than three times as large at 1.9 fC/$\mu m^2$.

In order to measure the capacitance transients, it is necessary for the buried-well structures to be much larger than would be practical for the capacitors of high-density dynamic memory arrays. In a capacitor dominated by bulk generation, the storage time is expected to be independent of the size of the device, because the stored charge and the generation rate scale equally. In a device dominated by generation at the perimeter, the storage time will be inversely proportional to the perimeter-to-area ratio, because the stored charge scales with area while the generation rate scales with the perimeter. The inverse of the storage time constant, which is proportional to the generation rate, can be expressed as

$$\frac{1}{\tau_s} = K[G_B + G_P P/A] \qquad (2)$$

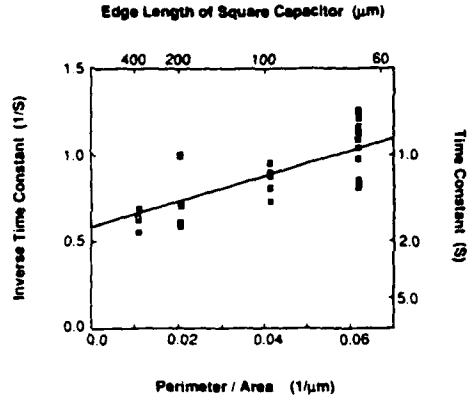


Fig. 3. Storage time performance of $p^+$-i-$n^+$-i-$p^+$ capacitors versus perimeter-to-area ratio at 130.5°C. This plot shows that both bulk generation and perimeter edge generation are significant leakage mechanisms limiting capacitor storage time (see text).

where $G_B$ is the bulk generation rate, $G_P$ is the perimeter generation rate, $P/A$ is the perimeter-to-area ratio, and $K$ is a proportionality constant. The relationship expressed by (2) has been experimentally observed as shown in Fig. 3, which plots inverse time constant versus perimeter-to-area ratio for several differently sized $p^+$-i-$n^-$-i-$p^+$ capacitors at 130.5°C.

The top axis in Fig. 3 shows the edge length of a square capacitor which corresponds to the perimeter-to-area ratio on the bottom axis. The storage time is longest for the largest devices and decreases as the devices become smaller and their perimeter-to-area ratios increase. The line represents a least squares fit of the data. The nonzero vertical intercept indicates the presence of a significant bulk generation component. The positive slope indicates that there is also a significant perimeter generation component. Extrapolating the line off-scale to the right of the figure allows prediction of the performance of very small devices. For example, a 10 × 10 $\mu m^2$ device would have a perimeter-to-area ratio of 0.4 $\mu m^{-1}$ and a storage time at 130.5°C of 730 ms. A 4 × 4 $\mu m^2$ device would have a perimeter-to-area ratio of 1.0 $\mu m^{-1}$ and a 130.5°C storage time of 320 ms. These results indicate that it is possible to produce GaAs diodes which simultaneously provide acceptable charge-storage density and sufficient storage time, even in minimum-dimension devices, for use as storage elements in dynamic memories operating at more than 125°C.

Room-temperature charge storage has also been demonstrated in GaAs p-n junctions formed by ion implantation. Loh *et al.* [10] observed storage times of several tens of seconds at room temperature for diodes formed by implanting Mg to form a shallow $p^+$ region on an n-type VPE epilayer. Recently, room temperature storage times of several seconds have been demonstrated in diodes in which both n and p layers were formed by implantation of Si and Mg [11]. Expected further improvements in ion-implanted capacitors results are important to the design of complete dynamic memory cells, as discussed in Section IV.

## III. Electrical Design Considerations for FET-Accessed Cells

There are many possible choices for access transistor types and cell configurations for one-transistor dynamic memories using p-n junction capacitors. MODFET and bipolar access are being researched, but this discussion will consider only directly connected n-channel MESFET- and JFET-accessed cells, as diagramed in Fig. 4.

The access transistor of a dynamic memory cell must be capable of supplying a very large range of drain-to-source currents. To achieve high-speed operation, the capacitor-to-bitline current must be as large as possible during reading and writing. In the storage state, the capacitor-to-bitline current must be extremely small in order to maintain the small-signal charge on the capacitor between refresh cycles. Without the gate insulator of the MOSFET access transistors used in Si dynamic memory cells, the range of gate biases which can be applied to the gate of a GaAs MESFET or JFET is restricted. If the gate is biased too far forward during cell access, significant current will flow to the capacitor or to the bitline, interfering with proper operation during reading and writing. When the transistor is biased below threshold during the storage state, making the gate potential more negative will cause the transistor-to-capacitor current to reach a minimum and then to slowly increase [12]–[14], reducing the storage time. Also, when the gate is held below threshold so that the channel is completely depleted, a large wordline-to-substrate punchthrough current will flow if the gate and substrate are not at the same potential. To accommodate these considerations, MESFET- and JFET-accessed dynamic memory cell arrays require shifted operating voltages compared to standard DCFL GaAs logic.

To identify the operating voltage requirements, define $\Delta V_{on}$ as the voltage beyond threshold which must be applied to the gate to achieve the desired bitline-to-capacitor current during reading and writing. $\Delta V_{off}$ is the amount of voltage below threshold which must be applied to the gate to reduce the bitline-to-capacitor current to the level needed during the storage state. $V_{GM}$ is defined as the maximum forward bias which can be applied to the gate-to-capacitor or gate-to-bitline junctions before an unacceptably large gate current begins to flow. $V_{high}$ and $V_{low}$ are the logic high and logic low voltages internal to the memory array. The body effect is neglected, so the threshold voltage $V_T$ is a fixed gate-to-source value.

The cell's write sequences relate the logic swing to the threshold voltage and the maximum gate forward bias. For example, to write a one, the bitline is taken to $V_{high}$ and the transistor is turned on. The transistor must remain on until the capacitor charges up to $V_{high}$. This requires that the wordline be held at $V_{high} + V_T + \Delta V_{on}$. The wordline voltage during the write cycle, $V_{WL(on)}$, must not exceed $V_{low} + V_{GM}$ to prevent excessive gate current in other cells connected to the same wordline. Thus

$$V_{WL(on)} = V_{high} + V_T + \Delta V_{on} \le V_{low} + V_{GM} \quad (3)$$

$$V_{high} - V_{low} \le V_{GM} - V_T - \Delta V_{on}. \quad (4)$$

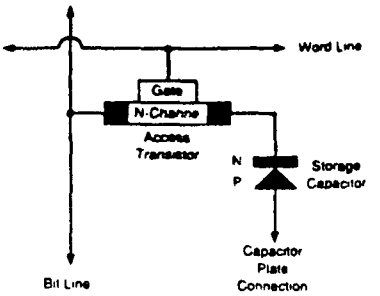


Fig. 4. Directly connected FET-accessed 1-T DRAM cell. The n channel of the FET is directly connected to the n region of a p-n junction storage capacitor.

$V_{GM}$ is established by the access transistor type. Typical values might be 0.6 V for a MESFET and 1.3 V for a JFET. $\Delta V_{on}$ is selected from the access transistor's $I_{DS}$-versus-$V_{GS}$ characteristics to satisfy the write cycle time requirements, and typically must be greater than 0.4 V. Equation (4) shows that once $V_{GM}$ and $\Delta V_{on}$ are established, making the threshold voltage more positive directly reduces the logic swing.

During storage, the capacitor will be at $V_{high}$ or at $V_{low}$, so the gate-to-source bias will never be more positive than $V_{WL(off)} - V_{low}$, where $V_{WL(off)}$ is the wordline voltage in the storage state. To keep the capacitor-to-bitline leakage at an allowable level, the gate-to-source bias must be more negative than $V_T - \Delta V_{off}$, so

$$V_{WL(off)} - V_{low} \le V_T - \Delta V_{off} \quad (5)$$

$$V_{low} \ge V_{WL(off)} + \Delta V_{off} - V_T. \quad (6)$$

The wordline voltage during storage must be chosen to be the same as the substrate voltage to prevent the large gate-to-substrate punchthrough current mentioned earlier. Defining the grounded substrate potential as zero, (6) becomes

$$V_{low} \ge \Delta V_{off} - V_T. \quad (7)$$

The value necessary for $\Delta V_{off}$ is determined by the subthreshold swing of the transistor and the acceptable capacitor-to-bitline leakage in the storage state. The subthreshold swing is defined as the change in gate potential needed to change the subthreshold drain-to-source current by an order of magnitude. Subthreshold swing depends on threshold voltage, gate-to-channel barrier height, channel doping, gate length, and temperature [5]. Assuming that the leakage current in the storage state must be six orders of magnitude lower than at threshold, and using a conservative value of 112 mV/decade for subthreshold swing, an estimate for $\Delta V_{off}$ is 675 mV.

Treating (3), (4), and (7) as equalities, $V_{low}$, $V_{high}$, and $V_{WL(on)}$ can be plotted as a function of threshold voltage, using $\Delta V_{on}$, $\Delta V_{off}$, and $V_{GM}$ as parameters. Fig. 5 shows these relationships for a JFET-accessed memory cell using $V_{GM} = 1.3$ V, $\Delta V_{on} = 0.5$ V, and $\Delta V_{off} = 0.675$ V. $V_{WL(off)}$ is required to be zero. For a specified logic swing, there is an upper limit on the threshold voltage. For $\Delta V_{on}$

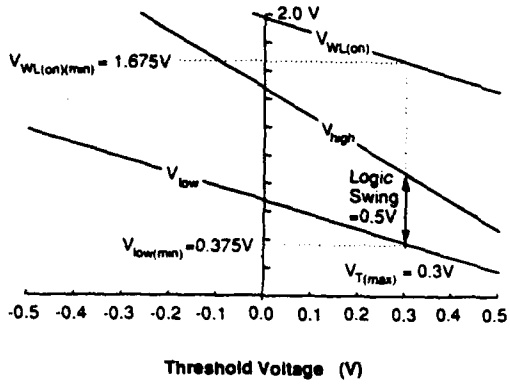


Fig. 5. Operating voltages versus access-transistor threshold for a JFET-accessed DRAM cell.

= 0.5 V and a minimum logic swing of 0.5 V, the figure shows that the most positive JFET threshold is 0.3 V. Similarly, for a MESFET-accessed cell using the same parameters with $V_{GM}$ = 0.6 V, the maximum threshold voltage is −0.4 V.

For a specified logic swing, shifting the threshold negatively will allow larger values of $\Delta V_{on}$. This increases capacitor-to-bitline current during reading and writing. However, more negative threshold voltages also require larger values for $V_{low}$, $V_{high}$, and $V_{WL(on)}$. $V_{WL(off)}$ must remain at ground, so increasing $V_{WL(on)}$ increases the wordline voltage swing, which will eventually increase the cycle time. The wordline-to-capacitor leakage in the "stored one" state increases with $V_{high}$. A maximum lower limit on the threshold is reached when the logic high voltage reaches the gate junction breakdown limit.

Summarizing, given a transistor type, signal charge, desired cycle times, and operating temperature range, the values for $V_{GM}$, $\Delta V_{on}$, and $\Delta V_{off}$ are approximately fixed. $V_{WL(off)}$ is required to be zero. The necessary logic swing is fixed by the sense amplifier design, placing an upper limit on the threshold voltage. The exact target for the threshold voltage below this limit is determined by considering the effects of its variation on operating speed and storage time. The p-type capacitor plate is held at ground, or at $V_{low}$ if the reduced generation and increased signal charge justify the additional dc supply level. The sense amplifiers must translate the shifted logic levels used by the peripheral circuitry.

## IV. Cell Configurations

The physical configuration chosen for the complete GaAs dynamic memory cell will affect the performance of the storage capacitor and the access transistor. For example, the most obvious way to extend the buried-well test capacitors to include an access transistor is to form a JFET by etching through the upper p layer and adding an ohmic bitline contact to the n layer, as shown in Fig. 6. This type of cell has been used to demonstrate the storage time capability of a JFET-accessed cell [12], as described in the next section. Because the same junctions form the transistor and the storage node, the transistor leakage does not greatly reduce the storage time. However, the cell suffers from two problems which point out the need for configurations in which the transistor and capacitor can be optimized separately.

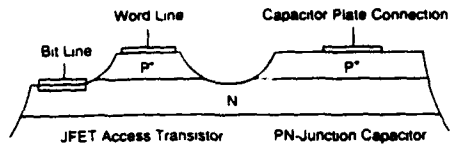


Fig. 6. A simple epitaxial JFET-accessed DRAM cell.

The first difficulty occurs because the doping and thickness of the n layer in the capacitor must be the same as in the transistor channel. Ideally, the doping and thickness of the capacitor's n layer would be much greater than in the transistor channel so that the storage node would not be close to depletion at any logic level. Otherwise, the lateral flow of carriers through the capacitor to the access FET will be restricted, slowing the cell's operation. The second difficulty with the cell design of Fig. 6 occurs because the parasitic capacitance of the bitline and gate contacts must be minimized by using very light doping in the underlying layers. As described in Section II, a large depletion region under the capacitor results in a large generation volume, reducing storage time and increasing collection efficiency for alpha-particle-induced charge.

The first problem can be avoided by using a recess-etched MESFET access transistor as shown in Fig. 7. The $n^+$ layer decreases the bitline resistance and prevents parasitic transistor action in the capacitor, while the MESFET threshold is controlled by the recess etch depth. Such recess-etched epitaxial MESFET's have demonstrated very high transconductances [15]. The lower barrier height of the MESFET compared to the JFET results in increased leakage due to thermionic emission. However, the operation of MESFET-accessed cells has been demonstrated at room temperature, as will be reported in Section V. The configuration of Fig. 7 could also employ a JFET-access transistor by ion-implanting a shallow $p^+$ gate region after the recess-etch.

The problem of confining the depletion region below the capacitor without increasing the parasitic capacitance of the transistor could be solved by using an all-implanted cell as shown in Fig. 8. The p implant beneath the storage node confines the fields in the capacitor, reducing the generation volume and the alpha-particle collection efficiency. The only additions to a standard ion-implanted MESFET process needed to form the cell of Fig. 8 are the deep p implant and the associated alloyed contact. As with the recess-etched cell, a JFET version of the all-implanted cell could be produced using a shallow $p^+$ gate implant. The penalty for using an ion-implanted storage region is increased thermal generation in the capacitor. Complete ion-implanted memory cells have not yet been demonstrated, but the results for isolated implanted capacitors reported in [11] suggest that room-temperature operation should be achievable.

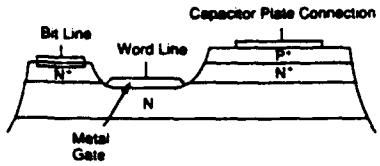


Fig. 7. An epitaxial recess-etched gate MESFET-accessed DRAM cell.

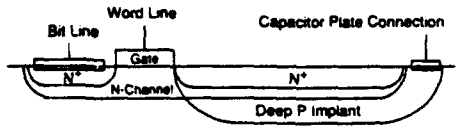


Fig. 8. A planar ion-implanted MESFET DRAM cell. This cell could be fabricated by adding a deep p implant and an associated capacitor plate contact to a standard MESFET process.

## V. Preliminary FET-Accessed DRAM Cell Results

The first complete memory cells constructed and characterized are MBE common-n-channel JFET DRAM cells as shown in Fig. 9 [12]. The cells consist of two 100 × 300 $\mu m^2$ p-n junction storage capacitors surrounded by a 5-$\mu$m ring-gate JFET with a threshold voltage of −1.0 V. As discussed in Section IV, this structure is nonoptimal in that it uses a depletion-mode access transistor with a large perimeter ring gate, the lower junction of the capacitor has a large generating depletion width, and the FET channel layer is used as the n-well of the storage capacitor. Nevertheless, the devices demonstrate full DRAM cell capabilities and storage times sufficient for room-temperature DRAM operation.

Writing of information into the cell is demonstrated in Fig. 10. Logic 1's and 0's are written successively to the cell by quickly pulsing the gate from its off condition ($V_G$ = −1.5 V) to an on condition ($V_G$ = 0) with the bitline held at an appropriate voltage ($V_{Bitline}$ = 0 to write a logic 0, $V_{Bitline}$ = +0.6 V to write a logic 1). The charge state of the storage region, which is monitored by measuring its capacitance, is not affected by changes in the bitline voltage with the gate off, showing good bitline-to-capacitor isolation. Some decay in the capacitance of the storage node in the logic 1 state is observed as charge escapes via capacitor and transistor leakage mechanisms. There is no such decay for a stored 0 since this is the capacitor's zero bias equilibrium state. The $1/e$ storage time of a logic 1 at room temperature is 2 s and the activation energy is 0.627 eV [12].

As shown in Fig. 11, the read capability of the cell is tested by measuring the response of a 0.5-pF active FET probe acting as the bitline. Logic 1's are written to the cell by briefly pulsing the top of the capacitor positive with the access transistor off ($V_{G(off)}$ = −1.5 V). Isolation between the capacitor and the bitline is again confirmed by the lack of response of the active probe to the change in capacitor voltage. A half millisecond later the cell is read by turning on the access transistor causing the

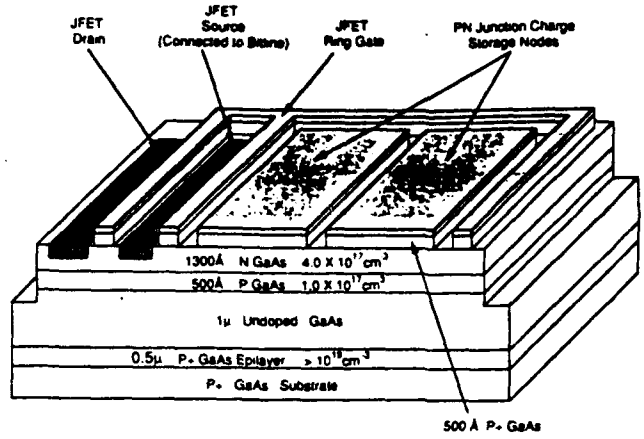


Fig. 9. The first JFET-accessed GaAs DRAM cell test structure [13]. The n GaAs layer is the active channel, and the p+ layers above serve as transistor and storage node gates. The thin p layer below the channel is used to improve the subthreshold characteristics of the JFET and is totally depleted. The storage capacitor plates are 100 × 100 $\mu m^2$, the JFET gate lengths are 5 $\mu$m, and the source and drain contacts are 20 × 300 $\mu m^2$.

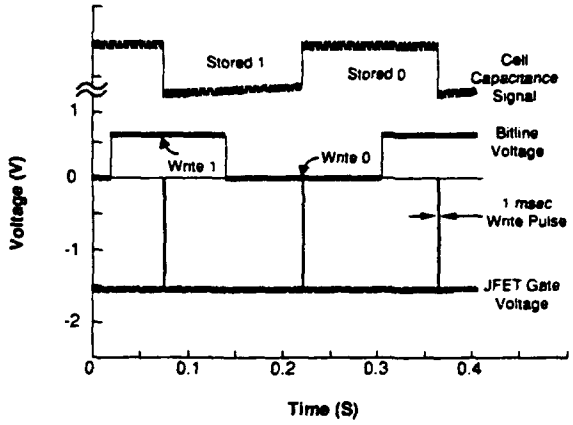


Fig. 10. Pulse train demonstrating writing of 1's and 0's to the JFET-accessed DRAM cell. For this demonstration, the charge on the storage node is monitored by measuring the capacitance. The cell is written when the gate of the access transistor is briefly pulsed to 0 V from its off condition of −1.5 V.

FET probe to respond to the positive charge stored on the capacitor. The leading edge is the important feature of the probe response because in a complete integrated circuit, sense amplifiers would detect and latch the data from the initial voltage excursion of the bitline. The bitline voltage decays in about 250 $\mu$s due to leakage through the resistance of the probe. This also discharges the storage capacitor, which is connected to the bitline through the access transistor. Thus the second gate pulse of Fig. 11 shows the bitline response when an uncharged capacitor (stored 0) is read. The small positive response of the FET probe during the read 0 is due to charge redistribution when the gate is turned on; some electrons from the bitline are needed to fill the shrinking gate depletion area as the gate voltage swings positive.

Depletion-mode MESFET-accessed DRAM cells based on the recess-etch design of Fig. 7 have also been con-

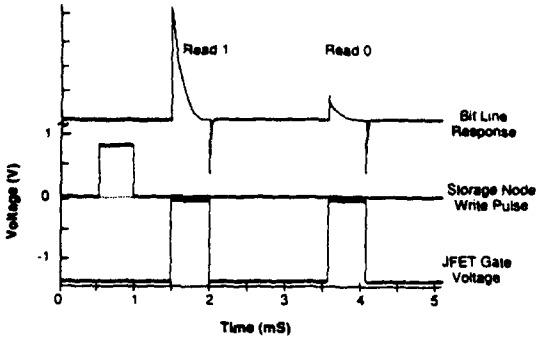


Fig. 11. Waveforms demonstrating that the cell can be read through the access transistor. The top waveform is the potential of the bit line, which is monitored by a low-capacitance active probe. The middle waveform is a pulse applied to the p-n junction storage capacitor to remove electrons and precharge the capacitor to a positive voltage, and the lower waveform is the read pulse train applied to the gate of the access transistor. During the first read operation, the bit line potential goes positive due to charge sharing between the bit line and the positively charged storage capacitor. The rapid discharge is due to the resistance of the probe. The second read operation shows little voltage excursion since the storage capacitor was discharged to a logic zero during the first read.

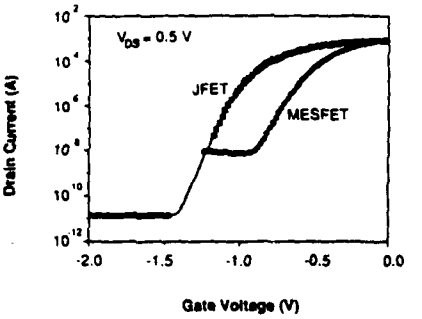


Fig. 12. Comparison of JFET- and MESFET-accessed DRAM cell transistor turn-off characteristics. The increased MESFET leakage is due to thermionic emission over the gate. The storage time of JFET-accessed cell biased at $V_{G(off)} = -1.5$ V was 2 s while the MESFET cell biased at $V_{G(off)} = -1.3$ V was 2.4 ms. The 300 × 5 $\mu m^2$ ring-gate JFET (Figs. 6 and 9) has a 1300 Å thick $4 \times 10^{17}$ $cm^{-3}$ channel while the 300 × 10 $\mu m^2$ recess etched ring-gate MESFET (Fig. 7) has a $4 \times 10^{17}$ $cm^{-3}$ channel that is approximately 750 Å thick. Both transistors feature a depleted buried p-layer (500 Å, $1 \times 10^{17}$ $cm^{-3}$) to improve turn-off characteristics.

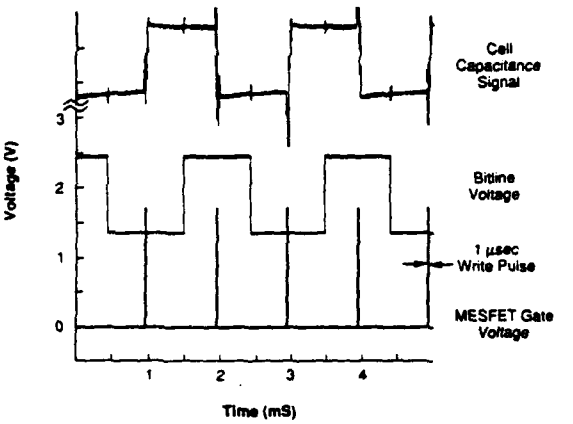


Fig. 13. Pulse train demonstrating write operation of the MESFET-accessed DRAM cells with positively shifted logic levels. The transistor ($V_T = -0.8$ V) is off with $V_G = V_{substrate} = 0$ V so that no gate to substrate current flows in the storage state. This reduces the total power dissipated by the cell in the standby (storage) state to less than 300 nW.

structed. These cells are characterized and operated at room temperature in the same manner as the initial JFET cells. MESFET-accessed cells with nearly the same geometry as the JFET-accessed cell of Fig. 9 exhibit a storage time of only 2.4 ms at room temperature. The drop in storage time is directly attributable to increased gate leakage from the MESFET. Fig. 12 shows drain current as a function of gate-to-source voltage for the transistors of a JFET-accessed cell and a MESFET-accessed cell with nearly identical geometries. The subthreshold current minimum of a GaAs FET is limited by leakage from the reverse-biased gate diode [12]–[14]. Thermionic emission over the lower Schottky barrier of the MESFET results in a much higher current minimum than the JFET, which has a p-n junction gate barrier. The decrease in storage time of the MESFET-accessed cell compared to the JFET cell roughly corresponds to the increased off current of Fig. 12.

For all MESFET cell geometries tested, the gate leakage of the access transistor dominates the leakage of the p-n junction storage capacitors despite the fact that the capacitors have a much larger area. Longer storage times are obtained by shrinking the size of the gate (leakage current) relative to the capacitor (stored charge). A $1/e$ storage time of 1 s at room temperature is observed on a device with a 220 × 220 $\mu m^2$ storage region accessed by two 10 × 50-$\mu m^2$ MESFET's. The MESFET-accessed cells are less temperature-dependent ($E_A = 0.305$ eV) than the JFET-accessed cells ($E_A = 0.627$ eV), so the storage time disparity shrinks with increasing temperature.

As discussed in Section III, minimum power dissipation in the storage state is achieved using positively shifted logic levels to eliminate gate-to-substrate punchthrough current. This is demonstrated for the MESFET-accessed cell in Fig. 13. With the gate and substrate at ground, the access transistor is turned off by shifting the logic low level positive according to (7). The top plate of the capacitor is held at $V_{low} = 1.3$ V, and the bitline swings from $V_{low} = 1.3$ V to $V_{high} = 2.45$ V. The cell is written when the gate of the access transistor is pulsed to 1.7 V. The storage times of the cells do not change significantly with the shift in operating voltages.

The total power consumption in the storage state is less than 300 nW for the MESFET cells and 20 nW for the JFET cells when operated with positively shifted logic voltages to eliminate gate-to-substrate current. These numbers, even though measured on very large cells, compare very favorably to the 1 to 10 $\mu$W per bit of standby power obtainable with GaAs SRAM's [16]. This power advantage is due to the fact that only small leakage currents flow in the DRAM cell when the access transistor is off. Since the leakage currents scale with junction area and perimeter, further improvement in power dissipation

is expected as the DRAM cell is shrunk to practical dimensions.

## VI. Conclusions

p-n junction-capacitor-based GaAs dynamic memory technology has been investigated for very-high speed, medium-density cache applications. The storage time and charge density performance of epitaxial p-n junctions has been investigated as a function of doping. The storage time performance reaches a peak as doping is increased due to the competing effects of shrinking generation volume and increasing field-enhanced generation. Charge storage densities of greater than 2 $fC/\mu m^2$ at 1 V and storage times of greater than 1000 s at room temperature have been obtained simultaneously using $p^+$-i-$n^+$ structures. The perimeter-to-area dependence of the storage time indicates that such capacitors could be scaled to minimum dimensions while maintaining adequate storage time for dynamic memory operation above 125°C. Preliminary results on ion-implanted junctions show that it is possible to achieve several seconds of storage in junctions in which both the n and p regions have been formed by ion implantation.

The operating voltages of GaAs dynamic memory arrays have been considered. A scheme for achieving low-power operation in MESFET- and JFET-accessed cells by using positively shifted logic levels in the array has been presented and demonstrated experimentally. The direct relationship between logic swing and access transistor threshold voltage has been derived as a consequence of the limitation on forward gate bias in GaAs FET's.

Some possible configurations for complete memory cells including both p-n junction capacitors and access transistors have been presented. The detrimental effects of parasitic transistor action with p-n junction capacitors and of unconfined capacitor depletion regions have been discussed. Recess-etched gate and all-ion-implanted cell designs have been proposed to alleviate these difficulties.

The first complete one-transistor dynamic RAM cells in GaAs have been fabricated and characterized. MESFET- and JFET-accessed DRAM cells have shown full read/write capability as well as storage times sufficient for room-temperature operation. When operated using positively shifted logic levels, these nonoptimized cells consume almost two orders of magnitude less standby power than the best commercial GaAs SRAM cells.

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# Arsenic precipitates and the semi-insulating properties of GaAs buffer layers grown by low-temperature molecular beam epitaxy

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Arsenic precipitates have been observed in GaAs low-temperature buffer layers (LTBLs) used as "substrates" for normal molecular beam epitaxy growth. Transmission electron microscopy has shown the arsenic precipitates to be hexagonal phase single crystals. The precipitates are about $6 \pm 4$ nm in diameter with a density on the order of $10^{17}$ precipitates per $cm^3$. The semi-insulating properties of the LTBL can be explained in terms of these arsenic precipitates acting as "buried" Schottky barriers with overlapping spherical depletion regions. The implications of these results on LTBL resistivity stability with respect to doping and anneal temperature will be discussed as will the possible role of arsenic precipitates in semi-insulating liquid-encapsulated Czochralski-grown bulk GaAs.

Recently, a new type of semi-insulating GaAs epilayer, known as a low-temperature buffer layer (LTBL) was found to reduce "sidegating" or "backgating", an important parasitic problem associated with GaAs field-effect transistor circuit technology.[1] Even though there is currently much interest concerning possible applications of this material, there is a certain "mystery" about its chemistry, atomic structure, and electronic properties. Most of this mystery is well documented by Kaminska *et al.*[2] It can be summarized as follows. The LTBL is grown by molecular beam epitaxy (MBE) at about 200 °C using "standard" MBE parameters. Next, this LTBL is used as a "substrate" or "superstrate" upon which film structures for active GaAs devices, such as metal-semiconductor field-effect transistors (MESFETs) or high electron mobility transistors (HEMTs), are grown by MBE at "normal" substrate temperatures, i.e., in the vicinity of 600 °C. If the LTBL is characterized before continued growth or anneal at 600 °C, it has the following properties. At normal excitation intensities there is no measurable photoluminescence (PL) signal compared with that for "normal" buffer layers.[1] The LTBL has a $>1$ at. % excess arsenic over the stoichiometric amount and it is "highly resistive."[2] It has a "giant" electron paramagnetic resonance (EPR) signal corresponding to $5 \times 10^{18}$ As antisites per $cm^3$ and it has a 0.1% larger lattice constant than for bulk GaAs.[2] However, if the LTBL is (1) "annealed" (defined as either a 600 °C, 10 min anneal or used for MBE growth at 600 °C) or (2) grown above 250 °C instead of at 200 °C and with or without a subsequent anneal, its properties change in a peculiar way. It is now found to have a very small PL signal with a decay time $<100$ ps.[3] It still has a $>1$ at. % excess arsenic. It is now uniformly semi-insulating with a lattice constant the same as that for bulk GaAs, and it has no measurable EPR signal (resolution $\sim 10^{18}$ $cm^{-3}$). It has also been observed that LTBLs doped greater than $10^{18}$ Si atoms per $cm^3$ remain semi-insulating after a 600 °C anneal.[4,5]

Given that, to first order the above listed properties of the as-grown LTBL can be explained by the presence of a high concentration of antisite defects, there are at least two intriguing questions which come to mind concerning the annealed LTBL. First, how has the excess arsenic been redistributed? Second, what makes the annealed LTBL remain semi-insulating, especially highly Si-doped layers?

In this letter we show that for our growth conditions we observe the excess arsenic as hexagonal phase arsenic precipitates. Second, we show that the semi-insulating properties of the annealed LTBL can be explained by a simple model in which the arsenic precipitates act as buried Schottky barriers with "spherical" depletion regions. The layers become semi-insulating when either the doping level is low enough or the precipitate density is high enough for the depletion regions to overlap. Since Schottky barriers in GaAs have both large *n*-type (0.8 eV) and *p*-type (0.6 eV) barriers,[6] and thus deplete both donors and acceptors, our model can explain in simple terms why, for example, highly Si-doped annealed LTBLs are semi-insulating.[4,5]

The samples used in this work were grown in a Varian GEN II MBE system. The details of the film growth have been reported previously.[7] Transmission electron microscopy (TEM) images of cross-sectional specimens have shown the existence of a large number of small precipitates in the LTBL. These precipitates give rise to weak spots near spots of GaAs in electron diffraction patterns. By analysis of diffraction patterns and high-resolution electron microscope images, these precipitates have been identified as elemental arsenic having a hexagonal structure.[8] Figure 1 is a dark field image obtained by using one of the spots of


FIG. 1. Dark field image of the GaAs buffer layer grown at a substrate temperature of 220 °C. Arsenic precipitates are seen as bright sphere-like particles.

the arsenic precipitates. A weakly excited (111) spot of GaAs was also included in the objective lens aperture and, hence, gives rise to thickness contours. In the image, arsenic precipitates appear as bright sphere-like particles showing moiré fringes inside. Diameters of the arsenic precipitates range from 2 to 10 nm. Because of the nature of the dark field imaging technique, only a limited number of arsenic precipitates existing in the area can be seen in the observed image. Considering this effect, one can estimate that the density of arsenic precipitates in the LTBL is of the order of $10^{17}$–$10^{18}$ cm$^{-3}$. (This estimate was made by selecting sections of the TEM image where the sample thickness was approximately 1000 Å and counting the observed precipitates.) Using the lower limit of $10^{17}$ arsenic precipitates per cm$^3$ and a cluster radius of 3 nm, we estimate $5\times10^{20}$ atoms of excess arsenic precipitates per cm$^3$ of GaAs which agrees well with the previously reported excess arsenic concentration of over 1 at. %, i.e., $>4\times10^{20}$ arsenic atoms per cm$^3$ of GaAs.[2] More details of the observation and analysis of the TEM images will be reported elsewhere.[9]

Given both the greatly decreased antisite defect concentration in annealed LTBLs and the existence of a high density of precipitates, it is tempting to recall the role of excess arsenic or arsenic clusters in the formation of Schottky barriers at metal/GaAs interfaces. Arsenic clusters can be associated with Schottky barrier formation either through their role in generation of metal-induced gap states (MIGs)[10] or in their role in native defect generation which pins the interface Fermi level at a value which corresponds to the Schottky barrier height.[11] Within this model, arsenic clusters will be surrounded by spherical depletion regions analogous to the planar regions at two-dimensional metal/GaAs interfaces, with characteristic barrier heights of $\phi_{bn} = 0.8$ eV and $\phi_{bp} = 0.6$ eV, for $n$- and $p$-type material respectively. When these depletion regions are isolated, namely for low cluster density, $N_s$, and/or high doping density, $N_D$, the GaAs will be partially compensated but still conducting as shown in Fig. 2(a). In

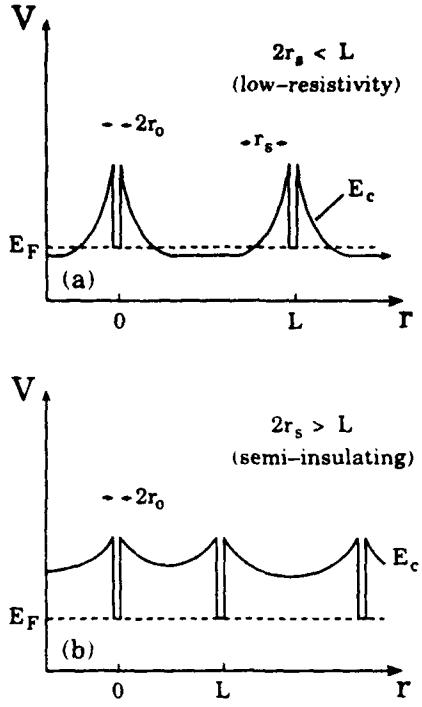


FIG. 2. Band bending for $n$-type semiconductor with isolated Schottky barrier clusters: (a) high doping/low cluster density, (b) low doping/high cluster density.

contrast, for high cluster density and/or low doping density the GaAs will be completely depleted and semi-insulating [Fig. 2(b)]. Solving Poisson's equation, it is found that the maximum depletion radius $r_s$ is related to barrier height $\phi_b$ and cluster radius $r_o$ by

$$\phi_b = (qN_D/6\epsilon)\,[(2r_s^3/r_o) + r_o^2 - 3r_s^2], \tag{1}$$

where $N_D$ is the doping density. For a cluster radius of 3 nm, barrier height of 0.8 eV, and a doping level of $1\times10^{18}$ cm$^{-3}$, the calculated depletion radius is about 190 Å so that depletion spheres will begin to overlap for cluster densities greater than $2\times10^{16}$ cm$^{-3}$. A perhaps clearer explanation is obtained by calculating the amount of charge on a cluster. Laplace's equation gives

$$n_m = (4\pi\epsilon/q)\, r_o\phi_b, \tag{2}$$

where $n_m$ is the number of electron charges. This number, times the cluster density, is the maximum density of dopants that the clusters can compensate, and for 3 nm clusters one obtains $n_- = 22$ and $n_+ = 16$ for $n$- and $p$-type material, respectively. This model implies that for fixed cluster size, compensation limits are proportional to cluster density, as shown in Fig. 3. As can be seen, the cluster density in our LTBL will render GaAs semi-insulating for $N_D < 2.2\times10^{18}$ cm$^{-3}$ and $N_A < 1.6\times10^{18}$ cm$^{-3}$. This value is in good agreement with previous $n$-type doping results in which the annealed LTBL is still semi-insulating for high Si-doping levels.[4,5] It should also be noted that in the crossover regime, where depletion spheres are starting to overlap but the GaAs is not yet completely depleted, conductivity will be affected by percolation behavior and will likely lead to hopping-like conductivity at low temperatures.

We should like to note that the nature of the arsenic

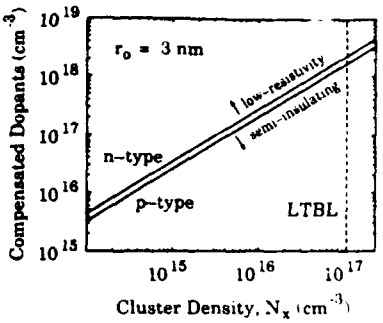


FIG. 3. Conductivity regime for *n*- and *p*-GaAs with 3 nm radius clusters. Upper left corresponds to Fig. 2(a) lower right to Fig. 2(b). The cluster density for the LTBL is indicated.

precipitation will very likely depend on both the thermochemical history of the LTBL and the kinetics associated with the transition from a supersaturated arsenic state to an equilibrium state when the LTBL is annealed. For example, Ref. 2 has no mention of arsenic precipitation. However, using samples similar to Ref. 2 arsenic precipitation has been reported recently.[12–14] Clearly, the excess arsenic concentration in the LTBL is determined by the MBE conditions, especially the As/Ga flux ratio and the substrate temperature during the low-temperature growth phase. The formation and properties of the arsenic precipitates must depend on the details of the anneal, especially anneal time, temperature, and strain environment. In this regard it is quite likely, for example, that a rapid thermal anneal (RTA) to high temperatures (750–900 °C) would cause some fraction of the arsenic precipitates to redissolve in the crystal lattice. This in turn would decrease the precipitate density and would result in highly doped LTBLs converting to low-resistivity material at least for one conductivity type. This effect has been seen in Si-doped LTBLs.[4]

We have recently used LTBL material as the photoconductor in an optoelectronic receiver for THz beams.[15,16] Due to the ultrafast turn-on of the photoconductivity of this material when driven with 70 fs laser pulses, 0.46 ps THz pulse widths were measured. Consequently, the bandwidth of the optoelectronic THz beam system[16] has been extended to beyond 2.5 THz for the first time. Since a photoexcited carrier must on average diffuse 10 nm to the nearest As precipitate, and since normal Schottky barrier contacts can capture both holes and electrons, we interpret our fast optoelectronic response as additional evidence that As precipitates act as buried Schottky barriers.

Finally, in Fig. 3 we extrapolate our results to lower arsenic precipitate densities for the purpose of speculating on the role arsenic precipitates play in rendering bulk liquid-encapsulated Czochralski (LEC) grown GaAs semi-insulating. This speculation is reasonable since deep level defects, i.e., EL2 and/or antisite arsenic defects, have been long correlated with arsenic-rich bulk crystal growth conditions.[17] Also, arsenic precipitates in bulk GaAs crystals have been previously reported.[18] Using Ref. 2 we find that the ratio of excess arsenic in LTBL GaAs to that in bulk LEC GaAs is about 100. In the spirit of speculative arguments we assume that this would correspond to LEC-grown material with an arsenic precipitate density which would be a factor of 0.01 for that of annealed LTBL or $10^{15}$ particles per $cm^3$. A more conservative argument would be that since the maximum EPR signal ($5\times10^{18}$ $cm^{-3}$) is approximately equal to 0.01 times the total excess arsenic concentration ($5\times10^{20}$ $cm^{-3}$) the total excess arsenic concentration in bulk LEC GaAs would be expected to be 100 times its EPR signal ($10^{16}$ $cm^{-3}$). This would be $10^{18}$ arsenic atoms per $cm^3$ or $2\times10^{14}$ precipitates per $cm^3$ assuming 6 nm diameter precipitates. Thus from Fig. 3 we see that for this mechanism, bulk GaAs doped less than mid $10^{15}$ $cm^{-3}$ would be semi-insulating. This agrees qualitatively with the known carrier versus doping properties of LEC GaAs. (It can be shown that the compensation efficiency, namely the ratio of maximum compensation to excess arsenic, is proportional to $1/r_0^2$, so that conditions leading to small clusters will result in even greater compensation limits at the same density of excess arsenic.) The implications of this argument along with the experimental results of this study might lead to the following conjecture. Even though the arsenic antisite defect and the EL2 defect have been well studied and correlated, it is possible that they do not directly contribute to the semi-insulating character of the undoped GaAs found in technology applications. Rather, might it be possible that their signal is indicative of the presence of arsenic precipitates which in turn dominate the semi-insulating properties of undoped arsenic-rich GaAs? This notion might be a fruitful topic of further research.

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# Formation of arsenic precipitates in GaAs buffer layers grown by molecular beam epitaxy at low substrate temperatures

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We have grown film structures by molecular beam epitaxy which include GaAs buffer layers grown at low substrate temperatures (250 °C). The film structures have been examined using transmission electron microscopy. The layers grown at normal temperatures (600 °C) were free of defects or clusters. In contrast, the layer which was grown at low substrate temperatures contained precipitates which have been identified as hexagonal arsenic. The density of the arsenic precipitates is found to be very sensitive to the substrate temperature during growth.

The growth of GaAs by molecular beam epitaxy (MBE) at low substrate temperatures has recently attracted much attention.[1-5] These low-temperature buffer layers (LTBLs) are highly resistive and have been shown to virtually eliminate side gating in GaAs integrated circuits.[1,2] LTBLs have been found to contain an excess of arsenic.[5] We have used transmission electron microscopy (TEM) to examine film structures grown by MBE which include an LTBL. The layers grown at normal substrate temperatures (600 °C) were found to be free of defects. In contrast the layer grown at low substrate temperatures (250 °C) was found to contain precipitates which have been identified as hexagonal arsenic. The formation of the arsenic precipitates is very sensitive to the growth conditions and post-growth "thermo-history" of the sample. This point is clearly evident from previous lack of observation of arsenic precipitates in as-grown LTBLs and LTBLs which were annealed at 600 °C.[5] However, several groups have recently reported the observation of arsenic precipitates in LTBLs following growth of a layer at normal substrate temperatures on top of the LTBL or after an anneal following the growth of the LTBL.[6-8] In this letter we present the details of the MBE of our LTBLs and TEM analysis of our films.

The film used in this work was grown in a Varian GEN II MBE system on a 2-in.-diam liquid-encapsulated Czochralski GaAs substrate. Some of the details of the film growth have been reported previously.[3] However the thermo-history of the sample plays a key role in the formation of the arsenic precipitates. Therefore, a more detailed description of the film growth will be presented so that the TEM results at various levels of the film structure can be correlated with the growth conditions.

The substrate was degreased, etched in a 60 °C solution of 5:1:1 of $H_2SO_4$:$H_2O_2$:$H_2O$ for 1 min and placed in a nonbonded substrate mount. The substrate was outgassed for 2 h at 200 °C in the entry chamber of the MBE, moved to the buffer chamber where it was outgassed for 1 h at 300 °C, and then loaded into the growth chamber. In the growth chamber, the sample was heated to 615 °C for 2 min (the surface oxides desorbed at 580 °C) and then lowered to the initial growth temperature of 600 °C.

The growth rates for all layers were 1 $\mu$m/h with a group V to group III beam equivalent pressure of 16. (The arsenic source was the tetramer $As_4$.) Initially, 0.8 $\mu$m of undoped GaAs was grown. Then the substrate temperature was lowered from 600 to 250 °C during the growth of the next 0.25 $\mu$m of GaAs. The evolution of the reflection high-energy electron diffraction (RHEED) pattern during this lowering of the substrate temperature has been reported previously.[3] After reaching a substrate temperature of 250 °C, 1 $\mu$m of undoped GaAs was grown. The substrate temperature was then ramped back to 600 °C during the growth of the next 0.15 $\mu$m of GaAs. After attaining the normal growth temperature of 600 °C, an additional 0.85 $\mu$m of undoped GaAs was grown. This was followed by the growth of a modulation-doped heterojunction which consisted of a 200 Å $Al_{0.3}Ga_{0.7}As$ spacer layer, an $n$-type 600 Å $Al_{0.3}Ga_{0.7}As$ region, and a 50 Å $n^+$ GaAs cap. The gallium furnace temperature was lowered during the growth of the last 2000 Å of the GaAs before initiating growth of the $Al_{0.3}Ga_{0.7}As$ spacer layer so that the $Al_{0.3}Ga_{0.7}As$ growth rate would be 1 $\mu$m/h. The $Al_{0.3}Ga_{0.7}As$ regions were grown at a substrate temperature of 615 °C.

There was no interruption of the growth process except in the early stages of the GaAs layer grown at a substrate temperature of 600 °C following the growth of the LTBL. The purpose of the growth interruptions (which were of ~15 s in duration) was to see if RHEED oscillations could be observed shortly after completion of the growth of the LTBL. RHEED oscillations were clearly visible indicating a layer-by-layer growth with up to 40 periods being observed after growing as little as 300 Å of GaAs at normal substrate temperatures.

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Hall bridges were fabricated and complete electrical characterization of the two-dimensional electron gas (2-deg) has been reported previously.[3] In brief, the 2-deg exhibited a carrier density of $5.5\times10^{11}$ cm$^{-2}$ and mobility of 7800 cm$^2$/V s at a temperature of 300 K and a carrier density of $4\times10^{11}$ cm$^{-2}$ and mobility of $2.0\times10^6$ cm$^2$/V s at a temperature of 4.2 K. Only recently have there been reports of higher mobilities in a 2-deg,[9–11] clearly indicating high quality MBE material can be grown on top of these LTBLs.

For the TEM observation, (011) cross-sectional samples were prepared by Ar ion thinning. A JEM 2000 EX electron microscope with an ultrahigh resolution objective lens pole piece was used. The spherical aberration coefficient of the pole piece is 0.7 mm which yields a point resolution of 2.0 Å. Bright field images of cross-sectional samples showed a large number of small particles in the area corresponding to the LTBL. Figure 1(a) is a bright field image taken from an area including the LTBL, boundaries of which are indicated by arrows. In the image, the small particles appear as dark circular spots with a nearly uniform distribution. Diameters of observed particles range from 20 to 100 Å, and their density is of the order of $10^{17}$ to $10^{18}$ cm.$^{-3}$ Despite the existence of a large number of particles, no defects such as dislocation lines or dislocation loops were found in the sample, including the LTBL.

In selected area diffraction patterns taken from the LTBL, weak spots appear near the spots of GaAs as seen in Fig. 1(b). The small particles in the LTBL appear with bright contrast in a dark field image taken by using one of these weak spots. This observation suggests that the small particles have a different crystal structure from that of GaAs and have a certain orientation relationship with the surrounding GaAs crystal. By analyzing diffraction patterns and high-resolution electron microscope (HREM) images, these particles have been identified as elemental arsenic having a hexagonal structure with lattice parameters of $a=3.760$ Å and $c=10.548$ Å.[12] Weak spots indicated by arrows in Fig. 1(b) correspond to the (102) and (003) planes of the hexagonal structure. In HREM images, clear lattice fringes are observed in the arsenic precipitates which exist in the thinner parts of the sample. Figure 2 is a HREM image showing one arsenic precipitate. The beam direction is in the [011] direction of the GaAs crystal, and the amount of defocusing is about 450 Å. Lattice fringes corresponding to (102) and (003) planes of the hexagonal structure are seen in the precipitates near the edge of the sample. As expected from diffraction patterns, these lattice fringes are nearly parallel to (111) type lattice planes of GaAs. A part of the area in this precipitate shows an amorphous-like image which is believed to be caused by destruction of the arsenic crystal during the ion thinning. In the precipitates existing in the thicker part of the observed area, no lattice fringes of the arsenic crystal are seen due to overlapping of the arsenic and GaAs crystals, which gives rise to Moiré fringes. These HREM images suggest that the shapes of the arsenic precipitates are spherical or ellipsoidal without having any well-defined boundary planes.

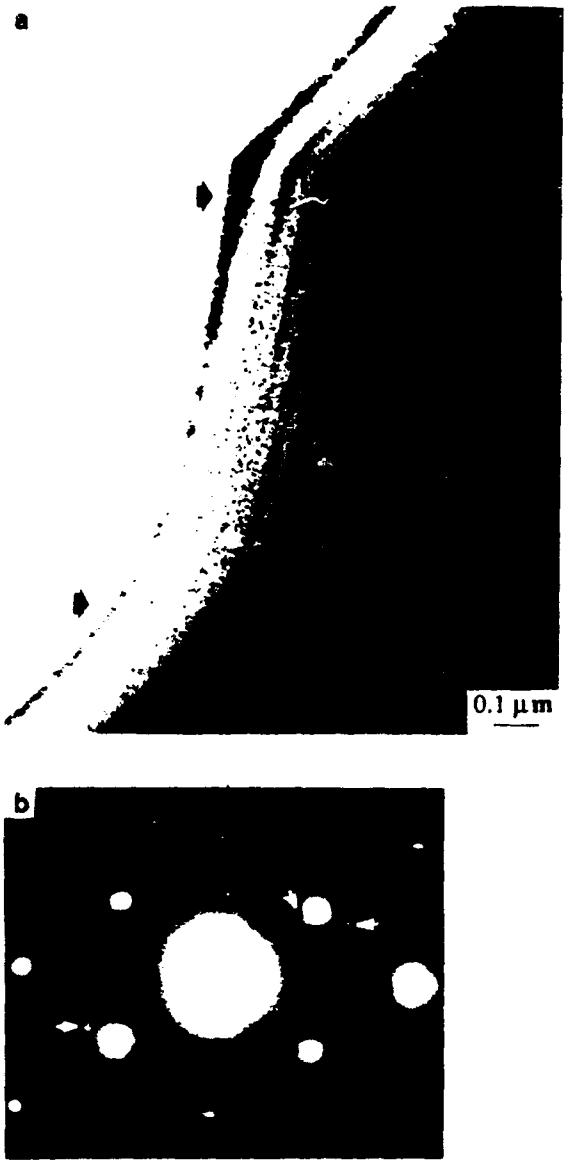


FIG. 1. (a) Bright field image of a cross-sectional sample which includes a LTBL. (b) Electron diffraction pattern taken from the LTBL. Weak spots of arsenic are indicated by arrows.

In earlier TEM studies, the existence of elemental arsenic precipitates were found in annealed arsenic-rich bulk GaAs crystals.[13,14] Diffraction patterns and HREM images of those arsenic particles are very similar to the ones observed in the present study. There is, however, one important difference. In the annealed bulk GaAs crystals, arsenic precipitates are always observed along dislocation lines or inside dislocation loops, which is explained as a result of preferential nucleation of arsenic precipitates on these defects. In our LTBLs, no such defects are found around the arsenic precipitates. The arsenic precipitates in the LTBLs are surrounded by a perfect GaAs crystal and uniformly distributed.

One interesting feature regarding the distribution of the arsenic precipitates is found in the GaAs layer where the substrate temperature was gradually reduced from 600 to 250 °C over a thickness of 0.25 μm prior to the growth

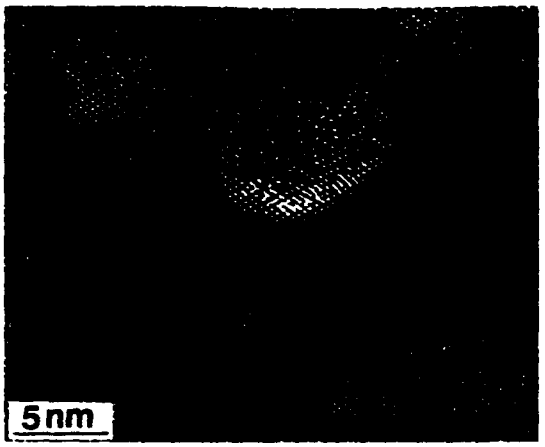


FIG. 2. High-resolution electron microscope image showing one arsenic precipitate in the LTBL.

of the LTBL. Figure 3 is a bright field image taken from this GaAs region. As seen in the image, the density of arsenic precipitates gradually increases towards the LTBL as the substrate temperature was lowered. This observation suggests that the formation of arsenic precipitates occurs even at temperatures considerably higher than the growth temperature of the LTBL (250 °C) and that the density and sizes of the precipitates have a direct correlation with the substrate temperature during the growth of the GaAs.


FIG. 3. Bright field image of the boundary region between the LTBL and the lower GaAs bufter layer. The direction of growth, [100], is indicated by an arrow.

The TEM images reported in this letter were of LTBLs which were grown using $As_4$. We have recently grown LTBLs using $As_2$. We have not investigated the LTBLs which were grown with $As_2$ by TEM, but indications from the optoelectronic response of the material indicate the presence of As precipitates.[15]

In summary, we have observed the formation of arsenic precipitates in GaAs regions which were grown by MBE at low substrate temperatures. For growth at a substrate temperature of 250 °C and an $As_4$ to Ga beam equivalent pressure of 16, the precipitates were found to range in size from 20 to 100 Å with a density of $10^{17}$– $10^{18}$ $cm.^{-3}$ In earlier TEM studies of LTBLs, arsenic precipitates were not observed.[5] In order for the arsenic precipitates to condense, growth of a layer at normal substrate temperatures on top of the LTBL or an anneal sometime following the growth of the LTBL is required as has been observed recently by several groups.[6–8]

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# Electrical characterization of GaAs *PiN* junction diodes grown in trenches by atomic layer epitaxy

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We report the electrical characterization of GaAs *PiN* junction diodes grown over the sidewalls of patterned trenches by atomic layer epitaxy. The diodes exhibit excellent rectifying behavior demonstrating that high quality GaAs was grown on the entire trench structure including sidewalls and corners. The sidewall material is characterized electrically through reverse bias diode leakage from thermal generation in the depletion region. 2-$\mu$m-deep trenches contribute a leakage current of less than 60 $\mu A/cm^2$ of sidewall area under 1 V reverse bias at 144 °C, which is satisfactory for most device applications.

The ability to epitaxially grow high quality III-V layers on sidewalls of patterned mesas and trenches would facilitate the fabrication of many new device structures.[1-3] Atomic layer epitaxy (ALE) is to date the most promising technique for sidewall growth. Metalorganic chemical vapor deposition and molecular beam epitaxy produce nonuniform growth (or no growth) on sidewall surfaces, resulting in inadequate material in areas underneath overhangs and traversing sharp etched corners.[4-7] In contrast, ALE proceeds in a self-limiting fashion that enables growth to take place on all crystal surfaces with greater uniformity.[8] ALE's sidewall growth capability was first demonstrated with GaAs/InGaAs multilayer structures.[9] More recently, intentionally heavily doped ALE sidewall layers were used to reduce the parasitic resistances of a delta-doped field-effect transistor.[10,11] Previous work, however, has failed to address the electrical quality of the sidewall material. One reflection of material quality is leakage due to thermal generation in the depletion region of a reverse-biased diode. Planar ALE diodes have achieved record-low leakages,[12] and most of this leakage current was attributable to surface generation at the etched perimeter of the device. In this letter, we report on the fabrication and characterization of GaAs *PiN* diodes grown over the sidewalls of etched trenches by ALE.

The diodes were fabricated on $N^+$ silicon-doped GaAs (100) substrates. The substrate preparation prior to growth is vital to the quality of epitaxially grown layers. On planar substrates, an etch of several microns is typically employed to provide a pristine surface for initiation of growth with minimal defects. The addition of trenches prior to growth complicates substrate preparation in that the final clean-up must preserve the previously etched trench pattern. The first wafer clean consists of standard solvent rinses and an etch for 1 min in 15 $H_2SO_4$:1 $H_2O_2$:1 $H_2O$. Rectangular trench patterns oriented $\sim 15°$ off the {110} cleaved edges are patterned by standard photolithography. Trenches 2 $\mu$m in depth are wet-etched using 1 $H_3PO_4$:1 $H_2O_2$:3 $H_2O$ for 45 s. The photoresist is stripped with another solvent clean, and a final clean in concentrated HCl for 1 min preserves the trench pattern.

The growth system, conditions, and active layer structure are described in Ref. 12. A 200 nm buffer layer of $2\times10^{18}$ $cm^{-3}$ $N^+$ GaAs is grown, followed by a $1\times10^{18}$ $cm^{-3}$ Se-doped layer, 200 nm thick, which forms the *N* side of the junction. Next, a 30 nm unintentionally doped layer is grown under conditions optimized to achieve a background doping level of less than $10^{15}$ $cm^{-3}$. A 200 nm layer of $1\times10^{17}$ $cm^{-3}$ Zn-doped GaAs is grown as the *P* side of the junction, and the growth is finished by the addition of a 100 nm degenerately doped $P^+$ cap layer. Following growth, gold is evaporated and patterned by lift-off to form a nonalloyed Ohmic contact to the $P^+$ cap layer. Fabrication is completed by a 0.8 $\mu$m patterned mesa etch in 3 $H_3PO_4$:1 $H_2O_2$:25 $H_2O$. A schematic cross section of a mesa-isolated diode with a single trench is shown in Fig. 1.

Leakage currents due to the trenches were characterized using three $100\times100$ $\mu$m diode structures. One diode has a planar top surface, one contains a single $30\times30\times2$ $\mu$m trench (cf. Fig. 1), and one contains nine $10\times10\times2$ $\mu$m trenches. The total horizontal surface area is the same ($10^4$ $\mu m^2$) on each of the three diode mesas. Moreover, the horizontal area at the bottom of trenches is exactly 900

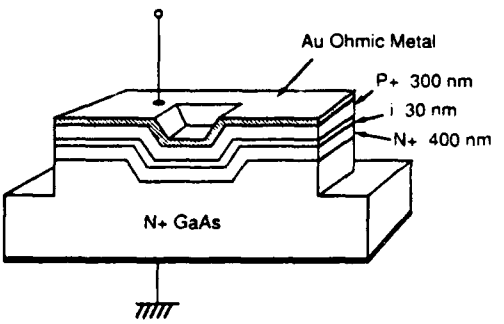


FIG. 1. Schematic cross section of a single-trench mesa-isolated *PiN* diode. The two doping regions in the $N^+$ and $P^+$ layers are omitted for clarity.

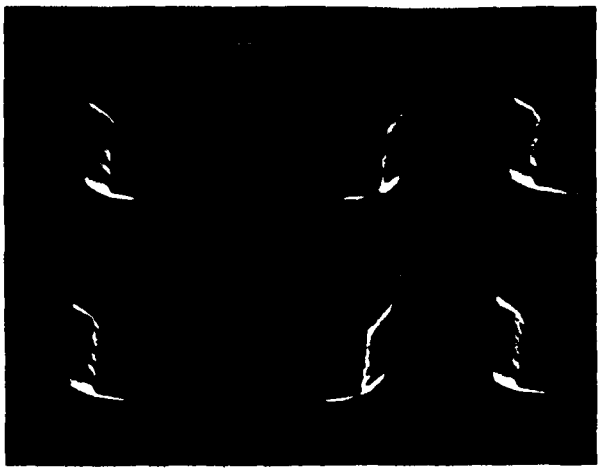

FIG. 2. SEM photo of the nine-trench diode after ALE growth but before metallization. The ALE-grown material covers all visible surfaces, and the surface morphology is smooth. The horizontal scale bar at the top of the photograph represents 10 $\mu$m.

$\mu m^2$ on both the 1-trench and the 9-trench samples. The only difference between the 1-trench and 9-trench samples is the trench perimeter (which has a 3:1 ratio) and the number of trench corners (which has a 9:1 ratio). An independent test structure was used to verify that material in the bottom of the trenches is electrically connected to the top planar surfaces via the ALE-grown sidewalls. Figure 2 shows a scanning electron microscopy (SEM) photograph of the nine-trench structure after ALE growth (but before metallization).

At room temperature the reverse diode leakage currents were below the noise limit of conventional current measurement equipment, so current-voltage ($I$-$V$) characterization was conducted at 144 °C. The $I$-$V$ curves of the three $100\times100$ $\mu$m diodes are given in Fig. 3 along with the $I$-$V$ curve of a $100\times100$ $\mu$m low leakage diode[12] which was fabricated on a planar substrate with no trenches. The nearly identical characteristics of the two planar diodes shows that planar material on the trenched substrate is comparable to the excellent material reported in Ref. 12. Planar devices fabricated entirely on the flat bottom surfaces of large trenches show the same leakage characteristics as planar devices on the top surface.

Figure 4 shows the dependence of leakage on trench

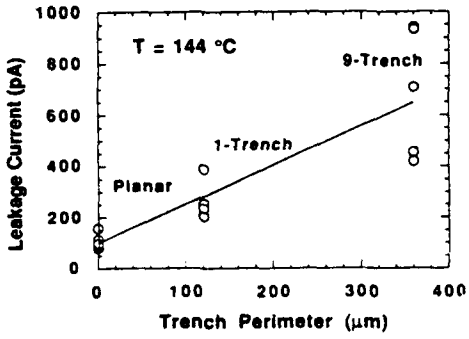


FIG. 4. Dependence of reverse current on trench perimeter at 144 °C and 1 V reverse bias. All samples have the same top surface area ($100\times100$ $\mu$m).

perimeter for several devices of each type. A general linear dependence is apparent, indicating that sidewall leakage scales directly with trench perimeter and not with the number of trench corners. It is not possible from these data to determine whether sidewall leakage actually scales with sidewall perimeter or with sidewall area, since all trenches are the same depth. Further experiments are planned to determine the dependence on trench depth and on trench orientation. However, if the sidewall leakage component is normalized to sidewall area for these samples, we obtain a value of about 60 $\mu A/cm^2$ at 144 °C and 1 V reverse bias, which is quite satisfactory for most device applications.

The reverse-bias sidewall current varies approximately as the square root of applied voltage, which suggests that thermal generation in the depletion region is the primary source of sidewall leakage. The temperature dependence of leakage current at 1 V reverse bias for the three $100\times100$ $\mu$m diodes is given in Fig. 5. The activation energy of leakage current on the 1-trench and 9-trench diodes are nearly the same, at 0.844 eV, while the activation energy of the planar sample is 0.713 eV.

In conclusion, we have fabricated and characterized the first $PiN$ junction diodes from GaAs grown in trenches by ALE. The quality of sidewall material has been measured electrically for the first time through reverse bias leakage due to thermal generation in the depletion region. The leakage current due to the trench sidewalls is significant compared to the current due to the planar surfaces.

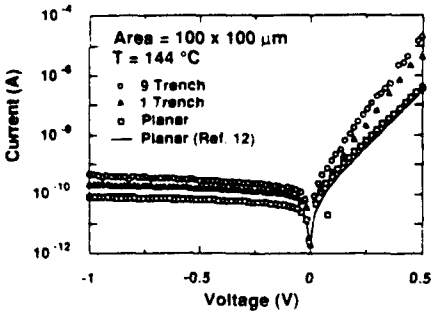


FIG. 3. High-temperature ALE $PiN$ $100\times100$ $\mu$m diode $I$-$V$ characteristics. The solid line is the $PiN$ diode reported in Ref. 12.

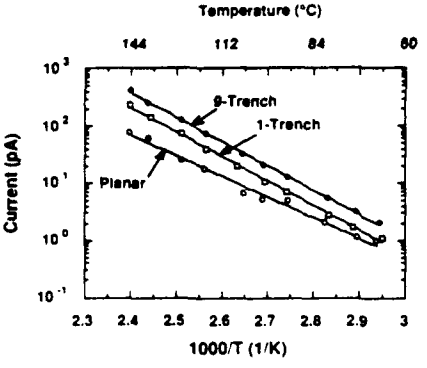


FIG. 5. Temperature dependence of leakage current at 1 V reverse bias for $100\times100$ $\mu$m test diodes.

However, this leakage is low enough for a number of practical device applications.

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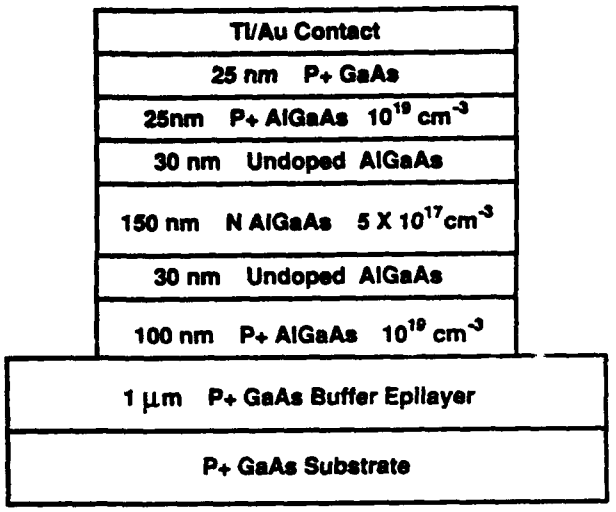


FIG. 1. *PiNiP* $Al_{0.4}Ga_{0.6}As$ charge storage capacitor.

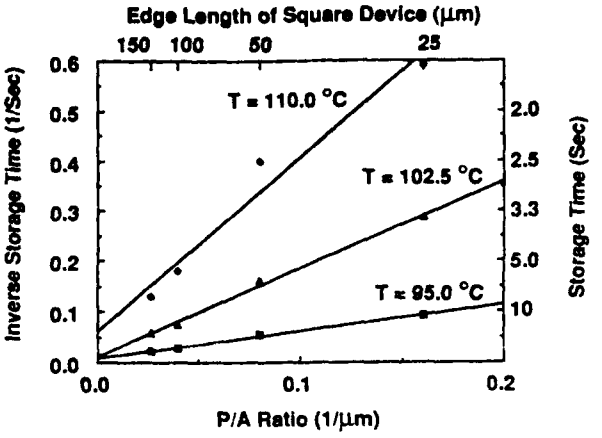


FIG. 3. Inverse storage time as a function of $P/A$ ratio for three different temperatures. The $y$ intercepts are proportional to the bulk generation rate $G_B$ and the slopes are proportional to the perimeter generation rate $G_P$.

An aluminum mole fraction of 0.4 was chosen for the experiment. The epilayers shown in Fig. 1 were grown on a (100) $P^+$-GaAs substrate in a Varian Gen II molecular beam epitaxy system using silicon and beryllium for $n$ and $p$-type dopants. 100 nm of Ti and 200 nm of Au were then deposited in an electron beam evaporation system and patterned by liftoff to form a nonalloyed ohmic contact to the $P^+$-GaAs cap layer. The metal contact layer acted as a mask during a 5 min etch in 3 $H_3PO_4$:1 $H_2O_2$:100 $H_2O$ which isolated the devices.

Figure 2 shows the storage time performance of four sizes of $Al_{0.4}Ga_{0.6}As$ *PiNiP* devices over the temperature range 70–145 °C. The activation energies change with device size, and they do not correspond to half the extrapolated zero-temperature band gap of $Al_{0.4}Ga_{0.6}As$ (extrapolated $E_G/2 = 1.11$ eV as calculated from parameters in Ref. 8). Above half-band-gap activation suggests that nonmidgap centers play a significant role in $Al_{0.4}Ga_{0.6}As$ thermal generation, and the trend of higher activation energies for smaller devices implies that $G_P$ has a higher activation energy than $G_B$.

To resolve the two mechanisms, the bulk and perimeter generation rates at each temperature were calculated by applying (6) to plots of $1/\tau_s$ vs $P/A$ (Fig. 3). The temperature dependence of the two mechanisms is presented in Fig. 4. The bulk generation rate $G_B$ exhibits an activation energy (1.16 eV) that is close to half the extrapolated *zero-temperature* $Al_{0.4}Ga_{0.6}As$ band gap. This temperature dependence is consistent with the theory that near-midgap centers dominate thermal generation in the bulk. In contrast, the measured temperature dependence of $G_P$ does not conform with the supposition that near-midgap surface states dominate perimeter edge generation. Instead, the experimental behavior of $G_P$ can be modeled within the framework of (4) by dominant surface generation centers that are approximately 0.5 eV off the middle of the band gap. Whether these centers lie above or below $E_i$ cannot be

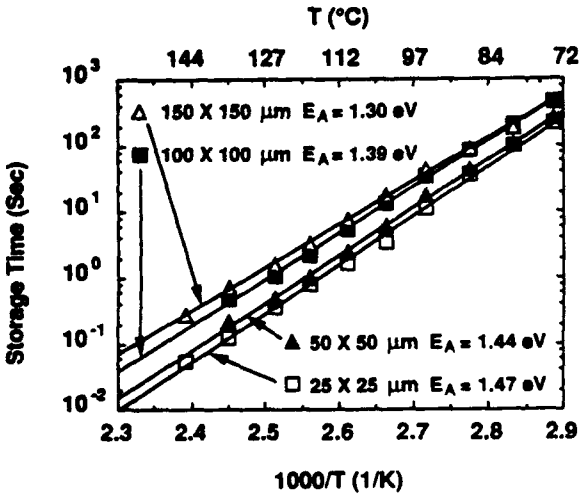


FIG. 2. $1/e$ storage time vs temperature data for *PiNiP* capacitors ranging in size from 25×25 μm to 150×150 μm. A 1 V, 2 s bias pulse was used to initially charge the capacitor.

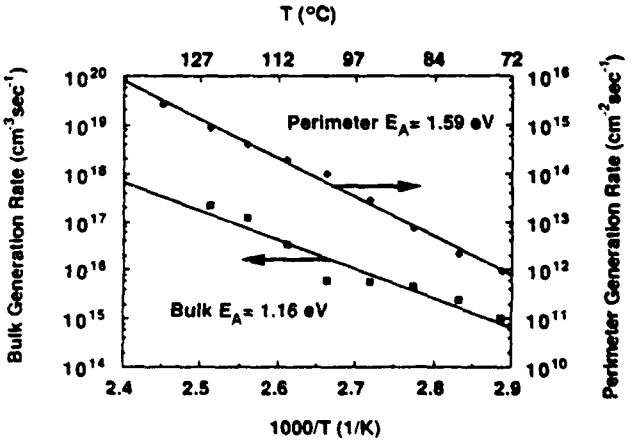


FIG. 4. $Al_{0.4}Ga_{0.6}As$ bulk and perimeter generation rates as a function of temperature. Bulk generation rates were calculated from $y$-intercepts of plots of $1/\tau_s$ vs $P/A$ (Fig. 3), while perimeter generation rates were calculated from the slopes.

directly inferred from these measurements, due to the energetic symmetry of (4).

In conclusion, we have experimentally characterized the mechanisms governing thermal generation in reverse-biased $Al_{0.4}Ga_{0.6}As$ *PiN* junctions. Both bulk and perimeter edge generation are significant leakage mechanisms. The experimental data are consistent with the theory that near-midgap centers dominate generation in the bulk, while perimeter generation appears to be governed by centers that are around 0.5 eV above or below $E_i$.

This work was supported by SDIO/IST under Grant N00014-88-0527, and by ONR under Grant N0014-89-J-1864.

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# Subpicosecond, freely propagating electromagnetic pulse generation and detection using GaAs:As epilayers

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Using GaAs epilayers with arsenic precipitates (GaAs:As) as the photoconductive material in a broad-band optoelectronic terahertz beam system, we have generated and detected freely propagating, subpicosecond electromagnetic pulses. The receiver signal gave a measured integrated pulse width of 0.71 ps. Fast photoconductive rise times have been achieved which are characteristic of good mobility GaAs. In addition, the material exhibits a short "effective" carrier lifetime of several ps due to the embedded, closely spaced (about 20 nm) arsenic precipitates.

The use of subpicosecond pulsed laser technology to drive photoconductive switches [1] has led to a widespread interest in the development of ultrafast optoelectronic materials and devices which can generate and detect subpicosecond electrical pulses.[2–10] Generally, achieving ultrafast optoelectronic performance depends on both the properties of the photoconductive material and the configuration of the sampling device. Nonetheless, it is well understood that the ideal photoconductive material would have high dark resistivity, high carrier mobility, and short carrier lifetimes. Such material would exhibit a fast rise time, high output signal, and a fast turn-off time. The best previously studied subpicosecond material, namely, implanted silicon-on-sapphire (SOS), achieved short carrier lifetimes via high defect densities—this results in excellent receiver noise characteristics, but compromises somewhat the carrier mobility and pulse rise time, and thereby the ultimate high-frequency performance.

An alternative photoconductive material is GaAs grown by molecular beam epitaxy (MBE) at 200–250 °C (LT GaAs). As grown, this material contains roughly 1% excess As, producing an extreme concentration of bulk defects.[11] When used as the photoconductive material in a transmission line, electrical pulse "launcher,"[9] it produced an electrical pulse width of 1.6 ps and a large improvement in signal amplitude over SOS-based structures. From that study, its authors surmised an electron mobility of 200 $cm^2/V$ s. Since then, electrical pulses as short as 0.6 ps have been generated on coplanar transmission lines with this material.[10]

Recently, it has been shown that under certain annealing conditions, the excess arsenic in LT GaAs will coalesce into arsenic precipitates (GaAs:As) about 6 nm in diameter with an average spacing of about 20 nm.[12] In this letter we demonstrate the relatively large signal generation and detection of subpicosecond freely propagating electromagnetic pulses using these GaAs:As epilayers as the photoconductive emitters and detectors in a complete, broadband optoelectronic terahertz beam system.[5,6] Our results indicate that the photoconductive response of the GaAs:As material consists of an ultrafast, subpicosecond turn-on time similar to that for "normal" GaAs, but followed by a turn-off time of several picoseconds. Consequently, for the transmitter the emitted THz pulse is produced by the leading transient. Similarly, this photoconductive response "gates" the receiver so that it operates in an integrating mode, where the high-frequency limit is determined by the sharpness of the photoconductive rise time.

Since the process windows which produce GaAs:As are not yet well established, the details of the relevant epigrowth procedure will be described. The epilayers used in this study were grown in a Varian GEN II molecular beam epitaxy (MBE) system on a 2-in. diam, liquid-encapsulated-Czochralski (100) GaAs substrate. The substrate was degreased, etched in a 60 °C solution of 5:1:1 of $H_2S0_4$:$H_2O_2$:$H_2O$ for 1 min and placed in a nonbonded substrate mount. The substrate was outgassed for 2 h at 200 °C in the entry chamber of the MBE, moved to the buffer chamber where it was outgassed for 1 h at 300 °C, and then loaded into the growth chamber. In the growth chamber, the sample was heated to 615 °C for 2 min (the surface oxides desorbed at 580 °C) and then lowered to the initial growth temperature of 600 °C.

The growth rate for all layers was 1 $\mu$m/h, with a group V to group III ratio (beam equivalent pressure) of 22. The arsenic source used was the dimer $As_2$. First, 0.75 $\mu$m of undoped GaAs buffer was grown. Then the substrate temperature was ramped from 600 °C to 250 °C, during the growth of the next 0.25 $\mu$m of GaAs. After reaching a substrate temperature of 250 °C, 1 $\mu$m of undoped GaAs was grown. The substrate temperature was then ramped back to 600 °C during the growth of the next 500 Å of GaAs, and the structure was capped with an additional 100 Å of undoped GaAs. The structure growth was followed by an *in situ* anneal in the $As_2$ flux for 1 h at 600 °C. The substrate was rotated at 5 rpm during the growth of all layers and during the one hour 600 °C anneal. Transmission electron microscopy revealed arsenic precipitates (6

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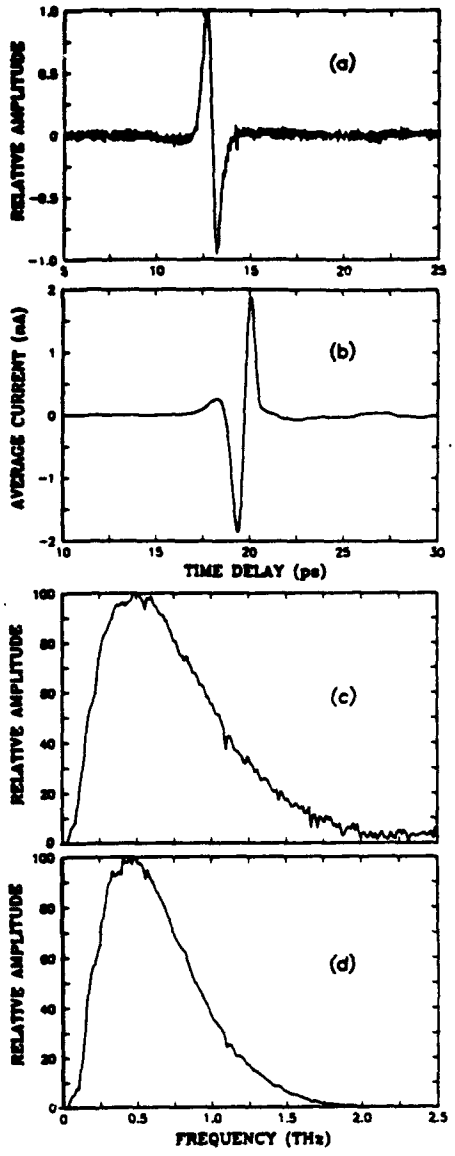


FIG. 2. Direct comparison between GaAs:As and SOS receivers, using a GaAs:As transmitter (the difference in time delay is arbitrary): (a) Numerical derivative of the measured GaAs:As receiver pulse shown in Fig. 1(b); (b) measured SOS receiver pulse; (c) amplitude spectrum of derivative pulse in (a) (GaAs:As); (d) amplitude spectrum of pulse in (b) (SOS).

receiver operates in an integrating mode, in contrast to SOS operation in a sampling mode, a more direct pulse width comparison was made by using a GaAs:As transmitter with both receivers, but differentiating the GaAs:As receiver results. Figures 2(a) and 2(b) show these signals for GaAs:As and SOS, respectively, yielding minimum-maximum differences of 0.58 ps for the numerical derivative of the GaAs:As receiver signal and 0.67 ps for the SOS. The derivative signal has the opposite polarity compared to the SOS signal, because the original GaAs:As signal is proportional to the negative integral. It should also be noted that the measured pulse width is extremely sensitive to precise alignment of the silicon lens, which we optimized for each antenna. Figures 2(c) and 2(d) show the amplitude spectra for 2(a) and 2(b), respectively, illustrating a slight advantage in bandwidth for the GaAs:As signal after differentiation. Lastly, by comparing noise levels in the GaAs:As and SOS receivers, it is estimated that the photoexcitation decay in the GaAs:As is on the order of 2 ps, which is consistent with mediation by sparse As clusters rather than a high density of bulk defects (as in SOS or LT GaAs). Because of the indirect nature of this pulse shape inference it would be dubious to attempt a rigorous direct comparison with earlier LT GaAs work.[9] Nevertheless, the above results and corroborating DLTS measurements[14] suggest a quality now approaching that of intrinsic GaAs.

In conclusion, we have demonstrated an optoelectronic THz beam transceiver system, which uses GaAs:As as the photoconductive material in the laser driven Auston switches. The system generates relatively powerful subpicosecond pulses of THz radiation. Our measured integrated pulse widths of 0.71 ps indicate that the GaAs:As photoconductive material has the desired combination of an ultrafast, subpicosecond turn-on time, due to the excellent mobility in the high-quality, epitaxial material, together with a reasonably short carrier lifetime of several picoseconds due to the high density of As clusters acting as recombination centers.

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# Robust infrared gratings in photorefractive quantum wells generated by an above-band-gap laser

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Probe beam intensities more than an order of magnitude larger than pump beam intensities do not erase photorefractive gratings during nondegenerate four-wave mixing in photorefractive GaAs/AlGaAs quantum wells. The pump and probe laser wavelengths are absorbed in spatially separated regions of the multilayer structure. The photoconductivity of a probe beam around 840 nm is confined to the GaAs quantum wells and cannot easily erase the trapped space-charge gratings in the AlGaAs barriers written by an above-band-gap HeNe laser at 633 nm. This allows a weak visible control beam to modulate a strong infrared signal beam.

A requirement of any efficient control system is the ability to control strong signals with weak signals. In bulk photorefractive devices this ideal has been elusive because probe beams erase photorefractive gratings, forcing the pump lasers to have intensities equal to or larger than probe beams. Recent work has begun to combine the resonant quadratic electro-optic effects associated with excitonic absorption,[1,2] with semi-insulating materials to produce high-sensitivity photorefractive devices.[3-5] In this letter, we use nondegenerate four-wave mixing in semi-insulating multiple quantum wells (SIMQWs) of GaAs/AlGaAs to spatially isolate the photoconductivity of the probe beam from the space-charge gratings generated by a visible HeNe laser. By isolating the probe photoconductivity to the GaAs quantum wells, the gratings in the AlGaAs barriers are not easily erased. Probe intensities therefore can be more than an order of magnitude larger than the pump intensity without erasing the grating.

The photorefractive sample is a SIMQW structure.[4] A superlattice with 60 periods of alternating 75 Å GaAs wells between 100 Å $Al_{0.3}Ga_{0.7}As$ barriers is grown on top of 8000 Å of AlGaAs stop-etch layers. A cap of $Al_{0.3}Ga_{0.7}As$ 500 Å thick was grown on top of the multiple quantum wells. The active photorefractive interaction length is 1.05 $\mu$m, the thickness of the multiple quantum well superlattice. After growth, the sample was proton implanted from the surface using 160 keV protons at a dose of $10^{12}$ cm$^2$. The proton implant introduces defects that pin the Fermi level mid gap, producing semi-insulating material.[6] The sample was mounted on a glass slide with epoxy and the substrate was removed by a selective etch that stops at the $Al_{0.5}Ga_{0.5}As$ stop-etch layer. The sample was proton implanted again with the same dose and implant energy from the stop-etch side to ensure that the entire structure was semi-insulating. Gold contact strips were evaporated on the stop-etch layer with a separation of 1 mm. A voltage applied to these contacts generates an electric field inside the thin sample that is parallel to the quantum well planes.

The electric field modifies the optical properties of the excitons through the Franz–Keldysh effect. For the experiments, the wavelength ranges of interest are 825–845 nm, at the excitonic absorption, and 633 nm at the wavelength of the HeNe laser. The HeNe photon energy is large enough to excite electron-hole pairs in the quantum wells as well as the AlGaAs barriers and buffer layer. This laser therefore experiences absorption throughout the device thickness. In contrast, the 840 nm light is absorbed only in the GaAs quantum wells. The sample absorption coefficient at $\lambda = 840$ nm is $\alpha = 1.4\times10^4$ cm$^{-1}$ (considering an interaction length of 1.05 $\mu$m) and at $\lambda = 633$ nm is $\alpha = 2.8\times10^4$ cm$^{-1}$ (considering an interaction length of 2 $\mu$m). The dark conductivity of the sample is $\sigma_d = 10^{-6}$ S after proton implantation. The absorption as a function of wavelength exhibits sharp excitonic absorption at room temperature. The heavy hole exciton width is 5 meV, and the light hole exciton width is 6 meV. Electroabsorption measurements at 837 nm yield a change in transmission of 8.8% for an applied field of 7 kV/cm.

The nondegenerate optical mixing geometry is shown in Fig. 1. The HeNe laser writes the holographic gratings with two beams that intersect inside the sample between the two electrodes. The half-angle $\theta_w$ between the two write beams is 8°, yielding a grating spacing of 2.2 $\mu$m in the quantum well sample. The sample is oriented so that the write beams enter from the quantum well side. The internal gratings are probed by a Spectra-Physics Ti:Sapphire laser pumped by a 5 W argon ion laser with tunable wavelengths between 825 and 845 nm, spanning the exciton absorption. The diffracted signal is detected by a Si photodiode through a 750 nm longpass filter. Lock-in detection is performed by modulating the applied electric field on the sample and locking in at the modulation frequency. The photocurrent was monitored to ensure that there was no Joule heating of the sample.

The thin grating in the 1 $\mu$m interaction length of the SIMQW allows Raman–Nath diffraction.[7] This simplifies the experiment, because Bragg conditions are satisfied for all incident probe-beam angles. The probe is directed perpendicular to the sample between the electrodes. The dif-

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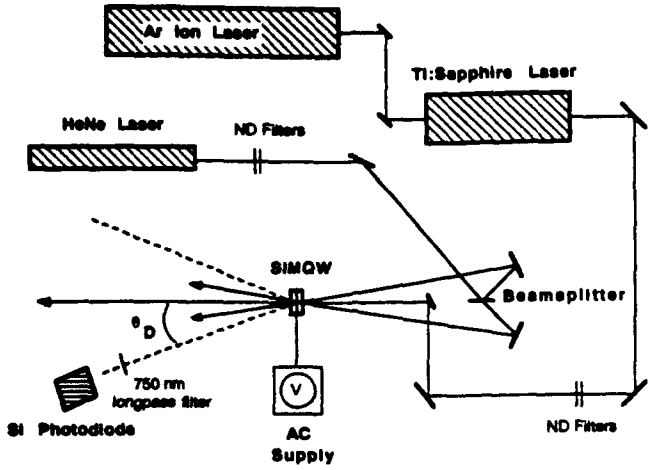


FIG. 1. Nondegenerate four-wave mixing geometry for measuring the infrared gratings generated by the HeNe laser. The ac field modulates the diffraction into the Si detector.

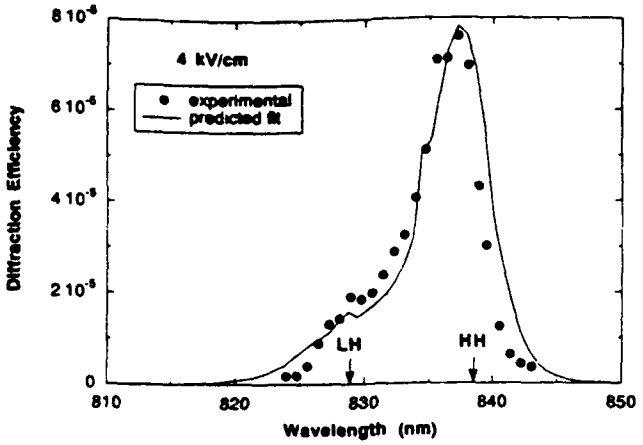


FIG. 2. Diffraction efficiency as a function of wavelength for an applied field of 4 kV/cm at 290 Hz. The Ti intensity was 4 mW/cm$^2$, and the HeNe intensity was 20 mW/cm$^2$. The predicted fit is obtained from electroabsorption data and Eq. (2), adjusting only the peak diffraction efficiency to fit the data.

fracted signal in the $m$th diffraction order is detected at an angle $\theta_D$ given by

$$\sin(\theta_D) = 2m \frac{\lambda_p}{\lambda_{\text{HeNe}}} \sin(\theta_w), \tag{1}$$

where $\lambda_p$ is the probe wavelength and $m$ is the diffraction order. For a probe wavelength of 837 nm, the detection angle for the first-order diffraction is $\theta_D = 22°$. The diffraction efficiency into the $m$th order is given by

$$\eta_m = J_m^2 \left| \left( \frac{2\pi \Delta n L_{\text{int}}}{\lambda_p \cos \theta_p} \right) + \left( \frac{i \Delta \alpha L_{\text{int}}}{2 \cos \theta_p} \right) \right|, \tag{2}$$

where $J_m$ is a Bessel function of the first kind, $\Delta n$ and $\Delta \alpha$ are the first Fourier components of the excitonic electrorefraction and electroabsorption, $\theta_p$ is the internal angle for the probe beam (in our case $\theta_p = 0$), and $L_{\text{int}}$ is the SIMQW thickness. In this letter, we consider diffraction into the first order. Diffraction from higher orders, or from second Fourier components, will be discussed elsewhere.

The diffraction efficiency from the first order as a function of wavelength is shown in Fig. 2 for an applied ac field of 4 kV/cm at 290 Hz. The points are the experimental data. The HeNe intensity was 20 mW/cm$^2$, with the probe intensity at 4 mW/cm$^2$. The solid curve is the predicted diffraction efficiency based on electroabsorption data and Kramers–Kronig analysis.[8] The height of the predicted curve is fit to the diffraction data, but has no other adjustable parameters. The diffraction efficiency reaches a peak near 837 nm. The positions of the heavy and light hole excitons are included in the figure. A diffraction efficiency of $8 \times 10^{-5}$ is observed near the peak for this electric field magnitude. This diffraction efficiency is comparable to the diffraction efficiencies obtained in bulk GaAs for nonresonant excitation,[9] in spite of the fact that the interaction length is four orders of magnitude smaller!

A requirement for any control device is the ability for a weak control input to control or modulate a strong signal. Large values for the signal-to-control ratio $I_s/I_c$ are possible using nondegenerate mixing in the photorefractive quantum wells. The HeNe pump is absorbed everywhere, but the Ti probe is absorbed only in the quantum wells. This isolates the photoconductivity of the probe away from the space-charge gratings in the barriers, allowing a weak control beam to control a strong signal beam, analogous to a weak base current controlling a strong collector-emitter current in a transistor. The diffracted signal intensity is expressed as a fraction $\eta$ of the incident probe intensity. The dependence of the diffracted intensity on the incident probe intensity and on photoconductivity is given approximately by

$$I_{\text{Ti}}^{\text{diff}} = I_{\text{Ti}}^{\text{inc}} \eta_{\text{sat}} (1 + \sigma_{\text{Ti}}/\sigma_{\text{He}})^2 , \tag{3}$$

where $\eta_{\text{sat}}$ is the saturation diffraction efficiency at low probe intensities, and $\sigma_{\text{Ti}}$ and $\sigma_{\text{He}}$ are the photoconductivities for the probe and pump lasers. The second power derives from the quadratic electro-optic effect.[4] When the photoconductivity of the Ti:Sapphire probe laser exceeds the photoconductivity of the HeNe pump laser everywhere, then the gratings are erased and the diffracted signal decreases. The diffracted signal as a function of the Ti:sapphire laser intensity is shown in Fig. 3 for a HeNe intensity of 2 mW/cm$^2$. The data at 837 nm are from the peak in the diffraction efficiency, and the data at 840 nm are from the zero-crossing of the electroabsorption on the low-energy side of the heay-hole exciton. The diffracted signal goes through a maximum as the probe intensity is increased. The fivefold increase in the peak probe intensity on detuning from the exciton resonance reflects the exponential decrease of the absorption coefficient for photon energies below the band edge.[10]

A control parameter $\beta'$ (analogous to current gain in a transistor) can be defined as the ratio of the incident probe beam intensity to the pump beam intensity for which the diffracted signal is a maximum. Ideally, $\beta'$ should be as large as possible. An expression for $\beta'$ is derived from Eq. (3) by relating photoconductivity to absorption, giving

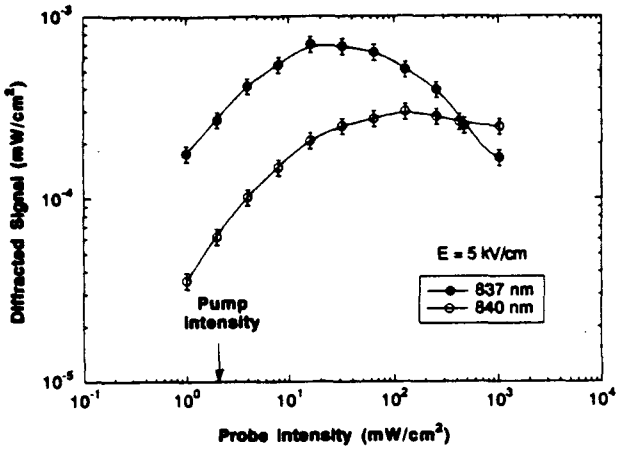


FIG. 3. Diffracted signal as a function of probe intensity for a pump intensity of $I_{HeNe} = 2$ mW/cm$^2$, and an ac applied field of 5 kV/cm. Charge trapped in the AlGaAs barriers cannot be erased directly by the probe intensity, leading to gratings that persist for probe intensities nearly 100 times larger than the pump intensity. The data at $\lambda = 837$ nm and $\lambda = 840$ nm demonstrate the increasing persistence of the gratings as the wavelength is detuned from the exciton.

$$\beta' = \left(\frac{I_{Ti}^{inc}}{I_{HeNe}}\right)_{max} \approx \frac{\lambda_{He}}{\lambda_{Ti}} \frac{\alpha_{He}}{\alpha_{Ti}}. \quad (4)$$

Based on Eq. (4), the control parameter is $\beta' \approx 0.5$ for the gratings to be erased in the GaAs wells, where the absorption is large for both laser wavelengths. However, the parameters obtained from Fig. 3 are $\beta'_{837} = 10$ and $\beta'_{840} = 50$, more than an order of magnitude larger. This is because the absorption of the probe wavelengths in the AlGaAs barriers is negligible: $\alpha_{Ti} \approx 1$ cm$^{-1}$. *The infrared probe laser cannot erase the gratings that are generated in the quantum well barriers by the visible laser!* This situation is unique to photorefractive multilayer structures. The pump and the probe beams are absorbed in different portions of the structure. Therefore the space-charge fields stored in the AlGaAs barriers do not erase with increasing probe intensity until sufficient carrier density is developed in the GaAs wells such that appreciable numbers of carriers can overcome the barriers through thermionic emission or tunneling.

The $\beta'$ factor can be increased further if the barriers are made wider and if the band-edge discontinuity is increased. This would decrease both tunneling and thermionic emission. Substantial charge could then be stored in the space-charge gratings in the barriers, relatively unaffected by the probe beam. More work is necessary to study the limits of space-charge isolation from the probe photoconductivity. In particular, relaxation of the space-charge through thermionic emission of carriers from the quantum wells will be strongly temperature dependent, which should distinguish that relaxation mechanism from tunneling of the carriers into the barrier. Further applications of above-band-gap lasers also need to be explored, because in the thin multilayer structures one is no longer restricted to use lasers with below-band-gap wavelengths. This opens a wide new range of flexibility in the engineering of multilayer photorefractive materials.

In conclusion, we have demonstrated the use of above-band-gap laser wavelengths to write holographic gratings in a semiconductor quantum well structure. The strong absorption at the HeNe wavelength in GaAs normally makes it impossible to use this common laser for bulk photorefractive experiments. The thin interaction length of the SIMQW, on the other hand, allows transmission of the writing beams, producing intensity gratings throughout the interaction length. The infrared probe beam is unable to erase the space-charge gratings generated in the AlGaAs barrier layers, leading to a significant persistence of the infrared grating for probe intensities much larger than the HeNe pump intensity, allowing a weak control beam to control a strong signal beam.

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# GaAs buffer layers grown at low substrate temperatures using $As_2$ and the formation of arsenic precipitates

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We have grown GaAs layers by molecular beam epitaxy at low substrate temperatures (250 °C) using the dimer arsenic source $As_2$. Following a one hour anneal at 600 °C, the GaAs layers were examined with transmission electron microscopy. The GaAs layers contained arsenic precipitates of average diameter 100 Å and density of $10^{17}\,cm^{-3}$.

GaAs buffer layers grown by molecular beam epitaxy (MBE) at low substrate temperatures (LT-BLs) have been attracting attention because they can be used to eliminate sidegating in field effect transistors (FETs) [1–3]. In addition, the layers which are grown at normal substrate temperatures on top of LTBLs exhibit extremely high electrical quality [4]. By growing at low substrate temperatures, excess arsenic is incorporated into these buffer layers [5]. Raising the substrate temperature back to normal growth temperatures results in the excess arsenic forming precipitates [6]. These arsenic precipitates then act as buried "Schottky barriers" whose overlapping depletion regions render the material semi-insulating [7]. What is truly remarkable is that the GaAs material between the Schottky barriers exhibits mobility indicative of "normal" GaAs [8]. This combination of buried Schottky barriers in high quality GaAs makes LTBLs an excellent material for optoelectronic applications [8,9]. Previously, all LTBLs have been grown using the tetramer arsenic source $As_4$. Using an LTBL grown with the dimer arsenic source $As_2$ as the photoconductive material in a broad-band receiver, we have been able to generate and detect electrical pulses with full width at half maximum of 0.71 ps [8]. In this paper we describe the growth of LTBLs using the dimer arsenic source, present transmission electron microscopy (TEM) analysis of these LTBLs, and compare LTBLs grown with $As_2$, and $As_4$.

The films used in this work were grown in a Varian GEN II MBE system on 2-inch diameter undoped semi-insulating liquid-encapsulated Czochralski (100) GaAs substrates. The substrates were degreased, etched in a 60 °C solution of 5 : 1 : 1 of $H_2SO : H_2O_2 : H_2O$ for 1 min and placed in non-bonded substrate mounts. The substrates were outgassed for 2 h at 200 °C in the entry chamber of the MBE, moved to the buffer chamber where they were outgassed for 1 h at 300 °C, and then loaded into the growth chamber. In the growth chamber, each sample was heated to 615 °C for 2 min (the surface oxides desorbed at 580 °C) and then lowered to the initial growth temperature of 600 °C.

The growth rate for all layers was 1 μm/h. For samples grown with $As_2$ the group V to group III

beam equivalent pressure was 22. For samples grown with $As_4$ the group V to group III, beam equivalent pressures were 16. Initially, 0.75 $\mu$m of undoped GaAs was grown. Then the substrate temperature was lowered from an actual temperature of 600 °C to a thermal couple reading of 250 °C during the growth of the next 0.25 $\mu$m of GaAs. (At the actual temperature of 600 °C, the thermocouple reads in the neighborhood of 700 °C.) After reaching a thermocouple reading of 250 °C, 1 $\mu$m of undoped GaAs was grown. The substrate temperature was then ramped back to 600 °C during the growth of the next 500 Å of GaAs. After attaining the normal growth temperature of 600 °C, an additional 100 Å of undoped GaAs was grown. This was followed by an in-situ anneal in the $As_2$ or $As_4$ flux for 1 h at 600 °C. The substrate was rotated at 5 rpm during the growth of all layers and during the one hour 600 °C anneal.

The TEM examination of LTBLs grown with $As_2$ and $As_4$ was performed by using a JEM 2000 EX electron microscope. For the examination, [011] cross-sectional samples were prepared by the ion thinning technique. TEM images of both LTBLs have shown the existence of a large number of As precipitates, the appearance of which is similar to that observed in our earlier study [6]. Figs. 1a and 1b are bright field images taken from LTBLs grown with $As_2$ and $As_4$, respectively. The two images were taken under identical conditions; cross-sectional samples were tilted from the [011] axis by a few degrees to excite only one of the (111) type reflections. This condition gives rise to broad dark and bright bands of thickness contours in the images, which were used for the estimation of thicknesses of the observed areas. The small spacing of thickness contours in fig. 1b is caused by a large change of the thickness across the observed area of the sample. In the images, As precipitates appear with either dark or bright contrasts, depending on their locations with respect to those of the thickness contours. As seen in the two images, the sizes of the As precipitates are distinctly different between the two LTBLs; the average diameter of the precipitates in fig. 1a is 100 Å, while that in fg. 1b is 50 Å. Observations of other parts of the two LTBLs also showed this same

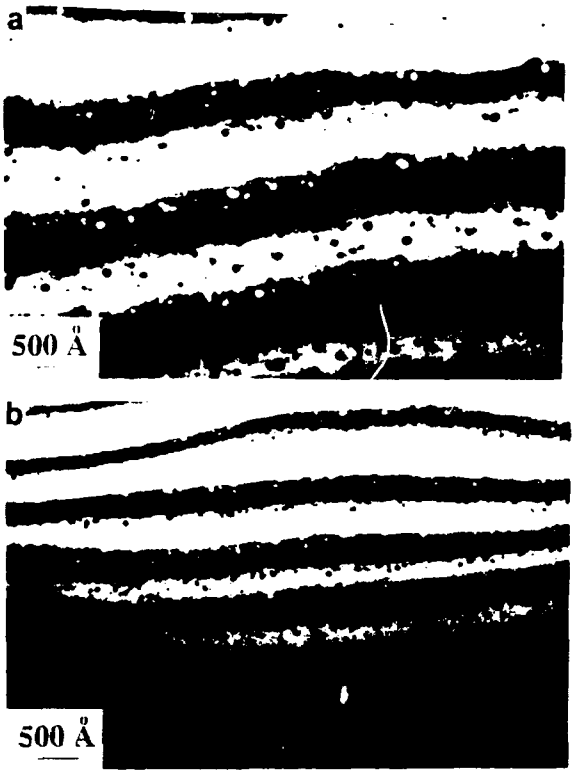


Fig. 1. Bright field images of cross-sectional samples of the LTBLs grown with (a) $As_2$ and (b) $As_4$.

difference in sizes of As precipitates. All observed precipitates in the LTBL grown with $As_4$ appear as nearly spherical particles. However the boundaries between the As precipitates and the GaAs for many of the large precipitates in the LTBL grown with $As_2$ exhibited flat sections, suggesting the formation of low energy boundaries along certain crystallographic planes. Fig. 2 is a high magnification bright field image showing such precipitates in the LTBL grown with $As_2$. In the image in fig. 2, many of the precipitates exhibit moire fringes.

Densities of the As precipitates were estimated from the bright field images. The thicknesses of the estimated areas were determined by using the extinction distance of 370 Å in GaAs for the (111) reflection of 200 kV electrons. Estimated densities are on the order of $10^{-1}$ cm$^{-3}$ for both LTBLs. No significant difference in the density of precipitates

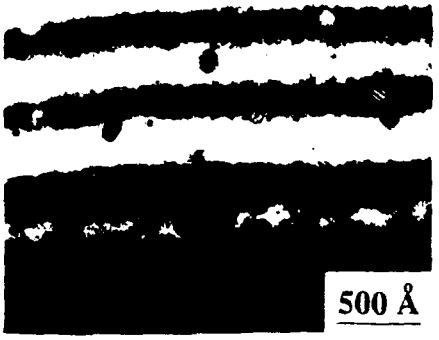


Fig. 2. High magnification bright field image of As precipitates in the LTBL grown with $As_2$.

was observed between the two samples, although the estimated density for the LTBL grown with $As_4$ appears to be slightly greater than that for the other LTBL. Since arsenic precipitates play a key role in the electrical properties of LTBLs [7], LTBLs grown with $As_2$ and $As_4$ should exhibit similar electrical characteristics due to the similar densities of arsenic precipitates. Recently, similar electrical properties for GaAs LTBLs grown using dimer and tetramer arsenic sources have been observed [10,11].

In comparing the two film growths used in this work, the film grown with $As_2$ had a slightly higher arrival rate of As atoms than the film grown with $A_4$, as determined from the measured beam equivalent pressures for $As_2$ and $As_4$, and taking into account the variation in sensitivity of an ion gauge due to the difference in number of electrons in the two molecules [12]. However, we find that the volume fraction of the elemental As phase in the LTBL grown with $As_2$, is significantly greater than that in the LTBL grown with $As_4$, indicating a higher incorporation efficiency of $As_2$, than that of $As_4$. The larger sizes but the similar density of As precipitates in the LTBL grown with $As_2$, compared to those in the LTBL grown with $As_4$, may be explained by assuming that the ev 'ution process of As precipitates in these two samples had already entered the coarsening stage due to the relatively long period of annealing; nearly all excess As was already incorporated in precipitates in these two LTBLs. This assumption may explain the high quality of the GaAs matrix in these LTBLs [8]. In order to confirm these explanations, however, one needs to carry out further systematic study on the precipitation process of As in LTBLs.

In summary, we report the growth of GaAs LTBLs by MBE using the dimer arsenic source $As_2$. We have observed the formation of arsenic precipitates in these LTBLs. TEM analysis of the LTBLs indicates an average As precipitate diameter of 100 Å and a density in the range of $10^{17}$ $cm^{-3}$ for the growth conditions used (beam equivalent pressure of $As_2$ to Ga of 22, a substrate temperature thermocouple reading of 250 °C, and followed by a one hour anneal at a temperature of 600 °C in the $As_2$ flux). We have also found that the incorporation of As in LTBLs is much more efficient when $As_2$ is used rather than $As_4$ during molecular beam epitaxy.

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# Substrate temperature dependence of arsenic precipitate formation in AlGaAs and GaAs

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GaAs epilayers which are grown by molecular-beam epitaxy under "normal" group III–V fluxes but at very low substrate temperatures contain as much as 1% excess arsenic. Upon annealing these epilayers at a temperature of 600 °C, the excess arsenic forms precipitates. We have undertaken a systematic study of the substrate growth temperature dependence of this incorporation of excess arsenic in both GaAs and $Al_{0.3}Ga_{0.7}As$ epilayers. The substrate growth temperature was varied in increments of 25 °C from 225 to 375 °C after every 0.25 $\mu$m of film growth for a GaAs and an $Al_{0.3}Ga_{0.7}As$ epilayer. Both epilayers were grown using a dimer arsenic source and a group V to total group III beam equivalent pressure ~20. After growth the films were annealed for 1 h in the $As_2$ flux at a temperature of 600 °C. Cross-sectional samples were than prepared by the ion thinning technique and examined by transmission electron microscopy (TEM). Both epilayers contained arsenic precipitates; this is the first observation of arsenic precipitates in an $Al_{0.3}Ga_{0.7}As$ epilayer. The density of the arsenic precipitates in the two epilayers had a strong dependence on substrate growth temperature. Details of the film growth and of the TEM observations are reported.

## I. INTRODUCTION

GaAs epilayers grown by molecular-beam epitaxy (MBE) at low substrate temperatures (200–300 °C) have attracted much attention since Smith *et al.*[1] used such low temperature buffer layers (LTBLs) to virtually eliminate sidegating in GaAs metal–semiconductor field effect transistors (MESFETs). Remarkably, epilayers grown at normal substrate temperatures (600 °C) on top of these LTBLs exhibit normal film characteristics. In fact we have observed a mobility of $2\times10^6$ cm$^2$/V s at a temperature of 4.2 K for a modulation-doped two-dimensional electron gas which was grown on top of a GaAs LTBL.[2] LTBLs are rapidly finding additional device applications. Yin *et al.*[3] have utilized a LTBL on top of a MESFET structure to obtain a substantial improvement in the gate-to-drain breakdown voltage. LTBLs have also been shown to be fast photoconductors and have been utilized as the photoconducting material in several fast pulse generation systems.[4–6]

Kaminska *et al.*[7,8] have observed that LTBLs contain as much as 1%–1.5% excess arsenic and that the as-grown LTBL has a 0.1% increase in lattice parameters due to this excess arsenic. However upon annealing the LTBL at 600 °C, which occurs if one grows an epilayer at normal substrate temperatures on top of the LTBL, the lattice constant decreases to that characteristic of GaAs.[7,8] This relaxation of the the lattice constant occurs due to the excess arsenic precipitating from the LTBL during the anneal.[9–11] We have previously reported details of transmission electron microscopy (TEM) studies of LTBLs grown at a substrate temperature of 250 °C using both the tetramer arsenic source $As_4$ and the dimer arsenic source $As_2$.[12,13] (Note Puechner *et al.*[14] have observed comparable electronic properties for GaAs LTBLs grown using dimer and tetramer arsenic sources.) The density we observed for the arsenic precipitates was on the order of $10^{17}$ cm$^{-3}$ with an average diameter in the range of 30–100 Å, indicating most of the excess arsenic precipitates out of the LTBL. Therefore the arsenic precipitates must play a dominant role in the properties of annealed LTBLs,[15] and it is very important to understand the parameters which control the precipitate formation. Besides GaAs LTBLs, researchers are investigating the growth of other III–V materials at low substrate temperatures.[16,17] In this paper we investigate the substrate growth temperature dependence of the incorporation of excess arsenic in GaAs and in $Al_{0.3}Ga_{0.7}As$.

## II. FILM GROWTH

The films used in this study were grown in a Varian GEN II MBE system on 2 in. diam undoped GaAs substrates. The substrates were degreased, etched for 1 min in a 60 °C solution of 5:1:1 $H_2SO_4$:$H_2O_2$:$H_2O$ and placed in nonindium mounts. The substrates were then loaded on a trolley and placed in the entry chamber of the MBE system where they were outgassed for 2 h at 200 °C before being introduced into the buffer chamber of the MBE system. Liquid nitrogen was circulated through the radial vane and cryoshrouds of the growth chamber starting 2 h before film growth. The substrates were outgassed at 350 °C for 1 h on a heater station in the buffer chamber immediately before being loaded into the growth chamber.

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Two films were grown for this work, one containing a low temperature (LT) GaAs epilayer and the other a LT $Al_{0.3}Ga_{0.7}As$ epilayer. The arsenic source used was the dimer $As_2$ which has been reported to be a more efficient source for arsenic incorporation in a LTBL than the tetramer source $As_4$.[13] Two Ga effusion furnaces were used so that the $Al_{0.3}Ga_{0.7}As$ epilayer was grown at the same rate as the GaAs epilayer accomplished by closing the shutter to one of the Ga effusion furnaces while opening the shutter to the Al effusion furnace; the growth rates were 1 $\mu$m/h. The beam equivalent pressures (bep) of the arsenic to the total group III flux was 23 for the growth which contained the LT GaAs epilayer and 21 for the growth which contained the LT $Al_{0.3}Ga_{0.7}As$ epilayer; the beps were measured with an ion gauge placed in the substrate growth position. The substrate was rotated at 5 rpm during the film growth and the subsequent anneal in the $As_2$ flux.

Initially 0.75 $\mu$m of undoped GaAs was grown at a substrate temperature of 600 °C. While still growing GaAs, the substrate temperature was reduced to 225 °C for the film which would contain the LT GaAs epilayer and to 250 °C for the film which would contain the LT $Al_{0.3}Ga_{0.7}As$ epilayer. This GaAs temperature transition region was 0.25 $\mu$m thick. In the case of the LT GaAs epilayer the procedure was to then grow 0.25 $\mu$m of GaAs at a substrate temperature of 225 °C, raise the substrate temperature to 250 °C and grow an additional 0.25 $\mu$m of material. This procedure was continued, incrementing the substrate temperature by 25 °C and growing 0.25 $\mu$m of material, up to a substrate temperature of 375 °C. After growing the 0.25 $\mu$m of material at 375 °C, the substrate temperature was ramped to 600 °C during the growth of the next 500 Å of GaAs, an additional 200 Å of GaAs was grown, and the Ga effusion furnace shutters were closed to end the growth. The sample was then maintained at a substrate temperature of 600 °C for 1 h under the $As_2$ flux.

In the case of the film which contained the LT $Al_{0.3}Ga_{0.7}As$ epilayer, after growing the 0.25 $\mu$m GaAs temperature transition region the shutter to one of the Ga effusion furnaces was closed and the shutter to the Al effusion furnace was opened. A similar procedure was then followed for the LT $Al_{0.3}Ga_{0.7}As$ epilayer as described above for the LT GaAs epilayer. After each increment of 25 °C in substrate temperature 0.25 $\mu$m of $Al_{0.3}Ga_{0.7}As$ was grown up to a substrate temperature of 375 °C. After growth of the 0.25 $\mu$m of $Al_{0.3}Ga_{0.7}As$ at a substrate temperature of 375 °C, the aluminum shutter was closed and the shutter reopened to the second Ga effusion furnace. The temperature was ramped to 600 °C during the growth of the next 500 Å of GaAs, an additional 200 Å of GaAs was grown, and the growth was then terminated by closing the shutters to the Ga effusion furnaces. The $Al_{0.3}Ga_{0.7}As$ epilayer was then annealed for 1 h at 600 °C in the $As_2$ flux.

## III. RESULTS

Both the LT GaAs and the LT $Al_{0.3}Ga_{0.7}As$ epilayers were examined by cross-sectional transmission electron microscopy (XTEM). For the examination, (011) cross-sectional samples were prepared by Ar ion thinning at low temperatures and observed by using a JEM 2000EX transmission electron microscope. Arsenic precipitates were observed in the TEM images of both the LT GaAs and the LT $Al_{0.3}Ga_{0.7}As$ epilayers. Figure 1 is a bright field image of the LT GaAs including areas of all substrate growth temperatures from 225 to 375 °C. The arsenic precipitates appear as tiny dark spots in this bright field image. As seen in this image, the density of the arsenic precipitates rapidly decreases with the increase in the substrate growth temperature.

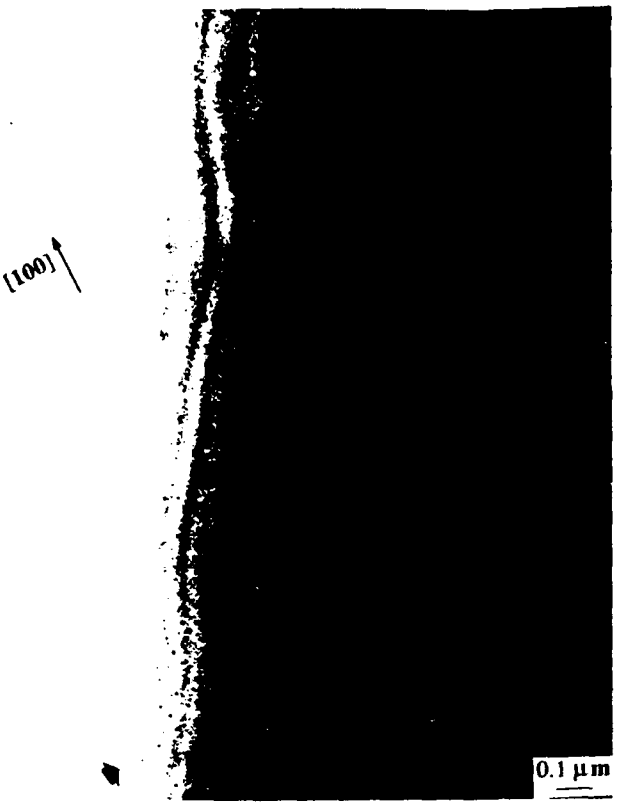


FIG. 1. Bright field image of the LT GaAs epilayer. The temperature transition region is indicated by an arrow.

Shown in Fig. 2 is a dark field image of the LT


FIG. 2. Dark field image of the LT $Al_{0.3}Ga_{0.7}As$ epilayer. The boundary between the LT $Al_{0.3}Ga_{0.7}As$ layer and the temperature transition region of the GaAs buffer is indicated by an arrow. The upper side of the image is the LT $Al_{0.3}Ga_{0.7}As$ layer.


FIG. 3. Weak beam dark field image of the LT GaAs layer grown at a substrate temperature of 250 °C.

$Al_{0.3}Ga_{0.7}As$ which was taken by using a 111 reflection of the $Al_{0.3}Ga_{0.7}As$. The area shown in Fig. 2 includes the temperature transition region of the GaAs buffer and the $Al_{0.3}Ga_{0.7}As$ layer grown at 250 °C. The TEM images as well as the diffraction spots of the arsenic precipitates in the LT $Al_{0.3}Ga_{0.7}As$ epilayer are identical to those in the LT GaAs epilayer.[12] Weak diffraction spots resulting from precipitates appear near 111 diffraction spots of the $Al_{0.3}Ga_{0.7}As$ crystal, similar to those observed in diffraction patterns of the LT GaAs layer. These weak spots were identified as 102 spots of elemental arsenic having a hexagonal structure. The change in the density and sizes of the arsenic precipitates with substrate growth temperature also appear to be similar between the two LT epilayers. One interesting observation was made regarding the distribution of arsenic precipitates in the LT $Al_{0.3}Ga_{0.7}As$. A significant change in density of arsenic precipitates was found at the boundary between the LT $Al_{0.3}Ga_{0.7}As$ and the temperature transition region of the GaAs buffer layer despite nearly equal growth temperatures on both sides of the boundary. As seen in Fig. 2, the density of arsenic precipitates is much higher on the GaAs side of the boundary than on the $Al_{0.3}Ga_{0.7}As$ side where a narrow precipitate-free band exists along the boundary. This observation suggests that excess arsenic atoms may have migrated from the LT $Al_{0.3}Ga_{0.7}As$ layer to the GaAs buffer during the anneal or during the growth of the epilayer.

Quantitative analyses of sizes and densities of arsenic precipitates in the LT GaAs epilayer were carried out by using weak beam dark field images. Figure 3 is an example of the weak beam dark field images used for the analysis, which includes a layer grown at 250 °C. For each growth temperature, sizes and the number of arsenic precipitates in a rectangular area with edge lengths of $0.12 \times 0.16\ \mu m$ were measured using an EYECOM image analyzer. The average thicknesses of the measured areas for all growth temperatures were kept constant by placing the rectangular area on the same thickness contours of the weak beam dark field images. Only arsenic precipitates which exhibit distinct bright contrast or clear moire fringes in the images were included in the measurements. Table I lists the results of two independent sets of measurements from one thin area of the sample. The two sets of measurements were made by using two different reflections, 111 and $1\,\overline{1}\,1$, for weak beam dark field imaging. A volume for each precipitate was estimated by assuming a spherical shape. Volume fractions as well as densities of arsenic precipitates which are listed in Table I are relative values for different growth temperatures because of the inclusion of only a portion of the arsenic precipitates in the measurement. Figure 4 is a representation of the resulting size distribution of the arsenic precipitates. As seen in Fig. 4, the distribution has one well-defined maximum with relatively narrow spreading towards both sides. For each temperature, the diameter corresponding to the distribution maximum was found to be nearly equal to the average value of the diameters. Results of two sets of measurements show that the density of arsenic precipitates and their volume fraction rapidly decrease with the increase in substrate growth temperature. The average diameter, on the other hand, re-

TABLE I. Two independent measurements of arsenic precipitate density and average diameter as a function of substrate growth temperature, and the corresponding volume fraction of arsenic in precipitates. The densities and hence the volume fractions are relative values because only a portion of the arsenic precipitates were included in the measurements.

| | Measurement set No. 1 | | | Measurement set No. 2 | | |
|---|---|---|---|---|---|---|
| Temperature (°C) | Density ($\times 10^{16}$ cm$^{-3}$) | Diameter (Å) | Volume fraction ($\times 10^{-3}$) | Density ($\times 10^{16}$ cm$^{-3}$) | Diameter (Å) | Volume fraction ($\times 10^{-3}$) |
| 225 | 4.3 | 74 | 3.410 | 3.1 | 70 | 2.03 |
| 250 | 3.9 | 55 | 0.951 | 2.8 | 52 | 0.676 |
| 275 | 1.7 | 61 | 0.635 | 1.3 | 62 | 0.667 |
| 300 | 0.78 | 76 | 0.556 | 0.78 | 51 | 0.212 |
| 325 | 0.52 | 46 | 0.077 | 0.39 | 45 | 0.051 |
| 350 | 0.39 | 29 | 0.016 | ... | ... | ... |


FIG. 3. Weak beam dark field image of the LT GaAs layer grown at a substrate temperature of 250 °C.

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| | Measurement set No. 1 | | | Measurement set No. 2 | | |
|---|---|---|---|---|---|---|
| Temperature (°C) | Density ($\times 10^{16}$ cm$^{-3}$) | Diameter (Å) | Volume fraction ($\times 10^{-4}$) | Density ($\times 10^{16}$ cm$^{-3}$) | Diameter (Å) | Volume fraction ($\times 10^{-4}$) |
| 225 | 4.3 | 74 | 3.410 | 3.1 | 70 | 2.03 |
| 250 | 3.9 | 55 | 0.951 | 2.8 | 52 | 0.676 |
| 275 | 1.7 | 61 | 0.635 | 1.3 | 62 | 0.667 |
| 300 | 0.78 | 76 | 0.556 | 0.78 | 51 | 0.212 |
| 325 | 0.52 | 46 | 0.077 | 0.39 | 45 | 0.051 |
| 350 | 0.39 | 29 | 0.016 | ... | ... | ... |

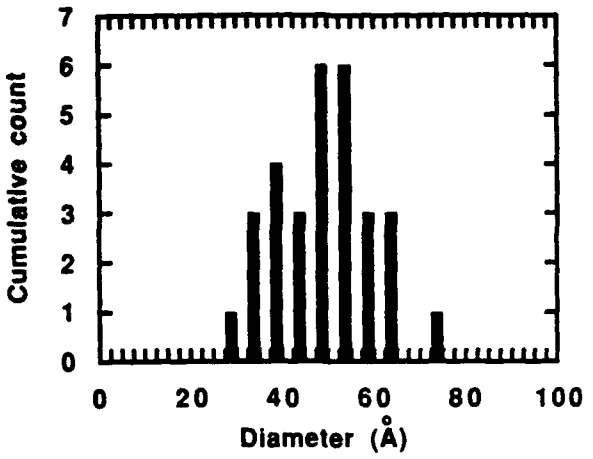


FIG. 4. Size distribution of arsenic precipitates in the GaAs layer grown at a substrate temperature of 250 °C.

mains at roughly the same value except for the two highest growth temperatures. Further studies on the precipitation process of excess arsenic during the annealing are required to understand the dependencies of the precipitate diameter and density on the growth temperature.

Plotted in Fig. 5 is the natural logarithm of the volume fractions of arsenic precipitates versus the inverse value of the substrate growth temperature. The plot is linear resembling an Arrhenius-type relationship, as indicated by the straight line in the figure. The slope of the straight line corresponds to an energy of 0.87 eV. Similar results were obtained from both sets of measurements. Note that the volume fraction of arsenic precipitates in an annealed LT GaAs epilayer approximately corresponds to a degree of nonstoichiometry of an as-grown LT GaAs epilayer, i.e., a concentration of excess arsenic atoms. It is interesting to point out that the temperature dependence of nonstoichiometry in an equilibrium system normally obeys an Arrhenius-type relationship but is opposite to that observed in the present study; the

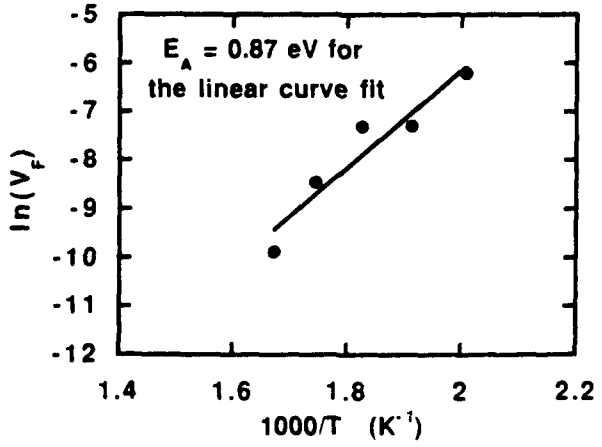


FIG. 5. Plot of the natural logarithm of the volume fraction of arsenic precipitates vs inverse substrate growth temperatures.

degree of nonstoichiometry increases with the temperature in an equilibrium system. One possible explanation for the present observation is as follows. The adsorption of excess arsenic occurs first at a growing surface of a GaAs epilayer for all substrate growth temperatures and is followed by thermally activated recovery processes towards a stoichiometric surface. A degree of nonstoichiometry of an as-grown layer and, hence, a volume fraction of arsenic precipitates in an annealed layer are determined by these recovery processes. One such process could be re-evaporation of excess arsenic atoms from the growing surface. Under the MBE conditions used in this work, including those of the LTBLs, evaporation of As atoms from a GaAs crystal is known to be negligible. In the present case, however, excess As atoms have to occupy high energy sites such as antisites and hence, are likely to evaporate more easily even at low temperatures. The fact that the "activation energy" estimated from Fig. 5 is comparable to the nearest-neighbor anion–cation bond energy of GaAs[18] and considerably lower than experimental values ( ~4.6 eV) of the activation energy for re-evaporation of GaAs[19,20] supports the aforementioned explanation. The present results, therefore, suggest that valuable insights of surface atomic processes of the MBE of GaAs can be obtained from a study of arsenic precipitates in LT GaAs layers. A further detailed study on the temperature dependence of the volume fraction of As precipitates is underway to clarify underlying atomic processes and will be reported in a separate paper.

## IV. SUMMARY

In summary, we have investigated the substrate growth temperature dependence of the incorporation of excess arsenic in both GaAs and $Al_{0.3}Ga_{0.7}As$ epilayers grown by MBE. By annealing the films after growth at 600 °C for 1 h, the excess arsenic precipitates and can then be observed with TEM. Arsenic precipitates were observed in both the LT GaAs and the LT $Al_{0.3}Ga_{0.7}As$ epilayers. This is the first reported observation of arsenic precipitates in $Al_{0.3}Ga_{0.7}As$ epilayers. The density of the arsenic precipitates was found to decrease with increase in substrate growth temperature. The average diameter, on the other hand, remains at roughly the same value over the substrate growth temperature range of 225–325 °C and then begins to decrease for higher growth temperatures. TEM studies of arsenic precipitates in annealed LTBLs may prove to be a valuable tool for studying surface atomic processes of the MBE of GaAs.

## ACKNOWLEDGMENTS

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# Two-wave mixing in photorefractive AlGaAs/GaAs quantum wells

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We have observed two-wave mixing in semi-insulating AlGaAs/GaAs multiple quantum well structures at wavelengths near the exciton absorption. The photorefractive index changes are caused by the Franz–Keldysh effect on quantum-confined excitons. Photorefractive gains larger than 200 $cm^{-1}$ are obtained for the first time at wavelengths near 836 nm using stationary fringes and dc applied fields up to 5 kV/cm. The direction of energy transfer between the two beams is determined by the direction of applied electric field.

The photorefractive effect in a variety of materials has been studied extensively.[1] Semiconductors have gained increased interest because of their faster response rate over ferroelectrics and because of their infrared sensitivity. However, the gain coefficient of two-beam coupling obtained in bulk semiconductors, relying on the linear electro-optic effect, is small. Quadratic electro-optic effects can be large for strong fields. Recently, two-beam coupling has been performed relying on the combination of linear electro-optic and quadratic Franz–Keldysh effects. A gain of 19 $cm^{-1}$ was obtained[2] in bulk InP:Fe, using band-edge resonance and temperature stabilization. The Franz–Keldysh effect at room temperature is especially strong for quantum-confined excitons,[3] which can be several orders of magnitude larger than the linear electro-optic effect for large fields.[4] The advantage of this large electro-optic effect in semi-insulating multiple quantum wells (SIMQWs) has been demonstrated in four-wave mixing measurements.[4] Here we show that it is possible to generate a large energy transfer with two-wave mixing in a SIMQW, without using moving fringes[5–7] or ac fields.[8]

The samples used in the experiment were grown by molecular beam epitaxy (MBE) on a GaAs substrate. The multiple quantum well structure (MQW) is sandwiched between a cap of AlGaAs and an AlGaAs stop-etch layer, which are transparent at the wavelengths near the of quantum-confined exciton absorption. The MQW consists of 60 periods of alternating GaAs wells (75 Å thick) and $Al_{0.3}Ga_{0.7}As$ barriers (100 Å thick). The samples were proton implanted using 160 keV protons at a dose of $10^{12}/cm^2$ from the AlGaAs cap side. The implanted side of the samples were epoxied to a glass slide and the GaAs substrate was removed with a selective etch. The samples were proton implanted again with the same dose and implant energy from the etched side so that the entire sample became semi-insulating. Two gold strips were evaporated on the stop-etch layer with a separation of 1 mm. A field parallel to the MQW is generated when a voltage is applied across the two electrodes, and the exciton absorption is altered by the Franz–Keldysh effect. The quantum-confined stark effect is not present in this geometry.

In our two-beam coupling measurement, the SIMQW is illuminated symmetrically with respect to the normal vector of the quantum well (QW) plane by two coherent laser beams. Each beam is *s*-polarized perpendicular to the plane of incidence and parallel to the QW layers. The fringe spacing of the interference pattern is $\Lambda = \lambda/2 \sin\theta$, where $\lambda$ is the laser wavelength in air, $2\theta$ is the intersection angle between two laser beams, and the fringe spatial frequency is $K = 2\pi/\Lambda$. The total electric field inside the sample parallel to the MQW is $E = \mathrm{Re}[E_0 + E_{sc} \times \exp(iKx + \phi)]$, where $E_{sc}$ is a space-charge field generated from the interference pattern of two laser beams, $E_0$ is the external dc applied field, and $\phi$ is the shift of the electric field relative to the interference fringes. The space-charge field $E_{sc}$ is nonzero only when both beams are present. A dielectric index grating is generated by the space-charge field through the Franz–Keldysh effect. In the Franz–Keldysh geometry, the linewidth of the exciton absorption is broadened by the field-ionization process. This effect does not depend on the sign of the electric field, only on its magnitude. To lowest order, the electroabsorption is therefore quadratic in electric field strength. In a quadratic electro-optic effect, the absorption and index changes $\Delta\alpha$ and $\Delta n$ are given by

$$\Delta\alpha = -(2\pi/\lambda) n^3 s_2 E^2, \qquad \Delta n = -\tfrac{1}{2} n^3 s_1 E^2, \tag{1}$$

where $s_1$ and $s_2$ are quadratic electro-optic coefficients, and where the square of the field is given by

$$E^2 = (E_0^2 + 0.5E_{sc}^2) + 0.5E_{sc}^2 \cos(2Kx + 2\phi) - 2E_0 E_{sc} \cos(Kx + \phi). \tag{2}$$

In the first term of Eq. (2), the screening field results in an average electroabsorption, which we describe below. The second term in Eq. (2) results in diffraction signals from a grating with twice the spatial frequency of the interference fringes, which will be described in a separate paper. The third term represents the field grating that allows two-beam coupling.

In the thin grating limit, the beam coupling is given by

$$I_1^+ = \left[ I_1(1 - \bar{\alpha}_E L) + \sqrt{I_1 I_2}\left( + \frac{\Delta\alpha L \cos\phi}{2\cos\theta'} + \frac{2\pi\Delta n L \sin\phi}{\lambda \cos\theta'} \right) \right], \tag{3}$$

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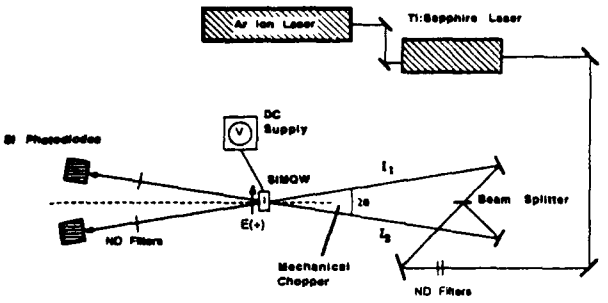


FIG. 1. Schematic of the two-wave mixing experiment. The beam coupling direction is defined by the direction of the applied electric field.

$$I_2^+ = \left[ I_2(1-\bar{\alpha}_E L) + \sqrt{I_1 I_2}\left( + \frac{\Delta\alpha L \cos\phi}{2\cos\theta'} - \frac{2\pi\Delta n L \sin\phi}{\lambda\cos\theta'} \right) \right], \tag{4}$$

where $I_1^+$ and $I_2^+$ are the transmission intensities of the two beams when both are present, and $I_1$ and $I_2$ are the transmission intensities of the two beams in the absence of the other beam. The thickness of the sample is $L$, and $\theta'$ is the internal angle. The phase shift of $E_{sc}$ with respect to the interference pattern is given by $\phi$. Note that the terms involving electroabsorption are symmetric for beams 1 and 2, while the terms involving the electrorefraction are asymmetric. The interaction between the two laser beams results in three terms: one term describing the average electroabsorption change, another describing the electroabsorption grating, and the third term describing an energy exchange due to the refractive index grating. The average electroabsorption change because of $E_{sc}$ is denoted by $\bar{\alpha}_E$, which arises because of the "corrugation" of the index due to the $E_{sc}$ portion in the first term in Eq. (2) when both beams are present. The average electroabsorption $\bar{\alpha}_E$ is zero for the linear electro-optic effect.

The geometry of our experiment is shown in Fig. 1. The measurements are performed by monitoring the intensity modulation of one transmitted beam as the other beam is mechanically chopped at a frequency of 290 Hz. A dc electric field of 5 kV/cm is applied, with the positive direction indicated in Fig. 1. The intersection angle between the laser beams is $2\theta = 10.4°$, giving a fringe spacing of 4.6 $\mu$m for a wavelength of 840 nm. The infrared light source is a Spectra-Physics Ti:sapphire laser which is tunable across the exciton absorption between 800 nm and 850 nm.

To study the energy transfer and electroabsorption properties of beam coupling, the mixing signals of both beams were measured. The intensities of both incident beams were approximately equal (0.1 W/cm$^2$). When the direction of applied field is reversed, the phase shift $\phi$ changes sign in Eqs. (3) and (4), in contrast to the linear electro-optic photorefractive effect.[1] The net energy transfer is obtained by reversing the direction of the applied electric field, and detecting the change in the modulation of the signal. The energy transfer for the quadratic Franz–Keldysh effect in thin gratings is given by

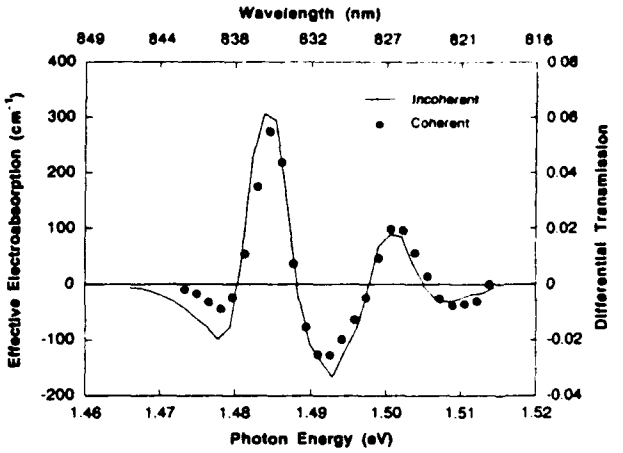


FIG. 2. The coherent effective electroabsorption coefficient $\Delta\alpha_{eff}$ of the two-wave mixing experiment for a dc field of $E = 5$ kV/cm, compared with the incoherent differential transmission data for an ac applied field of 0–5 kV/cm.

$$\gamma = \frac{1}{2}\frac{I_1^+(E) - I_1^+(-E)}{I_1} = \left(\frac{I_2}{I_1}\right)^{1/2}\frac{2\pi\Delta n L \sin\phi}{\lambda\cos\theta'}. \tag{5}$$

Assuming $E_{sc}$ is proportional to the modulation index $m$ of light intensity (as it is for bulk materials), then $\Delta n$ is proportional to $m$ because the third term in Eq. (2) is a linear function of $E_{sc}$. The above equation can therefore be expressed as

$$\gamma = (\beta/1+\beta)\Gamma L, \tag{6}$$

where

$$\Gamma = \frac{4\pi\Delta n_m \sin\phi}{\lambda\cos\theta'}, \tag{7}$$

$\Delta n_m$ is the maximum amplitude of the refractive index grating, and $\beta = I_2/I_1$ is the beam intensity ratio. It is convenient to define an effective electroabsorption coefficient $\Delta\alpha_{eff}$, which combines all the electroabsorption terms in Eqs. (3) and (4), which are measured experimentally as the symmetric part of the modulated signal. The effective electroabsorption is defined by

$$\frac{1}{2}\frac{I_1^+(E) + I_1^+(-E)}{I_1} = 1 - \Delta\alpha_{eff}\frac{L}{\cos\theta'}. \tag{8}$$

The effective electroabsorption coefficient $\Delta\alpha_{eff}$ caused by the mixing is plotted in Fig. 2, compared with the incoherent differential transmission measured with a single beam for an external 0–5 kV/cm ac field. Notice that the differential transmission and the effective electroabsorption have the same sign, which may appear counterintuitive. This is because the second term in Eqs. (3) and (4), which represents diffraction by the absorption grating, wins out over the increase in absorption from the average electroabsorption $\bar{\alpha}_E$. Therefore, there is a net decrease in the overall absorption because of the coherent interference between the two beams.

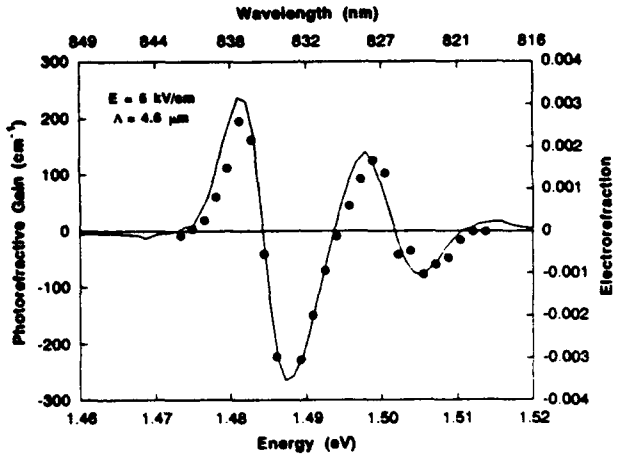


FIG. 3. Two-wave mixing photorefractive gain (data), and refractive index modulation (solid line) as a function of photon energy. The refractive index modulation is obtained from the Kramers–Kronig transformation of the incoherent differential transmission data from Fig. 2. The relative signs in the figure are set by the electric field direction in Fig. 1.

The gain $\Gamma$ is shown in Fig. 3, compared with the electrorefraction data derived from the Kramers–Kronig analysis of the incoherent differential transmission data in Fig. 2. The result is in good agreement with the prediction in Eqs. (3) and (4), giving unambiguous evidence for photorefractive gratings in this coupling process. For the applied field of 5 kV/cm in the sample of Fig. 3, gains larger than 200 $cm^{-1}$ were observed. Gains as large as 400 $cm^{-1}$ have been observed in other samples under similar conditions. No gain is observed when the writing beams are cross polarized with respect to each other. The gain obtained corresponds to a refractive index modulation of $\Delta n = \lambda \cos\theta' \Gamma/(2\pi \sin\phi)$. Assuming this refraction index modulation is the same as the $\Delta n$ in Fig. 3, we find a phase shift of $\phi = +30°$. It is worth mentioning that the maximum gain obtained in our measurement is more than ten times larger than the previous maximum gain obtained in a semiconductor.[2]

In bulk photorefractive materials, in order to have a significant phase shift, the applied field should be either much smaller than the diffusion field $E_d$, or comparable with the maximum internal field modulation, which is limited by the space-charge density $N_t$ and the defect occupancy $f$ in the expression $E_{max} = ef(1-f)N_t/(K\epsilon\epsilon_0)$. When a single photocarrier dominates, the phase shift is given by[9] $\phi = \tan^{-1}(E/E_{max})$, for an applied field $E$. If the phase shift of the grating is generated by space-charge limitation, an estimate of $N_t$ can be made from the above formula, which yields $N_t = 10^{15}/cm^3$ for the defect occupancy. However, such a small $N_t$ is far below the expected defect density according to Eq. (A1) in Ref 10. Each proton is expected to generate 40 displaced atoms, which yields $N_t = 10^{17}/cm^3$. Because of this discrepancy, we cannot rule out other mechanisms for the phase shift that may be related to the multilayer structure. More work is necessary to resolve the origin of the phase shift.

In conclusion, we have performed two-beam coupling experiments for semi-insulating multiple quantum well structures. The strong quadratic electroabsorption and associated electrorefraction generates strong coupling of two coherent beams. A significant net energy transfer is observed caused by a shifted grating. More work on the photorefractive transport in MQW is needed in order to clarify the origin of the phase shift of the grating.

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# 1.3-$\mu$m P-i-N Photodetector Using GaAs with As Precipitates (GaAs:As)

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***Abstract*—We report the successful fabrication of the first GaAs detector which operates in the 1.3- to 1.5-$\mu$m optical range. The detector is a P-i-N photodiode with an intrinsic layer composed of undoped GaAs which was grown at 225°C and subsequently annealed at 600°C. This growth process has been demonstrated to produce a high density of As precipitates in the low-temperature grown region, which we show here to exhibit absorption through internal photoemission. The internal Schottky barrier height of the As precipitates is found to be 0.7 eV, leading to reasonable room-temperature responsivity out to around 1.7 $\mu$m.**

## I. Introduction

MOST commercial optical receivers today are *hybrid* circuits of silicon-based electronics with Ge- or GaInAsP-based photonics, designed to detect the fiber-optic wavelengths of 1.3- and 1.5-$\mu$m light. A preferred configuration would involve *integrated* electronic and photonic devices fabricated from one material, or from lattice-matched heterostructures such as InP/InGaAsP and InP/InAlAsP. Progress in the commercial development of InP-based integrated receivers, however, has been slow. And while high-performance GaAs-based integrated electronic circuits and receivers can now be fabricated reliably, conventional GaAs detectors are not sensitive in the 1.3–1.5-$\mu$m range.

Recently, it was found that GaAs grown at 200–250°C yielded a substrate that virtually eliminates the effects of back- and sidegating in GaAs circuits [1]. Melloch *et al.* [2] found that such material, when subsequently annealed at 600°C, contains a high density of As precipitates and proposed that the electronic properties of the material were the result of internal Schottky barriers between the precipitates and the surrounding GaAs [3]. That model suggests the possibility of internal photoemission from precipitates, governed by the As/GaAs Schottky barrier. This paper is the first report of P-i-N photodetectors using GaAs with As precipitates (GaAs:As) which detect 1.3-$\mu$m light with reasonable efficiency at room temperature. Since high-performance GaAs electronic circuits are not only compatible with but benefit from GaAs:As, an all-GaAs 1.3-$\mu$m optical receiver chip should now be possible.

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## II. Photodetector Structure and Fabrication

A cross section of the epilayers used for this work is shown in Fig. 1. On an $n^+$ GaAs substrate, the $n^+$ side of the P-i-N diode is grown first (eliminating effects from the substrate/epi interface) at 600°C, followed by a 1-$\mu$m-thick undoped i-layer grown at 225°C, and a $p^+$ top-side contact grown at 600°C. No growth interruption was employed, resulting in "temperature-grade" regions on the substrate and surface sides of the i-layer of 0.25 and 0.05 $\mu$m, respectively. The structure sees a 600°C anneal during both the top contact (p-type) growth and an additional 60 min in the $As_2$ beam after growth has been completed. This process has been demonstrated to produce a high-quality GaAs matrix containing As precipitates of roughly 7 nm diameter with a density of $10^{17}/cm^3$ (GaAs:As), which has been used as the active photoconductive material in a complete terahertz-beam transceiver system [4]. It should be noted that this material is fundamentally different from that grown at 200°C or not completely annealed, which retains a high density of bulk defects in the GaAs [5].

For device fabrication, a 100-$\mu$m-diameter mesa was used to isolate device p-contacts and define the device active area. After refilling with evaporated $SiO_x$, Ti/Pt/Au ring contacts and pads were patterned for the front contact and a blanket Au/Ge/Ni layer deposited for back-side n-contact. With this geometry, illumination is provided from the top via the hole in the ring contact. Control samples were fabricated in an identical manner, except that the epilayers were grown at 600°C throughout so that the i-layer was free of As precipitates.

## III. Measured Device Performance

The room-temperature performance of these photodiodes in response to incident light with a wavelength of 1.3 $\mu$m was examined in some detail. $I/V$ characteristics of a typical 100-$\mu$m diode are shown in Fig. 2, with the lower curve giving data for the unilluminated (dark) case, and the upper for 1-mW incident illumination. The first point of interest in these data is that the diode does not turn on hard in the forward direction as a "normal" P-i-N diode would. This suggests that the As clusters in the GaAs:As are acting as strong current sinks. There is some asymmetry and increase current in the forward direction, but not enough to preclude

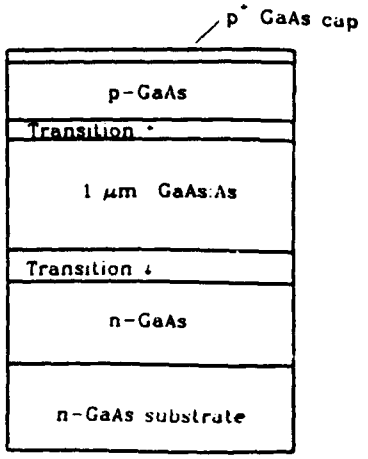


Fig. 1. Heterostructure cross section for the GaAs:As P-i-N photodiode. "Normal material" growth occurred at 600°C, and low-temperature growth at 250°C. Continuous growth produced the "temperature-grade" regions above and below the undoped low-temperature i-layer.

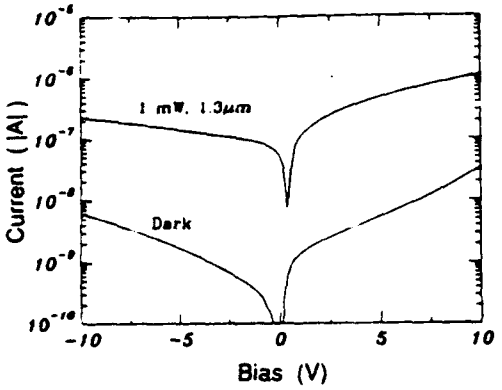


Fig. 2. Photocurrent versus bias in the dark (lower curve) and with 1 mW of 1.3-μm incident illumination (upper).

detector operation with a bias at either polarity. The second point of note is the low level of dark $I/V$ leakage current, roughly 5 nA at −10-V bias for 100-μm dots. This is 60 μA/cm$^2$, which, while 10 times greater than that exhibited by control devices, compares favorably with results from Si with $CoSi_2$ by Fathauer *et al.* [6], which suffered from leakage currents of 600 μA/cm$^2$ with a reverse bias of only 1 V and operated at 77 K. Even with a *forward* bias of 10 V, the GaAs:As photodiodes only yield 300-μA/cm$^2$ dark current.

The upper curve shows the $I/V$ response of these photodiodes when illuminated with 1 mW of 1.3-μm light. A slight positive threshold shift is observed, accompanied by a strong increase in current, producing 450 nA at −20-V bias. Control samples exhibited negligible change upon illumination with the 1.3-μm light, as expected. Through transmission experiments, we find that only 3–5% of the 1.3-μm radiation is absorbed or scattered in the 1-μm i-layer, and assuming 3% absorption and allowing for 33% reflectance, obtain an *internal* quantum efficiency of 2–2.5%. The forward-bias responsivity is even stronger, producing 1 μA at +10-V bias.

Clearly, a structure which only intercepts 3–5% of the incident light is not ideal. As an initial improvement, we

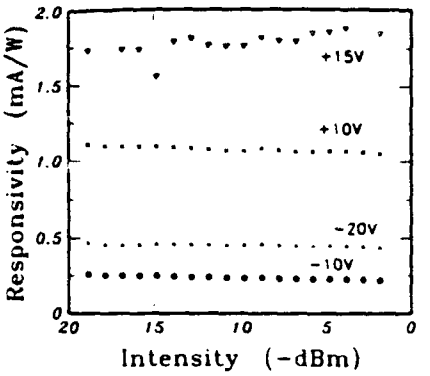


Fig. 3. Intensity dependence of GaAs:As photodiode responsivity at $V_b$ of −20, −10, +10, and +15 V.

have fabricated GaAs:As *laterally coupled* P-i-N photodiodes, where the incident light is channeled into the i-layer in-plane. The heterostructure for these devices included AlGaAs ($x = 0.3$) cladding layers above and below the active low-temperature grown i-layer for waveguiding. In spite of having no antireflection coating and only coupling roughly 25% of the light (estimated, from initial optics and geometric factors), we find a factor of 10 increase in the responsivity. The dark current for these "lateral photodiodes" is greater than that for the vertical structures, and is probably related to the inclusion of AlGaAs in the temperature-grade regions. And while the dark current scaled with device length, we find no change in responsivity for diode lengths greater than 50 μm. This is consistent with our independent observation of 3–5% loss through the 1-μm i-layer in the vertical devices.

Fig. 3 shows the intensity dependence of the responsivity to 1.3-μm illumination for various applied biases. As is shown, it is intensity *independent* for a 1-mW source attenuated from 0 to −20 dBm and applied biases from −20 to +15 V. This indicates that over this intensity range saturation effects due to precipitate charging are not a factor, and suggests that a two-photon absorption process is unlikely. Preliminary results from the wavelength dependence of the responsivity give an extrapolated barrier height for this internal emission of 0.7 eV, which is consistent with the barrier height of As to GaAs as observed in planar Schottky structures.

A final interesting observation regards the speed with which these photodiodes respond to modulation of 1.3-μm light. Using standard lock-in techniques, we find that under forward bias, the diode current response begins to fall off in the 50-kHz range. At this point, it is unclear whether the limit here is due to charging effects in the As clusters, or to recombination rate limitations. Details regarding emission and precipitate charging and neutralization further complicate the picture. In the reverse-bias direction though, the photoresponse is faster than our initial equipment limit of 2 GHz. Work in progress on metal–semiconductor–metal (MSM) detectors push this value to above 50–100 GHz and with no extended "tail" to the response using 0.7-ps excitation pulses [7]. This suggests that the recombination is similar to that observed for electron–hole pairs with above-bandgap illumi-

nation [4], where the photoresponse decay time was observed to be of the order of 2 ps.

## IV. Summary

In summary, we report on the first GaAs-based P-i-N photodiodes which operate in the 1.3-$\mu$m range. The devices exhibit low leakage currents at 295 K under both forward and reverse bias. Initial results from laterally coupled devices have produced a factor of 10 increase in responsivity over the top-illuminated device with further improvement expected through optimization. The photoresponse speed in these devices is in excess of our initial testing limit of 50–100 GHz.

## Acknowledgment

The authors would like to thank Dr. N. Braslau for assistance with initial characterization work.

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# Significant Long-Term Reduction in n-Channel MESFET Subthreshold Leakage Using Ammonium-Sulfide Surface Treated Gates

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*Abstract*—**Ammonium-sulfide ($(NH_4)_2S$) treated gates have been employed in the fabrication of GaAs MESFET's that exhibit a remarkable reduction in subthreshold leakage current. A greater than 100-fold reduction in drain current minimum is observed due to a decrease in Schottky gate leakage. The electrical characteristics have remained stable for over a year during undesiccated storage at room temperature, despite the absence of passivation layers.**

IN RECENT YEARS an increasing number of high-speed digital integrated circuits have been implemented in GaAs metal–semiconductor field-effect transistor (MESFET) technologies. Large-scale integration (LSI) has been achieved with acceptable production yields, and an increasing variety of GaAs chips is becoming available for incorporation in digital systems. A number of device-oriented issues currently being researched are crucial towards further improvements in the performance and capability of GaAs MESFET IC's. One such concern is the parasitic subtreshold leakage current of a MESFET, which can seriously affect circuit margins and performances [1]–[3]. This letter reports a simple technique that has been used to dramatically reduce subtreshold drain leakage in GaAs MESFET's.

The important drain and gate currents present in a GaAs FET biased in the subthreshold regime are depicted in Fig. 1. In most conventional-gate MESFET's, $I_{DS}$ and $I_{DG}$ are the dominant sources of drain subthreshold current [3]–[6]. $I_{DS}$ can be turned off exponentially by applying an increasingly negative gate voltage, so the drain current minimum of a long-channel MESFET is usually determined by reverse-biased Schottky gate diode conduction ($I_{DG}$ of Fig. 1) [3]–[6].

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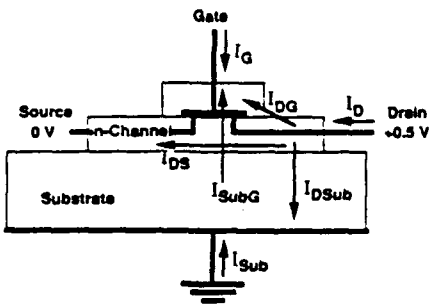


Fig. 1. Pictorial representation of drain and gate leakages present in an n-channel GaAs MESFET biased in the subthreshold regime ($V_G < V_T$). In most conventional-gate MESFET's, $I_{DS}$ and $I_{DG}$ are the dominant sources of subthreshold leakage. Since $I_{DS}$ can be turned off exponentially by applying an increasingly negative gate voltage, the drain current minimum of a long-channel MESFET is usually determined by reverse-biased Schottky gate diode conduction $I_{DG}$ [3]–[6].

The chief leakage mechanism in GaAs Schottky barriers is thermionic emission of carriers over the junction potential barrier [7], [8]. In Schottky diodes prepared using conventional fabrication techniques, the Fermi level at the GaAs surface is effectively pinned near midgap, and the Schottky barrier height is essentially independent of the metal–semiconductor work function [9], [10]. However, Waldrop observed an increase in Schottky barrier height for metals deposited on a GaAs surface which had prior exposure to elemental sulphur [11]. Recently, Carpenter *et al.* have shown that pretreating the GaAs surface with ammonium sulfide ($(NH_4)_2S$) before metal deposition can lead to a significant variation in Schottky barrier height with the metal deposited [12], [13], and this result was subsequently confirmed by Fan *et al.* [14]. The purpose of this work is to investigate the effect of $(NH_4)_2S$-treated gates on the subthreshold leakage of GaAs MESFET's fabricated using conventional LSI processing techniques.

The devices (Fig. 2) were fabricated in epilayers grown by molecular beam epitaxy on a (100) undoped GaAs substrate. The buried p-layer is completely depleted, but provides a potential barrier that minimizes substrate subthreshold conduction in short-channel devices [15]. Conventional lithography based on AZ 1350J-SF positive photoresist was used to pattern isolation mesas and ohmic contacts. Mesas were defined by a 2.5-min wet etch in 3 $H_3PO_4$:1 $H_2O_2$:50 $H_2O$

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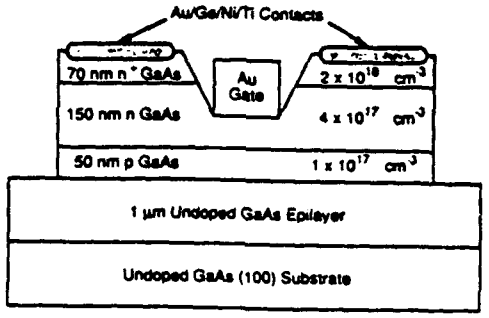


Fig. 2. Recess-etched epitaxial MESFET cross section.

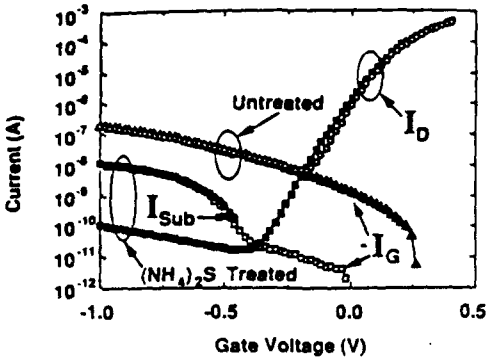


Fig. 3. $I_D$, $I_G$, and $I_{Sub}$ versus $V_G$ at room temperature for untreated and $(NH_4)_2S$-treated $10 \times 350$-$\mu m^2$ ring-gate n-channel MESFET's with $V_{DS} = 0.5$ V. The $I_{Sub}$ shown was measured on the $(NH_4)_2S$-treated device, and is similar to the untreated device substrate current. These data were measured one year after device fabrication, and showed no change from data taken within one week of device fabrication.

to remove approximately 2500 Å of material. Au/Ge/Ni/Ti layered ohmic source/drain contacts were then electron-beam evaporated onto the $n^+$ regions, patterned by lift-off, and furnace annealed at 350°C for 1 min in $N_2$ [16].

In the final masking step, the MESFET gate pattern was aligned, exposed, and developed. A recess etch self-aligned to the gate pattern was carried out for 160 s in 3 $H_3PO_4$:1 $H_2O_2$:100 $H_2O$; this left an estimated 80-nm-thick n-layer to serve as the MESFET channel. The wafer was then cleaved into two pieces, one of which was treated by soaking it in a saturated $(NH_4)_2S$ solution for 2 min [12], [13]. To preserve the gate pattern under exposure to the highly alkaline gate treatment solution, 4% PMMA was used as the resist for the final masking step. Following a deionized water rinse and $N_2$ blow dry, both pieces were placed into a vacuum system and Au gates were thermally evaporated with the wafers cooled to near 77 K by circulating $LN_2$ through the substrate holder [13]. To minimize defect-forming surface chemical reactions, the processing from the treatment to pump-down of the evaporation system was carried out without delay, and use of excited electron sources (e.g., electron beams and ionization gauges) was explicitly avoided. Fabrication was concluded by metal lift-off.

Fig. 3 compares the measured drain, gate, and substrate currents of typical $(NH_4)_2S$-treated and untreated $10 \times 350$-$\mu m^2$ ring-gate MESFET's as a function of gate voltage with $V_{DS} = 0.5$ V. The device characteristics have remained stable for over a year during undesiccated storage at room temperature, despite the absence of passivation layers. Although nonuniformities in the recess etch resulted in intra-wafer threshold variations, both treated and untreated devices exhibited similar ON characteristics with $V_{T0} = 0.1 \pm 0.2$ V. Below threshold, the drain current in both samples declines exponentially at 70 mV/decade until gate leakage becomes significant. The data presented in Fig. 3 clearly show more than a 100-fold reduction in the drain current minimum of the $(NH_4)_2S$-treated gate MESFET over its untreated counterpart. This decrease is directly attributable to the reduction in leakage current of the ammonium-sulfide-treated Schottky gates.

When a negative gate voltage is applied to turn off an n-channel GaAs FET, a punchthrough condition is created between the gate and the substrate, which can result in holes being injected from the substrate [3], [8]. This conduction ($I_{SubG}$ of Fig. 1), which is relatively unaffected by the metal–semiconductor barrier height, dominates the measured gate current $I_G$ for $V_G < -0.5$ V in the $(NH_4)_2S$-treated device (Fig. 3). The drain leakage current is expected to scale with shrinking gate size until mechanisms unrelated to channel–gate diode conduction become dominant. Drain-to-substrate leakage ($I_{DSub}$ in Fig. 1), which arises from the positive drain bias with respect to the substrate, can sometimes determine the measured drain current minimum even though highly insulating substrates are employed [3], [17]. The treatment is not expected to improve the subthreshold characteristics of very short-channel devices ($L_G \sim 0.1$ $\mu$m) where drain-to-source conduction through the substrate is totally dominant [19].

To summarize, we have used ammonium-sulfide-treated Au gates to reduce gate-diode-limited subthreshold conduction in GaAs MESFET's by over a factor of 100. The treated device characteristics have remained stable for over a year despite unpassivated exposure to room air. This technique shows promise for use with gate materials other than gold, provided deposition techniques and gate-to-semiconductor work-function differences are optimized. As no exotic *in-situ* processing is required, the technique appears suitable for use in large-scale integrated circuits.

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# Observation of above-barrier quasi-bound states in asymmetric single quantum wells by piezomodulated reflectivity

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The piezomodulated reflectivity spectrum of asymmetric GaAs/AlGaAs single quantum well heterostructures display interband excitonic transitions from bound and quasi-bound valence states to bound and quasi-bound states in the conduction band. The quasi-bound states with maximum occupancy in the well region in these compositionally asymmetric quantum wells participate "resonantly" in interband transitions. These spectra are compared with those from symmetric quantum wells with the same well width.

Semiconductor quantum well structures grown by molecular beam epitaxy (MBE) provide a unique opportunity to control their electronic and optical properties by adjusting layer thicknesses and material compositions. The quantum confinement of carriers is reflected in the enhanced band gaps of such structures; this has led to the practical implementation of band-gap engineering.[1] With this ability of implementing one-dimensional quantum mechanical effects in layered quantum well and superlattice heterostructures at hand, it is of interest to study the role played by unequal barrier heights in generating bound as well as quasi-bound states in single quantum wells. As is well known, symmetric quantum wells must have at least one bound state even for arbitrarily small barrier heights. However, single quantum wells with unequal barriers need not have any bound state under conditions derived in text books on quantum mechanics.[2] In this letter we report a direct observation of quasi-bound, resonant levels in compositionally asymmetric $Al_{x_1}Ga_{1-x_1}As/GaAs/Al_{x_3}Ga_{1-x_3}As$ single quantum wells using piezomodulated reflectivity. The asymmetric wells have different Al concentrations, $x_1$ and $x_3$, on either side of the GaAs layer (i.e., $x_2 = 0$) leading to different potential barrier heights $V_1$ and $V_3$ on either side. We have studied asymmetric wells of widths 100, 50, 33, and 20 Å, and compared them with their symmetric counterparts. The piezomodulation technique has recently been demonstrated to be a powerful and sensitive method for the observation of spectral features in GaAs/AlGaAs heterostructures. Interband excitonic transitions have been observed in the piezomodulated reflectivity of single, multiple, and parabolic quantum wells. These include transitions from spin-orbit split-off quantum confined levels in the valence band to those of the conduction band levels.[3,4]

The films used in this work were grown in a Varian GEN II MBE system on (100)-GaAs substrates. Initially, a 0.5 $\mu$m GaAs buffer layer was grown. This was followed by either a symmetrical or asymmetrical single quantum well. The symmetrical well had 400 Å $Al_{0.3}Ga_{0.7}As$ barrier layers. The asymmetrical single quantum wells had a 400 Å $Al_{0.3}Ga_{0.7}As$ upper barrier and a 400 Å $Al_{0.1}Ga_{0.9}As$ lower barrier. There were 30s growth interruptions upon completing the $Al_{0.3}Ga_{0.7}As$ barrier and the GaAs well to provide for smooth interfaces and a uniform thickness for the quantum well. The experimental procedure for piezomodulation reflectivity is described in Refs. 3 and 4.

We have calculated the quantum well energy levels for the various geometries in our experiment using an eight-band **k·p** model[5] within the framework of a double precision finite element procedure.[6] The input parameters in the **k·p** model for each layer are obtained from the standard compilation,[7] with interpolation for the energy gap for the AlGaAs layers as given by Bosio *et al.*[8] The wavefunctions belonging to the allowed continuum of states in asymmetric wells for $V_1 < E < V_3$ are taken to be of the form

$$\psi(z) = \begin{cases} e^{ik_1 z} + re^{-ik_1 z} & -\infty < z \leq 0 \\ 2Ae^{i\phi_1}\sin(k_2 z + \phi_2) & 0 \leq z \leq d \\ 2Be^{i\phi_1}e^{-\kappa_3(z-d)} & d \leq z < \infty \end{cases}, \qquad (1)$$

where $k_1$, $k_2$, and $\kappa_3$ are wavevectors of the carrier in the three regions defined by the potentials $V_1$ in the left barrier, $V_2 = 0$ in the well, and $V_3 (> V_1)$ in the right barrier. Also, $\phi_1$ and $\phi_2$ are phase angles defined for convenience in implementing the boundary conditions at the interfaces and $r$ is the complex reflection amplitude of the carrier wavefunction in the left region. The reflected intensity $|r|^2$ is not a useful parameter since $|r(E)|^2 = 1$ for all energies such that $V_1 < E < V_3$. With a slight refinement of Messiah,[2] we define $\Omega$ as the occupancy of the carrier in the well region:

$$\Omega(E) = \int_0^d |\psi(z)|^2 dz$$

$$= |A|^2\left[2d - \frac{1}{k_2}\{\sin(2\alpha) - \sin(2\phi_2)\}\right], \qquad (2)$$

where $\alpha = k_2 d + \phi_2$ and in the one-band approximation the coefficient $|A|^2$ is given by

$$|A|^2 = 1/[1 + \{(k_2 m_1^*/k_1 m_2^*)^2 - 1\}\cos^2\phi_2]. \qquad (3)$$

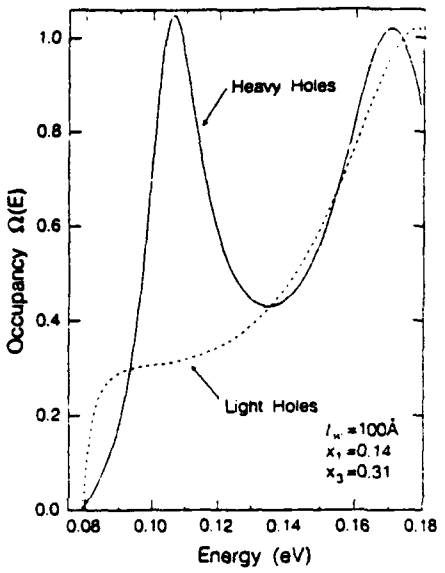


FIG. 1. A plot of occupancy in the well $\Omega(E)$, defined in Eq. (2), as a function of energy, $E$, for heavy holes (solid line) and light holes (dashed line).

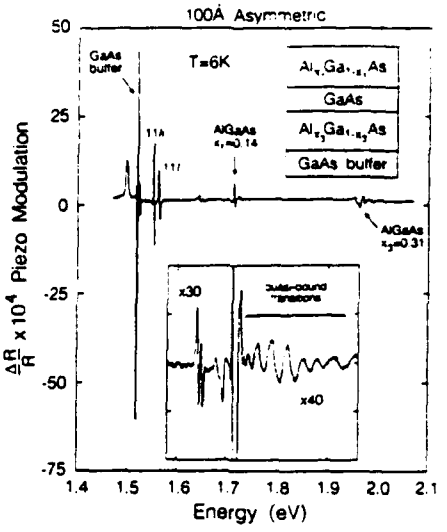


FIG. 2. Piezomodulated reflectivity spectrum of an asymmetric single quantum well of 100 Å width ($l_w$). The transition energies and their identifications are presented in Table I.

The resonant states participating in the *interband* transitions are those for which Ω is a maximum. We have identified the resonant quasi-bound states for the conduction as well as the heavy-hole and light-hole bands as occurring with energies corresponding to these maxima, with typical widths of 20 meV. A typical energy dependence of Ω for the heavy- and light-holes in a 100 Å well is shown in Fig. 1.

These quasi-bound resonant states exist at energies between the barriers in asymmetric wells. The boundary conditions on their wave functions differ from those for fully bound states in that to the left of the interface at the lower barrier the wave functions are travelling waves. The resonant states are those for which multiples of half their wavelengths can be very nearly fitted into the well region. However, these states are not as sharply defined in energy as their fully bound counterparts as can be seen in Fig. 2. The spectrum of the companion symmetric well is shown in Fig. 3. The transitions are labeled with the first number indicating the conduction band state and the second the valence band state, with "$h$" and "$l$" identifying heavy and light holes. The superscript "$q$" denotes a quasi-bound state.

The calculations were performed using the Al concentrations as determined from the excitonic signatures attributable to the barrier layers. Using the bound state energies given by the eight-band k·p model and the quasi-bound state energies by the peaks in $\Omega(E)$, we are able to identify the lines in the spectra resulting from transitions between both bound and quasi-bound states. The theoretical transition values presented in Table I have not been corrected for the excitonic binding energies.

We note that interest in asymmetric quantum wells has been based on the fact that they have second-order optical nonlinear susceptibilities which can be three orders of magnitude larger than those of bulk GaAs [$\chi^{(2)}_{GaAs}(SHG) \sim 2 \times 10^{-10}$ m/V, at 10.6 $\mu$m]. Asymmetry due to a compositional step change in the Al concentration inside the well,[9] due to the presence of an externally applied electric field,[10] or due to unequal well widths in double quantum wells[11] have been considered as means of removing the inversion symmetry in quantum well structures. The single quantum wells with unequal barrier heights studied here are the simplest of structures with inversion asymmetry. Our theoretical estimate[12] for the second-order nonlinear optical susceptibility $\chi^{(2)} \simeq 6 \times 10^{-7}$ m/V in the near infrared region from *interband* transitions for a 100 Å quantum well with Al concentrations of 10% and 40% on either side of the well, compare favorably with the

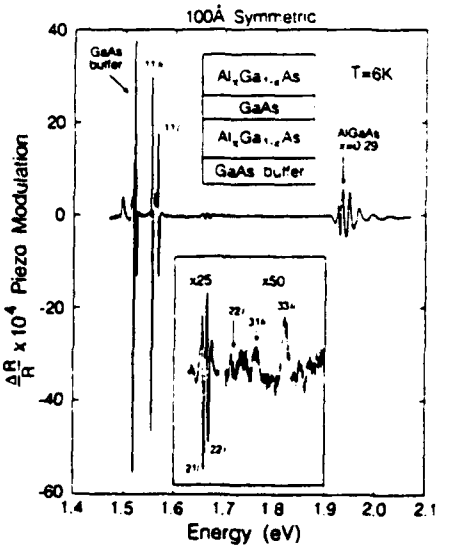


FIG. 3. Piezomodulated reflectivity spectrum of a symmetric single quantum well of 100 Å width ($l_w$).

TABLE I. Transition energies (eV) for the 100 Å asymmetric well. The transitions are labeled with the first number indicating the conduction band state and the second the valence band state, with "*h*" and "*l*" identifying heavy and light holes. The superscript "*q*" denotes a quasi-bound state. Note that the theoretical values are uncorrected for excitonic binding energies.

| Expt. | Theory | Identification |
|---|---|---|
| 1.551 | 1.557 | 1*h* |
| 1.562 | 1.571 | 1*l* |
| 1.604 | 1.611 | 3*h* |
| 1.644 | 1.648 | 2*l* |
| 1.651 | 1.655 | 2*h* |
| 1.681 | 1.688 | 3*h* |
| 1.694 | 1.698 | 2*l* |
| 1.735 | 1.728 | $3^{q}l$ |
| ... | 1.733 | $2^{4q}h$ |
| 1.742 | ... | ... |
| 1.759 | 1.782 | $3^{q}1h$ |
| 1.785 | 1.796 | $3^{q}1l$ |
| ... | 1.797 | $2^{5q}h$ |
| ... | 1.803 | $3^{q}2h$ |
| ... | 1.805 | $2^{3q}l$ |
| 1.812 | 1.836 | $3^{q}3h$ |
| 1.838 | 1.846 | $3^{q}2l$ |
| 1.862 | 1.881 | $3^{q}4^{q}h$ |
| 1.897 | ... | ... |

experimental *intraband* measurements.[9,10,12] An experimental study of the interband optical nonlinearity in our asymmetric quantum wells is envisaged.

In conclusion, we have shown that piezomodulation spectroscopy is capable of revealing transitions associated with above-barrier quasi-bound states in asymmetric quantum wells. The spectra provide direct experimental evidence for the existence of quasi-bound resonant states in both the valence and conduction bands in an asymmetric quantum well. The presence of such states can be exploited in photodetectors, modulators, and switching devices. A complete presentation of theoretical and experimental results for all the samples will appear in a later publication.

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# Spatial-harmonic gratings at high modulation depths in photorefractive quantum wells

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High-order spatial harmonics of photorefractive gratings are detected directly in multiwave mixing experiments in photorefractive AlGaAs/GaAs quantum wells operating in the Franz–Keldysh geometry. We have observed diffraction signals from the first-, second-, and third-harmonic refractive-index gratings. The quadratic electro-optic effect in the quantum wells guarantees a strong nonlinear response for generating a second-spatial-harmonic grating.

Photorefractive transport is strongly nonlinear and commonly leads to nonsinusoidal responses to interference fringes. Higher spatial harmonics of the resulting index grating can have amplitudes comparable with those of lower harmonics, especially under high modulation depth. Furthermore the nonlinear response of the material can mix the spatial frequencies of several individual gratings. These nonlinear effects can have image-processing applications, such as high-bandwidth image correlation[1] and nondestructive difference-frequency image readout.[2] These applications rely on obtaining a maximum nonlinear material response. On the other hand, recording nonlinearity can degrade the quality and density of holographic storage. Despite the importance of material nonlinearity, much of the early research on photorefractive responses has concentrated on linearized solutions to the transport equations. For a better understanding of the formation and role of higher harmonics and nonlinearities in photorefractive effects, theoretical studies have ranged from perturbative approaches and special cases[3–6] to solutions with high modulation depths and arbitrary electric-field strengths.[7–9] These studies have been restricted to materials with linear electro-optic effects.

In this Letter, we present experimental results on second-spatial-harmonic complex index gratings in photorefractive quantum-well samples with quadratic electro-optic effects. To make a comparison with higher spatial harmonics in bulk materials, we consider here only the Franz–Keldysh geometry, which generates the same transport processes as in bulk materials. The quadratic effect automatically guarantees a strong nonlinear response to sinusoidal illumination gratings, generating second-harmonic gratings by mixing the first-harmonic electric field with itself. The short interaction length of the quantum wells generates Raman–Nath diffraction, which removes the necessity for aligning probe beams to the Bragg condition. In our experiments, we observe the second- and the third-harmonic gratings directly in a multiwave mixing experiment.

Nonlinearity in the transport equations arises from several sources. One source is the feedback between charge transport and the resulting space-charge fields; another is depletion or saturation of available traps. Because of the feedback and saturation effects, a sinusoidal illumination intensity $I = I_0(1 + m \sin Kx)$ with spatial frequency $K$ and modulation index $m$ generates a nonsinusoidal space-charge electric field that has higher harmonic components. The internal field up to third order can be expressed as

$$E = E_0 + E_{sc} = E_0 - [E_1 \cos(Kx + \phi_1) + E_2 \cos(2Kx + \phi_2) + E_3 \cos(3Kx + \phi_3)], \quad (1)$$

where $E_0$ is the applied field and $E_1$, $E_2$, and $E_3$ are the first-, second-, and third-harmonic amplitudes that screen the applied field. (We consider only the case of large applied fields and negligible diffusion.) The Franz–Keldysh effect is a quadratic electro-optic effect that relates refractive index and absorption changes to the square of the local electric field. The complex index change is

$$\Delta\tilde{n} = -\frac{1}{2} n^3 \tilde{s} E^2, \quad (2)$$

where $\Delta\tilde{n} = \Delta n + i\Delta\kappa$, $\kappa = \alpha c/2\omega$ is the extinction coefficient, and $\tilde{s} = s_1 + is_2$ is the quadratic electro-optic coefficient. The squared internal field that appears in Eq. (2) is

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$$E_{sc}^2 = E_0^2 + \frac{1}{2}(E_1^2 + E_2^2 + E_3^2) - 2E_0E_1 \times \cos(Kx + \phi_1) + E_1E_2\cos(Kx + \phi_2 - \phi_1) + E_2E_3\cos(Kx + \phi_3 - \phi_2) + \frac{1}{2}E_1^2\cos(2Kx + 2\phi_1) - 2E_0E_2\cos(2Kx + \phi_2) + E_1E_3\cos(2Kx + \phi_3 - \phi_1) - 2E_0E_3 \times \cos(3Kx + \phi_3) + E_1E_2\cos(3Kx + \phi_1 + \phi_2). \quad (3)$$

The first and second terms represent the average-squared field. The next three terms represent the first-harmonic grating that is generated by mixing the first harmonic with the dc field, by mixing the second-harmonic electric field with the first harmonic, and by mixing the third harmonic with the second. Finally, the last two terms in Eq. (3) represent the third-harmonic grating, which can exist only under the condition of transport nonlinearity. Clearly, the quadratic electro-optic effect in these materials generates a strong nonlinear response to sinusoidal illumination. Even under conditions where no significant $E_2$ is present, there will still be a second-harmonic refractive-index grating because of the $E_1^2$ term.

According to the coupled-mode analysis,[10] Bragg and Raman–Nath diffraction regimes are distinguished by the dimensionless parameter

$$Q = \Delta kL = \frac{2\pi\lambda L}{n\Lambda^2}M^2, \quad (4)$$

where $M$ is the grating harmonic, $\Delta k$ is the $k$-vector mismatch because of deviation from the Bragg condition, $L$ and $n$ are the thickness and the refractive index of the medium, respectively, and $\lambda$ and $\Lambda$ are the wavelength of the probing beam and the fringe spacing of the intensity grating, respectively. When $Q < 1$, Raman–Nath diffraction occurs with multiple diffraction orders. The total diffraction efficiency into the $N$th order by the dielectric grating with a complex index of refraction grating, $\Delta\tilde{n} = (\Delta n + i\lambda\Delta\alpha/4\pi)\cos(MKx)$, is given by[10]

$$\eta_N = \frac{1}{N!^2}\left[\left(\frac{\pi\Delta nL}{\lambda_p\cos\theta_p'}\right)^2 + \left(\frac{\Delta\alpha L}{4\cos\theta_p'}\right)^2\right]^N, \quad (5)$$

where $\theta_p'$ is the internal angle of the probe beam. The direction of the $N$th-order diffraction from the $M$th harmonic is given by $\sin\theta_N = NMK\lambda/2\pi + \sin\theta_p$, where $\theta_p$ and $\theta_N$ are the external incident and diffraction angles of the probing and the diffracted beams, respectively. In our experiments, we consider only the first diffraction order $N = 1$, but first-, second-, and third-harmonic gratings $M = 1, 2, 3$. The first-order diffraction efficiencies for our sample are $\eta_1 \approx 10^{-4}$, which makes $\eta_2 \approx 10^{-8}$, which is below our detection limit. In the small modulation regime, $E_1$ and $E_2$ in Eq. (3) are proportional to $m$ and $m^2$, respectively. For first-order diffraction, Eq. (5) in conjunction with Eqs. (3) and (2) will produce an $m^2$ dependence for diffraction from the first-harmonic grating and an $m^4$ dependence for diffraction from the second-harmonic grating.

The structure of the semi-insulating multiple quantum wells (SIMQW's) has been described previously.[11,12] The optical interaction region of our SIMQW sample is composed of 60 periods of GaAs wells (7.5-nm thickness) and $Al_{0.3}Ga_{0.7}As$ (10-nm thickness) barriers, with a total optical interaction length of 1.05 $\mu$m. The sample was made semi-insulating by proton implantation. This process introduces deep-level defects that provide traps to store charge and pin the Fermi-level midgap, which makes the entire sample semi-insulating. The electro-optic properties of the sample were characterized in the Franz–Keldysh geometry with the applied field parallel to the quantum wells. Two exciton absorption peaks at 838 and 826 nm, corresponding to heavy and light holes, respectively, were observed in our differential transmission measurement. The infrared light source in our experiment was a Ti:sapphire laser tuned from 800 to 850 nm, which covered the exciton absorption range of the SIMQW.

Our multiwave mixing experimental setup is shown in Fig. 1. The SIMQW is illuminated symmetrically with respect to the normal vector of the quantum-well plane by two coherent laser beams, with each beam polarized perpendicular to the plane of incidence and parallel to the quantum-well layers. The intensities of the two beams are approximately equal. A dc-biased ac field is applied across the sample in the direction indicated in Fig. 1. To justify the diffraction regime of our measurement, typical values of our measurements were $L = 1$ $\mu$m, $\lambda = 840$ nm, $n = 3.6$ for GaAs wells, and $\Lambda = 4.6$ $\mu$m. Thus $Q = 0.14$, putting us in the strong Raman–Nath regime.

First-order diffraction signals were observed from the fundamental, second-, and third-spatial-frequency gratings. The dependence on the modu-

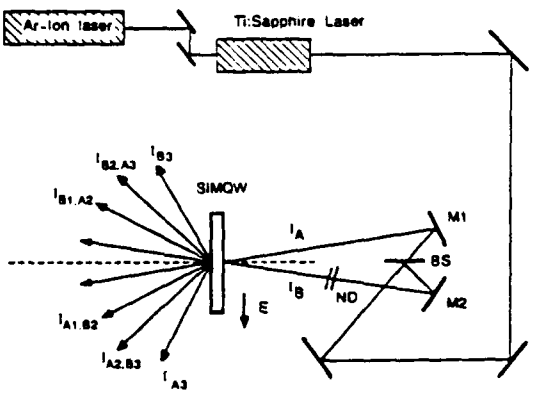


Fig. 1. Experimental geometry for the multiwave mixing experiment. The two beams $I_A$ and $I_B$ write intensity fringes that generate first- and higher-harmonic index gratings. The electric field is applied in the plane of the quantum wells. The multiple diffracted beams all arise from first-order diffraction but from different spatial harmonics of the index grating. ND, neutral-density filter; BS, beam splitter; M1, M2, mirrors.

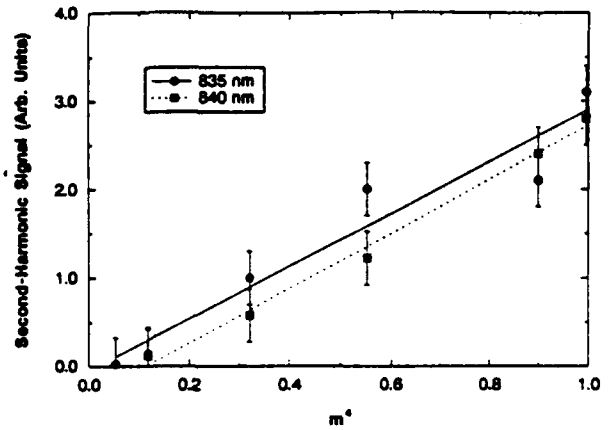


Fig. 2. Diffraction from the second-harmonic grating as a function of the fourth power of the modulation index. The data at 840 and 835 nm are from the zero crossings in the electroabsorption. The lines are the best fits.

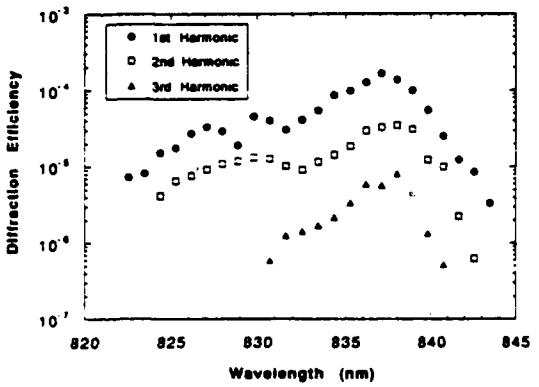


Fig. 3. Diffraction efficiency versus wavelength for diffraction from the first-, second-, and third-harmonic gratings. The modulation index is $m \approx 1$, and $\Lambda = 8.8$ $\mu$m. The data have been averaged for both field directions.

lation index $m$ of the diffraction signal from the second-spatial-harmonic grating was measured at the zero crossings of electroabsorption with $\Lambda = 4.6$ $\mu$m. The results are shown in Fig. 2. The diffraction efficiency exhibits an approximately $m^4$ dependence at both wavelengths, which is consistent with the expectation from Eqs. (3) and (5) and is also in agreement with earlier experimental and numerical results.[1,7]

The wavelength dependences of the diffraction efficiencies for beam $I_A$ are shown in Fig. 3. The measurement was performed with a larger fringe spacing of $\Lambda = 8.8$ $\mu$m. The diffraction from the first harmonic is larger than the diffraction from the second harmonic. An estimate of $E_1/E_2$ can be made by taking the largest terms in Eq. (3). As a result, we have

$$\frac{\eta_1(2K)}{\eta_1(K)} = \left(\frac{E_2}{E_1} - \frac{E_1}{4E_0}\right)^2 \approx \frac{1}{4}, \qquad (6)$$

which yields an $E_2$ that is 75% of the strength of $E_1$. This value is consistent with numerical results from Ref. 7 for a large modulation depth.

We found that the first diffraction order from the fundamental spatial frequency grating depends on the direction of the applied field, although the measurement of differential transmission shows no indication of field-direction dependence. Two processes may be related to this asymmetry in a diffraction order. First, there is an interference effect between the first-order diffraction signal of $I_A$ from the fundamental spatial-frequency component of the grating and the first-order diffraction signal of $I_B$ from the double spatial-frequency grating component. Second, the intensities of $I_A$ and $I_B$ can be field-direction dependent because of two-wave mixing and beam depletion.[12] More research is needed to clarify the contribution of each process to the asymmetry effect.

In conclusion, we have directly observed diffraction from second- and third-spatial-harmonic gratings in photorefractive quantum wells. In addition to second-harmonic electric-field components that arise from transport nonlinearity, second-harmonic complex index gratings are generated by the quadratic electro-optic effect. Our Franz–Keldysh geometry generates the same transport processes as in bulk samples, which allows direct study of higher spatial harmonics in photorefractive gratings under high modulation depths and in the presence of simultaneous electron and hole transport. These studies will have relevance to near-resonant photorefractive properties,[13] which share much of the underlying physics.

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# A Vertically Integrated GaAs Bipolar Dynamic RAM Cell with Storage Times of 4.5 h at Room Temperature

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*Abstract*—**The storage times of FET-accessed GaAs dynamic RAM cells are limited to less than 1 min at room temperature by gate leakage in the access transistor. These transistor leakage mechanisms have been eliminated by designing a vertically integrated DRAM cell in which an n-p-n bipolar access transistor is merged with a p-n-p storage capacitor. Storage times of 4.5 h are obtained at room temperature, a 1000-fold increase over the best FET-accessed cells.**

## I. Introduction

DYNAMIC charge storage on p-n junctions in GaAs is very efficient both in charge storage density ($>1.9$ fC/$\mu m^2$ at 1 V) [1] and storage time ($>6$ h at room temperature) [2]. However, when the p-n junction storage capacitor is connected to a field-effect access transistor (FET-access) to form a one-transistor dynamic random access memory (DRAM) cell, gate leakage in the field-effect transistor reduces the overall storage time to less than 1 min at room temperature [1]. Generally, storage times of this magnitude are adequate for DRAM applications since refresh rates are typically around 1 kHz. However, because gate leakage increases exponentially with temperature, the upper operating temperature of FET-accessed GaAs DRAM cells is limited.

The gate leakage currents associated with FET-accessed DRAM cells can be eliminated by using a bipolar access transistor. Silicon bipolar DRAM's were investigated in the mid-1970's [3], [4], and circuits of up to 16-kb complexity were demonstrated. In this letter, we report on the first bipolar DRAM cells realized in GaAs, and the first DRAM cells in any semiconductor to have room-temperature storage times measured in hours [5].

## II. Device Structure and Fabrication

Fig. 1 illustrates a GaAs n-p-n bipolar access transistor vertically integrated with a p-n-p storage capacitor. In this design, the floating collector of the access transistor is merged with the n-region of the storage capacitor. During operation as a DRAM, the n-type emitter is connected to the bit line, the p-type base is connected to the word line, and the p-type substrate serves as the ground plate of the storage capacitor. The structure of Fig. 1 was fabricated on epitaxial layers grown in a Varian GEN-II molecular beam epitaxy system. The doping densities and layer thicknesses chosen for the p-n-p storage capacitor are optimal for charge storage density and storage time requirements [1]. The doping and thicknesses of the n-p-n bipolar transistor, however, have not been optimized for high-speed, low-power digital circuit applications.

A four-level non-self-aligned process was used to define discrete DRAM cells with dimensions ranging from $36 \times 48$ to $90 \times 120$ $\mu m^2$. The emitter was defined by wet chemical etching, and was contacted by thermally evaporating AuGe and alloying at 370°C for 90 s. (It has been found that electron-beam evaporation severely degrades storage times [5]; details will be reported elsewhere [2].) In order to avoid damage during testing, a 200-nm overlayer of Au was evaporated following the anneal. This Au also served as the nonalloyed ohmic contact to the $p^+$-base region. The devices were completed with a mesa-isolation etch to a depth of 300 nm.

## III. Experimental Results

For these experiments, the charge state of the bipolar DRAM is determined by monitoring the capacitance between the $p^+$-base and the p-type substrate. When the n-type floating collector is at zero bias with respect to the substrate, a high capacitance is measured. This state represents a logic ZERO. A logic ONE is written to the cell when a positive bias is simultaneously applied to the bit line and the word line. At this instant, a positive bias is developed across the base–collector junction allowing electrons to flow from the n-type floating collector to the bit-line contact. This action charges the n-region to a positive potential with respect to the substrate, thereby causing the collector–substrate $p^+$-$n$ junction to become reverse biased and the measured capacitance to drop. When the word line is returned to ground potential, the only source of electrons to return the floating collector to equilibrum are those supplied by thermal generation. This recovery process is monitored by observing the capacitance transient following the turn-off of the access transistor.

The room-temperature capacitance transient of a $36 \times 48$-$\mu m^2$ bipolar DRAM cell is shown in Fig. 2. Initially, no bias is applied to the bit line and the word line. In order to assure that the floating collector is at zero bias with respect to the

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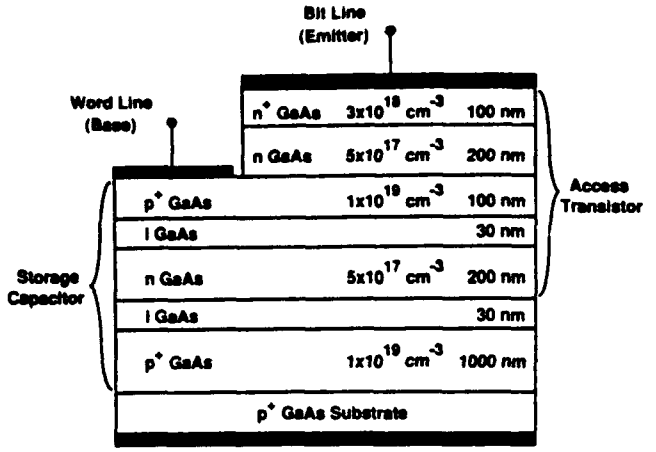


Fig. 1. Cross section of the first GaAs bipolar DRAM cell. The top n-p-i-n layers function as a bipolar access transistor, while the bottom p-i-n-i-p layers serve as the storage capacitor. The middle p-i-n layers are common to both.

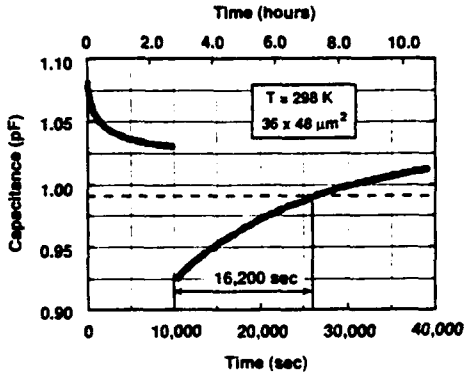


Fig. 2. Charge storage transient of the bipolar DRAM cell at room temperature monitored by observing the capacitance of the base terminal. The sample was illuminated for $t < 0$ to insure the storage cell was not depleted of electrons. The illumination was removed at $t = 0$. A 1-V pulse was applied to base and emitter terminals at $t = 10\,000$ s to empty the storage well.

substrate, for time $t < 0$ the cell is exposed to light, causing the $p^+$-n junctions of the storage node to become slightly forward biased. At time $t = 0$, the light is removed and the recombination of excess carriers returns the cell to its zero-bias equilibrium value. After 10 000 s, a positive pulse is applied to the bit line and the word line causing a sharp decrease in the capacitance of the cell. When the bias is removed 600 s later, an exponential capacitance recovery is observed. The storage time of a cell is defined as the time required for the capacitance to return to within $1/e$ of its equilibrium value. Using this definition, the room temperature storage time of this bipolar DRAM cell is approximately 16 200 s or 4.5 h.

Plots of storage time versus temperature for complete bipolar DRAM cells with various perimeter-to-area ratios are shown in Fig. 3. An activation energy $E_A$ for the generation process can be determined from an exponential fit to this experimental data using

$$\tau_s = C_1 \exp(E_A / k_B T) \qquad (1)$$

where $C_1$ is a proportionality constant, $k_B$ is the Boltzmann

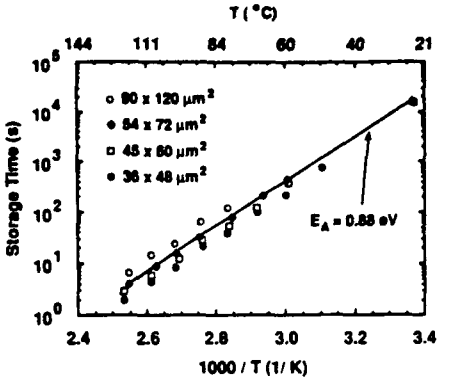


Fig. 3. Storage time as a function of temperature for several different bipolar DRAM cells. If 100 ms is taken as the minimum storage time for proper operation, these cells should function at temperatures above 130°C.

constant, and $T$ is the absolute temperature. For the 54 × 72-$\mu m^2$ cell, $E_A = 0.88$ eV. The larger (90 × 120 $\mu m^2$) cell has a lower activation energy, while the smaller cells have activation energies greater than 0.88 eV. This variation is expected because the storage time is comprised of components due to bulk and perimeter generation [1]. In particular,

$$\frac{1}{\tau_s} = C_2\left(G_B + G_P\frac{P}{A}\right) \qquad (2)$$

where $C_2$ is a proportionality constant, $G_B$ is the bulk generation rate, $G_P$ is the perimeter generation rate, $P$ is the perimeter, and $A$ is the area of the device. By combining (1) and (2), the bulk and perimeter activation energies can be separated. For these devices, $E_{A,\text{Bulk}} = 0.7$ eV while $E_{A,\text{Perimeter}} = 1.0$ eV. Therefore, as device size decreases, the effective activation energy tends towards that of the perimeter. At room temperature all four devices have storage times of approximately 4.5 h. In digital circuits where a minimum storage time of 100 ms is specified, these bipolar DRAM cells could be used in applications where the operating temperature exceeds 130°C.

Writing the value of the bit line into a cell through the access transistor is demonstrated in Fig. 4. The top waveform is the room-temperature capacitance of the cell measured between the word-line (base) and substrate contacts, and the bottom waveform is the voltage applied to the bit-line (emitter) contact. On this time scale, 100 s per division, the short 1-ms word-line pulses could not be captured readily on a digitizing oscilloscope and are not shown in this figure. Instead, it should be noted that the 3-V, 1-ms word-line pulses occur when there is an abrupt change in the capacitance signal. The data on the bit line are written into the cell during each 1-ms pulse applied to the base of the transistor. Initially, a logic ONE is stored in the DRAM cell, and a low capacitance is measured. During the first pulse, the bit-line voltage is low and the capacitance rises, indicating that the cell has returned to its zero-bias equilibrium state. As described previously, the capacitance decay is due to the turn-off time of the forward-biased base–collector $p^+$-n junction. Likewise, during the second word-line pulse, the bit-line voltage is high and the capacitance falls, indicating charge has been removed from the storage capacitor. This lower

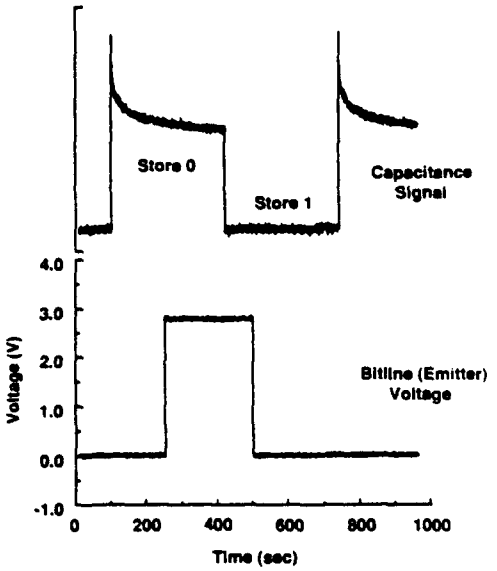


Fig. 4. Electrical writing of the bipolar DRAM cell. For this test, the charge state of the cell is monitored by observing the base capacitance. The low-capacitance store-ONE state is the nonequilibrium condition. This capacitance will gradually increase with a time constant of 4.5 h at room temperature.

capacitance value represents the nonequilibrium state of the cell and will rise exponentially with a time constant of about 4.5 h. This rise is imperceptible on the time scale of these waveforms.

The stored information has been read electrically by monitoring the bit-line voltage with a low-capacitance active probe. The bit-line voltage excursions during a read ONE and a read ZERO differ by approximately 250 mV. In an integrated circuit application, this voltage difference would be detected by sense amplifiers and latched for data readout.

In addition to increased storage times over FET-accessed cells, the bipolar design has several other distinct advantages. First, since no applied bias is required during the store state and there are no measurable leakage currents, the bipolar cell has zero static power dissipation and could be used as a short-term nonvolatile memory. Moreover, the access times of bipolar cells should be shorter than those of FET-accessed DRAM's because charge is removed vertically rather than laterally. Finally, since the storage capacitor is vertically integrated with the bipolar access transistor, no additional area is needed for the access transistor. Consequently, a complete DRAM cell capable of storing approximately one million electrons with a 1-V reverse bias could be fabricated in an area as small as $5 \times 5\ \mu m^2$.

## IV. Summary

In summary, a vertically integrated GaAs bipolar DRAM cell that eliminates the gate leakage present in FET-accessed cells has been described. Electrical reading and writing of the cell have been demonstrated, and storage times of 4.5 h at room temperature and greater than 100 ms at 130°C have been observed. These storage times represent a 1000-fold increase over those reported for FET-accessed DRAM cells. Moreover, since no applied bias is needed during the store state, the bipolar DRAM has potential for use as a short-term nonvolatile memory.

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# Arsenic precipitate accumulation and depletion zones at AlGaAs/GaAs heterojunctions grown at low substrate temperature by molecular beam epitaxy

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$Al_xGa_{1-x}As$/GaAs heterojunctions were grown by molecular beam epitaxy under normal growth conditions except that the substrate temperature was 250 °C. After a 1 h anneal at 600 °C, a narrow precipitate depletion (PD) zone was observed on the $Al_xGa_{1-x}As$ sides of the heterojunctions, while a high density precipitate accumulation (PA) zone was observed on the GaAs sides. The formation of these PD and PA zones is explained as a result of diffusion of excess As atoms across the interface from the $Al_xGa_{1-x}As$ layer to the GaAs layer. No significant difference in PD and PA zones was found at interfaces between $Al_xGa_{1-x}As$ grown on GaAs and GaAs grown on $Al_xGa_{1-x}As$, indicating a negligible effect due to the growth sequence. Widths of PDs were about 250 Å, exhibiting a weak dependence on the Al concentration of the $Al_xGa_{1-x}As$ layers.

GaAs and $Al_xGa_{1-x}As$ epilayers that are grown by molecular beam epitaxy (MBE) under "normal" group III–V fluxes but at very low substrate temperatures contain as much as 1% excess arsenic.[1] Upon annealing these epilayers at a temperature of 600 °C, the excess arsenic forms precipitates (GaAs:As, $Al_xGa_{1-x}As$:As).[2–4] Because of their unique electrical and optical properties, these III–V:V epilayers have found many device applications[5–13] since Smith *et al.*[5] first used GaAs:As to eliminate side gating in GaAs metal semiconductor field effect transistors. In this article we present our study of arsenic precipitate formation at annealed $Al_xGa_{1-x}As$/GaAs heterojunctions which were grown at low substrate temperatures.

The film used in this work was grown in a Varian GEN II MBE system. A GaAs buffer layer was first grown at 600 °C and then the substrate temperature was lowered to 250 °C while continuing to grow GaAs. The heterojunctions were then grown at a substrate temperature of 250 °C using $As_2$, two Ga effusion furnaces, and one Al effusion furnace. The growth rate was 1 μm/h and the group V to total group III beam equivalent pressure was kept at 20 for the GaAs and $Al_xGa_{1-x}As$ layers. This was possible without growth interruptions by adjusting the temperatures of the two Ga and the Al effusion furnaces during growth. Three heterojunctions of different Al concentration were contained in the film as shown in Fig. 1. The $Al_xGa_{1-x}As$ and GaAs layers were all of about 0.2 μm in thickness. After growth the film was annealed in the MBE chamber at 600 °C for 1 h under an $As_2$ flux.

Distributions of As precipitates in the $Al_xGa_{1-x}As$/GaAs multilayer structure were examined by using a JEM 2000EX electron microscope. Cross-sectional samples parallel to {110} planes were prepared by Ar ion milling at low temperatures for the transmission electron microscope (TEM) observations. The TEM images show the presence of a high density of As precipitates in all layers grown at 250 °C. No significant differences in the sizes or densities of the precipitates were found between the GaAs and $Al_xGa_{1-x}As$ layers. The average diameter of the precipitates is 80 Å and their density is in the range of $10^{16}$ cm$^{-3}$. These values are comparable to those obtained in earlier studies of GaAs:As and $Al_xGa_{1-x}As$:As layers.[2–4]

At each $Al_xGa_{1-x}As$/GaAs interface, a narrow precipitate depletion (PD) zone was found on the $Al_xGa_{1-x}As$ side. Figure 2 is a 200 dark field image of an interface between $Al_{0.3}Ga_{0.7}As$ and GaAs. In the image, $Al_{0.3}Ga_{0.7}As$ and GaAs layers appear as bright and dark regions respectively, and the As precipitates are seen as dark spots. As seen in the image, a narrow PD zone with a width of about 250 Å exists along the interface on the $Al_{0.3}Ga_{0.7}As$ side. The image also shows the existence of a precipitate accumulation (PA) zone on the GaAs side of the interface, in which the density of the As precipitates is higher than that in the interior of the GaAs layer. These PD and PA zones were observed at all $Al_xGa_{1-x}As$/GaAs interfaces in this sample. Figure 3 is a 200 dark field image showing all three $Al_xGa_{1-x}As$ layers. Two important points regarding the PD zones are seen in this image. First is the existence of similar PD and PA zones in both normal and inverted interfaces, which indicates no significant dependence of the formation of these zones on the growth sequence. The second point is the nearly identical widths of the PD zones at all interfaces, suggesting no or a weak dependence on the Al concentration in the $Al_xGa_{1-x}As$ layers.

The TEM observations described above suggest that the

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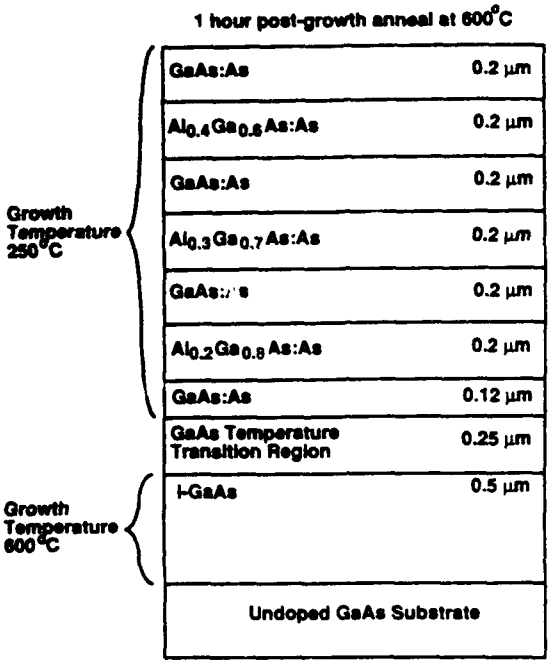


FIG. 1. Cross section of the film structure

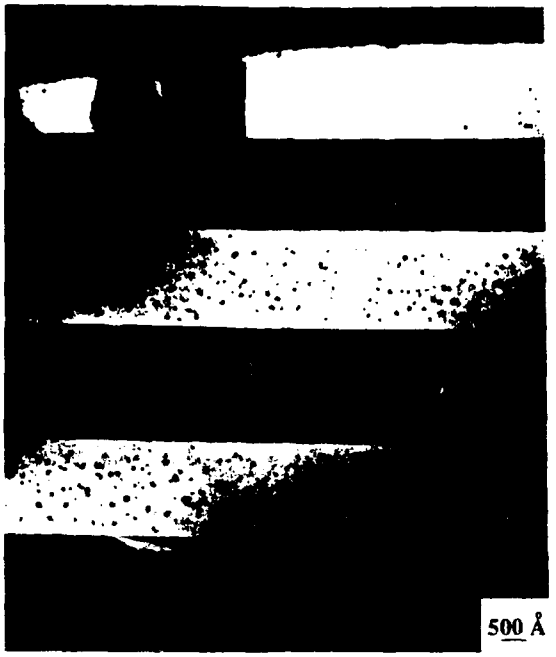


FIG. 3. 200 dark field image of three $Al_xGa_{1-x}As$/GaAs heterojunctions.

formation of PD and PA zones is a result of diffusion of excess As from an $Al_xGa_{1-x}As$ layer to a GaAs layer during the post-growth anneal. It is difficult to assume that these zones resulted from nonuniform concentrations of excess As in the as-grown sample. The flux ratio of As to group III elements was kept approximately constant during the growth of the multilayer structure, which should yield a uniform As concentration in each layer. In addition, the symmetrical appearance of PD and PA zones between normal and inverted interfaces rules out the possibility that the PD and PA zones resulted from a change of the flux condition at a transition from one layer to the next layer. It is also difficult to assume that excess As atoms exist in these PD zones with the same concentration as that in the interior of an as-grown $Al_xGa_{1-x}As$ layer but have not formed precipitates.


FIG. 2. 200 dark field image of the interface at the $Al_{0.3}Ga_{0.7}As$/GaAs heterojunctions

The diffusion of excess As from an $Al_xGa_{1-x}As$ layer to a GaAs layer during post-growth anneal is suggested by the following observations. The average spacing of the As precipitates in the interior of the $Al_xGa_{1-x}As$ layers and of the widths of the PD zones is similar. This similarity is explained by the fact that both lengths are determined by the mean square distance of the diffusion of individual As atoms for the period of the post-growth anneal. (It should be noted that TEM images in Figs. 2 and 3 correspond to projections of three-dimensional microstructures so the spacing of the As precipitates in the images appear smaller than they are.) The other and more direct evidence is the existence of a PA zone along each PD zone. The difference of the precipitate density between a PA zone and an interior of a GaAs layer appears to correspond well to the density of precipitates that are missing in the PD zone. In an earlier study, we observed a PD zone in an $Al_{0.3}Ga_{0.7}As$:As/GaAs:As heterostructure that was annealed at 600 °C for a half-hour.[4] The width of the PD zone in that sample was found to be smaller than those in the present sample as expected from its shorter annealing time.

The most interesting aspect of the PD and PA zones is the driving force for the diffusion of excess As across an interface. As seen from densities of As precipitates in interiors of GaAs and $Al_xGa_{1-x}As$ layers, no significant difference of the As concentration exists between the two layers in the as-grown sample. Therefore, it is unlikely that the As diffusion across the interface is caused by a gradient of the As concentration. The difference that can be found in the present sample is only the presence and the absence of Al on the two sides of the interface. Therefore, our

# Increased thermal generation rate in GaAs due to electron-beam metallization

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Leakage currents due to thermal generation in a reverse-biased *p-n* junction can be accurately monitored by measuring the capacitance recovery transient of a *p-n-p* structure. Using this technique, it has been demonstrated that the thermal generation in the bulk depletion region of GaAs *p-n* junctions grown by molecular beam epitaxy can be as much as three orders of magnitude greater for samples metallized in electron-beam evaporators as compared to thermal evaporators. The increase in thermal generation rate is shown to be dependent upon the device area exposed during the evaporation, the type of metal initially evaporated onto the sample, the growth conditions during molecular beam epitaxy, and the depth of the *p-n* junction from the semiconductor surface.

## INTRODUCTION

Electron-beam (E-beam) evaporation of metals for use as ohmic or Schottky contacts and first-level interconnects is a common fabrication technique used in planar GaAs integrated circuit (IC) processes.[1] Recently, however, it has been reported that metallization performed using E-beam evaporation causes a factor of five degradation in the mobility of a modulation-doped two-dimensional electron gas (2-DEG)[2] and a slight increase in the forward-biased current of Schottky barrier diodes.[3] The effect of E-beam metallization on the thermal generation rate in the bulk depletion region of GaAs *p-n* junctions is also significant.[4] In this paper, it is demonstrated that thermal generation rates can increase by more than three orders of magnitude when samples are metallized in E-beam evaporators rather than in thermal evaporators. Moreover, it is shown that this increase in thermal generation rate is dependent upon the device area exposed during the evaporation, the type of metal initially evaporated onto the sample, the growth conditions used during molecular beam epitaxy (MBE), and the depth of the *p-n* junction from the semiconductor surface.

## DEVICE FABRICATION

In order to investigate the effect of E-beam metallization on the generation rate, several structures like the one shown in Fig. 1 were grown in a Varian GEN II MBE system on two-inch diameter, non-indium-mounted $p^+$-GaAs substrates. The growths were conducted at a substrate temperature of 600 °C, a growth rate of 1 μm/h, and a group V molecule to Ga beam equivalent pressure of 20 (as measured with an ion gauge in the substrate growth position). The arsenic species used in one growth was the dimer $As_2$, while the tetramer $As_4$ was used in all other growths.

Each film was divided into three samples that were processed simultaneously using the following procedure. First, an electrical contact was made to the $p^+$ substrate by alloying indium. A liftoff procedure was then used to form the top ohmic contacts. In this process, a 1.5 μm layer of AZ1350J-SF positive photoresist protected areas of the wafer where no metal film was desired. Approximately 250 nm of metal was deposited onto two of the three samples using a 9-kV Airco Temescal E-beam evaporator. On the first sample, the contact to the top $p^+$-region was formed using 250 nm of Au, while the contact to the second sample was formed using 100 nm of Ti followed by 150 nm of Au. The third piece of each film was used as a control sample, and in this case 250 nm of Au was deposited in a Norton Research Corporation (NRC) thermal evaporation system. Following the metal liftoff, the devices were completed with a mesa-isolation etch in 1 $NH_4OH$:3.5$H_2O_2$:500 DI.

## MEASUREMENT TECHNIQUE

The *p-i-n-i-p* buried-well structure shown in Fig. 1 can be used to monitor very accurately the small currents due to thermal generation in a reverse-biased GaAs *p-n* junction. When using this structure, the thermal generation currents are observed by measuring the depletion capacitance between the top and bottom $p^+$-GaAs regions.[5–7] More specifically, a positive voltage is applied to the top $p^+$ contact to deplete the floating *n* region of electrons and charge it to a positive potential with respect to the substrate. After charging the *n* region, the applied voltage is removed and the top contact is grounded. The *n* region then returns to an equilibrium condition due to reverse-bias leakage currents which result primarily from generation in the bulk space-charge region of the two *p-n* junctions and generation at the mesa-etched perimeter. During this recovery process, a capacitance transient can be observed as the reverse-bias depletion widths shrink.

For the *p-i-n-i-p* structure, this capacitance recovery transient can be characterized by a time constant $\tau_s$ which is inversely proportional to the generation rate. In particular,[6,7]

$$\tau_s = N_B\left[\frac{1}{G}\right] = N_B\left[\frac{1}{G_B + G_P(P/A)}\right], \quad (1)$$

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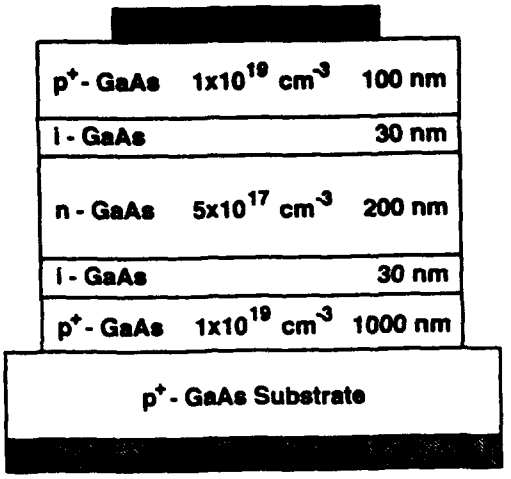


FIG. 1. Cross section of the *p-i-n-i-p* structure used to characterize the leakage currents due to thermal generation in a reverse-biased GaAs *p-n* junction. Thin intrinsic regions are included to reduce the peak electric field, thereby eliminating field-enhanced generation.

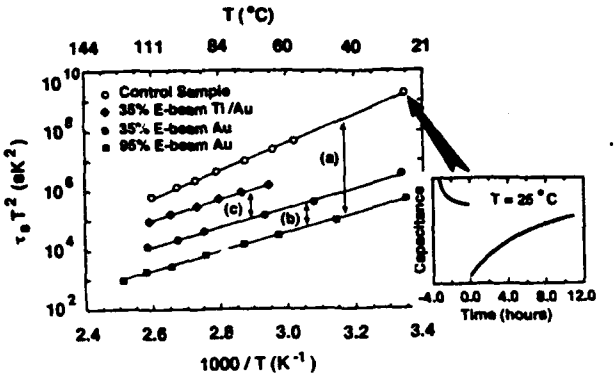


FIG. 2. Recovery time constant as a function of temperature for 100 $\times 100\ \mu m^2$ devices fabricated on the film grown using $As_2$-flux. The insert shows the room temperature capacitance transient of a device on the control sample. The room temperature transient has a time constant of approximately 6 h.

where $G$ is the total generation rate, $G_B$ is the bulk generation rate, $G_P$ is the effective perimeter generation rate, $P/A$ is the diode perimeter-to-area ratio, and $N_B$ is the doping concentration given by

$$N_B = \frac{N_D N_A}{N_D + N_A}, \tag{2}$$

where $N_D$ is the donor concentration and $N_A$ is the acceptor concentration. If a device is dominated by bulk generation ($G_B \gg G_P P/A$), the recovery time constant can be expressed as

$$\tau_{sB} = \frac{N_B}{G_B} = \frac{N_B \tau_g}{n_i}, \tag{3}$$

where $n_i$ is the intrinsic carrier concentration, and $\tau_g$ is the bulk generation lifetime. For a perimeter-dominated device ($G_P P/A \gg G_B$),

$$\tau_{sP} = \frac{N_B A}{G_P P} = \frac{N_B A}{s_0 n_i P}, \tag{4}$$

where $s_0$ is the surface generation velocity. By substituting expressions for $\tau_g$, $s_0$, and $n_i$[8] (3) and (4) can be rewritten in an exponential form given by

$$\tau_{sB} = \frac{C_1}{T^2} \exp(E_{AB}/k_B T), \tag{5}$$

$$\tau_{sP} = \frac{C_2}{T^2} \exp(E_{AP}/k_B T), \tag{6}$$

where $C_1$ and $C_2$ are proportionality constants, $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, and $E_{AB}$ and $E_{AP}$ are the effective bulk and perimeter generation activation energies, respectively. The $T^2$ temperature-dependent prefactor arises from the temperature dependences of the thermal velocity included in $\tau_g$ and $s_0$ and the effective density of states term included in $n_i$. For the purpose of analysis, it will be assumed that the recovery time constant $\tau_s$ can be approximated by a single exponential term. In this case,

$$\tau_s = \frac{C_3}{T^2} \exp(E_A/k_B T), \tag{7}$$

where $C_3$ is a proportionality constant and $E_A$ is an effective activation energy of the total generation process.[7] Using (7), values for $E_A$ can be obtained from an exponential fit to a $\ln(\tau_s T^2)$ vs $1/T$ Arrhenius plot.

## EXPERIMENTAL RESULTS

The recovery time constant as a function of temperature for $100 \times 100\ \mu m^2$ devices fabricated on the film grown using $As_2$ flux are shown in Fig. 2. In this figure, data for the control sample are indicated by open circles, while data for samples with contacts formed by E-beam metallization are indicated with filled squares, circles, and diamonds. The various filled markers are also used to represent data for samples having different contact metal-to-active area ratios and/or different contact metals. In particular, filled squares represent devices with a 95% metal-to-active area Au contact, filled circles represent devices with a 35% metal-to-active area Au contact, and filled diamonds represent devices with a 35% metal-to-active area Ti/Au contact.

Several important conclusions regarding the effect of E-beam metallization can be drawn from the data given in Fig. 2. Most significantly, more than a three order of magnitude degradation in the recovery time constant is observed at all measured temperatures following E-beam deposition of Au. This difference is labeled (a) in Fig. 2. For example, the room-temperature recovery time constant for the control sample is approximately 6 h, as shown in the insert of Fig. 2, whereas the time constant is only 4.5 s for devices with 95% metal-to-active area E-beam evaporated Au contacts. The activation energy of the generation process is also reduced by E-beam evaporation, from about 0.92 eV for the thermally-evaporated control sample to

approximately 0.63 eV for the E-beam evaporated samples. Similar experiments performed in a Varian E-beam evaporation system yield comparable results. However, there is evidence to suggest that the degree of degradation may vary with the type and design of E-beam evaporator used to deposit the metal.[9]

The data in Fig. 2 also indicate that the increase in the generation rate is proportional to the active area exposed during the E-beam metal deposition. In particular, the line segment labeled (b) in Fig. 2 shows the difference between the recovery time for devices with 35% and 95% metal-to-active areas. To explain this result, the expression for recovery time given in (1) can be extended to include a term due to the metallized area $A_M$. In particular,

$$\frac{1}{\tau_s}=\frac{1}{N_B}\left[G_M\frac{A_M}{A}+G_B\frac{(A-A_M)}{A}+G_P\frac{P}{A}\right]$$

$$=\frac{1}{N_B}\left[(G_M-G_B)\frac{A_M}{A}+G_B+G_P\frac{P}{A}\right], \qquad (8)$$

where $G_M$ is the bulk generation rate under the metal contact and $G_B$ is the bulk generation rate under the nonmetallized device area. Figure 3(a) shows the reciprocal of the room-temperature recovery time plotted as a function of metal contact-to-active area for devices metallized with E-beam evaporated Au. By comparison to (8), it is evident that the recovery is dominated by generation in the bulk regions below the metal contacts ($G_M$) which were not protected by photoresist during E-beam evaporation. Moreover, generation in bulk regions outside the metal contact ($G_B$) and generation at the etched perimeter ($G_P$) are negligible compared to generation under the metal contact, as suggested by the shaded area at the bottom of the graph. In contrast, Fig. 3(b) shows that the control sample, which was not exposed to the E-beam environment, has clearly discernible bulk and perimeter components.

Finally, line segment (c) of Fig. 2 demonstrates that the generation rate is also a function of the type of metal initially evaporated onto the sample. When Ti is used as the first layer of the metal contact, the degradation in the recovery time constant is one order of magnitude less than when Au is deposited directly onto the GaAs. Similarly, Auret *et al.* found that Schottky barrier diodes (SBD's) formed with Ti were of higher quality than SBD's made with Pt.[3] This group determined that during deposition, stray electrons from the electron gun introduce defects in *n*-type GaAs. The difference was attributed to the lower E-beam intensity used to melt Ti and the corresponding reduction in electron dose imparted to the sample during the evaporation. This conclusion is consistent with the results presented here since a higher E-beam intensity was used during the Au evaporation than during the Ti evaporation.

## ACTIVATION ENERGY OF THE CONTROL SAMPLE

The difference in measured activation energies of 0.92 eV for the control sample and 0.63 eV for the E-beam

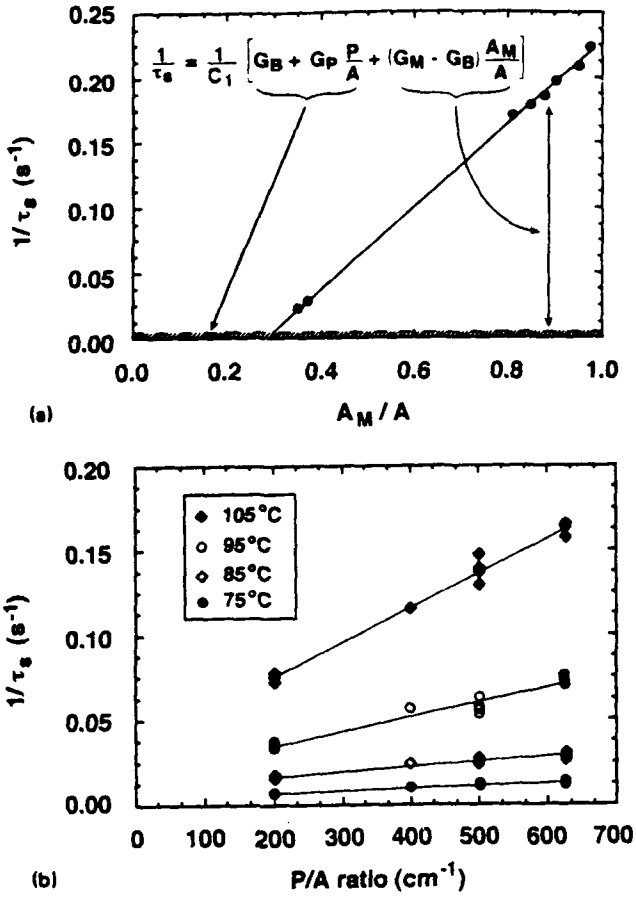


FIG. 3. (a) Inverse recovery time constant at room temperature as a function of metallized area for devices with E-beam evaporated Au. For small metal-to-active area ratios, the reverse-biased leakage results primarily from generation in the bulk space-charge region and generation at the mesa-etched perimeter (indicated schematically by the dashed line). For ratios larger than 0.3, however, the leakage is due to generation in the bulk depletion region under the metal contact. (b) Inverse recovery time constant of the thermally-evaporated control sample as a function of perimeter-to-area ratio. The intercept indicates the bulk generation rate $G_B$ while the slope indicates the perimeter generation rate $G_P$. These generation mechanisms are obscured in the E-beam samples by the much larger generation $G_M$ in the E-beam damaged regions.

evaporated sample can be explained by considering the relative contributions of the various generation mechanisms: $G_M$, $G_B$, and $G_P$. As described previously, the recovery process in the control sample consists of components due to bulk and perimeter generation. By combining (3), (4), and (8) and setting $G_M = G_B$ (there are no E-beam damaged regions in the control sample), we can write

$$\frac{1}{\tau_s}=\frac{1}{\tau_{sB}}+\frac{1}{\tau_{sP}}. \qquad (9)$$

Figure 4 shows a plot of $1/(\tau_s T^2)$, $1/(\tau_{sB}T^2)$, and $1/(\tau_{sP}T^2)$ versus temperature. From the slopes of $1/(\tau_{sB}T^2)$ and $1/(\tau_{sP}T^2)$ the activation energies for bulk and perimeter generation can be determined using (5) and (6). For the control devices, $E_{AB} = 0.68$ eV while $E_{AP} = 1.1$ eV. The dashed line in Fig. 4 is a plot of $1/\tau_s$ obtained by adding $1/\tau_{sB}$ and $1/\tau_{sP}$ according to (9). The activation energy for this line is approximately 0.91 eV.

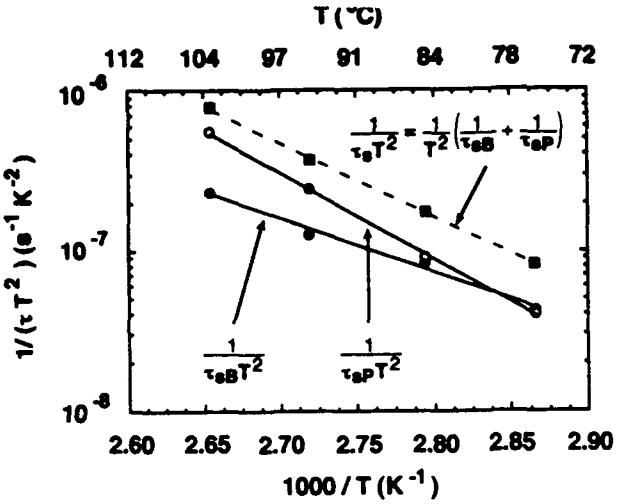


FIG. 4. Inverse recovery time constant of thermally-evaporated control sample as a function of temperature. Generation due to the bulk and perimeter are indicated with solid lines, whereas the sum is indicated with a dashed line. From the slopes, $E_{AB} = 0.68$ eV, $E_{AP} = 1.1$ eV, and $E_A = 0.91$ eV.

Thus, the measured activation energy of the control sample can be viewed as a weighted average of the activation energies for bulk and perimeter generation.

## ACTIVATION ENERGY OF THE E-BEAM METALLIZED SAMPLES

The activation energy of 0.63 eV observed in the E-beam evaporated samples, however, is entirely due to generation in the bulk depletion region under the metal contact ($G_M$). In this case, it is reasonable to assume that the activation energy might be used to identify a specific deep-level trap. Two groups have characterized E-beam induced defects using deep-level transient spectroscopy (DLTS).[9,10] Following E-beam irradiation, both groups identified two dominant deep levels: a trap identified as EL2 which was present in the as-grown metalorganic chemical vapor deposition (MOCVD) and metalorganic vapor phase epitaxy (MOVPE) material and an electron trap at $E_C - 0.57$ eV which was introduced during the E-beam metallization. The EL2 was present with a concentration of $10^{14}$ $cm^{-3}$ which did not change with exposure to the E-beam environment. The trap at $E_C - 0.57$ eV was not detected in the as-grown film. After E-beam metallization, however, the density of this trap was about $10^{16}$ $cm^{-3}$ near the surface and decreased almost exponentially with distance into the material. The concentration dropped below the DLTS detection limit at 130 nm from the surface.

In general, it is assumed that the activation energy of a generation process should correspond to the largest energy transition an electron must make in order to move from the valence band to the conduction band. Thus, the activation energy for generation through a trap at $E_C - 0.57$ eV in GaAs would appear to be 0.85 eV. Under specific conditions, however, it can be shown that the lower activation energy can actually dominate the process. An equation which more accurately describes the generation process in a depletion region is derived beginning with (3), and substituting for the generation lifetime $\tau_g$[8]

$$\tau_{sB} = \frac{N_B}{n_i}\left[\tau_p \exp\left(\frac{E_T - E_i}{k_B T}\right) + \tau_n \exp\left(-\frac{E_T - E_i}{k_B T}\right)\right], \tag{10}$$

where $E_T$ is the trap level, $E_i$ is the intrinsic Fermi level, and $\tau_p$ and $\tau_n$ are the hole and electron lifetimes. Simplifying further, using

$$n_i = \sqrt{N_C N_V}\exp\left(\frac{-E_G}{2k_B T}\right), \tag{11}$$

(10) becomes

$$\tau_{sB} = \frac{N_B}{\sqrt{N_C N_V}}\left[\tau_p \exp\left(\frac{E_T - E_V}{k_B T}\right) + \tau_n \exp\left(\frac{E_C - E_T}{k_B T}\right)\right], \tag{12}$$

where $N_C$ and $N_V$ are the conduction band and valence band effective density of states. Finally, by substituting the expressions for $\tau_n$ and $\tau_p$[8]

$$\tau_{sB} = \frac{N_B}{\sqrt{N_C N_V}\nu_{th} N_T}\left[\frac{1}{\sigma_p}\exp\left(\frac{E_T - E_V}{k_B T}\right) + \frac{1}{\sigma_n}\exp\left(\frac{E_C - E_T}{k_B T}\right)\right], \tag{13}$$

where $\nu_{th}$ is the thermal velocity, $N_T$ is the trap density, and $\sigma_p$ and $\sigma_n$ are the hole and electron capture cross sections. Equation (13) can be rewritten to include the $T^2$ temperature-dependent prefactor which appears in (5)

$$\tau_{sB} = \frac{C_4}{T^2}\left[\frac{1}{\sigma_p}\exp\left(\frac{E_T - E_V}{k_B T}\right) + \frac{1}{\sigma_n}\exp\left(\frac{E_C - E_T}{k_B T}\right)\right], \tag{14}$$

where $C_4$ is a proportionality constant.

If it is assumed that the E-beam induced trap at $E_C - 0.57$ eV reported in Refs. 9 and 10 is responsible for the bulk generation in these samples, then $E_C - E_T = 0.57$ eV. This requires that $E_T - E_V = 0.85$ eV. Since electron emission to the conduction band would require less thermal energy than hole emission to the valence band, one would expect hole-electron pair generation to be limited by hole emission, yielding an activation energy of 0.85 eV. However, if the electron capture cross section is smaller than the hole capture cross section, then electron emission could become the rate-limiting process, and the smaller activation energy would be observed.

The generation activation energy of 0.63 eV measured on our samples is close to that reported in Refs. 9 and 10. As discussed, our generation data would be consistent with the DLTS data under the assumption of asymmetrical capture cross sections. We hasten to point out, however, that based on our data alone, we cannot unambiguously identify a specific trap position within the band gap, and cannot say whether the trap is in the upper or lower half of the band

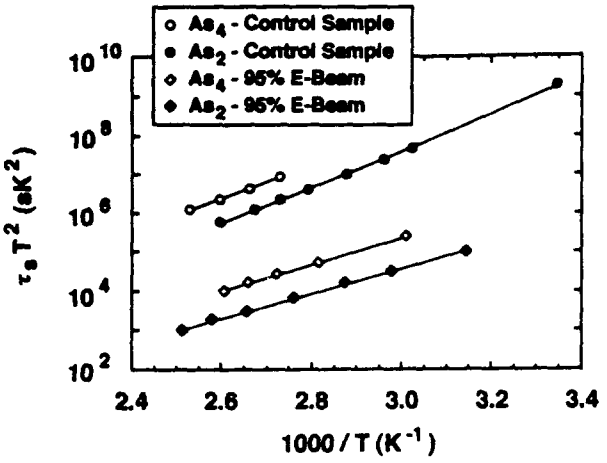


FIG. 5. Recovery time constant as a function of temperature for 100 $\times 100\ \mu m^2$ devices fabricated on films grown using the $As_2$ and the $As_4$ species of arsenic flux.

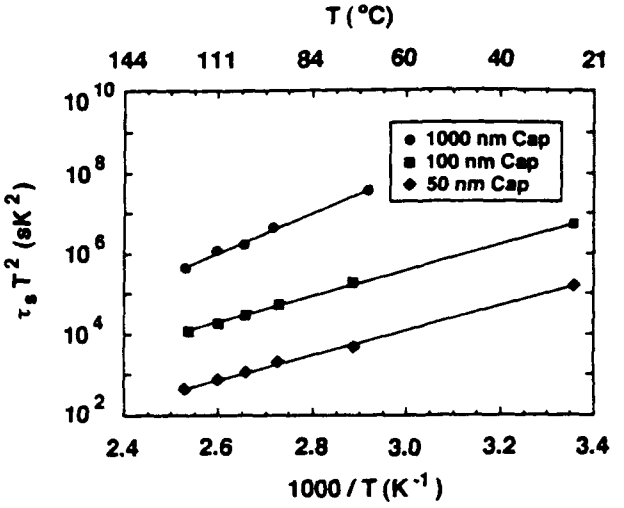


FIG. 6. Recovery time constants of E-beam damaged samples as a function of cap layer thickness. All samples were grown with $As_4$ flux. The sample with a 1000 nm cap layer has a recovery time within a factor of two of the control sample, indicating that the penetration depth of the damaging species is much less than 1000 nm.

gap. As a result, the association of our generation process with the trap identified in Refs. 9 and 10 must be regarded as tentative.

## EFFECT OF GROWTH CONDITIONS ON GENERATION RATE

As indicated in Fig. 5, the generation rate also depends on the growth conditions during MBE. In this figure, the recovery time constant is plotted as a function of temperature for samples grown using the $As_2$ and the $As_4$ species of arsenic flux. The $As_4$-grown sample demonstrates the properties described previously for the $As_2$-grown sample. In particular, there is more than a three order of magnitude increase in the generation rate following E-beam metallization, and the activation energy of the generation process changes from 0.92 eV to approximately 0.63 eV. There is, however, a larger recovery time constant associated with both the $As_4$-grown control sample and the $As_4$-grown sample metallized using E-beam evaporation.

Since the activation energy of the $As_2$- and $As_4$-grown samples are the same after E-beam metallization, it is likely that the generation mechanism is the same in both samples. During MBE, the $As_2$ and $As_4$ fluxes are produced from different effusion cells, so it is possible that different types and/or densities of impurities might be present in the films. Even if no impurities are present, the difference in arsenic incorporation mechanisms[11,12] could possibly lead to a difference in the density of defects in the film. Whatever the source, we postulate that nonelectrically active defects are present in the as-grown film and the density and nature of these defects depend upon the MBE conditions. Upon exposure in the E-beam system, however, some of these defects change configuration and become efficient generation sites.

## DEPTH DEPENDENCE AND DAMAGE MECHANISM

Since leakage in the E-beam irradiated samples is due to generation in the bulk space-charge region of the *p-i-n* junctions, the depth dependence of the mechanism causing the increased generation rate can be determined by varying the distance of the *p-i-n* junctions from the top surface of the structure shown in Fig. 1. Two additional films having $p^+$-cap layers of 50 and 1000 nm were grown using the $As_4$ arsenic species. In these two films, the thickness of the *n* region between the two *p-i-n* junctions was not changed. Both samples were processed in a manner identical to that described previously. Figure 6 shows a plot of the recovery time constant versus temperature for the samples with 50, 100, and 1000 nm cap layers. The recovery time constant of the sample with the 1000 nm cap-layer thickness is essentially equal to that of the thermally evaporated sample. (The time constants of the 1000 nm cap-layer thermally evaporated samples are approximately a factor of two lower than the 100 nm cap-layer thermally evaporated samples. This is attributed to an increase in the perimeter generation due to a deeper mesa-isolation etch profile.) In contrast, the recovery time constant of the 100 nm cap-layer sample is approximately two orders of magnitude lower, and the 50 nm cap-layer sample is approximately three orders of magnitude lower than that of the control sample.

A plot of the inverse recovery time constant at 95 °C as a function of cap-layer thickness is shown in Fig. 7. In addition, the data of the depth dependent $E_C - 0.57$ eV electron trap measured by Kleinhenz *et al.* is also included.[9] Extrapolating from the 50 and 100 nm cap-layer data (assuming the damage decreases nearly exponentially with depth), the damage which causes increased generation appears to be limited to the first 200 nm of semiconductor material, at which point the recovery time constant becomes equal to that measured for the thermally evaporated samples. This is consistent with the depth dependence of the $E_C - 0.57$ eV trap observed in the MOCVD samples.

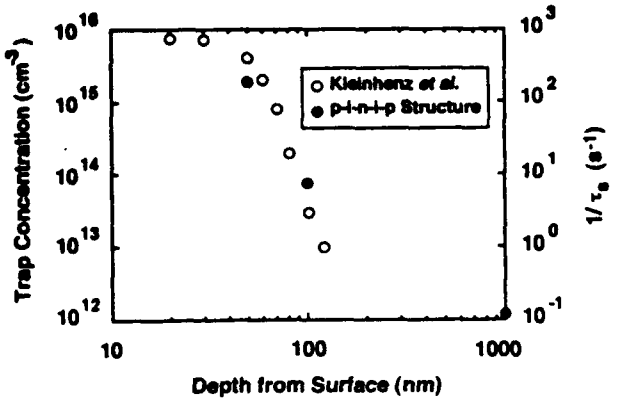


FIG. 7. The data of the depth dependent $E_C - 0.57$ eV electron trap measured by Kleinhenz *et al.* are shown using the left vertical axis, while the inverse recovery time constant at 95 °C as a function of cap-layer thickness are shown using the right vertical axis. The depth dependence of the mechanism causing the increased generation rate is consistent with that of the $E_C - 0.57$ eV trap observed using DLTS in the MOCVD samples.

In addition to information related to the trap energy level and its effect on generation rate, the mechanism causing the introduction of these defects during E-beam exposure is also of interest. Possible mechanisms include x-rays, energetic electrons, and ions. In order to demonstrate that the damage species is indeed energetic electrons as reported in Refs. 9 and 10 and not x-rays or ions, the relative penetration depths of these species in GaAs can be estimated and compared to the experimental data described previously. The calculated range for 9 keV electrons in GaAs using the expression given in Ref. 13 is approximately 300 nm. For x-rays, the intensity decreases exponentially with depth into the GaAs.[14] Assuming a gold target bombarded with 9 keV electrons, the point at which the intensity of the resulting 3 keV emitted x-ray has fallen to 1/e of its initial value is around 1.7 $\mu$m. Finally, the penetration depth of Au ions as determined from standard tables is less than 10 nm.[15] As a result of these calculations, it seems reasonable that any damage due to x rays present in the system would extend much deeper than the 200 nm region within which damage is occurring in these samples. Likewise, the damage occurring from Au ions would be limited to the near surface region of the GaAs $p^+$-cap layer, and would not penetrate to the *p-n* junction. Thus, it can be concluded that the damage in the E-beam metallized samples is due primarily to energetic electrons.

## CONCLUSIONS

In summary, more than a three order of magnitude increase in the thermal generation rate of E-beam metallized GaAs *p-n* junctions has been observed compared to samples metallized in a thermal evaporator. The increase in generation rate depends on the device area exposed during evaporation, the type of metal initially evaporated onto the sample, the growth conditions during MBE, and the depth of the *p-n* junction from the semiconductor surface. The generation activation energies of all the samples exposed to the E-beam environment are approximately 0.63 eV. Additionally, the depth dependence of the induced defect causing the increased generation is similar to that reported for an $E_C - 0.57$ eV level introduced into MOCVD films by E-beam exposure. Finally, from studies of the depth dependence, it can be concluded that the primary damage mechanism is high-energy electrons.

## ACKNOWLEDGMENTS

This work was supported by SDIO/IST under Grant N00014-88-K-0527 and by ONR under Grant N00014-89-J-1864. T.B.S. acknowledges fellowship support from Eastman Kodak. This work benefited from technical discussions with R. F. Pierret and S. M. Durbin.

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# High resolution x-ray diffraction analysis of annealed low-temperature gallium arsenide

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High resolution x-ray diffraction methods have been used to characterize GaAs grown at low substrate temperatures by molecular beam epitaxy and to examine the effects of post-growth annealing on the structure of the layers. Double crystal rocking curves from the as-deposited epitaxial layer show well-defined interference fringes, indicating a high level of structural perfection despite the presence of excess arsenic. Annealing at temperatures from 700 to 900 °C resulted in a decrease in the perpendicular lattice mismatch between the GaAs grown at low temperature and the substrate from 0.133% to 0.016% and a decrease (but not total elimination) of the visibility of the interference fringes. Triple-crystal diffraction scans around the 004 point in reciprocal space exhibited an increase in the apparent mosaic spread of the epitaxial layer with increasing anneal temperature. The observations are explained in terms of the growth of arsenic precipitates in the epitaxial layer.

Gallium arsenide epitaxial layers grown at low substrate temperatures (LT-GaAs) have recently attracted considerable attention due to their interesting and potentially useful electrical properties. Following growth by molecular beam epitaxy (MBE) at temperatures in the vicinity of 200 °C, LT-GaAs films that are annealed at elevated temperatures exhibit extremely high resistivities and breakdown strengths.[1] Despite the fact that this material is grown at temperatures that are much lower than those typically employed in MBE, numerous studies have indicated that the crystalline quality of LT-GaAs is surprisingly high.[2–7]

X-ray diffraction is an obvious method for characterizing LT-GaAs and for observing the effects of post-growth annealing on the structure and perfection of this material. X-ray rocking curves of as-grown LT-GaAs typically exhibit a lattice parameter that is larger than that of bulk GaAs, whereas samples annealed at 600 °C were reported to revert to the bulk lattice constant of GaAs.[2,5] Wie and co-workers have reported that the lattice parameter of LT-GaAs changes abruptly at an anneal temperature of around 350 °C, where the perpendicular lattice mismatch decreases significantly.[8,9] They also reported that samples subjected to either furnace annealing or rapid thermal annealing show a transition from a lattice expansion to a lattice contraction at higher temperatures. We have conducted a high resolution x-ray diffraction analysis of LT-GaAs grown by MBE to better understand the structure of the as-grown material and to clarify the effects of post-growth processing on this material.

The films used in this work were grown in a Varian GEN II MBE system on two-in.-diam undoped ⟨001⟩ GaAs substrates. The nominally undoped layers were grown at 1 μm/h using an $As_4$/Ga beam equivalent pressure ratio of 20. The growth sequence consisted of first depositing a 0.5 μm GaAs layer using a substrate temperature of 600 °C. The substrate temperature was then lowered to 225 °C while growth of GaAs continued. This temperature decrease took 15 min, resulting in a 0.25 μm temperature transition region. After attaining the target substrate temperature of 225 °C, a GaAs layer with a nominal thickness of 1 μm was grown. The wafer was then removed from the MBE system and cleaved into samples that were annealed in a computer-controlled AG Associates mini-pulse rapid thermal processor. The anneals were done using a proximity cap for a duration of 30 s; samples were annealed at 700, 800, and 900 °C. These anneals result in the formation of As precipitates due to the excess As that was incorporated in the GaAs layer. Using transmission electron microscopy, it has been observed that the average diameter of the precipitates increases and their density decreases as the anneal temperature is increased.[7] For 30 s anneals, typical average precipitate diameters and densities are 70 Å and $1\times10^{17}$ $cm^{-3}$ (700 °C anneal), 150 Å and $1\times10^{16}$ $cm^{-3}$ (800 °C anneal), and 200 Å and $3\times10^{15}$ $cm^{-3}$ (900 °C anneal).

High resolution x-ray diffraction analyses were performed using a Bede 150 double-crystal diffractometer. Instead of the conventional single reflection monochromator, a pair of grooved silicon crystals was used in which the incident x-ray beam executed four (220) reflections in the $(-,+,+,-)$ geometry.[10] Copper $K\alpha_1$ radiation was obtained from a Rigaku RU200 rotating anode generator. A relatively large beam size on the sample (6 $mm^2$) was used. Analogues to conventional double-crystal rocking curves were obtained with the sample situated on the first axis of the diffractometer (i.e., in the location usually used for the monochromator in the double-crystal geometry), and the x rays diffracted by the sample were recorded with a wide-open scintillation counter. Alternatively, the intensity diffracted by the samples was also examined by placing a triple bounce (220) grooved silicon crystal on the second

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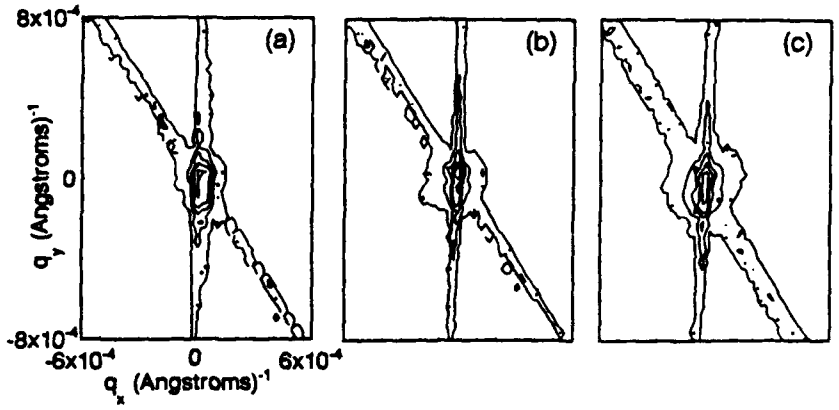


FIG. 3. Triple-crystal scans from annealed LT-GaAs (identical ranges of $q_x$ and $q_y$ in all scans). (a) 700, (b) 800, (c) 900 °C.

the main Bragg peak. The angular deviations of the sample and analyzer crystals from the (004) reflection were converted into the orthogonal reciprocal space coordinates $q_x$, $q_y$ using the relationships given by Iida and Kohra.[13]

The intensities in the figures are recorded on a logarithmic scale as a function of position in reciprocal space; the equal intensity contours are given in increments of 0.8 units of the logarithm of the measured intensity. Visible in the figure are the so-called surface streaks in the $q_y$ direction which arise from the truncation of the crystal lattice at the sample surface.[14] Residual scattering from the analyzer crystal is also apparent as an inclined streak in the intensity contour plots. Close examination of the surface streak confirmed the presence of interference fringes in the annealed samples. More important is the angular extent of the diffuse intensity in the $q_x$ direction; the triple-crystal scans show that the extent of this scattering increases with increasing anneal temperature. The apparent width of the residual scattering from the analyzer crystal also increases, presumably due to the greater angular extent of the diffuse scattering from the LT-GaAs layer.

Studies of oxygen precipitation in silicon have demonstrated that similar growth phenomena result in long-range distortions in the vicinity of precipitates.[15] We believe that the increase in the extent of the x-ray scattering in the $q_x$ direction is due to strain fields that arise from the arsenic precipitates. These strain fields would locally increase the angular range over which Bragg diffraction could occur, thus increasing the angular extent of diffracted intensity observed in the $q_x$ direction.[10] In other words, the apparent mosaic spread of the epitaxial layer increases with an increase in anneal time and average size of the arsenic precipitates. Dynamical diffraction effects would also be disrupted by the presence of precipitate strain fields; hence the reduction in the visibility of the interference fringes that was noted in the annealed samples would occur naturally during precipitate growth. Although the visibility of the interference fringes in the double-crystal scans does not vary as strongly with anneal temperature as does the intensity distribution in the $q_x$ direction, this difference may be due to the enhanced strain sensitivity of the triple-crystal configuration.

In conclusion, the structural properties of as-grown and annealed GaAs grown at low temperature by MBE has been examined by high resolution x-ray diffraction techniques. We have found that the crystallographic quality of the material examined in this study is extremely high, as evidenced by the presence of well-defined interference fringes in the as-grown material. Triple-crystal x-ray diffraction reveals an increase in the apparent mosaic spread of the LT-GaAs with increasing anneal temperature. We attribute this observation to the presence of strain fields that are associated with the thermally-induced arsenic precipitates.

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# Characterization of a GaAs/AlGaAs Modulation-Doped Dynamic Random Access Memory Cell

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## ABSTRACT

We report the electrical properties of a GaAs dynamic random access memory (DRAM) cell in which the storage capacitor is a modulation-doped heterojunction and the access transistor is a modulation-doped field-effect transistor (MODFET). Experimental waveforms illustrating both reading and writing are exhibited. Isolated storage capacitors have 1/e storage times as long as 4.3 hours at room temperature. The complete DRAM cell exhibits a room temperature storage time of about 3 minutes, limited by gate leakage in the access transistor.

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In recent years, several groups have investigated GaAs heterojunction structures for use in dynamic memory applications. The earliest work involved charge storage at the interface between GaAs and undoped AlGaAs [1-4]. In this type of capacitor, the storage time is "leakage limited": An excess electron concentration stored at the heterojunction leaks away over time as the device returns to its equilibrium state. Since the electrons are confined by the relatively small conduction band offset at the heterojunction, charge retention in this structure is too short for DRAM operation at room temperature [4]. Other investigators have studied a leakage-limited memory device which stores electrons in a GaAs/AlGaAs quantum well [5,6]. Storage times of 1-2 sec were reported at room temperature. However, it is not possible to quickly erase the charge stored in this structure.

It has been recognized for some time that a modulation-doped structure would make an ideal storage capacitor [7]. Unlike undoped layers, a donor-doped AlGaAs layer bends the semiconductor bands sufficiently that a two-dimensional electron gas (2DEG) is present at the GaAs/AlGaAs interface in equilibrium. To store information, electrons are removed from the cell, and the cell gradually returns to equilibrium by thermal generation. This type of cell is termed "generation-limited". Cells of this type were recently reported by Chen et al. [8], and exhibited a storage time of about 5.4 sec at room temperature.

In this letter, we report modulation-doped storage capacitors having storage times in excess of four hours at room temperature and MODFET DRAM cells with storage times of three minutes at room temperature. A schematic diagram of the DRAM cell is shown in Fig. 1. The cell consists of a modulation-doped storage capacitor and a MODFET access transistor. The gate of the storage capacitor is biased at the substrate potential. The inversion charge at the GaAs/AlGaAs interface (or 2DEG), present in equilibrium, serves as one plate of the storage capacitor. A "one" is written to the storage capacitor by removing the 2DEG through the access transistor. During the storage period, the capacitor is isolated from the bit line by biasing the transistor to the off state. In a production DRAM, the substrate would be semi-insulating; we have used a $p^+$ substrate to facilitate monitoring the operation by observing the capacitance of the storage gate.

The epitaxial layers in Fig. 1 are grown in a Varian GEN-II MBE machine. The AlGaAs barrier consists of a 36 nm doped layer ($1.3 \times 10^{18}$ $cm^{-3}$ silicon) surrounded by undoped spacer layers. All AlGaAs layers have an AlAs mole fraction of 30%. The resulting 2DEG density is $1.5 \times 10^{12}$ electrons/$cm^2$. An undepleted $p^+$ GaAs cap layer is used as the gate for both the access transistor and the storage capacitor in order to reduce leakage currents from the gate [9]. The ohmic contact to the 2DEG consists of thermally evaporated and alloyed Au and Ge. Contact to the $p^+$ cap layer is made with thermally evaporated Au. Electron-beam evaporation is explicitly avoided, since this has been shown to increase the thermal generation rate in GaAs pn junctions [10]. The storage gate, transistor gate, and bit line are isolated from each other by removing the intervening $p^+$ cap with an electrically monitored etch. The entire cell is mesa isolated by wet etching

Figure 2 shows the drain current for a typical MODFET access transistor at a drain bias of 2.5 V. This transistor is depletion mode with a threshold voltage of -2.08 V. The subthreshold slope is 81.3 mV/decade, higher than the undoped limit of 60 mV/decade due

to the $p^-$ doping in the substrate. The drain current consists of three components: drain-to-source, drain-to-gate, and drain-to-substrate current. For gate biases more negative than -2.4 V, the drain current begins to increase due to drain-to-gate and drain-to-substrate leakage. The drain-to-substrate component arises because of the alloyed ohmic contact to the drain. Since the DRAM cell does not contain an ohmic contact adjacent to the storage capacitor, the alloy contact leakage is not present in the DRAM cell and the minimum current would be slightly lower than shown here.

In Fig. 3, both a "one" and a "zero" are written to a MODFET DRAM cell. For the purposes of this demonstration, the charge state of the storage capacitor is monitored by recording the capacitance between the storage gate and ground. When the 2DEG within the storage capacitor is removed, the substrate depletion layer expands and the capacitance decreases. In the figure, the arrows indicate the points where the access transistor is momentarily pulsed to the "on" state. At these points the storage capacitor quickly charges to the potential of the bit line, and an abrupt capacitance change is noted. When the transistor is off, transitions in the bit line potential do not affect the capacitor charge. However, the charge density in the capacitor gradually returns to its equilibrium value (rising capacitance) as a result of generation in the depletion region. For the present case, a gate bias of -2.9 V maximizes the storage time. We are able to write the DRAM cell with gate pulses as short as 20 nsec, limited only by our present measurement equipment. This demonstrates that the charge is mobile and not stored in traps.

Figure 4 shows the temperature dependence of the storage time for a DRAM cell and for an isolated capacitor. Capacitor storage times of up to 4.3 hours are observed at room temperature. The capacitor exhibits two different activation energies, indicating two competing generation processes are present. Both these activation energies are higher than half-bandgap, suggesting that generation is occurring through centers which are at some

distance from the middle of the bandgap. This DRAM cell has a storage time of 120 sec at room temperature and an activation energy intermediate between the two values observed in the capacitor. The dramatic reduction in storage time is due to gate leakage in the MODFET access transistor. Both these structures were metalized by thermal evaporation. As stated earlier, the storage time is seriously degraded if electron-beam evaporation is used for metal deposition. Identical storage capacitors metalized by electron-beam evaporation exhibited storage times of only about 15 minutes at room temperature. This is consistent with recent observations of Stellwag, et al. [10].

A demonstration of electrical read-out is shown in Fig. 5. Here the potential of the bit line is monitored by a high-impedance FET probe. Initially, the 2DEG is removed (or partially removed) by pulsing the storage gate to a negative bias for sufficient time for the electrons to recombine with substrate holes. Then the storage gate bias is returned to zero. When the access transistor is turned on 50 msec later (at $t = 0$), charge sharing occurs between the storage capacitor and the combined capacitance of the bit line and FET probe, resulting in a voltage output proportional to the storage capacitor potential. The decay of the output signal for $t > 0$ is due to the conductance of the FET probe and leakage in the bit line ohmic contact.

In summary, we have built and characterized modulation-doped storage capacitors with storage times in excess of four hours at room temperatur These storage capacitors have been combined with MODFET access transistors to produce DRAM cells with storage times up to three minutes at room temperature. A $p^+$ GaAs gate is used to reduce gate leakage in both the storage capacitors and the access transistors, and electron-beam evaporation of metal layers is avoided to reduce generation in the depletion regions.

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# Figure Captions

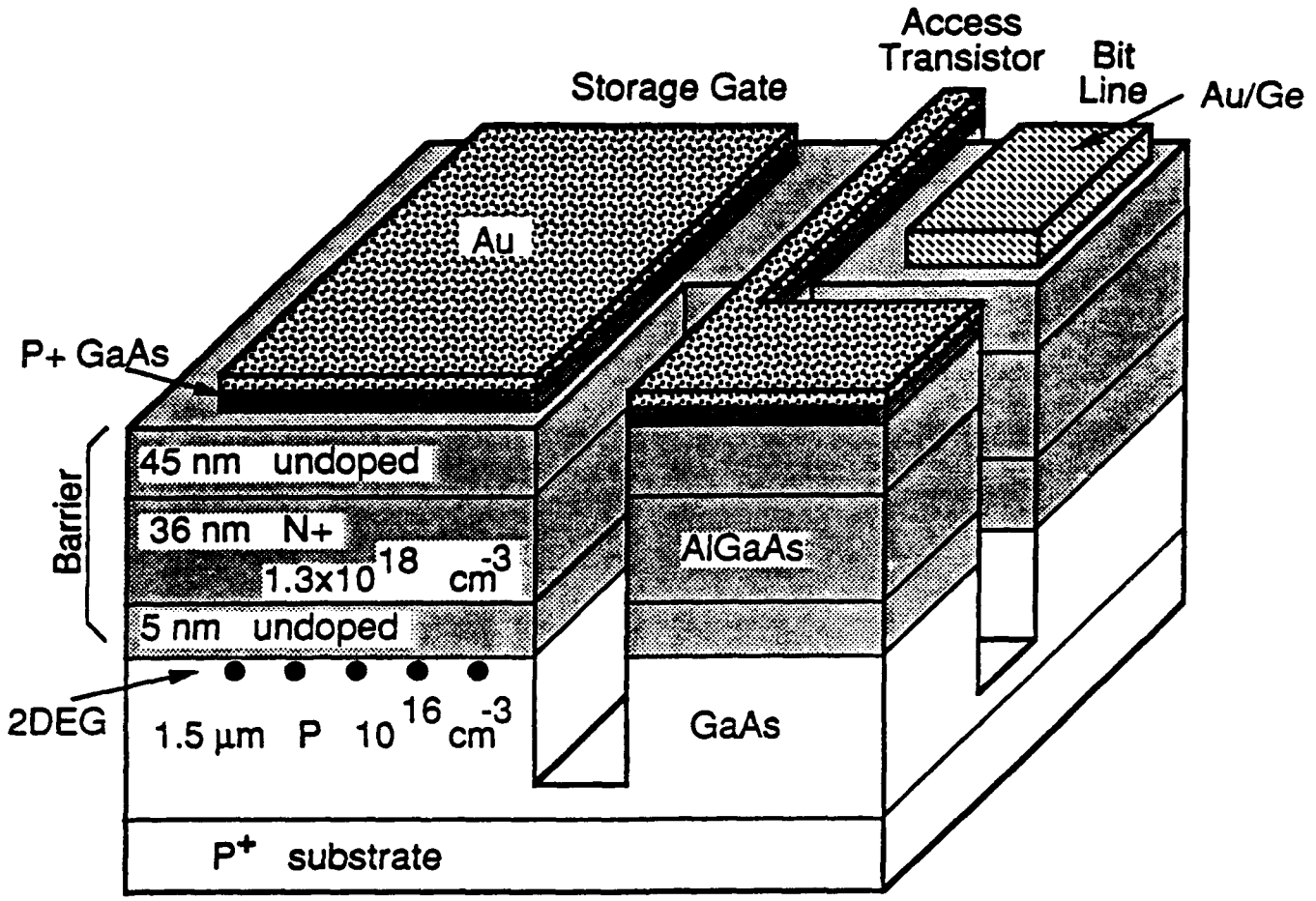
Figure 1. Structure of the MODFET DRAM cell. A $p^+$ GaAs gate is used for both the storage capacitor and the access transistor. The capacitor is 187 x 189.5 μm and the access transistor gate is 5.5 x 54 μm.

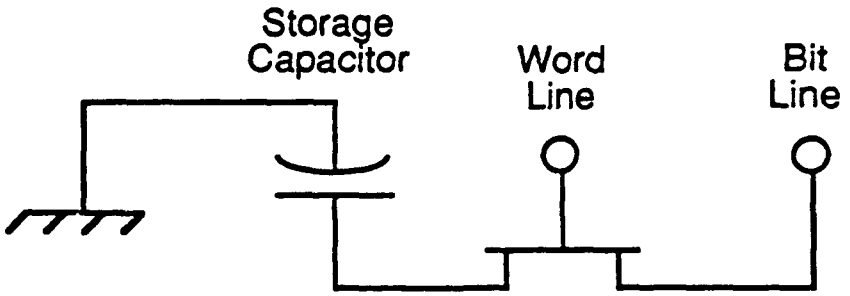
Figure 2 Drain current at room temperature in a typical MODFET at a drain bias of 2.5 V. The transistor has a gate length of 5 μm and a width of 26 μm. For gate voltages below -2.4 V, drain-to-gate and drain-to-substrate leakage dominate.

Figure 3. Demonstration of writing the DRAM cell. Write pulses are applied to the word line at the points indicated by arrows. Capacitance is proportional to the 2DEG charge in the storage capacitor. Note that the storage capacitor is unaffected by changes in bit line potential when the access transistor is off. The 1/e recovery time of this cell is approximately three minutes at room temperature.

Figure 4. Temperature dependence of the storage time in a DRAM cell and an isolated capacitor. A 1 sec, -1 V pulse is used to empty the isolated capacitor of its charge. The capacitor exhibits two activation energies, indicating two competing process are present.

Figure 5. Bit line waveforms during reading as a function of the write pulse voltage used to empty the storage capacitor. The access transistor is turned on at time t=0, which occurs 50 msec after a "one" is written to the cell. The storage capacitor contains a partial 2DEG even for the -1.5 V case, since the threshold voltage for removal of the 2DEG is -2.08 V.


Access Transistor
Bit Line
Au/Ge
Storage Gate
Au
P+ GaAs
Barrier
45 nm undoped
36 nm N+
1.3x10^18 cm^-3
5 nm undoped
AlGaAs
2DEG
1.5 µm P 10^16 cm^-3
GaAs
P+ substrate


Storage Capacitor
Word Line
Bit Line

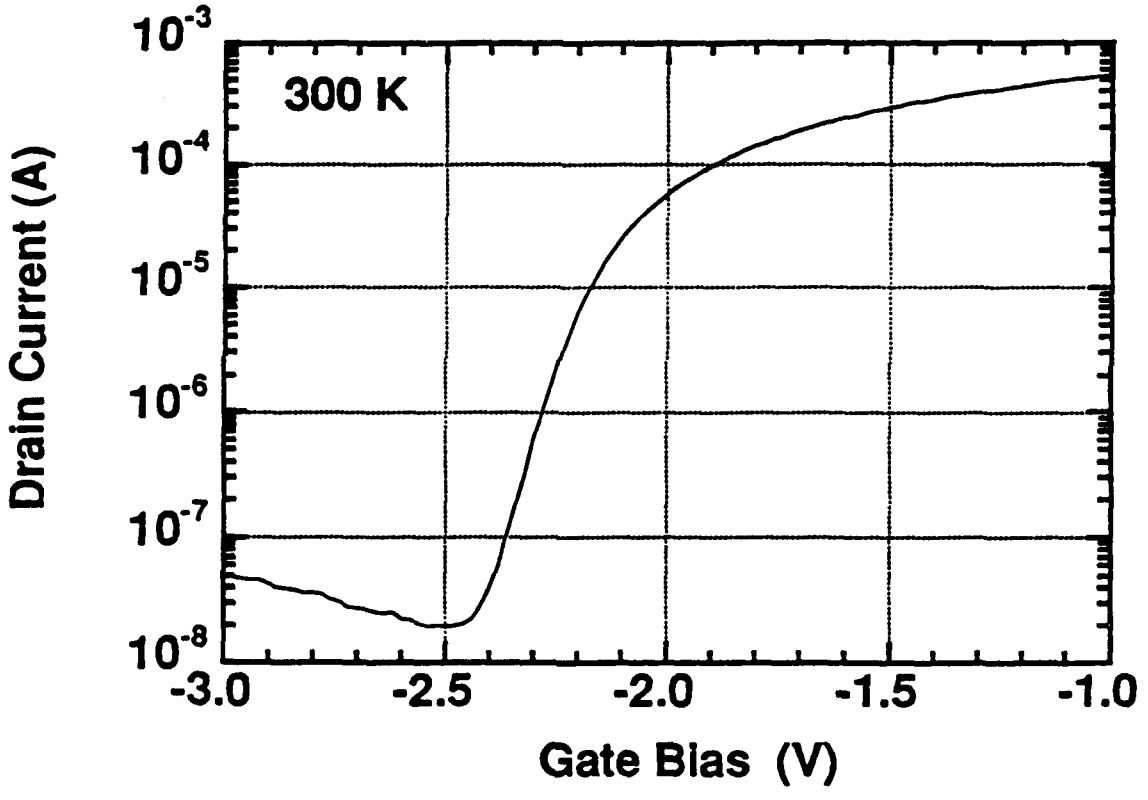
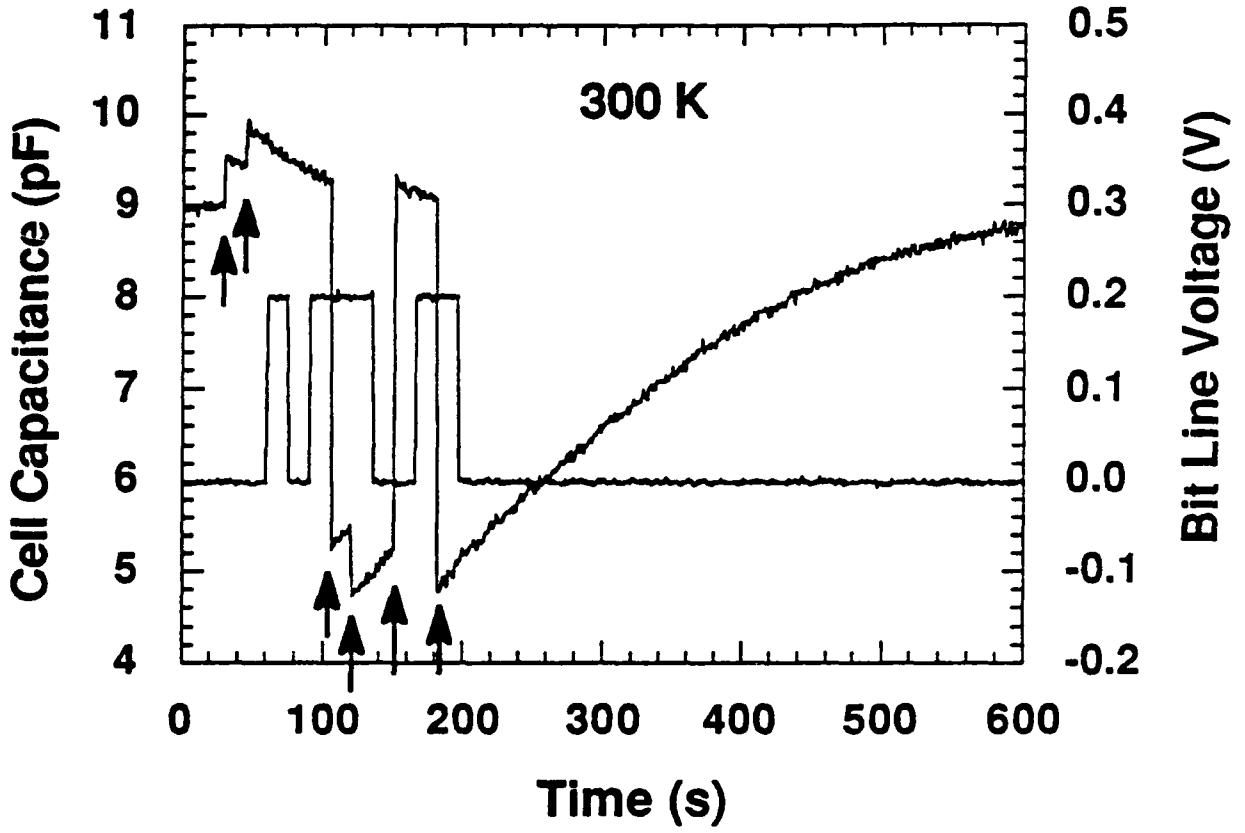
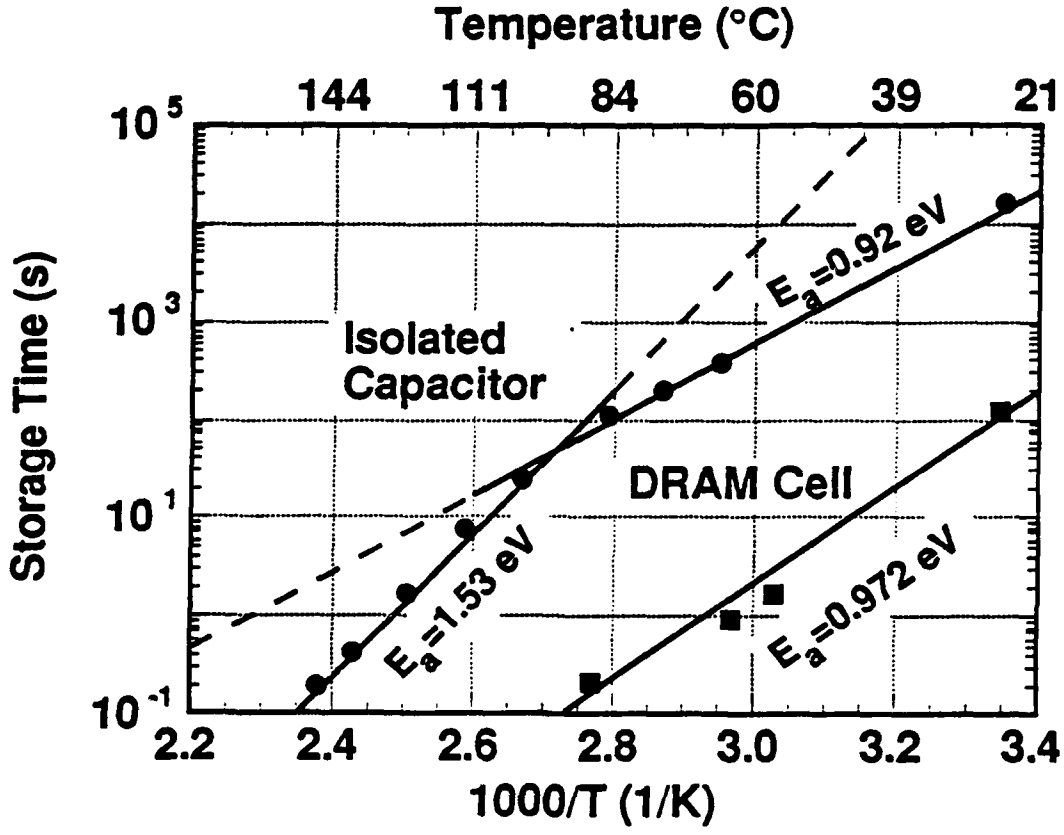

300 K
Drain Current (A)
10^-3
10^-4
10^-5
10^-6
10^-7
10^-8
-3.0
-2.5
-2.0
-1.5
-1.0
Gate Bias (V)

Fig. 2b


300 K
Cell Capacitance (pF)
Bit Line Voltage (V)
Time (s)
11
10
9
8
7
6
5
4
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
0
100
200
300
400
500
600

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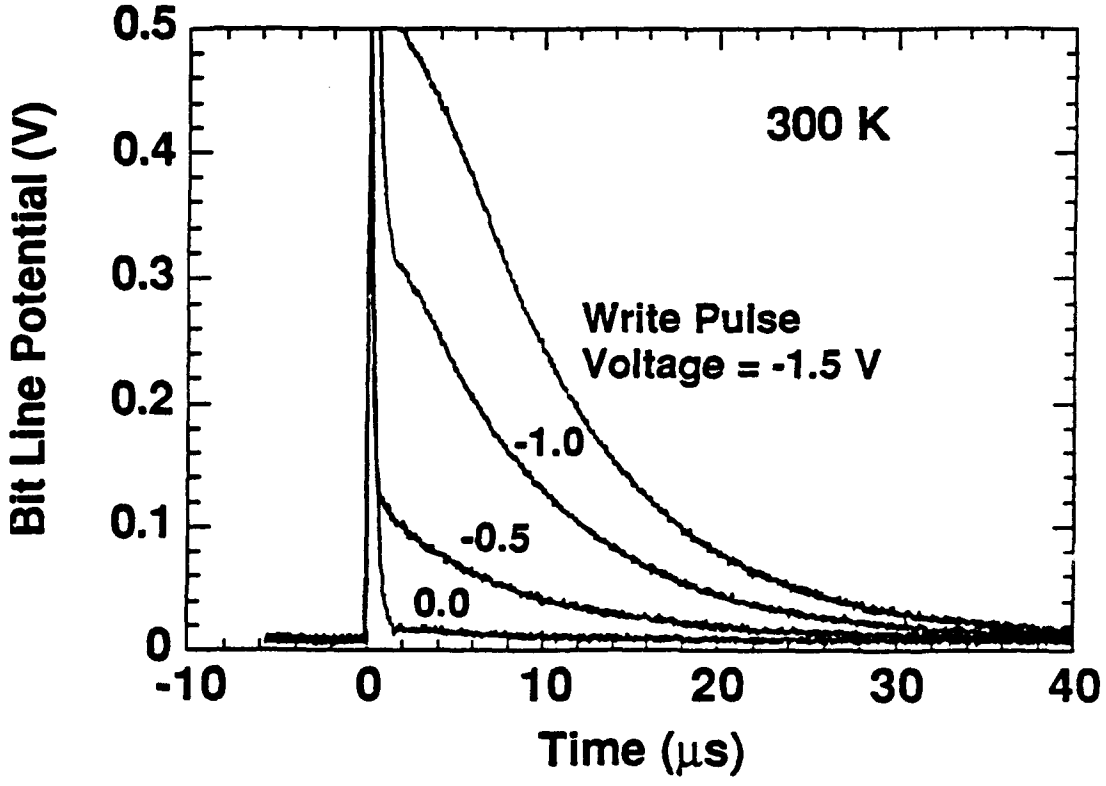
Bit Line Potential (V)
0.5
0.4
0.3
0.2
0.1
0
-10
0
10
20
30
40
Time (μs)
300 K
Write Pulse
Voltage = -1.5 V
-1.0
-0.5
0.0